

Compal confidential

EPW00 Schematics Document

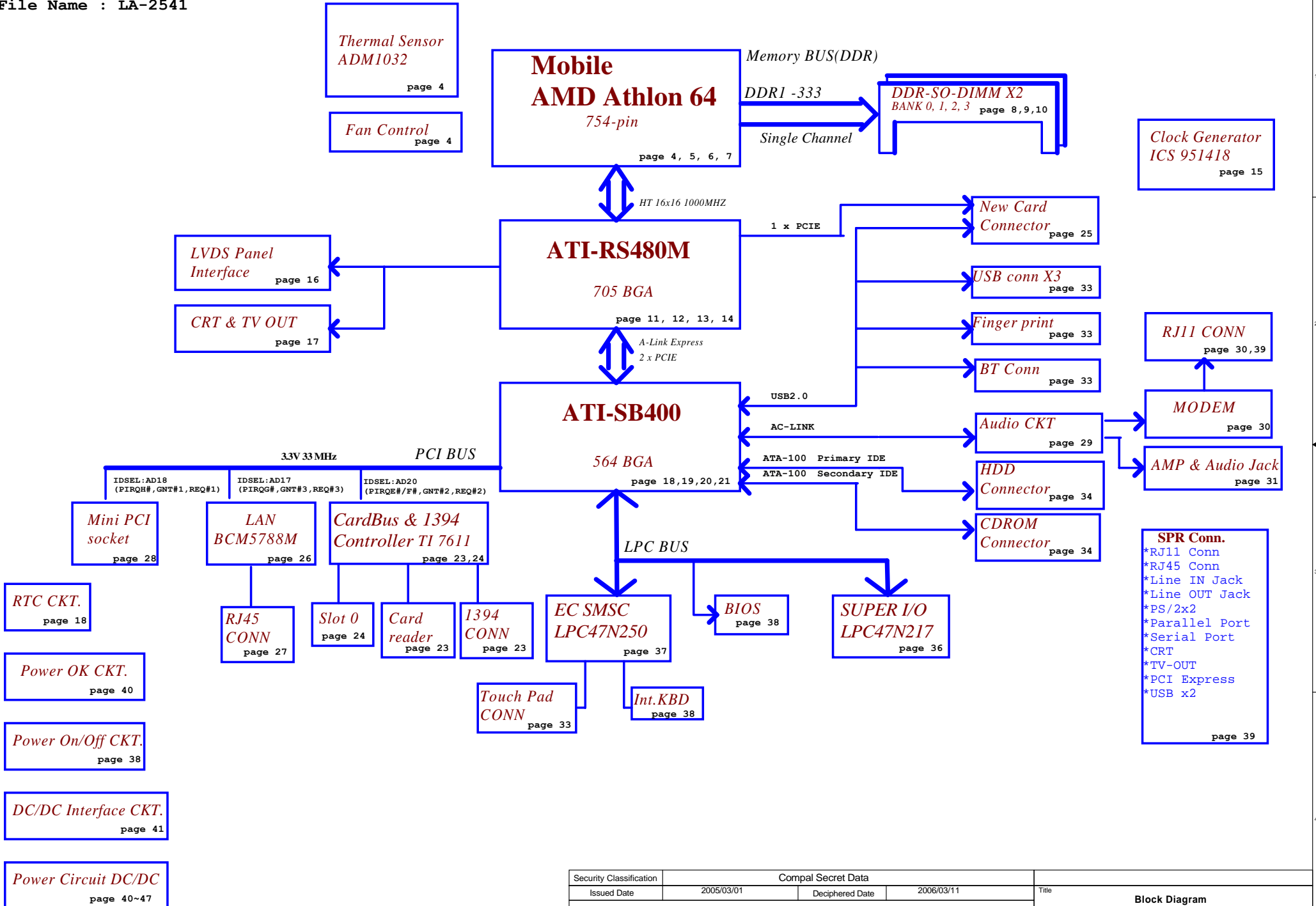
Mobile AMD Athlon 64 with ATI RS480M+ATI SB400

2005-04-15

REV:0.5



Security Classification	Compal Secret Data			Title		
Issued Date	2005/03/11	Deciphered Date	2006/03/11	Cover Sheet		
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Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	Block Diagram	
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				Rev	0.4

Voltage Rails

power plane State	+5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT +RS480_Core
S0	○	○	○
S1	○	○	○
S3	○	○	✗
S5 S4/AC	○	✗	✗
S5 S4/AC don't exist	Only +3VL ON	✗	✗

○ MEANS ON
✗ MEANS OFF

Symbol note:

↓ :means digital ground.

↓ :means analog ground.

@ :means reserved(un-mount).

4401@ :means populate for BCM4401 only.

5788@ :means populate for BCM5788M only.

7611@ :means populate for PCI7611 only.

4510@ :means populate for PCI4510 only.

PCI Devices

INTERNAL DEVICE	PIRQ
SMBUS	
IDE	A
LPC I/F	
PCI to PCI	
AC97 AUDIO	B
AC97 MODEM	B
OHCI#1 USB	D
OHCI#1 USB	D
EHCI USB	D
SATA#1	A
SATA#2	A

EXTERNAL	IDSEL #	REQ/GNT #	
CARD BUS & 1394	AD20	2	E, F
LAN	AD17	3	H
Mini-PCI	AD18	1	G

Jump	Normal operation	KBC Internal ROM flash	Comment
PJ1	Short Pad	Short Pad	+3VL
PJ3	Short Pad	Short Pad	+3VALW
PJ4	Short Pad	Short Pad	+1.8VALW
PJ5	Short Pad	Short Pad	+5VALW
PJ6	Short Pad	Short Pad	+1.5VS
PJ7	Short Pad	Short Pad	+2.5V
PJ8	Short Pad	Short Pad	+1.25V
PJ9	Short Pad	Short Pad	+1.2V_HT
PJ11	Short Pad	Short Pad	
PJ12	Short Pad	Short Pad	
PJ14	Short Pad	Short Pad	+RS480_Core
J1	Short Pad	No Short Pad	For ATE
J2	Short Pad	No Short Pad	For ATE
J3	No Short Pad	No Short Pad	
J4	No Short Pad	No Short Pad	Clear CMOS
J5	No Short Pad	Short Pad	For ATE
J6	No Short Pad	Short Pad	For ATE
J7	No Short Pad	Short Pad	For ATE
J8	Short Pad	No Short Pad	For ATE
J9	No Short Pad	Short Pad	For ATE

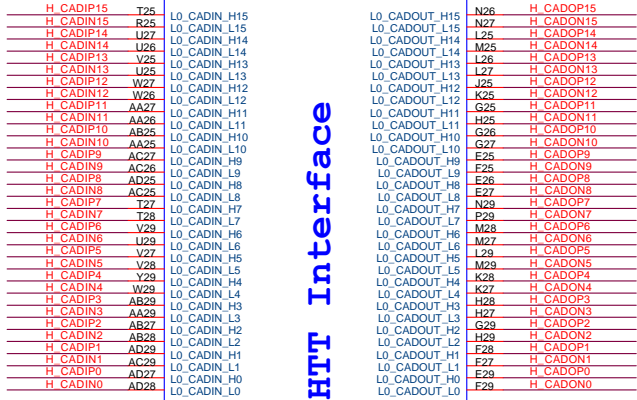
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Issued Date	2005/03/01	Deciphered Date	2006/03/11	Notes List		
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<11> H_CADIP[0..15] H_CADIP[0..15]
 <11> H_CADIN[0..15] H_CADIN[0..15]

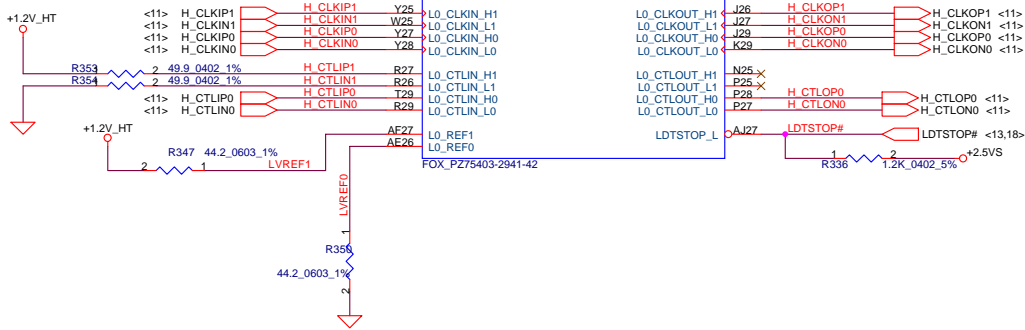
H_CADOP[0..15] H_CADOP[0..15] <11>
 H_CADON[0..15] H_CADON[0..15] <11>

U10A

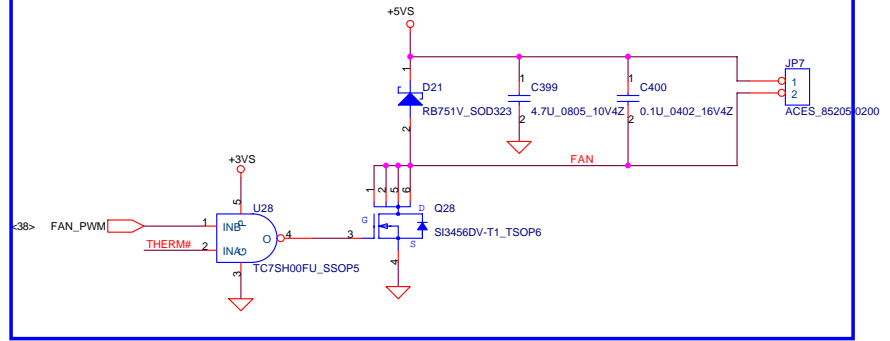
Claw Hammer-DTR



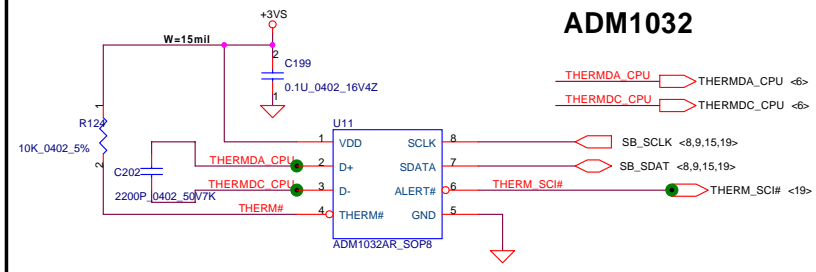
HTT Interface



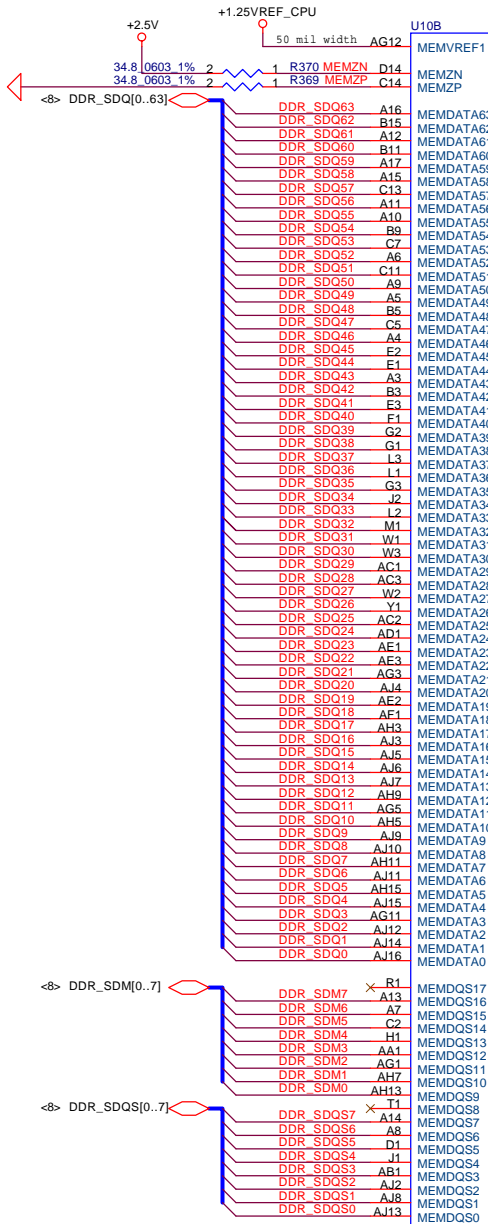
PWM Fan Control circuit



Thermal Sensor ADM1032



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Issued Date	2005/03/01	Deciphered Date	2006/03/11	Claw Hammer CPU (Host Bus)
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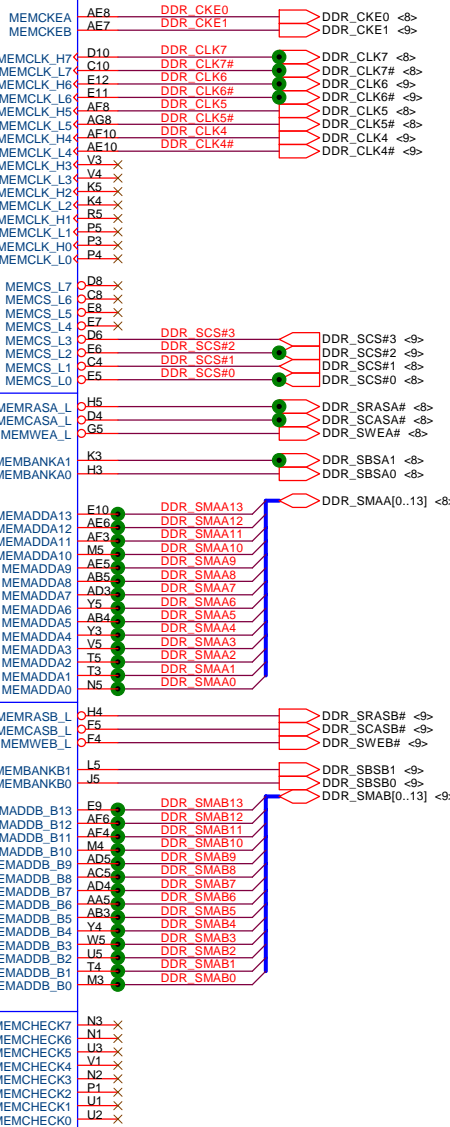


Claw Hammer-DTR

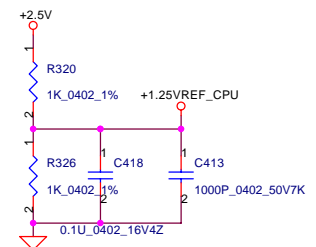
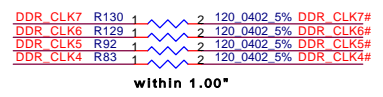
DDR Memory

A CHANGE ADDRESS

B CHANGE ADDRESS

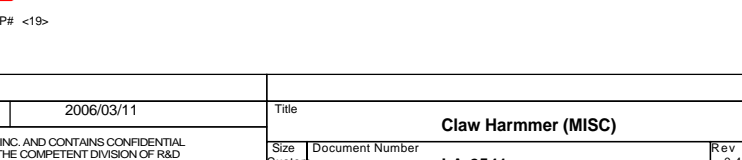
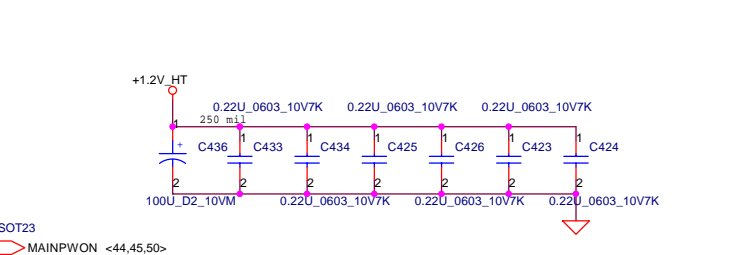
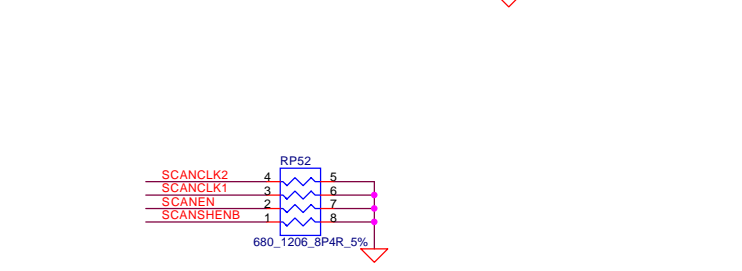
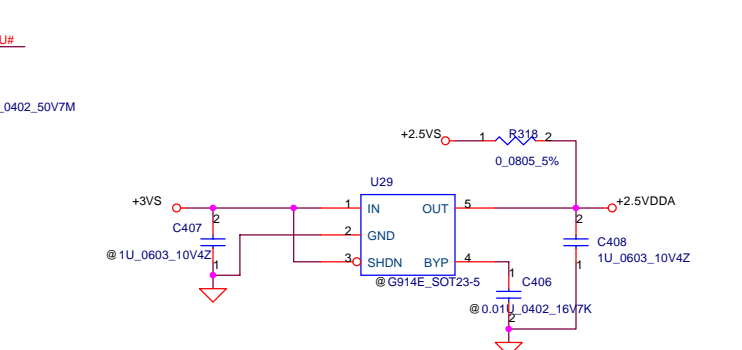
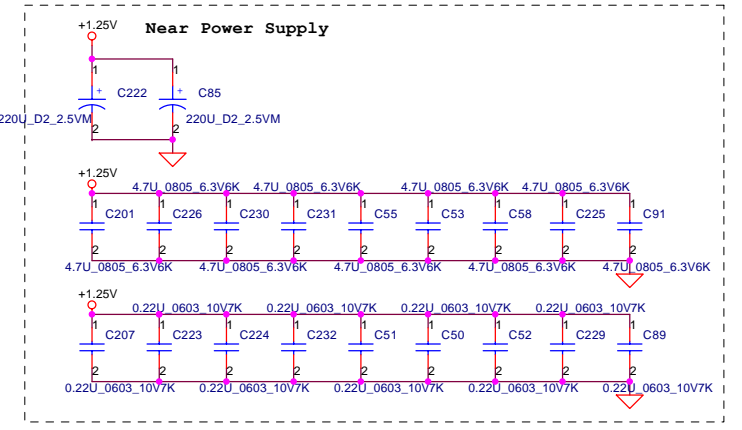
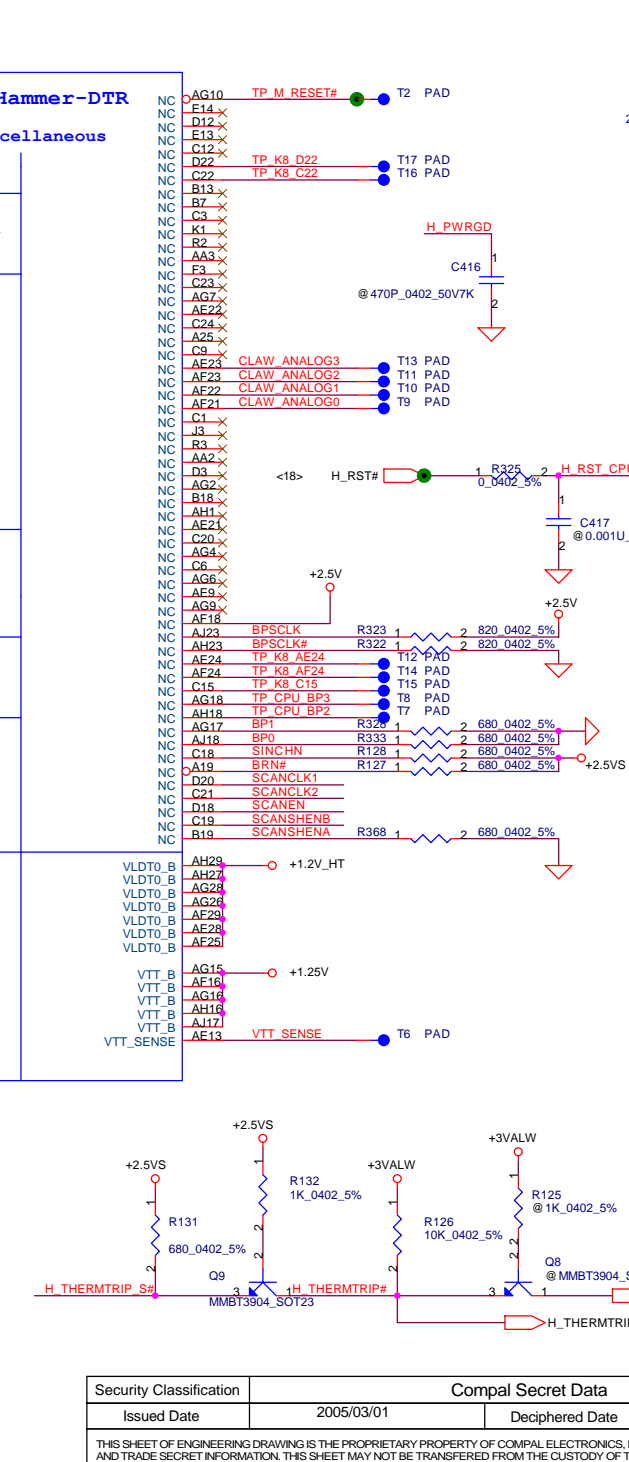
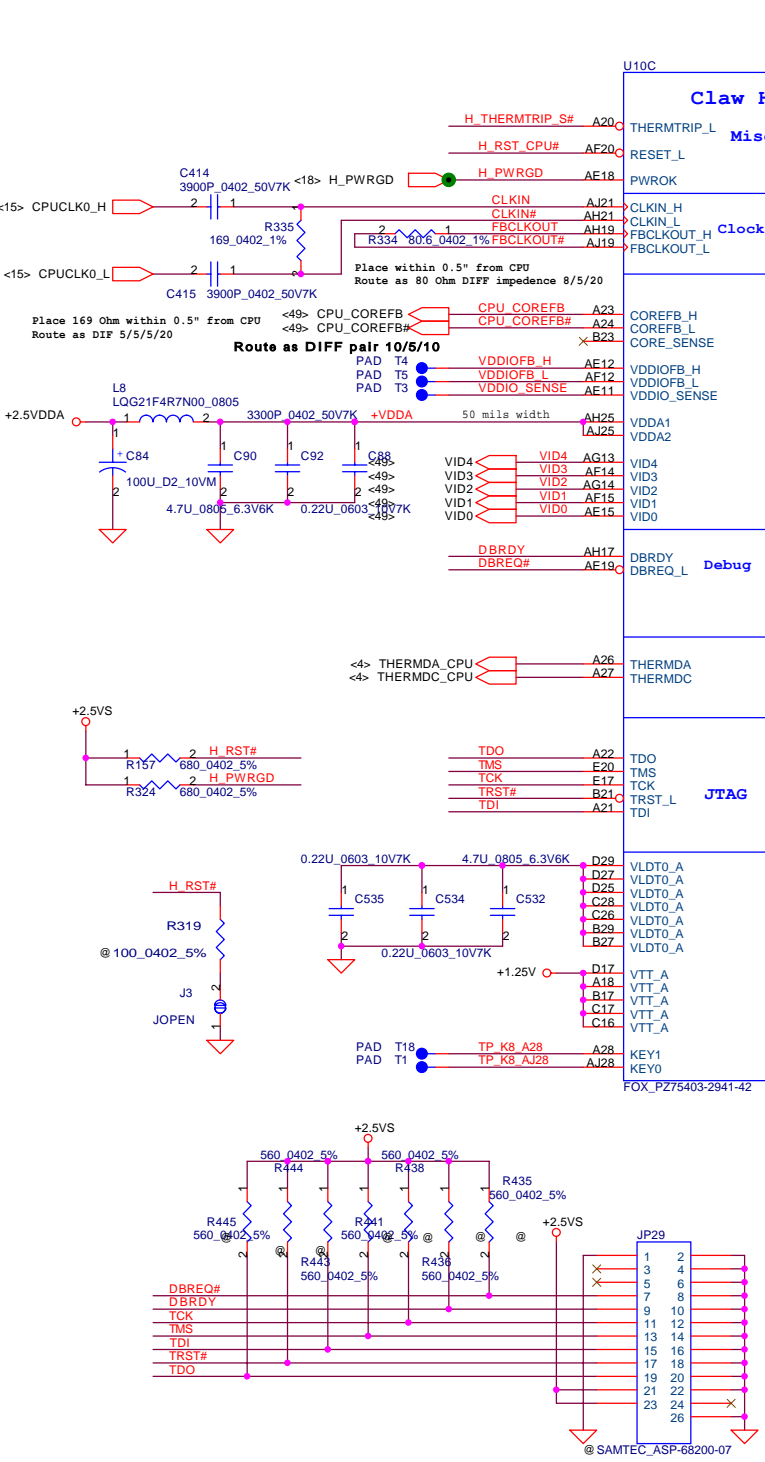


DDR_CLK5/5# & DDR_CLK7/7#
route to nearest DIMM
DDR_CLK4/4# & DDR_CLK6/6#
route to farthest DIMM

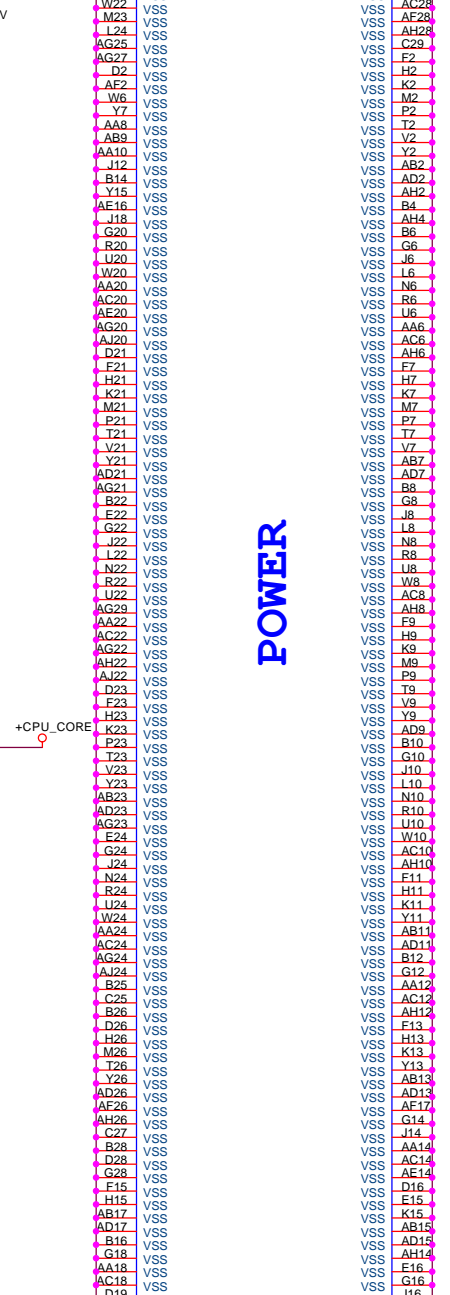
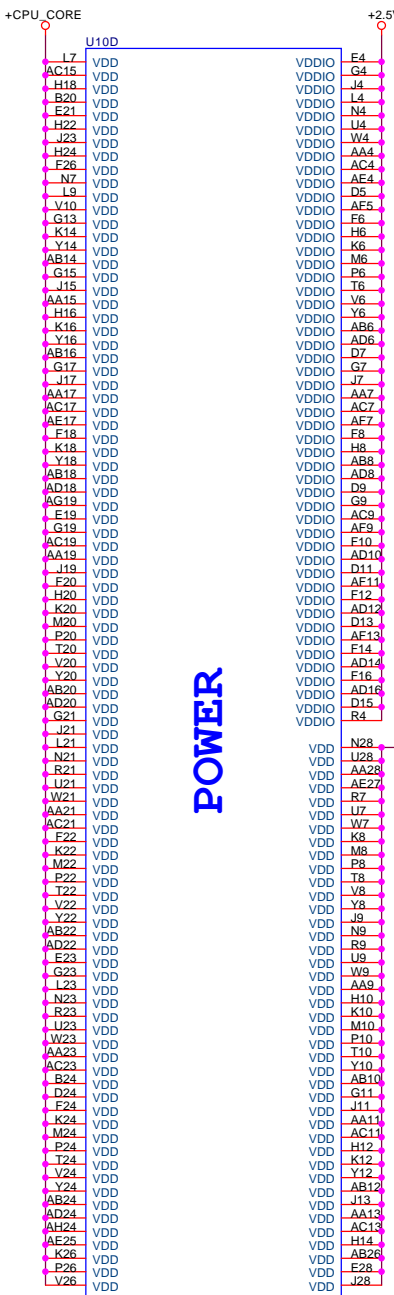


FOX_PZ75403-2941-42

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Issued Date	2005/03/01	Deciphered Date	2006/03/11	Claw Hammer (Memory Bus)	
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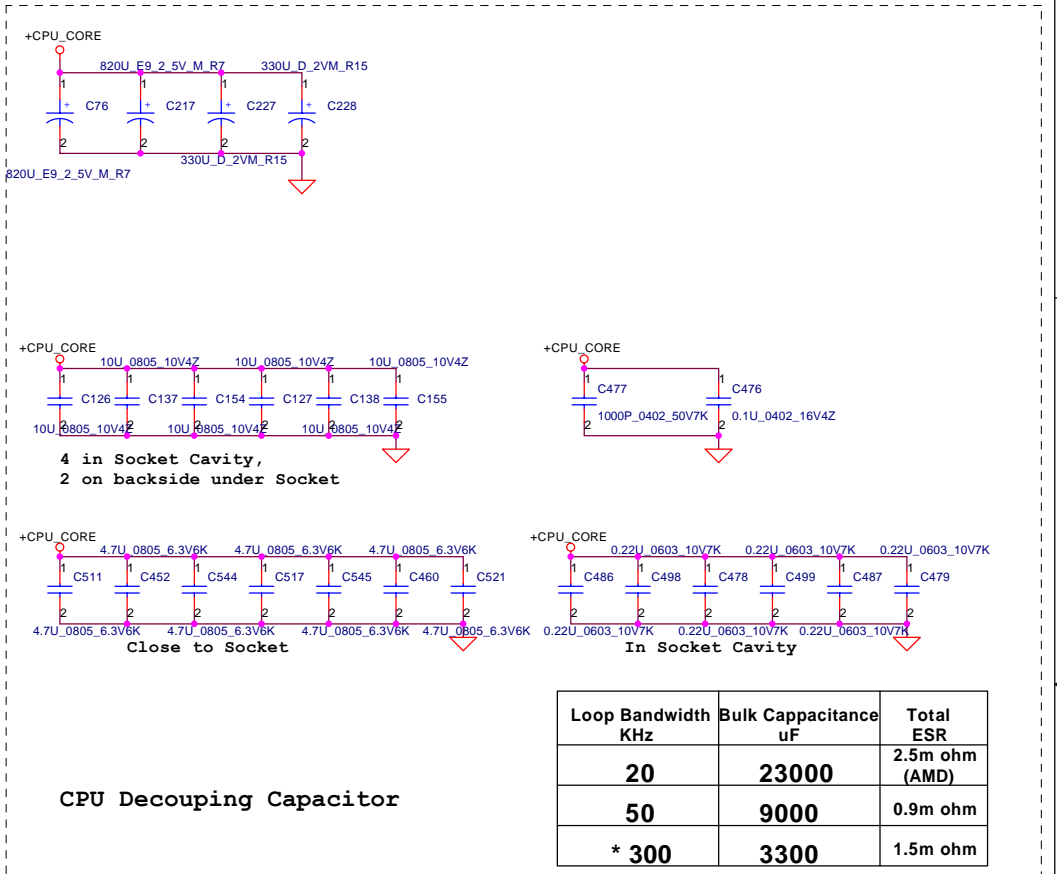


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Issued Date	2005/03/01	Deciphered Date	2006/03/11	Claw Hammer (MISC)	
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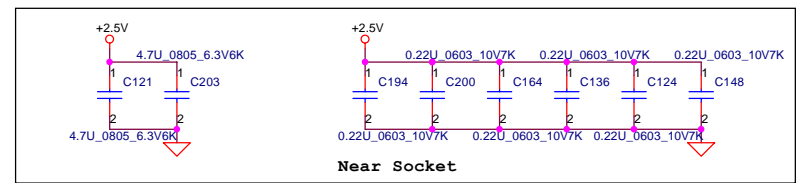


POWER

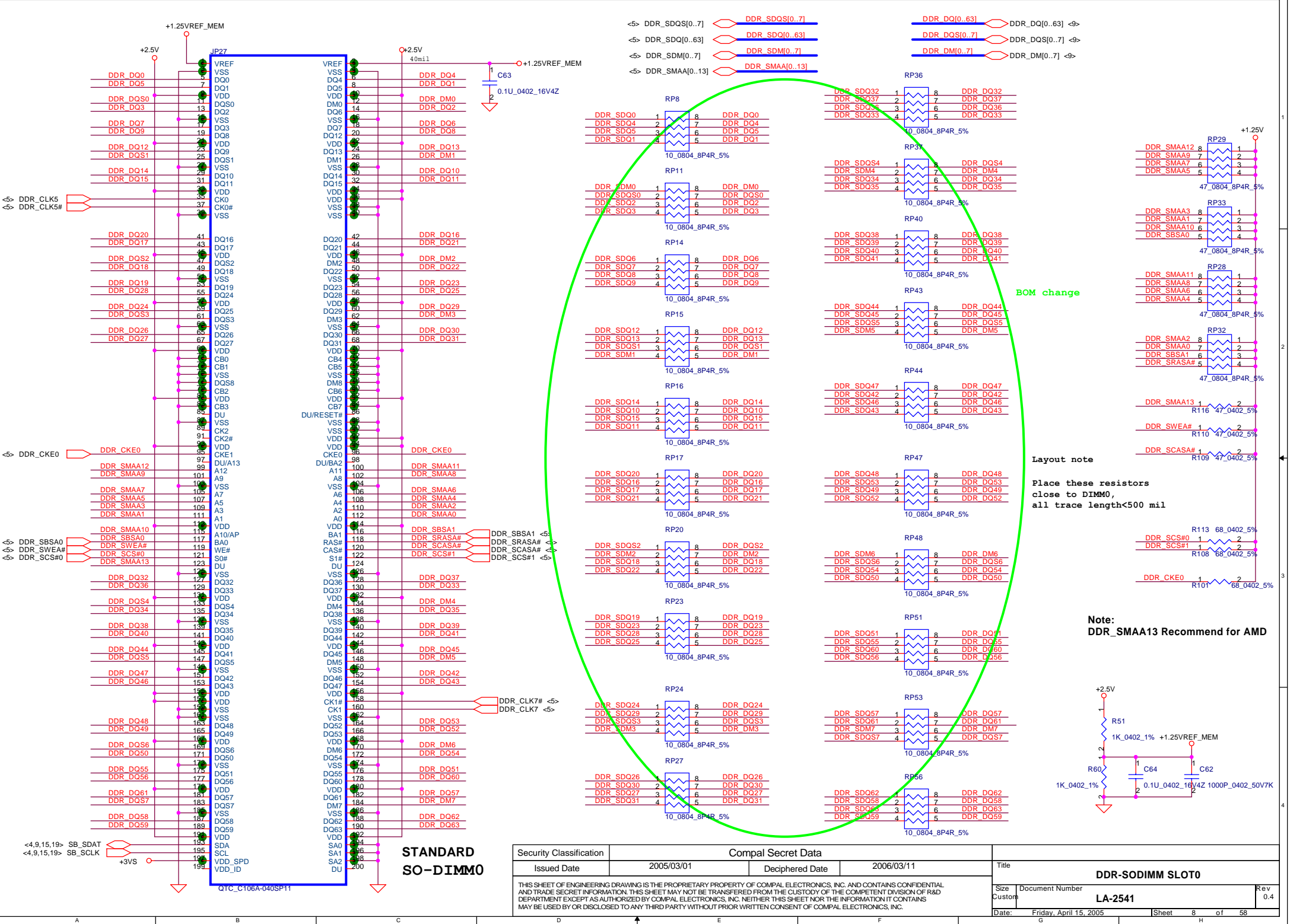
POWER



Loop Bandwidth KHz	Bulk Cappacitance uF	Total ESR
20	23000	2.5m ohm (AMD)
50	9000	0.9m ohm
* 300	3300	1.5m ohm

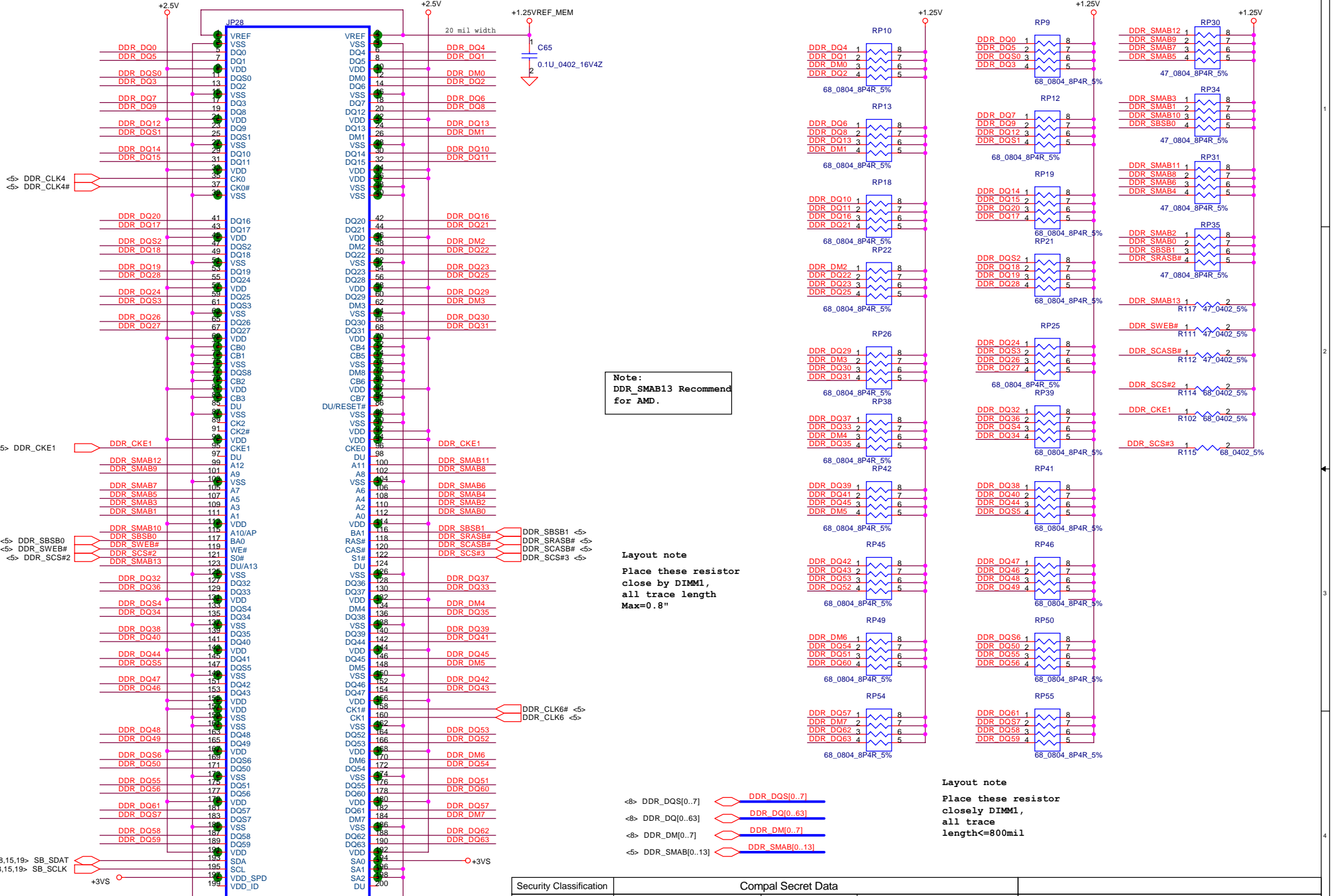


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Title		
DDR-SODIMM SLOT0		
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Note:
DDR_SMAB13 Recommend
for AMD.

Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

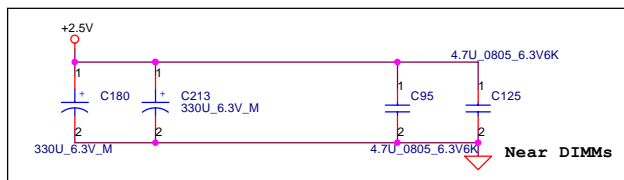
Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil

- <8> DDR_DQS[0..7]
- <8> DDR_DQ[0..63]
- <8> DDR_DM[0..7]
- <5> DDR_SMAB[0..13]

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Issued Date	2005/03/01	Deciphered Date	2006/03/11	DDR-SODIMM SLOT1	
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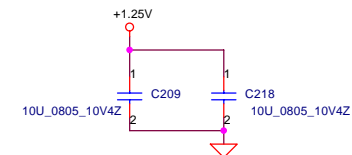
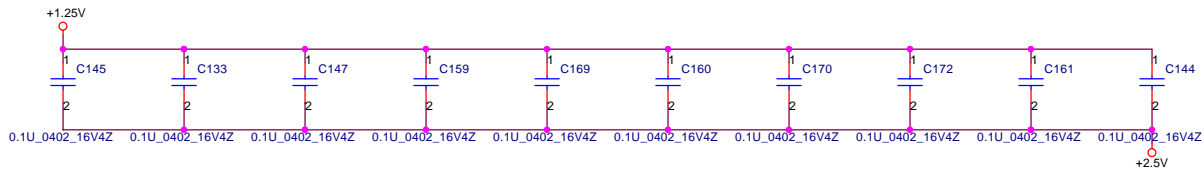
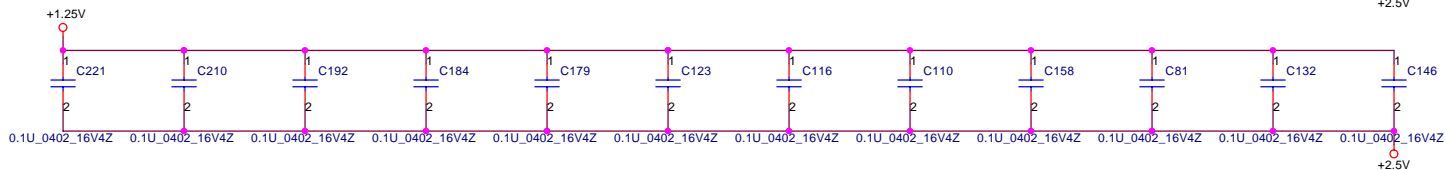
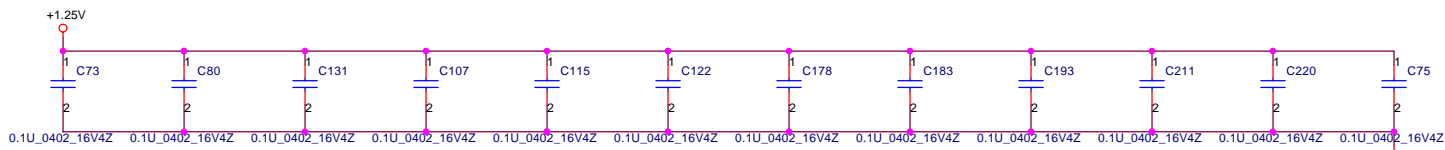
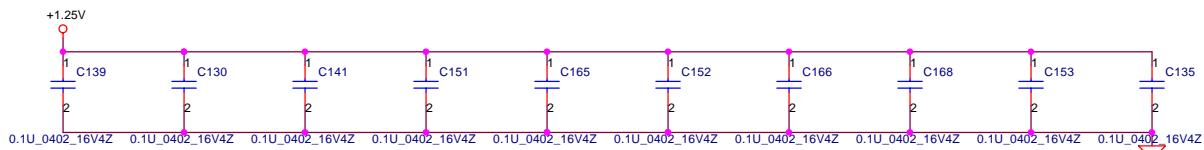
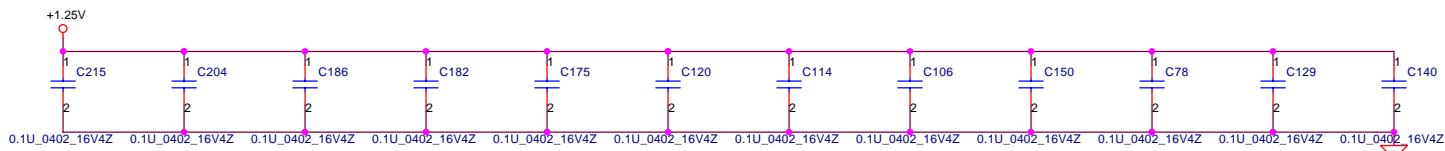
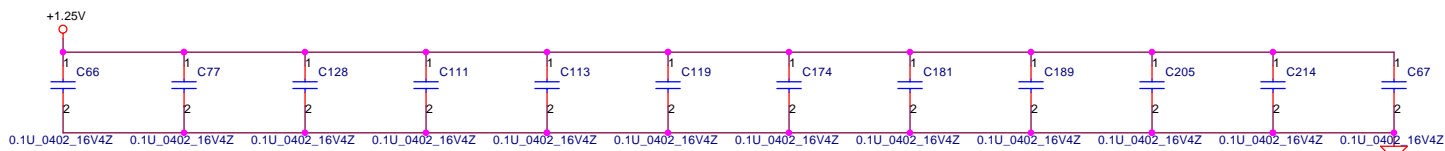
DIMM1
REVERSE

TYCO_1812560-1

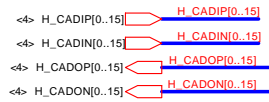


Layout note :

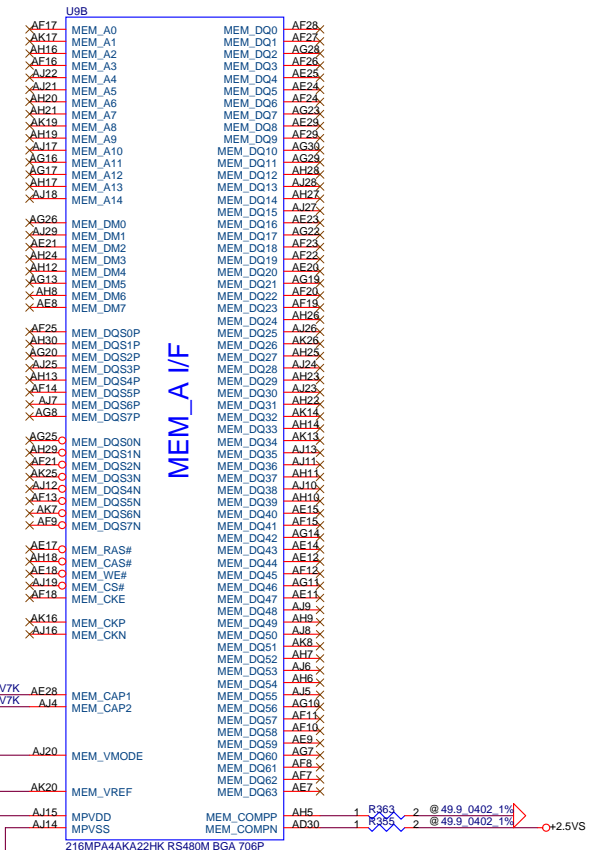
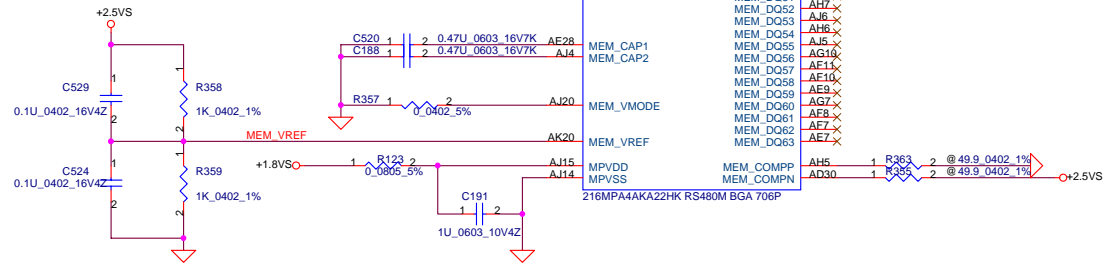
Place one cap close to every 2 pull up resistors termination to +1.25V



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Issued Date	2005/03/01	Deciphered Date	2006/03/11	DDR SODIMM Decoupling	
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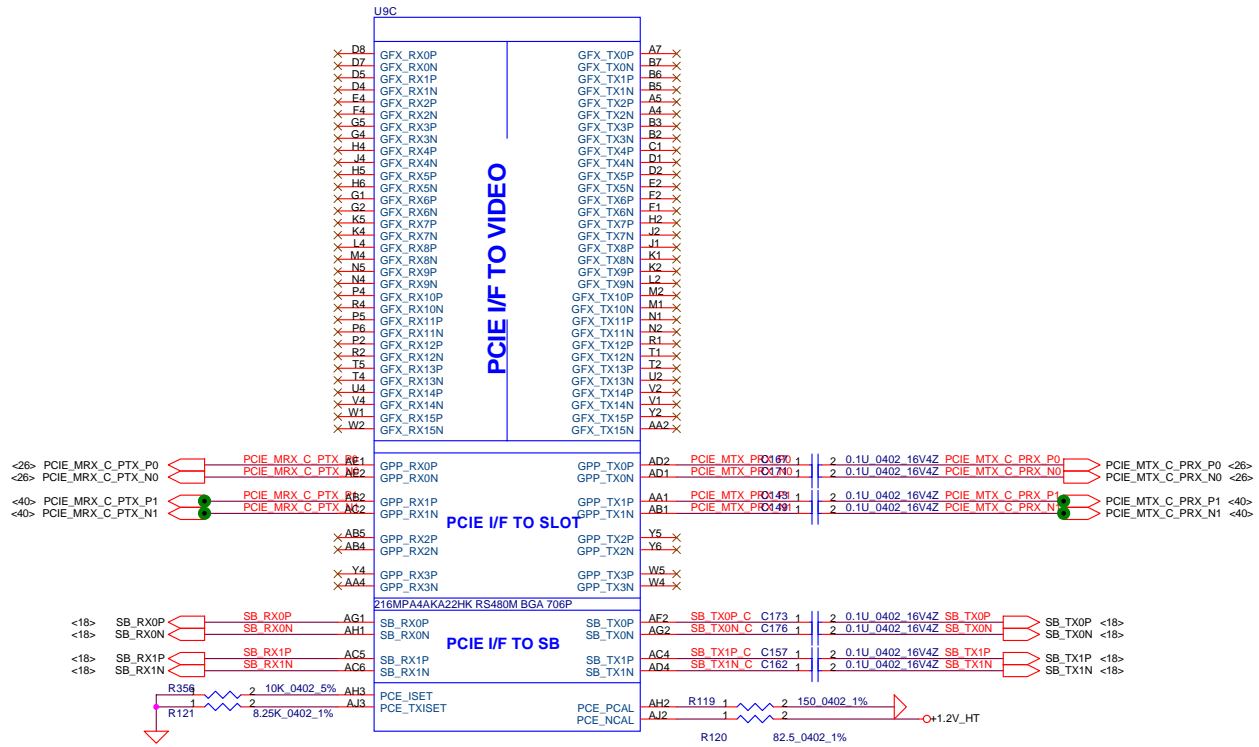
HYPER TRANSPORT CPU I/F



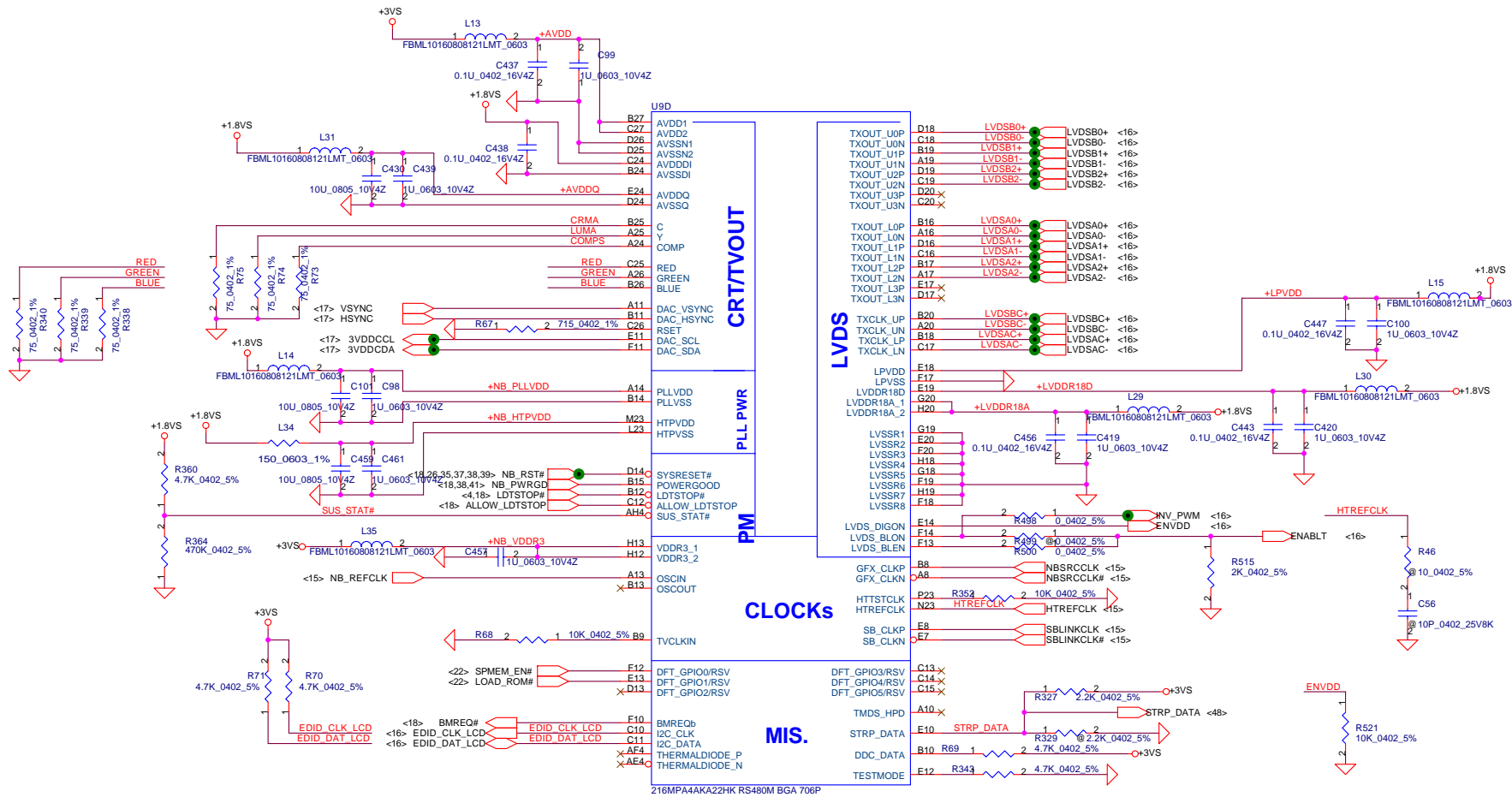
MEM_A I/F

Security Classification				Compal Secret Data			
Issued Date	2005/03/01		Deciphered Date	2006/03/11		Title	
						RS480M HT/MEM	
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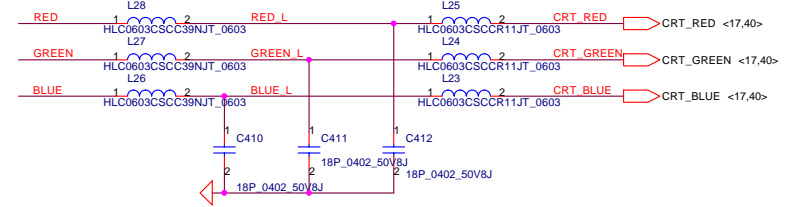
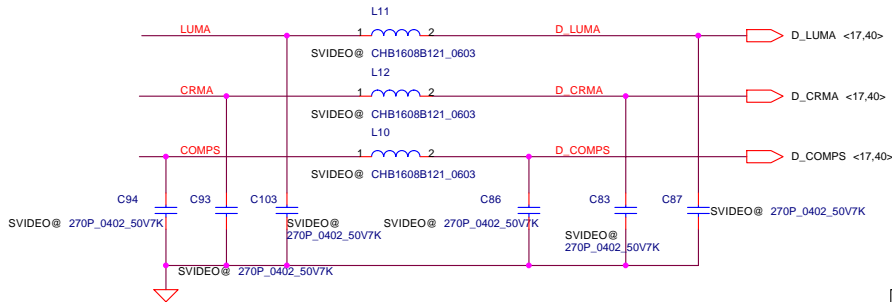
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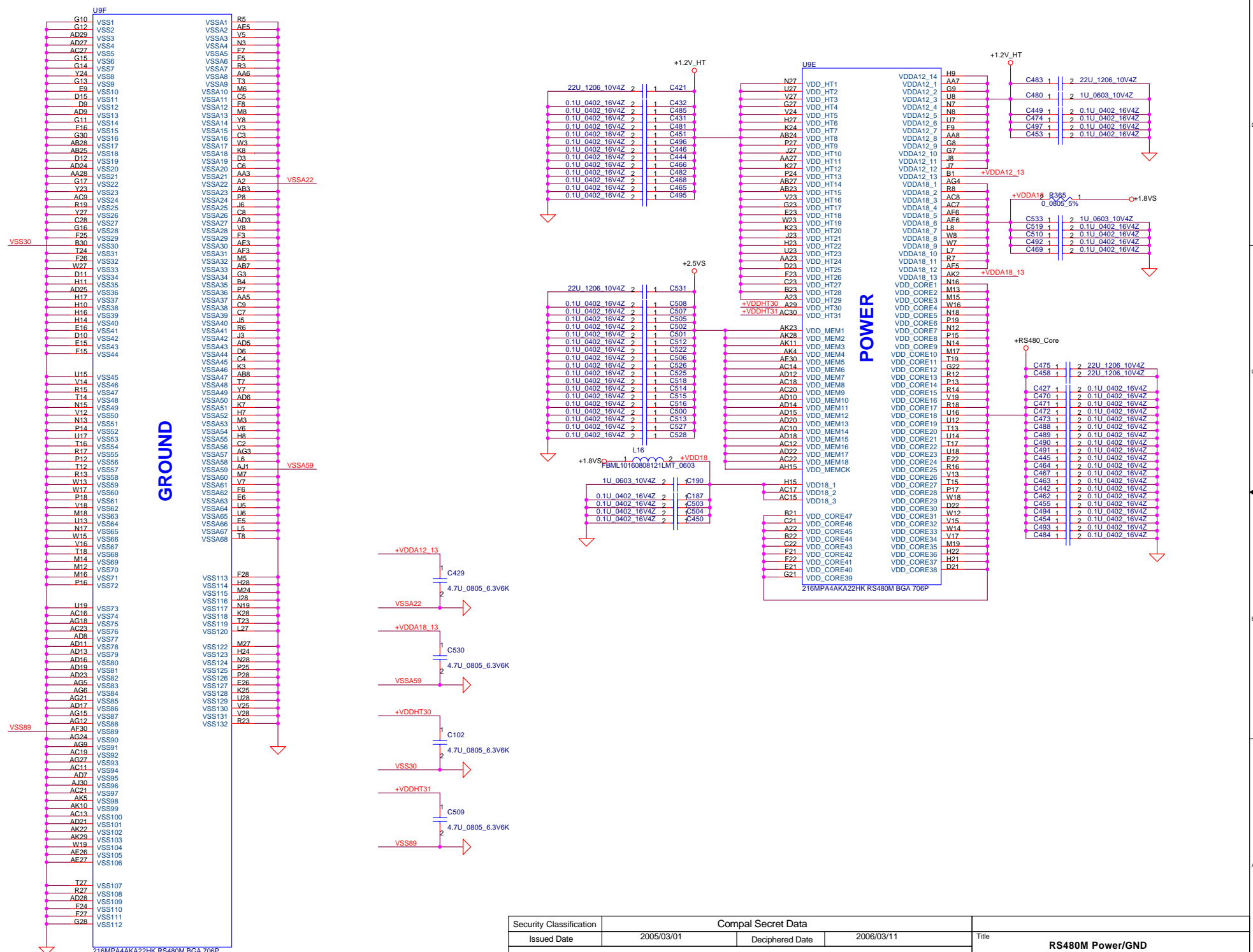
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Issued Date	2005/03/01	Deciphered Date	2006/03/11	RS480M PCIe/DVI Controller	
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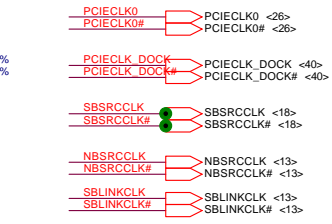
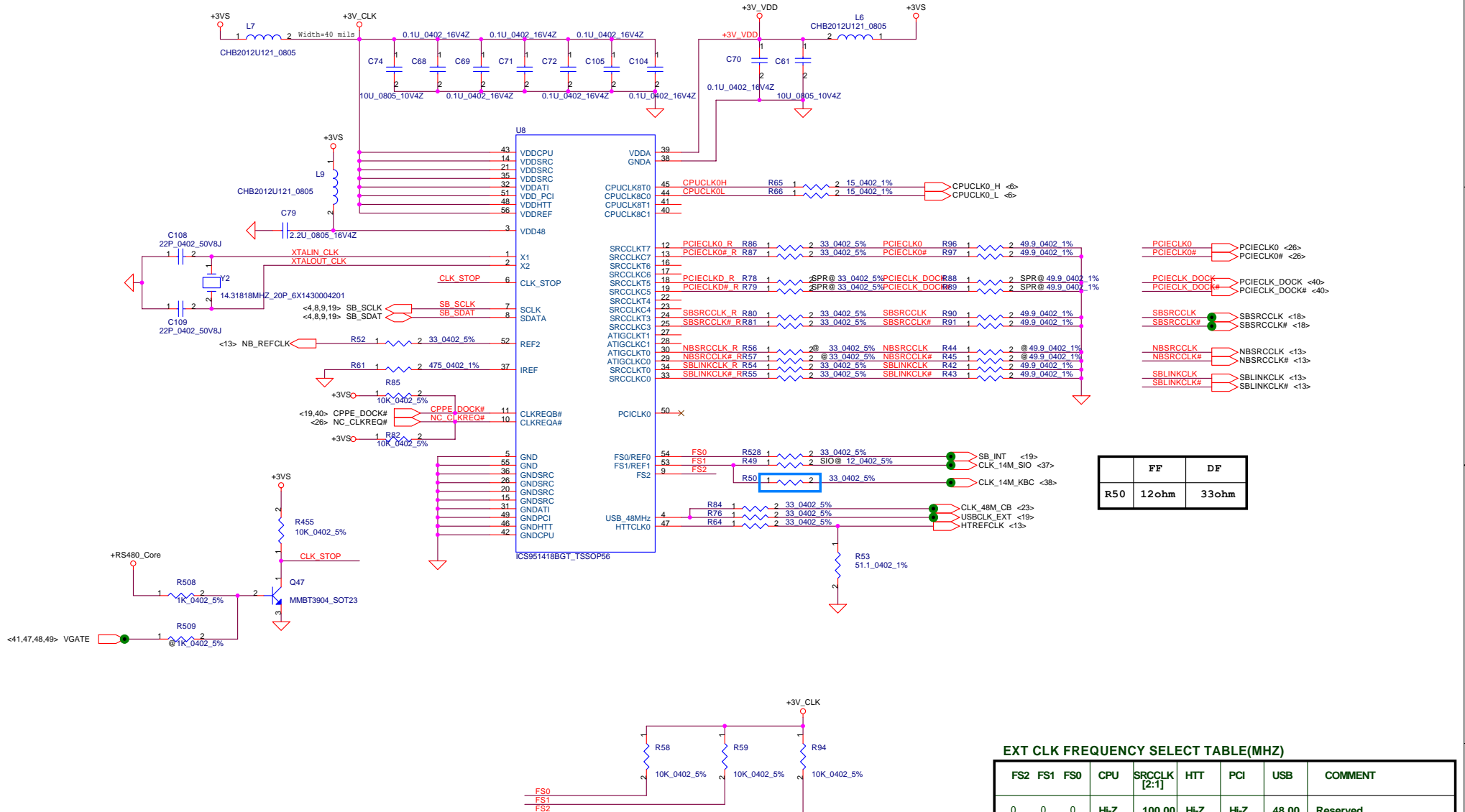
216MPA4AKA22HK RS480M BGA 706P



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Issued Date	2005/03/01	Deciphered Date	2006/03/11	RS480M VIDEO_IF/CLOCK GEN	
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Issued Date	2005/03/01	Deciphered Date	2006/03/11	RS480M Power/GND	
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	FF	DF
R50	12ohm	33ohm

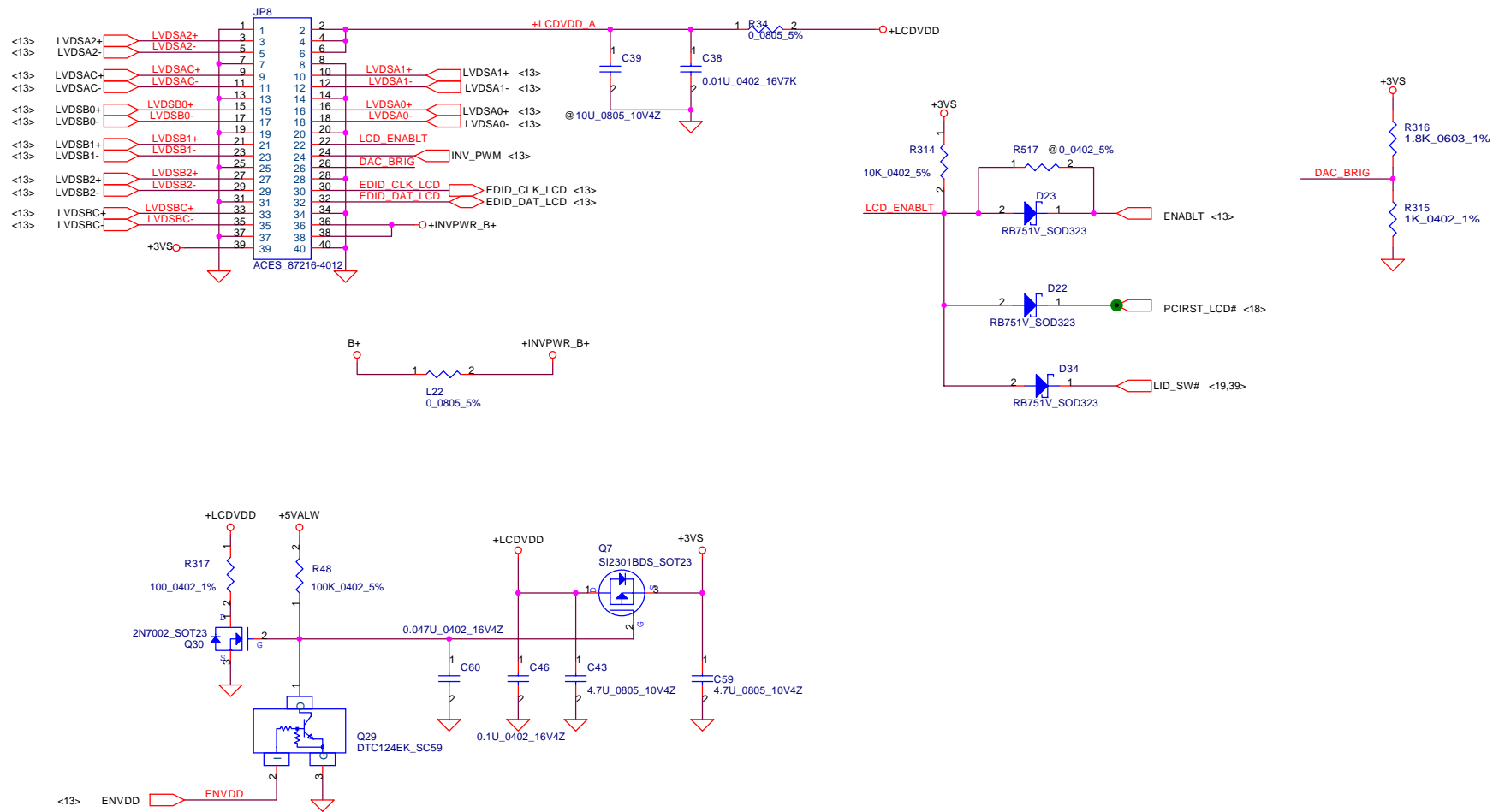
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	Clock Generator
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size Custom Document Number LA-2541 Rev 0.4
Date: Friday, April 15, 2005			Sheet 15 of 58	

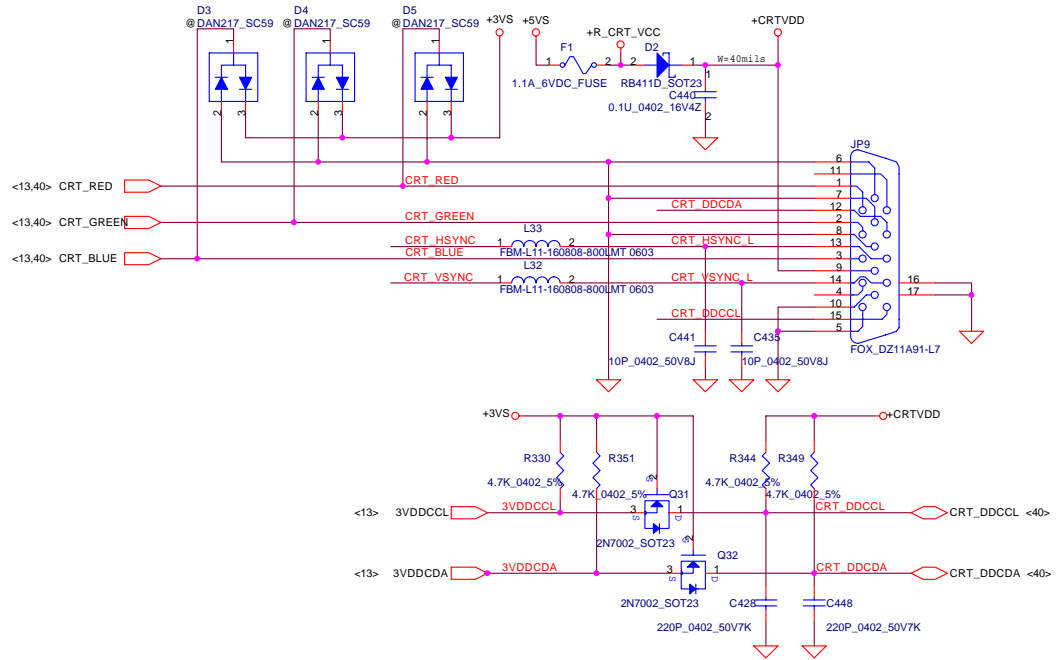
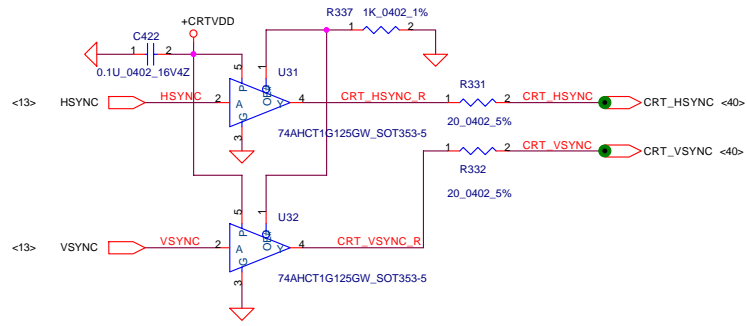
LCD Panel Connector

The cap.'s colselly to LCD CONN.



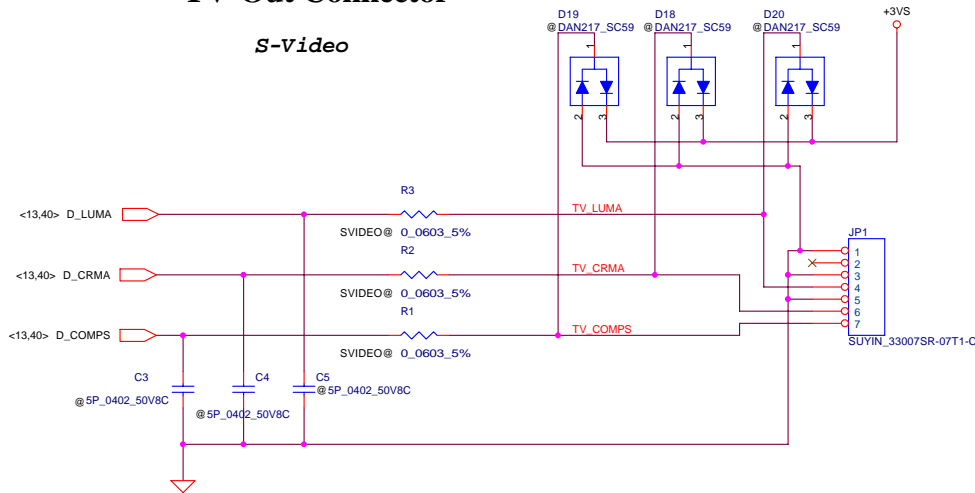
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	LVDS Connector	
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				LA-2541	
				Date:	Rev
				Friday, April 15, 2005	0.4
				Sheet	16 of 58

CRT CONNECTOR

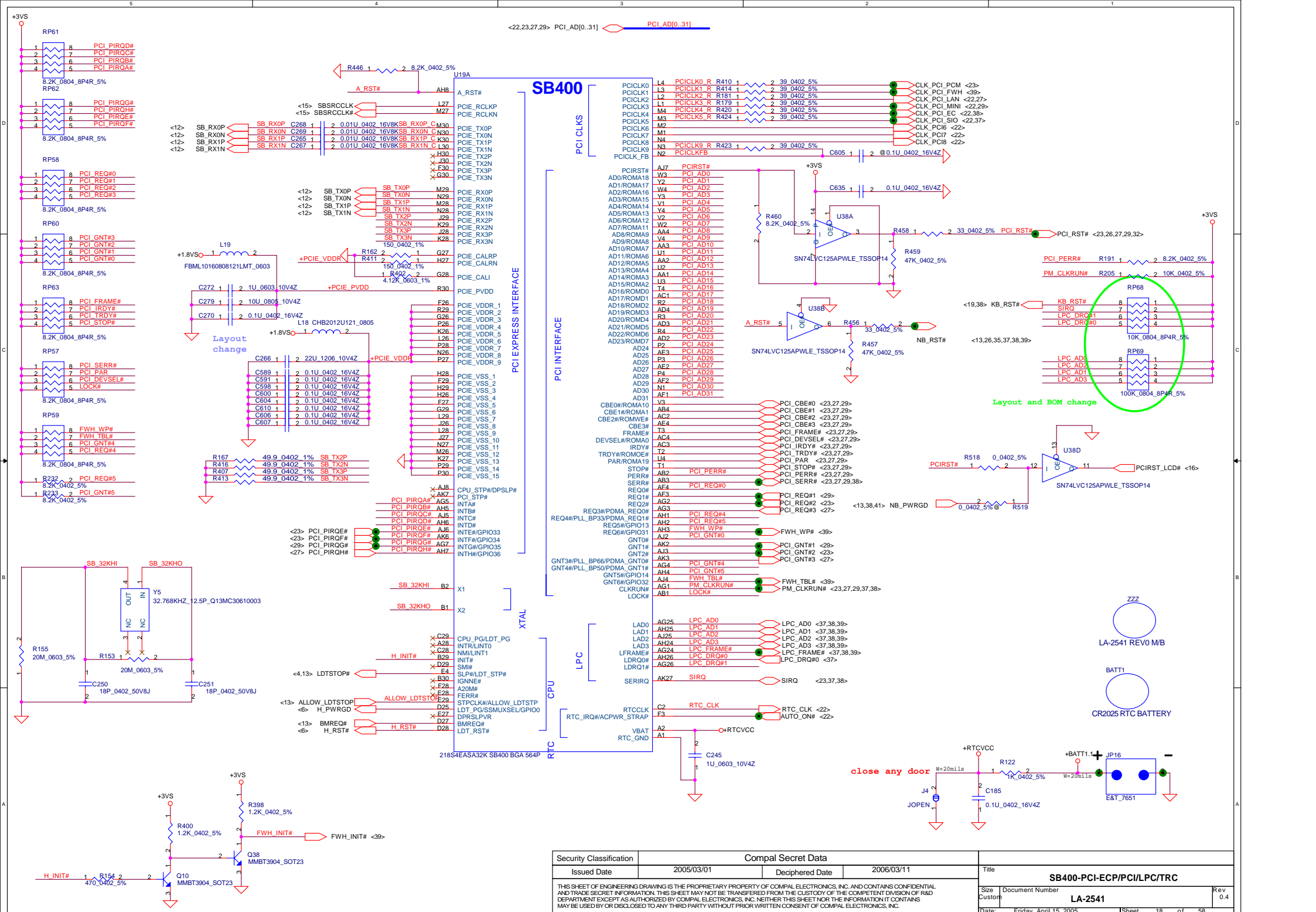


TV-Out Connector

S-Video

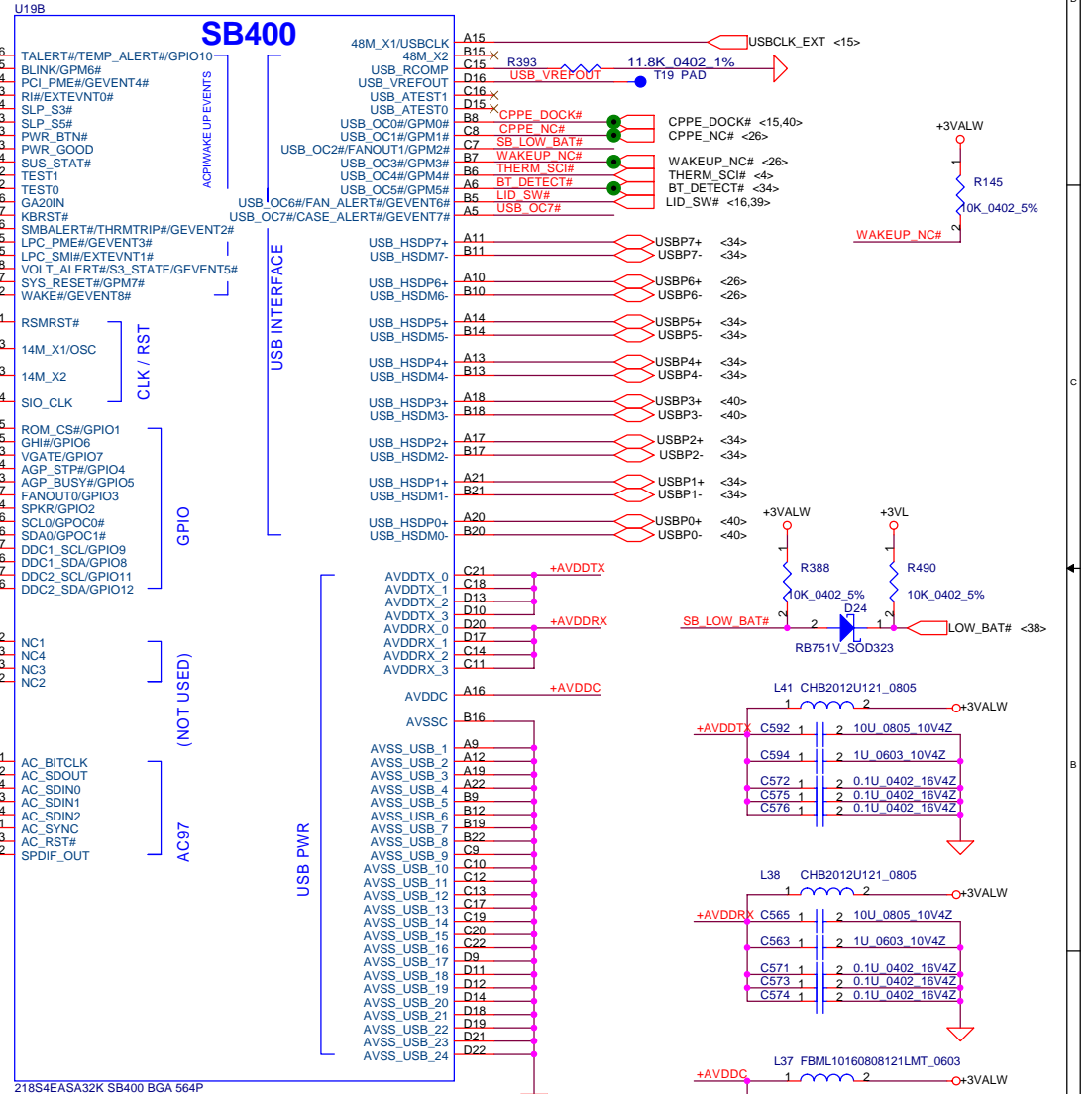
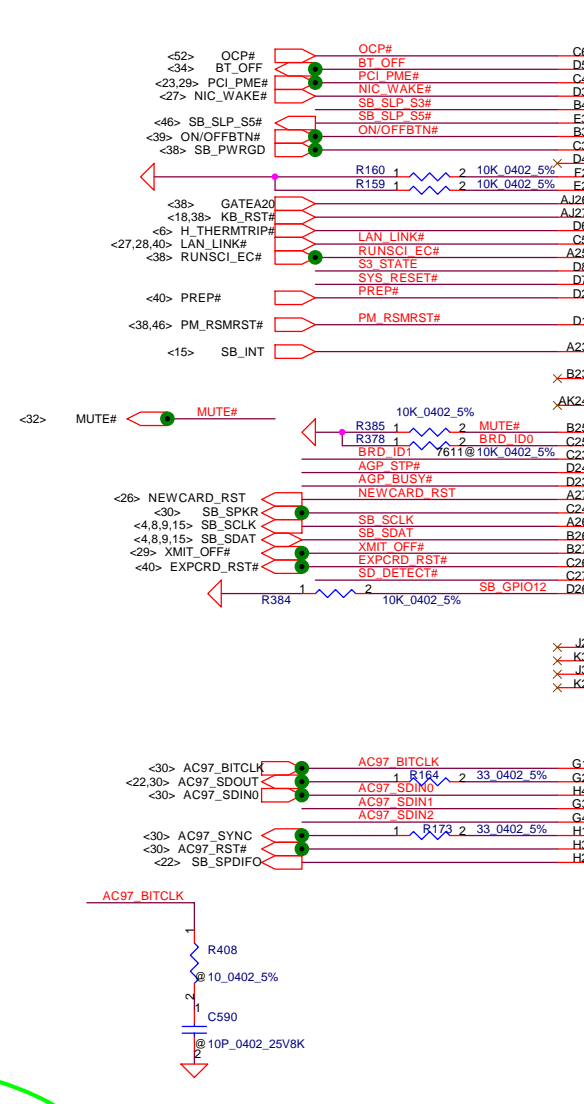
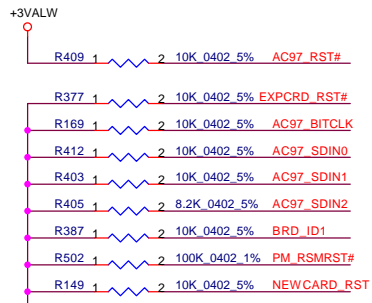
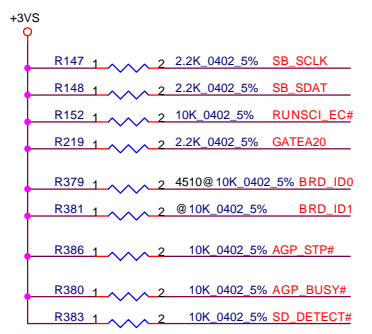
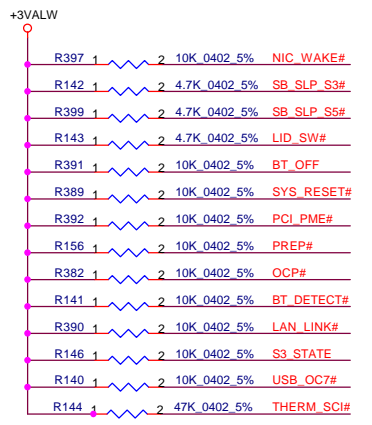


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	CRT & TV out Connector	
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Size	Document Number	Rev		Date	
Custom	LA-2541	0.4		Friday, April 15, 2005	
Date			Sheet 17 of 58		

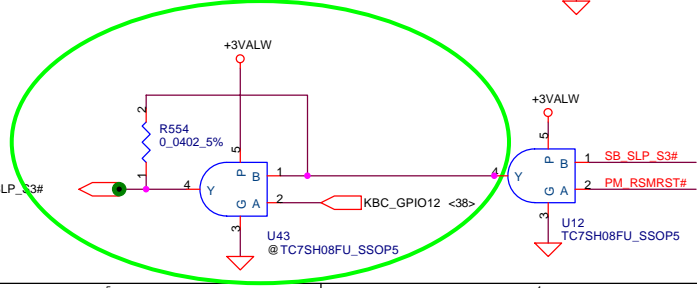


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	SB400-PCI-ECP/PCI/LPC/RTC	
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Date:	Friday, April 15, 2005	Sheet	18	of	58

Board ID Settings		
BRD ID1	BRD ID0	feature
0	0	full-featured
0	1	de-featured

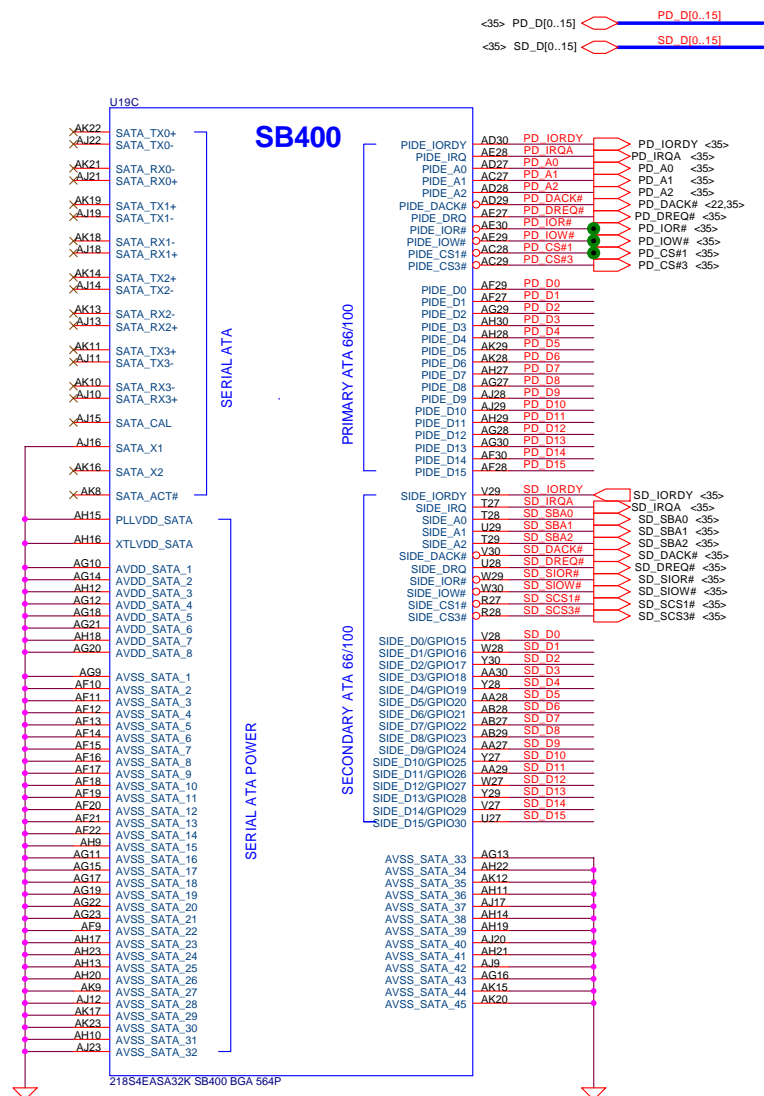


BOM and layout modify

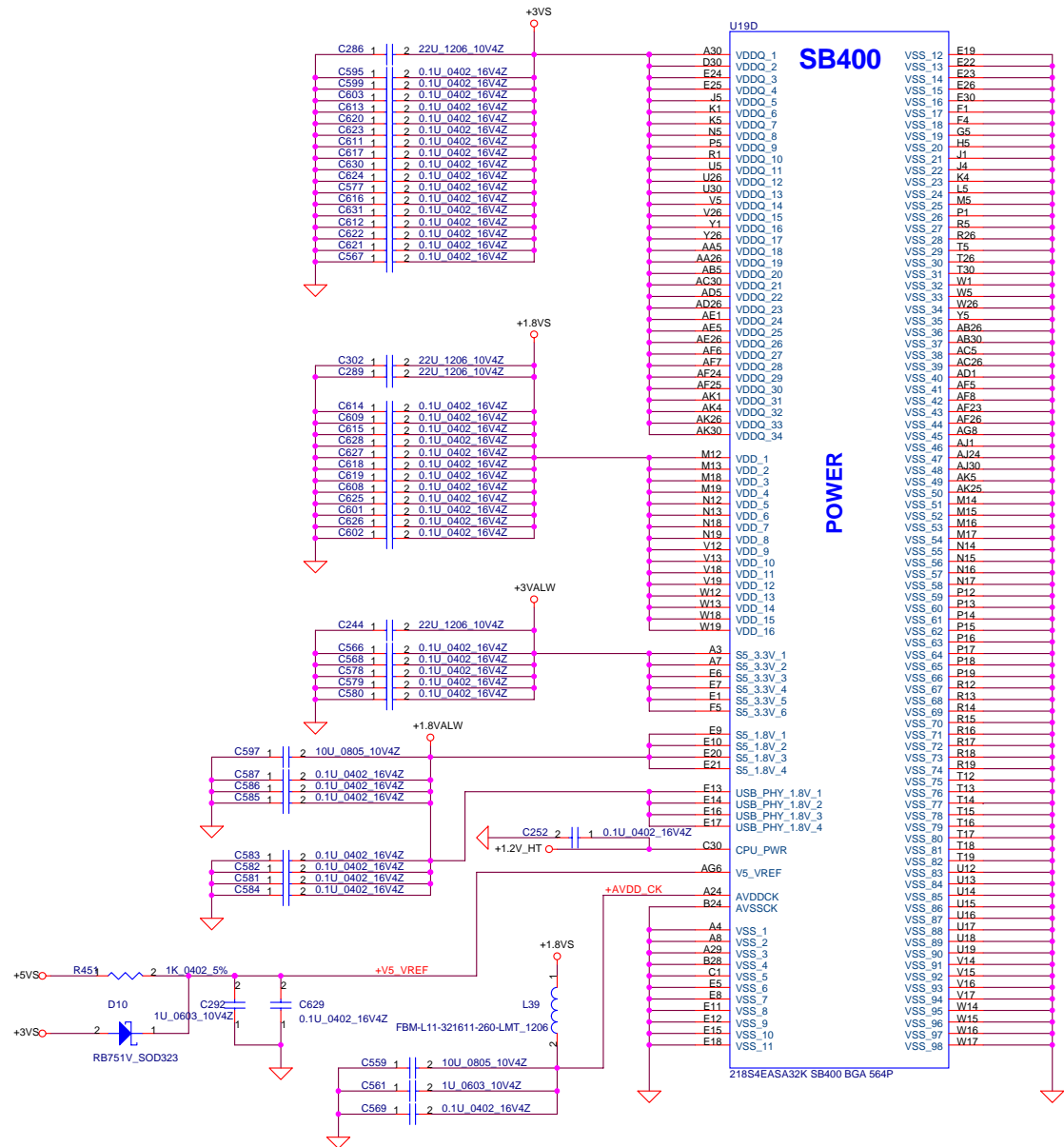


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	SB400 USB/ACPI/AC97/GPIO	
Size	Custom	Document Number	LA-2541	Rev	0.4
Date:	Friday, April 15, 2005	Sheet	19	of	58

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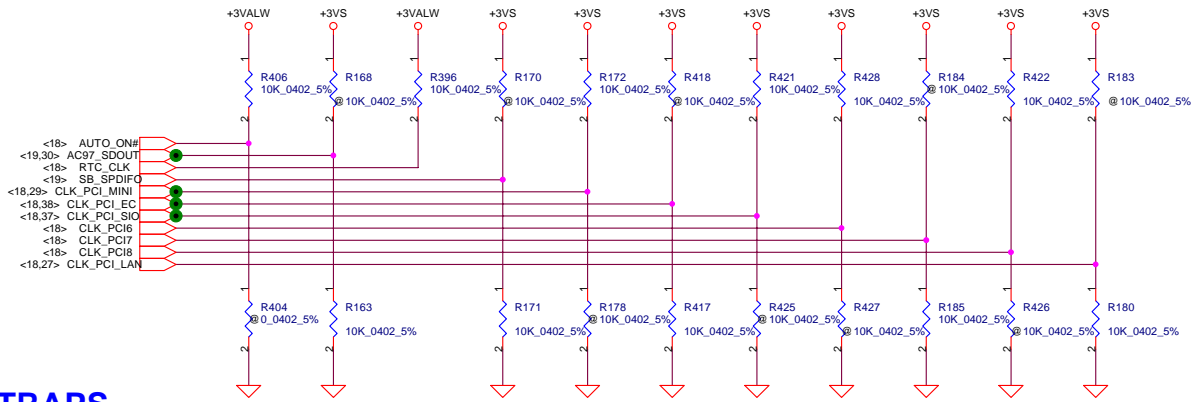


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	SB400 IDE/SATA	
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				Custom	LA-2541
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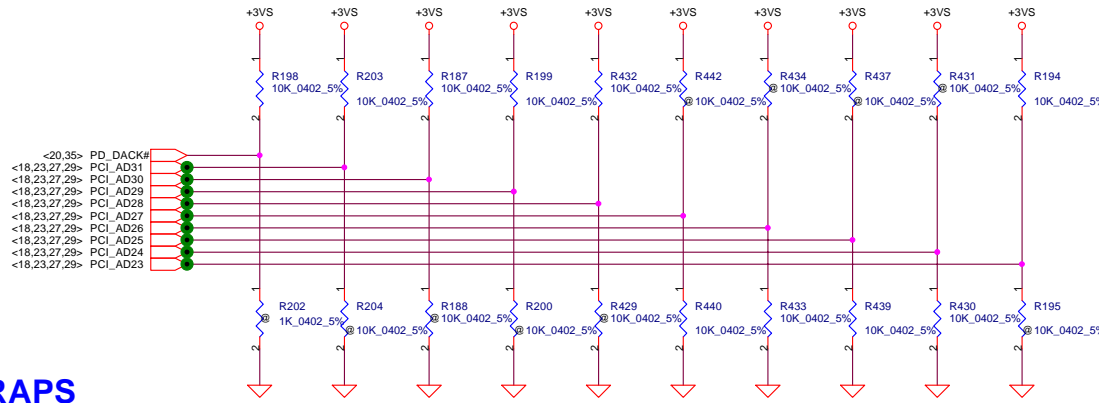
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Issued Date	2005/03/01	Deciphered Date	2006/03/11	SB400 Power/GND	
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REQUIRED STRAPS



	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7	PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz XTAL MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz OSC / Clock buffer MODE DEFAULT	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	14MHz XTAL MODE	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM	DEFAULT

DEBUG STRAPS



	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	USE USB PLL
PULL LOW	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BY PASS USB PLL DEFAULT

NB STRAPS (internal pulled up)

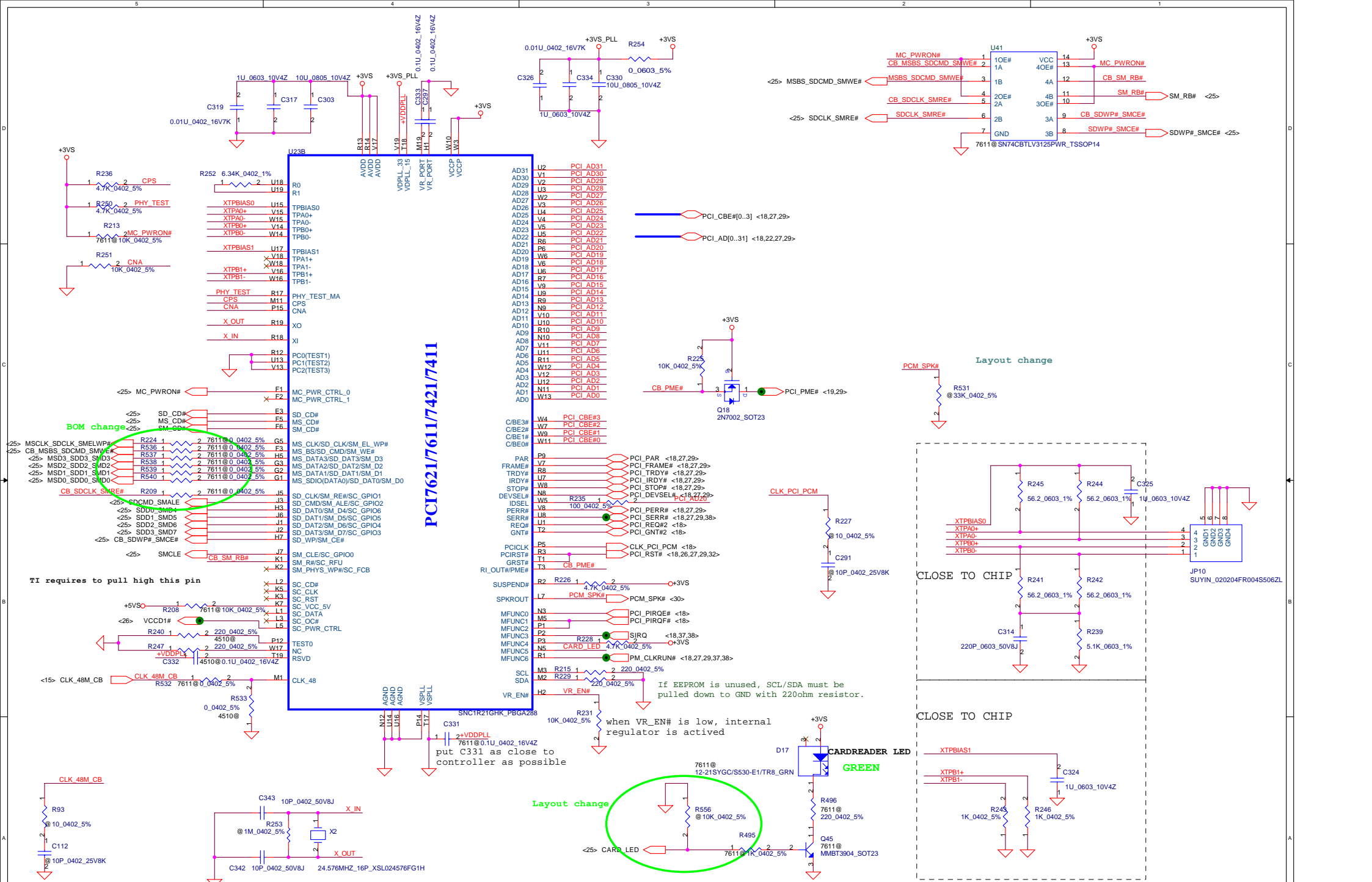
LOAD_ROM#: LOAD ROM STRAP ENABLE strap

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

SPMEM_EN#: SIDE PORT MEMORY ENABLE strap

High, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	Hardware Strap	
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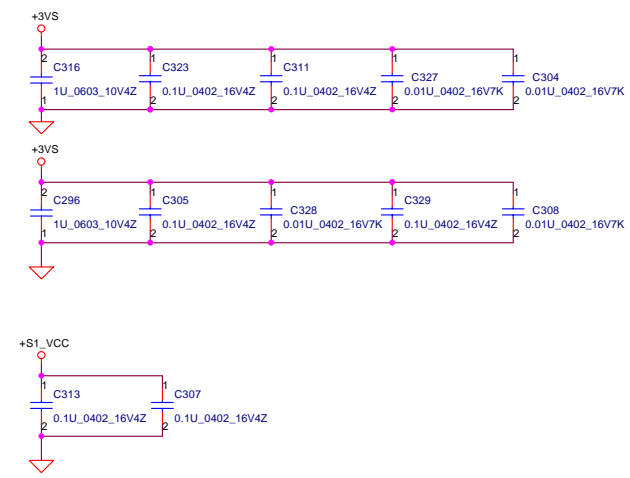
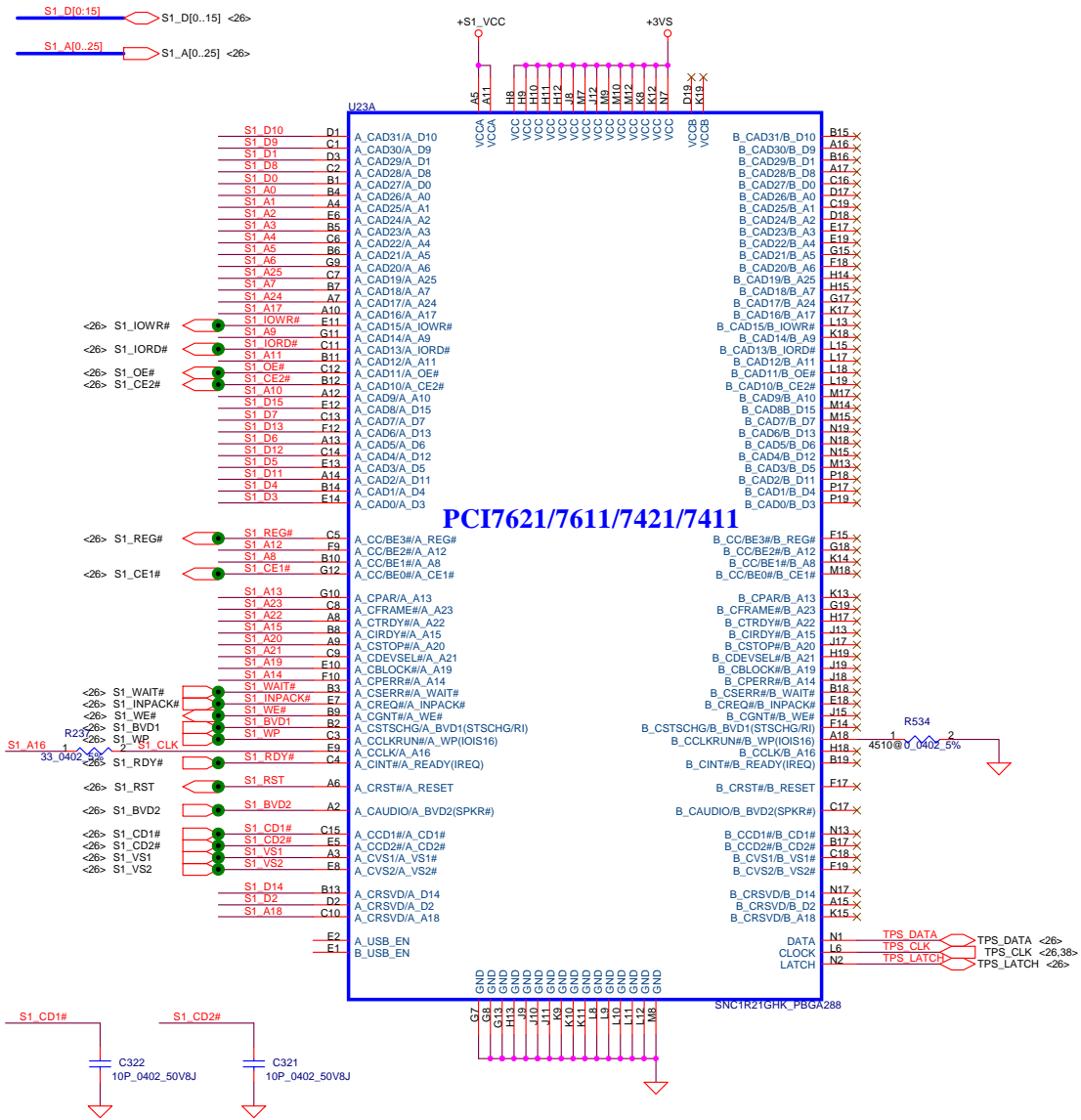
PCI7621/7611/7421/7411

Security Classification		Compal Secret Data	
Issued Date	2005/03/01	Deciphered Date	2006/03/11

Title			
CardBus Controller TI7611			
Size	Document Number	Rev	
Custom	LA-2541	0.4	
Date:	Friday, April 15, 2005	Sheet	23 of 58

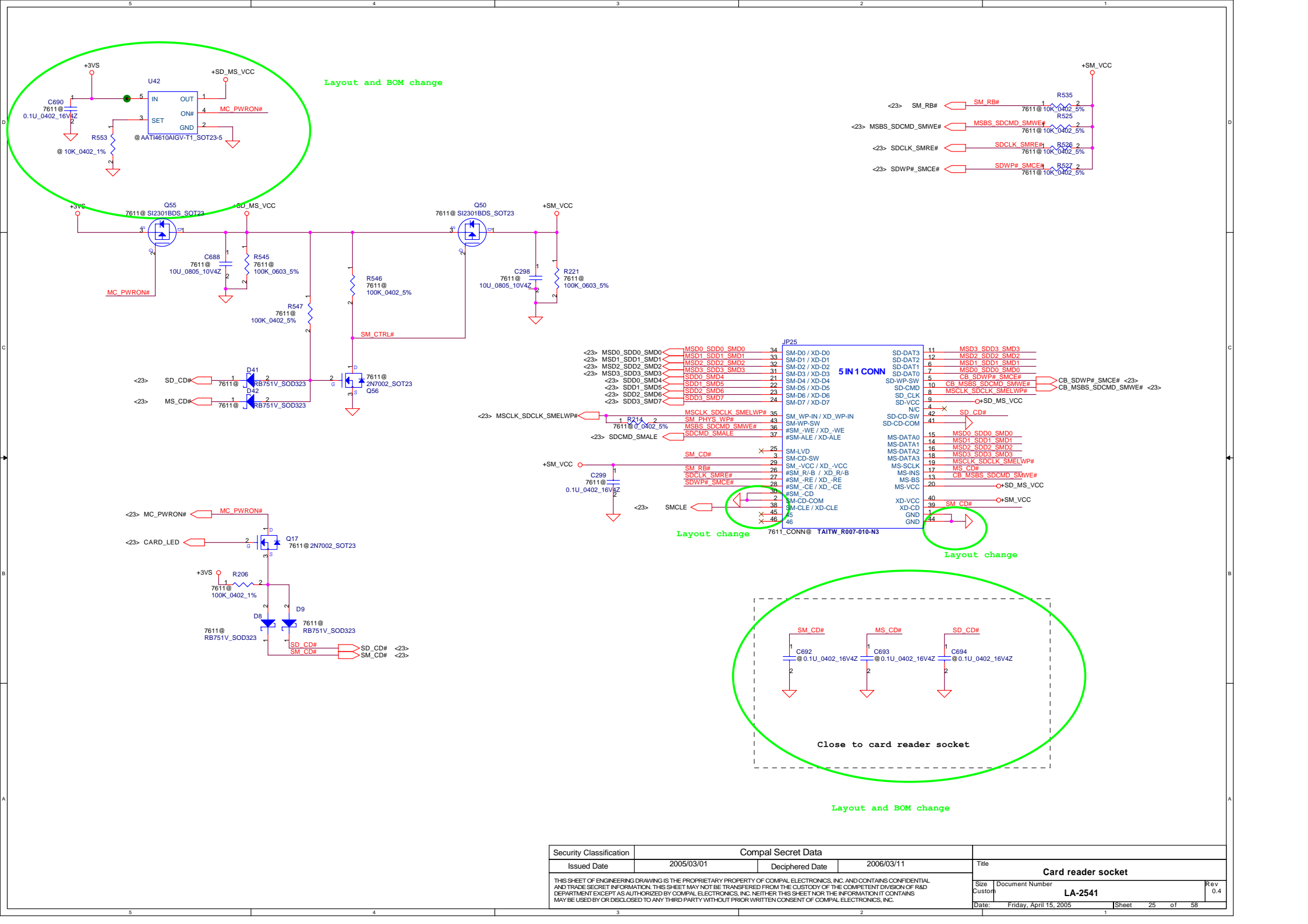
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S1_D[0..15] <26>
S1_A[0..25] <26>



PCI621/7611/7421/7411

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	CardBus controller TI 7611	
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				LA-2541	Rev 0.4
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Layout and BOM change

Layout change

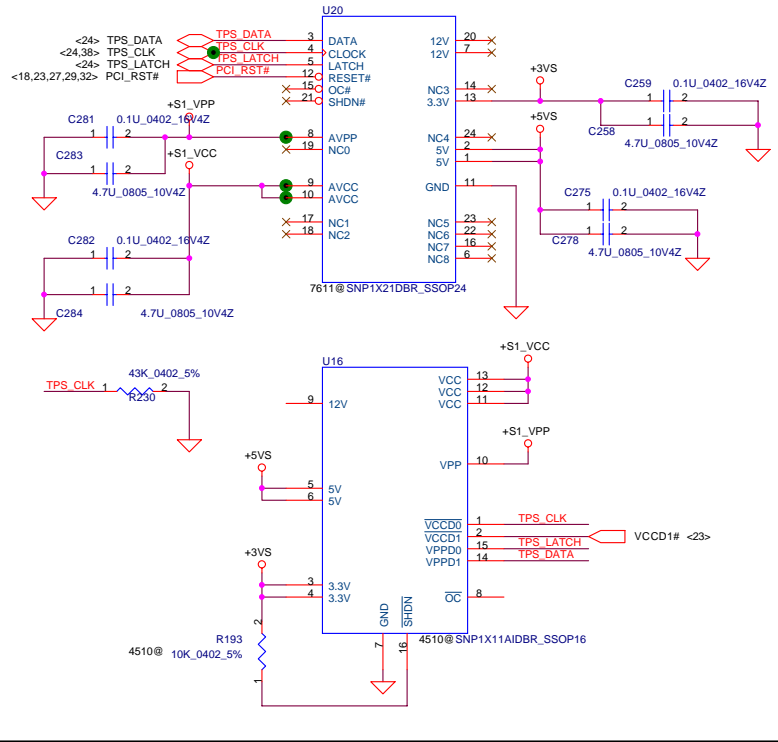
Layout change

Close to card reader socket

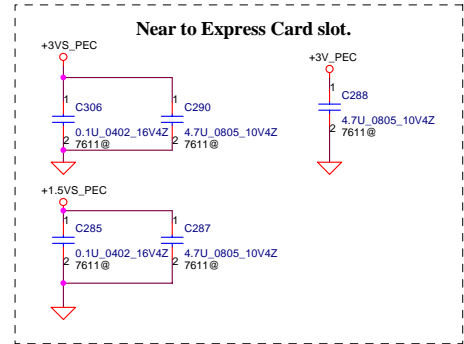
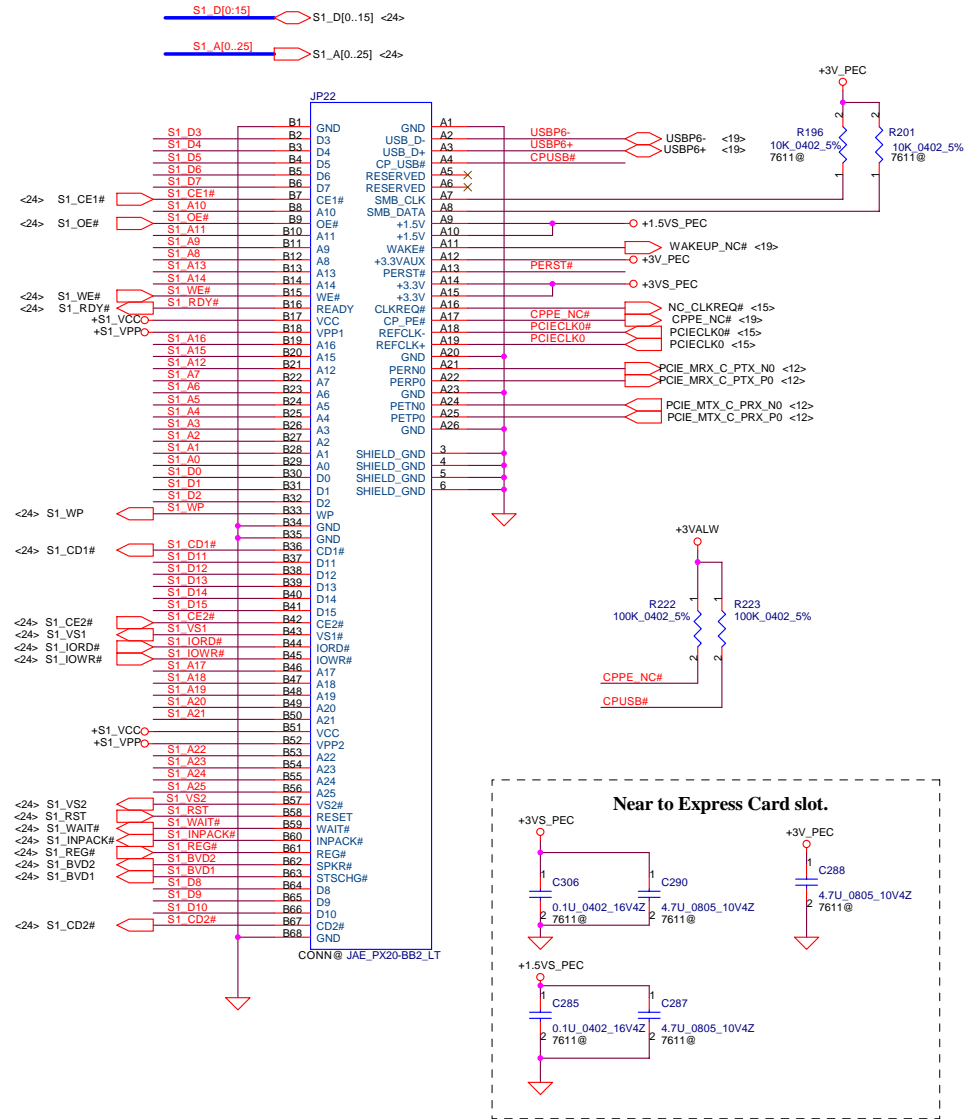
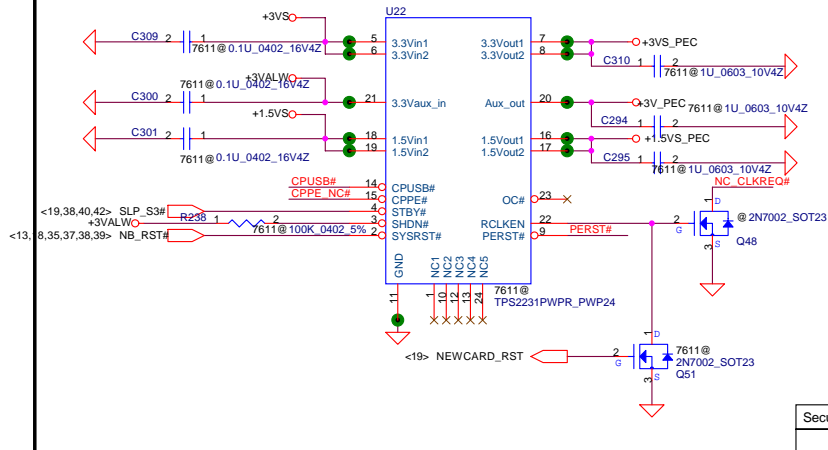
Layout and BOM change

Security Classification	Compal Secret Data		Title	Card reader socket	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	Size	Document Number
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				Date:	Friday, April 15, 2005
				Sheet	25 of 58
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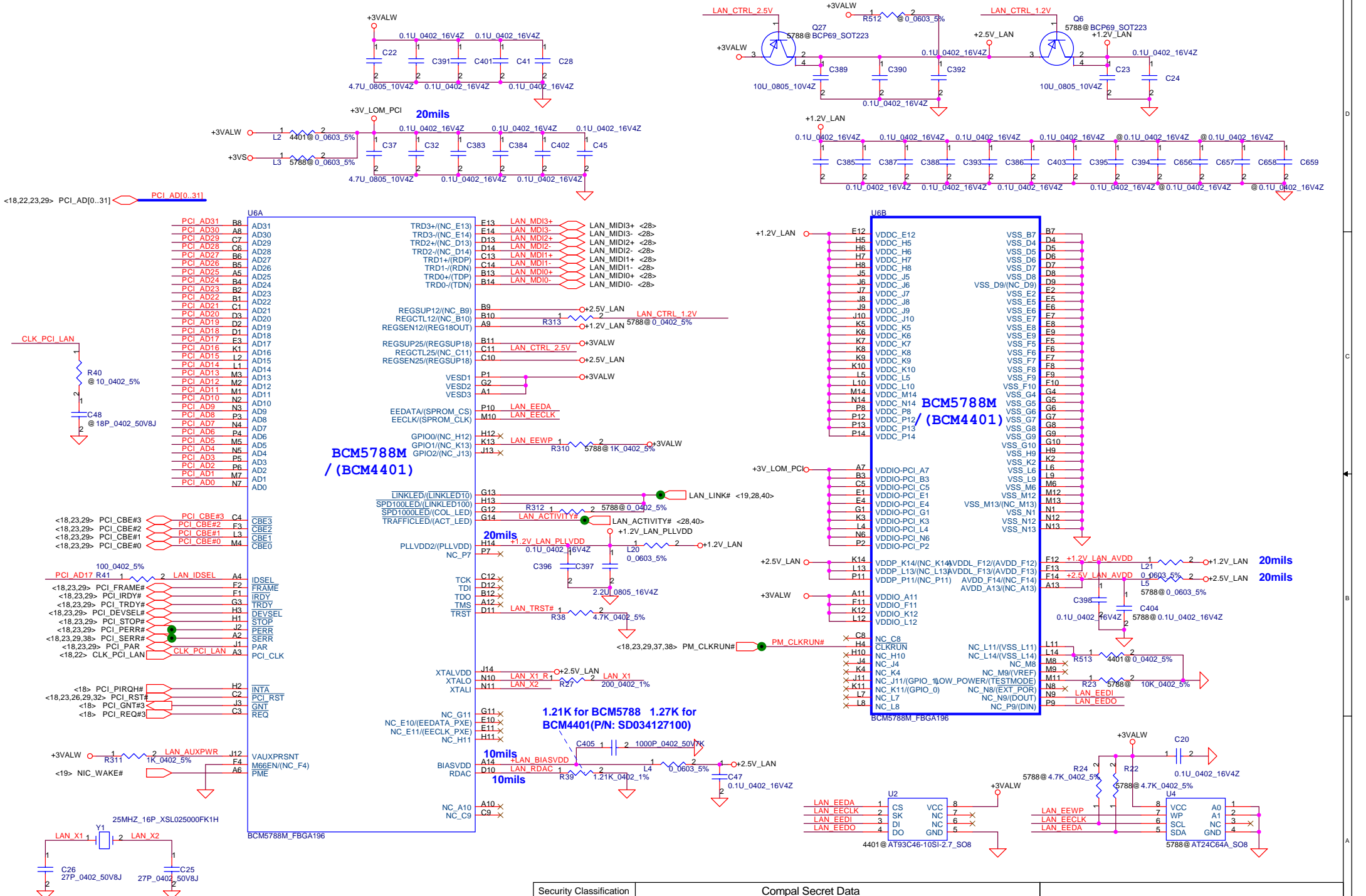
CardBus Power Switch



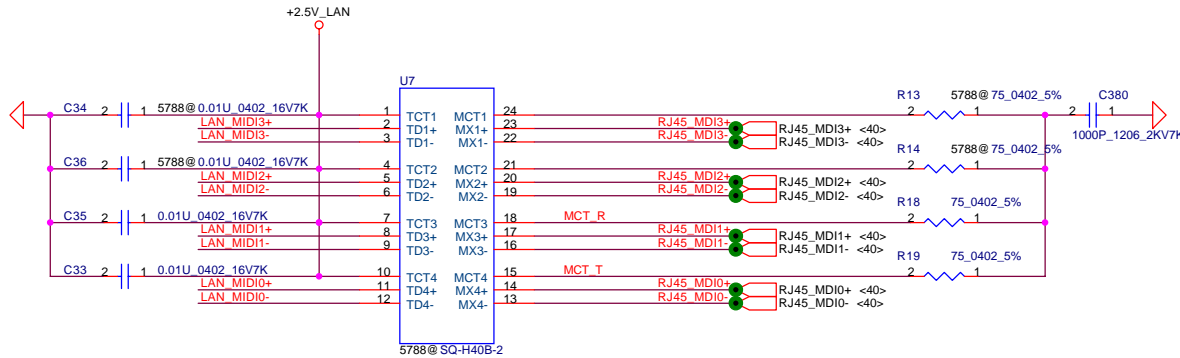
New Card Power Switch



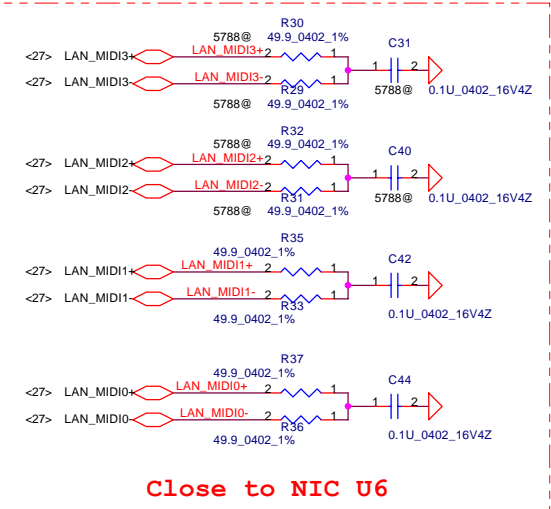
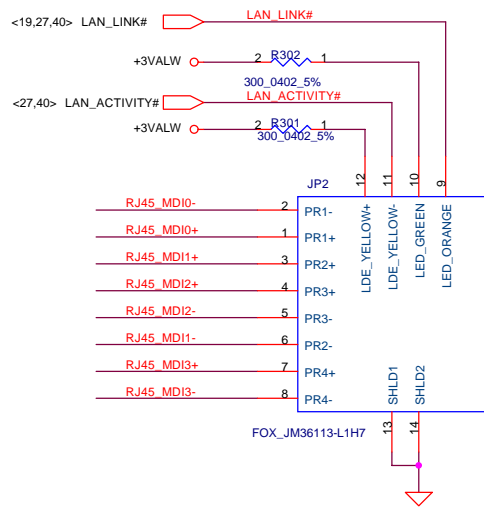
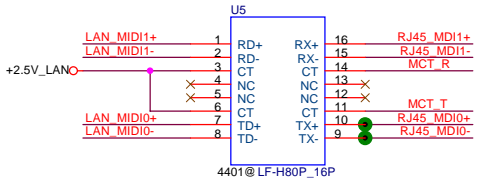
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Issued Date	2005/03/01	Deciphered Date	2006/03/11	PCMCIA /Express card socket	
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Issued Date	2005/03/01	Deciphered Date	2006/03/11	LAN controller BCM5788M	
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Size	Document Number			Rev	
B	LA-2541			0.4	
Date:	Friday, April 15, 2005	Sheet	27	of	58

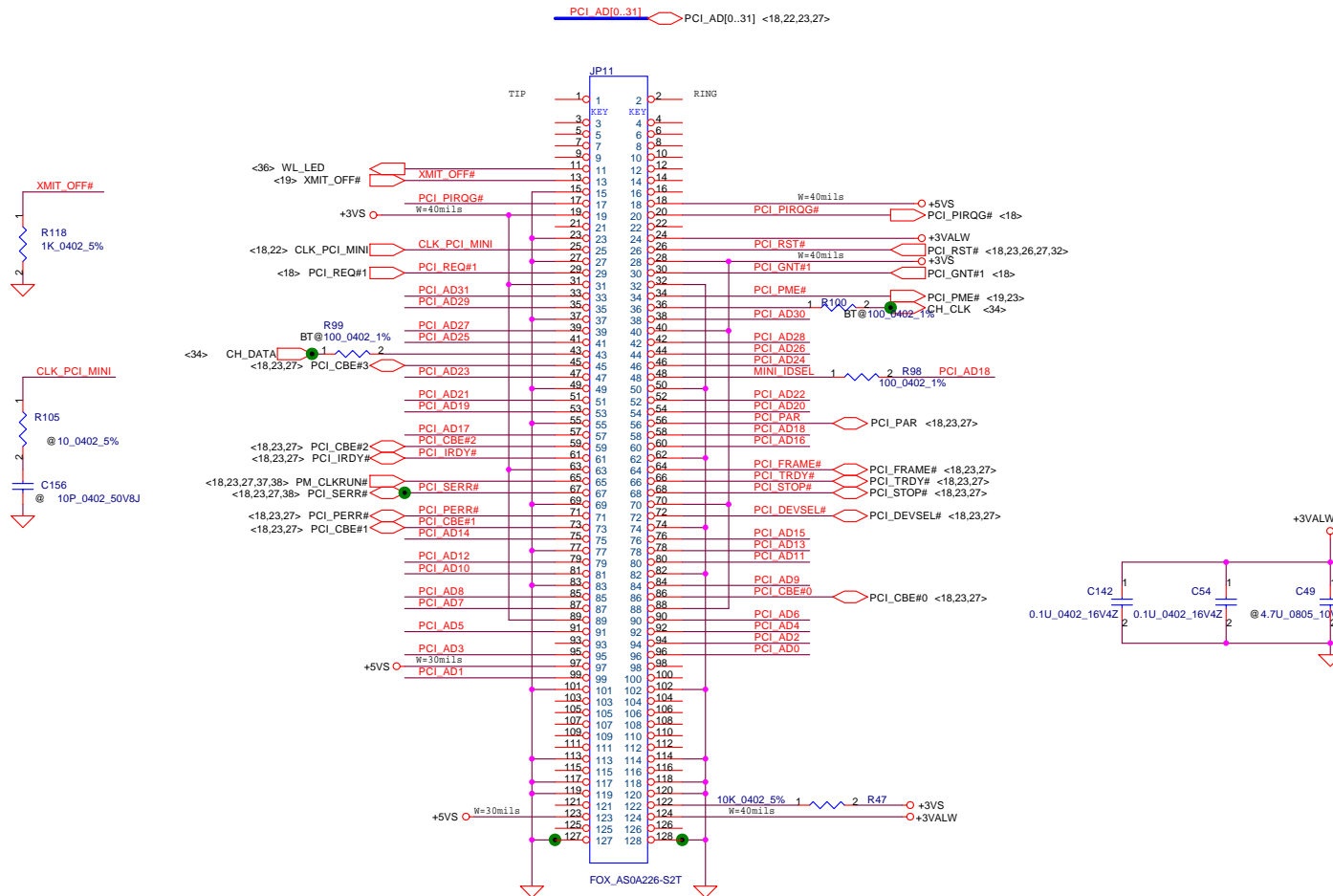
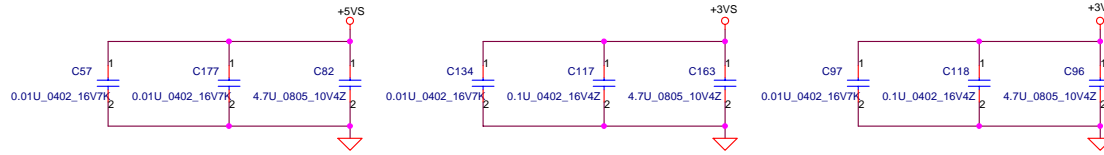


BOM change

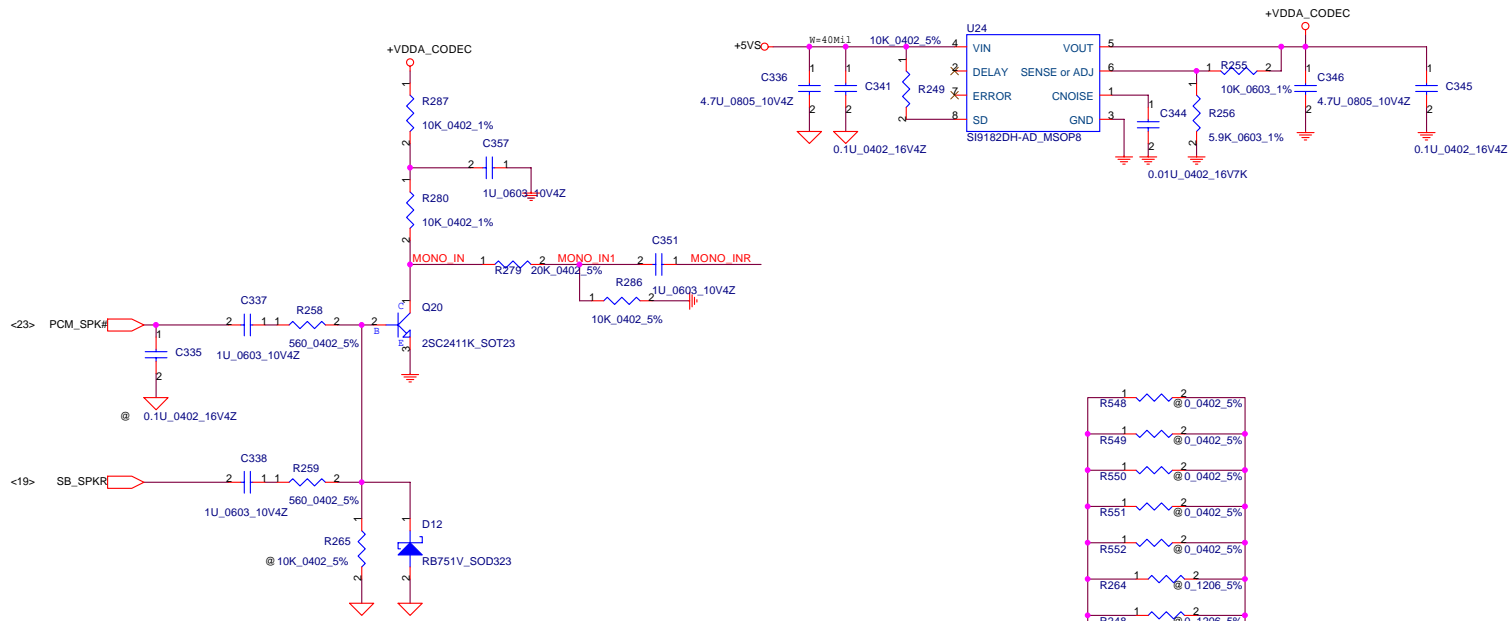


Close to NIC U6

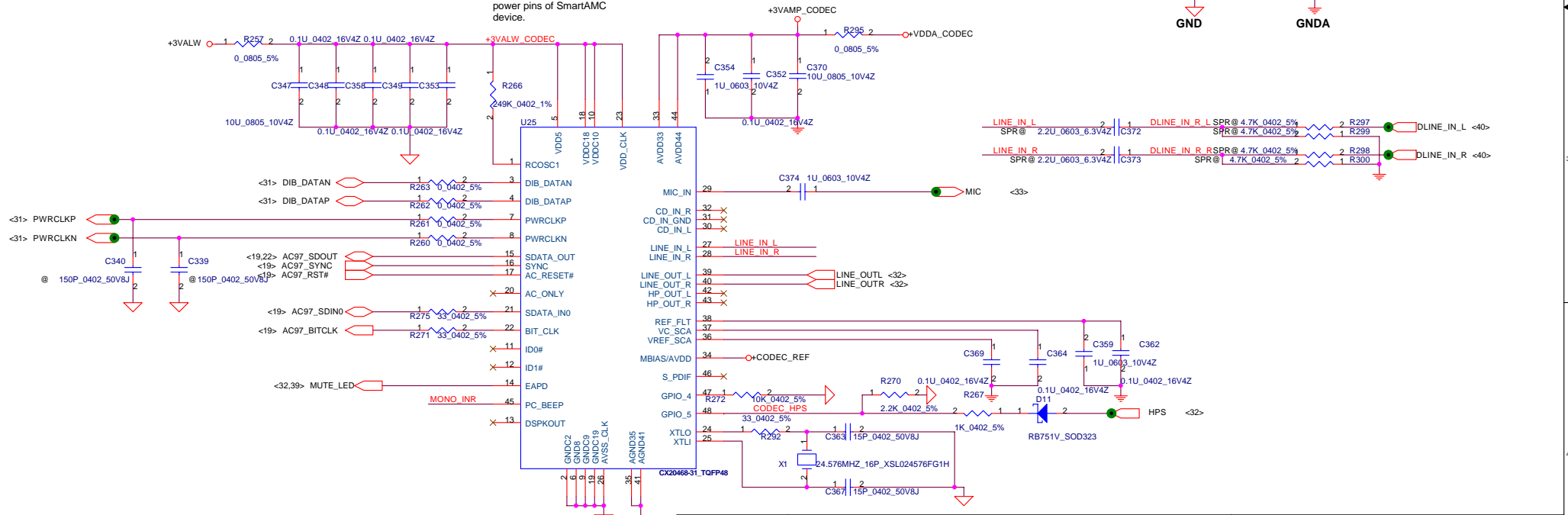
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Issued Date	2005/03/01	Deciphered Date	2006/03/11	LAN Magnetic & RJ45	
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				B	0.4
				Date:	Friday, April 15, 2005
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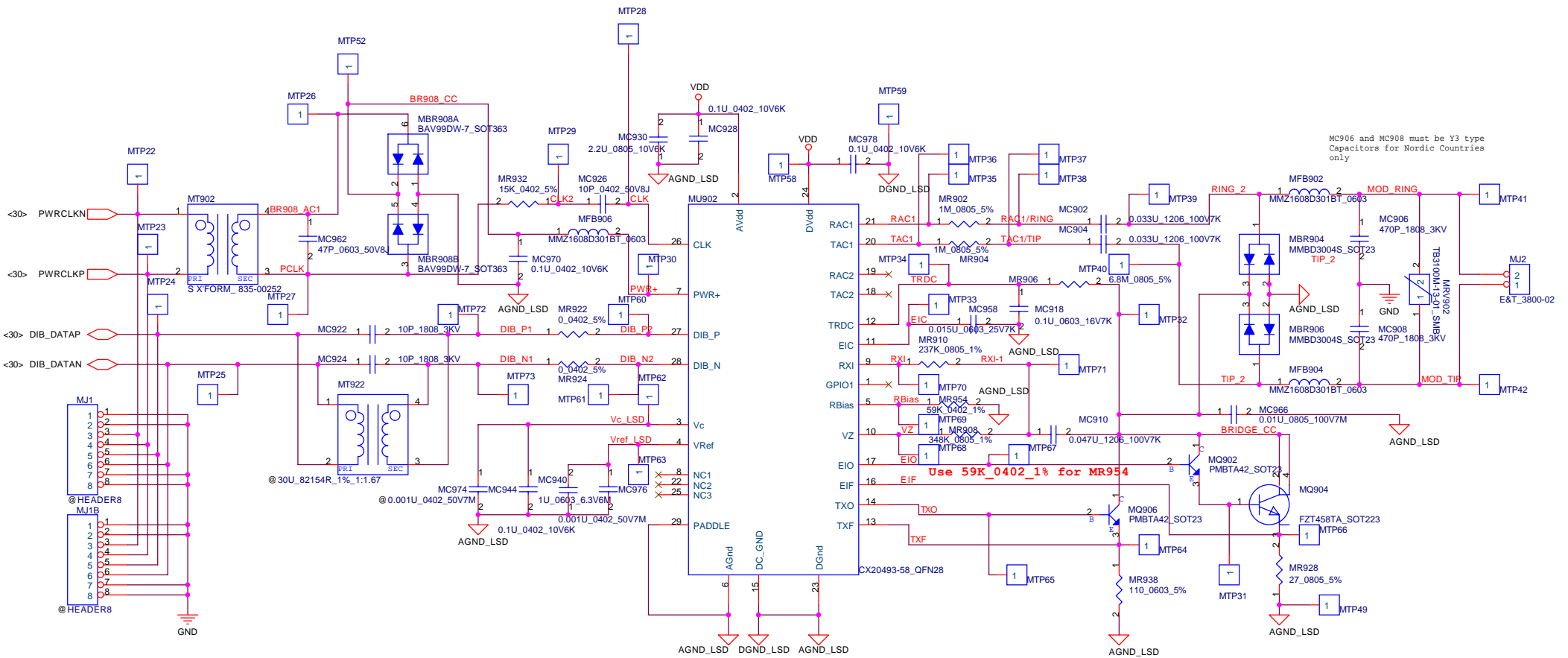
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	Mini PCI slot	
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For Layout:
Place decoupling caps near the power pins of SmartAMC device.



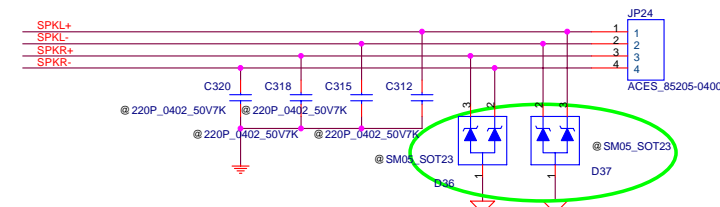
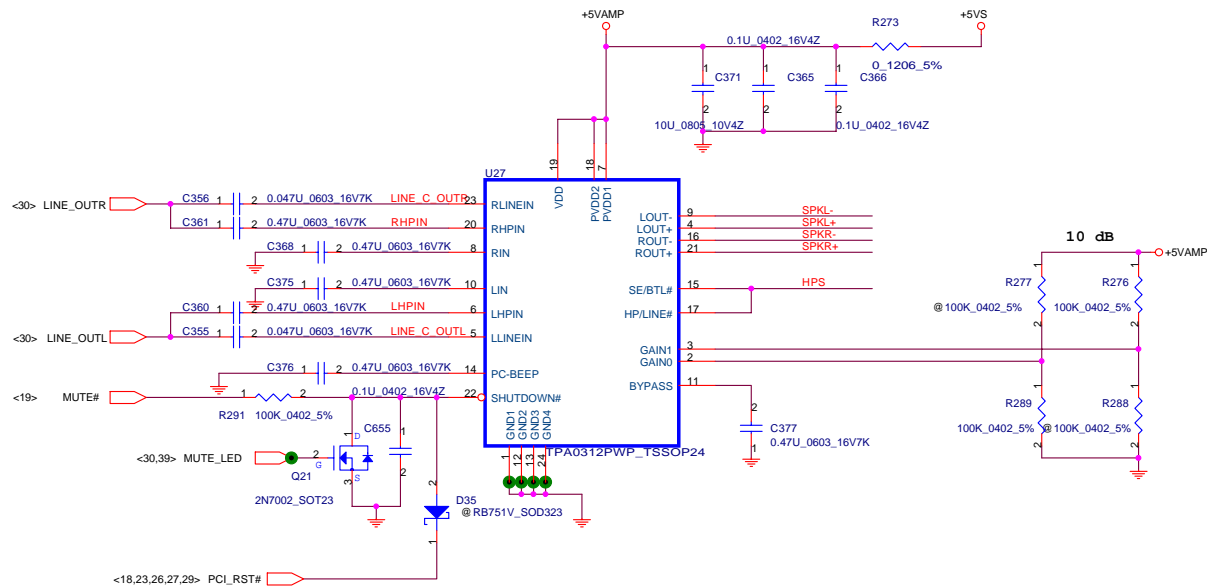
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MC906 and MC908 must be Y3 type Capacitors for Nordic Countries only

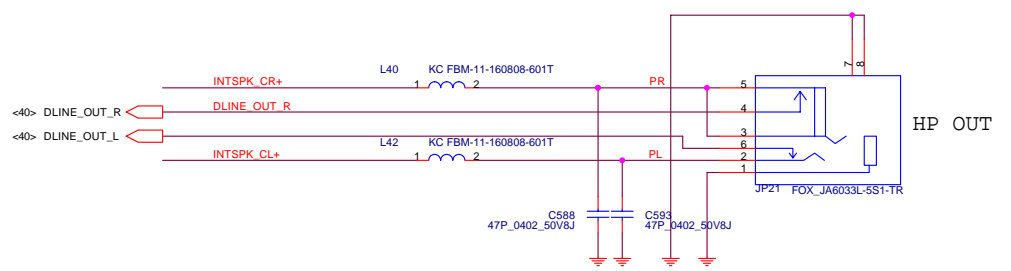
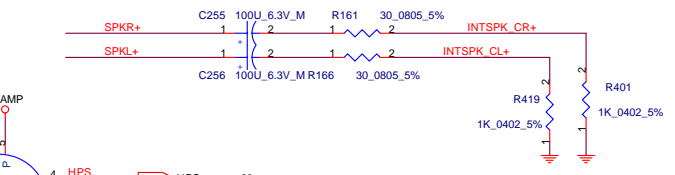
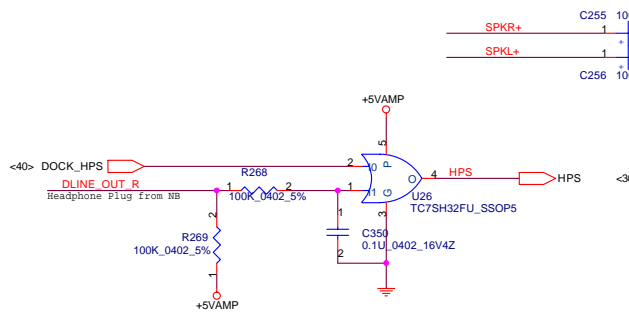
Use 59K_0402_1% for MR954

Security Classification	Compal Secret Data		Title
Issued Date	2005/03/01	Deciphered Date	2006/03/11
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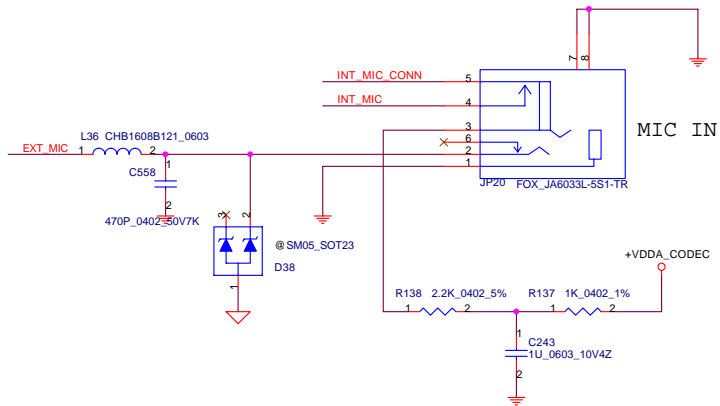
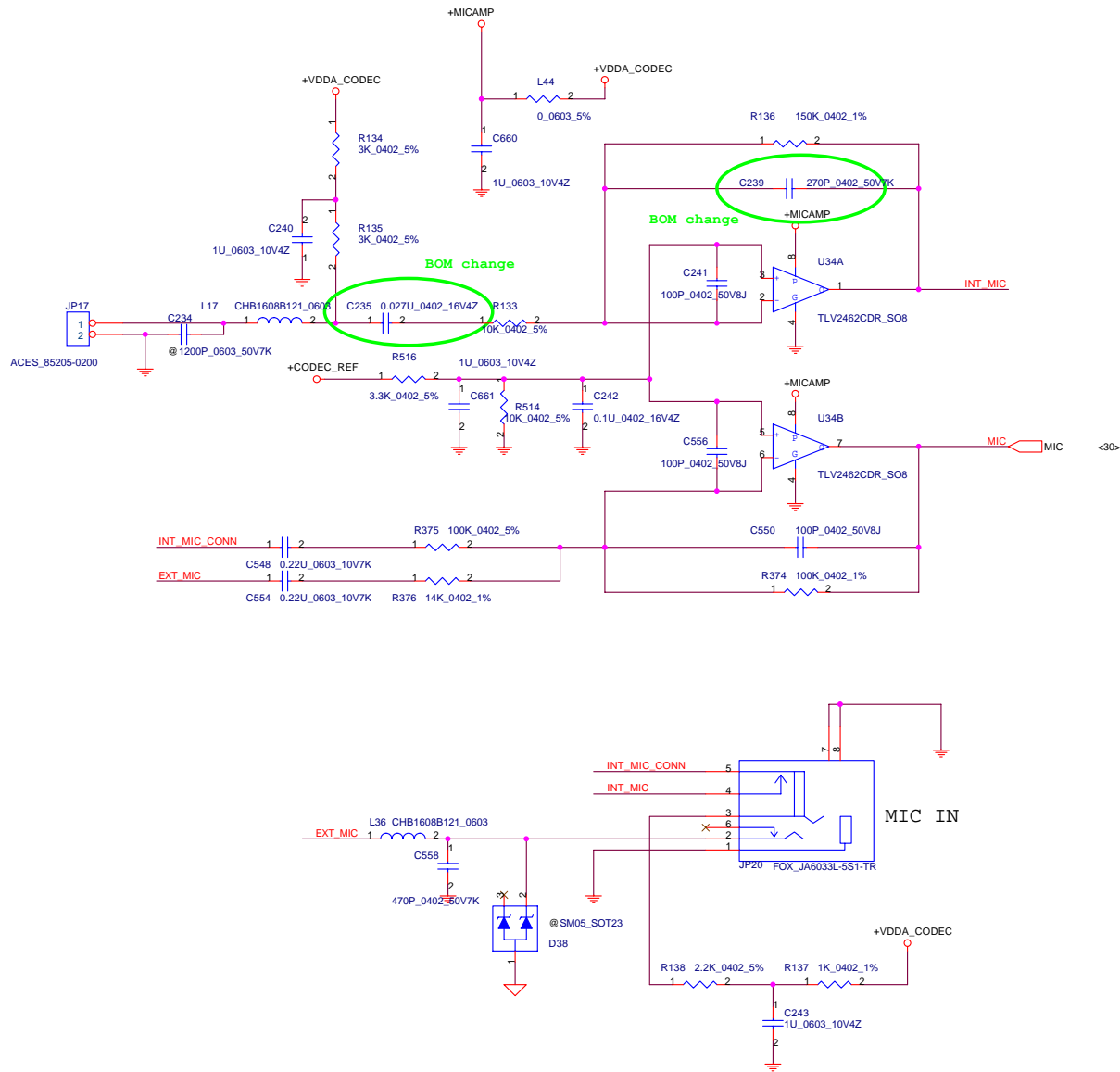
Gain Settings		
GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

HEADPHONE OUT/LINE OUT

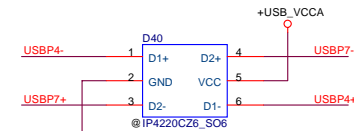
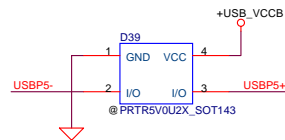
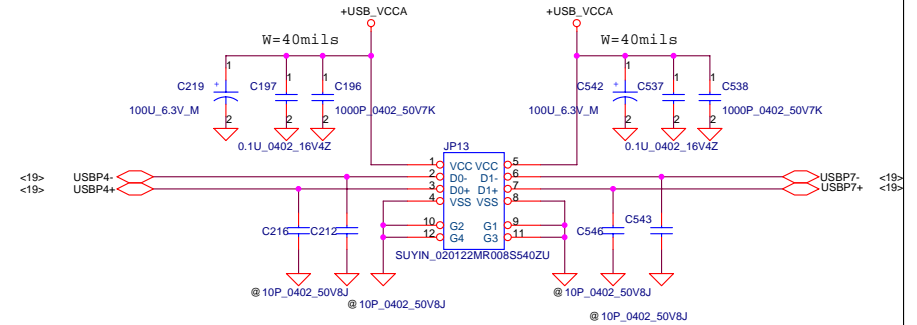
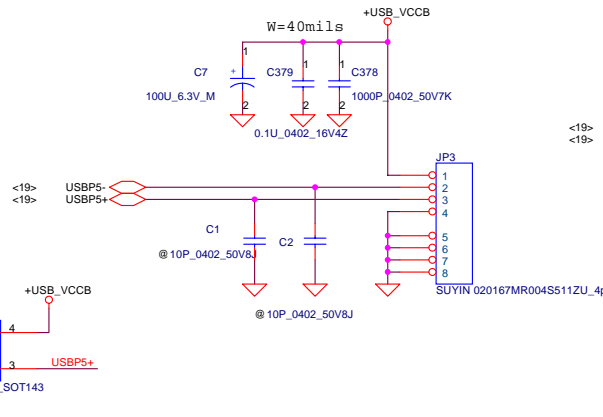
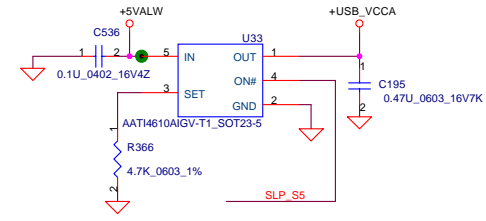
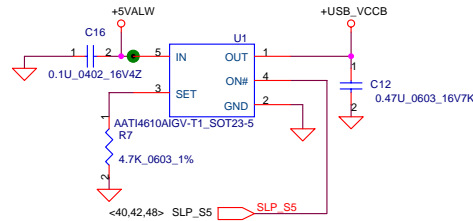


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Issued Date	2005/03/01	Deciphered Date	2006/03/11	AMP & Audio Jack	
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				Custom	LA-2541
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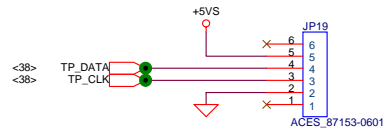
Internal/External MIC



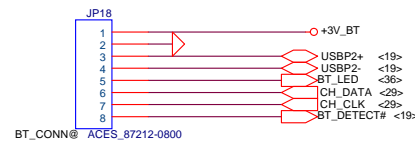
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	Internal / External MIC	
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				Custom	0.4
				Date:	Friday, April 15, 2005
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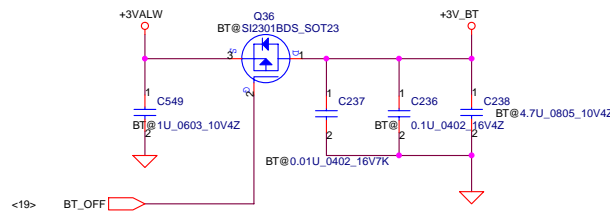
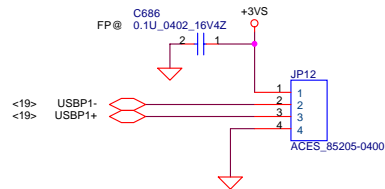
TP CONNECTOR



BT CONN.



FINGER PRINT CONN.



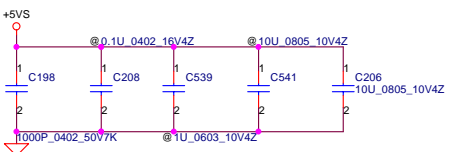
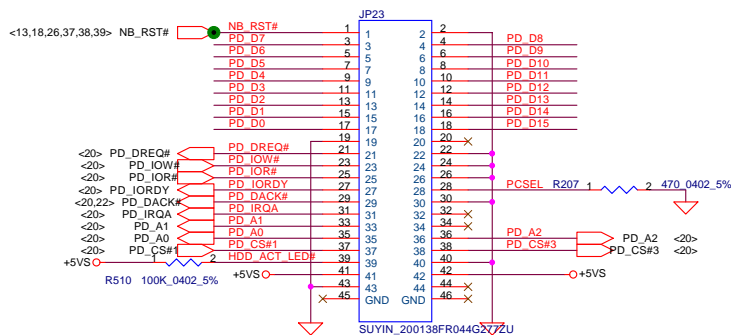
Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2006/03/11
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HDD/ODDModule

Placea caps. near HDD CONN.

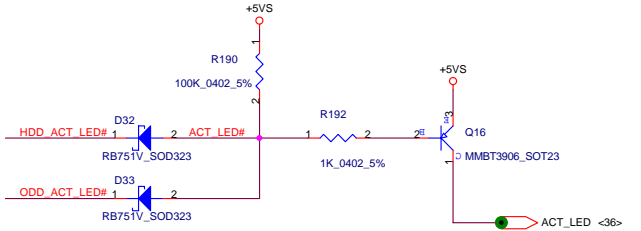
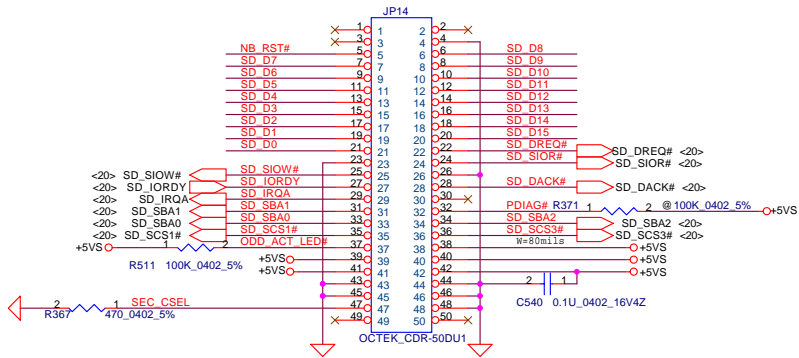


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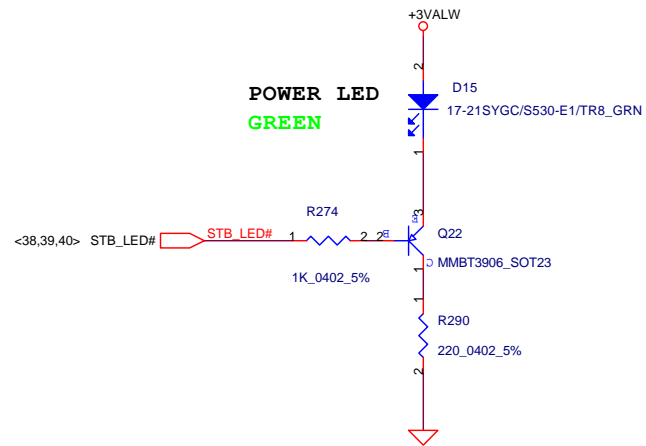
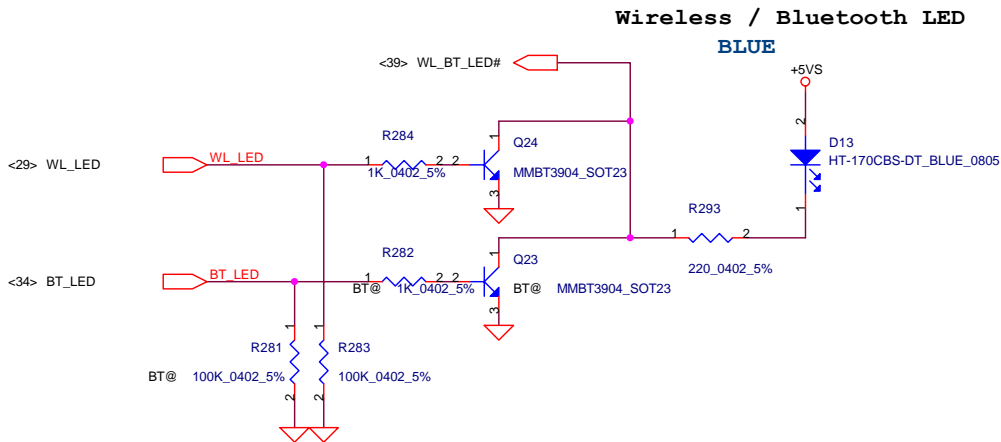
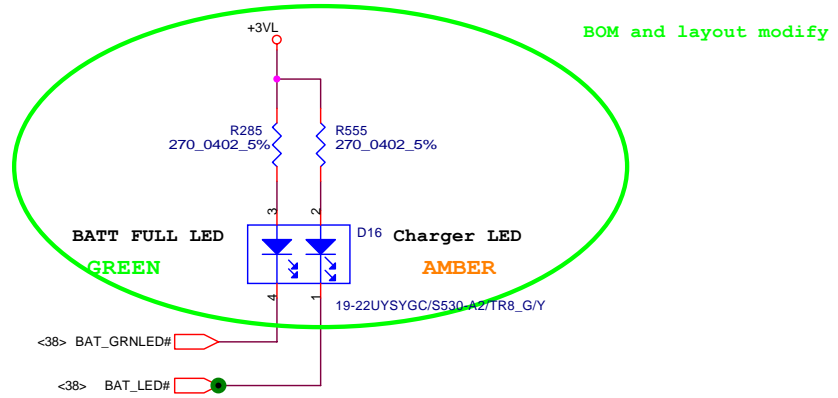
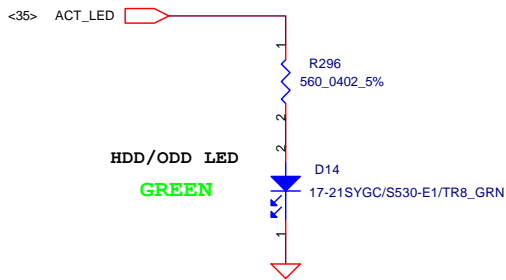


Place caps. near ODD CONN.

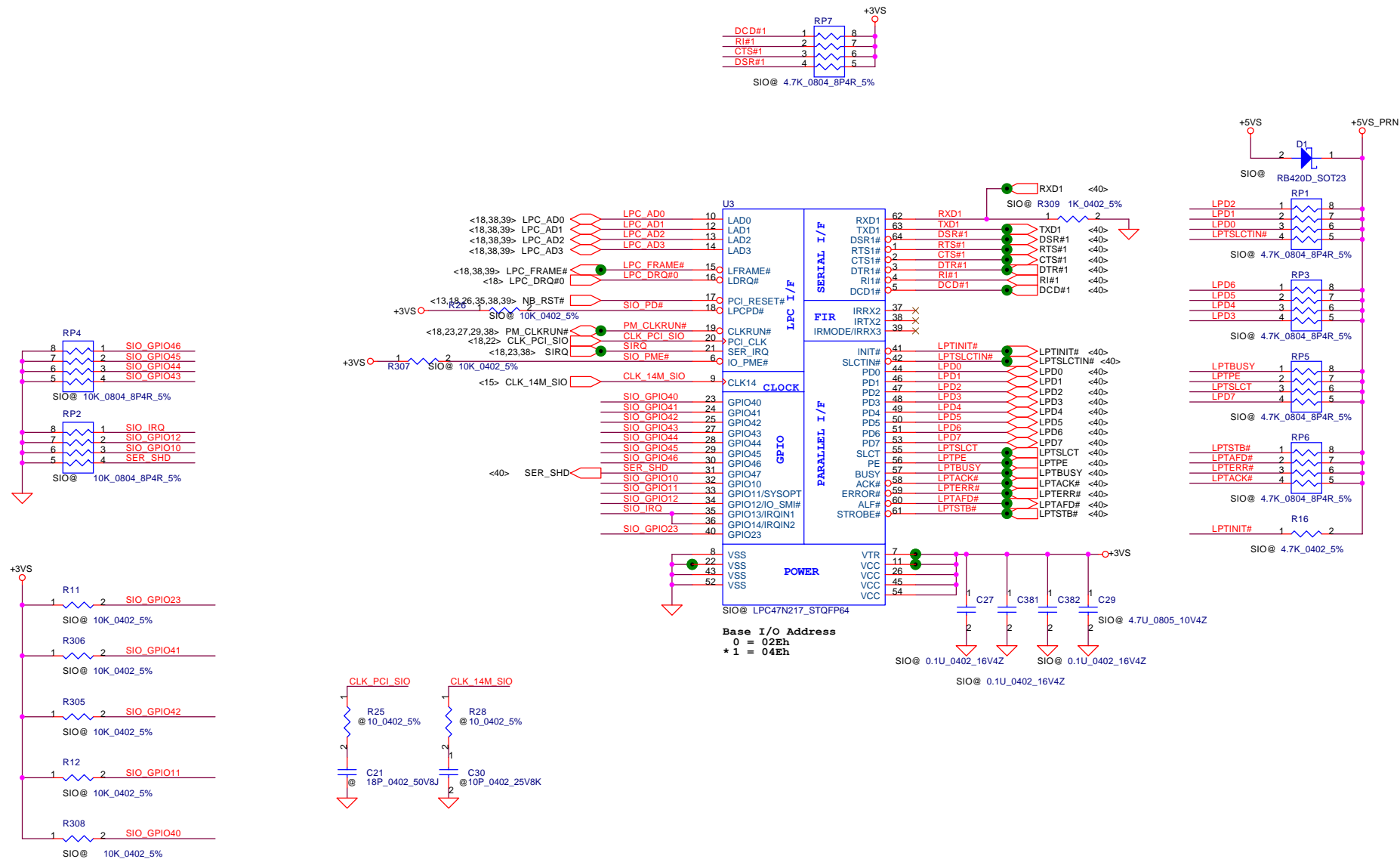
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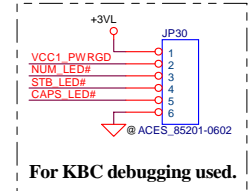
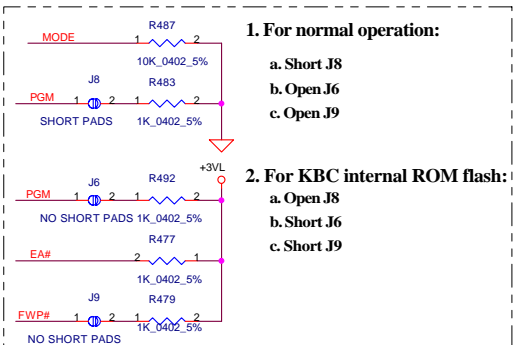
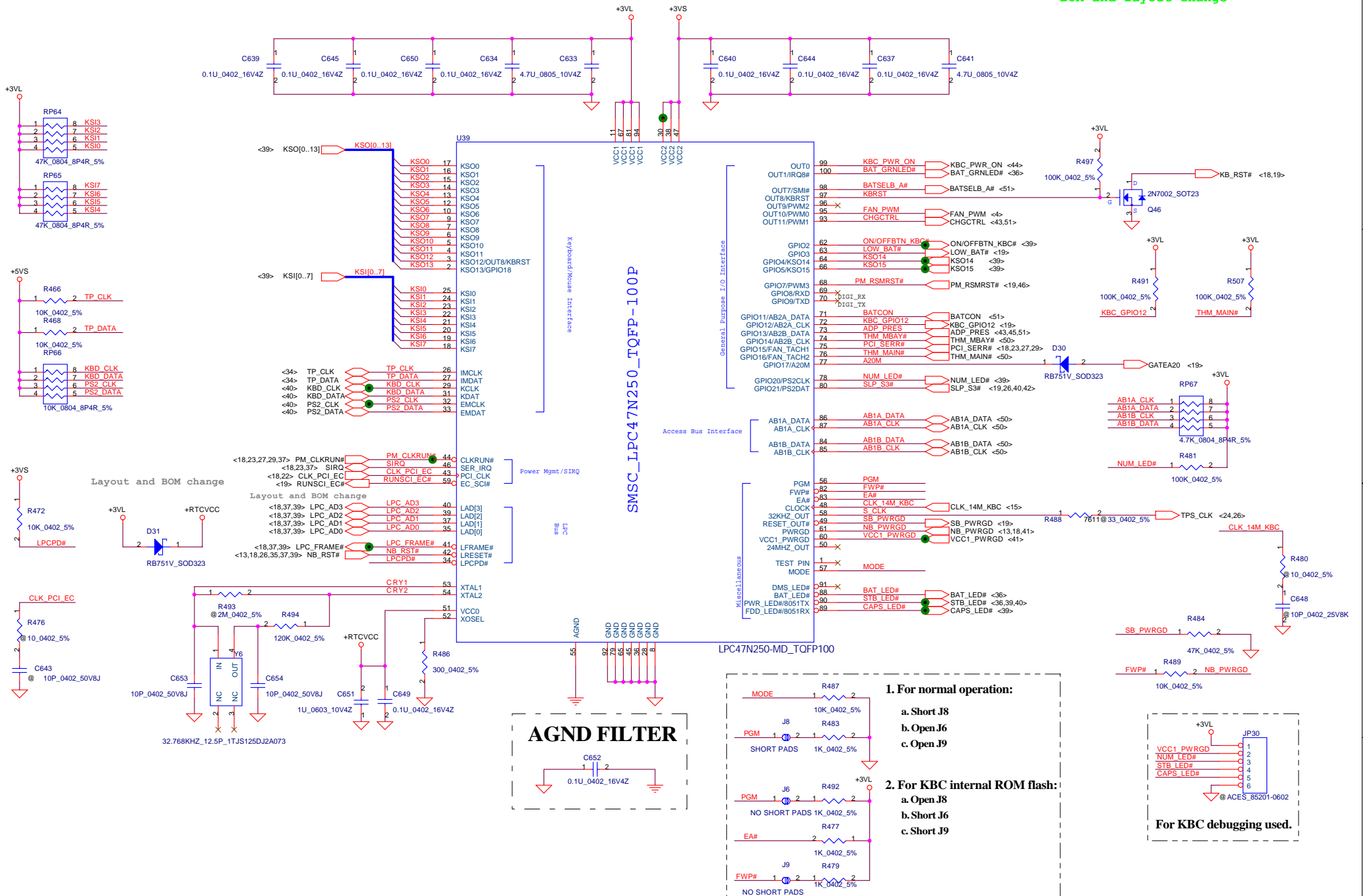
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/11	HDD / ODD connector	
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				Document Number	0.4
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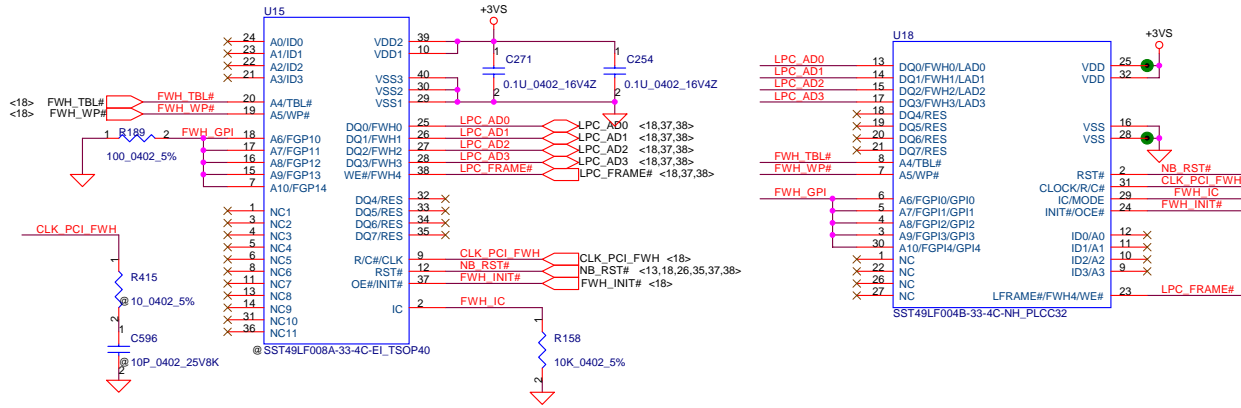


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Size	Document Number			Rev	
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Date:	Friday, April 15, 2005	Sheet	37	of	58

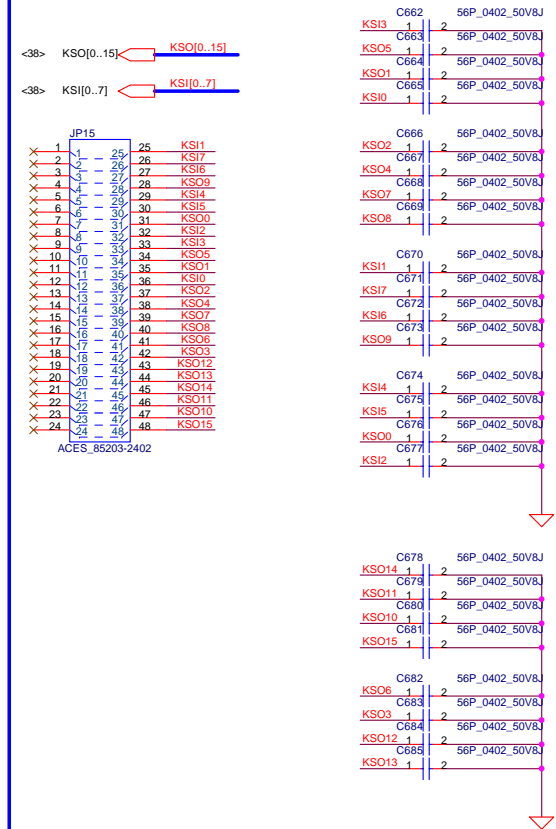


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Issued Date	2005/03/01	Deciphered Date	2006/03/11	EC LPC47N250	
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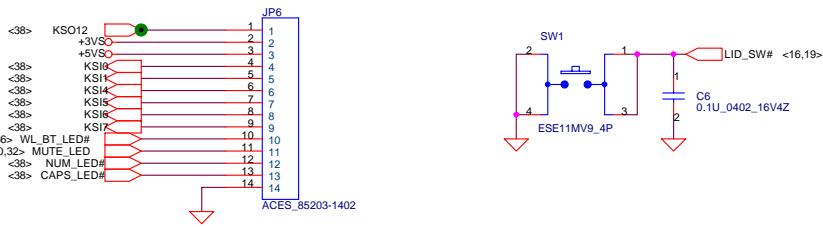
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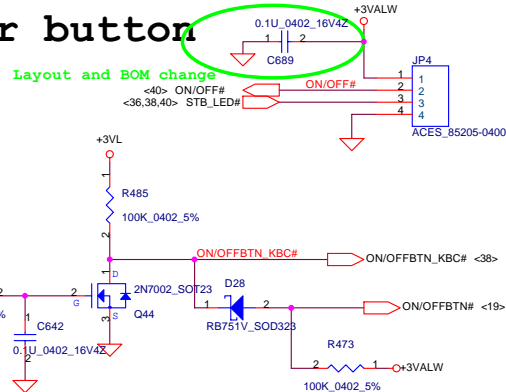
INT_KBD CONN.



Switch Board conn./ LID Switch

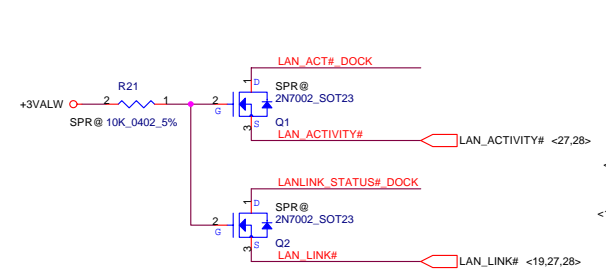
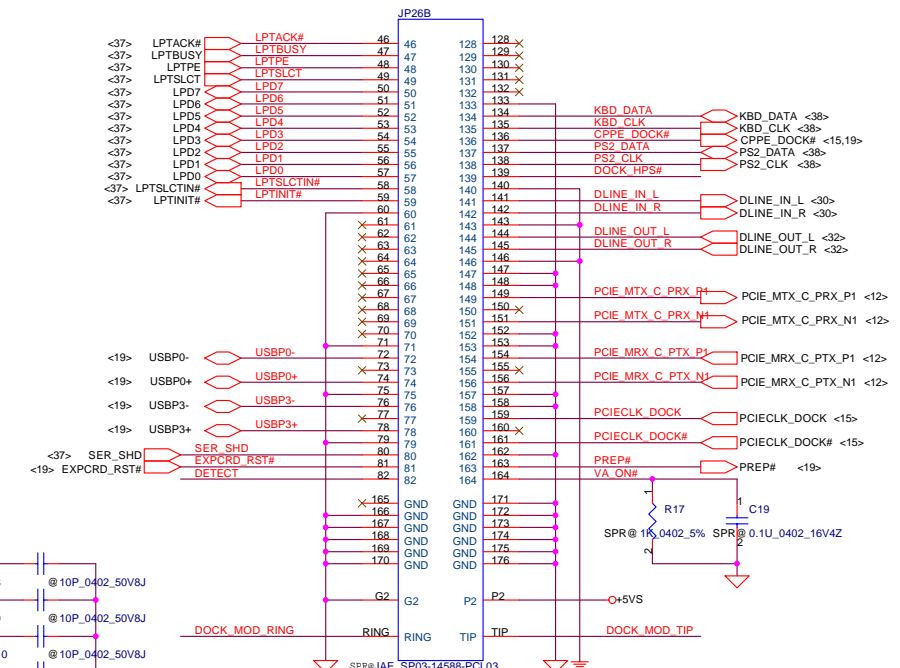
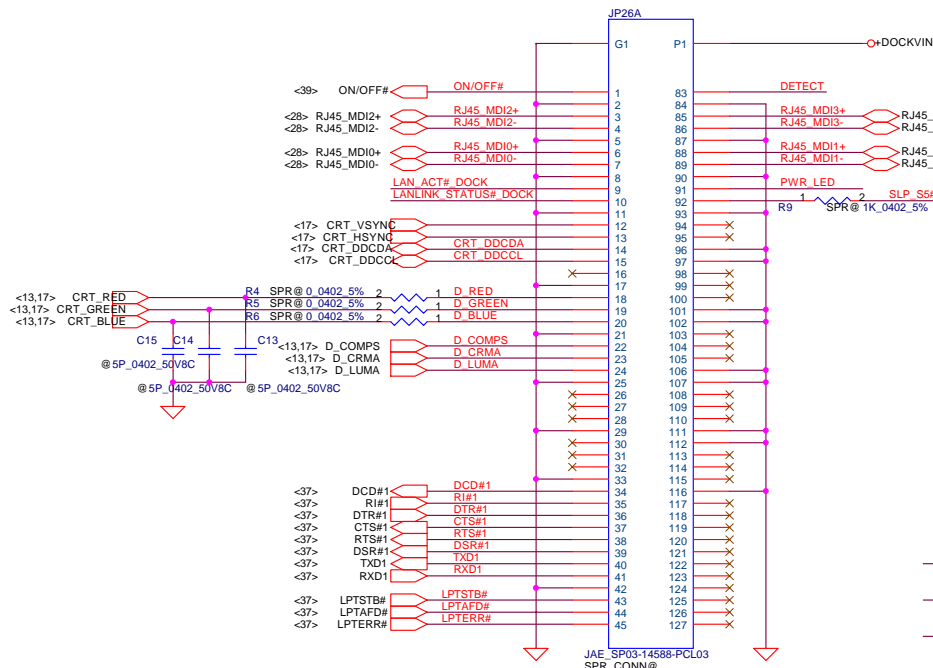
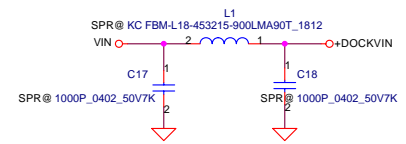


Power button



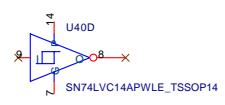
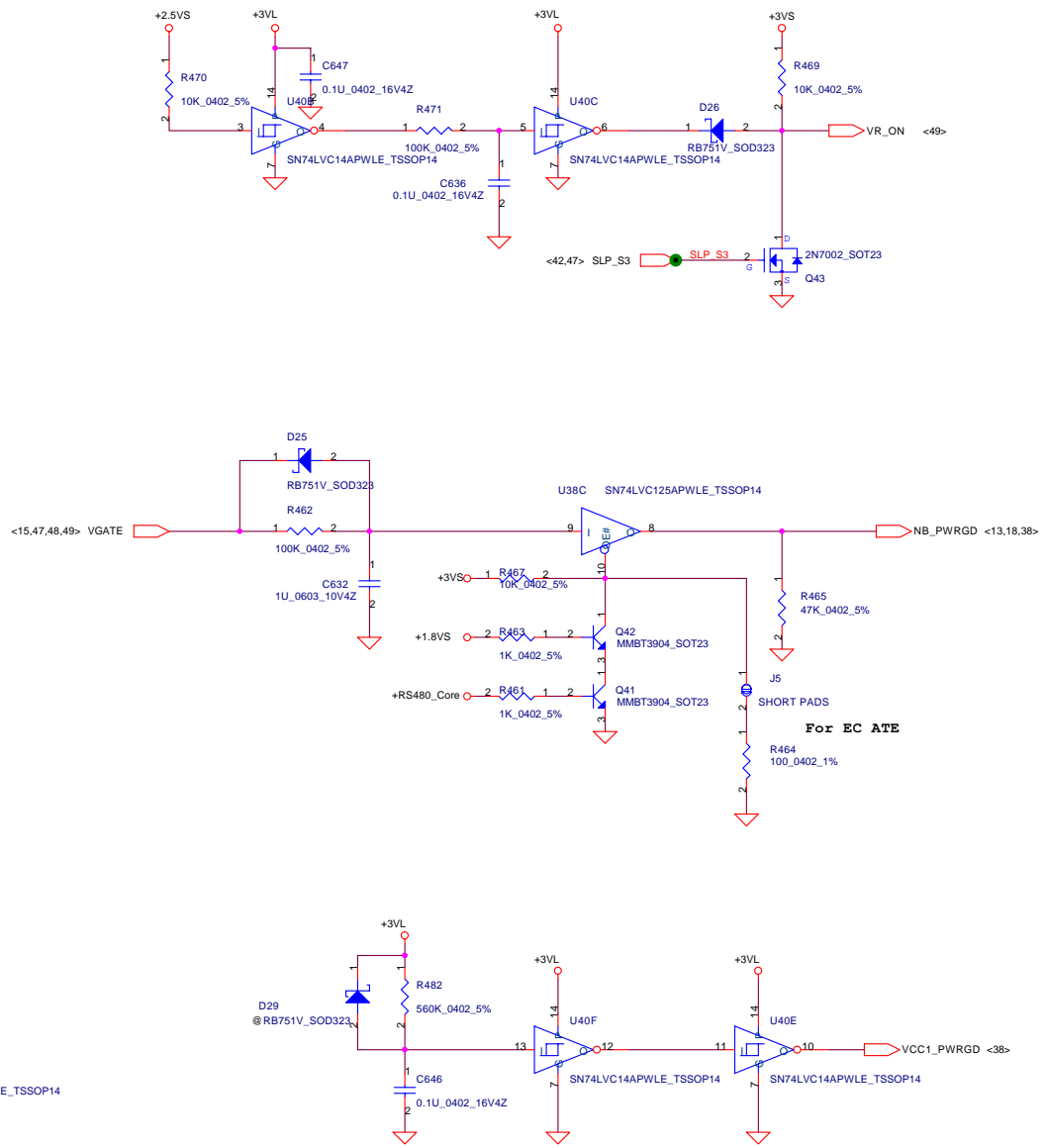
Security Classification		Compal Secret Data		Title		
Issued Date	2005/03/01	Deciphered Date	2006/03/11	BIOS BOM/SW BD CONN/KB CONN		
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DOCK CONN. 184PIN



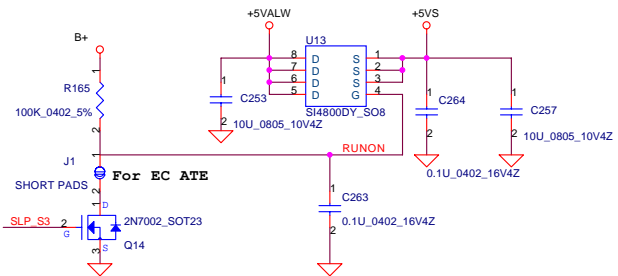
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Title			
SPR Connector			
Size	Document Number	Rev	
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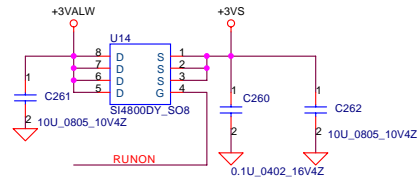


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Issued Date	2005/03/01	Deciphered Date	2006/03/11	Power OK	
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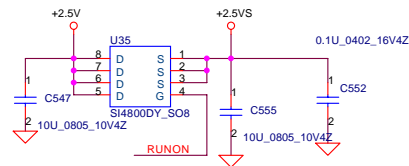
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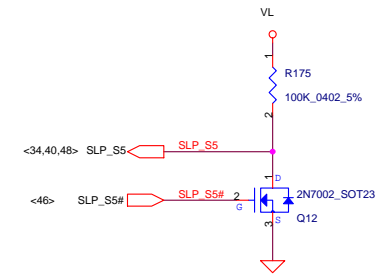
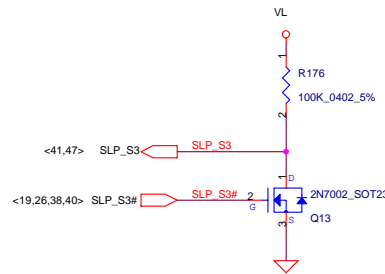
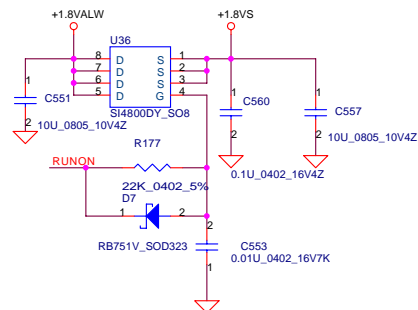
+3VALW to +3VS Transfer



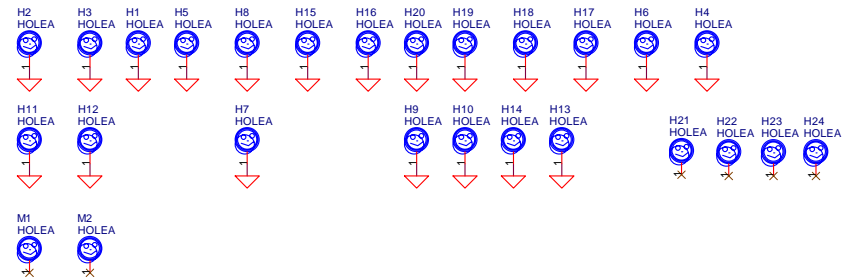
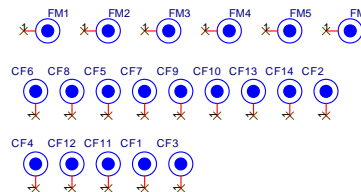
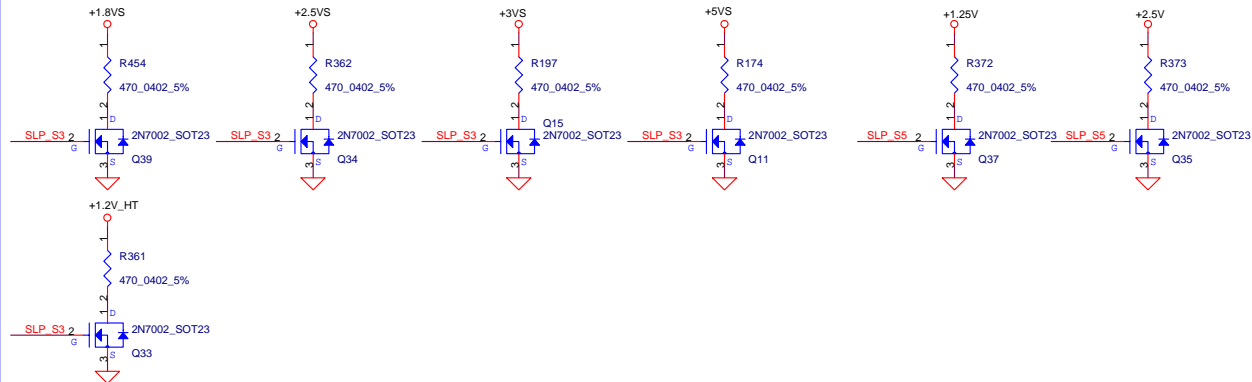
+2.5V to +2.5VS Transfer



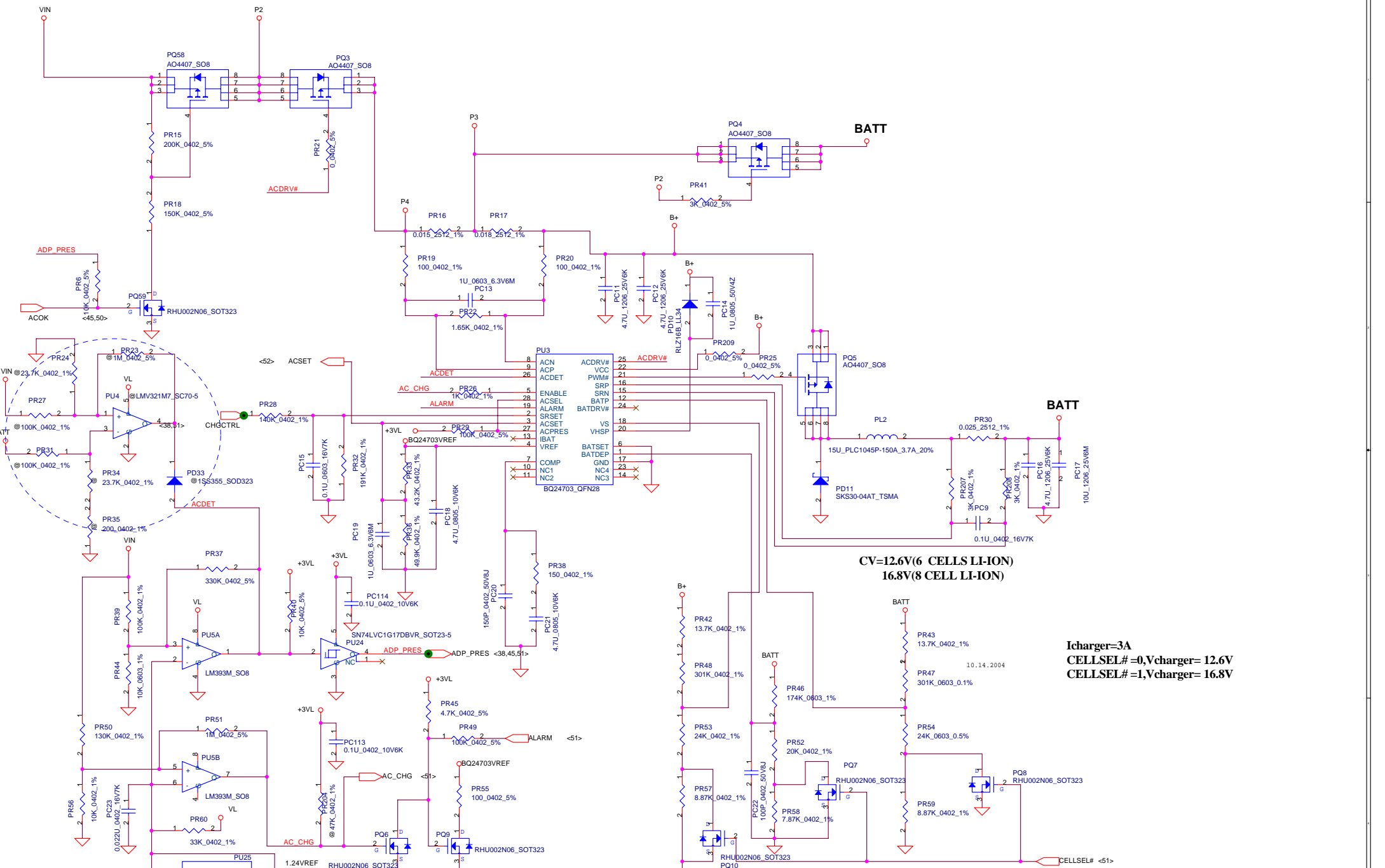
+1.8VALW to +1.8VS Transfer



Discharge circuit



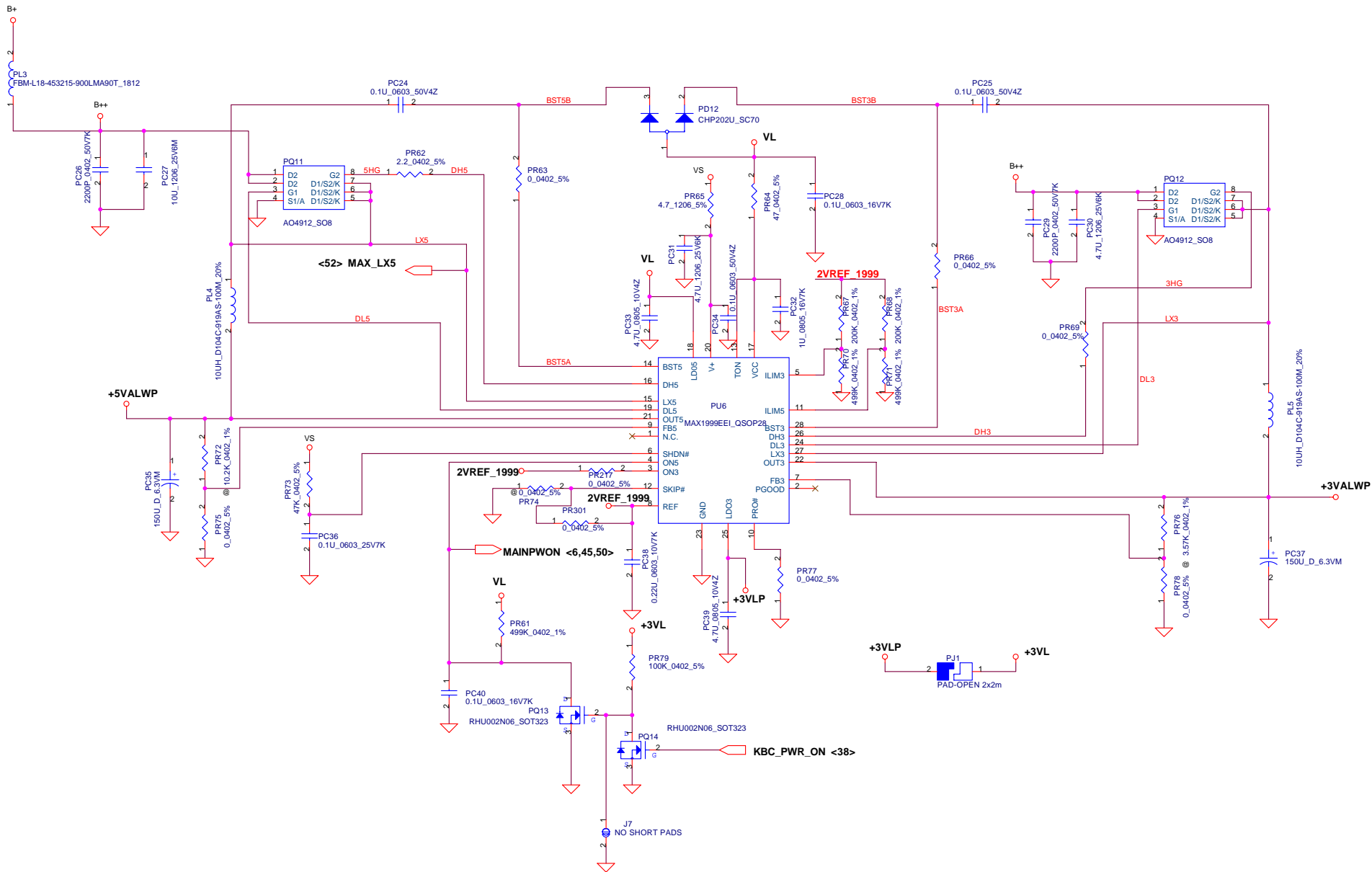
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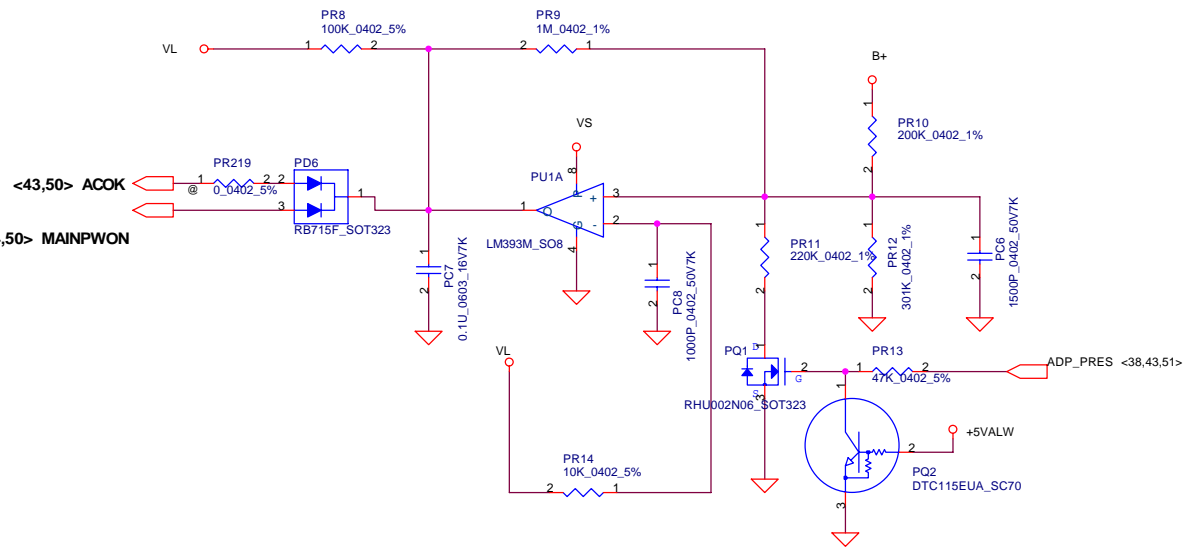
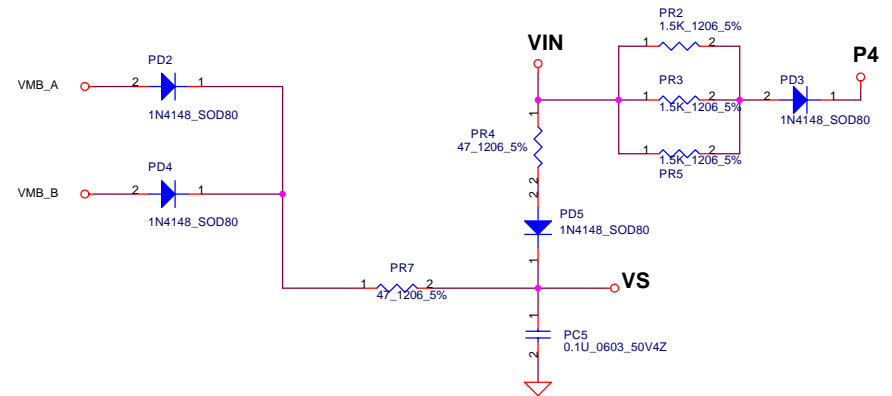
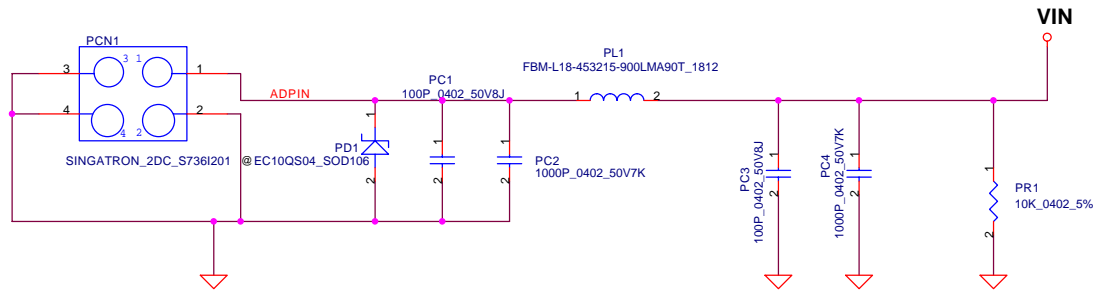
CV=12.6V(6 CELLS LI-ION)
16.8V(8 CELL LI-ION)

Icharger=3A
CELLSEL#=0,Vcharger= 12.6V
CELLSEL#=1,Vcharger= 16.8V

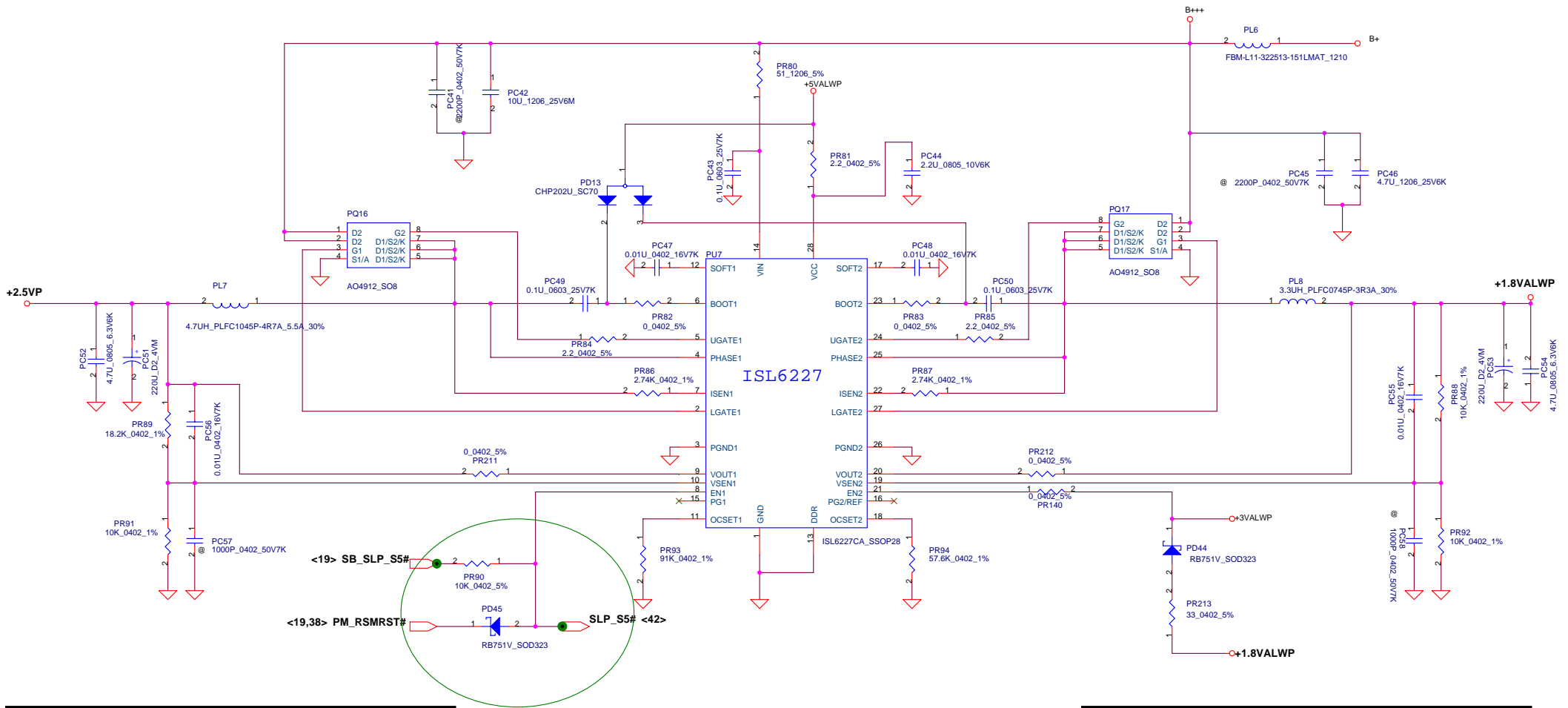
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				Rev	0.4
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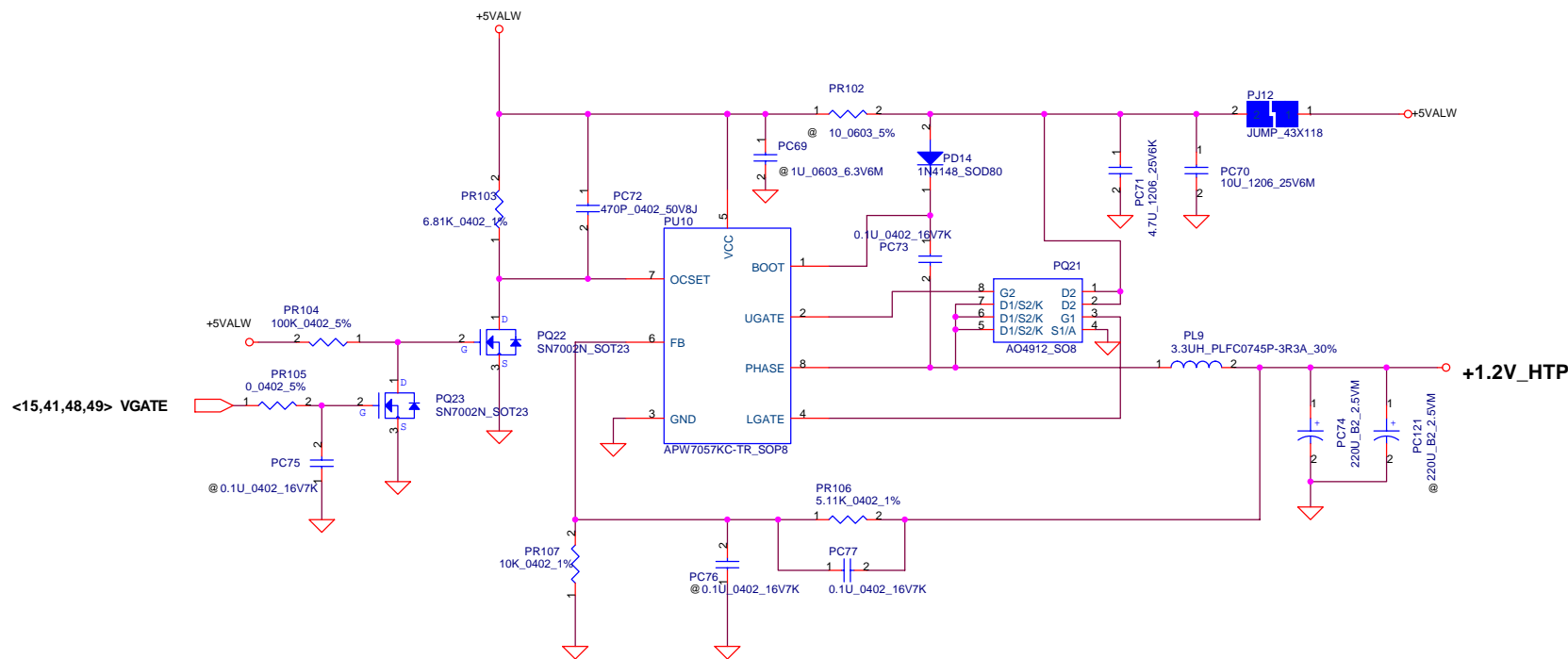
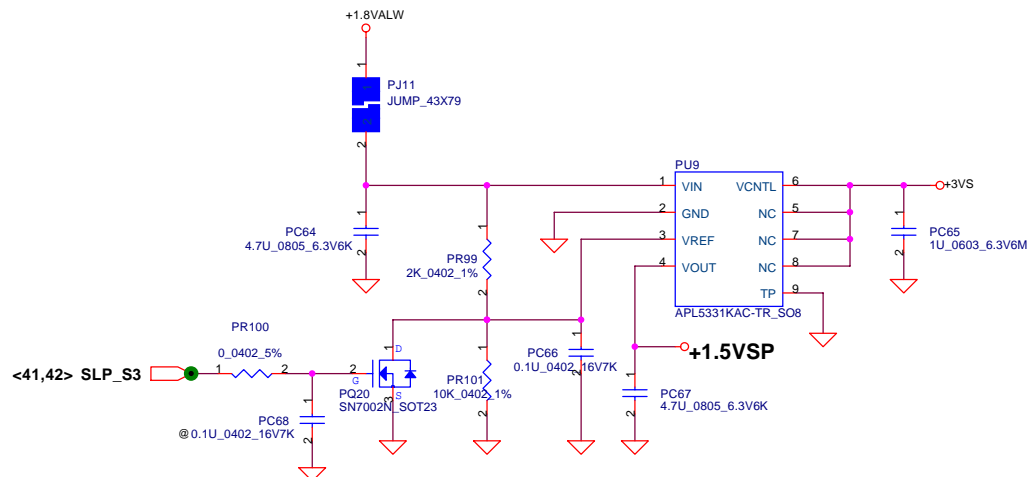
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Issued Date	2005/03/01	Deciphered Date	2006/03/01	DCIN / Pre-Charge	
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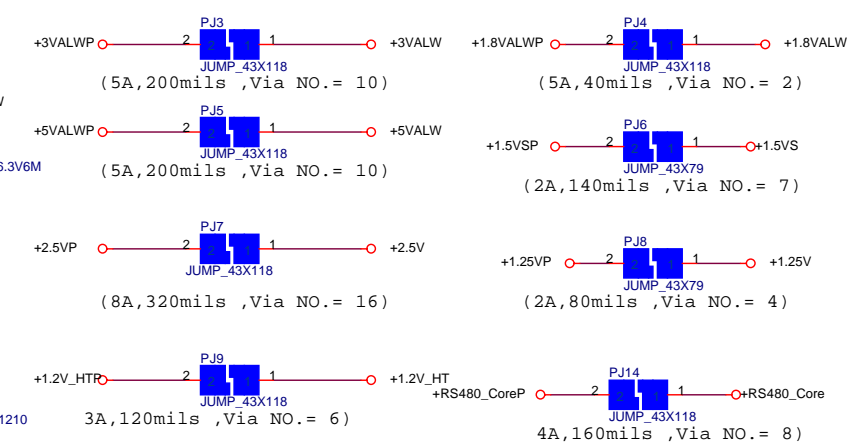
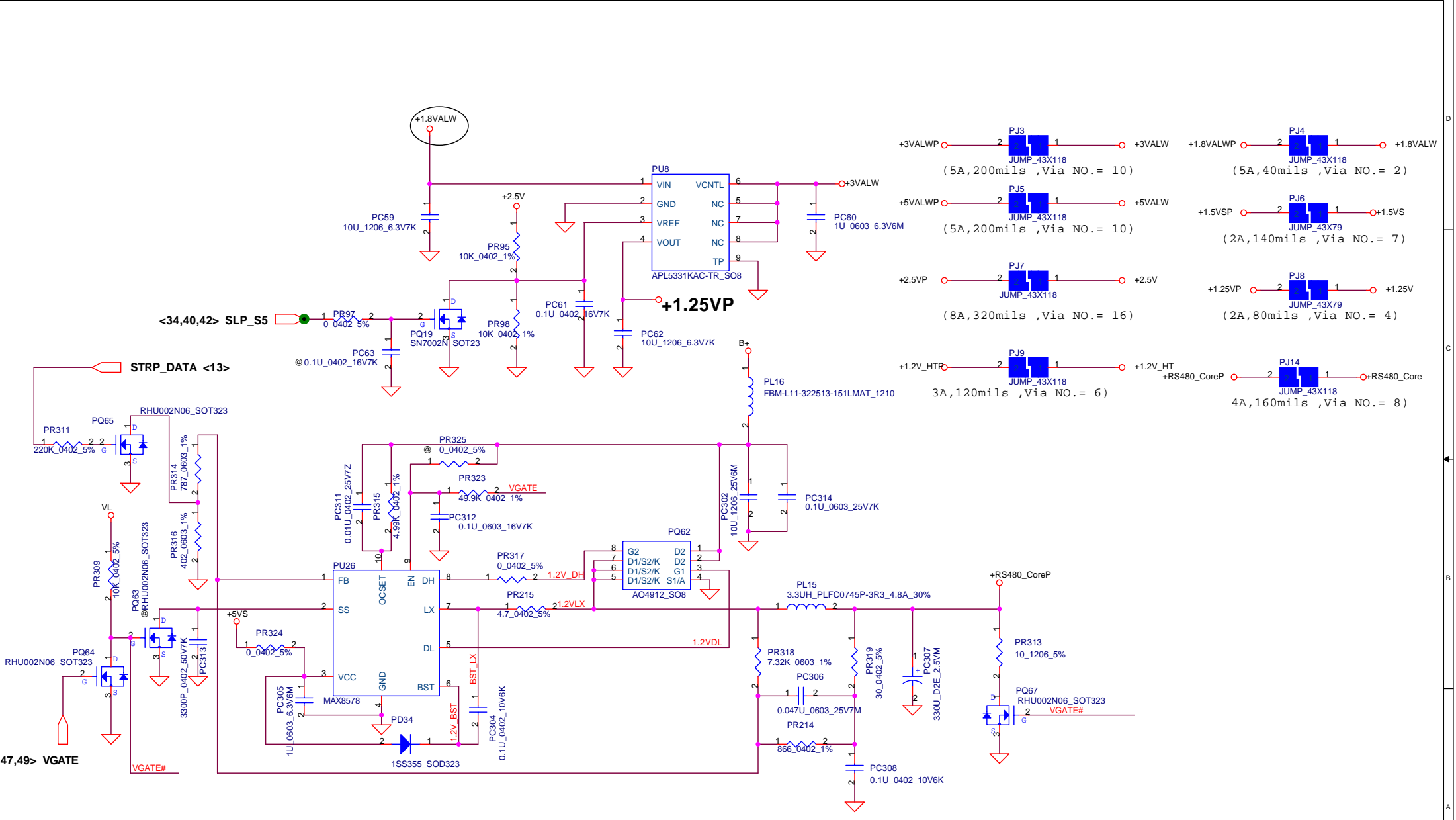
$I_{limit} = (10.3 - 8\mu A \cdot R_{limit}) \cdot (R_{sense} + 140) / (R_{sense} \cdot R_{ds})$
 $R_{sense} = 1K, R_{ILM} = 51K, R_{ds(on)} \text{ tpy.} = 19.7m\Omega, \text{Max} = 24m\Omega$
 $I_{limit \text{ Min}} = 9.6 / 51K \cdot (100 + 1K) / (24m\Omega \cdot 1.3) = 6.636A$
 $I_{limit \text{ Max}} = 9.6 / 51K \cdot (100 + 1K) / 19.7m\Omega = 10.897A$
 $+VCCP \text{ O.C.P.} = 6.636A \sim 10.897A$

$I_{limit} = (10.3 - 8\mu A \cdot R_{limit}) \cdot (R_{sense} + 140) / (R_{sense} \cdot R_{ds})$
 $R_{sense} = 2K, R_{ILM} = 107K, R_{ds(on)} \text{ tpy.} = 19.7m\Omega, \text{Max} = 24m\Omega$
 $I_{limit \text{ Min}} = 9.6 / 107K \cdot (100 + 2K) / (24m\Omega \cdot 1.3) = 6.0388A$
 $I_{limit \text{ Max}} = 9.6 / 107K \cdot (100 + 2K) / 19.7m\Omega = 9.564A$
 $+VCCP \text{ O.C.P.} = 6.038A \sim 9.564A$

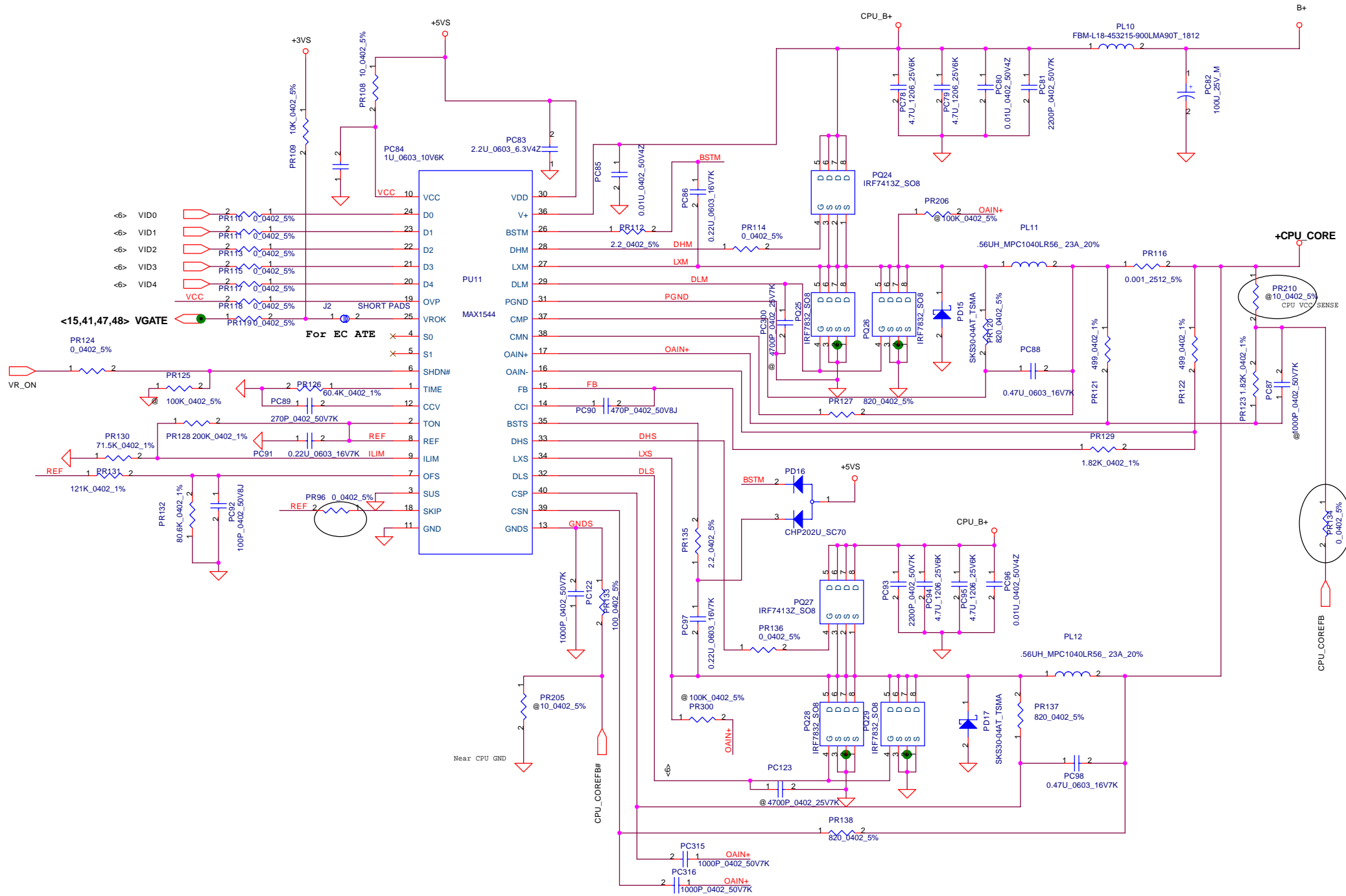
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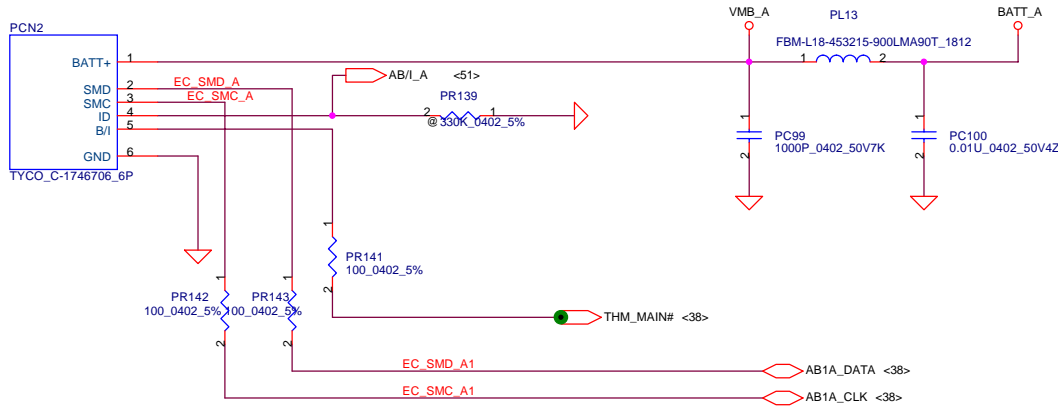
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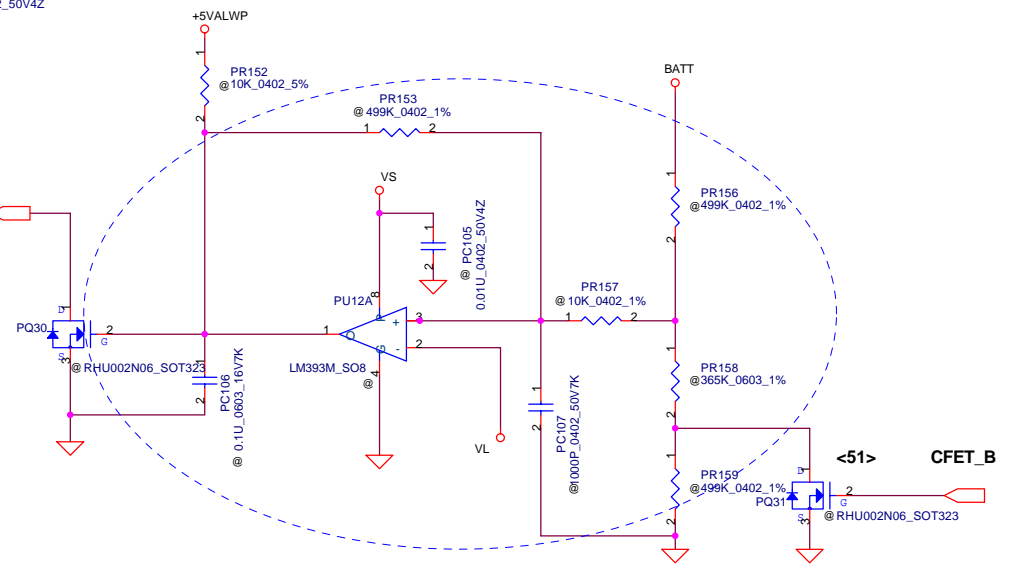
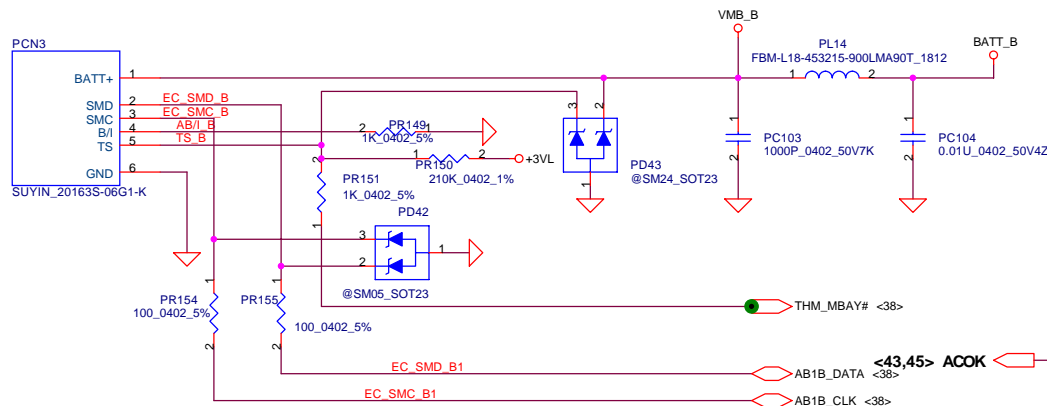
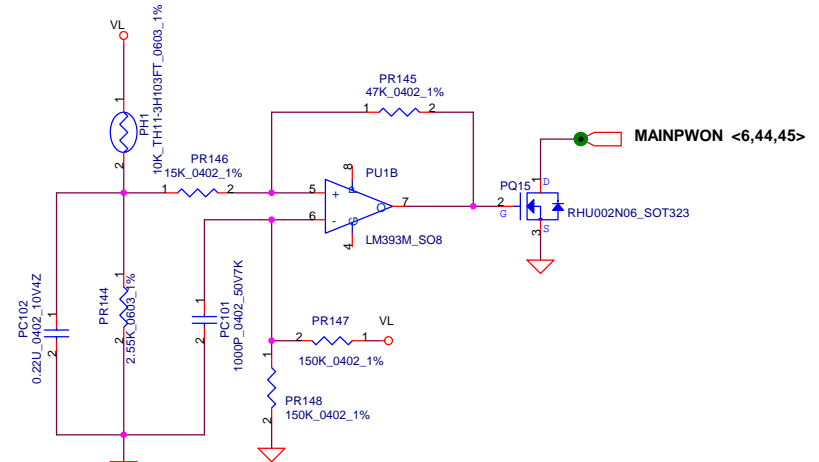
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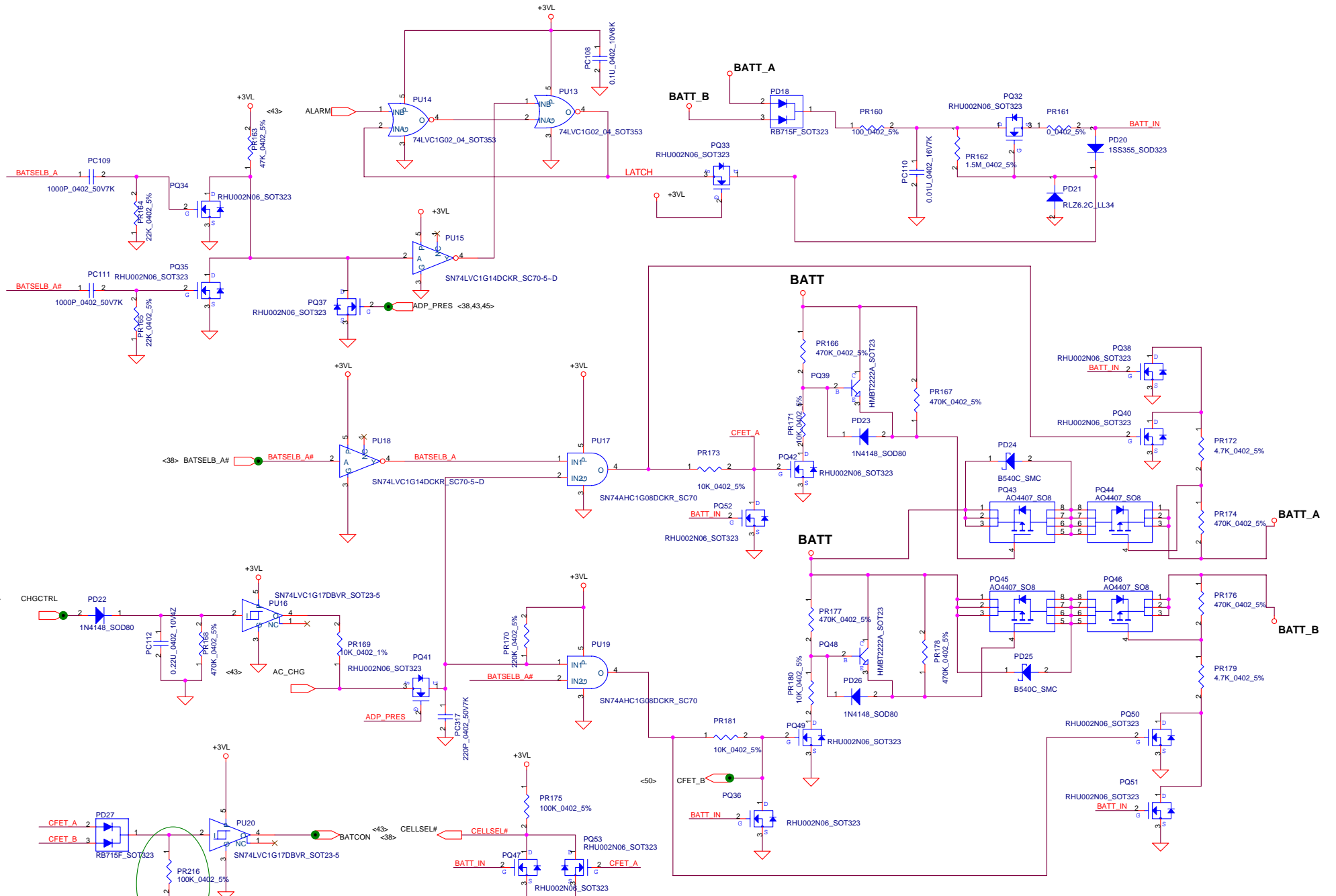
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Issued Date	2005/03/01	Deciphered Date	2006/03/01	+CPU_CORE	
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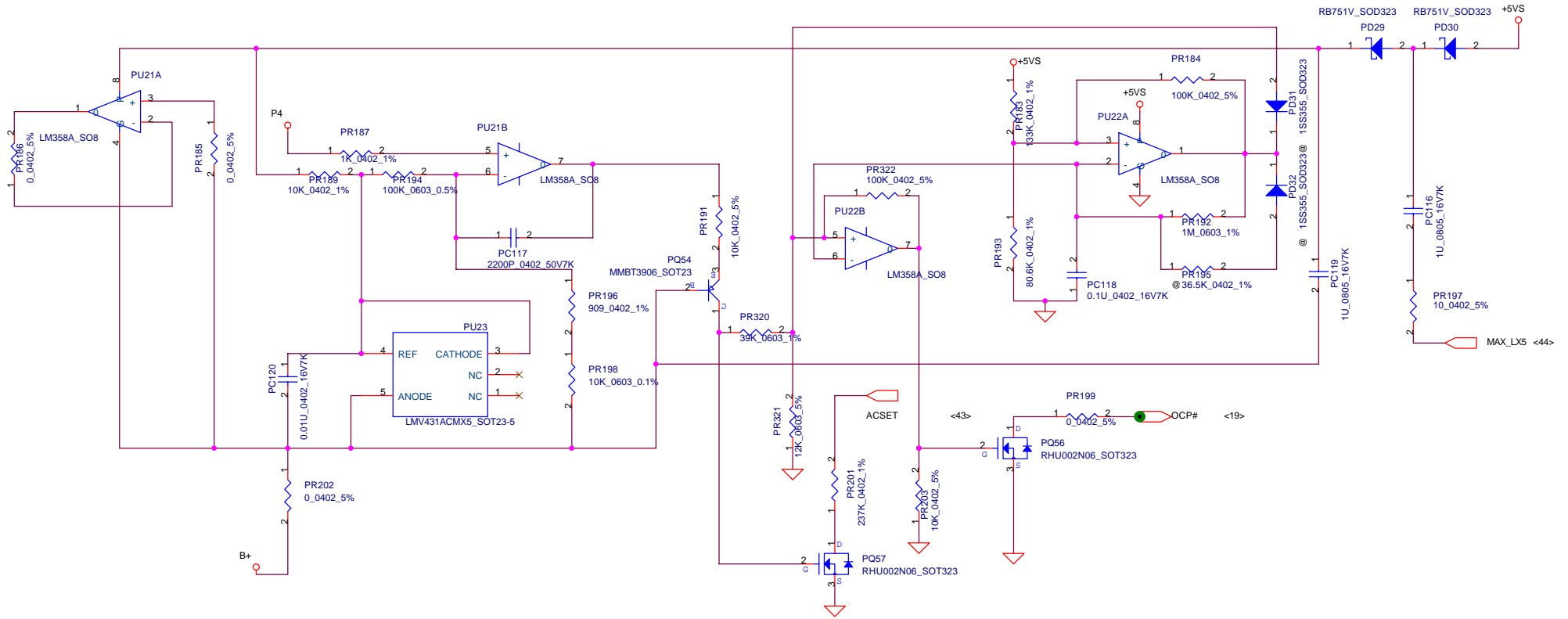
PH1 near CPU :
PCBA thermal protection at 90 degree C
Recovery at 45 degree C



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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	CHARGER	08/17/2004 (DB)	HP	The reason for the change is reslove the timing diff between two compator for AC detect	add PQ33	DB
2	41	CHARGER	08/17/2004 (DB)			Change PR16 to 15m ohm ,change PR17 to 18m ohm change PR30 to 25m ohm. add PR207,PR208,PC9	DB
3	41	CHARGER	08/26/2004 (DB)	HP		add a PC113 4.7uF cap for +3VL and add PC114 a 4.7uF cap for VL. Both caps can be non-installed	DB
4	46	RS480_Core	10/14/2004 (SI-1)	HP	To implement PS480 power play	add PU26 (MAX8576) ,PQ62 (AO4912) ,PL15,PC307,	SI
5	48	Battery CONN	10/14/2004 (SI-1)	HP	To change main battery CONN. pin define for supporting NiMH battery (10/20-Cancel the design change,don't support the NiMH battery)		SI
6	45	1.8VALWP	11/1/2004 (SI-1)	HP	To add 1.8VALWP discharge circuit	add PD44,PR213	SI
7	46	RS480_Core	12/27/2004 (SI2)	HP	To set RS480_Core(1.0V) from 1.04V to 1.0V	Change PR314 from 750ohm to 787ohm , PR316 from 255ohm to 402ohm	SI2
8	50	Battery Selector	12/27/2004 (SI2)	HP		Add PR216 (100k) to connect PU20 pin2	SI2
9	45	2.5V	12/27/2004 (SI2)	HW		add PD45	SI2
10	51	OCP	2/21/2005 (PV)	HP	To change the work mode of OCP function	Remove PR182,PR188,PR190,PR200,PQ55 add PR320,PR321,PR322	PV
11	44	CHARGER	4/7/2005 (MV)	HP	Airline with travel battery issue	Remove PU4,PD33,PR23,PR24,PR27,PR31,PR34,PR35	MV
12		Battery Selector	4/14/2005 (MV)			add PC317	MV

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<93.08.09>	1	codec is the primary codec and must be tied to AC_SDINO	19, 30	Change AC97_SDIN2 to AC97_SDINO for CODEC	0.1
	2	Conexant recommendation	30	Change R351 and R352 to be zero ohm resistors	0.1
	3	This shutdown pin of TPS2211A does not have a internal pullup	26	Add R770	0.1
	4	AMD recommendation	6	Connect pin 3(SD#) of U4 to +3VS directly	0.1
<93.08.11>	5	Driving standby/power LED by STB_LED# pin directly for cost saving.	36	Delete Q79, R384 and R578	0.1
	6	If +2.5VDDA can be connected to +2.5VS directly, we can save the cost of U4	6	Reserve R772	0.1
	7	TI recommendation	23, 24	Add Q85, D50, D51, R773, R774, R775 and C665. Change C403 and C406 from 0.33uF to 1uF	0.1
			26	Connect pin 12 of U12 to PCI_RST#	
	8	ATI recommendation	18	Change R141 from 4.53k 1% to 5.49k 1%	0.1
	9	HP request	27, 28	Change NIC from RTL8110SBL to BCM5788M	0.1
			33	Reserve C704	
			18	Add R799, R800, R801 and R802	
<93.08.11>	10	re-annotation for process rule	4~30, 32~42	re-annotation for all components, excluding MOM and power components.	0.1
<93.10.18>	11	Power saving	5, 8	Change R51, R60, R320 and R326 from 100 ohm to 1K ohm	0.2
			23	Change R496 from 150 ohm to 220 ohm	
			36	Change R285, R290 and R293 from 150 ohm to 220 ohm; Change R296 from 300 ohm to 560 ohm	
	12	Delete useless components which were reserved in rev.0.1	7, 13	Delete C233, C523, R321, C409, U30, R234, C293 and U21	0.2
	13	Pin-9(FS2) of U8(Clock gen.) is not a clock output pin.	13	Delete R95, add R72.	0.2
	14	Use Link# instead of Activity# for NIC_LINK# function	19	Connect U19.C5 to LAN_LINK#	0.2
	15	CARD_LED is an active high signal	23	Change Q45 from MMBT3906 to MMBT3904	0.2
	16	PETp0 and PETn0 should be connected to Tx on the host, PERp0 and PERn0 should be connected to Rx on the host.	26	Swap these differential pairs	0.2
	17	Add an inverter between KBRST from KBC(U39) to KBRST# in SB400(U19)	38	Add Q46 and R497	0.2
	18	The reset signal(PCI_RST#) for LPC BIOS ROM de-assert too late	39	Use NB_RST#(A_RST#) instead of PCI_RST#	0.2
	19	PowerPlay support	13, 14	Add R327, connect U9.E10 to power circuit. Change VDD_CORE of U9 from +1.2V_HT to +R5480_Core	0.2
	20	VariBright support	13, 38	Add R499 and R501, reserve R498 and R500 depopulate R499 and R501, populate R498 and R500	0.2
	21	HP request	19	Add R502	0.2
			36	Change Bat_LED to be on +3VL rail	
			38	Add R503, R504 and R505	
			15	Delete Q40, add R508(reserved), R509 and Q47	
	22	Main battery pin definition change	38	Change the net of U39.76 from THM_MAIN# to KBC_GPIO16; Add R507	0.2
<93.10.21>	23	Mandatory ATI R5480 Design Change(PA_RS480F1)	11	Change R357 from 1K ohm to 0 ohm, delete R355 and R363 from BOM.	0.2

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<93.10.21>	23	ATI Application Note(AN_IXP400A62)	20	Delete R216, R217 and R218, pull SATA_X1, PLLVDD_SATA, XTALVDD_SATA and AVDD_SATA[B:1] to GND	0.2
	24	Power team recommendation	16	Change R316 from 22K_+/-5% to 1.8K_+/-1%, Change R315 from 10K_+/-5% to 1K_+/-1%	0.2
<93.10.26>	25	IDE DASP# signal route error	35	Add D32, D33, R510 and R511	0.2
<93.11.02>	26	To fix USB signal rate failed issue	15 19 22	Populate R76 Do not populate C246 and C247 for external 48MHz OSC. Populate R183 and R417, do not populate R418	0.2
	27	To improve drive strength/Min Bottom Margin for PCIE	18	Change R402 from 5.49K ohm to 4.12K ohm	0.2
	28	ATI Product Advisory(PA_IXP400AC10)	18	Short PJ13; needn't to populate U17, R182 and R186; Change C265, C267, C268 and C269 back to 0.1uF	0.2
	29	HP request	14 15 19 38 41	Delete D6 Populate R508 and do not populate R509 Change R382 from 10K ohm to 47K ohm Change R491, R497 and R507 from 10K ohm to 100K ohm Change C636 from 1uF to 0.1uF	0.2
	30	Charge LED show wrong color	36	Swap the net of D16 pin 1 for the net of pin4	0.2
	31	Once power up Conexant CODEC, We got a pop sound issue. We have used SB GPIO1 to asserted MUTE# for audio amp shutdown to avoided this pop sound. Unfortunately, GPIO1 will output about 1.2m second "Hi" pulse once SB get aux-power, so we can't shutdown amp during this interval. We have to add RC delay circuit to eliminate this pulse.	32	Change R291 from 10K ohm to 100K ohm, add C655	0.2
	32	MIC can't work	33	Change the power of U34 from +VDDA_CODEC to +5V5	0.2
	33	The gain of MIC amp. is too big	33	Change R136 from 150K ohm to 100K ohm	0.2
<93.11.09>	34	HP request	13	Change L23~L25 from FBM-L10-160808-800LMT to HLC0603CSCCR11JT; Change L26~L28 from 0 ohm to HLC0603CSCC39NJT	0.2
	35	To improve overshoot for PCI clock	18	Change R410, R414, R181, R179, R420, R424 and R423 from 22 ohm to 39 ohm	0.2
	36	To improve RTC accuracy	18	Change C250 and C251 from 12pF to 18pF	0.2
	37	Broadcom recommendation	27 28	Add R513 and reserve R512 for BCM4401; Change R313 from 1K ohm to 0 ohm for BCM5788M; Reserve C656~C659 Populate C35 for both BCM5788M and BCM4401	0.2
	38	To improve background noise for microphone	33	Add L43, C660 and R514	0.2
	39	To fix white screen issue after pressing Ctl+Alt+Del to restart	13	Add R515	0.2
<93.11.12>	40	HP request	32	Change C356 and C355 from 0.47uF (X7R 10%) to 0.047uF (X7R 10%); Change C320, 318, 315, and 312 from 470pF to 220pF but still reserved only	0.2
	41	Add Lid switch control from HW side	16	Add D34	0.2
<93.11.17>	42	change PCIRST# to NB_RST#	35 37 38		0.2
	43	HP request for microphone and audio	32 33	Add D35 Add L44,C661,R516 Change R376 to 14K Change U34 to TLC2462 Change R136 to 150K	0.2
	44	reserve for new card clock request	26	reserve Q48	0.2

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<93.11.18>	45	HP request	18 16	Add R518 and R519 Add R517	0.2
<93.12.23>	46	Remove unused component	18 19 33	Del U17,R182,R186 Del R139 Del L43	0.3
	47	Fixed ENVDD pulse when power on	13	Add R521	0.3
	48	Fixed V_VS,SLP_S3 and SLP55 pulse when ALWS apply	19 42	Add U12 (AND gate) Pull high R175 and R176 to VL	0.3
	49	Support Smart Card	23,25	Change U23 from 7411 to 7611 U23 pin k7 pull high to +5VS	0.3
	50	Support XD 1.2	23,25	Reserve U41 (Quick switch) Add R522,R523,R524,R525,R526,R527	0.3
	51	Improve LAN performance	27 28	Change R29 to 1.21K Change U7 to PULSE_H5007	0.3
<93.12.29>	52	Reserve ESD diode on external MIC and speaker connector	32 33	Reserve D36,D37 Reserve D38	0.3
<94.01.07>	53	Remove unused component	2 18 19 38	Del R103,R104,R106,R107 (10K 0402 5%) Del PJ13,U17,R186,R182 (Modify net name from +1.9VS to +1.8VS) Del R150,Y4,C246,C247,C248,C248,C249,Y3,R151,U37,R394 Del R520,C662,R505,R501,R503,R504	0.3
	54	Reserve ESD diode on USB port	34	Reserve D39,D40,D41	0.3
	55	For TI request	23,25	Del R522,R523,R524 (on quick switch) Change R452 to 2.2K Change JP25,pin5 net name to CB_SDWP#_SMCE# Change JP25,pin10 net name to CB_MSBS_SDCMD_SMWE# Change JP25,pin13 net name to CB_MSBS_SDCMD_SMWE# Reserve R531 Add R532 on net CLK_48M_CB for 7611 Add R533 on net CLK_48M_CB for 4510 Add R534 for 4510	0.3
<94.01.10>	56	For TI request	23,25	Add R535 Del R452 Add R536,R537,R538,R539,R540 Del R453	0.3
<94.01.13>	57	For MS card issue	25	Del Q19 Add R544,Q50,R543R545 Reserve U42,Q49,R542,R541,C687,R546	0.3
	58	For HP recommend	04 18	Change R336 to 1.2K 0402 5% Change R398 and R400 to 1.2K	0.3

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<94.02.24>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
59		Improve EMI issue on DDR data bus	8	Change RP8, RP11, RP14~RP17, RP20, RP23, RP24, RP27, RP36, RP37, RP40, RP43, RP44, RP47, RP48, RP51, RP53, RP56 from 10Ω to 39Ω	0.4
60		For S3,S4 resume issue	13 18	Change L34 from FBML10160808121LMT bead to 150Ω 1% resistor Change C268, C269, C265, C267 from 0.1u to 0.01u	0.4
61		Support HW throttling (OCP)	19 19	Change U19.C6 NETNAME from THERM_SCI to OCP# Change U19.B6 NETNAME from OCP# to THERM_SCI	0.4
61		Can't detect Nee card when warm boot	19 19 19 19,29 26	Change MINIPCI_DIS# NETNAME to NEWCARD_RST Del R395 and R530 Change R149 from pull high to pull down Change MINIPCI_RST# NETNAME to PCI_RST# Add Q51	0.4
62		Modify LED brightness	36	Change R285 from 220Ω to 68Ω	0.4
63		Remove unused component and footprint	28 38	Del R303, Q25, Q26 Del R478	0.4
<94.03.07>		Connect Mini PCI clamp to GND	29	Connect JP11.127 and JP11.128 to GND	0.4
65		Remove unused footprint	15	Del R62, R63, R77	0.4
66		Fixed ATI SB400 32.576MHz RTC accuracy issue	18	Change Y5 to EPSON 12.5P 20ppm crystal	0.4
67		Modem time drift issue	30	Change C363 and C367 to 15PF	0.4
<94.03.09>		Separate Cardreader SM_XD power rail	25	Del U42, R545, R546 Add R546, R547, Q56, D41, D42	0.4
69		Change SB 14.318MHz from NB to clock gen	13 19	Delete R67 footprint and let NB OSCOUT pin NC. Delete R529 footprint ,connect SB 14.318MHz from clock gen	0.4
70		Change clock gen 14.318MHz driving method	15	Let Clock gen pin 54 only drive 14.318MHz to SB Let Clock gen pin 53 drive 14.318MHz to Super IO and KBC	0.4
71		Strap on SB400 PCICLK2 redefine.	25	Pop R180 and unpop R183	0.4
72		For ATI recommend to modify PCIE driving strength	12	Change R121 to 8.25KΩ, R120 to 82.5Ω	0.4
73		For ATI recommend	19 13	Let SB SUS_STAT# NC NB SUS_STAT# pull high to 1.8V5, R360 change to 4.7KΩ, R364 change to 470KΩ	0.4
74		Reserve USB ESD diode footprint Reserve resistor footprint between A_ground and D_ground for ESD concern	34 30	Reserve D39 and D40 footprint Reserve R548, R549, R550, R551, R552 footprint	0.4
75		Broadcom 5788M version change	27	Change 5788M from revA3 to revA5	0.4
76		TI 7611 version change	23	Change TI 7611 from revA to revC	0.4
77		Amber LED change for HP request	36	Change D16 to 19-22UY5YG/C/S530-A2/TR8 19X16 G/Y	0.4
78		Layout space save	18	Add RP68, RP69 Del R449, R210, R211, R450, R446, R447, R212, R220	

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<94.04.11>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
79		DDR memtest failed	8	Change RP8, RP11, RP14~RP17, RP20, RP23, RP24, RP27, RP36, RP37, RP40, RP43, RP44, RP47, RP48, RP51, RP53, RP56 from 39Ω to 10Ω	0.5
80		Workaround for S3 resume failed	19	Reserve U43 and add R554	0.5
81		For Sandisk MS pro 512MB card issue	23	Change R209, R224, R536, R537, R538, R539, R540 to 0 ohm	0.5
82		For insert MS card shut down issue	25	Reserve U42, R553 and add C690 Change Cardreader socket pin 45,46 to N.C. Change Cardreader socket pin 1 to GND	0.5
83		For SM card detect abnormal issue	26	Change cardreader pin30 to GND	0.5
84		Charger and BATT full LED brightness abnormaml	36	Add R555	0.5
85		Improve EMI issue	39	Add C689	0.5
86		Improve internal mic noise	33	Change C235 to 0.047u and C239 to 220p	0.5
<94.04.14> 87		TI recommend	23 25	Reserve R556 (pull down on CARD_LED) Reserve C692, C693, C694 (0.1u cap on card detect pin)	
88		Improve internal mic noise	33	Change C235 to 0.027u and C239 to 270p	

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