OP8 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

DDRII-SODIMM1 PAGE 6,7
DDRII-SODIMM2 PAGE 6,7
DDRII 667/800 MHz

AMD Lion Tigris
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

14.318MHz
CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP628VTR-->HP
RTM880N-796 -->HP
PAGE 2
CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E
PCI-Express 16X

NORTH BRIDGE
RS880
A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

HDMI PAGE 25
CRT PAGE 24
LVDS PAGE 23

ATI M92-S for Discrete only
64 Bit,DDR2*4
M92-S2
PAGE 17,18,19 20,21,22

Side port
256mb RAM for UMA only PAGE 8

X1 LAN Realtek PCIE-LAN RTL8103E (10/100) PAGE 30
RJ45 PAGE 30
X1 Mini PCI-E Card (Wireless LAN) PAGE 33

10 PCI-E WLAN Card x1 PAGE 33

ALINK X4
SBSRC_CLK
USB2.0

SOUTH BRIDGE
SB710 A14
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

SATA - HDD PAGE 29 — SATA0 150MB
SATA - CD-ROM PAGE 29 — SATA4 150MB
E-SATA PAGE 29 — SATA1 150MB

1,8,9 USB2.0 Ports X2 PAGE 29
5 Blueflame PAGE 29
2 Webcam X1 PAGE 23
3 Flash Media RTS5159 PAGE 26

Azalia
IDT 92HD75B2 PAGE 27
MDC CONN PAGE 28
AUDIO Amplifier TPA6017A2 PAGE 28
Ang MIC PAGE 28
AUDIO CONN (Phone/ MIC) PAGE 28
Audio Conn PAGE 27

LPC
ENE KBC KB3926 Dx PAGE 32
Keyboard PAGE 32
Touch Pad PAGE 32
FAN PAGE 28
SPI PAGE 35

SYSTEM CHARGER(ISL6251) PAGE 40
SYSTEM POWER ISL6237 PAGE 34
DDR II SMDDR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
VCCP +1.1V AND +1.2V(RT8204) PAGE 35
VGACORE(1.1V~1.2V)Oz8118 PAGE 38
CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Friday, March 20, 2009 Sheet 1 of 42

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP48 STUFF	RP48 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP47 STUFF	RP47 NC	to M92-S external reference clock -RX780 only
SBLINK_CLKP SBLINK_CLKN	RP43 STUFF	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R213,R215 STUFF	R213,R215 NC	To M92-S 27Mhz - RX780 only

600 ohm, 0.5A

+1.2V L45 BLM18PG181SN1D(180,1.5A)_6

C492 22U/6.3V_8, C489 0.1U/10V_4, C468 0.1U/10V_4, C494 0.1U/10V_4, C490 0.1U/10V_4, C428 0.1U/10V_4, C485 0.1U/10V_4

+1.2V_CLKVDDIO

600 ohm, 0.5A

+3V L46 BLM18PG181SN1D(180,1.5A)_6

+3V_CLKVDD

C511 22U/6.3V_8, C430 2.2U/6.3V_6, C434 0.1U/10V_4, C481 0.1U/10V_4, C491 0.1U/10V_4, C479 0.1U/10V_4, C446 0.1U/10V_4, C423 0.1U/10V_4, C412 0.1U/10V_4, C424 0.1U/10V_4

Need check the net name for the short pad

U11

RTM880N-796_QFN64

QFN64

+3V_CLKVDD

Place very close to C/G

+3V_CLKVDD L35 BLM18PG181SN1D(180,1.5A)_6 +3V_CLK_VDDA

C396 2.2U/6.3V_6, C411 0.1U/10V_4

+1.2V_CLKVDDIO

VDDDOT 4, VDDSRC 16, VDDATIG 26, VDDSB 35, VDD_SATA 40, VDDCPU 48, VDDHTT 55, VDDREF 56, VDD48 63

VDDSRC_IO 11, VDDSRC_IO 17, VDDATIG_IO 25, VDDSB_IO 34, VDDCPU_IO 47

GND48 1, GNDDOT 7, GNDSRC 10, GNDSRC 18, GNDATIG 24, GNDSB 33, GNDSATA 43, GNDCPU 46, GNDHTT 52, GNDREF 60

C406 33P/50V_4 CG_XIN

Y1 14.318MHZ

C405 33P/50V_4 CG_XOUT

CG_XIN 61 X1, CG_XOUT 62 X2

can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/S0 power level

6,7,13,33 PCLK_SMB, 6,7,13,33 PDAT_SMB

PCLK_SMB 2 SMBCLK, PDAT_SMB 3 SMBDAT

CLK_PD# 51 PD#

CLKREQ0# 23 *CLKREQ0#
CLKREQ4# 38 *CLKREQ4#
CLKREQ3# 39 *CLKREQ3#
CLKREQ2# 44 *CLKREQ2#
CLKREQ1# 45 *CLKREQ1#

TGND 65

Place within 0.5" of CLKGEN

R178 *261_4

CPUK8_0T 50 CPUCLKP, CPUK8_0C 49 CPUCLKN — RP42 4 3 *0_4P2R_4 2 1 — CPUCLKP CPUCLKN

CPUCLKP 3
CPUCLKN 3

ATIG0T 30 NBGFX_CLKP, ATIG0C 29 NBGFX_CLKN — RP48 4 3 *0_4P2R_4 2 1 — NBGFX_CLKP NBGFX_CLKN

ATIG1T 28 EXT_GFX_CLKP_L, ATIG1C 27 EXT_GFX_CLKN_L — RP47 4 3 *0_4P2R_4 2 1 — EXT_GFX_CLKP EXT_GFX_CLKN

Clock for Dis only

NBGFX_CLKP 10
NBGFX_CLKN 10
EXT_GFX_CLKP 17
EXT_GFX_CLKN 17

to NB for external Graphics reference clock
to M92-S -RX780 only

SB_SRC0T 37 SBLINK_CLKP, SB_SRC0C 36 SBLINK_CLKN — RP43 4 3 *0_4P2R_4 2 1 — SBLINK_CLKP SBLINK_CLKN

SB_SRC1T 32 SBSRC_CLKP, SB_SRC1C 31 SBSRC_CLKN — RP46 4 3 *0_4P2R_4 2 1 — SBSRC_CLKP SBSRC_CLKN

SBLINK_CLKP 10
SBLINK_CLKN 10
SBSRC_CLKP 12
SBSRC_CLKN 12

to NB for AC-LINK reference clock
to SB

SRC0T 22 PCIE_MINI1_CLKP, SRC0C 21 PCIE_MINI1_CLKN — RP45 4 3 *0_4P2R_4 2 1 — PCIE_MINI1_CLKP PCIE_MINI1_CLKN

PCIE_MINI1_CLKP 33
PCIE_MINI1_CLKN 33

to WLAN

SRC1T 20, SRC1C 19, SRC2T 15, SRC2C 14

SRC3T 13 PCIE_LAN_CLKP, SRC3C 12 PCIE_LAN_CLKN — RP44 4 3 *0_4P2R_4 2 1 — PCIE_LAN_CLKP PCIE_LAN_CLKN

PCIE_LAN_CLKP 30
PCIE_LAN_CLKN 30

SRC4T 9, SRC4C 8

SRC7T/27M_SS 6 CLK_VGA_27M_SS, SRC7C/27M 5 CLK_VGA_27M_NSS, SRC6T/SATAT 42, SRC6C/SATAC 41

R217 33_4, R213 75/F_4, R215 100/F_4 — OSC_SPREAD

OSC_SPREAD 18
EVGA-XTALI 18

27Mhz for Dis only

SSIN - for M82 - 3.3V level input
X_TALIN --for M92 -1.8V level input

HTT0T/66M 54 NBHTREFCLK0P, HTT0C/66M 53 NBHTREFCLK0N — R188 *0_4/S NBHT_REFCLKP, R189 *0_4/S NBHT_REFCLKN

NBHT_REFCLKP 10
NBHT_REFCLKN 10

48MHz_0 64 CLK48MUSB — R174 22_4 CLK_48M_USB, R191 22_4 CLK_48M_CR

CLK_48M_USB 13
CLK_48M_CR 26

REF0/SEL_HTT66 59 SEL_HT66
REF1/SEL_SATA 58 SEL_SATA
REF2/SEL_27 57 SEL_27 — T25

R186 33_4 — EXT_SB_OSC 12

R171 Ra 158/F_4
R169 Rb 90.9/F_4 — EXT_NB_OSC 10

	RX880	RS880
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

SI change 1.2V to 3.3V from AMD request

+3V

R207 *8.2K_4 CLKREQ1#

R190 8.2K_4 CLK_PD#

For EMI

C399 *10P/50V_4 EXT_NB_OSC
C404 *10P/50V_4 CLK_48M_USB
C440 *10P/50V_4 EVGA-XTALI
C456 *10P/50V_4 OSC_SPREAD

+3V

R247 *8.2K_4 CLKREQ0#
R212 *8.2K_4 CLKREQ2#
R222 *8.2K_4 CLKREQ3#
R231 *8.2K_4 CLKREQ4#

if use clock request pin , need to pull Hi for default sttting

SLG SLG8SP628VTR--AL8SP628000

RTL RTM880N-796-- AL000880001

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

+3V_CLKVDD

R173 *8.2K_4, R176 8.2K_4

SEL_27
SEL_SATA
SEL_HT66

R192 8.2K_4, R185 *8.2K_4

not need to stuff , R169 have pull LOW

RS780M/RX780M

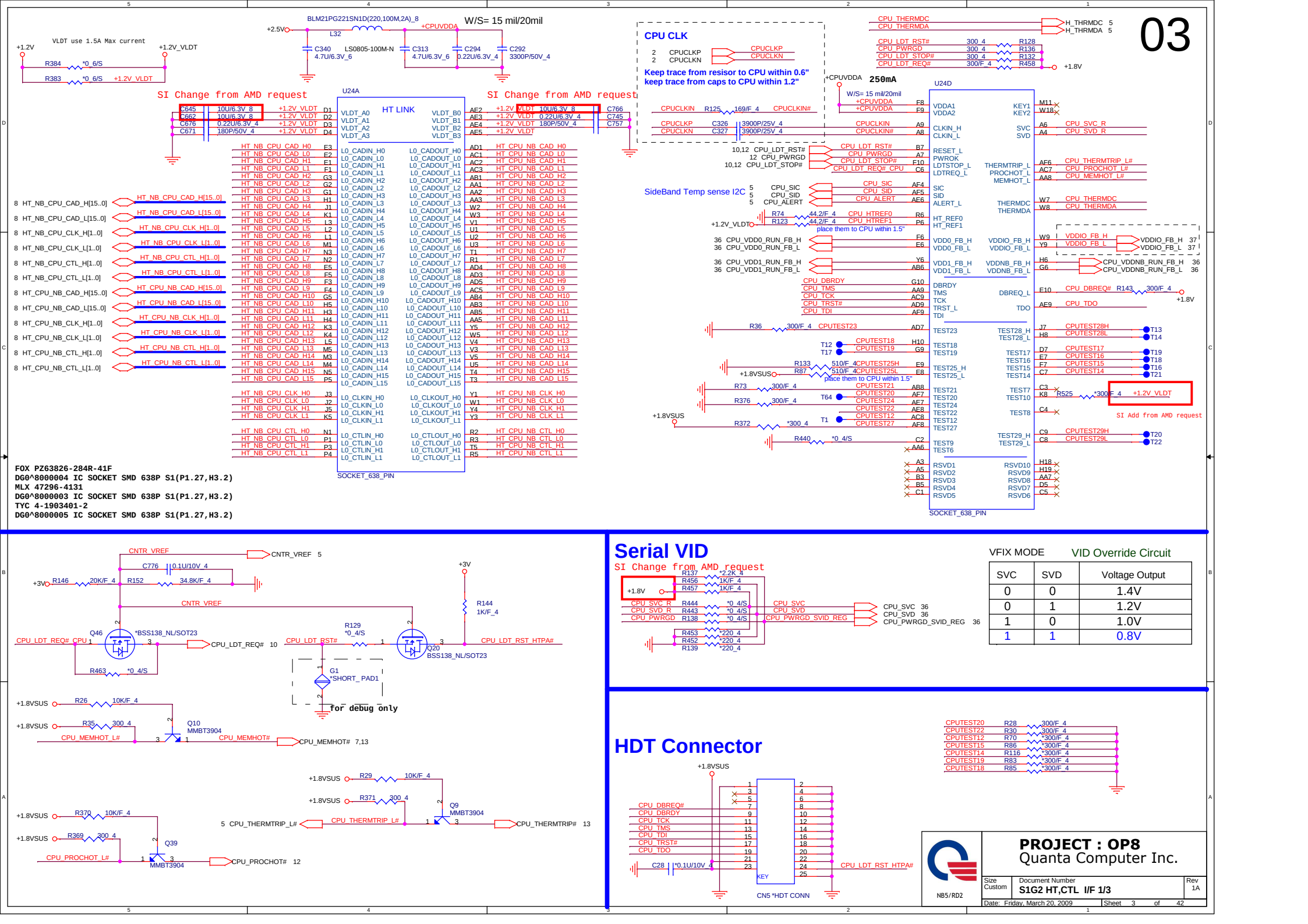
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A

Date: Friday, March 20, 2009 Sheet 2 of 42


03
VLDT use 1.5A Max current
+1.2V
+1.2V_VLDT
R384 *0_6/S
R383 *0_6/S
BLM21PG221SN1D(220,100M,2A)_8
W/S= 15 mil/20mil
+2.5V
L32
+CPUVDDA
C340 4.7U/6.3V_6
LS0805-100M-N
C313 4.7U/6.3V_6
C294 0.22U/6.3V_4
C292 3300P/50V_4
SI Change from AMD request
U24A
HT LINK
SOCKET_638_PIN
CPU CLK
CPUCLKP
CPUCLKN
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
CPUCLKIN R125 169/F_4 CPUCLKIN#
CPUCLKP C326 3900P/25V_4
CPUCLKN C327 3900P/25V_4
+CPUVDDA 250mA
W/S= 15 mil/20mil
U24D
SideBand Temp sense I2C
CPU_SIC
CPU_SID
CPU_ALERT
R74 44.2/F_4 CPU_HTREF0
R123 44.2/F_4 CPU_HTREF1
+1.2V_VLDT
place them to CPU within 1.5"
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
CPU_VDD1_RUN_FB_H
CPU_VDD1_RUN_FB_L
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
R36 300/F_4 CPUTEST23
CPUTEST18
CPUTEST19
R133 510/F_4 CPUTEST25H
R87 510/F_4 CPUTEST25L
+1.8VSUS
R73 300/F_4 CPUTEST21
R376 300/F_4 CPUTEST20
CPUTEST24
CPUTEST22
CPUTEST12
CPUTEST27
R372 *300_4
R440 *0_4/S
CPU_THERMDC
CPU_THERMDA
H_THRMDC 5
H_THRMDA 5
CPU_LDT_RST# 300_4 R128
CPU_PWRGD 300_4 R136
CPU_LDT_STOP# 300_4 R132
CPU_LDT_REQ# 300/F_4 R458
+1.8V
CPU_SVC_R A6
CPU_SVD_R A4
CPU_THERMTRIP_L# AF6
CPU_PROCHOT_L# AC7
CPU_MEMHOT_L# AA8
CPU_THERMDC W7
CPU_THERMDA W8
VDDIO_FB_H W9
VDDIO_FB_L Y9
VDDIO_FB_H 37
VDDIO_FB_L 37
CPU_VDDNB_RUN_FB_H 36
CPU_VDDNB_RUN_FB_L 36
CPU_DBREQ# R143 300/F_4
+1.8V
CPU_TDO
CPUTEST28H T13
CPUTEST28L T14
CPUTEST17 T19
CPUTEST16 T18
CPUTEST15 T16
CPUTEST14 T21
R525 *300/F_4 +1.2V_VLDT
SI Add from AMD request
CPUTEST29H T20
CPUTEST29L T22
SOCKET_638_PIN
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
CNTR_VREF
CNTR_VREF 5
C776 0.1U/10V_4
R146 20K/F_4
R152 34.8K/F_4
R144 1K/F_4
Q46 *BSS138_NL/SOT23
CPU_LDT_REQ# CPU
CPU_LDT_REQ# 10
R463 *0_4/S
R129 *0_4/S
CPU_LDT_RST#
Q20 BSS138_NL/SOT23
CPU_LDT_RST_HTPA#
G1 *SHORT_PAD1
for debug only
R26 10K/F_4
R35 300_4
Q10 MMBT3904
CPU_MEMHOT_L#
CPU_MEMHOT#
CPU_MEMHOT# 7,13
R29 10K/F_4
R371 300_4
Q9 MMBT3904
CPU_THERMTRIP_L#
CPU_THERMTRIP#
CPU_THERMTRIP# 13
R370 10K/F_4
R369 300_4
Q39 MMBT3904
CPU_PROCHOT_L#
CPU_PROCHOT#
CPU_PROCHOT# 12
Serial VID
SI Change from AMD request
R137 *2.2K_4
R456 1K/F_4
R457 1K/F_4
CPU_SVC_R R444 *0_4/S
CPU_SVD_R R443 *0_4/S
CPU_PWRGD R138 *0_4/S
CPU_SVC
CPU_SVD
CPU_PWRGD_SVID_REG
CPU_SVC 36
CPU_SVD 36
CPU_PWRGD_SVID_REG 36
R453 *220_4
R452 *220_4
R139 *220_4
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
HDT Connector
+1.8VSUS
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
C28 *0.1U/10V_4
CPU_LDT_RST_HTPA#
CN5 *HDT CONN
CPUTEST20 R28 300/F_4
CPUTEST22 R30 300/F_4
CPUTEST12 R70 *300/F_4
CPUTEST15 R86 *300/F_4
CPUTEST14 R116 *300/F_4
CPUTEST19 R83 *300/F_4
CPUTEST18 R85 *300/F_4
NB5/RD2
PROJECT : OP8
Quanta Computer Inc.
Size Custom
Document Number S1G2 HT,CTL I/F 1/3
Rev 1A
Date: Friday, March 20, 2009
Sheet 3 of 42

Processor Memory Interface

04

PLACE THEM CLOSE TO CPU WITHIN 1"

750 mA

U24B

SOCKET_638_PIN

U24C

MEM:DATA

SOCKET_638_PIN

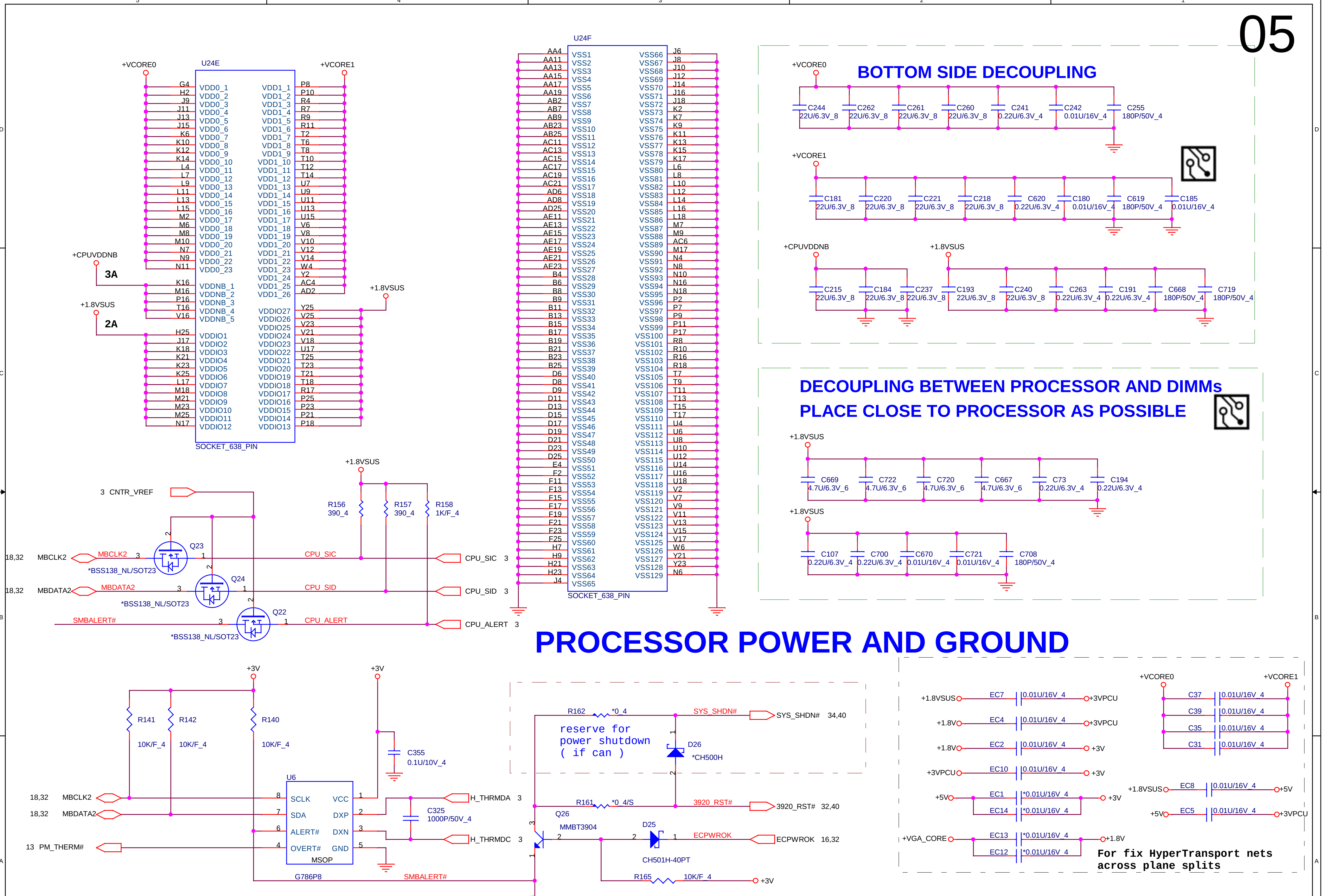
Place close to socket

Close to CPU within 1500 mils

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

PROJECT : OP8		
Quanta Computer Inc.		
Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/3	Rev: 1A
Date: Friday, March 20, 2009	Sheet 4 of 42	

NB5/RD2

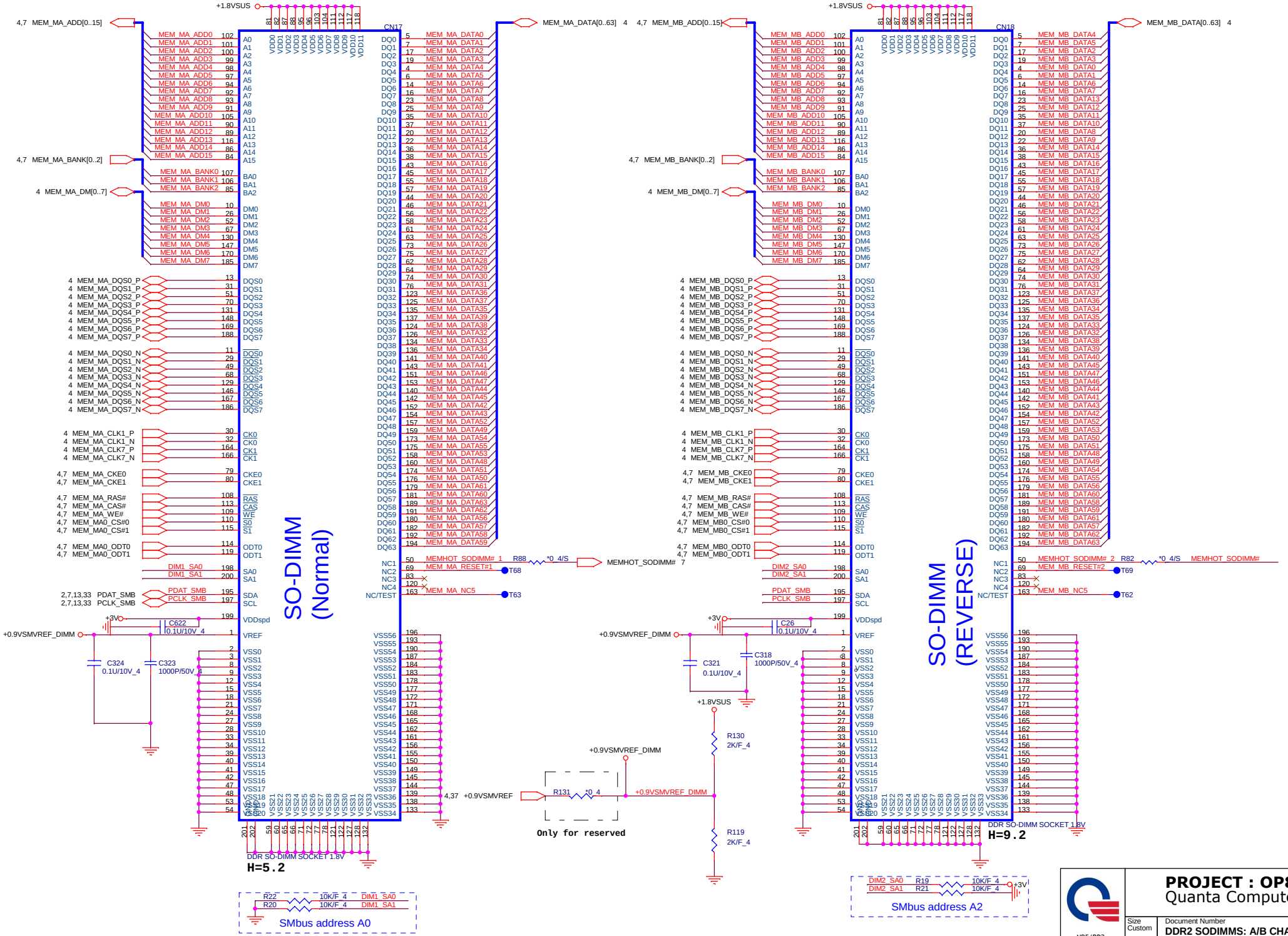

05
U24E
+VCORE0
+VCORE1
+CPUVDDNB
3A
+1.8VSUS
2A
VDD0_1 … VDD0_23
VDD1_1 … VDD1_26
VDDNB_1 … VDDNB_5
VDDIO1 … VDDIO27
SOCKET_638_PIN
U24F
VSS1 … VSS129
SOCKET_638_PIN
BOTTOM SIDE DECOUPLING
C244 22U/6.3V_8
C262 22U/6.3V_8
C261 22U/6.3V_8
C260 22U/6.3V_8
C241 0.22U/6.3V_4
C242 0.01U/16V_4
C255 180P/50V_4
C181 22U/6.3V_8
C220 22U/6.3V_8
C221 22U/6.3V_8
C218 22U/6.3V_8
C620 0.22U/6.3V_4
C180 0.01U/16V_4
C619 180P/50V_4
C185 0.01U/16V_4
C215 22U/6.3V_8
C184 22U/6.3V_8
C237 22U/6.3V_8
C193 22U/6.3V_8
C240 22U/6.3V_8
C263 0.22U/6.3V_4
C191 0.22U/6.3V_4
C668 180P/50V_4
C719 180P/50V_4
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE
C669 4.7U/6.3V_6
C722 4.7U/6.3V_6
C720 4.7U/6.3V_6
C667 4.7U/6.3V_6
C73 0.22U/6.3V_4
C194 0.22U/6.3V_4
C107 0.22U/6.3V_4
C700 0.22U/6.3V_4
C670 0.01U/16V_4
C721 0.01U/16V_4
C708 180P/50V_4
3 CNTR_VREF
R156 390_4
R157 390_4
R158 1K/F_4
18,32 MBCLK2
18,32 MBDATA2
SMBALERT#
Q23 *BSS138_NL/SOT23
Q24 *BSS138_NL/SOT23
Q22 *BSS138_NL/SOT23
CPU_SIC 3
CPU_SID 3
CPU_ALERT 3
PROCESSOR POWER AND GROUND
+3V
R141 10K/F_4
R142 10K/F_4
R140 10K/F_4
C355 0.1U/10V_4
U6 G786P8 MSOP
SCLK VCC SDA DXP ALERT# DXN OVERT# GND
C325 1000P/50V_4
H_THRMDA 3
H_THRMDC 3
13 PM_THERM#
+1.8VSUS R450 *10K/F_4
Q43 *MMBT3904
3 CPU_THERMTRIP_L#
R162 *0_4
SYS_SHDN# 34,40
reserve for
power shutdown
(if can)
D26 *CH500H
R161 *0_4/S
3920_RST# 32,40
Q26 MMBT3904
D25 CH501H-40PT
ECPWROK 16,32
R165 10K/F_4
PQ56 *2N7002E-G
R459 *10K/F_4
TEMP_FAIL 18
ADD VGA TEMP_ FAIL function
M92 is active Hi
EC11 EC9 EC6 EC3 *0.1U/10V_4
EC7 EC4 EC2 EC10 0.01U/16V_4
EC1 EC14 EC13 EC12 *0.01U/16V_4
C37 C39 C35 C31 0.01U/16V_4
EC8 EC5 0.01U/16V_4
+VGA_CORE +3VPCU +5V +1.8V +3VS5
For fix HyperTransport nets
across plane splits

PROJECT : OP8
Quanta Computer Inc.

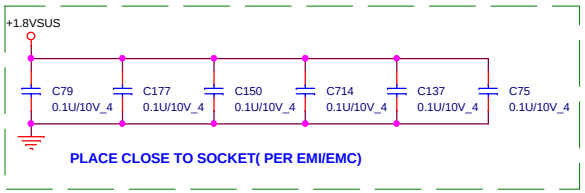
NB5/RD2

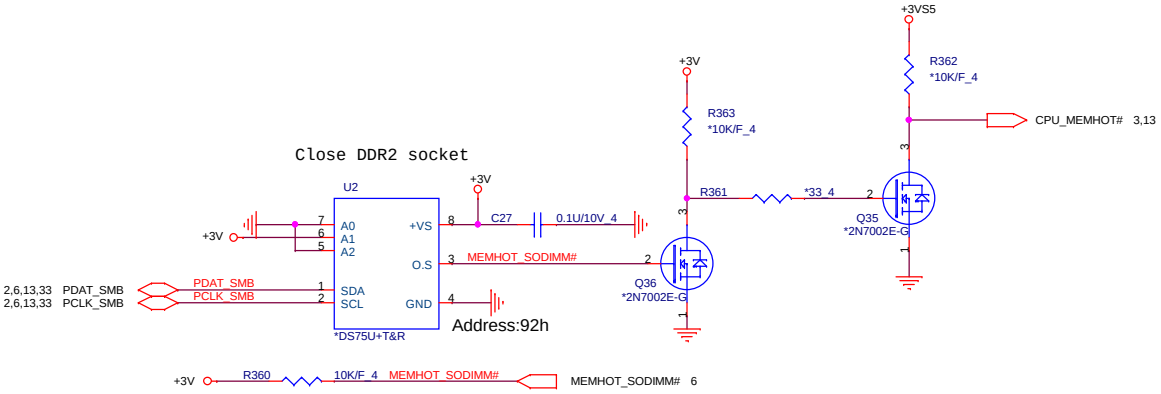
Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	1A

Date: Friday, March 20, 2009 Sheet 5 of 42



NB5/RD2	**PROJECT : OP8** Quanta Computer Inc.	
Size Custom	Document Number **DDR2 SODIMMS: A/B CHANNEL**	Rev 1A
Date: Friday, March 20, 2009	Sheet 6 of 42	



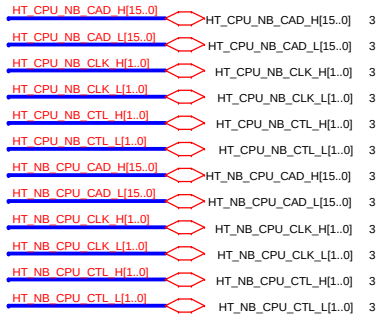


PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

NB5/RD2

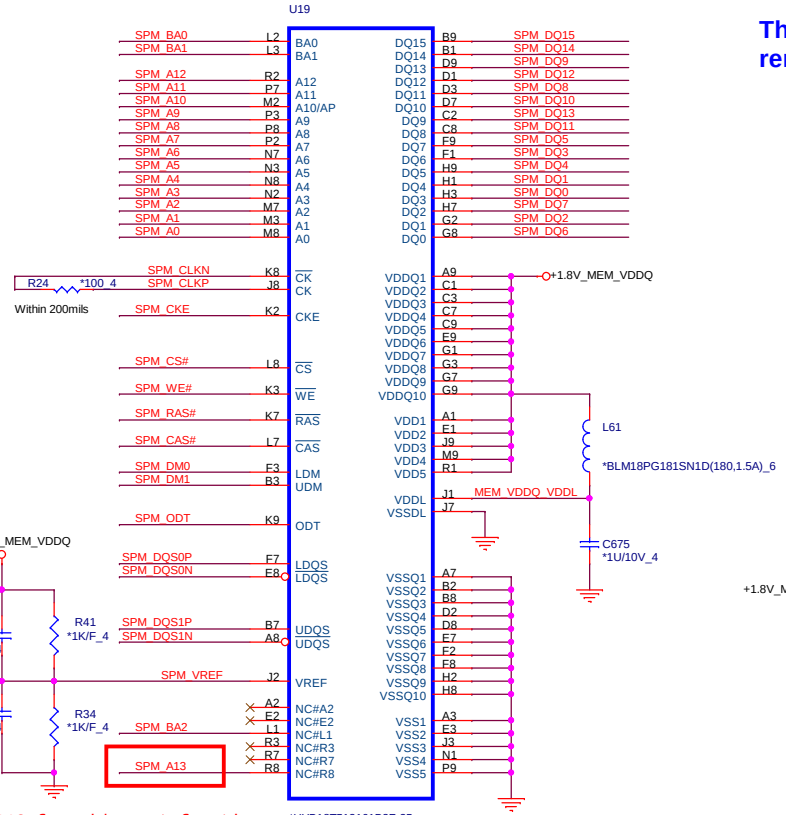
Date: Friday, March 20, 2009 | Sheet 7 of 42



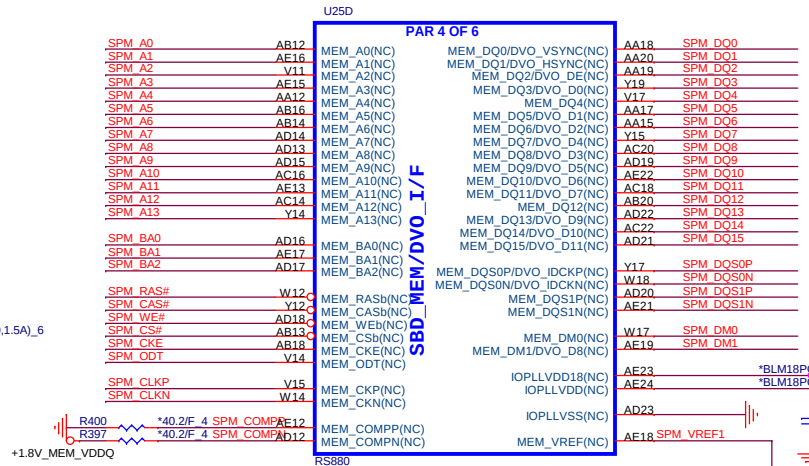
signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

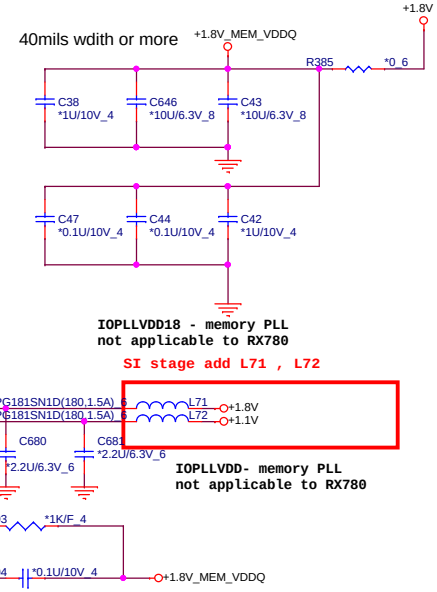
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14



This block is for UMA RS880 only , RX880 can remove all component



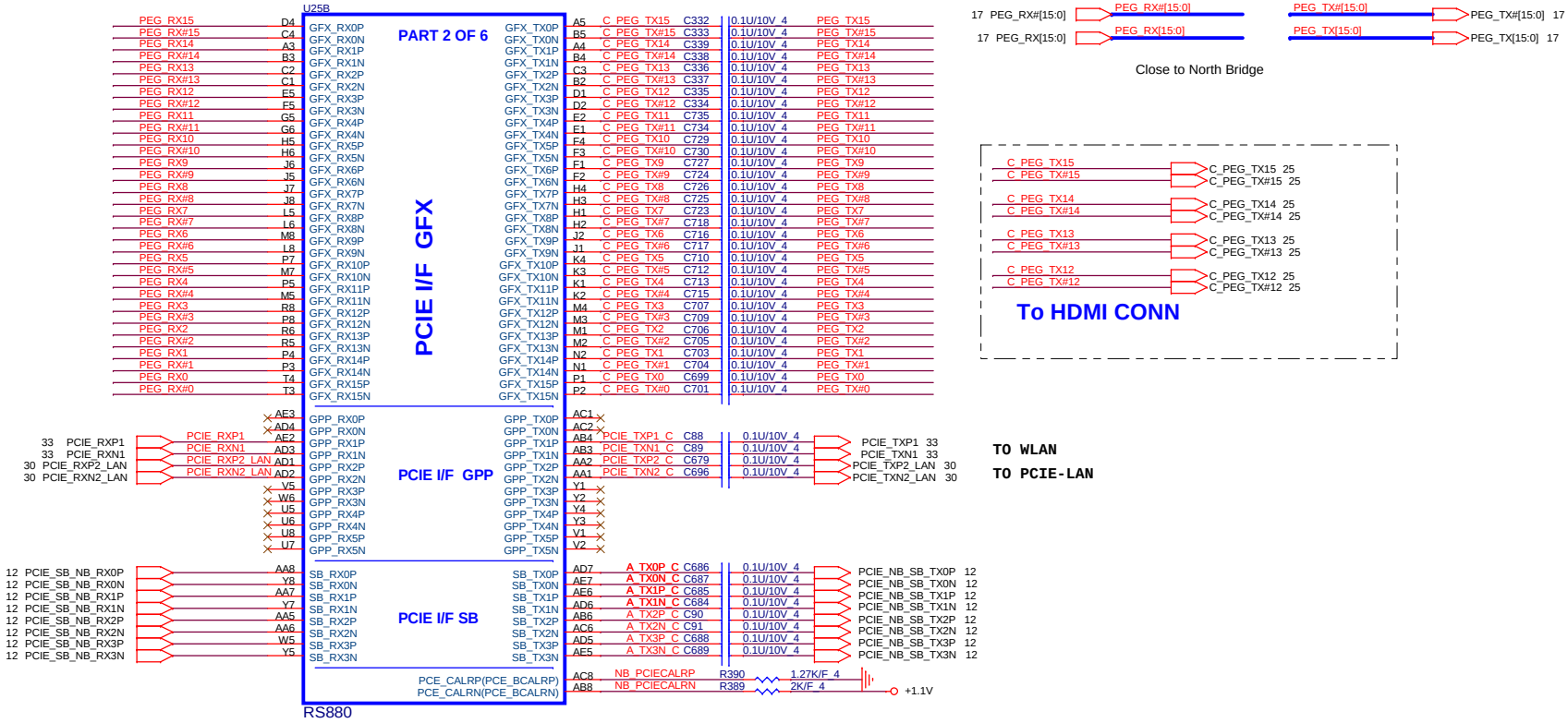


PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-HT LINK I/F 1/5	1A

NB5/RD2

Date: Friday, March 20, 2009 Sheet 8 of 42



17 PEG_RX#[15:0] → PEG_RX#[15:0]
17 PEG_RX[15:0] → PEG_RX[15:0]
PEG_TX#[15:0] → PEG_TX#[15:0] 17
PEG_TX[15:0] → PEG_TX[15:0] 17

Close to North Bridge

C_PEG_TX15 → C_PEG_TX15 25, C_PEG_TX#15 25
C_PEG_TX14 → C_PEG_TX14 25, C_PEG_TX#14 25
C_PEG_TX13 → C_PEG_TX13 25, C_PEG_TX#13 25
C_PEG_TX12 → C_PEG_TX12 25, C_PEG_TX#12 25

To HDMI CONN

PCIE_TXP1 33, PCIE_TXN1 33, PCIE_TXP2_LAN 30, PCIE_TXN2_LAN 30

TO WLAN

TO PCIE-LAN

PCIE_RXP1 33, PCIE_RXN1 33, PCIE_RXP2_LAN 30, PCIE_RXN2_LAN 30

A_TX0P_C C686, A_TX0N_C C687, A_TX1P_C C685, A_TX1N_C C684, A_TX2P_C C90, A_TX2N_C C91, A_TX3P_C C688, A_TX3N_C C689

PCIE_NB_SB_TX0P 12, PCIE_NB_SB_TX0N 12, PCIE_NB_SB_TX1P 12, PCIE_NB_SB_TX1N 12, PCIE_NB_SB_TX2P 12, PCIE_NB_SB_TX2N 12, PCIE_NB_SB_TX3P 12, PCIE_NB_SB_TX3N 12

PCIE_SB_NB_RX0P 12, PCIE_SB_NB_RX0N 12, PCIE_SB_NB_RX1P 12, PCIE_SB_NB_RX1N 12, PCIE_SB_NB_RX2P 12, PCIE_SB_NB_RX2N 12, PCIE_SB_NB_RX3P 12, PCIE_SB_NB_RX3N 12

RS880 Display Port Support (muxed on GFX)

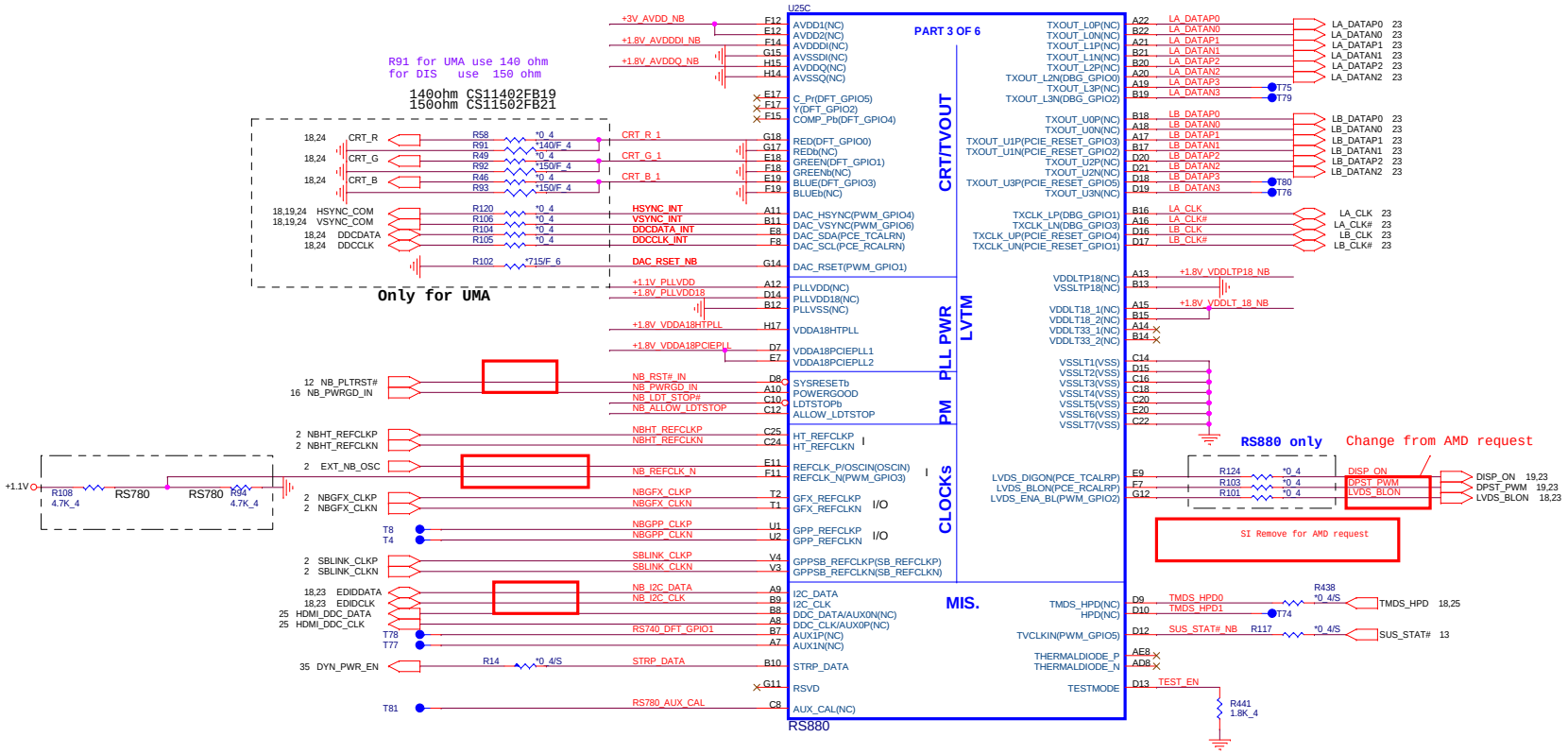
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

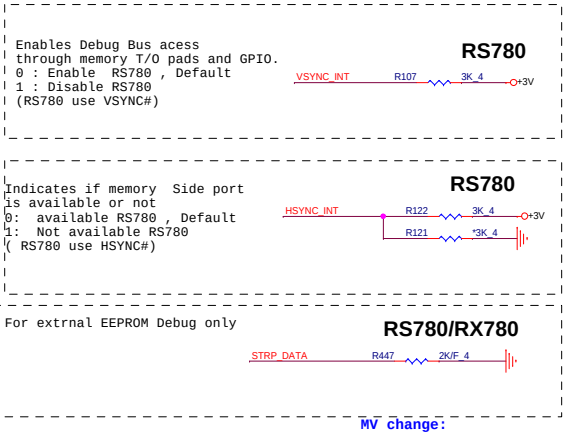
NB5/RD2

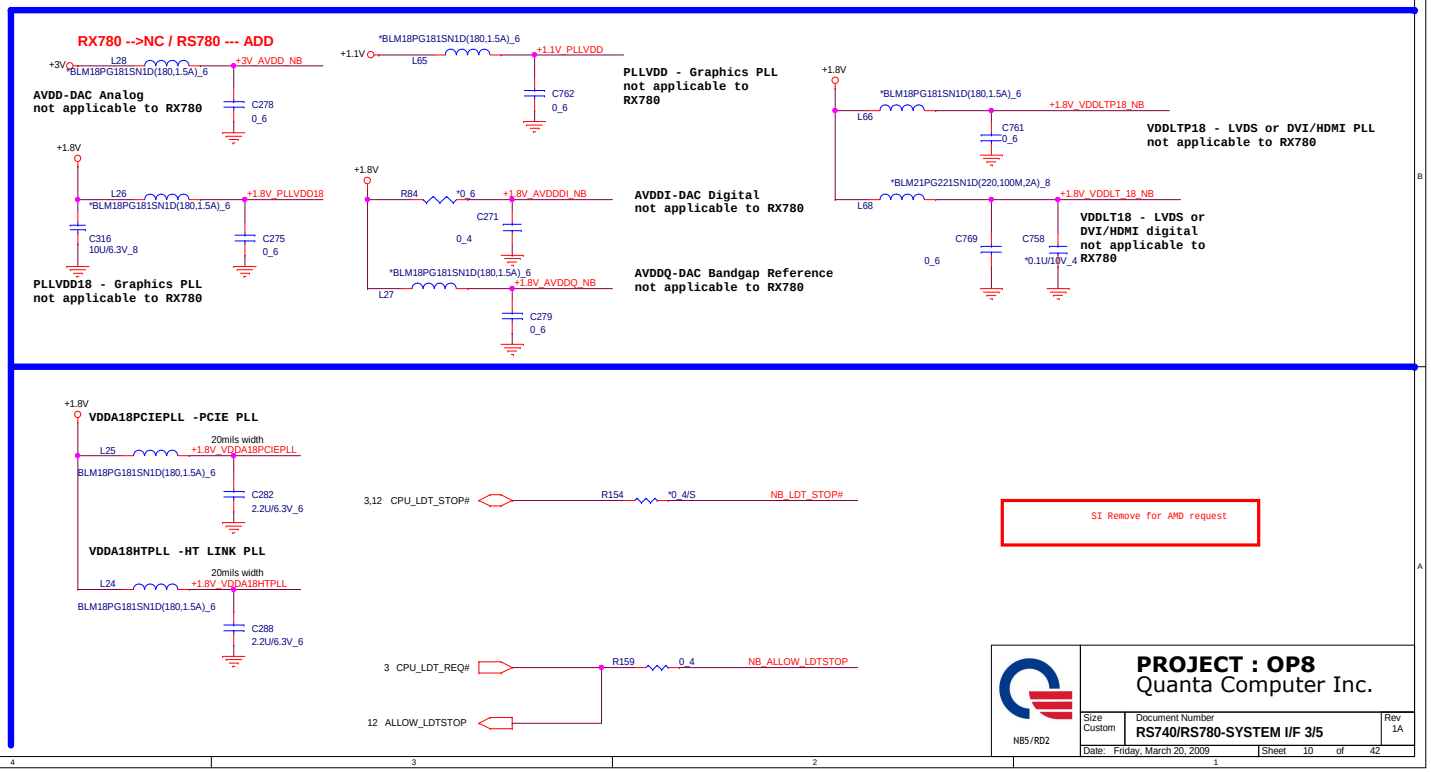
PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-PCIE I/F 2/5	1A

Date: Friday, March 20, 2009 Sheet 9 of 42


U25C
PART 3 OF 6
RS880
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKS
MIS.
R91 for UMA use 140 ohm
for DIS use 150 ohm
140ohm CS11402FB19
150ohm CS11502FB21
Only for UMA
RS880 only
Change from AMD request
SI Remove for AMD request


Enables Debug Bus acess
through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780
Indicates if memory Side port
is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780
For extrnal EEPROM Debug only
RS780/RX780
MV change:


RX780 -->NC / RS780 --- ADD
AVDD-DAC Analog
not applicable to RX780
PLLVDD18 - Graphics PLL
not applicable to RX780
PLLVDD - Graphics PLL
not applicable to
RX780
AVDDI-DAC Digital
not applicable to RX780
AVDDQ-DAC Bandgap Reference
not applicable to RX780
VDDLTP18 - LVDS or DVI/HDMI PLL
not applicable to RX780
VDDLT18 - LVDS or
DVI/HDMI digital
not applicable to
RX780
VDDA18PCIEPLL -PCIE PLL
VDDA18HTPLL -HT LINK PLL
SI Remove for AMD request

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

PART 6/6 — GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

VDDHT - HT LINK digital I/O for RX780/RS780

+1.1V — 0.6A — L58 *0_8/S — +1.1V_VDDHT

C693 4.7U/6.3V_6 | C224 0.1U/10V_4 | C265 0.1U/10V_4 | C238 0.1U/10V_4

+1.1V 2A for RS880M

VDDHTRX - HT LINK RX I/O for RX780/RS780

0.45A — L64 *0_8/S — +1.1V_VDDHTRX

C770 4.7U/6.3V_6 | C272 0.1U/10V_4 | C763 0.1U/10V_4 | C759 0.1U/10V_4

VDDHTTX - HT LINK TX I/O for RX780/RS780

+1.2V — L13 *0_8/S — 0.5A — **+1.2V 2A for RS780M+SB700** — +1.2V_VDDHTTX

C80 4.7U/6.3V_6 | C152 0.1U/10V_4 | C139 0.1U/10V_4 | C195 0.1U/10V_4 | C151 0.1U/10V_4

+1.8V 1A for RS780M+SB700

+1.8V — L17 BLM21PG221SN1D(220,100M,2A)_8 — 600mA — +1.8V_VDDA18PCIE

C141 4.7U/6.3V_6 | C126 4.7U/6.3V_6 | C209 0.1U/10V_4 | C166 0.1U/10V_4 | C257 0.1U/10V_4 | C188 0.1U/10V_4

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

+1.8V — R110 *0_6/S — 0.005A — C267 1U/10V_4 — +1.8V_VDDG18_NB

+1.8V — R395 *0_6/S — 0.005A — C692 1U/10V_4 — +1.8V_VDD18_MEM

VDD18_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

U25E — **PART 5/6** — **POWER** — RS880

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC)

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC)

VDDG33_1(NC) VDDG33_2(NC)

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE — 0.7A — R99 *0_8/S — +1.1V

C226 0.1U/10V_4 | C277 0.1U/10V_4 | C268 1U/10V_4 | C273 1U/10V_4 | C281 4.7U/6.3V_6

VDDC - Core Logic power

7A — +1.1V_DYN

C203 0.1U/10V_4 | C250 0.1U/10V_4 | C252 0.1U/10V_4 | C258 0.1U/10V_4 | C29 10U/6.3V_8

C239 0.1U/10V_4 | C232 0.1U/10V_4 | C202 0.1U/10V_4 | C30 10U/6.3V_8

VDD_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

+1.8V_VDD_MEM — 1.8V(0.15A) — BLM21PG221SN1D(220,100M,2A)_8 — L18 — +1.8V

C149 0.1U/10V_4 | C128 0.1U/10V_4 | C127 1U/10V_4 | C168 1U/10V_4 | C138 10U/6.3V_8

+3V_VDDG33 — R111 RS780 *0_6/S — 3.3V(0.03A) — +3V

C276 0.1U/10V_4 | C274 0.1U/10V_4

VDD33 - 3.3V I/O Not applicable to RX780

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-POWER5/5	1A

Date: Friday, March 20, 2009 | Sheet 11 of 42

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780

PCIE_PVDD-- PCIE PLL POWER

40mA

Change for SB710 chip

FOR A14 chip

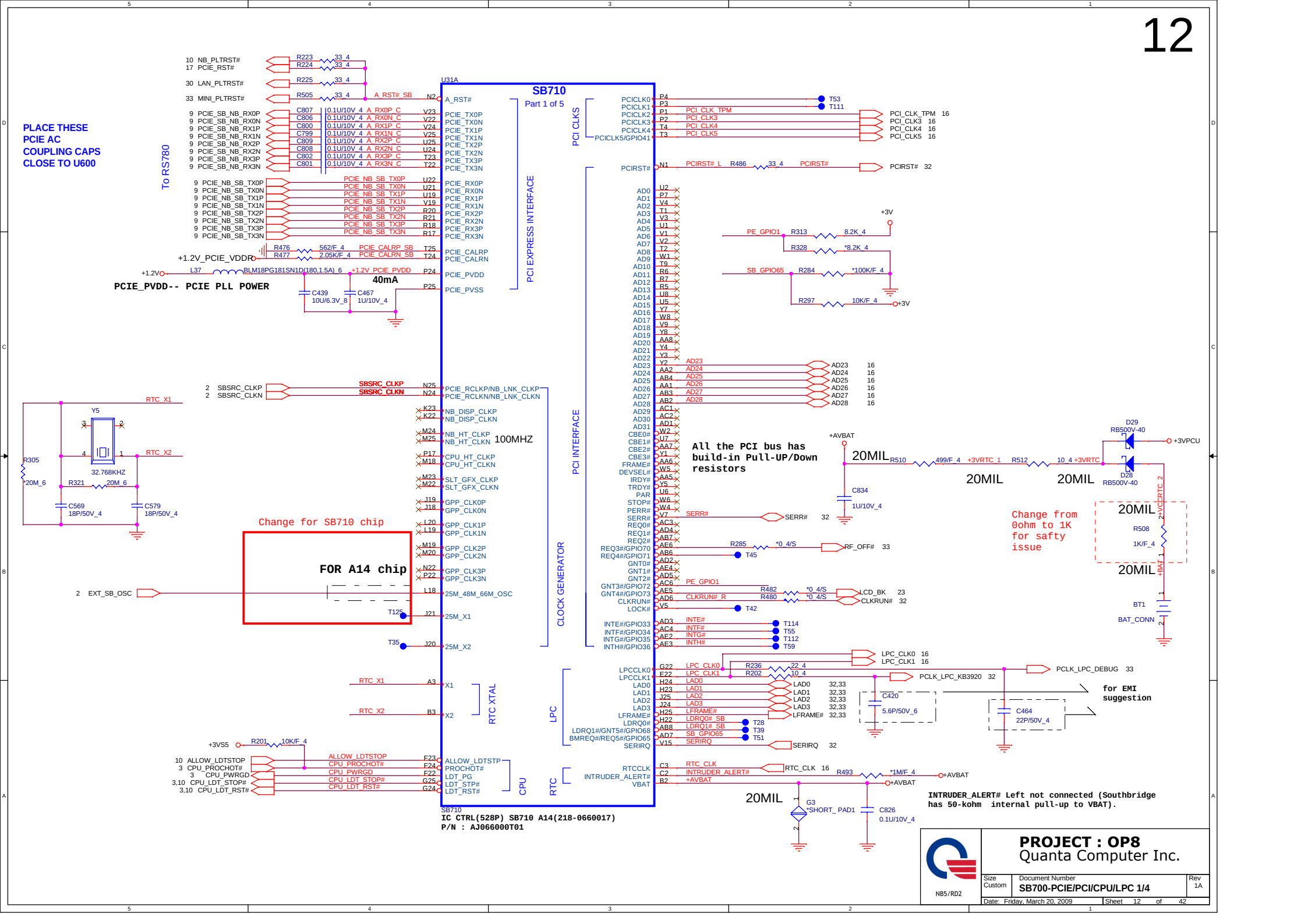
All the PCI bus has build-in Pull-UP/Down resistors

Change from 0ohm to 1K for safty issue

for EMI suggestion

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB710
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01



NC only ,Can't be install

+3VS5 R319 *2.2K_4 SB_TEST0
R180 *2.2K_4 SB_TEST1
R296 *2.2K_4 SB_TEST2

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R238 2.2K_4 PCLK_SMB
R241 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

Check BIOS for no connetcor pin for the power

Change for test point for Debug mode

30,33 PCIE_WAKE# T56 T124 C840 100P/50V_4

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R492 2.2K_4 SB_SMBCLK1
R494 2.2K_4 SB_SMBDATA1

remove pull hi
(chip internal
have pull hi)

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R204 2.2K_4 SB_SCLK2
R205 2.2K_4 SB_SDATA2

+3V R290 3K_4 SUS_STAT#

Change from AMD request

+3VS5 R288 2.2K_4 DNBSWON#

To Azalia

ACZ_SDOUT R487 33_4 C830 *10P/50V_4 ACZ_SDOUT_AUDIO 27
ACZ_SYNC R303 33_4 C562 *10P/50V_4 ACZ_SYNC_AUDIO 27
ACZ_BCLK R489 33_4 C832 10P/50V_4 BIT_CLK_AUDIO 27
ACZ_RST# R317 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0 ACZ_SDIN0 27

Remove short pad

To Modem Board

ACZ_SDOUT R488 33_4 C831 *10P/50V_4 ACZ_SDOUT_AUDIO_MDC 28
ACZ_SYNC R320 33_4 C580 *10P/50V_4 ACZ_SYNC_AUDIO_MDC 28
ACZ_BCLK R490 33_4 C833 10P/50V_4 BIT_CLK_AUDIO_MDC 28
ACZ_RST# R312 33_4 ACZ_RST#_AUDIO_MDC 28
ACZ_SDIN1 ACZ_SDIN1 28

Remove short pad

Modified for EMI suggestion

HD audio interface is 3.3S5 voltage

SB JTAG

CN11 +3VSUS C393 10P/50V_4
SB_JTAG_TCK SB_JTAG_TDO SB_JTAG_TDI SB_TEST1 SB_JTAG_RST#

*S/W JTAG DEBUG

U31D SB710 Part 4 of 5

PCI_PME#/GEVENT4# RI#/EXTEVNT0# SLP_S2/GPM9# SLP_S3# SLP_S5# PWR_BTN# PWR_GOOD SUS_STAT# TEST2 TEST1 TEST0 GA20IN/GEVENT0# KBRST#/GEVENT1# LPC_PME#/GEVENT3# LPC_SMI#/EXTEVNT1# S3_STATE/GEVENT5# SYS_RESET#/GPM7# WAKE#/GEVENT8# BLINK/GPM6# SMBALERT#/THRMTRIP#/GEVENT2# NB_PWRGD RSMRST#

ACPI / WAKE UP EVENTS

SATA_IS0#/GPIO10 CLK_REQ3#/SATA_IS1#/GPIO6 SMARTVOLT/SATA_IS2#/GPIO4 CLK_REQ0#/SATA_IS3#/GPIO0 CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39 CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40 SPKR/GPIO2 SCL0/GPOC0# SDA0/GPOC1# SCL1/GPOC2# SDA1/GPOC3# DDC1_SCL/GPIO9 DDC1_SDA/GPIO8 LLB#/GPIO66 SHUTDOWN#/GPIO5 DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6# USB_OC5#/IR_TX0/GPM5# USB_OC4#/IR_RX0/GPM4# USB_OC3#/IR_RX1/GPM3# USB_OC2#/GPM2# USB_OC1#/GPM1# USB_OC0#/GPM0#

USB OC

AZ_BITCLK AZ_SDOUT AZ_SDIN0/GPIO42 AZ_SDIN1/GPIO43 AZ_SDIN2/GPIO44 AZ_SDIN3/GPIO46 AZ_SYNC AZ_RST# AZ_DOCK_RST#/GPM8#

HD AUDIO

IMC_GPIO0 IMC_GPIO1 SPI_CS2#/IMC_GPIO2 IDE_RST#/F_RST#/IMC_GPO3 IMC_GPIO4 IMC_GPIO5 IMC_GPIO6 IMC_GPIO7

INTEGRATED uC

USBCLK/14M_25M_48M_OSC CLK_48M_USB 2
USB_RCOMP R263 11.8K/F_6

USB MISC

USB_FSD13P USB_FSD13N T54 T57
USB_FSD12P USB_FSD12N T38 T40

USB 1.1

USB_HSD11P USB_HSD11N
USB_HSD10P USB_HSD10N USBP10+ USBP10- 33 WLAN Min-Card
USB_HSD9P USB_HSD9N USBP9+ USBP9- 29 BLUETOOTH
USB_HSD8P USB_HSD8N USBP8+ USBP8- 29 USB Connector

Si Change USB port reference Raven 2.0 design

USB_HSD7P USB_HSD7N
USB_HSD6P USB_HSD6N
USB_HSD5P USB_HSD5N USBP5+ USBP5- 29 USB Connector
USB_HSD4P USB_HSD4N
USB_HSD3P USB_HSD3N USBP3+ USBP3- 26 USB card reader
USB_HSD2P USB_HSD2N USBP2+ USBP2- 23 Carama USB
USB_HSD1P USB_HSD1N USBP1+ USBP1- 29 E-SATA and USB Connector
USB_HSD0P USB_HSD0N

USB 2.0

IMC_GPIO8 IMC_GPIO9 IMC_PWM0/IMC_GPIO10 SCL2/IMC_GPIO11 SDA2/IMC_GPIO12 SCL3_LV/IMC_GPIO13 SDA3_LV/IMC_GPIO14 IMC_PWM1/IMC_GPIO15 IMC_PWM2/IMC_GPIO16 IMC_PWM3/IMC_GPIO17 SB_SCLK2 SB_SDATA2 SB_SCLK3 T32 5158_RST_R# 26 SB_GPIO16 16 SB_GPIO17 16 SPI/LPC define

IMC_GPIO18 IMC_GPIO19 IMC_GPIO20 IMC_GPIO21 IMC_GPIO22 IMC_GPIO23 IMC_GPIO24 IMC_GPIO25 IMC_GPIO26 IMC_GPIO27 IMC_GPIO28 IMC_GPIO29 IMC_GPIO30 IMC_GPIO31 IMC_GPIO32 IMC_GPIO33 IMC_GPIO34 IMC_GPIO35 IMC_GPIO36 IMC_GPIO37 IMC_GPIO38 IMC_GPIO39 IMC_GPIO40 IMC_GPIO41

for EMI

CLK_48M_USB C516 *2.2P/50V_4

PROJECT : OP8			
Quanta Computer Inc.			
NB5/RD2	Size Custom	Document Number SB700-ACPI/GPIO/USB 2/4	Rev 1A
	Date: Friday, March 20, 2009	Sheet 13 of 42	

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SATA1

SATA ODD

E-SATA

U31B

SB710
Part 2 of 5

SERIAL ATA

SATA_TX0P / SATA_TX0N
SATA_RX0N / SATA_RX0P
SATA_TX1P / SATA_TX1N
SATA_RX1N / SATA_RX1P
SATA_TX2P / SATA_TX2N
SATA_RX2N / SATA_RX2P
SATA_TX3P / SATA_TX3N
SATA_RX3N / SATA_RX3P
SATA_TX4P / SATA_TX4N
SATA_RX4N / SATA_RX4P
SATA_TX5P / SATA_TX5N
SATA_RX5N / SATA_RX5P
SATA_CAL
SATA_X1
SATA_X2
SATA_ACT#/GPIO67

SATA PWR

PLLVDD_SATA
XTLVDD_SATA

ATA 66/100/133

IDE_IORDY, IDE_IRQ, IDE_A0, IDE_A1, IDE_A2, IDE_DACK#, IDE_DRQ, IDE_IOR#, IDE_IOW#, IDE_CS1#, IDE_CS3#
IDE_D0/GPIO15 … IDE_D15/GPIO30

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SPI ROM

SPI_DI/GPIO12, SPI_DO/GPIO11, SPI_CLK/GPIO47, SPI_HOLD#/GPIO31, SPI_CS#/GPIO32
LAN_RST#/GPIO13, ROM_RST#/GPIO14

HW MONITOR

FANOUT0/GPIO3, FANOUT1/GPIO48, FANOUT2/GPIO49
FANIN0/GPIO50, FANIN1/GPIO51, FANIN2/GPIO52
TEMP_COMM, TEMPIN0/GPIO61, TEMPIN1/GPIO62, TEMPIN2/GPIO63, TEMPIN3/TALERT#/GPIO64
VIN0/GPIO53 … VIN7/GPIO60
SIDE_PORT_ID0, SIDE_PORT_ID1, BOARD_ID0, BOARD_ID1, BOARD_ID2, BOARD_ID3

AVDD, AVSS

SB710

R361 1K/F_4 — SATA_RBIAS_PN

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

Y4 25MHZ, C501 27P/50V_4, C487 27P/50V_4, R246 10M_6

U12 TC7SH08FU — SATA_LED# / SB_SATA_LED#

C500 0.1U/10V_4

+1.2V (1.2V @ 60mA) — L42 BLM21PG221SN1D(220,100M,2A)_8 — +1.2V_PLLVDD_SATA 77mA
C495 1U/10V_4, C520 0.1U/10V_4, C510 22U/6.3V_8, C509 22U/6.3V_8

+3V (3.3V @ 1.2mA) — L41 BLM18PG181SN1D(180,1.5A)_6 — +3V_XTLVDD_SATA 1mA
C504 1U/10V_4 Place near ball

AVDD: 5mA — +3V_VDD_HWM — L47 *0_6/S — +3VS5
C566 *0.1U/10V_4, C561 *2.2U/6.3V_6

AVDD--H/W monitor Analog power

Add for design

SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	Samsung
0	1	Qimonda
1	0	Hynix
1	1	no supprot side port

+3VS5 R526 10K/F_4 SIDE_PORT_ID0 R527 *10K/F_4
+3VS5 R287 10K/F_4 SIDE_PORT_ID1 R294 *10K/F_4

+3VS5 R272 *10K/F_4 BOARD_ID0 R271 10K/F_4
R261 10K/F_4 BOARD_ID1 R251 *10K/F_4
R277 *10K/F_4 BOARD_ID2 R265 10K/F_4
R278 *10K/F_4 BOARD_ID3 R266 10K/F_4

ID3	ID2	ID1	ID0	
0	0	0	0	OP8 UMA
0	0	0	1	OP9 UMA
0	0	1	0	OP8 Dis
0	0	1	1	OP9 Dis
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

Date: Friday, March 20, 2009 Sheet 14 of 42

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

POWER

VDDQ--3.3V I/O power — 0.8A

+3V → C571 100U/6.3V_3528 + C537 10U/6.3V_8 + C551 1U/10V_4 + C564 1U/10V_4 + C556 1U/10V_4 + C517 0.1U/10V_4 + C528 0.1U/10V_4 + C565 0.1U/10V_4

AMD : Change from 1u to 0.1u

U31C SB710 Part 3 of 5

VDDQ_1 L9
VDDQ_2 M9
VDDQ_3 T15
VDDQ_4 U9
VDDQ_5 U16
VDDQ_6 U17
VDDQ_7 V8
VDDQ_8 W7
VDDQ_9 Y6
VDDQ_10 AA4
VDDQ_11 AB5
VDDQ_12 AB21

PCI/GPIO I/O

VDD-- S/B CORE power

+1.2V_VCC_SB_R

VDD_1 L15
VDD_2 M12
VDD_3 M14
VDD_4 N13
VDD_5 P12
VDD_6 P14
VDD_7 R11
VDD_8 R15
VDD_9 T16

CORE S0

604mA

C498 0.1U/10V_4 + C513 0.1U/10V_4 + C506 1U/10V_4 + C497 1U/10V_4 + C408 10U/6.3V_8

R179 *0_8/S → +1.2V

AMD : Change from 1u to 0.1u

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power — 0.45A

+3V → R216 *0_8/S → +VDD33_18

SI Remove R219 from AMD request

C441 *10U/6.3V_8 + C465 *1U/10V_4 + C442 *0.1U/10V_4 + C460 *0.1U/10V_4 + C443 *0.1U/10V_4

AMD : Change from 1u to 0.1u

AMD : Remove Cap for IDE mode

VDD33_18_1 Y20
VDD33_18_2 AA21
VDD33_18_3 AA22
VDD33_18_4 AE25

IDE/FLSH I/O

CKVDD_1.2V-- Internal clock Generator I/O power

+1.2V_CKVDD

CKVDD_1.2V_1 L21
CKVDD_1.2V_2 L22
CKVDD_1.2V_3 L24
CKVDD_1.2V_4 L25

CLKGEN I/O

286mA

C474 *2.2U/6.3V_6 + C445 *0.1U/50V_6 + C427 *0.1U/50V_6 + C433 *2.2U/6.3V_6

L38 *0_6/S → +1.2V

AMD : Change from inductance to short pad

AMD : Remove Cap for internal clock

PCIE_VDDR--PCIE I/O power — 844mA

+1.2V_PCIE_VDDR

+1.2V → L69 BLM18PG181SN1D(180,1.5A)_6

C431 10U/6.3V_8 + C466 1U/10V_4 + C438 1U/10V_4 + C473 1U/10V_4 + C447 0.1U/10V_4 + C437 0.1U/10V_4

AMD : Change from 1u to 0.1u

PCIE_VDDR_1 P18
PCIE_VDDR_2 P19
PCIE_VDDR_3 P20
PCIE_VDDR_4 P21
PCIE_VDDR_5 R22
PCIE_VDDR_6 R24
PCIE_VDDR_7 R25

A-LINK I/O

S5_3.3--3.3V standby power

+3VALW_R

S5_3.3V_1 A17
S5_3.3V_2 A24
S5_3.3V_3 B17
S5_3.3V_4 J4
S5_3.3V_5 J5
S5_3.3V_6 L1
S5_3.3V_7 L2

3.3V_S5 I/O

0.01A

C455 0.1U/10V_4 + C563 0.1U/10V_4 + C461 2.2U/6.3V_6 + C448 10U/6.3V_8

R239 *0_6/S → +3VS5

Change to 0603

AMD : Change from 1u to 0.1u

S5_1.2V--1.2V standby power

S5_1.2V_1 G2
S5_1.2V_2 G4

CORE S5

0.22A

C827 1U/10V_4 + C825 1U/10V_4

+1.2V_S5

USB_PHY_1.2V_1 A10
USB_PHY_1.2V_2 B10

0.2A

+1.2V_USB_PHY_R

AMD : Change from 1u to 0.1u

AVDD_SATA--SATA phy power — 0.2A

+1.2V_AVDD_SATA

+1.2V → L70 BLM18PG181SN1D(180,1.5A)_6

C816 22U/6.3V_8 + C812 0.1U/10V_4 + C818 0.1U/10V_4 + C817 1U/10V_4 + C813 1U/10V_4

AVDD_SATA_1 AA14
AVDD_SATA_4 AB18
AVDD_SATA_2 AA15
AVDD_SATA_3 AA17
AVDD_SATA_5 AC18
AVDD_SATA_6 AD17
AVDD_SATA_7 AE17

SATA I/O

For support USB wakeup-->3V_S5
AVDDTX--USB Phy Analog I/O power — 0.2A

+3V_AVDD_USB

+3VS5 → L40 BLM18PG181SN1D(180,1.5A)_6

C493 10U/6.3V_8 + C484 10U/6.3V_8 + C814 0.1U/10V_4 + C483 0.1U/10V_4

C482 1U/10V_4 + C503 1U/10V_4 + C811 1U/10V_4 + C477 0.1U/10V_4 + C476 0.1U/10V_4 + C478 0.1U/10V_4 + C502 0.1U/10V_4

AVDDTX_0 A16
AVDDTX_1 B16
AVDDTX_2 C16
AVDDTX_3 D16
AVDDTX_4 D17
AVDDTX_5 E17
AVDDRX_0 F15
AVDDRX_1 F17
AVDDRX_2 F18
AVDDRX_3 G15
AVDDRX_4 G17
AVDDRX_5 G18

USB I/O

V5_VREF--PCI 5V TOLERANCE

V5_VREF AE7 ← +5V_VREF — 4mA — R479 1K/F_4 → +5V

AVDDCK_3.3V J16 ← +3V_AVDDCK — 7mA

AVDDCK_1.2V K17 ← +1.2V_AVDDCK — 44mA — C823 1U/10V_4

AVDDC E9 ← +3V_AVDDC — 16mA

D27 CH501H-40PT → +3V

PLL

USB_PHY_1.2V--USB Phy digital power

+1.2V_S5 → R262 *0_6/S → +1.2V_USB_PHY_R

C507 0.1U/10V_4 + C508 0.1U/10V_4 + C499 10U/6.3V_8

AVDDC--USB Analog PLL power

+3VS5 → L44 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDC

C505 0.1U/10V_4 + C496 10U/6.3V_8

AVDDCK_1.2--USB Phy digital power

+1.2V → L39 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_AVDDCK

C480 2.2U/6.3V_6

AVDDCK_3.3--Analog system PLL power

+3V → L43 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDCK

C486 2.2U/6.3V_6

U31E SB710 Part 5 of 5

AVSS_SATA_1 T10
AVSS_SATA_2 U10
AVSS_SATA_3 U11
AVSS_SATA_4 U12
AVSS_SATA_5 V11
AVSS_SATA_6 V14
AVSS_SATA_7 W9
AVSS_SATA_8 Y9
AVSS_SATA_9 Y11
AVSS_SATA_10 Y14
AVSS_SATA_11 Y17
AVSS_SATA_12 AA9
AVSS_SATA_13 AB9
AVSS_SATA_14 AB11
AVSS_SATA_15 AB13
AVSS_SATA_16 AB15
AVSS_SATA_17 AB17
AVSS_SATA_18 AC8
AVSS_SATA_19 AD8
AVSS_SATA_20 AE8

AVSS_USB_1 A15
AVSS_USB_2 B15
AVSS_USB_3 C14
AVSS_USB_4 D8
AVSS_USB_5 D9
AVSS_USB_6 D11
AVSS_USB_7 D13
AVSS_USB_8 D14
AVSS_USB_9 D15
AVSS_USB_10 E15
AVSS_USB_11 F12
AVSS_USB_12 F14
AVSS_USB_13 G9
AVSS_USB_14 H9
AVSS_USB_15 H17
AVSS_USB_16 J9
AVSS_USB_17 J11
AVSS_USB_18 J12
AVSS_USB_19 J14
AVSS_USB_20 J15
AVSS_USB_21 K10
AVSS_USB_22 K12
AVSS_USB_23 K14
AVSS_USB_24 K15

PCIE_CK_VSS_1 H18
PCIE_CK_VSS_2 J17
PCIE_CK_VSS_3 J22
PCIE_CK_VSS_4 K25
PCIE_CK_VSS_5 M16
PCIE_CK_VSS_6 M17
PCIE_CK_VSS_7 M21
PCIE_CK_VSS_8 P16

AVSSC F9

VSS_1 A2
VSS_2 A25
VSS_3 B1
VSS_4 D7
VSS_5 F20
VSS_6 G19
VSS_7 H8
VSS_8 K9
VSS_9 K11
VSS_10 K16
VSS_11 L4
VSS_12 L7
VSS_13 L10
VSS_14 L11
VSS_15 L12
VSS_16 L14
VSS_17 L16
VSS_18 M6
VSS_19 M10
VSS_20 M11
VSS_21 M13
VSS_22 M15
VSS_23 N4
VSS_24 N12
VSS_25 N14
VSS_26 P6
VSS_27 P9
VSS_28 P10
VSS_29 P11
VSS_30 P13
VSS_31 P15
VSS_32 R1
VSS_33 R2
VSS_34 R4
VSS_35 R9
VSS_36 R10
VSS_37 R12
VSS_38 R14
VSS_39 T11
VSS_40 T12
VSS_41 T14
VSS_42 U4
VSS_43 U14
VSS_44 V6
VSS_45 Y21
VSS_46 AB1
VSS_47 AB19
VSS_48 AB25
VSS_49 AE1
VSS_50 AE24

PCIE_CK_VSS_9 P23
PCIE_CK_VSS_10 R16
PCIE_CK_VSS_11 R19
PCIE_CK_VSS_12 T17
PCIE_CK_VSS_13 U18
PCIE_CK_VSS_14 U20
PCIE_CK_VSS_15 V18
PCIE_CK_VSS_16 V20
PCIE_CK_VSS_17 V21
PCIE_CK_VSS_18 W19
PCIE_CK_VSS_19 W22
PCIE_CK_VSS_20 W24
PCIE_CK_VSS_21 W25

AVSSCK L17

GROUND

SB710

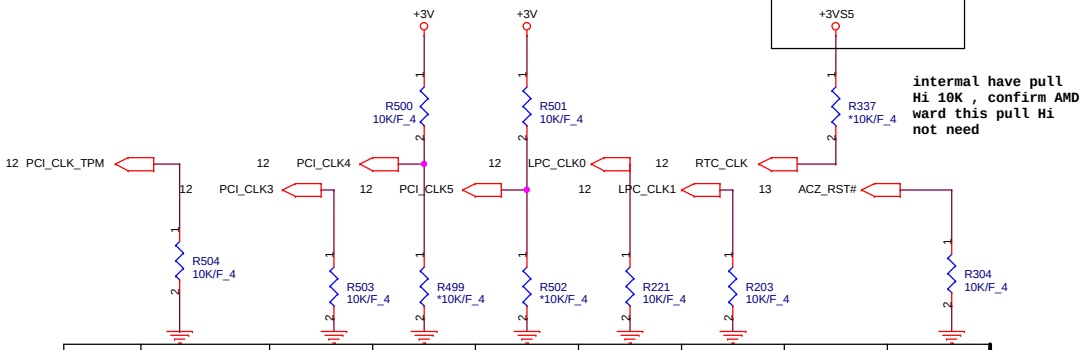
PROJECT : OP8			
Quanta Computer Inc.			
Size: Custom	Document Number: SB700-PWR/DECOUPLING 4/4		Rev: 1A
Date: Friday, March 20, 2009	Sheet 15 of 42		

NB5/RD2

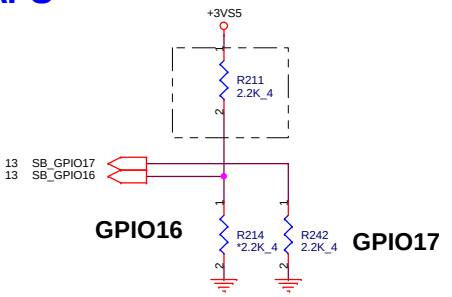
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



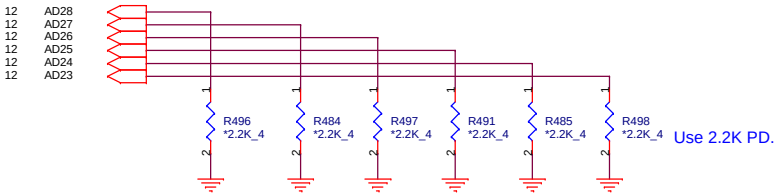
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

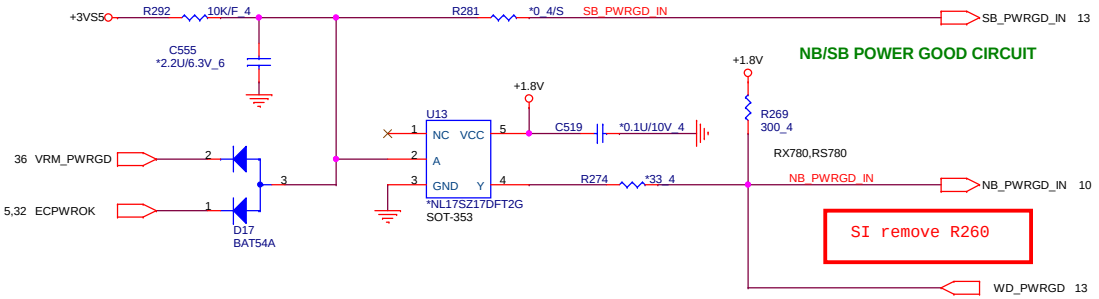
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	1A

Date: Friday, March 20, 2009 Sheet 16 of 42

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

U22A

2.5GT/s bit rate

PCI EXPRESS INTERFACE

9	PEG_TX0	PEG_TX0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	C_PEG_RXP0	C92	0.1U/10V_4
9	PEG_TX#0	PEG_TX#0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	C_PEG_RXN0	C84	0.1U/10V_4
9	PEG_TX1	PEG_TX1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	C_PEG_RXP1	C94	0.1U/10V_4
9	PEG_TX#1	PEG_TX#1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	C_PEG_RXN1	C99	0.1U/10V_4
9	PEG_TX2	PEG_TX2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	C_PEG_RXP2	C100	0.1U/10V_4
9	PEG_TX#2	PEG_TX#2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	C_PEG_RXN2	C112	0.1U/10V_4
9	PEG_TX3	PEG_TX3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	C_PEG_RXP3	C83	0.1U/10V_4
9	PEG_TX#3	PEG_TX#3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	C_PEG_RXN3	C82	0.1U/10V_4
9	PEG_TX4	PEG_TX4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	C_PEG_RXP4	C134	0.1U/10V_4
9	PEG_TX#4	PEG_TX#4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	C_PEG_RXN4	C146	0.1U/10V_4
9	PEG_TX5	PEG_TX5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	C_PEG_RXP5	C120	0.1U/10V_4
9	PEG_TX#5	PEG_TX#5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	C_PEG_RXN5	C131	0.1U/10V_4
9	PEG_TX6	PEG_TX6	Y30	PCIE_RX6P	PCIE_TX6P	AB27	C_PEG_RXP6	C153	0.1U/10V_4
9	PEG_TX#6	PEG_TX#6	W31	PCIE_RX6N	PCIE_TX6N	AB26	C_PEG_RXN6	C156	0.1U/10V_4
9	PEG_TX7	PEG_TX7	W29	PCIE_RX7P	PCIE_TX7P	Y27	C_PEG_RXP7	C164	0.1U/10V_4
9	PEG_TX#7	PEG_TX#7	V28	PCIE_RX7N	PCIE_TX7N	Y26	C_PEG_RXN7	C171	0.1U/10V_4
9	PEG_TX8	PEG_TX8	V30	PCIE_RX8P	PCIE_TX8P	W24	C_PEG_RXP8	C187	0.1U/10V_4
9	PEG_TX#8	PEG_TX#8	U31	PCIE_RX8N	PCIE_TX8N	W23	C_PEG_RXN8	C199	0.1U/10V_4
9	PEG_TX9	PEG_TX9	U29	PCIE_RX9P	PCIE_TX9P	V27	C_PEG_RXP9	C183	0.1U/10V_4
9	PEG_TX#9	PEG_TX#9	T28	PCIE_RX9N	PCIE_TX9N	U26	C_PEG_RXN9	C172	0.1U/10V_4
9	PEG_TX10	PEG_TX10	T30	PCIE_RX10P	PCIE_TX10P	U24	C_PEG_RXP10	C210	0.1U/10V_4
9	PEG_TX#10	PEG_TX#10	R31	PCIE_RX10N	PCIE_TX10N	U23	C_PEG_RXN10	C223	0.1U/10V_4
9	PEG_TX11	PEG_TX11	R29	PCIE_RX11P	PCIE_TX11P	T26	C_PEG_RXP11	C225	0.1U/10V_4
9	PEG_TX#11	PEG_TX#11	P28	PCIE_RX11N	PCIE_TX11N	T27	C_PEG_RXN11	C234	0.1U/10V_4
9	PEG_TX12	PEG_TX12	P30	PCIE_RX12P	PCIE_TX12P	T24	C_PEG_RXP12	C236	0.1U/10V_4
9	PEG_TX#12	PEG_TX#12	N31	PCIE_RX12N	PCIE_TX12N	T23	C_PEG_RXN12	C246	0.1U/10V_4
9	PEG_TX13	PEG_TX13	N29	PCIE_RX13P	PCIE_TX13P	P27	C_PEG_RXP13	C249	0.1U/10V_4
9	PEG_TX#13	PEG_TX#13	M28	PCIE_RX13N	PCIE_TX13N	P26	C_PEG_RXN13	C253	0.1U/10V_4
9	PEG_TX14	PEG_TX14	M30	PCIE_RX14P	PCIE_TX14P	P24	C_PEG_RXP14	C269	0.1U/10V_4
9	PEG_TX#14	PEG_TX#14	L31	PCIE_RX14N	PCIE_TX14N	P23	C_PEG_RXN14	C270	0.1U/10V_4
9	PEG_TX15	PEG_TX15	L29	PCIE_RX15P	PCIE_TX15P	M27	C_PEG_RXP15	C256	0.1U/10V_4
9	PEG_TX#15	PEG_TX#15	K30	PCIE_RX15N	PCIE_TX15N	N26	C_PEG_RXN15	C264	0.1U/10V_4

2	EXT_GFX_CLKP	EXT_GFX_CLKP	AK30	PCIE_REFCLKP					
2	EXT_GFX_CLKN	EXT_GFX_CLKN	AK32	PCIE_REFCLKN					
			L9	NC#1					
			N9	NC#2					
			N10	NC_PWRGOOD					
12	PCIE_RST#		AL27	PERSTB					

CLOCK

CALIBRATION

PCIE_CALRP	Y22	M72_PCIE_CALRP	R72	1.27K/F_4	
PCIE_CALRN	AA22	M72_PCIE_CALRN	R71	2K/F_4	+1.1V_PCIE_VDDC

SI Add

10K/F_4 R533

M92-S2

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

U22G

DP E/F POWER

+1.8V_DPE_VDD18	AG15	DPE_VDD18#1	
	AG16	DPE_VDD18#2	
+1.1V_DPE_VDD10	AG20	DPE_VDD10#1	
	AG21	DPE_VDD10#2	
	AG14	DPE_VSSR#1	
	AH14	DPE_VSSR#2	
	AM14	DPE_VSSR#3	
	AM16	DPE_VSSR#4	
	AM18	DPE_VSSR#5	
+1.8V_DPE_VDD18	AF16	DPF_VDD18#1	
	AG17	DPF_VDD18#2	
+1.1V_DPE_VDD10	AF22	DPF_VDD10#1	
	AG22	DPF_VDD10#2	
	AF23	DPF_VSSR#1	
	AG23	DPF_VSSR#2	
	AM20	DPF_VSSR#3	
	AM22	DPF_VSSR#4	
	AM24	DPF_VSSR#5	
R51 150/F_4	AF17	DPEF_CALR	

DP A/B POWER

	AE11	NC_DPA_VDD18#1	+1.8V
	AE11	NC_DPA_VDD18#2	
	AF6	DPA_VDD10#1	+1.1V_DPB_VDD10
	AF7	DPA_VDD10#2	
	AE1	DPA_VSSR#1	
	AE3	DPA_VSSR#2	
	AG1	DPA_VSSR#3	
	AG6	DPA_VSSR#4	
	AH5	DPA_VSSR#5	
	AE13	NC_DPB_VDD18#1	+1.8V
	AF13	NC_DPB_VDD18#2	
	AF8	DPB_VDD10#1	+1.1V
	AF9	DPB_VDD10#2	
	AE10	DPB_VSSR#1	
	AG9	DPB_VSSR#2	
	AH8	DPB_VSSR#3	
	AM6	DPB_VSSR#4	
	AM8	DPB_VSSR#5	
AE10 R63 150/F_4		DPAB_CALR	

1.1V(S100,D200mA)

BLM18PG181SN1D(180,1.5A)_6 L59

C677 0.1U/10V_4 C698 10U/6.3V_8 C118 1000P/50V_4

DP PLL POWER

+1.8V_DPE_PVDD	AG18	DPE_PVDD	
+1.8V_DPE_PVDD	AF19	DPE_PVSS	
+1.8V_DPE_PVDD	AG19	NC_DPF_PVDD	
+1.8V_DPE_PVDD	AF20	NC_DPF_PVSS	
	AG8	DPA_PVDD	+1.8V_DPA_PVDD
	AG7	DPA_PVSS	
	AG10	DPB_PVDD	+1.8V_DPA_PVDD
	AG11	DPB_PVSS	

M92-S2

+1.1V_DPE_VDD10 — 1.1V(S100,D200mA) — L51 BLM18PG181SN1D(180,1.5A)_6 — +1.1V
C114 0.1U/10V_4, C104 1000P/50V_4, C648 10U/6.3V_8

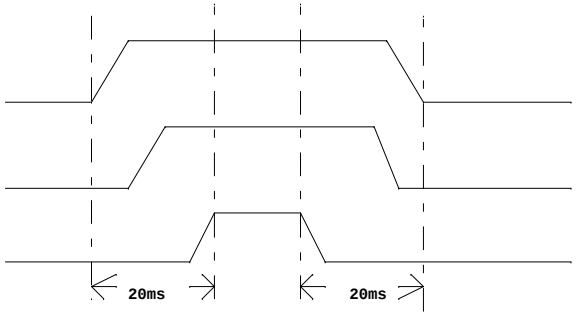
+1.8V_DPA_PVDD — 1.8V(40mA) — L54 BLM18PG181SN1D(180,1.5A)_6 — +1.8V
C658 0.1U/10V_4, C663 1000P/50V_4, C649 10U/6.3V_8

+1.8V_DPE_PVDD — 1.8V(20mA) — L10 BLM18PG181SN1D(180,1.5A)_6 — +1.8V
C54 0.1U/10V_4, C53 1000P/50V_4, C52 10U/6.3V_8

SI remove DPB power source

+1.8V_DPE_VDD18 — 1.8V -(300mA) — L12 BLM18PG181SN1D(180,1.5A)_6 — +1.8V
C111 0.1U/10V_4, C103 1U/10V_4, C56 10U/6.3V_8

VGA Core BPP
VGA Core VDDC
+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1
3.3V_Delay VDDR3



PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M7X/M8X_PCIE_Interface	1A

NB5/RD2

Date: Friday, March 20, 2009 Sheet 17 of 42

R414 10K/F_4 GPIO22

GPIO22(ROMCS#)
PD without external VBIOS ROM

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix	64*16-500MHZ	H5P51G63EFR-20L
0001	Samsung (E die)	64*16-500MHZ	K4N1G164QE-HC20
0010	Qimonda (Infineon)	64*16-500MHZ	TBD
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

U22B

M93-S3/M92-S2

DVCNTL_0/ DVPDATA_18
DVCNTL_1 / NC
DVCNTL_2 / NC
DVDATA_12 / DVPDATA_16
DVDATA_9 / DVPDATA_12
DVDATA_8 / DVPDATA_14
DVDATA_7 / DVPCNTL_0
DVDATA_6 / DVPDATA_8
DVDATA_5 / DVPDATA_6
DVDATA_4 DVPDATA_4
DVDATA_3 / DVPDATA_19
DVDATA_1 / DVPDATA_2
DVDATA_0 / DVPDATA_0

DVO

DPC_VDD18#2/DVPDAT23
DVDATA_10 / DVPDATA_22
DVDATA_2 / DVPDATA_21
DVDATA_11 / DVPDATA_20

M93-S3/M92-S2

DPC_PVDD / DVPDATA_11
DPC_VDD18#1/DVPDAT10
DPC_VDD10#1/DVPDAT15
DPC_VDD10#2/DVPDAT17
DPC_VSSR#1 / DVPCLK
DPC_VSSR#2 / DVPDAT5
DPC_VSSR#5/ DVPCNTL_MV0

DPA

TXCAP_DPA3P
TXCAM_DPA3N
TX0P_DPA2P
TX0M_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N

DPB

TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N

M92-S2/M93-S3

DVPDATA_3/TXCCP_DPC3P
DVPCNTL_2/TXCCM_DPC3N
DVPDATA_7 / TX0P_DPC2P
DVPDATA_1 / TX0M_DPC2N
DVPCNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPCNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR

DPC

M92-S2: Use 0R to VDDR4

+VDDR4 R69 0_4

I2C

SCL
SDA

GENERAL PURPOSE I/O

GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
GPIO_29
GPIO_30

JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN

GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
HPD1

VREFG

PLL/CLOCK

DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT

DPLUS
DMINUS
THERMAL

TS_FDO
TSVDD
TSVSS

M92-S2

DAC1

R
RB
G
GB
B
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1DI
VSS1DI

M92-S2/M93-S3

R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC

DAC2

C / NC
Y / NC
COMP / NC
H2SYNC
V2SYNC
VDD2DI / NC
VSS2DI / NC
A2VDD / NC
A2VDDQ / NC
A2VSSQ
R2SET / NC

DDC/AUX

DDC1CLK
DDC1DATA
AUX1P
AUX1N
DDC2CLK
DDC2DATA
AUX2P
AUX2N
DDCCLK_AUX5P
DDCDATA_AUX5N
DDC6CLK
DDC6DATA
DDCCLK_AUX3P
DDCDATA_AUX3N
NC#1
NC#2

SI Add GND from Check list

SI Add GND from Check list

Need check again

SI Add from AMD check list

1.8V_AVDD_Q 1.8V(70mA) L57 BLM18PG181SN1D(180,1.5A)_6 C659 10U/6.3V_8 C674 C673 0.1U/10V_4 1U/10V_4

1.8V_A2VDD_Q 1.8V(70mA) L52 BLM18PG181SN1D(180,1.5A)_6 C651 10U/6.3V_8 C650 C124 0.1U/10V_4 1U/10V_4

VDDD1 1.8V(45mA VDD1DI) L49 BLM18PG181SN1D(180,1.5A)_6 C641 10U/6.3V_8 C632 C654 0.1U/10V_4 1U/10V_4

VDDD2 1.8V(45mA VDD1DI) L9 BLM18PG181SN1D(180,1.5A)_6 C46 10U/6.3V_8 C113 C48 0.1U/10V_4 1U/10V_4

CL=20PF Y7 *27MHZ R388 10M_6 C657 C656 22P/50V_4 EVGA-XTALI EVGA-XTALO For Int Clk 27Mhz

1.8V(120mADPLL_PVDD) BLM18PG181SN1D(180,1.5A)_6 L63 C652 10U/6.3V_8 C644 1U/10V_4 C110 0.1U/10_4

1.1V(300mA DPLL_VDDC) BLM18PG181SN1D(180,1.5A)_6 L8 C59 10U/6.3V_8 C51 1U/10V_4 C123 0.1U/10V_4

1.8V(20mA TSVDD) BLM18PG181SN1D(180,1.5A)_6 L11 C55 10U/6.3V_8 C61 1U/10V_4 C143 0.1U/10V_4

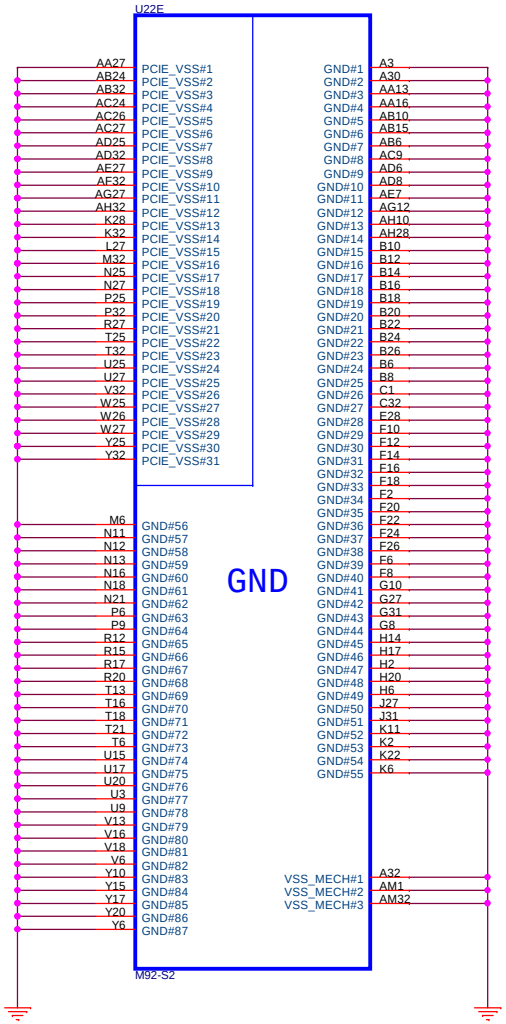
Thermal Sensor U3 G781-1P8@EV SMCLK SMDATA -ALT GND VCC DXP DXN -OVT C64 C78 R42 R55 R54 R53 R39 I2C ADDRESS: 9AH

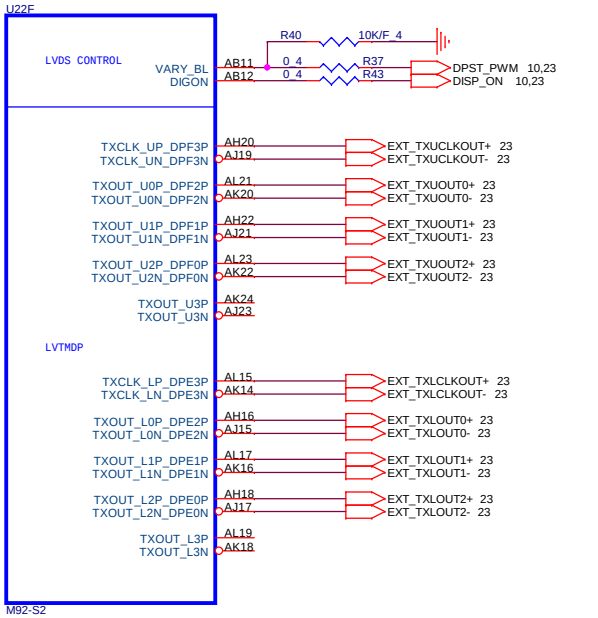
w/s 10 / 10

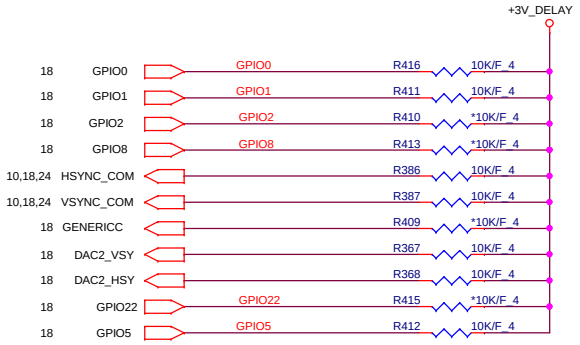
PROJECT : OP8
Quanta Computer Inc.

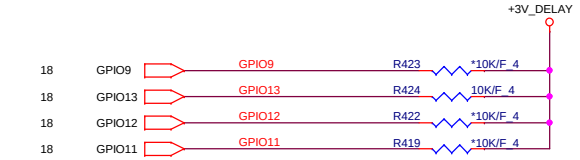
Size	Document Number	Rev
Custom	M7X/M8X_Main	1A
Date: Friday, March 20, 2009	Sheet 18 of 42	

N85/RD2









Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	· **PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		1
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VIP_DEVICE_STRAP_DIS	DAC2_VSY	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	DAC2_HSY		0
CCBYPASS	GENERICC		0

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M7X/M8X_GND / LVDS/ Straps	1A
Date: Friday, March 20, 2009	Sheet 19 of 42	

VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

U22D

MEM I/O
LEVEL TRANSLATION
M93-S3/M92-S2 I/O
MEM CLK
PLL
BACK BIAS
POWER
PCIE
CORE
ISOLATED CORE I/O

1.8V(2.2A VDDR1+VDDRHA)

C247 1U/10V_4, C251 1U/10V_4, C748 1U/10V_4, C233 1U/10V_4, C245 1U/10V_4, C248 1U/10V_4, C254 1U/10V_4, C243 1U/10V_4, C109 0.1U/10V_4, C102 1U/10V_4

C380 10U/6.3V_8, C368 10U/6.3V_8, C635 10U/6.3V_8, C280 10U/6.3V_8, C285 0.1U/10V_4

1.8V(136mA VDD_CT)

L14 BLM18PG181SN1D(180,1.5A)_6

C72 10U/6.3V_8, C145 1000P/50V_4, C163 0.1U/10V_4

Q7 AO3409

Gated 3.3V 60mA by VDDC

VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

R31 100K/F_4

C633 1U/10V_4, C157 1U/10V_4, C130 0.1U/10V_4

1.8V(170mA VDDR5)

L16 BLM18PG181SN1D(180,1.5A)_6

C97 10U/6.3V_8, C105 1U/10V_4, C170 1U/10V_4, C179 0.1U/10V_4

1.8V(170mA VDDR4)

L62 BLM18PG181SN1D(180,1.5A)_6

C702 10U/6.3V_8, C711 1U/10V_4, C165 0.1U/10V_4

D3 CH501H-40PT L-F

Q8 2N7002E

R23 68.1K_4

C45 0.1U/10V_4

L22 BLM18PG181SN1D(180,1.5A)_6

C227 10U/6.3V_8, C229 0.1U/10V_4

1.8V(68mA PCIE_PVDD)

L56 BLM18PG181SN1D(180,1.5A)_6

C665 10U/6.3V_8, C664 0.1U/10V_4

0.95V~1.1V(35mA SPV10)

L63 BLM18PG181SN1D(180,1.5A)_6

C732 10U/6.3V_8, C266 0.1U/10V_4

1.5/1.8V 120mA

C222 1U/10V_4, C231 0.1U/10V_4

*BLM18PG181SN1D(180,1.5A)_6

L23

+1.8V or +1.1V @ 1A MAX

Q13 2N7002E, Q12 ME2303T1

R64 100K/F_4

Q11 2N7002E

VDD_R4 -- Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDD_R5 -- Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

1.8V(500mA)

C125 0.1U/10V_4, C682 1U/10V_4, C691 1U/10V_4, C144 1U/10V_4, C683 1U/10V_4, C678 10U/6.3V_8

BLM18PG181SN1D(180,1.5A)_6

1.1V(2.0A)

L50 BLM21PG221SN1D(220,100M,2A)_8

C196 1U/10V_4, C174 1U/10V_4, C182 1U/10V_4, C219 1U/10V_4, C627 10U/6.3V_8

VDDC+VDDCI 0.95~1.1V(15A peak)(Ripple < 87.2mV)

C639 1U/10V_4, C638 1U/10V_4, C637 1U/10V_4, C211 1U/10V_4, C33 10U/6.3V_8

C161 1U/10V_4, C176 1U/10V_4, C643 1U/10V_4, C190 1U/10V_4, C625 10U/6.3V_8

C173 1U/10V_4, C175 1U/10V_4, C186 1U/10V_4, C626 1U/10V_4, C624 10U/6.3V_8

+BIF_VDDC

SI Add from AMD check list

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

0.95V~1.1V(2A VDDCI)

C228 1U/10V_4, C216 1U/10V_4, C230 1U/10V_4, C217 0.1U/10V_4, C200 10U/6.3V_8

BLM21PG221SN1D(220,100M,2A)_8

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.

Back Bias Enabled: (GPIO_21_BB_EN = 3.3 V): 1.5 V or 1.8 V

Back Bias Disabled: (GPIO_21_BB_EN = 0 V): VDDC

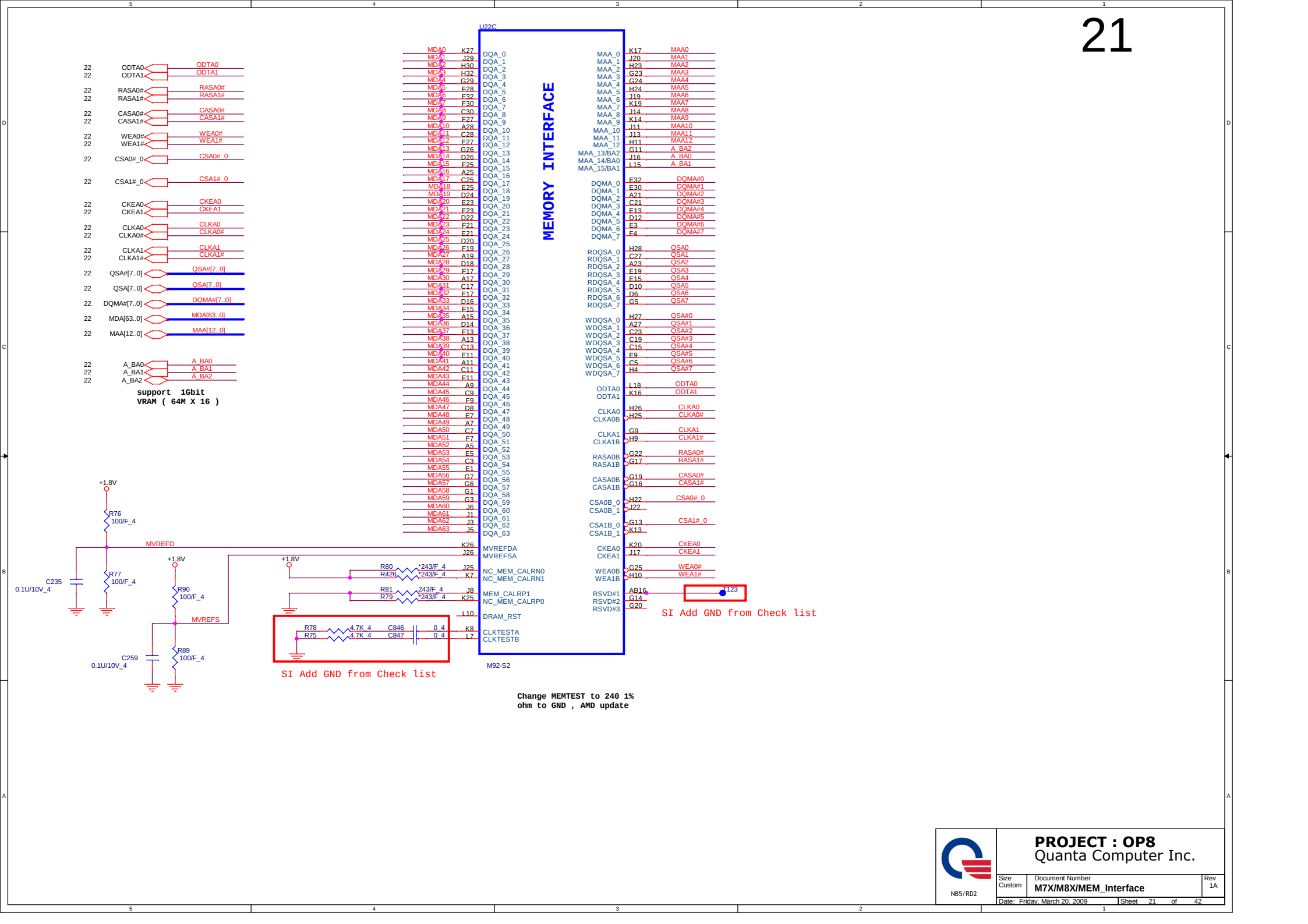
C160 1U/10V_4, C121 0.1U/10V_4, C690 1U/10V_4, C642 10U/6.3V_8, C634 10U/6.3V_8, C32 10U/6.3V_8, C34 10U/6.3V_8

SI Add from AMD check list

HCB1608KF-181T15_6 L73

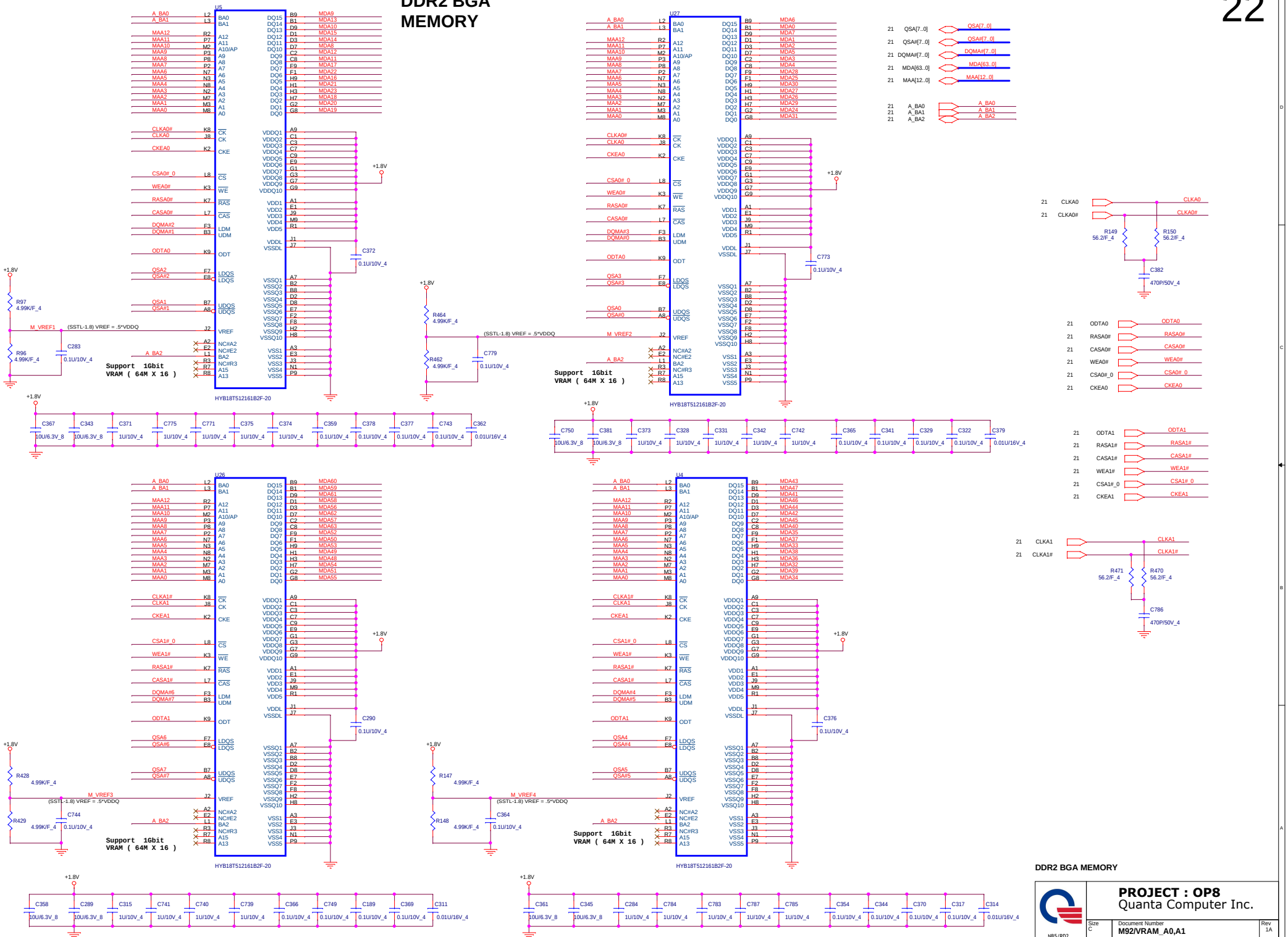
C844 10U/6.3V_8, C845 1U/6.3V_4

PROJECT :	OP8
Quanta Computer Inc.	
Size: Custom	Document Number: M7X/M8X_Power_and_NC
Rev: 1A	
NB5/RD2	
Date: Friday, March 20, 2009	Sheet 20 of 42



PROJECT : OP8	
Quanta Computer Inc.	
Size: Custom	Document Number: M7X/M8X/MEM_Interface
Rev: 1A	
NB5/RD2	
Date: Friday, March 20, 2009	Sheet 21 of 42

DDR2 BGA MEMORY



DDR2 BGA MEMORY

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
C	M92/VRAM_A0,A1	1A

Date: Friday, March 20, 2009 Sheet 22 of 42

NB5/RD2

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB to LVDS for UMA

10	LA_CLK	LA_CLK	RP1	*0_4P2R_4	TXLCLKOUT+
10	LA_CLK#	LA_CLK#			TXLCLKOUT-
10	LA_DATAP0	LA_DATAP0	RP2	*0_4P2R_4	TXLOUT0+
10	LA_DATAN0	LA_DATAN0			TXLOUT0-
10	LA_DATAP1	LA_DATAP1	RP3	*0_4P2R_4	TXLOUT1+
10	LA_DATAN1	LA_DATAN1			TXLOUT1-
10	LA_DATAP2	LA_DATAP2	RP4	*0_4P2R_4	TXLOUT2+
10	LA_DATAN2	LA_DATAN2			TXLOUT2-
10	LB_CLK	LB_CLK	RP5	*0_4P2R_4	TXUCLKOUT+
10	LB_CLK#	LB_CLK#			TXUCLKOUT-
10	LB_DATAP0	LB_DATAP0	RP6	*0_4P2R_4	TXUOUT0+
10	LB_DATAN0	LB_DATAN0			TXUOUT0-
10	LB_DATAP1	LB_DATAP1	RP7	*0_4P2R_4	TXUOUT1+
10	LB_DATAN1	LB_DATAN1			TXUOUT1-
10	LB_DATAN2	LB_DATAN2	RP8	*0_4P2R_4	TXUOUT2-
10	LB_DATAP2	LB_DATAP2			TXUOUT2+

OPTION SIGNAL FROM M92 to LVDS for discrete

19	EXT_TXLCLKOUT-	EXT_TXLCLKOUT-	RP49	0_4P2R_4	TXLCLKOUT-
19	EXT_TXLCLKOUT+	EXT_TXLCLKOUT+			TXLCLKOUT+
19	EXT_TXLOUT0-	EXT_TXLOUT0-	RP50	0_4P2R_4	TXLOUT0-
19	EXT_TXLOUT0+	EXT_TXLOUT0+			TXLOUT0+
19	EXT_TXLOUT1-	EXT_TXLOUT1-	RP51	0_4P2R_4	TXLOUT1-
19	EXT_TXLOUT1+	EXT_TXLOUT1+			TXLOUT1+
19	EXT_TXLOUT2+	EXT_TXLOUT2+	RP52	0_4P2R_4	TXLOUT2+
19	EXT_TXLOUT2-	EXT_TXLOUT2-			TXLOUT2-
19	EXT_TXUCLKOUT-	EXT_TXUCLKOUT-	RP53	0_4P2R_4	TXUCLKOUT-
19	EXT_TXUCLKOUT+	EXT_TXUCLKOUT+			TXUCLKOUT+
19	EXT_TXUOUT0+	EXT_TXUOUT0+	RP54	0_4P2R_4	TXUOUT0+
19	EXT_TXUOUT0-	EXT_TXUOUT0-			TXUOUT0-
19	EXT_TXUOUT1-	EXT_TXUOUT1-	RP55	0_4P2R_4	TXUOUT1-
19	EXT_TXUOUT1+	EXT_TXUOUT1+			TXUOUT1+
19	EXT_TXUOUT2-	EXT_TXUOUT2-	RP56	0_4P2R_4	TXUOUT2-
19	EXT_TXUOUT2+	EXT_TXUOUT2+			TXUOUT2+

+3V — R1 *4.7K_4 EDIDCLK
R2 *4.7K_4 EDIDDATA

+3V_DELAY — R420 4.7K_4 EDIDCLK
R418 4.7K_4 EDIDDATA

+3VLCD — L2 PBY201209T-4A_8 — +3VLCD_CON
C6 10U/6.3V_8
C2 *0.1U/10V_4
C3 0.01U/16V_4

+1.8V — C849 0.1U/10V_4 — +VGA_CORE
+1.8V — C854 0.1U/10V_4 — +VGA_CORE

SI Add for EMI

10,18 LVDS_BLON — LVDS_BLON R12 1K/F_4 — PN_BLON
D1 CH501H-40PT
+3VPCU — R13 33K_6 — BLONCON — C16 22P/50V_4
R11 100K/F_4
LID_EC# — LID_EC# 31,32
HWPG 32,34,35,37,38
12 LCD_BK — LCD_BK Q5 *PDTC144EU
D2 BAT54A

Del R21 and Pull hi R259 to +3VS5, no-stuff Q5, add D7 to HWPG on PV

+12VALW — R6 330K_6 — +5VSUS
AO3404 ID current 5.8A
N-MOS,5.8A Q1 AO3404
+3V — C10 0.1U/10V_4
+3VLCD — R3 22_8
LCDONG — Q2 2N7002E — C11 0.1U/10V_4
R7 100K/F_4
Q4 PDTC144EU
10,19 DISP_ON — R10 2.2K_4
LCDDISCHG
LCDON# — Q3 2N7002E

+3VLCD_CON
+3V — C4 1000P/50V_4
10,18 EDIDCLK
10,18 EDIDDATA
TXLOUT0- TXLOUT0+
TXLOUT1- TXLOUT1+
TXLOUT2- TXLOUT2+
TXLCLKOUT- TXLCLKOUT+
TXUOUT0- TXUOUT0+
TXUOUT1- TXUOUT1+
TXUOUT2- TXUOUT2+
TXUCLKOUT- TXUCLKOUT+
VADJ1
BLONCON
CN1 GS12401-1011-9F

*WCM-2012-900T(400mA)
13 USBP2+
13 USBP2-
+3.9V-CAMARA
L1 4
USBP2+
USBP2-
C14 .01U/16V_4
C15 *4.7U/6.3V_6
+VIN_BLIGHT

+3V — C842 0.047U/10V — U33
10,19 DPST_PWM — DPST_PWM
32 PWM_VADJ — PWM_VADJ
TC7SH08FU
R524 1K_4 — VADJ1
C9 *4.7U/6.3V_6
C8 0.01U/50V_4
R5 *0_4

SI add U33,R524,C842 for Vari bright function

+5V — C17 1U/10V_4
U1 AT5231H-3.9KER
VIN VOUT SHDN GND SET
+3.9V-CAMARA
R1 R9 *215K/F_4
R2 R8 *100K/F_4
C843 4.7U/6.3V_6

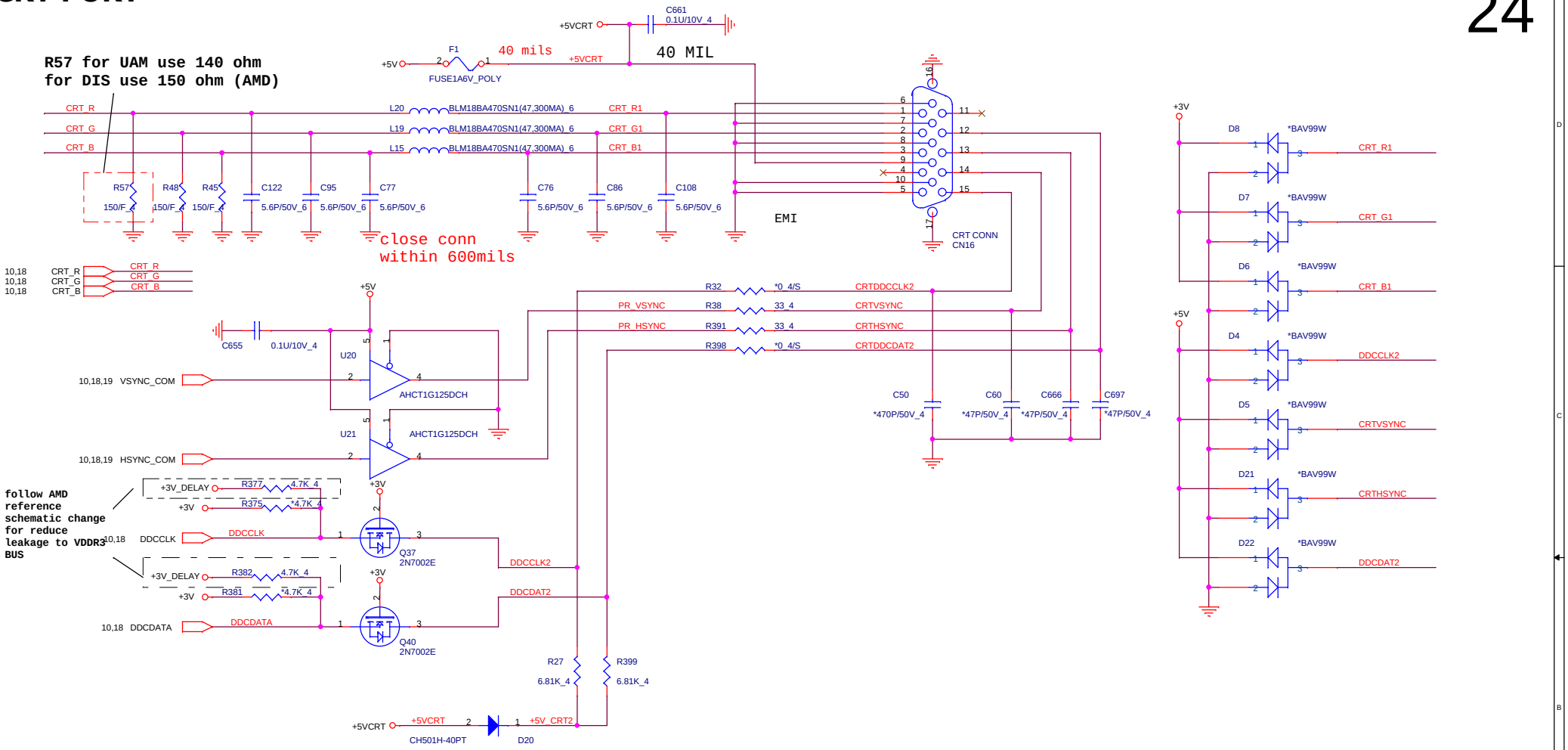
+VIN — L3 FBM2125 HM330-T(4A,0.015)_8 — +VIN_BLIGHT
C13 0.1U/50V_6
C1 0.01U/50V_4
C5 0.1U/50V_6
C12 *10U/25V_12
C7 0.1U/50V_6

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A
Date: Friday, March 20, 2009	Sheet 23 of 42	

CRT PORT



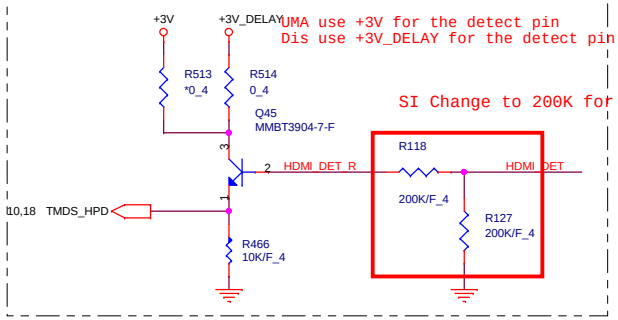
PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT	1A

Date: Friday, March 20, 2009 Sheet 24 of 42

NB5/RD2

HDMI HPD SENSE

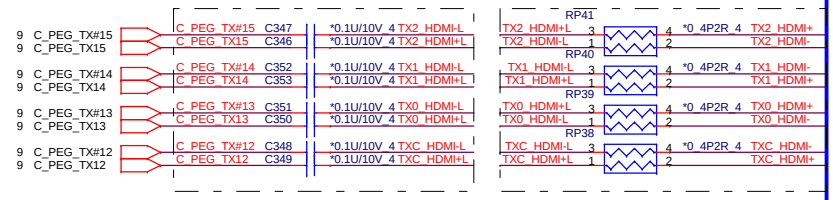


UMA/DISCRETE select for HDMI

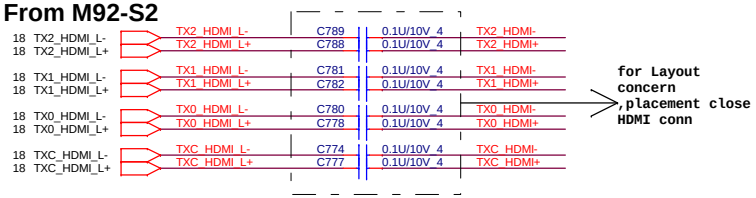
From RS780M

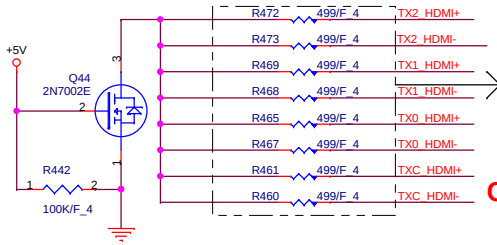
for Layout concern ,placement close north bridge

for Layout concern ,placement close HDMI conn



From M92-S2





UMA RS780M
上 715 ohm CS17152FB17

DIS M92-S
上 499 ohm CS14992FB24

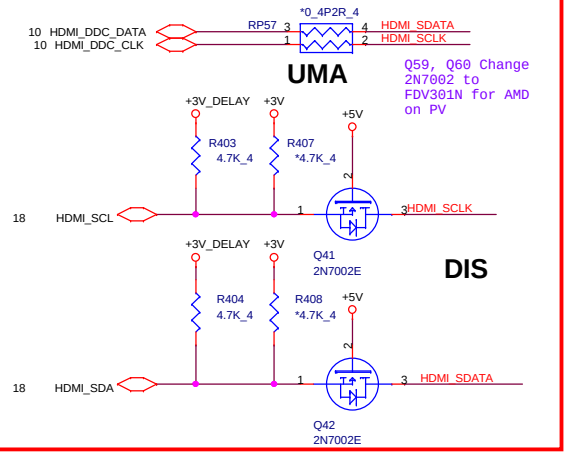
Close to HDMI Connector

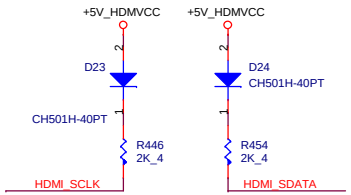
Discrete DDC4 is 5V tolerance , the MOSFET level shifter no need
UMA DDC is 3V tolerance,the MOSFET level shifter is need

SI Change for DIS HDMI

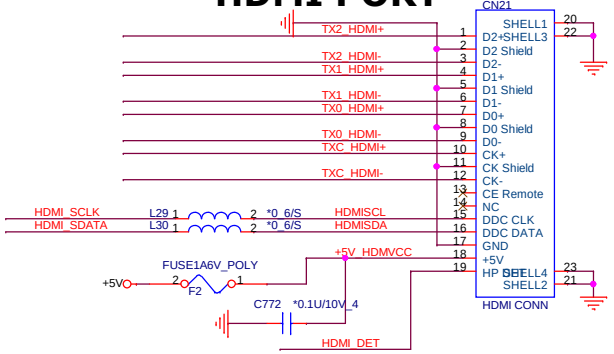
UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector





HDMI PORT



PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	1A

NB5/RD2

Date: Friday, March 20, 2009 | Sheet 25 of 42

For 5158E

2 CLK_48M_CR — CLK_48M_CR

SI remove R350 for langth trace

+3VSUS — R250 100K/F_4

31 CARD_LED#

U14

CF_CD# GPIO0 CF_D10 CF_D9 CF_D2 CF_D8/SM_CD# CF_D1/XD_CD# CF_D0/SM_WPM#/SD_WP CF_A0/SD_CD# CF_DMACK# CF_A1/XD_D4 CF_DMARQ

XD_CD# — SP2 — SD_CD# — SP4

R323 6.19K/F_4 RREF — RREF

13 USBP3- — DM
13 USBP3+ — DP

C610 *5.6P/50V_4 — CLK_48M_CR — 48 XTLO
R327 *270K_4 — *12MHz — Y6
C609 *5.6P/50V_4 — XTLI — 47 XTLI

For 5158 BG6120000717

MODE_SEL — 45 MODE_SEL
R325 10K/04 — C585 *47P/50V_4

For 5158

+3VSUS — R326 100K/F_4 — 5158_RST# — 44 RST# — C591 1U/10V_4

If SD_DAT1 connect to SP4 , MOD_SEL need to let it to N.C

RTS5159

XD_CLE/CF_D3 43 SP19
XD_CE#/CF_D11 42 SP18
XD_ALE/CF_D4 41 SP17
SD_DAT2/XD_RE#/CF_D12 40 SP16
SD_DAT3/XD_WE#/CF_D5 39 SP15
XD_RDY/CF_D13 38 SP14
SD_DAT4/XD_WP#/CF_D6 37 SP13
SD_CMD 36 SD_CMD_R
SD_DAT5/XD_D0/CF_D14 35 SP12
SD_CLK/XD_D1/MS_CLK/CF_D7 34 SP11
SD_DAT6/XD_D7/MS_D3/CF_D15 33 SP10
CF_CS0# 31
MS_INS#/CF_IORD# 30 MS_CD#
SD_DAT7/XD_D2/MS_D2/CF_IOWR# 28 SP8
SD_DAT0/XD_D6/MS_D0/CF_RST# 27 SP7
SD_DAT1/XD_D3/MS_D1/CF_IORDY 26 SP6
XD_D5/MS_BS/CF_A2 25 SP5

AV_PLL_IN 1 — C581 0.1U/10V_4 — C530 1U/10V_4

VREG_OUT 10 VREG — R300 *0_8/S — +3VSUS_RTS — +3VSUS
5V 8
A3V3_IN 3 — C552 0.1U/10V_4 — C557 4.7U/6.3V_6
D3V3_IN 33 — C568 0.1U/10V_4 — C558 0.1U/10V_4

D3V3_OUT 11 — C574 0.1U/10V_4 — C514 4.7U/6.3V_6 — +3VSUS

A3V3_OUT 7 — +3VSUS

CARD_3V3_OUT 9 — +3VCARD

AG33 6
AG_PLL 46 — C538 1U/10V_4
DGND2 32 — C518 0.1U/10V_4 — C573 0.1U/10V_4
DGND1 12

+3VCARD — C532 0.1U/10V_4 — C534 0.1U/10V_4 — C526 0.1U/10V_4

SP6 — R273 *0_4 — SD_DAT1
SP4 — R254 *0_4/S

For 5158

For 5158E

AL005158B10 -->RTS5158E
AL005158B00 -->RTS5158

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

SP7	R280	*0_4/S	MS-D0_SD-D0_XD-D6
SP6	R268	*0_4/S	MS-D1_XD-D3_SD_D1
SP9	R252	*0_4/S	MS-D2_XD-D2
SP16	R343	*0_4/S	XD-RE#_SD-D2
SP5	R259	*0_4/S	MS-BS_XD-D5
SP15	R342	*0_4/S	SD-D3_XD-WE
SP11	R314	*0_4/S	SD-CLK
	R523	*0_4/S	MS-CLK
SP2	R255	*0_4/S	SD-WP
SP13	R507	*0_4/S	XD-WP#
SP19	R345	*0_4/S	XD-CLE
SP4	R253	*0_4/S	XD-D4
SP10	R291	*0_4/S	MS-D3_XD-D7
SP14	R353	*0_4/S	XD-RB#
SP12	R322	*0_4/S	XD-D0
SP17	R354	*0_4/S	XD-ALE
SP18	R344	*0_4/S	XD-CE#
SD_CMD_R	R331	*0_4/S	SD-CMD

SP11 — C572 *27P/50V_4 — Can not more than 30p

5158_RST# — 2 D19 1 — 5158_RST_R# — 5158_RST_R# 13
RB501V-40

Add diode for 5158E cardreader driver lost issue

4 IN1 CARD READER XD,SD,MS/MSP

+3VCARD — R509 *10K/F_4

CN24 — TAI-SOL 144-2300001900

XD_CD#	1 XD-GND1	GND 43	
XD-RB#	2 XD-CD#		
XD-RE#_SD-D2	3 XD-R/B	SD-WP 42	SD-WP
XD-CE#	4 XD-RE	SD-GND1 41	
XD-CLE	5 XD-CE	SD-CD# 40	SD_CD#
XD-ALE	6 XD-CLE	SD-GND2 39	
SD-D3_XD-WE	7 XD-ALE	SD-D2 38	XD-RE#_SD-D2
XD-WP#	8 XD-WE	SD-D1 37	SD_DAT1
	9 XD-WP	SD-D0 36	MS-D0_SD-D0_XD-D6
XD-D0	10 XD-GND2	SD-GND 35	
SP11	11 XD-D0	SD-CLK 34	SD-CLK
MS-D2_XD-D2	12 XD-D1	SD_VCC 33	
MS-D1_XD-D3_SD_D1	13 XD-D2	SD-GND3 32	
XD-D4	14 XD-D3	SD-CMD 31	SD-CMD
MS-BS_XD-D5	15 XD-D4	SD-D3 30	SD-D3_XD-WE
MS-D0_SD-D0_XD-D6	16 XD-D5	MS-GND2 29	
MS-D3_XD-D7	17 XD-D6	MS-VCC 28	
	18 XD-D7	MS-SCLK 27	MS-CLK
	19 XD-VCC	MS-P-D3 26	MS-D3_XD-D7
	20 MS-GND1	MS-INS 25	MS_CD#
MS-BS_XD-D5	21 MS-BS	MS-P-D2 24	MS-D2_XD-D2
MS-D1_XD-D3_SD_D1	22 MS-D1	MS-SDIO 23	MS-D0_SD-D0_XD-D6

+3VCARD — C828 2.2U/6.3V_6 — R481 150K/F_4 — CLOSE CONN

+3VCARD — C829 0.1U/10V_4 — C810 0.1U/10V_4 — C824 0.1U/10V_4

+VIN — C852 0.1U/50V_6
+VIN — C851 0.1U/50V_6
+VIN — C850 0.1U/50V_6

H34 *spad-re63x213np — H35 *spad-c157np — H36 *spad-c157np
H1 *h-tri72bc315d118p2 — H2 *H-TC2368C118D18P2 — H3 *H-C315D118P2 — H4 *H-C315D118P2 — H28 *h-c354d118p2 — H9 *H-TE3-8X9-138C8P2 — H12 *H-TO10X138C8D8P2 — H14 *h-tshiebc3156118p2 — H27 *H-TC2368C118D18P2

H37 *spad-re142x339np — H38 *spad-c157np — H39 *spad-c134np
H23 *H-TE8X98C8D3P2 — H21 *H-C315D118P2 — H19 *H-TC88E8X7_5D3P2 — H24 *H-TC3158C394D118P2 — H22 *H-C315D276P2 — H20 *H-TO9X148C8D3P2 — H26 *H-O236X197D158X118P2 — H29 *h-c354d118p2 — H25 *H-C315D118P2

H40 *spad-op89-2 — H41 *spad-c157np — H42 *spad-c157np
PAD1 *SPAD-RE100X200NP — H11 *H-O79X11807SX118 — H30 *h-tc3545bs3544d18p2 — H31 *h-c354d118p2

H5 *H-C55D55N — H8 *H-C67D67N — H7 *H-197D87P2 — H6 *H-197D87P2

Battery Hole

H43 *spad-c157np — H44 *h-c18d118n — H45 *h-c91d89.1n

H10 *H-C236D181P2 — H15 *H-C236D181P2 — H16 *h-c307d181p2

VGA Hole

H18 *H-C217D181P2 — H13 *H-C217D181P2 — H17 *H-C217D181P2

CPU Hole

+1.8V — C286 0.1U/10V_4 — +Vcore0

Add for EMI request

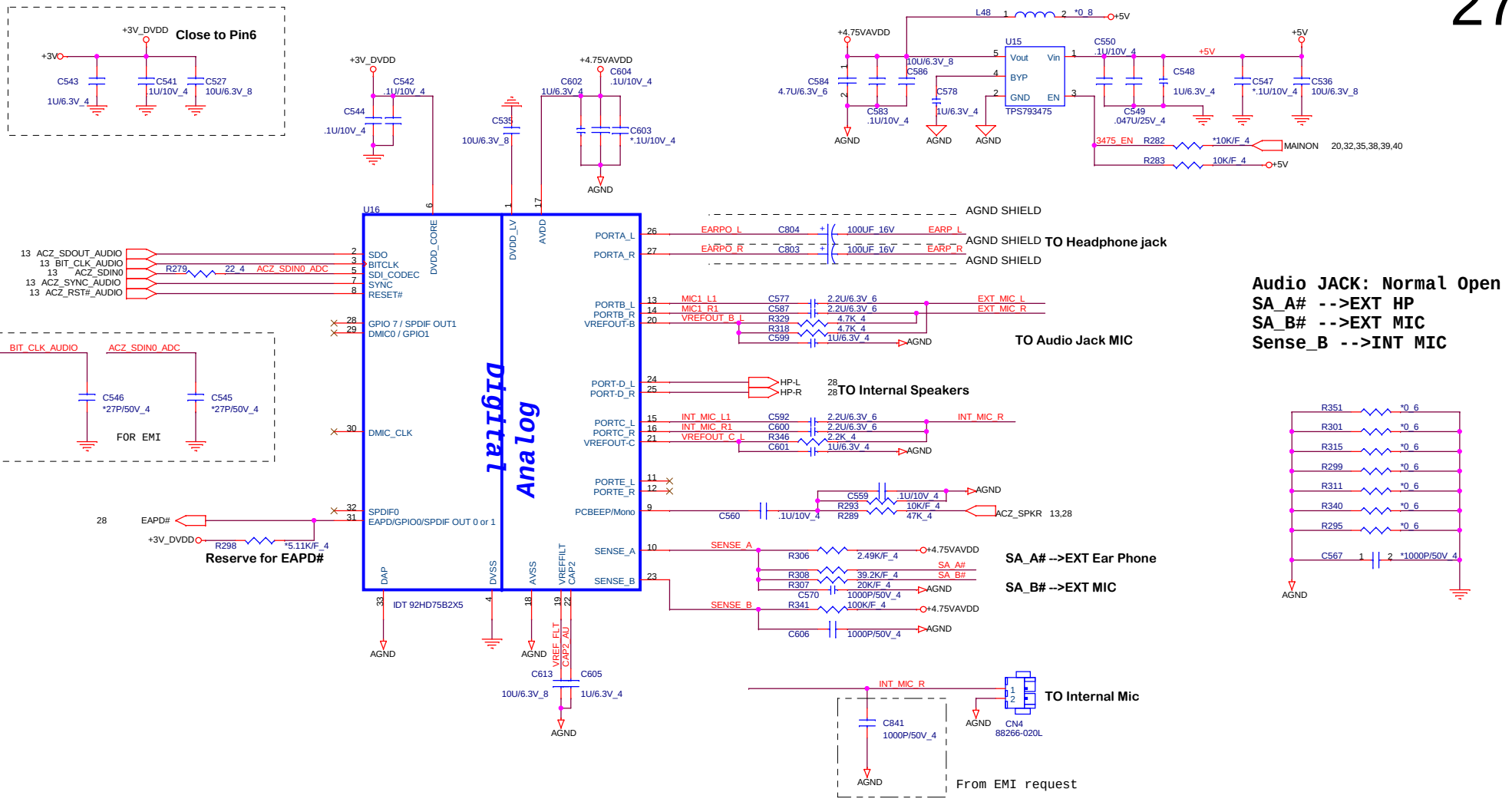
H52 — H51 *h-tc315bc127d87p2 — H46 *H-R103X67D103X67N — H47 *SPAD-RE98X298NP-1 — H48 *SPAD-RE98X298NP-2 — H49 *SPAD-RE59X315NP-1 — H50 *SPAD-RE59X315NP-2

NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

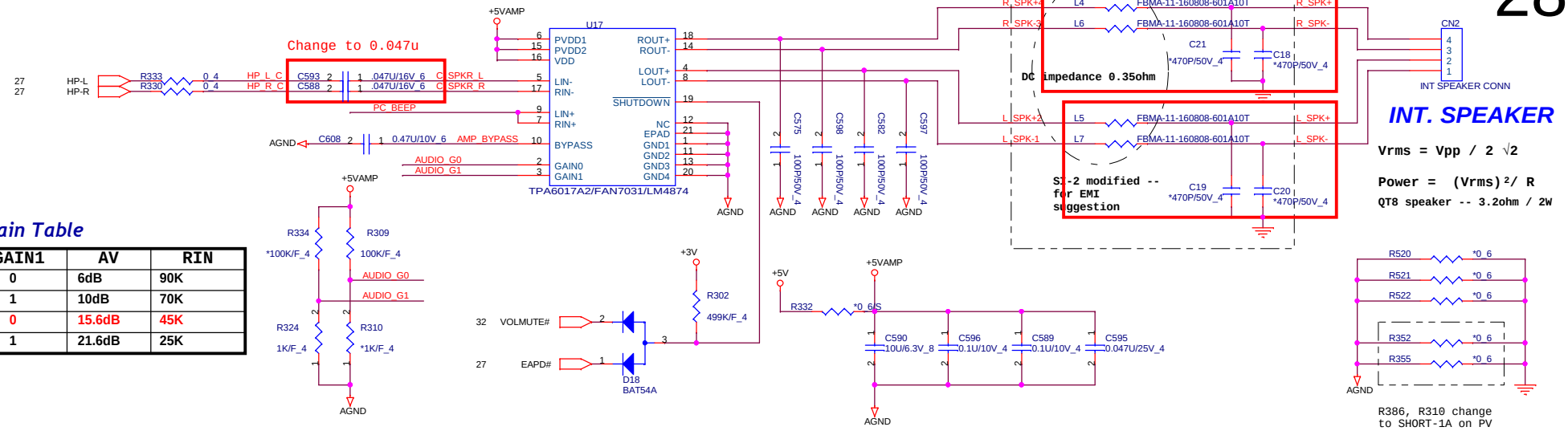
Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	1A

Date: Friday, March 20, 2009 — Sheet 26 of 42



NB5/RD2	**PROJECT : OP8** Quanta Computer Inc.	
Size: Custom	Document Number: **Azalia 92HD75B2X5**	Rev: 1A
Date: Friday, March 20, 2009	Sheet 27 of 42	

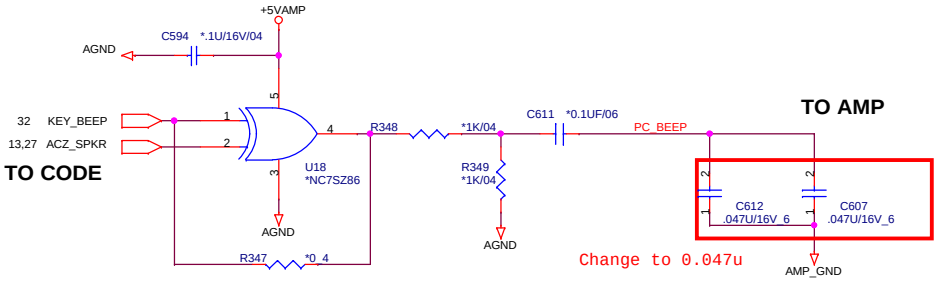
AUDIO AMPLIFIER



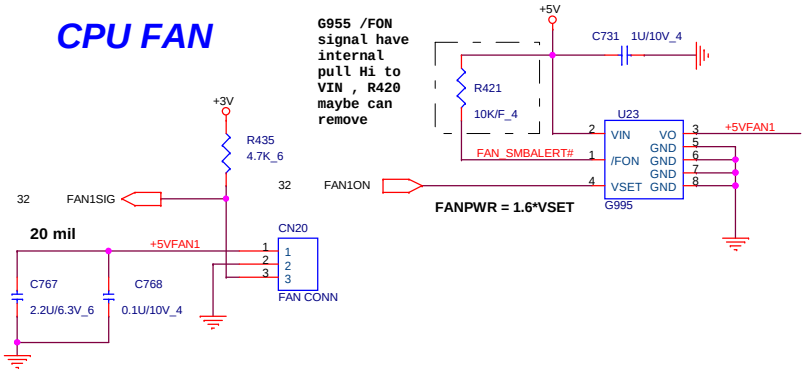
6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

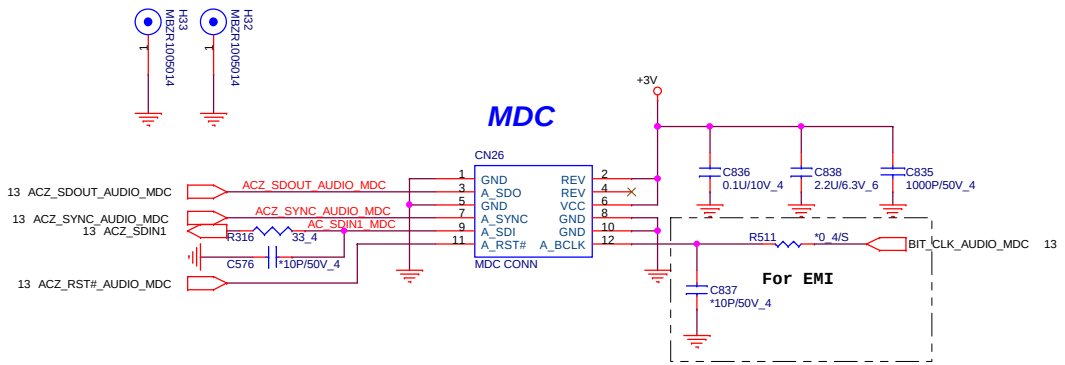
PC-BEEP



CPU FAN

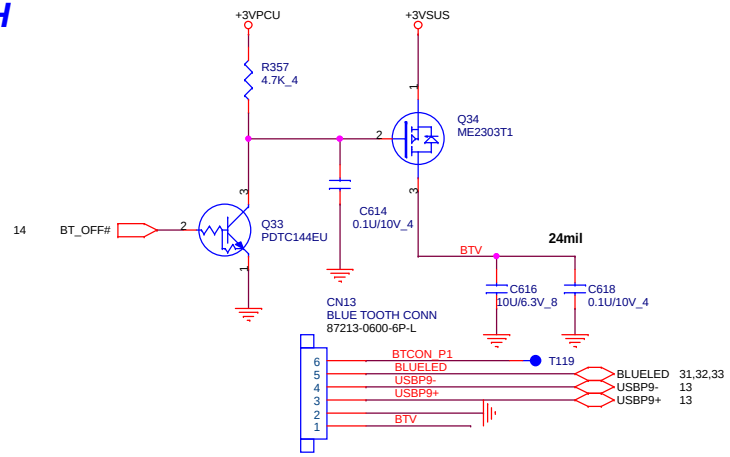


Modem CONN

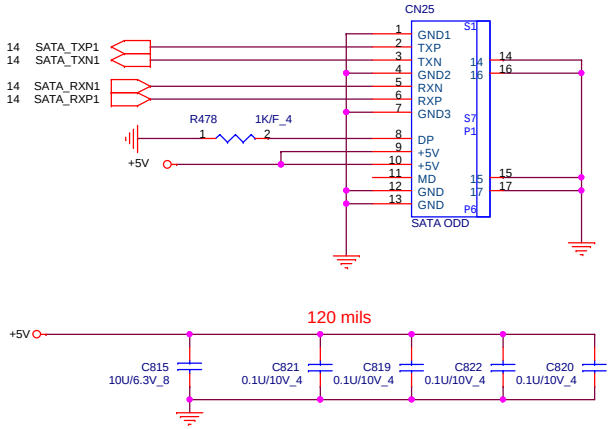


PROJECT : OP8		
Quanta Computer Inc.		
Size: Custom	Document Number: AMP_TPA6017/MDC1.5/CPU FAN	Rev: 1A
NB5/RD2	Date: Friday, March 20, 2009	Sheet 28 of 42

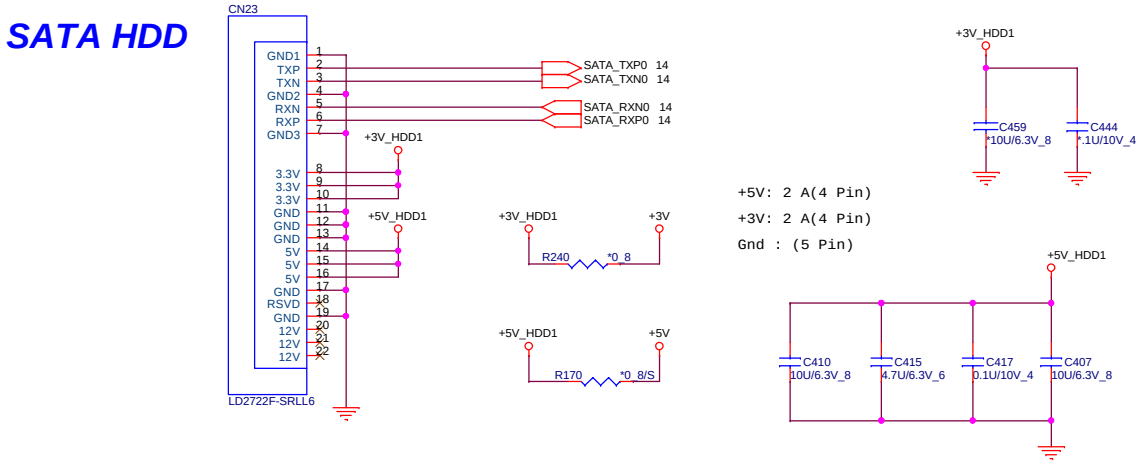
BLUETOOTH



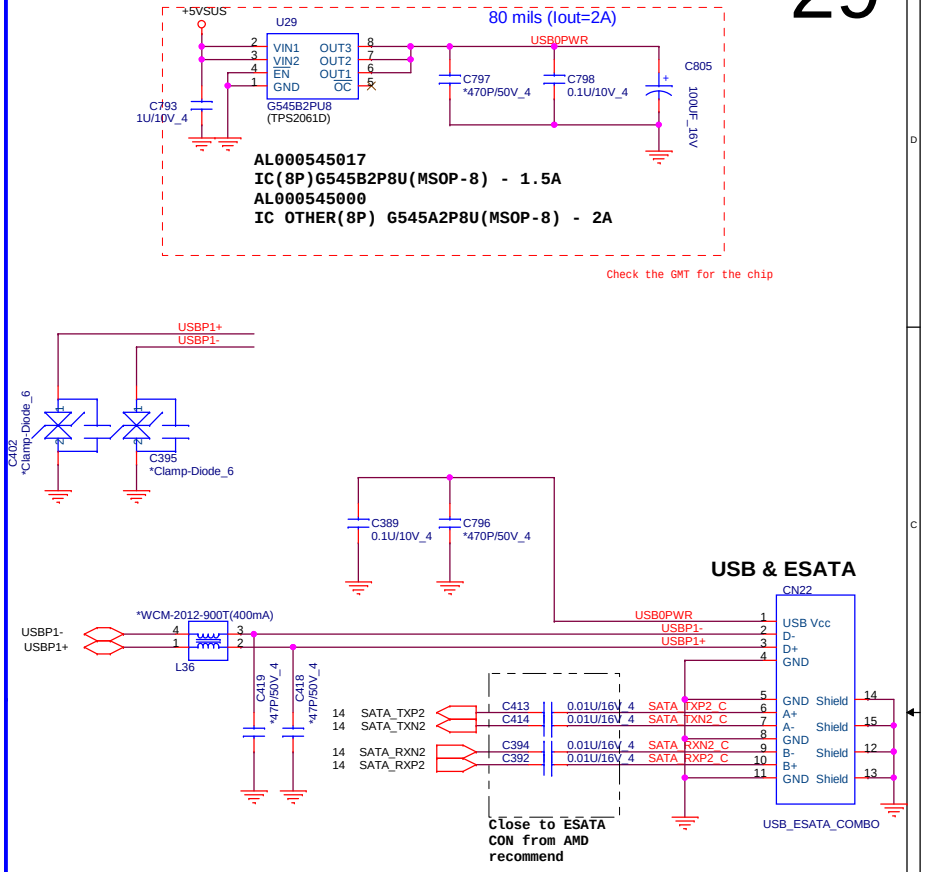
SATA CD-ROM



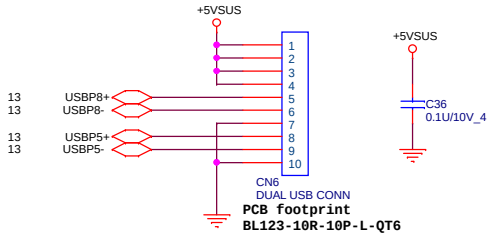
SATA HDD



LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2



PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/USBX3/ESATA/SATA ODD/HDD	1A

Date: Friday, March 20, 2009 Sheet 29 of 42

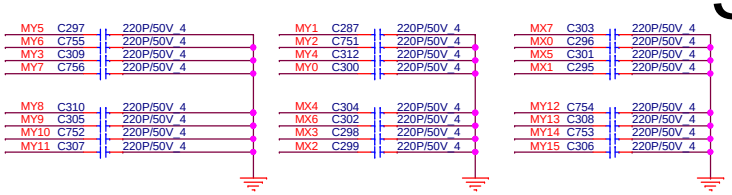
NB5/RD2

Power trace Layout 寬度> 30mil
CLOSE to Pin 10, 13, 30, 36
close to pin 19
LANVCC 1.2W 364mA
CLOSE to Pin 29,37
CLOSE to Pin 1
RTL8103EL
Delete R261 and add D38 as current loss issue
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)
U10
*M93C46-WMN6TP
Check the EEPROM for LAN
DB modified to short-pad
LAN_Transformer
NS681684
Bios need change
Link
Add for EMI request
RJ45
FOR EMI
RJ45_CONN
Fixed RJ45 Pin define (0829)

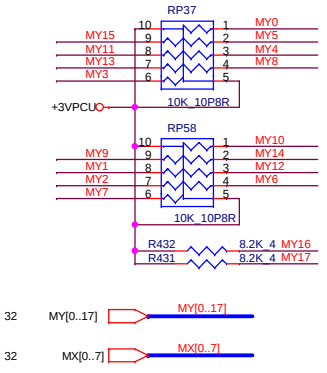
Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	
LED1	O	56	35	
LED2	O	55	34	
LED3	O	54	33	

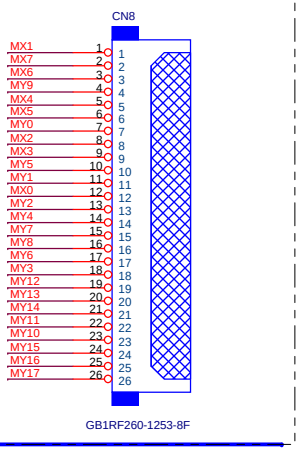
LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

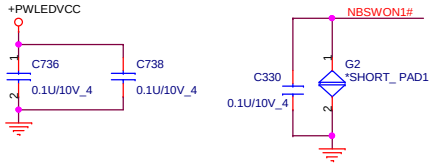
POWER BUTTON CONNECT

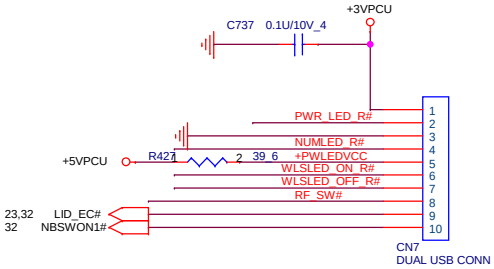


KEYBOARD PULL-UP

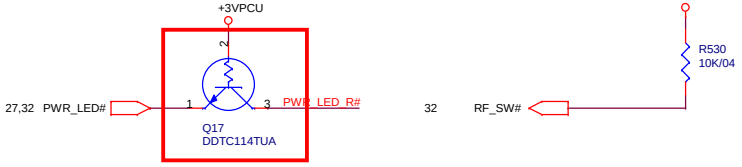




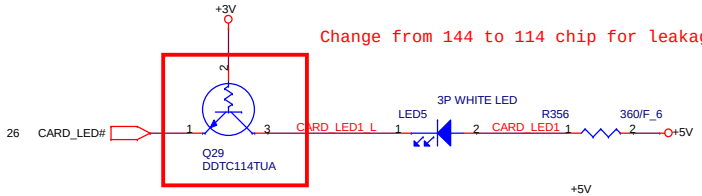


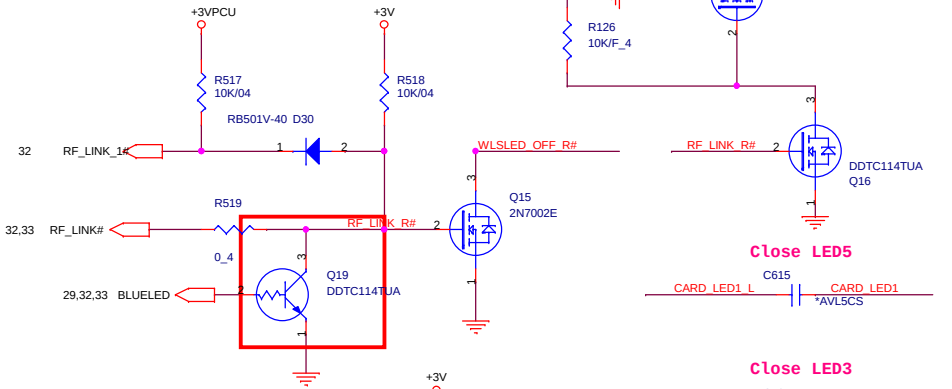


1. +3VPCU(LIDSWITCH PWR)
2. PWR_LED#
3. GND
4. NumLED
5. +5VPCU (PWRLED PWR)
6. WLSLED_ON#
7. WLSLED_OFF#
8. RF_SW#
9. LIDSWITCH
10. POWERON#



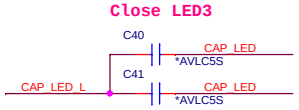
Change from 144 to 114 chip for leakage current



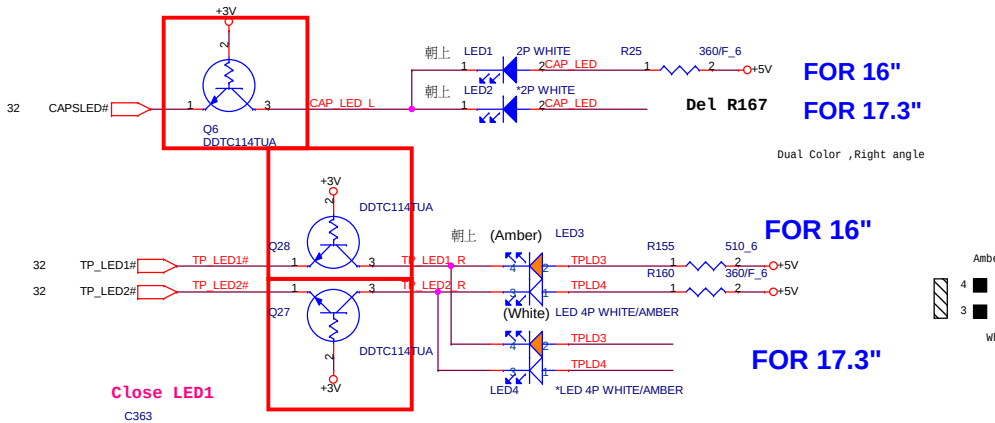


Close LED5

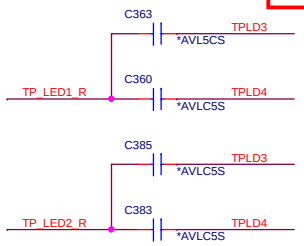
Close LED3



Close LED4



Close LED1



Close LED2

PROJECT : OP8
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW_BOARD	1A

Date: Friday, March 20, 2009 | Sheet 31 of 42

U8 — KB3926

Battery charge/discharge Cap button

VGA thermal system thermal

reserved for H/W CIR

Modify from RF LED control

For KB3926 C version

U7 *GMT_G910T21U

close conn

TOUCH PAD CONNECTOR

25 mils

CN9 TOUCH PAD CONN

PCB footprint BL121-12R-12P-L-QT6

CN10 *BL123-04R-TAND

TOUCH PAD L/R FOR 17" only

TOUCH PAD L/R FOR 16"

TOUCH PAD ON/OFF FOR 16"

TOUCH PAD ON/OFF FOR 17.3"

*TOUCH PAD EN SW

DB modified

Project Model	GPIO42
OPX 16"	Low
OPX 17.3"	High

GPIO42 control fan table

SB internal pull Hi 10k to 3v_s5

Change D12, D16 to RB500 for current loss

SB internal pull Hi 10k to 3v_s5

SST	AKE5GFK0Z09	1M byte SPI BIOS
WINBOND	AKE3GFP0N08	
PME	AKE3GZP0500	
EON	AKE3GZP0Q00	

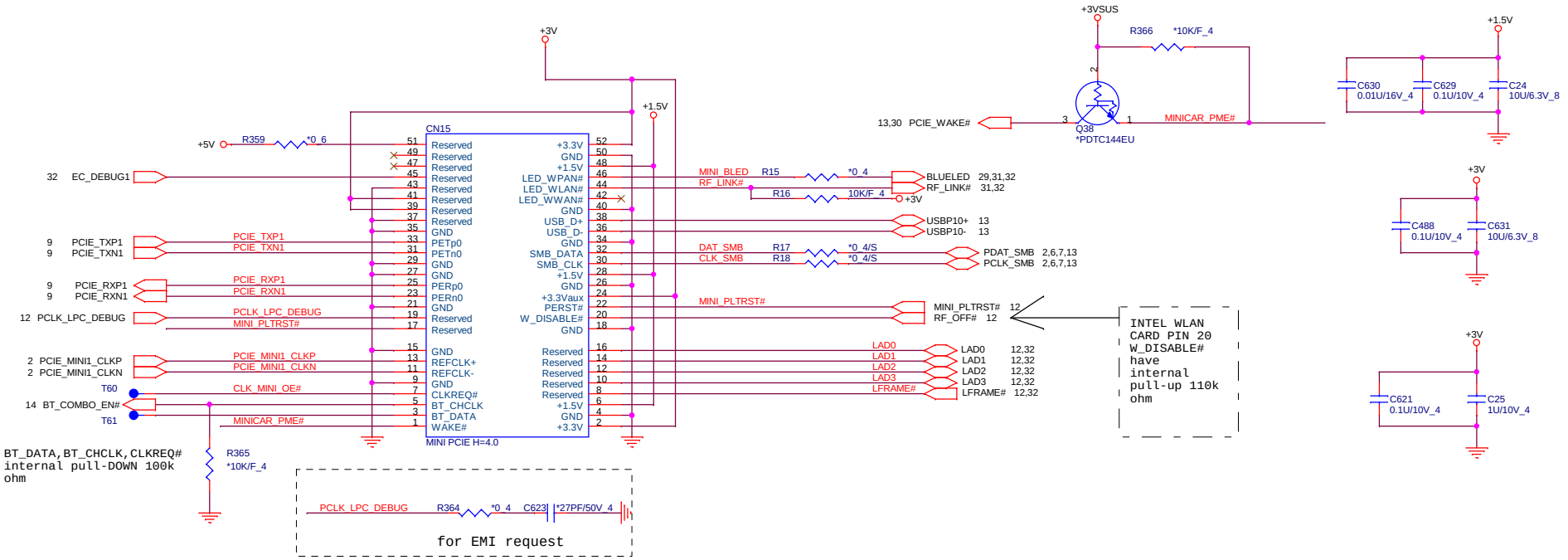
PROJECT : OP8
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Friday, March 20, 2009 Sheet 32 of 42

Mini PCI-E Card 1 WLAN



NB5/RD2	PROJECT : OP8 Quanta Computer Inc.	
	Size: Custom Document Number: Mini CARD	Rev: 1A
	Date: Friday, March 20, 2009	Sheet 33 of 42

DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,20,23,24,25,27,28,29,30,31,32,33,35,39

+5VPCU 27,31,32,35,36,37,38
+3VPCU 5,12,23,27,29,31,32,36,37,38,40
+3VSUS 13,26,29,33,35,37,39
+3VS5 5,7,12,13,14,15,16,39
+5VSUS 23,29,32,39
+5V 5,15,20,23,24,25,27,28,29,31,32,33,35,38,39
+3VLANVCC 30,39

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

DB modify

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Rds(on) 15m ohm

+12VALW is +15V power level
Please use +15VALW to prevent voltage rating issue

3.3 Volt +/- 5%
+3VPCU
C/C:8A
P/C:10A

+3V
6.76A
S0-S1

+3VS5
0.5A
S0-S5

+3VSUS
1.84A
S0-S3

+5V
4.31A
S0-S1

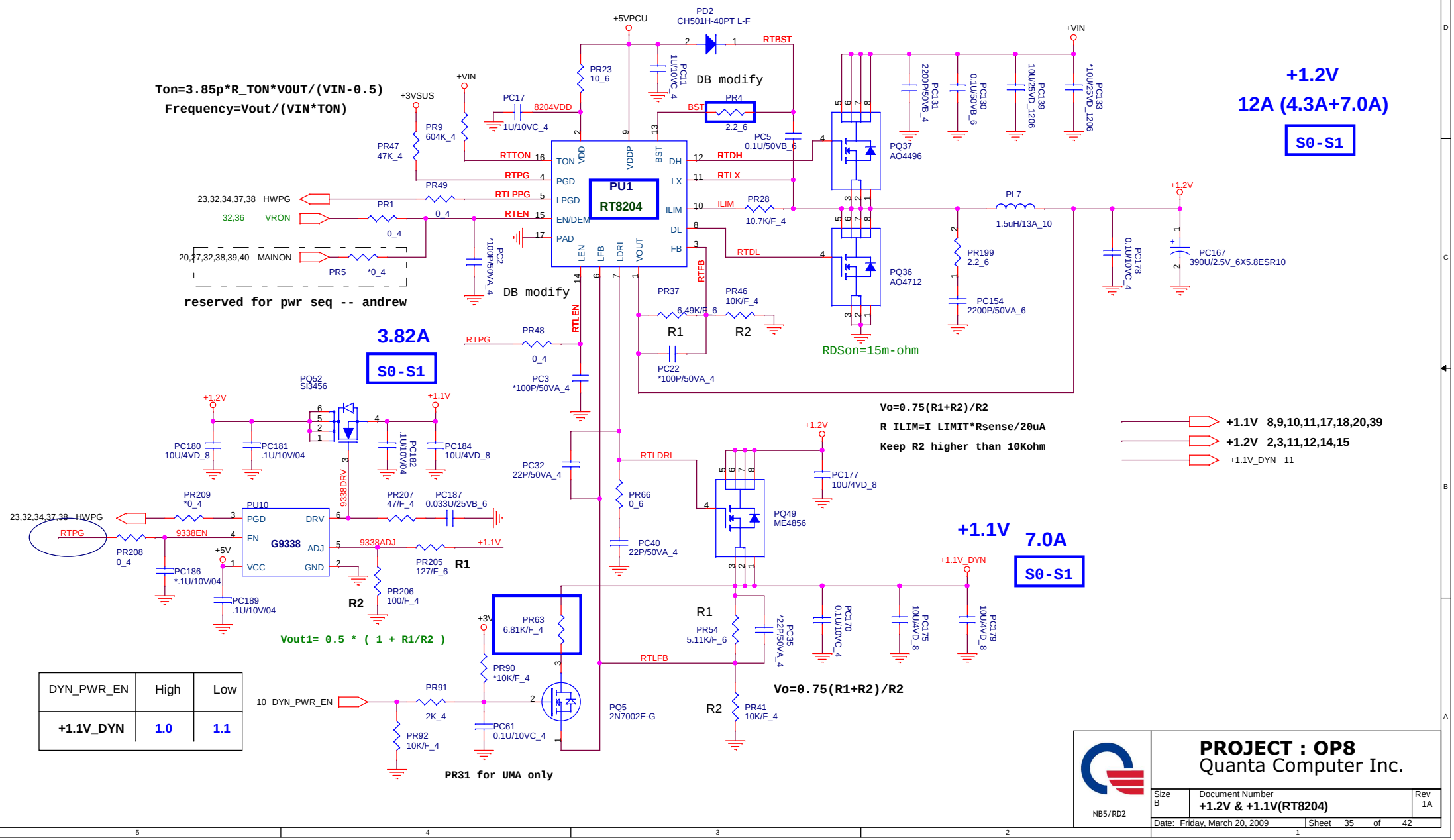
+5VSUS
4.5A
S0-S3

DB modify
+LANVCC
0.27A

For EMI-SI

PROJECT : OP8	
Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V(ISL6237)
Rev: 1A	
Date: Friday, March 20, 2009	Sheet 34 of 42
NB5/RD2	

+1.1V & +1.2V



DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.2V & +1.1V(RT8204)	1A

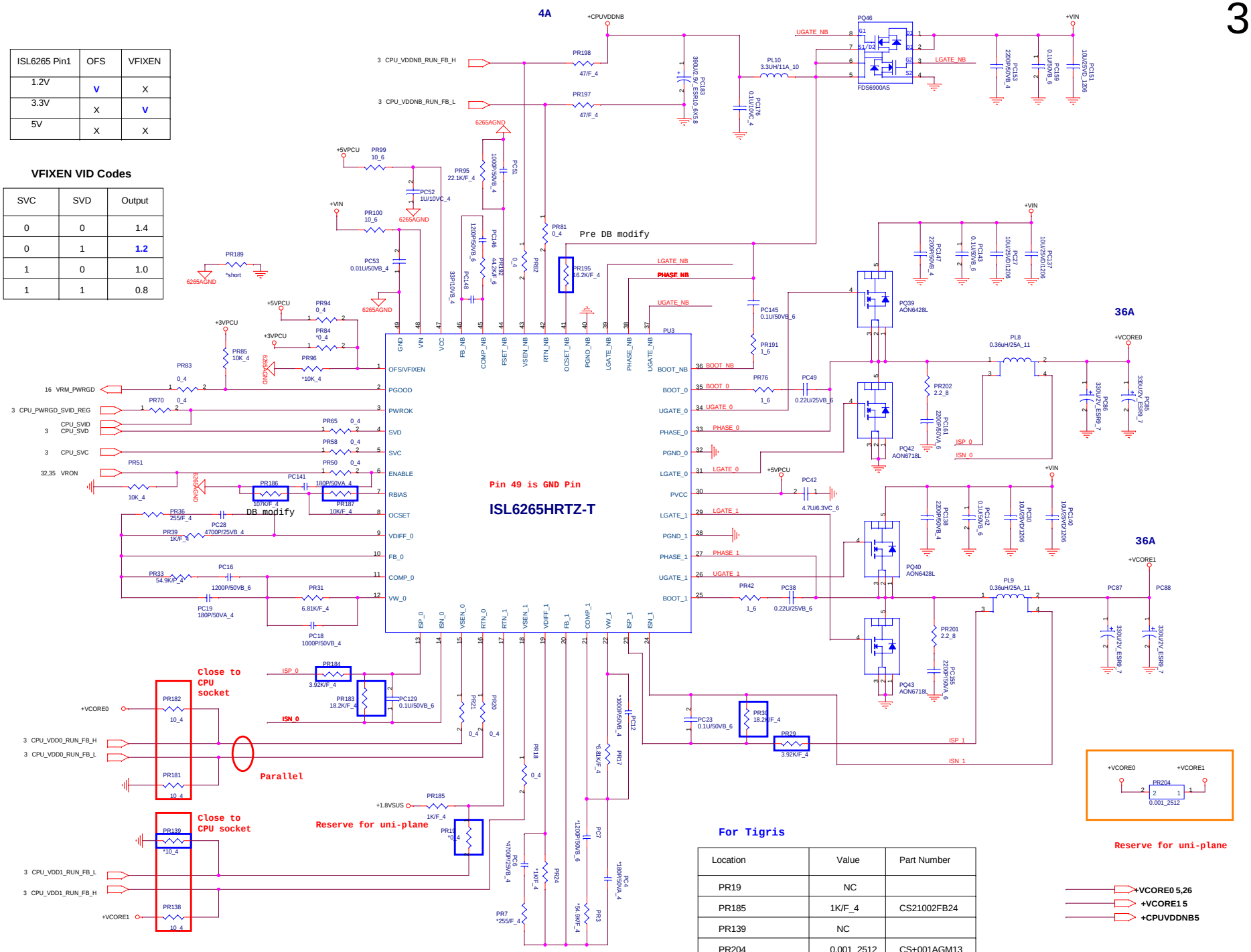
Date: Friday, March 20, 2009 Sheet 35 of 42

NB5/RD2

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



For Tigris

Location	Value	Part Number
PR19	NC	
PR185	1K/F_4	CS21002FB24
PR139	NC	
PR204	0.001_2512	CS+001AGM13
PC12,PR17,PC4,PC7, PR3,PR24,PC6,PR7	NC	

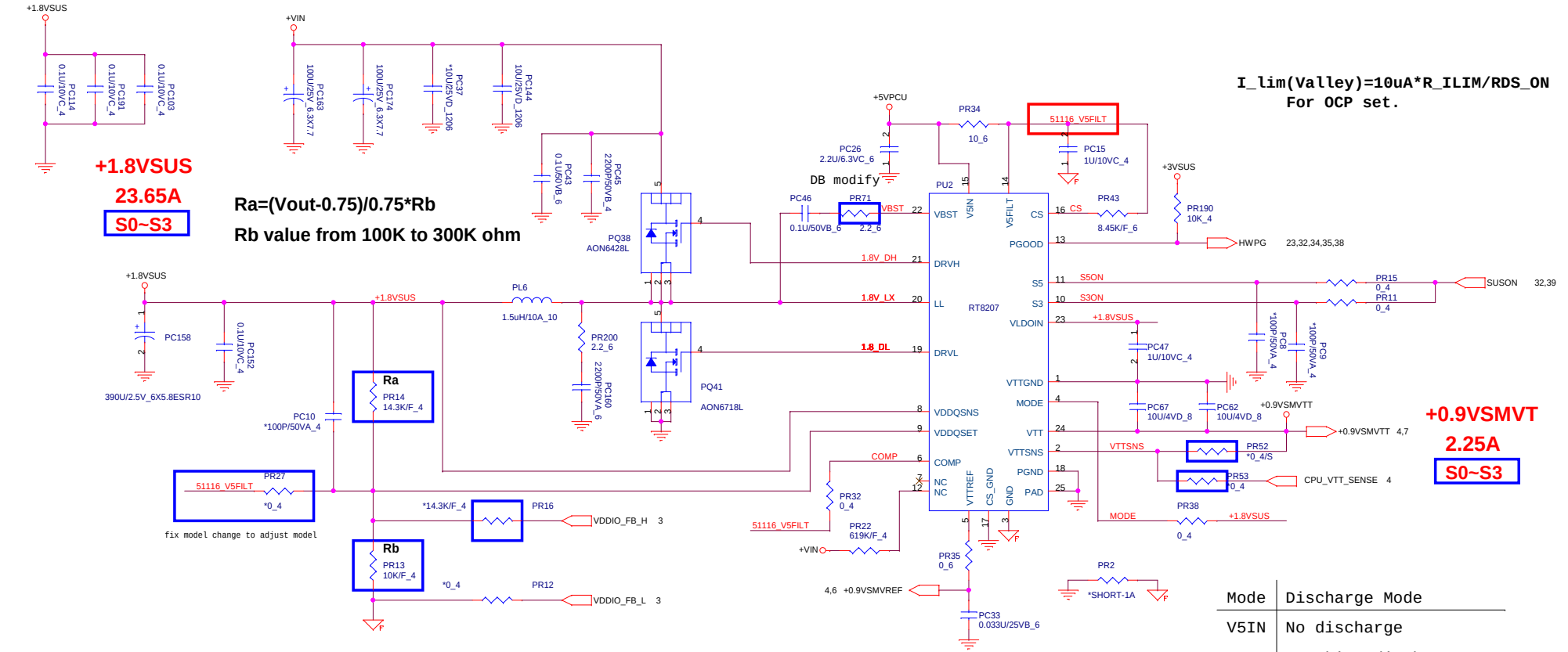
PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
C	CPU_CORE(ISL6265)	1A

NB5/RD2

Date: Friday, March 20, 2009 Sheet 36 of 43

+2.5V 3
+1.8VSUS 3,4,5,6,7,36,38



Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

PROJECT : OP8
Quanta Computer Inc.

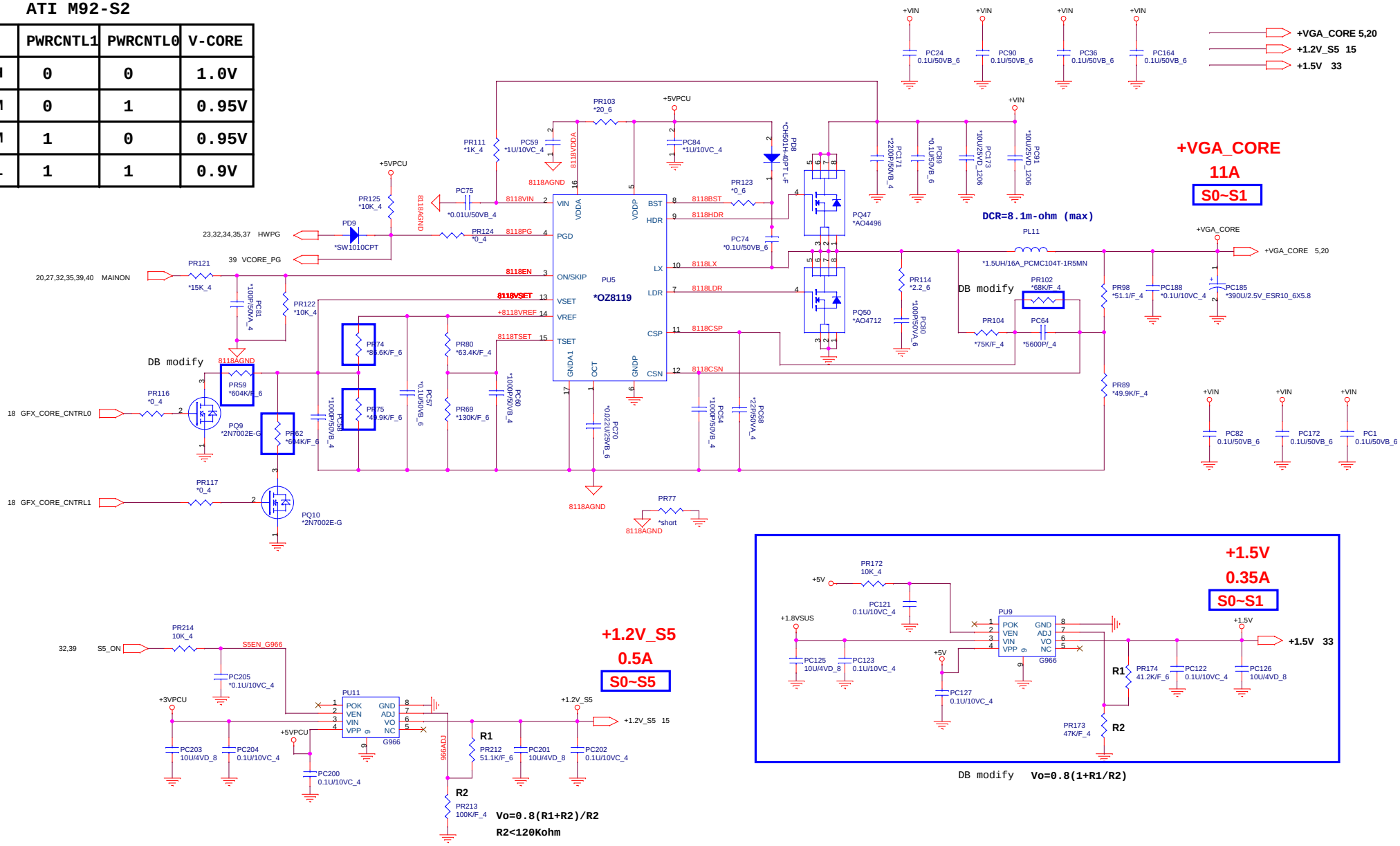
Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A

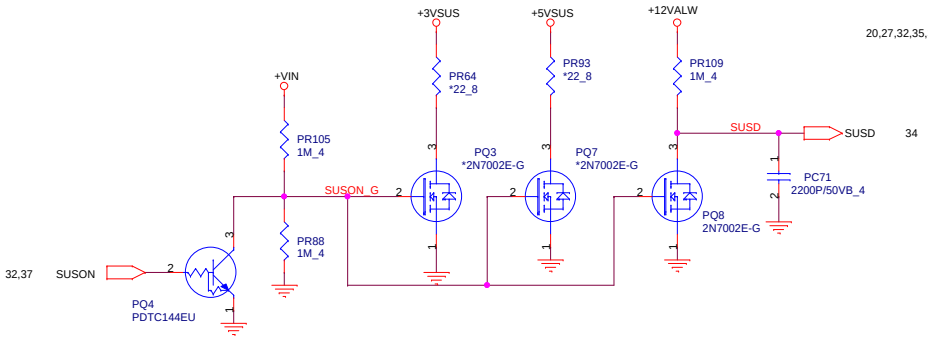
NB5/RD2

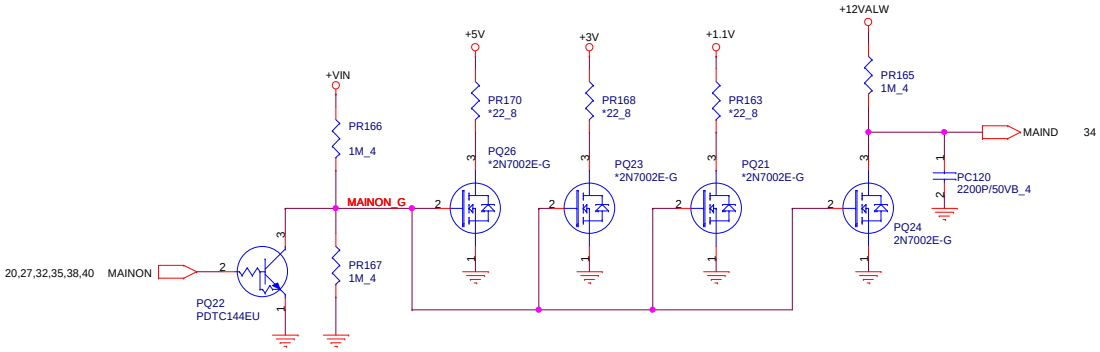
Date: Friday, March 20, 2009 Sheet 37 of 42

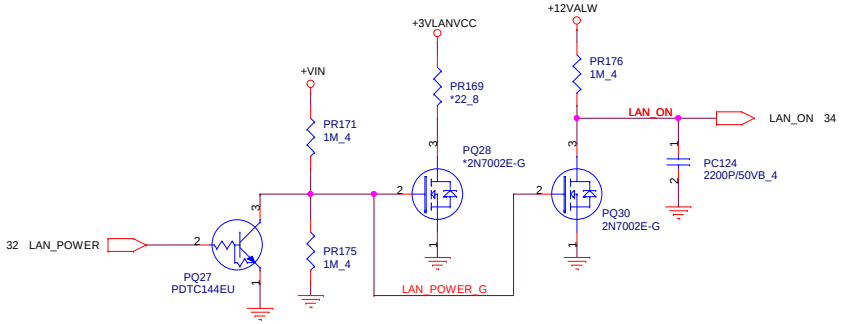
ATI M92-S2

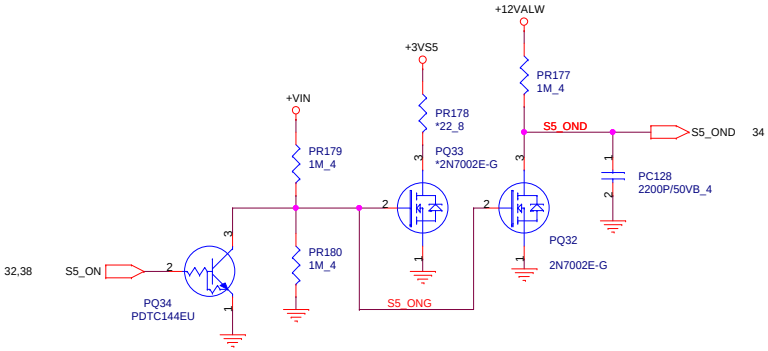
	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.0V
M	0	1	0.95V
M	1	0	0.95V
L	1	1	0.9V



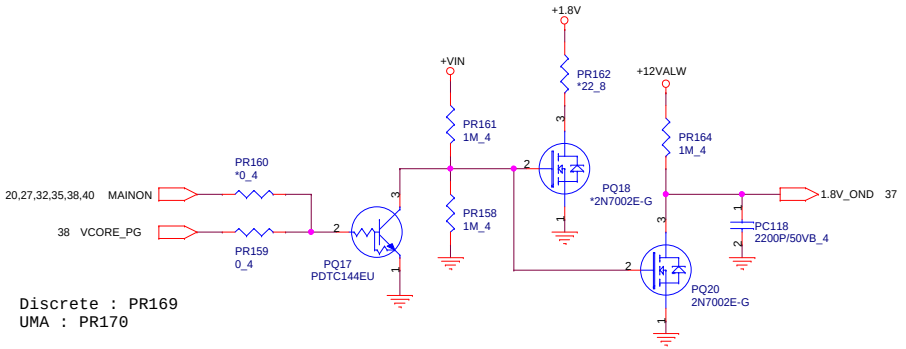








For Discrete Only

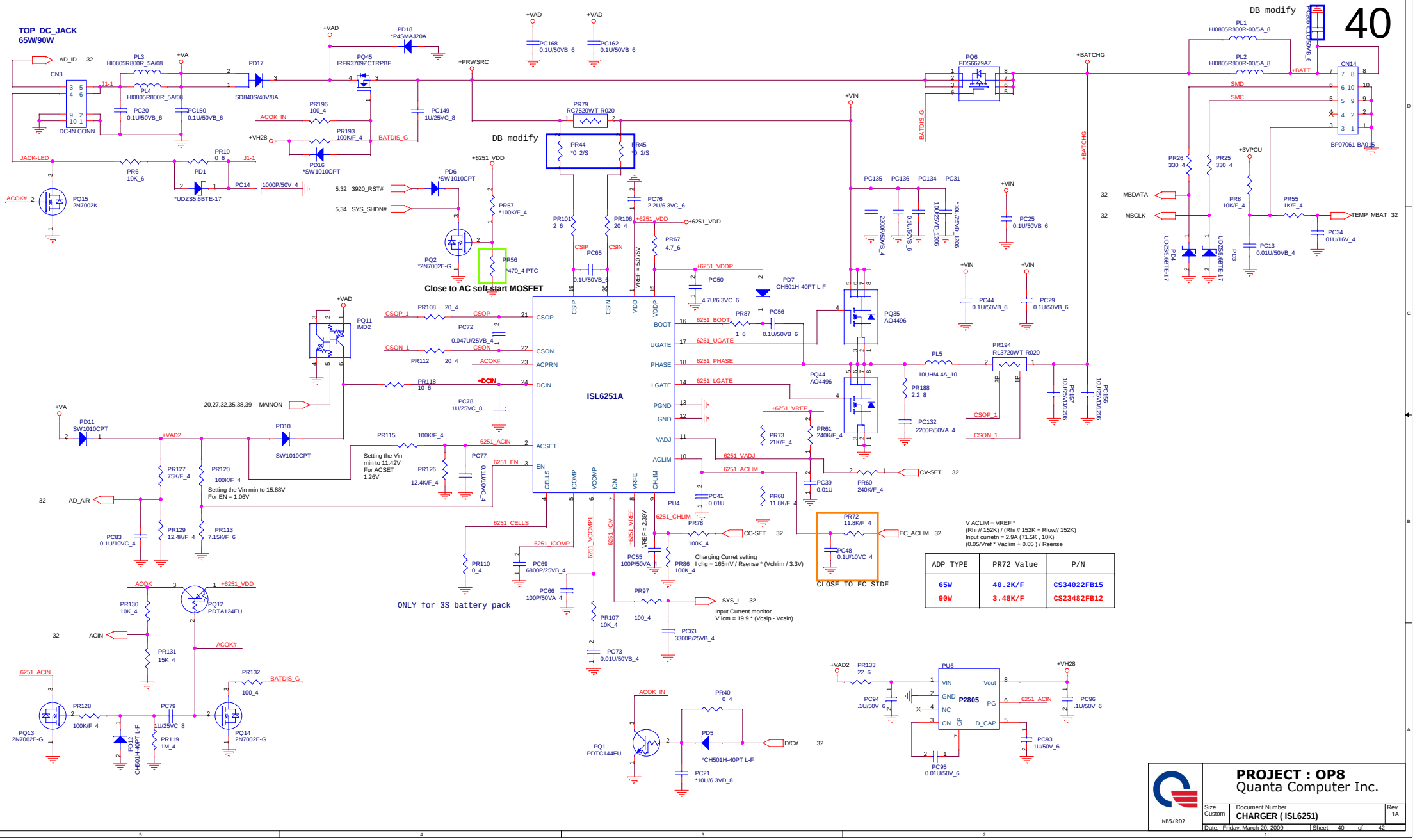


Discrete : PR169
UMA : PR170

PROJECT : OP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**DISCHARGE**	1A
Date: Friday, March 20, 2009	Sheet 39 of 42	

NB5/RD2


TOP DC_JACK
65W/90W
DB modify
40
ISL6251A
Close to AC soft start MOSFET
ONLY for 3S battery pack
CLOSE TO EC SIDE
Setting the Vin min to 11.42V For ACSET 1.26V
Setting the Vin min to 15.88V For EN = 1.06V
Charging Curret setting I chg = 165mV / Rsense * (Vchlim / 3.3V)
Input Current monitor V icm = 19.9 * (Vcsip - Vcsin)
V ACLIM = VREF * (Rhi // 152K) / (Rhi // 152K + Rlow// 152K)
Input currein = 2.9A (71.5K , 10K)
(0.05/Vref * Vaclim + 0.05) / Rsense
ADP TYPE | PR72 Value | P/N
65W | 40.2K/F | CS34022FB15
90W | 3.48K/F | CS23482FB12
PROJECT : OP8
Quanta Computer Inc.
CHARGER (ISL6251)
Document Number
Size Custom
Rev 1A
Date: Friday, March 20, 2009
Sheet 40 of 42
NB5/RD2