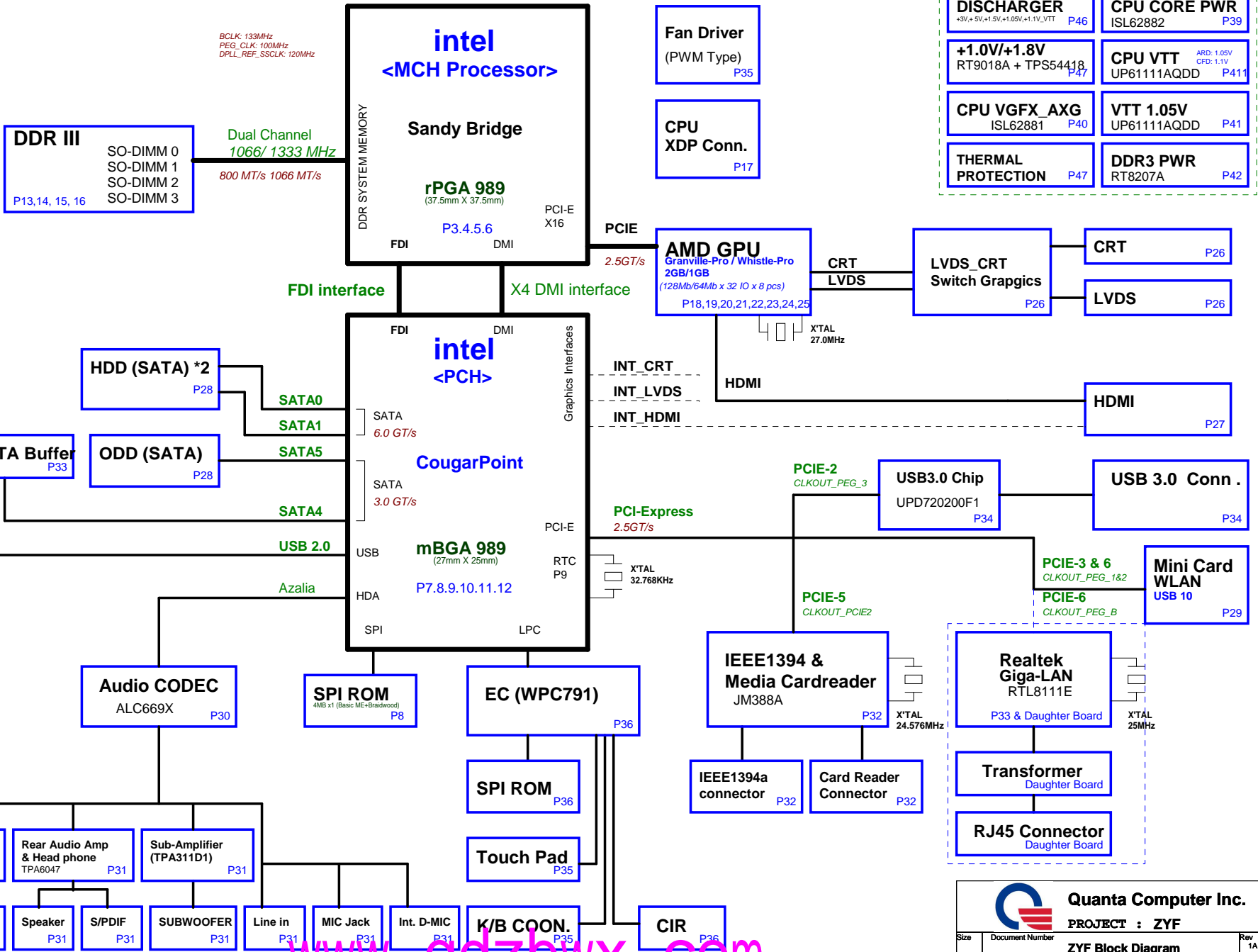


ZYF SYSTEM BLOCK DIAGRAM

EV@ --- GPU only
 MS@ --- iGPU & GPU Muxless
 W@ --- Whistler GPU
 G@ --- Granville GPU
 DO@ --- 4 DIMM
 SP@ --- Operation P/N

BCLK: 133MHz
 PEG_CLK: 100MHz
 DPLL_REF_SSCLK: 120MHz

GPU CORE PWR ISL6264 P44	CHARGER ISL8731 P37
GPU IO PWR ISL62827 P45	3/5V SYS PWR RT8206 P38
DISCHARGER +3V,+5V,+1.5V,+1.05V,+1.1V_VTT P46	CPU CORE PWR ISL62882 P39
+1.0V/+1.8V RT9018A + TPS54418 P47	CPU VTT UP61111AQDD P41
CPU VGFX_AXG ISL62881 P40	VTT 1.05V UP61111AQDD P41
THERMAL PROTECTION P47	DDR3 PWR RT8207A P42

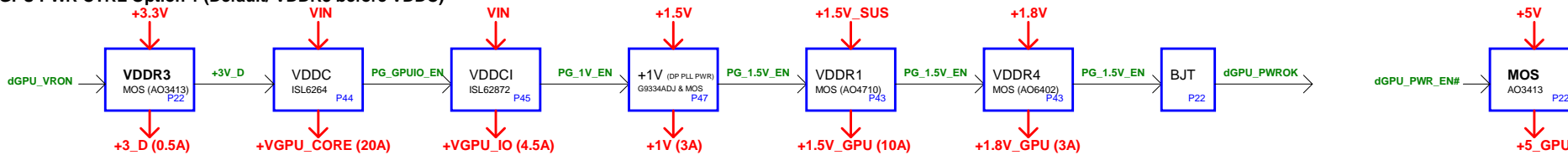


Note:
 HM65 does not support USB 6 & 7
 HM65 does not support SATA 2 & 3

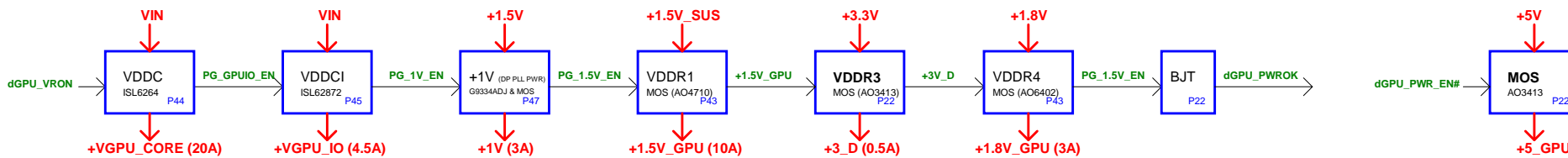
Front Stereo Amp (G1453L/ 2W+2W) P31	Center Mono Amp (G1442/ 2W) P30	Rear Audio Amp & Head phone TPA6047 P31	Sub-Amplifier (TPA311D1) P31
Front Speaker P31	Center Speaker P31	Speaker P31	S/PDIF P31
SUBWOOFER P31	Line in P31	MIC Jack P31	Int. D-MIC P31
K/B COON. P35	CIR P36		

www.qdzbwx.com

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



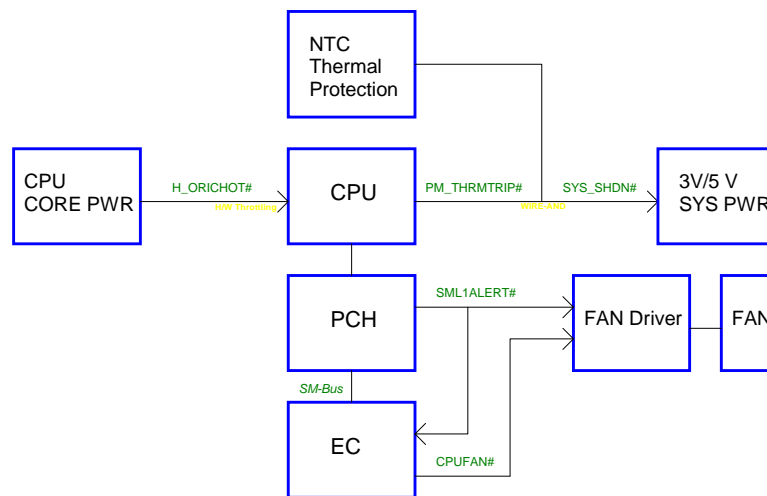
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



Sandy Bridge Processor (POWER)

CPU VTT
SNB 45W:8.5A

Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

Real
330uF/10mohm x 1
22uF x 10
10uF x 2

CPU VGT
SNB 45W:21.5A

Spec
470uF/4mohm x 2
22uF x 12

Real
330uF/10mohm x 2
22uF x 8
10uF x 6

Sandy Bridge Processor (GRAPHIC POWER)

POWER

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

DDR3 - 1.5V RAILS

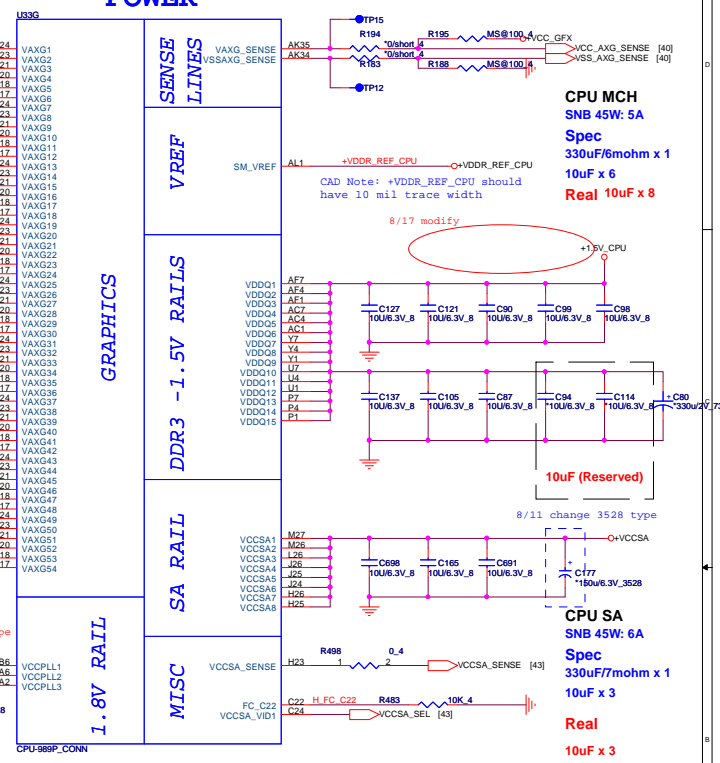
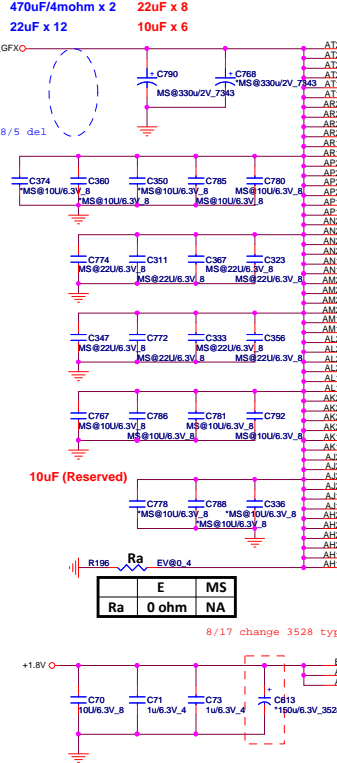
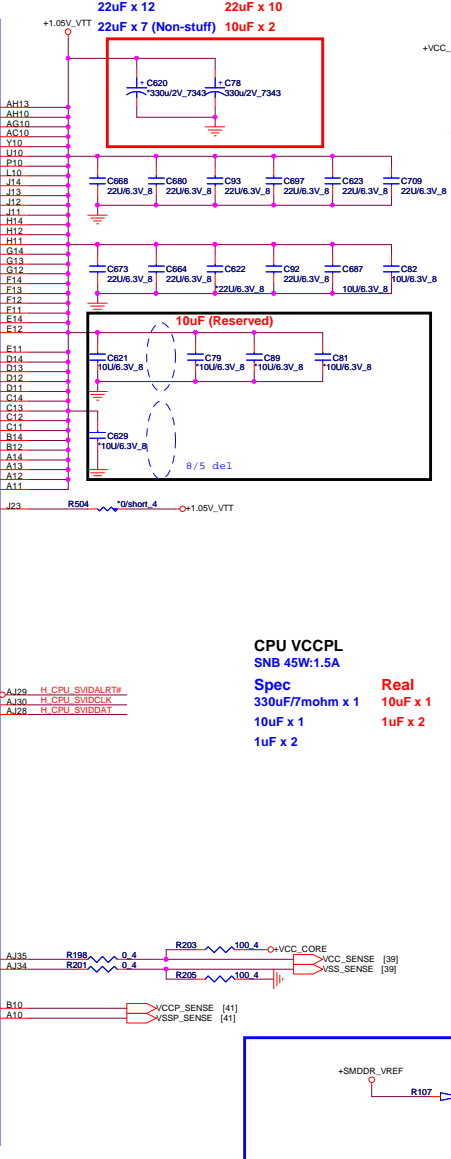
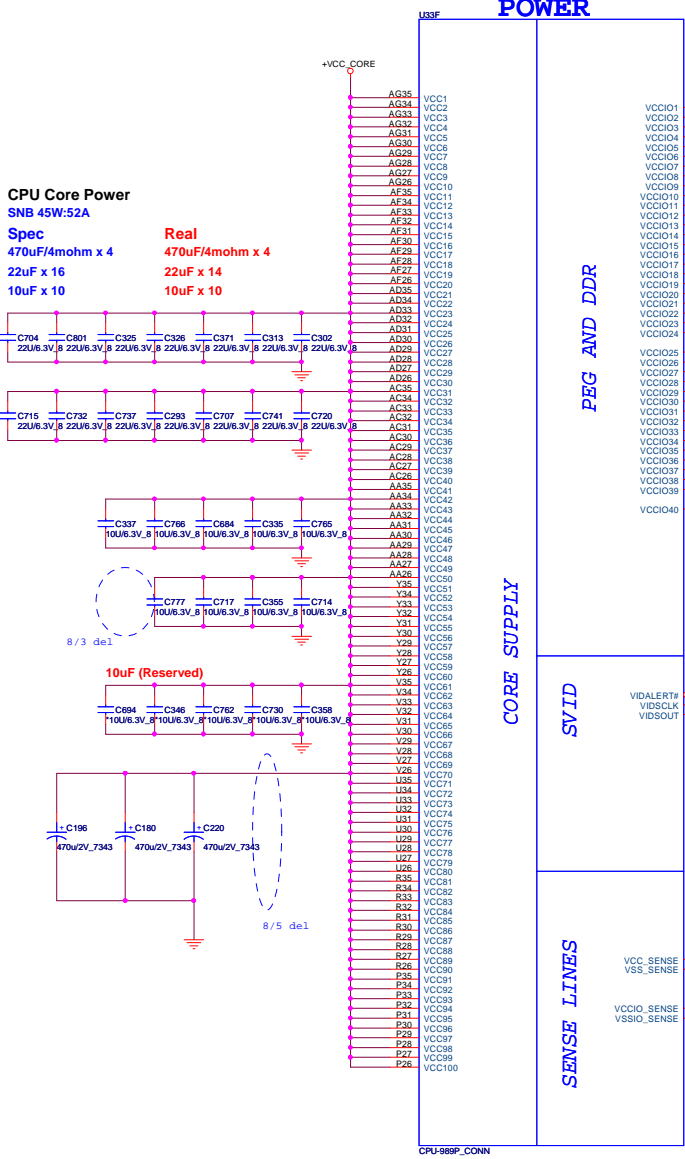
SA RAIL

MISC

CPU SA

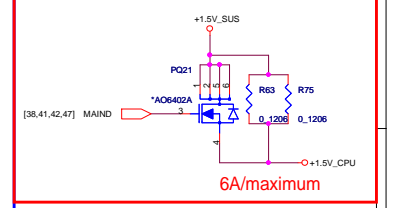
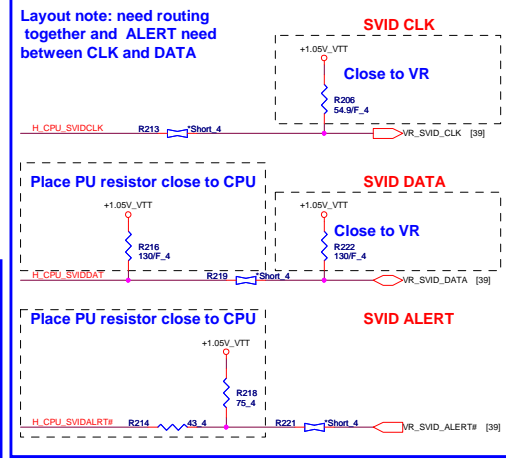
CPU Core Power
SNB 45W:52A
Spec
470uF/4mohm x 4
22uF x 16
10uF x 10

Real
470uF/4mohm x 4
22uF x 14
10uF x 10



CPU VCCPL
SNB 45W:1.5A
Spec
330uF/7mohm x 1
10uF x 1
1uF x 2

Real
10uF x 1
1uF x 2



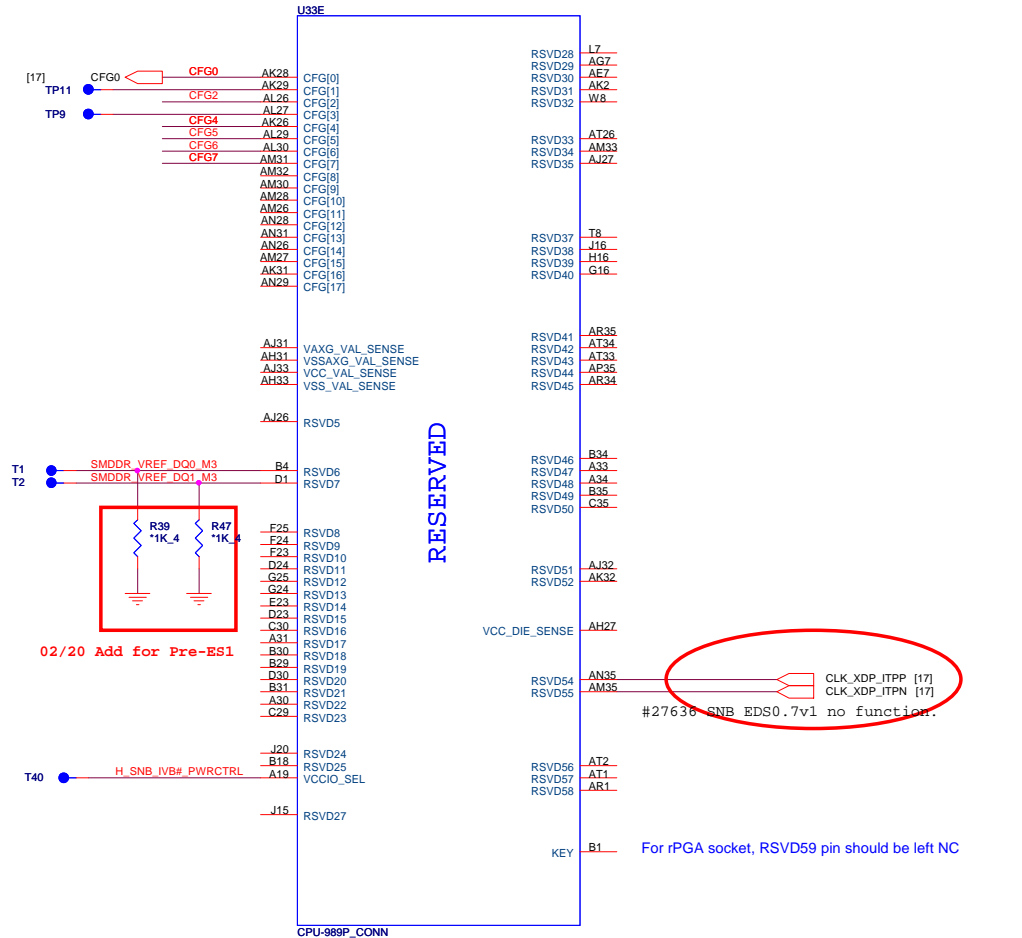
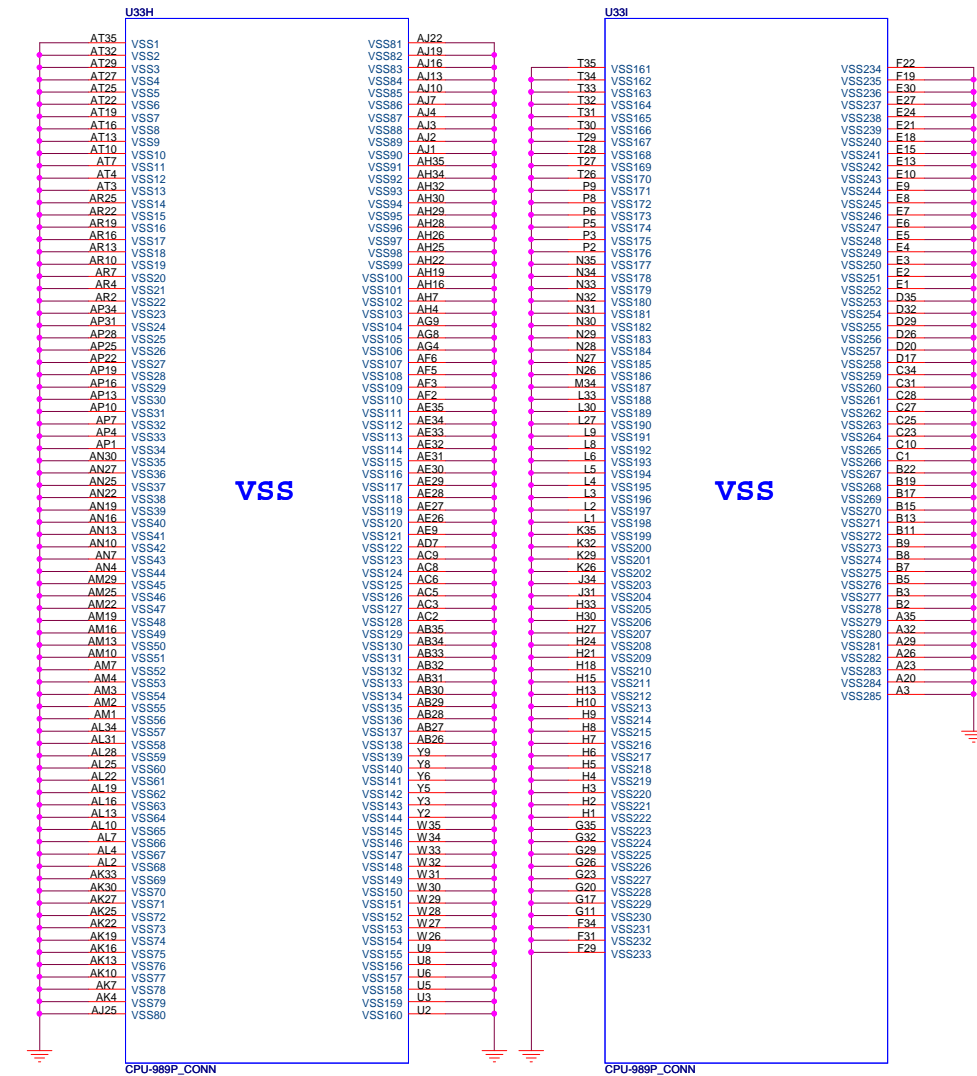
Quanta Computer Inc.
PROJECT : ZFY
Sandy Bridge 3/4

Size	Document Number	Rev
		1A

Date: Monday, November 08, 2010 Sheet 5 of 50

Sandy Bridge Processor (GND)

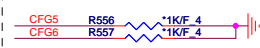
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

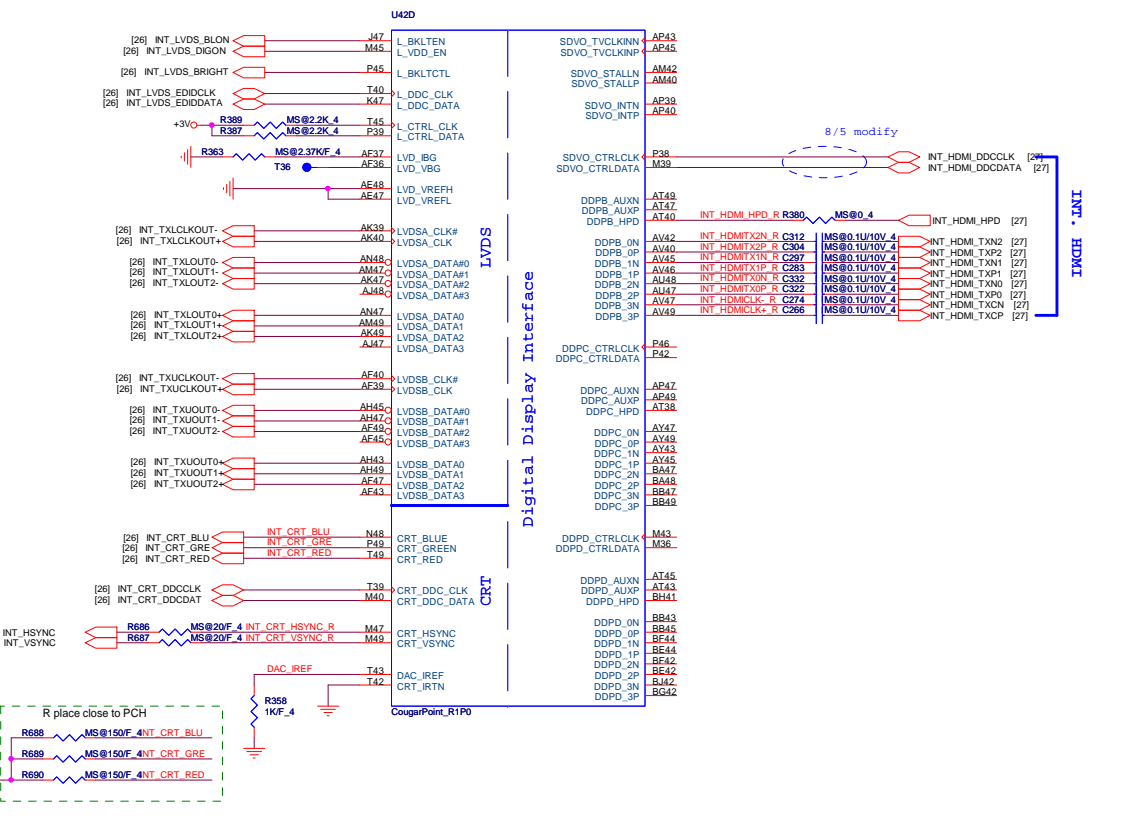
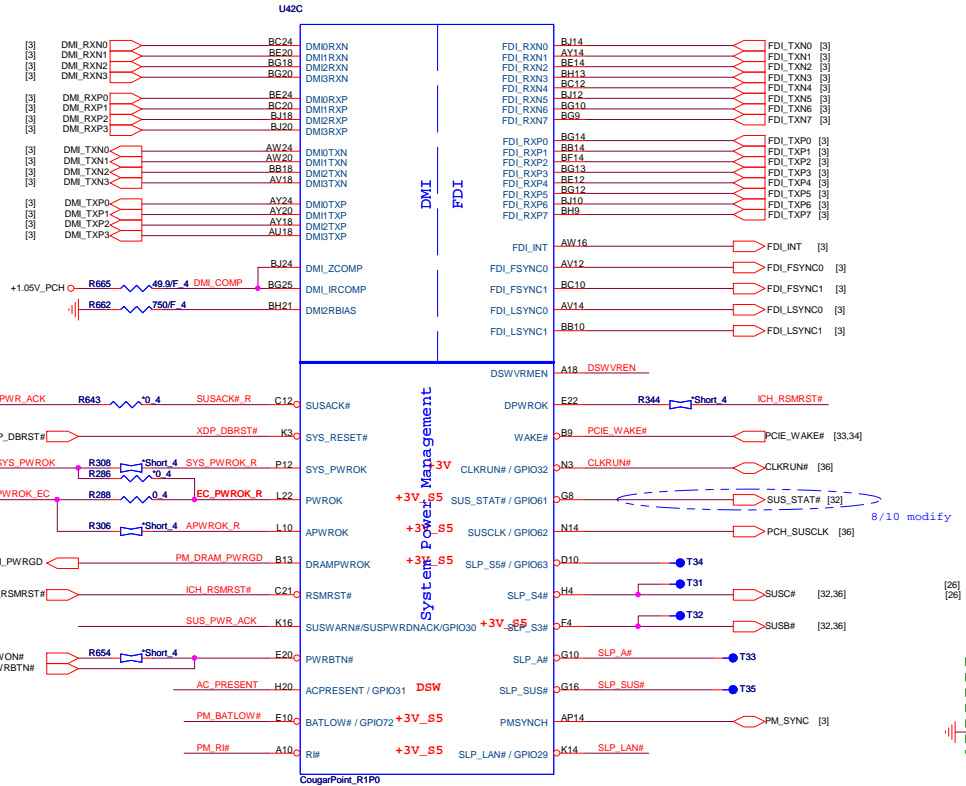
- 11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
- 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date:	Monday, November 08, 2010	Sheet 6 of 50

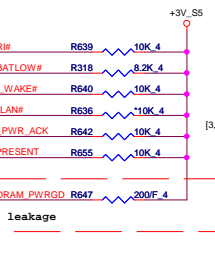
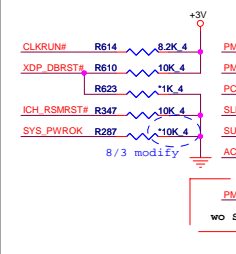
Cougar Point (LVDS, DDI)

Cougar Point (DMI, FDI, PM)

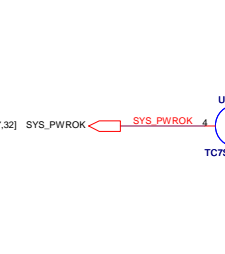


PCH Pull-high/low(CLG)

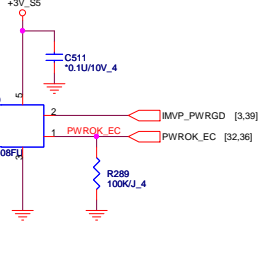
System PWR_OK(CLG)



SMBus(CLK)



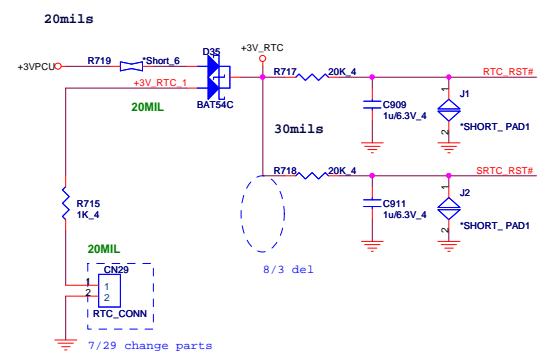
On Die DSW VR Enable



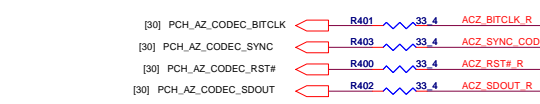
On Die DSW VR Enable
 High = Enable (Default)
 Low = Disable

PROJECT : ZYP		
Size	Document Number	Rev
	Cougar Point 1/6	1A
Date:	Monday, November 08, 2010	Sheet 7 of 50

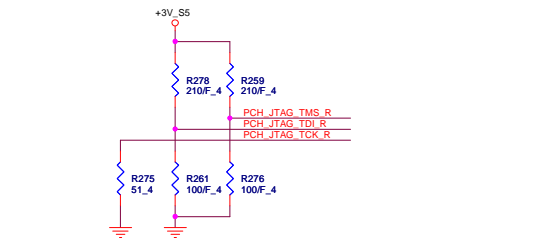
RTC Circuitry(RTC)



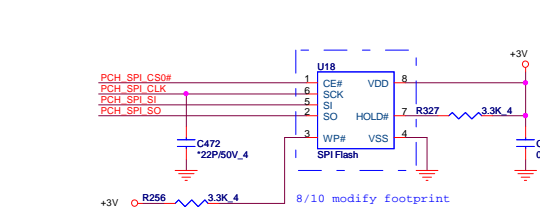
HDA Bus(CLG)



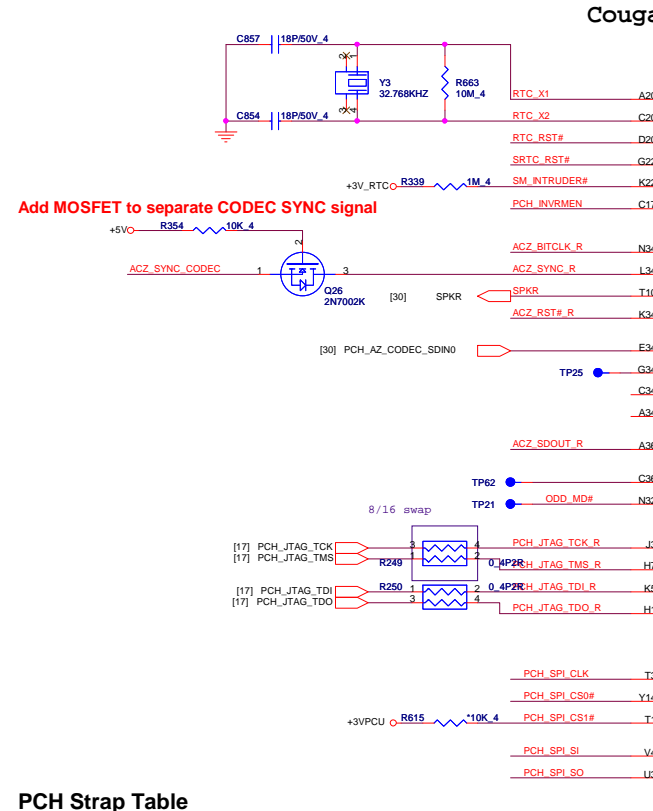
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)



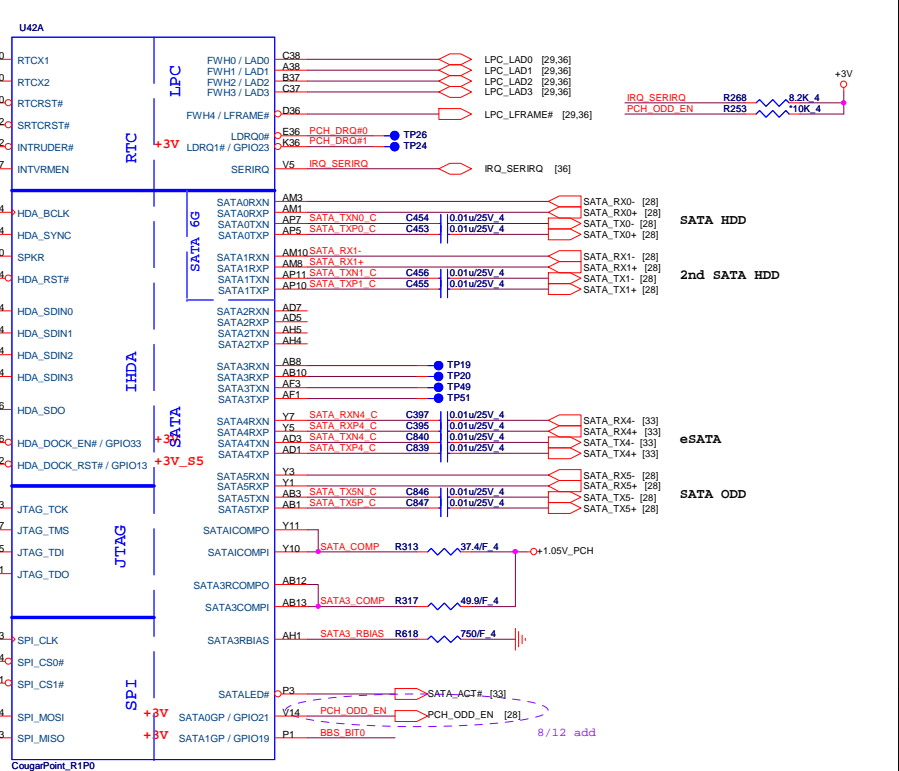
PCH2 (CLG)



PCH Strap Table

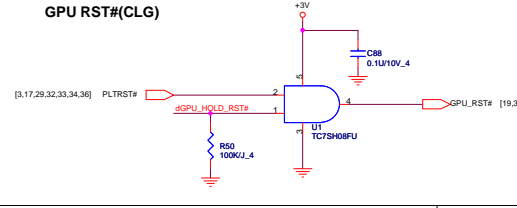
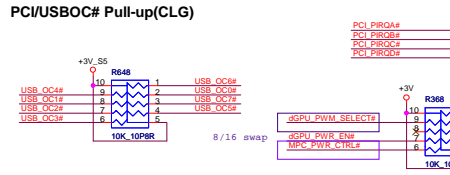
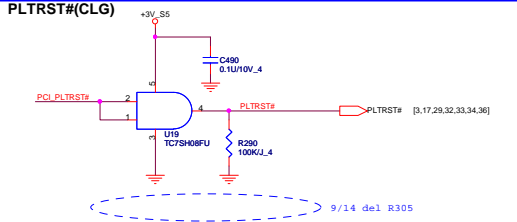
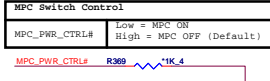
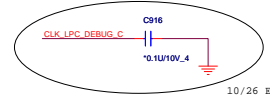
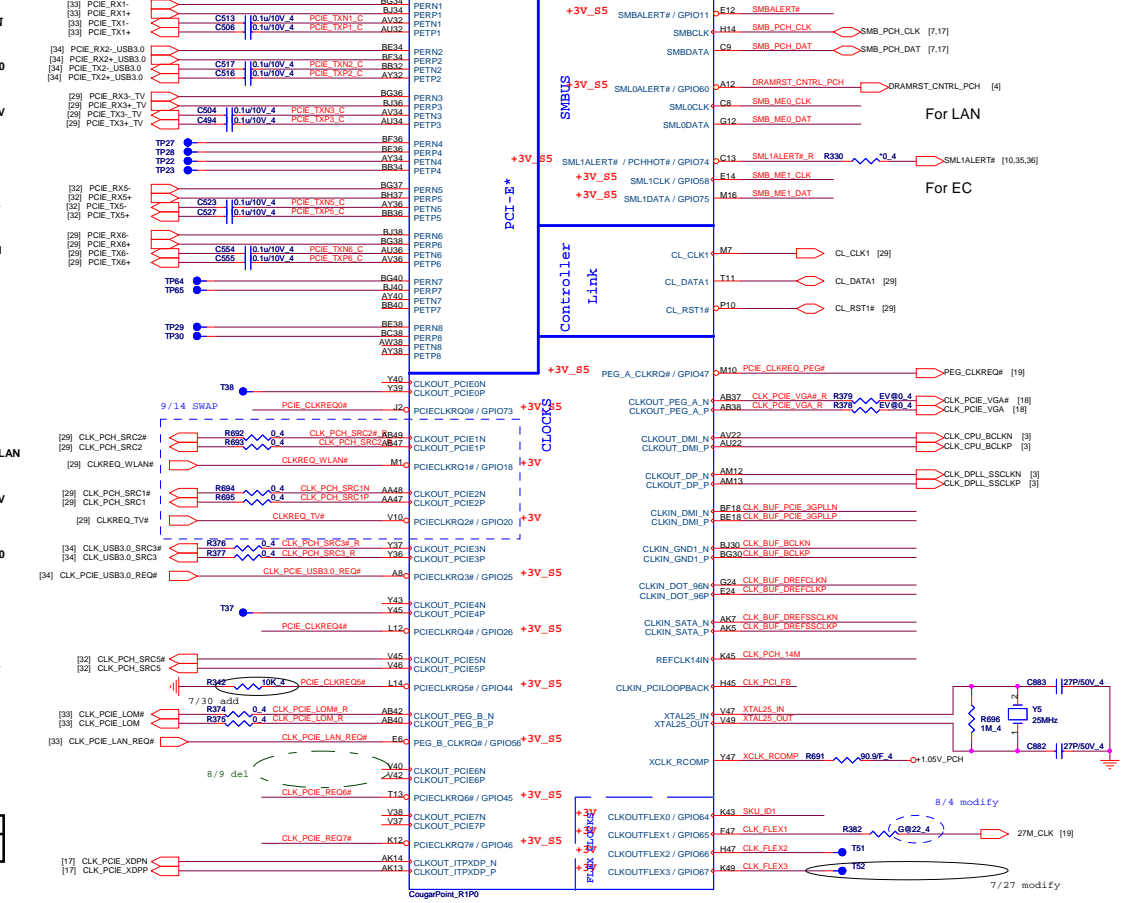
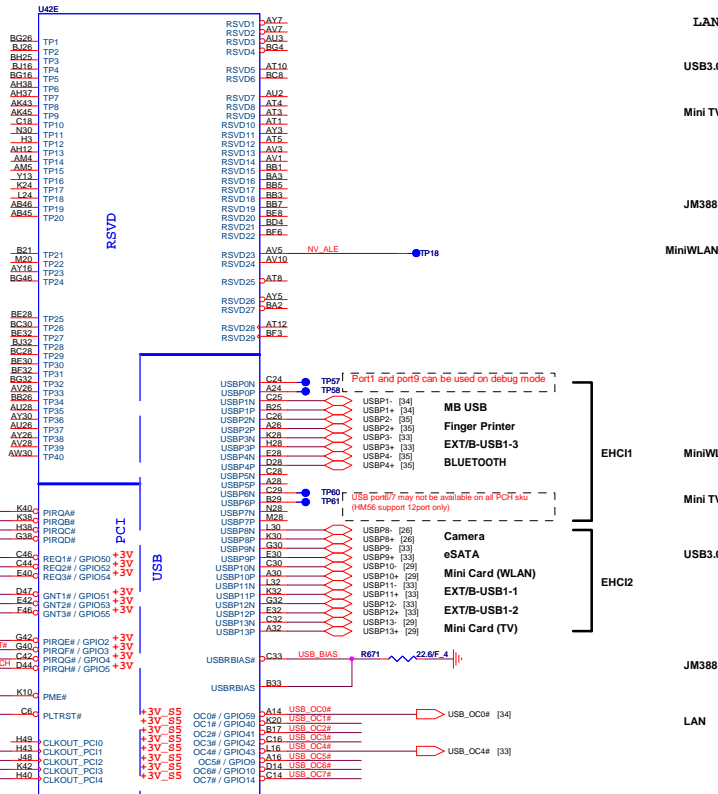
Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V - R660 1K_4 - SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R684 1K_4 - PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC - R656 330K_4 - PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]	R702 1K_4 - BBS_BIT1 [9] R262 1K_4 - BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	[36] ME_WR# - ACZ_SDO_TEST R356 0_4 - ACZ_SDOUT_R
DF_TV5	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R630 2.2K_4 - +1.8V R629 1K_4 - DF_TV5 [10] H_SNB_IVB# [10]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R263 1K_4 - PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 - R355 1K_4 - ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	Need check schematic
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

Cougar Point (HDA, JTAG, SATA)



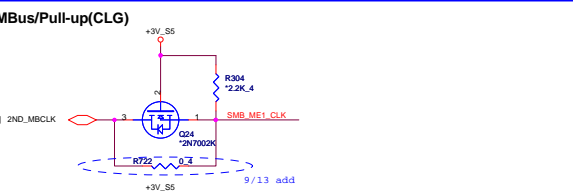
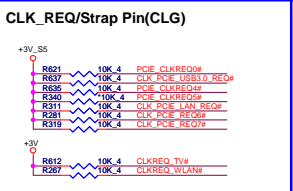
Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

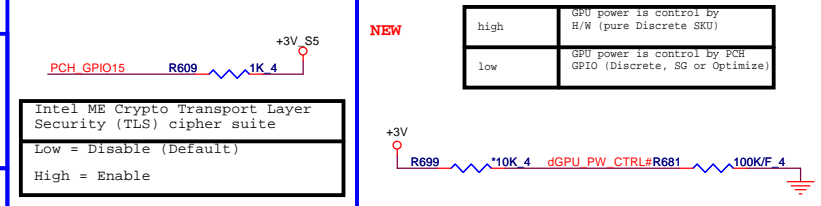
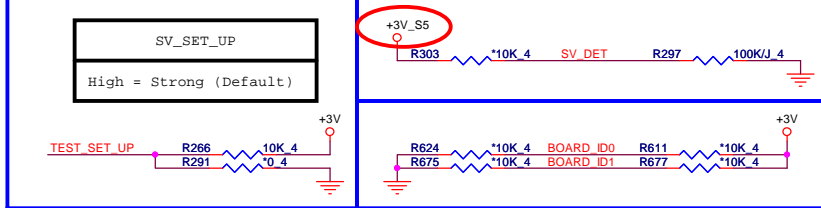
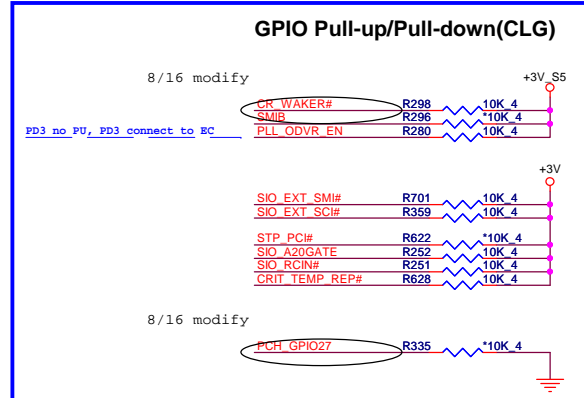
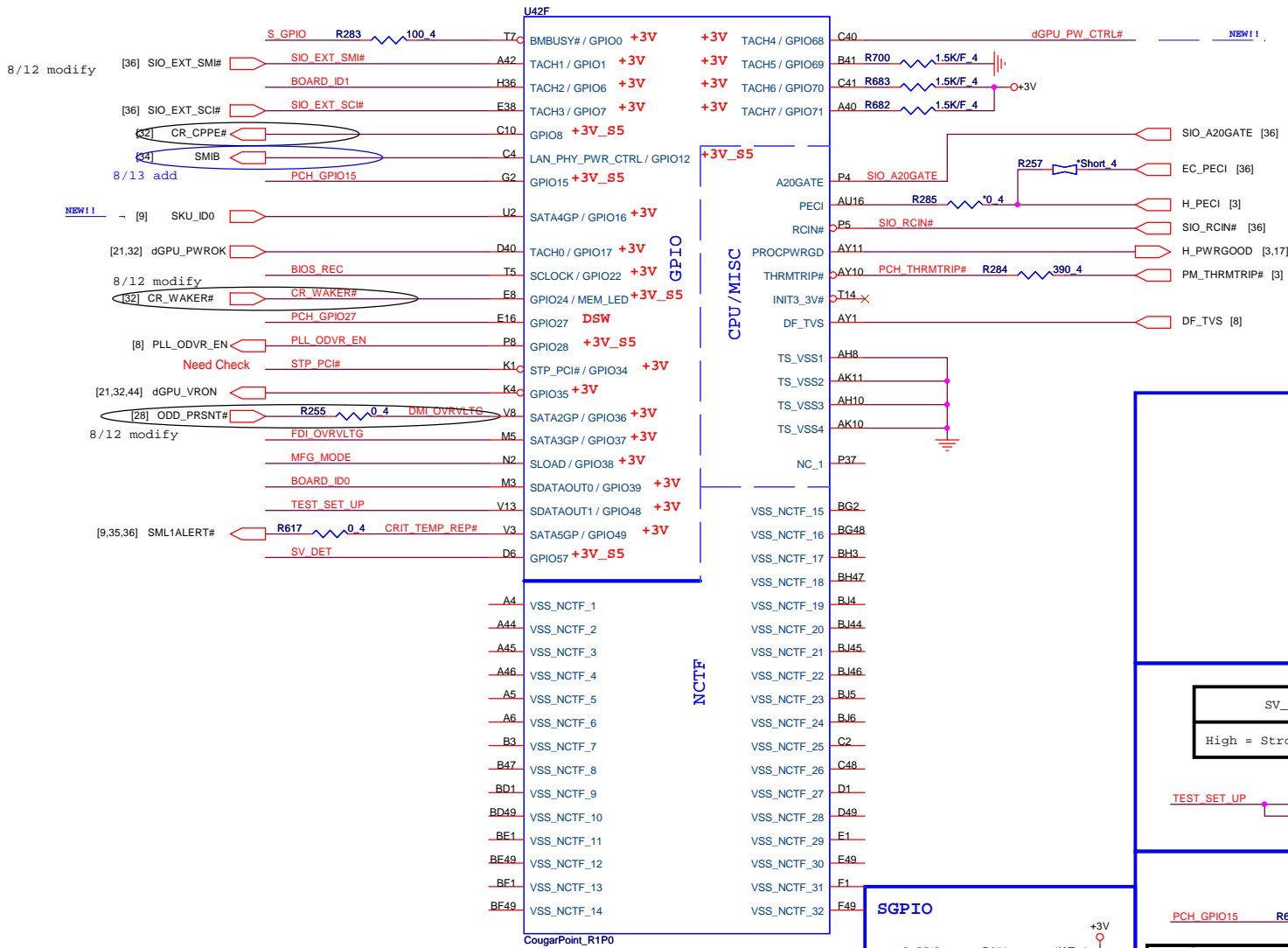


	GPU_PWR_CTRL# (GPIO6)	GPU_HOLD_RST# (GPIO5)	GPU_HOLD_RST# (GPIO5)	GPU_HOLD_RST# (GPIO5)	Setup Name	Setup
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0	0	1	GPU	Hidden	GPU boot
Switchable	0	1	1	UMA/GPU	Discrete/SW	UMA boot
Optimise (Muxless)	0	1	1	UMA	UMA/SW	UMA boot

0 = GPU power is control by PCI GPIO (Discrete, SW or Optimise)
1 = GPU power is control by N/W (pure Discrete SWU)

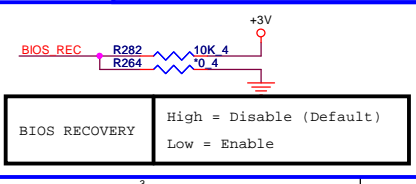
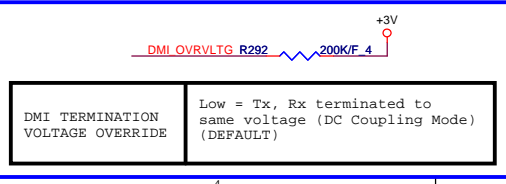
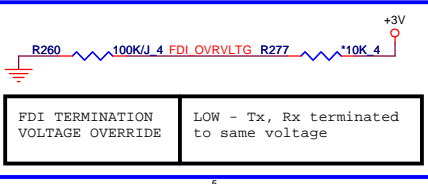


Cougar Point (GPIO,VSS_NCTF,RSVD)



NEW

high	GPU power is control by H/W (pure Discrete SKU)
low	GPU power is control by PCB GPIO (Discrete, SG or Optimize)



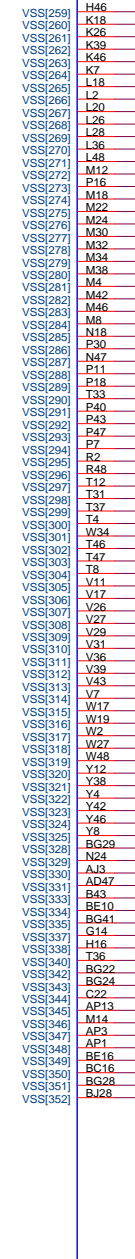
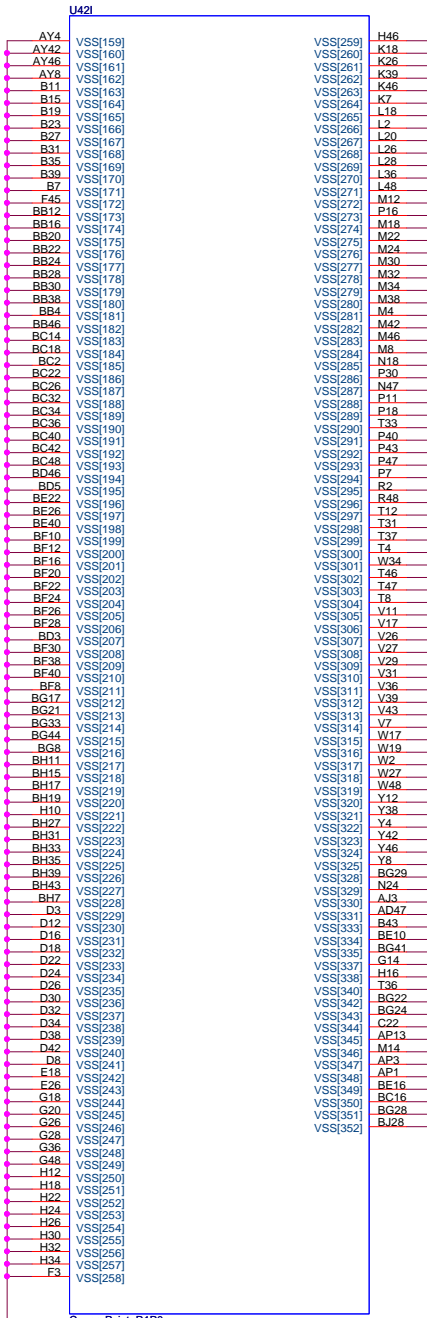
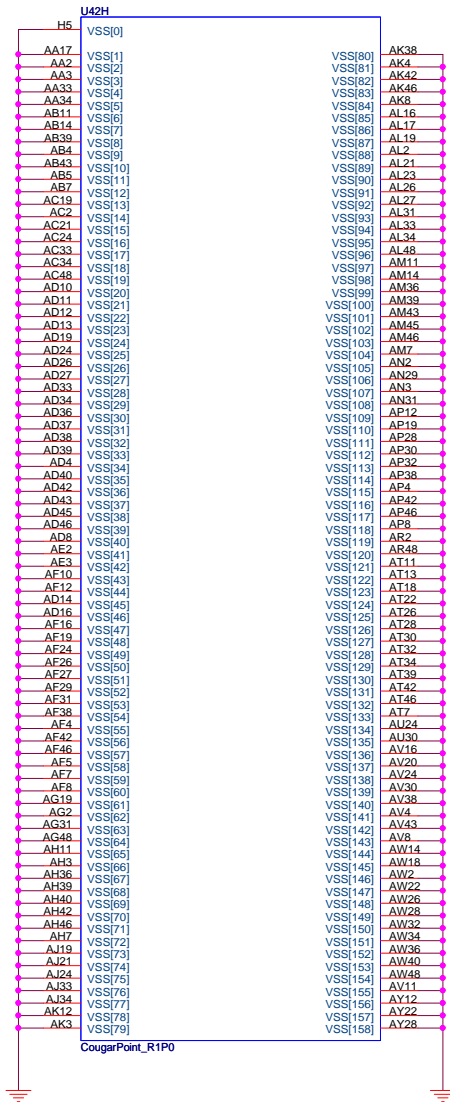
Quanta Computer Inc.
PROJECT : ZYF


Size Document Number Rev 1A

Cougar Point 4/6

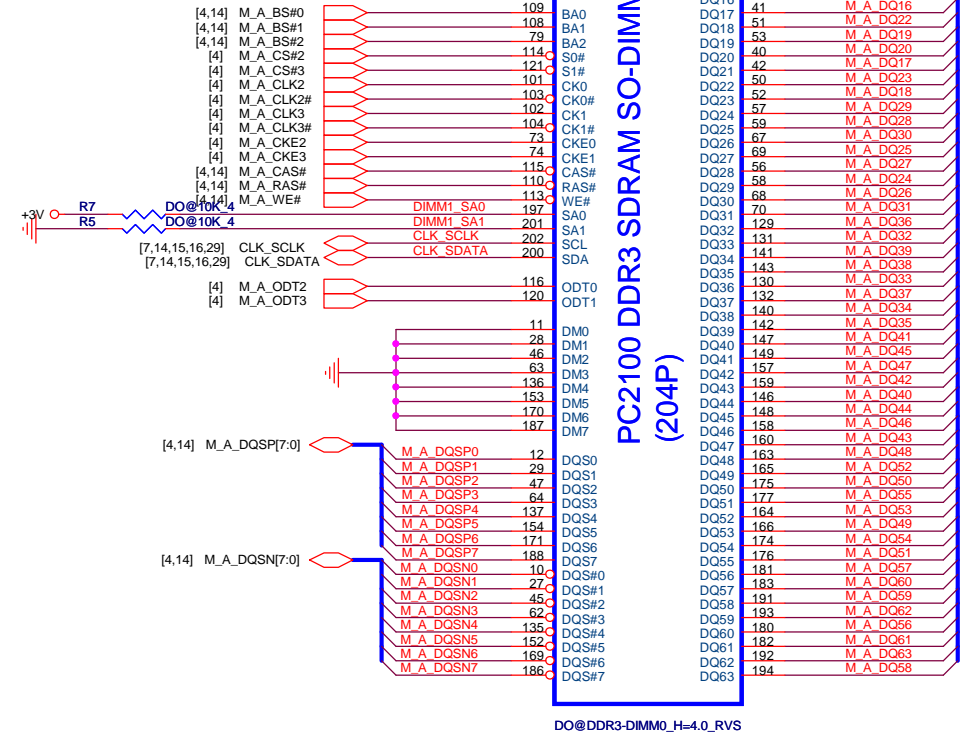
Date: Monday, November 08, 2010 Sheet 10 of 50

IBEX PEAK-M (GND)




Quanta Computer Inc.
 PROJECT : ZYF
 Document Number
Cougar Point 6/6
 Rev 1A
 Monday, November 08, 2010 12 of 50

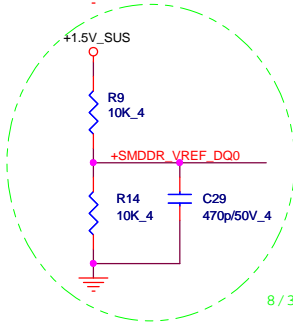
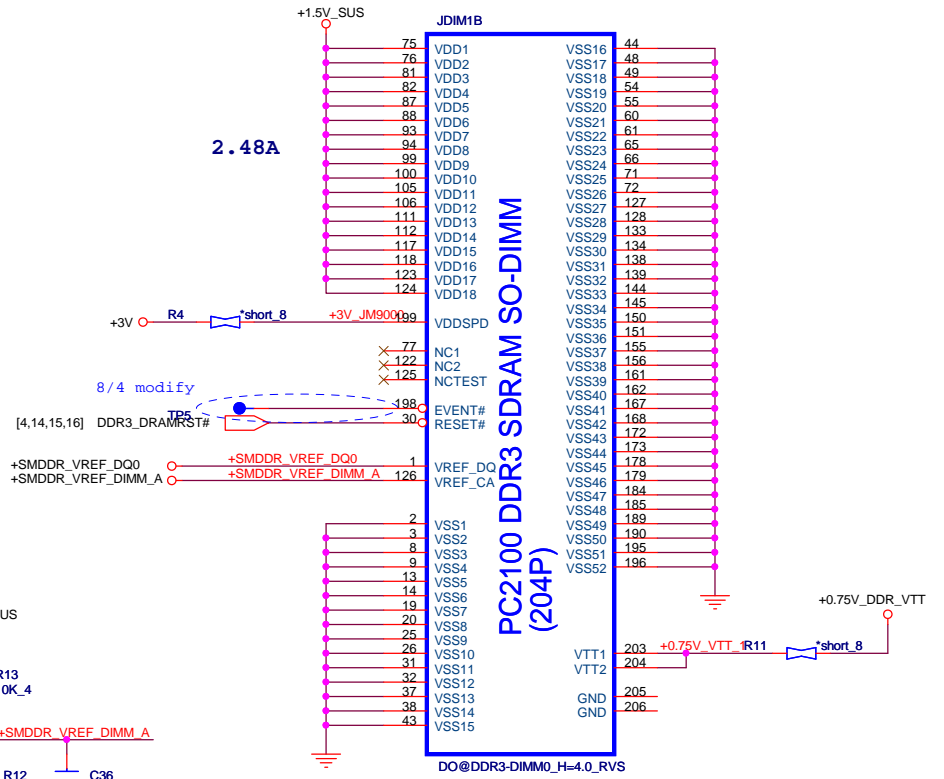
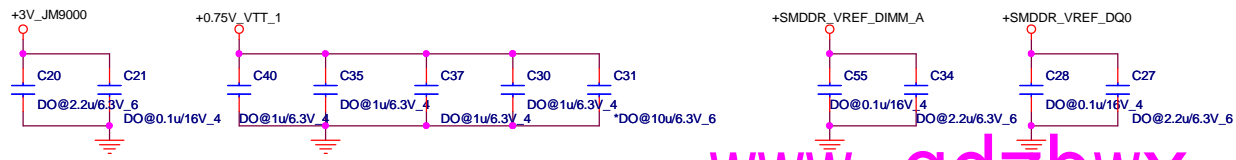
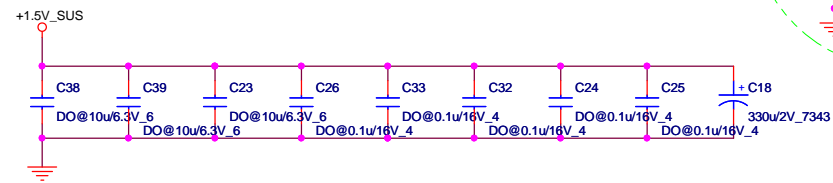
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

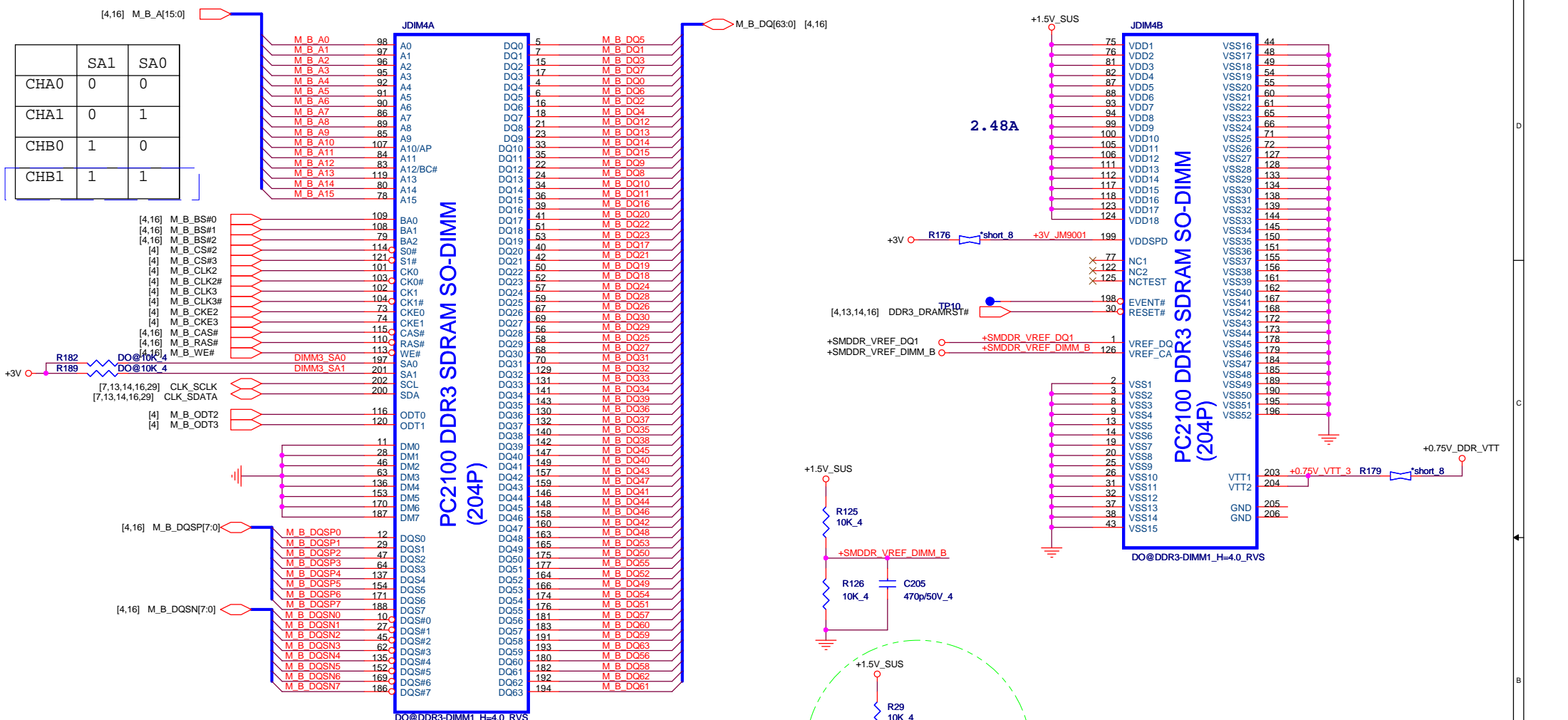


PC2100 DDR3 SDRAM SO-DIMM (204P)

DO@DDR3-DIMM0_H=4.0_RVS

Place these Caps near So-Dimm0.



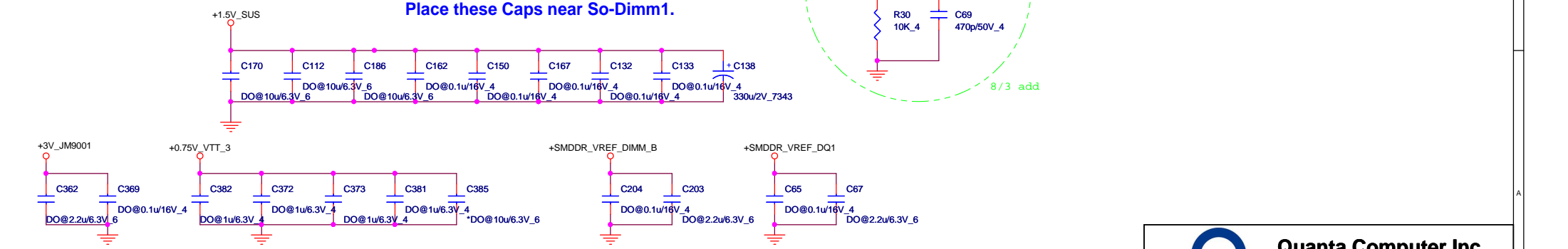


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

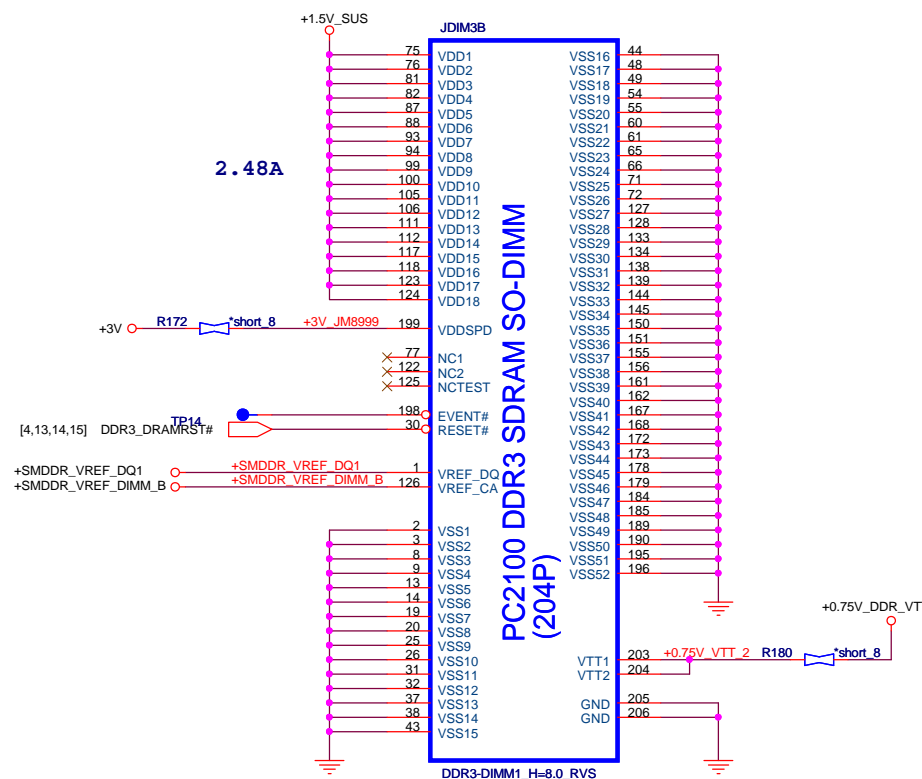
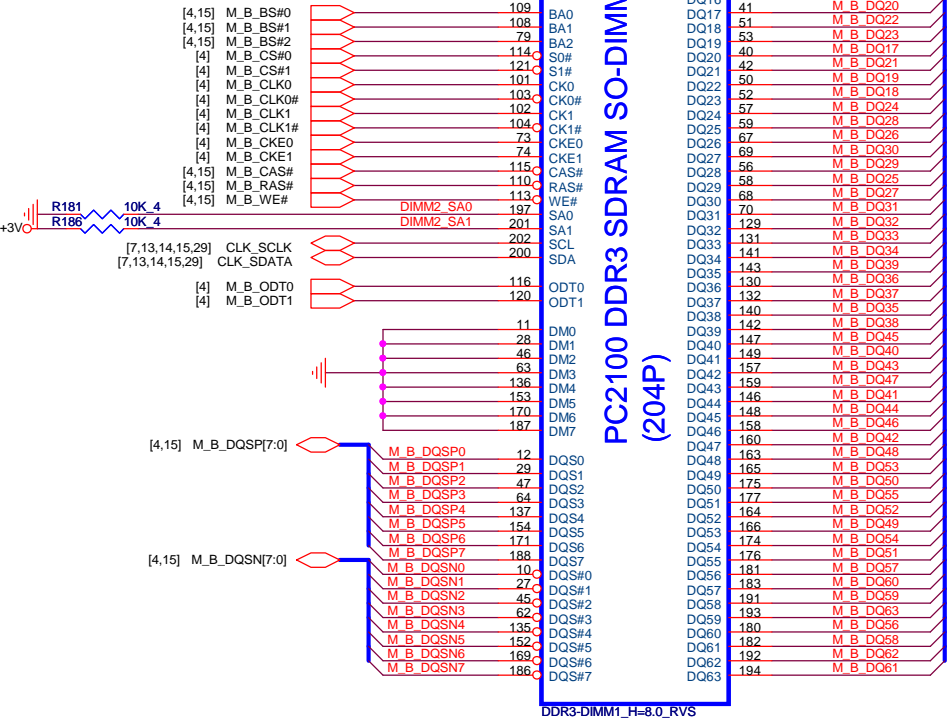
PC2100 DDR3 SDRAM SO-DIMM (204P)

PC2100 DDR3 SDRAM SO-DIMM (204P)

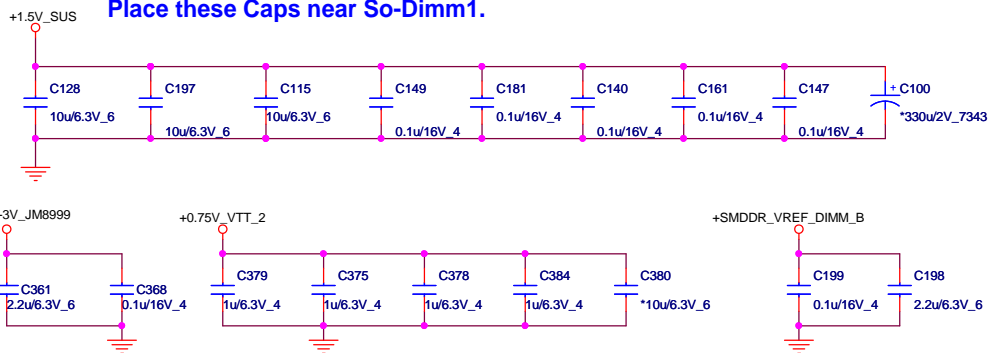
Place these Caps near So-Dimm1.



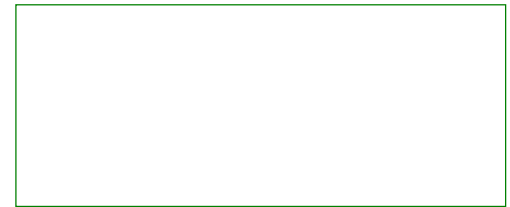
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near So-Dimm1.



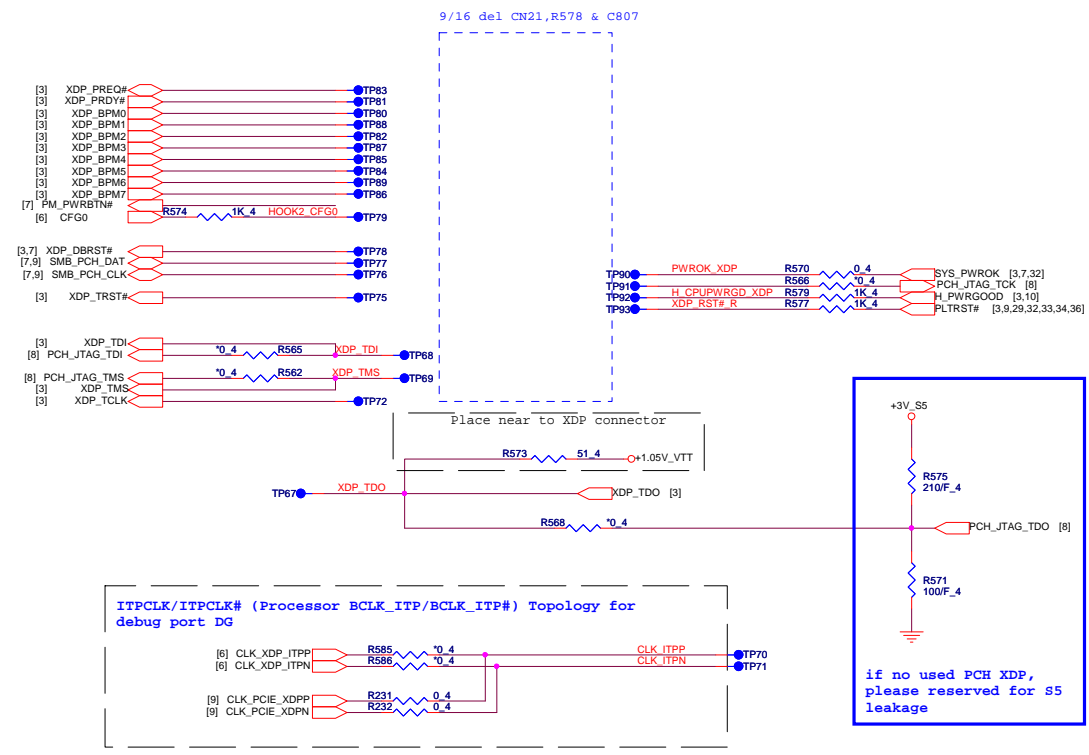
modify



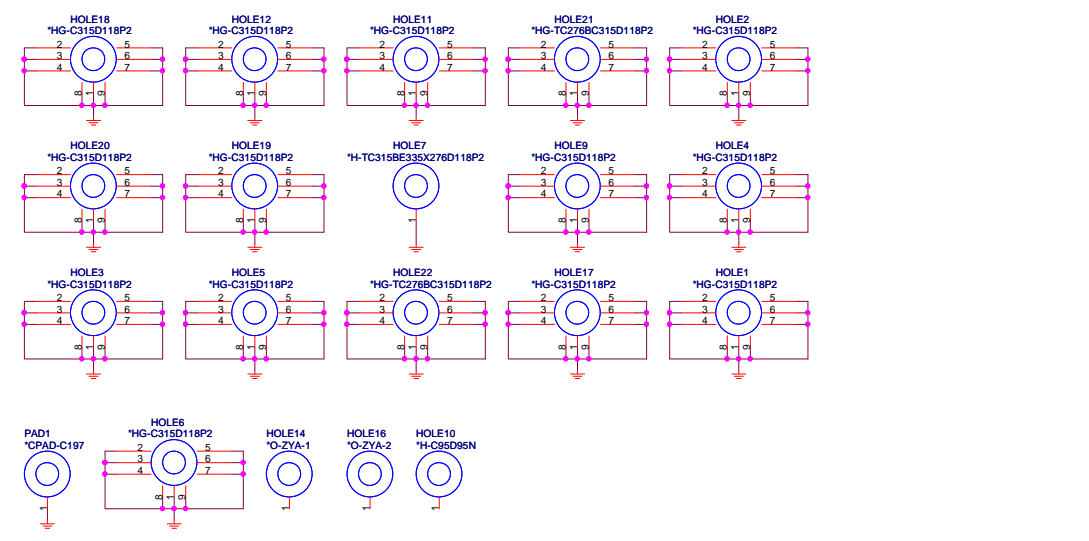
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	DDR3 SO-DIMM-1	1A
Date:	Monday, November 08, 2010	Sheet 16 of 50

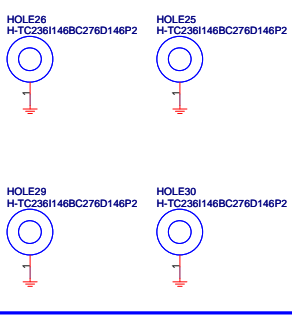
CPU XDP Connector(CPU)



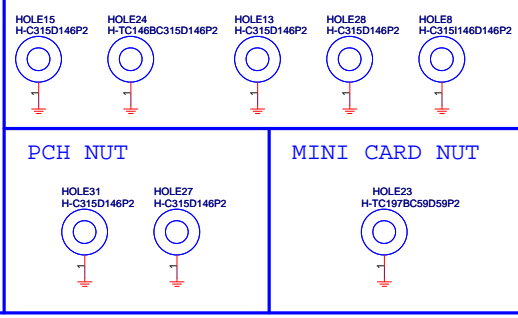
SCREW HOLE



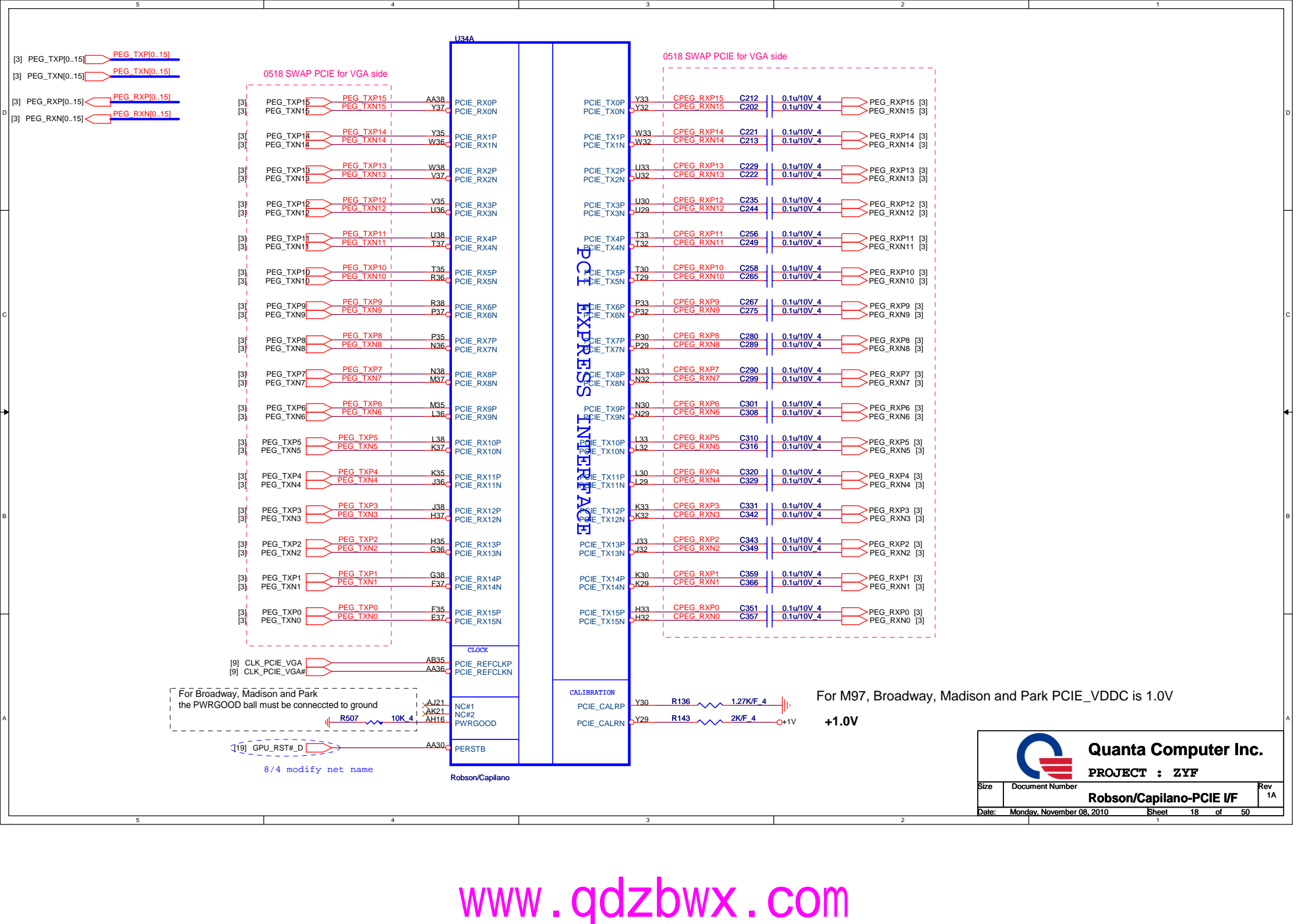
CPU NUT




PCH & GPU NUT



Quanta Computer Inc.
 PROJECT : ZYF
 Size Document Number Rev 1A
XDP Hole
 Date: Monday, November 08, 2010 Sheet 17 of 50



 Quanta Computer Inc. PROJECT : ZYF		Rev
		1A
Size	Document Number	Robson/Capilano-PCIE I/F
Date:	Monday, November 08, 2010	
Sheet		18 of 50

- [24] VMA_DQ[63..0] VMA_DQ[63..0]
- [24] VMA_DM[7..0] VMA_DM[7..0]
- [24] VMA_RDQS[7..0] VMA_RDQS[7..0]
- [24] VMA_WDQS[7..0] VMA_WDQS[7..0]

- [24] VMA_MA[13..0] VMA_MA[13..0]
- [24] VMA_BA0 VMA_BA0
- [24] VMA_BA1 VMA_BA1
- [24] VMA_BA2 VMA_BA2

- [25] VMB_DQ[63..0] VMB_DQ[63..0]
- [25] VMB_DM[7..0] VMB_DM[7..0]
- [25] VMB_RDQS[7..0] VMB_RDQS[7..0]
- [25] VMB_WDQS[7..0] VMB_WDQS[7..0]

- [25] VMB_MA[13..0] VMB_MA[13..0]
- [25] VMB_BA0 VMB_BA0
- [25] VMB_BA1 VMB_BA1
- [25] VMB_BA2 VMB_BA2

U34C

DDR2
DDR3 / DDR5
DDR3

MEMORY INTERFACE A

VMA_D00	C37	DQA0_0/DQA_0	MAA0_0/MAA_0	G24	VMA_MA0
VMA_D01	C38	DQA0_1/DQA_1	MAA0_1/MAA_1	J23	VMA_MA1
VMA_D02	A35	DQA0_2/DQA_2	MAA0_2/MAA_2	H24	VMA_MA2
VMA_D03	E34	DQA0_3/DQA_3	MAA0_3/MAA_3	J26	VMA_MA3
VMA_D04	G32	DQA0_4/DQA_4	MAA0_4/MAA_4	H25	VMA_MA4
VMA_D05	D33	DQA0_5/DQA_5	MAA0_5/MAA_5	J24	VMA_MA5
VMA_D06	F32	DQA0_6/DQA_6	MAA0_6/MAA_6	H26	VMA_MA6
VMA_D07	F32	DQA0_7/DQA_7	MAA0_7/MAA_7	G21	VMA_MA7
VMA_D08	F32	DQA0_8/DQA_8	MAA0_8/MAA_8	H19	VMA_MA8
VMA_D09	D31	DQA0_9/DQA_9	MAA0_9/MAA_9	H19	VMA_MA9
VMA_D10	F30	DQA0_10/DQA_10	MAA1_1/MAA_1	L13	VMA_MA10
VMA_D11	A30	DQA0_11/DQA_11	MAA1_2/MAA_2	G16	VMA_MA11
VMA_D12	F28	DQA0_12/DQA_12	MAA1_3/MAA_3	H16	VMA_MA12
VMA_D13	C28	DQA0_13/DQA_13	MAA1_4/MAA_4	H16	VMA_MA13
VMA_D14	A28	DQA0_14/DQA_14	MAA1_5/MAA_5	J17	VMA_BA0
VMA_D15	F28	DQA0_15/DQA_15	MAA1_6/MAA_6	H17	VMA_BA1
VMA_D16	D27	DQA0_16/DQA_16	MAA1_7/MAA_7	H17	VMA_BA2
VMA_D17	F26	DQA0_17/DQA_17	WCKA0_0/DQMA_0	A32	VMA_DM0
VMA_D18	C26	DQA0_18/DQA_18	WCKA0B_0/DQMA_1	C32	VMA_DM1
VMA_D19	A26	DQA0_19/DQA_19	WCKA0_1/DQMA_2	D23	VMA_DM2
VMA_D20	F24	DQA0_20/DQA_20	WCKA0B_1/DQMA_3	E22	VMA_DM3
VMA_D21	C24	DQA0_21/DQA_21	WCKA1_0/DQMA_4	D21	VMA_DM4
VMA_D22	A24	DQA0_22/DQA_22	WCKA1B_0/DQMA_5	A14	VMA_DM5
VMA_D23	F24	DQA0_23/DQA_23	WCKA1_1/DQMA_6	E19	VMA_DM6
VMA_D24	C22	DQA0_24/DQA_24	WCKA1B_1/DQMA_7	D9	VMA_DM7
VMA_D25	A22	DQA0_25/DQA_25	EDCA0_0/QSA_0/RDQSA_0	C34	VMA_RDQS0
VMA_D26	F22	DQA0_26/DQA_26	EDCA0_1/QSA_1/RDQSA_1	D29	VMA_RDQS1
VMA_D27	D21	DQA0_27/DQA_27	EDCA0_2/QSA_2/RDQSA_2	D25	VMA_RDQS2
VMA_D28	A20	DQA0_28/DQA_28	EDCA0_3/QSA_3/RDQSA_3	E20	VMA_RDQS3
VMA_D29	F20	DQA0_29/DQA_29	EDCA1_0/QSA_4/RDQSA_4	E16	VMA_RDQS4
VMA_D30	D19	DQA0_30/DQA_30	EDCA1_1/QSA_5/RDQSA_5	E12	VMA_RDQS5
VMA_D31	E18	DQA0_31/DQA_31	EDCA1_2/QSA_6/RDQSA_6	C18	VMA_RDQS6
VMA_D32	C18	DQA0_32/DQA_32	EDCA1_3/QSA_7/RDQSA_7	D7	VMA_RDQS7
VMA_D33	A18	DQA1_0/DQA_33			
VMA_D34	F18	DQA1_1/DQA_34			
VMA_D35	D17	DQA1_2/DQA_35			
VMA_D36	A16	DQA1_3/DQA_36			
VMA_D37	F16	DQA1_4/DQA_37			
VMA_D38	D15	DQA1_5/DQA_38			
VMA_D39	E14	DQA1_6/DQA_39			
VMA_D40	F14	DQA1_7/DQA_40			
VMA_D41	D13	DQA1_8/DQA_41			
VMA_D42	F12	DQA1_9/DQA_42			
VMA_D43	A12	DQA1_10/DQA_43			
VMA_D44	D11	DQA1_11/DQA_44			
VMA_D45	F10	DQA1_12/DQA_45			
VMA_D46	A10	DQA1_13/DQA_46			
VMA_D47	C10	DQA1_14/DQA_47			
VMA_D48	G13	DQA1_15/DQA_48			
VMA_D49	H13	DQA1_16/DQA_49			
VMA_D50	J13	DQA1_17/DQA_50			
VMA_D51	K13	DQA1_18/DQA_51			
VMA_D52	L13	DQA1_19/DQA_52			
VMA_D53	M13	DQA1_20/DQA_53			
VMA_D54	N13	DQA1_21/DQA_54			
VMA_D55	P13	DQA1_22/DQA_55			
VMA_D56	Q13	DQA1_23/DQA_56			
VMA_D57	R13	DQA1_24/DQA_57			
VMA_D58	S13	DQA1_25/DQA_58			
VMA_D59	T13	DQA1_26/DQA_59			
VMA_D60	U13	DQA1_27/DQA_60			
VMA_D61	V13	DQA1_28/DQA_61			
VMA_D62	W13	DQA1_29/DQA_62			
VMA_D63	X13	DQA1_30/DQA_63			

QSA[7..0]

QSA#[7..0]

ADBI#0/ODT#0

ADBI#1/ODT#1

CLK#0

CLK#1

CLK#2

CLK#3

CLK#4

CLK#5

CLK#6

CLK#7

CLK#8

CLK#9

CLK#10

CLK#11

CLK#12

CLK#13

CLK#14

CLK#15

CLK#16

CLK#17

CLK#18

CLK#19

CLK#20

CLK#21

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CLK#141

CLK#142

CLK#143

CLK#144

CLK#145

CLK#146

CLK#147

CLK#148

CLK#149

CLK#150

CLK#151

CLK#152

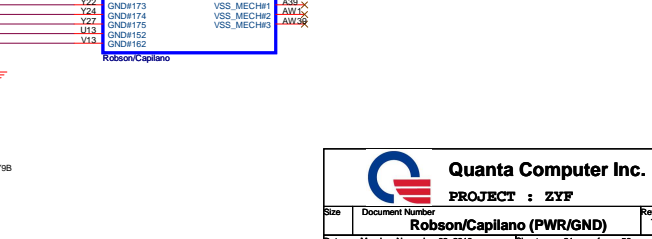
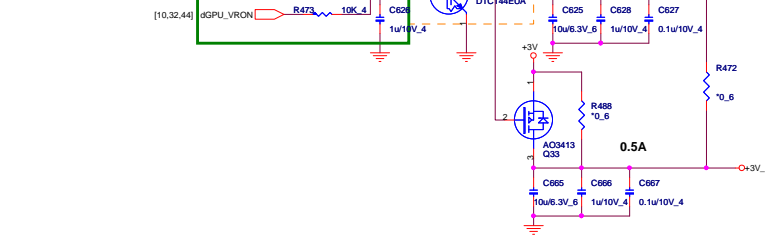
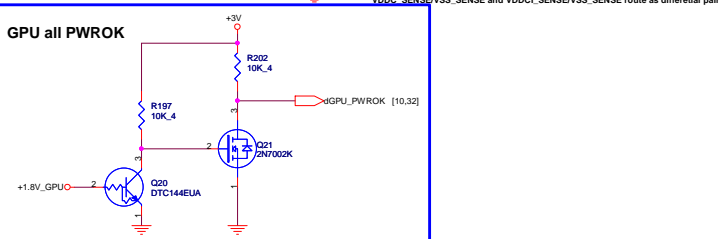
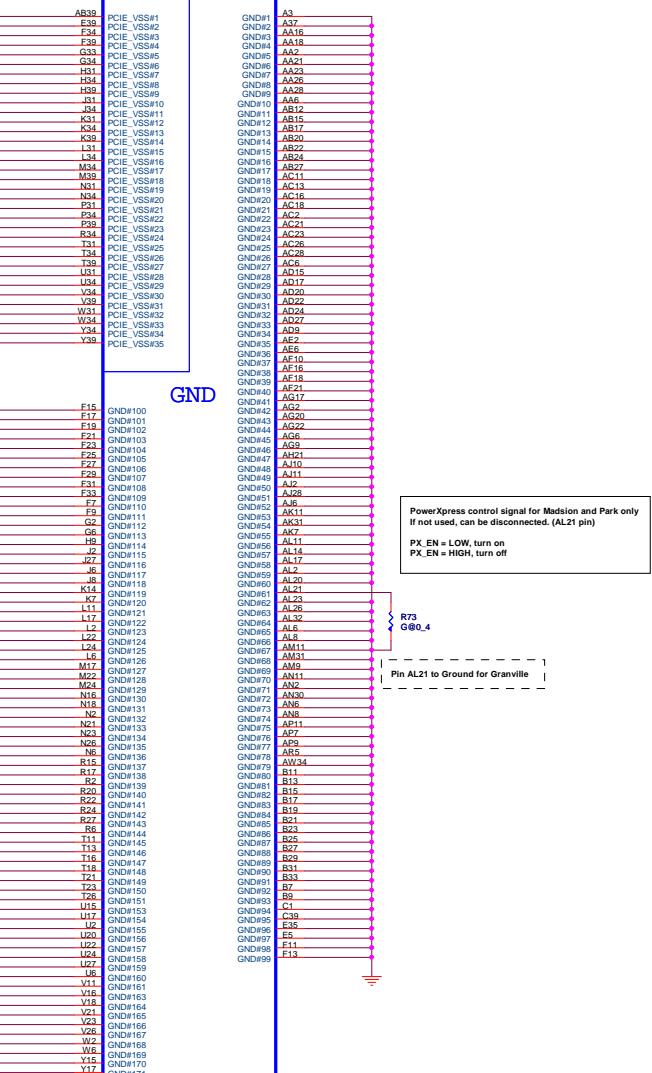
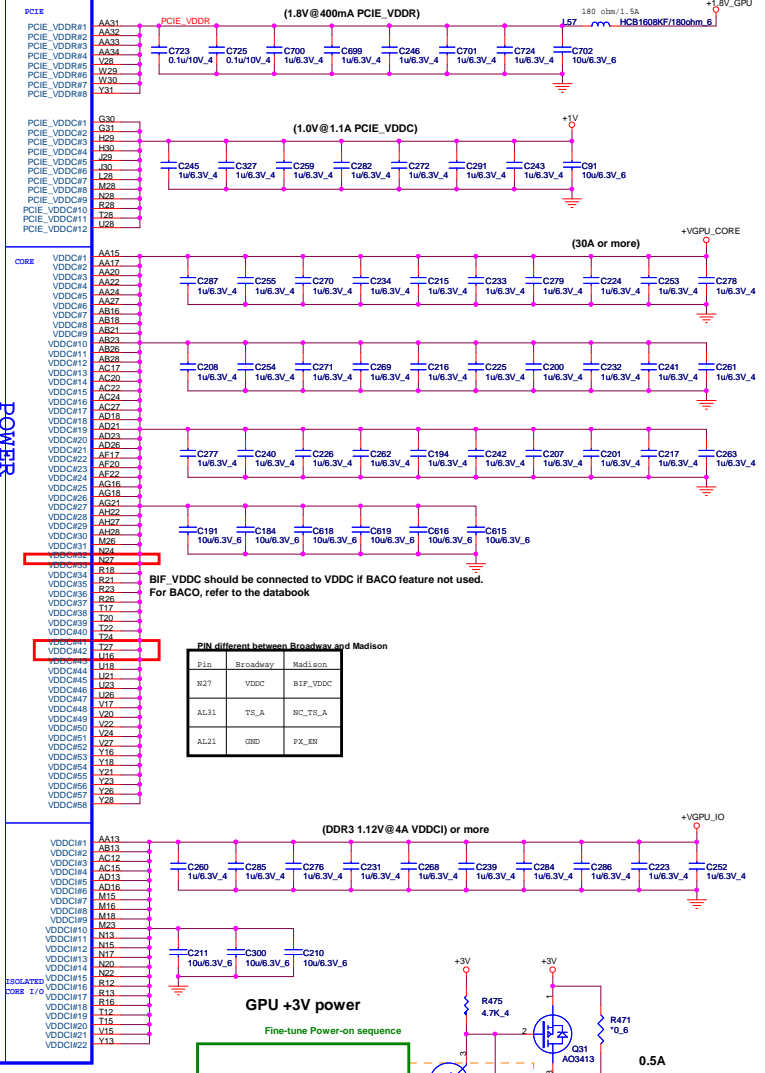
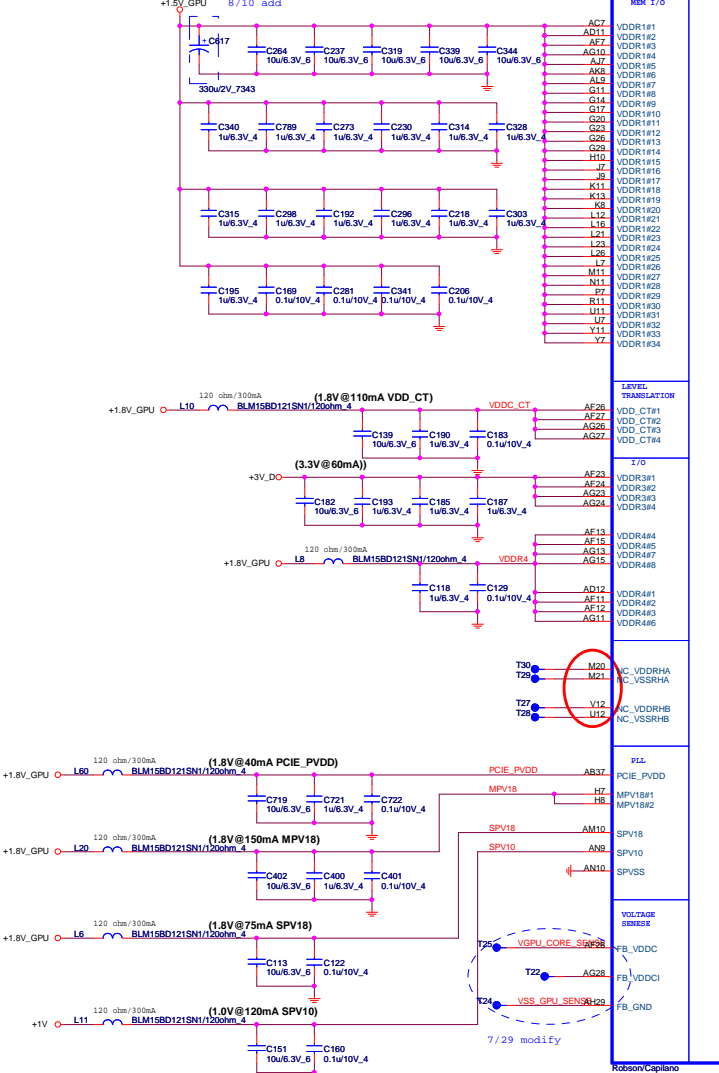
CLK#153

CLK#154

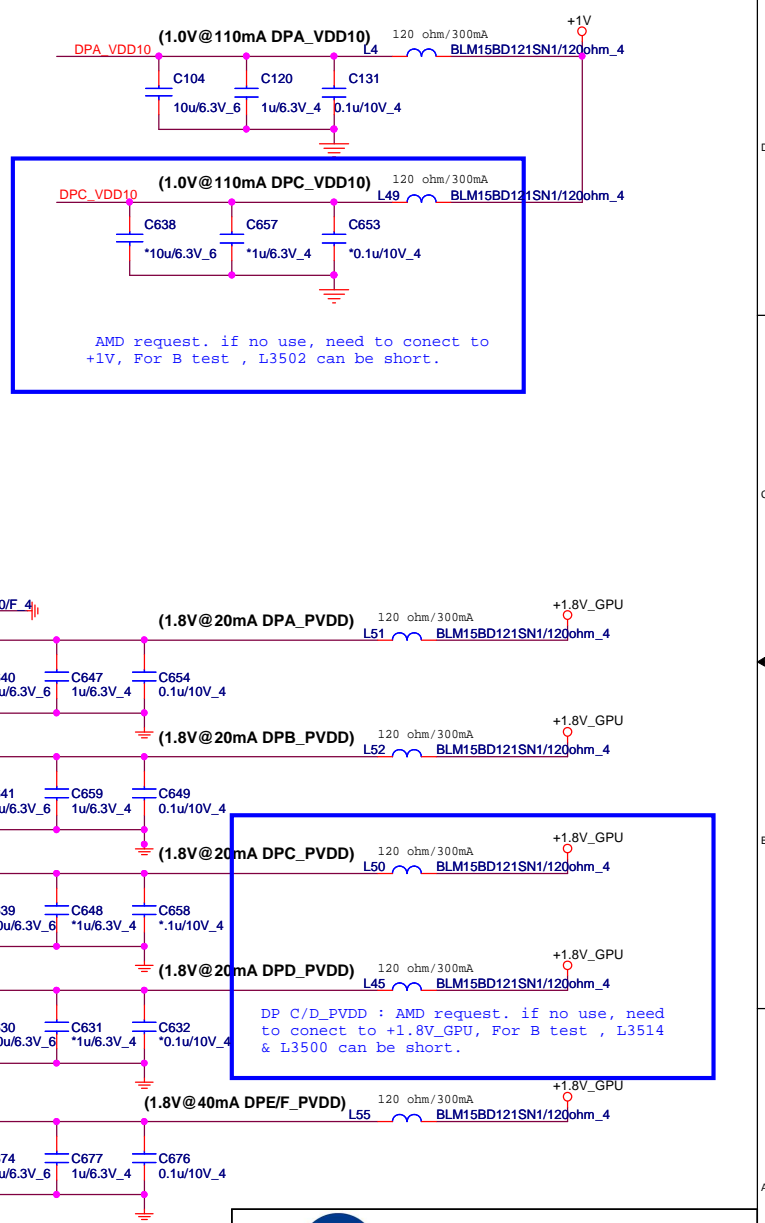
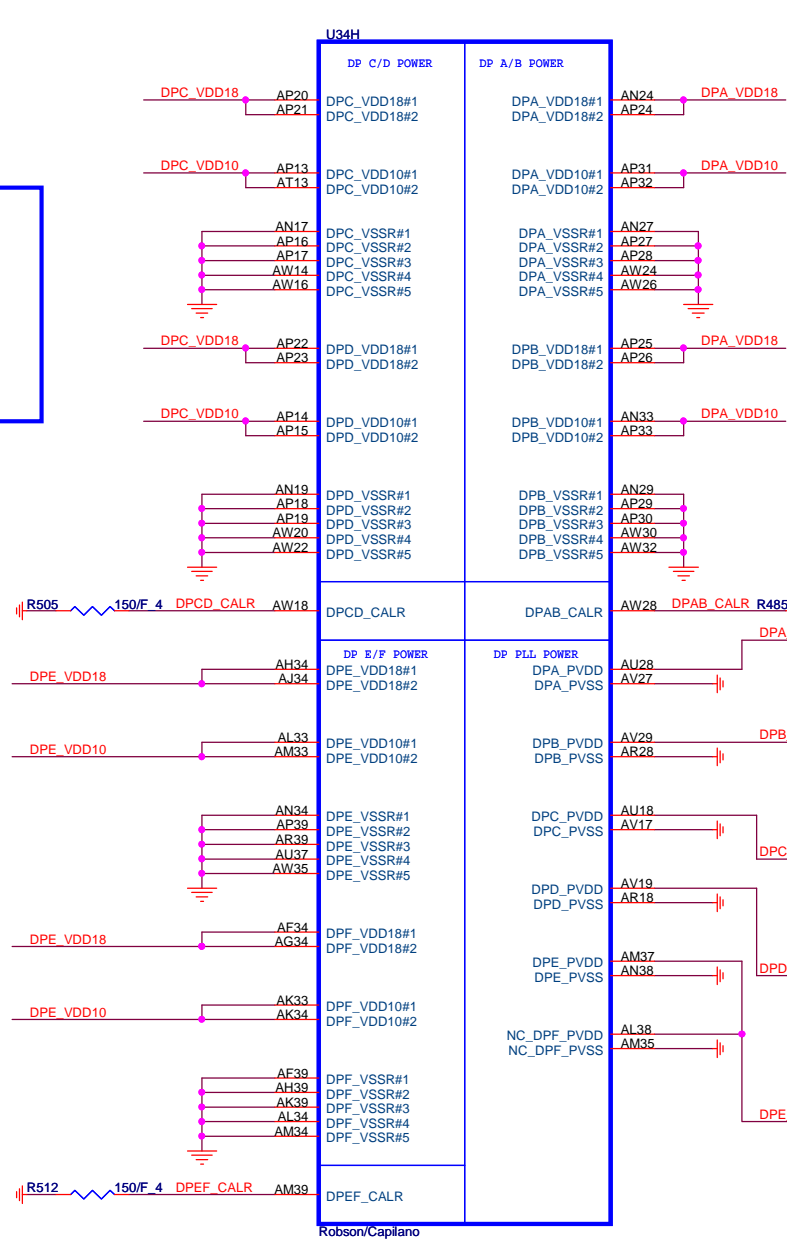
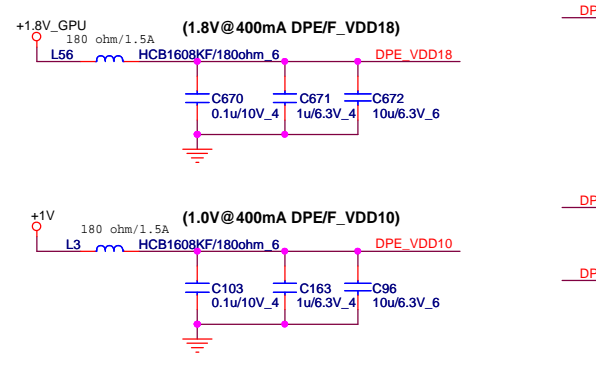
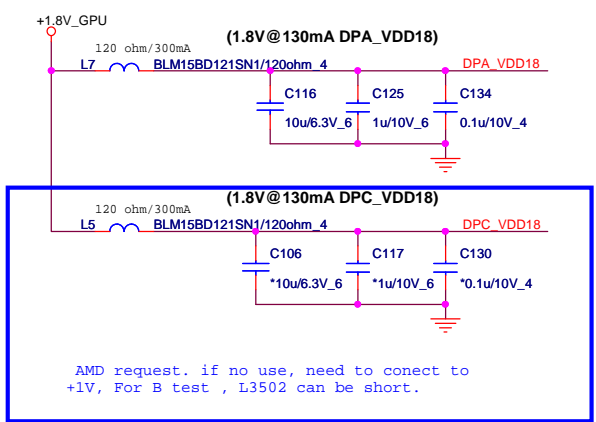
CLK#155

CLK#156

For DDR3, MVDDQ = 1.5V (7.5A)



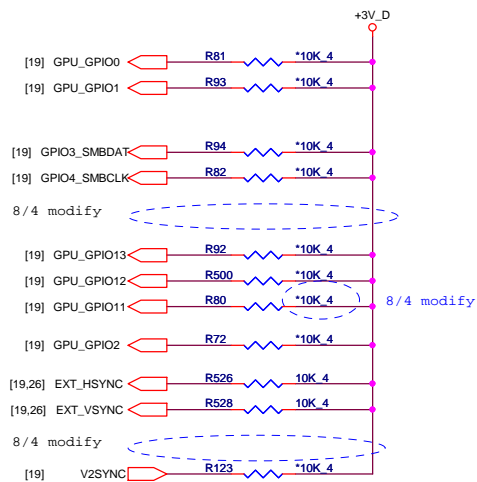
QUANTA Computer Inc.
 PROJECT : ZYF
 Robson/Capilano (PWR/GND)
 Date: Monday, November 08, 2010 Sheet 21 of 50



Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	Robson/Capilano (DP_PWR/GND)	1A
Date:	Monday, November 08, 2010	Sheet 22 of 50

PIN STRAPS



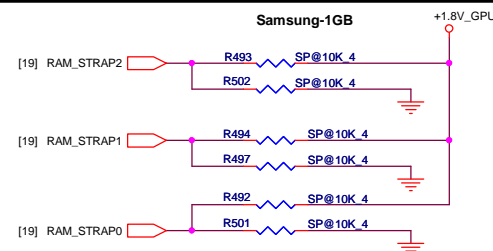
Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 VRAM SIZE Strap

DDR3 VRAM size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW05	1GB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04	1GB	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03	2GB	1	0	1
Samsung	K4W1G1646G-HC11	AKD5EGGT503		0	1	1
	K4W1G1646E-HC12	AKD5LGGT506	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT511	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700	1GB	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

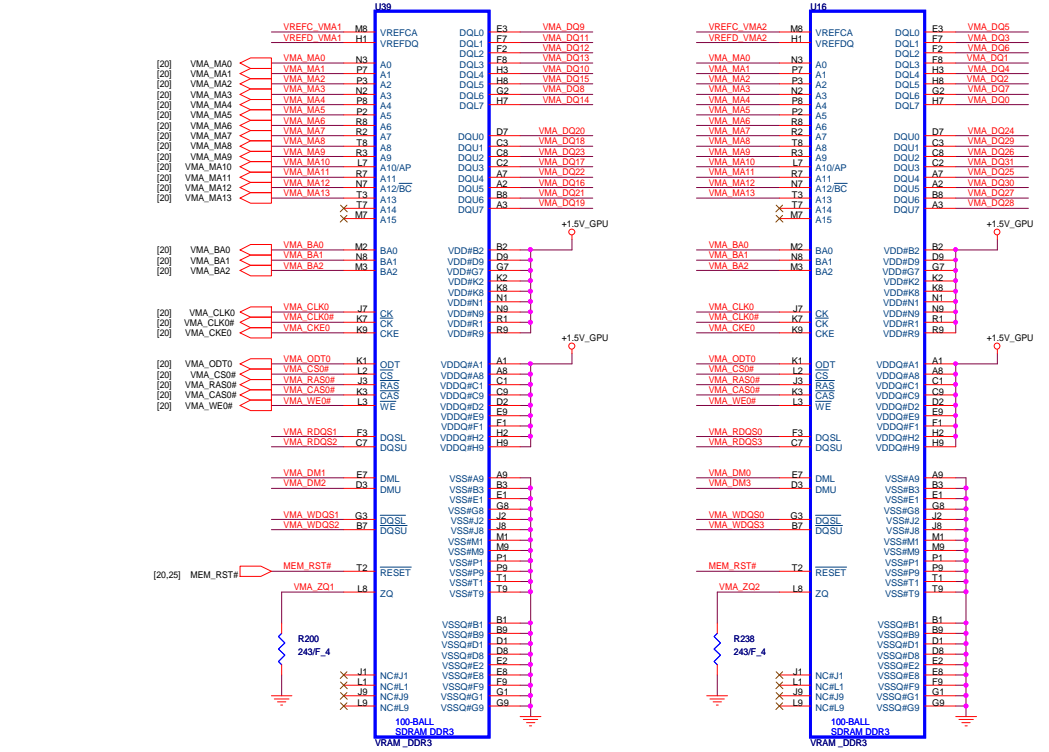
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	Strip/Thermal	1A
Date:	Monday, November 08, 2010	Sheet 23 of 50

CHANNEL A: 512 / 1GMB DDR3 (64/128M*16*4pcs)

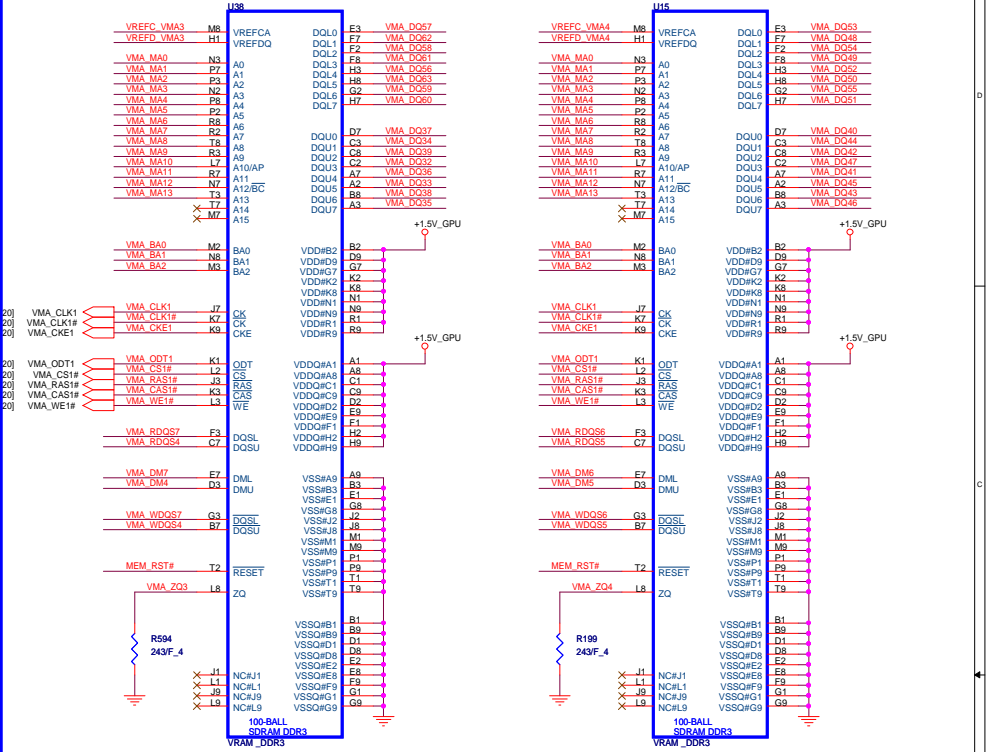
- [20] VMA_DQ[63..0] → VMA_DQ[63..0]
- [20] VMA_DM[7..0] → VMA_DM[7..0]
- [20] VMA_RDSQ[7..0] → VMA_RDSQ[7..0]
- [20] VMA_WDSQ[7..0] → VMA_WDSQ[7..0]

QSA[7..0]
QSA#[7..0]



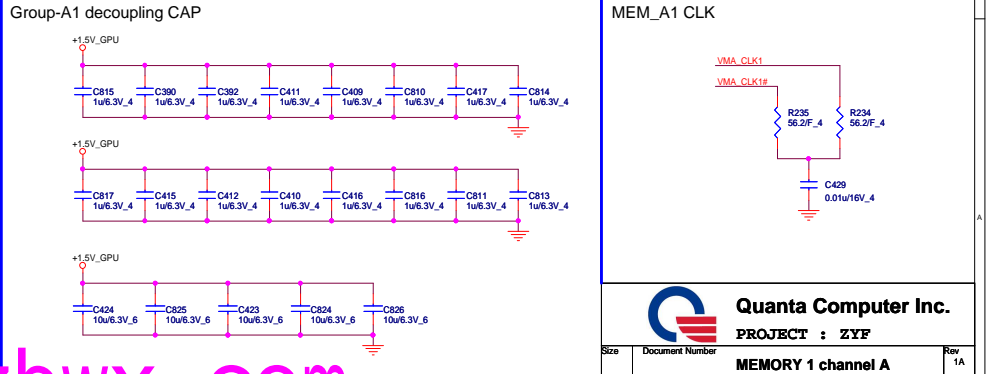
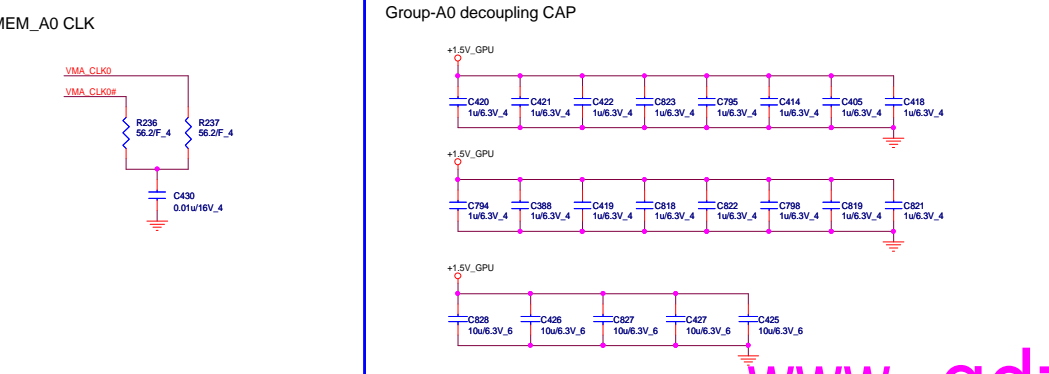
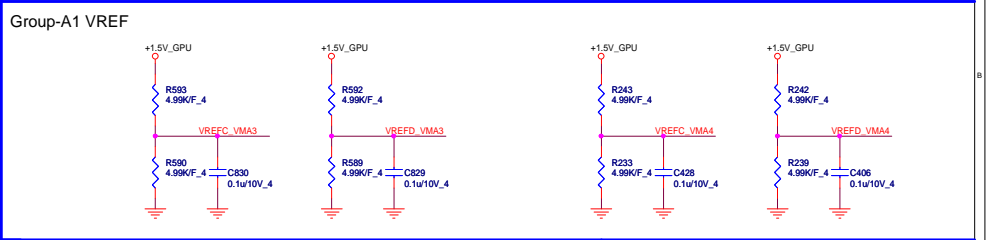
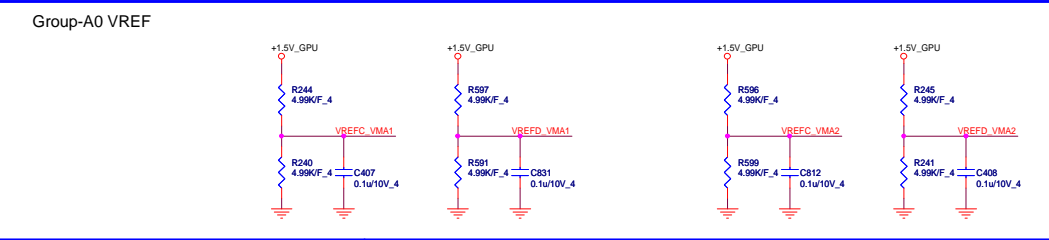
TOP Left

BOT Left



BOT Right

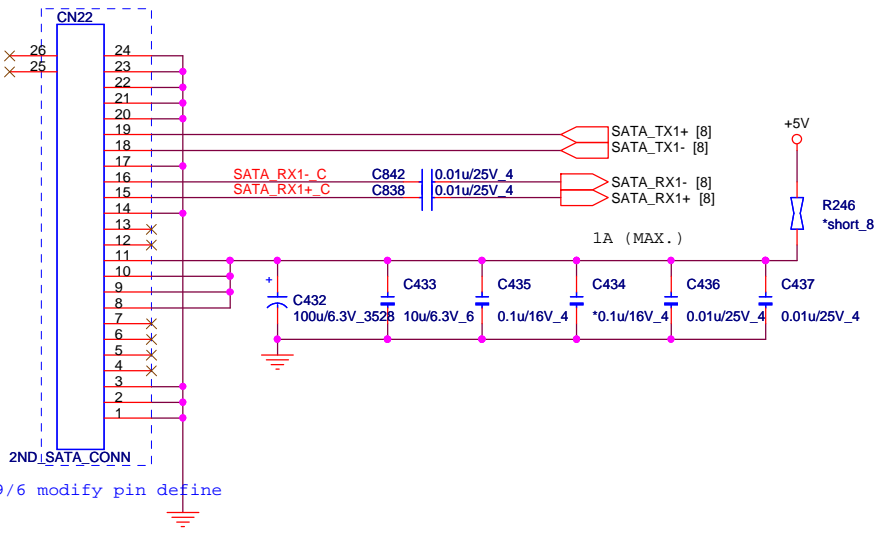
TOP Right



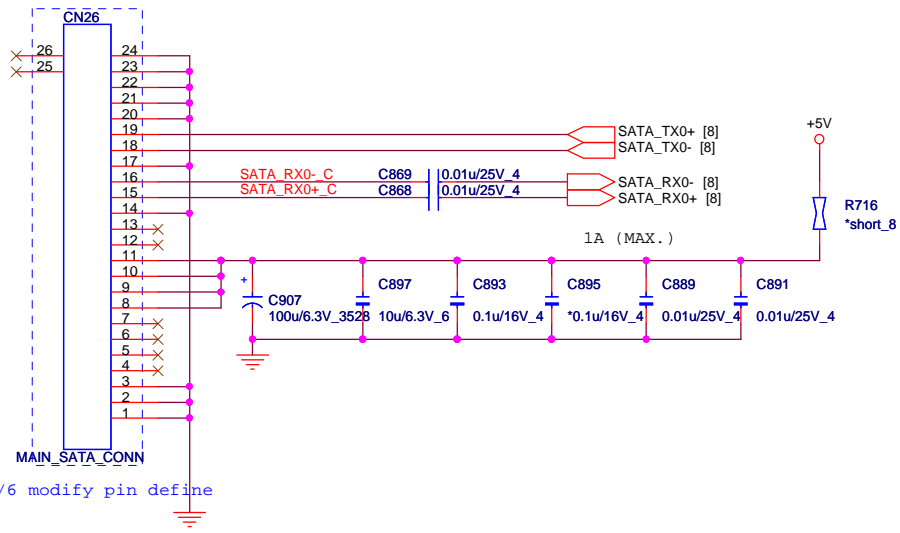
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	MEMORY 1 channel A	Rev 1A
Date	Monday, November 08, 2010	Sheet	24 of 50

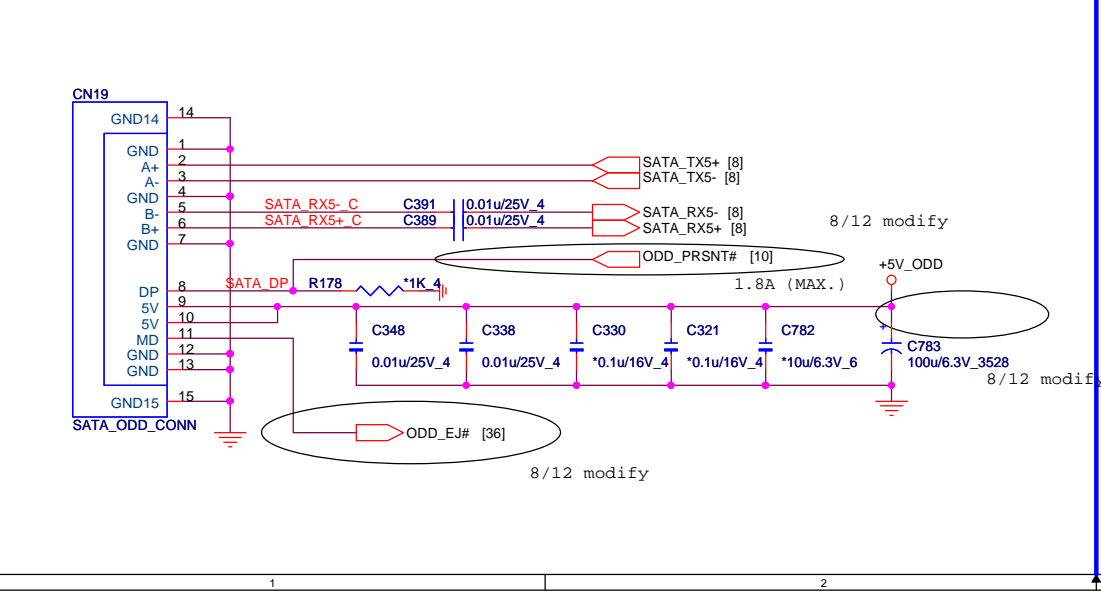
2nd SATA HDD (edge of board)



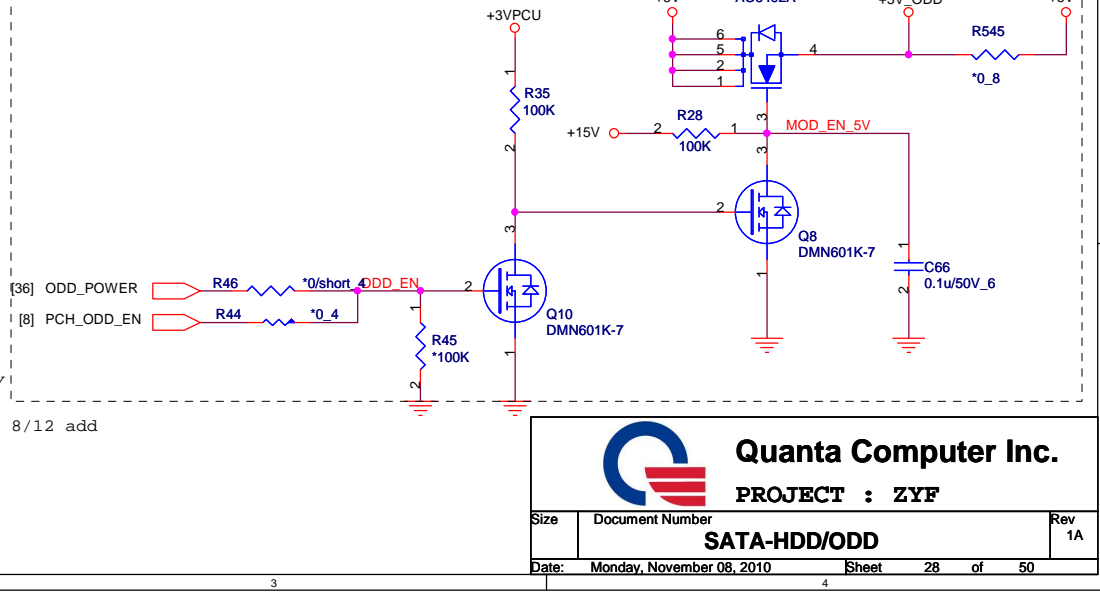
MAIN SATA HDD



ODD (SATA)



ODD Power (SATA)



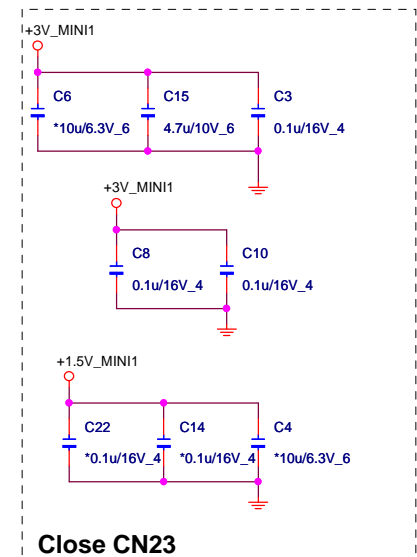
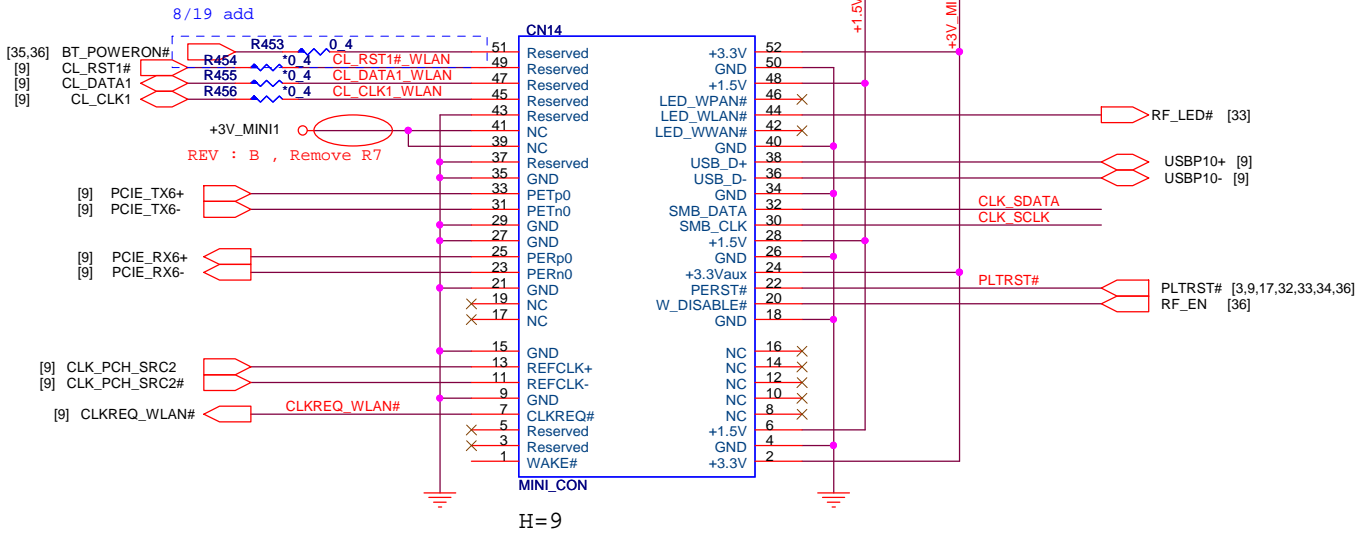
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date:	Monday, November 08, 2010	Sheet 28 of 50

Wireless

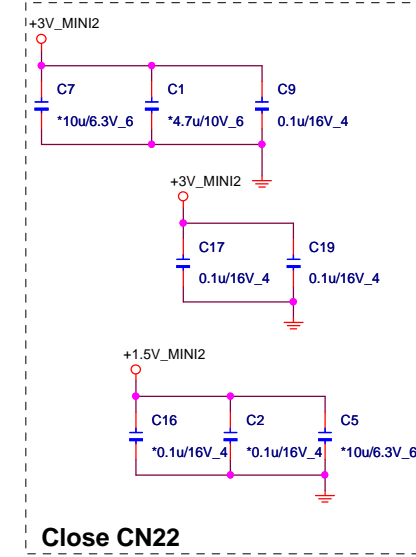
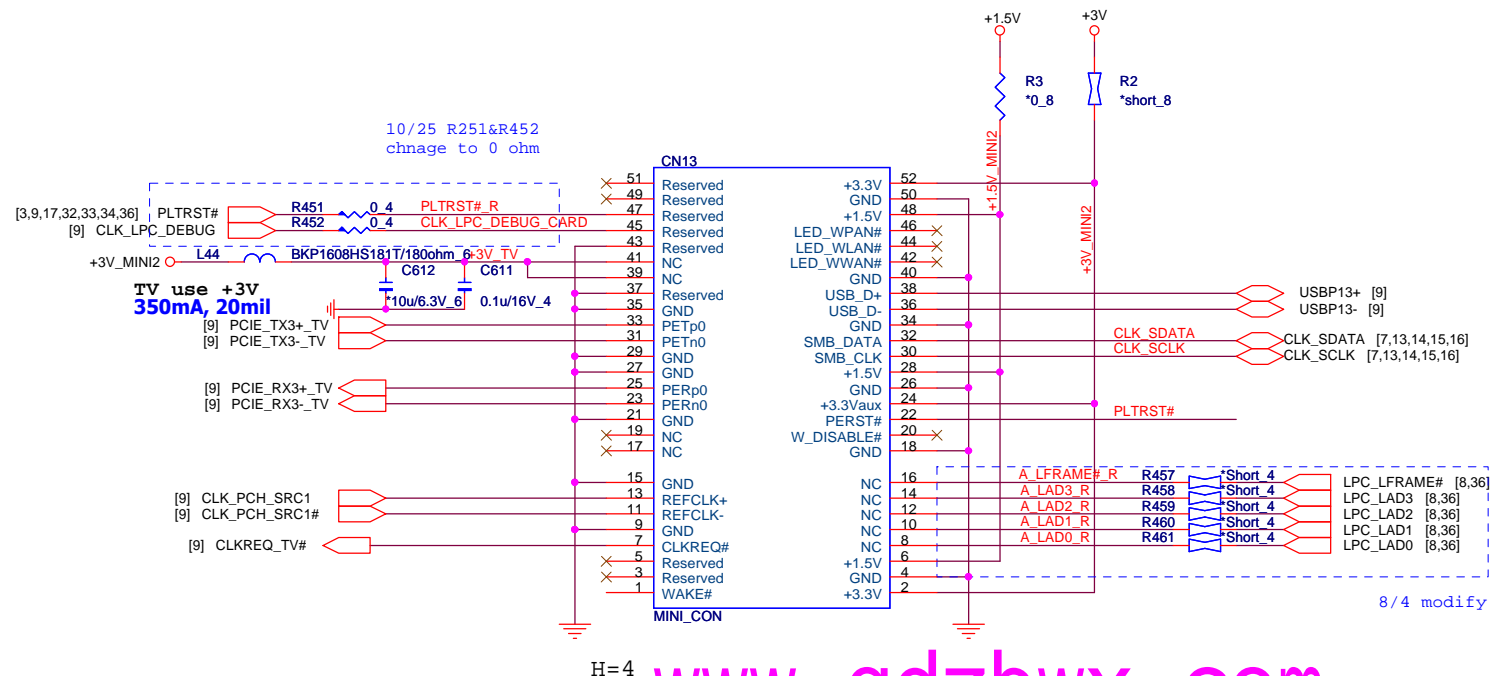
+3.3V: 2700mA
+1.5V: 500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



TV and Debug

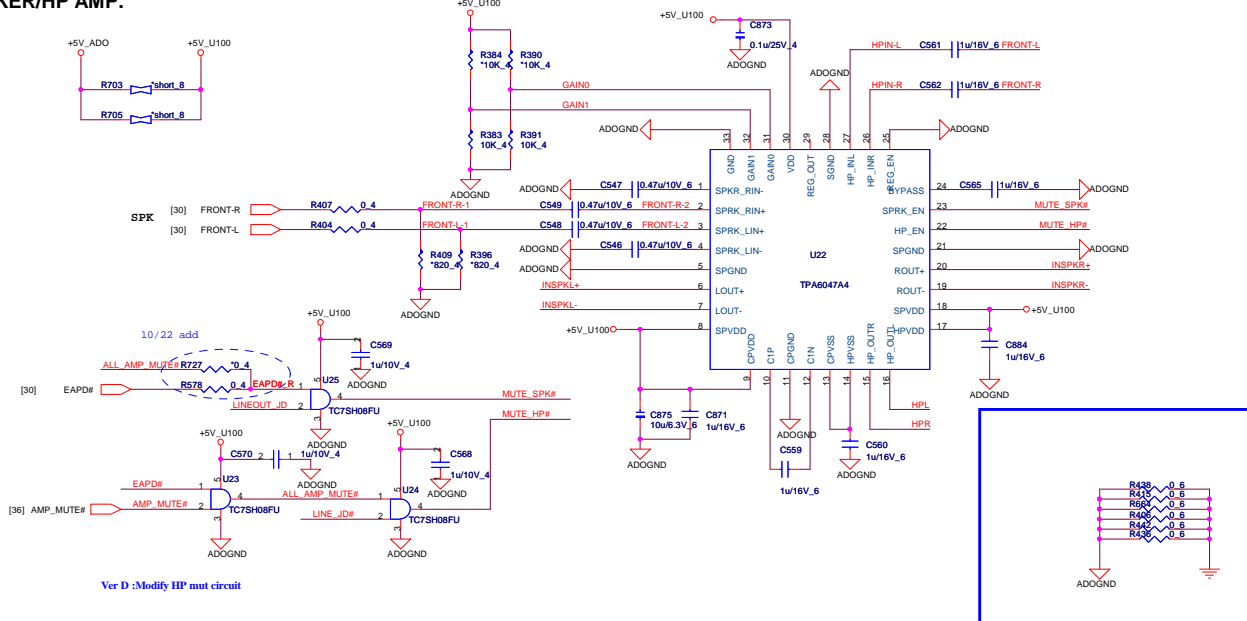
10/25 R251&R452
chnage to 0 ohm



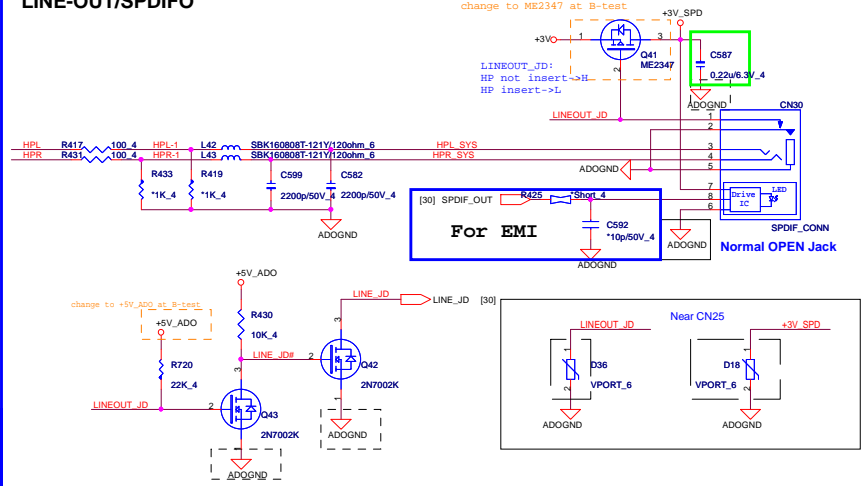
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date:	Monday, November 08, 2010	Sheet 29 of 50

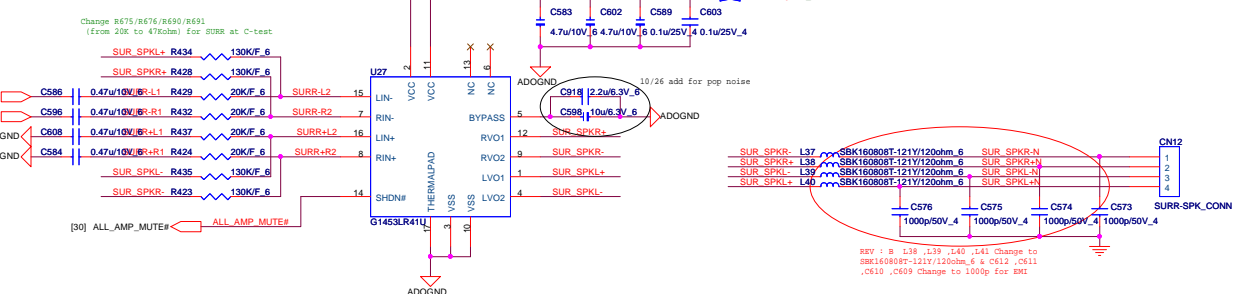
SPEAKER/HP AMP.



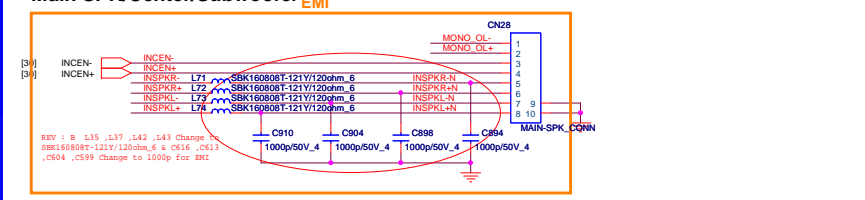
LINE-OUT/SPDIF0



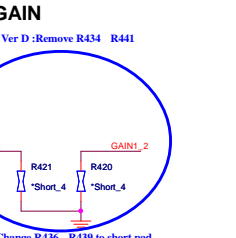
SURR-SPK



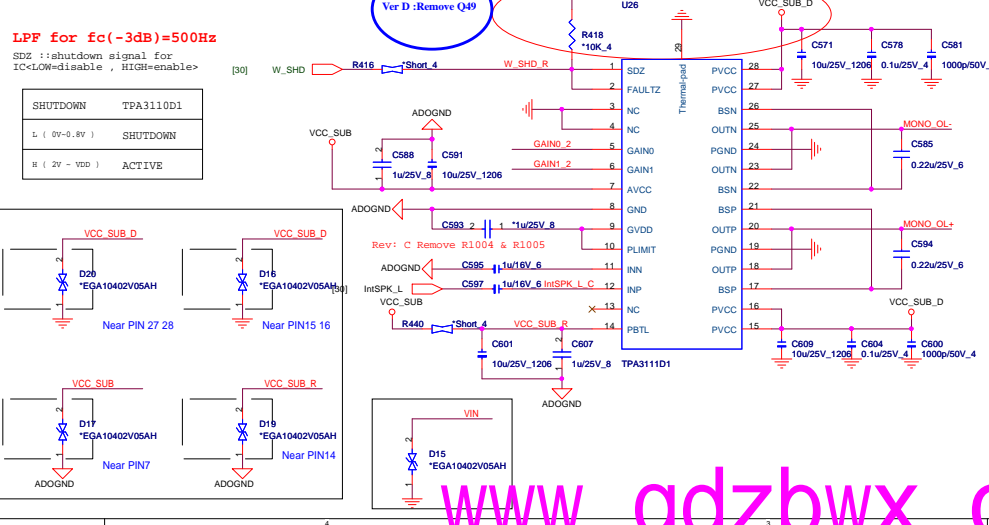
Main SPK/Center/Subwoofer EMI



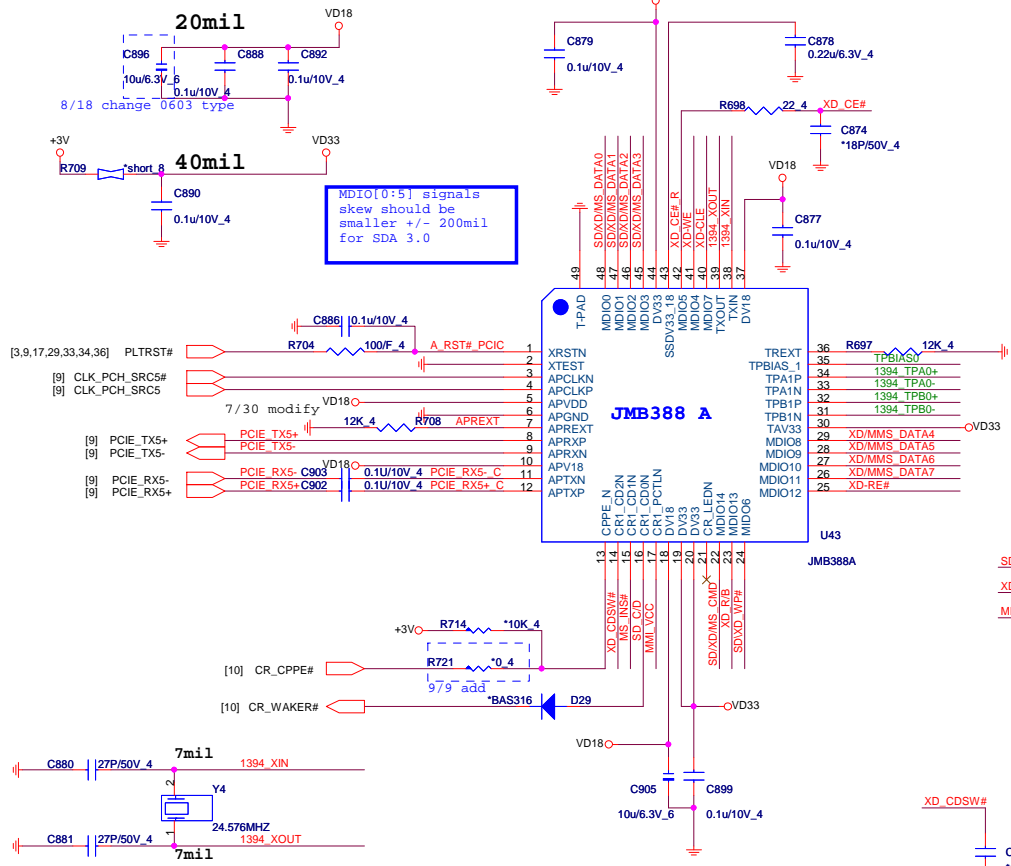
AMO GAIN



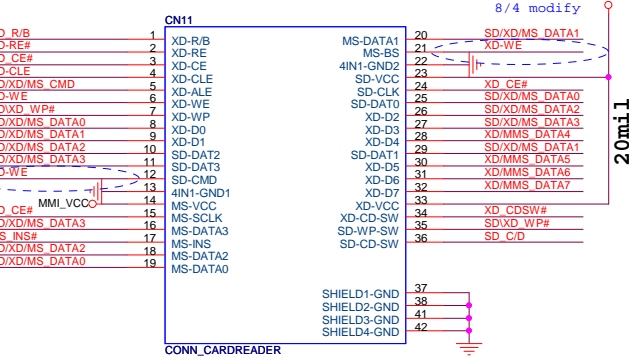
SUBWOOFER



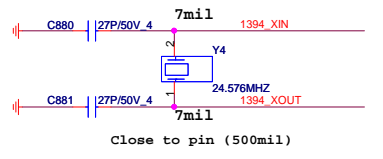
Card Reader



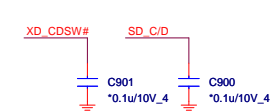
MDIO[0:5] signals skew should be smaller +/- 200mil for SDA 3.0



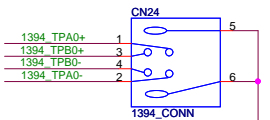
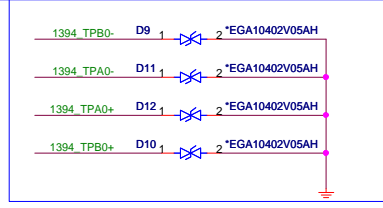
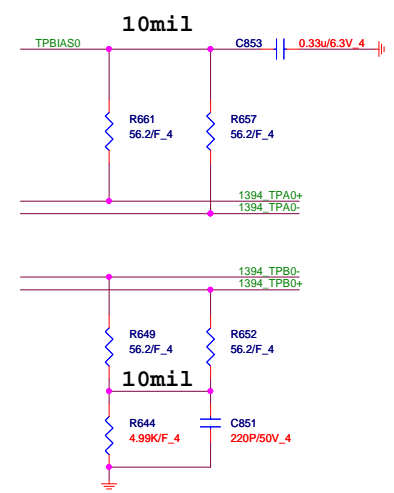
As close as possible to CN35 Pin12



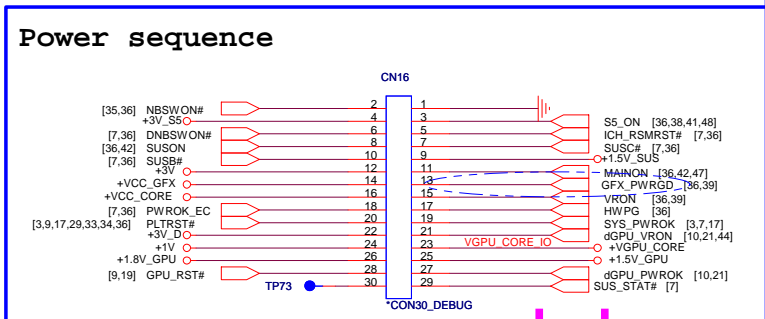
Close to pin (500mil)



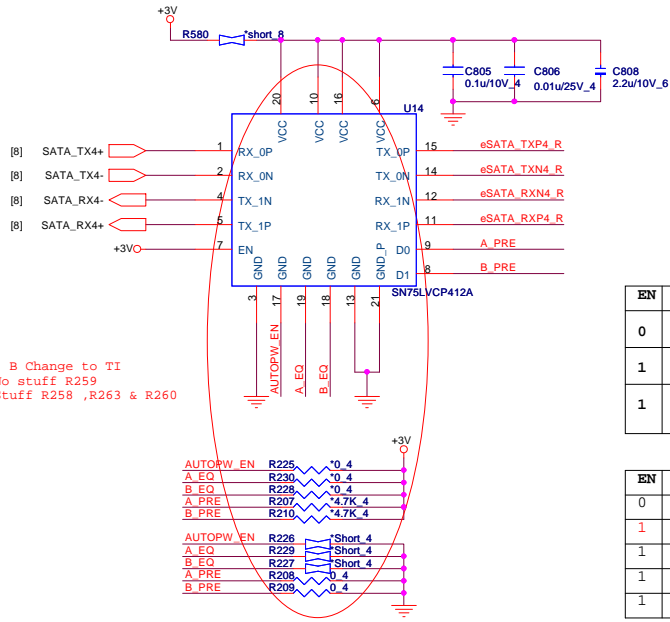
1394 [FIW]



These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.



ESATA & USB

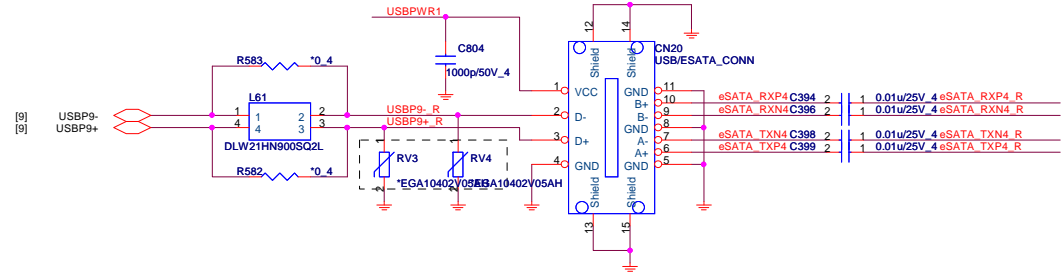
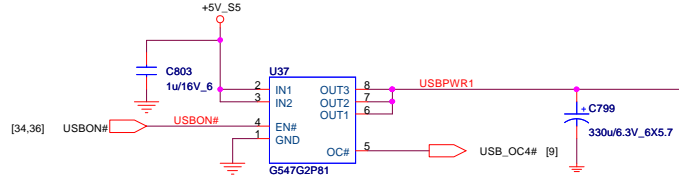


AL008511001

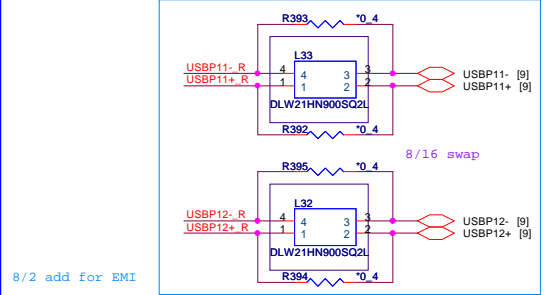
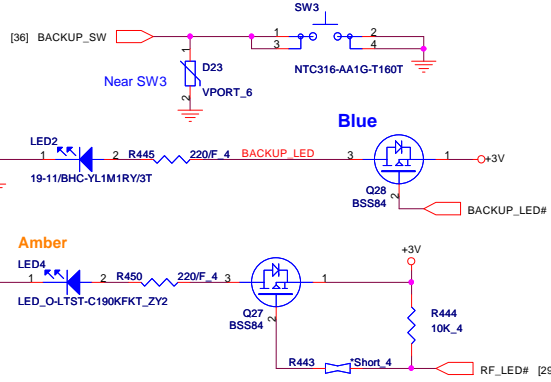
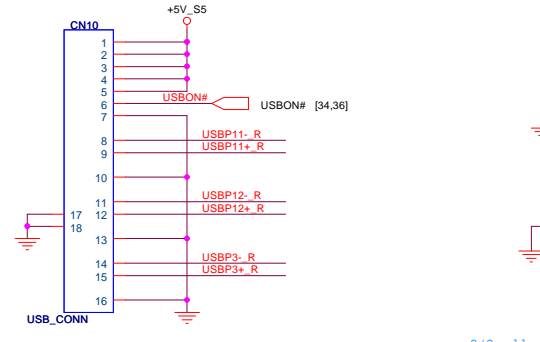
EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

ALLVC412000

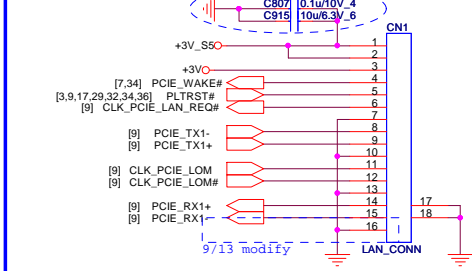
EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)



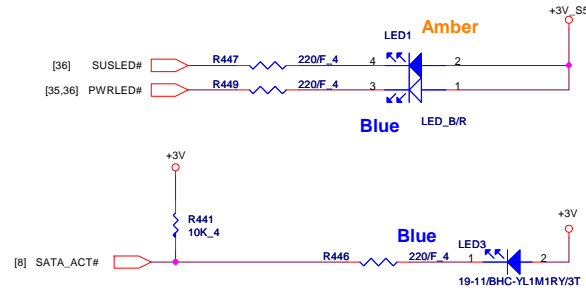
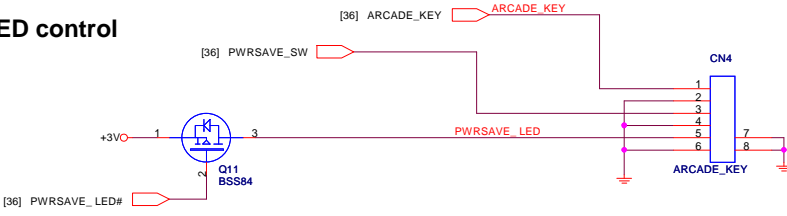
To USB/B

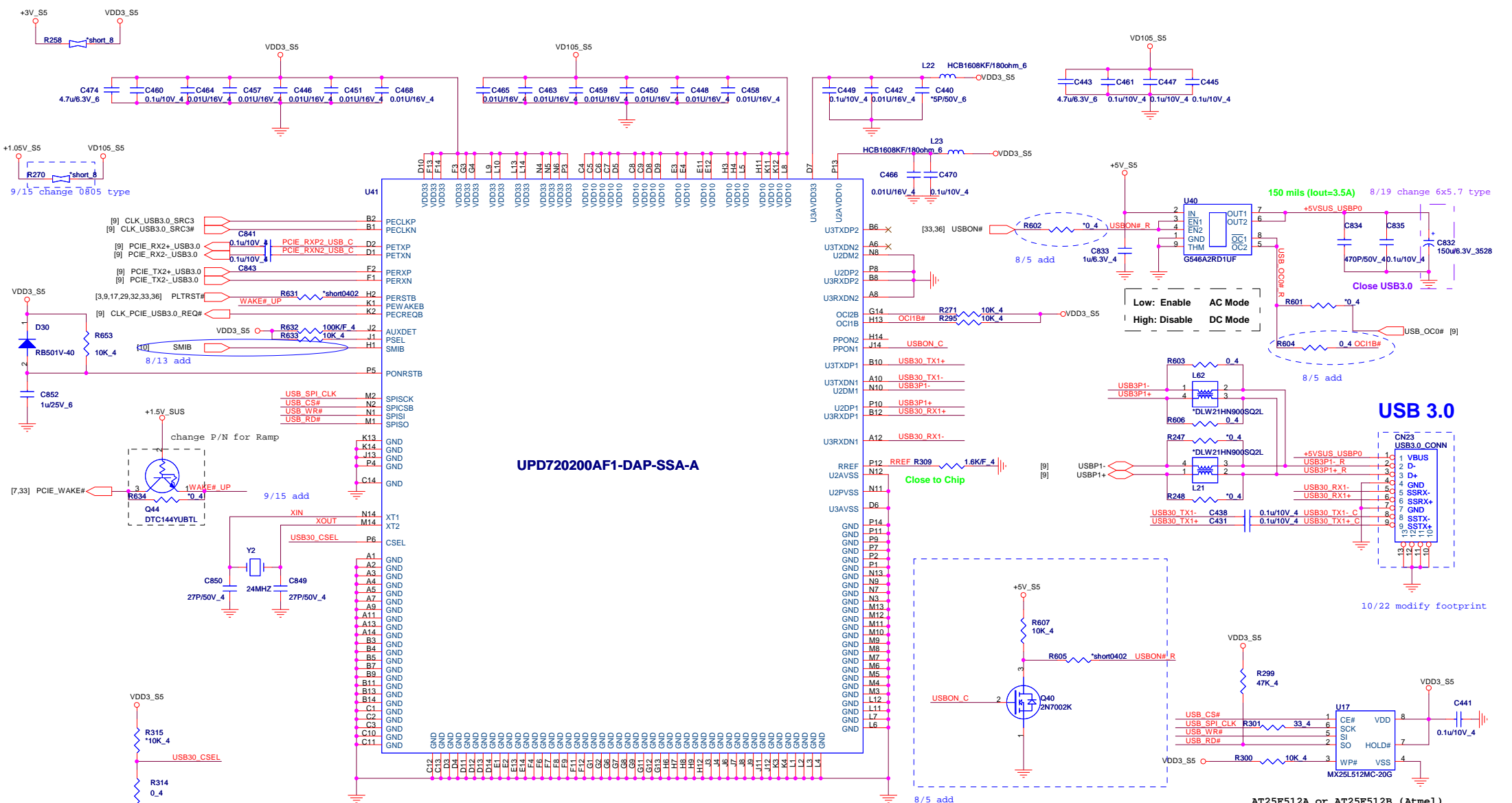


To LAN/B



Keyboard LED control





UPD720200AF1-DAP-SSA-A

Low: Enable AC Mode
High: Disable DC Mode

USB 3.0

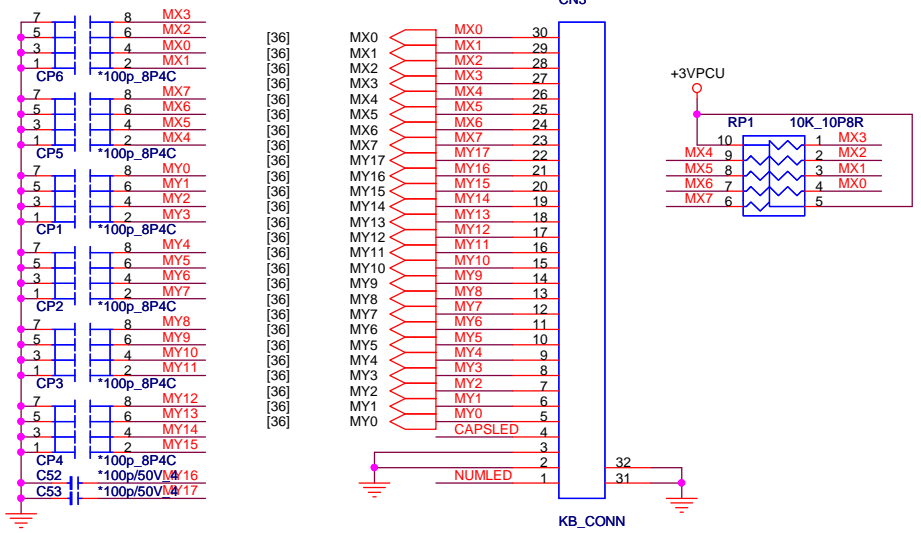
Clock select signal	
USB3.0_CSEL	High = External 48Mhz
	Low = 24MHz X'tal

AT25F512A or AT25F512B (Atmel)
AKE34FP0200 or AKE53FP0200 (Macronix)

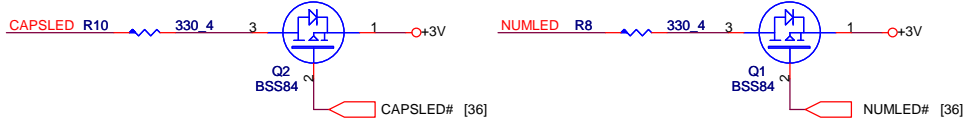
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	USB 3.0	Rev	1A
Date:	Monday, November 08, 2010	Sheet	34	of 50

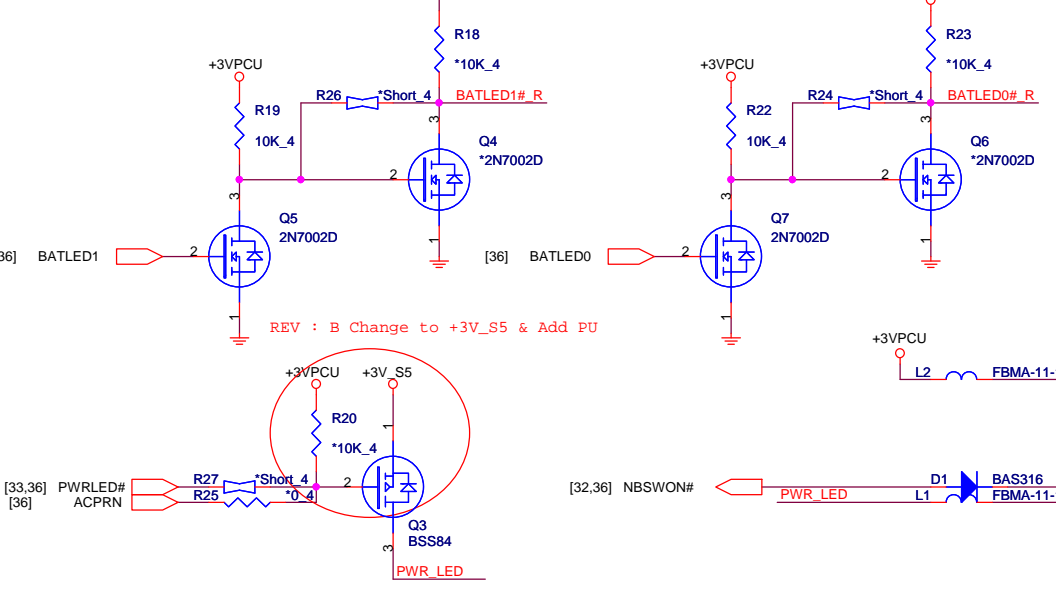
INT K/B



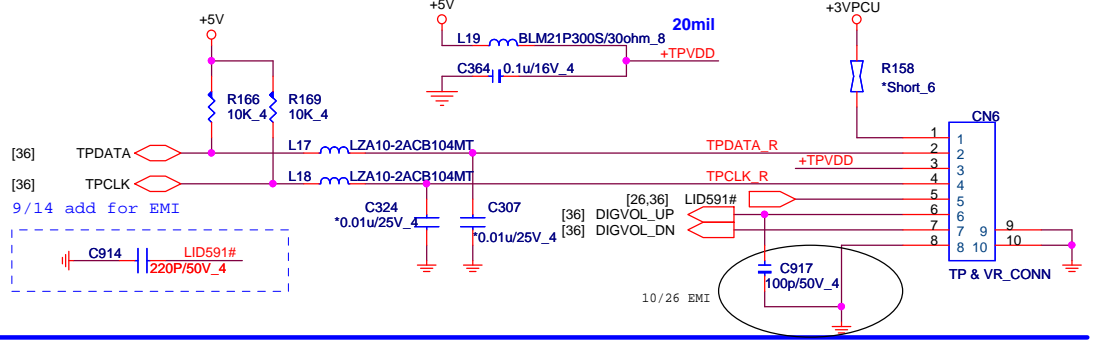
AMBER LED (HKC)



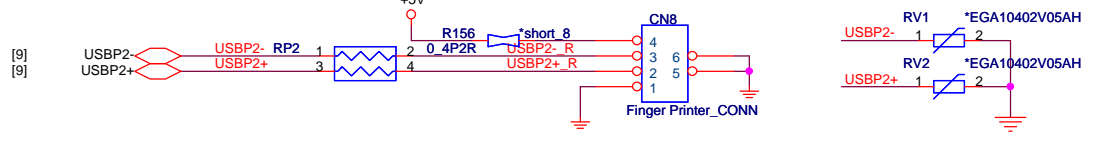
POWER BOARD



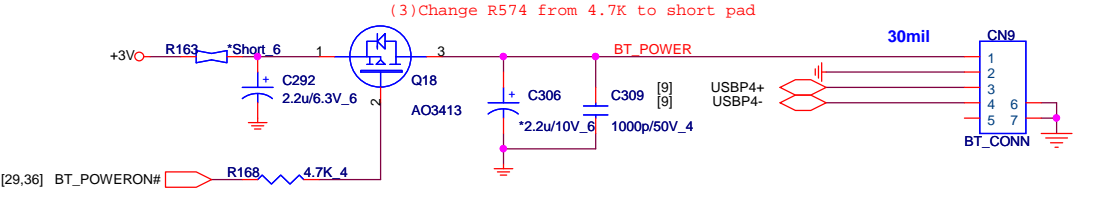
TOUCHPAD



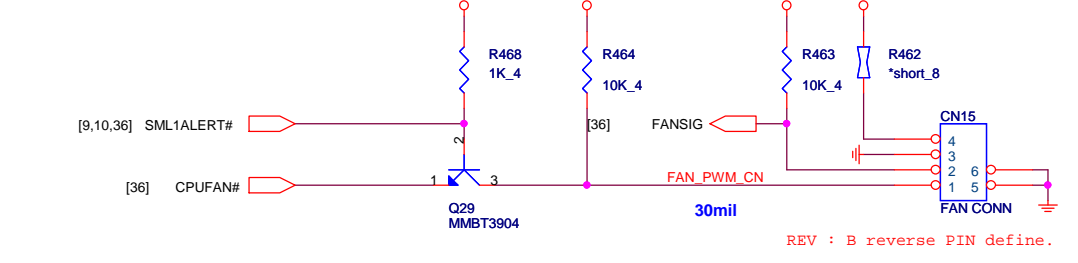
Finger-Printer



BLUETOOTH

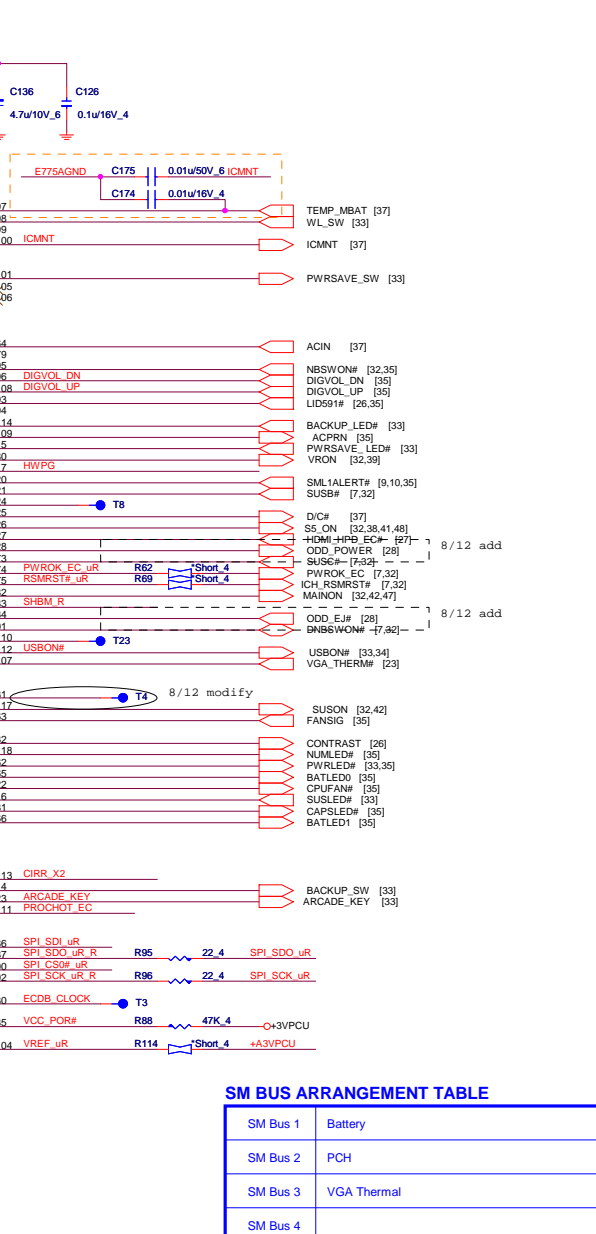
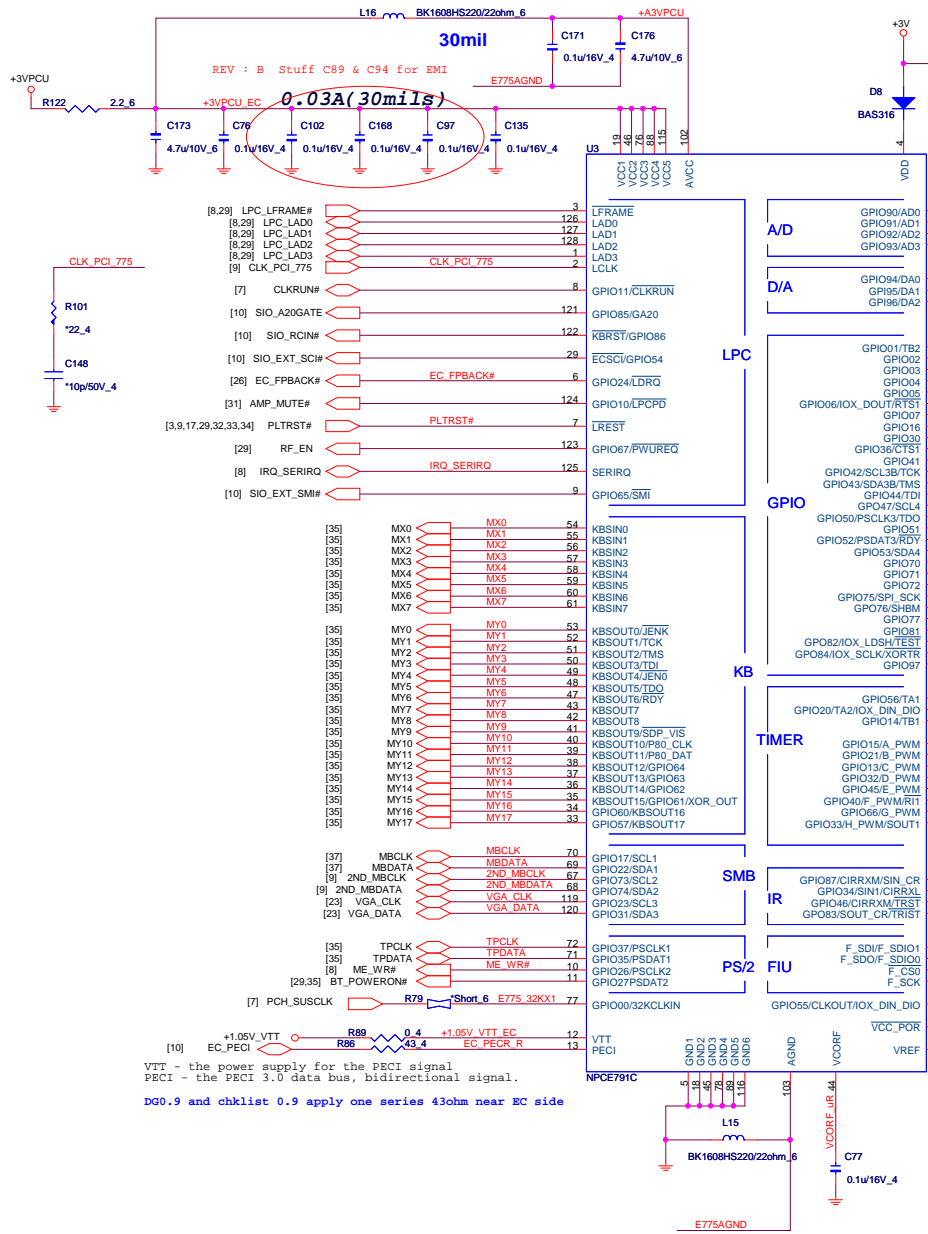


CPU FAN



Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	KB/FAN/TP+FP/BT	1A
Date:	Monday, November 08, 2010	Sheet 35 of 50



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

I/O ADDRESS SETTING

I/O Address	
BADDR1-0	Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

SHBM — SHBM_R — R84 — *10K_4

1/13 Confirm by vendor mail :
Disabled (*) if using FWH device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware

SM BUS PU

Change pull-up resistor (R148, R154) from 10K to 4.7Kohm

REV : B Change from +3V to +3V_S5

INTERNAL KEYBOARD STRIP SET

SPI FLASH

1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add
Winbond W25X16AVSSIG
AKE382PN01
EGON EN25F16-100HIP
AKE382A0000
AMIC A25L016
AKE382N0800

HWPG

7/29 modify

VR Cap.

Place two near EC

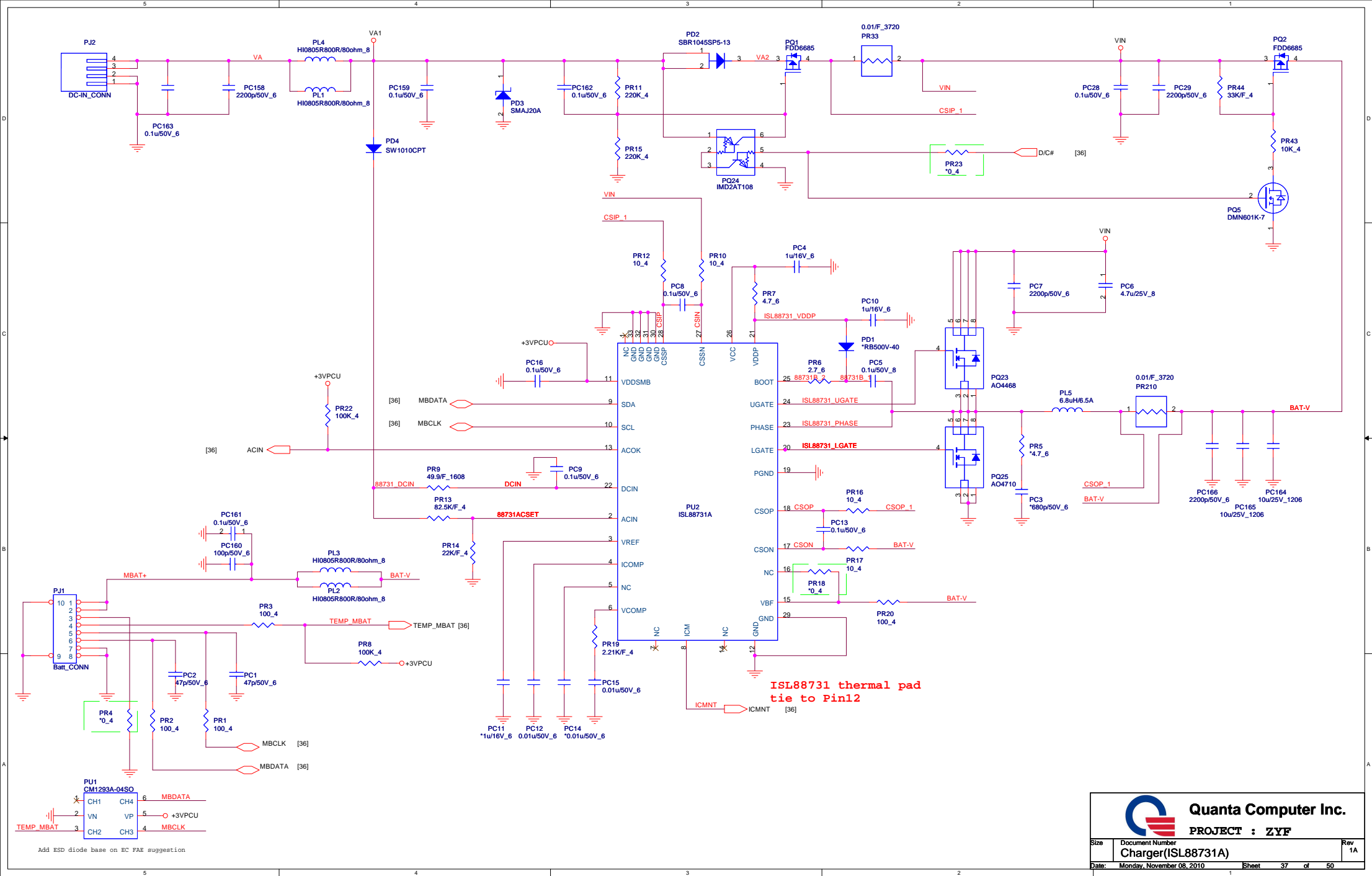
POWER-ON Switch


Rev: B not stuff SW1

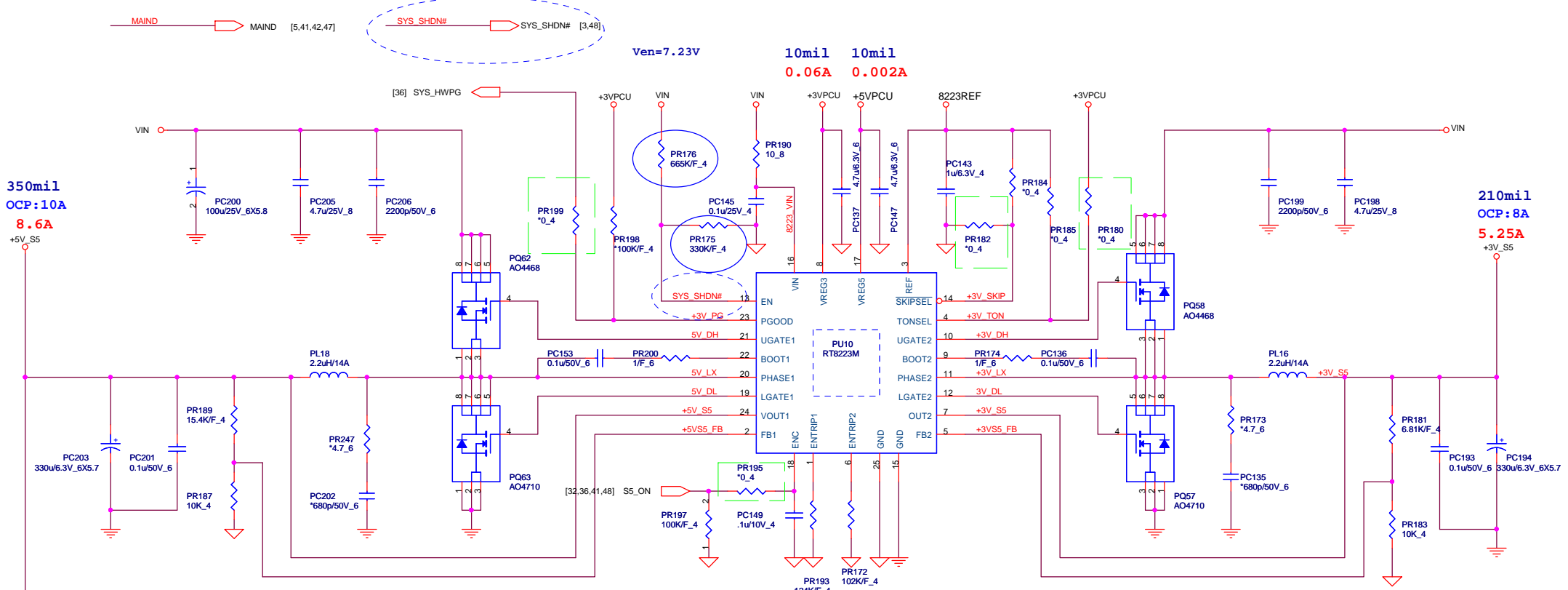
*TME-532-S-V-TR

CIRR

IRM-V538-TR1



 Quanta Computer Inc. PROJECT : ZYF		Rev
		1A
Size	Document Number	Sheet 37 of 50
	Charger(ISL88731A)	
Date:	Monday, November 08, 2010	

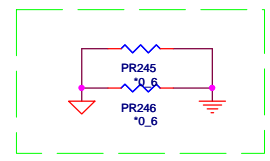
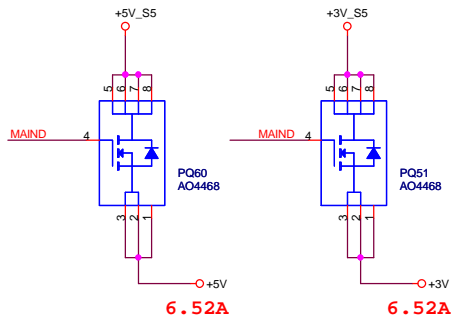


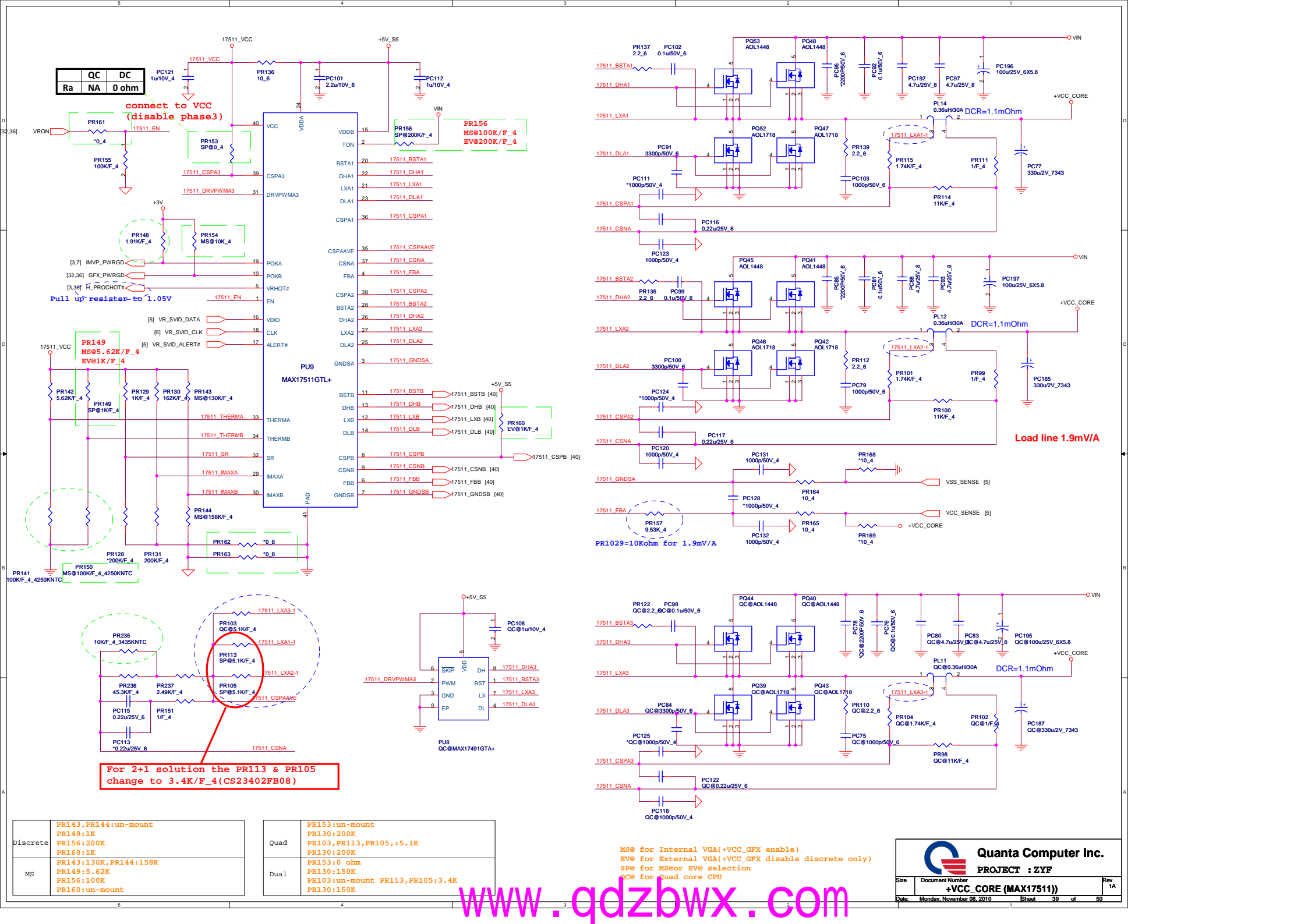
350mil
OCP: 10A
8.6A

210mil
OCP: 8A
5.25A

OCP:10A
 $L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \mu \cdot 0.4 \text{M} \cdot 9) = 2.525 \text{A}$
 $I_{\text{ocp}} = 10 - (2.525/2) = 8.74 \text{A}$
 $V_{\text{th}} = 8.74 \text{A} \cdot 14.2 \text{mOhm} = 124.07 \text{mV}$
 $R(\text{Ilim}) = (124.07 \text{mV} \cdot 10) / 10 \mu \text{A} \sim 124.07 \text{K}$

OCP:8A
 $L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.5 \text{M} \cdot 9) \sim 1.9 \text{A}$
 $I_{\text{ocp}} = 8 - (1.9/2) = 7.05 \text{A}$
 $V_{\text{th}} = 7.05 \text{A} \cdot 14.2 \text{mOhm} = 100.11 \text{mV}$
 $R(\text{Ilim}) = (100.11 \text{mV} \cdot 10) / 10 \mu \text{A} = 100.11 \text{K}$





QC	DC
Ra	0 ohm

connect to VCC (disable phase3)

Pull up resistor to 1.05V


Load line 1.9mV/A

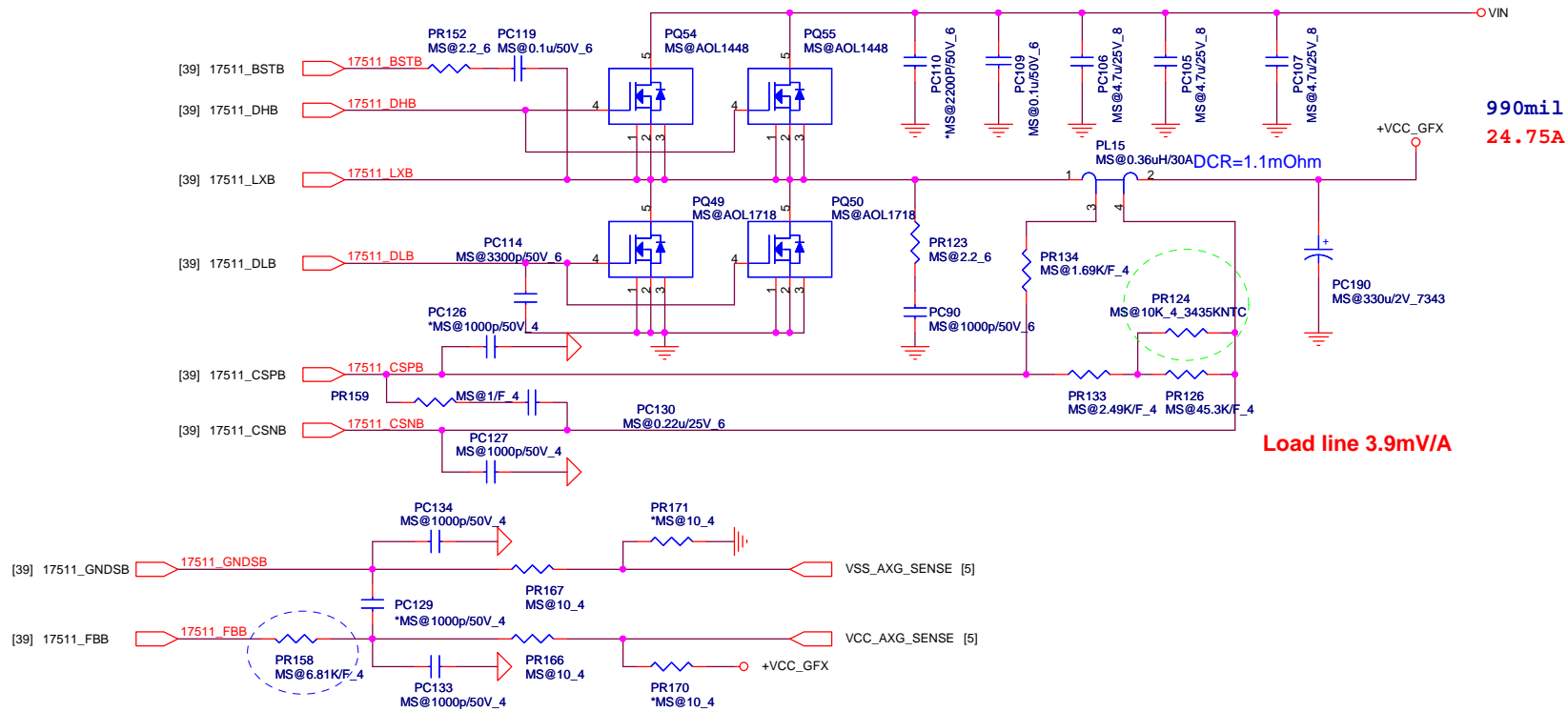
For 2+1 solution the PR113 & PR105 change to 3.4K/F_4(CS23402FB08)


Discrete	PR143, PR144: un-mount PR149: 1K PR156: 200K PR160: 1K
MS	PR143: 130K, PR144: 158K PR149: 5.62K PR156: 100K PR160: un-mount

Quad	PR153: un-mount PR130: 200K PR103, PR113, PR105: .5.1K PR130: 200K
Dual	PR153: 0 ohm PR130: 150K PR103: un-mount PR113, PR105: 3.4K PR130: 150K

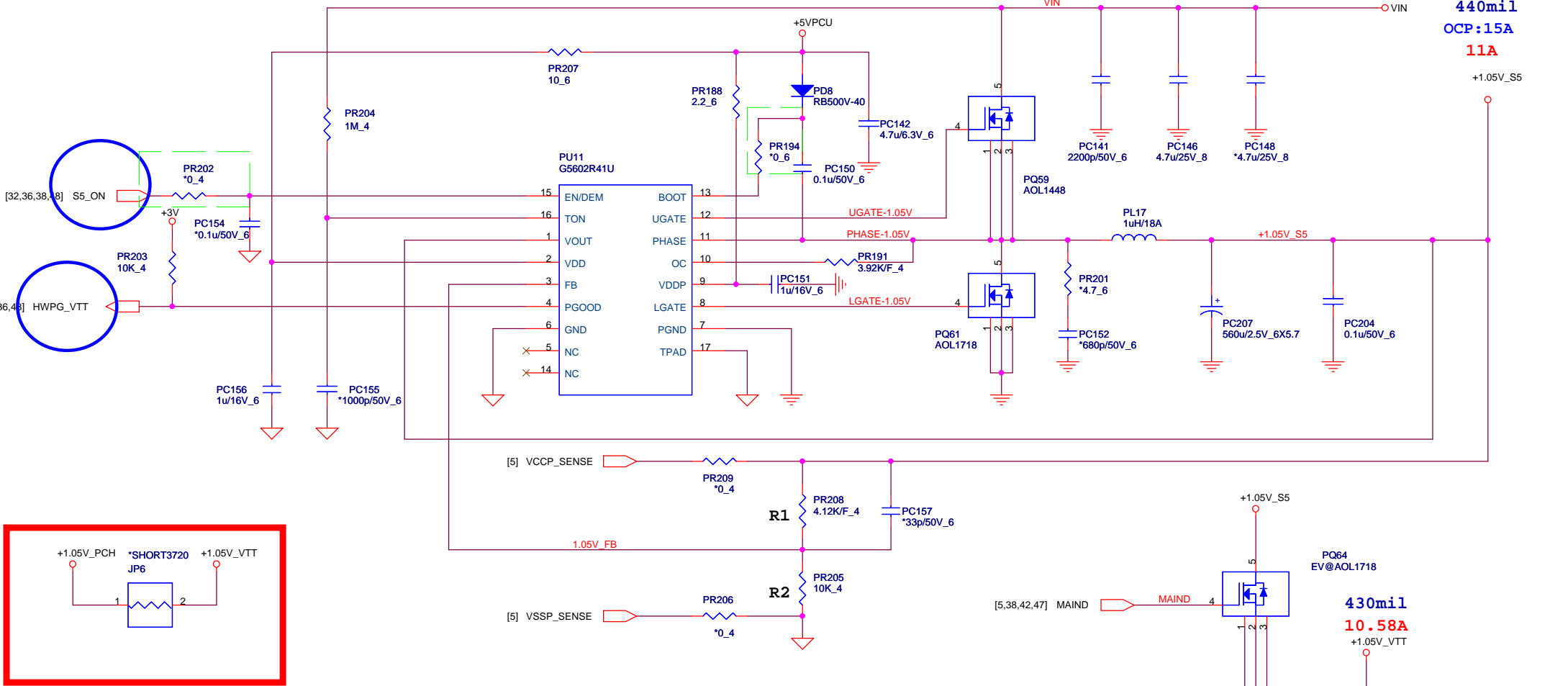
MS@ for Internal VGA(+VCC_GFX enable)
EV@ for External VGA(+VCC_GFX disable discrete only)
SP@ for MS@or EV@ selection
QC@ for Quad core CPU


Quanta Computer Inc.
 PROJECT : ZYF
 +VCC_CORE (MAX17511)
 Date: Monday, November 08, 2010 Sheet 39 of 50

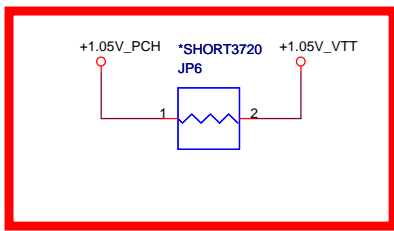


 Quanta Computer Inc. PROJECT : ZYF		Rev
		1A
Size	Document Number	
+VCC_GFX (MAX17511))		
Date:	Monday, November 08, 2010	Sheet 40 of 50

[PWM]

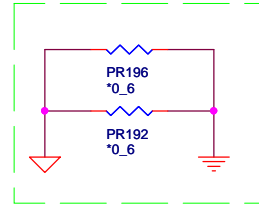



440mil
OCP:15A
11A
+1.05V_S5



$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin \cdot TON)$
 $TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

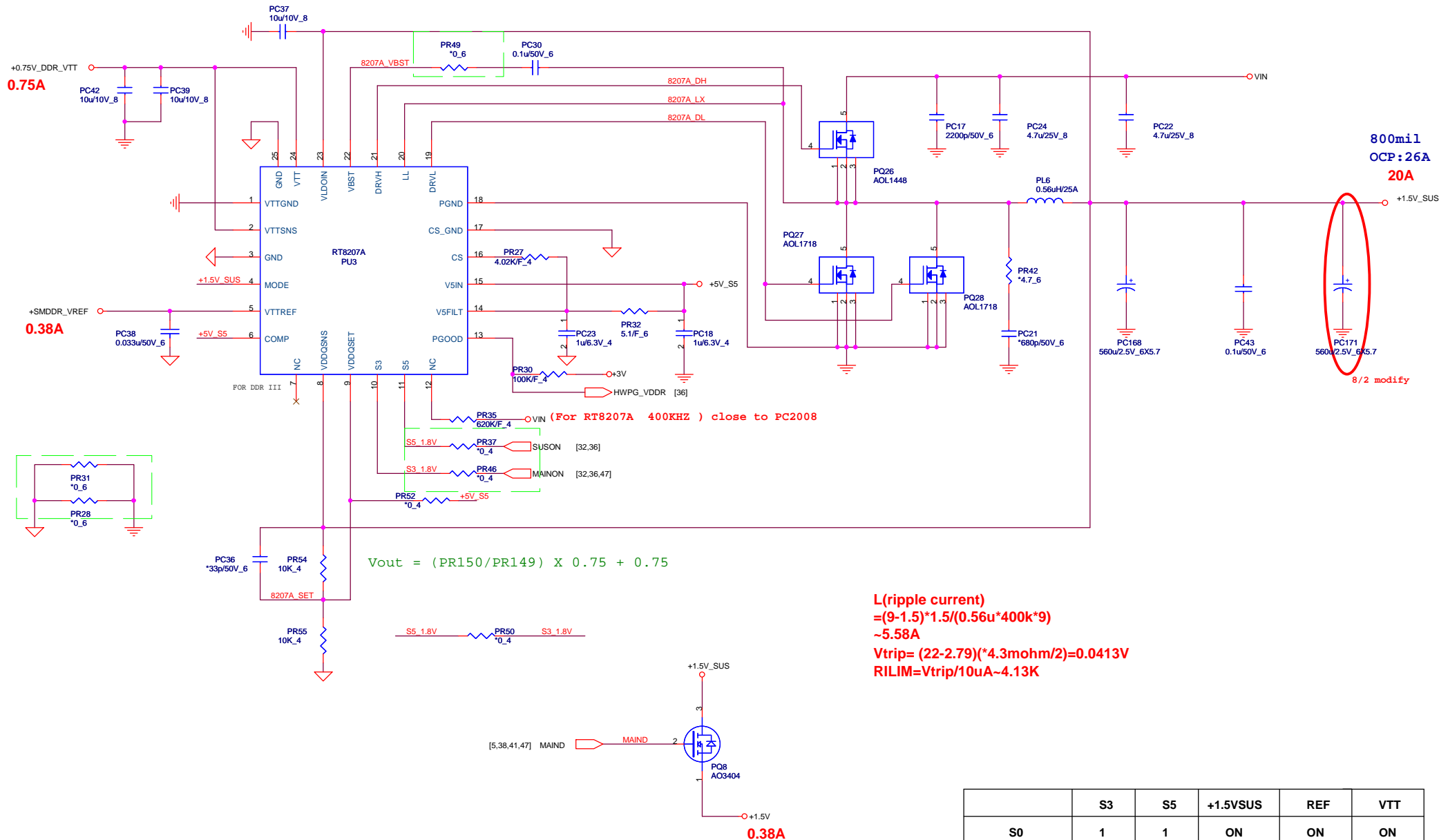
L(ripple current)
 $= (19 - 1.05) \cdot 1.05 / (1u \cdot 272k \cdot 19)$
 $\sim 3.64A$
 $4.3m \cdot 18 = RILIM \cdot 20uA$
 $RILIM = 3.87K \text{ --- } 3.92K$




Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date:	Monday, November 08, 2010	Sheet 41 of 50


[PWM]



$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

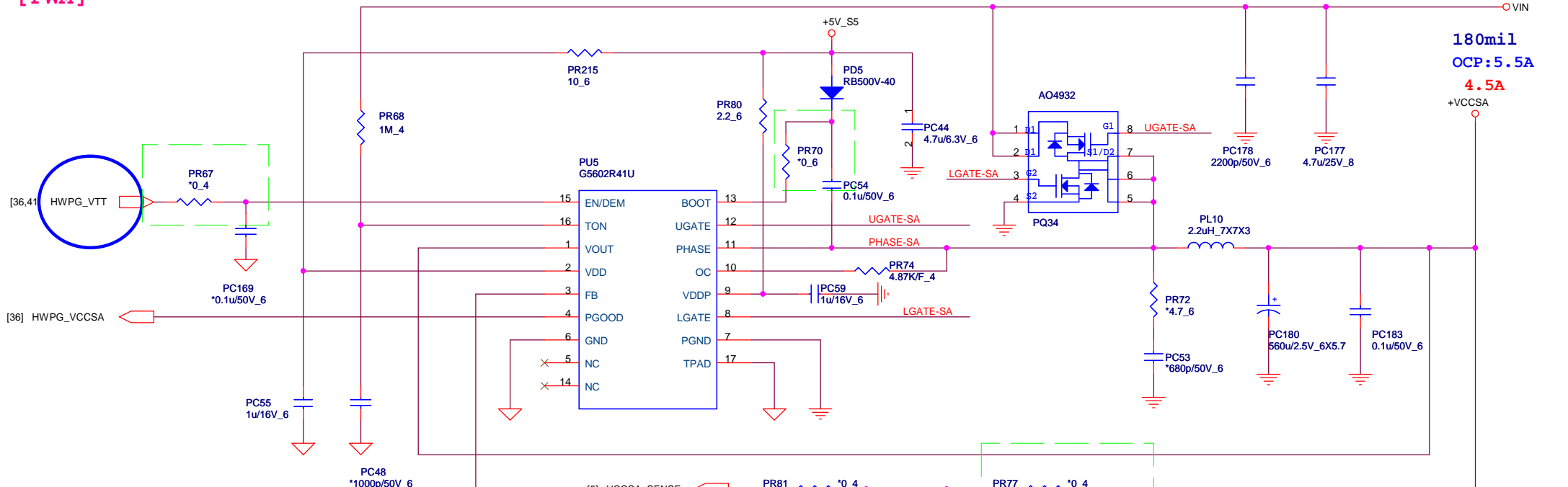
L(ripple current)
 $= (9-1.5) \times 1.5 / (0.56 \mu \times 400 \times 9)$
 $\sim 5.58A$
 $V_{trip} = (22-2.79) \times (4.3 \text{mohm}/2) = 0.0413V$
 $RILIM = V_{trip}/10 \mu A \sim 4.13K$

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF


Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date:	Monday, November 08, 2010	Sheet 42 of 50

[PWM]

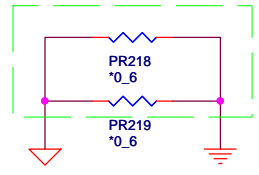


180mil
OCP: 5.5A
4.5A
+VCCSA

$TON = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$
 $Frequency = V_{out} / (V_{in} * TON)$
 $TON = 3.85p * 1M * 1 / (V_{in} - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AO4932 $R_{dson} = 15.8 \sim 19.6m\Omega$
L(ripple current)
 $= (19 - 0.8) * 0.8 / (2.2u * 272k * 19) = 1.281A$
 $R_{ILIM} = 19.6m\Omega * (5.5 - 0.64) / 20uA = 4.762K$
 $I_{peak} = 6.781A$

$V_{OUT} = (1 + R1 / R2) * 0.75$

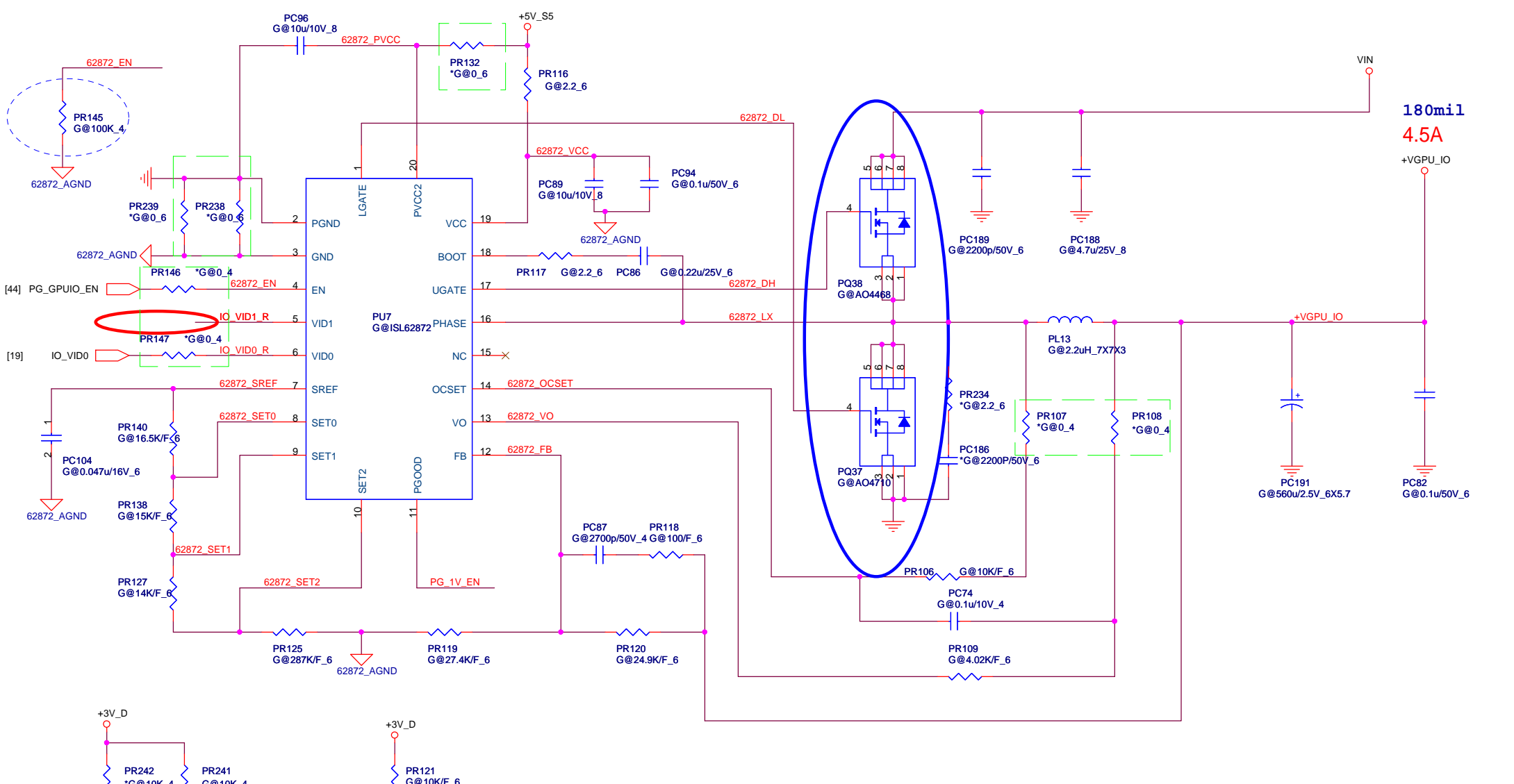


VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V


Quanta Computer Inc.
PROJECT : ZYF

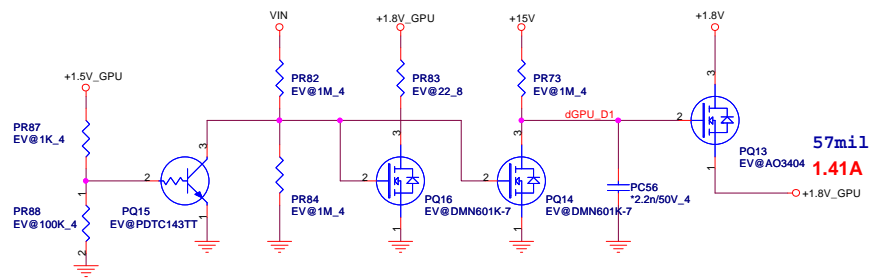
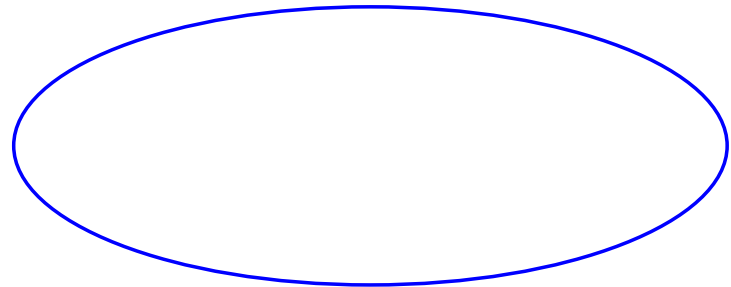
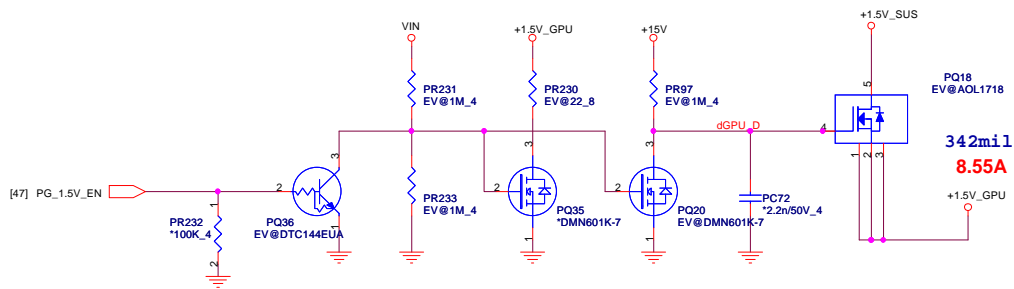
Size	Document Number +1.05V(UP6111AQDD)	Rev 1A
Date:	Monday, November 08, 2010	Sheet 43 of 50

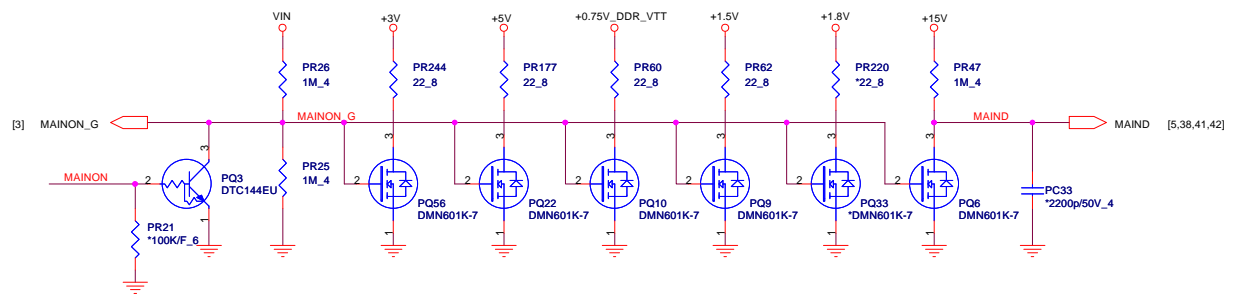
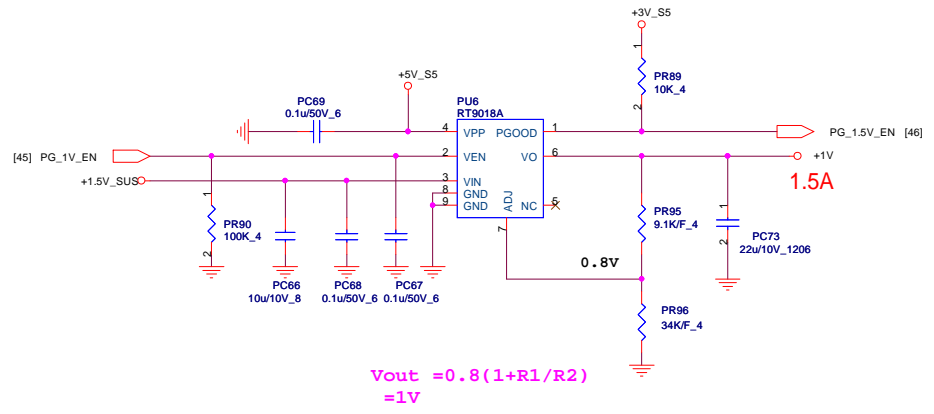
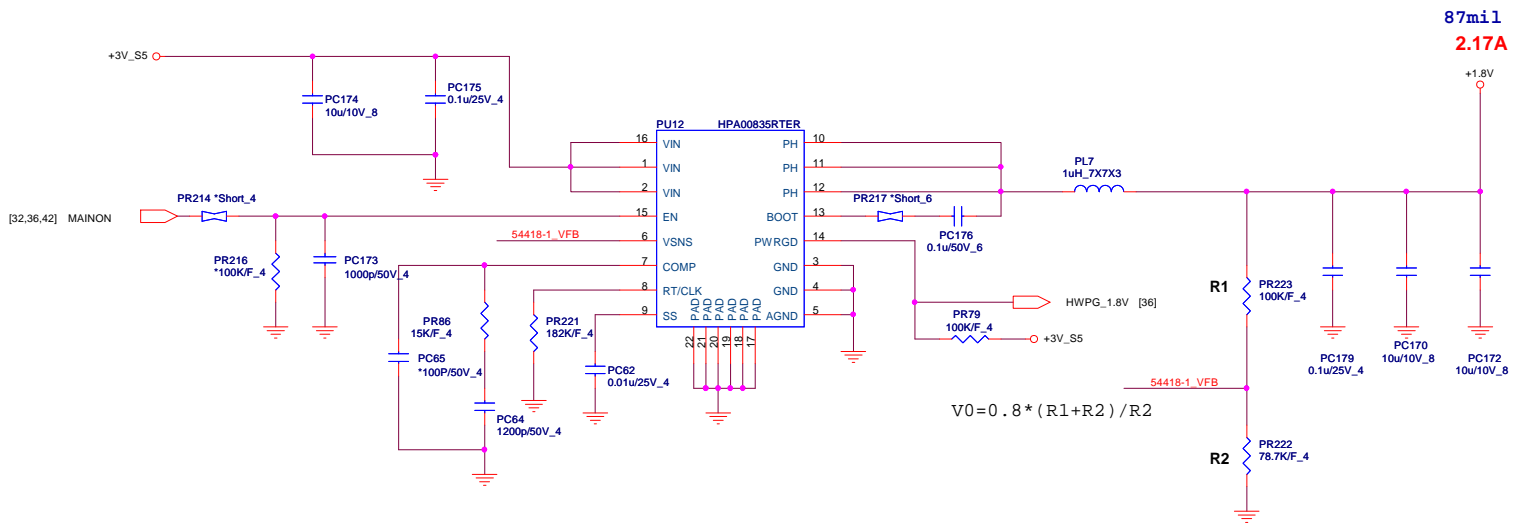


180mil
4.5A

IO_VID0	IO_VID1	+GPU_IO
0	0	1.101V
1	0	1.05V
0	1	1.0V
1	1	0.95V


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PROJECT : ZYF
 Size: Document Number
+VGPU_IO(ISL62872)
 Date: Monday, November 08, 2010 Sheet 45 of 50 Rev 1A





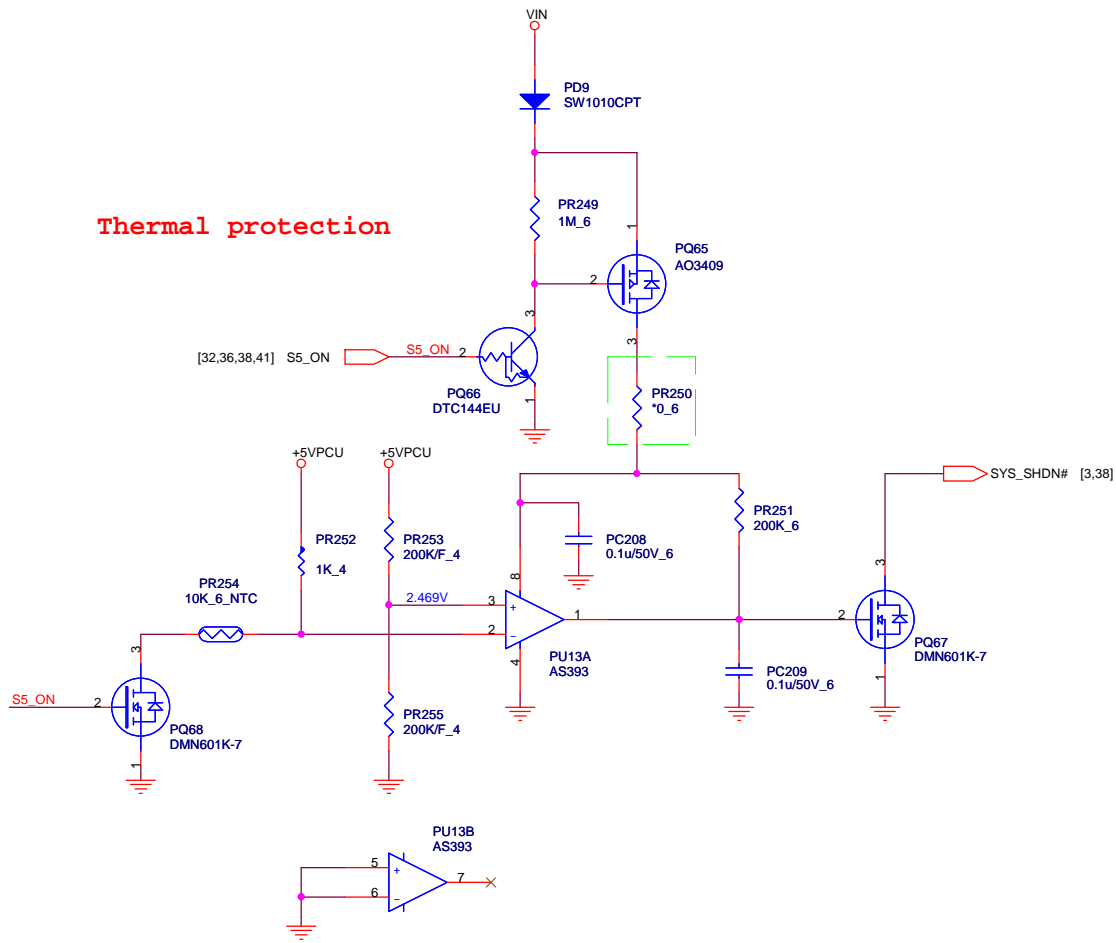
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
		1A


+1V/+1.8V/Discharge

Date: Monday, November 08, 2010 Sheet 47 of 50

Thermal protection



For EC control thermal protection (output 3.3V)

 Quanta Computer Inc. PROJECT : ZYF		Rev 1A
Thermal protect		
Date:	Monday, November 08, 2010	Sheet 48 of 50

Model	REV	CHANGE LIST
ZYF MB	A	2010/07/27 page 40:del Mark Lo change CPU solution page 26:Delete HDMI Switch circuit & add R584,R585 for Muxless DATA,CLK pin page 33:add CN27 for power sequence
		2010/07/28 page 14:del R18,R30,R32,R33,R39,R40,R45 page 16:del R47,R51,R60,76,R169,R180,R190,R213 Mark Lo change power circuit
		2010/07/29 page 9:change CN20 parts page 29:change CN22 & CN23 parts page 37:add T21,T23
		2010/07/30 page 28:add HDMI LEVEL SHIFTER circuit & del R584,R585 page 9:add R8421 page 8:add C1160,C1161 page 19:add T28
		2010/08/02 page 33:add L63,L64,L65 & R620,R621,R622,R623,R624,R625 for EMI
		2010/08/03 page 13:add R29,R30,C79 page 15:add R169,R179,C302 page 17:add hole 1-316 PADI
		2010/08/04 page 5:del C8348,C8479 page 8:del C8363 page 9:add R8587 page 10:add R8496,R8480 page 13:del R31,TP8231 page 14:del R34,TP8232 page 15:del R217,TP8233 page 16:del R218,TP8234 page 19:del R93,R103 & add T30,T31,T32,T29 & del SOUT_GPIO8 ,SIN_GPIO9,SCLK_GPIO10,IO_VIDI net page 23:del U1,R58,R57,C80 page 26:del RN12,RN11,RN5,RN7 & add R535,R552,R557,R575,R576,R549,R577,R580 page 27:del R552,R556,R557,R576,R577,R580,R581,R583 page 32:add D16 & CR_WAKER# net page 34:add R1331
		2010/08/06 page 8:del R64,R65 page 32:add R245,R1332,Q20,R1334,R1333 & OCII1B# net & del C1268,R1317,R1318 page 34:CN31 change footprint
		2010/08/11 page 3: CLK_DPLL_SSCLKN_R net from GND change PU to +1.05V_VTT page 5:C8474 change to 3528 type page 11: del R8498
		2010/08/12 page 8: add FCH_ODD_EN net page 10: add ODD_PSENT# net ,R8498 & CR_CPPE# net page 28: add ODD Power circuit page 36: add ODD_EJ# & ODD_POWER net
	2010/08/13 page 4: SWAP DDR control pin page 10: add SMIB net for USB3.0	
	2010/08/17 page 5: add P026 & change C682 to 3528 type,R8291,R8282 to 1206 type	
	2010/08/18 Power engineer update power circuit page 32 :C895,C897& C896 change to 0603 type	
	2010/08/19 page 34 :C1265 chnage to 6x5.7 type	
	C	2010/09/6 page 28 :CN22,CN26 change footprint page 32 :add R721
		2010/09/13 page 9 :add C912 page 9 :add R722,R723 for SMBus
		2010/09/14 page 3 :R567,R564 change short pad page 7 :R308,R306,R344 change short pad page 8 :R719 change short pad page 9 :Del R305 page 11 :R351,R310,R352,R66,R388,R620,R608,R659,R619,R274,R411,R410,R333,R669,R658,R349,R346,R337,R269,R272,R273, change short pad page 13 :R11 change short pad page 14 :R21 change short pad page 15 :R179 change short pad page 16 :R180 change short pad page 19 :add R724,R726,R725 page 26 :R153,R145 change short pad page 27 :R177 change short pad page 28 :R246,R716 change short pad page 29 :R1,R2 change short pad page 30 :R439,R364,R353,R332 change short pad page 31 :R703,R705,R422,R416,R440, change short pad page 32 :R709 change short pad page 33 :R580 change short pad page 34 :R258,R270,R605 change short pad page 35 :R158,R156,R462 change short pad
		2010/09/16 page 17 :Del CN21,R578,C807
		2010/10/22 page 30 :U28 pin1 chnge net name to ALL_AMP_MUTES# for "bo" noise & change footprint page 31 :add R727,R578 & ALL_AMP_MUTES# net for "bo" noise page 33 :add C807,C915
		3C