COMPAL CONFIDENTIAL

MODEL NAME : *HAL31(Discrete) & HAL30(UMA)*

PCB NO : *LA-3001P*

COMPAL P/N : *45140031L11 (For Discrete)*
45140031L01 (For UMA)

Bali (DIS&UMA) Schematics Document

uFCPGA Mobile Yonah
Intel Calistoga + ICH7M

2006-04-14

REV : 0.5 (DELL: X03)

@ : Nopop Component
1@ : UMA Used Only
2@ : Bali with descrete Used Only

MB PCB

Part Number	Description
DA800004W0L	PCB LA-3001P REV0.4 MB

BOM NO: *45140031L11 (For Discrete)*
45140031L01 (For UMA)

PCB P/N: *DA800004W0L*

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Title: Cover Sheet

Size: | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 1 of 73

Compal confidential
Model : Bali

Block Diagram

FAN
+FAN1_VOUT
page 16

Thermal
GUARDIAN II
EMC4000
+3V_SUS page 16

Pentium-M
Yonah-2M (Merom Support)
uFCPGA CPU
+VCCP (1.05V)
+VCC_CORE
478pin page 7,8,9

CPU ITP Port
+VCCP page 7

Clock Generator
CK410M+
+3V_RUN page6

8X32M GDDR3 x2

VGA CONN
+5VRUN page 20

LVDS CONN
+INV_PWR_SRC
+LCDVDD page 19

TV CONN
+5VRUN page 20

SPDIF

G72M
+1.22V_GFX_PCIE
+VCC_GFX_CORE
page 44,45,46,47,48,49,50

PCI-E 16X

H_A#(3..31)

System Bus
FSB 533/667 MHz

H_D#(0..63)

Memory BUS
(DDR2)
+1.8V_SUS 400/533 / 667MHz

DDRII-DIMM X2
BANK 0, 1, 2, 3, 4 ,5 ,6 ,7 ,8
page 17,18
+0.9V_DDR_VTT
+1.8V_SUS

For Integrity UMA Graphic

INTEL
Calistoga
1466pin BGA
+1.5V_RUN
+1.8V_SUS
+VCCP (1.05V)
+3V_RUN
+2.5V_RUN
page 10,11,12,13,14,15

PCI BUS
+3V_RUN 33MHz

IDSEL:AD17
(PIRQC,D#,GNT#1,REQ#1)

IDSEL:AD16
(PIRQC#,GNT#4,REQ#4)

R5C832
+3V_SUS page 28

BCM4401KQL
+3V_LAN page 26

5 in 1 Card Reader
page 28

1394 CONN
page 29

RJ45
page 27

PCI Express BUS
+3V_RUN/ +1.5V_RUN 100MHz

DMI
+1.5V_RUN
100MHz

On LCD Panel

Camera
+5V_RUN

Mini Card 2
WLAN
+3V_RUN
+1.5V_RUN page 29

Mini Card 1
WWAN
+3V_RUN
+1.5V_RUN page 29

USB[4]

USB[5]

48MHz

48MHz

INTEL
ICH7-M
652pin BGA
+3V_RUN
+3V_SUS
+1.5V_RUN
+VCCP
page 21,22,23,24

PCI Express BUS
+3V_RUN/ +1.5V_RUN 100MHz

Azalia I/F

S-ATA 0/2 ATA100

ATA100

ExpressCard CONN
+3V_RUN
+3V_SUS
+1.5V_RUN
IO/B

USB[3]

AMP & INT. Speaker
+5V_SUS IO/B

Azalia Codec
STAC9220
+3V_RUN
+VDDA IO/B

HeadPhone & MIC Jack
+3V_RUN IO/B

Left USB[6] USB[7]

Right USB[0] USB[1]

USB[2]

USB Ports X2
+5V_SUS page 25

USB Ports X2
+5V_SUS page 25

Bluetooth
+3V_RUN page 25

SPI

LPC BUS
+3V_RUN
33MHz

SMSC SIO
ECE5011
+3.3V_ALW
page 31

BC BUS

SMSC KBC
MEC5004
+RTC_CELL
+3.3V_ALW page 30

SPI

Touch Pad
page 34

Int.KBD
page 34

CD-ROM
+5V_MOD IO/B

S-HDD
+5V_HDD IO/B

MDC
+3V_SUS IO/B

On I/O daughter Card

ST M25P80
+3V_SUS
page 30

RJ11
page 27

1.8V/0.9V
page 41

+VDD_CORE
page 50

DC IN
page 37

Power Sequence
page 33

VCORE (IMVP-6)
page 42

1.5V/1.05V
page 40

BATT IN
page 38

Power On/Off SW & LED
page 35

CHARGER
page 43

3V/5V/15V
page 39

DC/DC Interface
page 37

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Title: Block Diagram

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PM TABLE

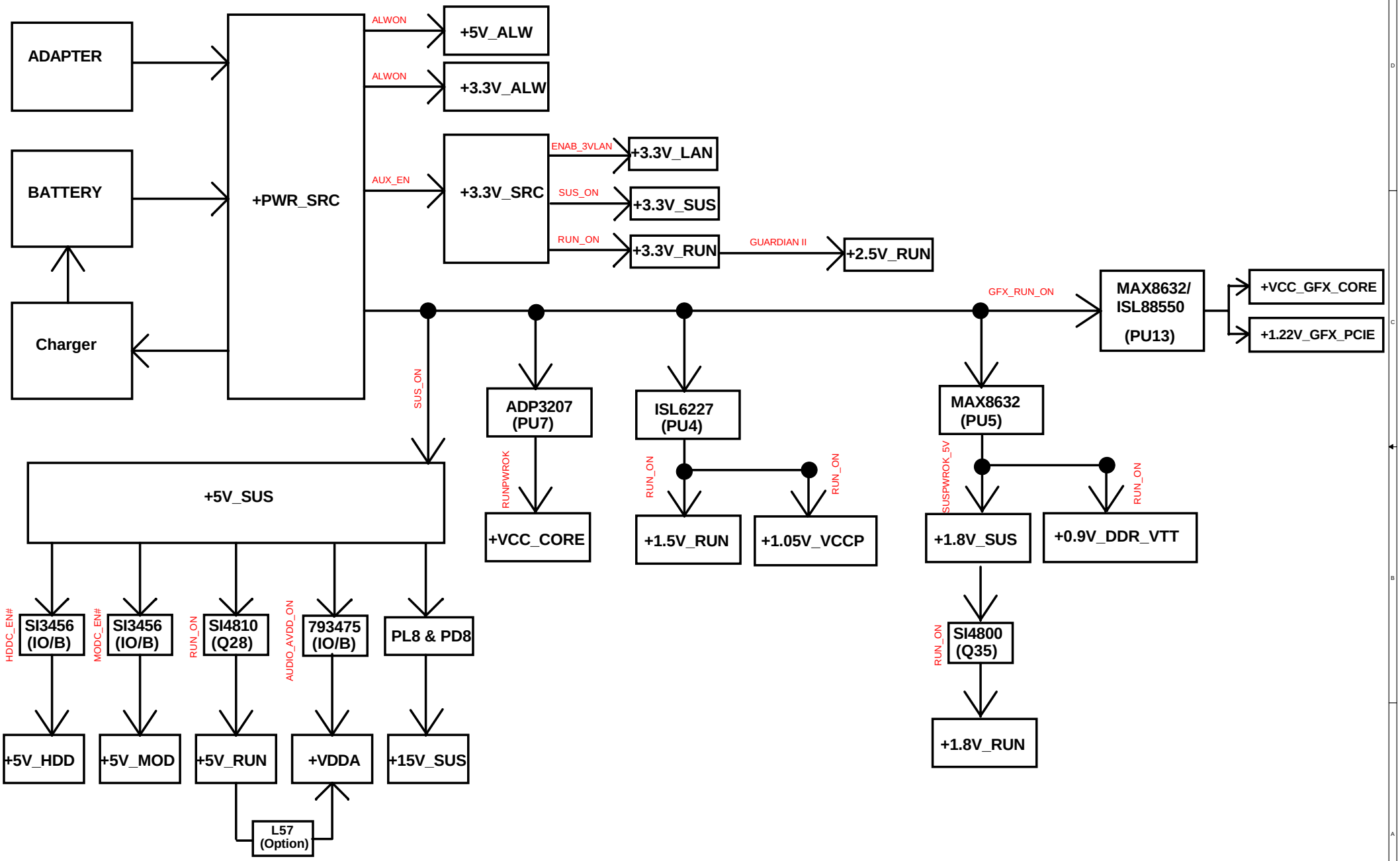
power plane / State	+5V_ALW +3.3V_ALW	+15V_SUS +5V_SUS +3.3V_SRC +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.5V_RUN +1.22V_GFX_PCIE +0.9V_DDR_VTT +VCC_GFX_CORE +VCC_CORE +1.05V_VCCP
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
LAN	AD16	REQ#3/GNT#3	IRQB
R5C832	AD17	REQ#2/GNT#2	IRQC IRQD

	USB PORT#	DESTINATION
ICH7-M	0	JUSB1 (Ext Back Right Side)
	1	JUSB1 (Ext Back Right Side)
	2	Blue Tooth
	3	EXPRESS CARD
	4	CCD Camera
	5	WWAN
	6	JUSB2 (Ext Back Left Side)
	7	JUSB2 (Ext Back Left Side)
SIO ECE5011	0	None
	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	None
Lane 4	EXPRESS CARD



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Title: Power Rail

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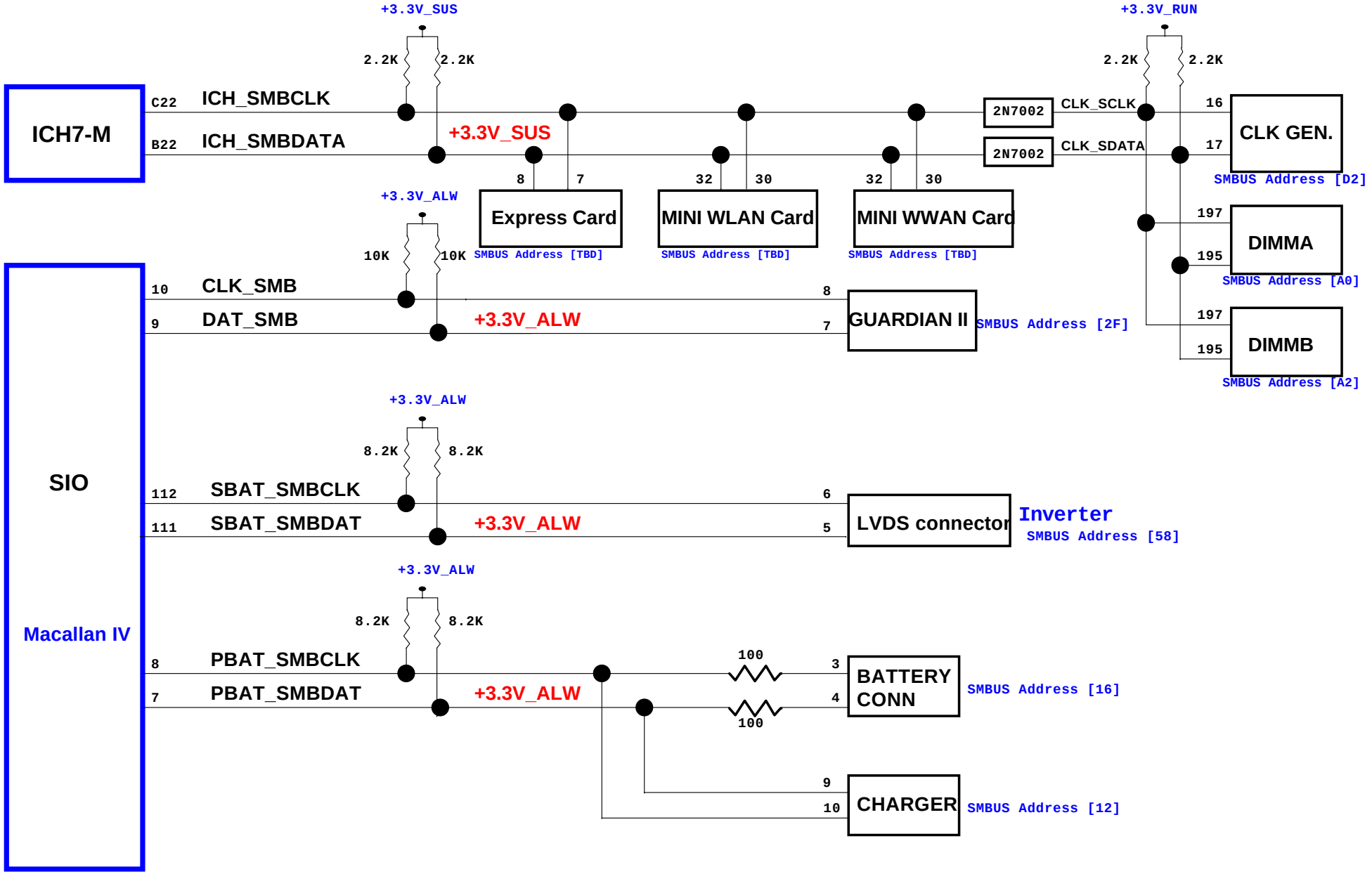
Date: Monday, April 17, 2006 | Sheet 4 of 73



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Title: SMBUS TOPOLOGY

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Date: Monday, April 17, 2006 | Sheet 5 of 73

Change to ECJCV50J106M 6.3V10UF 0805 X5R M H:0.85mm, wait CIS symbol.

2N7002

place Decoupling as closed physically possible to each VDD oins

Place near each pin W>40 mil

Place near CK410+

Placec these caps closed to CK410M

Place crystal within 500 mils of CK410M

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	Reserve		

Table : ICS954305AK

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1

Pop Ra,Rb,Rc, Rd for 27MHz output for G72 spectrum input
Routing trace length DOT96/DOT96# <50mil

Pop R451 for 27MHz output for G72

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
UMA	0	DOT96T	DOT96C	96/100M_T	96/100M_C
Discrete	1	27M_out	27M SSout	SRCT0	SRCC0

Swap signals for smooth routing

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Title: Clock Generator

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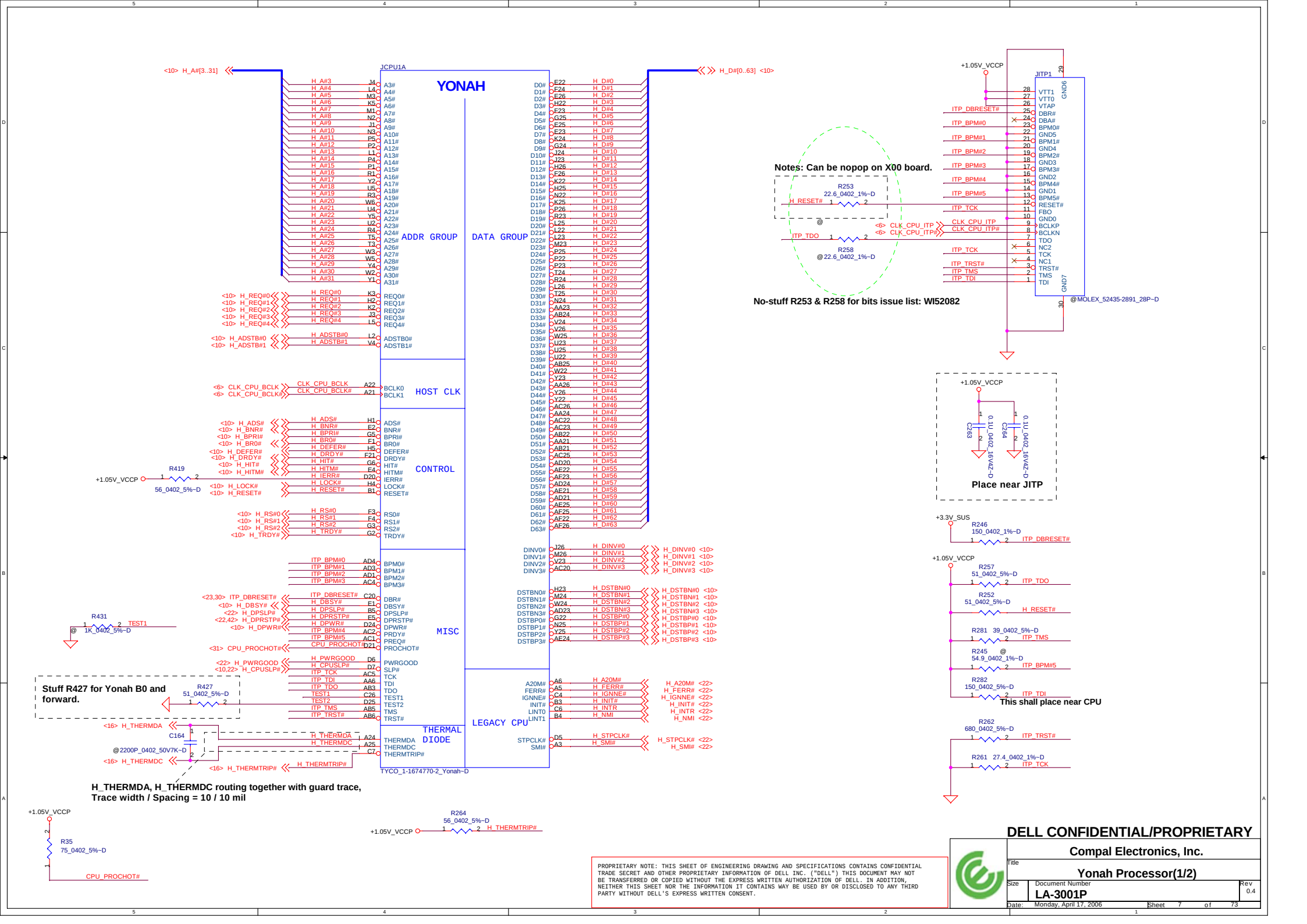
Date: Monday, April 17, 2006 | Sheet 6 of 73



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Title: Yonah Processor(1/2)

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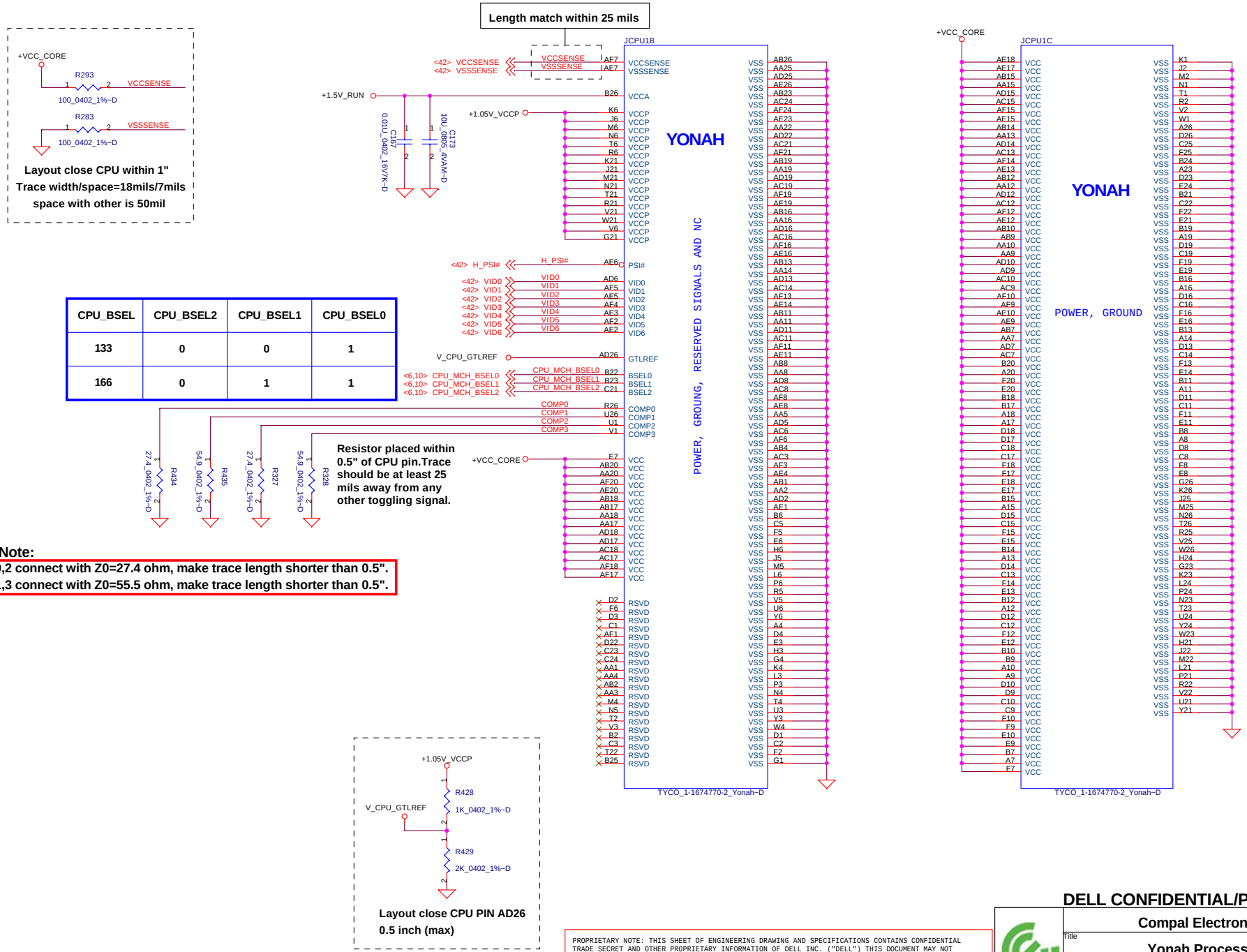

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Layout Note:

COMP0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
COMP1,3 connect with Z0=55.5 ohm, make trace length shorter than 0.5".

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Compal Electronics, Inc.

Title: Yonah Processor(2/2)

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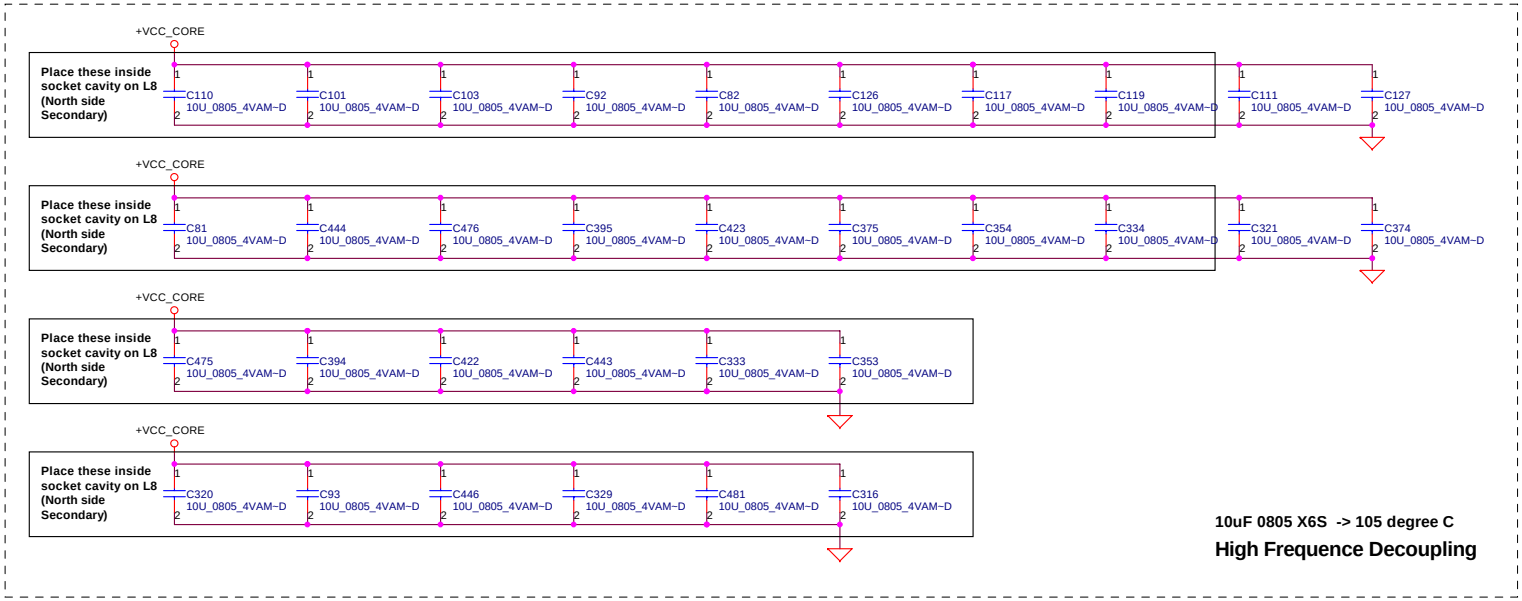
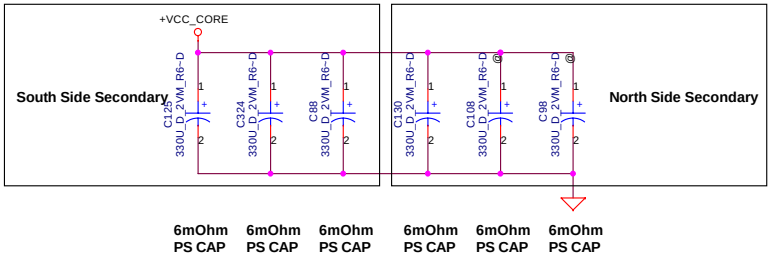
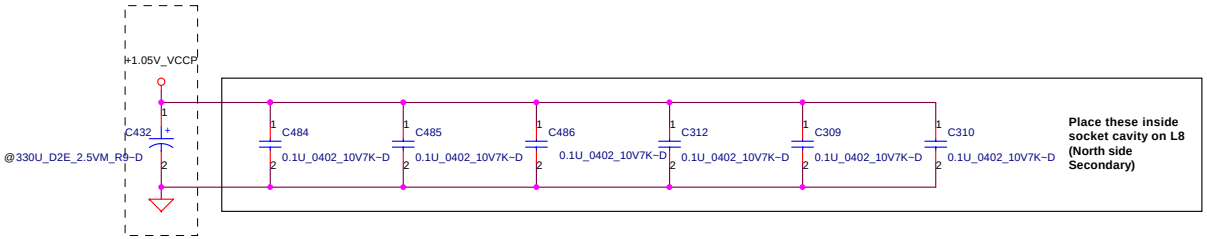
Intel CRB schematic suggest to use X5R or better



Near VCORE regulator



ESR <= 1.5m ohm
Capacitor > 1980uF



Compal Electronics, Inc.

Title: CPU Bypass

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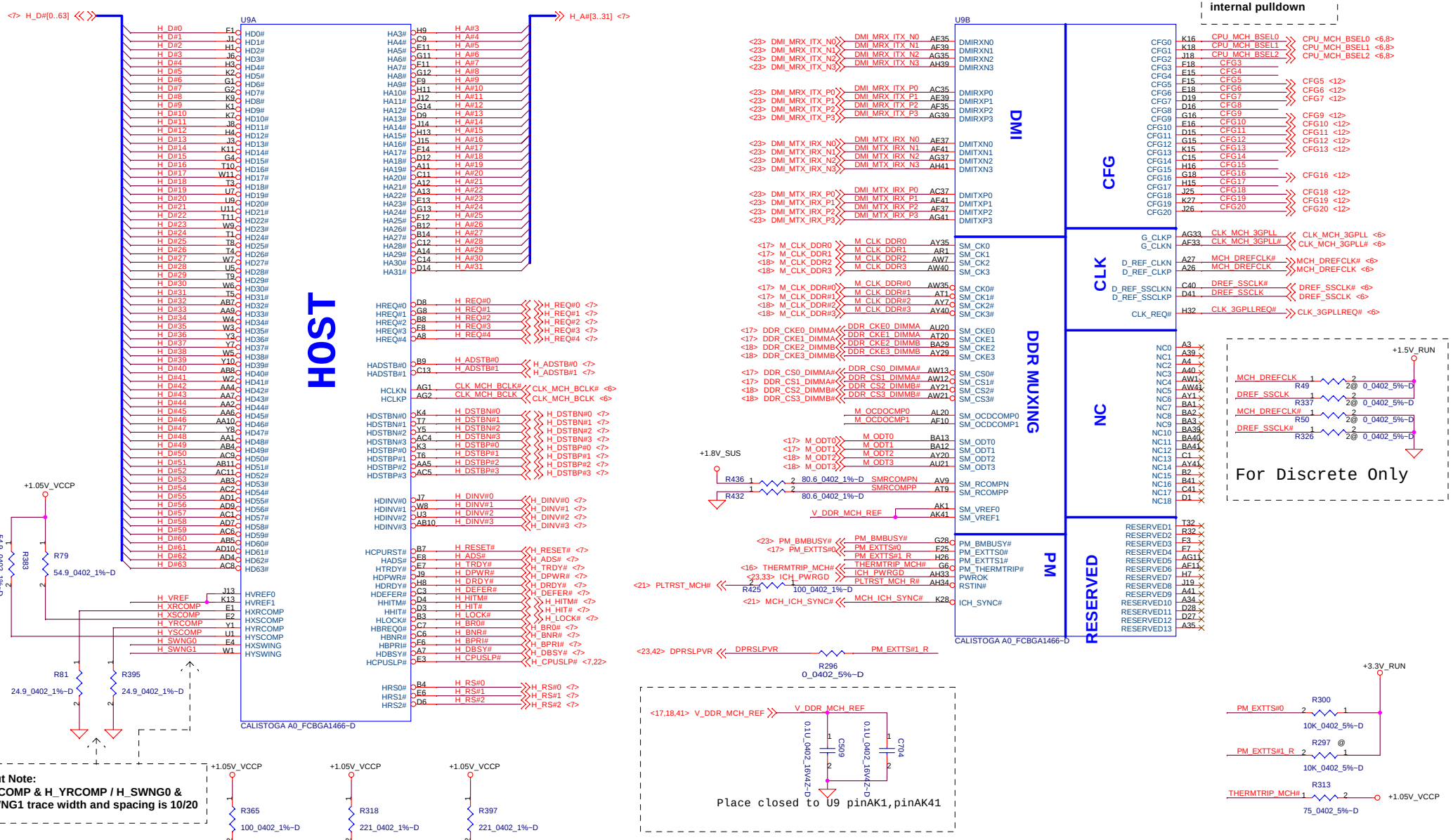
UMA use 945GM A2 (P/N: SA00000592L)
Discrete use 945PM A2 (P/N: SA00000KD1L)

Description at page12

Note :
CFG3:17 has internal pullup, CFG18:19 has internal pulldown

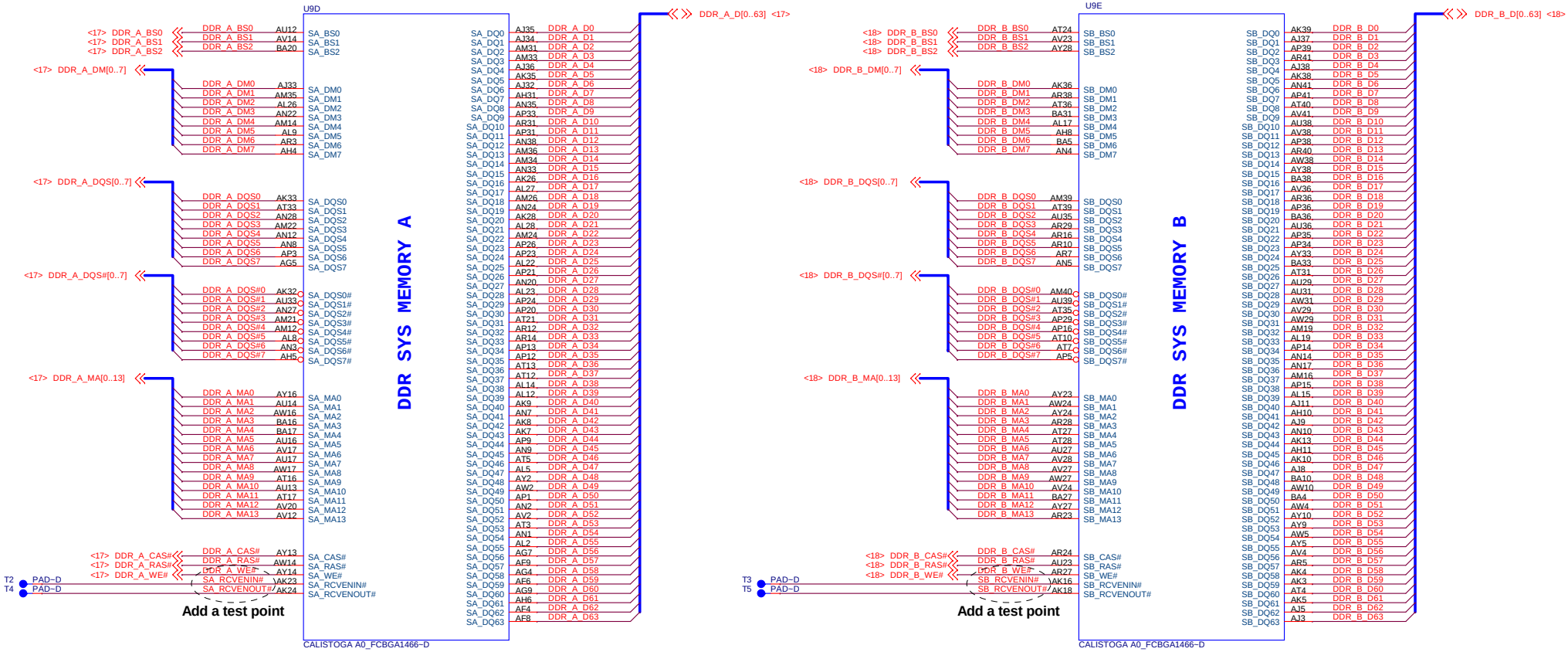


Compal Electronics, Inc.

Title: Calistoga(1 of 6)

Size: | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 10 of 73



Compal Electronics, Inc.

Title: Calistogo(2 of 6)

Size | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 11 of 73

Strap Pin Table

CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = Moby Dick High = Calistoga *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG10	Low = Reserved High = Mobility *
CFG11	Low = Calistoga * High = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (DMI Lane Reversal)	Low = Normal Operation (Default): * Lane number in Order High = Reverse Lane
SDVO_CTRLDATA	Low = No SDVO Device Present (Default) * High = SDVO Device Present
CFG20 (PCIE/SDVO select)	Low = Only PCIE or SDVO is operational. (Default) * High = PCIE/SDVO are operating simu.

CFG[3:17] have internal pullup

CFG[18:19] have internal pulldown

Resistors Stuff Table

UMA	R290,R305,R307,R308,R360 ,R366,R301,R302,R303,R294 ,R295,R292,R306,R304,R38 ,R39,298,R299,
Discrete	R271,R272,R273,R270,R53, R358,R345,R266,R267,R268, R371,R269

SDVO_CTRLDATA have internal pull down

LVREF for Alviso N.C
for Calistoga to GND

Close to U9.J20

Close to U9.J22

Trace CRT_IREF should be at least 25 mils away from any other toggling signal.

Stuff AC Caps For Discrete

NOTE:
1@ is for UMA Implemetation.
2@ is for Discrete Implementation.

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Title: Calistoga(3 of 6)

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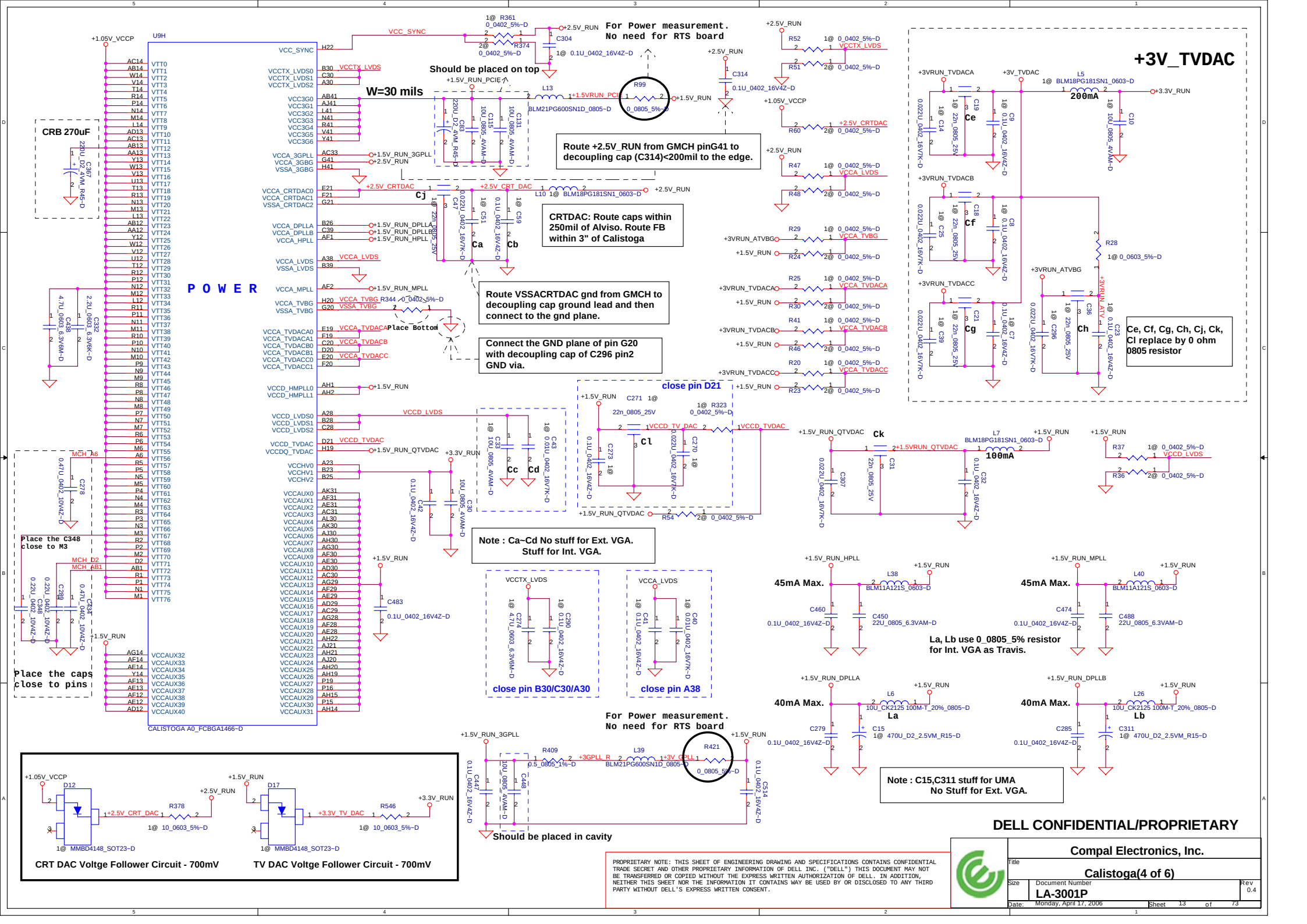

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Title: Calistoga(4 of 6)

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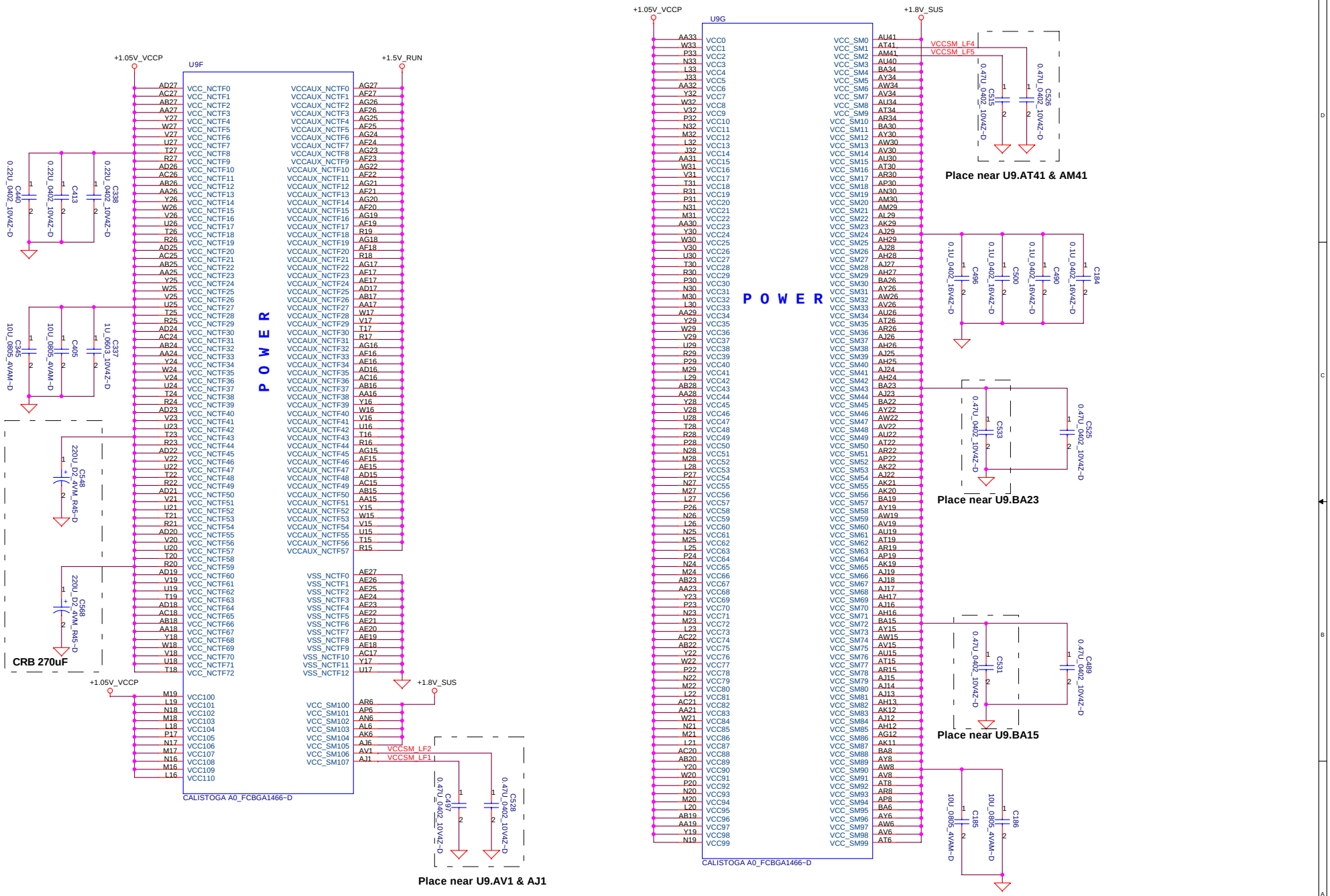

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Title: Calistoga(5 of 6)

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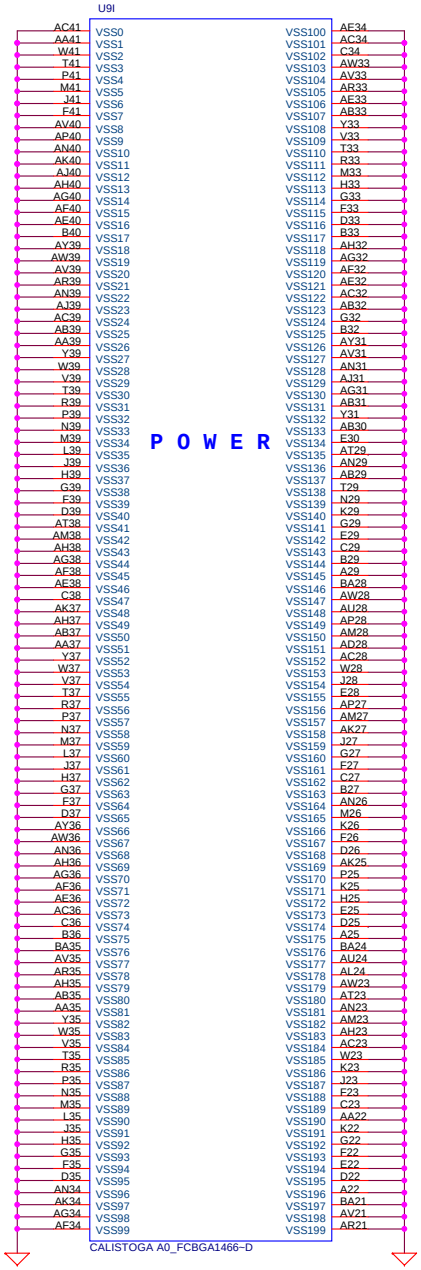

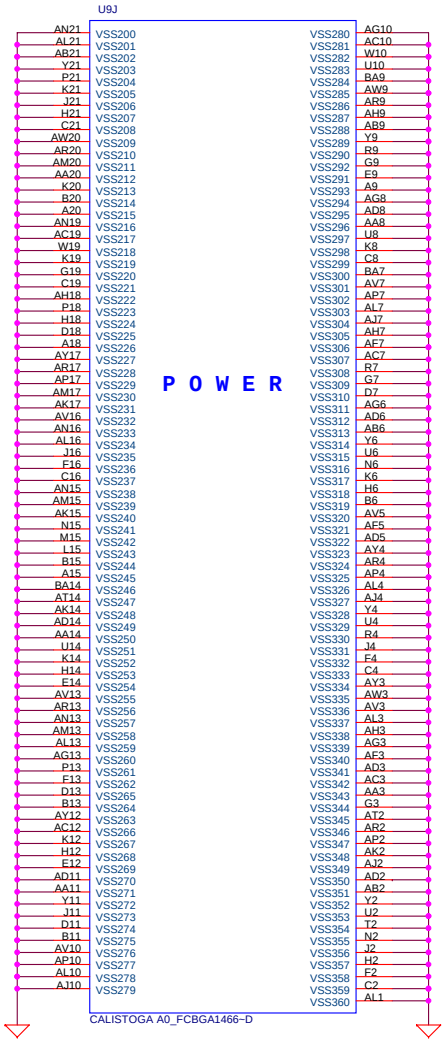

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Title: Calistoga(6 of 6)

Size: | Document Number: LA-3001 | Rev: 0.4

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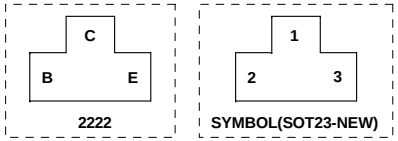
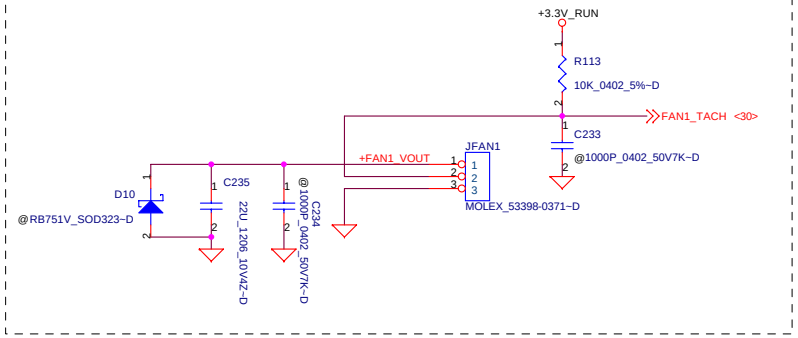
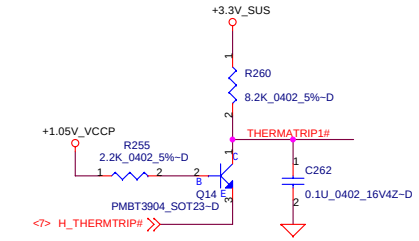
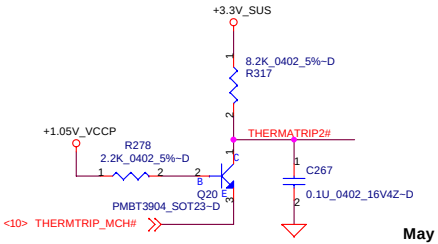


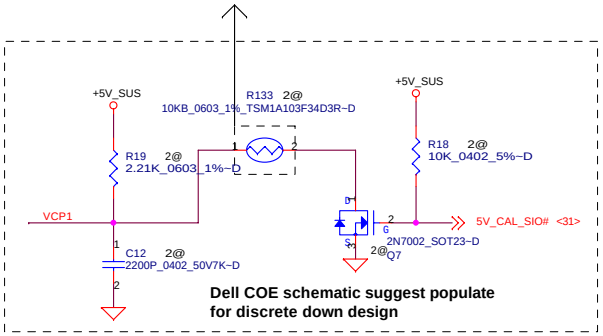
FAN1 Control and Tachometer





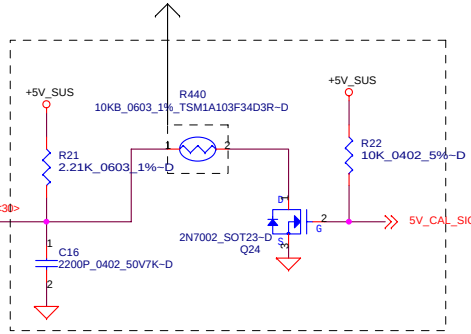


Place thermal resistor near the SODIMM For discrete design



Dell COE schematic suggest populate for discrete down design

May need to place thermal resistor underneath WWAN Mini Card stuff this thermistor circuit for additional sensor in Discrete Down Designs



H_THERMDA/H_THERMDC routing together. Trace width / Spacing = 10 / 10 mil

Place C252 as close to the Guardian pins as possible

REM_DIODE1_N, REM_DIODE1_P routing together. Trace width / Spacing = 10 / 10 mil

Place under CPU

Place C251 as close to the Guardian pins as possible

Vset=(Tp-70/21)

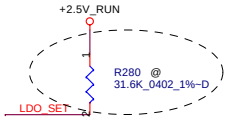
Place C255 as close to the Guardian pins as possible

VGA_THERMDN_R/VGA_THERMDN, VGA_THERMDP_R/VGA_THERMDP routing together. Trace width / Spacing = 10 / 10 mil

To cut the stub trace for discrete M/B

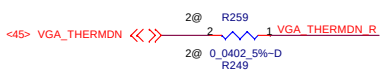
Place near the bottom SODIMM For UMA design

SMBUS ADDRESS : 2F



Voltage margining circuit for LDO output.For Vmargin, stuff R280=31.6K and R279=1K for production

For Discrete: Stuff R259,R249 and no stuff Q13,C253
For UMA: Stuff Q13 and no stuff R259,R249



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Title: Thermal sensor and Fan

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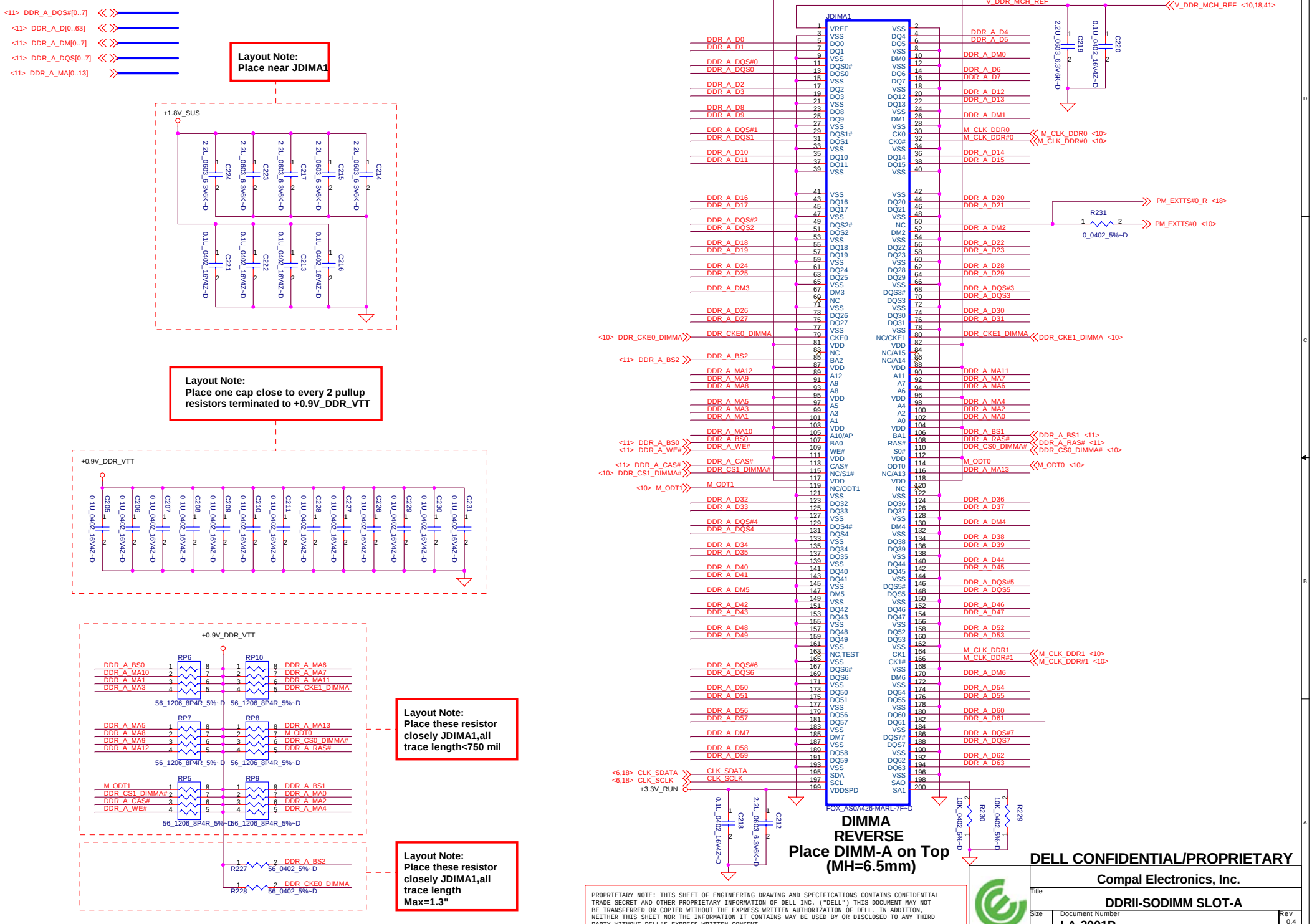
Date: Monday, April 17, 2006 | Sheet 16 of 73


Layout Note:
Place near JDIMA1
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Layout Note:
Place these resistor
closely JDIMA1,all
trace length<750 mil
Layout Note:
Place these resistor
closely JDIMA1,all
trace length
Max=1.3"
JDIMA1
DIMMA
REVERSE
Place DIMM-A on Top
(MH=6.5mm)
FOX_AS0A426-MARL-7F-D
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DDRII-SODIMM SLOT-A
LA-3001P
Monday, April 17, 2006
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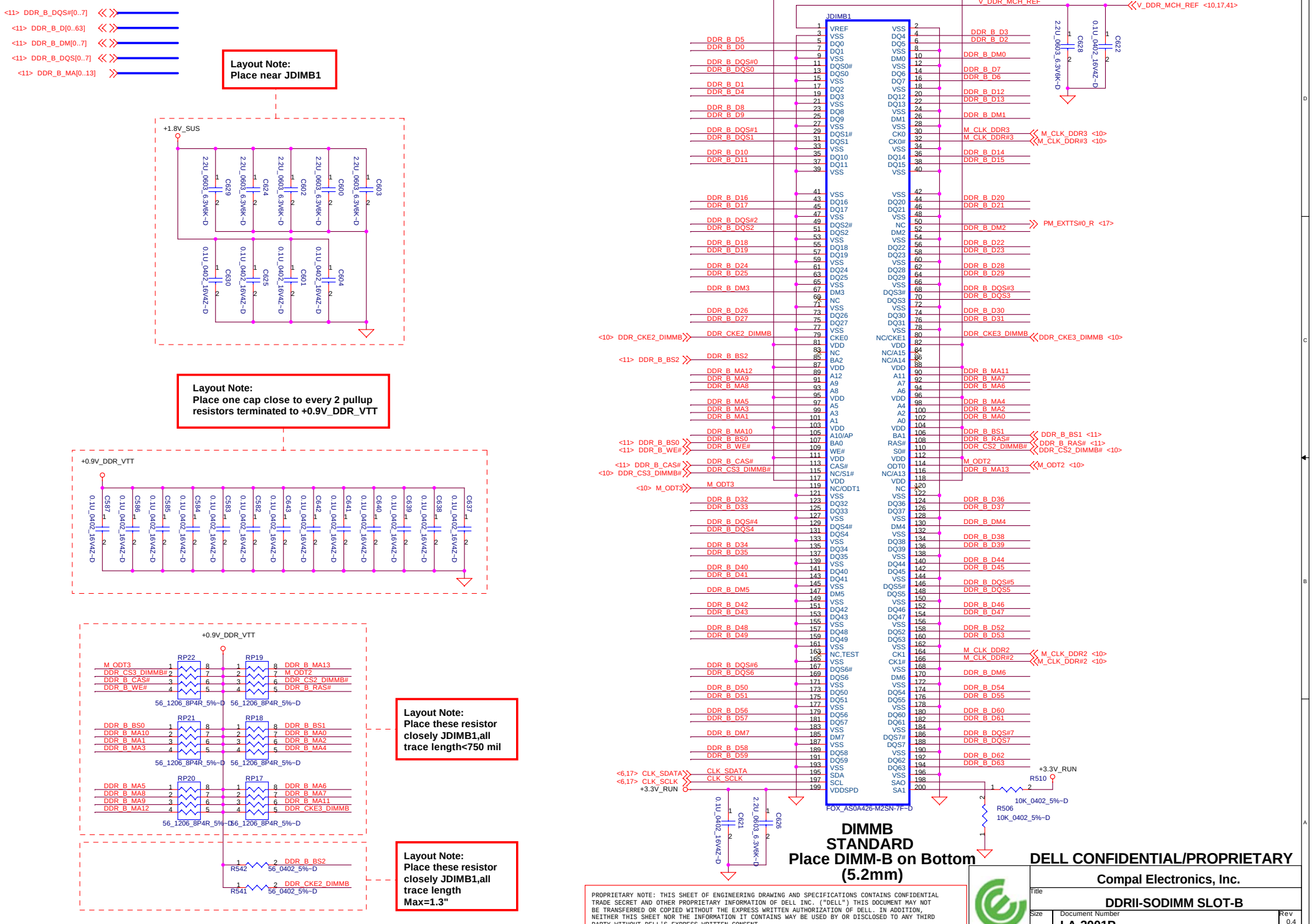

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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT-B

Size | Document Number: LA-3001P | Rev: 0.4

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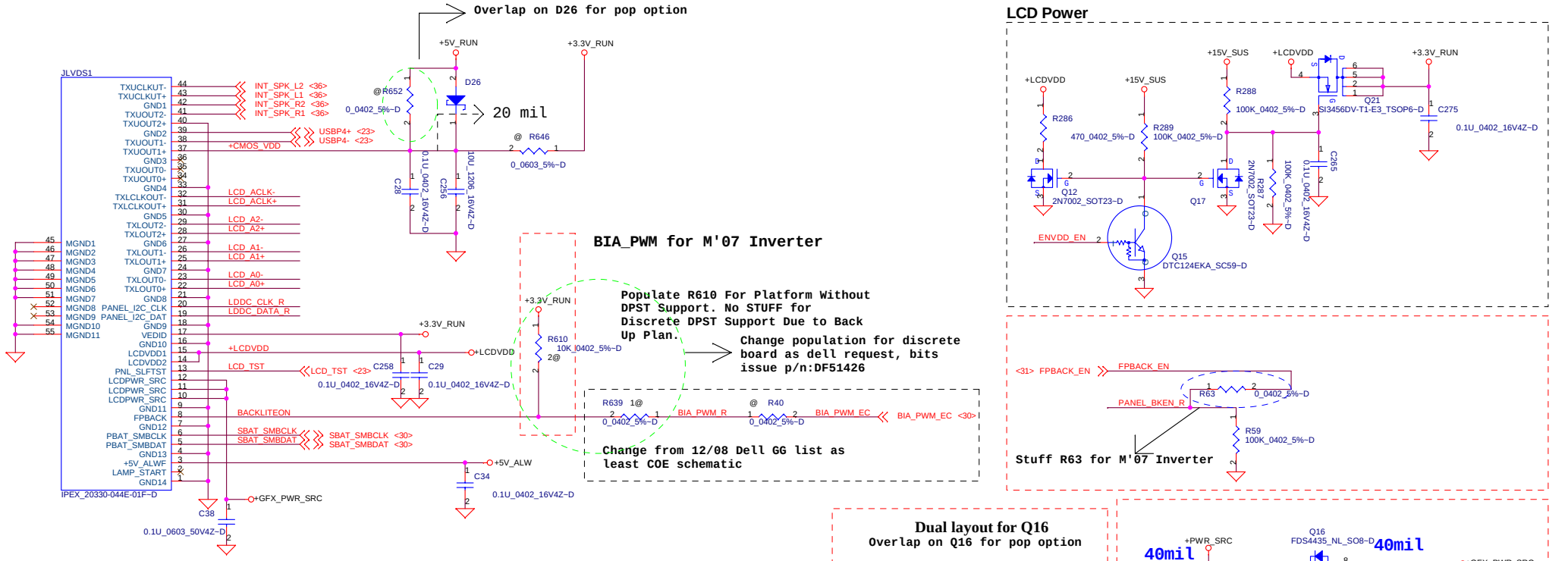
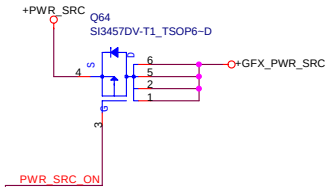


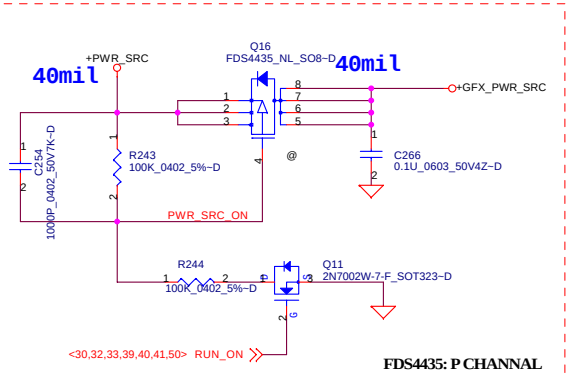
LCD Power

Dual layout for Q16

Overlap on Q16 for pop option



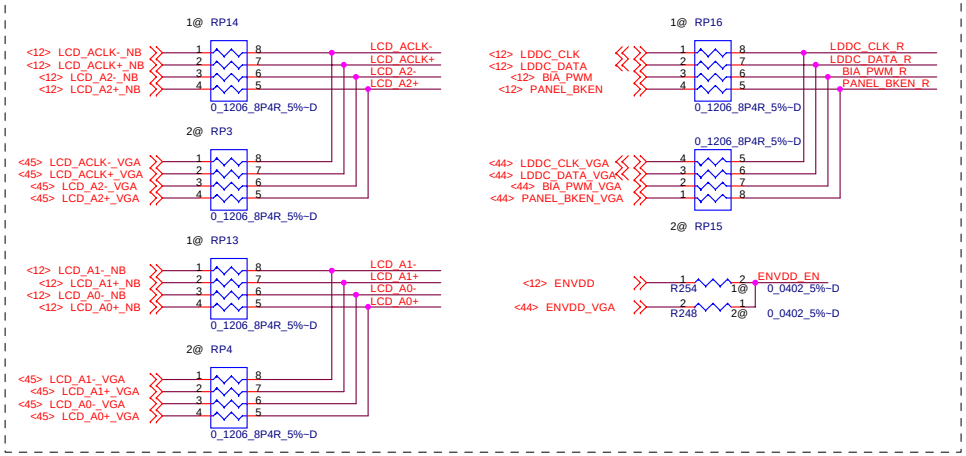
SI3457DV : P CHANNAL



FDS4435: P CHANNAL

Please put the resistors close to connector side

For Discrete: Populting RP3,RP4,RP15,R248
For UMA: Populting RP14,RP13,RP16,R254



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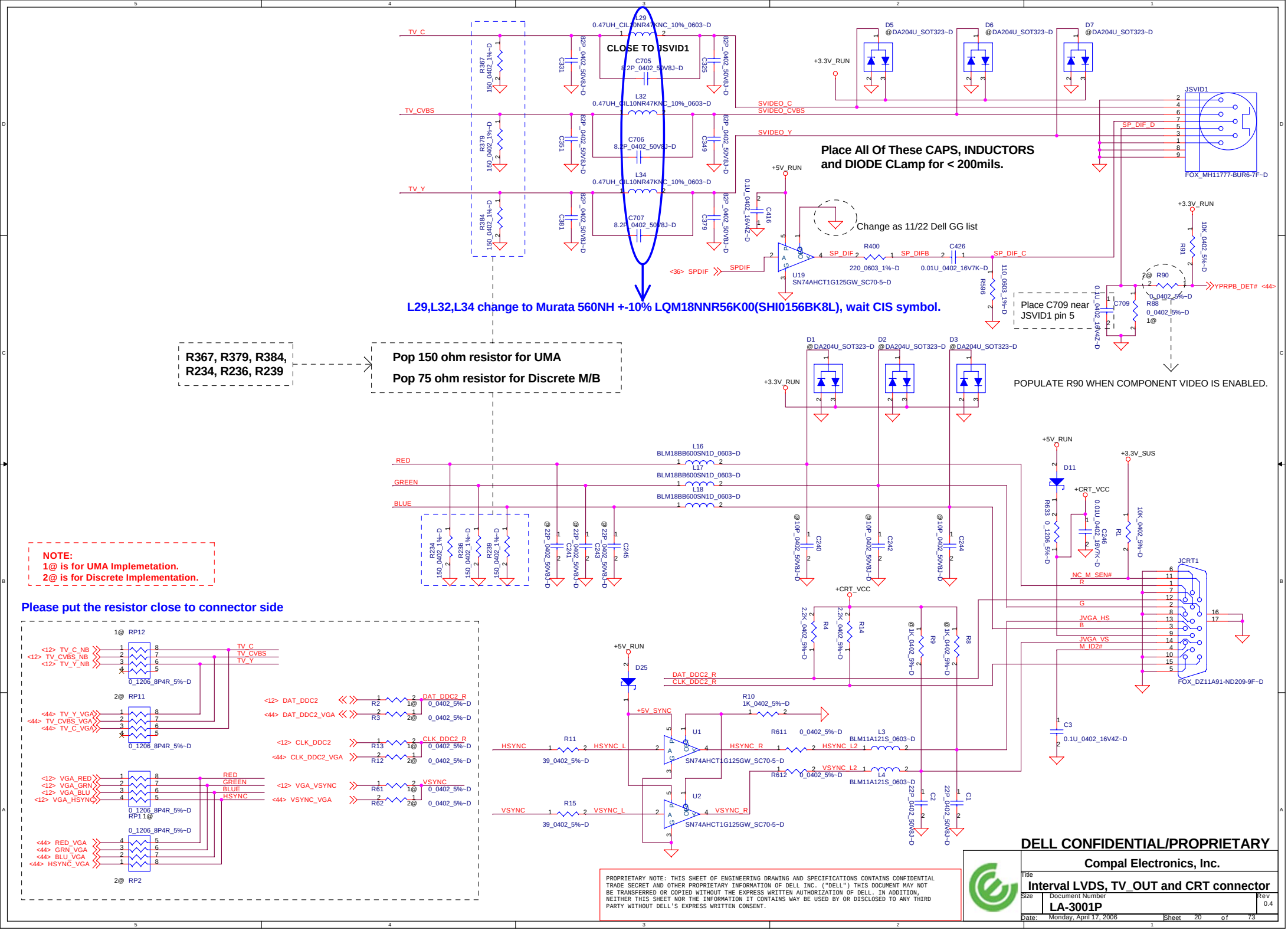
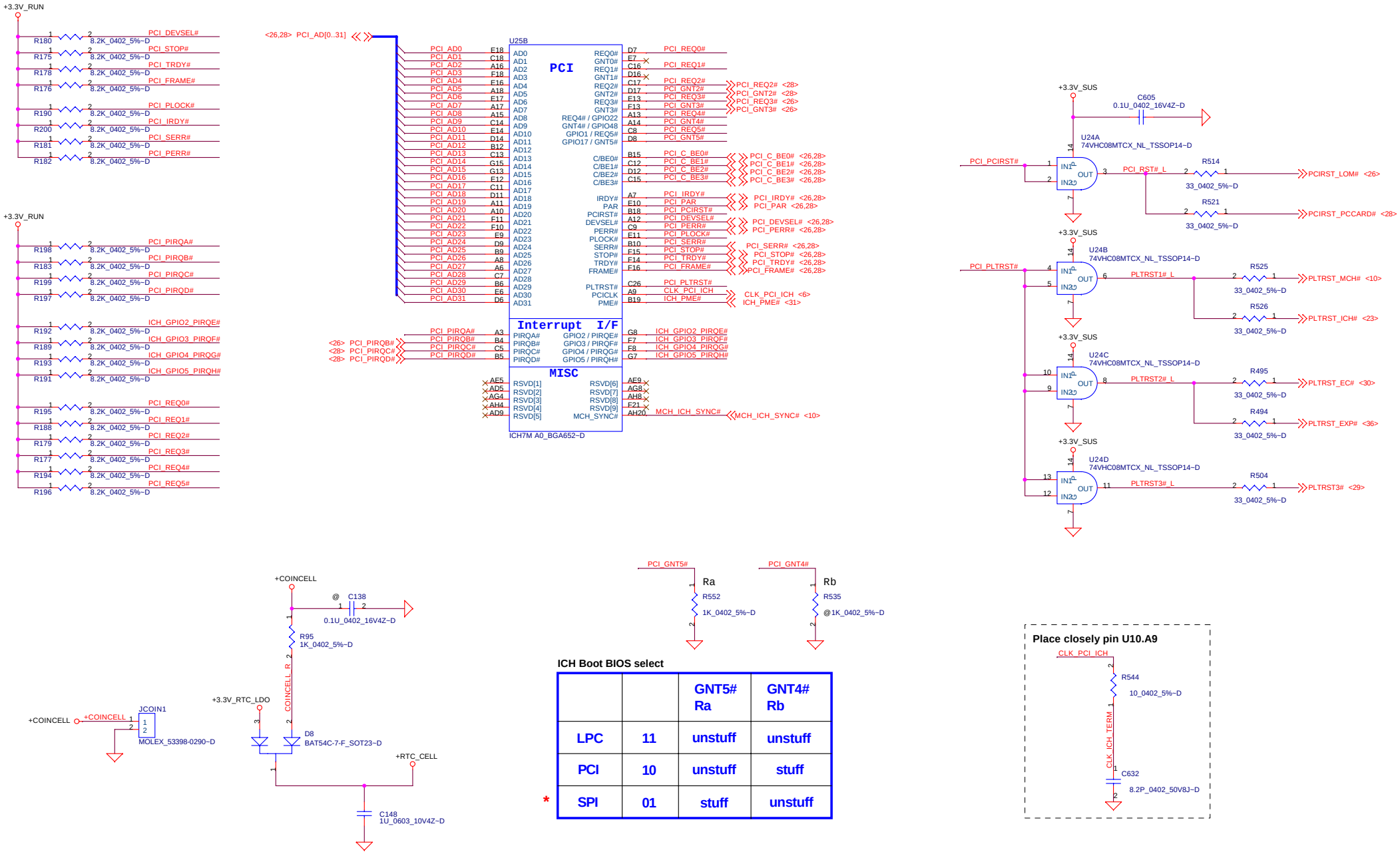
Compal Electronics, Inc.

Title: LVDS Conn

Size | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 19 of 73


CLOSE TO JSVID1
Place All Of These CAPS, INDUCTORS and DIODE CLamp for < 200mils.
L29,L32,L34 change to Murata 560NH +-10% LQM18NNR56K00(SHI0156BK8L), wait CIS symbol.
Change as 11/22 Dell GG list
Place C709 near JSVID1 pin 5
POPULATE R90 WHEN COMPONENT VIDEO IS ENABLED.
R367, R379, R384, R234, R236, R239
Pop 150 ohm resistor for UMA
Pop 75 ohm resistor for Discrete M/B
NOTE:
1@ is for UMA Implemetation.
2@ is for Discrete Implementation.
Please put the resistor close to connector side
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Interval LVDS, TV_OUT and CRT connector
LA-3001P
Monday, April 17, 2006

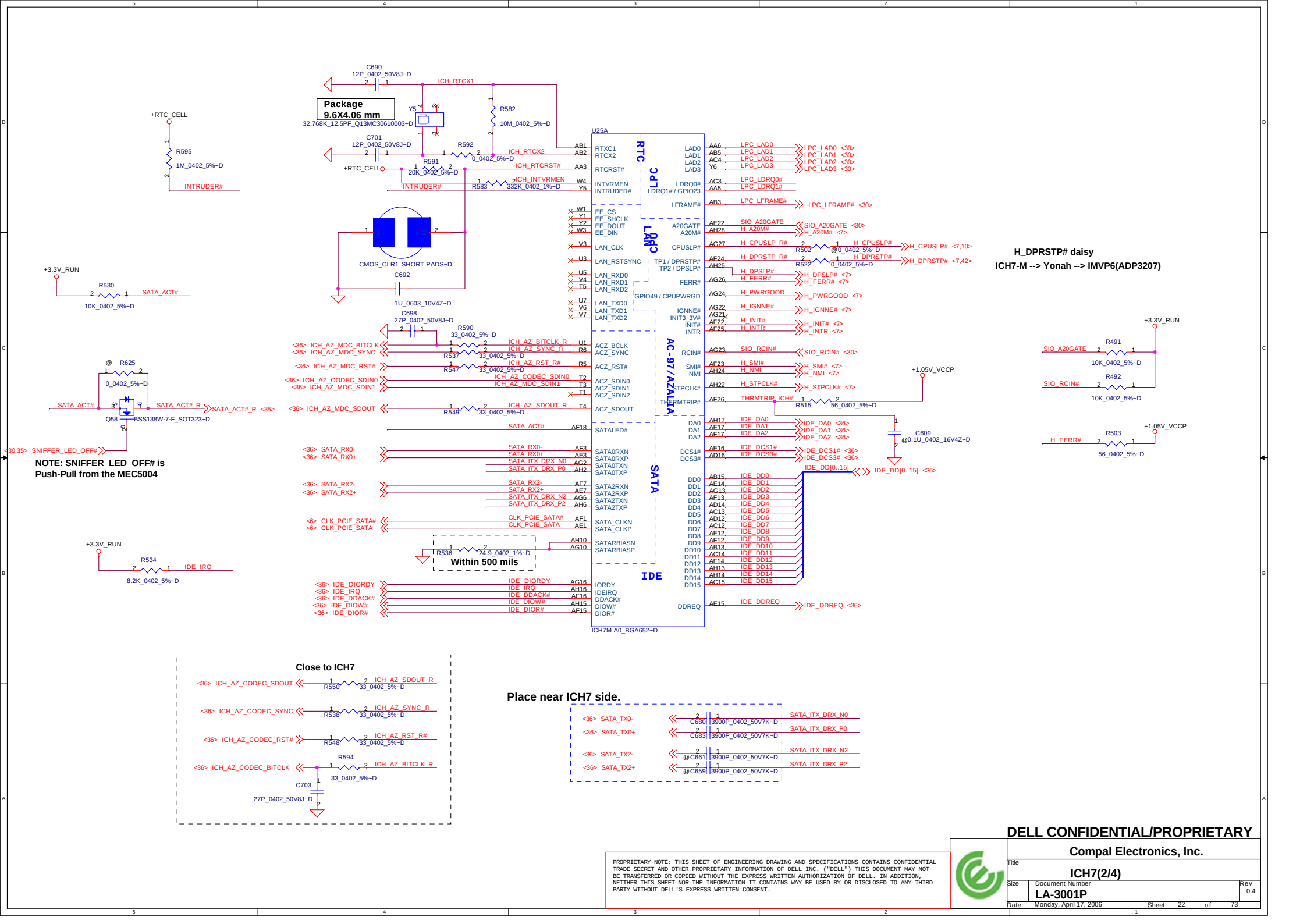


Compal Electronics, Inc.

Title: ICH7(1/4)

Size | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 21 of 73



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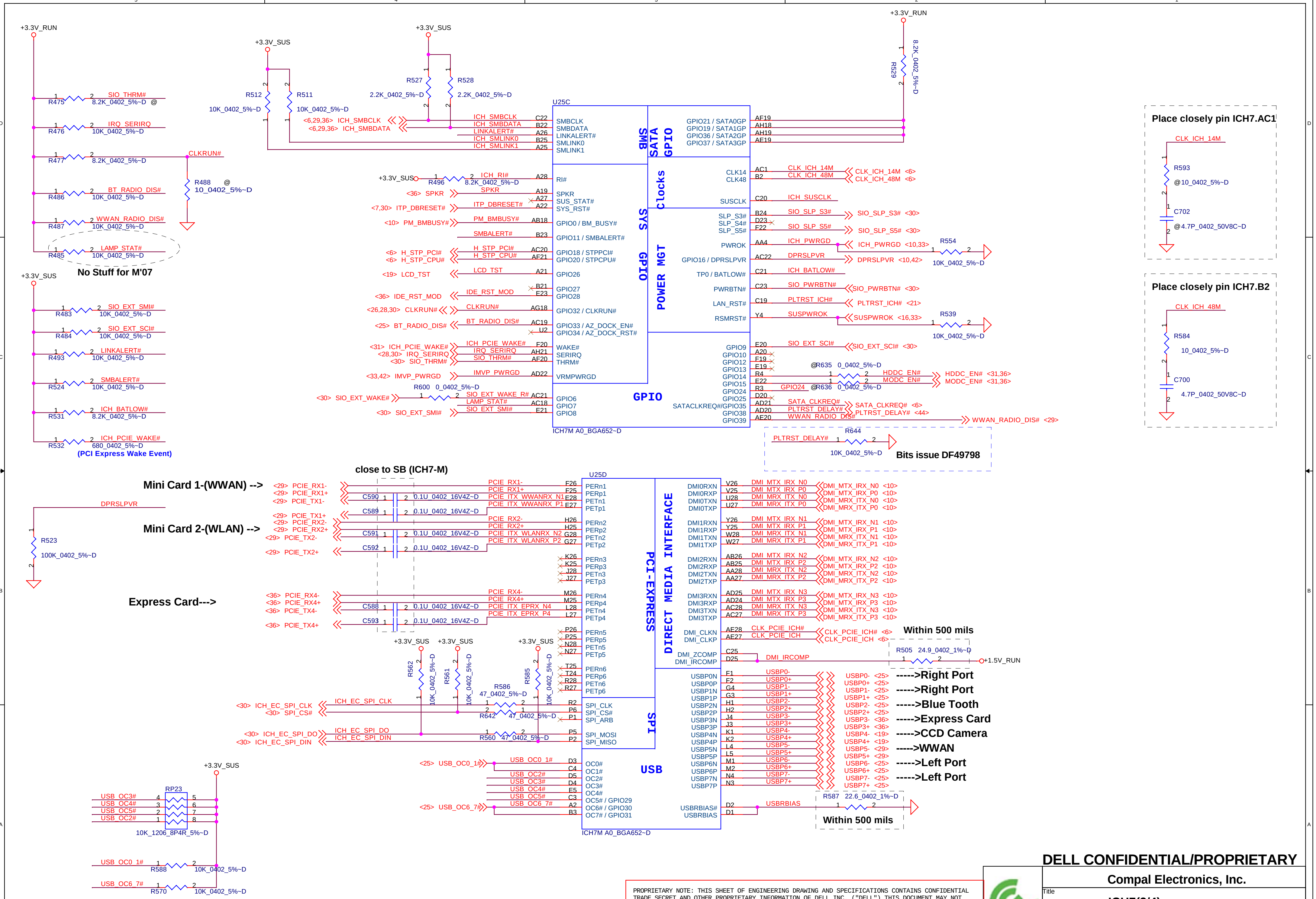
Compal Electronics, Inc.

Title: ICH7(2/4)

Size: | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 22 of 73



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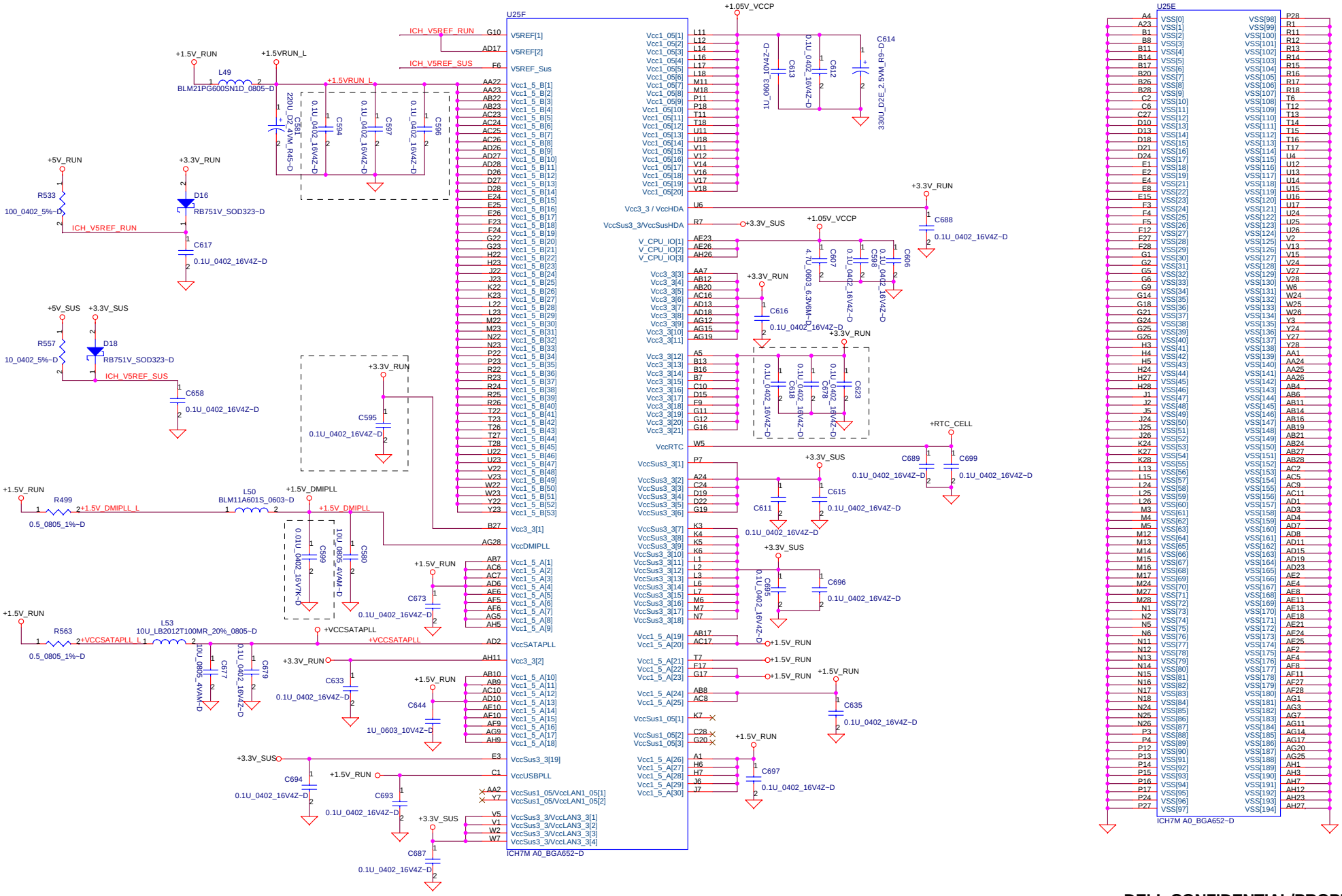
Compal Electronics, Inc.

Title	ICH7(3/4)
Size	Document Number: LA-3001P
Rev	0.4
Date:	Monday, April 17, 2006
Sheet	23 of 73



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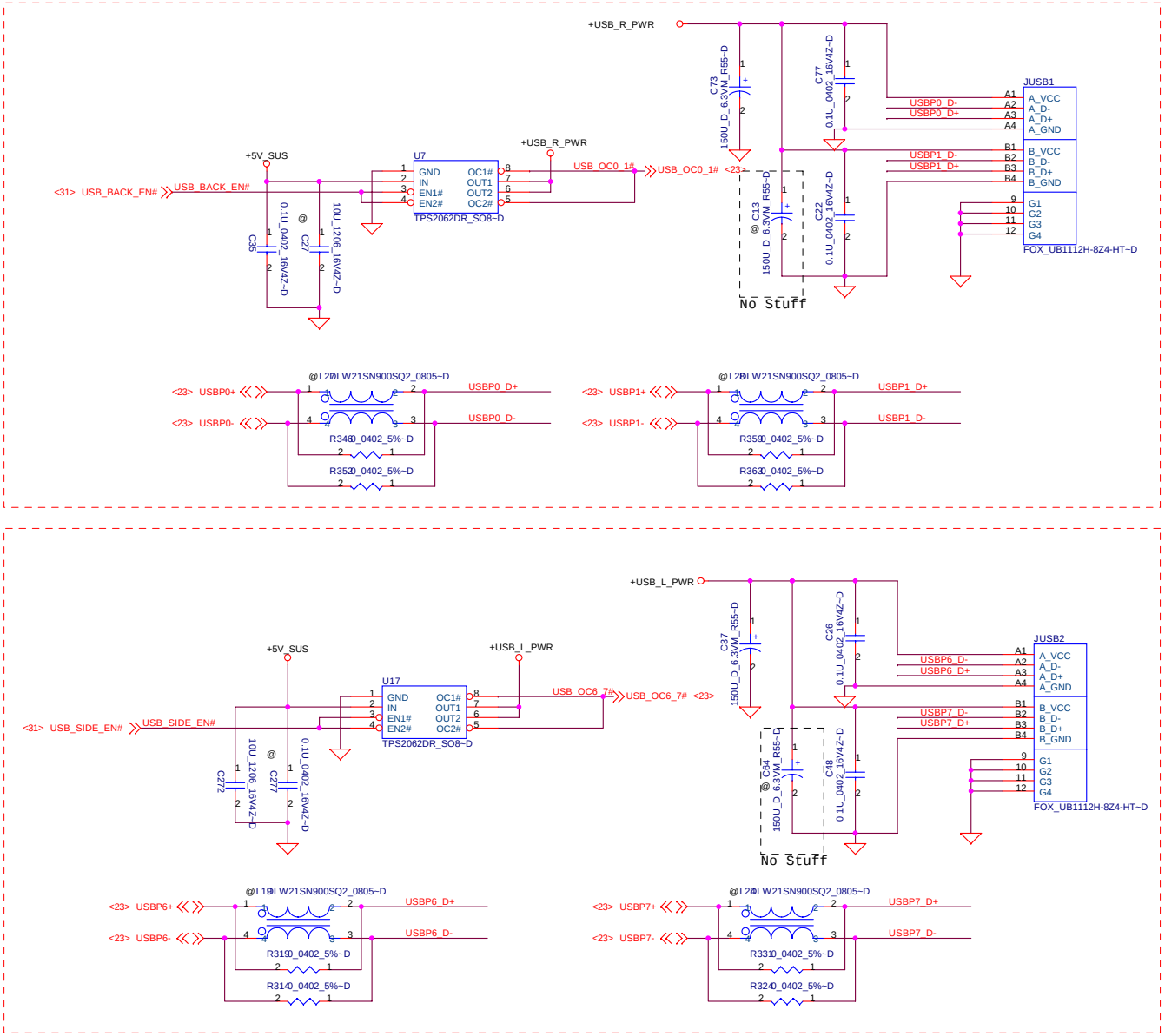
Compal Electronics, Inc.

Title: ICH7(4/4)

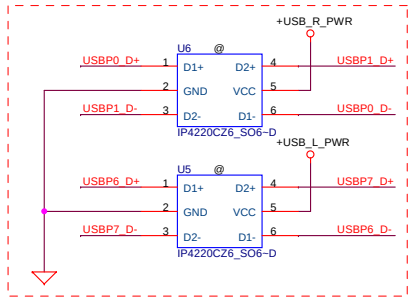
Size: | Document Number: LA-3001P | Rev: 0.4

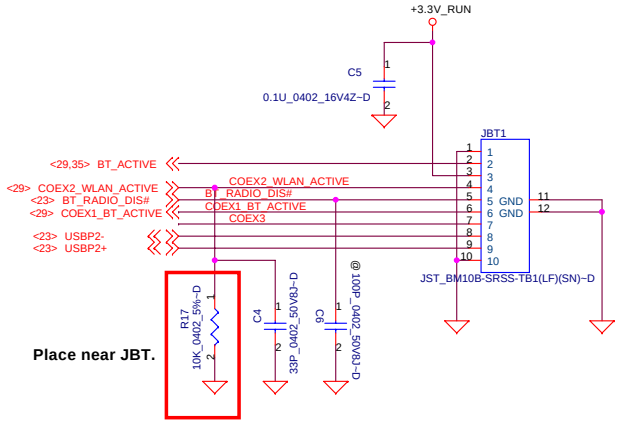
Date: Monday, April 17, 2006 | Sheet 24 of 73



USB PORT#	DESTINATION
0	JUSB1 (Ext Back Right Side)
1	JUSB1 (Ext Back Right Side)
2	Blue Tooth
3	EXPRESS CARD
4	CCD Camera
5	ECE5011 HUB
6	JUSB2 (Ext Back Left Side)
7	JUSB2 (Ext Back Left Side)

Place U5, U6 as close as USB connector.





Compal Electronics, Inc.

Title: USB 2.0 PORT

Size | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 25 of 73

Current Consumption: Max 1.5A

+3.3V_SRC
Q5
SI3456DV-T1-E3_TSOP6-D
<32> ENAB_3VLAN
R112
0_0805_5%-D
+3.3V_LAN
L14
BLM18PG181SN1_0603-D
+3.3V_SUS

LAN_TX+ R68 49.9_0603_1%-D
LAN_TX- R67 49.9_0603_1%-D
LAN_RX+ R65 49.9_0603_1%-D
LAN_RX- R66 49.9_0603_1%-D
C46 0.1U_0402_16V4Z-D
C44 0.1U_0402_16V4Z-D
Place close to LAN chip (U10)
R65-68 should be rated at least 1/16W

	SPROM_DOUT	SPROM_CLK
1Kb	None	None
4Kb	10K Pullup	None
16Kb	None	10K Pullup

+1.8V_LOM
+3.3V_LAN
C85 1000P_0402_50V7K-D

U10
Broadcom
BCM 4401KQL
BCM4401KQL_LQFP128-D

PCI_AD[0..31]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0

PCI_CBE3_L PCI_CBE2_L PCI_CBE1_L PCI_CBE0_L
PCI_FRAME_L PCI_IRDY_L PCI_TRDY_L PCI_DEVSEL_L PCI_STOP_L PCI_PERR_L PCI_SERR_L PCI_PAR PCI_INT_L
PCI_RST_L PCI_CLK PCI_GNT_L PCI_REQ_L PCI_PME_L PCI_IDSEL
PCI_CLKRUN_L
XTAL_IN XTAL_OUT

R101 100_0402_5%-D
PCI_AD16 LAN_AD16
<23,28,30> CLKRUN#
<21> PCIRST_LOM#
<6> CLK_PCI_LOM
<21> PCI_GNT3#
<21> PCI_REQ3#
<28,31> SYS_PME#
<21> PCI_PIRQB#

R92 806_0402_1%-D
Y2 25MHZ_20PF_1BG25000CKLA-D
XI XO
C97 27P_0402_50V8J-D
C99 27P_0402_50V8J-D

Place closely pin 118
CLK_PCI_LOM
R114 33_0402_5%-D
C171 22P_0402_50V8J-D

LED0_L LED1_L LED2_L LED3_L
LINK_LED10# LINK_LED100# ACTLED#
LINK_LED10# <27>
LINK_LED100# <27>
ACTLED# <27>

R389 10K_0402_5%-D
R399 10K_0402_5%-D
R402 10K_0402_5%-D

EPHY_AGND EPHY_AVDD
EPHY_BIAS_AVDD EPHY_BIAS_AVSS
EPHY_PLLVDD EPHY_PLLGND
EPHY_VREF EPHY_RDAC EPHY_TESTMODE
R387 1.27K_0402_1%-D
L11 BLM11A601S_0603-D
EPHY_BIAS_AVDD
EPHY_PLLVDD

EPHY_TDP EPHY_TDN EPHY_RDP EPHY_RDN
LAN_TX+ LAN_TX- LAN_RX+ LAN_RX-
LAN_TX+ <27>
LAN_TX- <27>
LAN_RX+ <27>
LAN_RX- <27>

NC0 NC2 NC3 NC4 NC5 NC6 NC7

VAUX_AVAIL GPIO0 GPIO1
R412 1K_0402_5%-D
EECLK_PXE EEDATA_PXE

SPROM_CS SPROM_CLK SPROM_DOUT SPROM_DIN

EXT_POR_L
LOM_LOW_PWR# <31>

JTAG_TDO JTAG_TCK JTAG_TDI JTAG_TRST_L JTAG_TMS

U12
SPROM_CS SPROM_CLK SPROM_DOUT SPROM_DI
CS SK DI DO VCC NC ORG GND
AT93C46-10SU-2.7_SO8-D
C122 0.1U_0402_16V4Z-D
U12:ORG NC is 16x64.

Place R381,C352,C493 close to pin69
R381 0_0603_5%-D
Replace with BLM11A601S if needed to meet noise guideline for EPHY_BIAS_AVDD pin
C352 C493 C70 C156 C155 C118
C152 C128 C72 C162 C160 C121 C75 C144 C86

Place C66,C78 close to pin64
C66 2.2U_0805_10V6K-D
C78 1000P_0402_50V7K-D

C133 C67 C69 C139 C143 C76
Place close to pin 57

place Decoupling as closed physically possible to each power pins

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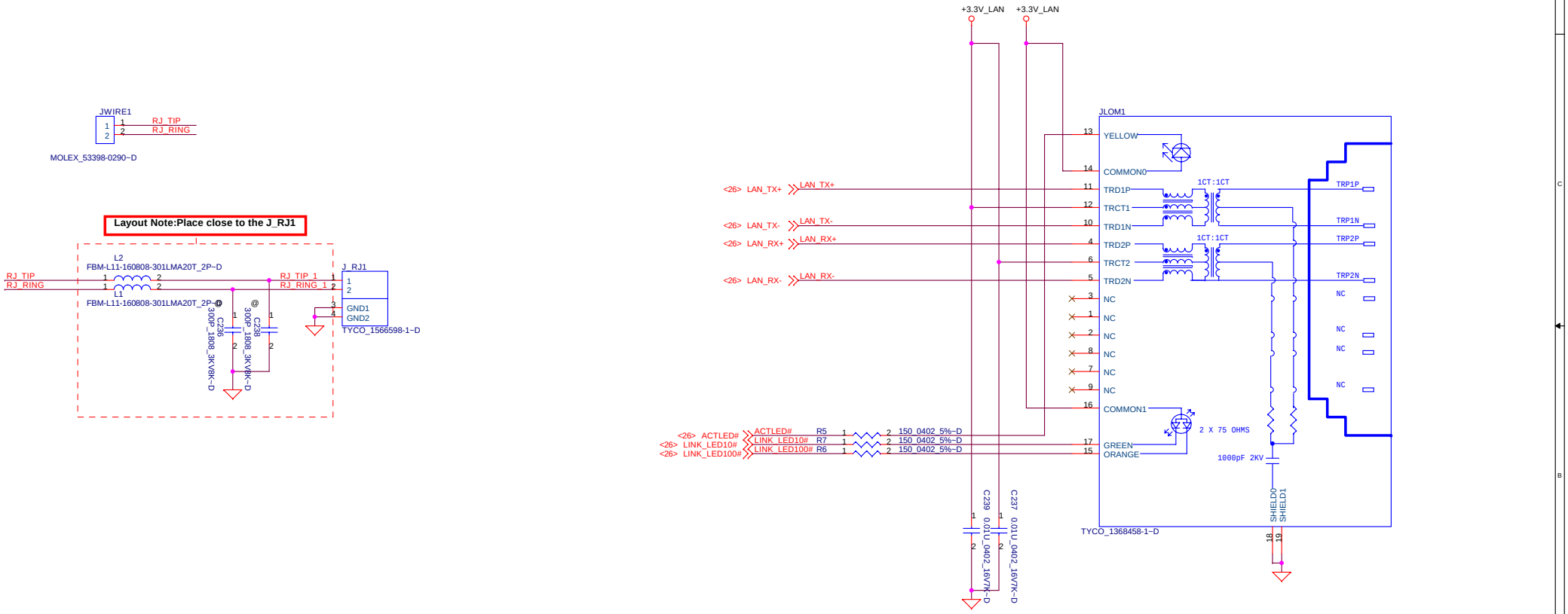
Compal Electronics, Inc.
Title: BROADCOM 4401L LAN
Size: Document Number: LA-3001P Rev: 0.4
Date: Monday, April 17, 2006 Sheet 26 of 73

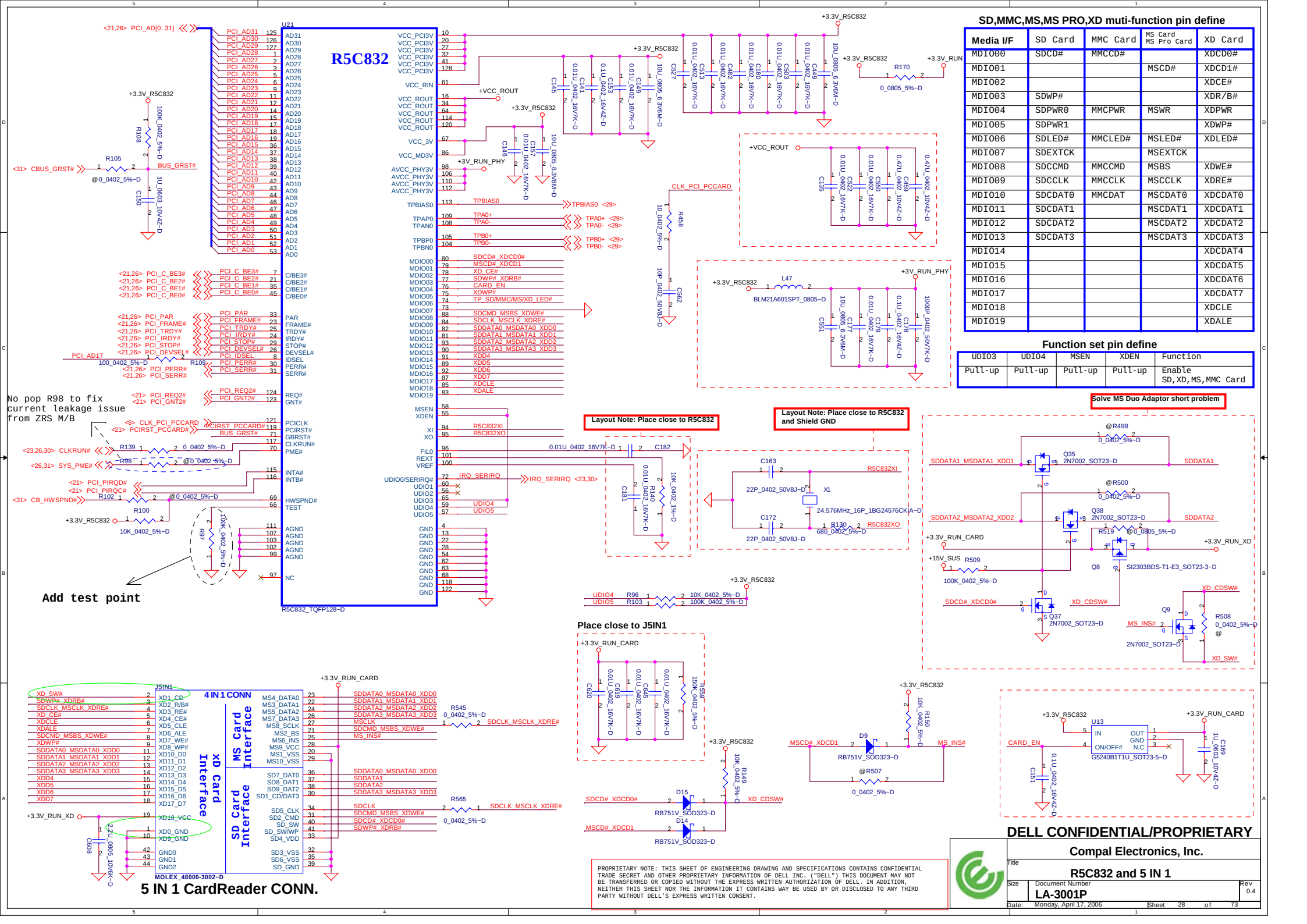


Compal Electronics, Inc.

Title: Magnetic & RJ45

Size | Document Number: LA-3001 | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 27 of 73



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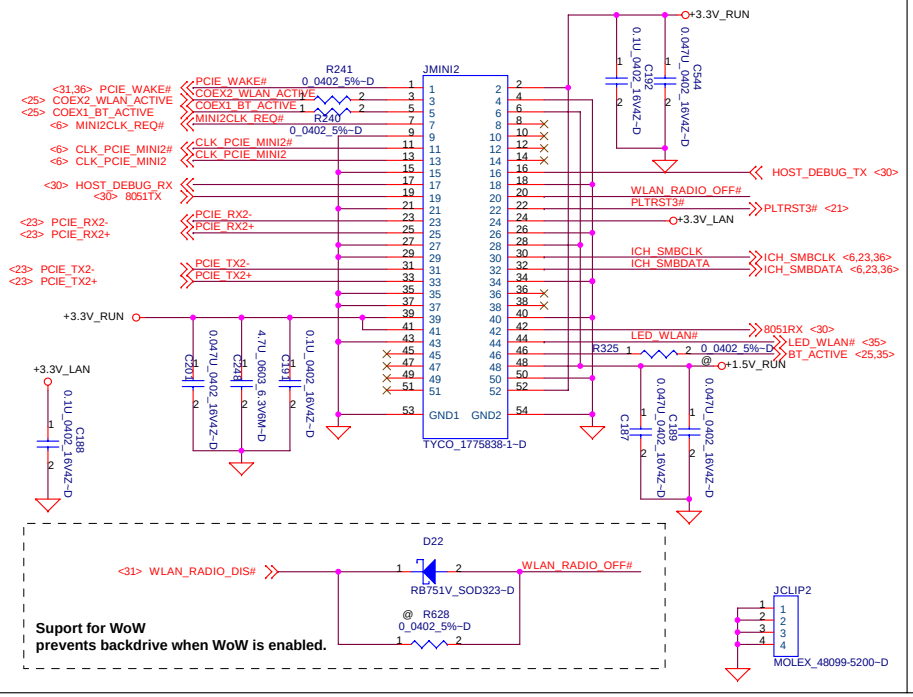
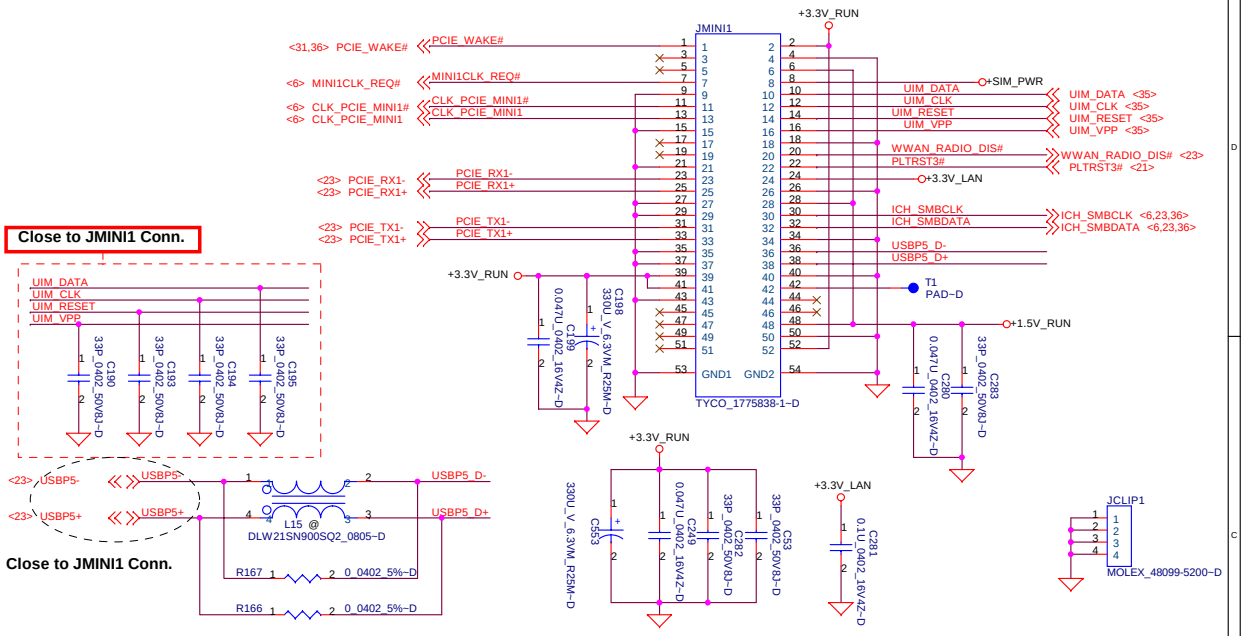
Mini Wireless LAN Card



Suport for WoW prevents backdrive when WoW is enabled.

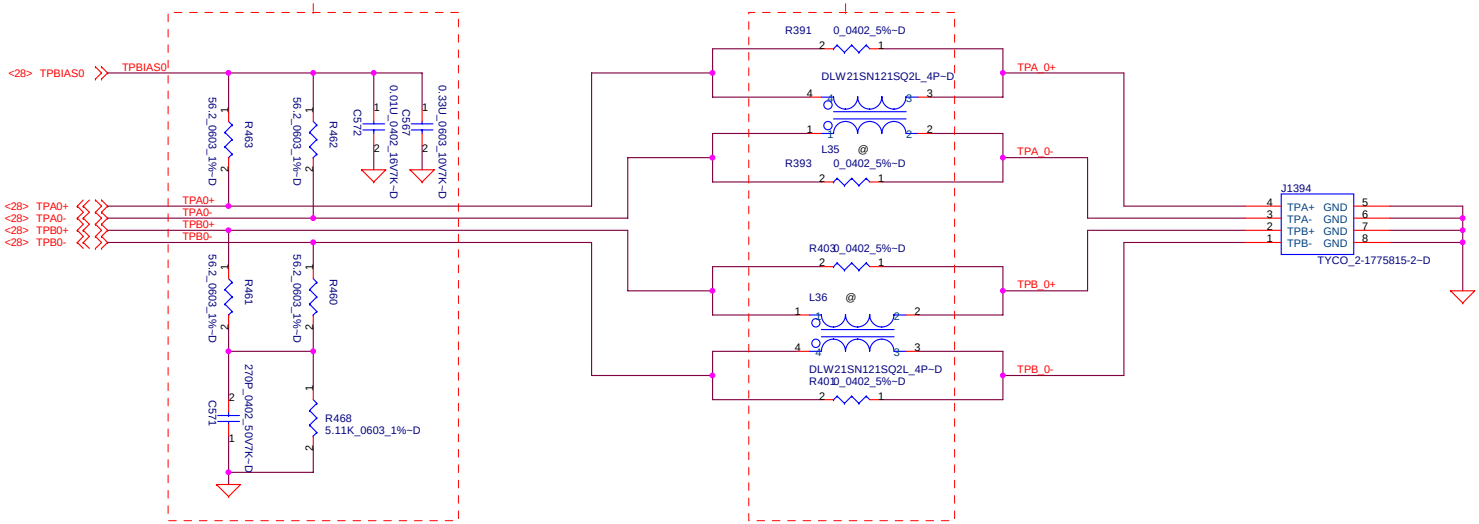
Mini Wireless WAN Card



Close to JMINI1 Conn.

Layout Note: Place close to R5C832 Chip

Layout Note: Place close to 1394 Connector



Compal Electronics, Inc.

Title: MINI CARD & 1394 Connector

Size: | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 29 of 73

5V tolerant pins

IMCLK,IMDAT,EMCLK,EMDAT,KCLK,KDAT,8051RX,8051TX GPIO43,GPIO35~37

Place closely pin 58

Keyboard and Mouse Interface

PWR SW

LPC Interface

Host/8051

BC Bus

U20

MEC5004_VTQFP128~D

For power 15V charge bump circuit

1 = Discrete Gfx (Pop Ra)

0 = UMA (Pop Rb)

Bits issue list: WI52662

Flash ROM

150 MIL SO8

200 MIL SO8

MX25L8005MI-15G_SOP8~D

M25P80-VMW6TP_SO8~D

Work around circuit for EMC5004 Rev.C version

1=Flash Recovery Enabled

0=Flash Recovery Disabled

Low = write protected

STUFF for Development

NO STUFF for Production

Flash write protect bottom 4K of internal bootblock flash

Use Low ESR cap<2 ohms

To SW/B

1.5mm SMT~D

@MOLEX_53398-0571~D

32.768K_12.5PF_Q13MC30610003~D

@RB751V_SOD323~D

@MMBT3906_SOT23~D

@2N7002_SOT23~D

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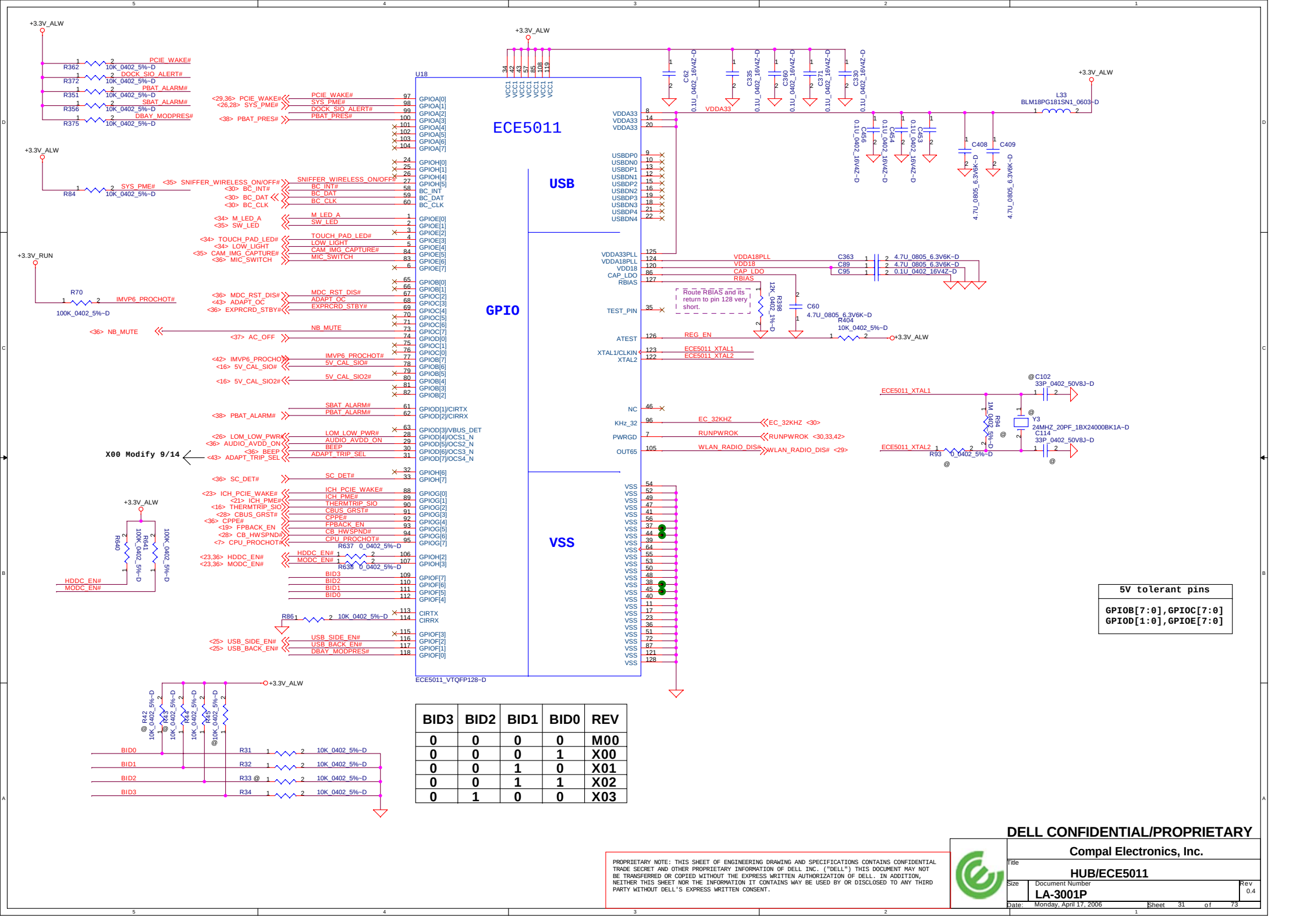
Compal Electronics, Inc.

Title: EMC5004

Size: | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 30 of 73



BID3	BID2	BID1	BID0	REV
0	0	0	0	M00
0	0	0	1	X00
0	0	1	0	X01
0	0	1	1	X02
0	1	0	0	X03

Compal Electronics, Inc.

Title: HUB/ECE5011

Size: | Document Number: LA-3001P | Rev: 0.4

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Run Planes Enable

+3VRUN Source

+3.3V_SRC
Q45 SI4810DY_SO8-D
+3.3V_RUN
R632 2@ 100K_0402_5%-D
GFX_RUN_ON <50>
C663 10U_0805_10V4Z-D
R568 20K_0402_5%-D
D23 MMBD4148_SOT23-D
<39> RUN_ENABLE
R631 200K_0402_5%-D
C708 470P_0402_50V7K-D

Updated as COE A06

3.3VRUN Turn ON Delay: Populate RC Componant

CPU VR Requirements: 5VRUN need to be > 1.5Vlevel, before 3.3VRUN canbe Switched ON.

+15V_SUS
+5V_ALW
R572 100K_0402_5%-D
R569 100K_0402_5%-D
RUN_ON_5V#
Q49 2N7002_SOT23-D
<19,30,33,39,40,41,50> RUN_ON
Q46 2N7002_SOT23-D
RUN_ENABLE
C685 4700P_0402_25V7K-D

+5VRUN Source

+5V_SUS
Q26 SI4810DY_SO8-D
+5V_RUN
R467 20K_0402_5%-D
C547 10U_0805_10V4Z-D

Maximum Rds for Q45, Q26,Q4 should 15mohm

+1.8VRUN Source

+1.8V_SUS
Q4 2@ SI4800DY-T1-E3_SO8-D
+1.8V_RUN
R138 20K_0402_5%-D 2@
C159 10U_0805_10V4Z-D 2@
2@ D24 MMBD4148_SOT23-D
R107 2@ 200K_0402_5%-D
C154 0.047U_0402_16V4Z-D 2@

For G72 GDDR3 Power

+5V_RUN
R58 @ 30_0805_5%
Z4005
Q2 @ 2N7002_SOT23-D
RUN_ON_5V#

+3.3V_RUN
R540 @ 30_0805_5%
Z4006
Q39 @ 2N7002_SOT23-D

+1.8V_RUN
R567 @ 30_0805_5%
Z4007
Q44 @ 2N7002_SOT23-D

+1.5V_RUN
R447 @ 30_0805_5%
Z4008
Q25 @ 2N7002_SOT23-D

Reserve for discharge path

+0.9V_DDR_VTT
R558 @ 30_0805_5%
Z4009
Q42 @ 2N7002_SOT23-D

+2.5V_RUN
R564 @ 30_0805_5%
Z4010
Q47 @ 2N7002_SOT23-D

+1.8V_SUS
R597 30_0805_5%
Z4011
SUS_ON_5V#
Q52 2N7002_SOT23-D

+3.3V_LAN power enable signal

+PWR_SRC
R497 100K_0402_5%-D
R513 100K_0402_5%-D
ENAB_3VLAN
ENAB_3VLAN <26>
Q36 2N7002_SOT23-D
R520 470K_0402_5%-D
<30,39> AUX_EN
AUX_EN
Q34 2N7002_SOT23-D
R501 200K_0402_5%-D

+3.3V_SUS Source

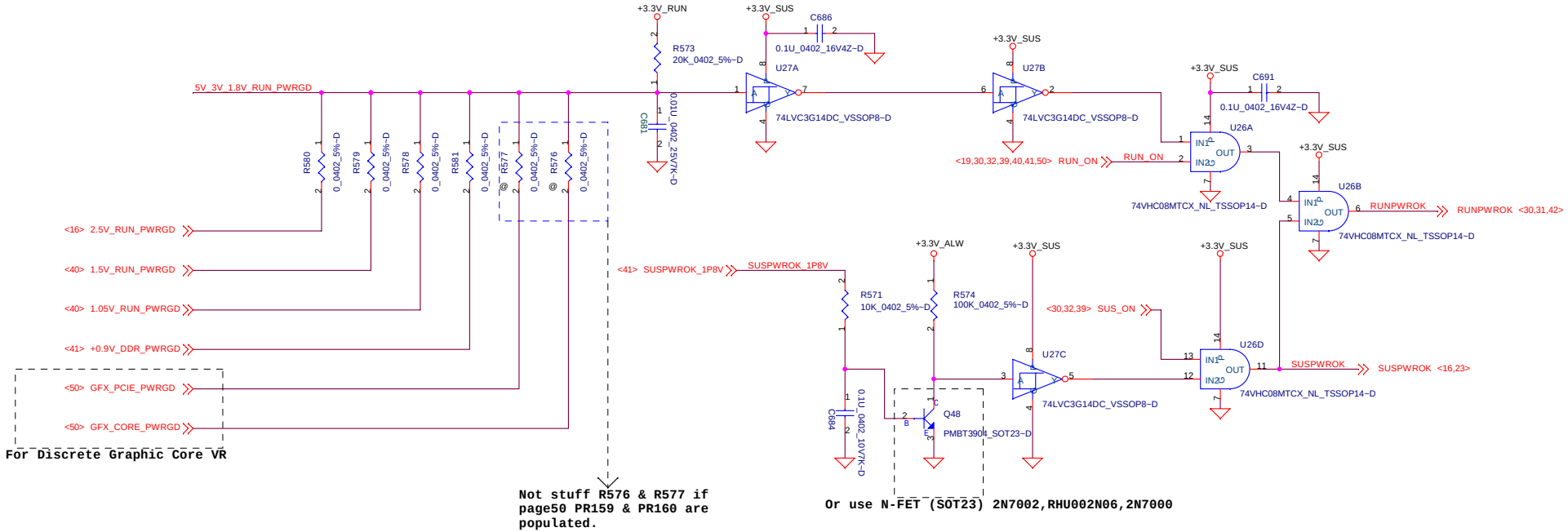
+15V_SUS
+5V_ALW
+3.3V_SRC
Q43 SI4810DY_SO8-D
+3.3V_SUS
R556 100K_0402_5%-D
R555 100K_0402_5%-D
SUS_ENABLE
C660 10U_0805_10V4Z-D
R553 20K_0402_5%-D
SUS_ON_5V#
Q41 2N7002_SOT23-D
<30,33,39> SUS_ON
SUS_ON
Q40 2N7002_SOT23-D

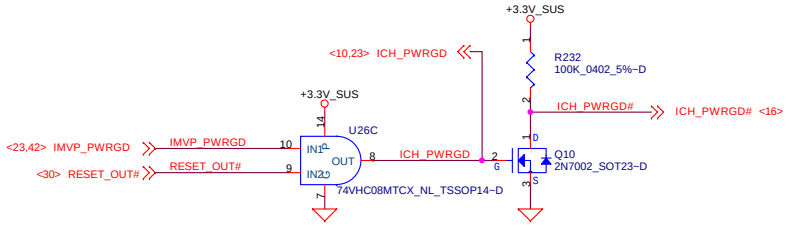
Compal Electronics, Inc.

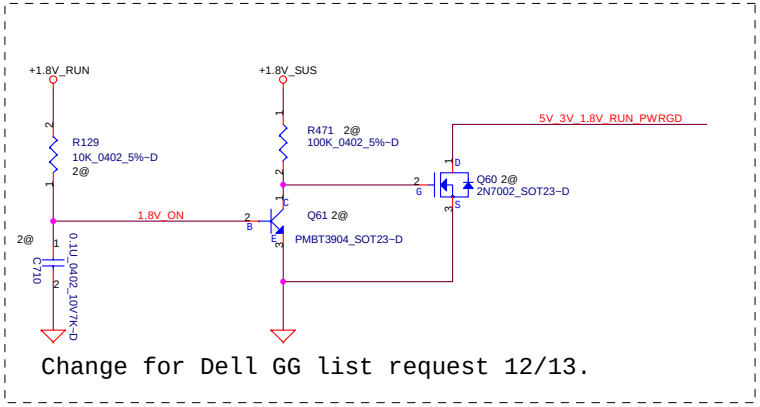
Title: POWER CONTROL

Size | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 32 of 73







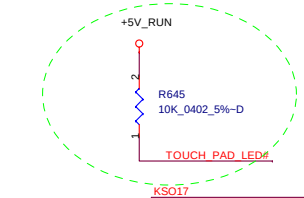
Compal Electronics, Inc.

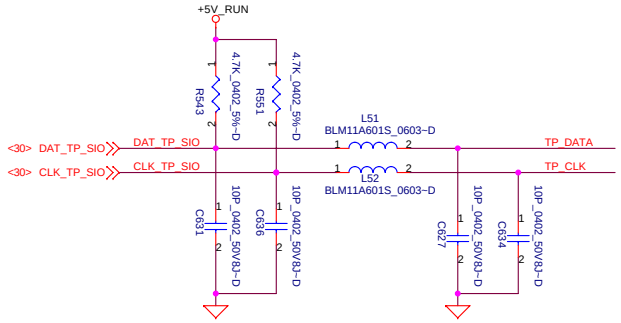
Title: POWER SEQUENCE

Size: | Document Number: LA-3001P | Rev: 0.4

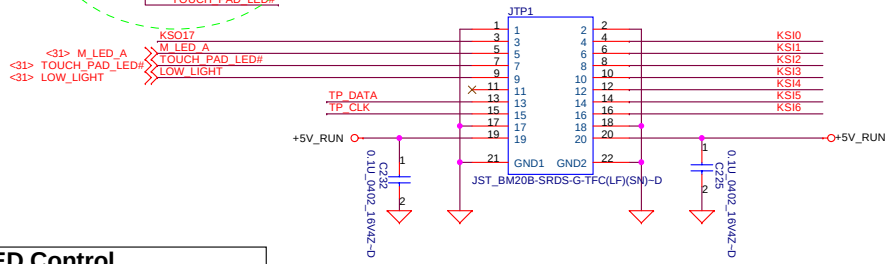
Date: Monday, April 17, 2006 | Sheet 33 of 73

Add a 10K pull-up to +5V_RUN from bits issue list: WI52078



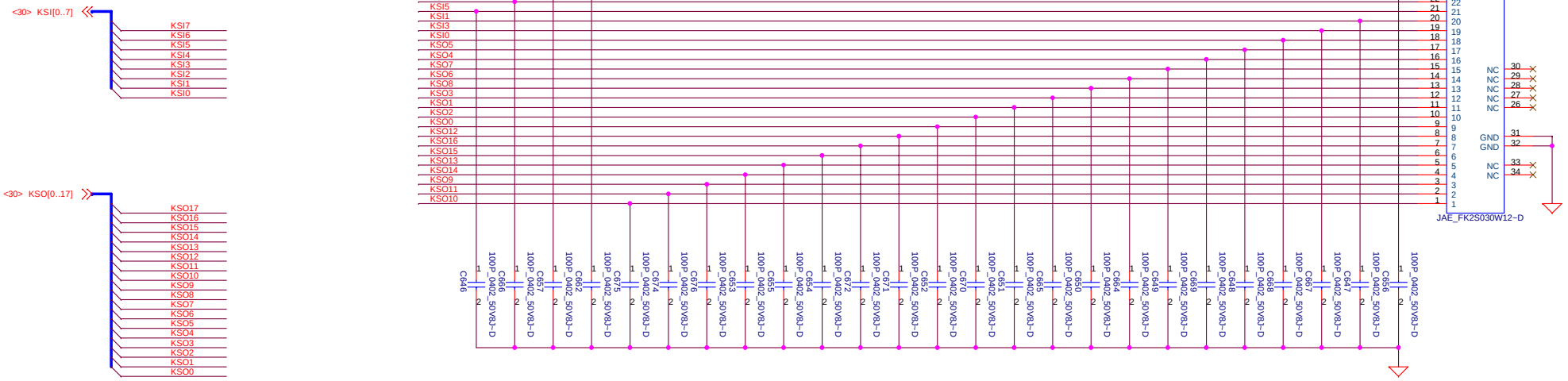


T/P & Media CONN.



LED Control		
Status	**LOW_LIGHT**	**TOUCH_PAD_LED#**
OFF	**L**	**L**
LOW	**L**	**H**
HIGH	**H**	**H**

Signals	Description
M_LED_A	**High bright for Media LED**
	High bright for Touch PAD LED
	Low bright for Media LED/Touch PAD LED

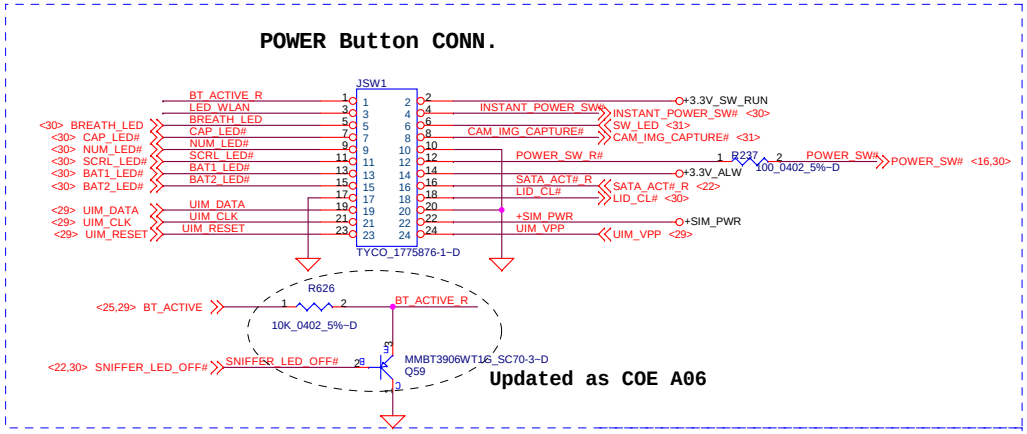


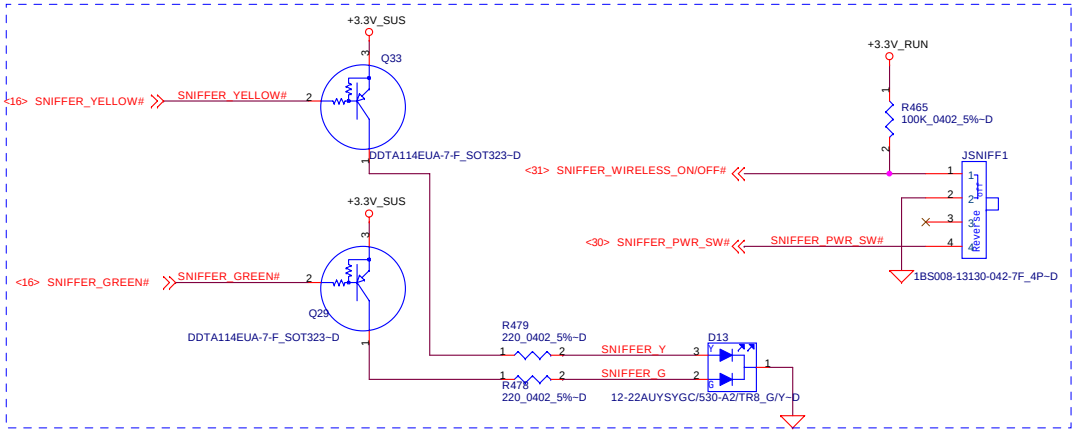
Compal Electronics, Inc.

Title: **INT KB/Touch Pad/Media CONN**

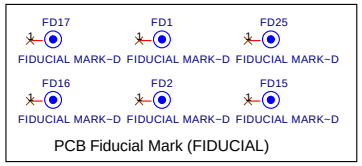
Size | Document Number: **LA-3001P** | Rev: 0.4

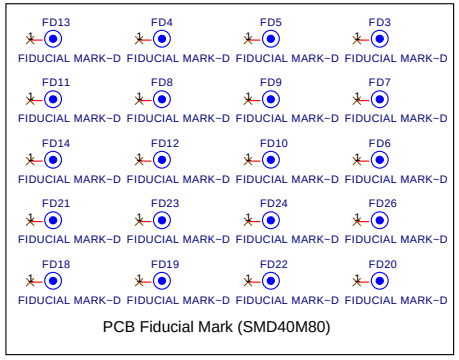
Date: Monday, April 17, 2006 | Sheet 34 of 73

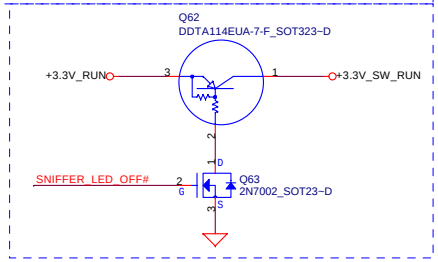


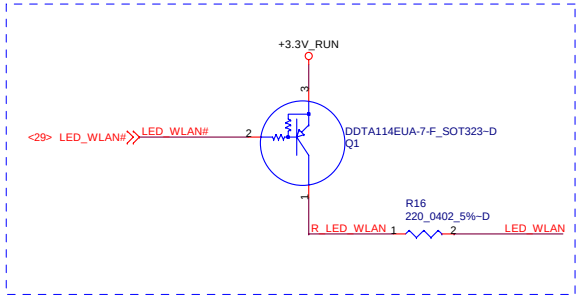


Fiducial Mark

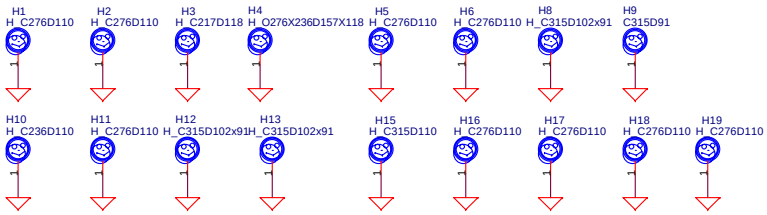


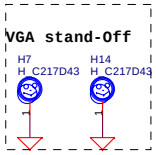






Screw





DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SW LED/B & ME & spare parts

Size | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 35 of 73

CD-ROM IDE BUS

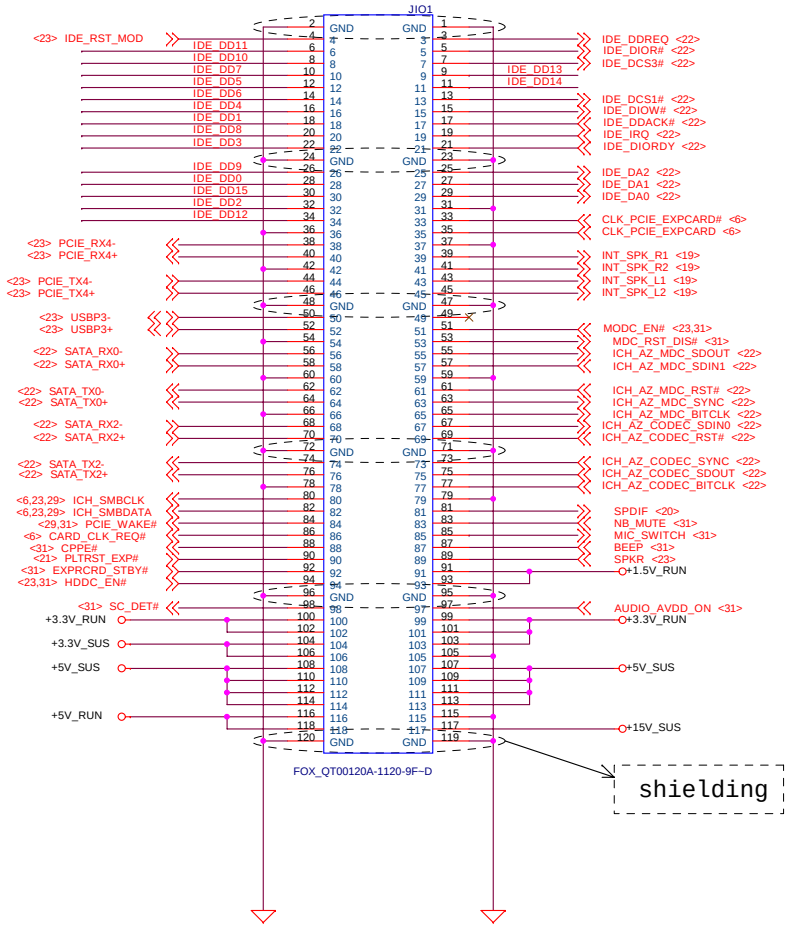
EXPRESS CARD

SATA HDD

SPEAKER

MDC

AC 97



DELL CONFIDENTIAL/PROPRIETARY

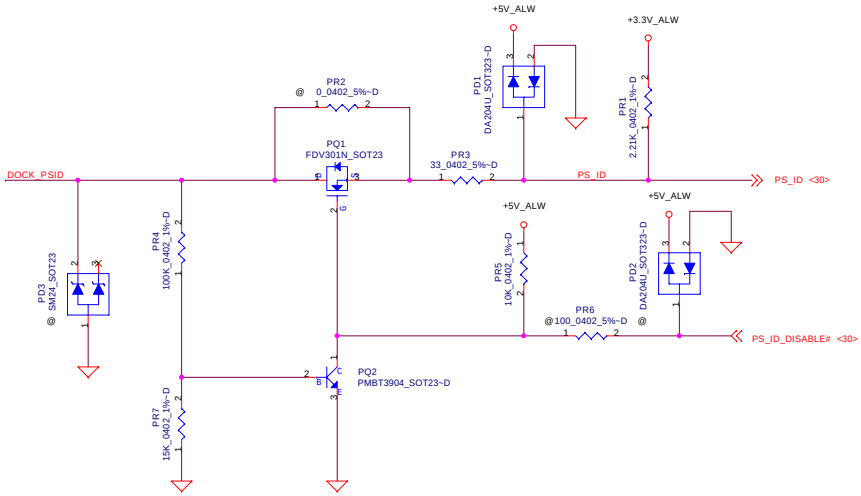
Compal Electronics, Inc.

Title: I/O BOARD DOCKING

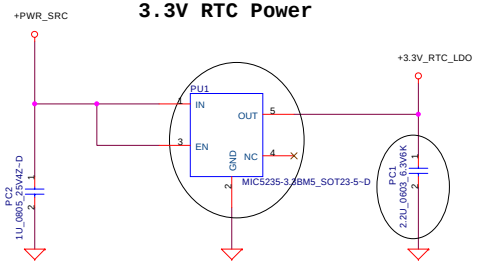
Size | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 36 of 73

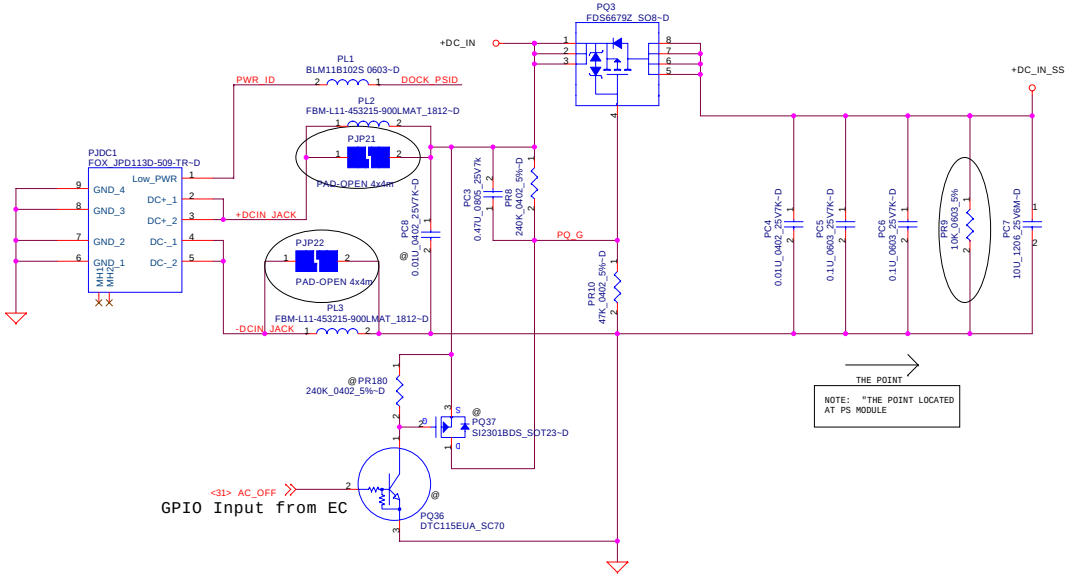
PS_ID Detector



3.3V RTC Power



+DC_IN Source



Compal Electronics, Inc.

Title: +DCIN

Size | Document Number: Bali | Rev: X02

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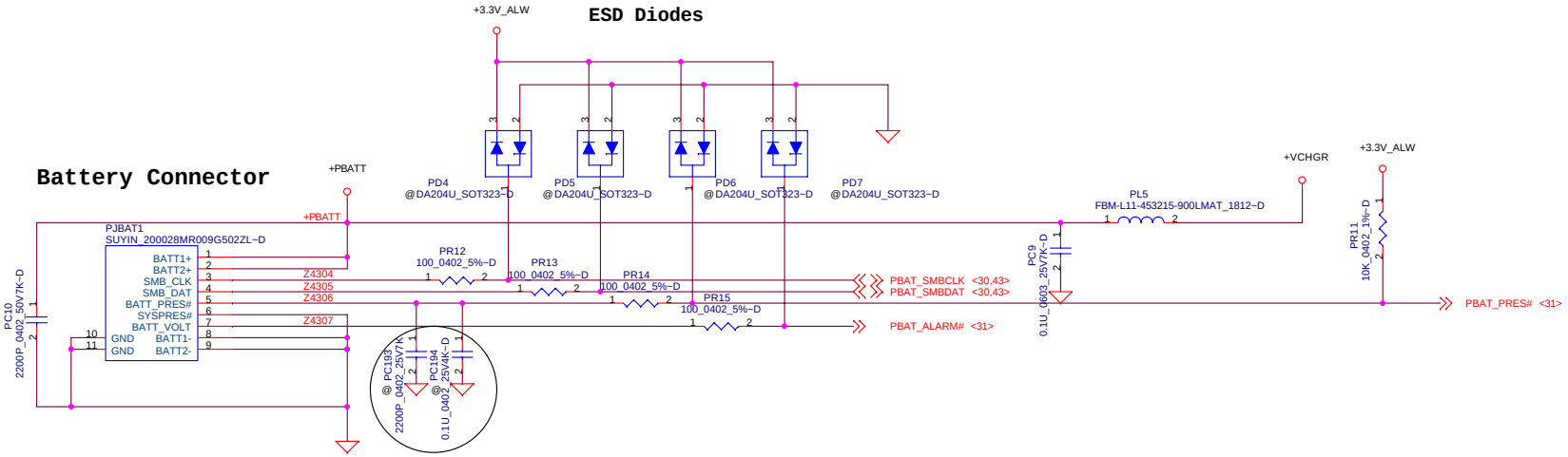
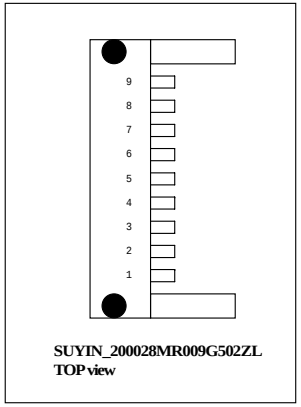
Battery Connector

ESD Diodes





Compal Electronics, Inc.

Title: Battery Conn

Size | Document Number: Bali | Rev: X02

Date: Monday, April 17, 2006 | Sheet 38 of 73

MAX8734 Current Limit Characteristics

	min	typ	max	Tolerance
VLIM=0.5V	40mV	50mV	60mV	20%
VLIM=1.0V	93mV	100m	107mV	7%

Reference COE system power Rev A 04

DC +3V/ +5V/ +15V

5 Volt +/-5%
design current: 4.1A
peak current: 5.8A
Min OCP: 5.9A

3.3 Volt +/-5%
design current: 7A
Max current: 9.9A
Min OCP: 11.5A

Unpop 15V charger bump

Place these CAPs close to FETs

Place these CAPs close to FETs

L-S Rds-on (max) =5.9~7.25m ohms

L-S Rds-on= 16~20m ohm

Output Caps ESR = 25// 25=12.5 m ohms

Enable Skip Mode

+3.3VSRC OCP
Ton=1/300k * Vo/Vin=0.578us
Toff=1/300k - 0.578us = 2.752us
DeltaI=3.3V/2uH * 2.752us = 4.54A
Iimit=(VILM*0.1)/Rds(on)+1/2 DeltaI
VILM=2*100/(100+97.6)=1.01V *0.1=101mV
IC 7% tolerance (min 94mV)(Typ 101mV)(max 108mV)
Iimit=(VILM)/Rds(on)+1/2 Delta I
Iimit Min=94mV//(7.25mOhm*1.4)+1/2 Delta I=11.5A
Iimit Typ=101mV//(5.9mOhm*1.4)+1/2 Delta I=14A
Iimit Max=108mV//(5.9mohm*1.4)+1/2 Delta I=15.3A

+5VSUSP OCP
Ton=1/200k * Vo/Vin=1.316us
Toff=1/200k - 1.316us = 3.684us
DeltaI=5V/4.7uH * 3.684us = 3.92A
Iimit=(VILM*0.1)/Rds(on)+1/2 DeltaI
VILM=2*102/(102+84.5)=1.094V *0.1=109.4mV
IC 7% tolerance (min 101.7mV)(Typ 109.4mV)(max 117mV)
Iimit=(VILM)/Rds(on)+1/2 Delta I
Iimit Min=101.7mV/(20mOhm*1.4)+1/2 Delta I=5.86A
Iimit Typ=109.4mV/(16mOhm*1.4)+1/2 Delta I=6.8A
Iimit Max=117mV//(16mohm*1.4)+1/2 Delta I=7.2A

Compal Electronics, Inc.

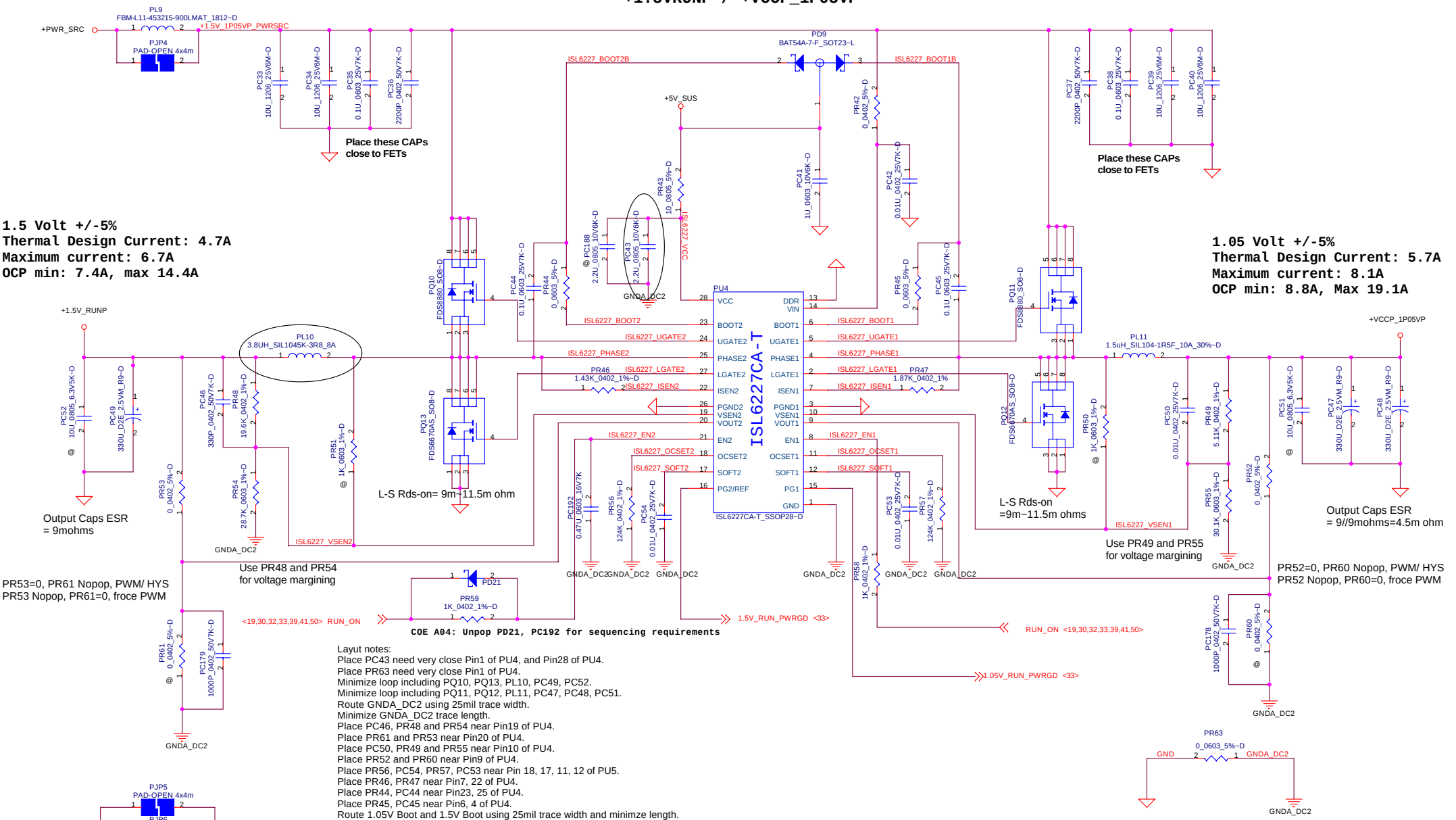
Title: +3.3V/+5V

Size: | Document Number: Bali | Rev: X02

Date: Monday, April 17, 2006 | Sheet 39 of 73

Reference COE 1.05/1.5V ISL6227 Rev A04

+1.5VRUNP / +VCCP_1P05VP



Layut notes:
Place PC43 need very close Pin1 of PU4, and Pin28 of PU4.
Place PR63 need very close Pin1 of PU4.
Minimize loop including PQ10, PQ13, PL10, PC49, PC52.
Minimize loop including PQ11, PQ12, PL11, PC47, PC48, PC51.
Route GNDA_DC2 using 25mil trace width.
Minimize GNDA_DC2 trace length.
Place PC46, PR48 and PR54 near Pin19 of PU4.
Place PR61 and PR53 near Pin20 of PU4.
Place PC50, PR49 and PR55 near Pin10 of PU4.
Place PR52 and PR60 near Pin9 of PU4.
Place PR56, PC54, PR57, PC53 near Pin 18, 17, 11, 12 of PU5.
Place PR46, PR47 near Pin7, 22 of PU4.
Place PR44, PC44 near Pin23, 25 of PU4.
Place PR45, PC45 near Pin6, 4 of PU4.
Route 1.05V Boot and 1.5V Boot using 25mil trace width and minimze length.
Need large copper fill areas to PQ10, PQ11, PQ12 and PQ13 for thermal inprovment.
Minize length of 1.5V phase node and 1.05V phase node.
PC33, PC34,PC35 and PC36 need close Pin5, 6, 7, 8 of PQ10.
PC37, PC38, PC39 and PC40 need close Pin5, 6, 7, 8 of PQ11.
Route +1.5V_1P05VP_PWRSRC using 50 mil trace width and minimize length.
"Route VSEN1 and VSEN2 away from the inductor and switch node.
Sense Vout directly at the output bulk capacitor"

Compal Electronics, Inc.

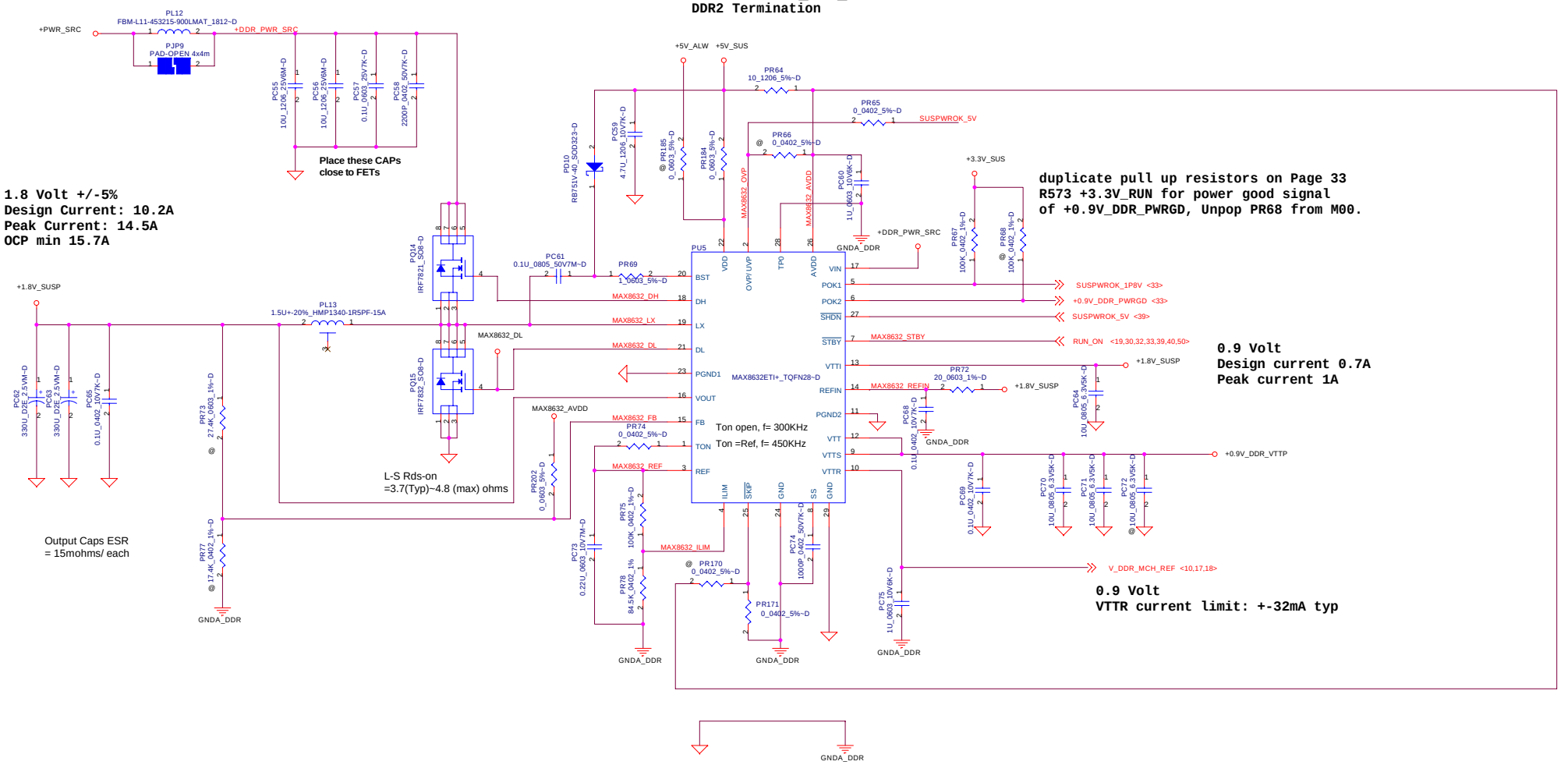
Title: +1.5VRUNP /+VCCP_1P05VP

Size | Document Number: Bali | Rev: X02

Date: Monday, April 17, 2006 | Sheet 40 of 73

Reference Coe Rev. A05

+1.8VSUSP/ +0.9V_DDR_VTT
DDR2 Termination



PJP12
PAD-OPEN 4x4m
PJP13
PAD-OPEN 4x4m
+1.8V_SUSP
+1.8V_SUS
(10A,320mils ,Via NO.=20)

PJP14
+0.9V_DDR_VTTP
PAD-OPEN 4x4m
+0.9V_DDR_VTT
(2A,200mils ,Via NO.=4)

+1.8VSUS OCP

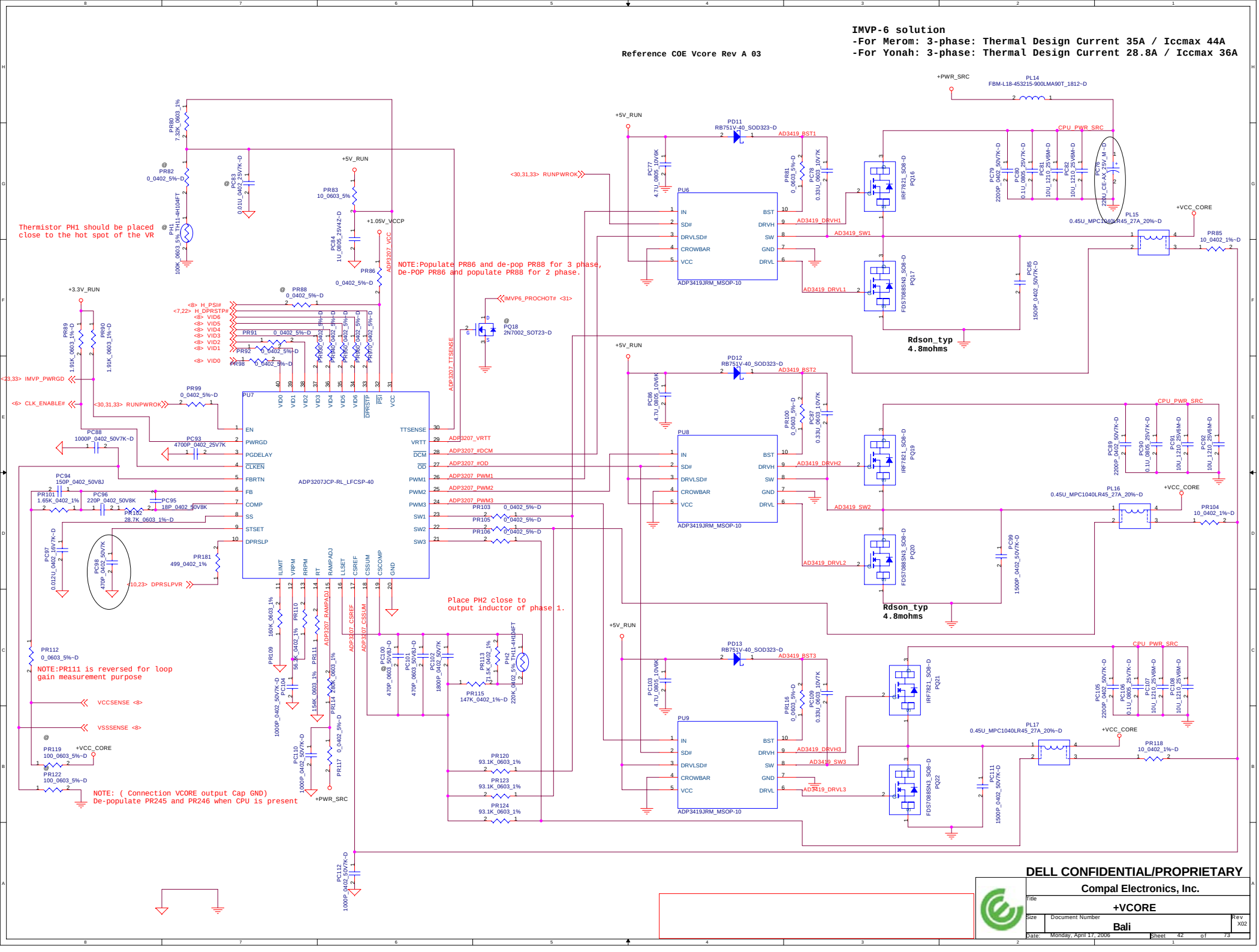
Toff=1/450k (1-1.8/19) = 2.22us
DeltaI=1.8V/1.5uH * 2.22us = 2.66A
Iimit=(VILM*0.1)/Rds(on)+1/2 DeltaI
VILM=2*100/(100+84.5)=1.08V *0.1=108mV
IC 10% tolerance (min 97.2mV)(Typ 108mV)(max 118.8mV)
Iimit=(VILM)/Rds(on)+1/2 Delta I
Iimit Min=97.2mV/(4.8mOhm*1.4)+1/2 Delta I=15.7A

DELL CONFIDENTIAL/PROPRIETARY

Title	+1.8VSUSP/ +0.9V_DDR_VT	
Size	Document Number: Bali	Rev: X02
Date: Monday, April 17, 2006	Sheet 41 of 73	

Reference COE Vcore Rev A 03

IMVP-6 solution
-For Merom: 3-phase: Thermal Design Current 35A / Iccmax 44A
-For Yonah: 3-phase: Thermal Design Current 28.8A / Iccmax 36A



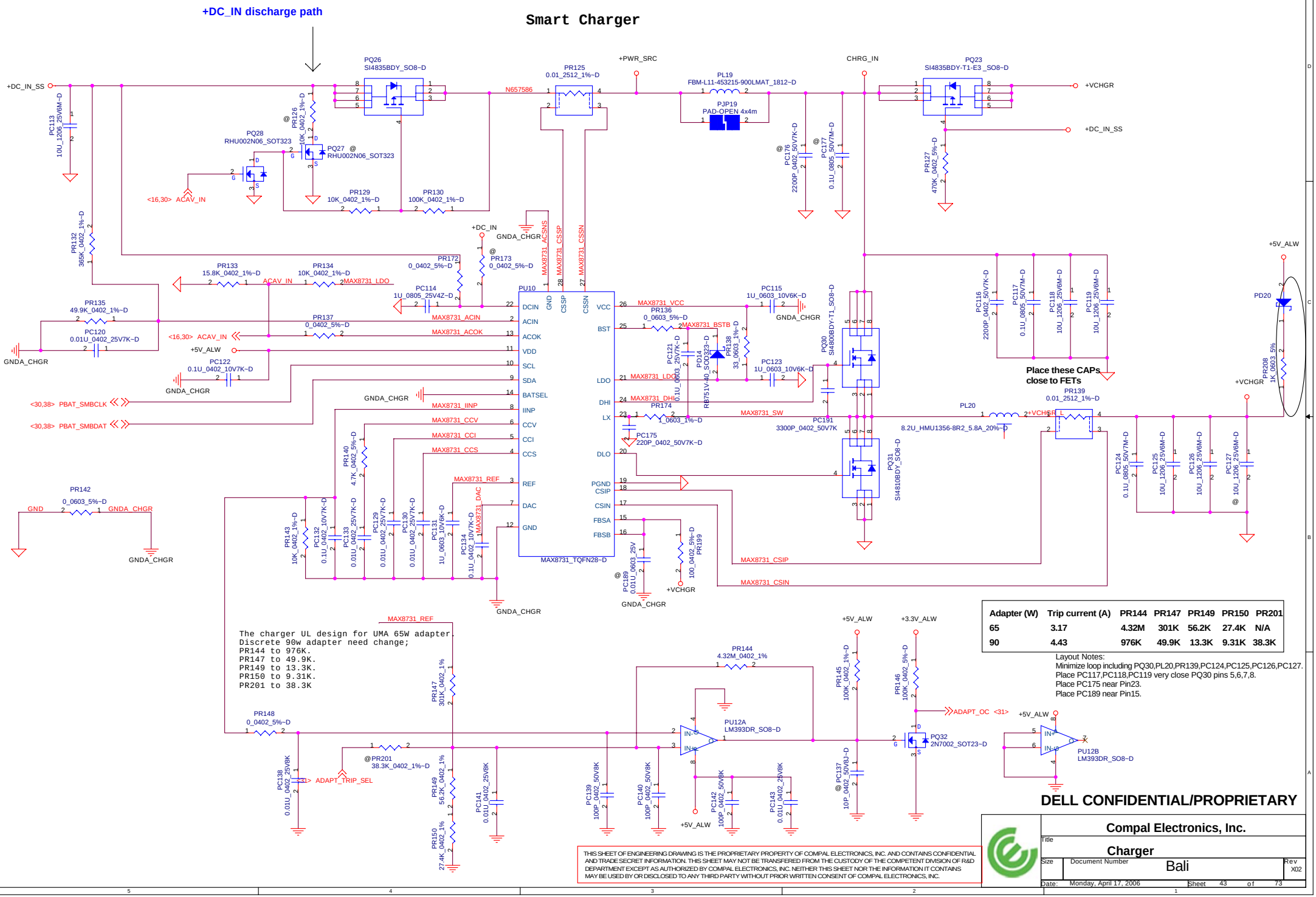
Compal Electronics, Inc.

Title	+VCORE	
Size	Document Number: Bali	Rev: X02
Date: Monday, April 17, 2006	Sheet 42 of 73	

Reference COE charger Rev A 11

Smart Charger

+DC_IN discharge path



Adapter (W)	Trip current (A)	PR144	PR147	PR149	PR150	PR201
65	3.17	4.32M	301K	56.2K	27.4K	N/A
90	4.43	976K	49.9K	13.3K	9.31K	38.3K

The charger UL design for UMA 65W adapter.
Discrete 90w adapter need change;
PR144 to 976K.
PR147 to 49.9K.
PR149 to 13.3K.
PR150 to 9.31K.
PR201 to 38.3K

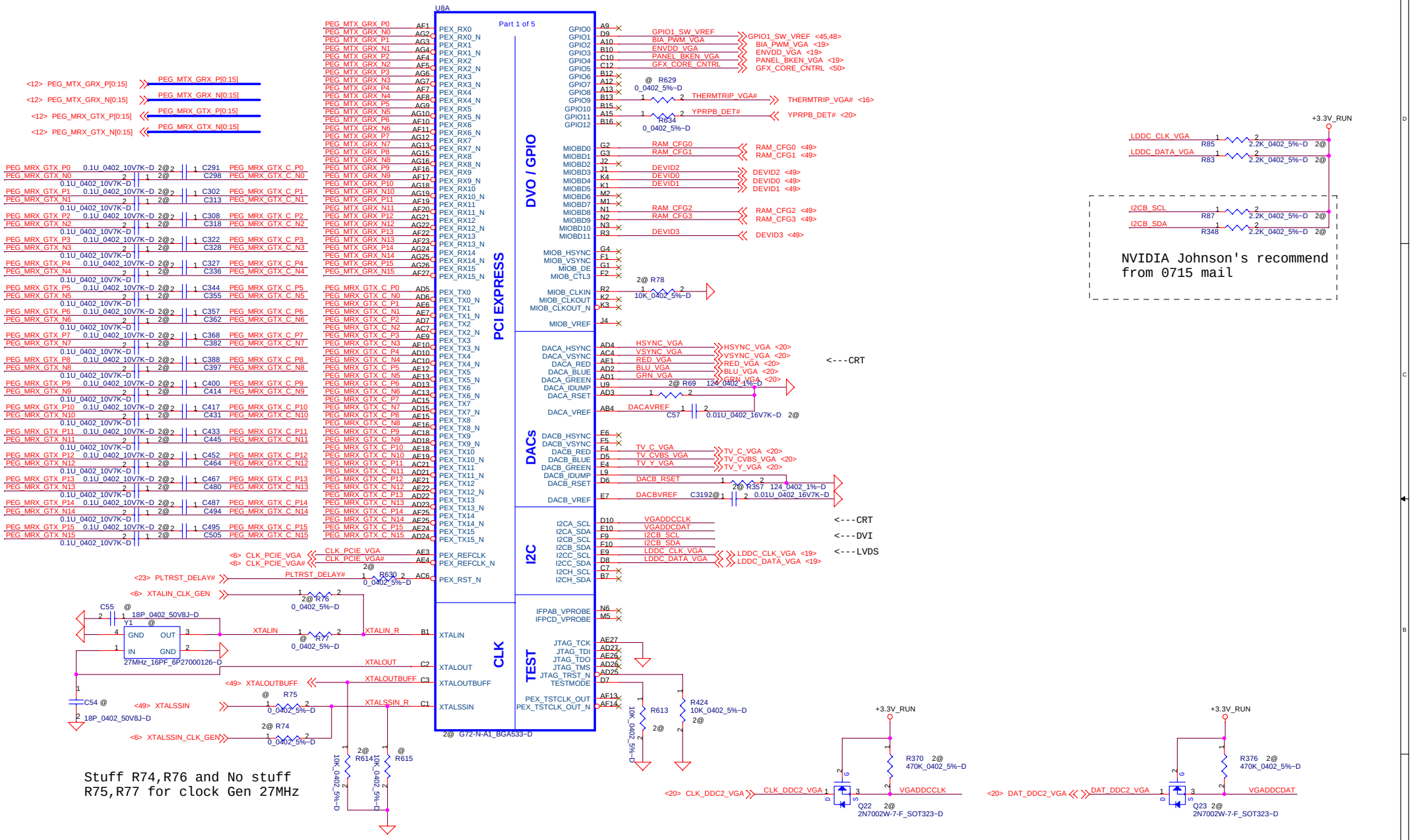
Layout Notes:
Minimize loop including PQ30,PL20,PR139,PC124,PC125,PC126,PC127.
Place PC117,PC118,PC119 very close PQ30 pins 5,6,7,8.
Place PC175 near Pin23.
Place PC189 near Pin15.

Compal Electronics, Inc.

Title: Charger

Size | Document Number: Bali | Rev: X02

Date: Monday, April 17, 2006 | Sheet 43 of 73



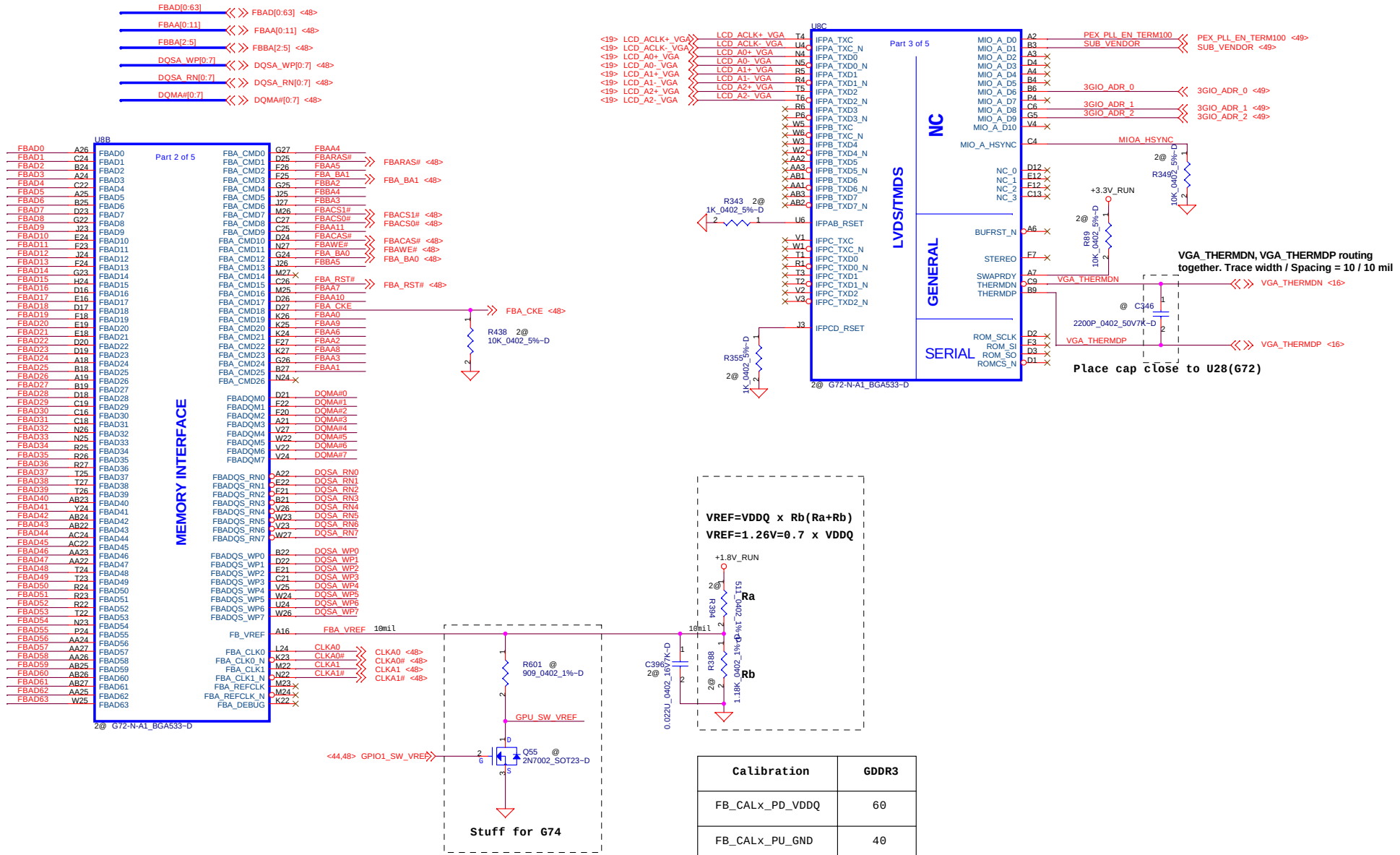
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: NVG72 PCIE,GPIO,CLK

Size: | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 44 of 73



Calibration	GDDR3
FB_CALx_PD_VDDQ	60
FB_CALx_PU_GND	40
FB_CALx_TERM_GND	60
VREF RATIO	0.7xFBVDDQ

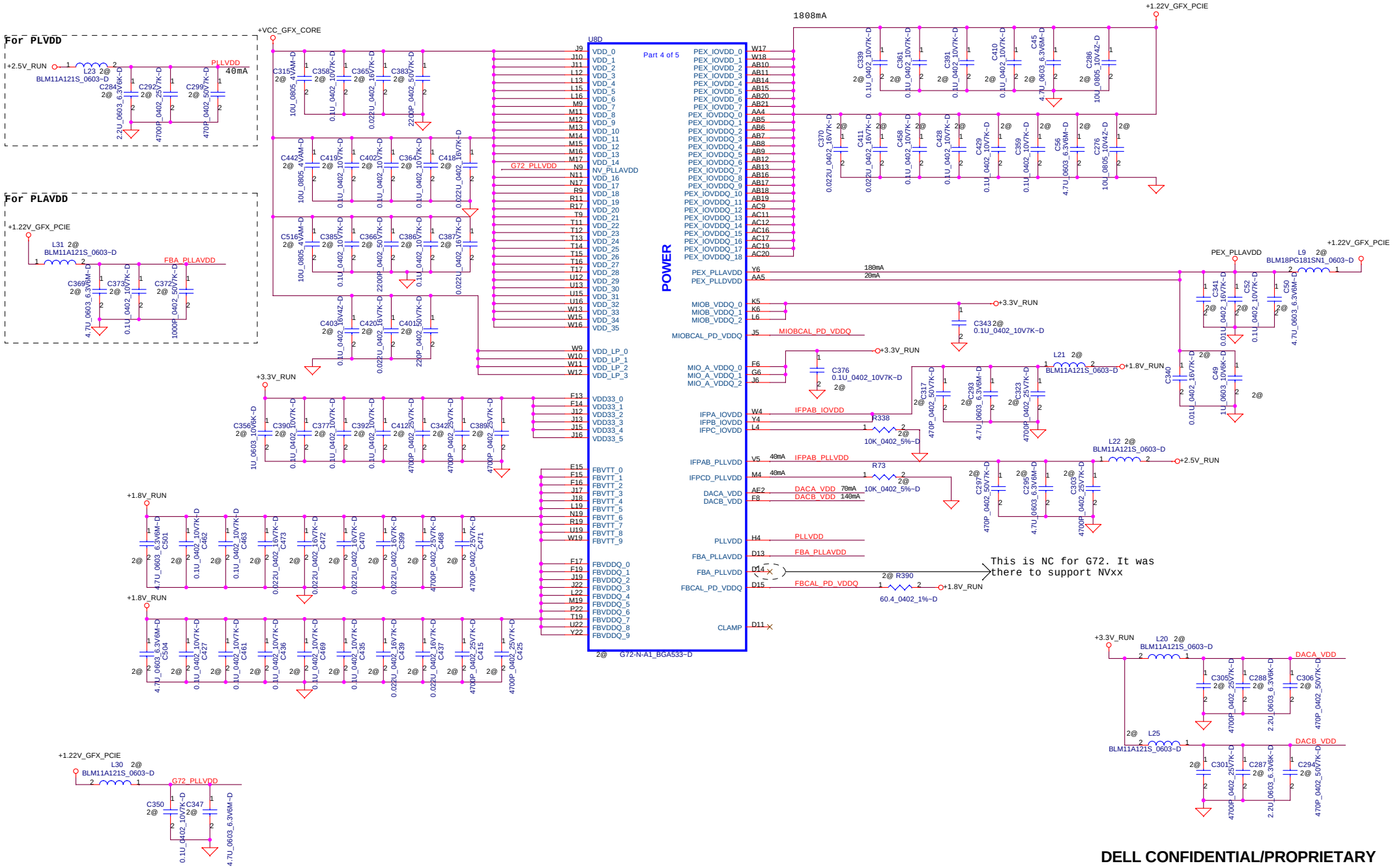
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: NVG72 Memory Interface,LVDS

Size: Document Number: LA-3001P Rev: 0.4

Date: Monday, April 17, 2006 Sheet 45 of 73



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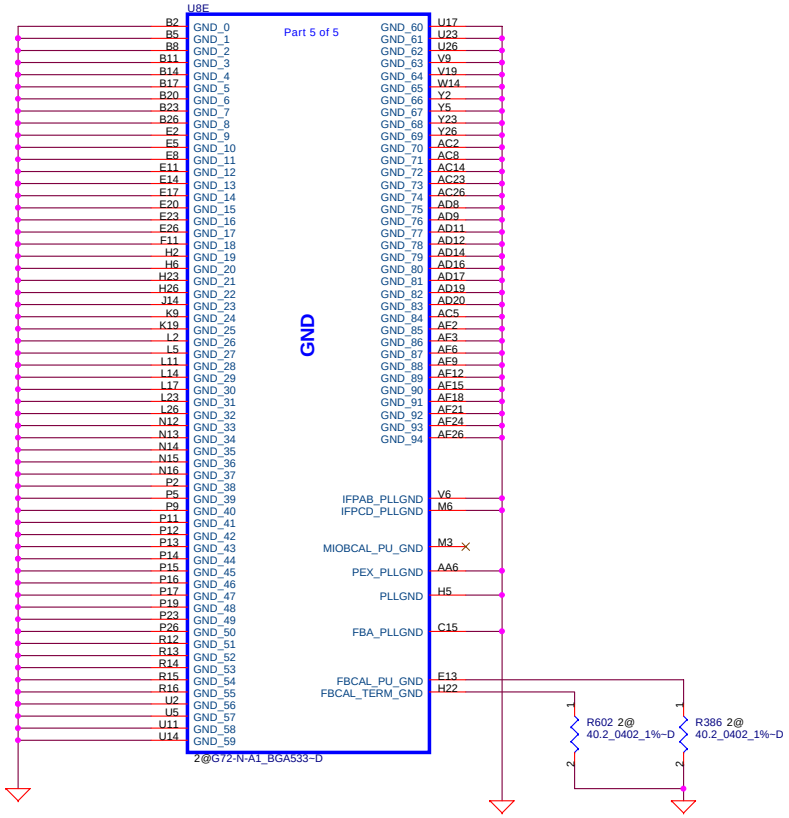
Compal Electronics, Inc.	
Title	NVG72 PWR
Size	Document Number: LA-3001P
Rev	0.4
Date:	Monday, April 17, 2006
Sheet	46 of 73



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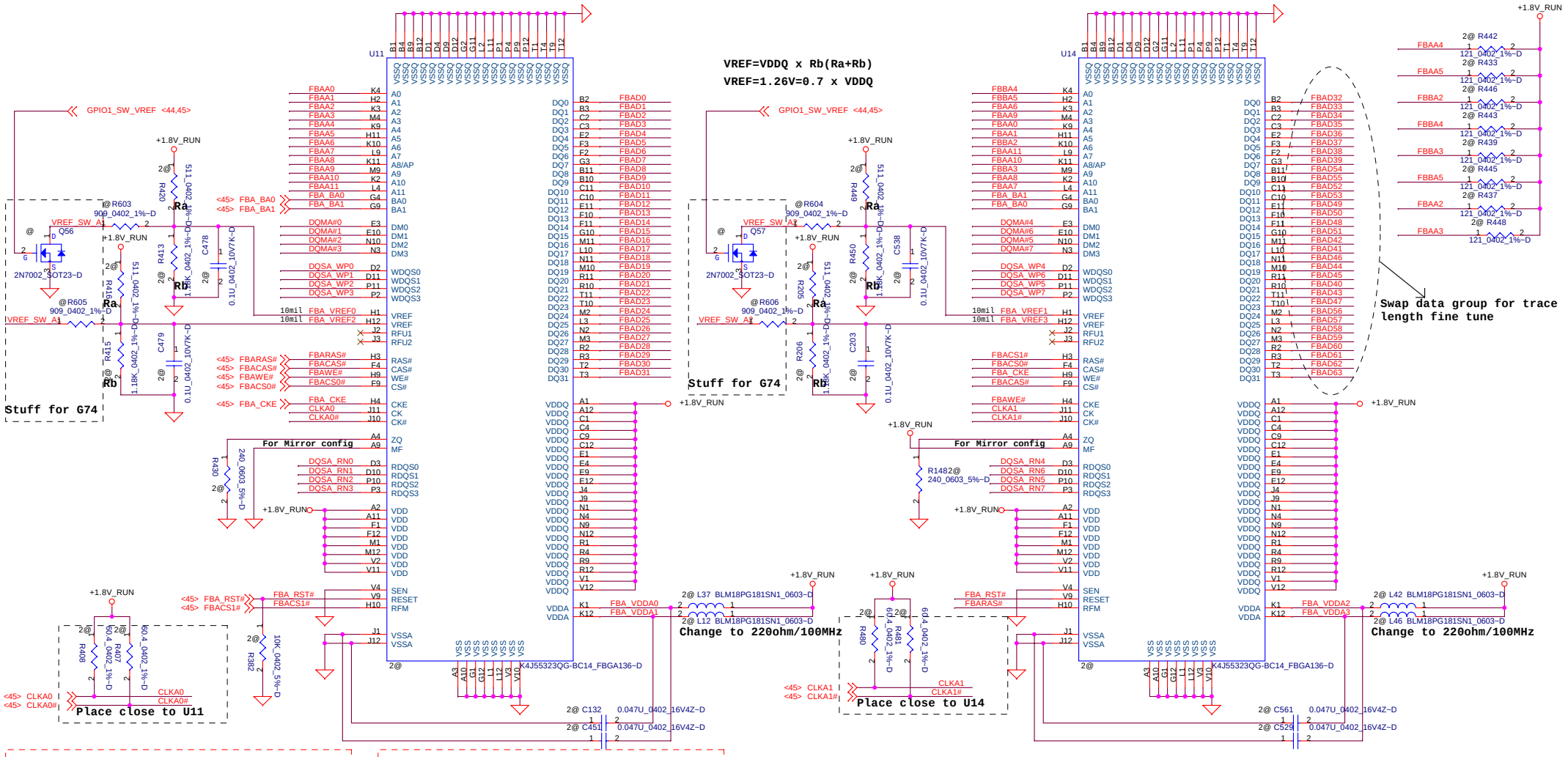
Compal Electronics, Inc.	
Title	NVG72 GND
Size	Document Number: LA-3001P
Rev	0.4
Date:	Monday, April 17, 2006
Sheet	47 of 73



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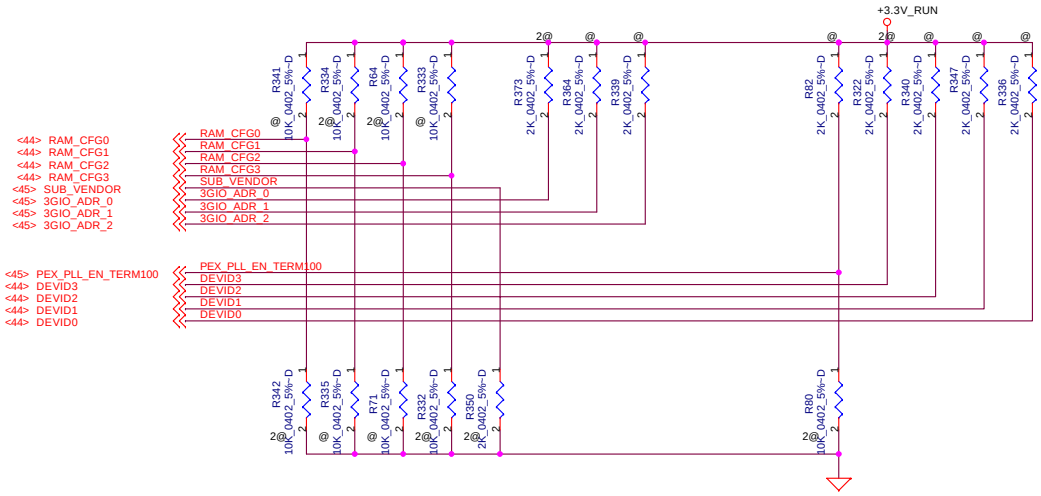
Compal Electronics, Inc.

Title: NVG72 External DDR

Size: | Document Number: LA-3001P | Rev: 0.4

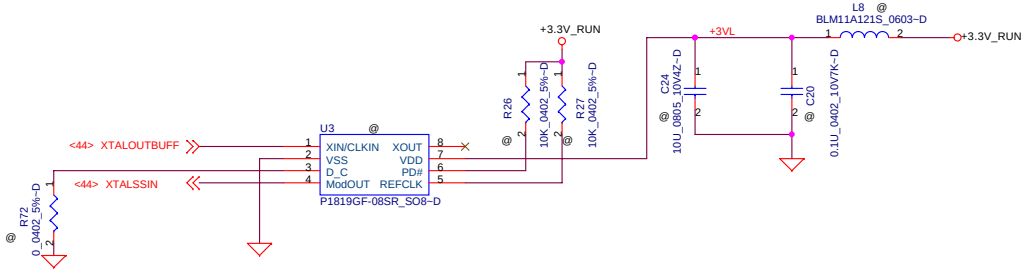
Date: Monday, April 17, 2006 | Sheet 48 of 73



G72xx				
	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1

G72MV STRAPS

STRAPS	PIN	DESCRIPTION		Value
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT, Serial SST45VF=10, LPC=11		01
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)		0
PEX_PLL_TERM	MIOAD0			0
RAM_CFG[3:0]	MIOBD0 MIOBD1 MIOBD8 MIOBD9	For GDDR1	8Mx32 DDR monolithic (64bit) 300MHz, 1.8V	0001
			8Mx32 DDR monolithic (32bit) 300MHz, 1.8V	1001
			8Mx32 DDR (Samsung K4D55323QF-GC) 300MHz, 1.8V	0010
			4Mx32 DDR generic (64bit) 1.8V I/O	0100
			4Mx32 DDR generic (32bit) 1.8V I/O	1100
		For GDDR3	Infineon 8Mx32 500MHz, 1.8V	0101
			Hynix 8Mx32 500MHz, 1.8V	0111
			Samsung 8Mx32 500MHz, 1.8V	0110 *



	U3.Pin3
-1.75% (DOWN)	0 *
±0.875% (CENTER)	1

Internal pull up

DELL CONFIDENTIAL/PROPRIETARY

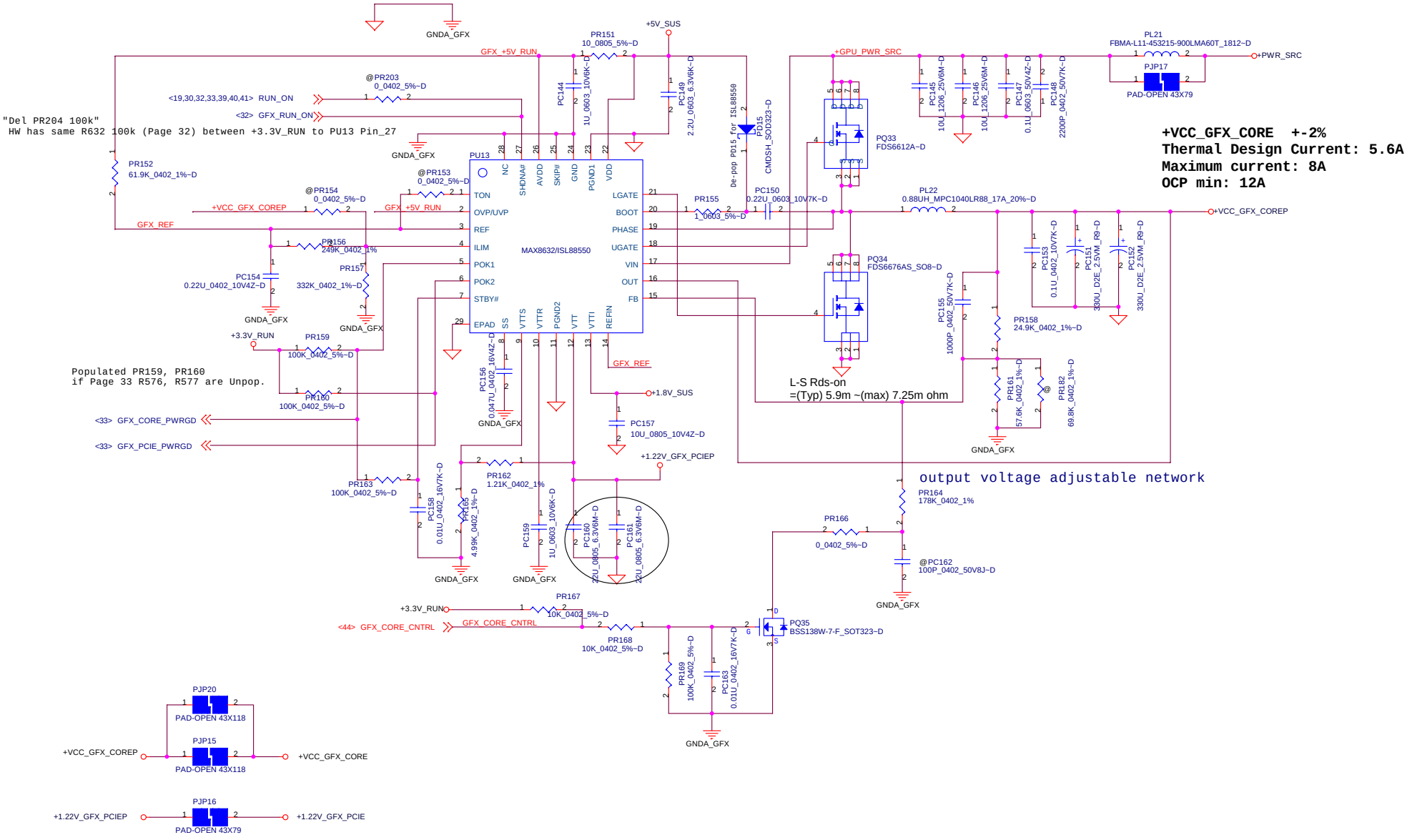
Compal Electronics, Inc.

Title: NVG72 Strapping

Size: | Document Number: LA-3001P | Rev: 0.4

Date: Monday, April 17, 2006 | Sheet 49 of 73

Graphics Power reference COE Rev A08
Graphics Power for HAL31 Discrete only.



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Compal Electronics, Inc.

Title	PWR_NVG72 +VDD_CORE	
Size	Document Number LA-3001P	Rev X02
Date: Monday, April 17, 2006	Sheet 50 of 73	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	ALL	H/W	9/14	Bill	Revision change to X00(0.2)	Modify Done.	0.2
2	31	H/W	9/14	Bill	Update Board ID to 0001 for X00	Stuff R42 and no-stuff R31	0.2
3	31	H/W	9/14	Bill	CoE update. (EC_A05)	Add GPIO USB_CAM_EN# and ADAPT_TRIP_SEL	0.2
4	19	H/W	9/20	Bill	CoE update. (CRT, LVDS, SVIDEO and DVI Interfaces_A06)	Delete U28, R607. Add R610.	0.2
5	20	H/W	9/20	Bill	CoE update. (CRT, LVDS, SVIDEO and DVI Interfaces_A06)	Update Populattion Note for the RGB and TV out Filter.	0.2
6	32	H/W	9/23	Reden	CoE update. (M07 SYSTEM POWER SEQUENCE_A03)	Change R58,R540,R567,R447,R558,R564,R597 to 30_0805_5%	0.2
7	23	H/W	9/28	Reden	Update the ICH7 USB bus connection	Add connection of USB4+/- for CCD, USB2+/- for Blue tooth	0.2
8	ALL	H/W	9/28	Reden	Change Connector for ME request	Update J1394, JTP1, JBT1, JLVDS1 connector	0.2
9	14	H/W	9/30	Reden	Update the note for MCH power	Remove the placement note for C489,C525 as COE schematic	0.2
10	22	H/W	9/30	Scott	Pull-up on SATA_ACT# (R530) should be populated	Modify OK	0.2
11	22	H/W	9/30	Scott	Capacitor on THRMTRIP_ICH# (C609) can be de-populated	Modify OK	0.2
12	23	H/W	9/30	Scott	Rename net LCM_SMB_CLK to ICH_SMLINK0	Modify OK	0.2
13	23	H/W	9/30	Scott	Rename net LCM_SMB_DAT to ICH_SMLINK1	Modify OK	0.2
14	29	H/W	9/30	B.McFarland	Can remove R489 and R490. Leave pins 3 and 5 as NC on JMINI1. See A06 Ref Schem.	Modify OK	0.2
15	20	H/W	9/30	John Lerma	Please check the latest reference schematics. Delete 75 ohm resistors on RED, GREEN, & BLUE. Add 39 ohms series resistors to ouputs of U1 & U2. Move L3 & L4 before caps C1 & C2.	Delete R233, R235, R238, Add R611, R612 (39 Ohm). And move L3 & L4 before caps C1 & C2.	0.2
16	20	H/W	9/30	John Lerma	Please check the latest reference schematics. Delete 75 ohm resistors on TV_C, TV_CVBS, & TV_Y. Filter circuit values have been changes and a cap in parallel with each inductor has been added.	Remove R368, R380, R385.	0.2
17	33	H/W	9/30	John Lerma	Add diode for power leakage in power sequence circuit	Change R129,R482,R466 to 100K,and change Q6,Q30,Q27 to 2N3906,and change R471,R474,R469 to 4.7K.	0.2
18	23	H/W	9/30	Reden	No stuff R485 (10k pull high) for M'07 inverter	Modify OK	0.2
19	47	H/W	9/30	Reden	Change pull down resistor value to follow COW schematic	Change R602,R386 to 37.4_0402_1%	0.2
20	20	H/W	10/04	Reden	Change S-video filter bead same as COE schematic	Change L29,L32,L34 to 0.47UH_CIL10NR47KNC_10%_0603	0.2

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	H/W	10/05	John	Swap CLKREQ signal between WWAN and WLAN	Modify ok.	0.2
2	27	H/W	10/05	John	Change C236,C238 from 1000p to 300p	Modify ok.	0.2
3	29	H/W	10/05	John	Add debug signals to WLAN connector	Connecting JMINI2 pins 16 - HOST_DEBUG_TX, 17 - HOST_DEBUG_RX, 19 - 8051_TX & 42 - 8051_RX.	0.2
4	32	H/W	10/05	John	Remove C682 and replace C685 with 4700pF as COE schematic	Modify ok.	0.2
5	44	H/W	10/05	John	Add signal THERMTRIP_VGA# to G72 pin B13 from Guardian II	Modify ok.	0.2
6	49	H/W	10/05	John	Change R341, R334, R64, & R333 from 2K to 10K	Modify ok.	0.2
7	20	H/W	10/05	John	Change Caps C331,C325,C351,C349,C381,& C379 from 82pF to 47pF and add C705~C707	Modify ok.	0.2
8	44	H/W	10/05	John	Add 10K pull-down resistor to G72 pins C3, C1, & D7	Modify ok.	0.2
9	31	H/W	10/06	Reden	Add signal U18 pin5 (GPIOE4) connect to TP connector for LED.	Modify ok.	0.2
10	44	H/W	11/02	John	Add 150ohm terminal resistor on GFx side.	Add 150ohm of R619~R624	0.3
11	22	H/W	11/02	Reden	Add SNIFFER LED Disable Circuit as COE schematic	Add Q58,R625	0.3
12	30	H/W	11/02	Reden	Added 0 ohm to EC5004 test pin	Modify ok.	0.3
13	29	H/W	11/02	Reden	Added circuit to support WoW from S3/S4. Blocking diode and bypass resistor as COE	Modify ok.	0.3
14	35	H/W	11/02	Reden	Added a circuit (Transistor and Resistors) to keep BT LED off when the SNIFFER is turned on	Modify ok.	0.3
15	44	H/W	11/02	Reden	Change pull up resistor same as COE graphic schematic.	Change R370,R376 from 4.7K to 470K.	0.3
16	20	H/W	11/17	Reden	Change VCC_CRT Diode D11 to RB500 (rate Io=100mA).	Modify ok.	0.3
17	44	**H/W**	11/17	Reden	Add series resistor on signal of PLTRST_DELAY#.	Modify ok.	0.3
18	44	H/W	11/17	Reden	Add series resistor on signal of THERMTRIP_VGA#.	Modify ok.	0.3
19 20	33	H/W	11/18	Reden	Change Q6,Q27,Q30 to MMBT3906, and delete D19~D21(RB751V_SOD323~D) same as COE schematic.	Modify ok.	0.3
21 23	32	H/W	11/18	Reden	Added 3VRUN Delay RC CKT, to Fix IMVP_PWRGD Glitch issue and add 1.8 VRUN Delay RC CKT, to meet GFX Power Sequence Requirement	Modify ok.	0.3
24	32	H/W	11/18	Reden	Added Diode Bleed off for 3VRUN and 1.8VRUN for GFX Power Down Sequence adjustment.	Modify ok.	0.3
25	32	**H/W**	11/21	Reden	Change the GFX_RUN_ON connection to VR turn on pin as COE A06 version schematic.	Modify ok.	0.3
26	20	H/W	11/23	John	Change U19 connection from EC to GND as GG list request.	Modify ok.	0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	H/W	11/23	John	Change JTP1 pin 19 from +5V_ALW to +5V_RUN as Dell GG list	Modify ok.	0.3
2	20	H/W	11/23	John	Place a 0 ohm 1206 place holder between D11 pin 1 and JCRT1 pin 9	Modify ok.	0.3
3	29	H/W	11/23	John	Change WWAN USB source from EC to ICH7M/USB5 and remove WWLAN USB signal from EC.	Modify ok.	0.3
4	44	H/W	11/24	John	Add connection for signal of YPRPB_DET# to G72 pin A15 through a series resistor.	Modify ok.	0.3
5	44	H/W	12/01	John	Change R615 to no-pop	Modify ok.	0.3
6	23/31	H/W	12/02	John	Add connection to EC for signal HDDC_EN# and MODC_EN#	Modify ok.	0.3
7	6	H/W	12/06	Reden	Change R456 to 150, R457 to 91 for internal spectrum clock.	Modify ok.	0.3
8	20	H/W	12/07	John	Add a diode for U1,U2 power pin.	Modify ok.	0.3
9	20	H/W	12/07	John	Add a cap 0.1uf for JSVID1 pin5	Modify ok.	0.3
10	28	H/W	12/07	John	Change u13 to G5240B1T1U	Modify ok.	0.3
11	30	H/W	12/07	John	Add connection for pin73 for LVDS BIA_PWM through resistor	Modify ok.	0.3
12	20	H/W	12/08	John	Remove the C104 form dell COE team request.	Modify ok.	0.3
13	6/44/49	H/W	12/12	Reden	Remove external spectrum and swap populated resistor for internal CLK GEN.	Modify ok.	0.3
14	31	H/W	12/12	John	Add pull up resistors to +3.3V_ALW for signals of HDDC_EN#,MDDC_EN#	Modify ok.	0.3
15	23/30	H/W	12/13	John	Add damping series resistors (47ohm) for signal SPI_CS# on EC and ICH7	Modify ok.	0.3
16	33	H/W	12/13	John	Removed 3V/5V power good sequence circuit and change +1.8V_RUN PWRGD circuit.	Modify ok.	0.3
17	35	H/W	12/14	Reden	Swap the Sniffer LED (D13) pin define, Pin3=>Yellow, Pin2=>Green.	Modify ok.	0.3
18	9	H/W	12/14	Reden	Change CPU VCORE area caps , 22uF->10uF and replace 330uF poly with 6m ohm x 4pcs.	Modify ok.	0.3
19	31	H/W	12/15	Reden	Change pull up resistors of HDDC_EN#,MDDC_EN# from 10k to 100K for leakage issue.	Modify ok.	0.3
20	49	H/W	12/15	Reden	Change Device ID from 0111 to 1000 for G72M	Modify ok.	0.3
21	32	H/W	2006/2/07	Reden	Change C154 from 0.01uf to 0.047uf to match G72 VDD_CORE&1.8V power up sequence	Modify ok.	0.4
23	13	H/W	2006/2/07	Reden	Change L6/L26 TDK to 2nd and use Taiyo for main source	Modify ok.	0.4
24	24	H/W	2006/2/07	Reden	Change L53 TDK to 2nd and use Taiyo for main source	Modify ok.	0.4
25	20	H/W	2006/2/08	Reden	Change TV filter caps valus as dell's suggest 1. Change C331,C351,C381,C325,C349,C378 from 47pf to 82pf 2. Change C705,C706,C707 from 22pf to 8.2pf	Modify ok.	0.4

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	35	H/W	02/17	Reden	To add logic circuit to control 3.3V_RUN for power switch board.	Modify ok.	0.4
2	35	H/W	02/17	Reden	Add pull down resistor (10K) for signal PLTRST_DELAY# to fix leakage issue	Modify ok.	0.4
3	19	H/W	02/21	Reden	Add SI3457DV P channel mos to dual-stuff for +GFX_PWR_SRC	Modify ok.	0.4
4	31	H/W	02/21	Reden	Change board ID to X02 (0011)	Modify ok.	0.4
5	19	H/W	02/21	Reden	Add voltage drop diode for CMOS power (+5V_RUN), and remove D'05 buffer.	Modify ok.	0.4
6	22,23,34	H/W	02/21	Reden	populate the 48MHz/bit_clk/keyboard signal termination for EMI issue	Modify ok.	0.4
7	19	H/W	02/21	Reden	Change population option for BACKLITEON,stuff R610 for DSC and stuff R639 for UMA.	Modify ok.	0.4
8	20	H/W	02/21	Reden	Change R611,R612 resister to 0 for signal quality.	Modify ok.	0.4
9	23	H/W	02/22	Reden	Stuff R485 for Bits issue WI52653	Modify ok.	0.4
10 11	16	H/W	02/22	Reden	Change thermal setpoint from 85 degrees to 88 degrees, change R242 from 147K ohm to 322K ohm 1% and R247 from 41.2K ohm to 118K ohm 1%.	Modify ok.	0.4
12	19	H/W	02/28	Reden	Add R652 overlap on D26 for CMOS power pop option	Modify ok.	0.4
13	31	H/W	04/03	Reden	Change board ID to X03 (0100)	Modify ok.	0.5
14	16	H/W	04/11	Reden	Switch Q7,Q24 Pin S,D connection	Modify ok.	0.5
15		H/W				Modify ok.	0.5
16		H/W				Modify ok.	0.5
17		H/W				Modify ok.	0.5
18		H/W				Modify ok.	0.5
19		H/W				Modify ok.	0.5
20		H/W				Modify ok.	0.5
21		H/W				Modify ok.	0.5
23		H/W				Modify ok.	0.5
24		H/W				Modify ok.	0.5
25		H/W				Modify ok.	0.5
26		H/W					

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P39	+3.3VALW	0926/2005	Dell	Dell request to change PC30 from 4.7U_1206 to 10U_1206	PC30 change to 10U_1206_10V	X00
2	P40	+1.5V / +1.05V OCP	0926/2005	Dell	+1.5V OCP min = 7.4A, +1.05V OCP min = 9.3A	1.) +1.5V OCP: PR56 change to 124K, PR46 change to 1.43K 2.) +1.05V OCP: PR57 change to 124K, PR47 change to 1.87K	X00
3	P41	+1.8V_SUS	0926/2005	Dell	Contact the FB pin of the controller to the AVDD pin via zero ohm resister	Add PR202 0 ohm 0603 between FB pin with AVDD pin of PU5 MAX8632	X00
4	P39	+15V_SUS	0926/2005	Compal	Follows COE +15V reference schematics	Unpop PR179 10K_0805	X00
5	P50	+VCC_GFX	0926/2005	Compal	Improve +1.22V_GFX_PCIEP pin7 STBY# and pin5 POK1 pull high resister of PU13 MAX8632.	Depop PR159, PR160 100K_0402	X00
6	P40	+1.5V / +1.05V	1004/2005	Dell	Improve better phase margin	PC46 change to 330pf/0402/50v	X00
7	P41	+1.8V_SUSP OCP	1004/2005	Dell	Improve 1.8V_SUSP OCP	PR78 change to 84.5K	X00
8	P39	+3.3VALW	1004/2005	Dell	Dell request to populate PC11 at the input to the 3V requlator	Populate PC11 10uf/1206/25V	X00
9	P50	+VCC_GFX	1007/2005	Dell	Dell request to Change PR167 pin 1 contact to +3.3V_RUN	PR167 pin1 contact to +3.3V_RUN	X00
10	P50 P41	+VCC_GFX +1.8V_SUSP	1007/2005	Dell	MAX8632 Just connect pin 24 directly to the exposed pad without using zero ohm resistor .	DEL PR186 and PR79	X00
12	P41	+1.8V_SUSP	1007/2005	Dell	Dell request to populate PR74. (PU5 MAX8632 f from 300K change to 450khz)	Add PR74	X00
13	P43	Charger	1007/2005	Dell	Dell request to change PR174 to 1_0603.	PR174 from 1_0805 change to 1_0603(refer to COE Rev A09)	X00
14							
15	P41	+1.8V_SUSP	1107/2005	Dell	Dell Coe DDR Rev A05 request to del PR70	DEL PR70 Change PR69 from 0 ohm to 1 ohm.	X01
16	P43	Charger	1107/2005	Dell	Dell Coe Cgarger Rev A07 requested	1. Change PR174 from 0_0805 to 1_0603. 2. Add PC175 220P_0402 3. Del PR200, Add PR199 100_0402, PC189 0.01U_0603 PU10 Pin 15 & Pin16 shorted. 4. Add PR144 4.3M 0402. 5. Del PR201. 6. Change PR149 from 59K to 56.2K 0402 7. Change PR150 from 33.2K to 27.4K 0402.	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
17	P50	+VDD_CORE	1108/2005	Dell	Dell COE Graphics Power reference A07 requested	1. Change PR155 to 1 ohm. 2. Change PR161 from 69.8K to 57.6K. 3. Change PR164 from 118K to 178K. 4. Change PR166 from 301 to 0 ohm. 5. Change PR162 from 1.1K to 1.21K 6. All +5V_RUN change to +5V_SUS. 7. All +3V_RUN change to +3V_SUS.	X01
18	P50	+VDD_CORE	1108/2005	Dell	Follow Coe ref De-pop PR203. Del PR204, H/W has same R632 100k on Page 32 between +3.3V_RUN to PU13 Pin_27.	Del PR203 Del PR204	X01
19	P37	+DC_IN	1202/2005	Dell	Add solder jumper pads in parallel with PL2 & PL3.	Add PJP21, PJP22	X01
20	P43	Charger	1120/2005	Dell	Dell COE Charger reference A09 requested	De pop PC189 Add PC191	X01
21	P42	+VCC_CORE	1120/2005	Compal	Improve VCC-CORE OCP to 55A. (original design X00 PR109 191K OCP point 45A only.)	Change PR109 to 160K	X01
22	P37 P38 P39 P40 P41 P42 P43 P50	EMI Bead	1122/2005	Compal	Change Footprint 'L_1812' to "L-1812-S" for 2nd source	Change PL2, PL5, PL6, PL9, PL12, PL14, PL19, PL21 footprint to L_1812-S for 2nd source	X01
23	P39	3.3VSRC	1124/2005	Dell	Nopop PQ39 since this will not be needed once the EC HUB is removed.	Unpop PQ39	X01
24	P42	+VCC_CORE	1130/2005	Compal	Tokin inductor 0.45uH/27A rusted on surface after storage test.	change PL15, PL16, PL17 to Panasonic ETQP4LR45XFC (0.45uH 10% Lead Free)	X01
25	P50	+VDD_CORE	1201/2005	Dell	Improve +3.3V_RUN leakage at S3 mode	1. Change PR167 Pin_1 net name from +3.3V_SUS change to +3.3V_RUN 2. Change PR159, PR160 Pin_1 net name from +3.3V_SUS change to +3.3V_RUN	X01
26	P43	Charger	1201/2005	Dell	CoE Charger Ref A10 request: Deeply discharged battery problem.	Add PR208, PD20	X01
27	P50	+VDD_CORE	1202/2005	Dell	Change PR167 to 4.7K to fix stair step issue seen on signal.	Change PR167 to 4.7K	X01
28	P40	+1.5V_RUN	1202/2005	Dell	Add PC192 0.1uF cap to pin 21 of PU4 for power-up sequencing. Also add PD20 diode in parallel with PR59 for power-down sequencing.	Add PC192, PD21	X01
29	P37	DC_IN	1206/2005	Dell	ChangePR9 from 4.7K to 10K. The exising 4.7K exceeds power dissipation rating of 0603 size at 20V.	Change PR9 from 4.7K to 10K	X01
30	P43	Charger	1206/2005	Dell	Unpop PQ27, PR126	Unpop PQ27, PR126	X01
31	P44	+15VP	1206/2005	Dell	Add a PR209 150 ohm between PD19 Pin_3 and PD18 Pin_2 to prevent +15V_SUSP short cause PD18 damage.	Add PR209 150 ohm	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	
32	P49	+VDD_CORE	1207/2005	Dell	Dell require to update.	Change PC98 from 680PF to 390PF	X01
33	P38 P40	Battery Conn +1.5VRUNP/+VCCP_1P05VP	1212/2005	Dell	Dell require to update.	1.Add 2200pF_0402 and 0.1uF_0402 unpop Cap at PJBAT1 pin 5 to GND. 2.Change PC192 from 0.1U to 0.47 uF. 3.Pop PC48.	X01
34	P39	+15V_CHAGRE PUMP	0215/2006	Dell	Dell require to update.	Unpop all 15v charge pump components 1.PU15 AND Gate change to SN74LVC1G08 (+-32mA) 2.Iccrease cap value PC190 at the AND gate Vcc from 0.1uf to 0.47uf. 3. Change PR209 to 0 ohm (There are already 100k resister for protection against excessive short current.) 4. Add new PR210 7.5k in series with AND Gate input to PWM path from U20. 5. Change out gate resister PR207 from 300 ohm to 120 ohm.	X02
35	P42	+VCC_CORE	0223/2006	Compal	Acoustic noise concern	Populate PC76 220uF AL Cap	X02
36	P39	+5V_SUSP	0215/2006	Compal	Power components PL8 interfere with log low	PL8 from 4.7u_STQB125A-4722PF 8A (5.7mm) change to STQB1250-4722APF 7A (5mm).	X02
37	P40	+1.5V_RUNP	0215/2006	Dell	Power components PL10 interfere with log low (pad short risk)	PL10 change to SIL1045K-3R8-R 8A	X02
38		+VCC_CORE	0407/2006	Dell	Acoustic noise concern	PC98 from 390pf change to 470pf	X02
39	P42	+VCC_CORE	0412/2006	Dell	Dell require to depoplation.	Depop PR119 and PR122	