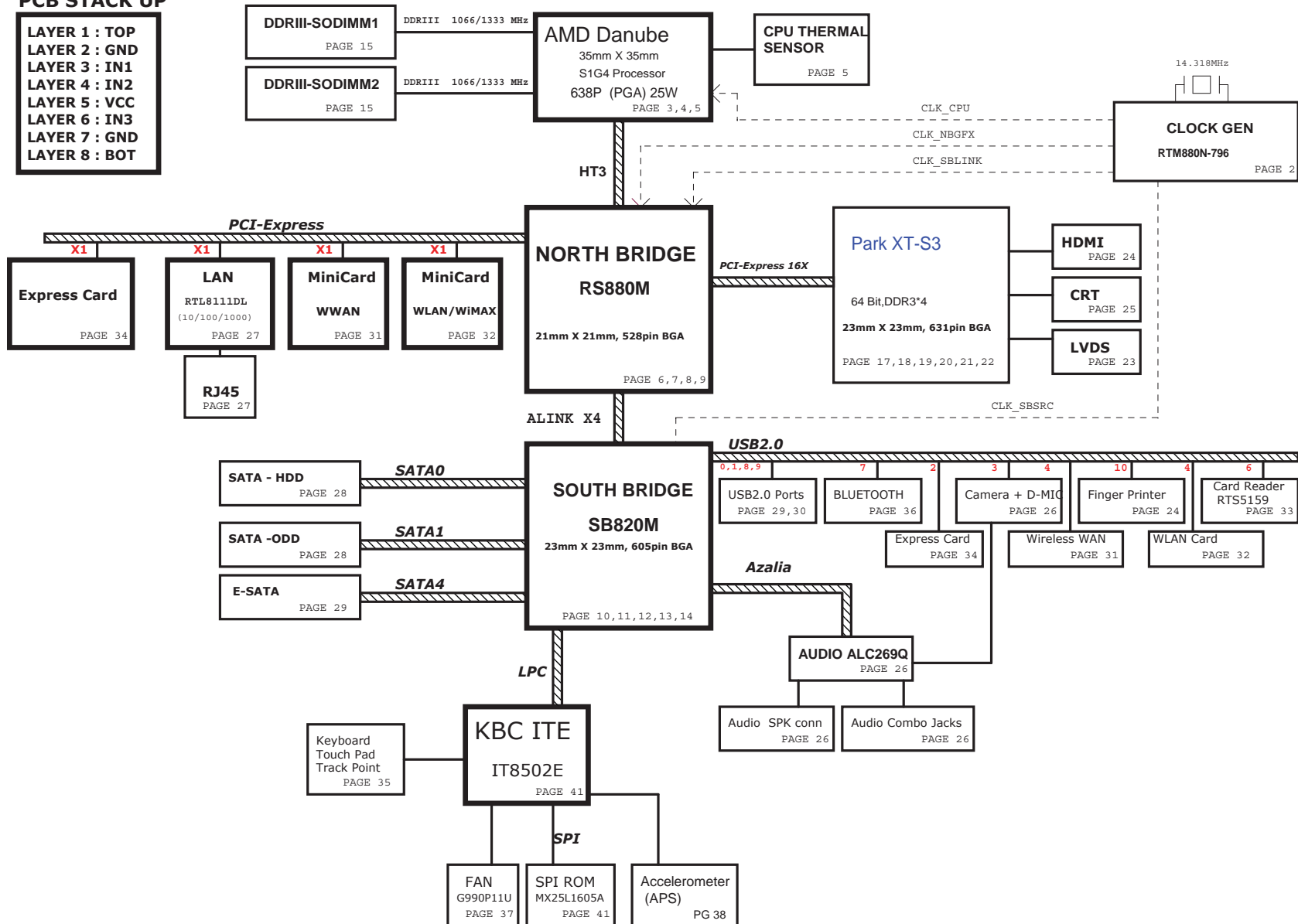
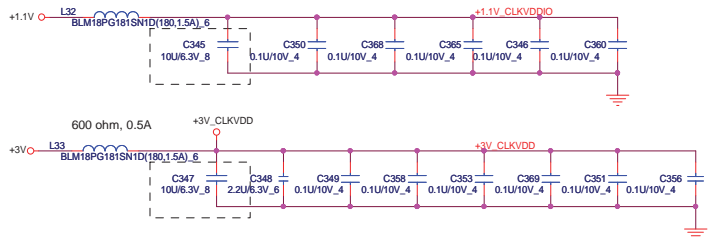


LD-Note Block Diagram -- AMD Danube

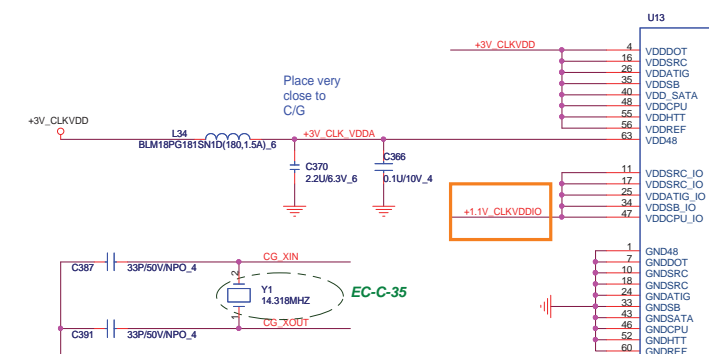
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

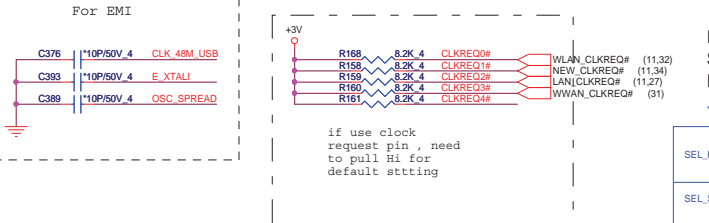
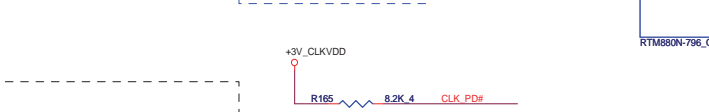
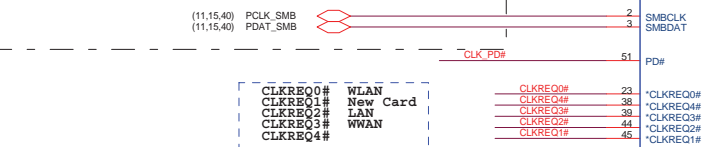




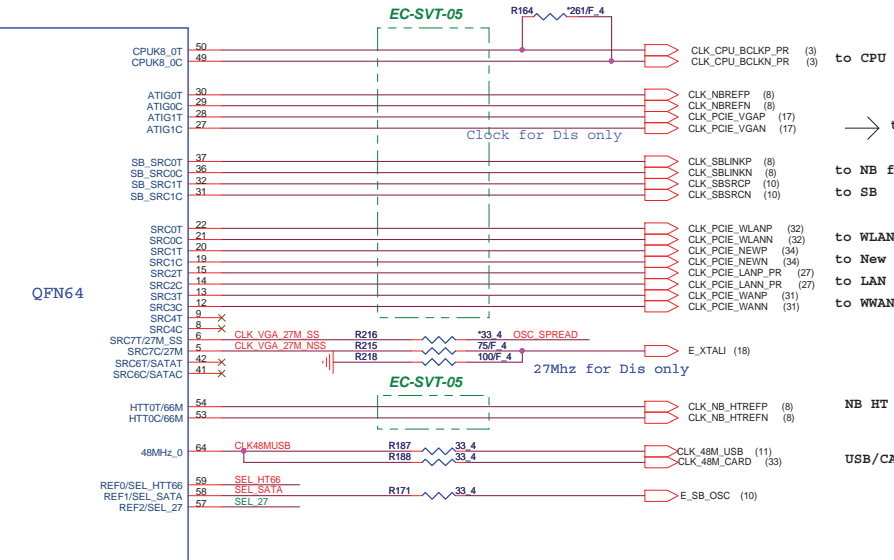
EXT GFX CLKP EXT GFX_CLKN	RP47 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_NSS CLK_VGA_27M_SS	R213,R215 STUFF	To Park-S3 27Mhz - Discrete only



can remove MOSFET level shift
SB/clock gen / DDR3 is 3.3V/80
power-level

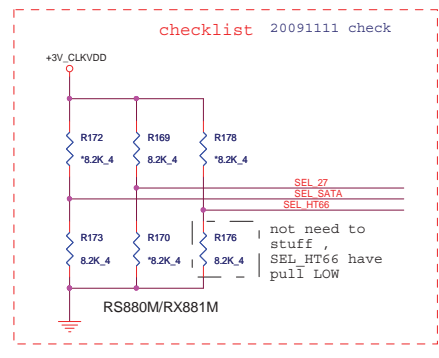


if use clock request pin, need to pull Hi for default setting



ICs: IDT ICS9LPRS476AKLFT, SLG SLG8SP628VTR--AL8SP628000, RTL RTM880N-796-- AL000880001

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
SEL_HTT66	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
SEL_SATA	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
SEL_27	0	100 MHz spreading differential SRC clock



clocklist 20091111 check

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

not need to stuff, SEL_HTT66 have pull LOW

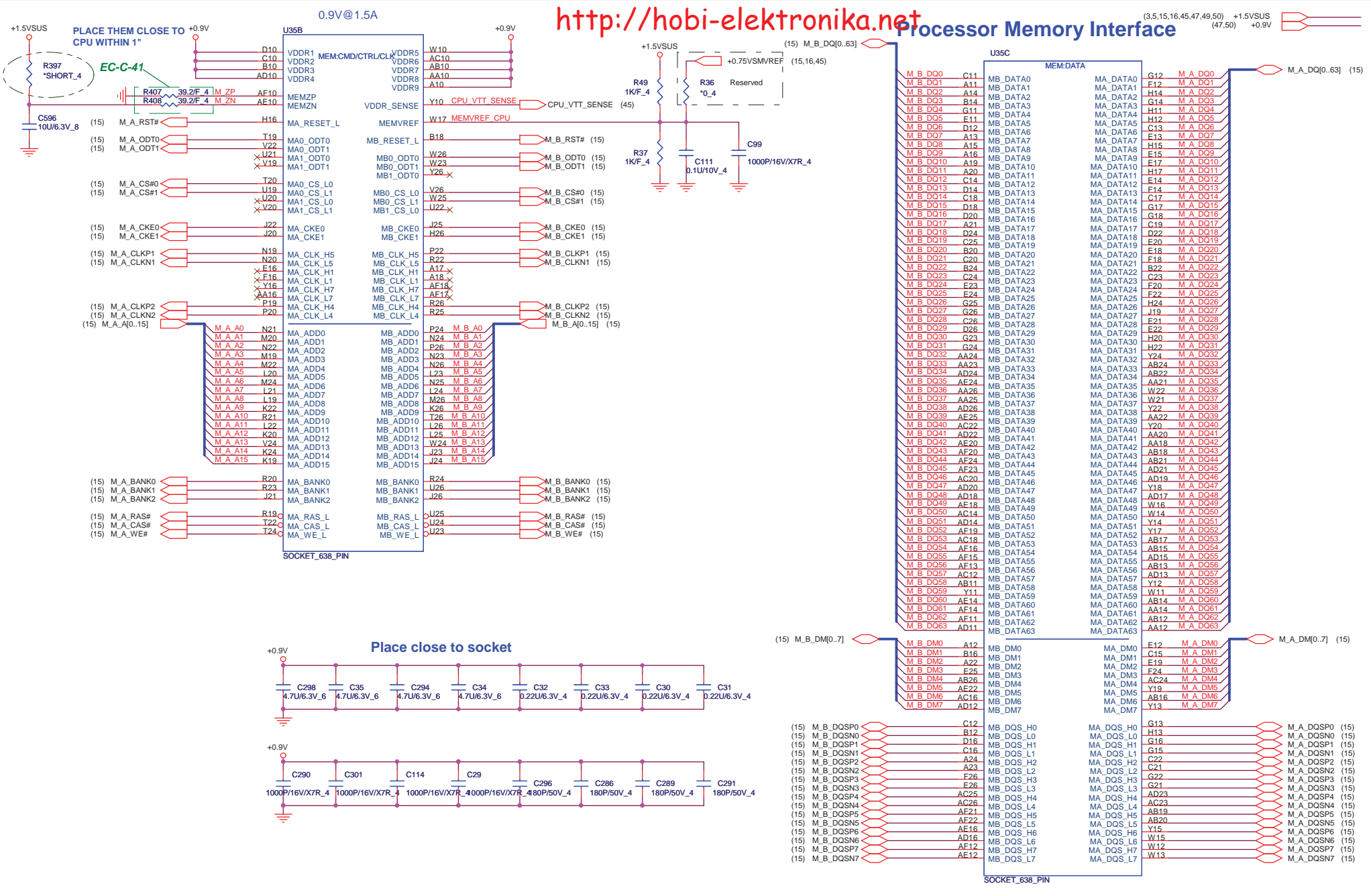
Quanta Computer Inc.

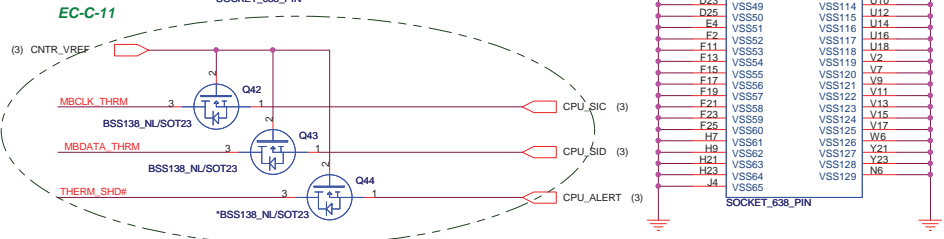
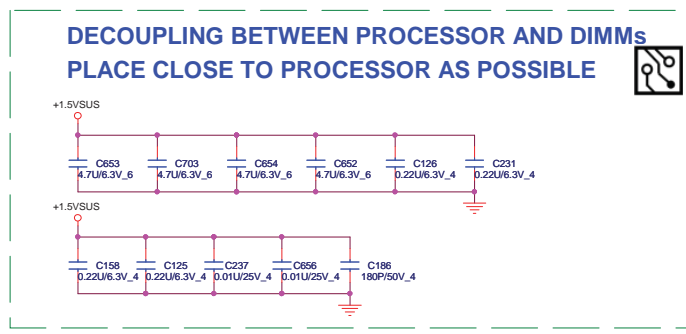
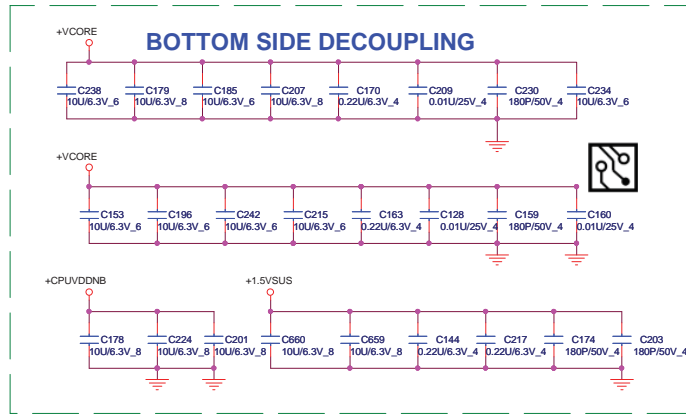
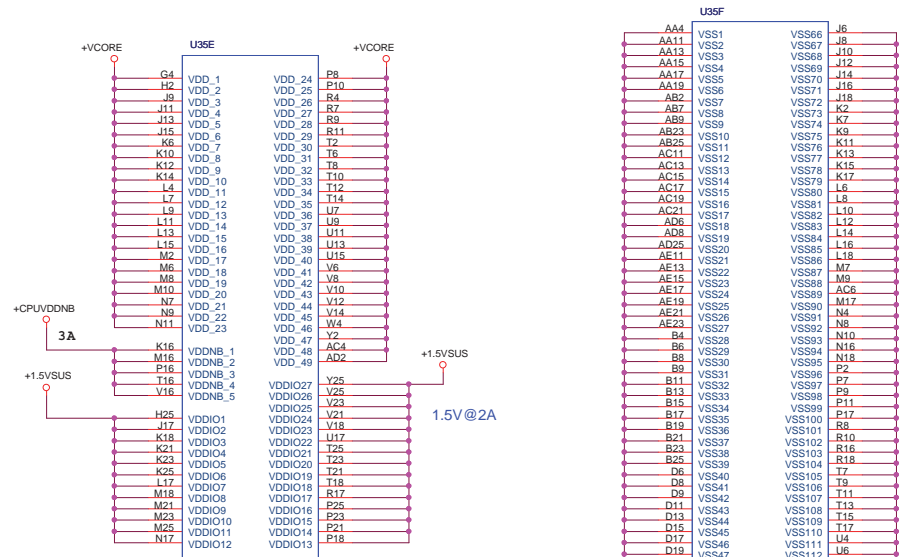
PROJECT : LD-Note AMD DIS

Size Document Number

Clock Generator

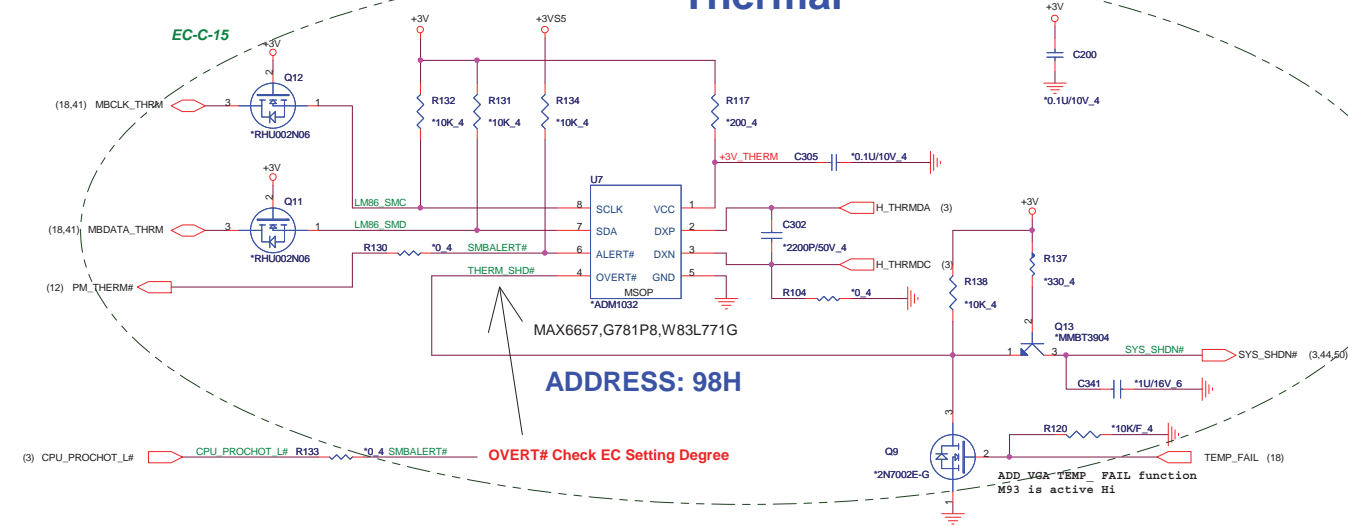
Date: Monday, June 14, 2010 Sheet 2 of 55





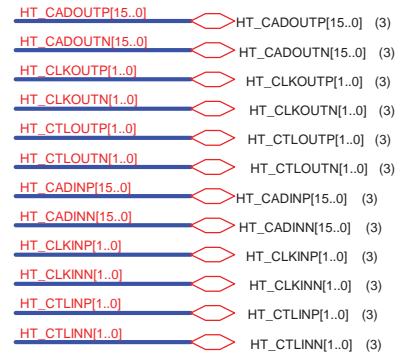
CPU H/W MONITOR

Thermal



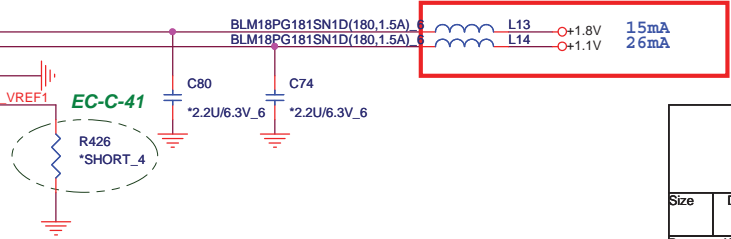
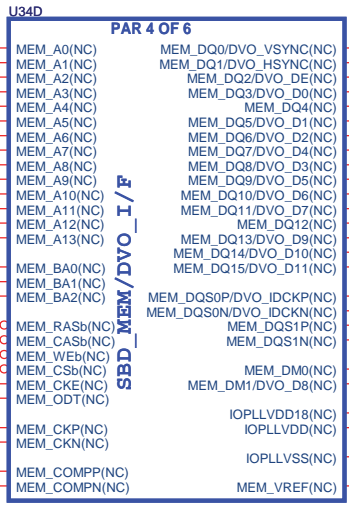


HYPER TRANSPORT CPU I/F



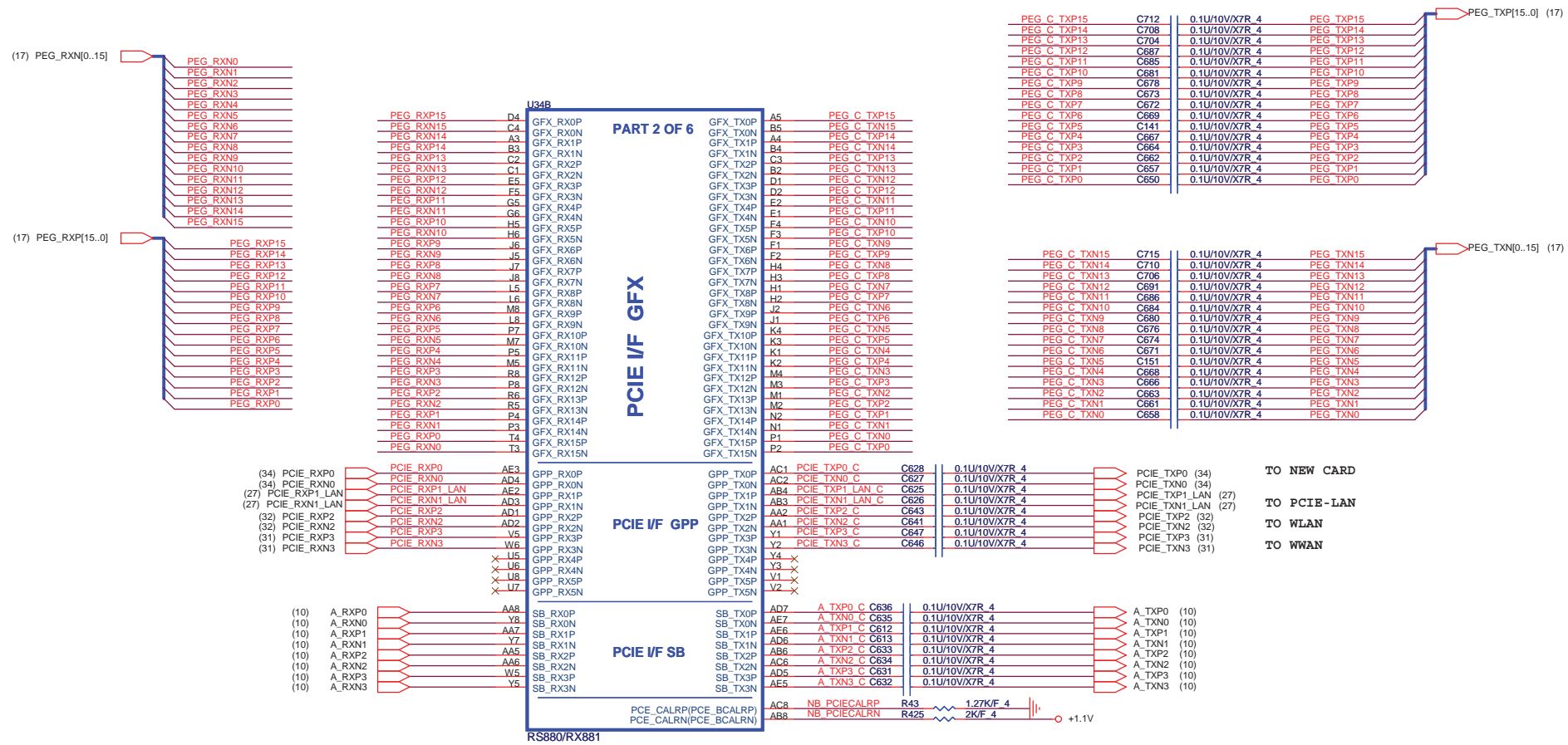
Close to NB within 1"

Close to NB within 1"



Quanta Computer Inc.
PROJECT : LD-Note AMD DIS

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date:	Wednesday, June 09, 2010	Sheet 6 of 55



Keep the impedance of PCIe lane to 85ohm +/-15% Including the A-link

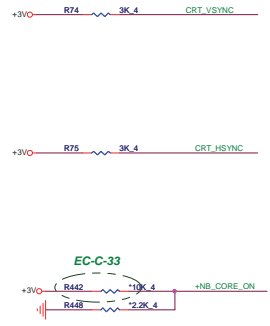
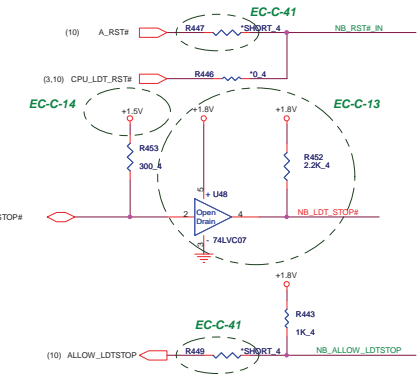
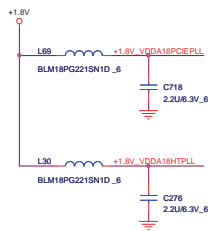
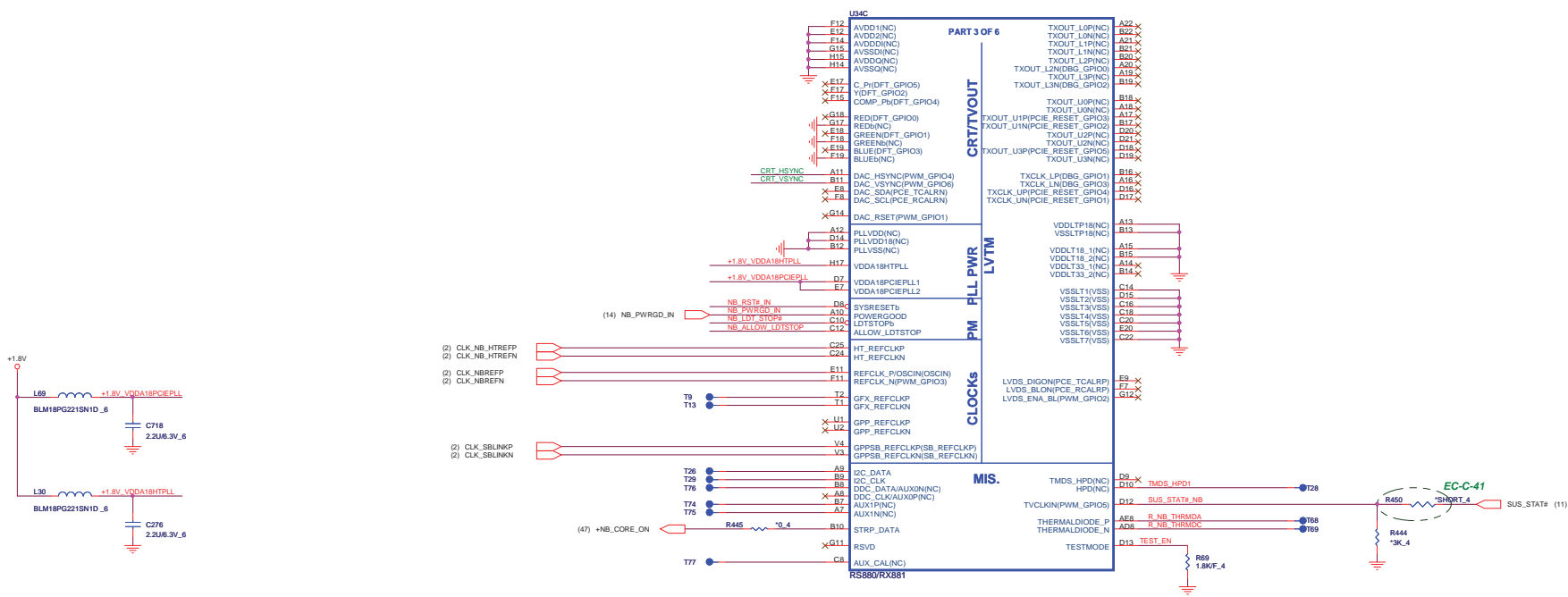
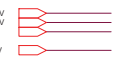
All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso cable for Guam.
Customer need to follow the MBDG.

Quanta Computer Inc.
PROJECT : LD-Note AMD DIS

Size Document Number Rev 1A
RS580M-PCIE /F/ 2/4

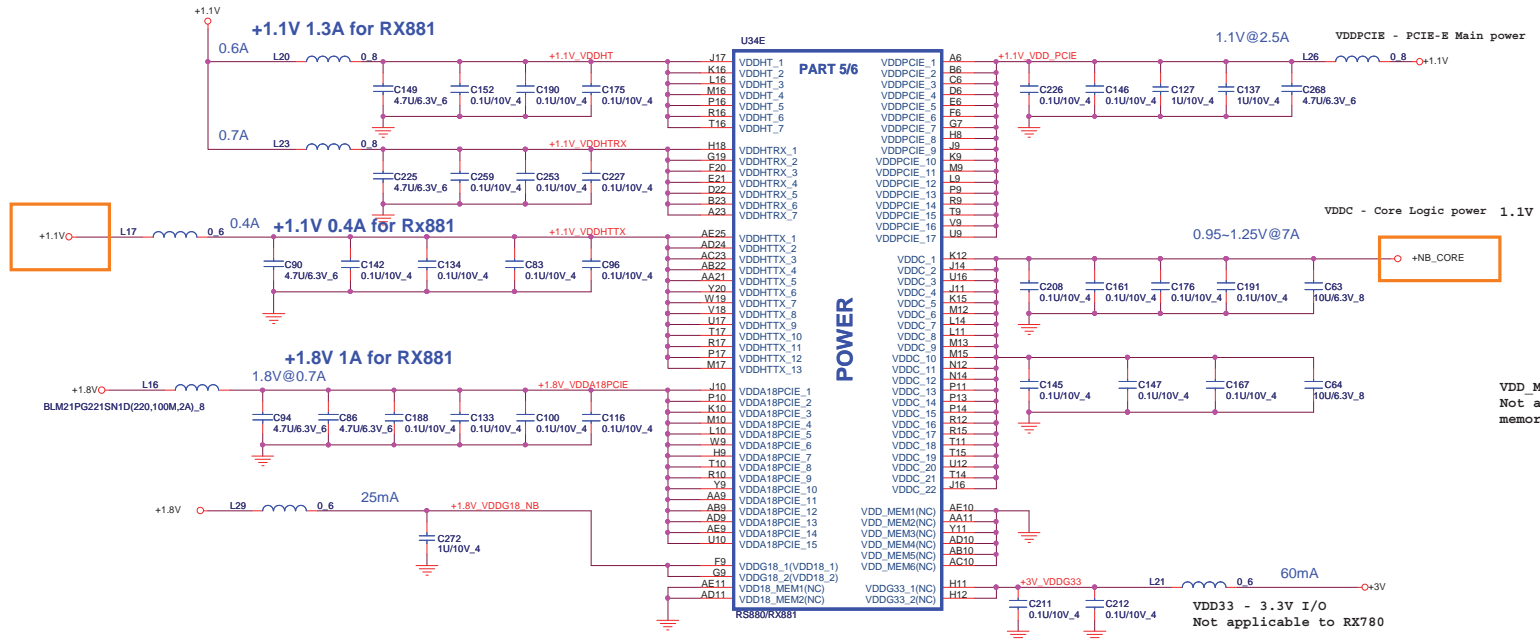
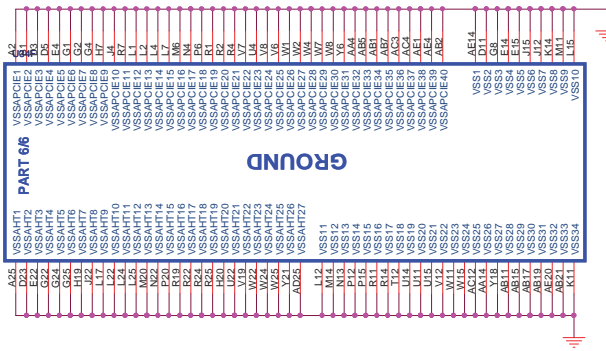
Date: Wednesday, June 09, 2010 Sheet 7 of 55

(2,3,6,7,9,13,46,50) +1.5V
 (6,9,14,46,50) +1.8V
 (2,3,5,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,36,37,40,41,46,47,50) +3V
 (23,44,45,48,50) +15V



RX881/RS880 POWER DIFFERENCE TABLE

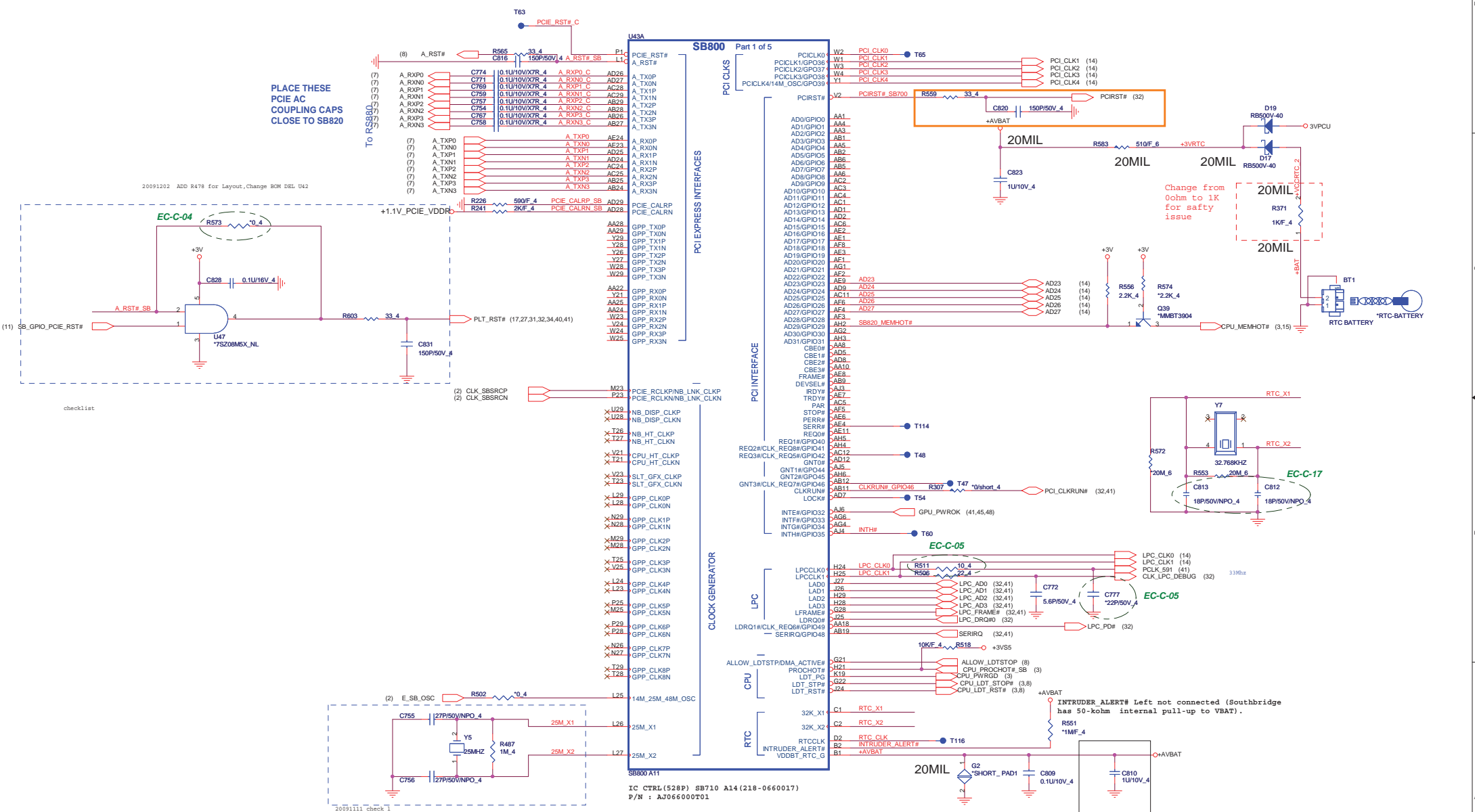
PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	AVDDQ	GND	GND
VDDHTRX	+1.1V	+1.1V	AVDDQ	GND	GND
VDDHTTX	+1.2V	+1.1V	PLLVD	GND	GND
VDDA18PCIE	+1.8V	+1.8V	PLLVD018	GND	GND
VDDG18	+1.8V	+1.8V	VDDA18PCIEPLL	GND	GND
VDD18_MEM	GND	GND	VDDA18HTPLL	GND	GND
VDDPCIE	+1.1V	+1.1V	VDDLT18	GND	GND
VDDC	+1.1V	+NB_CORE	VDDLT18	GND	GND
VDD_MEM	GND	GND	VDDLT33	NC	NC
VDDG33	+3.3V	+3.3V			
AVDD	GND	GND			



VDD MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

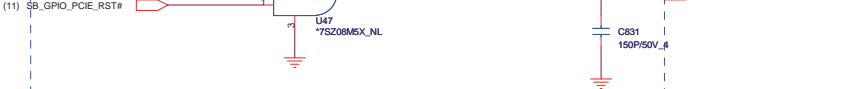
Quanta Computer Inc.
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	RS880M-POWER5 4/4	1A
Date:	Wednesday, June 09, 2010	Sheet 9 of 55

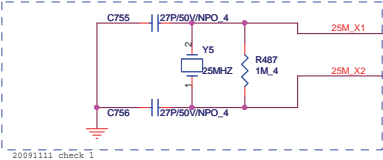
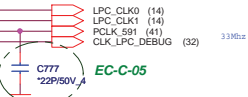
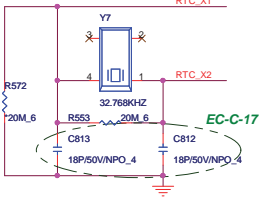


PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB820

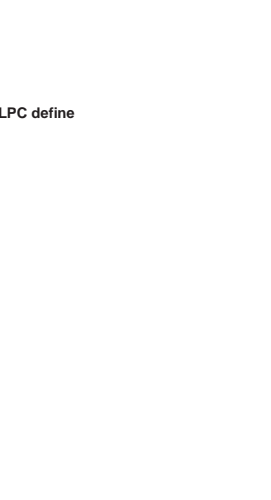
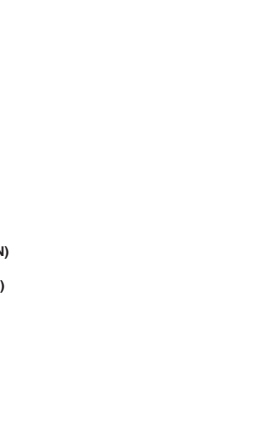
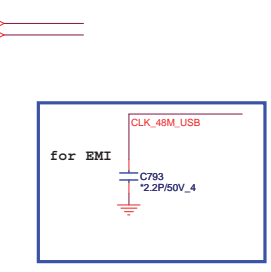
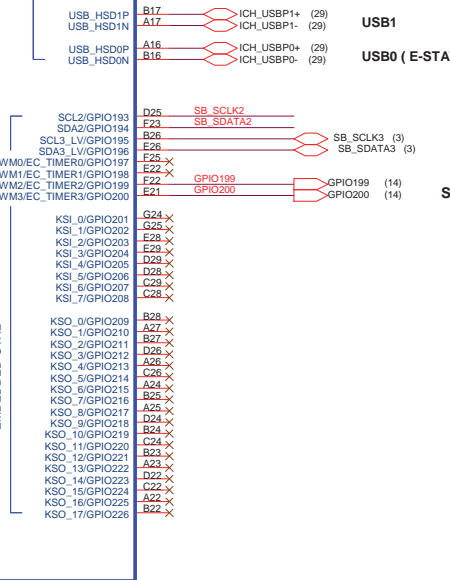
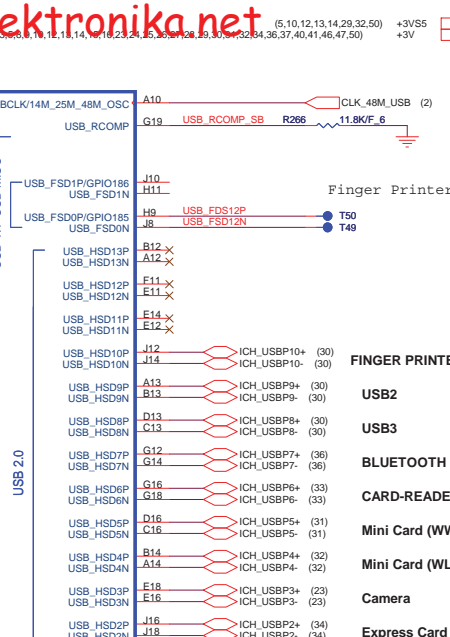
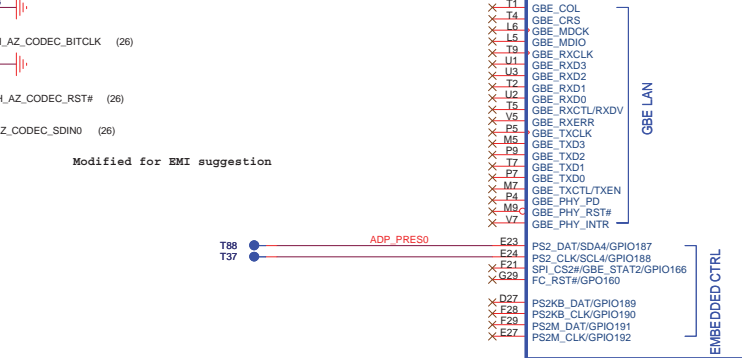
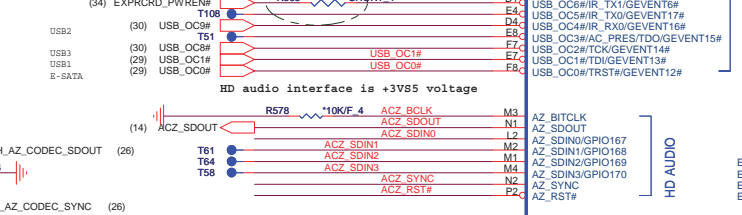
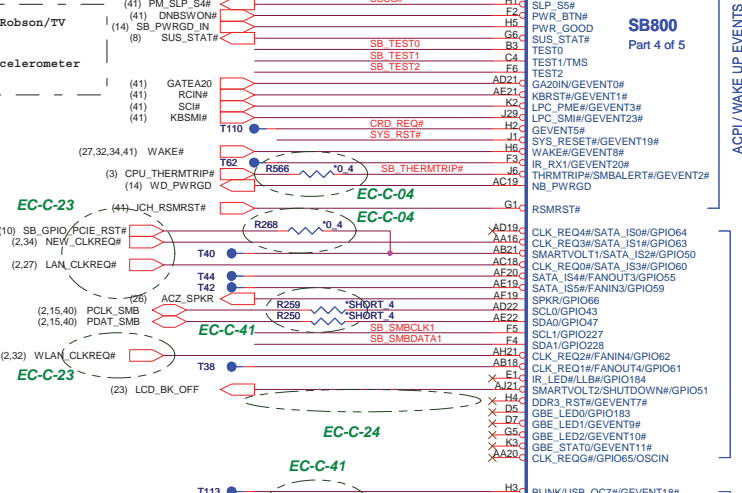
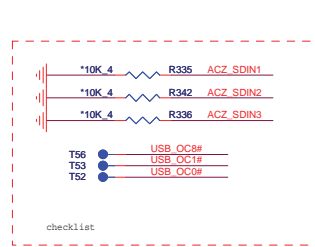
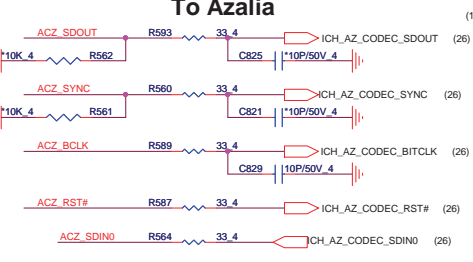
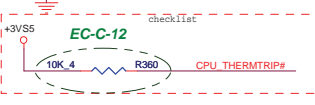
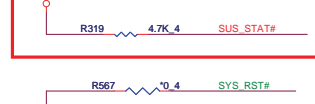
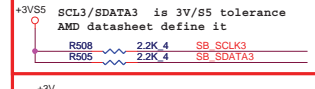
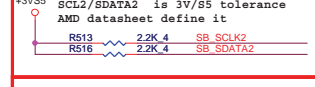
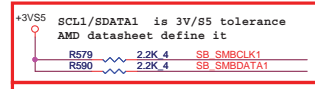
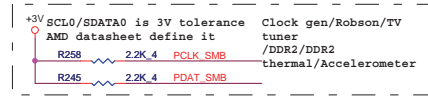
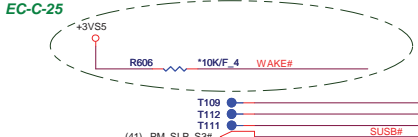
20091202 ADD R478 for Layout, change BOM DEL U42



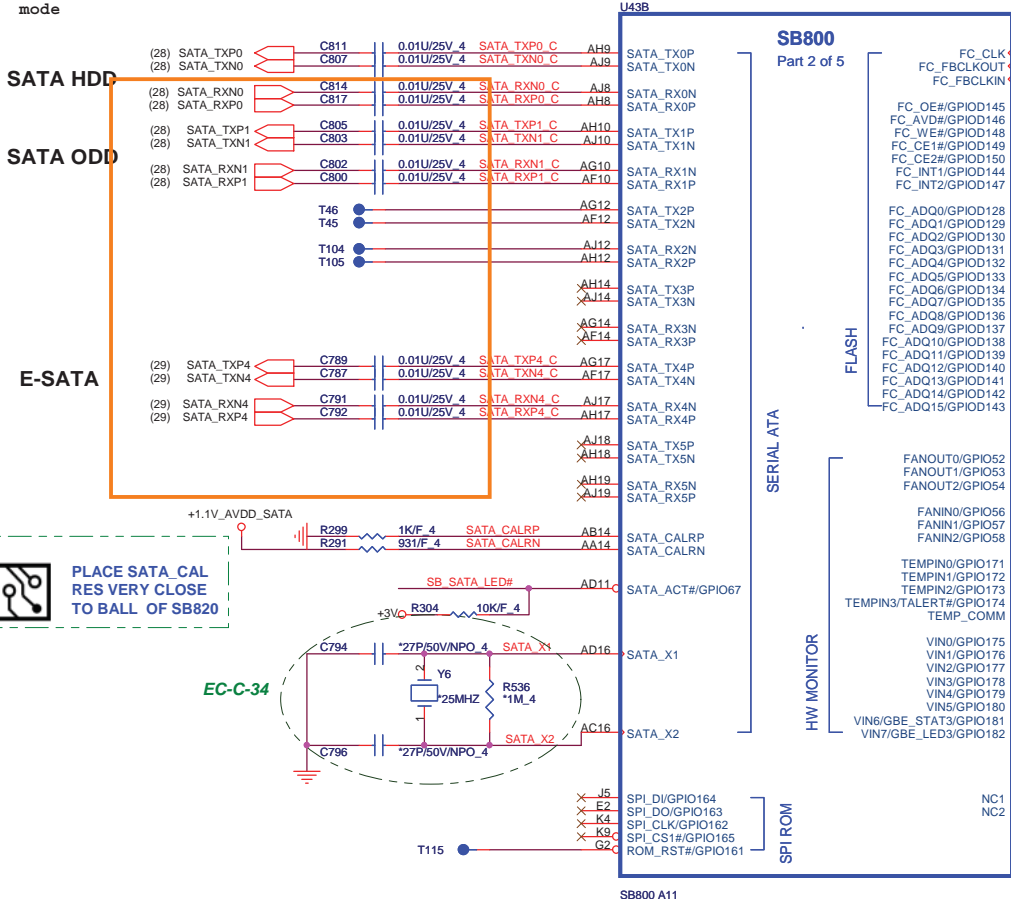
Change from
0ohm to 1k
for safety
issue



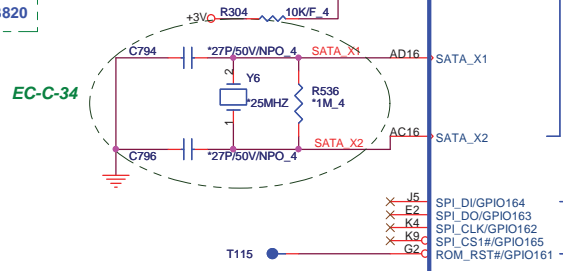
IC CTRL (528P) SB710 A14 (218-0660017)
P/N : AJ066000T01



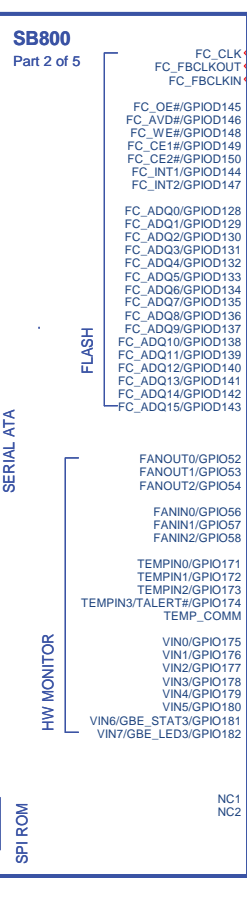
SATA PORT 0,1,2,3
can support AHCI
mode



PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

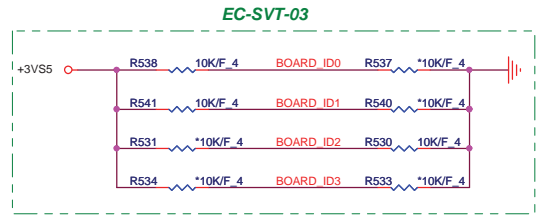
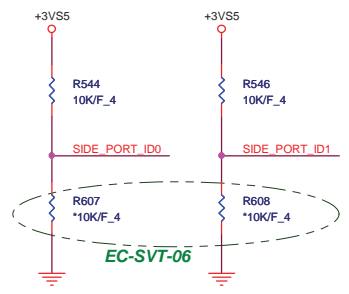


EC-C-29
EC-C-44

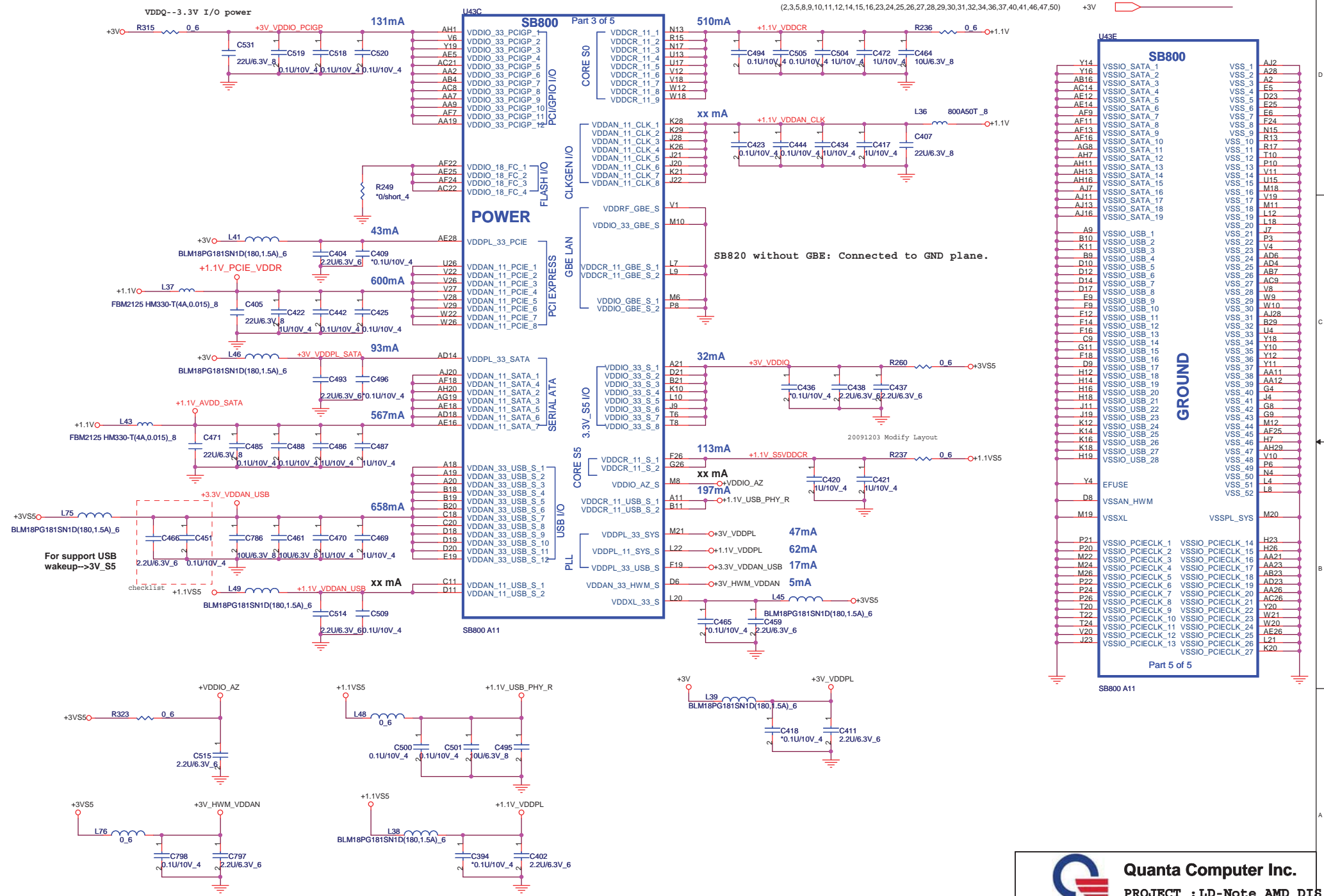


(5,10,11,13,14,29,32,50) +3VS5
+3V

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

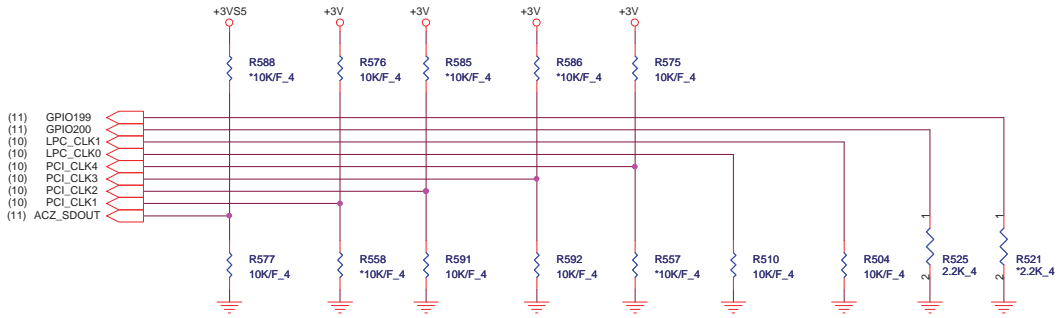


EC_ID1	ID3	ID2	ID1	ID0	
	0	X	X	X	BL GC5C UMA (14 ")
	1	X	X	X	LD GC6C UMA (15 ")
0	X	0	0	0	SDV
0	X	0	0	1	SIT
0	X	0	1	0	SIT-R2
0	X	0	1	1	SVT
0	X	1	0	0	SOVP
	X	1	1	1	USB HW solution implementation



REQUIRED STRAPS

(2,3,5,8,9,10,11,12,13,15,16,23,24,25,26,27,28,29,30,31,32,34,36,37,40,41,46,47,50) +3V
 (6,10,11,12,13,23,32,50) +3V5
 +3V



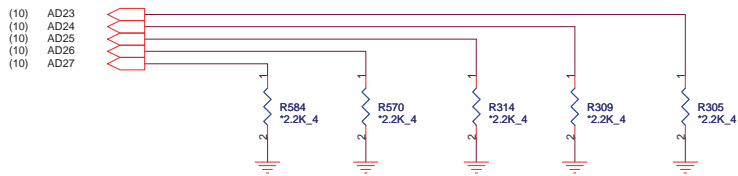
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 <i>DEFAULT</i>	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE <i>DEFAULT</i>	EC ENABLED	CLKGEN ENABLED	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE <i>DEFAULT</i>	FORCE PCIE Gen1	Watchdog Timer Disable <i>DEFAULT</i>	IGNORE DEBUG STRAPS <i>DEFAULT</i>	Fusion CLOCK MODE	EC DISABLED <i>DEFAULT</i>	CLKGEN DISABLED <i>DEFAULT</i>	L, H=LPC ROM <i>DEFAULT</i> L, L=FWH ROM	

internal have pull Hi 10K

NB_PWRGD_IN:
 RS880/RX881 = 1.8V;
 Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

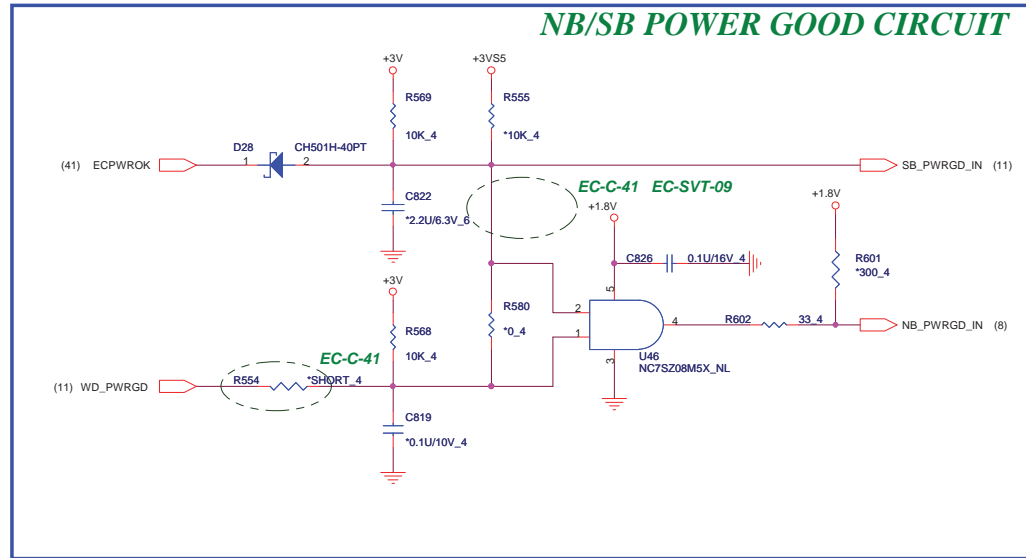
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL <i>DEFAULT</i>	DISABLE ILA AUTORUN <i>DEFAULT</i>	USE FC PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	DISABLE PCI MEM BOOT <i>DEFAULT</i>
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

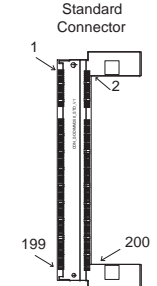
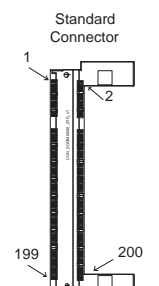
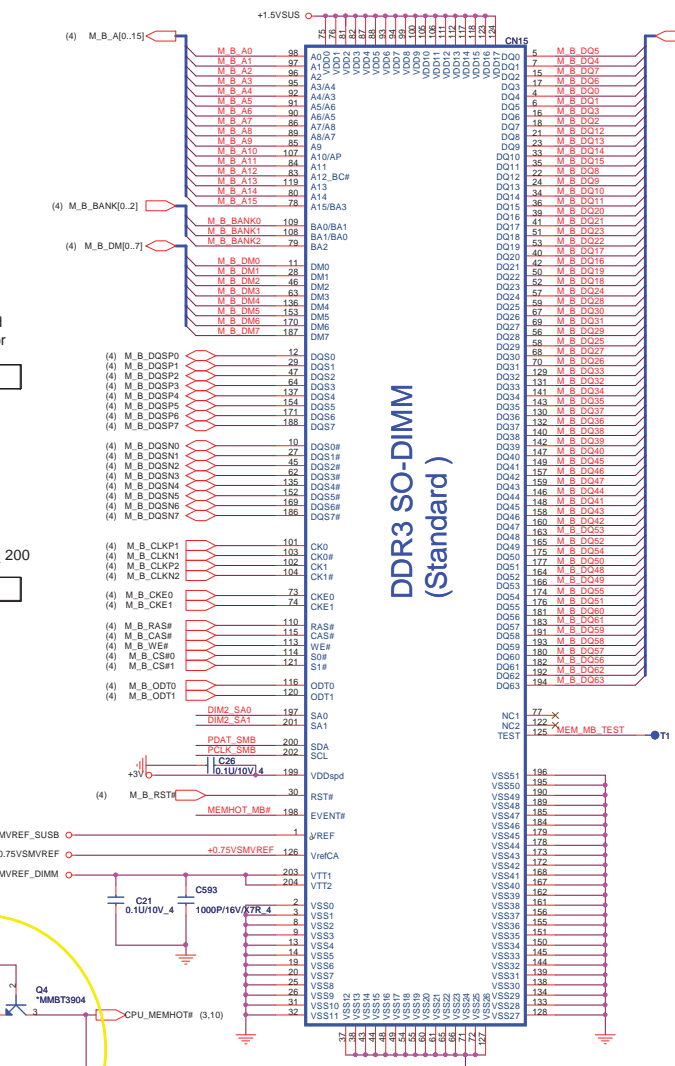
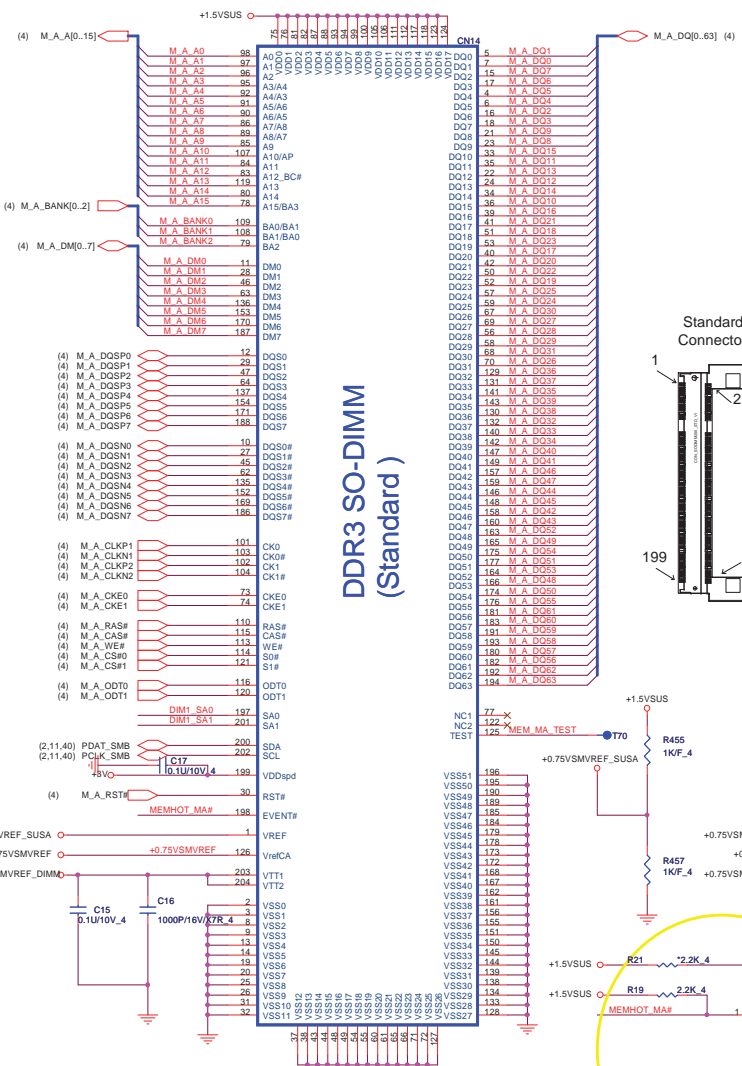
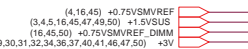
NB/SB POWER GOOD CIRCUIT



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
 ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

Place these Caps near So-Dimm0.

Place these Caps near So-Dimm1.

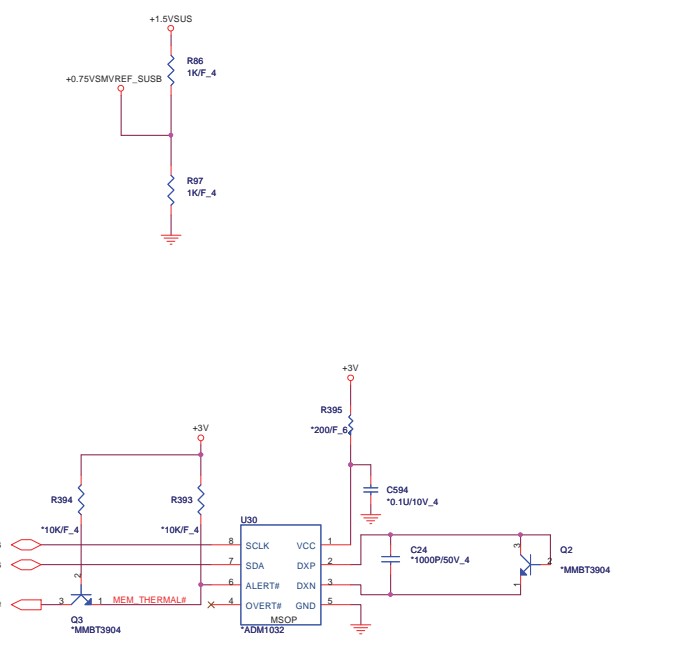
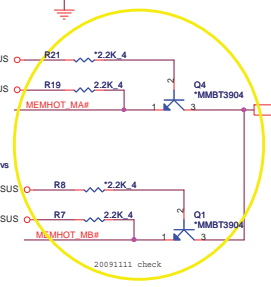
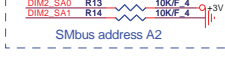


DDR3 SO-DIMM (Standard)

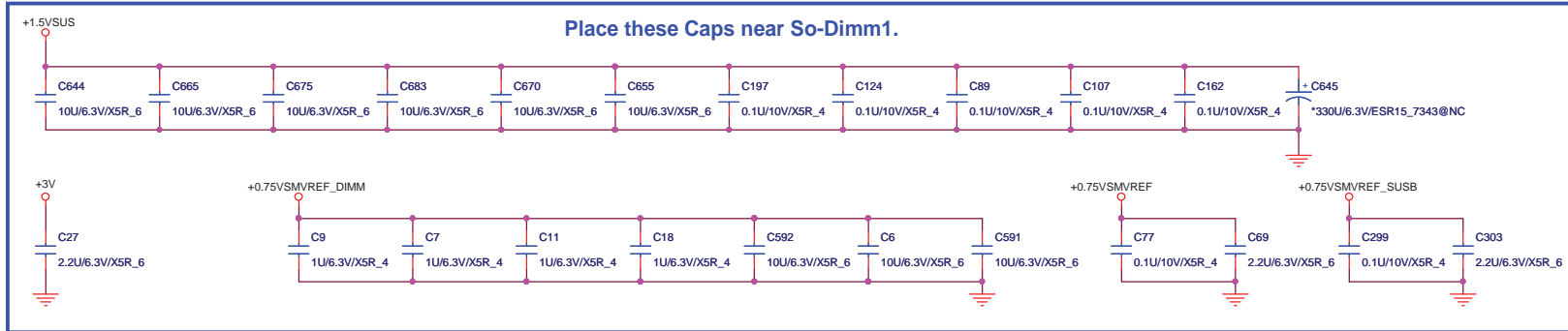
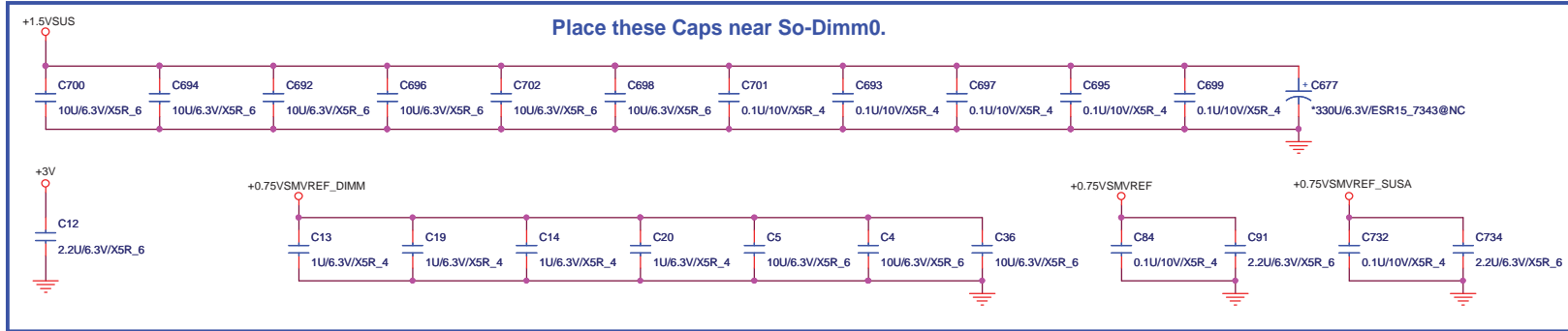
DDR3 SO-DIMM (Standard)

(DIMM-0 H=5.2)

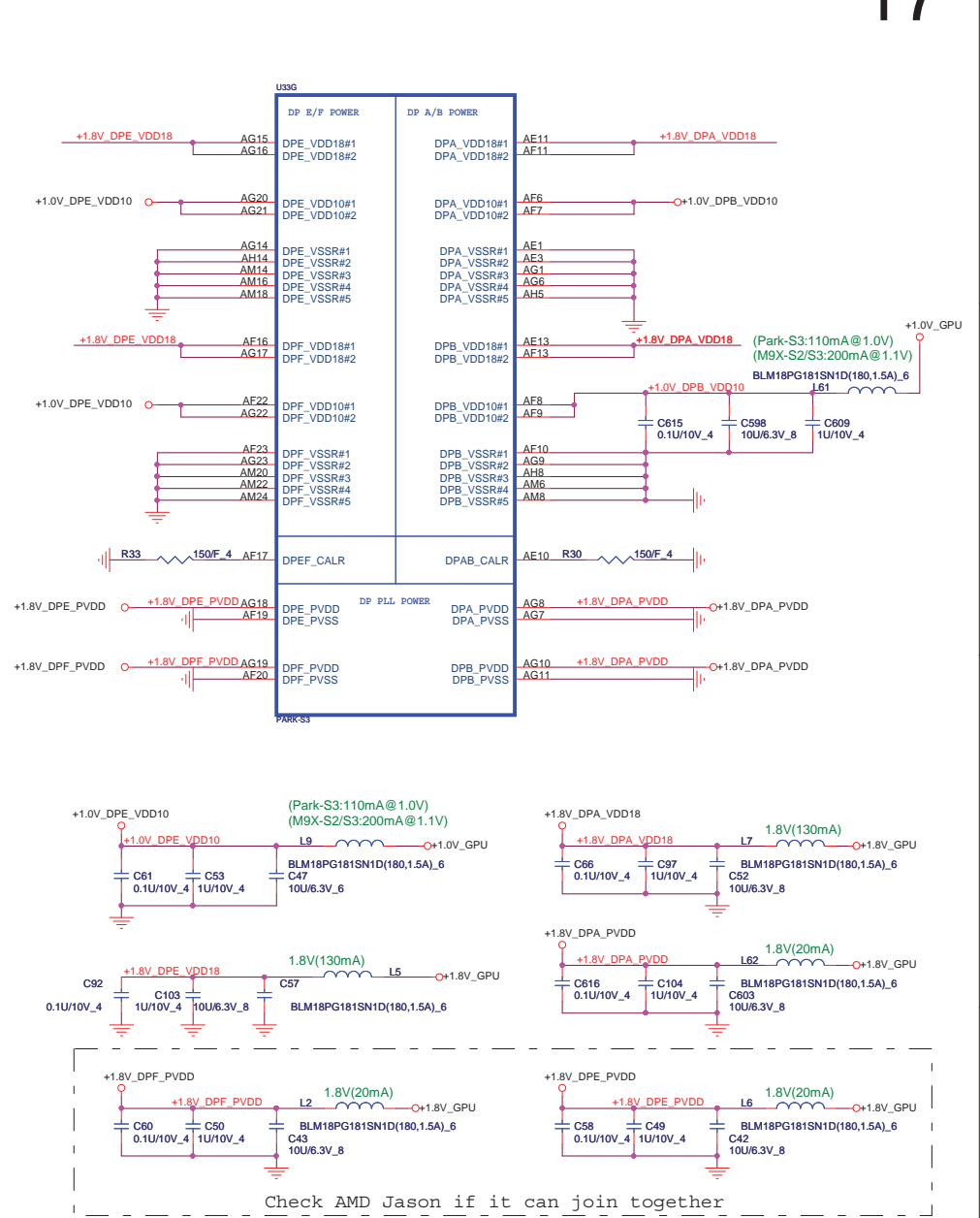
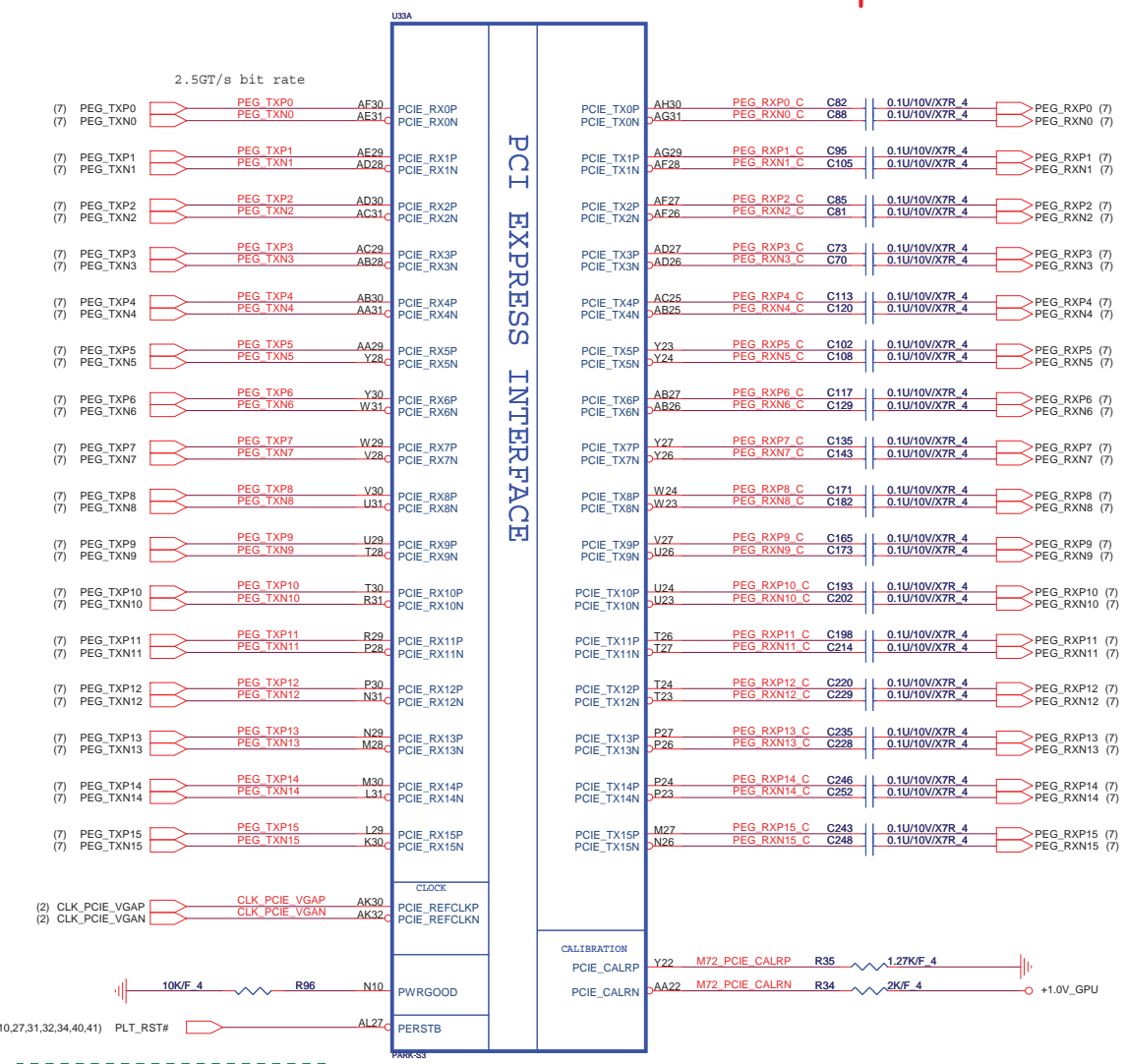
(DIMM-1 H=9.2)



Close DDR3 socket



PCI EXPRESS INTERFACE

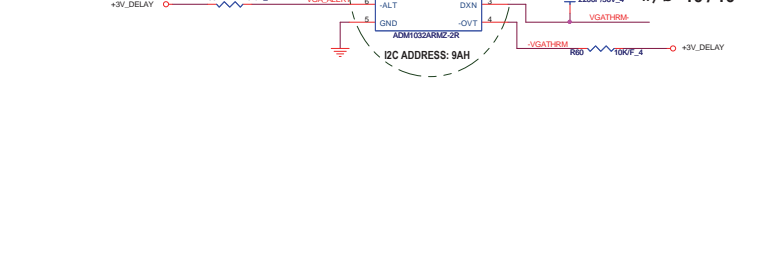
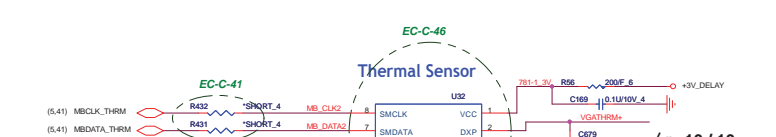
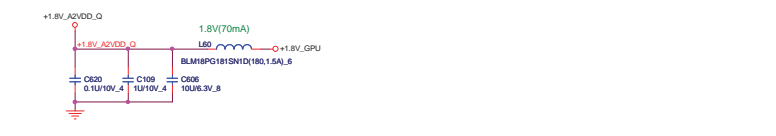
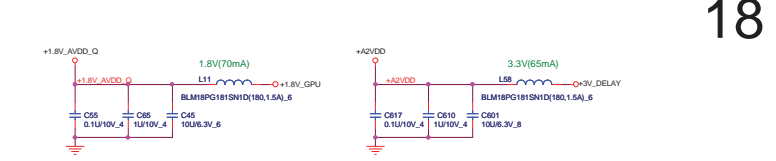
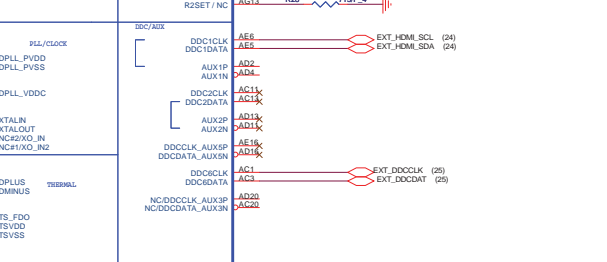
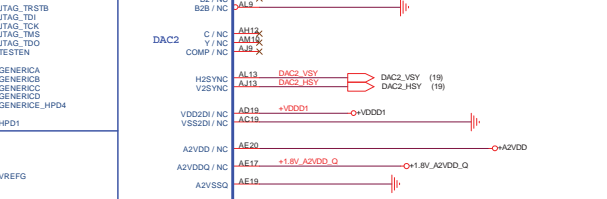
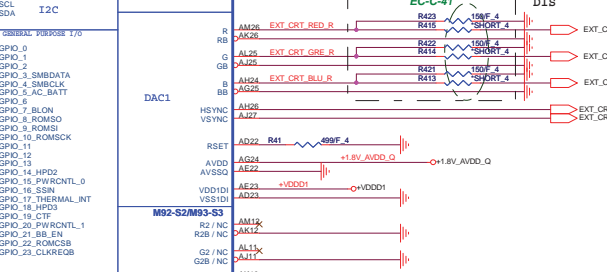
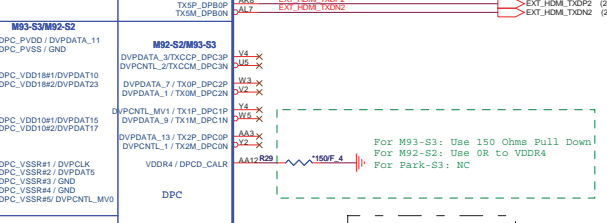
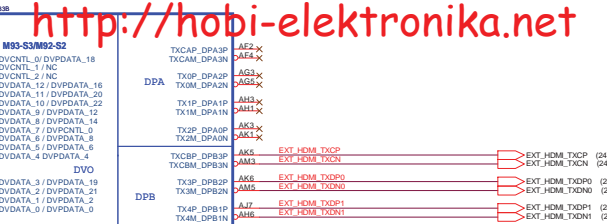
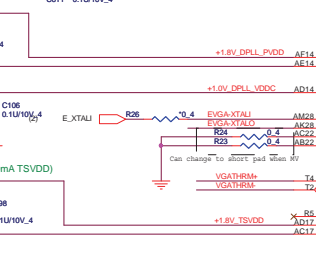
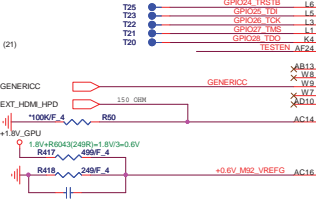
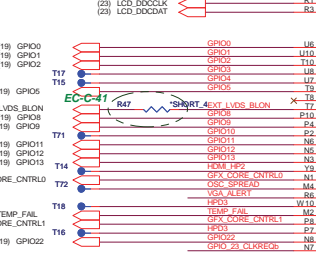
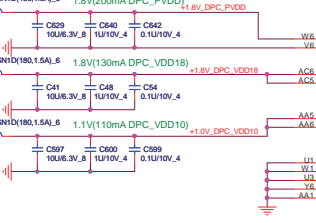
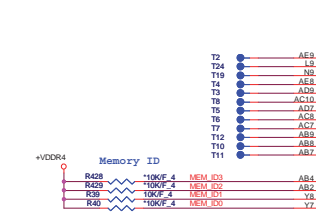
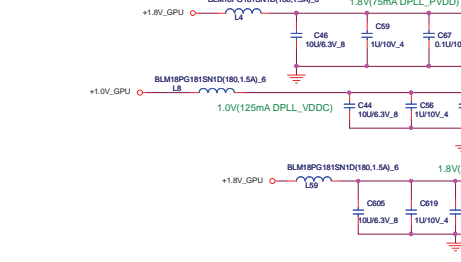
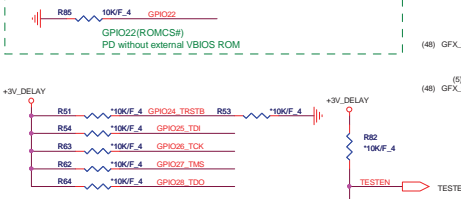


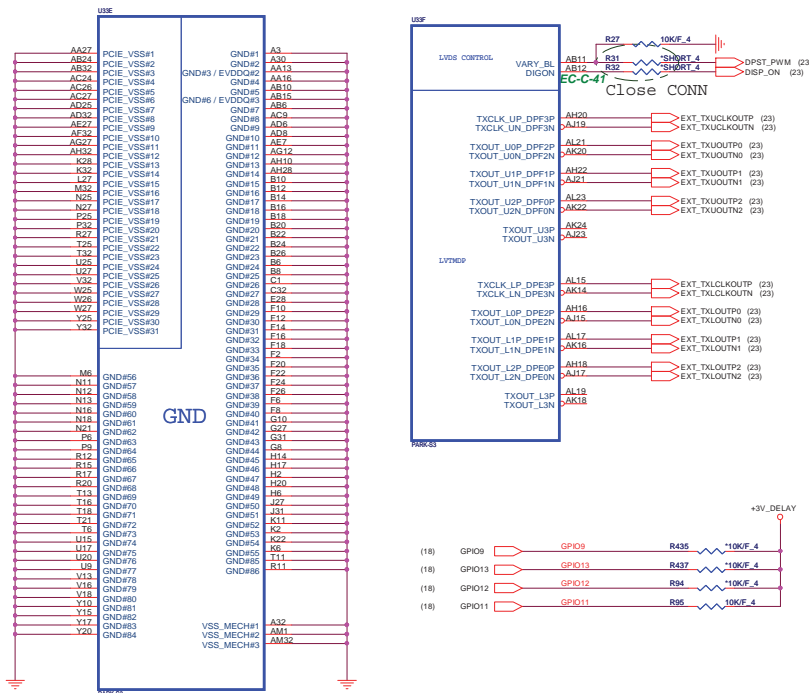
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix - Orion-die	64M*16-800MHZ	H5T0G53BFR-12C
0001	Samsung - E-die	64M*16-800MHZ	K4W1G1646B-HC12
0010	Hynix - Vega-die	128M*16-800MHZ	H5TQ39G3BFR-12
0011	Samsung - B-die	128M*16-800MHZ	K4W2G1646B-HC12
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

GPIO20 GPIO15

	PWRCTRL1	PWRCTRL0	VGA-CORE
L	1	1	0.9V
M	0	1	0.95V
H	1	0	1.12V





CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled (Default setting for Desktop) 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
RSVD	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	GENERIC		0
AUD(1)	HSYNC	AUD(1) AUD(0)	0
AUD(0)	VSNC	0: 0 No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

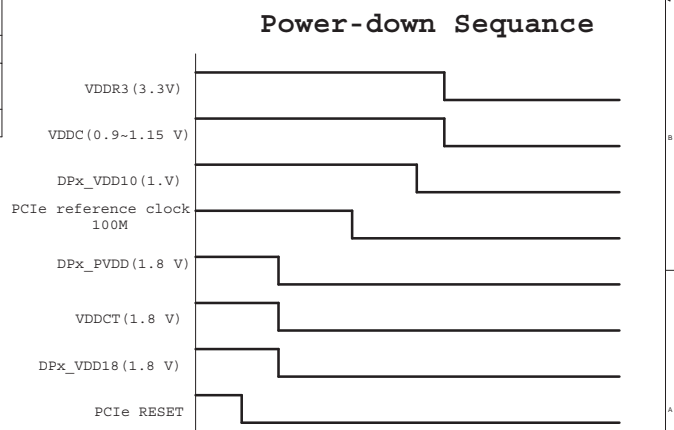
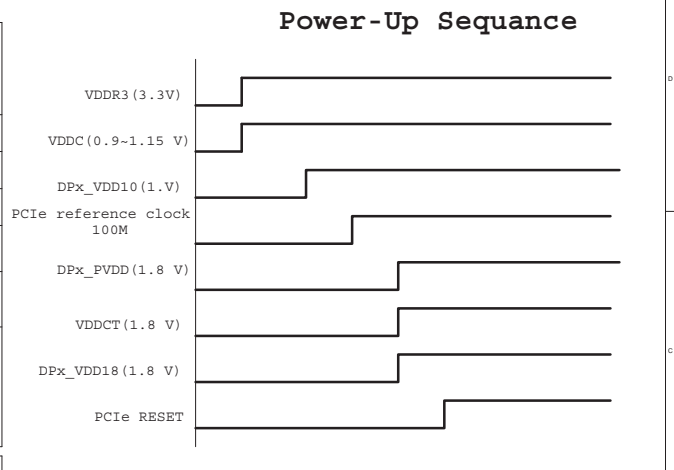
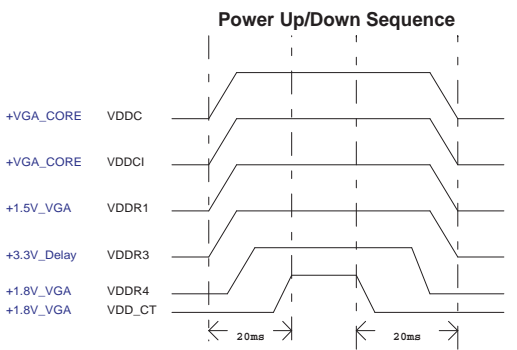
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

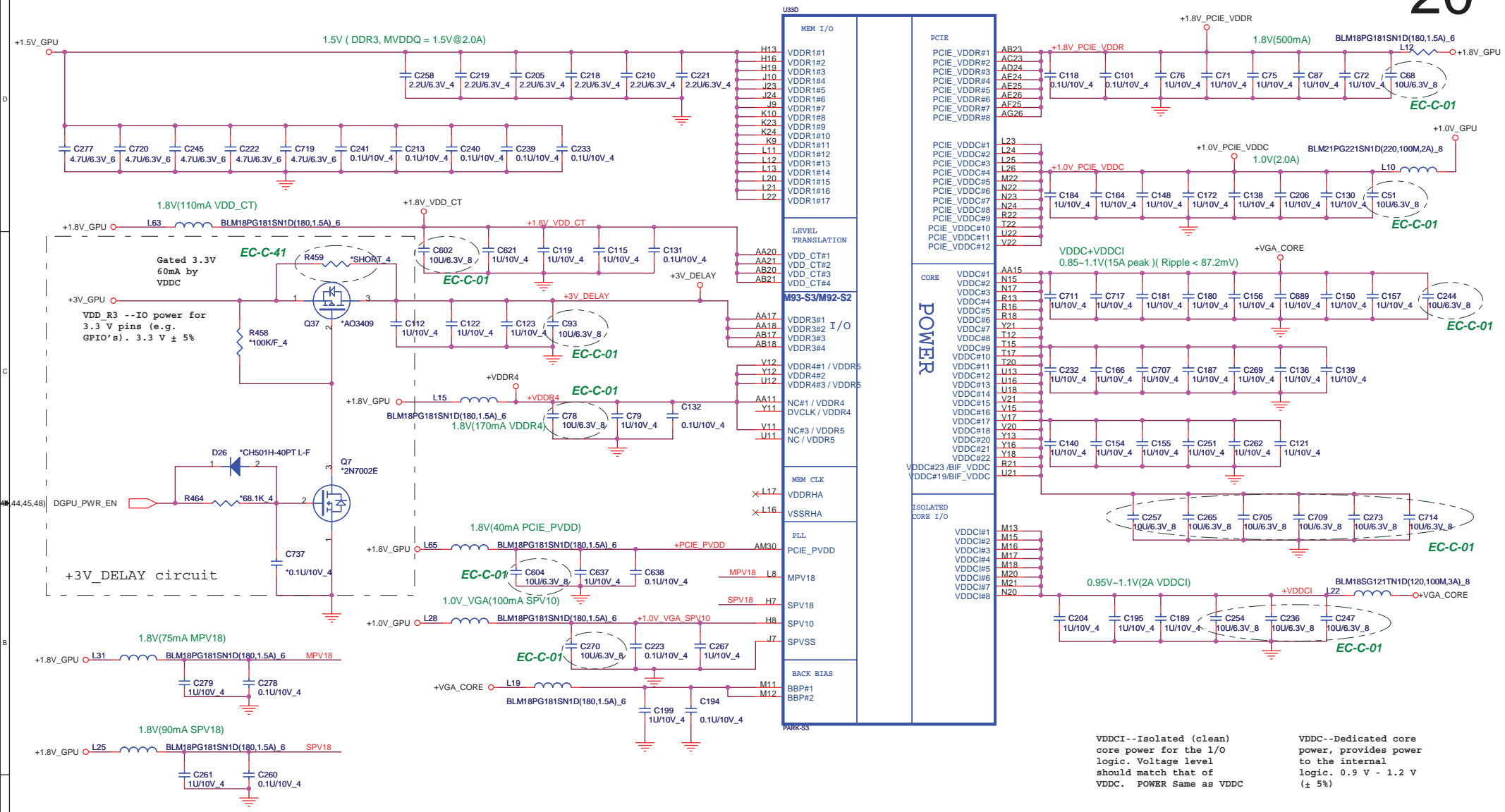
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
H2SYNC	GENERIC		0
GPIO21_BB_EN			0

Memory Aperture size

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	0
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.





VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

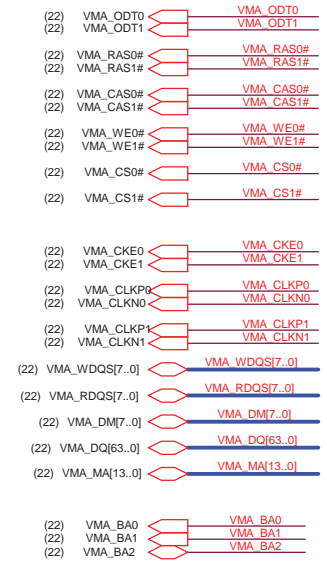
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

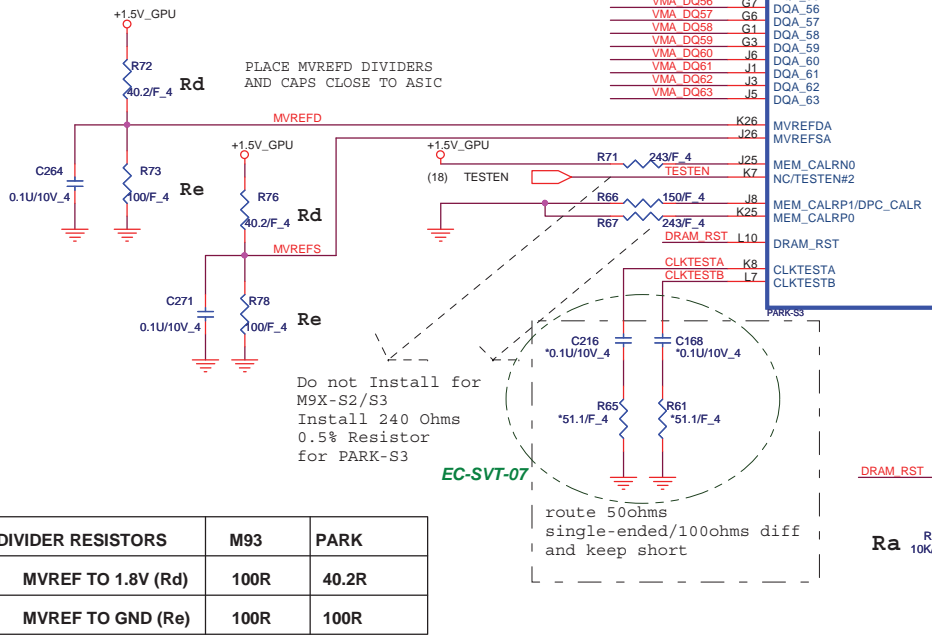
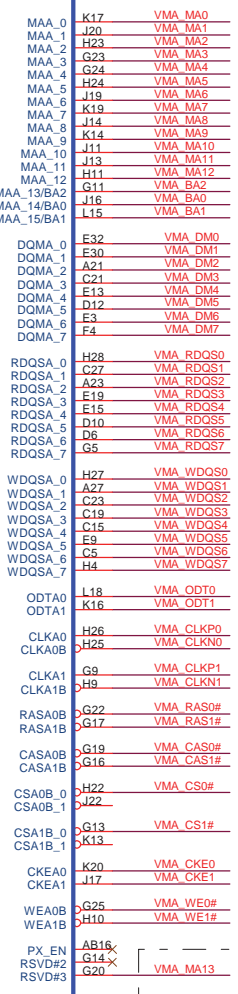
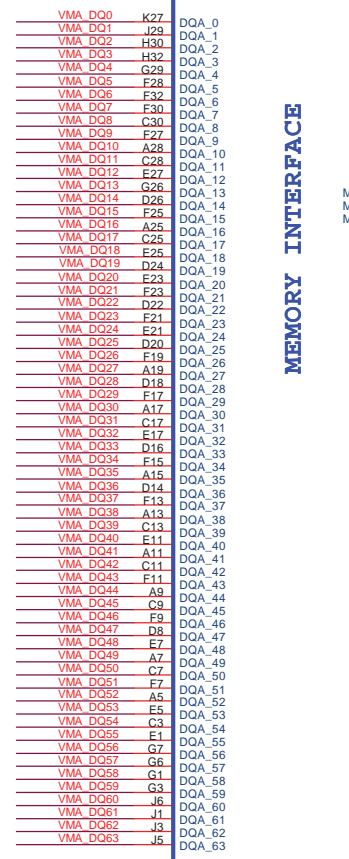
Quanta Computer Inc.
PROJECT : LD-Note AMD DIS
PARK Power and NC

Size: Document Number: Rev: 1A
 Date: Wednesday, June 09, 2010 Sheet: 20 of 55

MEMORY INTERFACE

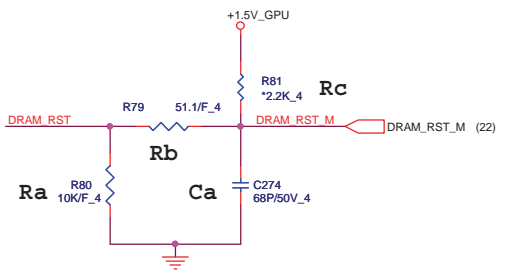


support 1gbit
VRAM (64M X 16)



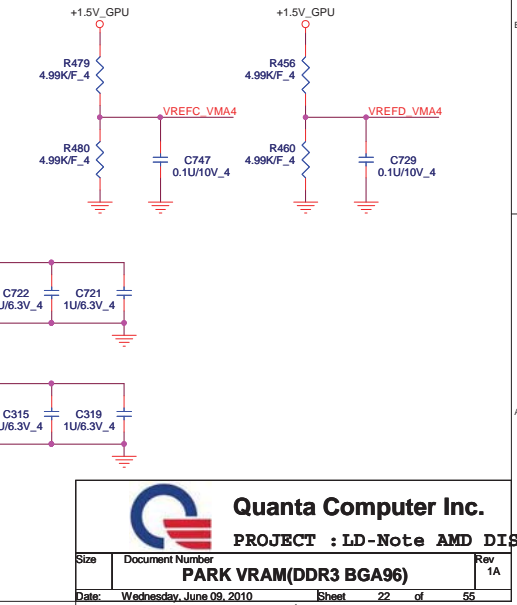
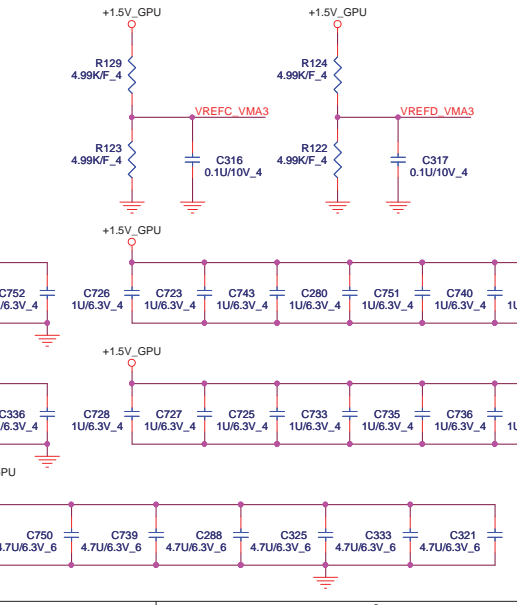
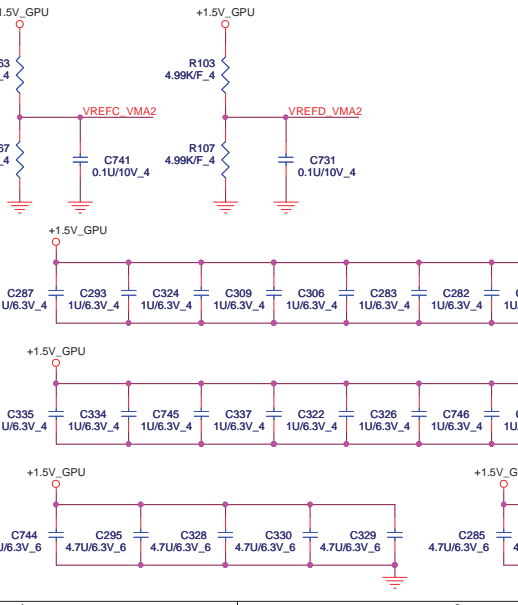
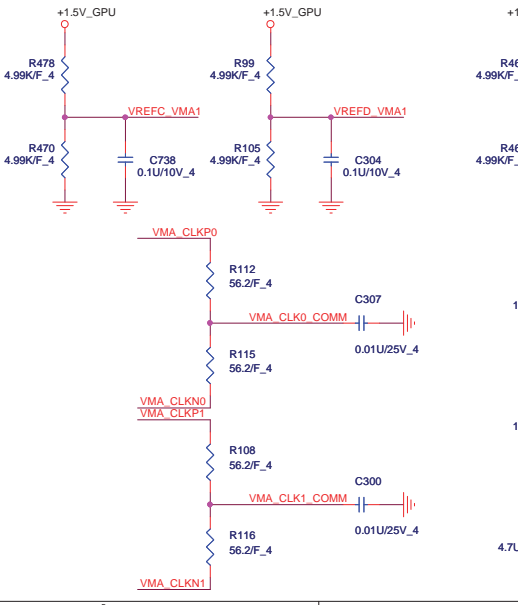
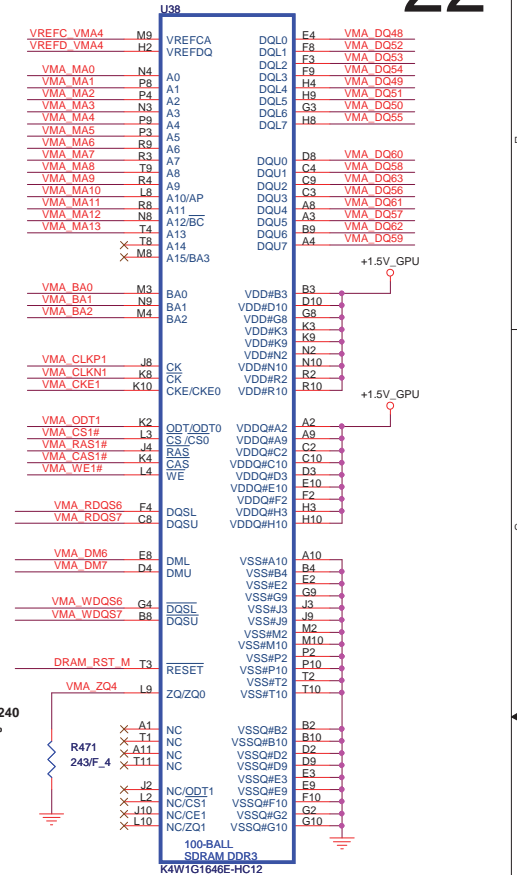
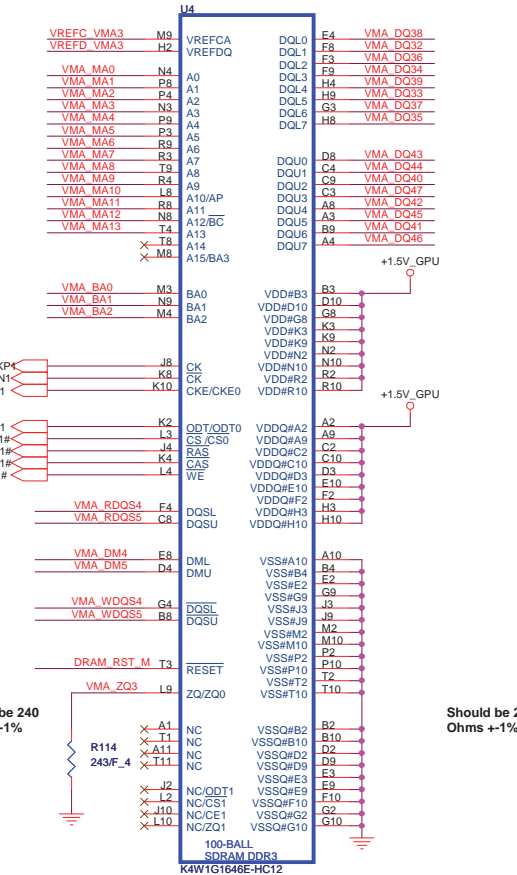
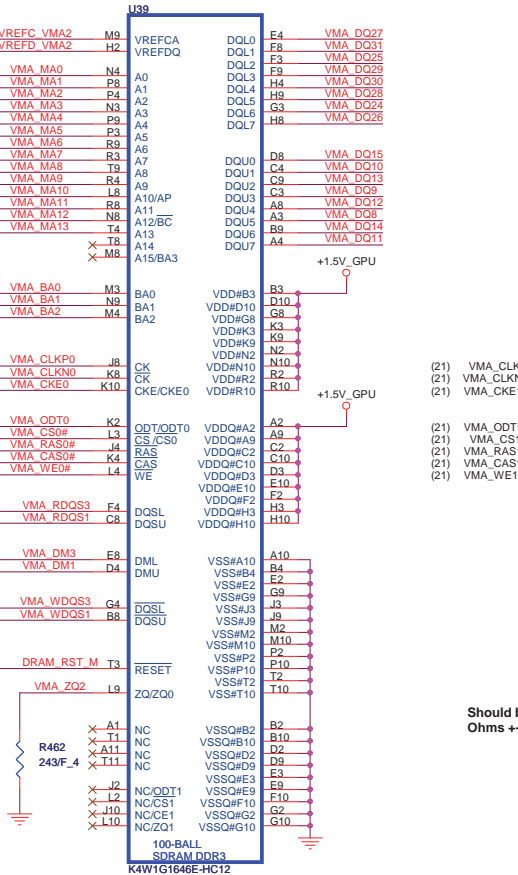
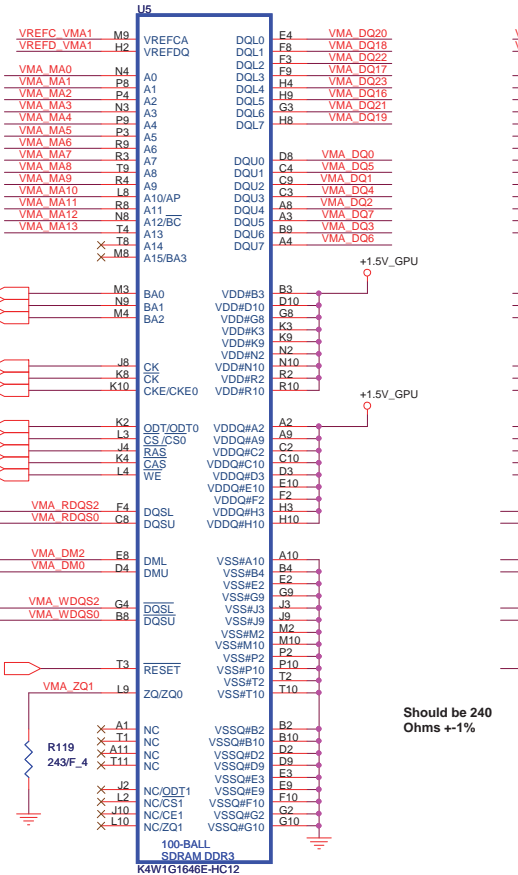
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

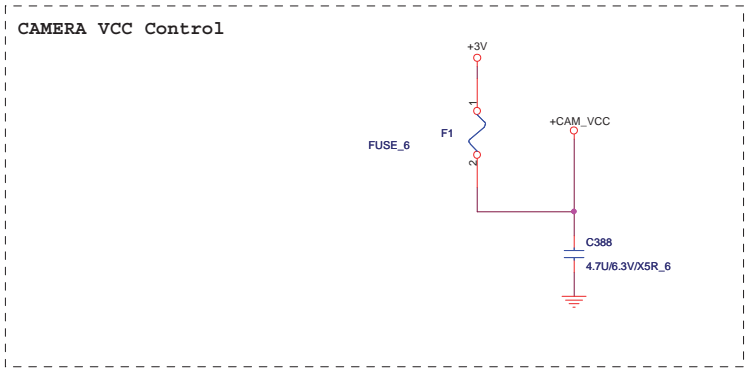
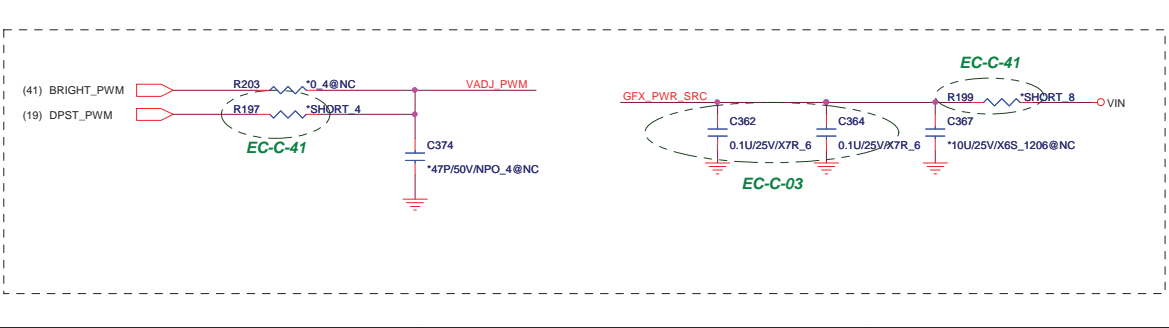
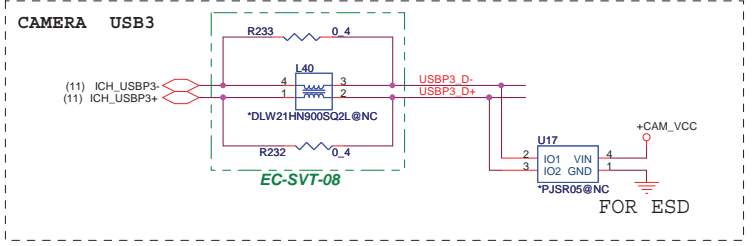
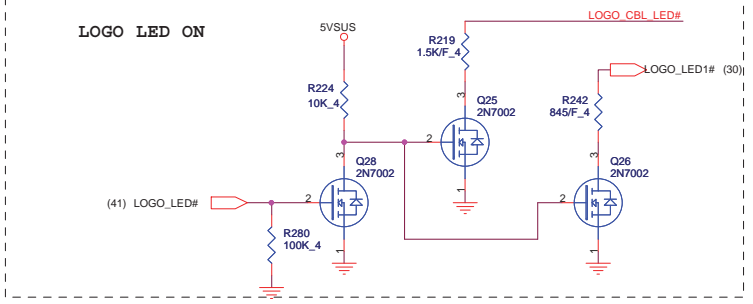
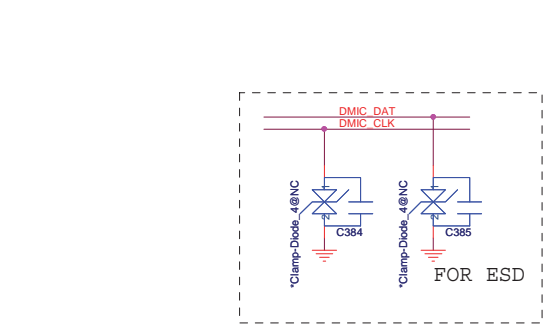
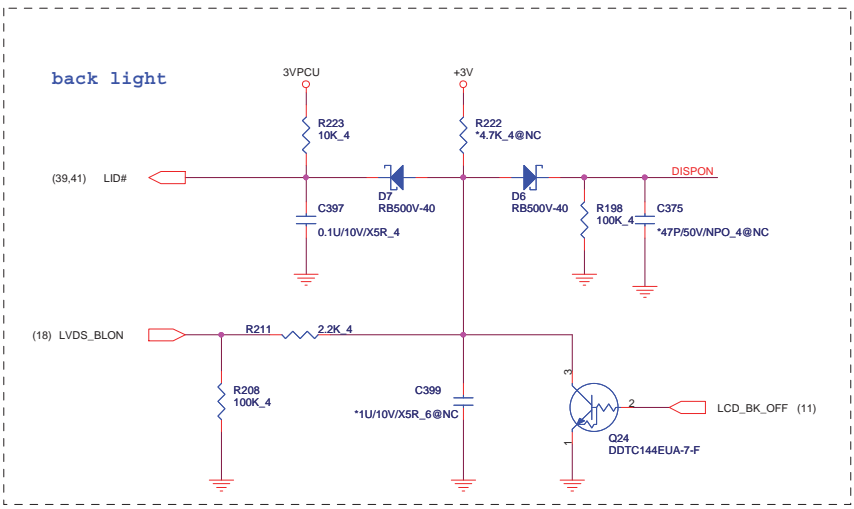
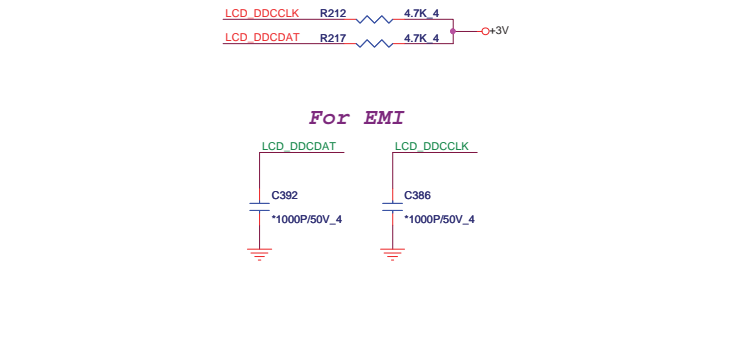
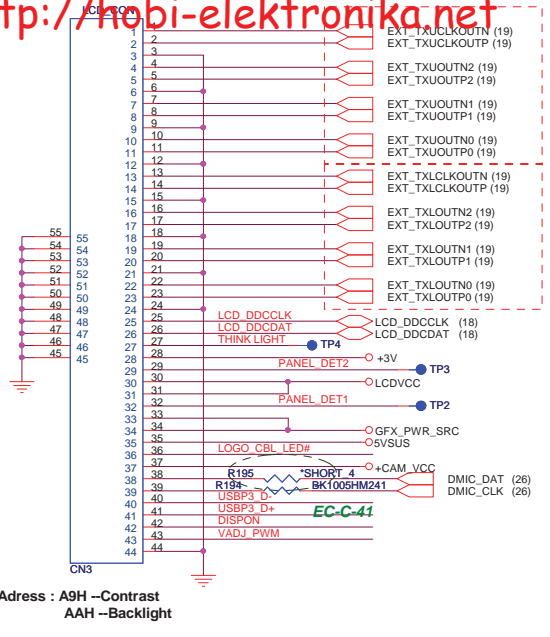
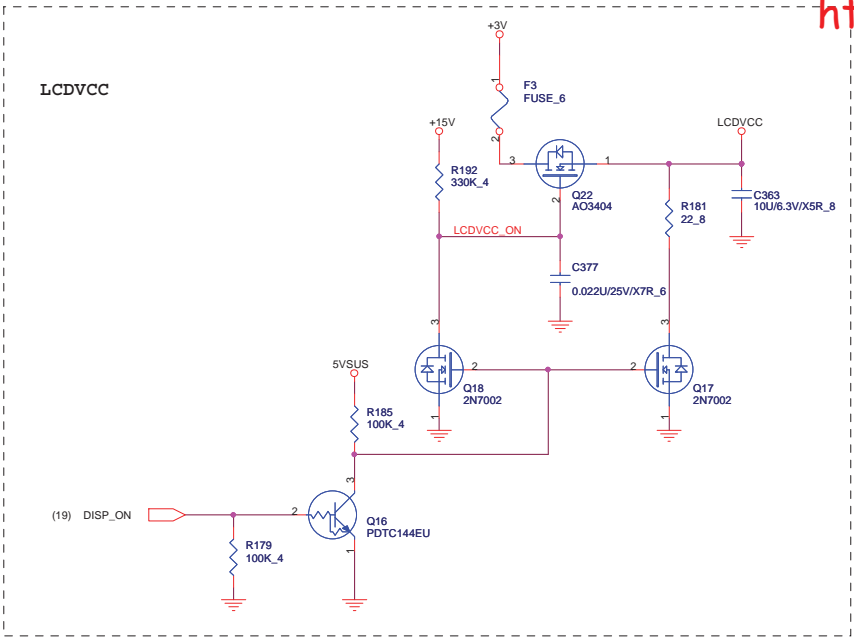
For PARK-S3 only
For M9X-S2/S3 with DDR3: this pin is not in use.

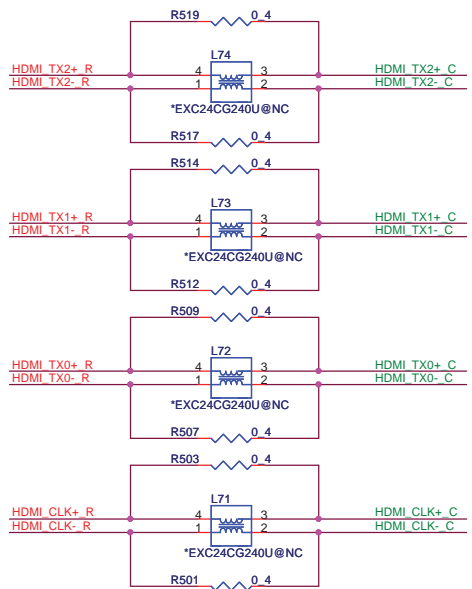


Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF

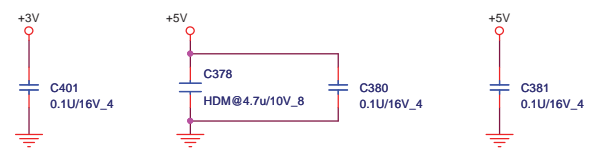
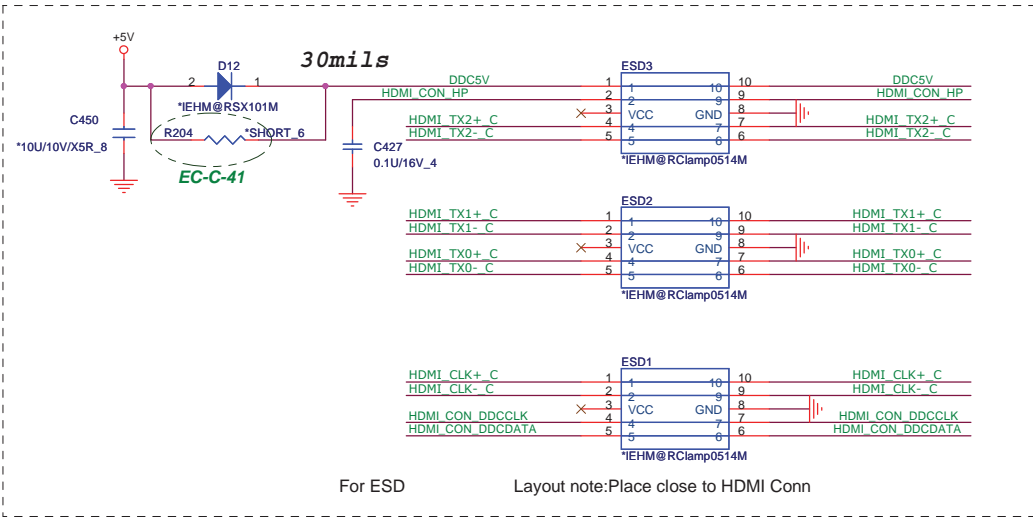
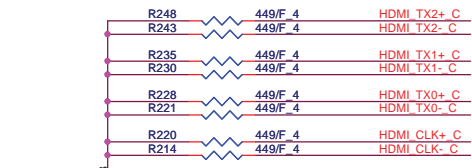
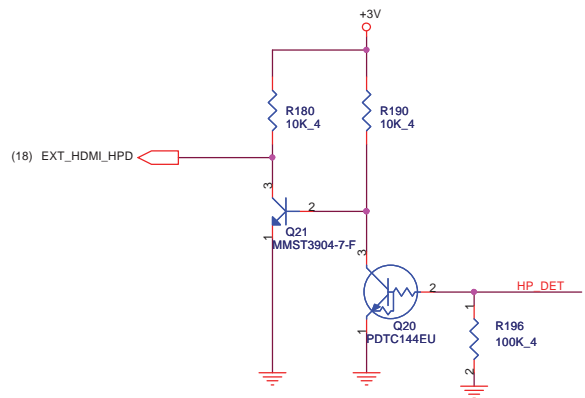
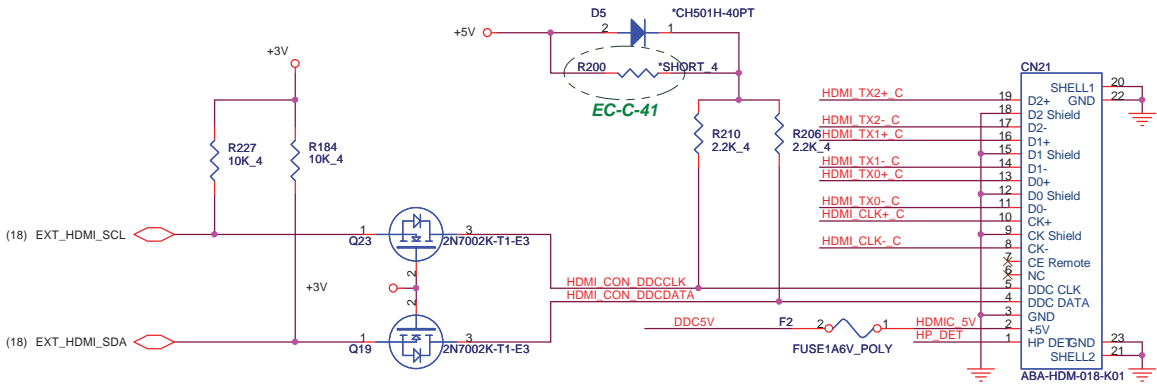
(21) VMA_MA[13..0] (21) VMA_MA[13..0] (21) VMA_DM[7..0] (21) VMA_DM[7..0] (21) VMA_DQ[63..0] (21) VMA_WDQS[7..0] (21) VMA_RDQS[7..0]

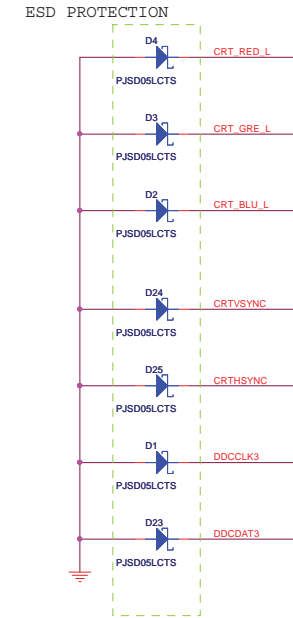
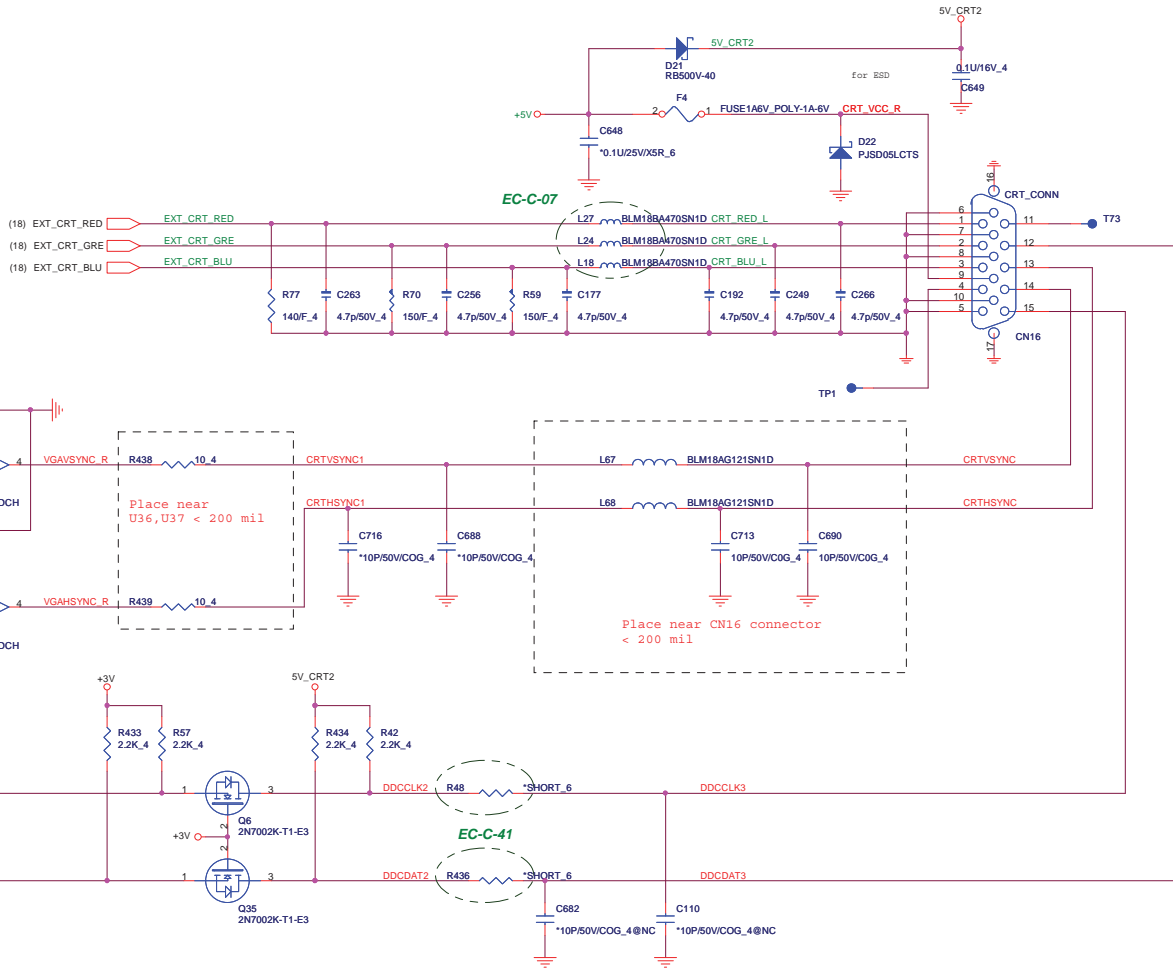






(18) EXT_HDMI_TXDP2	C783	0.1U/10V/X7R_4	HDMI TX2+ R
(18) EXT_HDMI_TXDN2	C782	0.1U/10V/X7R_4	HDMI TX2- R
(18) EXT_HDMI_TXDP1	C781	0.1U/10V/X7R_4	HDMI TX1+ R
(18) EXT_HDMI_TXDN1	C778	0.1U/10V/X7R_4	HDMI TX1- R
(18) EXT_HDMI_TXDP0	C776	0.1U/10V/X7R_4	HDMI TX0+ R
(18) EXT_HDMI_TXDN0	C773	0.1U/10V/X7R_4	HDMI TX0- R
(18) EXT_HDMI_TXCP	C770	0.1U/10V/X7R_4	HDMI CLK+ R
(18) EXT_HDMI_TXCN	C788	0.1U/10V/X7R_4	HDMI CLK- R

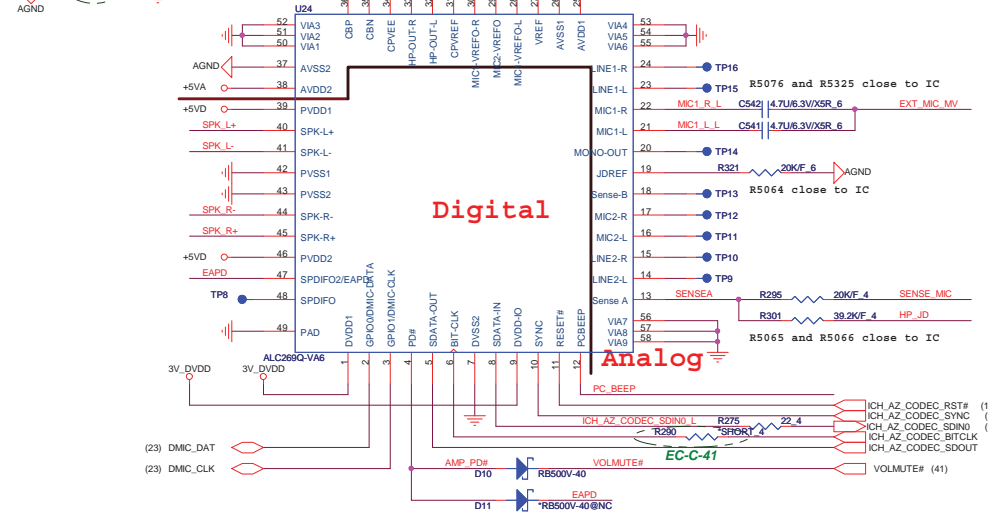




Quanta Computer Inc.
 PROJECT : LD-Note AMD DIS

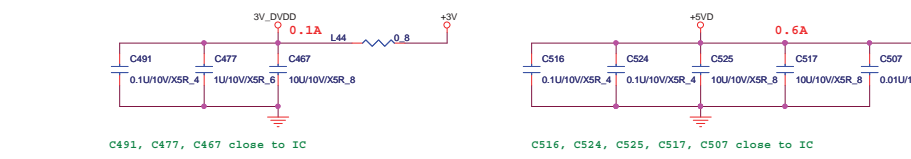
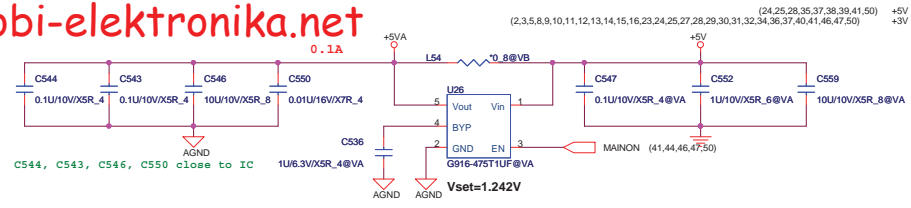
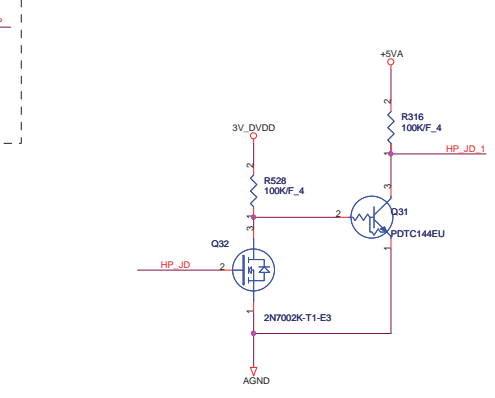
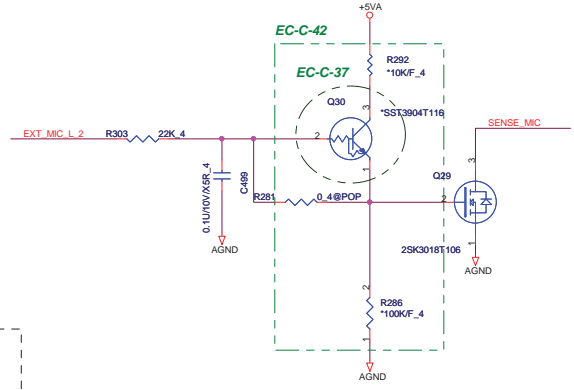
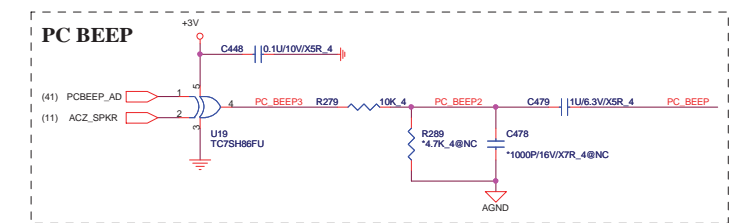
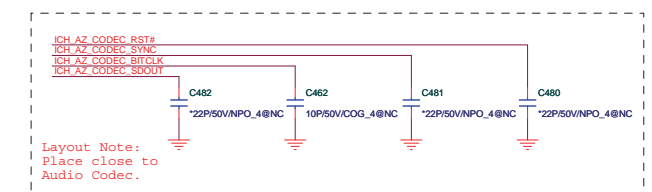
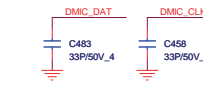
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Date:	Wednesday, June 09, 2010	Sheet 25 of 55

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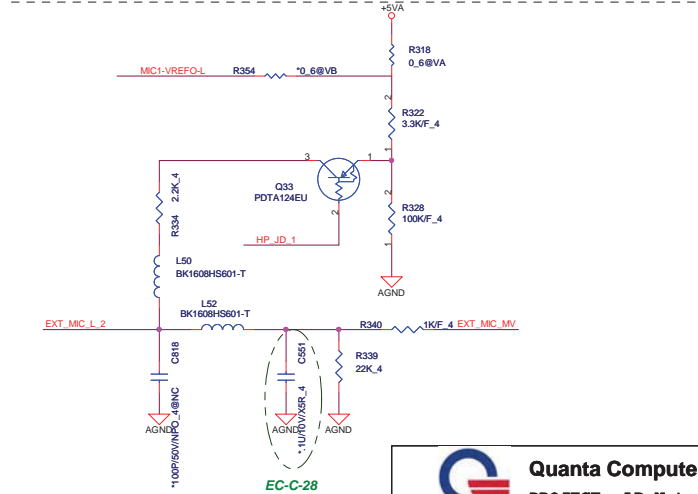
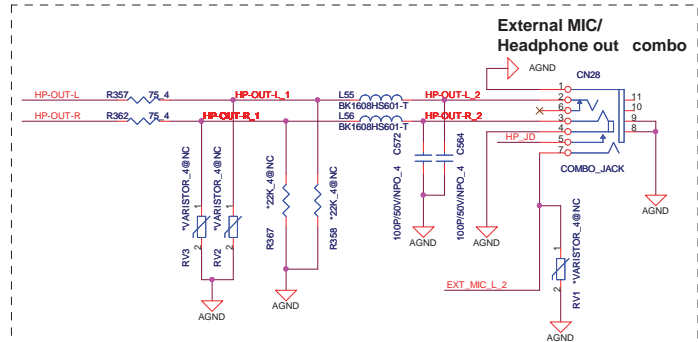
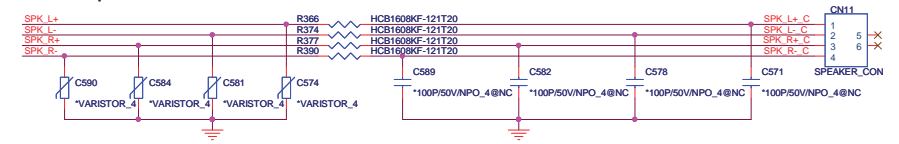


Digital

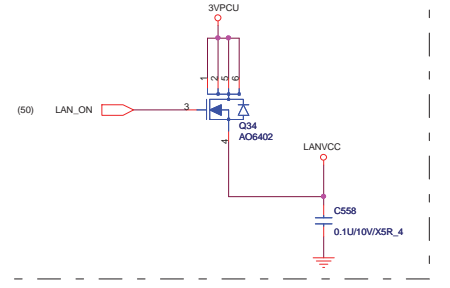
Analog



Internal Speaker

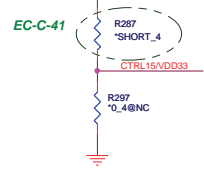
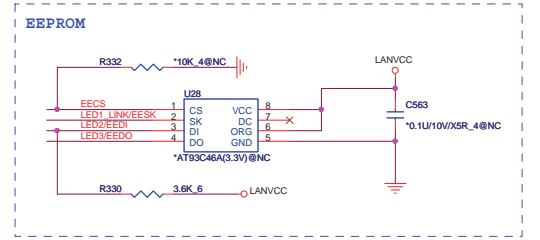
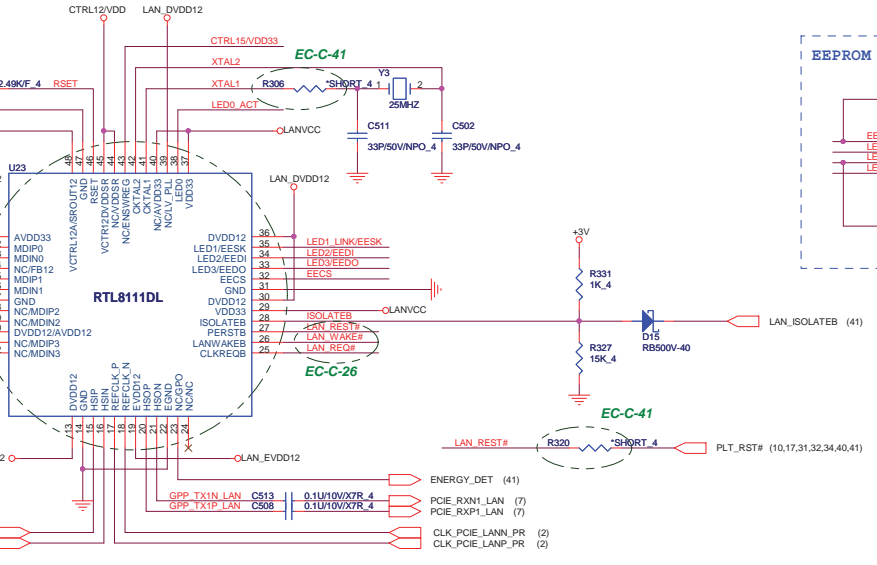
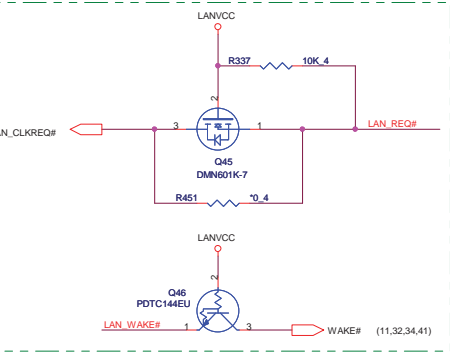


LANVCC



寬>60mils,長<200mils

EC-C-26

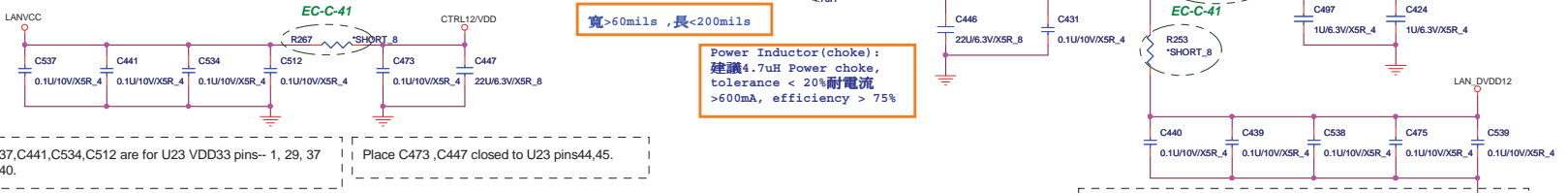


3.3V : Enable switching regulator
OV : Disable switching regulator

寬>40mils,長<200mils

寬>60mils,長<200mils

Power Inductor (choke):
建議4.7uH Power choke,
tolerance < 20%耐電流
>600mA, efficiency > 75%



Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

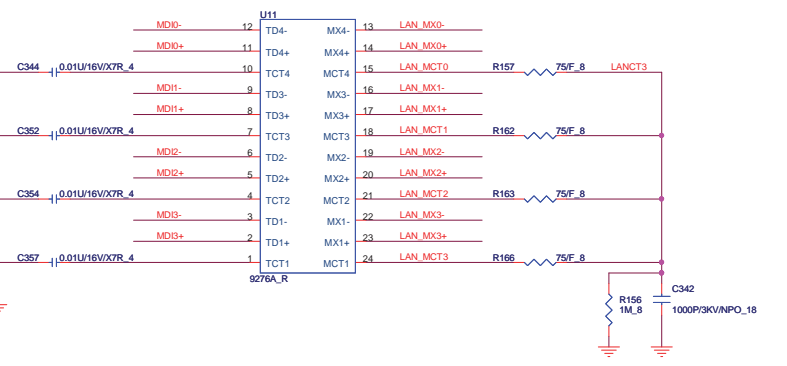
* C537,C441,C534,C512 are for U23 VDD33 pins-- 1, 29, 37 and 40.

Place C473, C447 closed to U23 pins44,45.

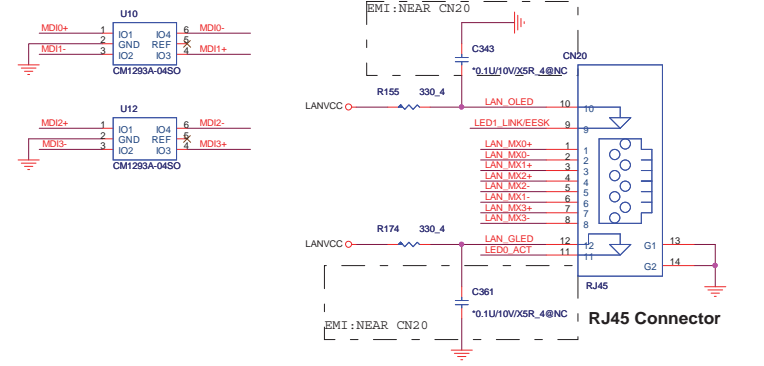
* C497 and C424 are for U23 EVDD12 pin 19.

C440,C439,C538,C475,C539 are for U23 VDD12 pins-- 10, 13, 30, 36, 39.

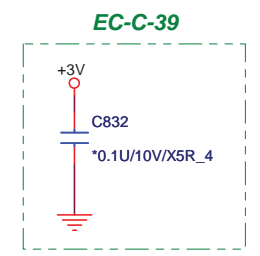
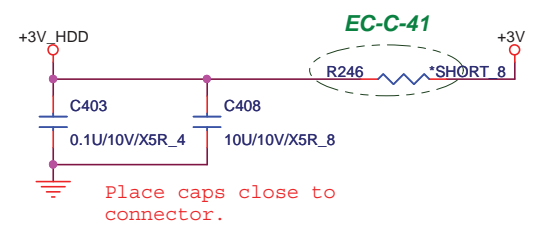
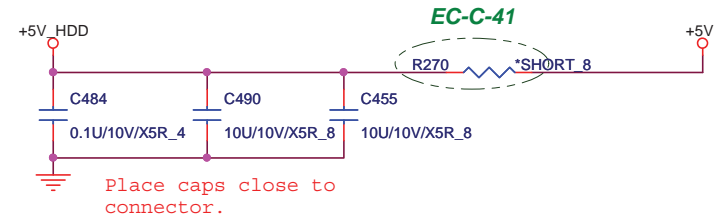
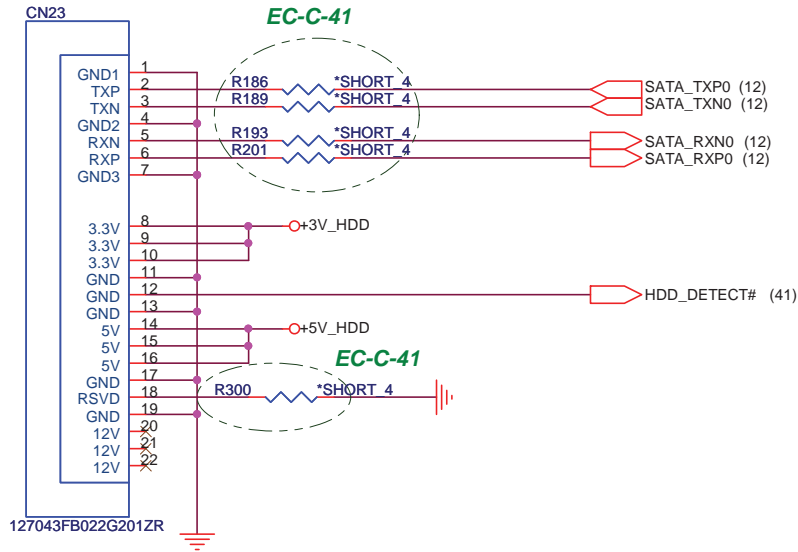
Transformer



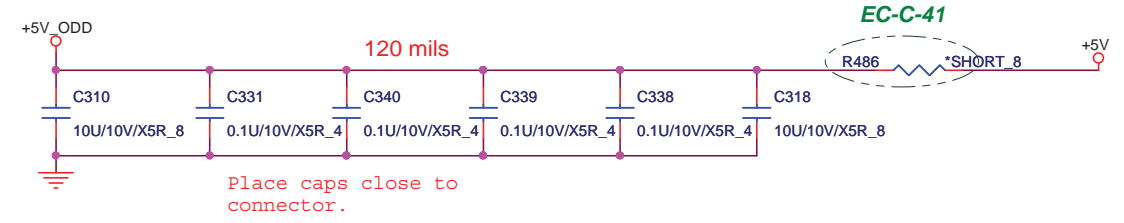
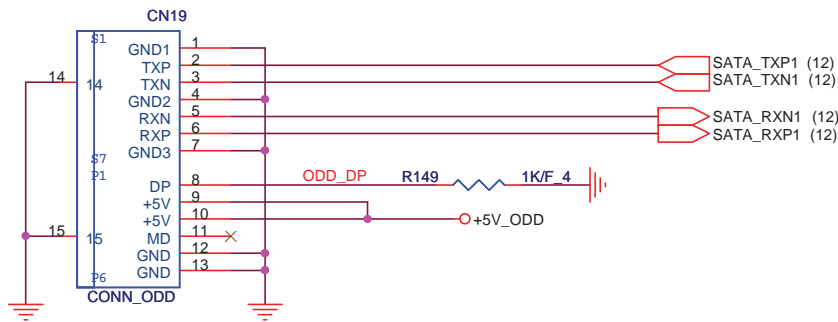
RJ45 Connector



SATA HDD Connector.



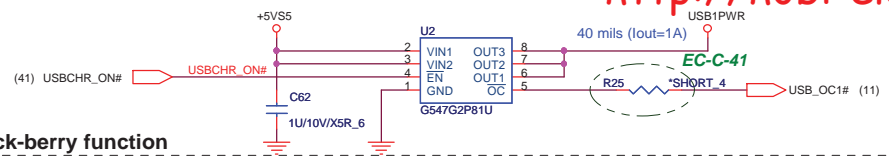
ODD Connector



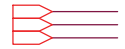
Quanta Computer Inc.
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	1A
Date:	Wednesday, June 09, 2010	Sheet 28 of 55

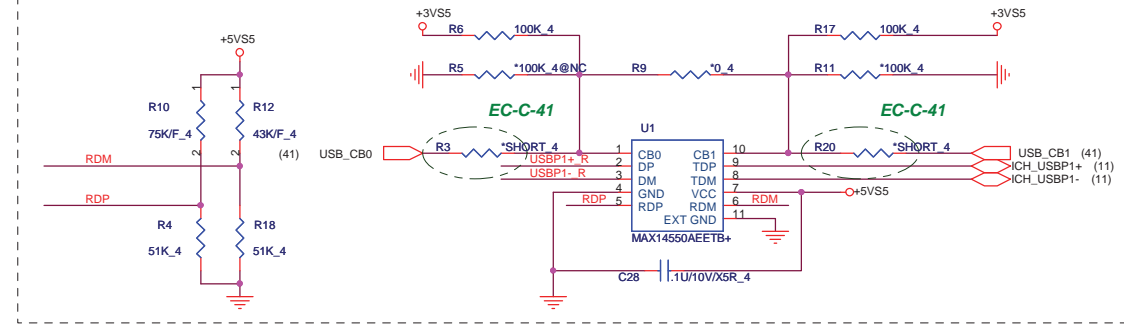
USBX1



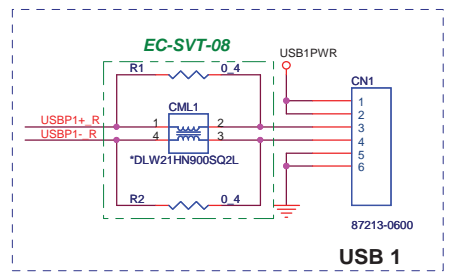
(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,30,31,32,34,36,37,40,41,46,47,50)
(5,10,11,12,13,14,32,50)



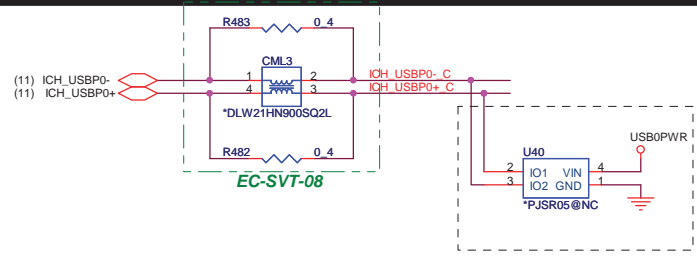
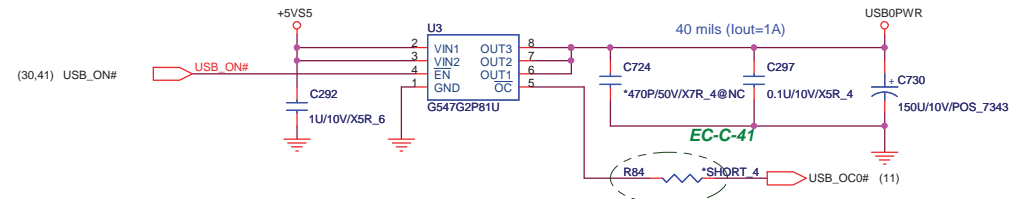
Support Black-berry function



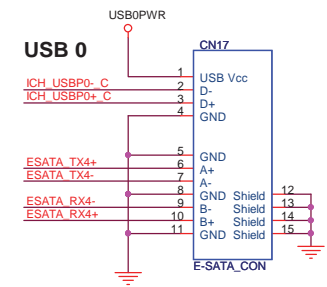
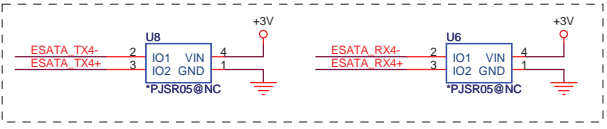
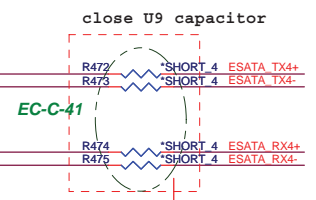
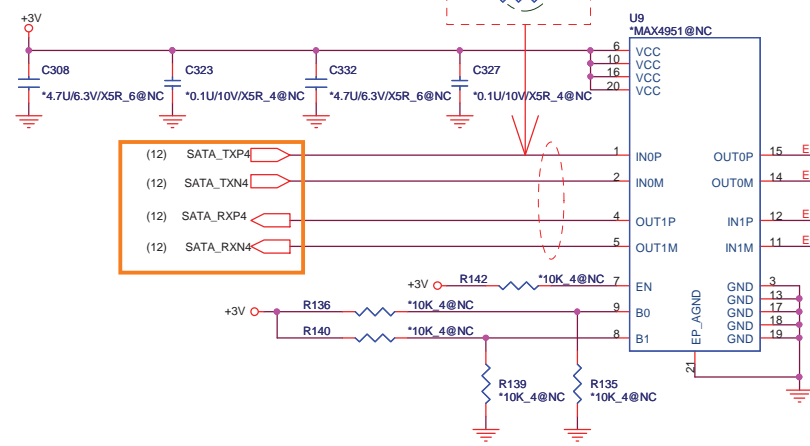
USB X1---> Wire to board conn



USB + E-SATA

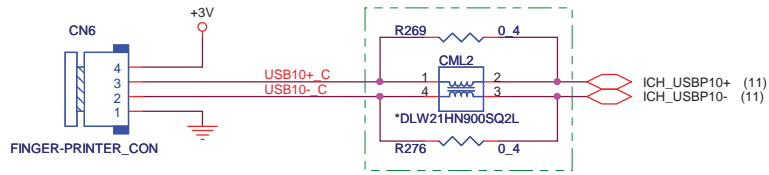


E-SATA RE-DRIVER

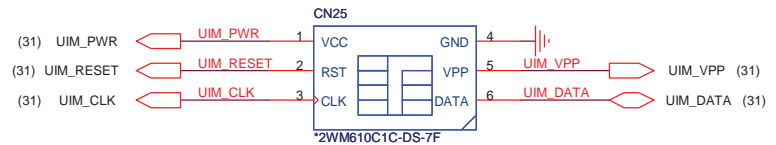


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

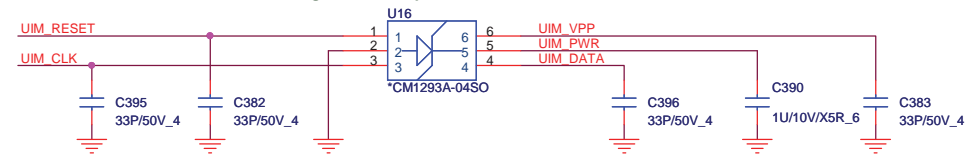
Finger Print



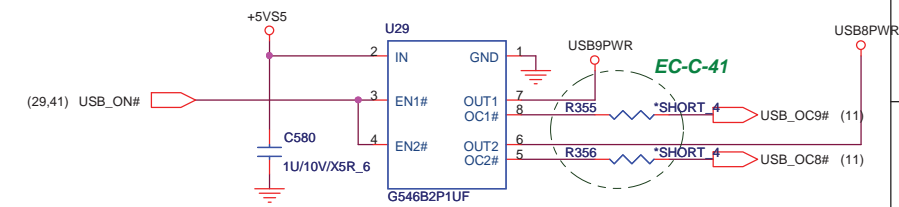
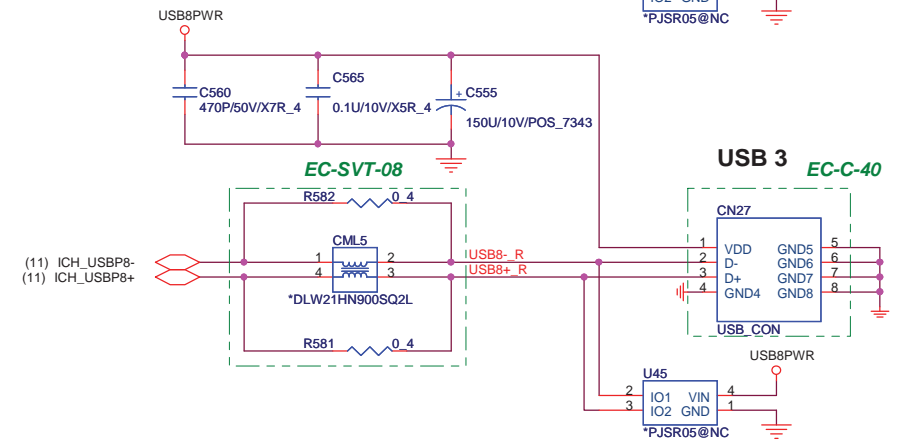
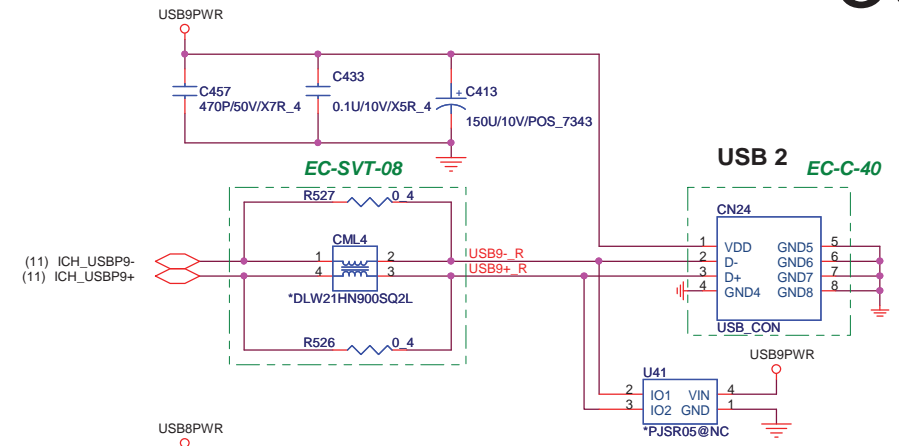
SIM Card CONN



Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible



FRONT LEDs

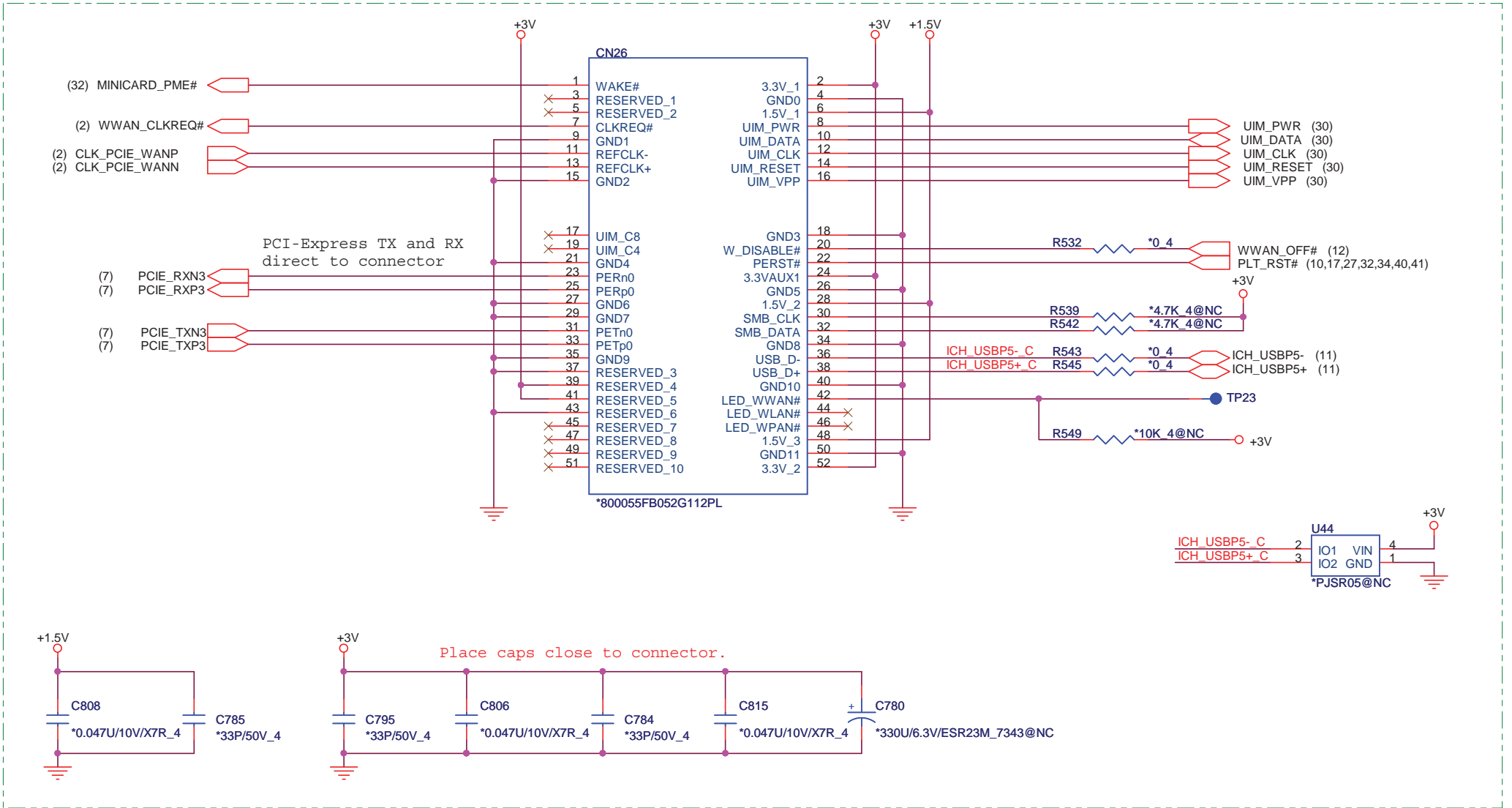


Quanta Computer Inc.
PROJECT : LD-Note AMD DIS

Size	Document Number	Rev
	USB X2/SIM_CARD/LEDs/RF	1A
Date:	Wednesday, June 09, 2010	Sheet 30 of 55

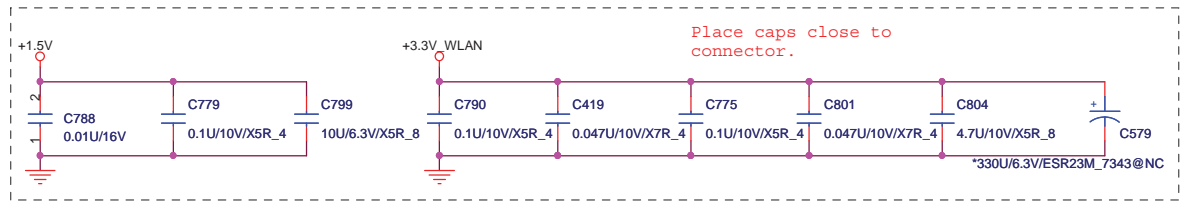
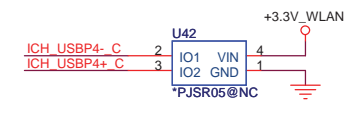
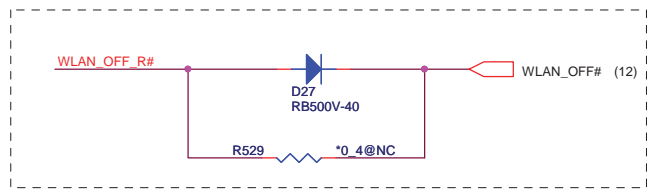
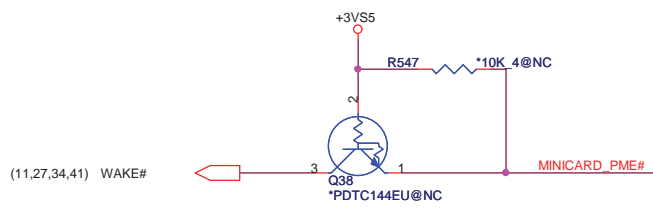
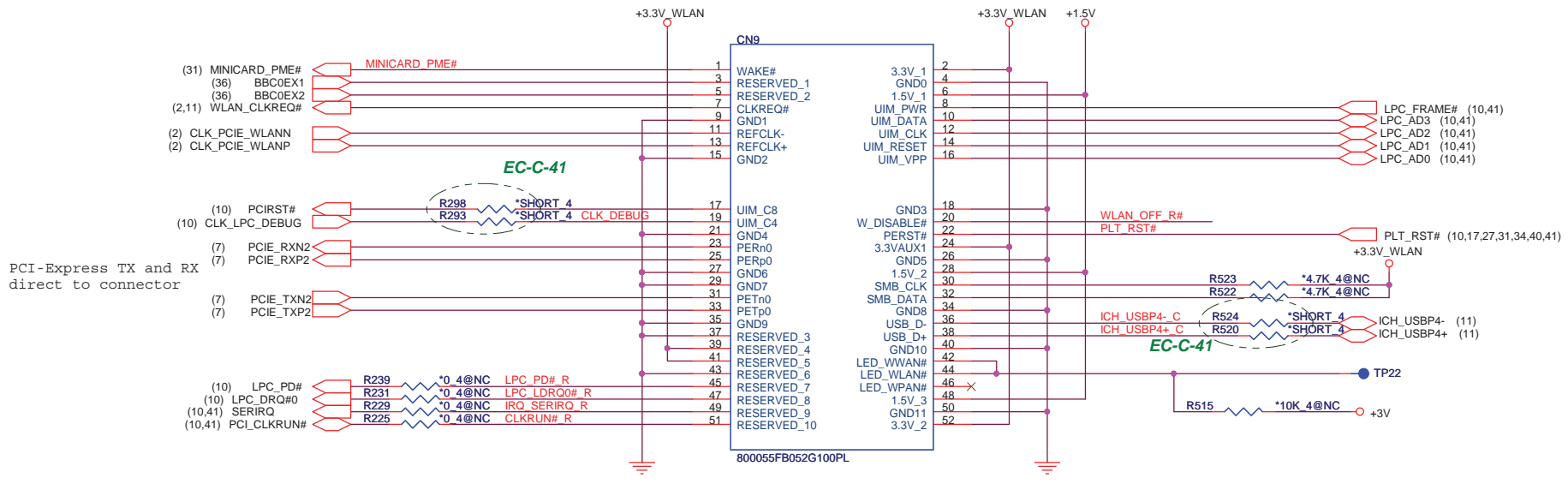
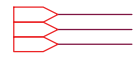
MiniCard WWAN connector

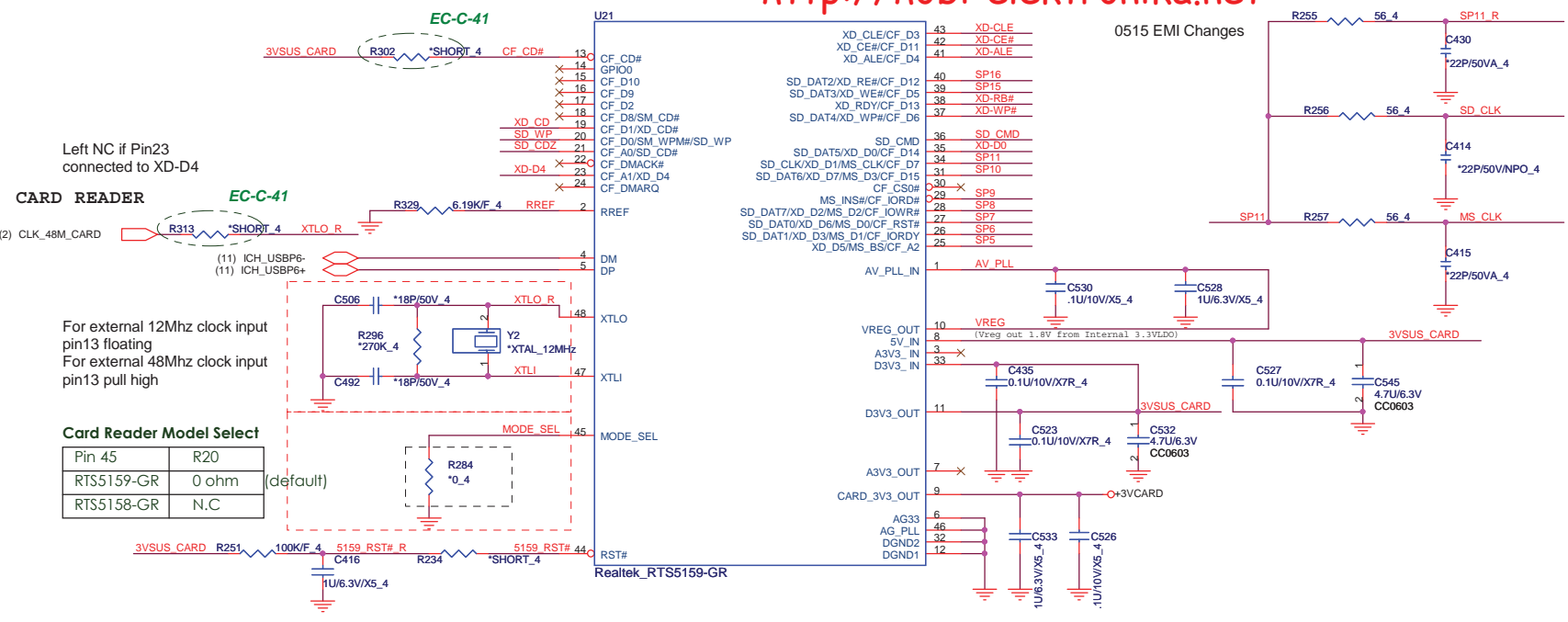
EC-C-30



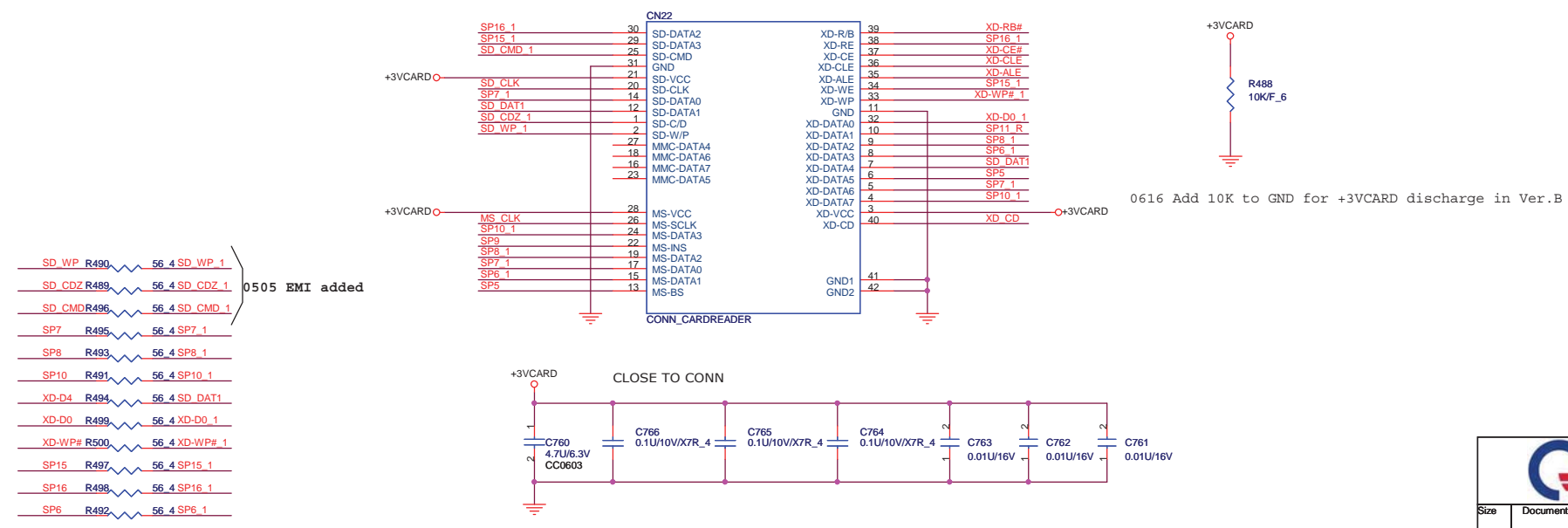
Quanta Computer Inc.
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	MINI-Card (UWB, WWAN)	1A
Date:	Wednesday, June 09, 2010	Sheet 31 of 55





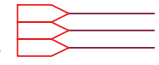
7 in 1 Socket (MS, MS PRO, SD, MMC, xD)



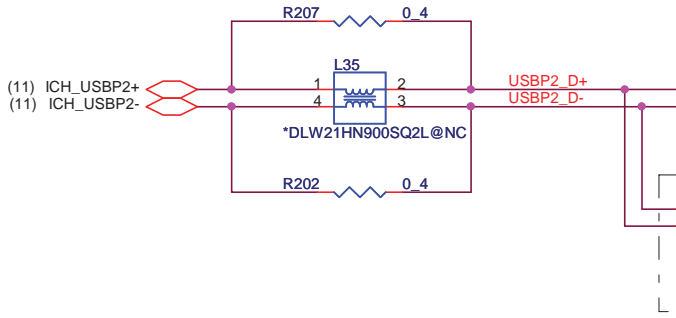
Express Card

<http://hobi-elektronika.net>

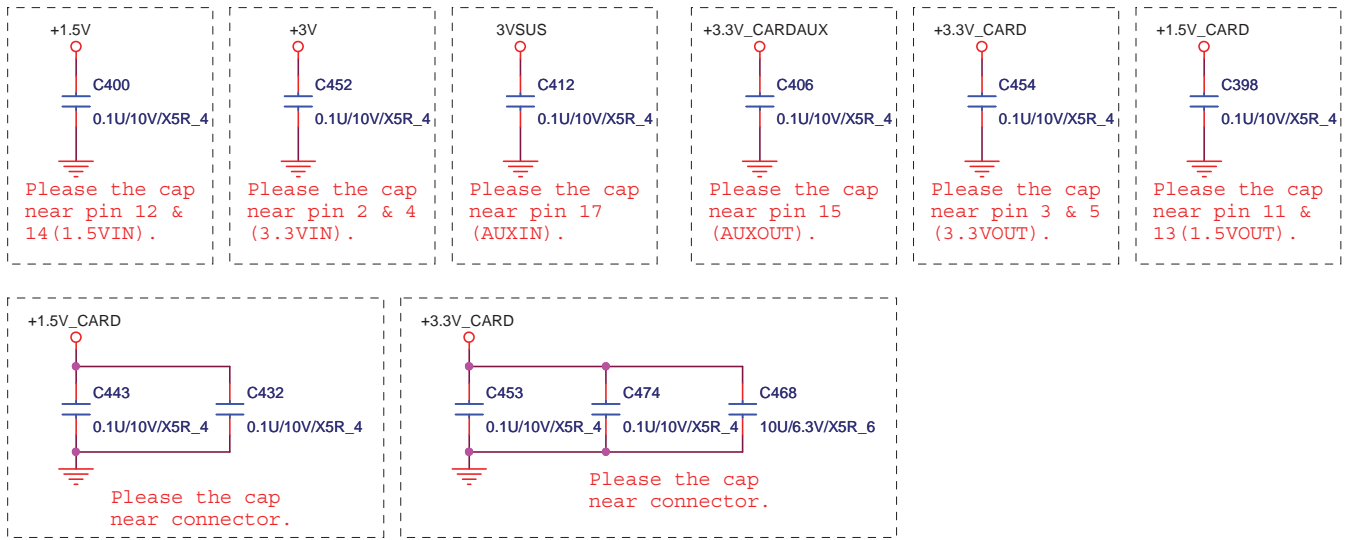
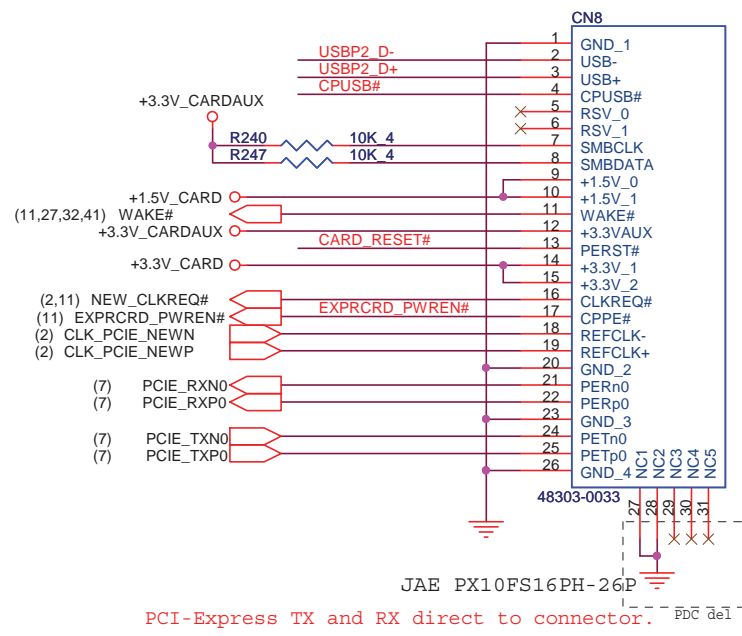
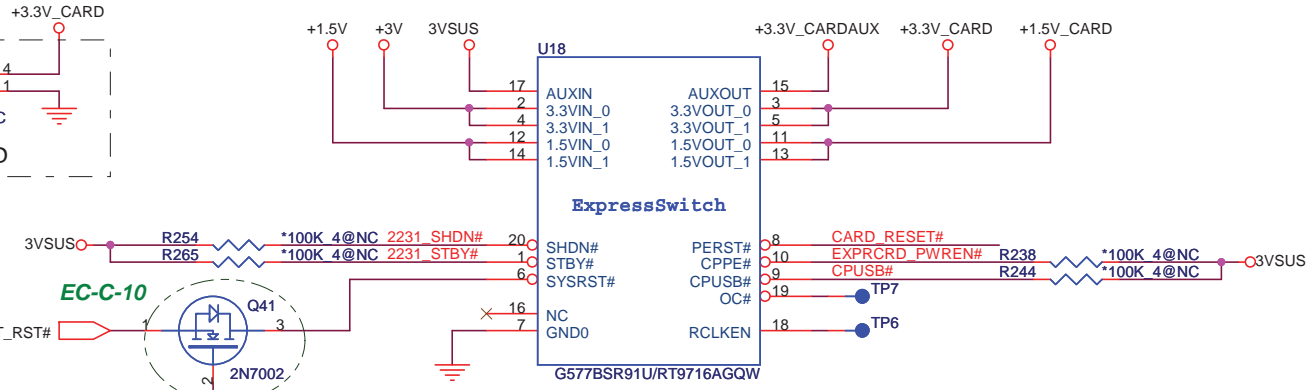
(2,3,6,8,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,36,37,40,41,46,47,50) +3V
 (3,8,31,32,50) +1.5V
 (30,33,41,46,47,49,50) 3VSUS




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+1.5V_CARD Max. 650mA, Average 500mA.
 +3V_CARD Max. 1300mA, Average 1000mA.



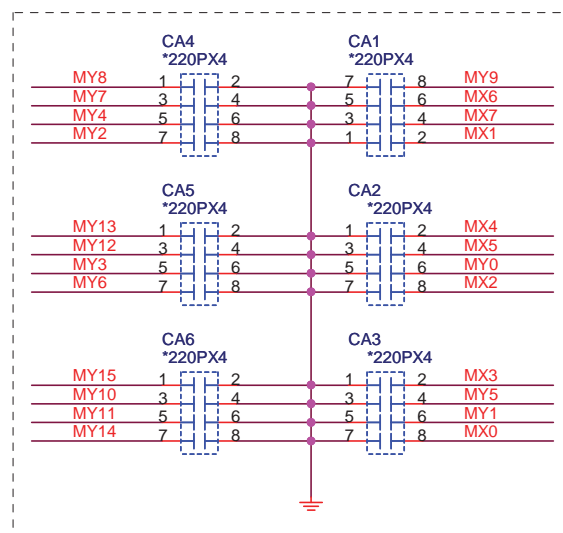
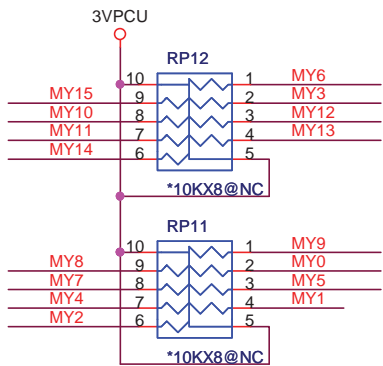
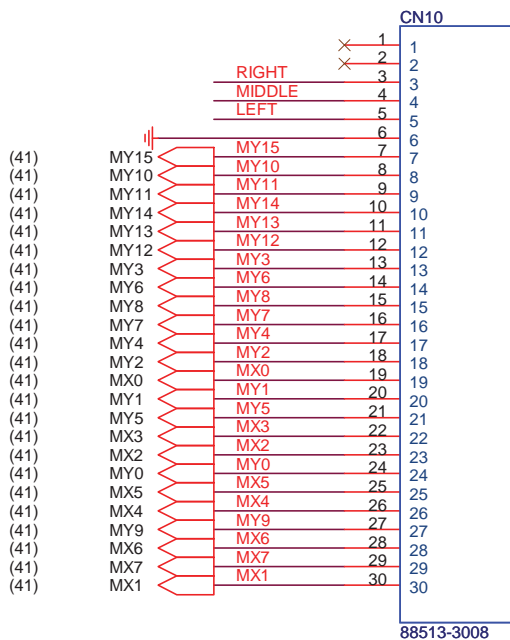


Quanta Computer Inc.
 PROJECT : LD-Note AMD DIS

Size	Document Number	Rev
	Express Card	1A
Date:	Wednesday, June 09, 2010	Sheet 34 of 55

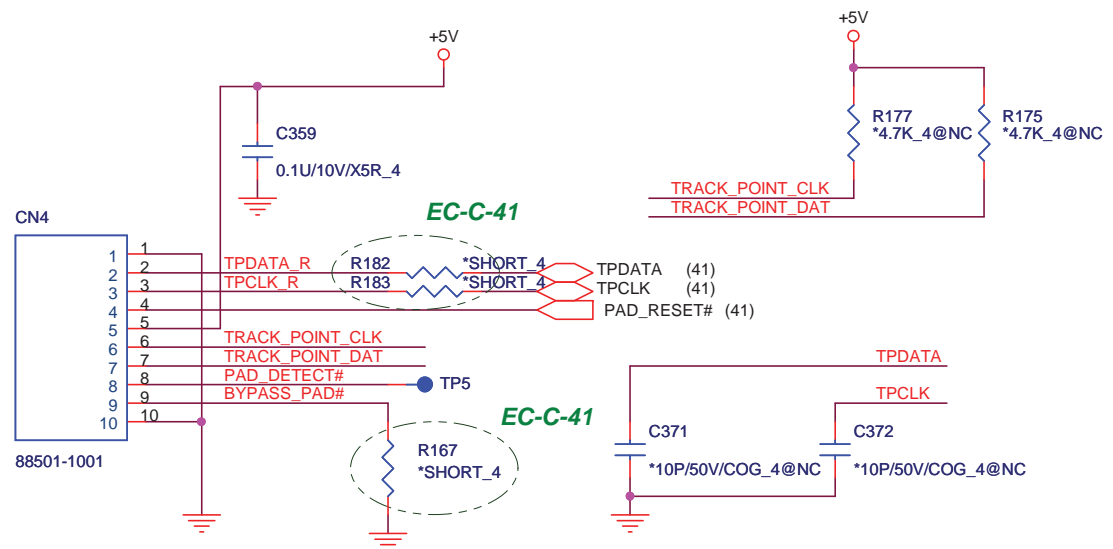


KEYBOARD connector



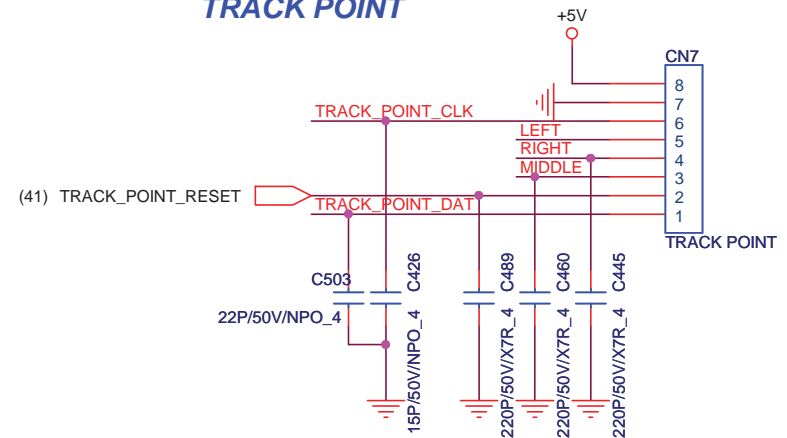
For EMI request

Touch pad



Place C371 ,C372 closed to CN4

TRACK POINT



Quanta Computer Inc.
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	K/B, T/P	1A
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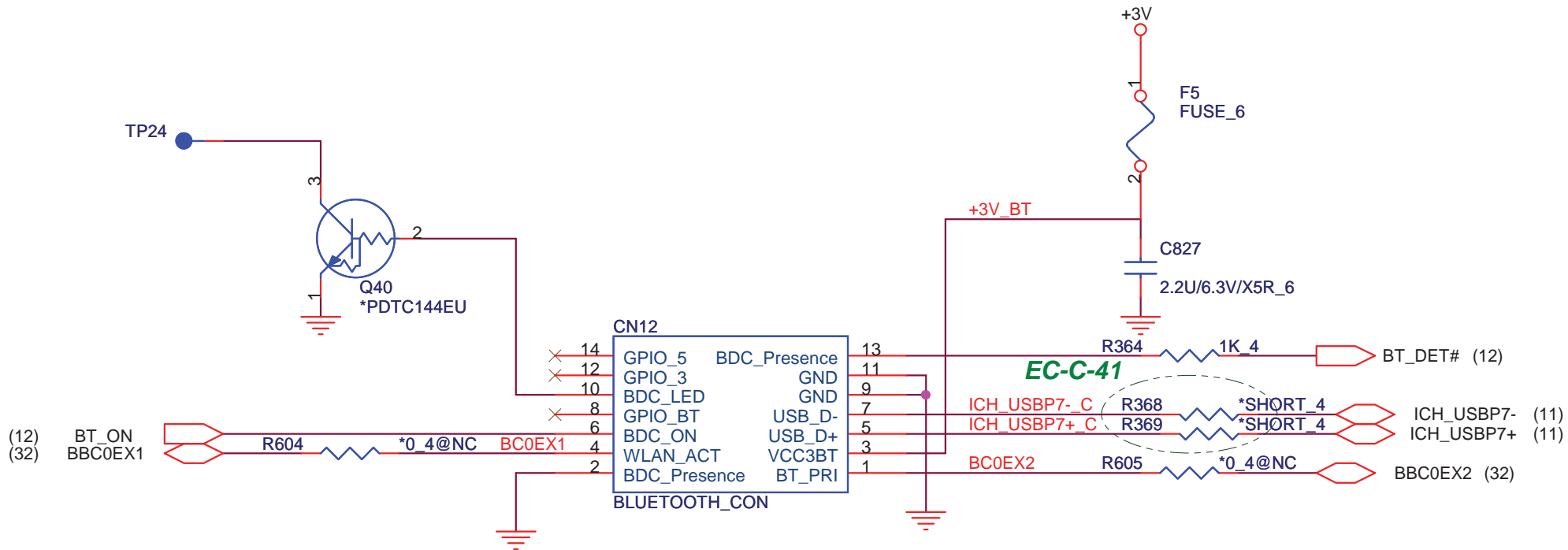
BLUETOOTH

<http://hobi-elektronika.net>

(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,37,40,41,46,47,50)

+3V

36

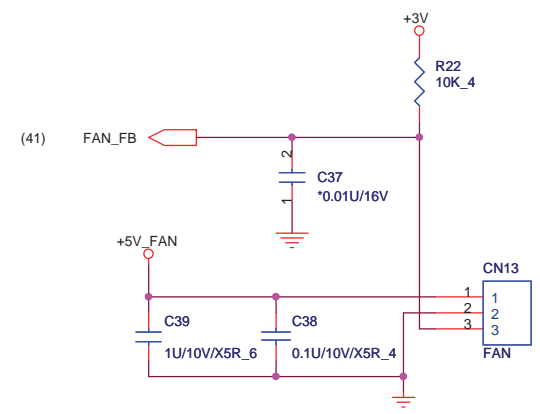
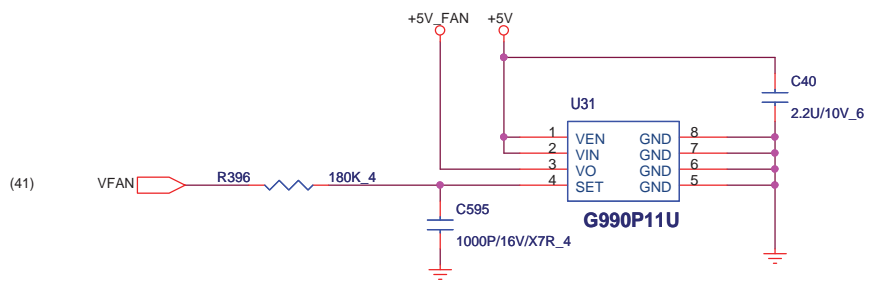



Quanta Computer Inc.

PROJECT : LD-Note AMD DIS

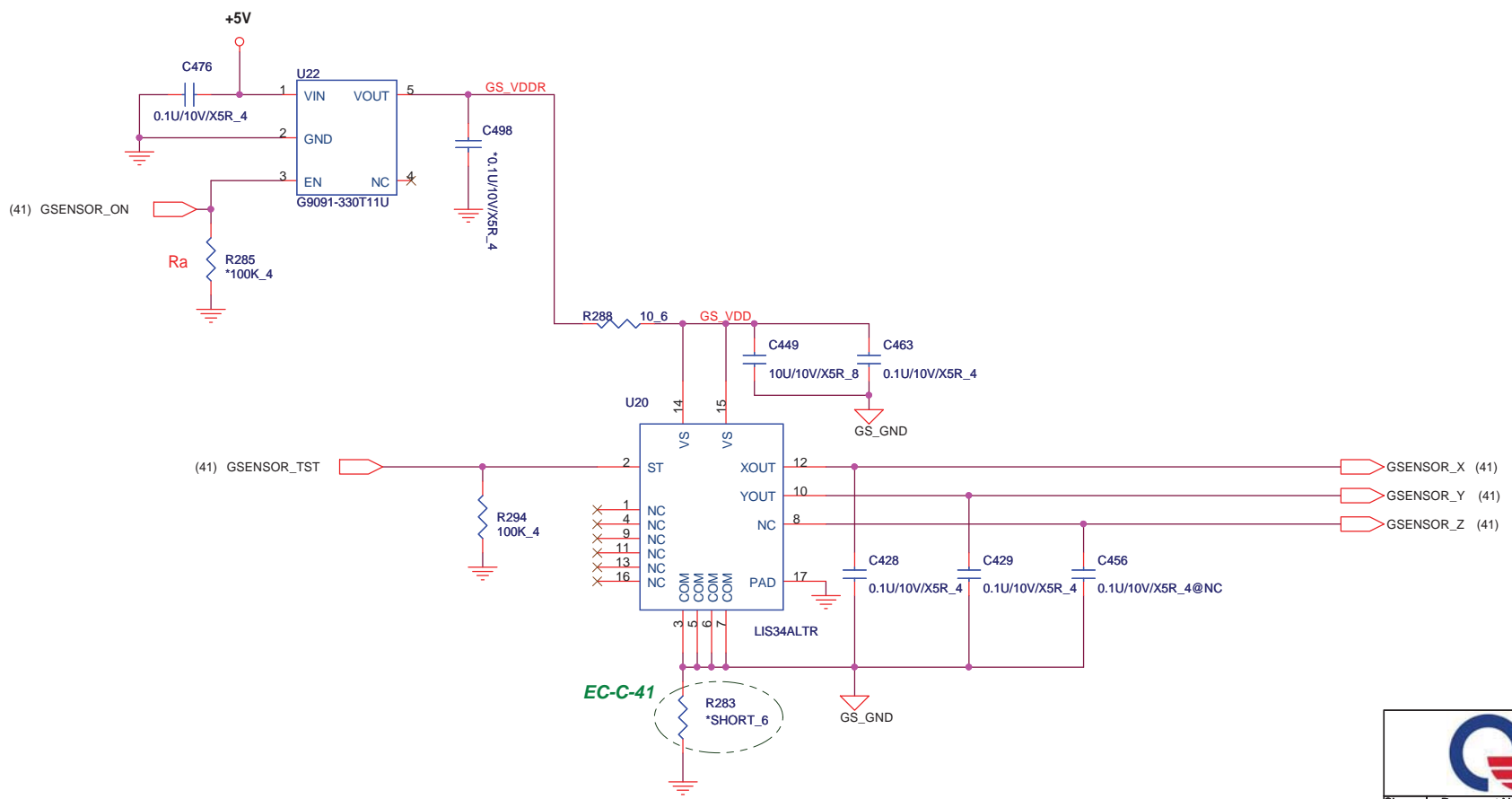
Size	Document Number B/T	Rev 1A
Date:	Wednesday, June 09, 2010	Sheet 36 of 55


FAN CONTROL



 Quanta Computer Inc. PROJECT : LD-Note AMD DIS		Rev
		1A
Size	Document Number	
FAN & THERMAL		
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G-SENSOR (3-Axial)



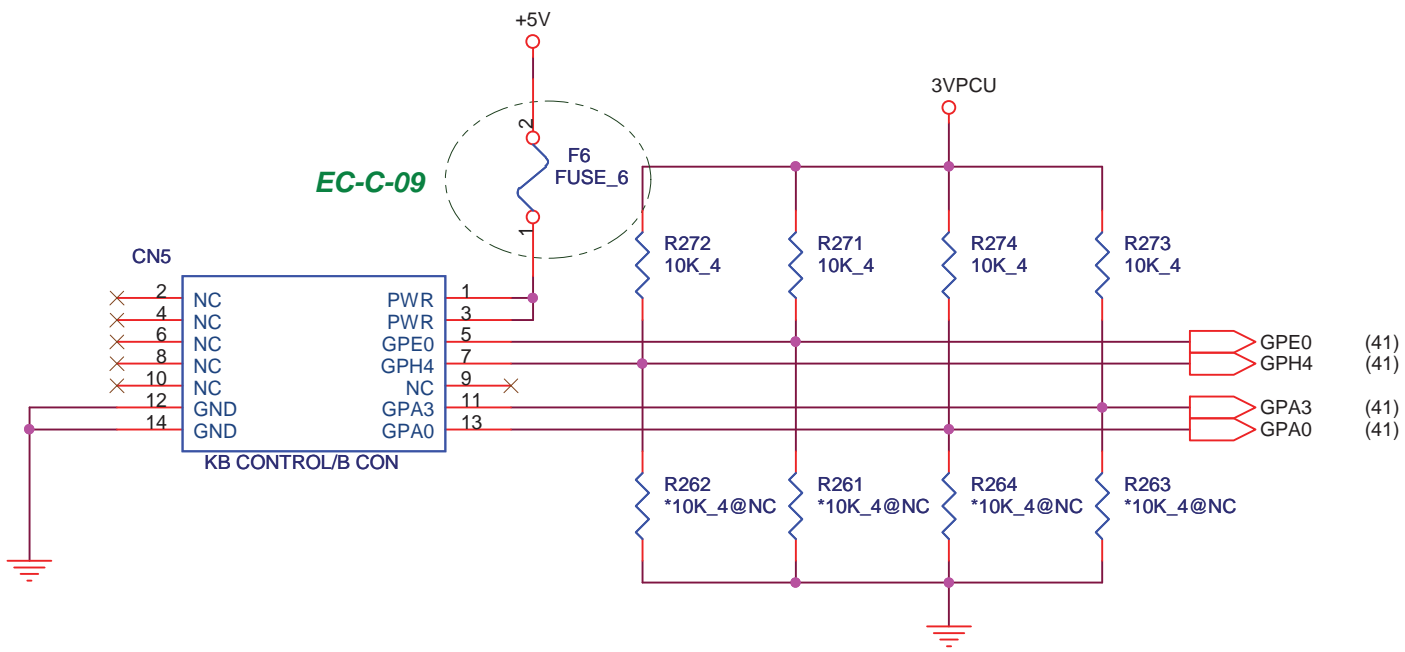
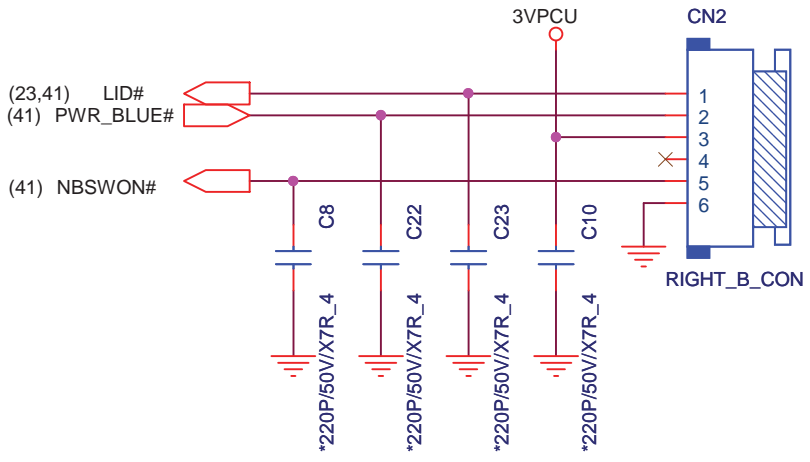
		Quanta Computer Inc.
		PROJECT : LD-Note AMD DIS
Size	Document Number	Rev
	G-SENSOR	1A
Date:	Wednesday, June 09, 2010	Sheet 38 of 55


FFC TO B LED RIGHT SIDE CONNECTOR

<http://hobi-elektronika.net>

(10,23,27,35,41,43,44,45,46,47,48,50) 3VPCU

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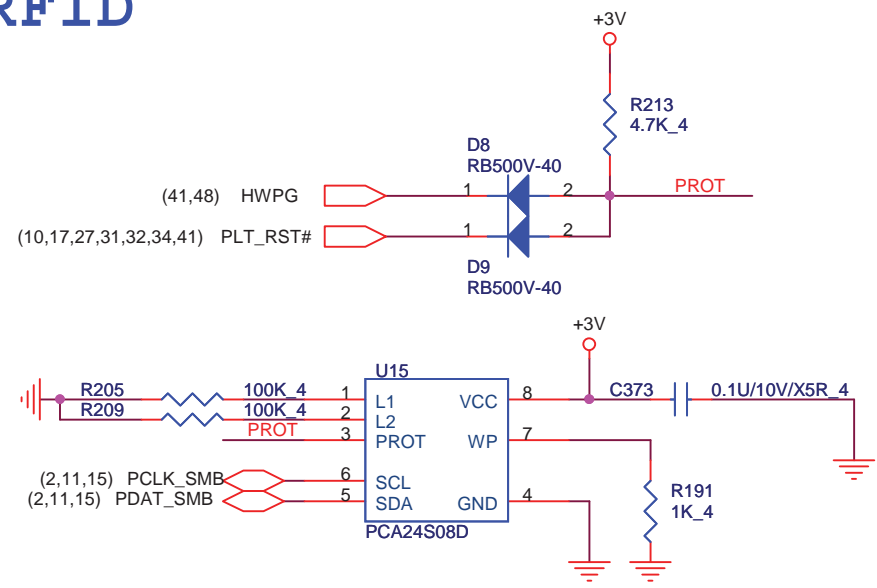


Quanta Computer Inc.
PROJECT :LD-Note AMD DIS

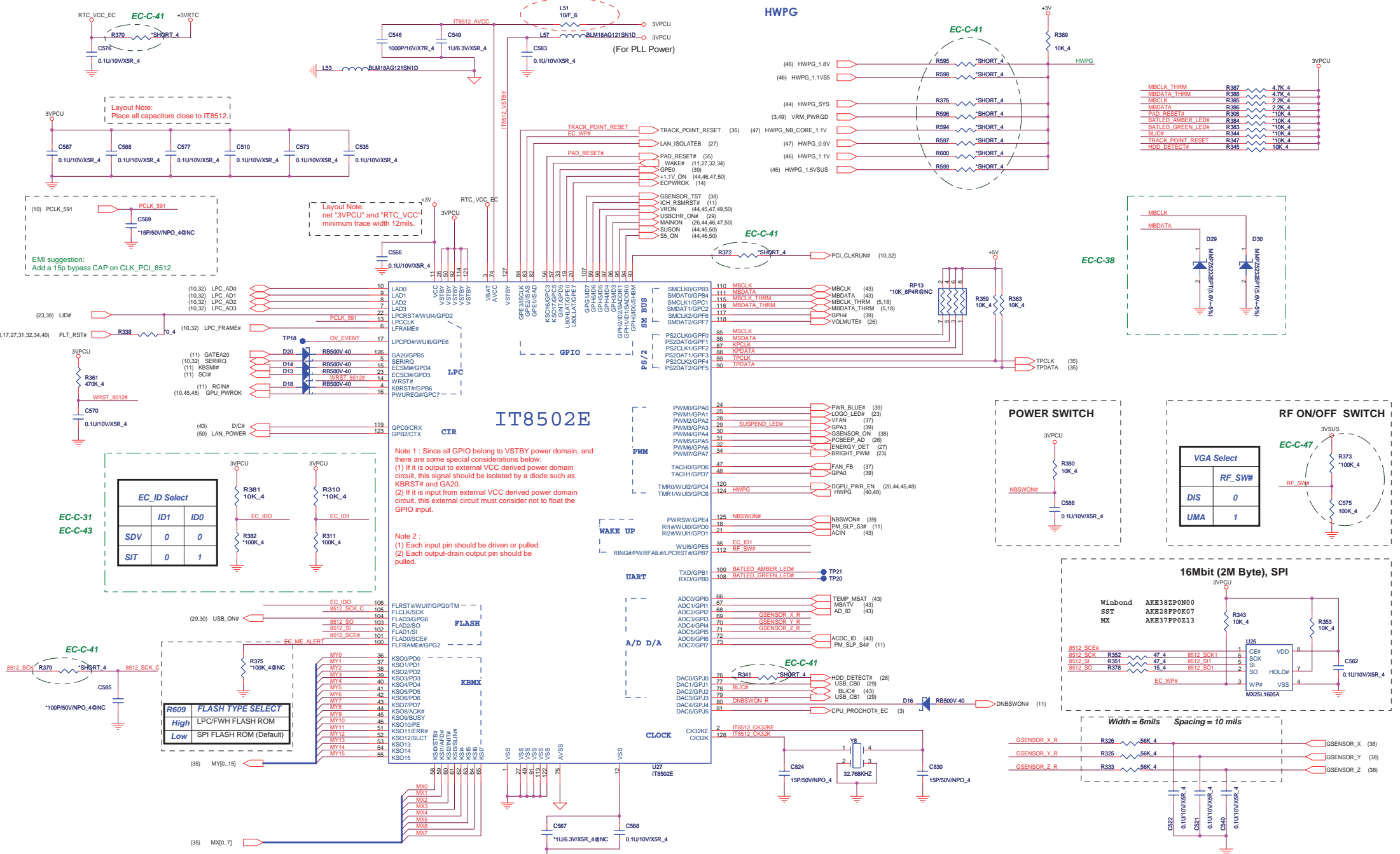
Size	Document Number	Rev
	B TO B CON	1A
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RFID



		Quanta Computer Inc.
		PROJECT :LD-Note AMD DIS
Size	Document Number	Rev 1A
RFID EEPROM		
Date:	Wednesday, June 09, 2010	Sheet 40 of 55



Layout Note: Place all capacitors close to IT8512.

Layout Note: net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

EMI suggestion: Add a 15p bypass CAP on CLK_PCL_8512

(10,17,27,31,32,34,40) PLT_RST#

EC-C-31 EC-C-43

EC-C-41

MX0-MX7

IT8502E

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

HWPG

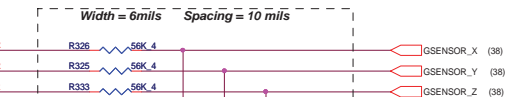
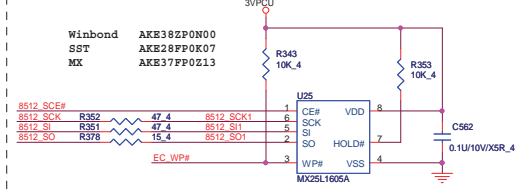
EC-C-41

EC-C-38

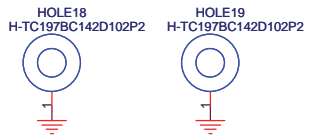
POWER SWITCH

RF ON/OFF SWITCH

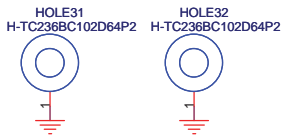
16Mbit (2M Byte), SPI



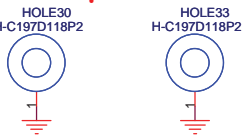
MiniCard WLAN



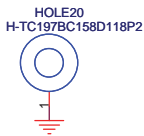
MiniCard WWAN



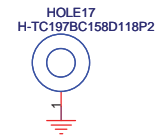
Hole for SB support



Blue nut

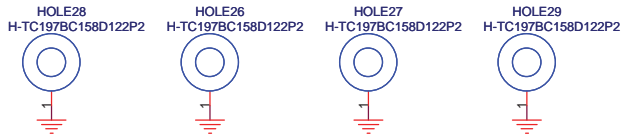


E/L KB nut

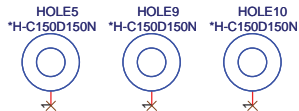


42

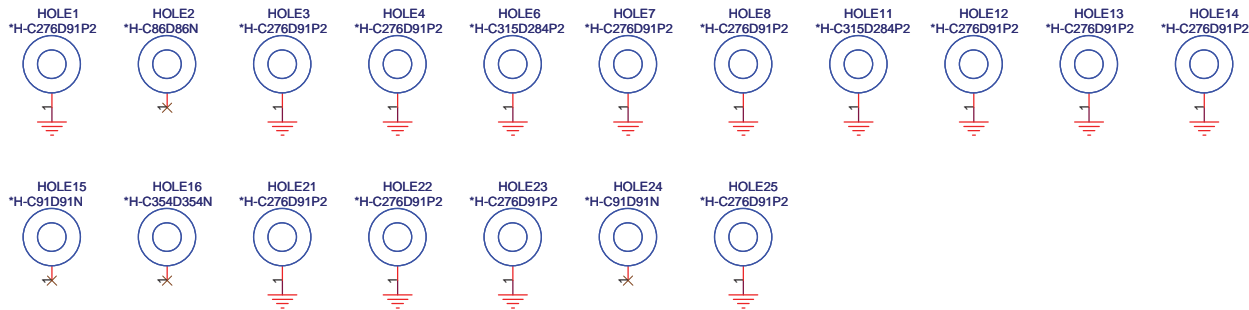
VGA NUT



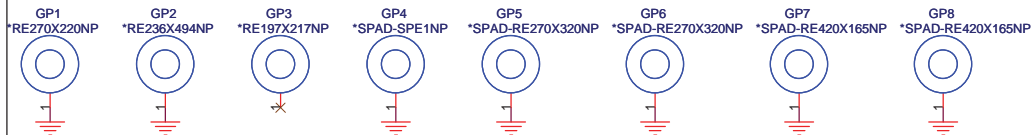
Hole for CPU support



Boundary Hole



PAD



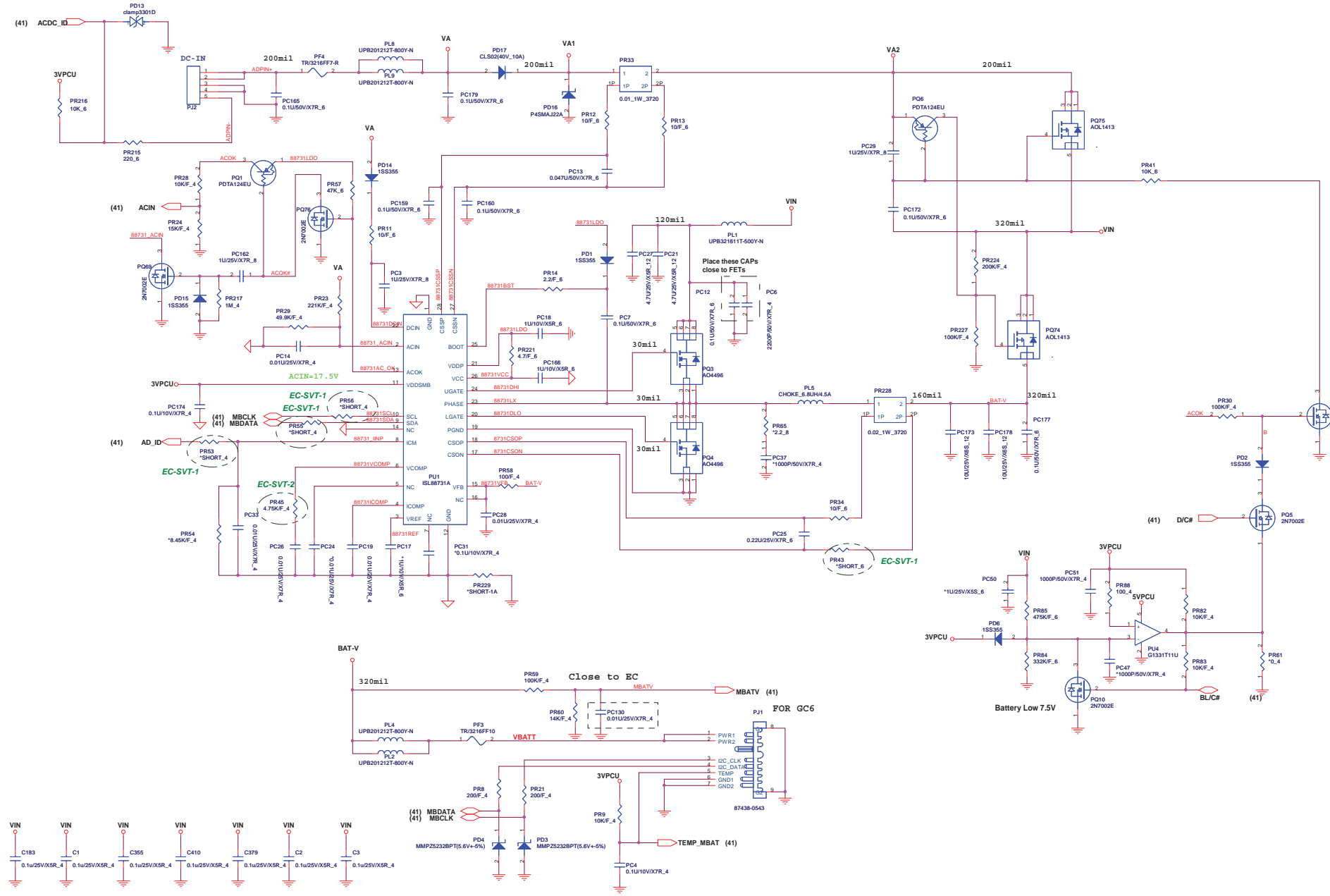
Quanta Computer Inc.

PROJECT :LD-Note AMD DIS

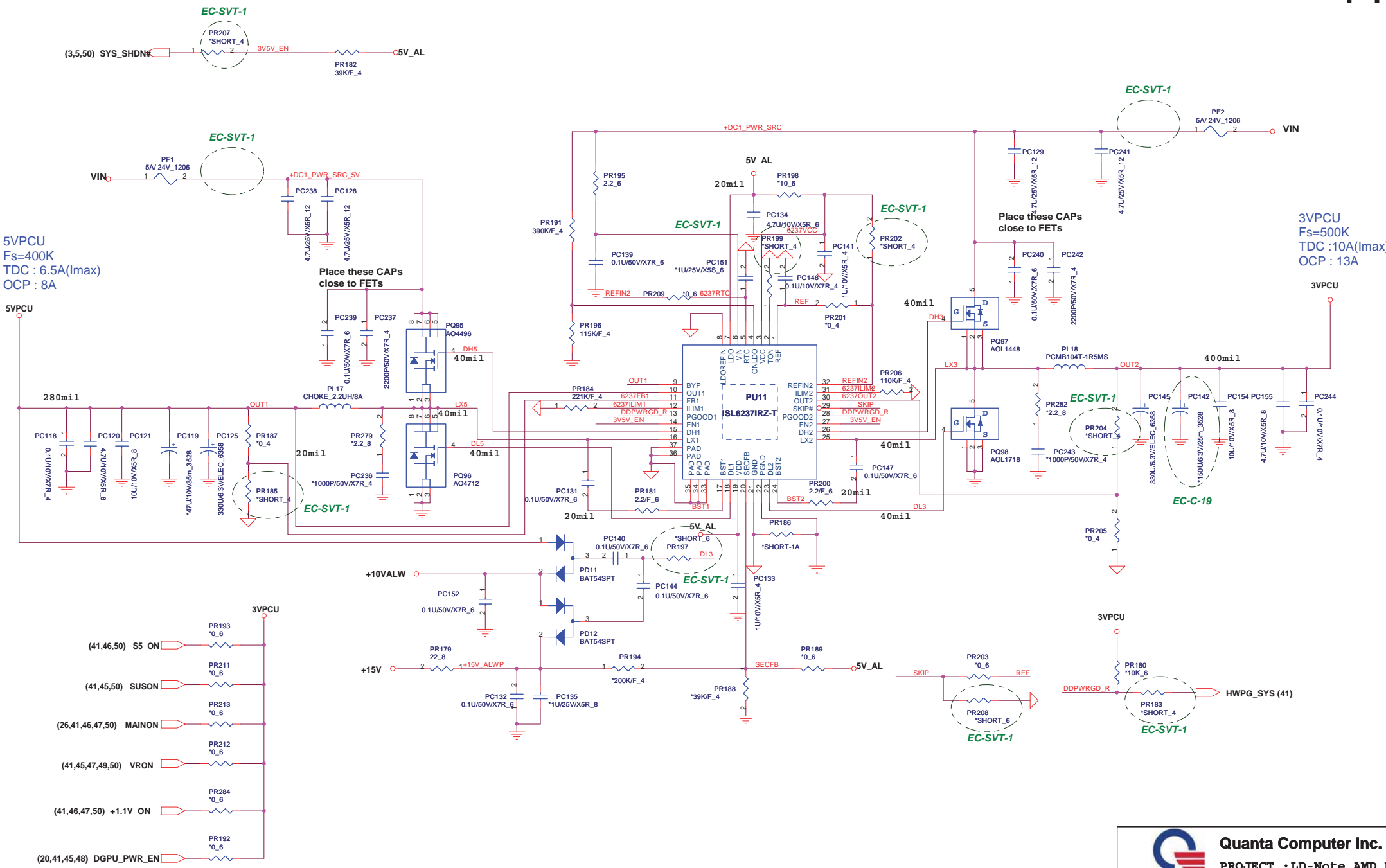
Size Document Number Rev

HOLD & SKEW 1A

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EMI Bypass capacitor



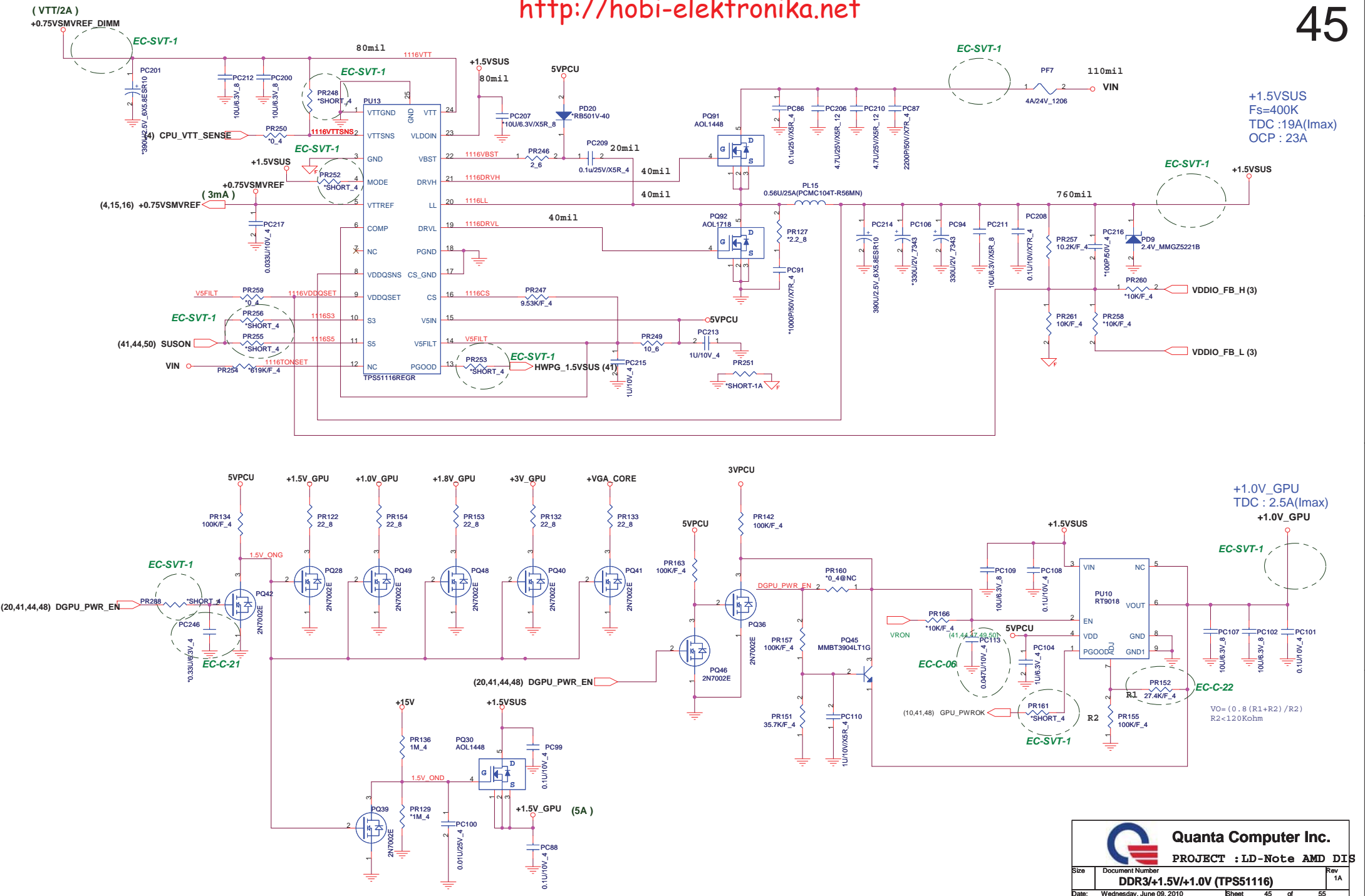
5VPCU
Fs=400K
TDC : 6.5A(I_{max})
OCP : 8A

Place these CAPs close to FETs

3VPCU
Fs=500K
TDC : 10A(I_{max})
OCP : 13A

Quanta Computer Inc.
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	3V/5V (ISL6237)	1A
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+1.5VSUS
 Fs=400K
 TDC : 19A(I_{max})
 OCP : 23A

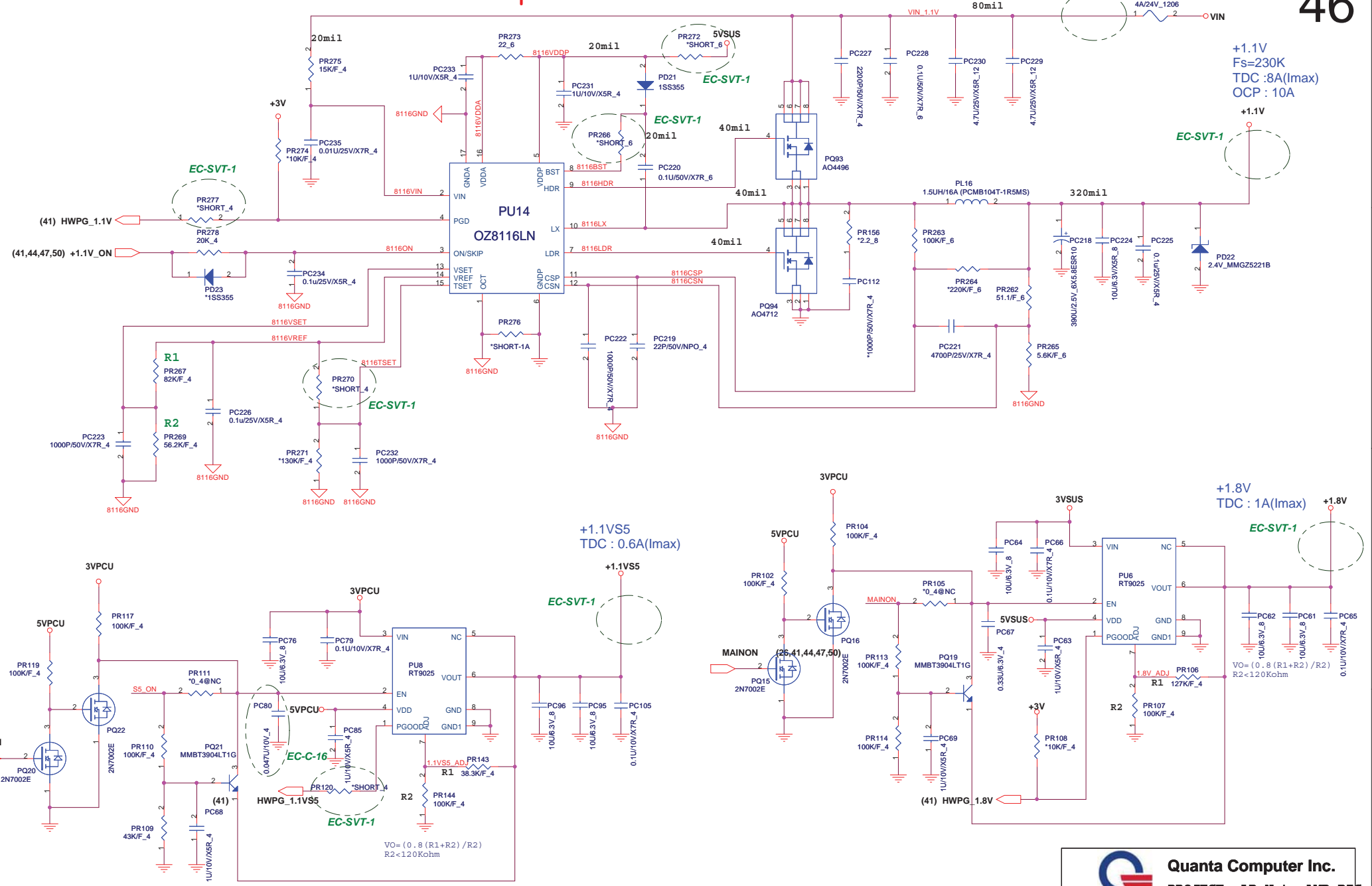
+1.0V_GPU
 TDC : 2.5A(I_{max})
 +1.0V_GPU

$$V_O = (0.8 \cdot (R1 + R2) / R2)$$

$$R2 < 120Kohm$$

Quanta Computer Inc.
 PROJECT : LD-Note AMD DIS

Size	Document Number	Rev
	DDR3/+1.5V/+1.0V (TPSS1116)	1A
Date:	Wednesday, June 09, 2010	Sheet 45 of 55



+1.1V
Fs=230K
TDC : 8A(I_{max})
OCP : 10A

+1.1VS5
TDC : 0.6A(I_{max})

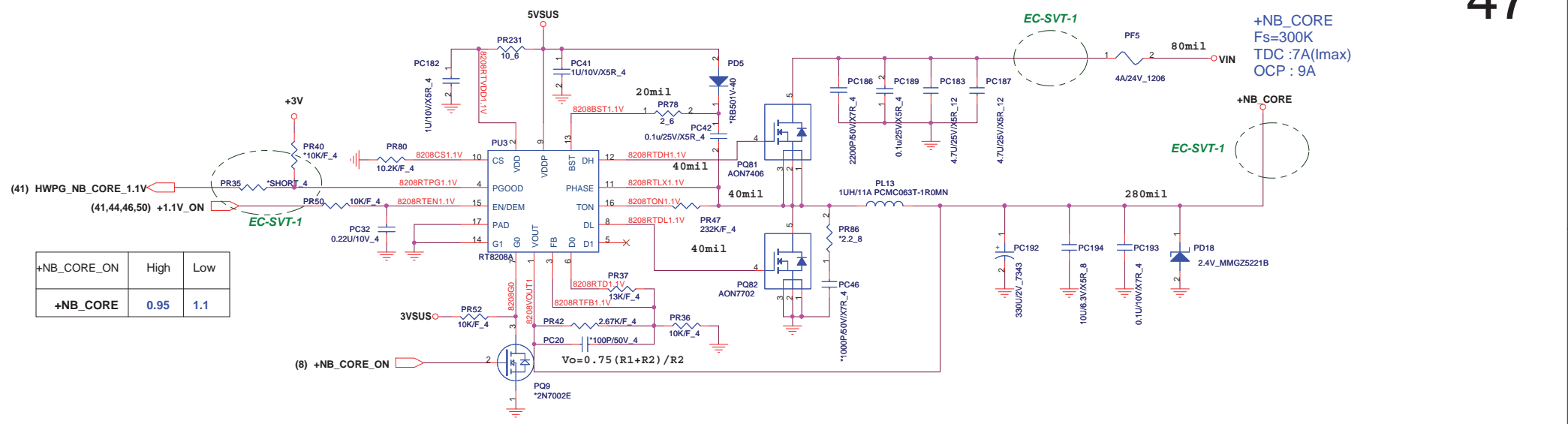
+1.8V
TDC : 1A(I_{max})

$$V_O = (0.8 (R_1 + R_2) / R_2)$$

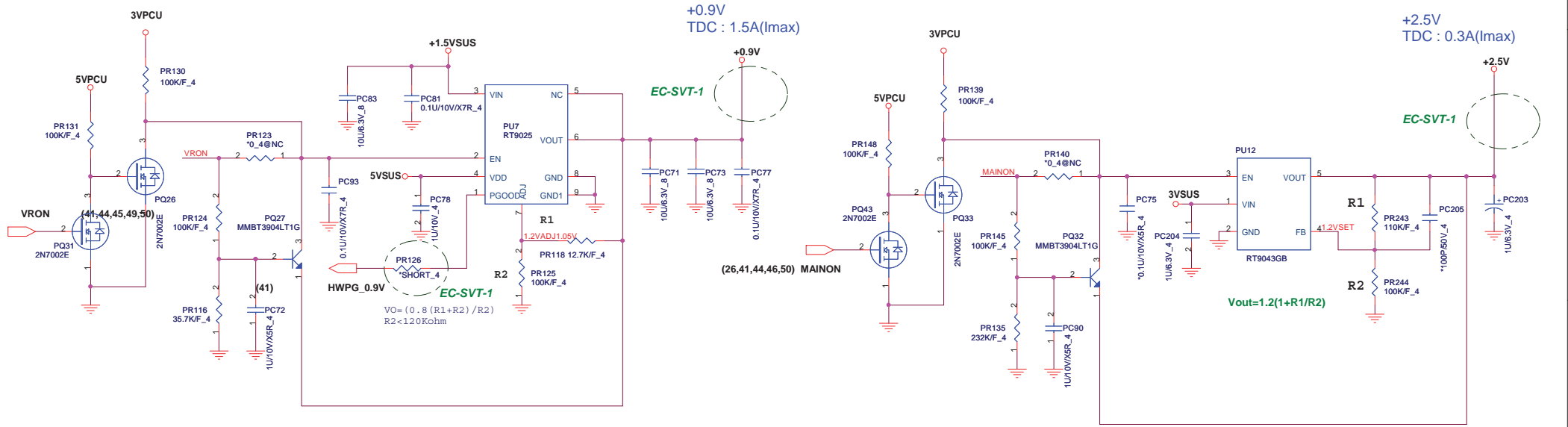
R2 < 120Kohm

$$V_O = (0.8 (R_1 + R_2) / R_2)$$

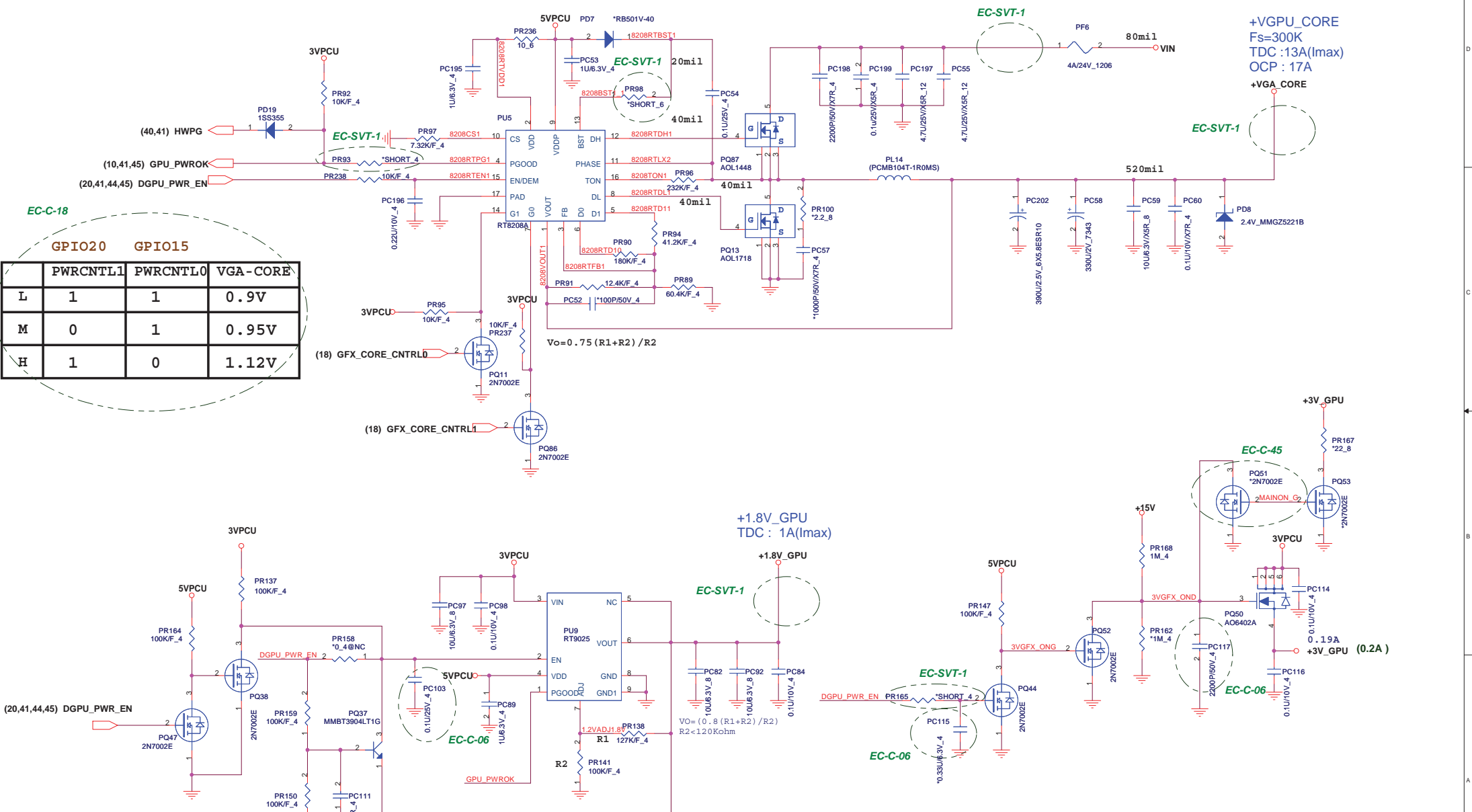
R2 < 120Kohm



+NB_CORE_ON	High	Low
+NB_CORE	0.95	1.1



VGA Core



EC-C-18

	GPIO20	GPIO15	VGA-CORE
L	1	1	0.9V
M	0	1	0.95V
H	1	0	1.12V

+VGPU_CORE
 Fs=300K
 TDC :13A(I_{max})
 OCP : 17A
 +VGA CORE

+1.8V_GPU
 TDC : 1A(I_{max})

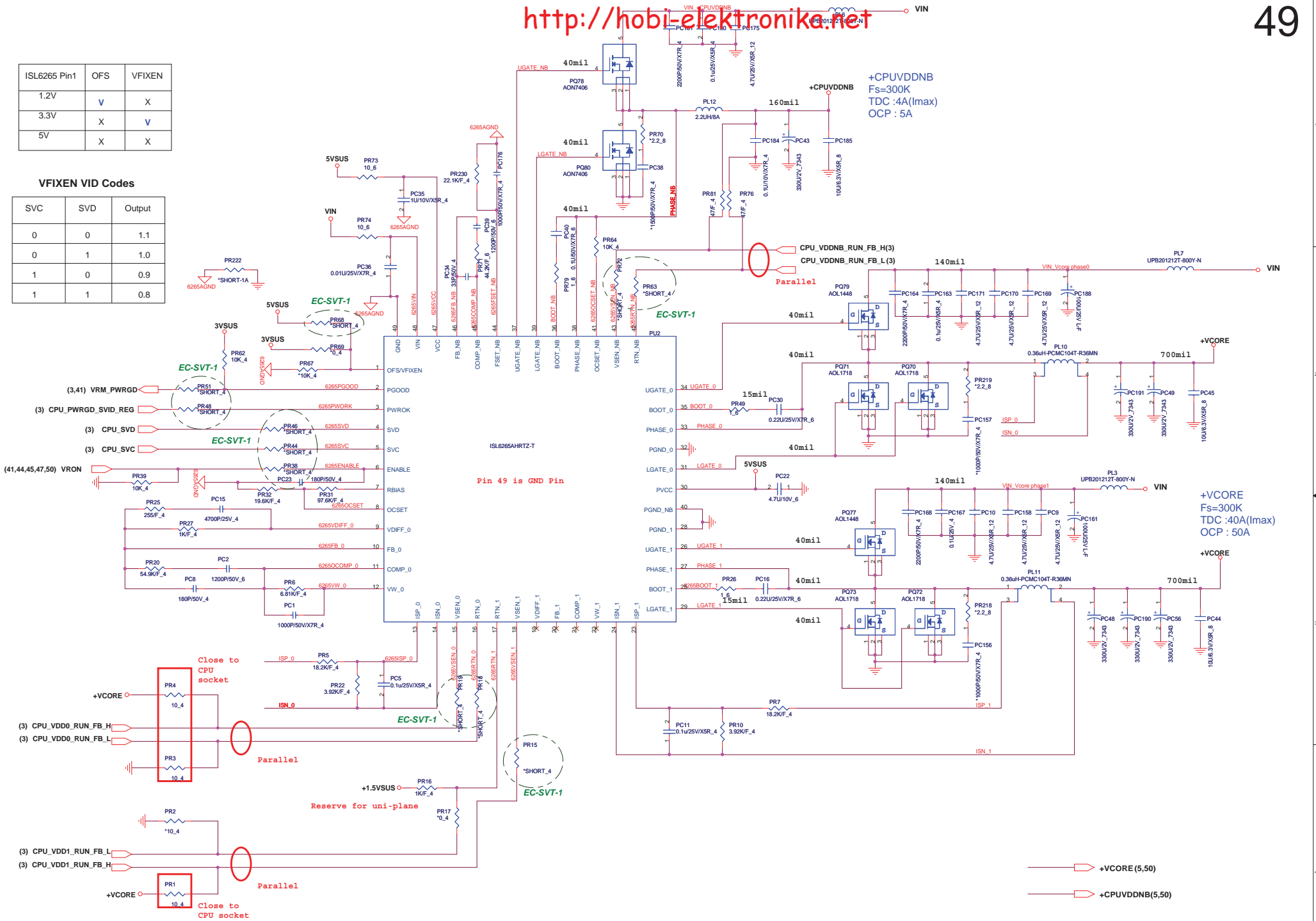
+3V_GPU
 0.19A
 +3V_GPU (0.2A)

Quanta Computer Inc.
 PROJECT : LD-Note AMD DIS
 Size Document Number
VGA/+1.8V/+3V (RT8208A) Rev 1A
 Date: Wednesday, June 08, 2010 Sheet 48 of 55

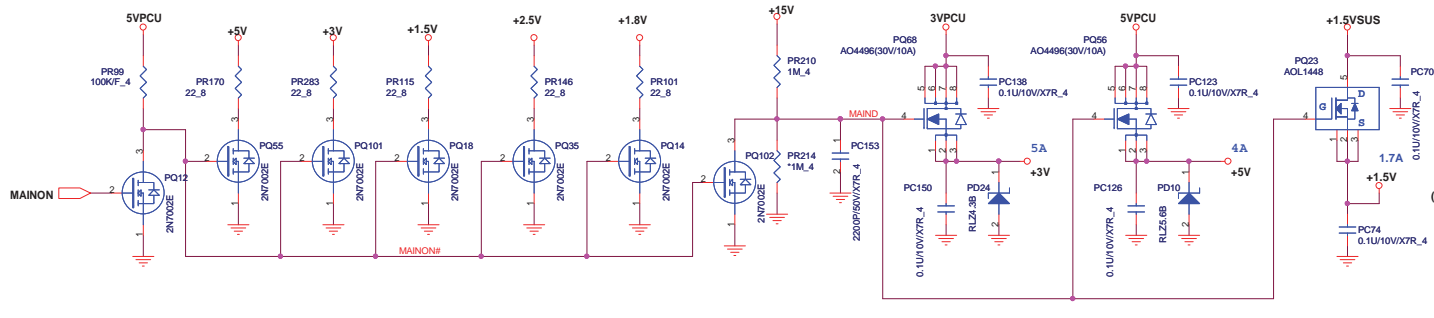
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

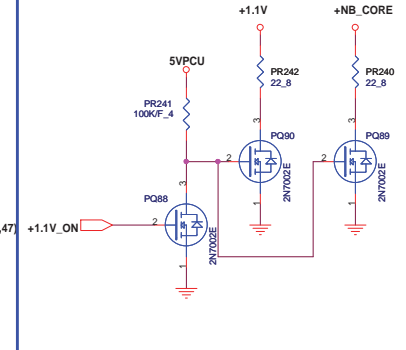
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



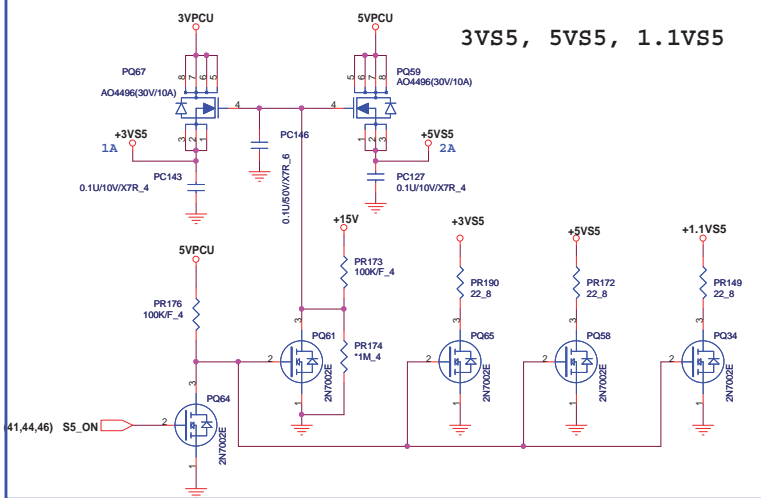
+3V, +5V,+2.5V,+1.8V,+1.5V



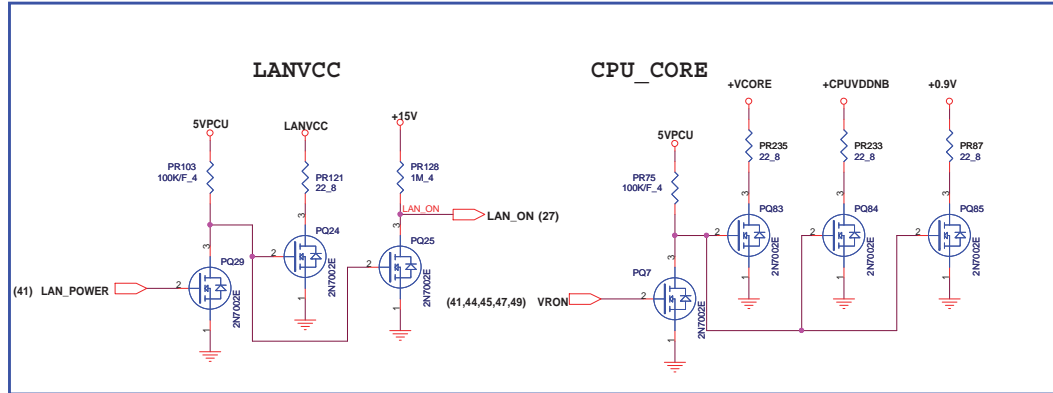
+1.1V, +NB_CORE



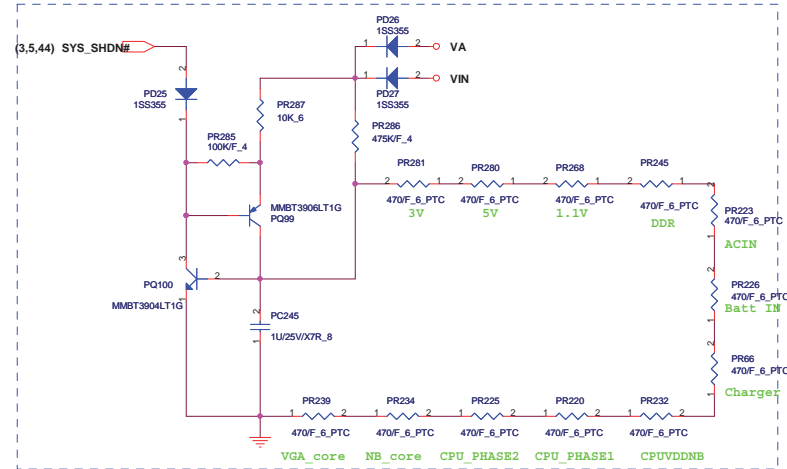
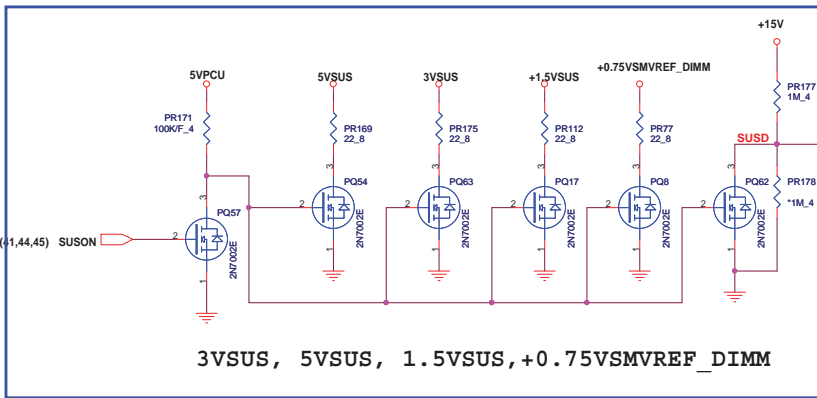
3VS5, 5VS5, 1.1VS5

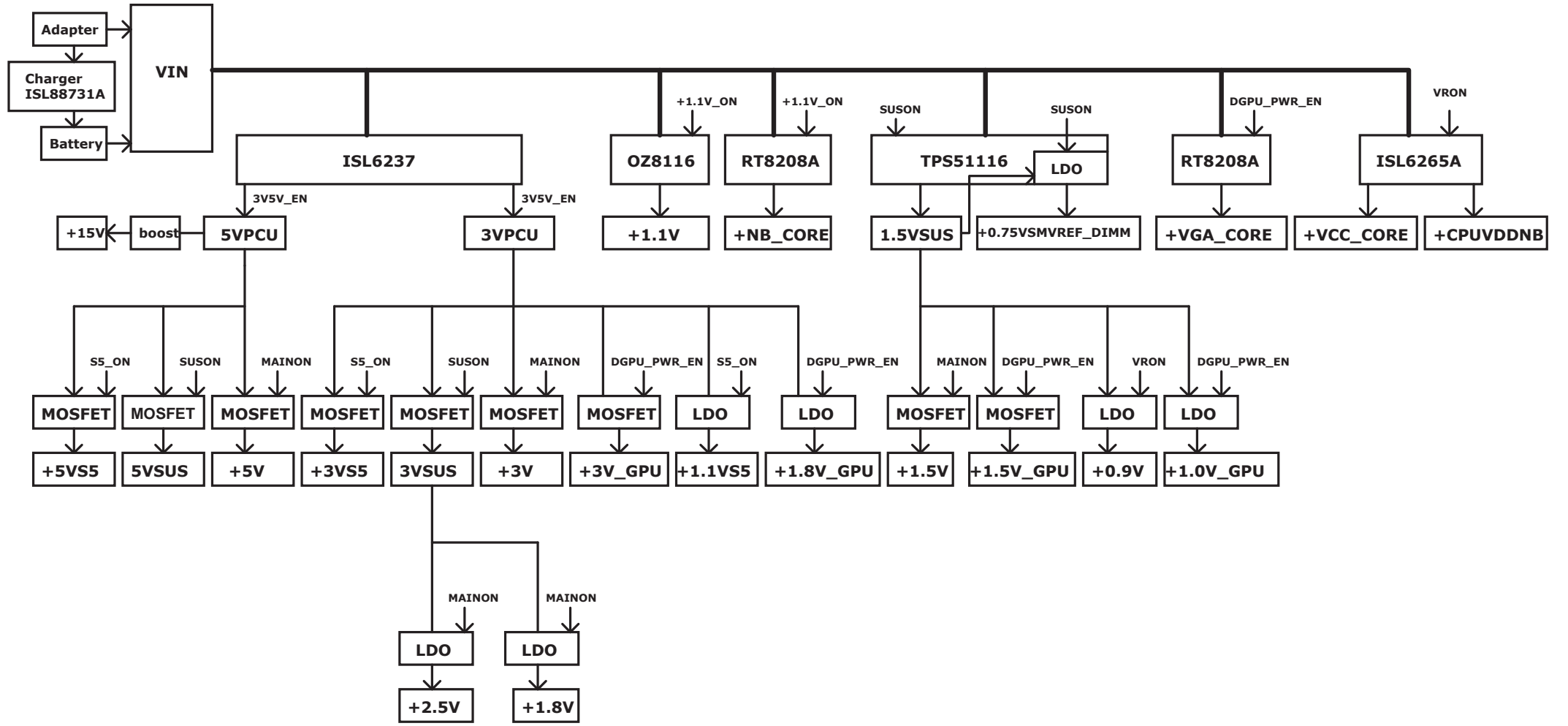


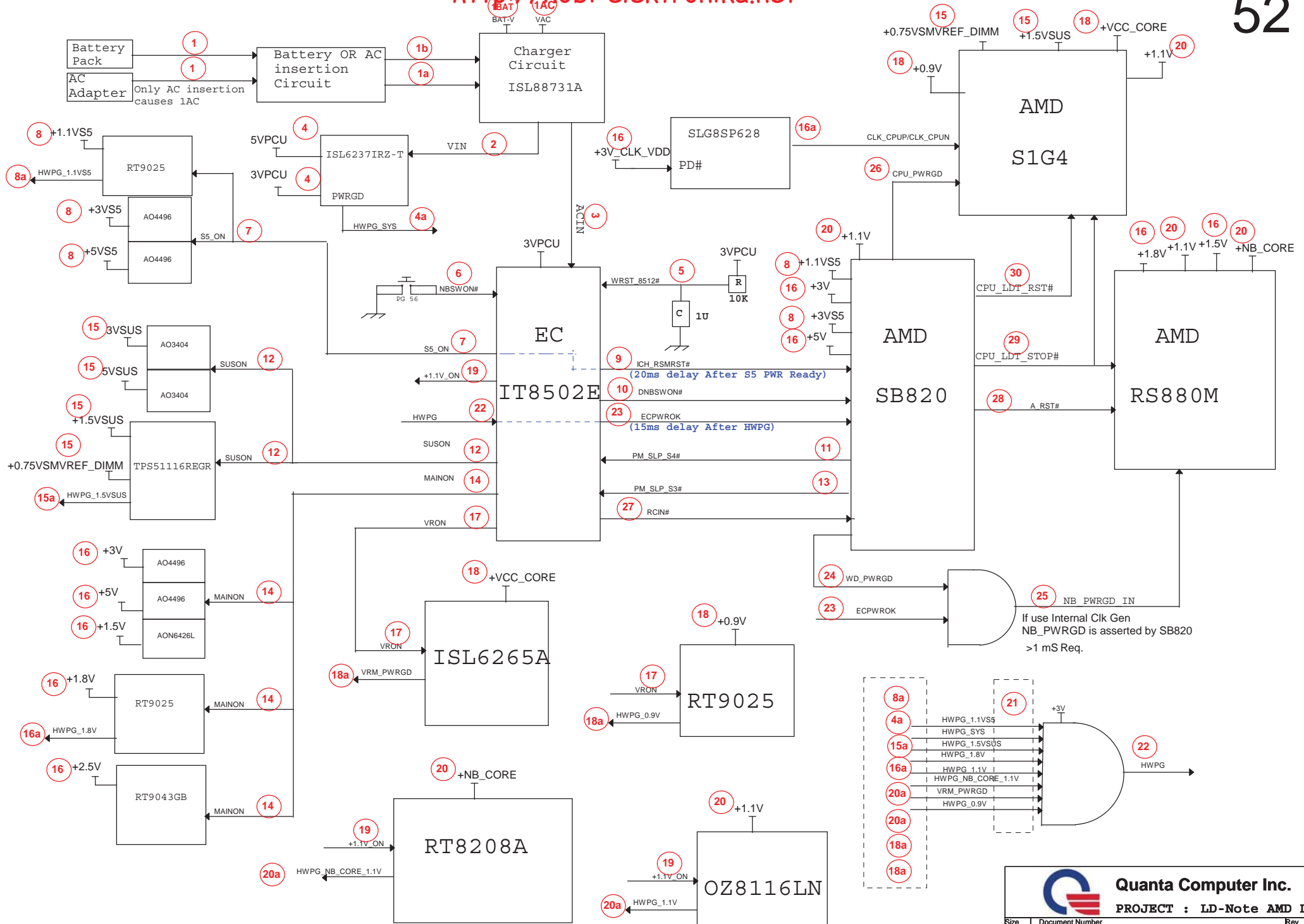
LANVCC

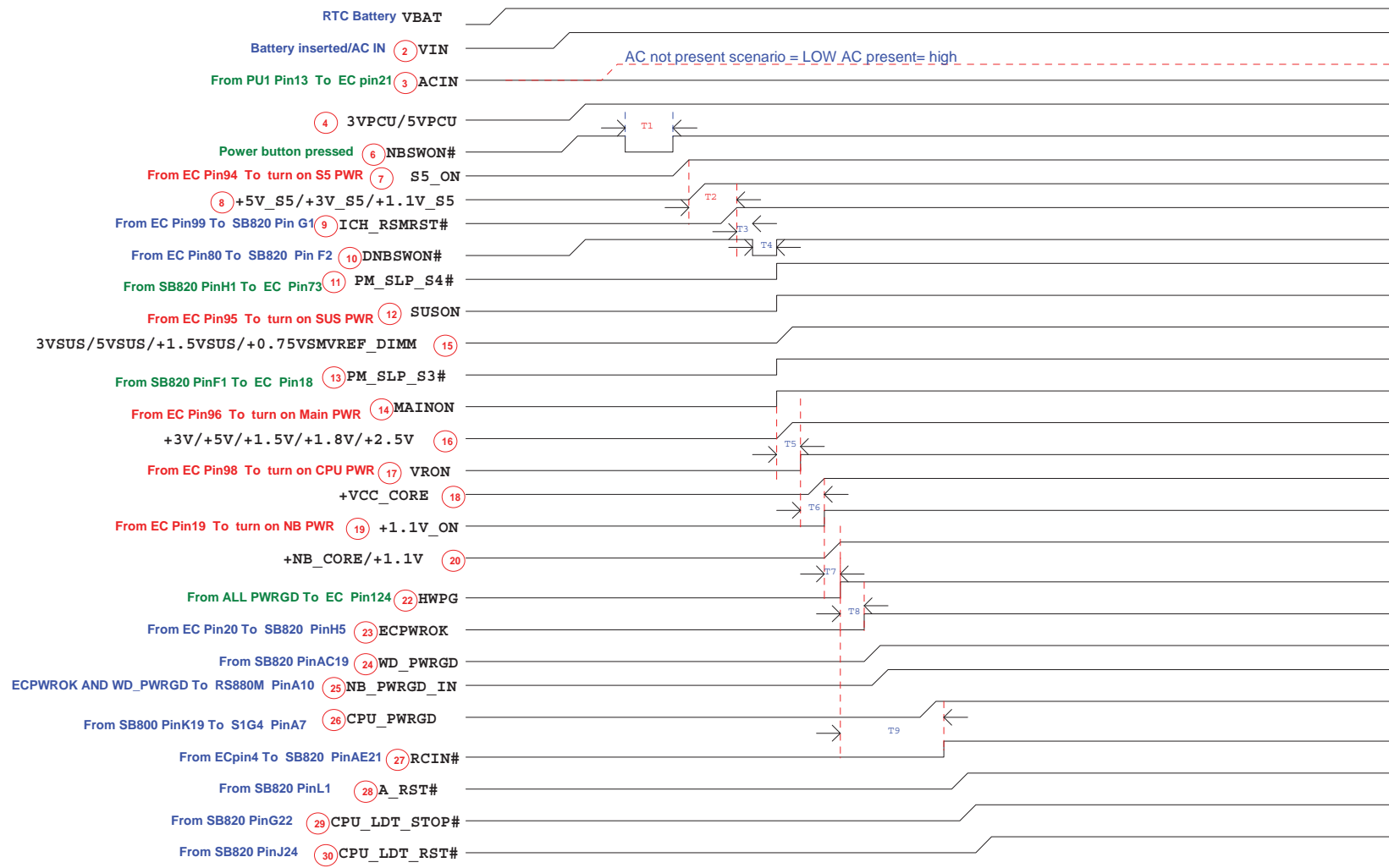


3VSUS, 5VSUS, 1.5VSUS,+0.75VSMVREF_DIMM









T1	>16ms
T2	20ms
T3	5ms
T4	1ms
T5	15ms
T6	5ms
T7	5ms
T8	15ms
T9	108ms

EC #	Page	Description	Part Affected
EC-C-01	20	Change error 10u footprint from 0603 to 0805	C51,C68,C78,C93,C236,C244,C247,C254,C257,C265,C270,C273,C602,C604,C705,C709,C714
EC-C-02		Layout change: Change TEST PAD size from 30mil to 20mil to increase ICT percentage	T1-1116,TP1-TP24
EC-C-03	23	Change X5R to X7R due to X5R stock is EOL	C362,C364
EC-C-04	3 10 11	Add value with ' * ' due to it is a short pad originally	R106,R466,R468 R573 R268,R566
EC-C-05	10	Un-stuff 22P coupling CAP & change RES from 22ohm to 10ohm to fix LPC_CLK rising time issue	C777,R511
EC-C-06	48 45	Modify some RC value to meet VGA power up sequence From 10K to 0 ohm From 0.33U to NA From 0.01U to 2200P From 0.33U to 0.1U From 0.33U to 0.047U	PR165 PC115 PC117 PC103 PC113
EC-C-07	25	Change RGB bead value to fix EA rising time issue	L18,L24,L27
EC-C-08	19	AMD suggest remove pull high RES AMD suggest add pull high RES	R91,R412,R419 R416,R420
EC-C-09	39	Add fuse for EL keyboard UL suggestion	F6
EC-C-10	34	Add 2N7002 to reduce leakage current	Q41
EC-C-11	5	Add transistors for EC to monitor thermal of CPU (SB_TSI mode)	Q42,Q43,Q44
EC-C-12	11	Stuff the RES due to BOM error	R360
EC-C-13	8	Change BOM to meet "CPU_LDT_STOP#F" power sequence Replace Q36 with U48,delete R454,R451,change R452 from 4.7K to 2.2K	Q36,U48,R454,R451,R452
EC-C-14	3,8	AMD suggest "CPU_LDT_RST#" & "CPU_LDT_STOP#"connect to +1.5V power for prevent current leakage	R110,R453
EC-C-15	5	Delete thermal sensor schematic due to AMD suggest that don't use external thermal IC to prevent thermal shut down issue.	Q11,Q12,U7,R131,R132,R117,C302,C305,R138,R137,C341,Q13,R120
EC-C-16	46	To improve +1.1VSS rise time waveform. Modify CAP value.	PC80
EC-C-17	10	For RTC test accurately, modify 32.768KHz XTAL coupling CAP	C812,C813
EC-C-18	48	AMD fine tune VBIOS to meet VGA_CORE table	
EC-C-19	44	BOM error,remove the component	PC142
EC-C-20		Change the power jump to short pad	PJP1-PJP18
EC-C-21	45	Reserve RC circuit to modify power sequence	PR288,PC246
EC-C-22	45	Change RES value to fine tune +1.0_GPU prevent from voltage drop issue	PR152
EC-C-23	11	Add NEW_CLKREQ#, LAN_CLKREQ#, WLAN_CLKREQ# function at BIOS side	U38D pin AA16,AC18,AH21
EC-C-24	11	Delete single net SP_DDR3_RST# & 0 ohm RES	R337
EC-C-25	11	Add WAKE# net with +3VSS pull high	R606
EC-C-26	27	Add thansistor to avoide leakage current of CLK request and wake up function of LAN. Delete 0 ohm RES	Q45,Q46,R337 R317
EC-C-27	3	Un-stuff RES for leakage issue Stuff RES for leakage issue	R484,R485 R476,R477
EC-C-28	26	Vendor suggest reserve it,BOM not mount	C551
EC-C-29	12	Update board ID table for BIOS to verify PCB version	
EC-C-30	30 31	Because sku in't build WWAN, reserve all of components about WWAN function	CN25,U16,C395,C382,C396,C390,C383 CN26,R532,R543,R545,C808,C785,C795,C806,C784,C815
EC-C-31	41	Because we add LDO circuit to control G-Sensor power and we change GSENSOR_ON to high enable. We need to verify EC version	R381,R382
EC-C-32		Layout modify: modify SB & NB footprint due to customer request	U34,U43
EC-C-33	8	AMD comment DIS only supply 1.1V for NB_CORE,no need to stuff strap pin RES	R442
EC-C-34	12	AMD comment unstuff SB SATA 25MHz XTAL if we had stuff 25MHz internal XTAL	Y6,C794,C796,R536
EC-C-35	2	Follow up GC5C design to change 14.318 XTAL from 30ppm to 10ppm	Y1
EC-C-36	27	Change LAN chip version to reduce power consumption	U23
EC-C-37	26	Follow up GC5 design to change sense MIC switch from BJT to MOSFET	Q30
EC-C-38	41	ESD solution	D28,D29
EC-C-39	28	Reserve 0.1u CAP due to ESD solution	C832
EC-C-40	30	Modify USB CONN footprint due to SMT request	CN24,CN27
EC-C-41		Change 0 ohm RES footprint from 0402 to short pad	R397,R431,R432,R459,R197,R200,R370,R372,R379,R250,R259,R563,R287,R306,R320,R182,R183 R426,R290,R186,R189,R193,R201,R148,R150,R151,R152,R20,R25,R3,R472,R473,R474,R475, R84,R355,R356,R293,R298,R520,R524,R167,R376,R594,R595,R596,R597,R598,R599,R600, R313,R300,R341,R195,R302,R368,R369,R413,R414,R415,R31,R32,R32,R47,R447,R449,R450,R554, R571,R283,R436,R48,R227,R278,R346,R365,R204,R199,R252,R253,R267,R246,R270,R486,R552
EC-C-42	26	For MIC not be found issue, stuff R281,un-stuff R292,Q30,R286	R281,R292,Q30,R286
EC-C-43	41	Modify EC ID table for EC setting	R381,R382
EC-C-44	12	Modify board ID table for BIOS setting	R537,R538
EC-C-45	48	Remove 2N7002 due to BOM error	PO51
EC-C-46	19	Change VGA thermal IC to ADM1032-2 in order to change address to 4D	U32
EC-C-47	41	BIOS set RF_SW# GPIO pull down to detect UMA & DISCRETE planer	R373,C575

EC #	Page	Description	Part Affected
EC-SVT-01		Delete all 0 ohm RES & jump for power portion schematic	
EC-SVT-02	43	Vendor suggest change RES value from 10K to 4.75K to fix 4 cell battery CC to CV ripple issue	PR45
EC-SVT-03	12	Change board ID for SVT planer revision	R540,R541,R533
EC-SVT-04	26	From vendor suggestion, change CAP value from 10u to 2.2u to fix beep sound issue	C556
EC-SVT-05	02	Delete all RP for CLKGEN output side	RP4,RP3,RP5,RP1,RP2,RP7,RP8,RP10,RP9,RP6
EC-SVT-06	12	Reserve GPIO pin for BIOS setting	R607,R608
EC-SVT-07	21	AMD suggest to un-stuff them due to CLKTESTA/B pin is for test	C216,C168,R65,R61
EC-SVT-08	23 29 29	Follow GC5C design to remove all common choke and fix EA test USB fail item at the same time	L40,R232,R233 CML1,R1,R2,CML3,R482,R483 CML2,R269,R276,CML4,R527,R526,CML5,R582,R581
EC-SVT-09	14	Delete R571 and short it directly to add test point for ICT fixture	R571