

COMPAL CONFIDENTIAL

MODEL NAME : ZAM81

PCB NO : LA-A913P

BOM P/N :

GPIO MAP: 3.1

Huston 15" DSC

Broadwell U

2013-08-20

REV : 0.1 (X00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component


XDP@ : XDP Component

CONN@ : Connector Component

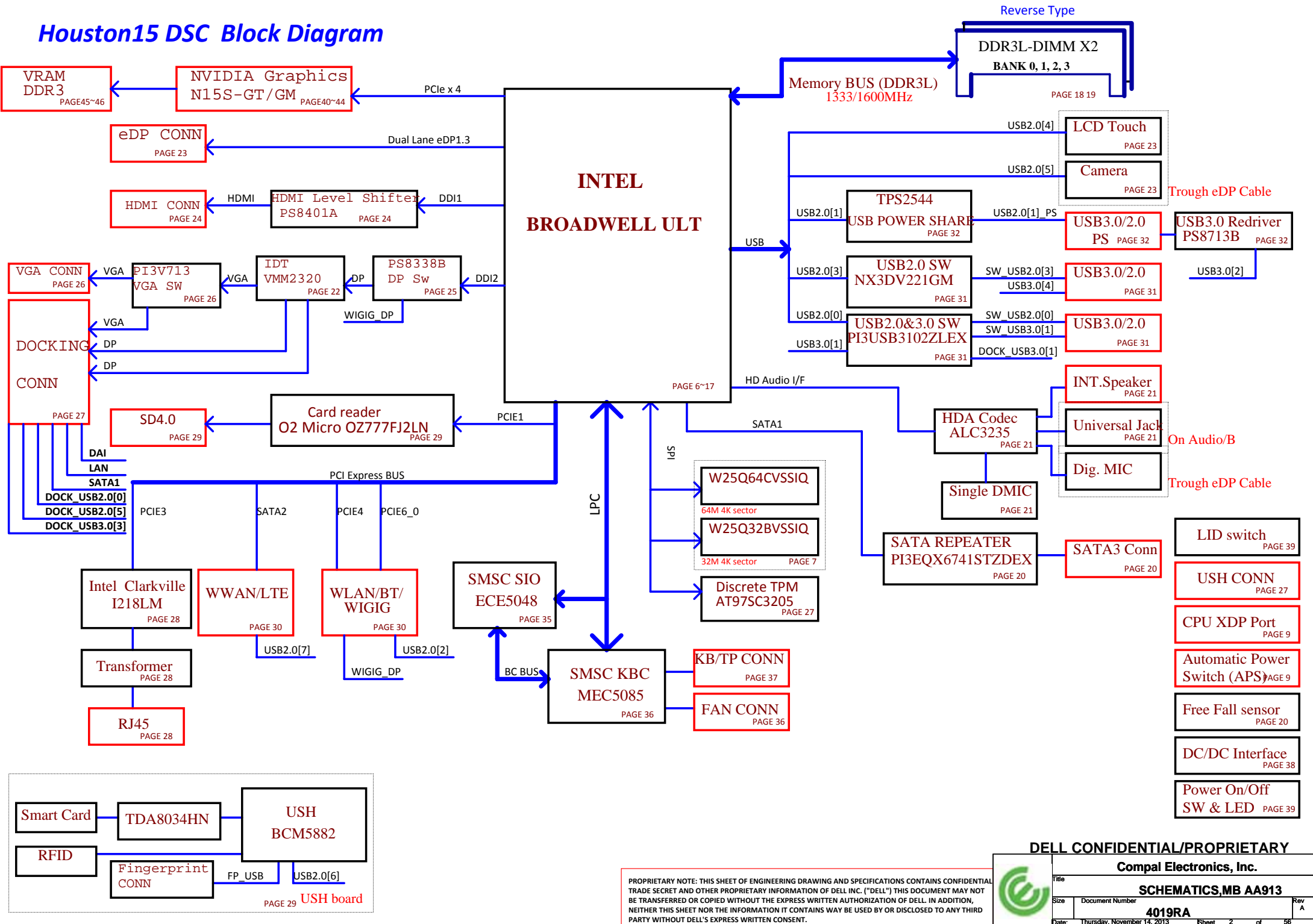
| Part Number | Description |
|-------------|-------------------------------------|
| DAA007Y000 | PCB 13N LA-A913P REV0 MB DSC DOCK 3 |

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| Size | Document Number | Rev |
| | 4019RA | A |
| Date | Thursday, November 14, 2013 | |
| | Sheet | 1 of 56 |

Houston15 DSC Block Diagram

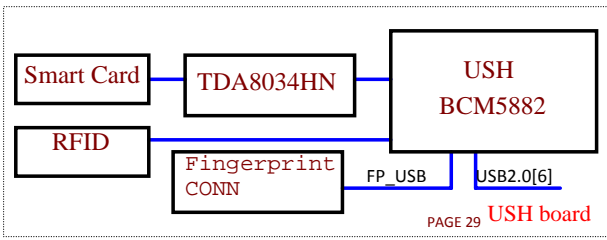


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POWER STATES

| State \ Signal | SLP S3# | SLP S4# | SLP S5# | SLP A# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|---------|---------|---------|--------|--------------|---------|-----------|-----------|--------|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3 (Suspend to RAM) / M3 | LOW | HIGH | HIGH | HIGH | ON | ON | ON | OFF | OFF |
| S4 (Suspend to DISK) / M3 | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF | OFF |
| S5 (SOFT OFF) / M3 | LOW | LOW | LOW | HIGH | ON | ON | OFF | OFF | OFF |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | LOW | ON | OFF | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | ON | OFF | OFF | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |

| PCIE | USB3.0 | SATA | DESTINATION |
|--------|----------|--------|--------------------|
| | USB3.0 1 | | JUSB1-->Rear left |
| | USB3.0 2 | | JUSB3-->Right |
| PCIE 1 | USB3.0 3 | | MMI (CARD READER) |
| PCIE 2 | USB3.0 4 | | JUSB2-->Rear Right |
| PCIE 3 | | | LOM |
| PCIE 4 | | | WLAN |
| PCIE 5 | | | GPU/WIGIG |
| PCIE 6 | | SATA 3 | WIGI/Express |
| | | SATA 2 | mSATA/PCIE |
| | | SATA 1 | HDD |
| | | SATA 0 | DOCK |

PM TABLE

| State \ power plane | +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO | +3.3V_SUS +1.35V_MEM | +5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE | +3.3V_M +1.05V_M | +3.3V_M +1.05V_M (M-OFF) |
|------------------------|--|-------------------------|--|---------------------|--------------------------------|
| S0 | ON | ON | ON | ON | ON |
| S3 | ON | ON | OFF | ON | OFF |
| S5 S4/AC | ON | OFF | OFF | ON | OFF |
| S5 S4/AC doesn't exist | OFF | OFF | OFF | OFF | OFF |

need to update Power Status and PM Table

| BDW ULT | USB PORT# | DESTINATION |
|------------|-----------|--------------|
| | 0 | JUSB1 |
| | 1 | JUSB3 |
| | 2 | WLAN + BT |
| | 3 | JUSB2 |
| | 4 | Touch Screen |
| | 5 | CAMERA |
| | 6 | USH |
| 7 | WWAN | |

| USH | 0 | BIO |
|-----|---|-----|
| | 1 | NA |

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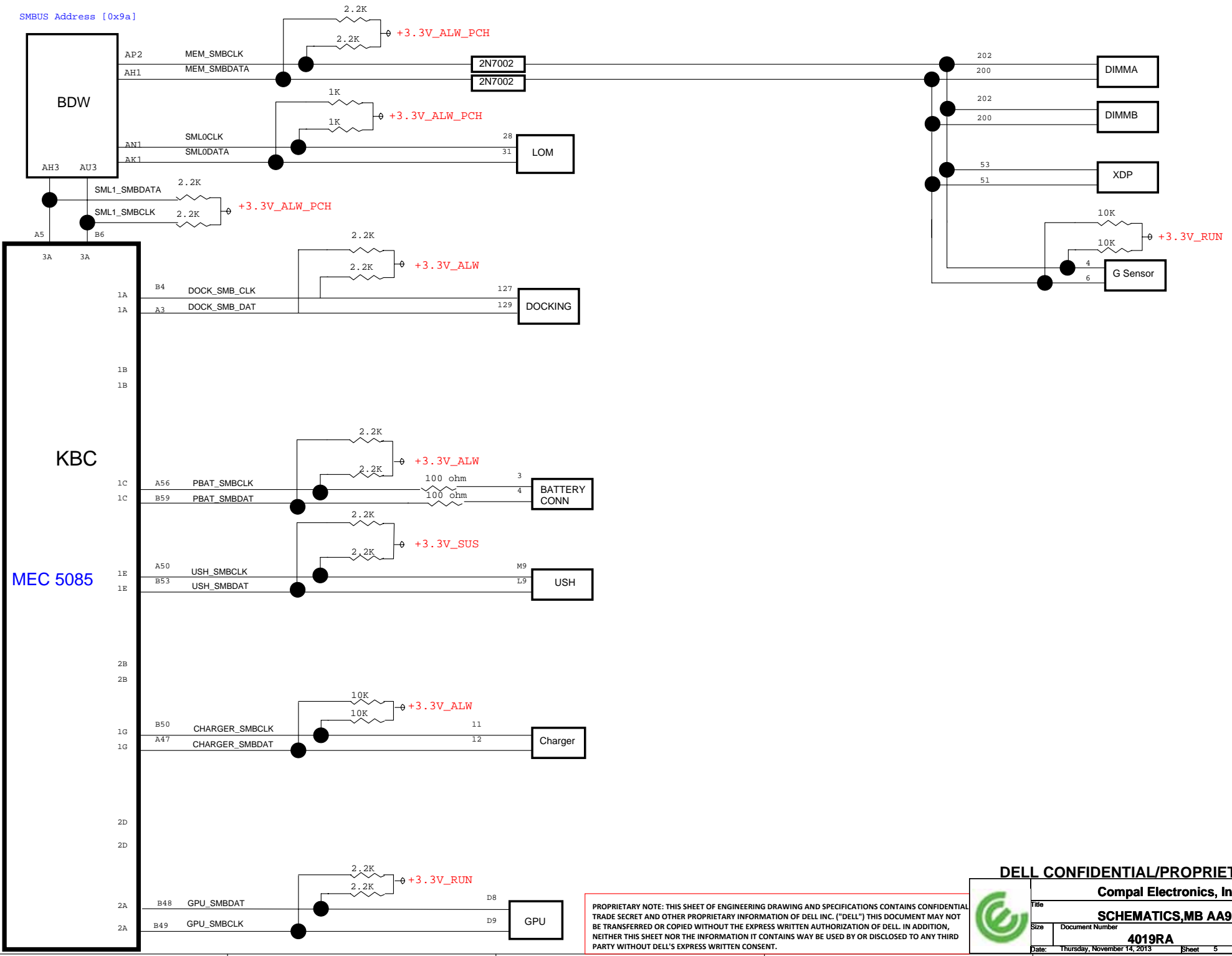
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| | | | | |
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SMBUS Address [0x9a]



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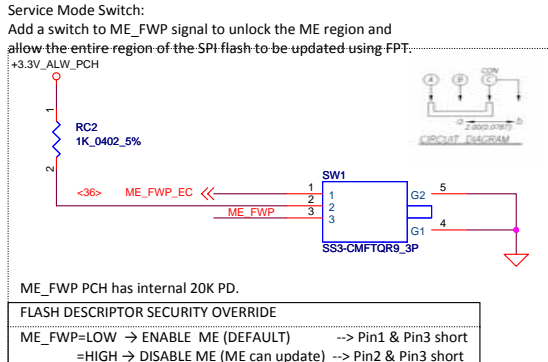
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Size: **4019RA** Rev: **A**

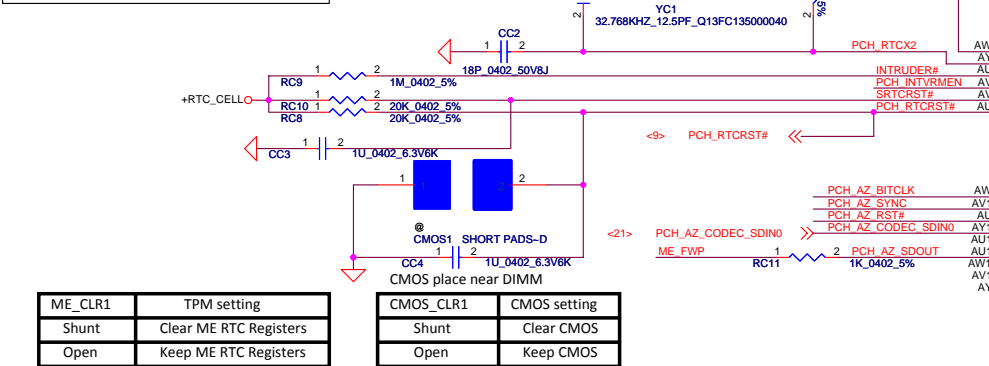
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DSC SATA port



| SATA0 | SATA1 | PCB | SATA2/PCIE6 L1 | SATA3/PCIE6 L0 | |
|--------|-------|-----------|---|-------------------------------|--|
| E-Dock | HDD | H12 UMA | M2 3042 2nd PCIe Lane for PCIe Cache | M2 3042 (HCA & SATA-Cache) | contact to WWAN |
| NA | HDD | H12 Entry | NA | NA | |
| E-Dock | HDD | H14 DSC | M2 3042 SATA-Cache(no HCA) | M2 3030 WIGIG | SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN |
| E-Dock | HDD | H14 UMA | M2 3042 2nd PCIe Lane for PCIe Cache | M2 3042 (HCA & SATA-Cache) | contact to WWAN |
| NA | HDD | H14D_En | NA | M2 3030 WIGIG | contact to WLAN |
| NA | HDD | H14U_En | NA | NA | |
| E-Dock | HDD | H15 DSC | M2 3042 SATA-Cache(no HCA) | M2 3030 WIGIG | SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN |
| E-Dock | HDD | H15 UMA | M2 3042 2nd PCIe Lane for PCIe Cache | M2 3042 (HCA & SATA-Cache) | contact to WWAN |
| NA | HDD | H15D_En | NA | M2 3030 WIGIG | contact to WLAN |
| NA | HDD | H15U_En | NA | Express card | contact to Express card |

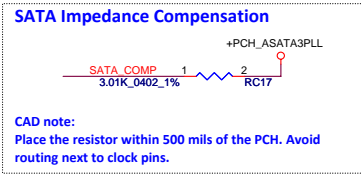
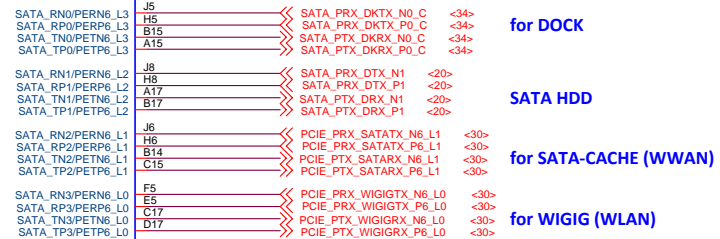
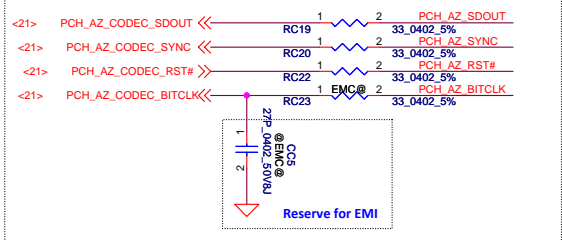
INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



| ME_CLR1 | TPM setting |
|---------|------------------------|
| Shunt | Clear ME RTC Registers |
| Open | Keep ME RTC Registers |

| CMOS_CLR1 | CMOS setting |
|-----------|--------------|
| Shunt | Clear CMOS |
| Open | Keep CMOS |

HDA for Codec



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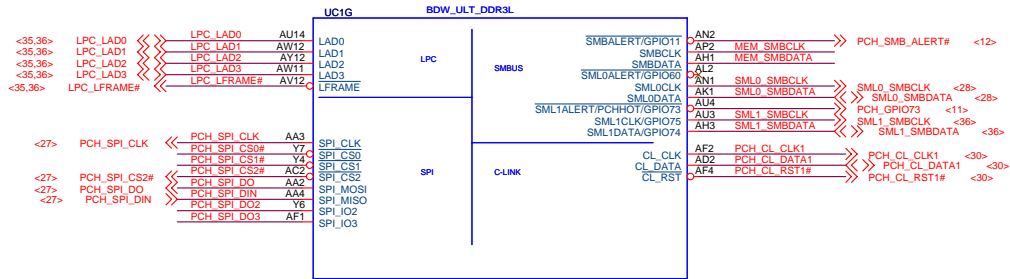
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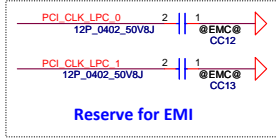
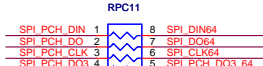
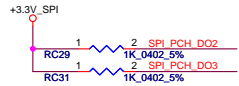
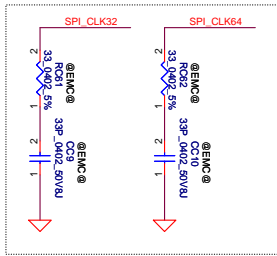
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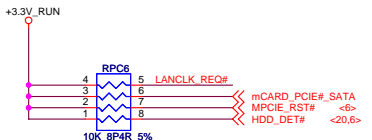


BDW_ULT_DDR3L_BGA1168
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SOFTWARE TAA



Reserve for EMI



PCIECLK for DSC

MMI --->



10/100/1G LAN --->



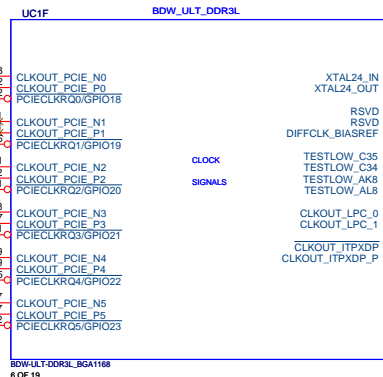
WLAN (NGFF1) --->



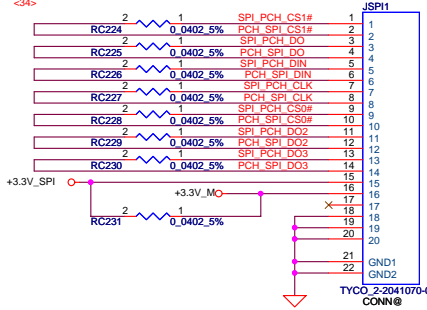
GPU --->



WIGIG --->



BDW_ULT_DDR3L_BGA1168
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| support SPI TPM | |
|-----------------|-------|
| LPC_0 | LPC_1 |
| SIO | DOCK |
| MEC | DEBUG |

| PCB | PCIE1 | PCIE2 | PCIE3 | PCIE4 | PCIE5 | PCIE6 |
|-----------|---------|-------|-------|-------|-------|----------------------------|
| H12 UMA | SD card | NA | LOM | WLAN | WIGIG | M2 3042 (HCA & SATA-Cache) |
| H12 Entry | SD card | NA | LOM | WLAN | WIGIG | NA |
| H14 DSC | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H14 UMA | SD card | NA | LOM | WLAN | WIGIG | M2 3042 (HCA & SATA-Cache) |
| H14D_En | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H14U_En | SD card | NA | LOM | WLAN | WIGIG | NA |
| H15 DSC | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H15 UMA | SD card | NA | LOM | WLAN | WIGIG | M2 3042 (HCA & SATA-Cache) |
| H15D_En | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H15U_En | SD card | NA | LOM | WLAN | WIGIG | Express card |

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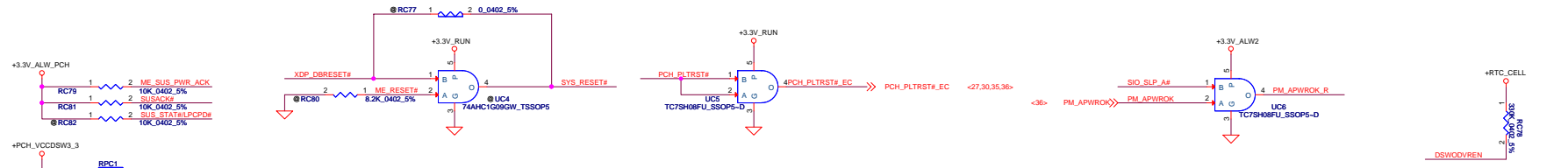
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Schematics_MB_AA913

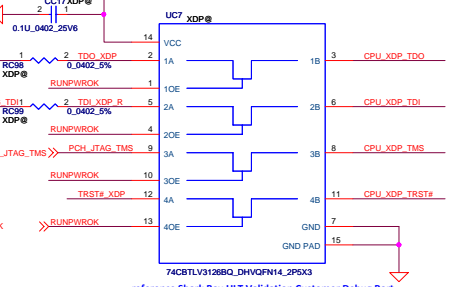
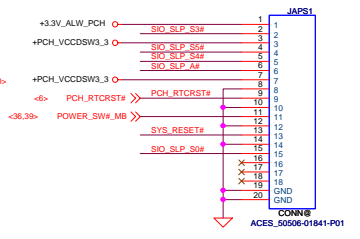
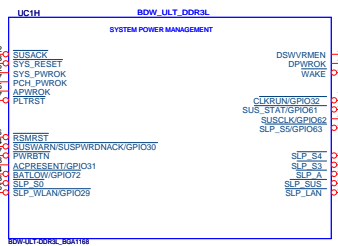
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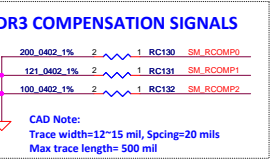
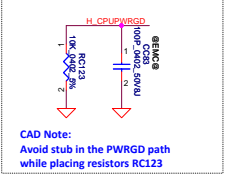
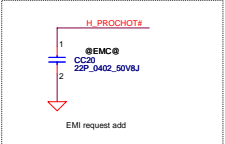
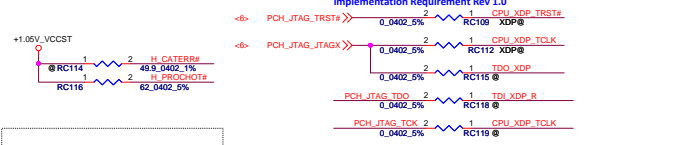


DSWODVREN - ON DIE DSW VR ENABLE
 HIGH = ENABLED (DEFAULT)
 LOW = DISABLED

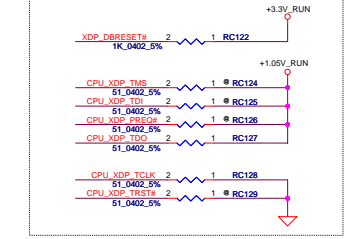
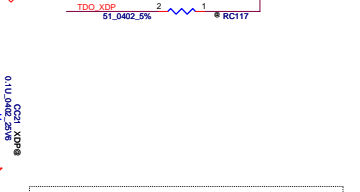
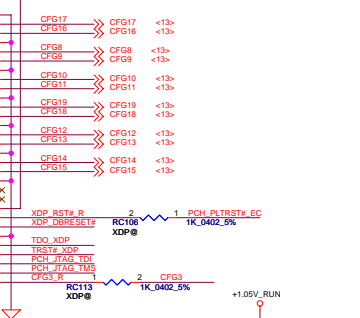
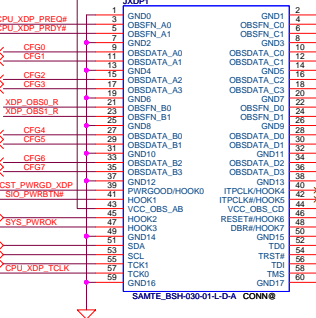
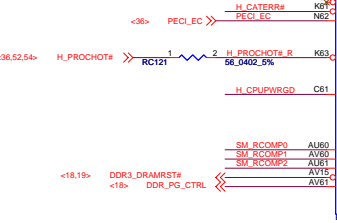
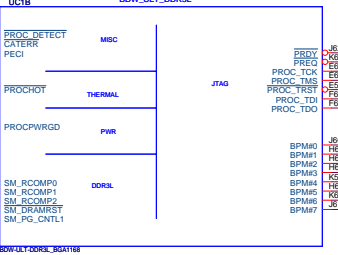
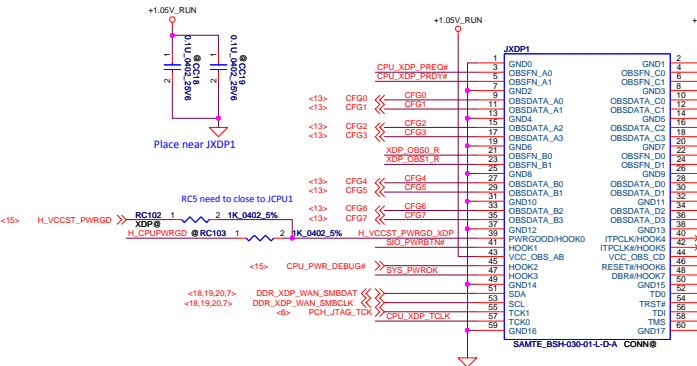
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- <<2>> PLTRST_USH# <<RC197 1 2 0.0402_5% >>
- <<2>> PLTRST_MM# <<RC198 1 2 0.0402_5% >>
- <<2>> PLTRST_LAN# <<RC199 1 2 0.0402_5% >>
- <<4>> PLTRST_GPU# <<RC200 2 2 0.0402_5% >>



reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0



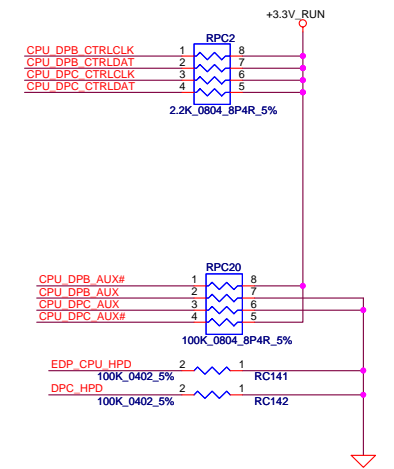
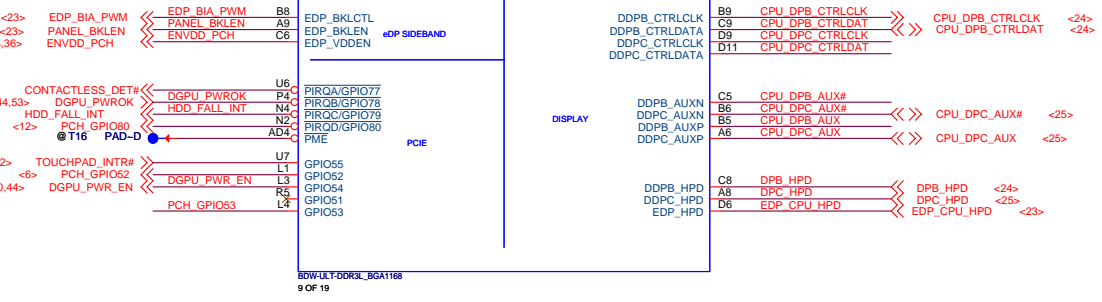
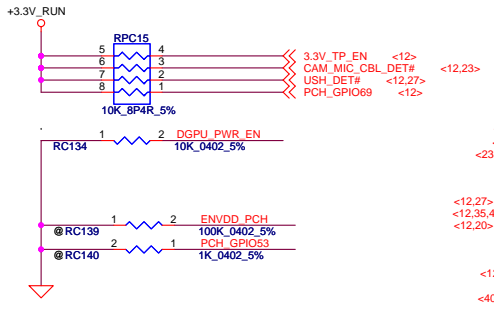
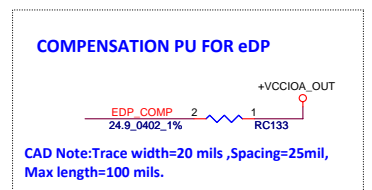
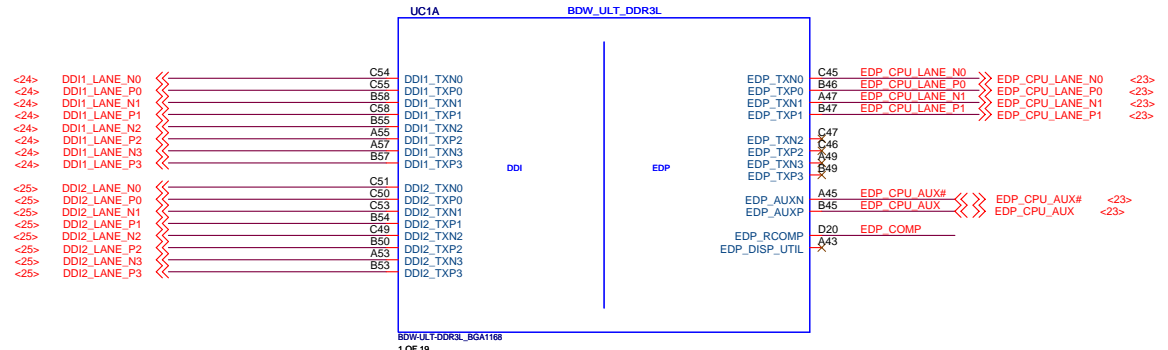
CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil



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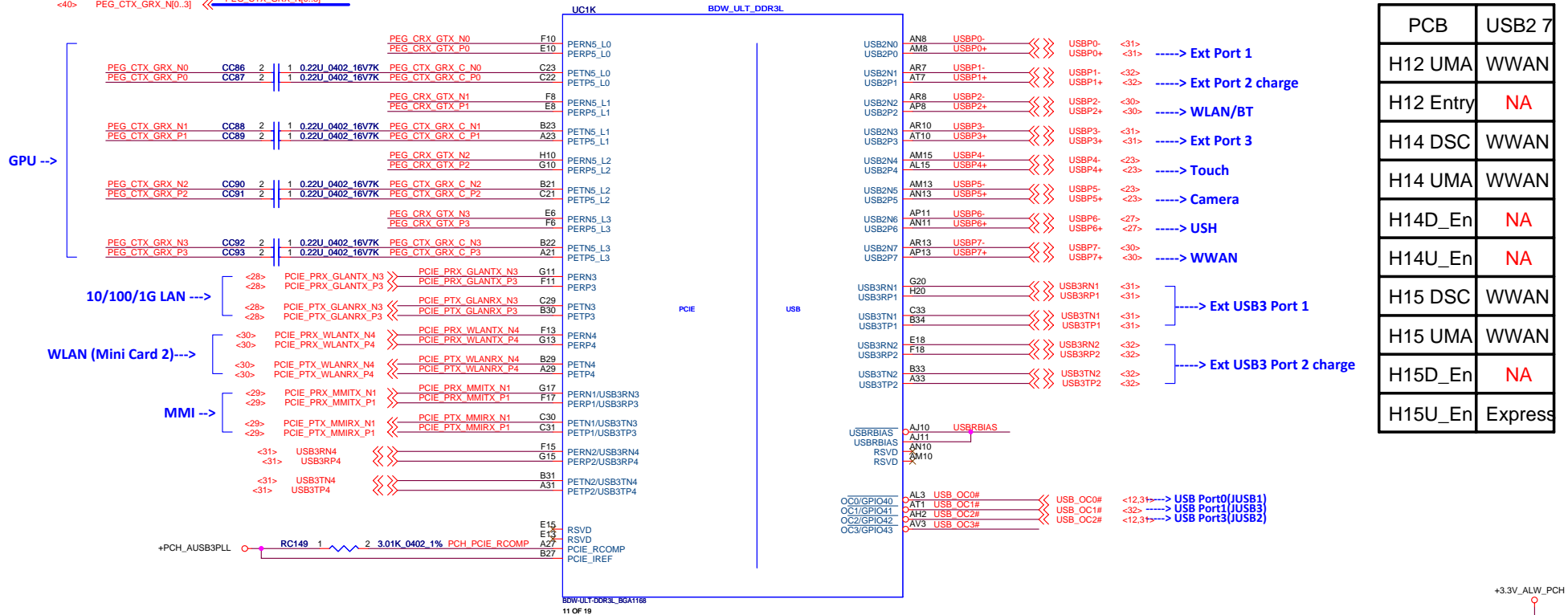
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Rev A

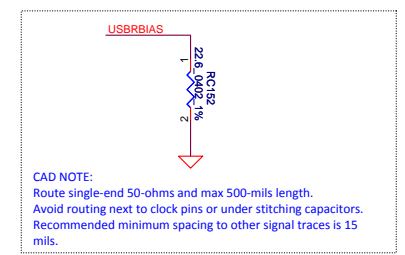
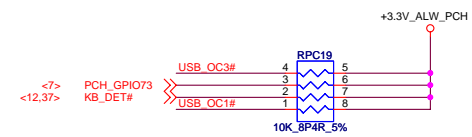
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PCIe for DSC



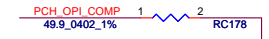
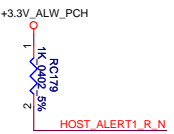
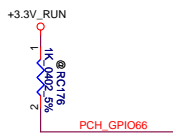
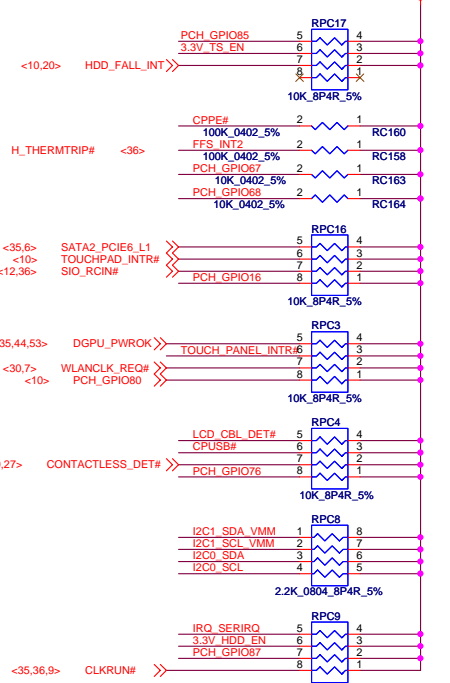
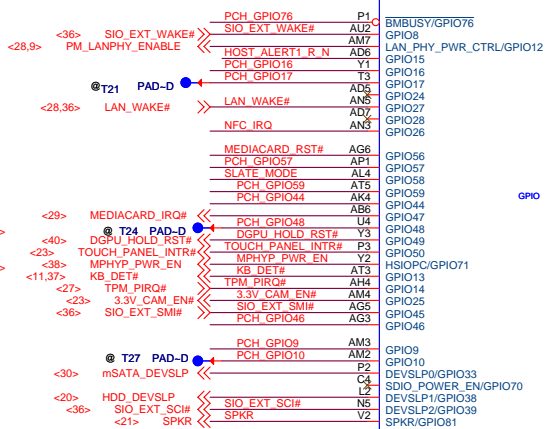
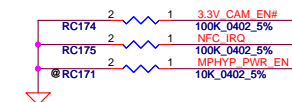
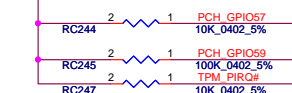
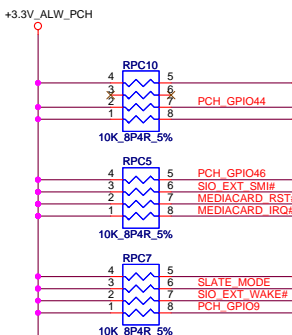
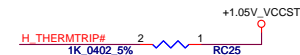
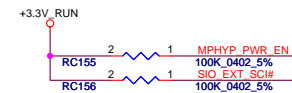
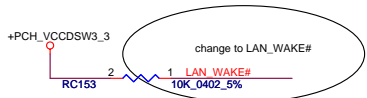
| PCB | USB2 7 |
|-----------|---------|
| H12 UMA | WWAN |
| H12 Entry | NA |
| H14 DSC | WWAN |
| H14 UMA | WWAN |
| H14D_En | NA |
| H14U_En | NA |
| H15 DSC | WWAN |
| H15 UMA | WWAN |
| H15D_En | NA |
| H15U_En | Express |

| PCB | PCIE1 | PCIE2 | PCIE3 | PCIE4 | PCIE5 | PCIE6 |
|-----------|---------|-------|-------|-------|-------|----------------------------|
| H12 UMA | SD card | NA | LOM | WLAN | WIGIG | M2 3042 (HCA & SATA-Cache) |
| H12 Entry | SD card | NA | LOM | WLAN | WIGIG | NA |
| H14 DSC | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H14 UMA | SD card | NA | LOM | WLAN | WIGIG | M2 3042 (HCA & SATA-Cache) |
| H14D_En | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H14U_En | SD card | NA | LOM | WLAN | WIGIG | NA |
| H15 DSC | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H15 UMA | SD card | NA | LOM | WLAN | WIGIG | M2 3042 (HCA & SATA-Cache) |
| H15D_En | SD card | NA | LOM | WLAN | GPU | WIGIG |
| H15U_En | SD card | NA | LOM | WLAN | WIGIG | Express card |



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| TOP-BLOCK SWAP OVERRIDE | |
|-------------------------|---------------------|
| HIGH | depop RC288 |
| LOW | pop RC288 (DEFAULT) |

| BOOT BIOS STRAP BIT BBS | |
|-------------------------|-----|
| HIGH | LPC |
| LOW(DEFAULT) | SPI |

| TLS CONFIDENTIALITY | |
|---------------------|---------|
| HIGH | ENABLE |
| LOW(DEFAULT) | DISABLE |

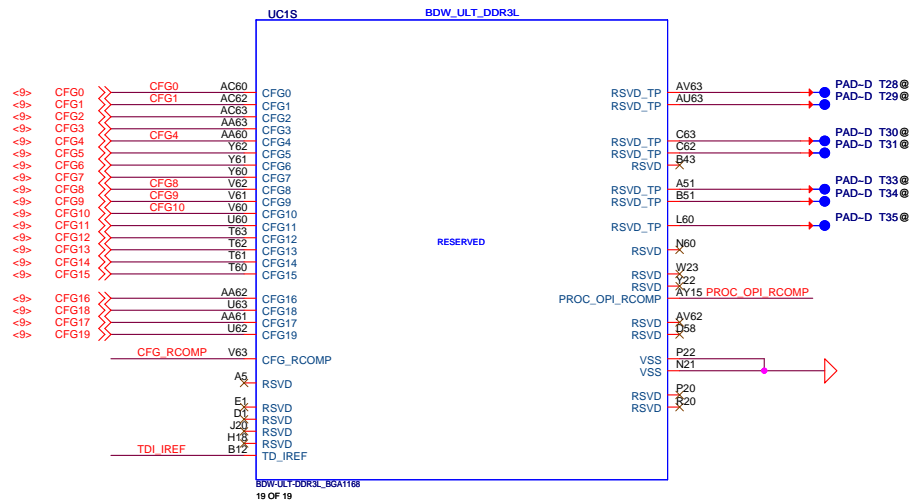
| NO REBOOT STRAP | |
|-----------------|---------|
| HIGH | ENABLE |
| LOW(DEFAULT) | DISABLE |

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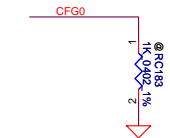
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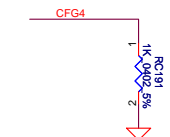
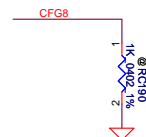
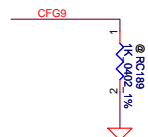
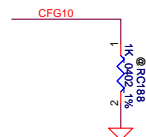
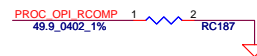
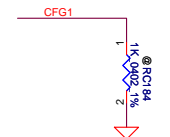


CFG STRAPS for CPU

| EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE | |
|---|---|
| CFG0 | 1:(Default) Normal Operation; No stall 0:Lane Reversed |



| PCH/PCH LESS MODE SELECTION | |
|-----------------------------|---|
| CFG1 | 1:(Default) Normal Operation 0:Lane Reversed |



| SAFE MODE BOOT | |
|----------------|--|
| CFG10 | 1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED |

| NO SVID PROTOCOL CAPABLE VR CONNECTED | |
|---------------------------------------|--|
| CFG9 | 1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity |

| ALLOW THE USE OF NOA ON LOCKED UNITS | |
|--------------------------------------|---|
| CFG8 | 1: Enable(Default): Noa will be disable in locked units and enable in un-locked 0:Disable Noa will be available pegrardless of the locking of the unit |

| Display Port Presence Strap | |
|-----------------------------|--|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

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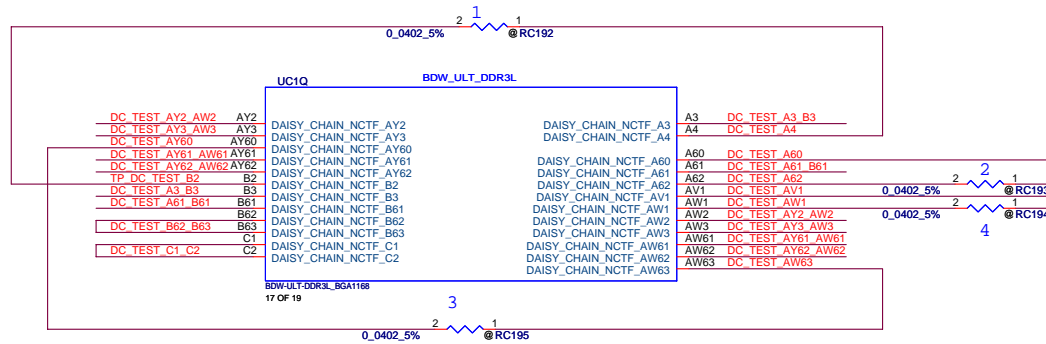


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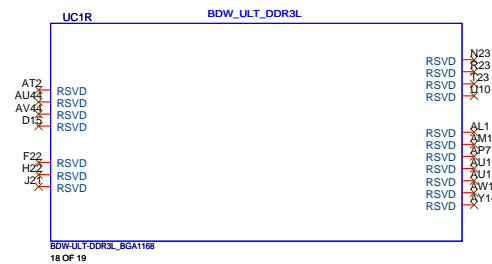
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Package Daisy Chain:

1. B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2. A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3. AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4. AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



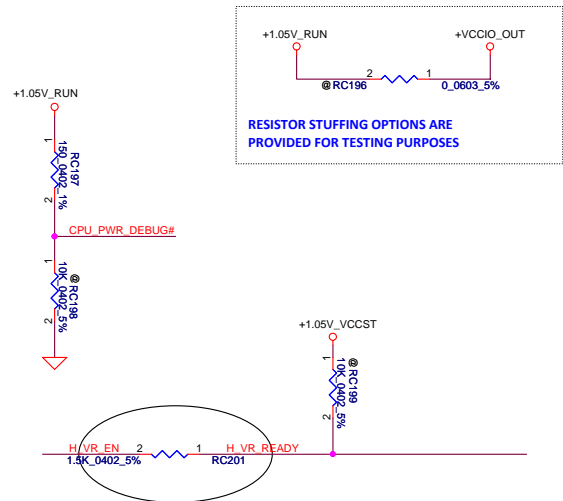
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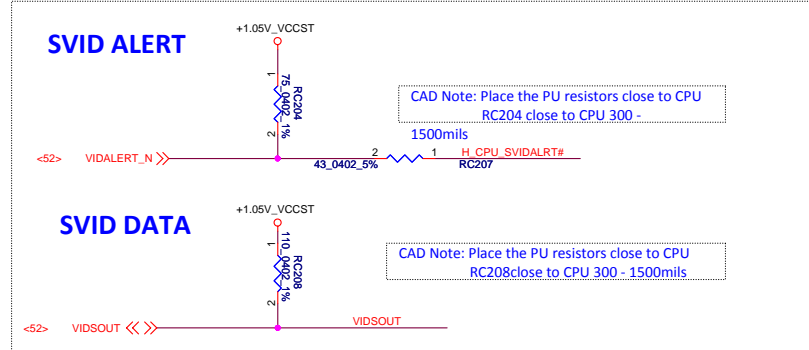
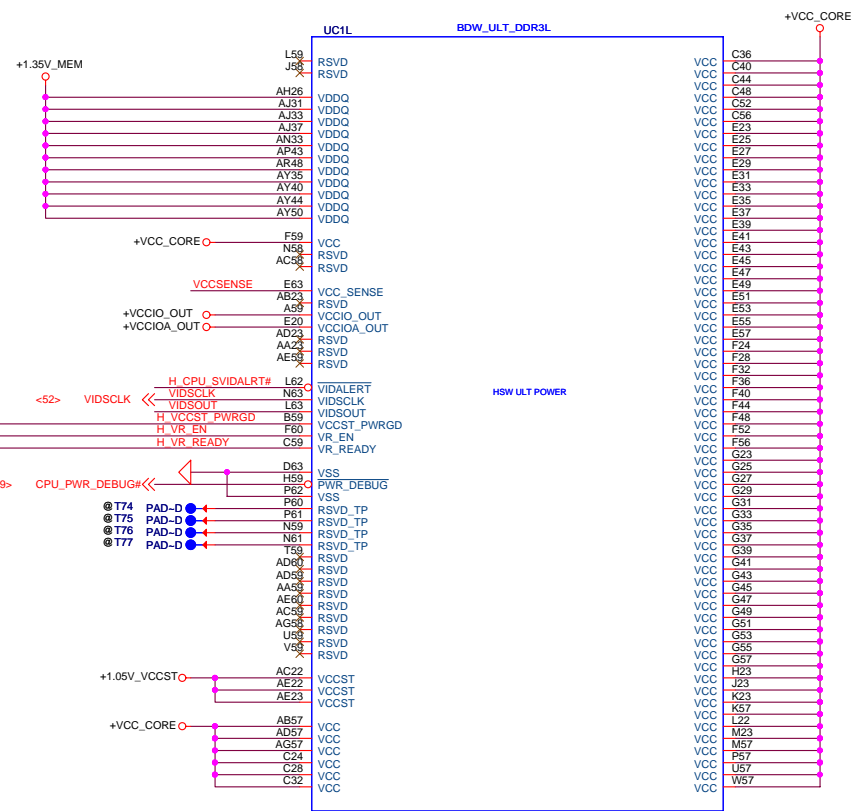
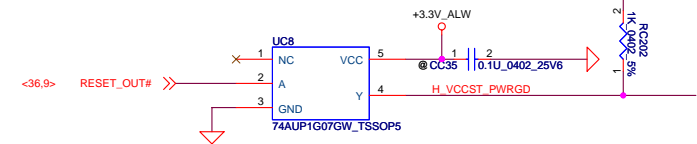
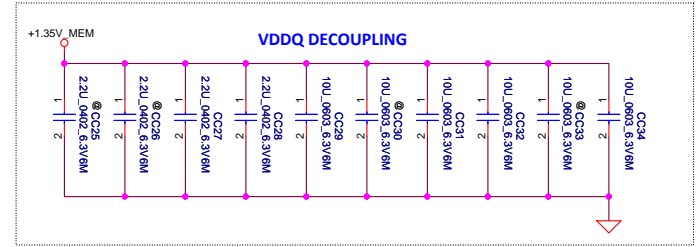
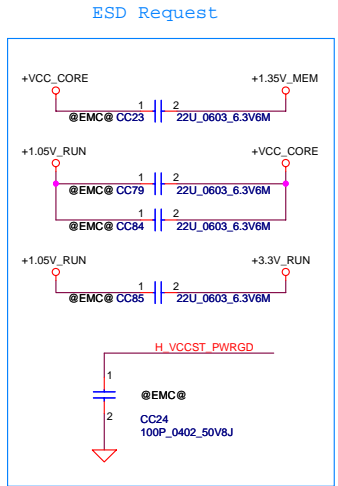


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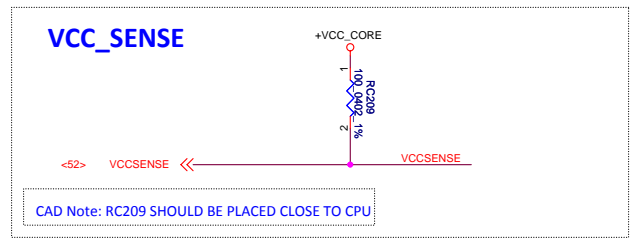


RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES

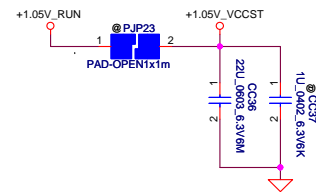


CAD Note: Place the PU resistors close to CPU RC204 close to CPU 300 -

CAD Note: Place the PU resistors close to CPU RC208 close to CPU 300 - 1500mils

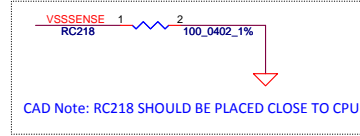
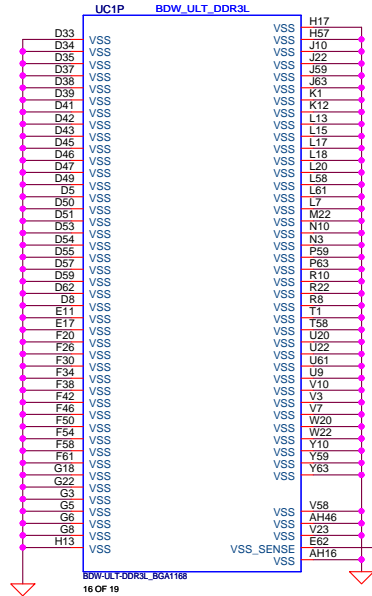
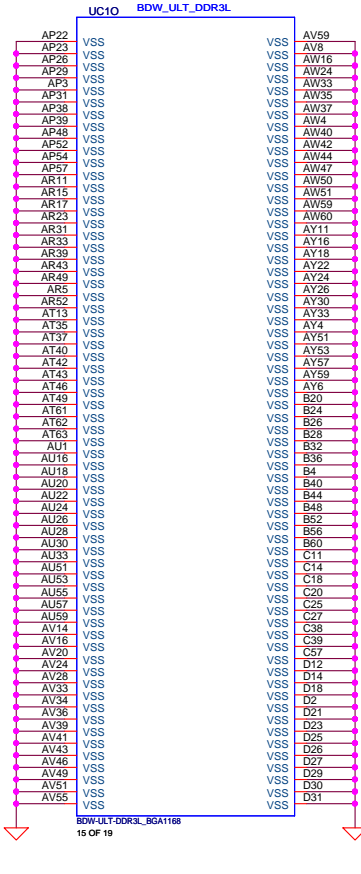
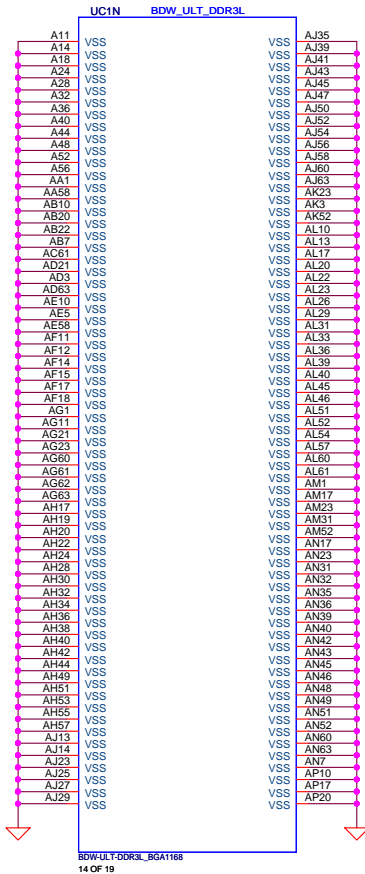


CAD Note: RC209 SHOULD BE PLACED CLOSE TO CPU



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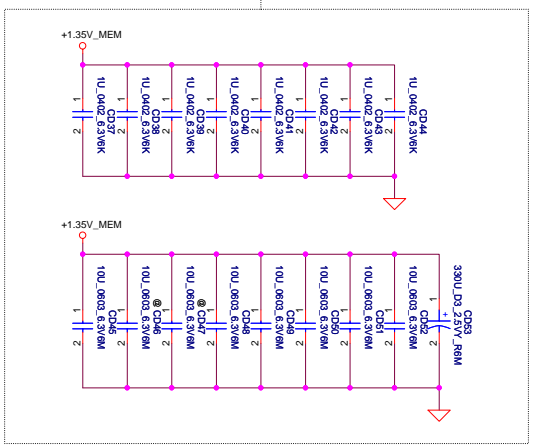
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H=4mm
Reverse Type

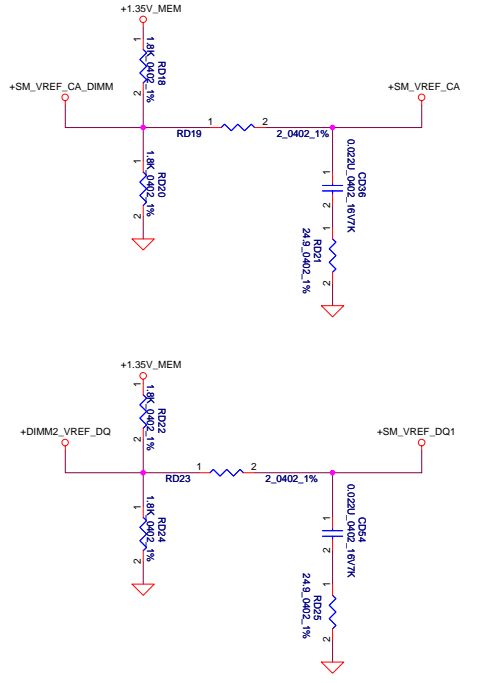
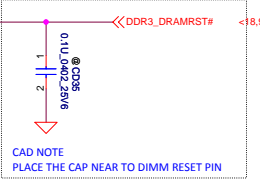
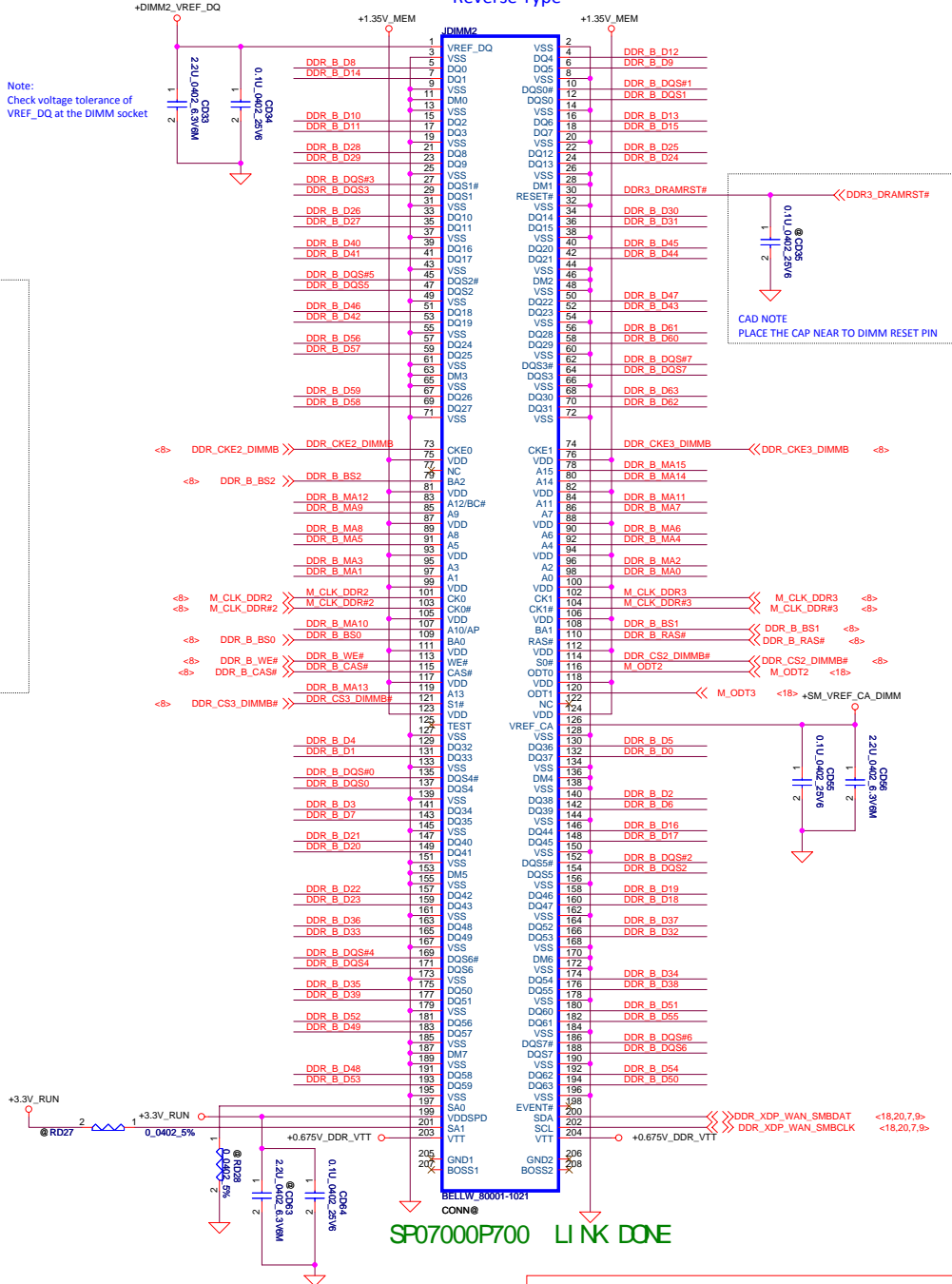
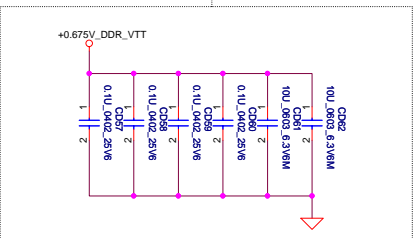


Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2



Layout Note:
Place near
JDIMM2.203,204



BELLW 80001-1021
CONN@
SP07000P700 LINK DONE

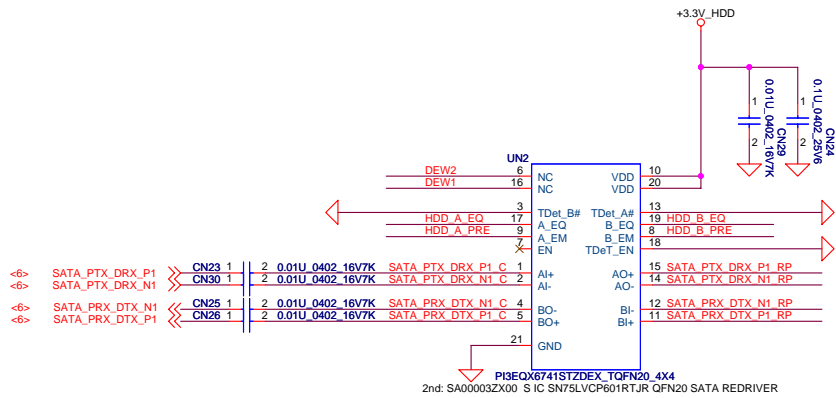
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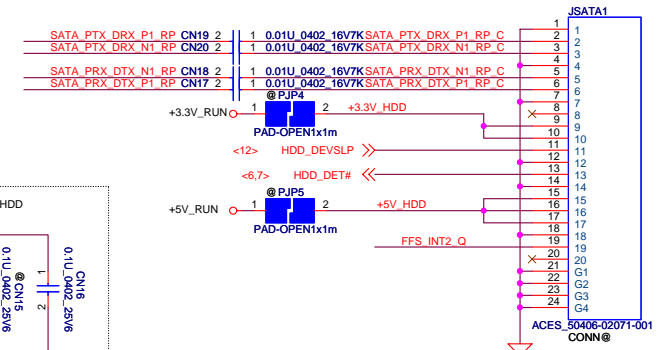
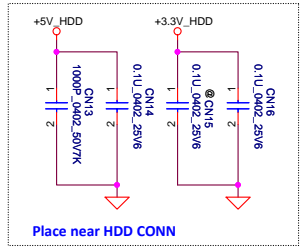
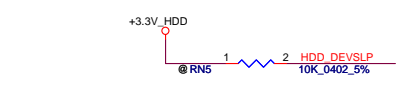
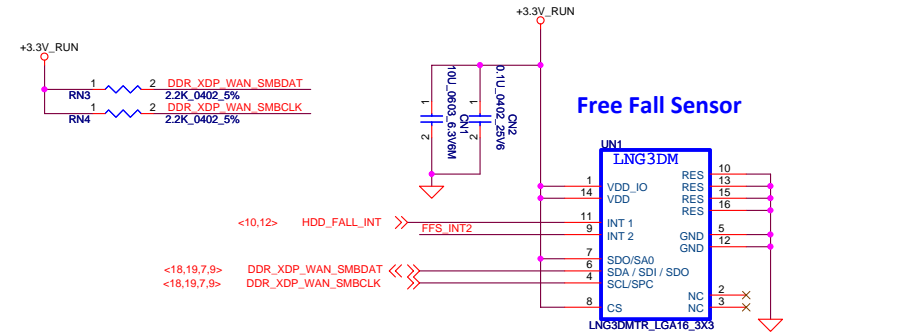
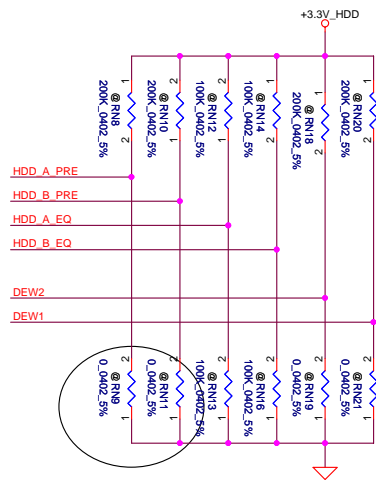
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SATA Repeater



PERICOM PI3EQX6741ST:
Pin6/16, NC
Pin8/9, Pre-emphasis

TI SN75LVCP601RTJR
Pin6/16, de-emphasis width setup
Pin8/9, de-emphasis



SP010016L00 LI NK DONE

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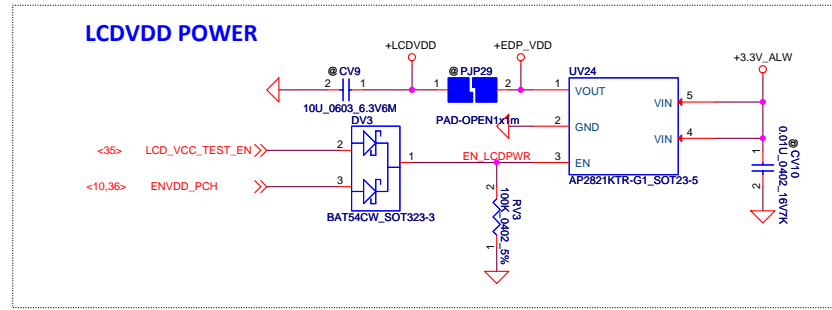
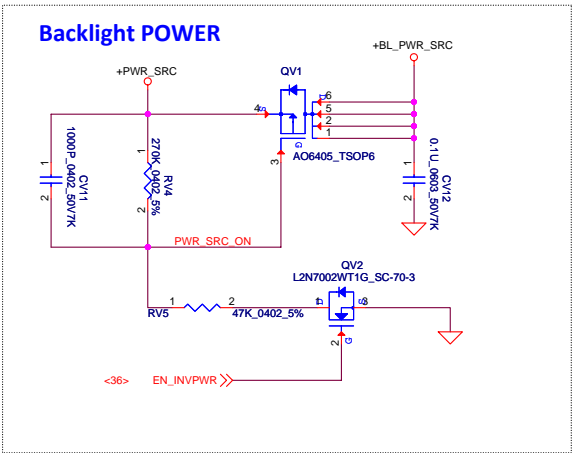
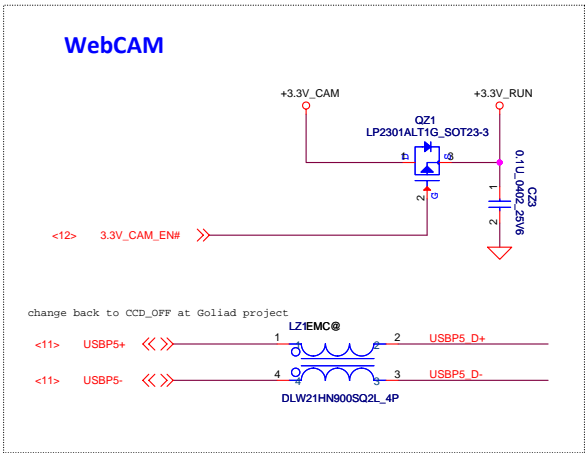
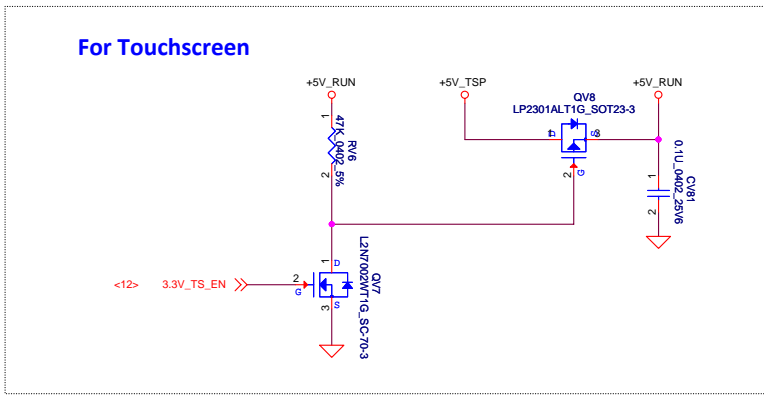
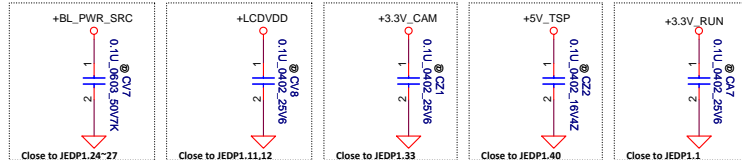
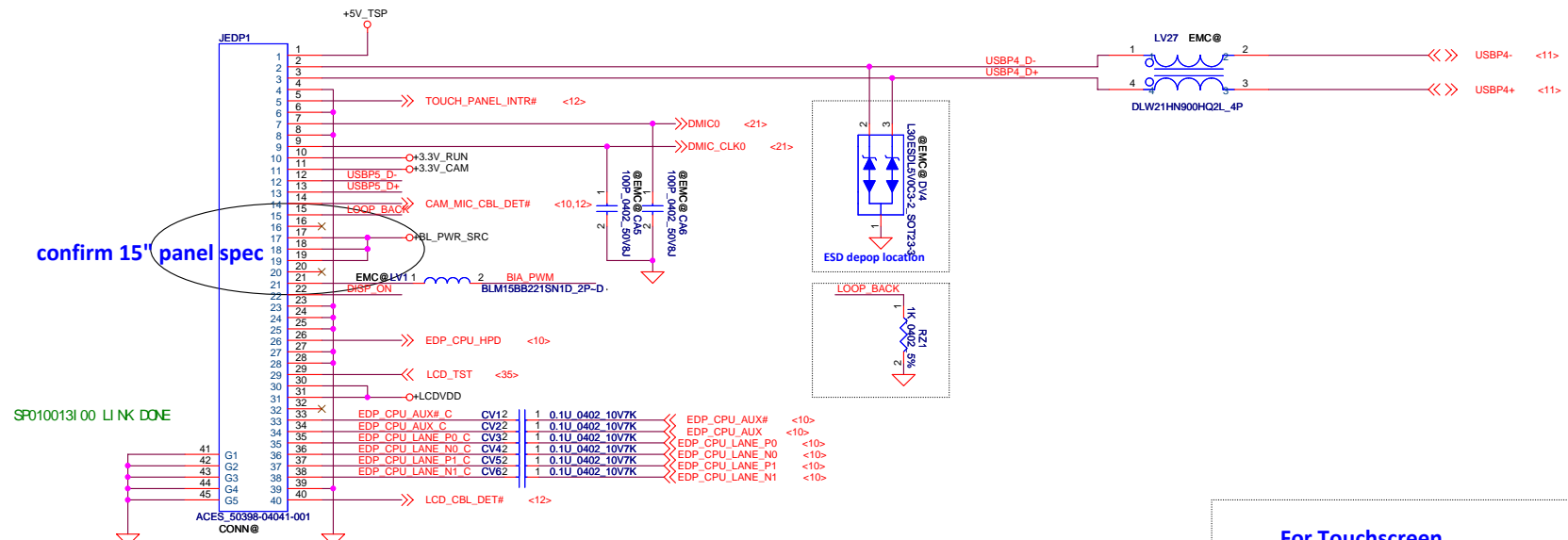
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confirm 15" panel spec

SP0100131 00 LINK DONE



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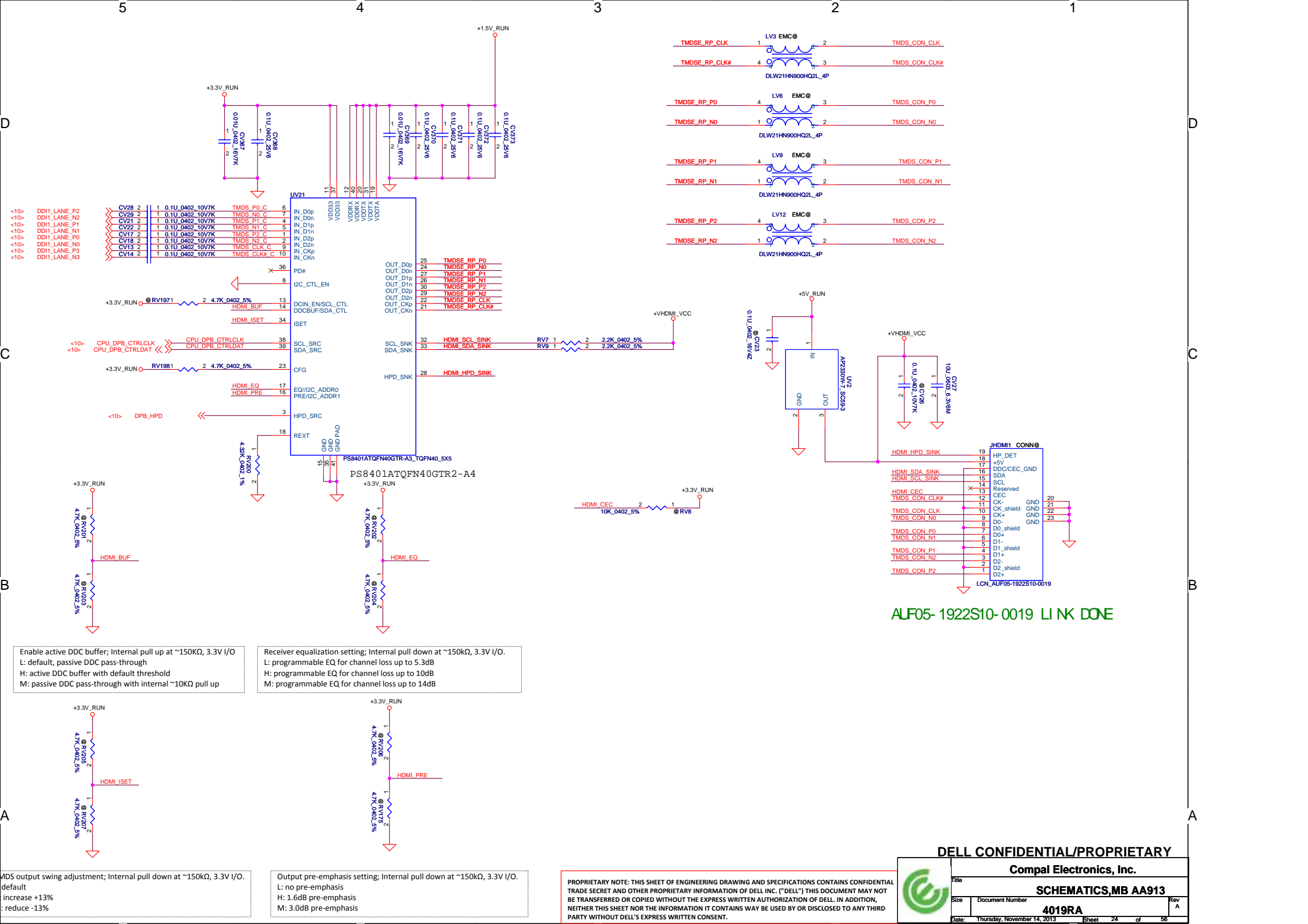
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 <10> DD1_LANE_N2
 <10> DD1_LANE_P1
 <10> DD1_LANE_N1
 <10> DD1_LANE_P0
 <10> DD1_LANE_N0
 <10> DD1_LANE_P3
 <10> DD1_LANE_N3

<10> CPU_DPB_CTRLCLK
 <10> CPU_DPB_CTRLDAT

<10> DPB_HPD

Enable active DDC buffer; Internal pull up at ~150kΩ, 3.3V I/O
 L: default, passive DDC pass-through
 H: active DDC buffer with default threshold
 M: passive DDC pass-through with internal ~10kΩ pull up

Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: programmable EQ for channel loss up to 5.3dB
 H: programmable EQ for channel loss up to 10dB
 M: programmable EQ for channel loss up to 14dB

TMDS output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
 default
 increase +13%
 reduce -13%

Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: no pre-emphasis
 H: 1.6dB pre-emphasis
 M: 3.0dB pre-emphasis

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AUF05-1922S10-0019 LI NK DONE

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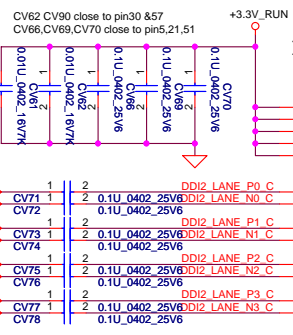
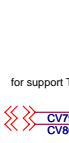
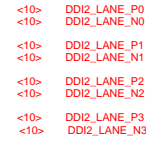
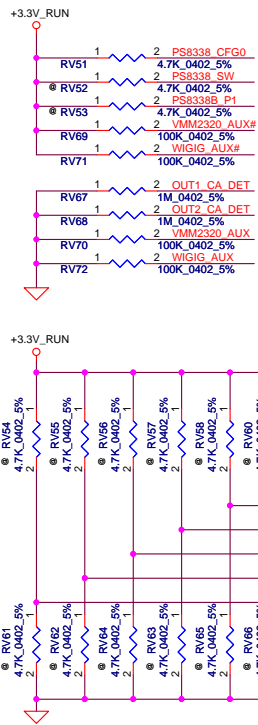
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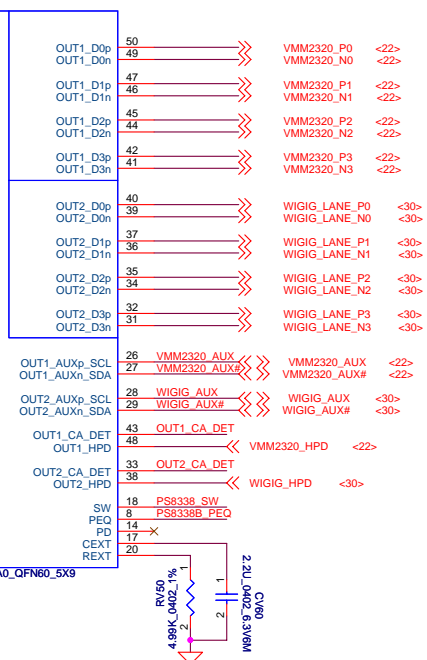
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12" use 8339
 14"/15" use 8338 at DOCK config
 14"/15" use 12412 at Entry config

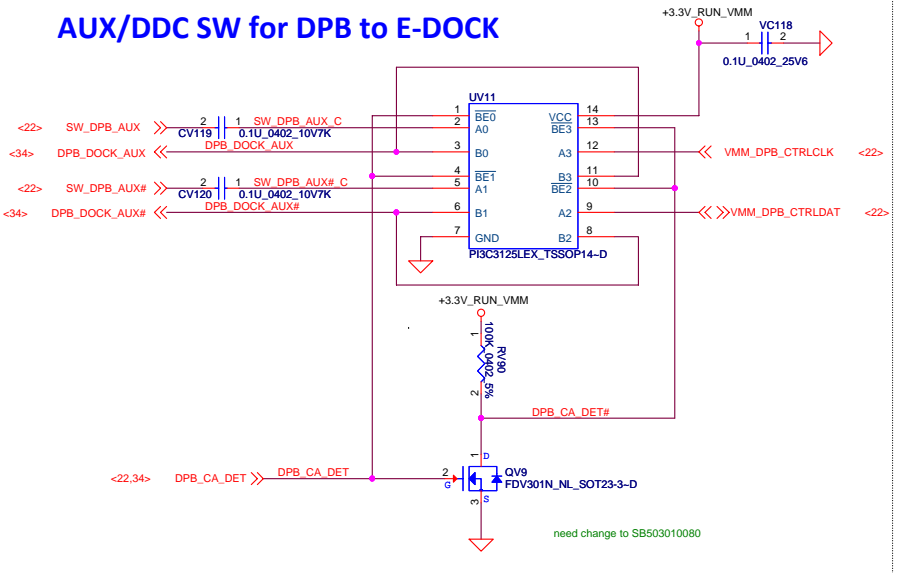
| PCB | DP SWITCH |
|-----------|----------------|
| H12 UMA | PS8339+DP12412 |
| H12 Entry | PS8339 |
| H14 DSC | PS8338 |
| H14 UMA | PS8338 |
| H14D_En | DP12412 |
| H14U_En | DP12412 |
| H15 DSC | PS8338 |
| H15 UMA | PS8338 |
| H15D_En | DP12412 |
| H15U_En | DP12412 |



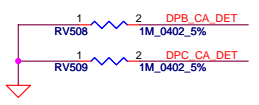
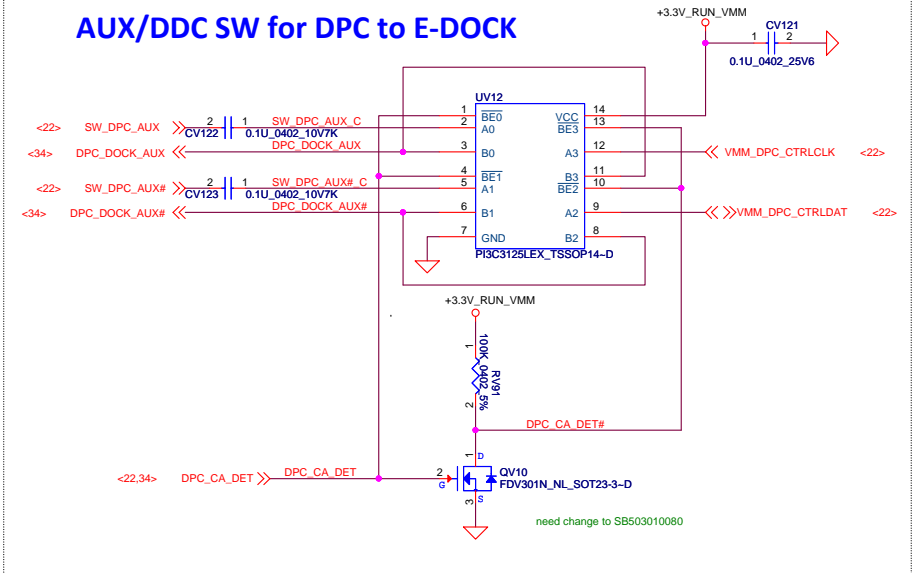
Dock has high priority when both ports plugged



AUX/DDC SW for DPB to E-DOCK



AUX/DDC SW for DPC to E-DOCK



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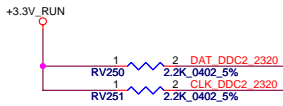
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 SCHEMATICS, MB AA913
 4019RA
 Thursday, November 14, 2013

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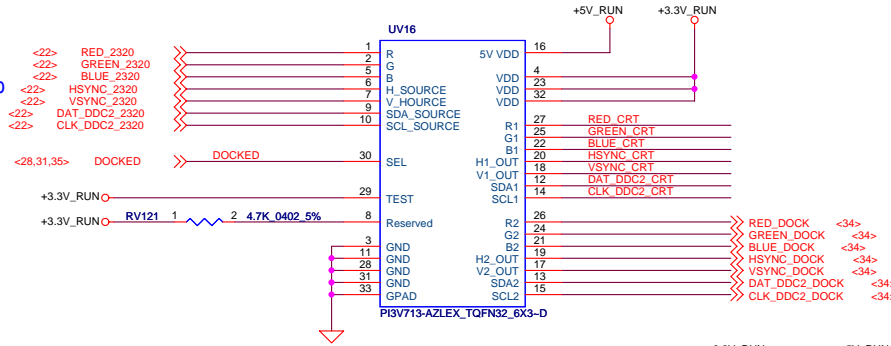
VGA SW for MB/DOCK

VGA SW

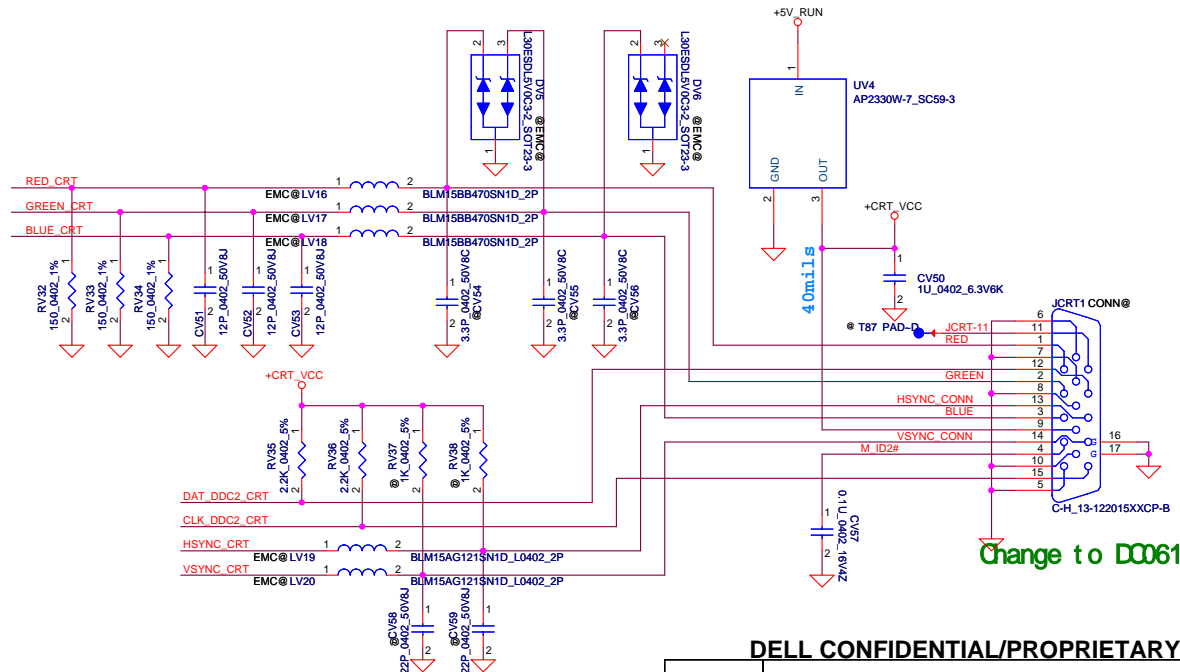
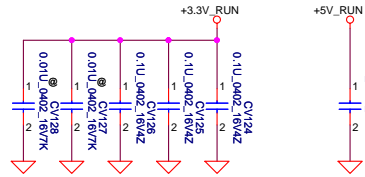
| PCB | VGA SWITCH |
|-----------|------------|
| H12 UMA | NA |
| H12 Entry | NA |
| H14 DSC | PI3V713 |
| H14 UMA | PI3V713 |
| H14D_En | NA |
| H14U_En | NA |
| H15 DSC | PI3V713 |
| H15 UMA | PI3V713 |
| H15D_En | NA |
| H15U_En | NA |



source from VMM2320



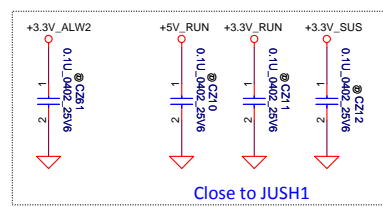
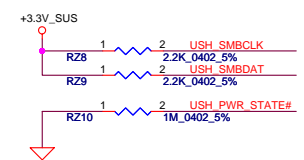
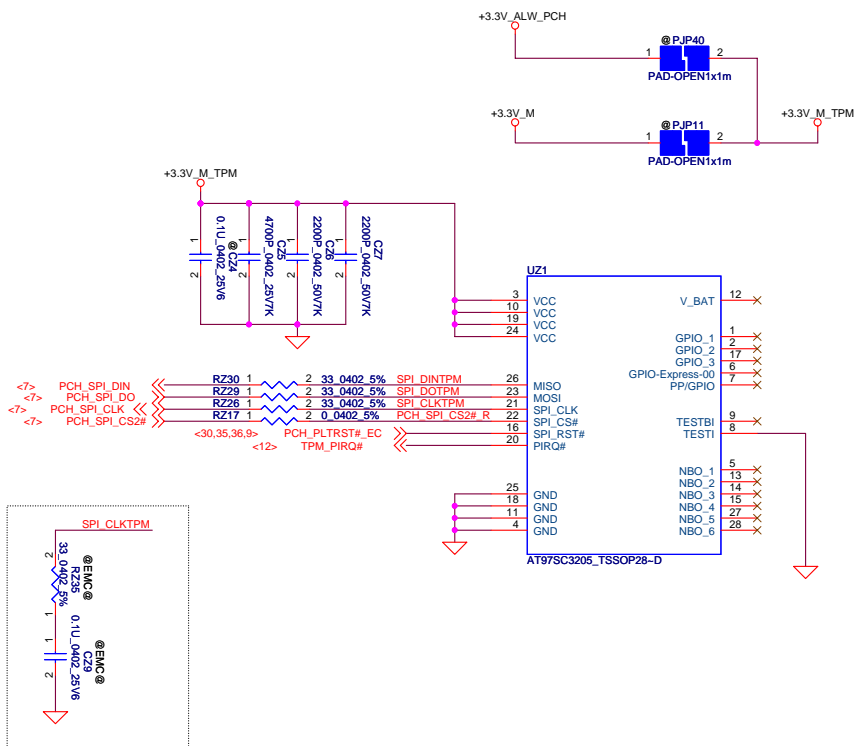
| SEL1/SEL2 | Chanel | Source |
|-----------|--------|---------|
| 0 | A=B1 | MB |
| 1 | A=B2 | APR/SPR |



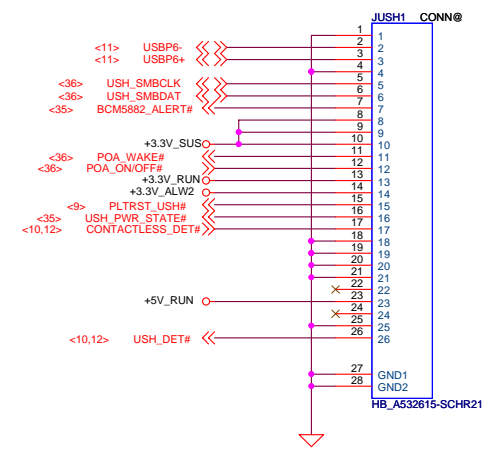
Change to D0061307290.

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USH CONN



SP01001SF00 LI NK DONE

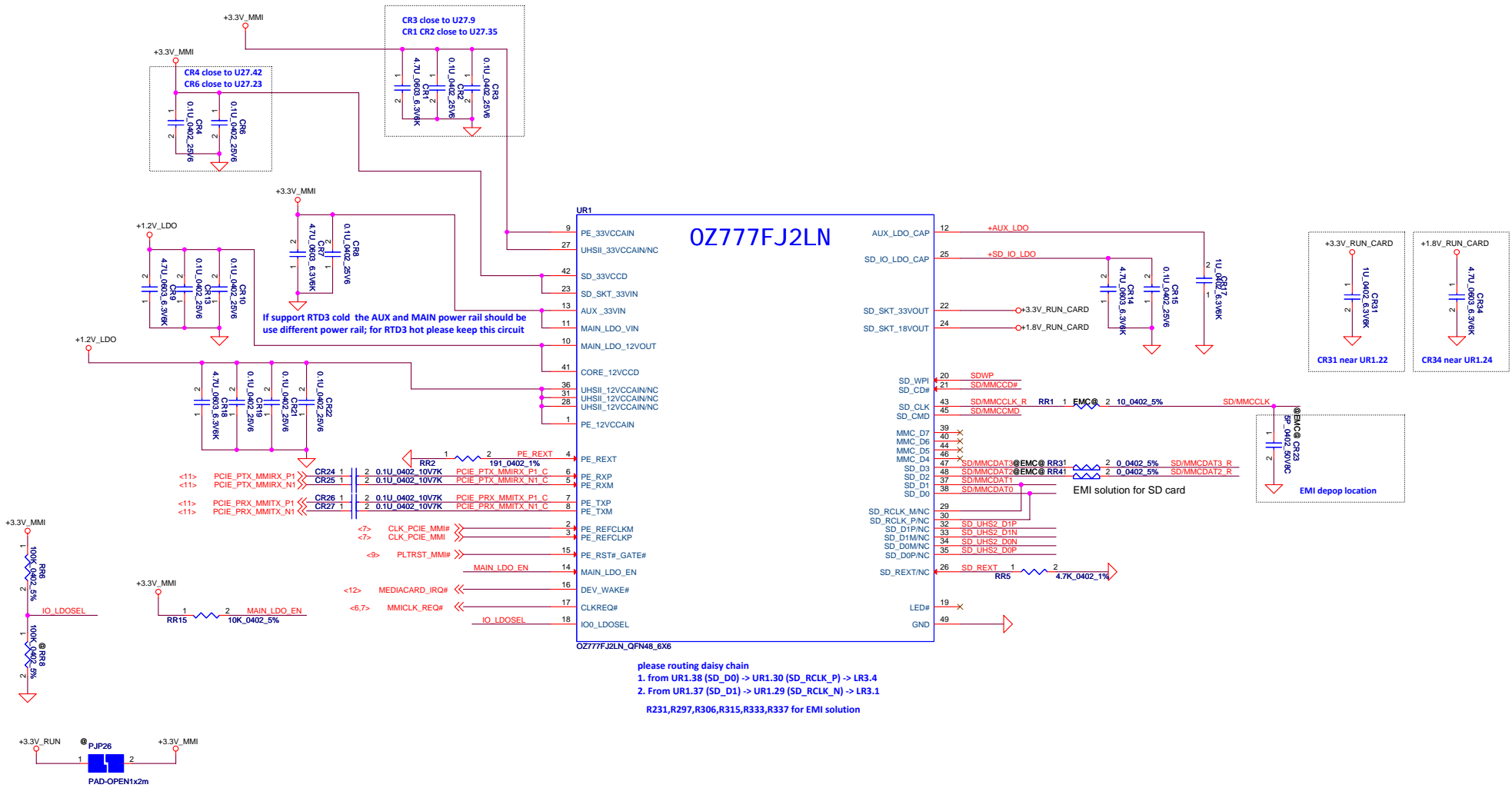
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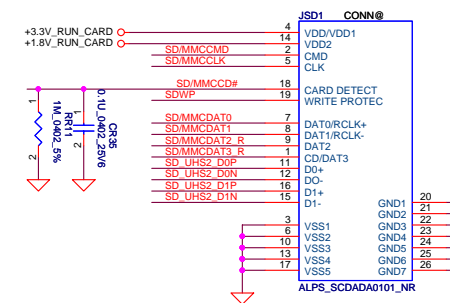


| | | | |
|-------|-----------------------------|---------------------|-------|
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please routing daisy chain
 1. from UR1.38 (SD_D0) -> UR1.30 (SD_RCLK_P) -> LR3.4
 2. From UR1.37 (SD_D1) -> UR1.29 (SD_RCLK_N) -> LR3.1
 R231,R297,R306,R315,R333,R337 for EMI solution



SF070011L00 LI NK DONE

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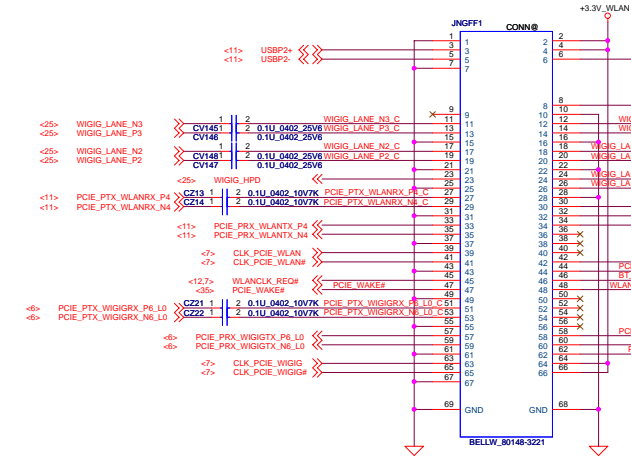
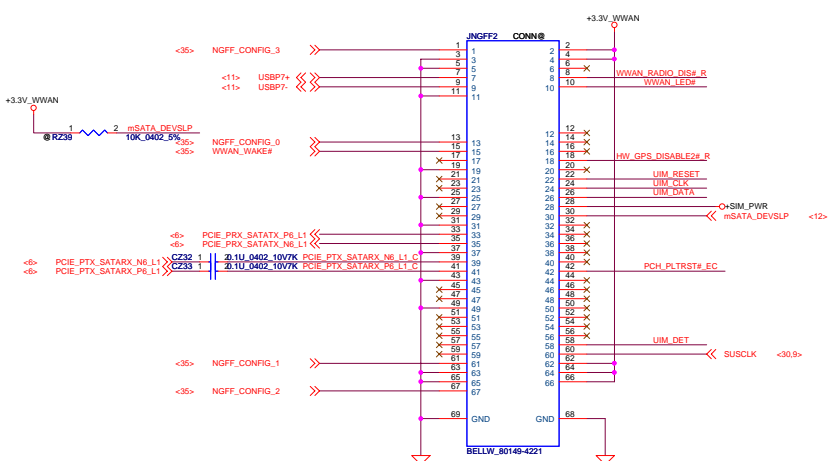
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|-------|-----------------------------|---------------------|----------|
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NGFF slot B Key B

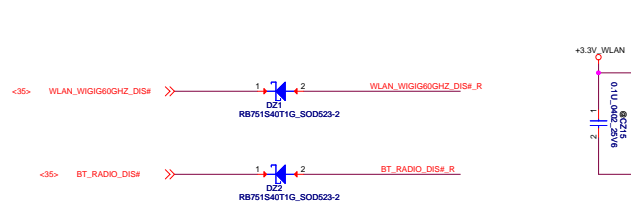
NGFF for DSC

NGFF slot A Key A



80149-4221 LINK DONE

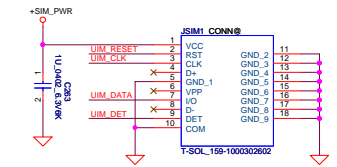
80148-3221 LINK DONE



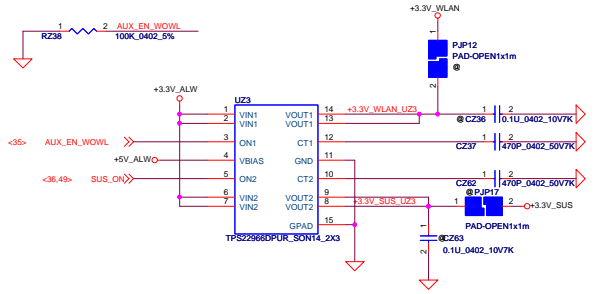
| STATE # | CONFIG_0 | CONFIG_1 | CONFIG_2 | CONFIG_3 | Module Type |
|---------|----------|----------|----------|----------|-------------|
| 0 | GND | GND | GND | GND | SSD-SATA |
| 1 | GND | HIGH | GND | GND | SSD-PCIE |
| 8 | HIGH | GND | GND | GND | WWAN |
| 14 | HIGH | GND | HIGH | HIGH | HCA-PCIE |
| 15 | HIGH | HIGH | HIGH | HIGH | NA |

| PWR Rail | Voltage Tolerance | Primary Power | | Aux Power |
|----------|-------------------|---------------|--------|-----------|
| | | Peak | Normal | Normal |
| +3.3V | | | | |

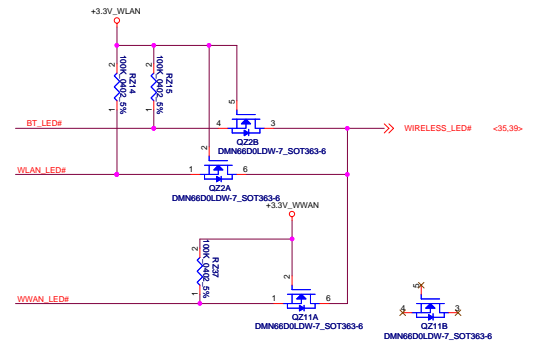
SIM Card Push-Push



SP070011M00 LINK DONE



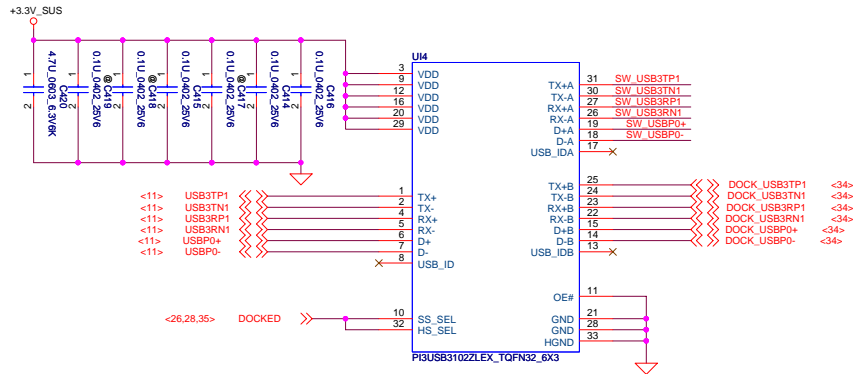
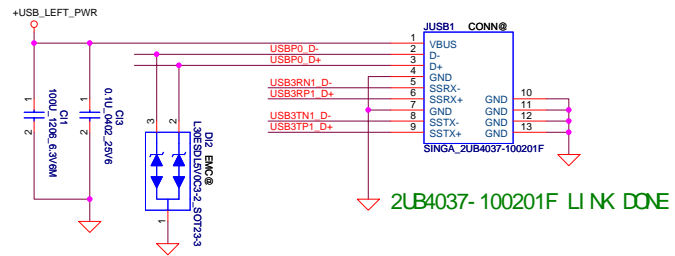
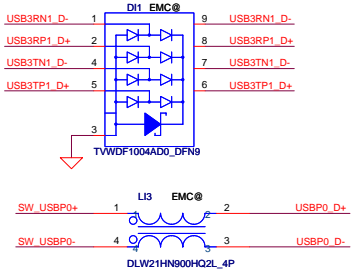
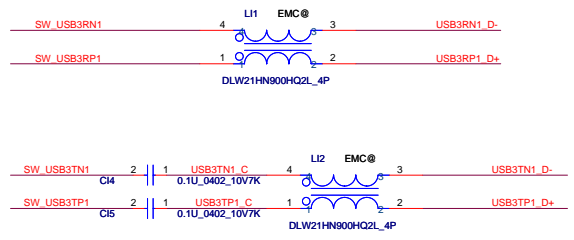
LED control circuit



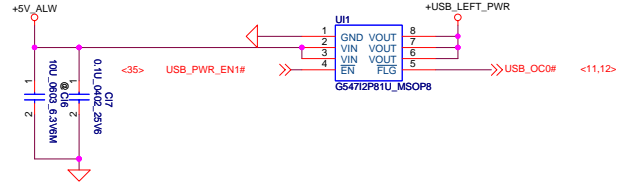
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 Size: Document Number
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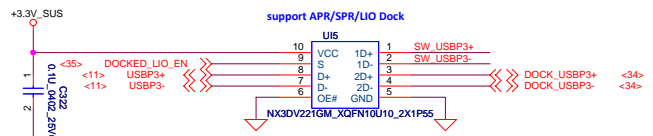
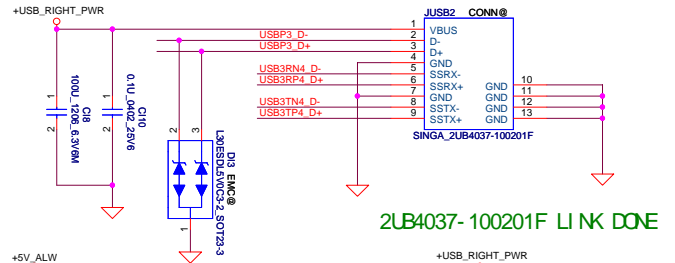
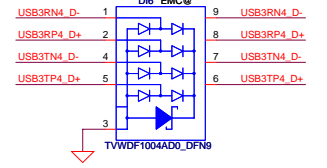
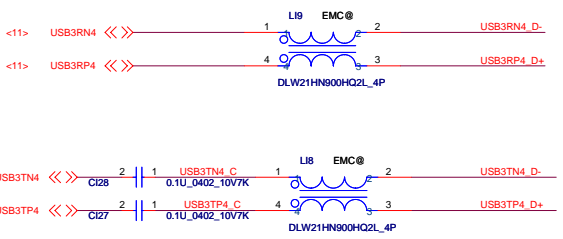


| PCB | USB2 0 | USB2 3 |
|-----------|---------|----------|
| H12 UMA | USB3102 | NX3DV221 |
| H12 Entry | NA | NA |
| H14 DSC | USB3102 | NX3DV221 |
| H14 UMA | USB3102 | NX3DV221 |
| H14D_En | NA | NA |
| H14U_En | NA | NA |
| H15 DSC | USB3102 | NX3DV221 |
| H15 UMA | USB3102 | NX3DV221 |
| H15D_En | NA | NA |
| H15U_En | NA | NA |



check port mapping

| DOCKED | function |
|--------|----------|
| 1 | Dock |
| 0 | M/B |



check port mapping

| DOCKED_LIO_EN | function |
|---------------|----------|
| 1 | Dock |
| 0 | M/B |

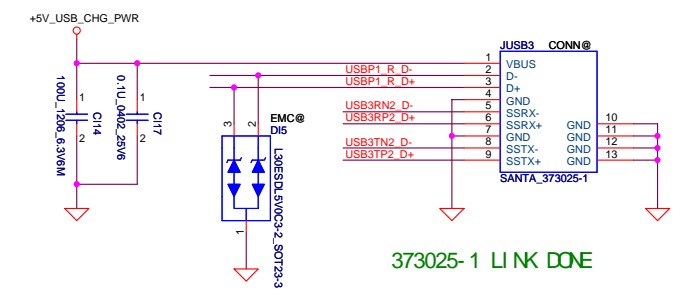
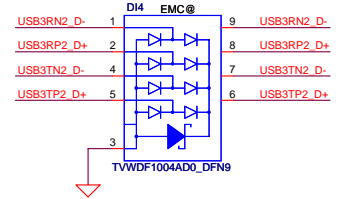
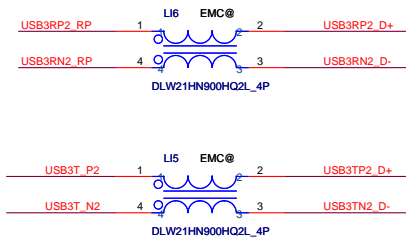
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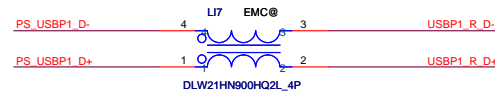
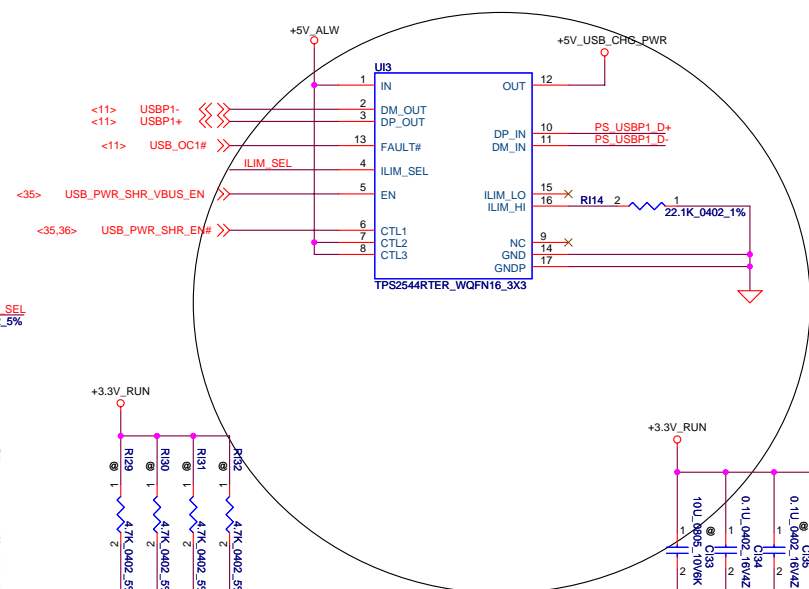


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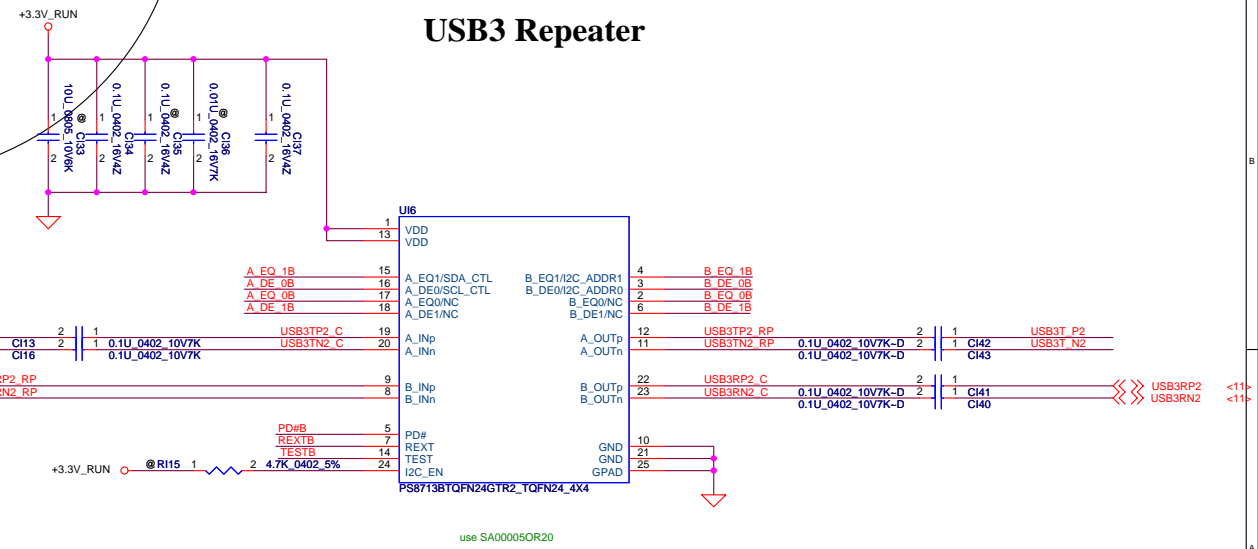
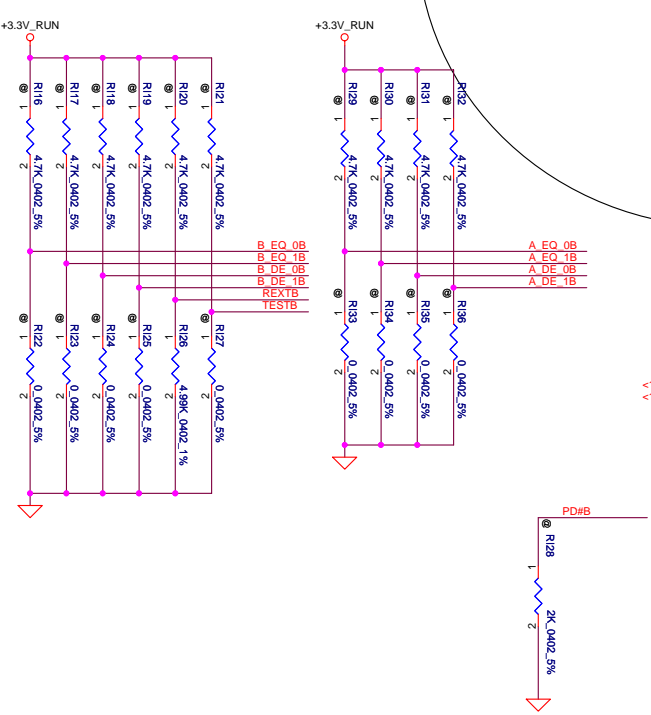
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373025-1 LINK DONE



USB3 Repeater



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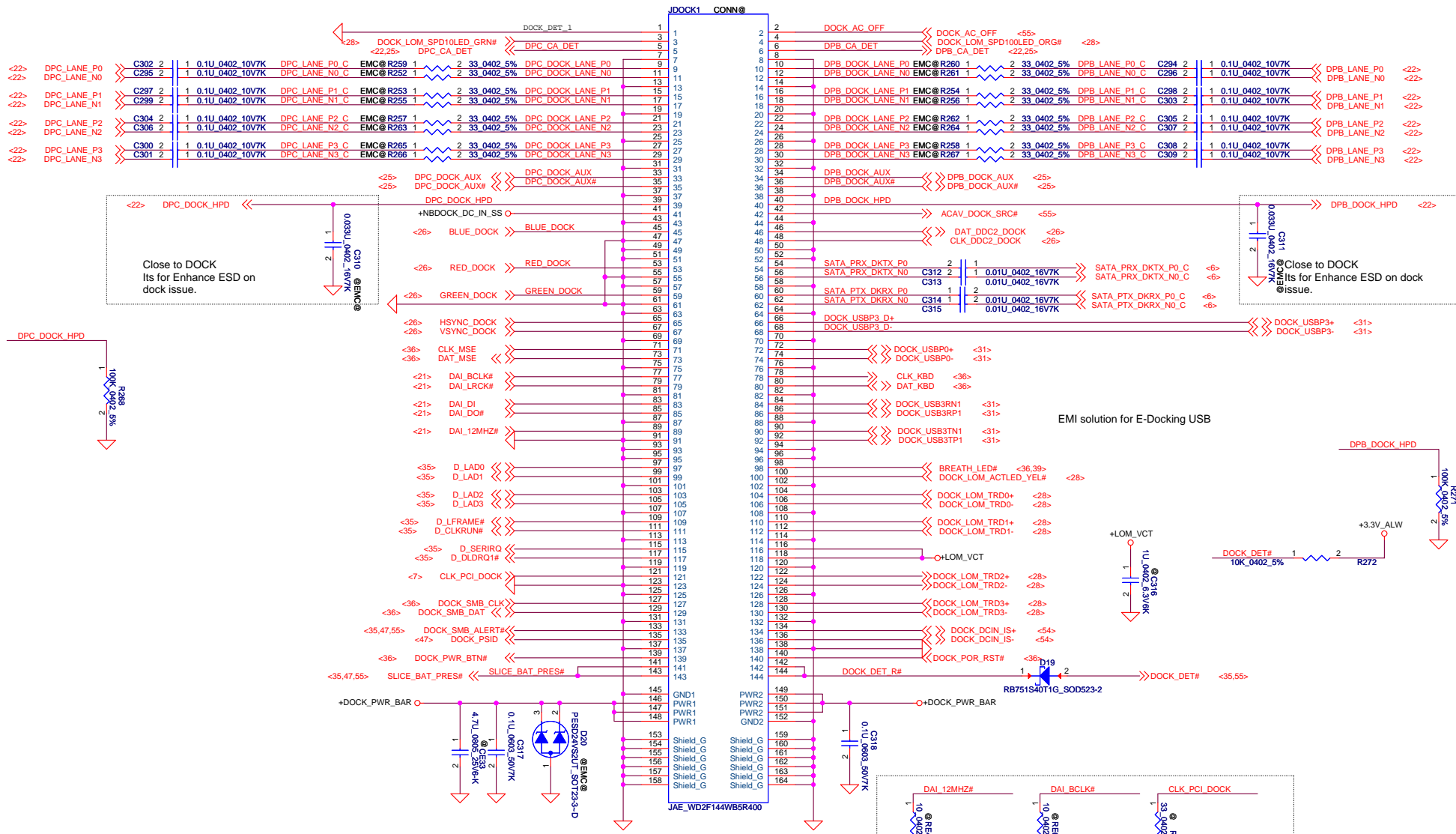
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Doesn't support.

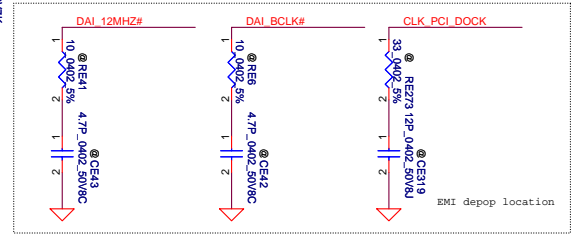
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SP0300013A0 LI NK DONE



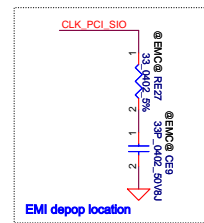
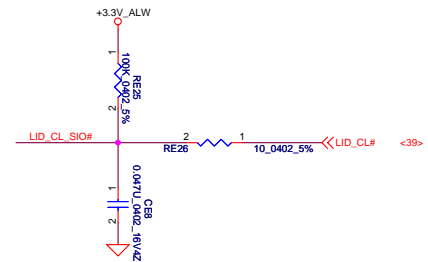
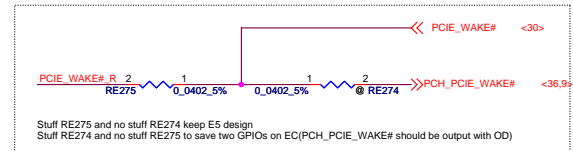
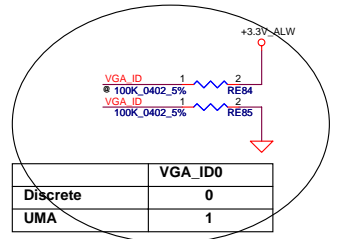
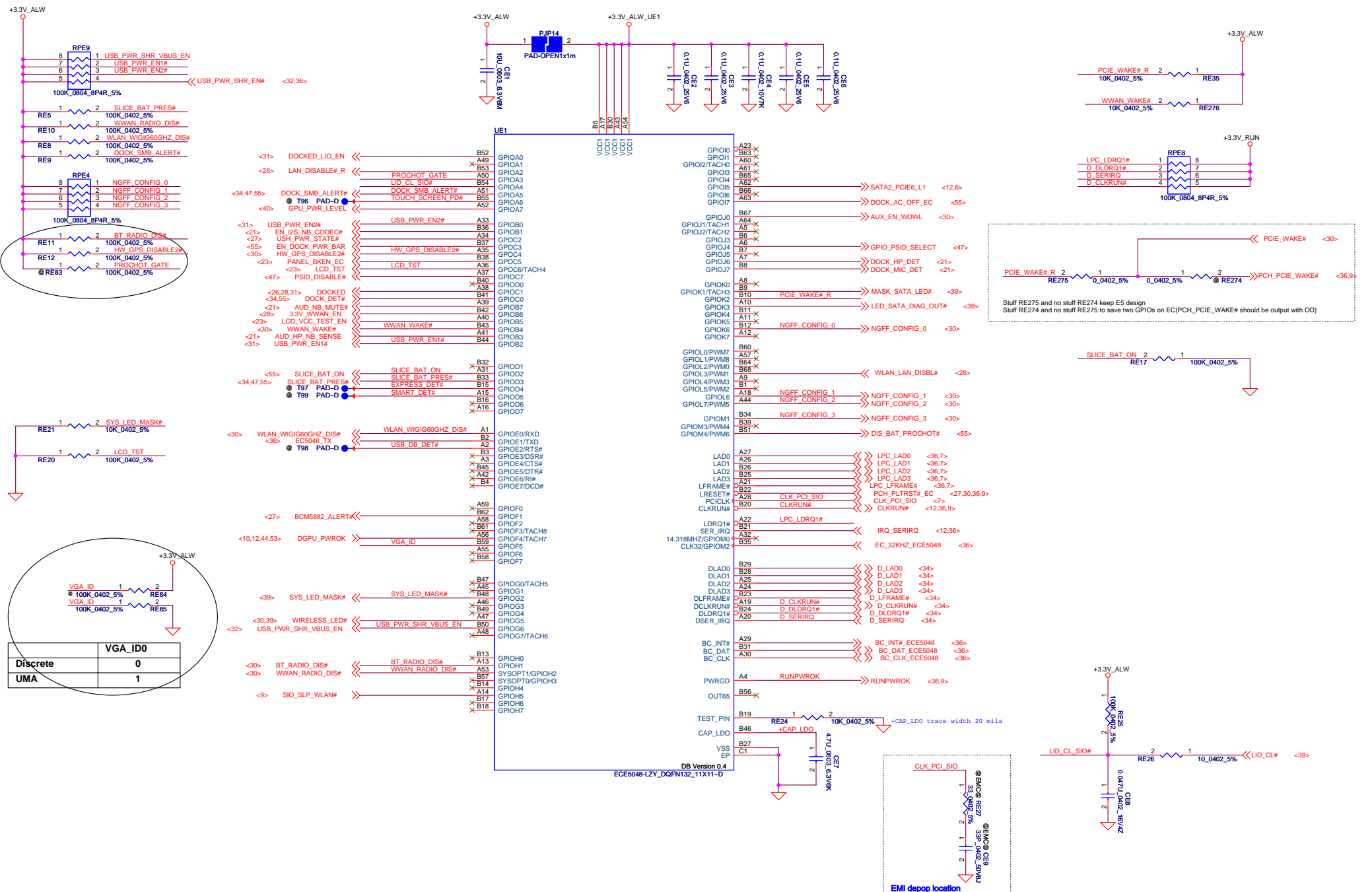
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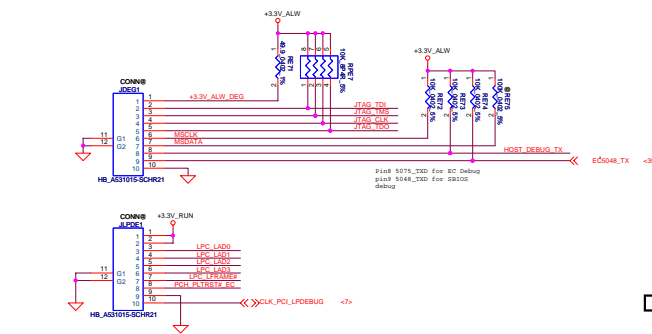
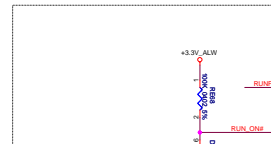
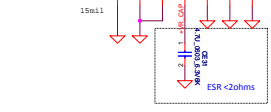
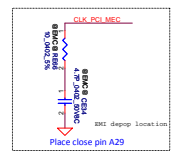
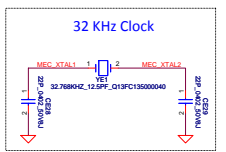
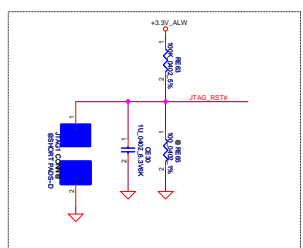
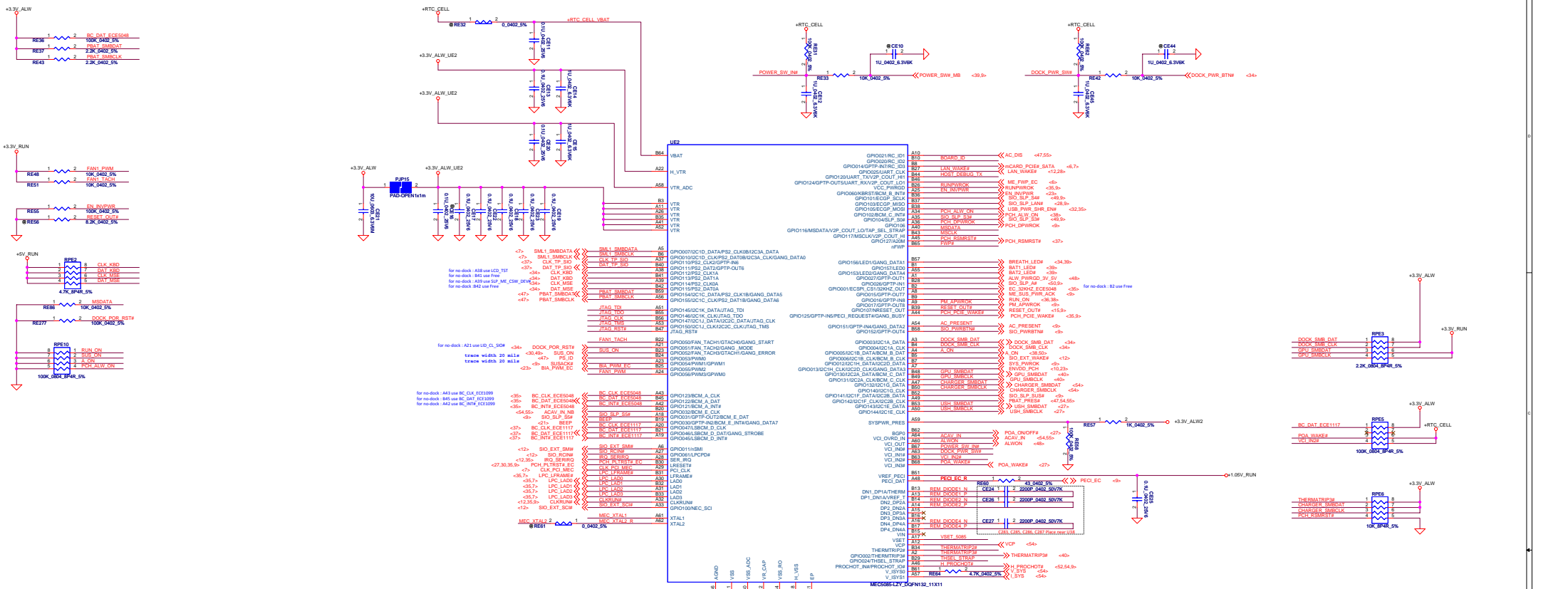


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| REV | DESCRIPTION | DATE |
|------|-------------|------|
| RE79 | CE40 | REV |
| 240K | 4700p | X00 |
| 130K | 4700p | X01 |
| 33K | 4700p | X02 |
| 1K | 4700p | A00 |

BOARD_ID rise time is measured from 5%-68%

Setting for Thermal Design

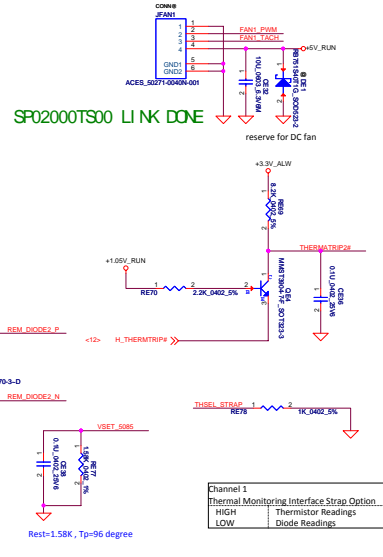
| 5085 Channel | Location |
|--------------|----------|
| DP1/DN1 | CPU |
| DP2/DN2 | DIMM |
| DN2a/DP2a | WIGIG |
| DP4/DN4 | V.R |

Place QE3 under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WIGig on QE7, place QE7 close to WIGig and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.



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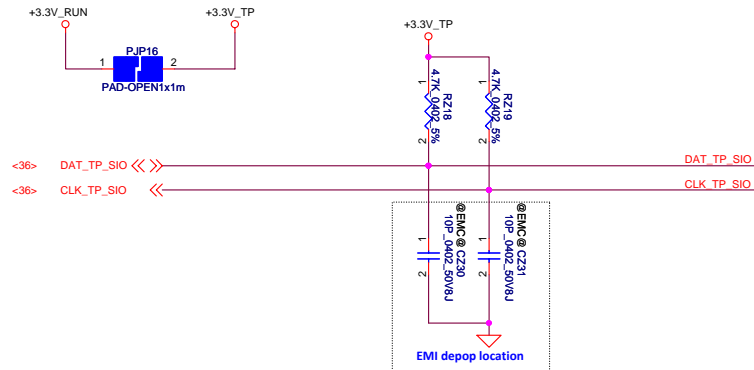
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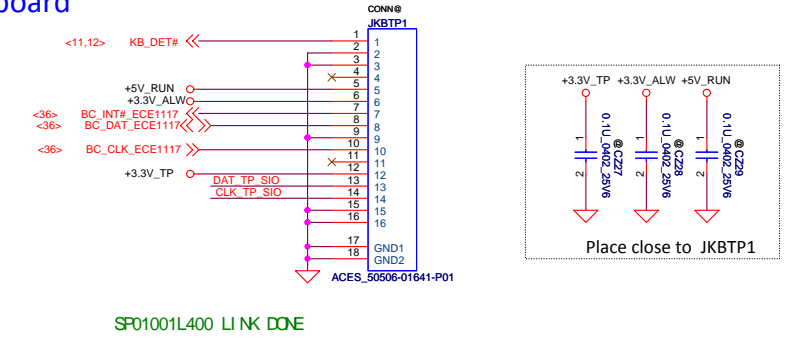
Channel 1
Thermal Monitoring Interface Strap Option
HIGH Thermistor Readings
LOW Diode Readings

SCHEMATICS_MB AA913
4019RA
Thursday, November 14, 2013

Touch Pad

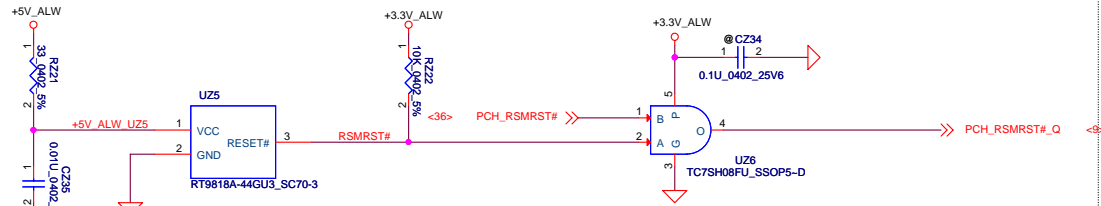


Keyboard



SP01001L400 LI NK DONE

RSMRST circuit



@eDP Cable

| Part Number | Description |
|-------------|-----------------------|
| DC02C007A00 | H-COHN SET 13M MB-EDP |

@eDP Cable w camera

| Part Number | Description |
|-------------|------------------------------|
| DC02C007900 | H-COHN SET 13M MB-EDP-CAMERA |

@eDP TS Cable w camera

| Part Number | Description |
|-------------|---------------------------------|
| DC02C007800 | H-COHN SET 13M MB-EDP-CAMERA-TS |

@SATA Cable-Spindle HDD

| Part Number | Description |
|-------------|-------------------------------|
| DC02C007800 | H-COHN SET 13M MB-SPINDLE HDD |

@SATA Cable-mSATA

| Part Number | Description |
|-------------|-----------------------------|
| DC02C007700 | H-COHN SET 13M MB-mSATA HDD |

@DC-IN Cable

| Part Number | Description |
|-------------|--|
| DC30100MF00 | CONN SET 0VN DCJACK-MB 2DW1003-038110F |

@RTC BATT

| Part Number | Description |
|-------------|--|
| DC30100MF00 | CONN SET 0VN DCJACK-MB 2DW1003-038110F |

@FAN

| Part Number | Description |
|-------------|--------------------------------------|
| DC28A000800 | FAN SET DAQ20 DC5V AB7405HB-HB3 ADPA |

@KBTP FFC

| Part Number | Description |
|-------------|---|
| NBX0001JH00 | FFC 16P G P0.5 PAD=0.3 66.5MM MB-TP 13M |

@Audio Board FFC

| Part Number | Description |
|-------------|--|
| NBX0001JP00 | FFC 12P F P.5 PAD=.35 26.85MM MB-AUDIO/B |

@USH Board FFC

| Part Number | Description |
|-------------|--|
| NBX0001JF00 | FFC 26P G P0.5 PAD=0.3 58MM MB-USH/B 13M |

@LED Board FFC

| Part Number | Description |
|-------------|--|
| NBX0001JM00 | FFC 10P G P.5 PAD.3 192.5MM MB-LED/B 13M |

@PWR Board FFC

| Part Number | Description |
|-------------|---|
| NBX0001JL00 | FFC 6P G P0.5 PAD=0.3 31MM MB-PWR/B 13M |

@FP FFC-Validity

| Part Number | Description |
|-------------|---|
| NBX0001JN00 | FFC 8P F P0.5 PAD=0.3 170MM USH/B-FP VALIDITY |

@FP FFC-TCS

| Part Number | Description |
|-------------|--|
| NBX0001JO00 | FFC 8P F P0.5 PAD=0.3 164.8MM USH/B-FP-TCS |

@Speak

| Part Number | Description |
|-------------|----------------------------|
| PK230003Q0L | SPK PACK ZJX 2.0W 4 OHM FG |

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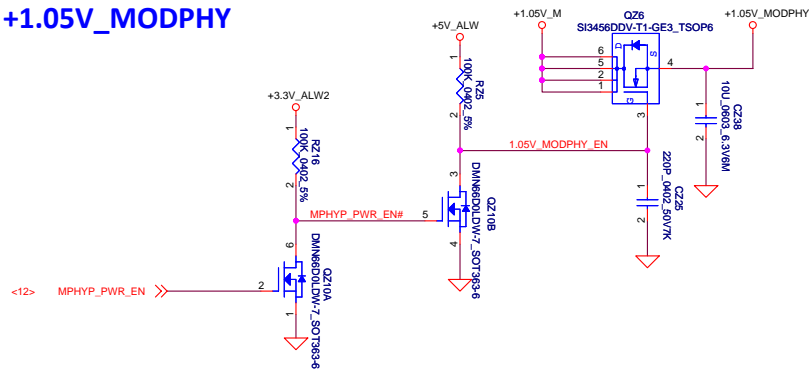
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| SCHEMATICS,MB AA913 | | A | |
| Size | Document Number | Date | Sheet |
| | 4019RA | Thursday, November 14, 2013 | 37 of 56 |

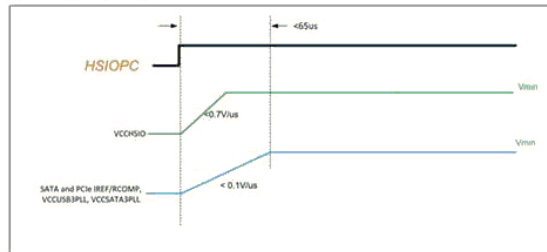
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+1.05V_MODPHY

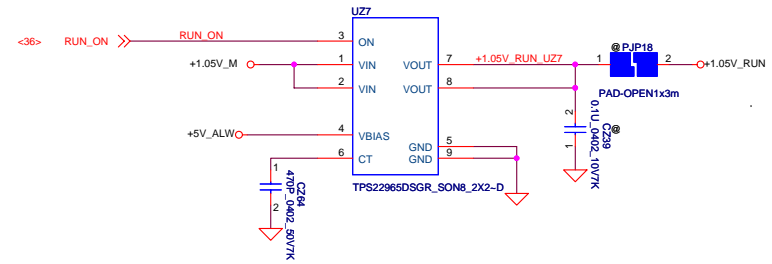


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

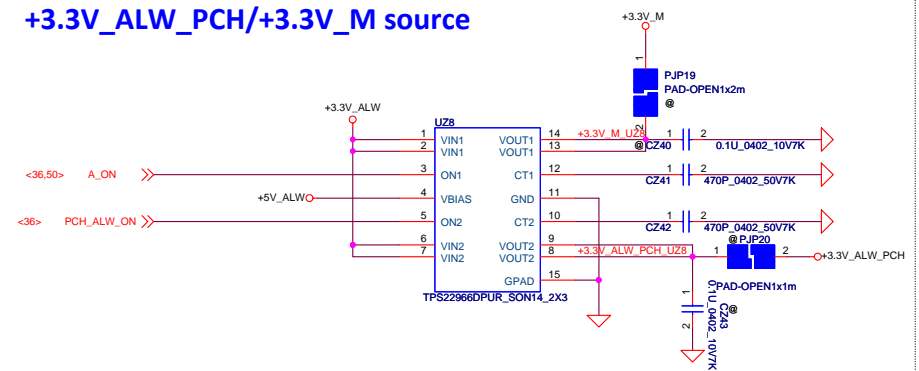
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



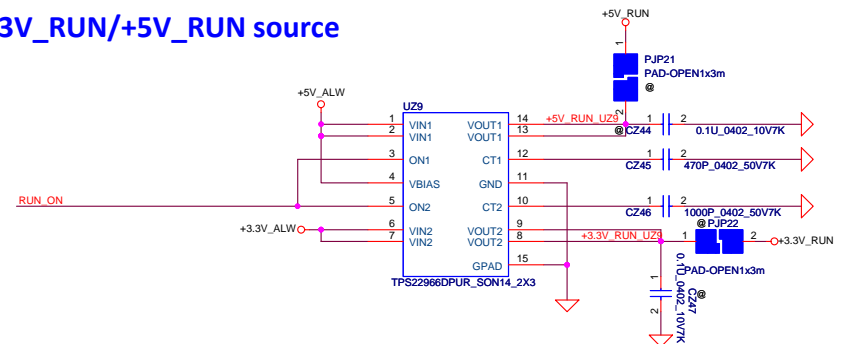
+1.05V_RUN source



+3.3V_ALW_PCH/+3.3V_M source



+3.3V_RUN/+5V_RUN source



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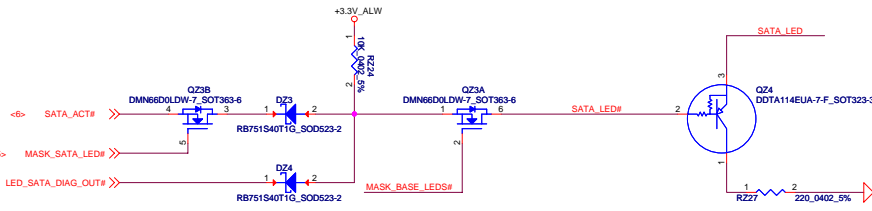
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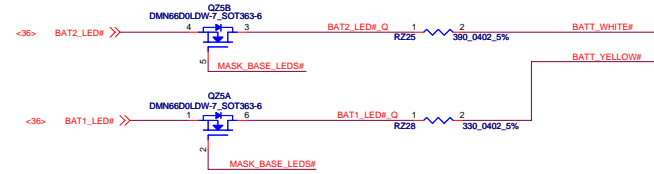
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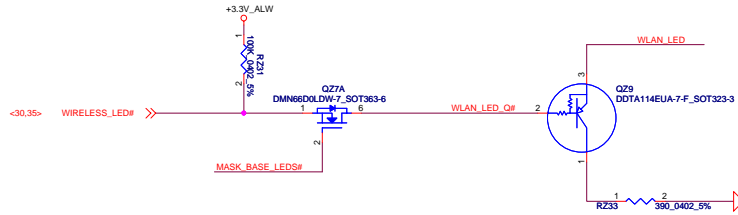
HDD LED solution for White LED



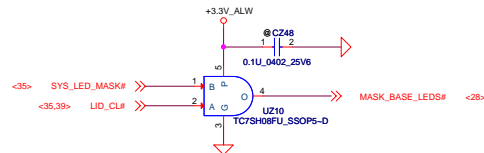
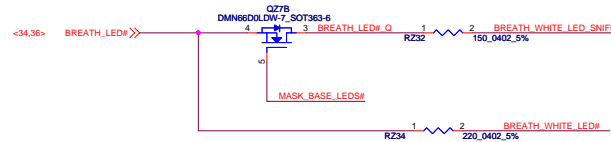
Battery LED



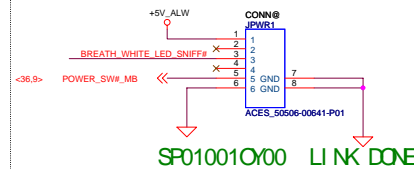
WLAN LED solution for White LED



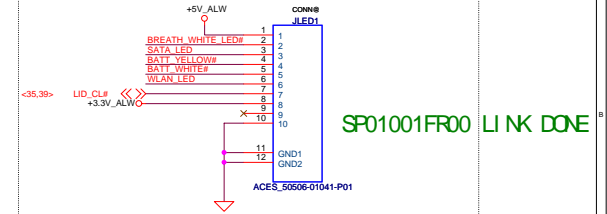
Breath LED



POWER board CONN



LED board CONN

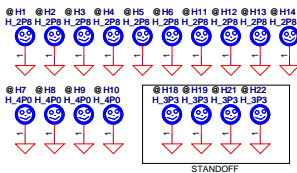


LED Circuit Control Table

| | SYS_LED_MASK# | LID_CL# |
|----------------------------------|---------------|---------|
| Mask All LEDs (Sniffer Function) | 0 | X |
| Mask Base MB LEDs (Lid Closed) | 1 | 0 |
| Do not Mask LEDs (Lid Opened) | 1 | 1 |

Fiducial Mark

- @FD1
FIDUCIAL MARK-D
- @FD2
FIDUCIAL MARK-D
- @FD3
FIDUCIAL MARK-D
- @FD4
FIDUCIAL MARK-D



STANDOFF

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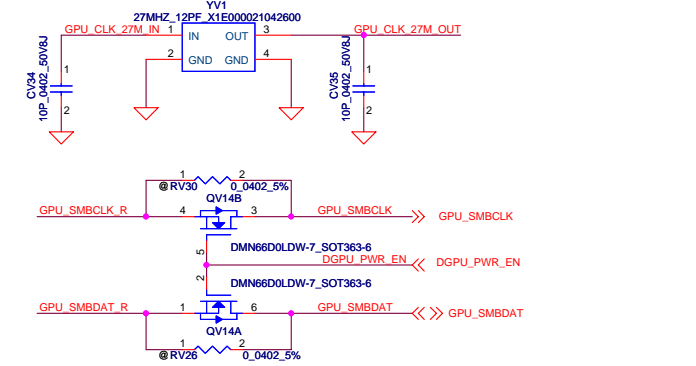
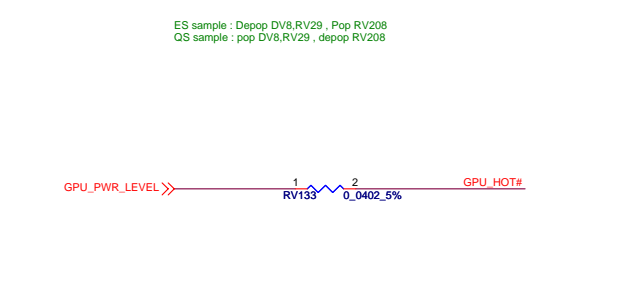
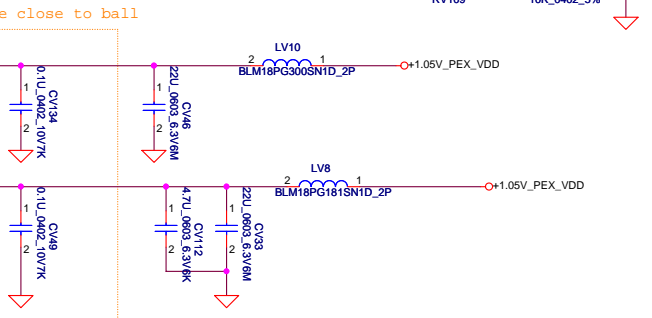
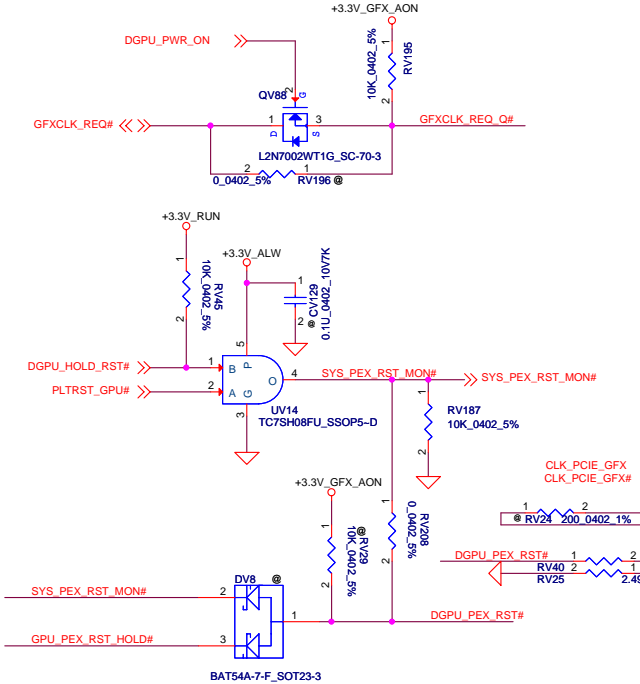
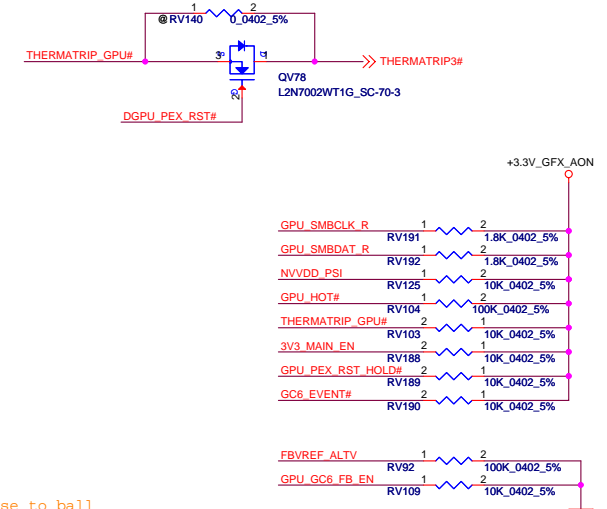
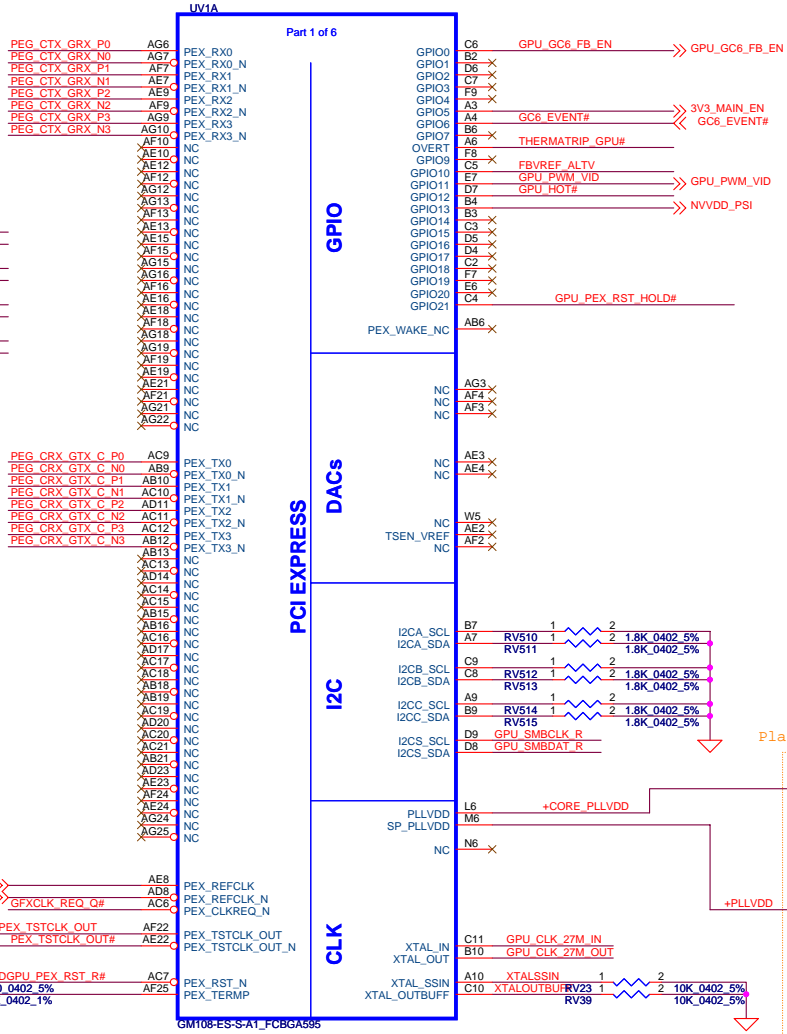
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PEG_CTX_GRX_P[0..3] >> PEG_CTX_GRX_P[0..3]
 PEG_CTX_GRX_N[0..3] >> PEG_CTX_GRX_N[0..3]
 PEG_CRX_GTX_P[0..3] << PEG_CRX_GTX_P[0..3]
 PEG_CRX_GTX_N[0..3] << PEG_CRX_GTX_N[0..3]

| | | | | | | | |
|----------------|-------|---|---|-------|-------|-------|------------------|
| PEG_CRX_GTX_P0 | CV188 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_P0 |
| PEG_CRX_GTX_N0 | CV189 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_N0 |
| PEG_CRX_GTX_P1 | CV190 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_P1 |
| PEG_CRX_GTX_N1 | CV191 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_N1 |
| PEG_CRX_GTX_P2 | CV192 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_P2 |
| PEG_CRX_GTX_N2 | CV193 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_N2 |
| PEG_CRX_GTX_P3 | CV194 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_P3 |
| PEG_CRX_GTX_N3 | CV195 | 2 | 1 | 0.22u | 0.402 | 16V7K | PEG_CRX_GTX_C_N3 |



SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

| Capacitor Type | Population |
|---------------------------------|------------|
| 0.1uF 0402 | 1 per ball |
| 4.7uF 0603 | 1 |
| 22uF 0805 | 1 |
| Bead 30 ohm (ESR=0.05 ohm) 0402 | 1 |

| | |
|---------------|------------------|
| GPU_PWR_LEVEL | |
| LOW | Low Performance |
| HIGH | High Performance |

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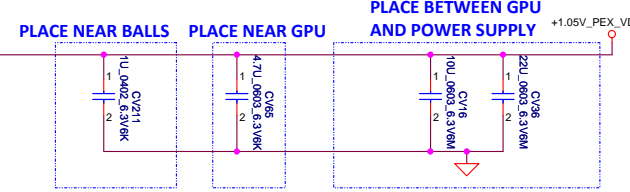
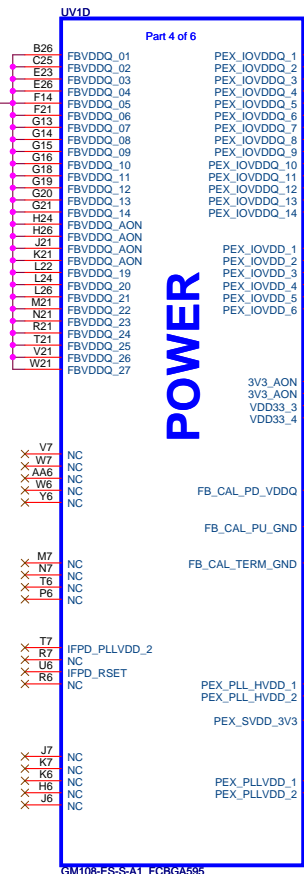
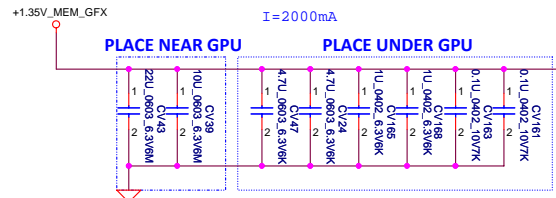
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Size: **4019RA**

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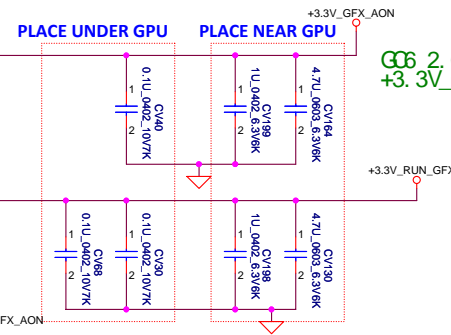
| Capacitor | Type | Population |
|------------|------|------------|
| 1uF 0402 | | 1 |
| 4.7uF 0603 | | 1 |
| 10uF 0805 | | 1 |
| 22uF 0805 | | 1 |

DDR3 CPU side FBVDD/FBVDDQ Combined Decoupling

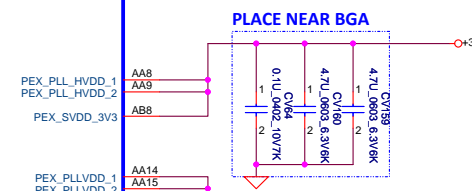
| Capacitor | Type | Population |
|------------|------|------------|
| 0.1uF 0402 | | 2 |
| 1.0uF 0603 | | 2 |
| 4.7uF 0603 | | 2 |
| 10uF 0805 | | 1 |
| 22uF 0805 | | 1 |

| Power Supply Rail | N15S-GM (V) | N15S-GM (A) | N15S-GT (A) |
|--------------------|-------------|--------------|--------------|
| GPU_Core | - | 26 | 31 |
| GPU_FBI_O | 1.5/1.35 | TBD | TBD |
| PEX_I_OVDD_Q | 1.05 | 0.765 | 0.765 |
| PEX_PLLVDD | 1.05 | 0.130 | 0.130 |
| FBA_PLL_AVDD | 1.05 | 0.062 | 0.062 |
| FBA_DLL_AVDD | 1.05 | 0.032 | 0.032 |
| PLL_VDD | 1.05 | 0.058 | 0.058 |
| SP_PLLVDD | 1.05 | 0.030 | 0.030 |
| 1.05V Total | 1.05 | 1.060 | 1.060 |
| VDD3+3V3AON | 3.3 | 0.036 | 0.036 |
| PEX_SVDD_3V3 | 3.3 | 0.167 | 0.167 |
| PEX_PLL_HVDD | 3.3 | 0.022 | 0.022 |
| 3.3V Total | 3.3 | 0.225 | 0.025 |

POWER



G06_2, 0 G10/G12 pin connect to +3.3V_GFX_AON



PEX_PLLVDD Decoupling

| Capacitor | Type | Population |
|------------|------|------------|
| 0.1uF 0402 | | 1 |
| 1uF 0603 | | 1 |
| 4.7uF 0805 | | 1 |

PEX_SVDD/PEX_PLL_HVDD Decoupling

| Capacitor | Type | Population |
|------------|------|------------|
| 0.1uF 0402 | | 1 |
| 4.7uF 0603 | | 2 |

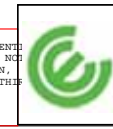
3V3_MAIN Decoupling

| Capacitor | Type | Population |
|------------|------|------------|
| 0.1uF 0402 | | 2 |
| 1uF 0603 | | 1 |
| 4.7uF 0603 | | 1 |

3V3_AON Decoupling

| Capacitor | Type | Population |
|------------|------|------------|
| 0.1uF 0402 | | 1 |
| 1uF 0603 | | 1 |
| 4.7uF 0603 | | 1 |

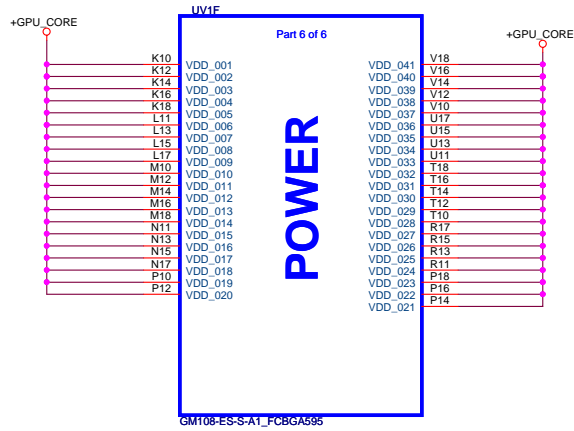
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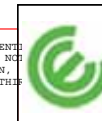
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Caps on Power Side
 1UX4 4.7UX10 under GPU
 4.7UX5 22UX1 47UX2 330UX2 near GPU



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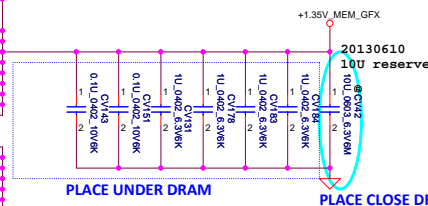
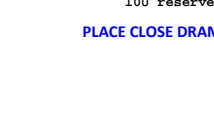
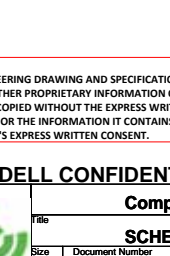
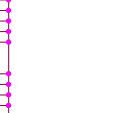
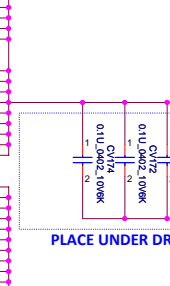
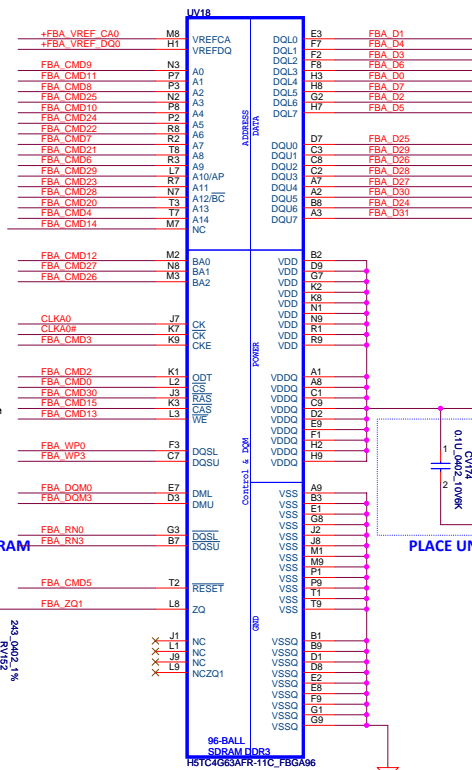
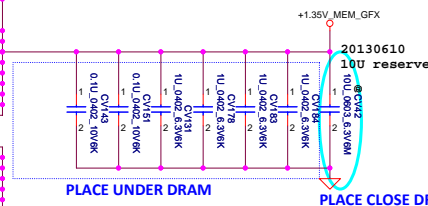
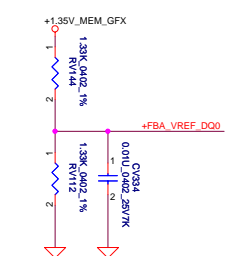
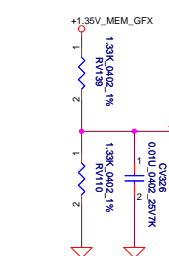
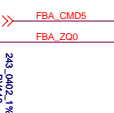
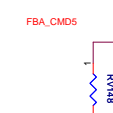
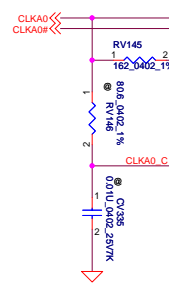
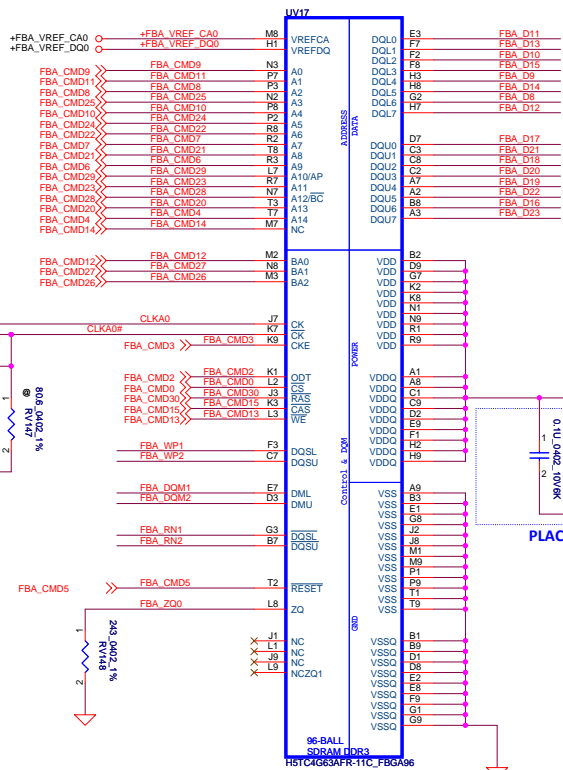
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Memory Partition A - Upper 16 bits

256x16 DDR3L

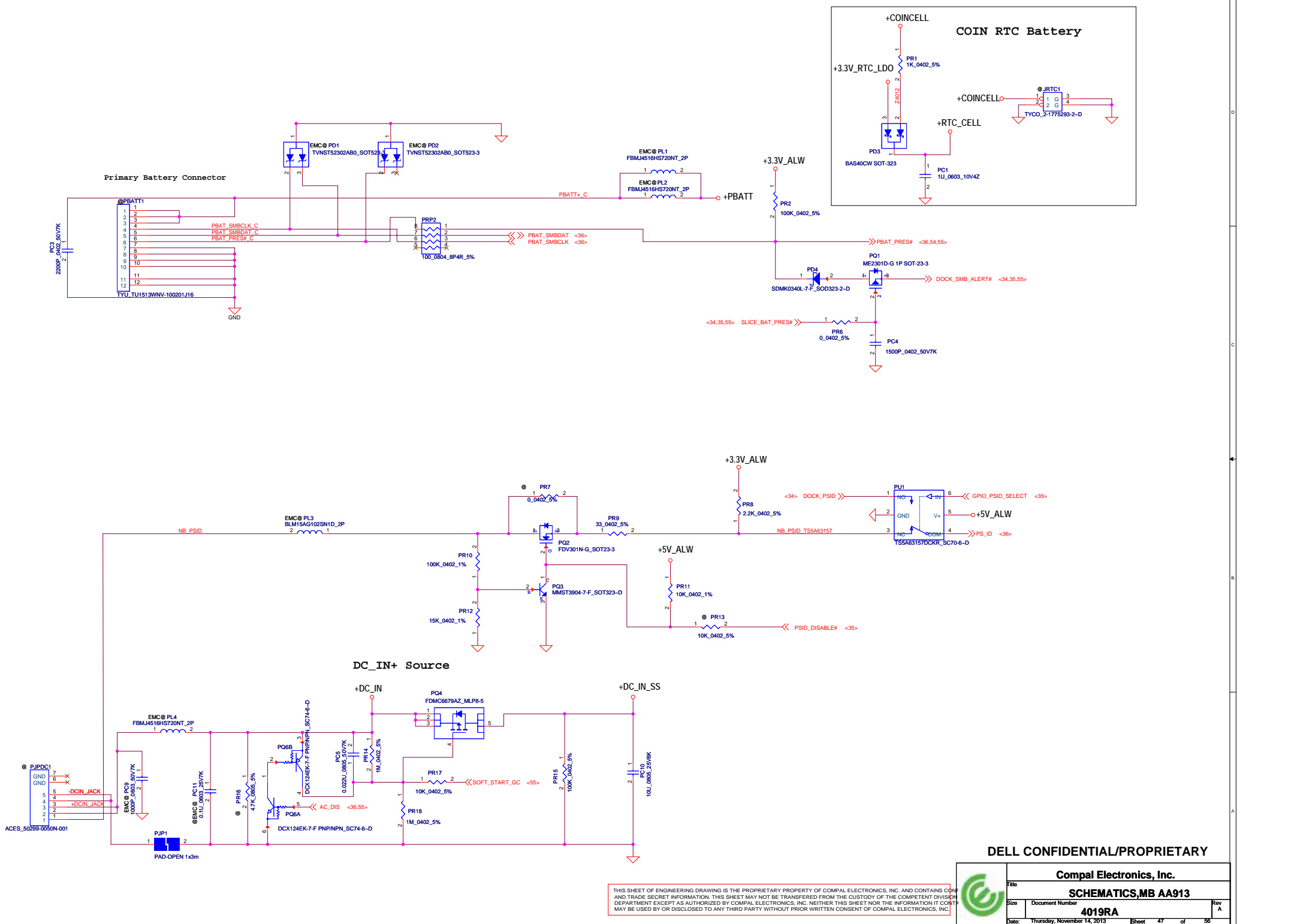


| DDR3 per Memory FBVDD/Q Decoupling | |
|------------------------------------|------------|
| FBVDD/Q Combined | |
| Capacitor Type | Population |
| 0.1uF 0402 | 2 |
| 1.0uF 0603 | 4 |
| 10uF 0805 | 0 |


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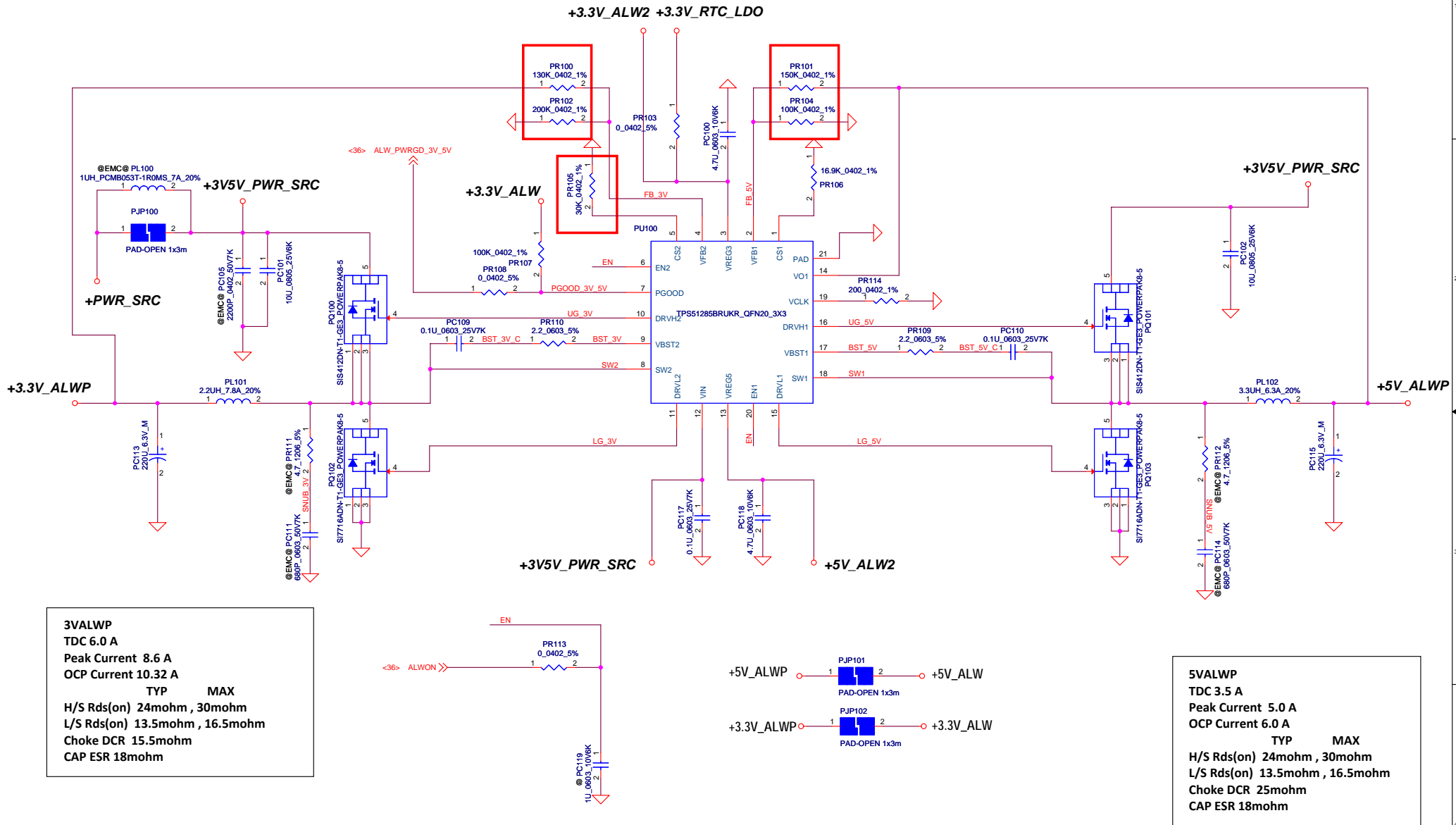
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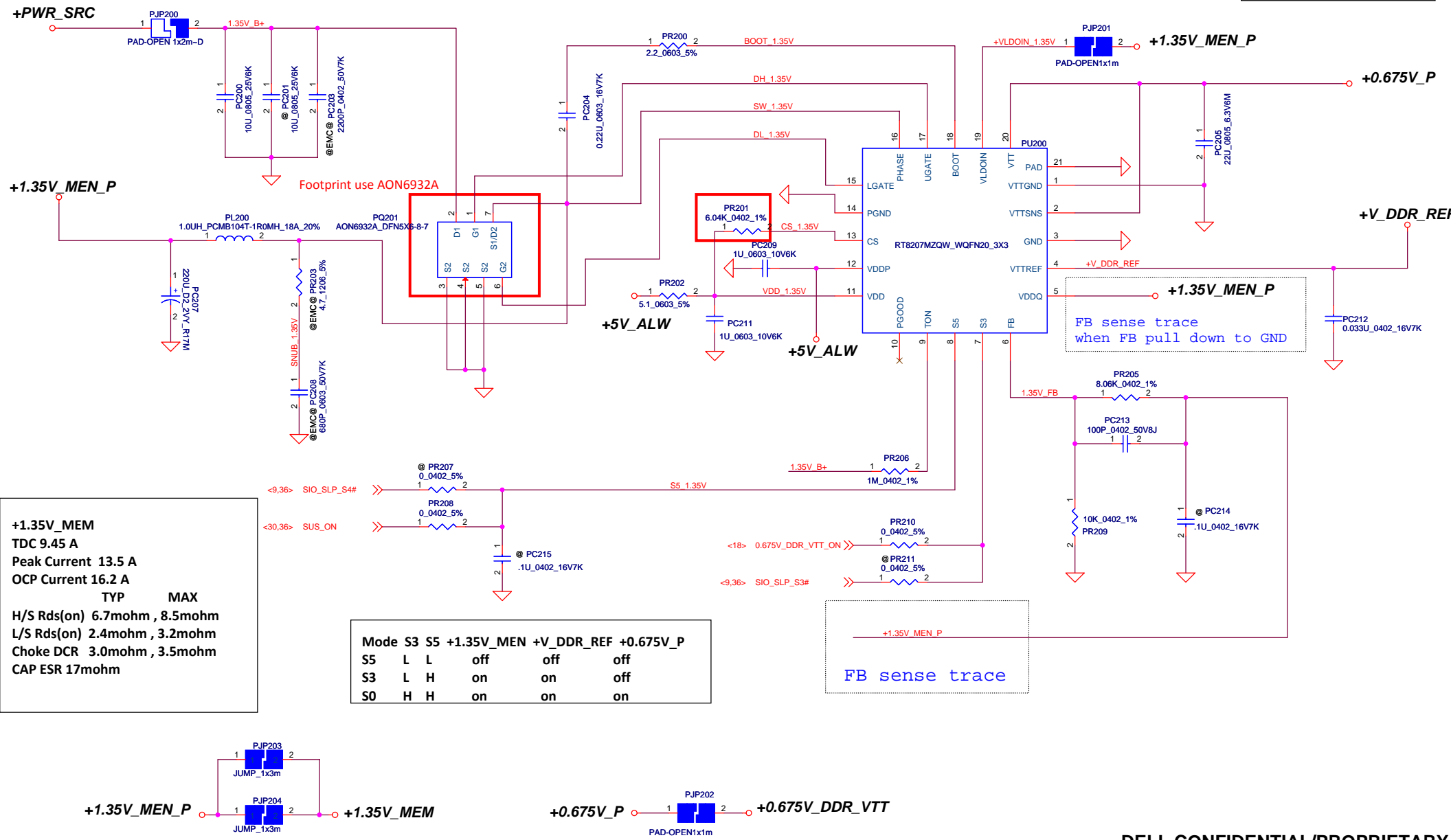


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0.675Volt +/- 5%
 TDC 0.7 A
 Peak Current 1.0 A
 OCP Current 1.2 A



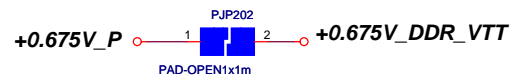
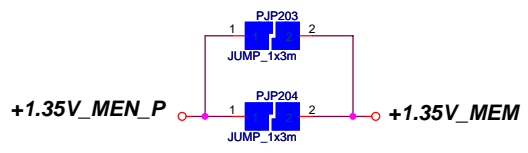
+1.35V_MEM
 TDC 9.45 A
 Peak Current 13.5 A
 OCP Current 16.2 A

| | TYP | MAX |
|-------------|-------------------|-----|
| H/S Rds(on) | 6.7mohm , 8.5mohm | |
| L/S Rds(on) | 2.4mohm , 3.2mohm | |
| Choke DCR | 3.0mohm , 3.5mohm | |
| CAP ESR | 17mohm | |

| Mode | S3 | S5 | +1.35V_MEN | +V_DDR_REF | +0.675V_P |
|------|----|----|------------|------------|-----------|
| S5 | L | L | off | off | off |
| S3 | L | H | on | on | off |
| S0 | H | H | on | on | on |

+1.35V_MEN_P
 FB sense trace

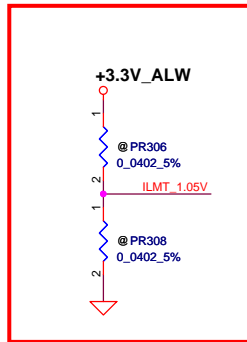
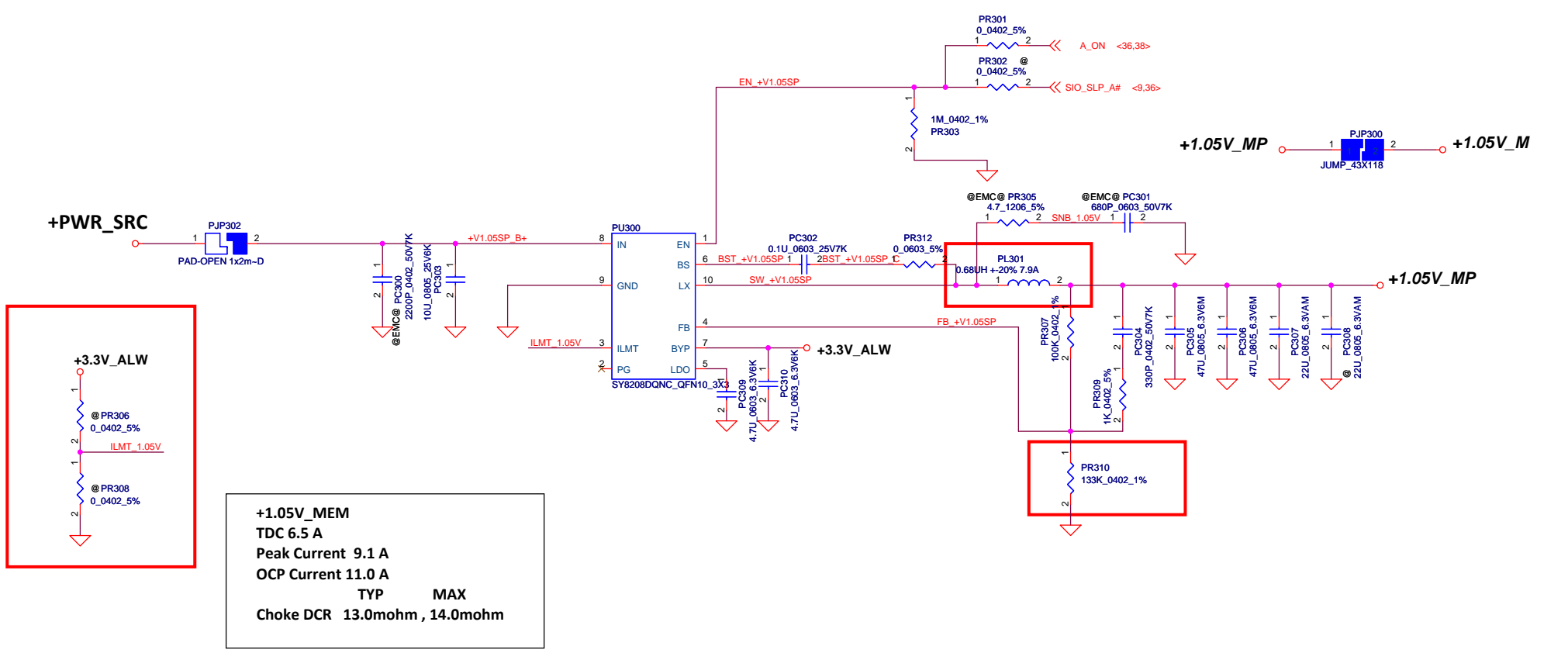
FB sense trace
 when FB pull down to GND



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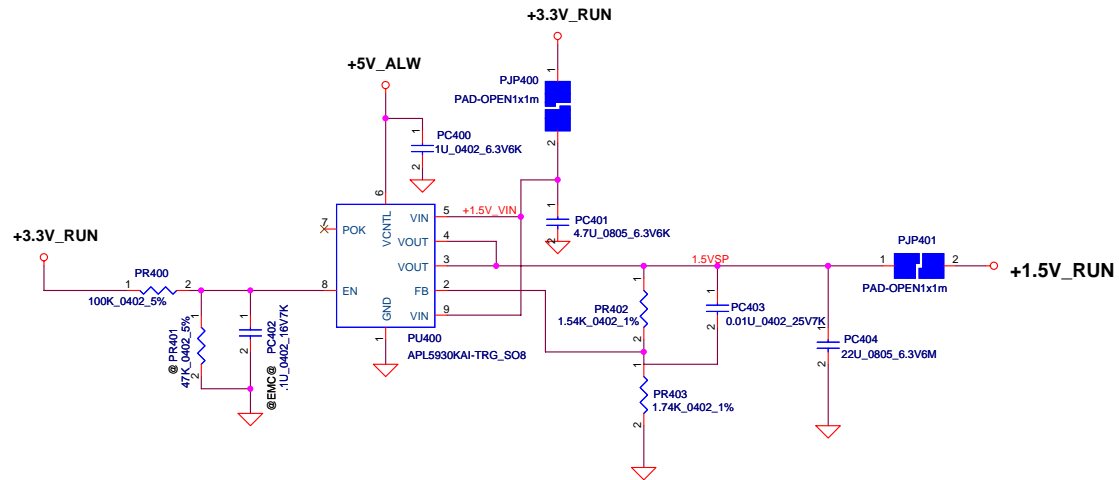


+1.05V_MEM
 TDC 6.5 A
 Peak Current 9.1 A
 OCP Current 11.0 A
 TYP MAX
 Choke DCR 13.0mohm , 14.0mohm

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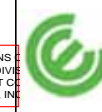
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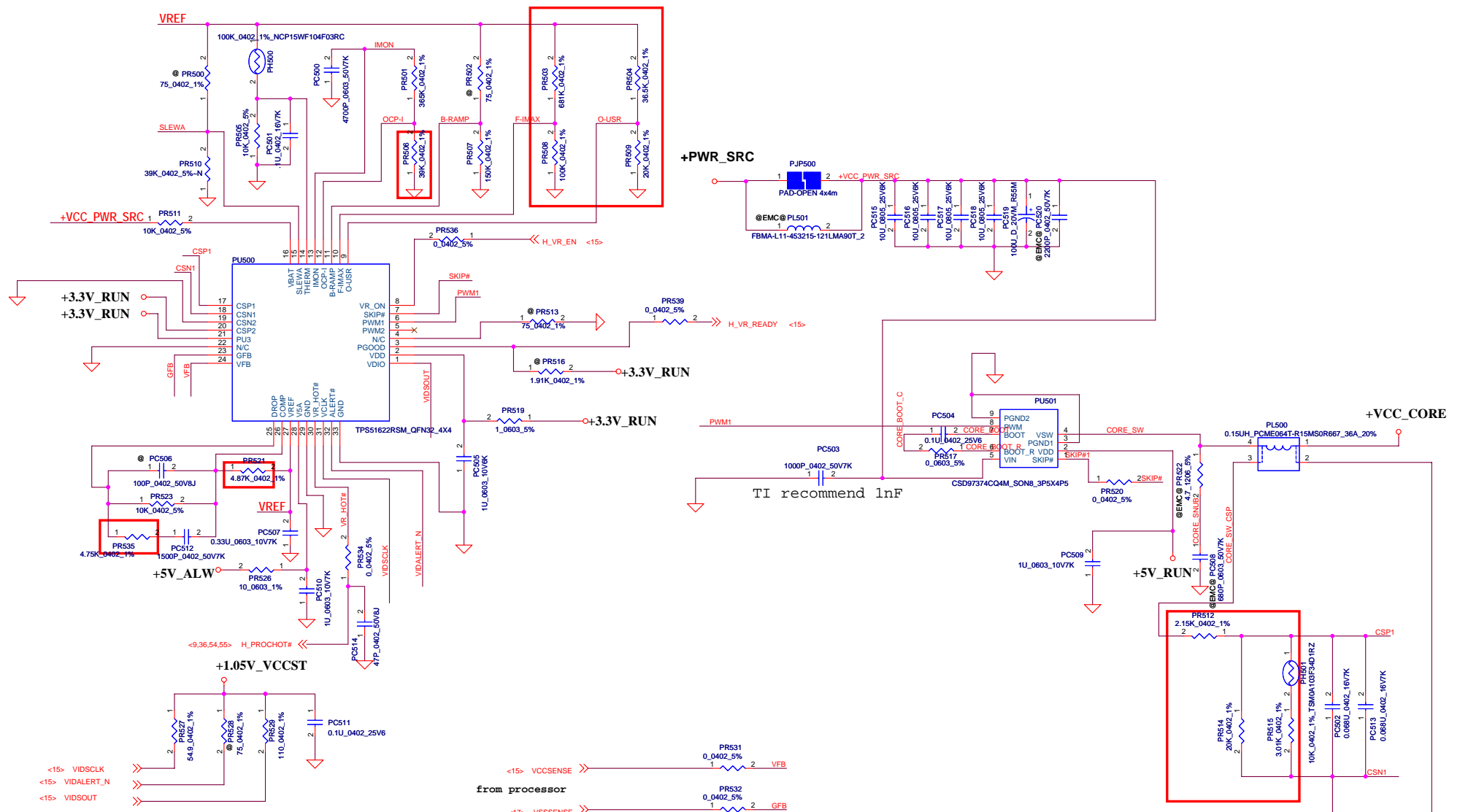
+1.5V_RUN
TDC 0.47 A
Peak Current 0.67 A

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CPU 15W
 TDC 10 A
 Peak Current 32 A
 OCP Current 38.4 A
 DC Load line -2.0 mV/A
 Icc_Dyn_VID1 27 A
 Choke DCR : 0.66m +-7% ohm
 PH500 B Value : 4250k 1%
 PH501 B Value : 3370k 1%

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Vboot=Vvref*(Rref1+Rref2+Rboot)
 Rt=Rrefadj // (Rboot+Rref2)
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} / R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

Current Limit threshold setting
 $R_{ds(on)} = (V_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10 \mu\text{A}$
 $I_{ripple} = (19 - 0.9) * 0.9 / (304.89 \text{ kHz} * 0.36 * 19) = 7.811 \text{ A}$
 OCP=54A/2=27A per phase
 $I_{valley} = 27 \text{ A} * 7.811 \text{ A} / 2 = 23.1 \text{ A}$

Different VGA Chip (different EDP-Peak Current) need select different solution

| VGA Chip | N14P-GV | N14P-GV2 | N14M-GS | N14M-LP | N14P-LP | N14P-GE | N14P-GS | N14P-GT |
|------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------|------------------------|
| OpenVReg Configurations | Config B | Config B | Config B | Config B | Config B | Config B | Config B | Config B |
| Rated TDP Power at Tj=102C | 18W | 25W | 18W | 13W | 18.9W | 25W | 25.6W | 35.5W |
| Boosted GPU Total at Tj=102C | 25W | 32W | 25W | 20W | 23W | N/A | 30W | 40W |
| EDP-Continuous at Tj=102C | 24A | 32A | 26A | 22A | 25A | 27A | 38A | 45A |
| EDP-Peak at Tj=102C | 35A | 55A | 45A | 35A | 35A | 40A | 60A | 75A |
| Istep max (Evaluation) | 15A | 27A | 25A | 20A | 14A | 12A | 31.5A | 35A |
| OCP Setting Current | 42A | 66A | 54A | 42A | 42A | 48A | 72A | 90A |
| Rocset | 8.96K | 12.45K | 10.7K | 8.96K | 8.96K | 9.83K | 8.3K | 9.93K |
| Recommendation | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H2L | 2phase 1H2L |
| Polymer Cap (330uF) | 6mohm * 2 | 9mohm * 3 | 9mohm * 3 | 6mohm * 2 | 6mohm * 2 | 6mohm * 2 | 6mohm * 3 (L=0.22uH) | 4.5mohm * 3 (L=0.15uH) |
| Or OSCON (390uF) | 10mohm * 3 | 10mohm * 3 | 10mohm * 3 | 10mohm * 3 | 10mohm * 3 | 10mohm * 3 | NULL | NULL |

Module model information:
 RT8813A_V1A for IC module
 RT8813A_V1B for SW module

PWM-VID Spec and component Values

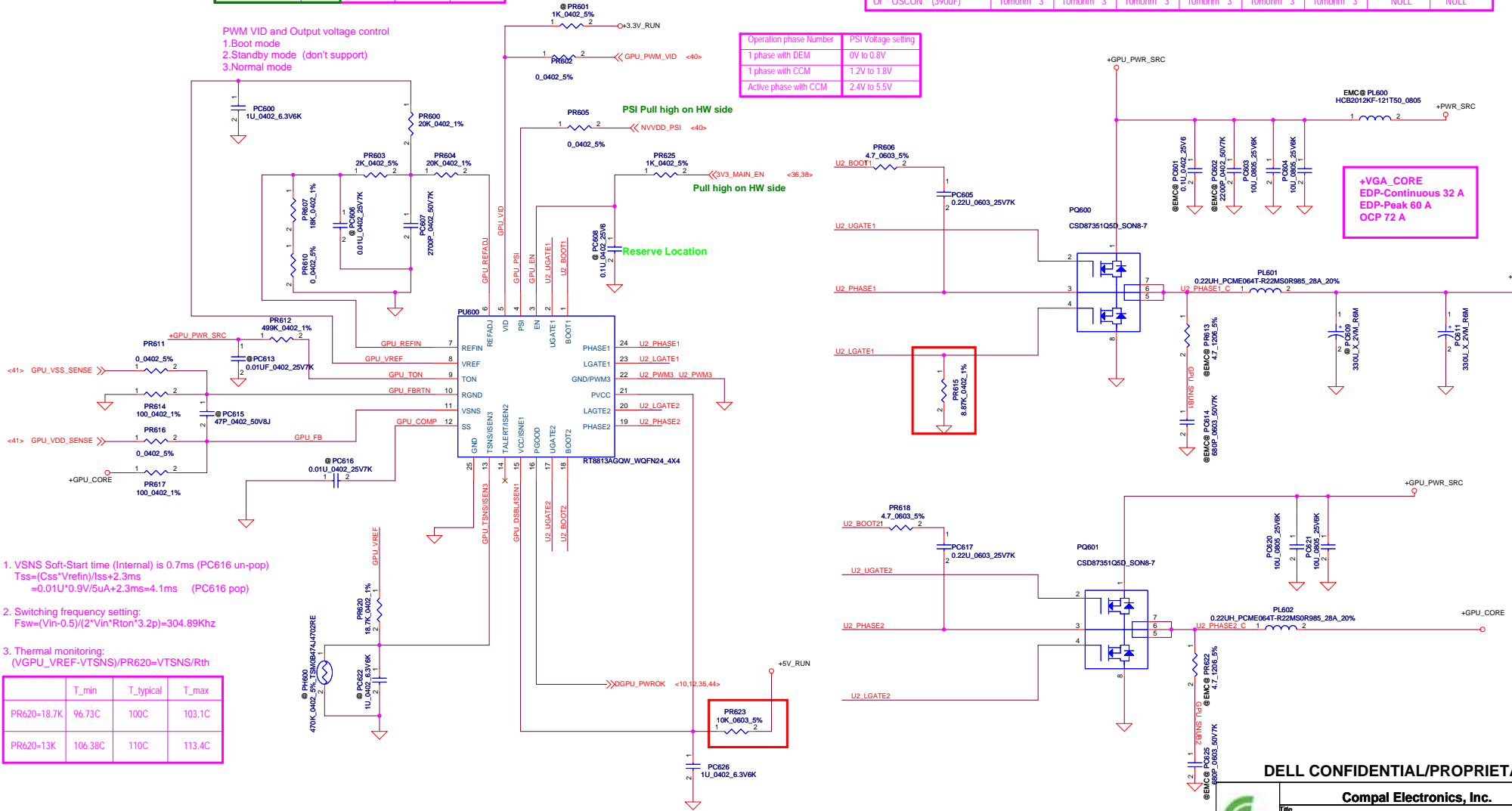
| PWM-VID Spec | Config A | Config B | Config C |
|--------------------|-----------|----------|----------|
| Vmin | 0.6V | 0.6V | 0.65V |
| Vmax | 1.2V | 1.2V | 1.15V |
| Vboot | 0.875V | 0.9V | 0.9V |
| Voltage step | 6.25mV | 6.25mV | 25mV |
| N of Voltage level | 96 | 96 | 20 |
| Rrefadj | PP9 39K | 20K | 39K |
| Rref1 | PR5 39K | 20K | 30K |
| Rboot | PR8 1.5K | 2K | 3K |
| Rref2=PR10+PR12 | PR10 30K | 18K | 24K |
| | PR12 1.5K | 0 | 3K |
| C | PC8 1.5nf | 2.7nf | 1.8nf |

H-side MOS:TPCA8065 Rds(on): 11.7mohm@Vgs=10V 9.4mohm@Vgs=4.5V Id:16A@Ta=25 degC
 L-side MOS:TPCA8057 Rds(on): 2.0mohm@Vgs=10V 2.6-3.2mohm@Vgs=4.5V Id:42A@Ta=25 degC

Choke: 0.36uH (Size:10*10*4)
 Rdc=1.1mohm +-5%
 Heat Rating Current=30A
 Saturation Current=50A

C=3*330uF (9mohm)=990uF
 Vrripple=ripple*ESR(min)=7.811A*3mohm=23.4mV

PWM VID and Output voltage control
 1.Boot mode
 2.Standby mode (don't support)
 3.Normal mode



- VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)
 $T_{ss} = (C_{ss} * V_{vrefin}) / I_{ss} + 2.3 \text{ ms}$
 $= 0.01 \mu\text{F} * 0.9 \text{ V} / 5 \mu\text{A} + 2.3 \text{ ms} = 4.1 \text{ ms}$ (PC616 pop)
- Switching frequency setting:
 $f_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2 \text{ p}) = 304.89 \text{ kHz}$
- Thermal monitoring:
 $(V_{GPU_VREF} - V_{TSNS}) / PR620 = V_{TSNS} / R_{th}$

| | T_min | T_typical | T_max |
|-------------|---------|-----------|--------|
| PR620=18.7K | 96.73C | 100C | 103.1C |
| PR620=13K | 106.38C | 110C | 113.4C |

| Operation phase Number | PSI Voltage setting |
|------------------------|---------------------|
| 1 phase with DEM | 0V to 0.8V |
| 1 phase with CCM | 1.2V to 1.8V |
| Active phase with CCM | 2.4V to 5.5V |

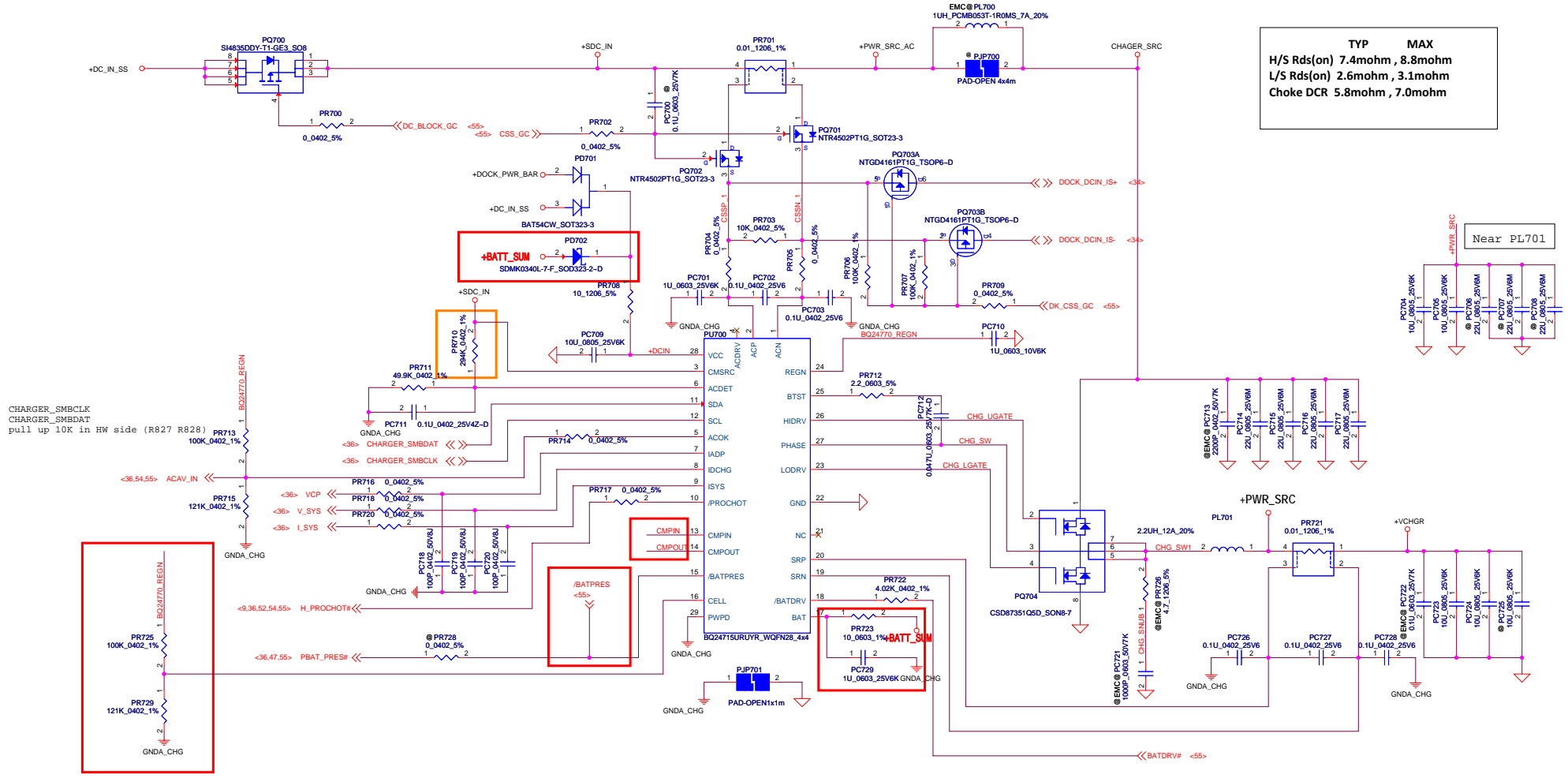
+VGA_CORE
 EDP-Continuous 32 A
 EDP-Peak 60 A
 OCP 72 A

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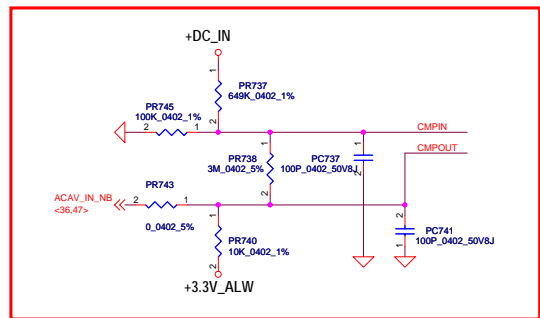
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TYP MAX
H/S Rds(on) 7.4mohm , 8.8mohm
L/S Rds(on) 2.6mohm , 3.1mohm
Choke DCR 5.8mohm , 7.0mohm



CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side (R827 R828)

Near PL701

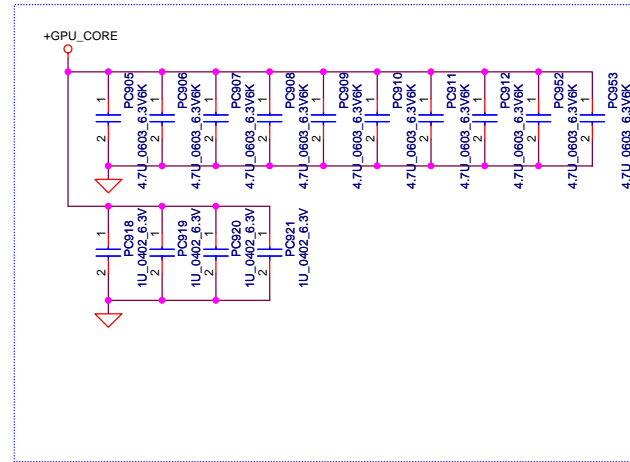
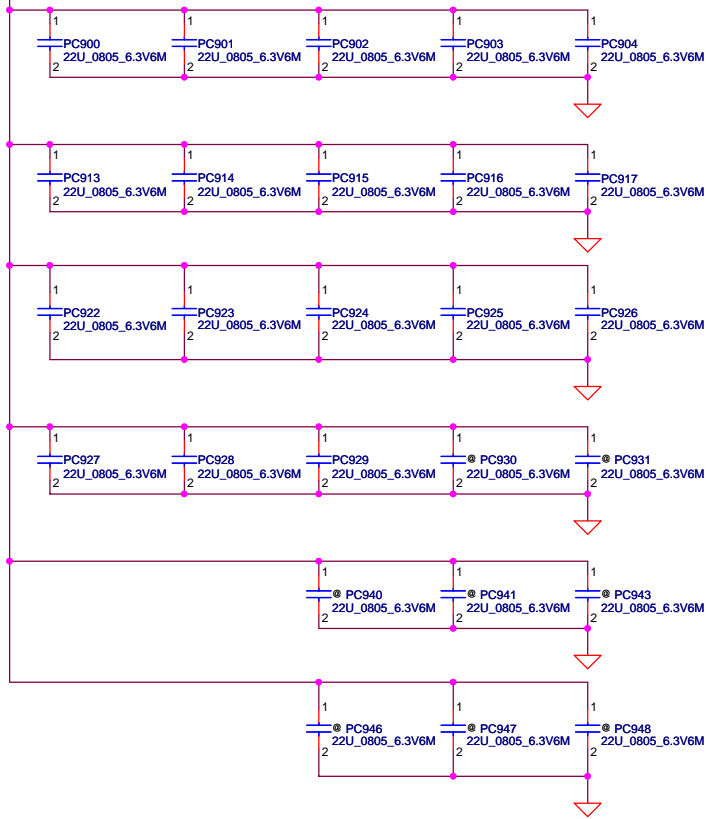


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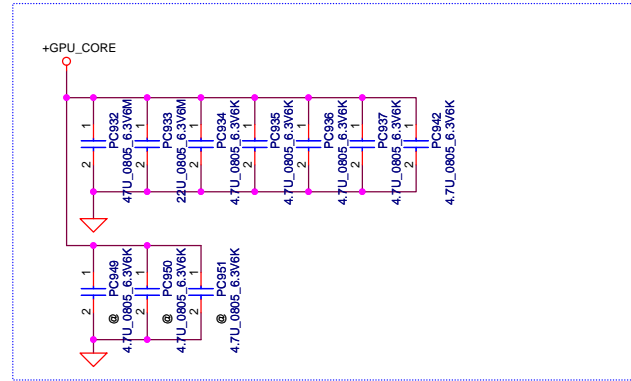
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+VCC_CORE




nVidia GB4-64 package
Under GPU
4.7uF 0603 * 10
1uF 0402 * 4



nVidia GB4-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

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