

Compal Confidential

Model Name : Z5WAH

File Name : LA-B162P

Compal Confidential

EA50_HB M/B Schematics Document

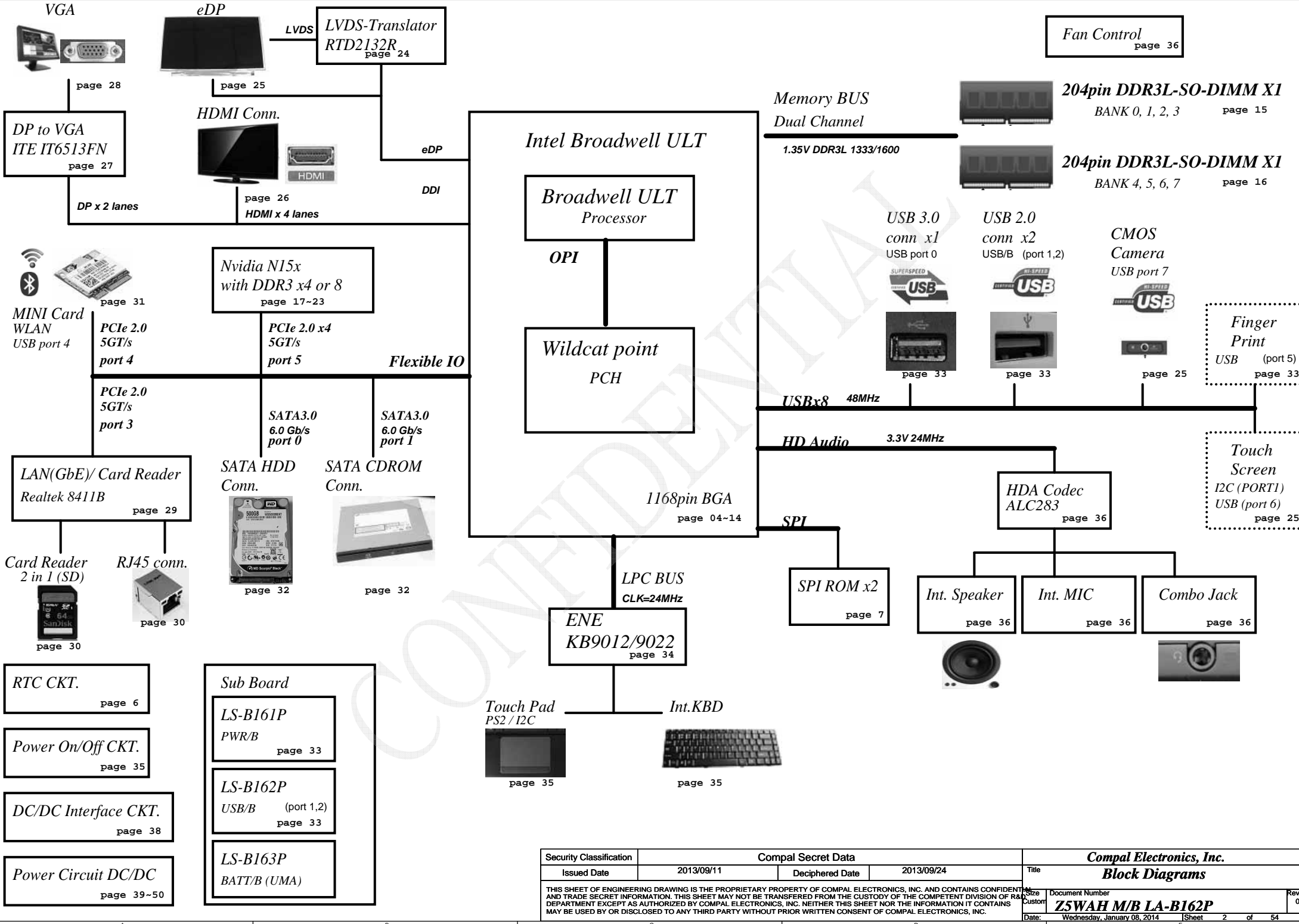
Intel Broadwell ULT (Broadwell + Wildcat point)

Nvidia N15S-GT / N15V-GM / N15V-GL

2013-12-24

REV: 0.2

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.423 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X

EC SM Bus2 address

Device	Address
On Board Thermal Sensor	0100 110x
VGA Internal Thermal Sensor	0100 000x
G Sensor	0011 000x

PCH SM Bus address

Device	Address
ChannelA DIMM0	1010 0000 JDIMM1
ChannelB DIMM1	1010 0010 JDIMM2

USB Port Table

USB 2.0	Port	3 External USB Port
EHC11	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	
	4	Mini Card (WLAN+BT)
	5	Touch Screen
	6	Camera
7	Finger Print	
USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
3		

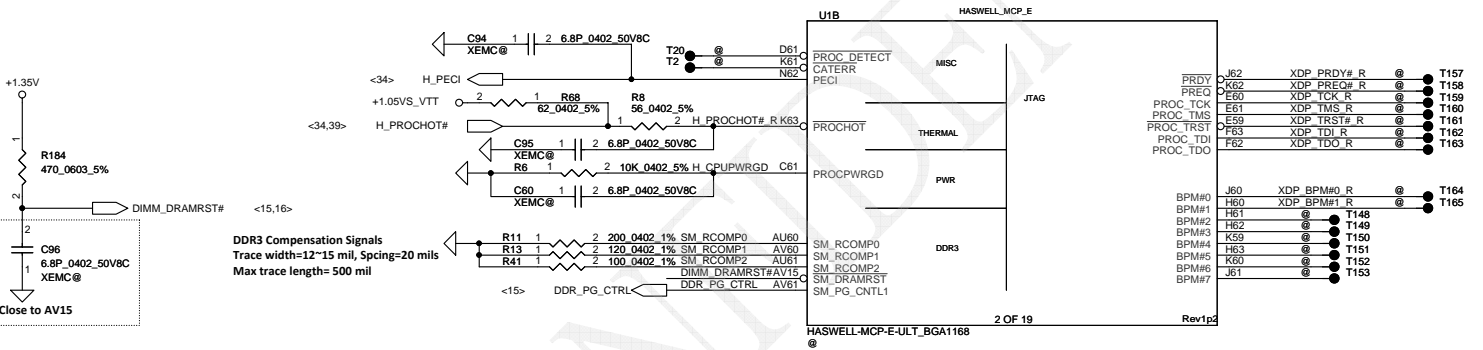
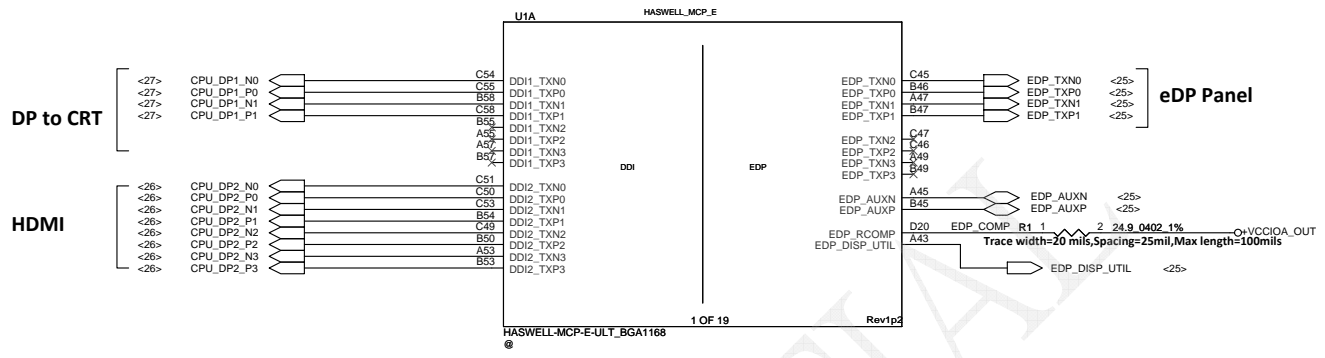
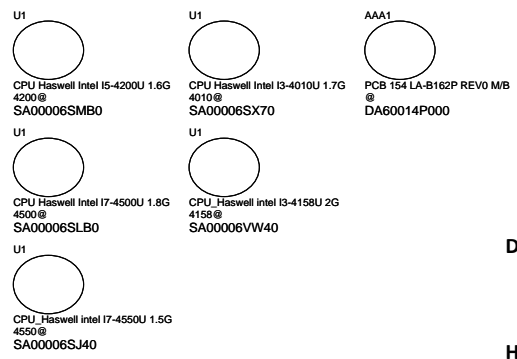
BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EC 9022	9022@
EC 9012	9012@
UMA Component	UMA@
GPU	VGA@
VRAM x 8pcs	128@
EDP panel	EDP@
eDP to LVDS	LVDS@
EMC Component	EMC@
EMC Reserve	XEMC@
On Board HDD	HDD@
G-Sensor	BA@
TPM Module	BA@
Redriver HDD	BA@
Touch Screen	TS@
DGPU_IDEN	VGL@, VGME@, SGT@
CPU_IDEN	HW@, BW@
GC6 2.0	GC6@
non GC6	NGC6@
One DMIC	EA50@
Two DMIC	EA54@
VRAM Selection	X76@

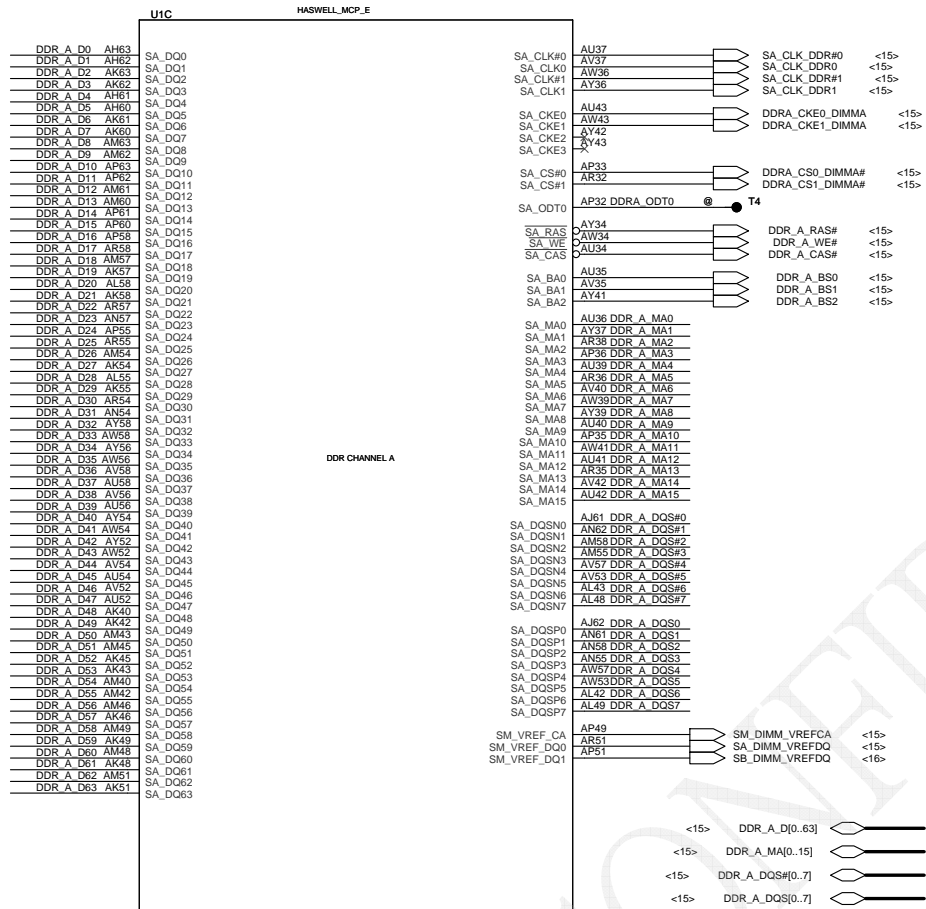
BOARD ID Table

Board ID	PCB Revision
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2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

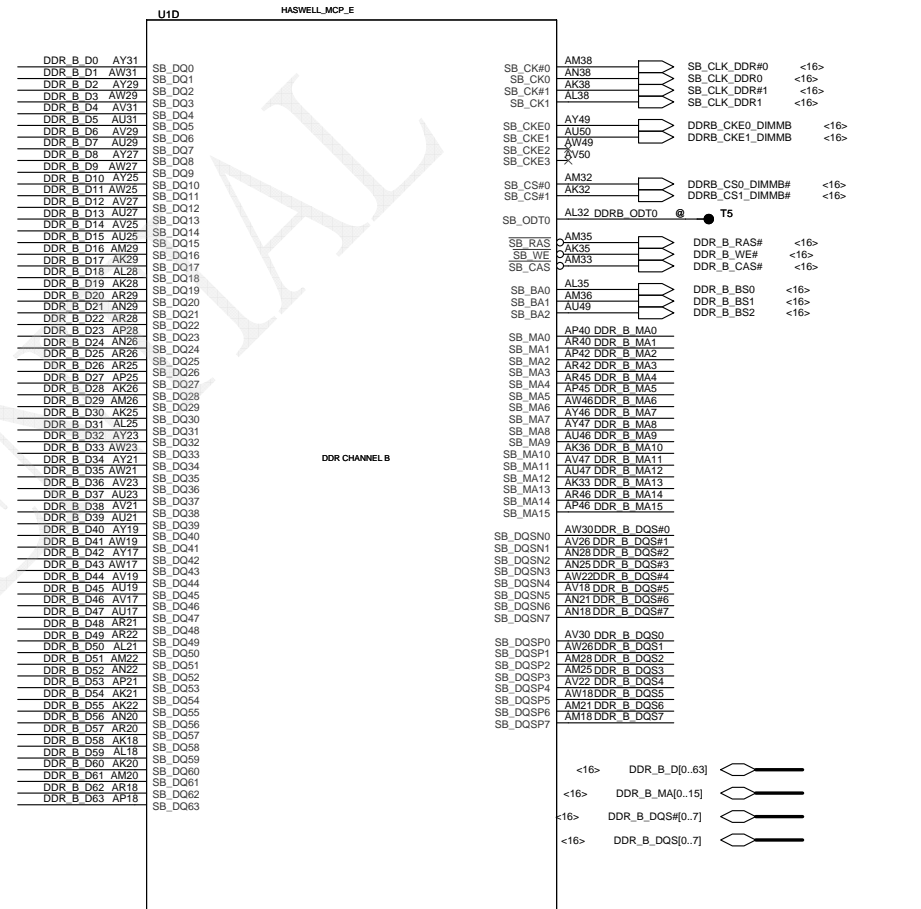
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Issued Date	2013/09/11	Deciphered Date	2013/09/24	BDW MCP(1/11) DDI,MSIC,XDP
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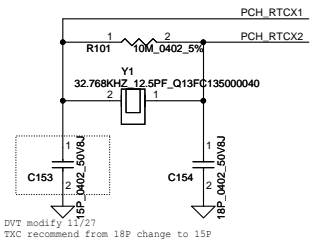


HASWELL-MCP-E-ULT_BGA1168

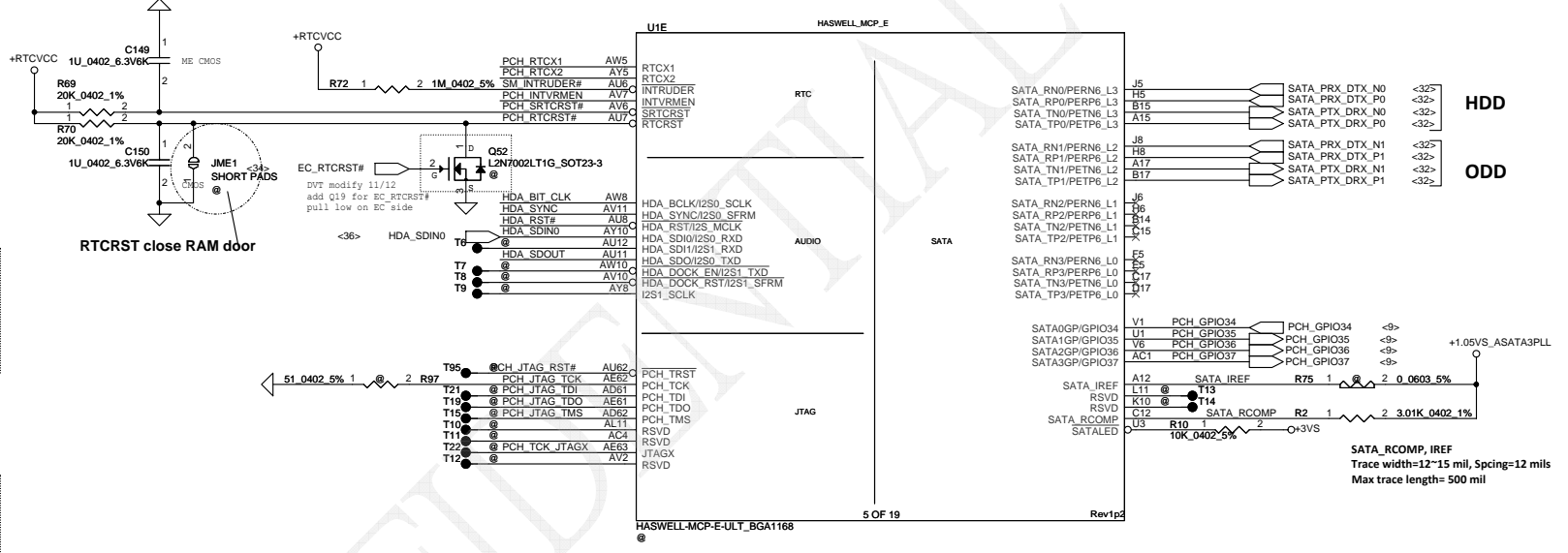
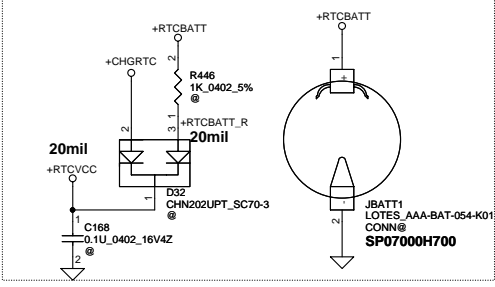
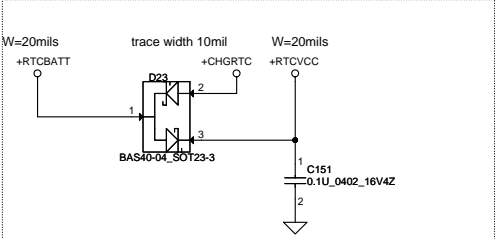
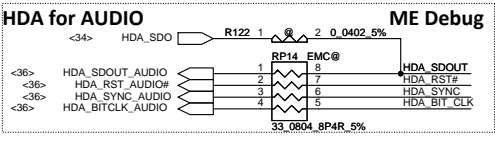
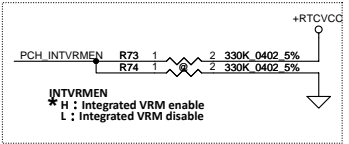


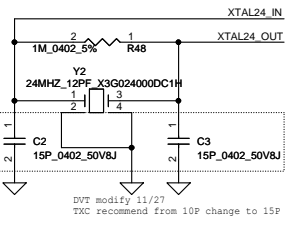
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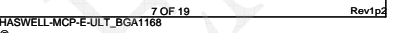
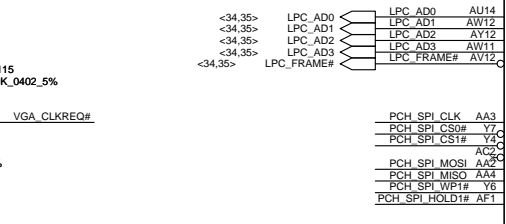
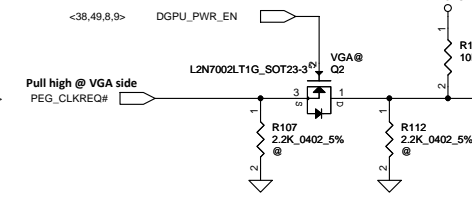
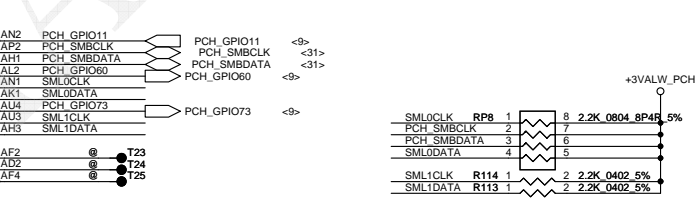
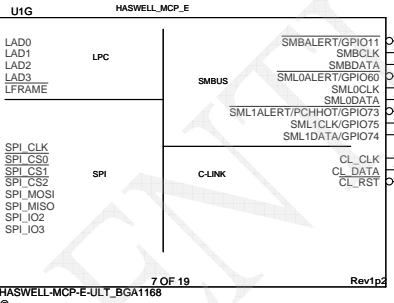
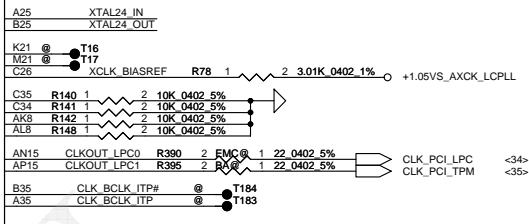
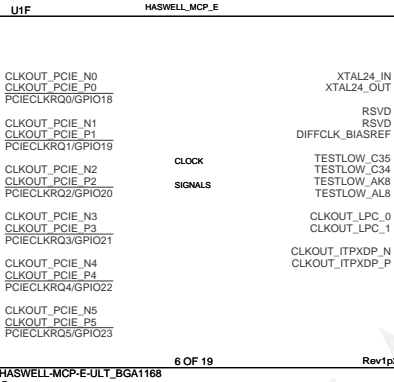
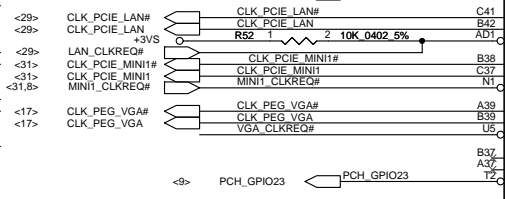


DVT modify 11/27
TKC recommend from 18P change to 15P

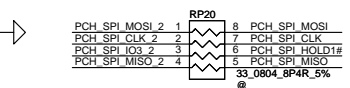
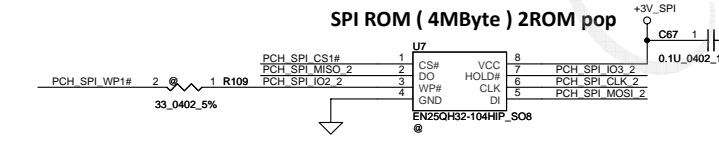
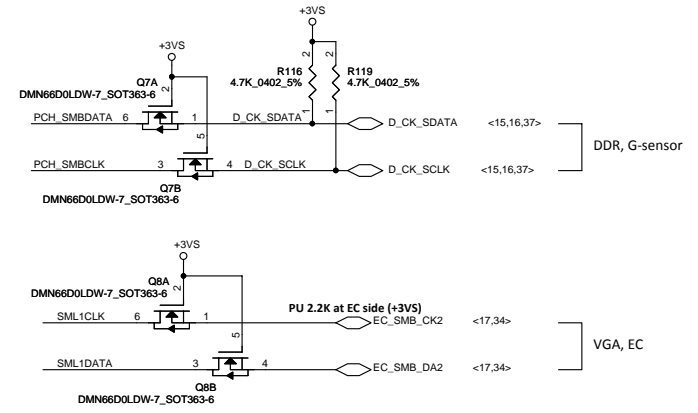
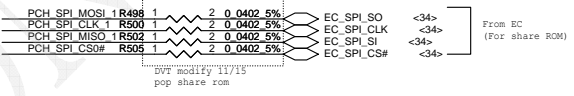
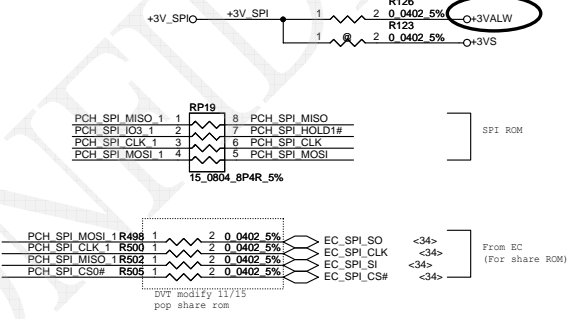
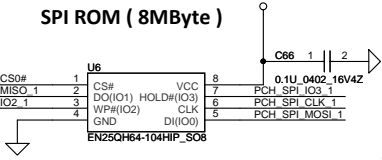
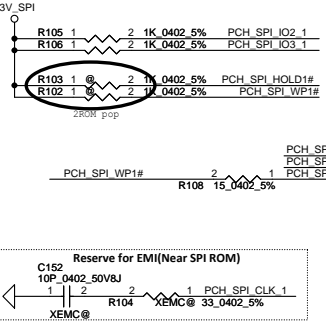




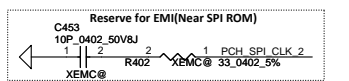
PCIe LAN
WLAN
VGA



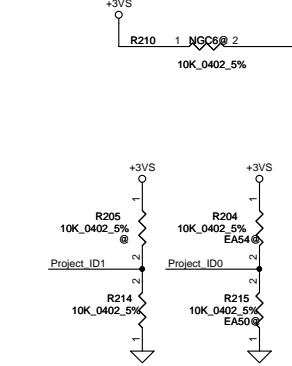
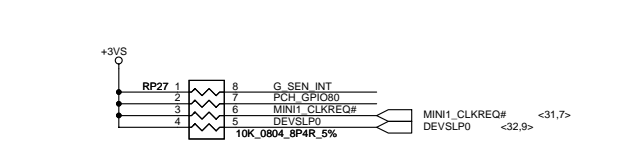
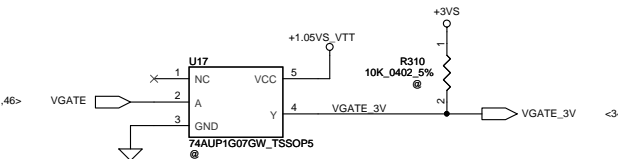
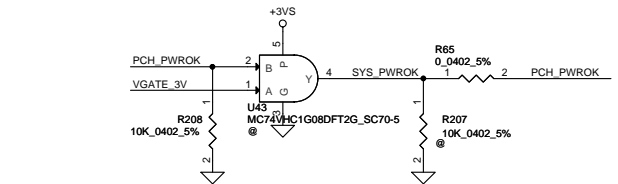
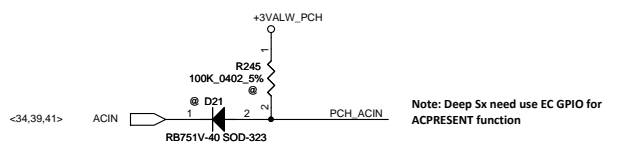
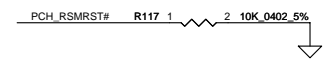
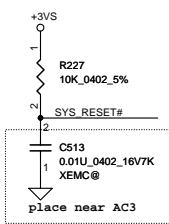
for Share EC ROM, +3VS change to +3VALW



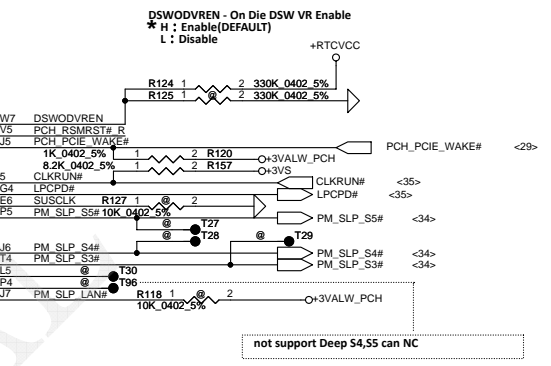
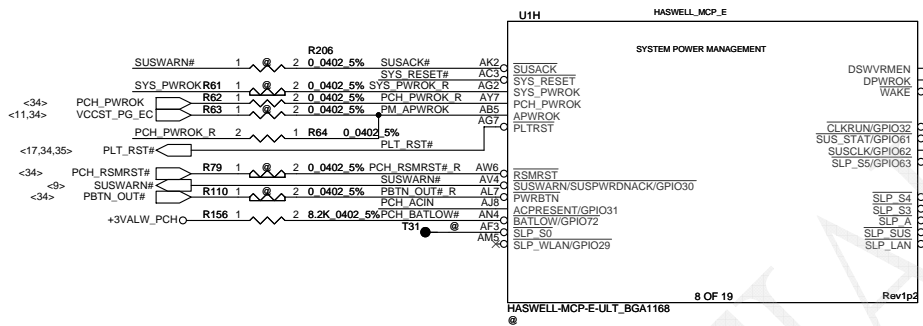
2ROM is SPI ROM 2M + 4M Byte
2ROM POP
U6 - EN25QH16-104HIP_S08 (SA00004UG00)
RP19 - 33_0804_8P4R_5% (SD309330A80)
R108 - 33_0402_5% (SD028330A80)



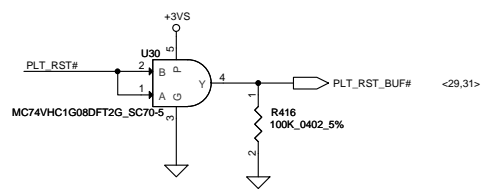
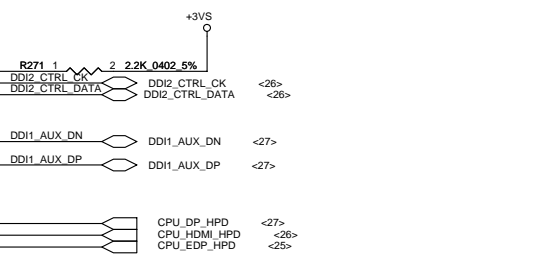
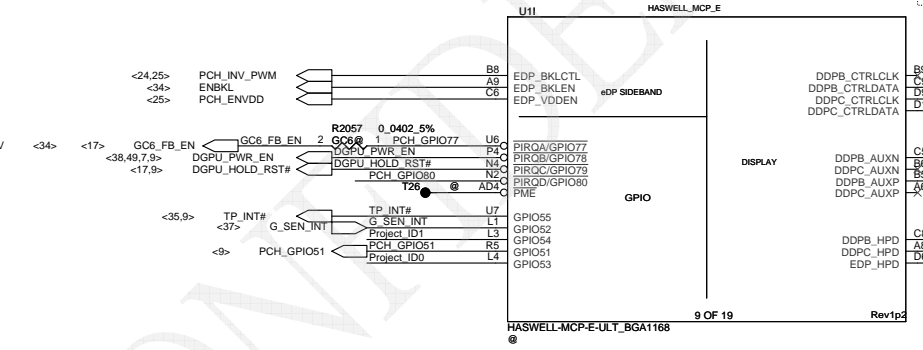
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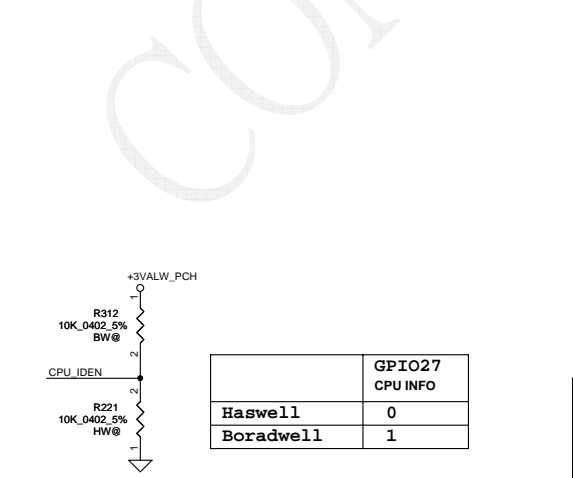
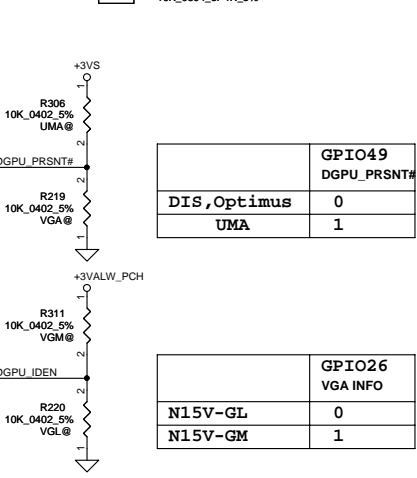
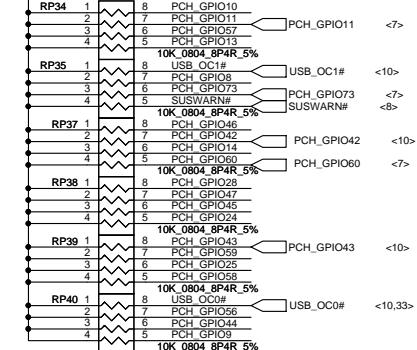
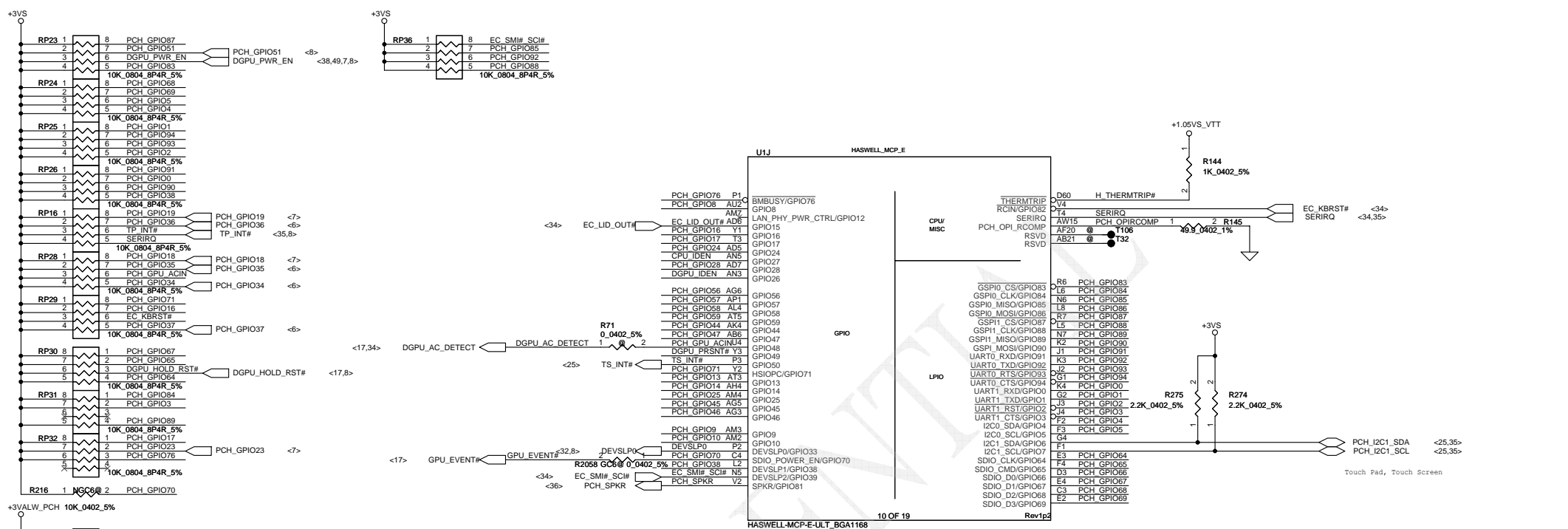


Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
*Z5WAH	0	0
Z5W1H	0	1
Z5WBH	1	0
Reserved	1	1



DDPB_CTRLDATA: Port B Detected
 DDPB_CTRLDATA: Port C Detected
 * 1: Port B or C is detected
 0: Port B or C is not detected
 (Have internal PD)

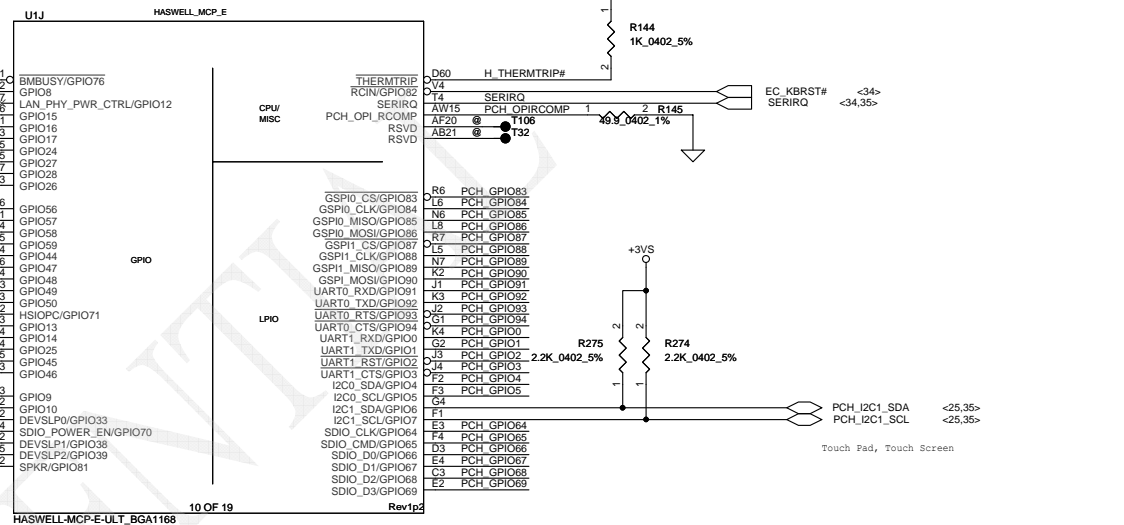




	GPIO49 DGPU_PRSNTE#
DIS,Optimus	0
UMA	1

	GPIO26 VGA INFO
N15V-GL	0
N15V-GM	1

	GPIO27 CPU INFO
Haswell	0
Boradwell	1



GPIO15 : TLS Confidentiality

1: Intel ME TLS with confidentiality
 * 0: Intel ME TLS with no confidentiality (Have internal PD)

SPKR / GPIO81 : NO REBOOT

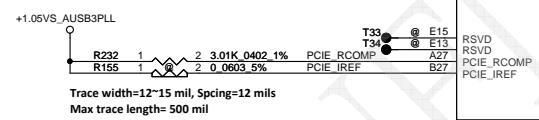
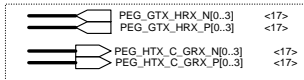
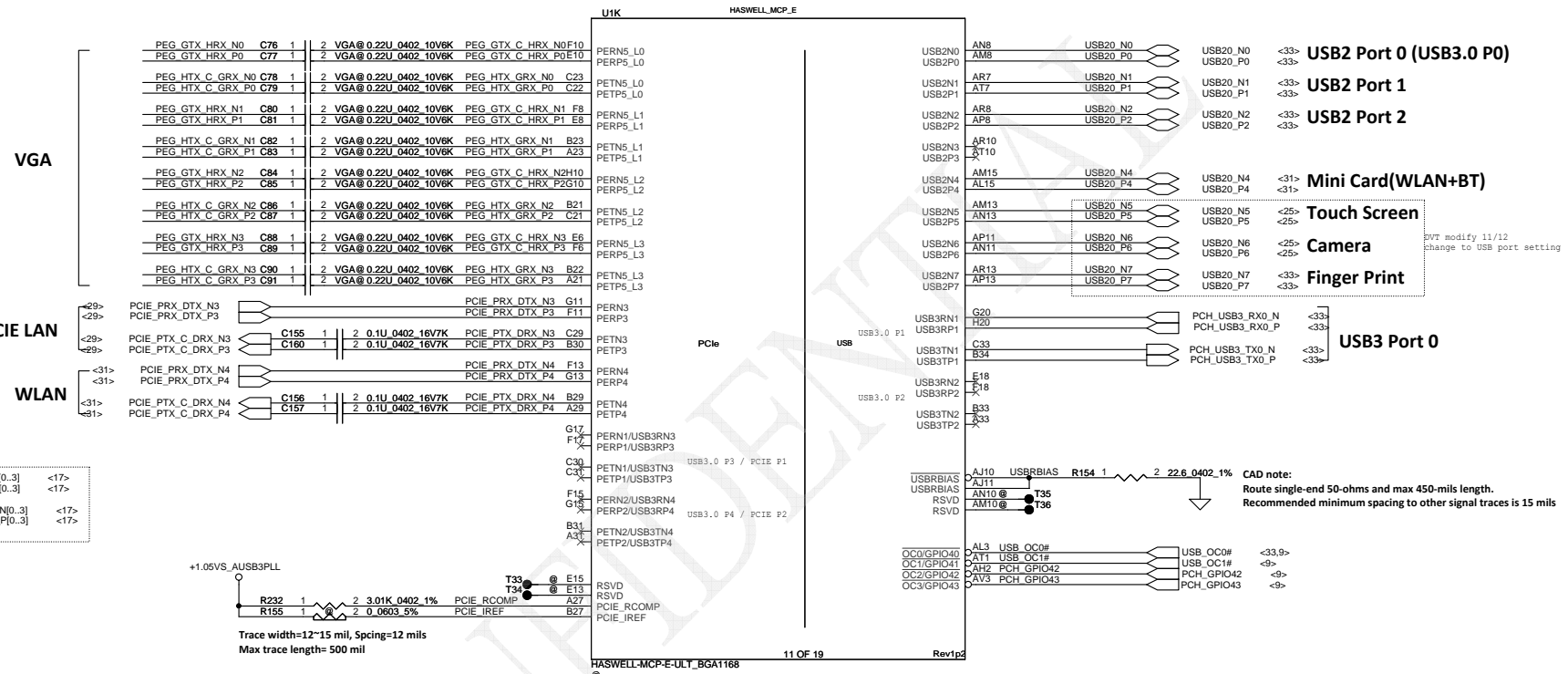
1: ENABLED
 * 0: DISABLED (Have internal PD)

GSP10_MOSI / GPIO86 : Boot BIOS Strap

1: ENABLED
 * 0: SPI ROM (Have internal PD)

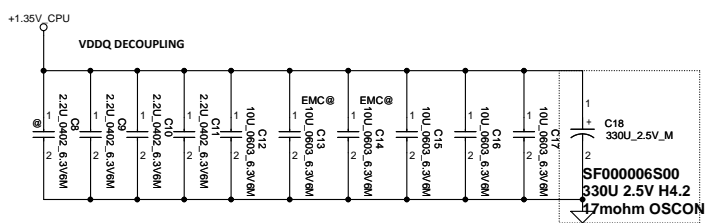
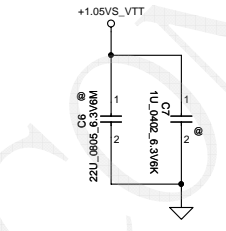
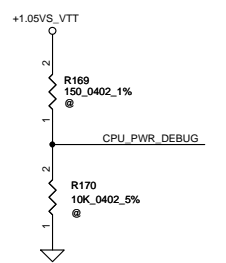
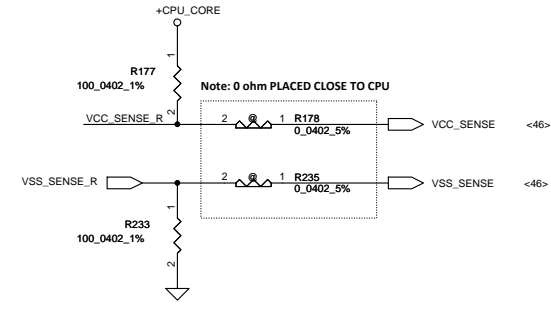
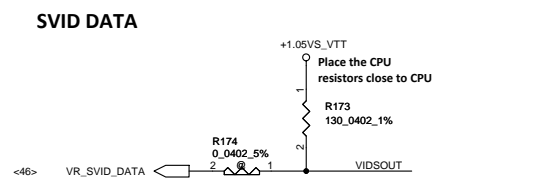
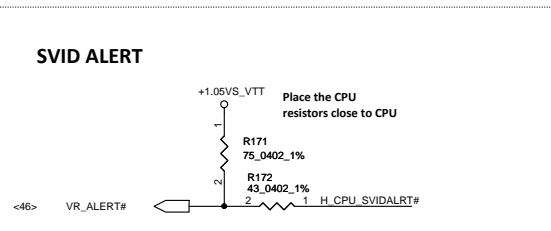
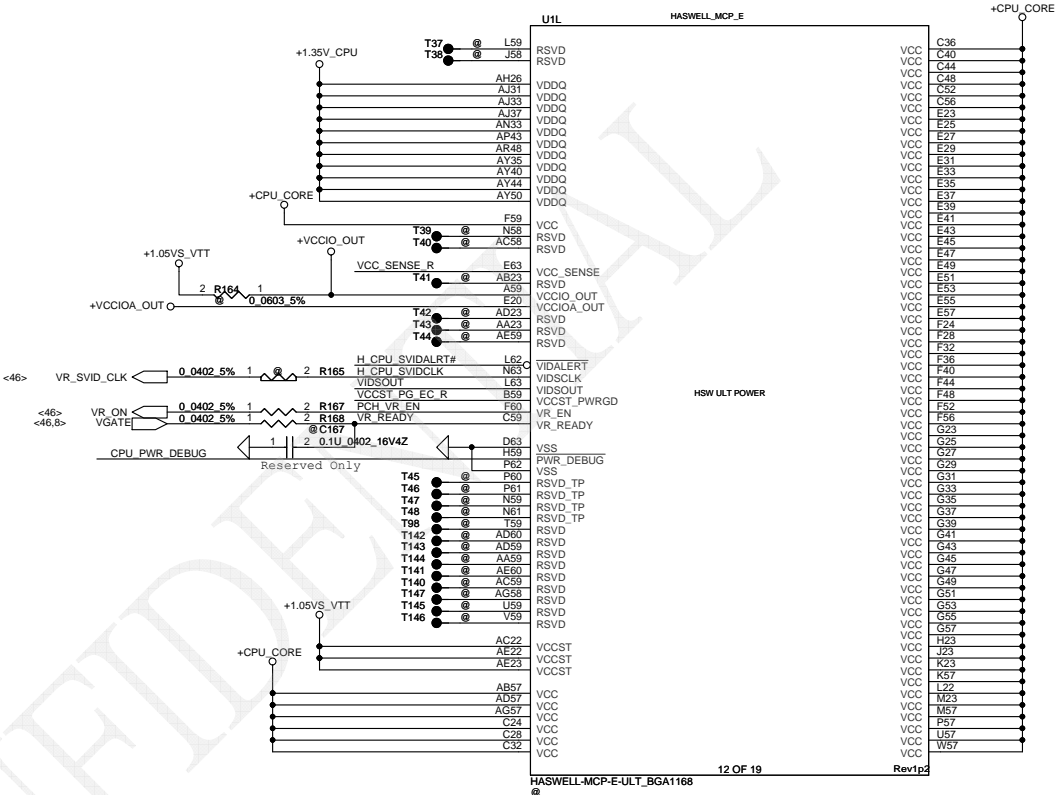
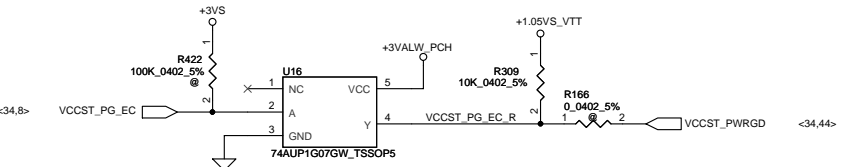
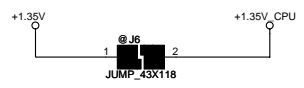
SDIO_D0 / GPIO66 : Top-Block Swap Override

1: ENABLED
 * 0: DISABLED (Have internal PD)



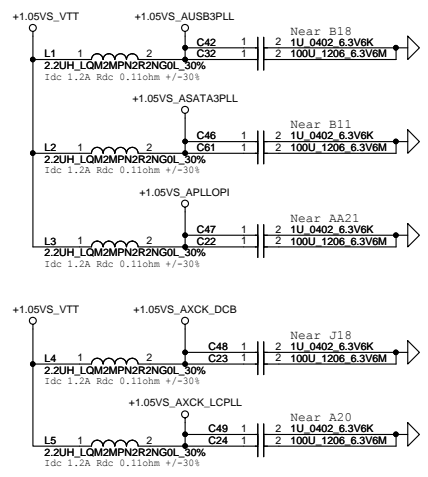
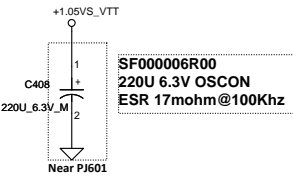
Trace width=12-15 mil, Spacing=12 mils
Max trace length= 500 mil

Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	BDW MCP(7/11) PCIE, USB		
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Date:	Wednesday, January 08, 2014	Sheet	10	of	54	Rev 0.3

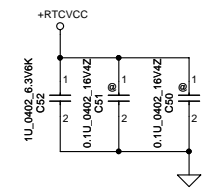
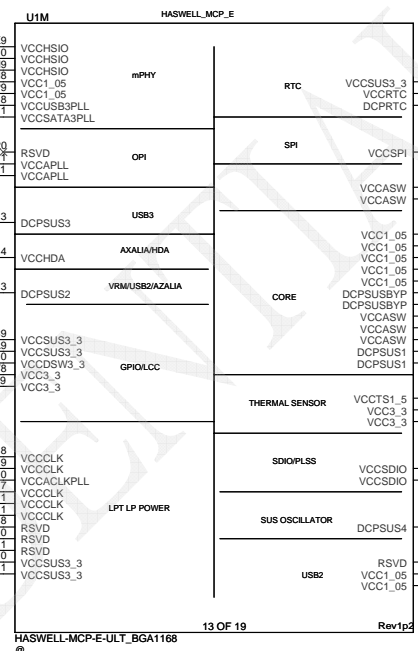
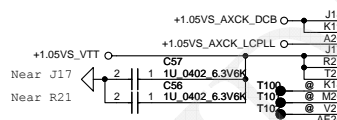
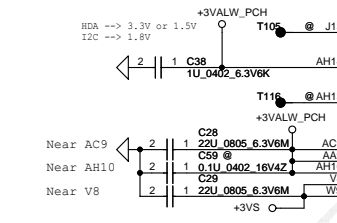
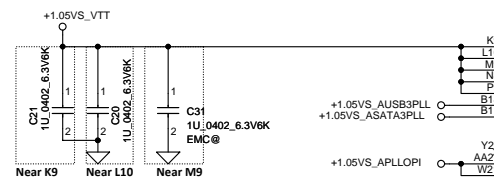
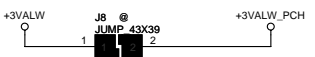


+1.35V : 470UF/2V/7343 * 2
 10UF/6.3V/0603 * 6
 2.2UF/6.3V/0402 * 4

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Date:	Wednesday, January 08, 2014	Sheet	11	of 54

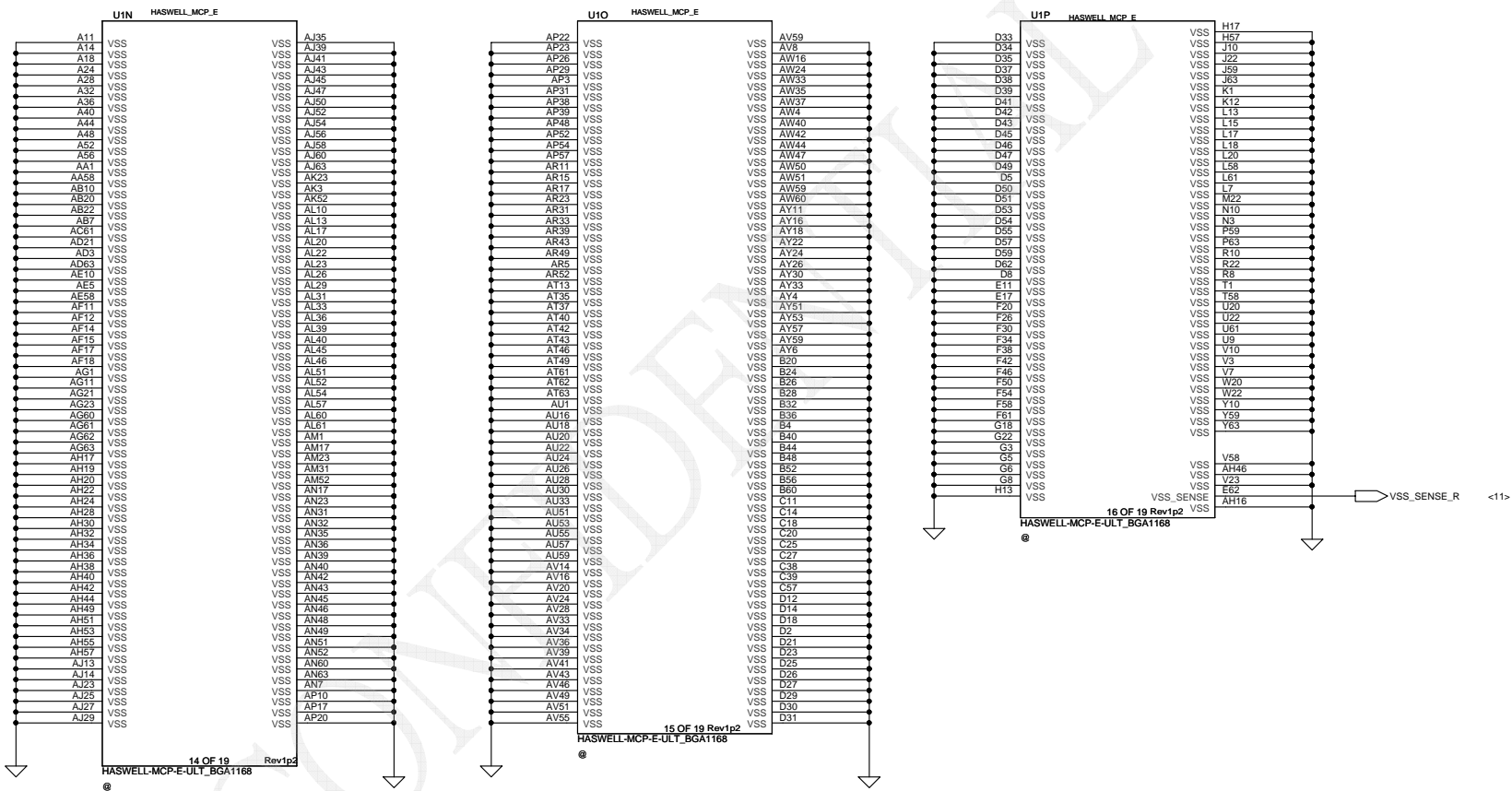


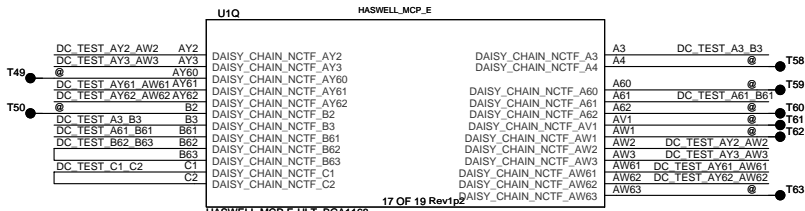
**+3VALW TO +3VALW(PCH AUX Power)
Short J8 for PCH VCCSUS3.3**



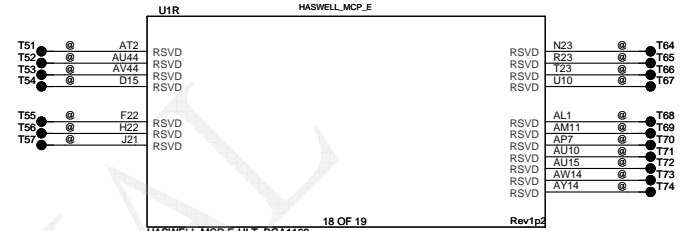
Broadwell only
Intel recommends a 0.47uF boot strap capacitor to be placed between V3.3DSW and DcpSUSBypp power rail to support in-rush current.

Security Classification	Compal Secret Data		Title	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	BDW MCP(9/11) Power
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Date: Wednesday, January 08, 2014				ZSWAH M/B LA-B162P
Sheet 12 of 54				

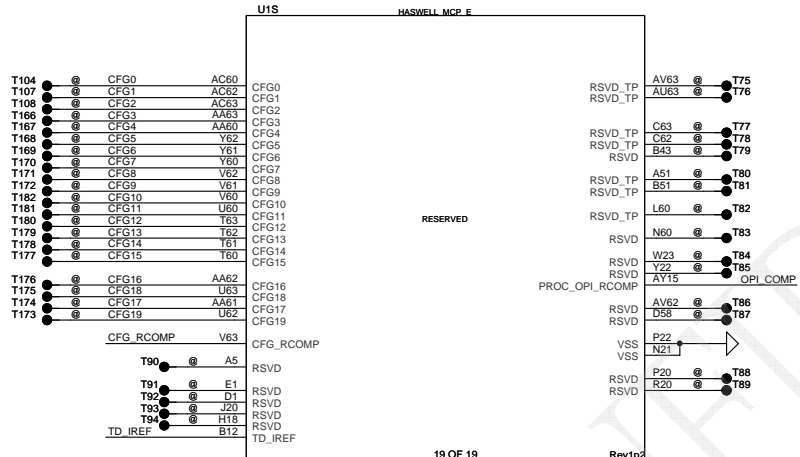




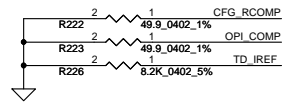
HASWELL-MCP-E-ULT_BGA1168
17 OF 19 Rev1p2



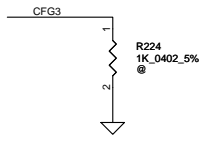
HASWELL-MCP-E-ULT_BGA1168
18 OF 19 Rev1p2



HASWELL-MCP-E-ULT_BGA1168
19 OF 19 Rev1p2

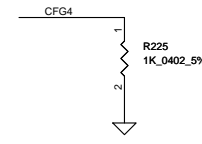


CFG Straps for Processor



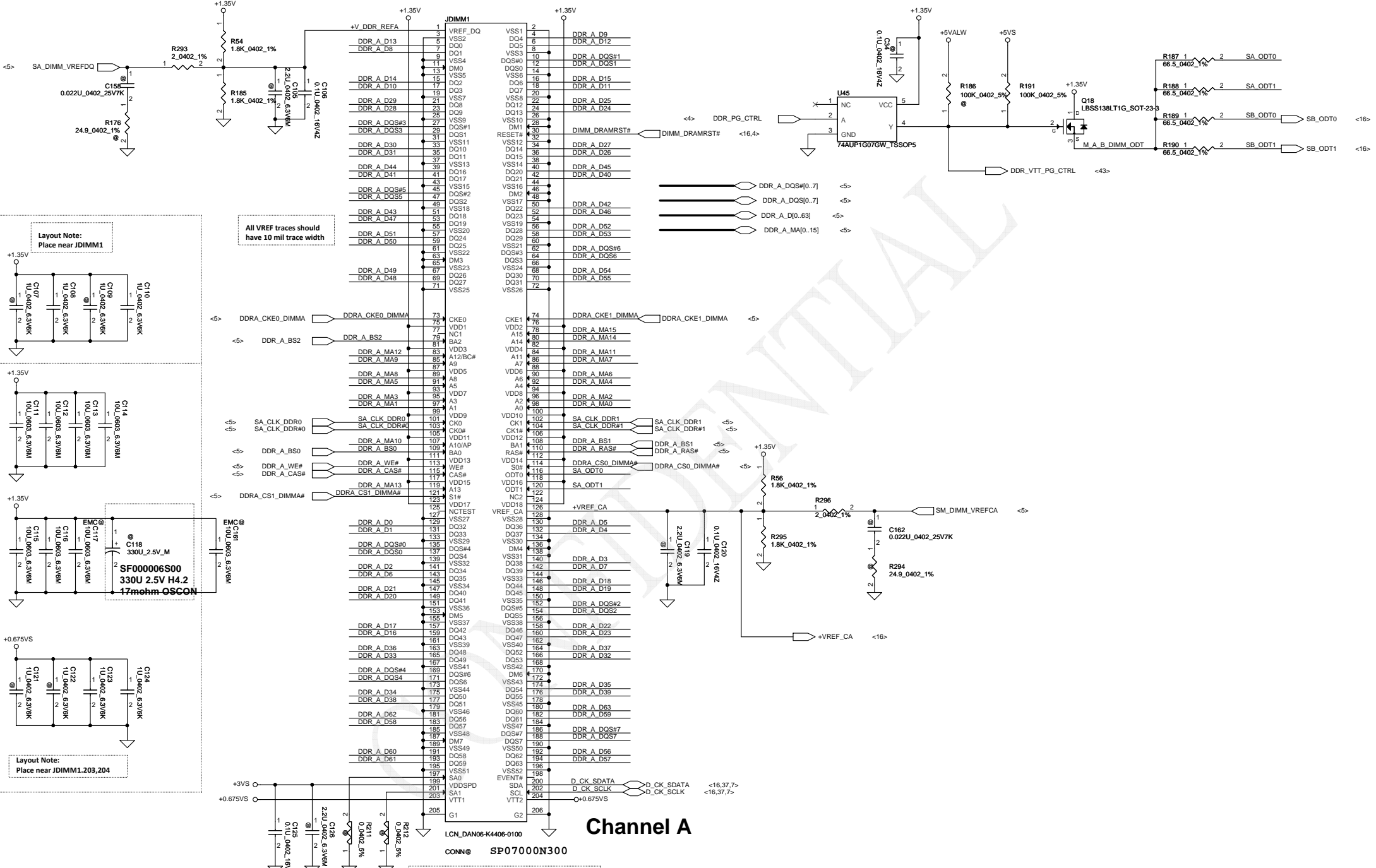
Physical Debug Enable (DFX Privacy)

CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
------	---



Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
------	--



Layout Note:
Place near JDIMM1

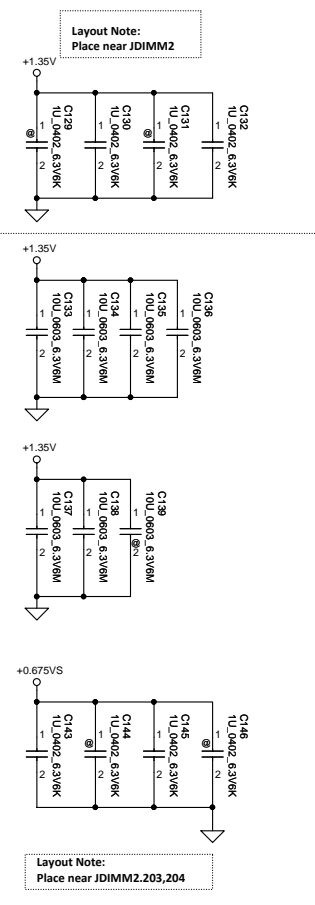
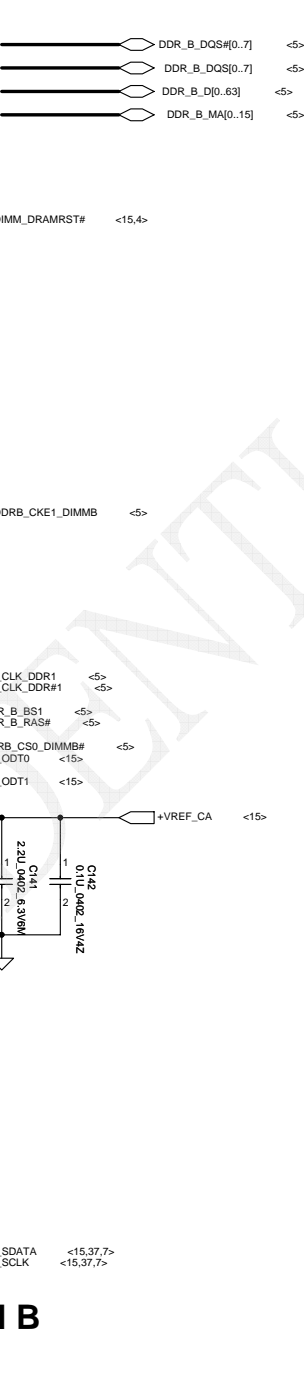
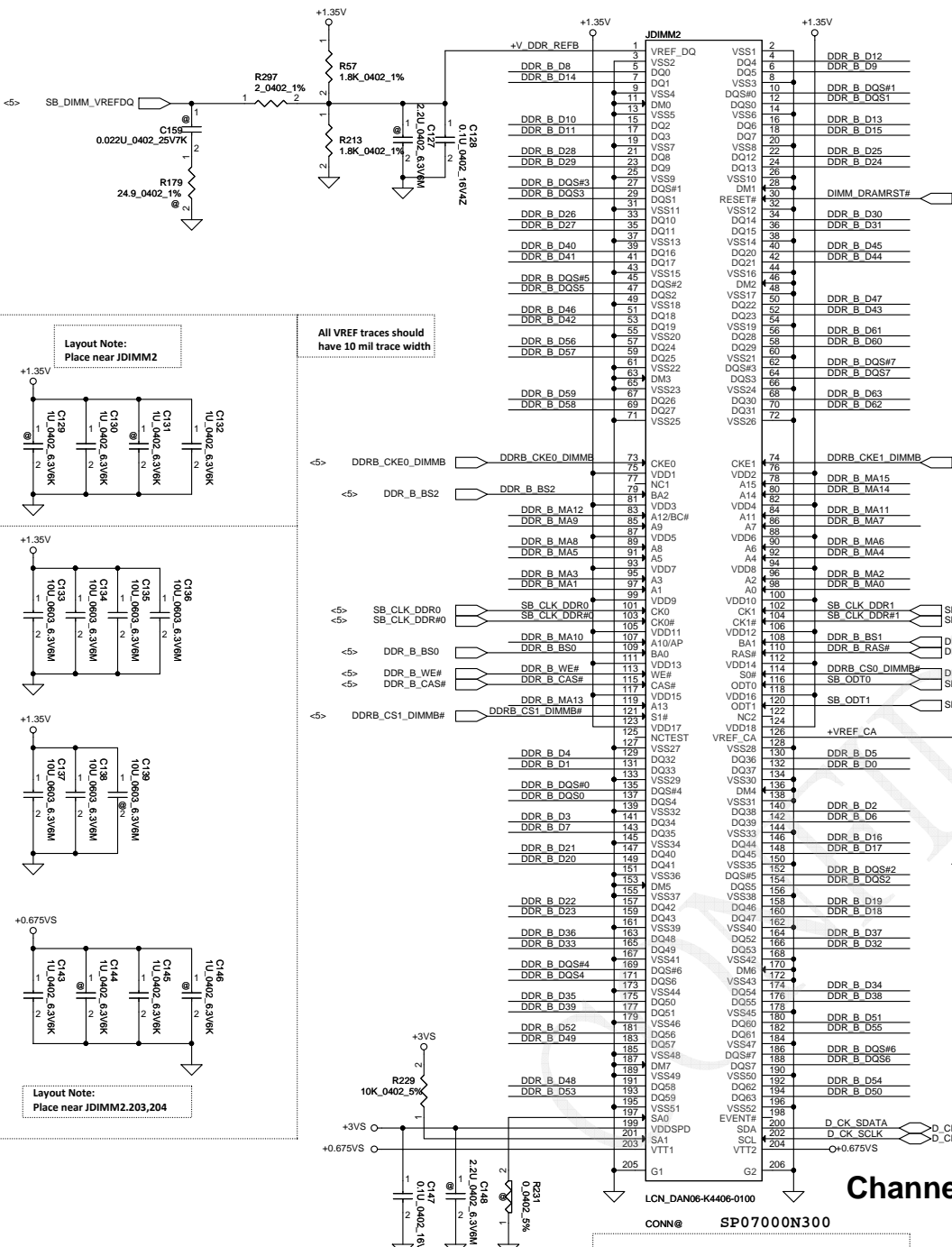
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1.203,204

Channel A

<Address: SA1:SA0=00>
DIMM_1 H:4mm
DIS for Standard type
UMA for Reverse type

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Customer			ZSWAH M/B LA-B162P	
Date:	Wednesday, January 08, 2014		Sheet	15 of 54

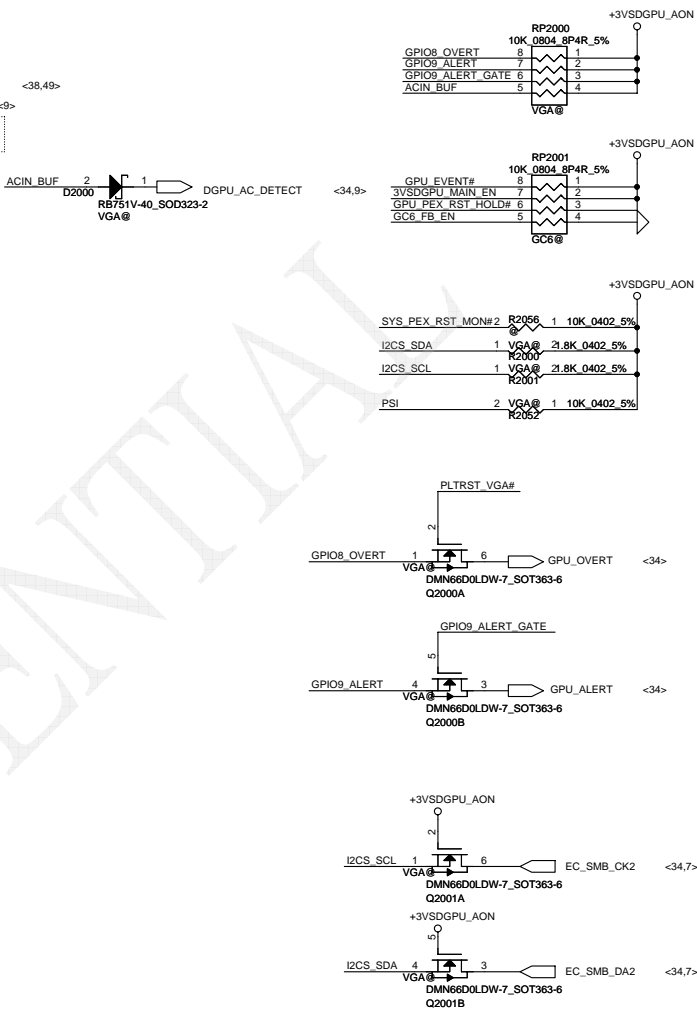
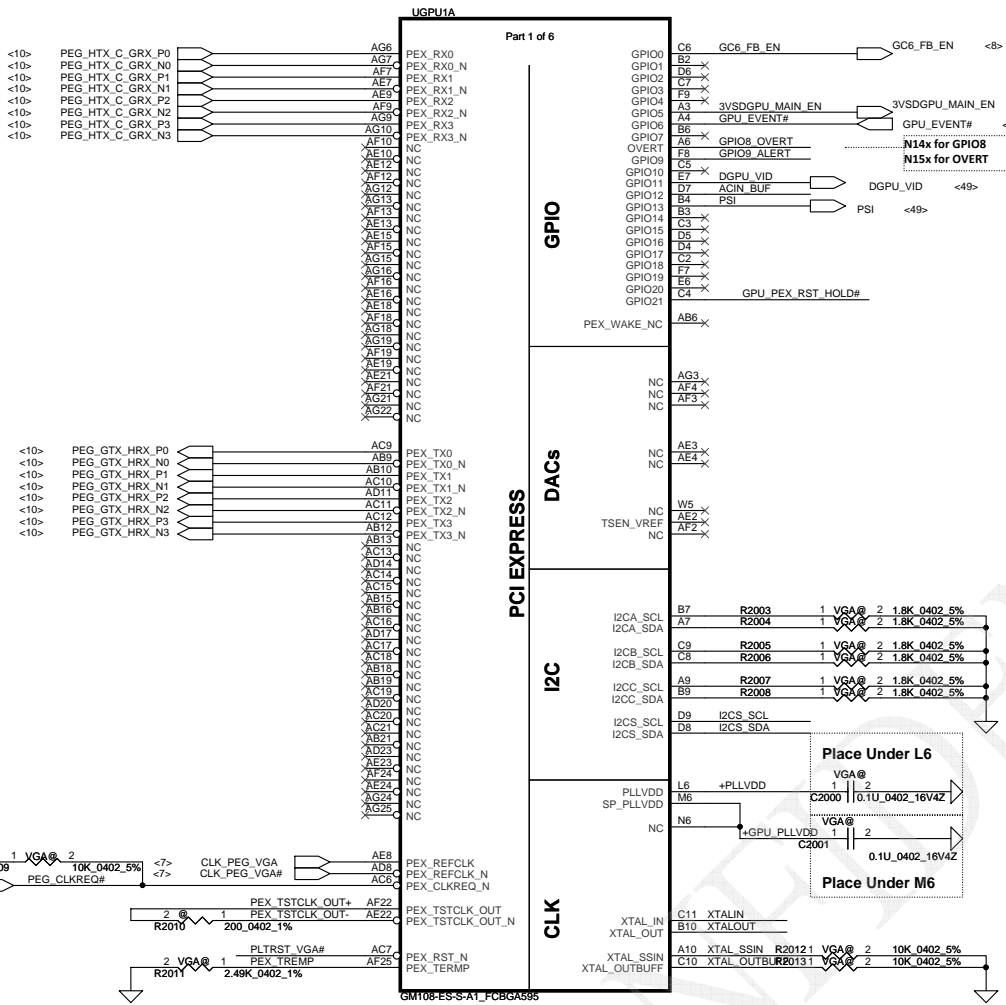


All VREF traces should have 10 mil trace width

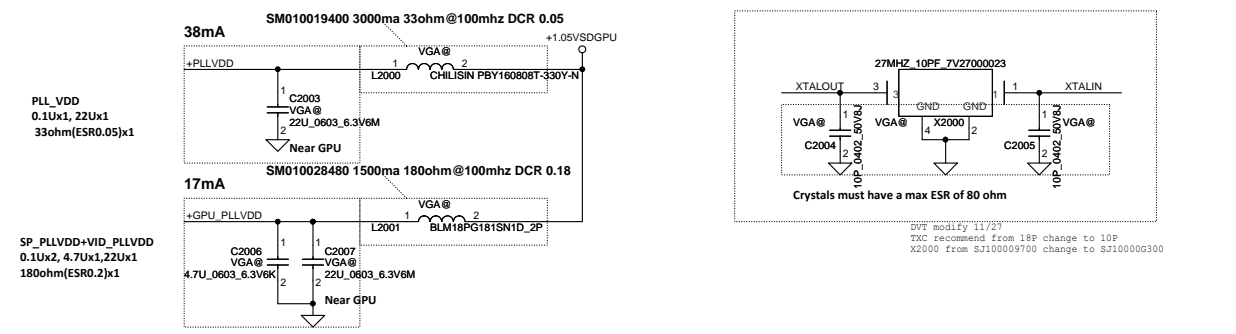
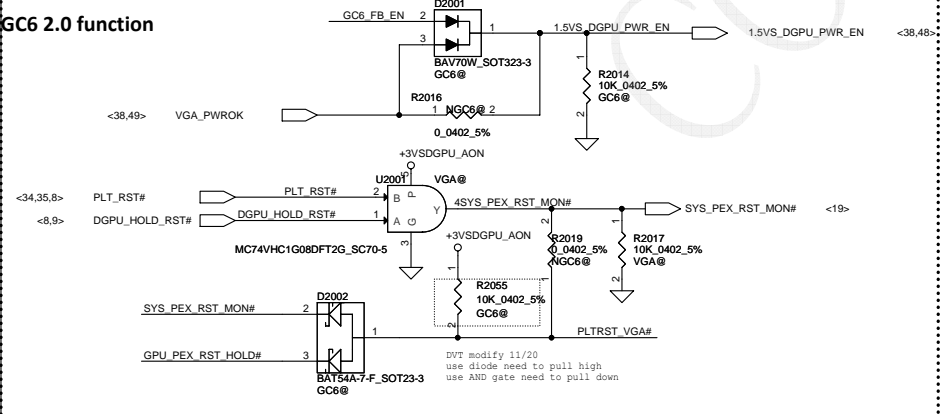
<Address: SA1:SA0=10>
DIMM_2 H:4mm
DIS for Standard type
UMA for Reverse type

Channel B

Security Classification	Compal Secret Data		Title	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	DDRIII DIMMB
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Document Number ZSWAH M/B LA-B162P			Date: Wednesday, January 08, 2014 Sheet 16 of 54	

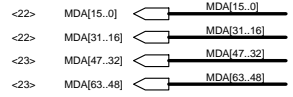


GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		



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Issued Date	2013/09/11	Deciphered Date	2013/09/24	Compal Electronics, Inc.	
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					Rev
					0.3
Date				Wednesday, January 08, 2014	Sheet 17 of 54

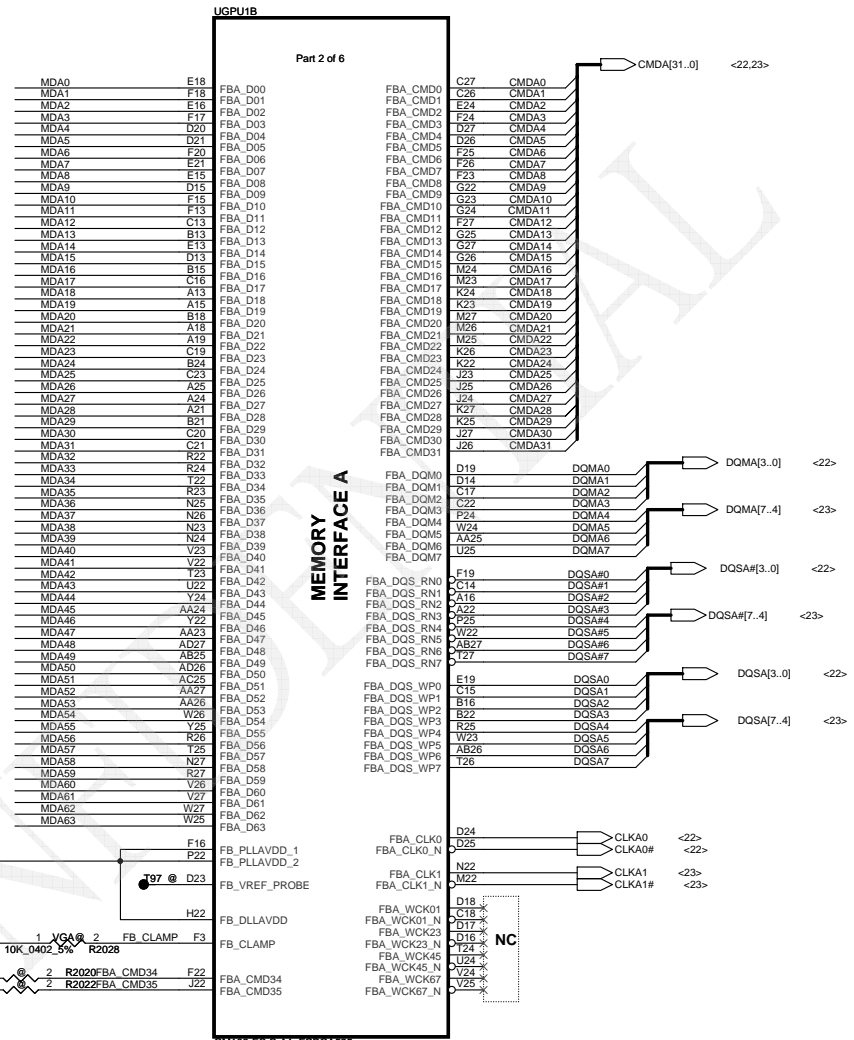
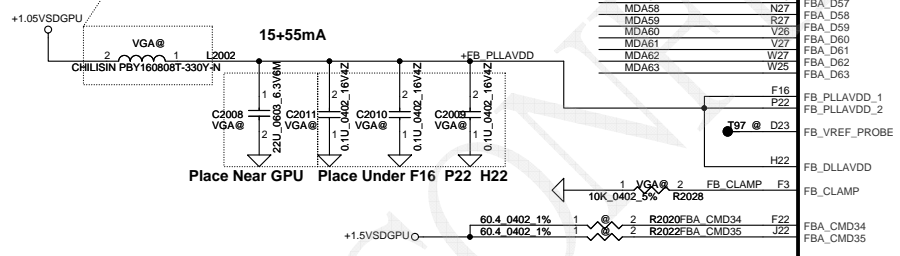
VRAM Interface



NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type	Footprint	Population	Location	
GB2B-64	FBx_PLL_AVDD	0.1 μF	X7R	0402	2	Under GPU
	FB_DLL_AVDD Combined	22 μF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05



UGPU1C

Part 3 of 6

AC3 NC
 AC4 NC
 Y4 NC
 Y9 NC
 AA3 NC
 AA2 NC
 AB1 NC
 AA1 NC
 AA4 NC
 AA5 NC
 XA5 NC
 AB5 NC
 AB4 NC
 AB9 NC
 AB2 NC
 AD5 NC
 AD2 NC
 AET NC
 AD4 NC
 AD5 NC
 T2 NC
 T9 NC
 T1 NC
 R1 NC
 R2 NC
 R3 NC
 N2 NC
 N3 NC
 V3 NC
 V4 NC
 U3 NC
 U4 NC
 T4 NC
 T5 NC
 R4 NC
 R5 NC
 N1 NC
 M1 NC
 M2 NC
 M3 NC
 K2 NC
 K3 NC
 K1 NC
 J1 NC
 M4 NC
 M5 NC
 L3 NC
 L4 NC
 K4 NC
 K5 NC
 J4 NC
 J5 NC
 N4 NC
 N5 NC
 P3 NC
 P4 NC
 J2 NC
 J3 NC
 H3 NC
 H4 NC
 C NC

NC

GENERAL

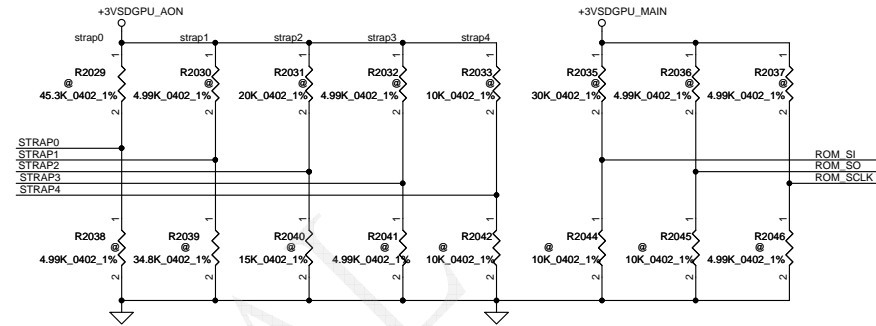
TEST

SERIAL

F11 AD10
 AD7
 B19
 V5
 V6
 T1
 G2
 G3
 G4
 G5
 G6
 G7
 V1
 V2
 W1
 W2
 W3
 W4
 D11 R2050 1 @ 2 10K 0402 5%
 D10
 E9 SYS_PEX_RST_MON#
 E10
 F10
 D1 STRAP0
 D2 STRAP1
 E4 STRAP2
 E3 STRAP3
 D3 STRAP4
 C1
 F6 MULTI STRAP REF0_GND 1 SGT @ 2
 F4
 F5
 F12
 E12
 F2 VCCSENSE_VGA
 VCCSENSE_VGA <49>
 F1 VSSSENSE_VGA
 VSSSENSE_VGA <49>
 AD9 TESTMODE R2054 1 VGA @ 2 10K 0402 5%
 AE5 JTAG_TCK PAD @ T18
 AE6 JTAG_TDI PAD @ T1
 AF6 JTAG_TDO PAD @ T186
 AD6 JTAG_TMS PAD @ T3
 AG4 JTAG_RST R2053 1 VGA @ 2 10K 0402 5%
 D12
 B12 ROM_SI
 A12 ROM_SO
 C12 ROM_SCLK

For G62.0 use
 N14x for CEC_NC
 N15x for GPIO8

MULTI LEVEL STRAPS



For N15S-GT Binary strap table

Decive ID : 0x1341

GPU	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15S-GT	X76550BOL01	1GHz	128Mx16x4	0x7 (SA000067550) Micron MT41J128M16JT-093G-K	PU 50K	NC	NC	NC	NC	PD 45.3K	PD 4.99K	PD 4.99K
	X76550BOL02			0x8 (SA000068U90) Samsung K4W2G1646Q-BC1A						PU 4.99K		
	X76550BOL07			0x6 (SA00006H430) Hynix H5TC2G63FFR-11C						PD 34.8K		
	X76550BOL05	0x1 (SA000077K20) Micron MT41J256M16HA-093G-E	PD 10K									
	X76550BOL06	2GHz	256Mx16x4	0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
				0x0 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 4.99K		

For N15V-GL/GM Binary strap table

Decive ID : 0x1140

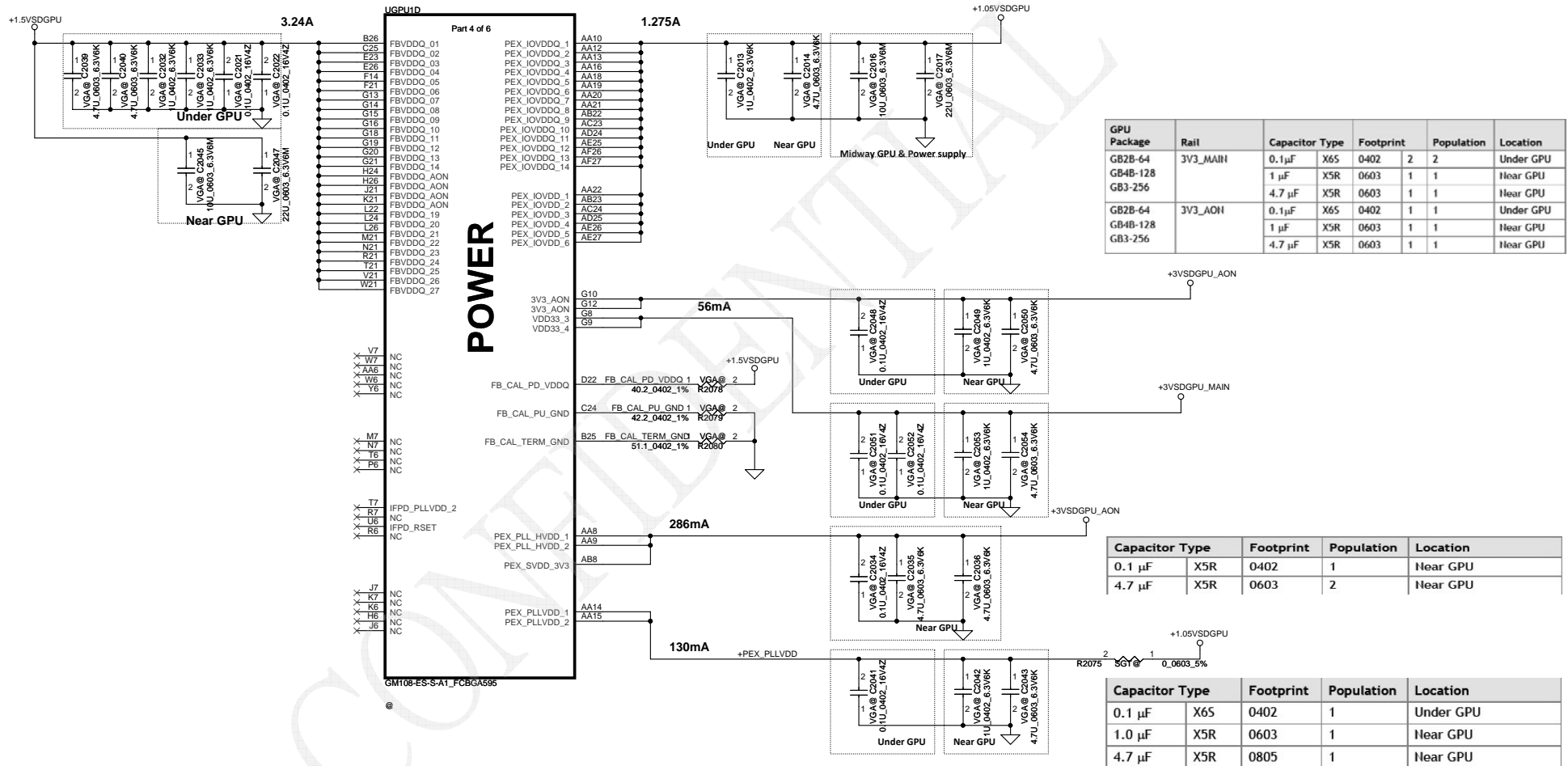
GPU	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GL N15V-GM	X76550BOL03	1GHz	128Mx16x4	0x1 (SA000067550) Micron MT41J128M16JT-093G-K	PU 10K	PD10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	X76550BOL04			0x5 (SA000068U00) Samsung K4W2G1646E-BC1A	PU 10K	PD10K	PU 10K	PD 10K				
	X76550BOL08			0xC (SA00006H430) Hynix H5TC2G63FFR-11C	PD 10K	PD10K	PU 10K	PU 10K				
	X76550BOL05	2GHz	256Mx16x4	0xE (SA000068U90) Samsung K4W2G1646Q-BC1A	PD 10K	PU 10K	PU 10K	PU 10K				
				0x9 (SA000076P20) Samsung K4W4G1646D-BC1A	PU 10K	PD10K	PD 10K	PU 10K				
				0xD (SA000077K20) Micron MT41J256M16HA-093G-E	PU 10K	PD10K	PU 10K	PU 10K				
X76550BOL06	0x4 (SA00006E840) Hynix H5TC4G63AFR-11C	PD 10K	PD10K	PU 10K	PD 10K							

GMT08-ES-S-A1_FCBGA595

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF	X7R 0402	2 2	Under GPU
	1µF	X7R 0603	2 2	Under GPU
	4.7µF	X6S 0603	2 2	Under GPU
	10µF	X5R 0805	1 1	Near GPU
	22µF	X5R 0805	1 1	Near GPU

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0µF	X6S 0402	1	Under GPU
	4.7µF	X6S 0603	1	Near GPU
	10µF	X5R 0805	1	Midway between GPU and Power Supply
	22µF	X5R 0805	1	Midway between GPU and Power Supply



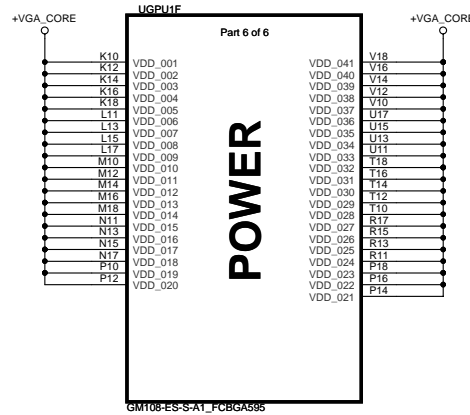
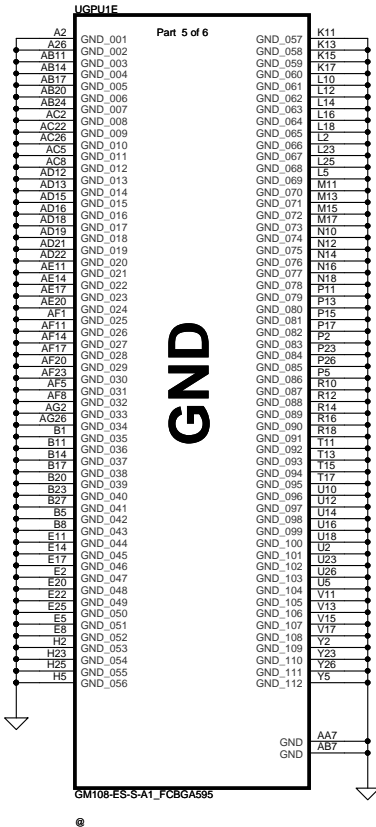
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIH	0.1µF	X6S 0402	2 2	Under GPU
GB4B-128		1µF	X5R 0603	1 1	Near GPU
GB3-256		4.7µF	X5R 0603	1 1	Near GPU
GB2B-64	3V3_AOH	0.1µF	X6S 0402	1 1	Under GPU
GB4B-128		1µF	X5R 0603	1 1	Near GPU
GB3-256		4.7µF	X5R 0603	1 1	Near GPU

Capacitor Type	Footprint	Population	Location
0.1µF	X5R	0402	1 Near GPU
4.7µF	X5R	0603	2 Near GPU

Capacitor Type	Footprint	Population	Location
0.1µF	X6S	0402	1 Under GPU
1.0µF	X5R	0603	1 Near GPU
4.7µF	X5R	0805	1 Near GPU



SM010028800 2000ma 120ohm @100mhz DCR 0.1



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X65	0603	10	10	Under GPU
	1 μ F	X65	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		(A)	(A)	(A)
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at $T_j = 102^\circ\text{C}$

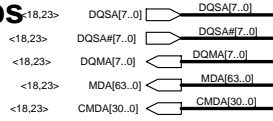
Power Supply Rail (V)	N15V-GM-S
	DDR3/L (A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

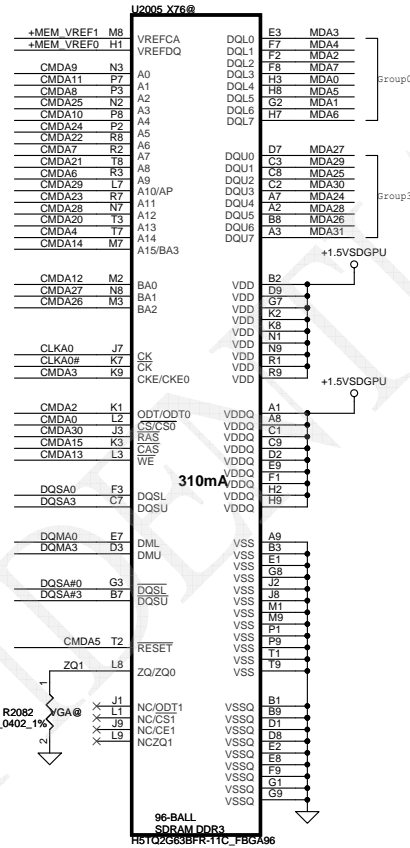
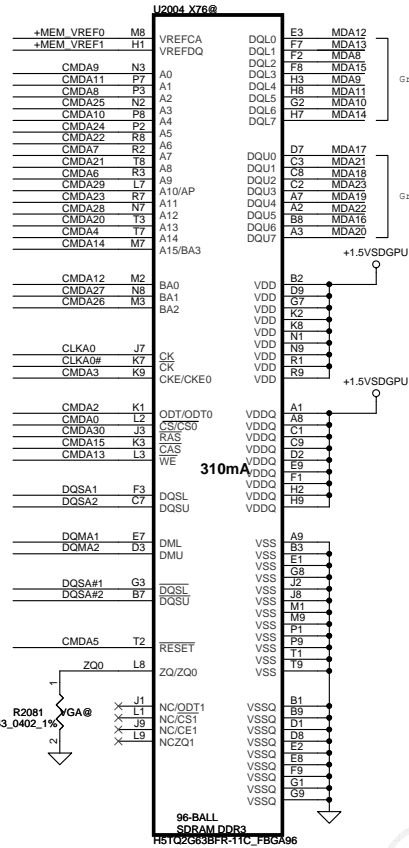
Table 7. EDP-Peak at $T_j = 102^\circ\text{C}$

Power Supply Rail (V)	N15V-GL
	DDR3 (A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

VRAM DDR3 chips

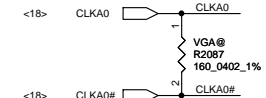
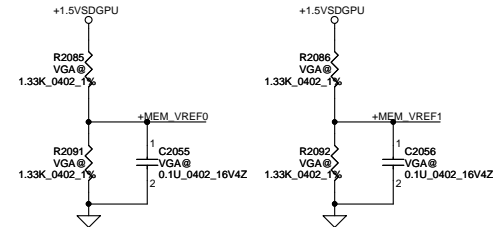
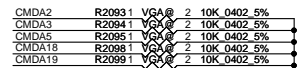
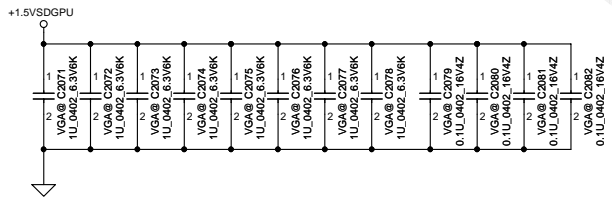


Low 32

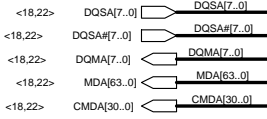


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

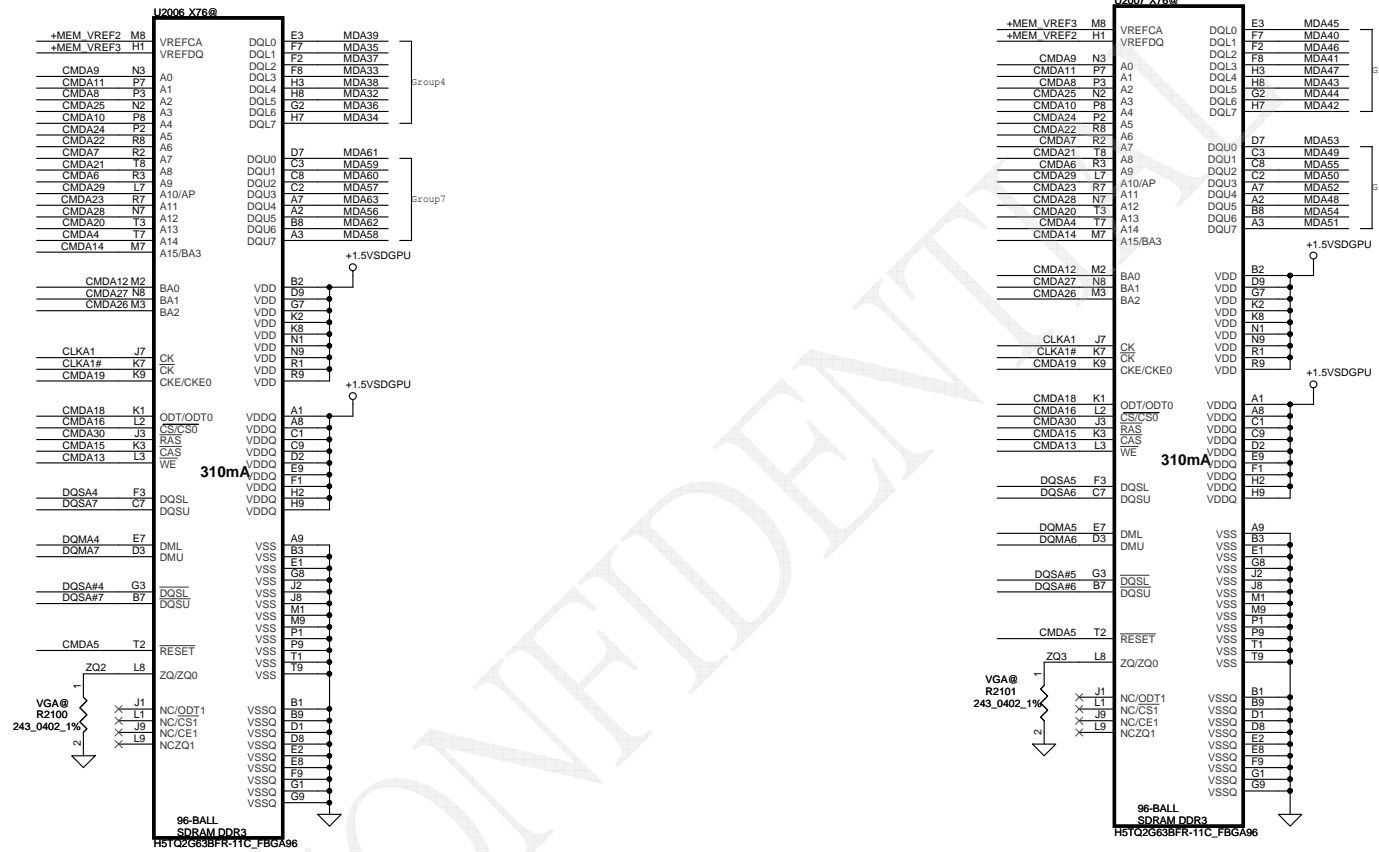
DDR3	Command Bit	Default Pull-down
	ODTx	10k
CKEx	10k	
RST	10k	
CS*	No Termination	



VRAM DDR3 chips



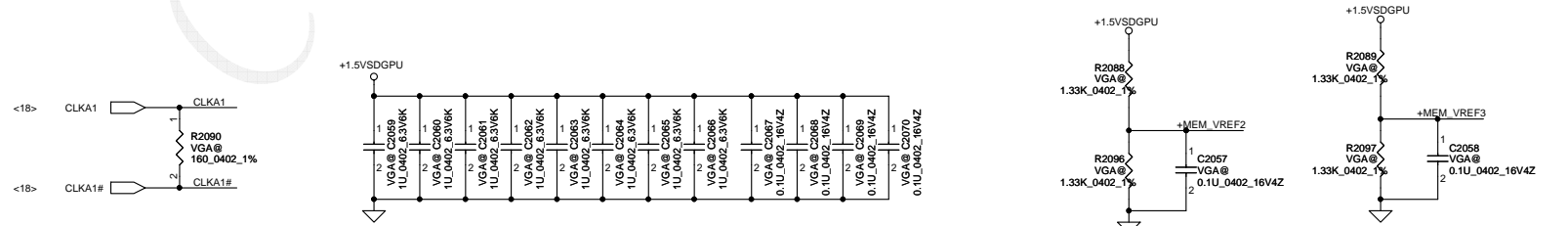
High 32



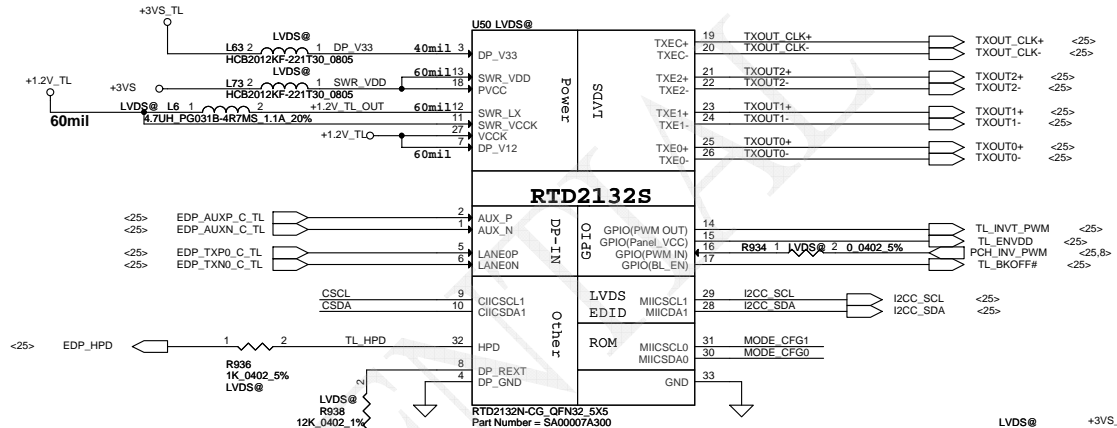
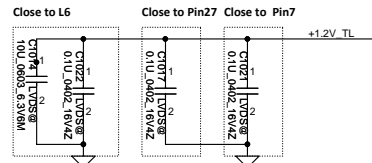
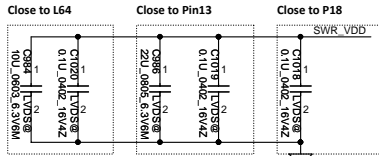
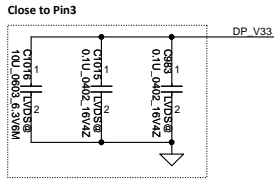
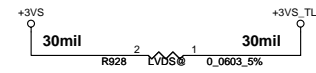
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

LOW HIGH

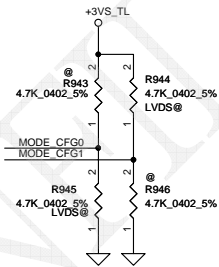
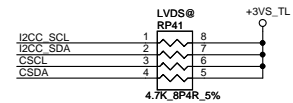
Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination



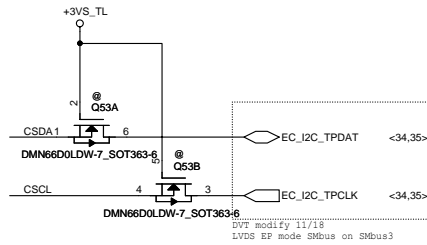
LVDS Translator - RTD2132R



use 2132S symbol

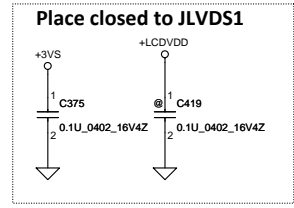
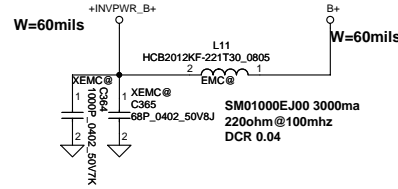
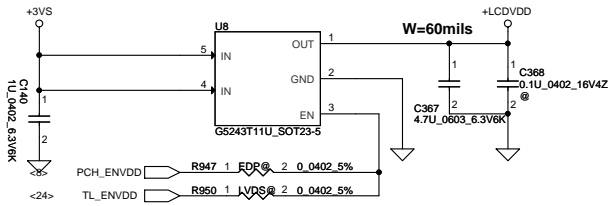


		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE*	EEPROM MODE

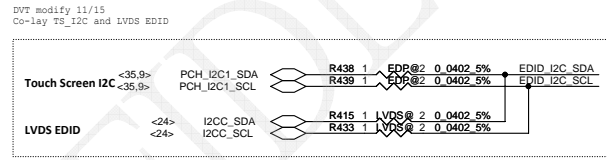
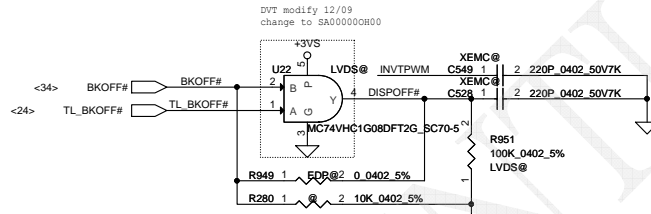
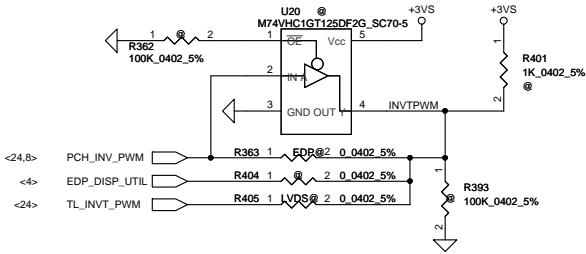
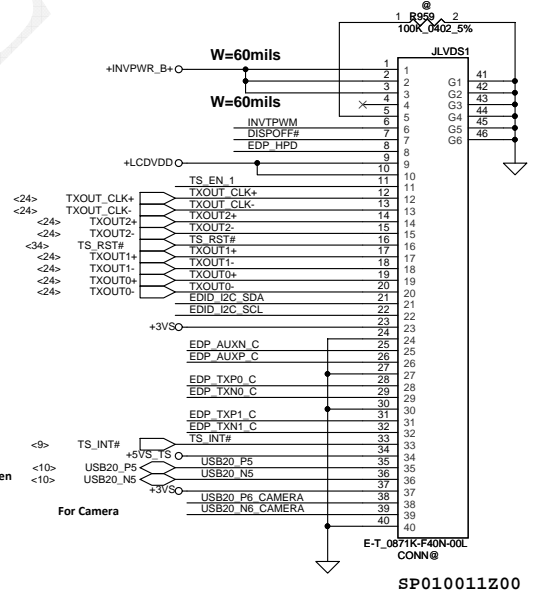


EDP / LVDS conn.

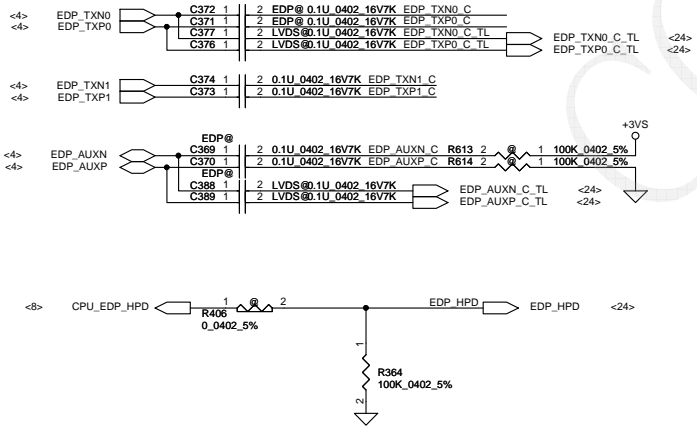
LCD POWER CIRCUIT



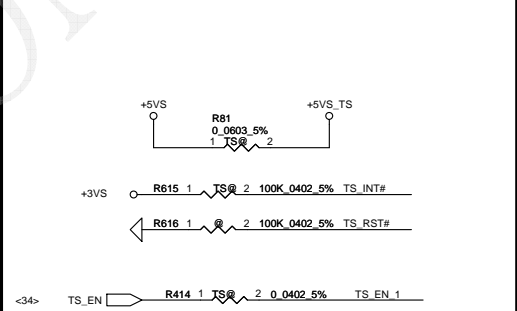
LCD / LED PANEL Conn.



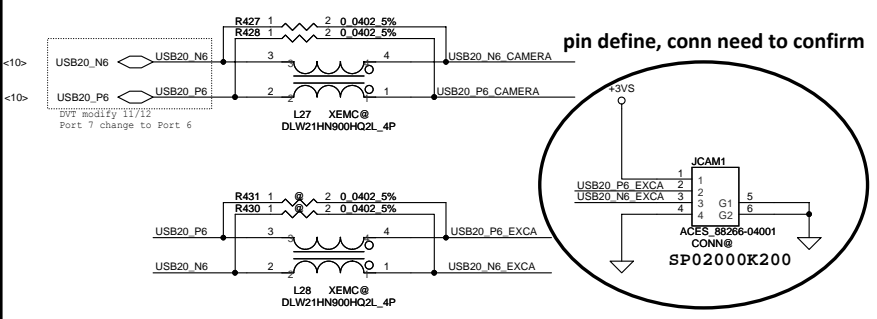
eDP



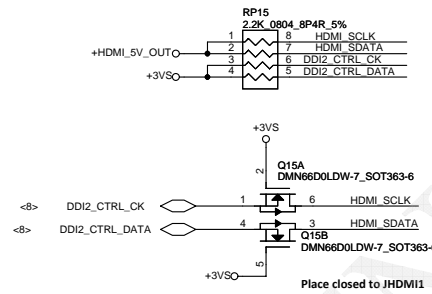
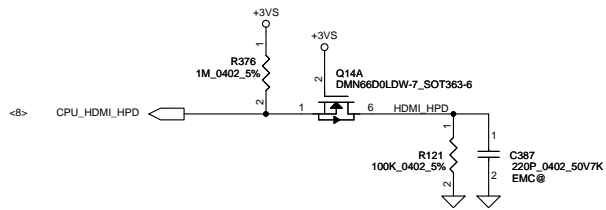
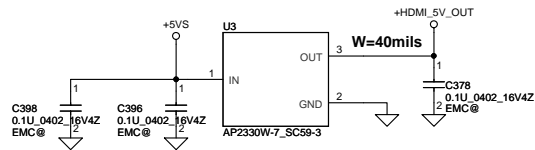
Touch Screen



Camera

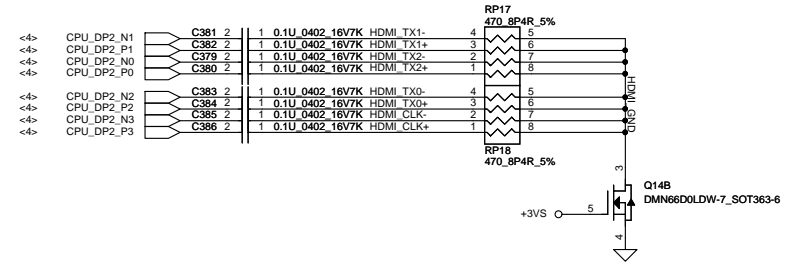


HDMI conn.

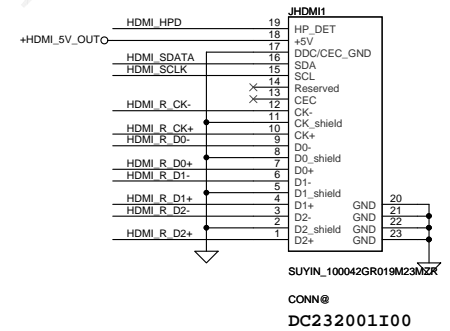


SM070001310 400ma 90ohm @100mhz DCR 0.3

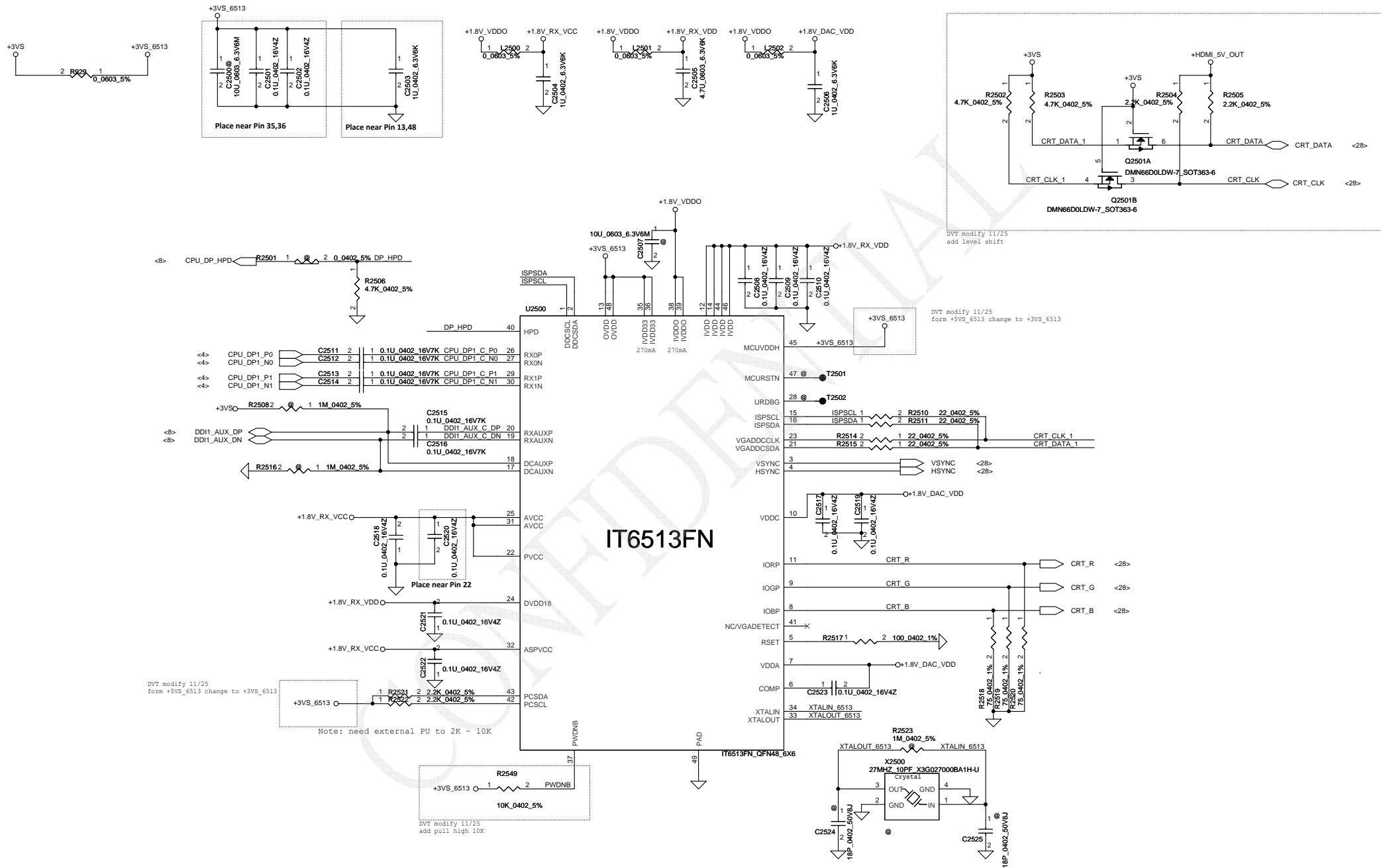
HDMI_CLK-	R368	1	XEMC@ 2	0.0402.5%	HDMI_R_CLK-
HDMI_CLK+	R369	1	XEMC@ 2	0.0402.5%	HDMI_R_CLK+
HDMI_TX0-	R370	1	XEMC@ 2	0.0402.5%	HDMI_R_D0-
HDMI_TX0+	R371	1	XEMC@ 2	0.0402.5%	HDMI_R_D0+
HDMI_TX1-	R372	1	XEMC@ 2	0.0402.5%	HDMI_R_D1-
HDMI_TX1+	R373	1	XEMC@ 2	0.0402.5%	HDMI_R_D1+
HDMI_TX2-	R374	1	XEMC@ 2	0.0402.5%	HDMI_R_D2-
HDMI_TX2+	R375	1	XEMC@ 2	0.0402.5%	HDMI_R_D2+



HDMI connector

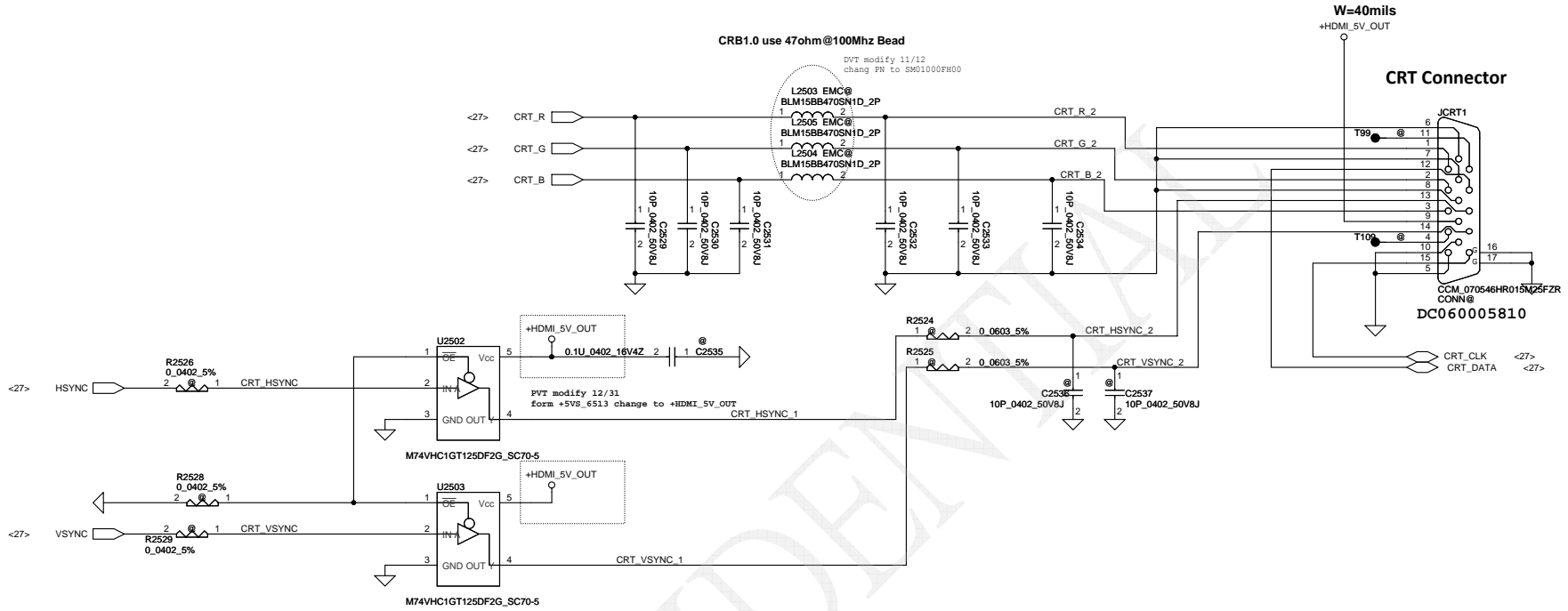


DP to VGA-IT6513



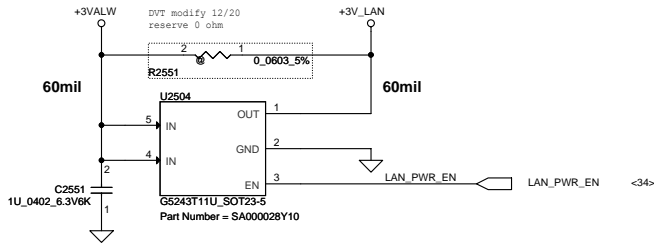
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	Title	
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				Z5WAH M/B LA-B162P	0.3
Date: Wednesday, January 08, 2014				Sheet	27 of 54

CRT conn.

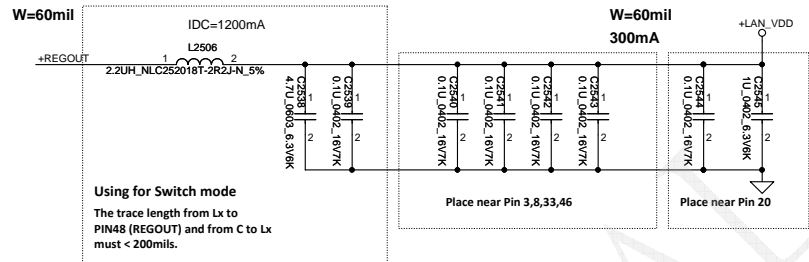


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Date: Wednesday, January 08, 2014				Sheet 28 of 54

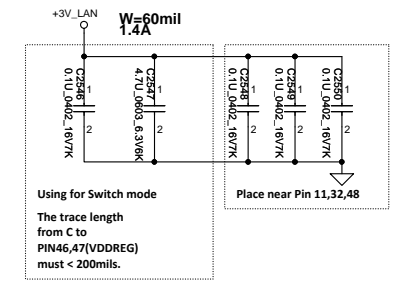
LAN-RTL8411B



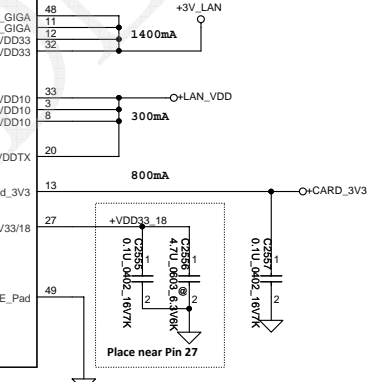
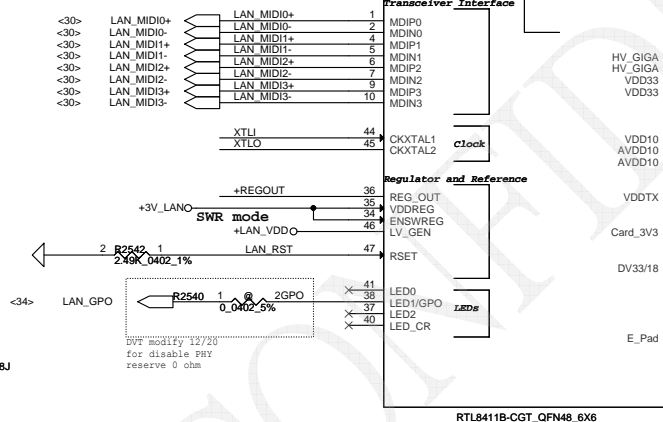
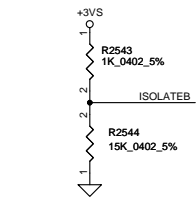
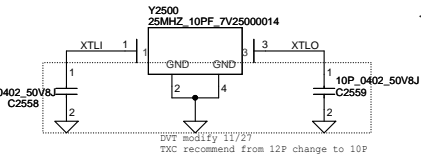
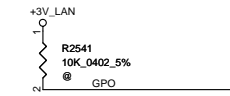
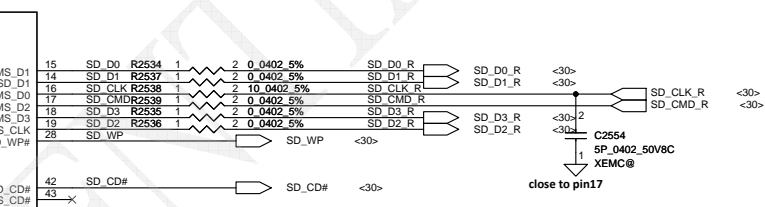
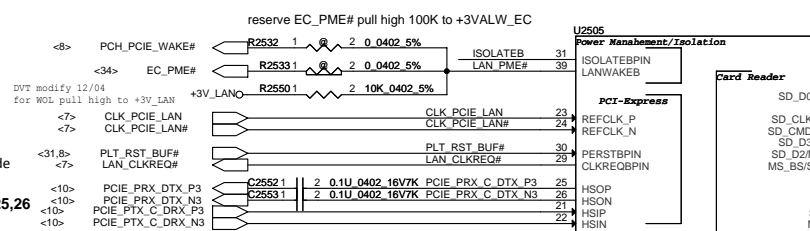
From EC
High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms



Using for Switch mode
The trace length from Lx to PIN48 (+REGOUT) and from C to Lx must < 200mils.

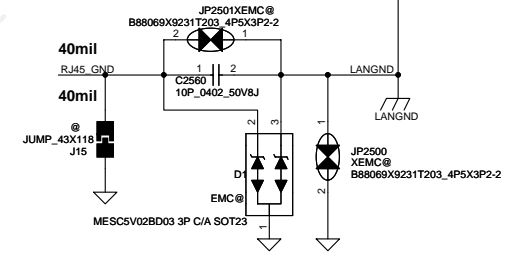
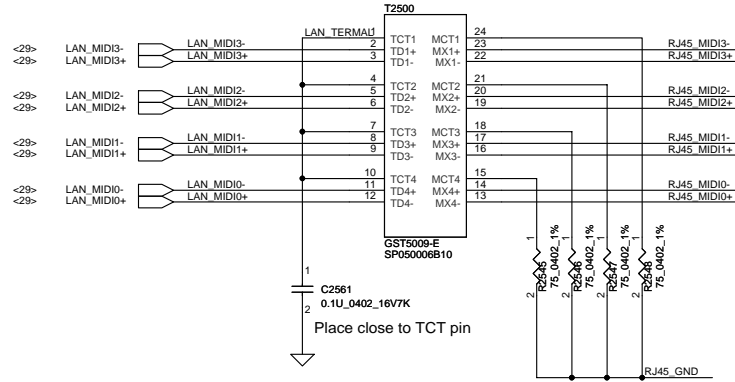


Using for Switch mode
The trace length from C to PIN47 (VDDREG) must < 200mils.

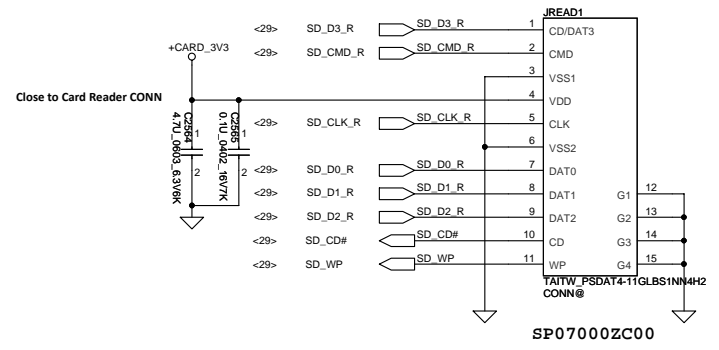


	Protect contact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

RJ45 / Card Reader conn.

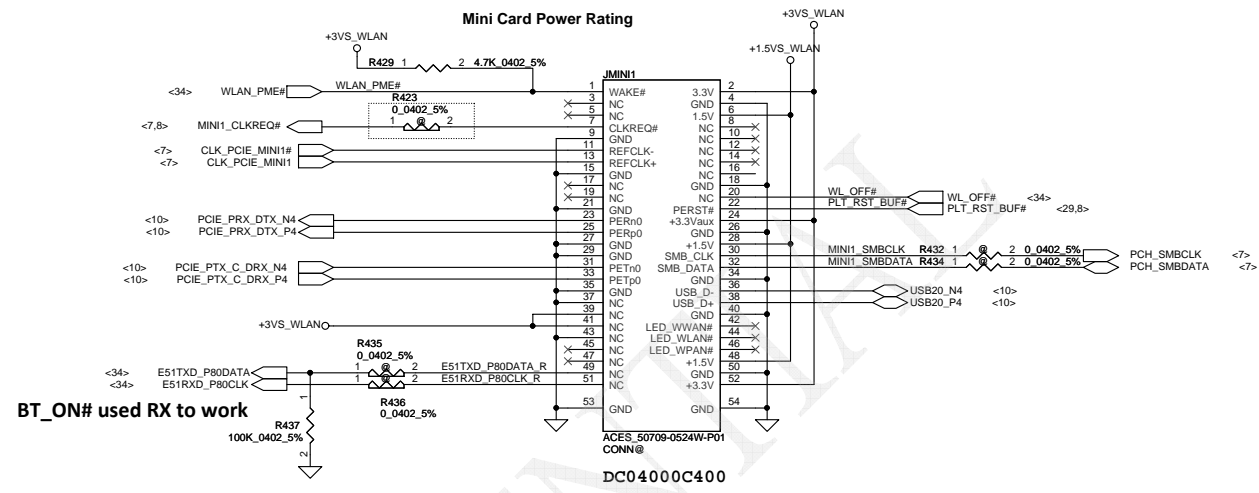
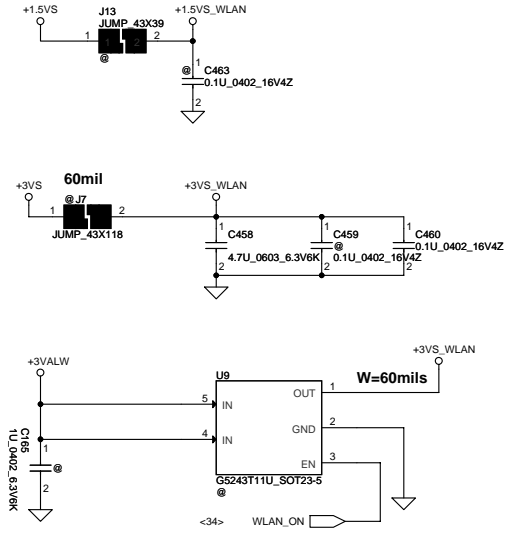


Card Reader Connector



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			Rev	0.3
			Date:	Wednesday, January 08, 2014
			Sheet	30 of 54

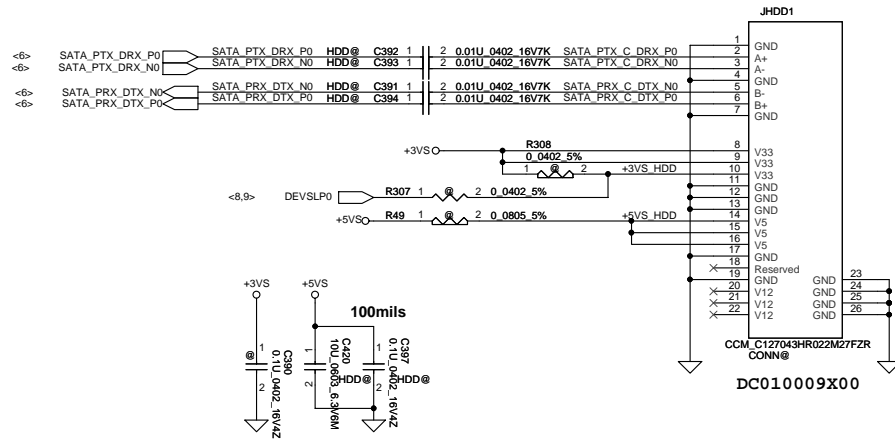
Wireless LAN



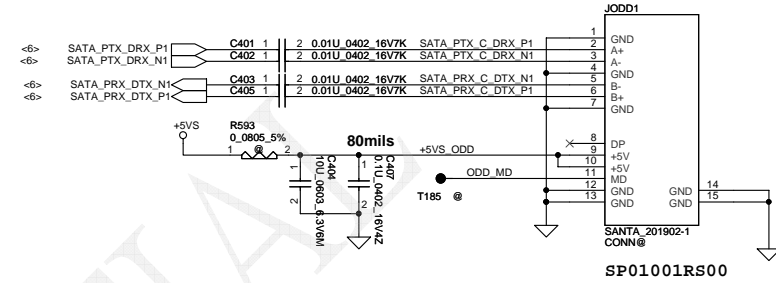
CONFIDENTIAL

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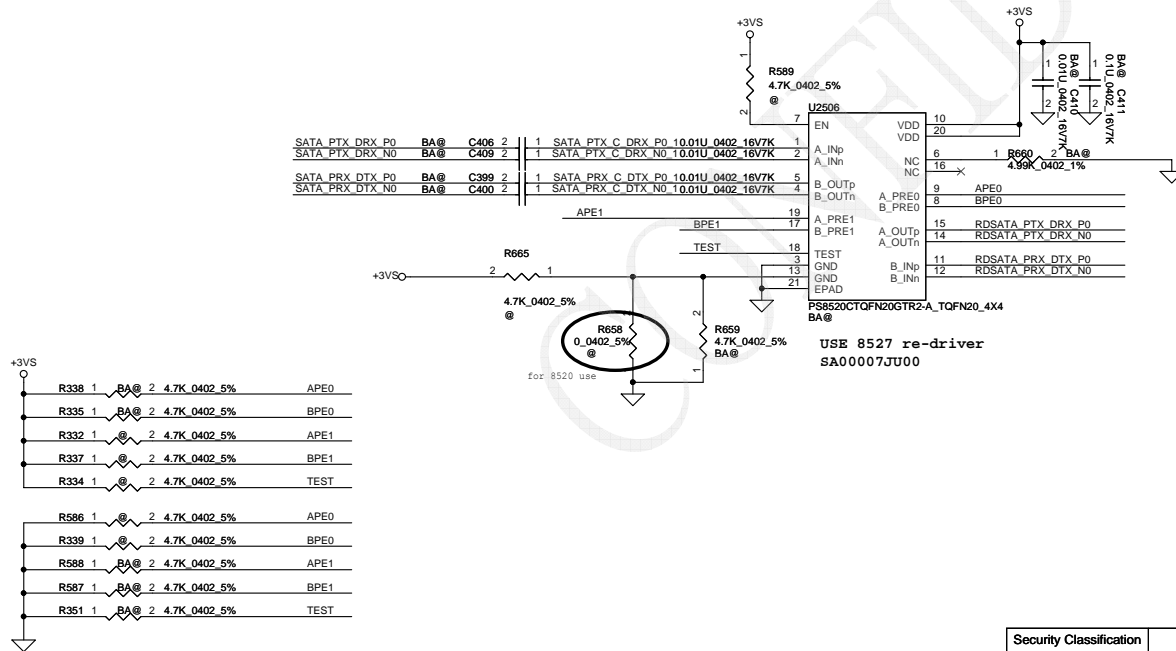
SATA HDD1 Conn.



SATA ODD Conn.

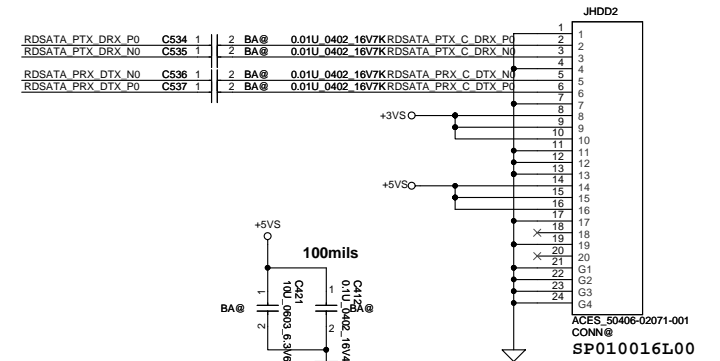


SATA Re-Driver HDD Conn. for BA50



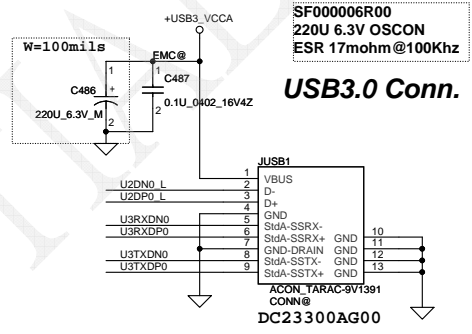
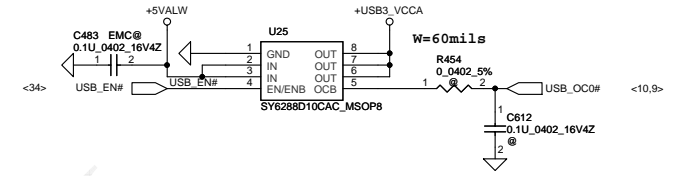
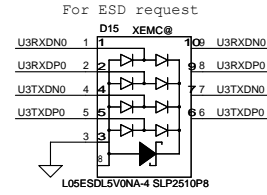
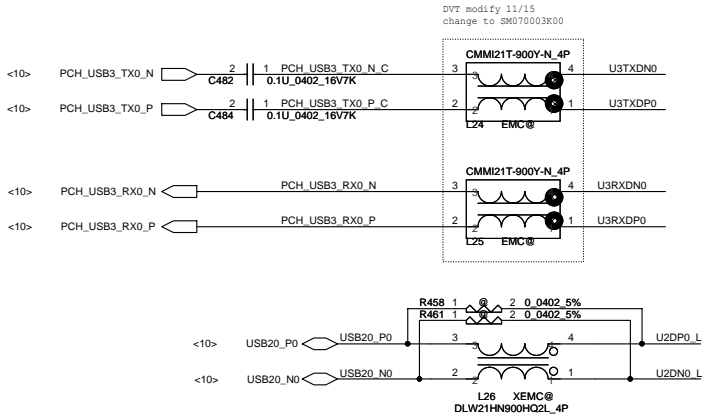
SATA HDD1 Conn.

CL 4.0 mm

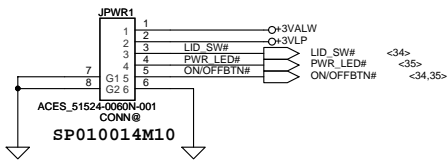


Security Classification	Compal Secret Data		Title	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	HDD/ODD/ HDD Re-Driver
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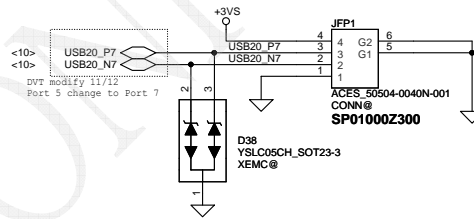
USB3.0 (Port 0)



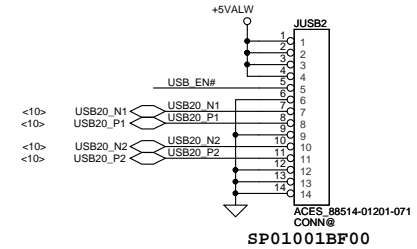
PWR/B



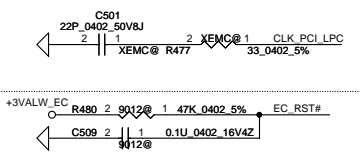
Finger Print /B for BA50



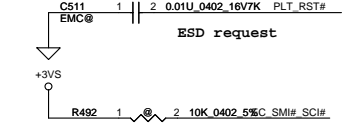
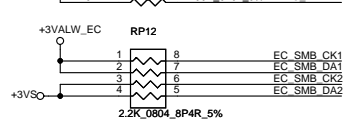
USB/B (USB Port 1, Port2)



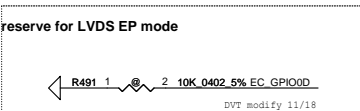
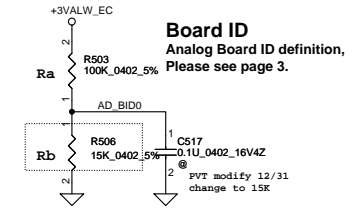
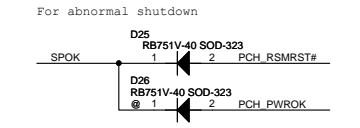
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				Document Number	Rev
				Z5WAH M/B LA-B162P	0.3
				Date: Wednesday, January 08, 2014	Sheet 33 of 54



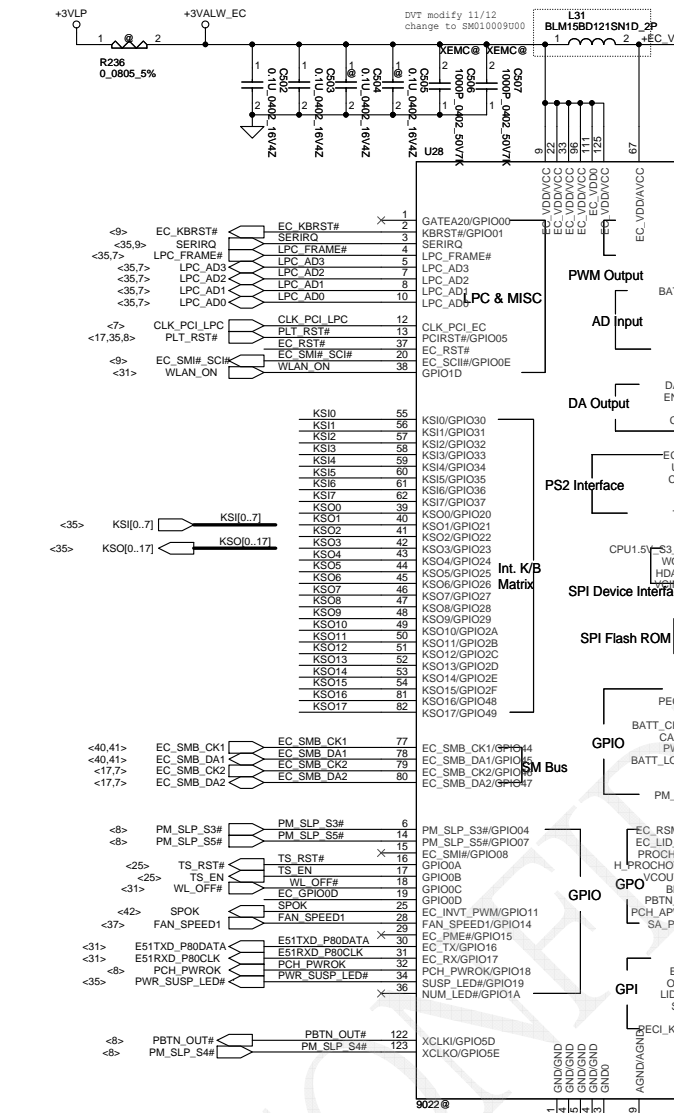
9022: ECRST# is internally pull-up to VCC via 40Kohm resistor, so can remove external pull-up resistor and capacitor.



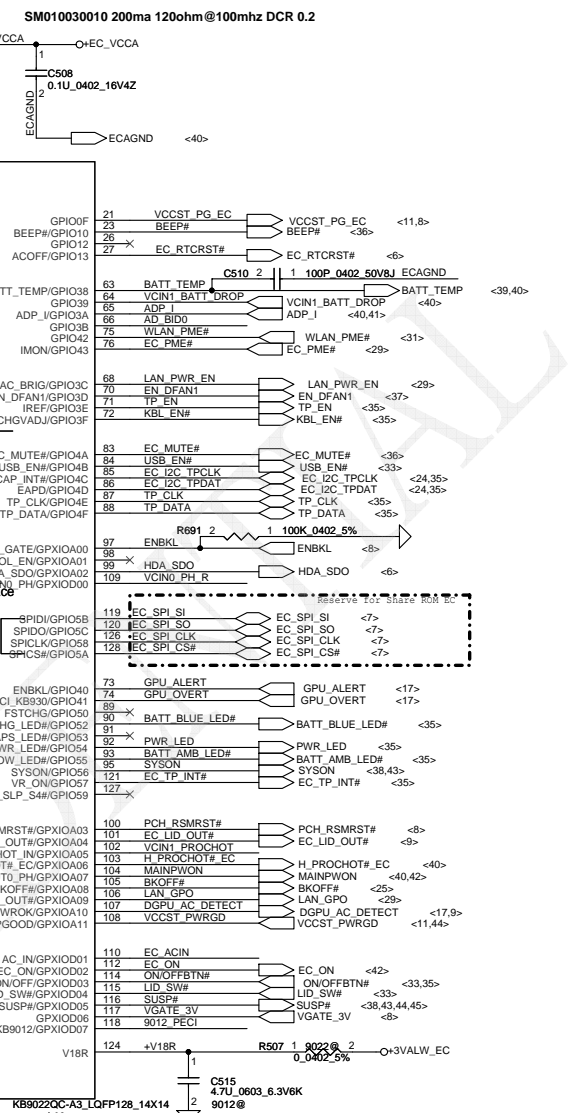
9022: Change control method from push-pull to open-drain, so EC_SCI# must be pull high. *PU on PCH side (Pull high in PCH side)



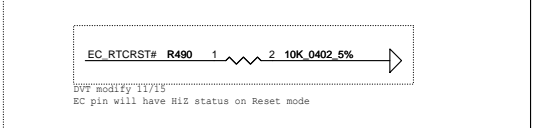
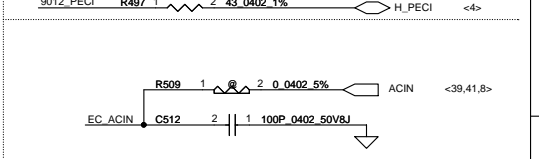
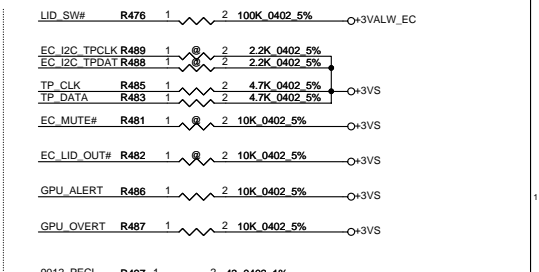
DVT modify 11/18



DVT modify 11/12 change to SM010009U00

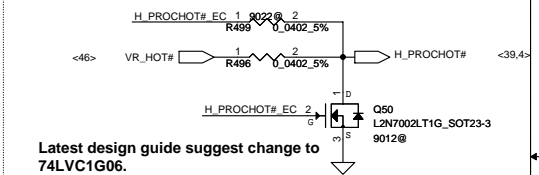


DVT modify 11/12 change to SM010009U00

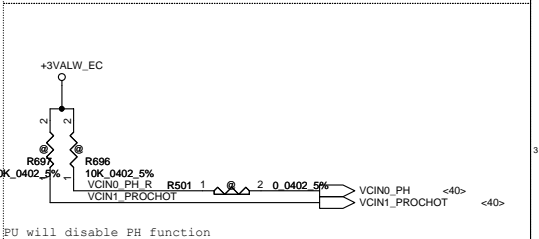


DVT modify 11/15 EC pin will have HiZ status on Reset mode

KB9022&9012 Co-Layout Item

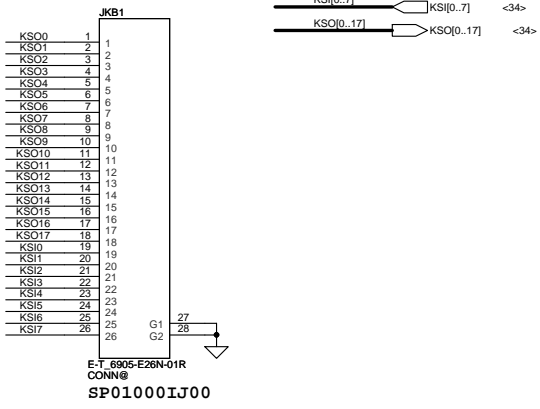


Latest design guide suggest change to 74LVC1G06.

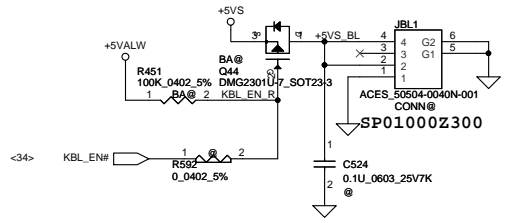


PU will disable PH1 function

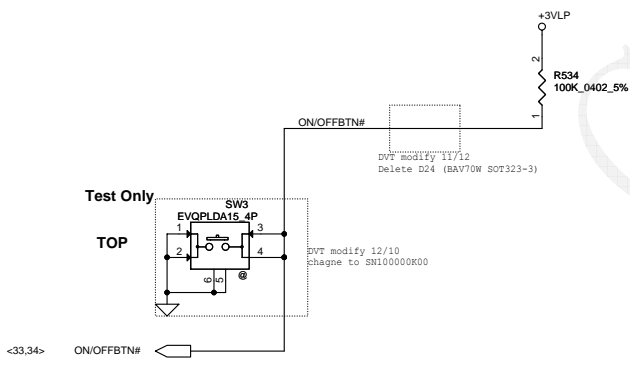
KB Conn.



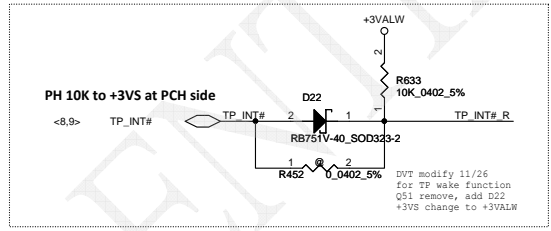
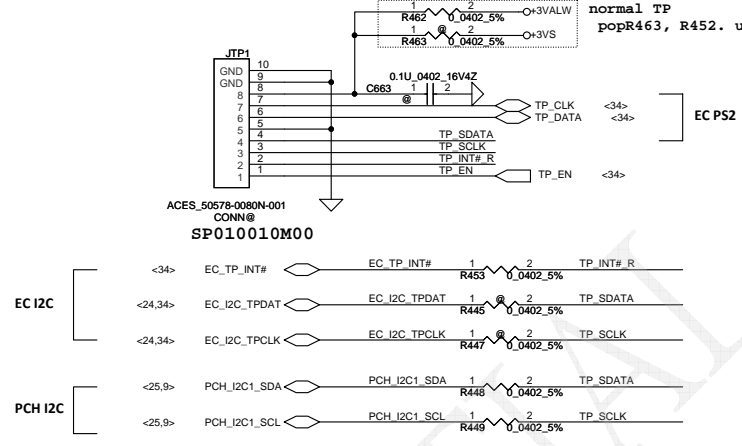
KB BackLight Conn. Reserve



ON/OFF BTN

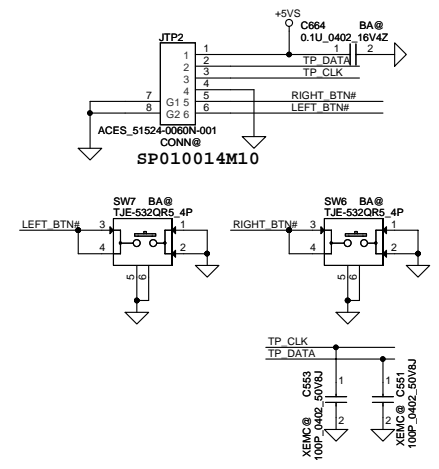


TP/B Conn.

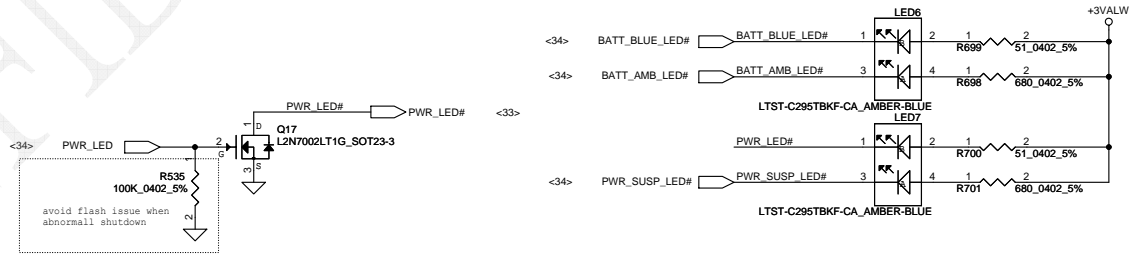


Support TP Wake
pop R462, D22. unpop R463, R452.
normal TP
pop R463, R452. unpop R462, D22

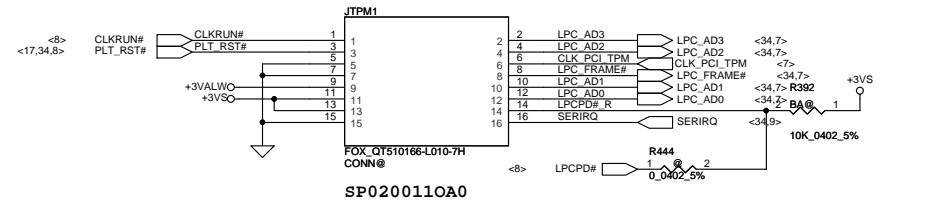
To BA50 TP/B Conn.



LED

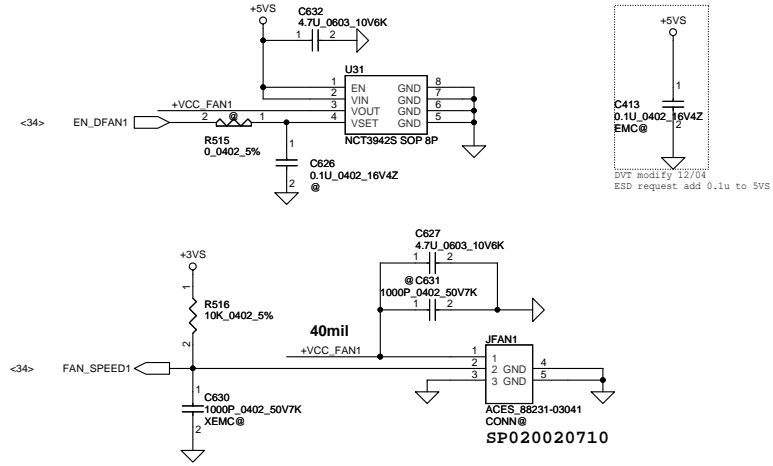


TPM Board for BA50

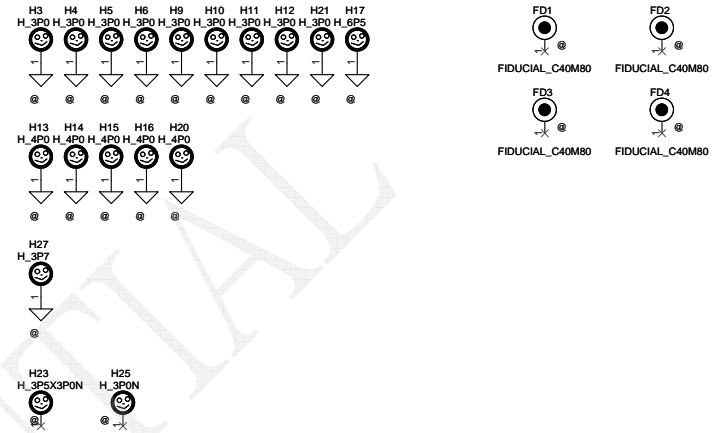


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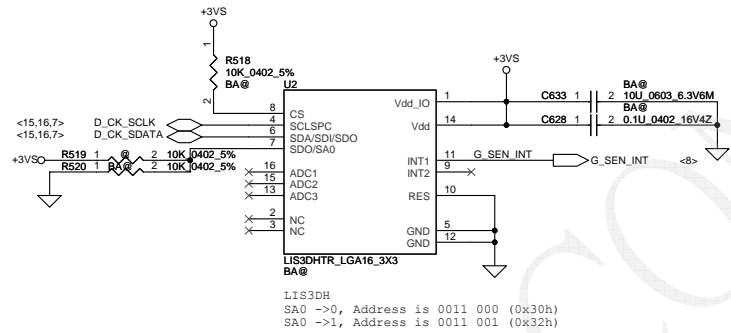
FAN1 Conn



Screw Hole

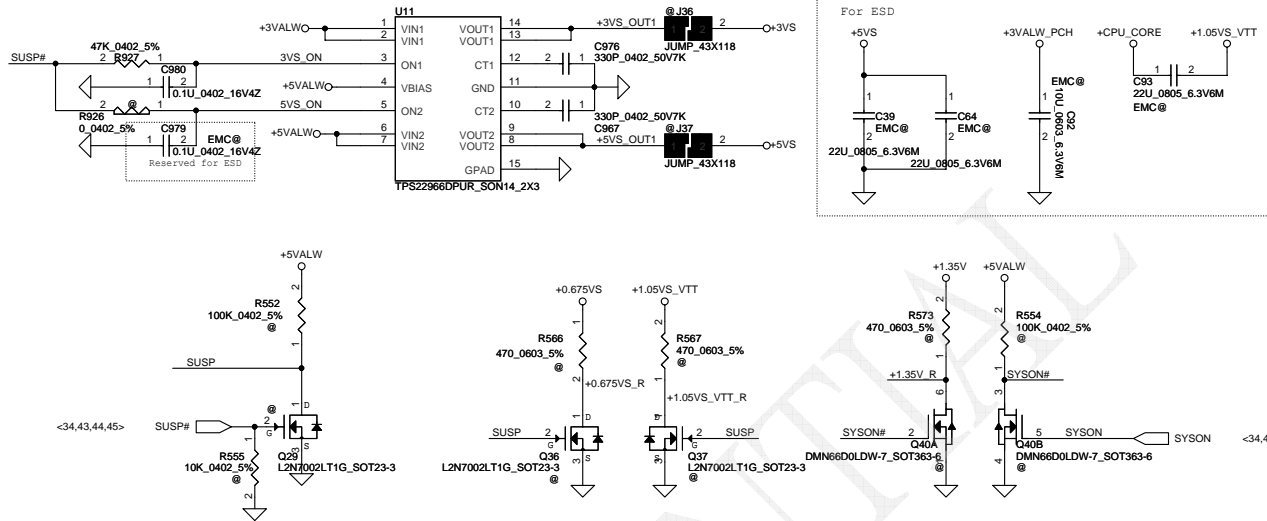


G-Sensor for BA50

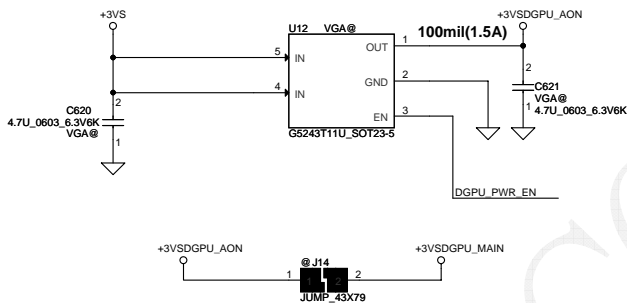


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Customer				Document Number	
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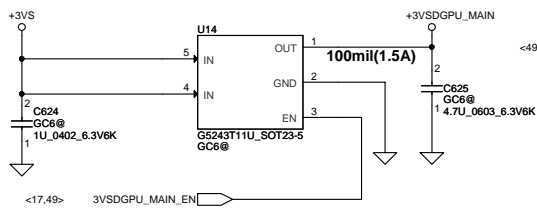
DC & VGA Interface



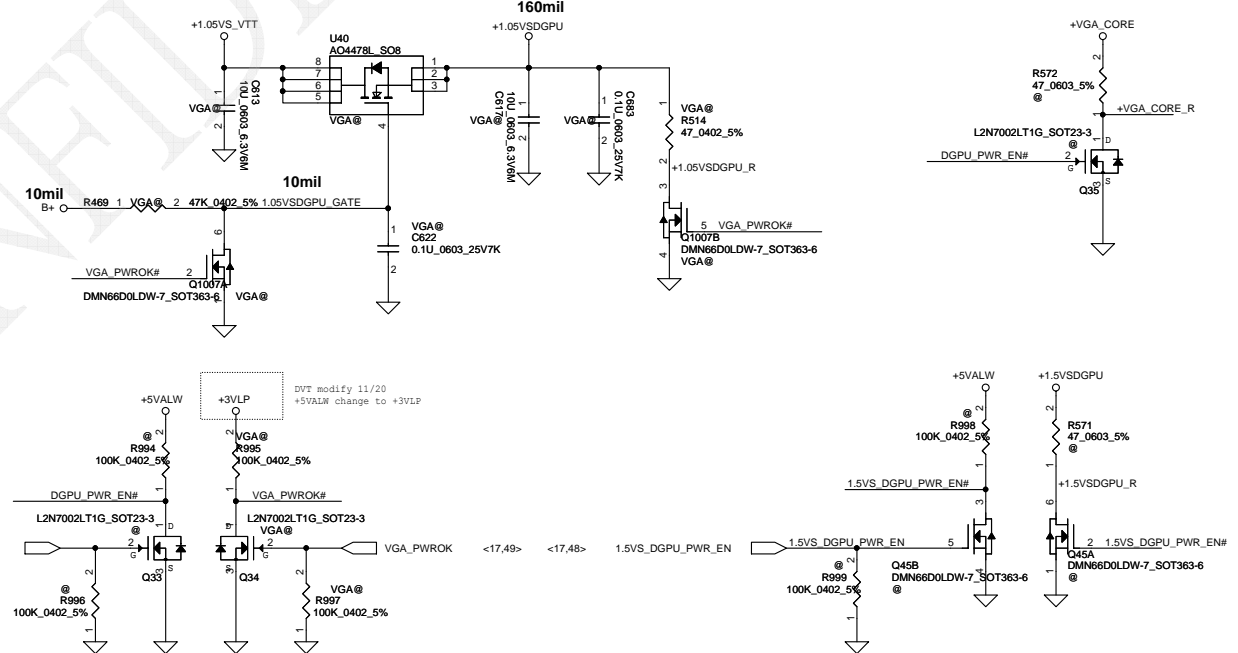
+3VS to +3VSDGPU_AON for GPU



+3VS to +3VSDGPU_MAIN for GC6-2.0

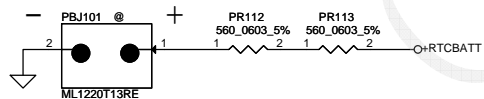
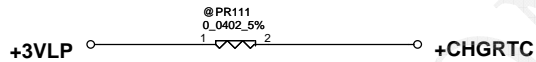
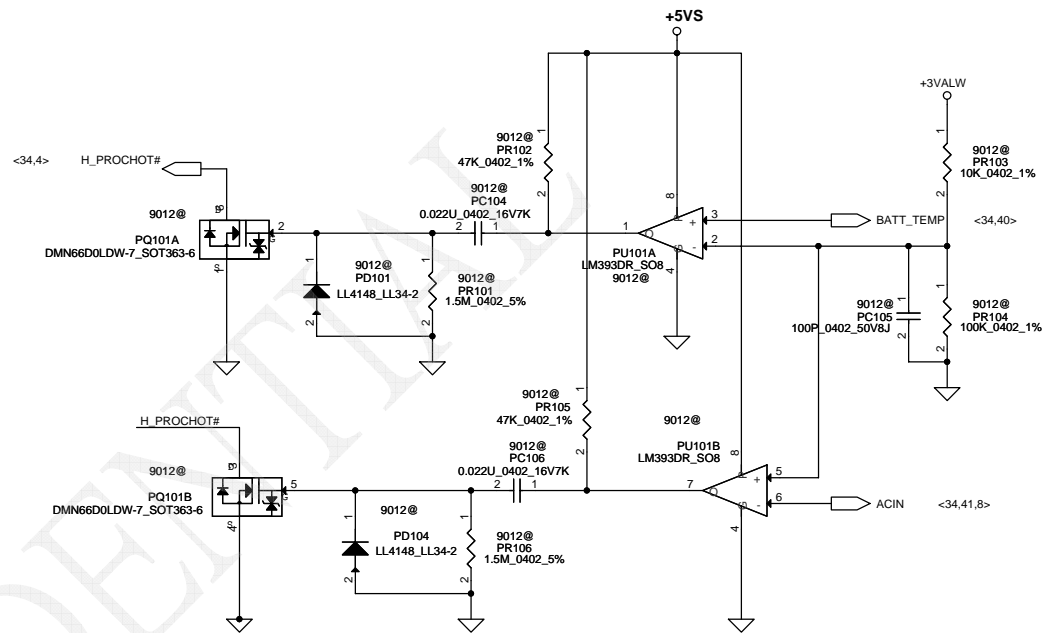
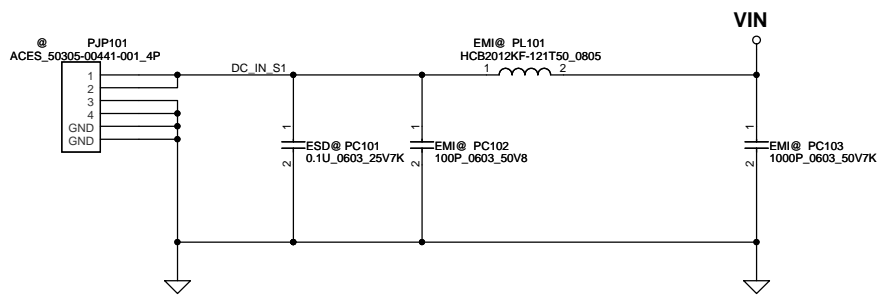


+1.05VS_VTT to +1.05VSDGPU

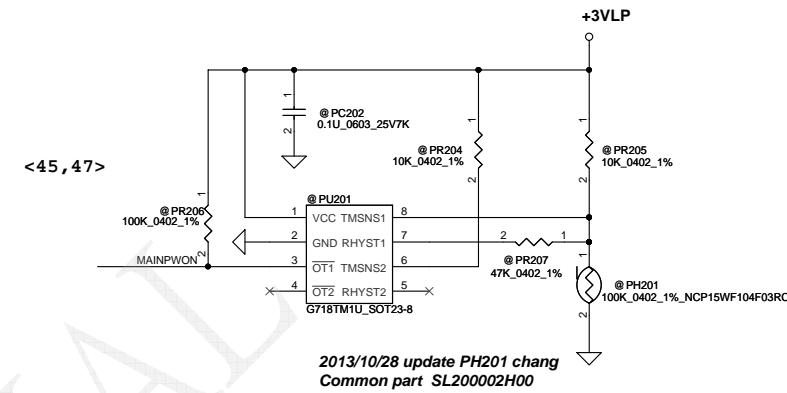
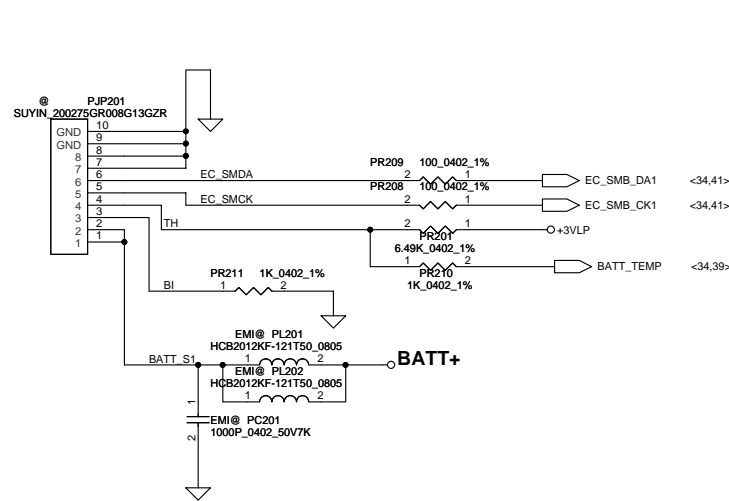


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3VSDGPU_MAIN_EN From GPU



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---Battery_pin define---

- PIN1 GND
- PIN2 GND
- PIN3 SMD
- PIN4 SMC
- PIN5 TS
- PIN6 B/I
- PIN7 Batt+
- PIN8 Batt+

---Battery Con_pin define---

- PIN8 GND
- PIN7 GND
- PIN6 SMD
- PIN5 SMC
- PIN4 TS
- PIN3 B/I
- PIN2 Batt+
- PIN1 Batt+

	For KB9012 OTP	For KB9022 OTP
92	1.2V	1.0V
56	1.2V	1.0V
PR216	22.6K ohm	32.4K ohm
PR227	26.1K ohm	30K ohm

2013/10/14 update

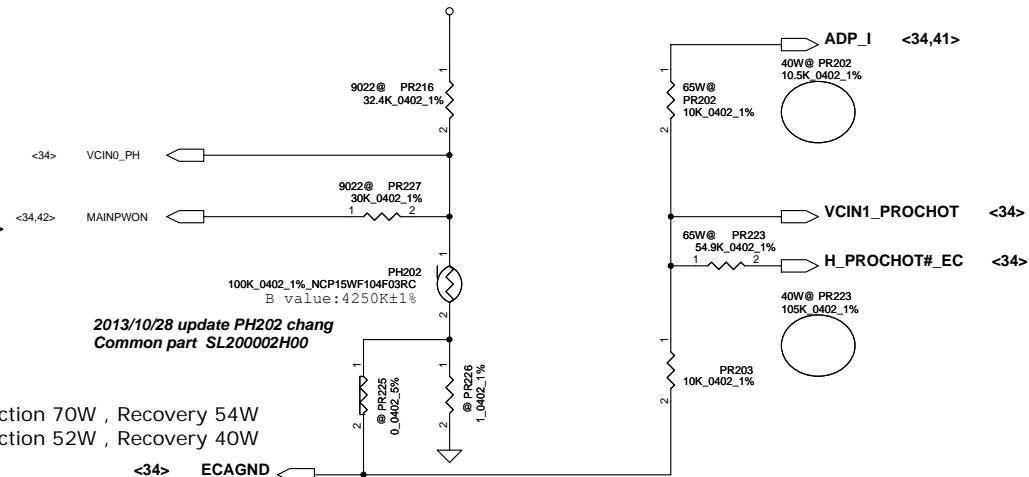
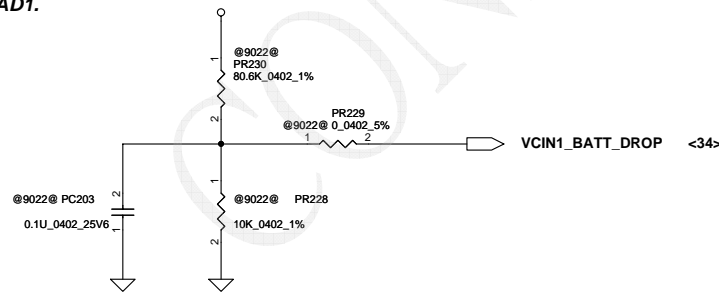
For KB9022 sense 20mΩ	Active	Recovery
40W	52W, 0.51V	40W, 0.51V
65W	84.5W, 0.82V	65W, 0.82V

PH201 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C +EC_VCCA

2013/10/02

Add for ENE9022 Battery Voltage drop detection. B+
Connect to ENE9022 pin64 AD1.

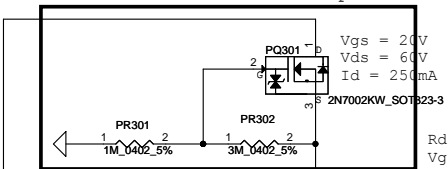
Battery is 3-cell design.
B+=9V



For 65W adapter==>action 70W , Recovery 54W
For 40W adapter==>action 52W , Recovery 40W

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				BATTERY CONN / OTP	
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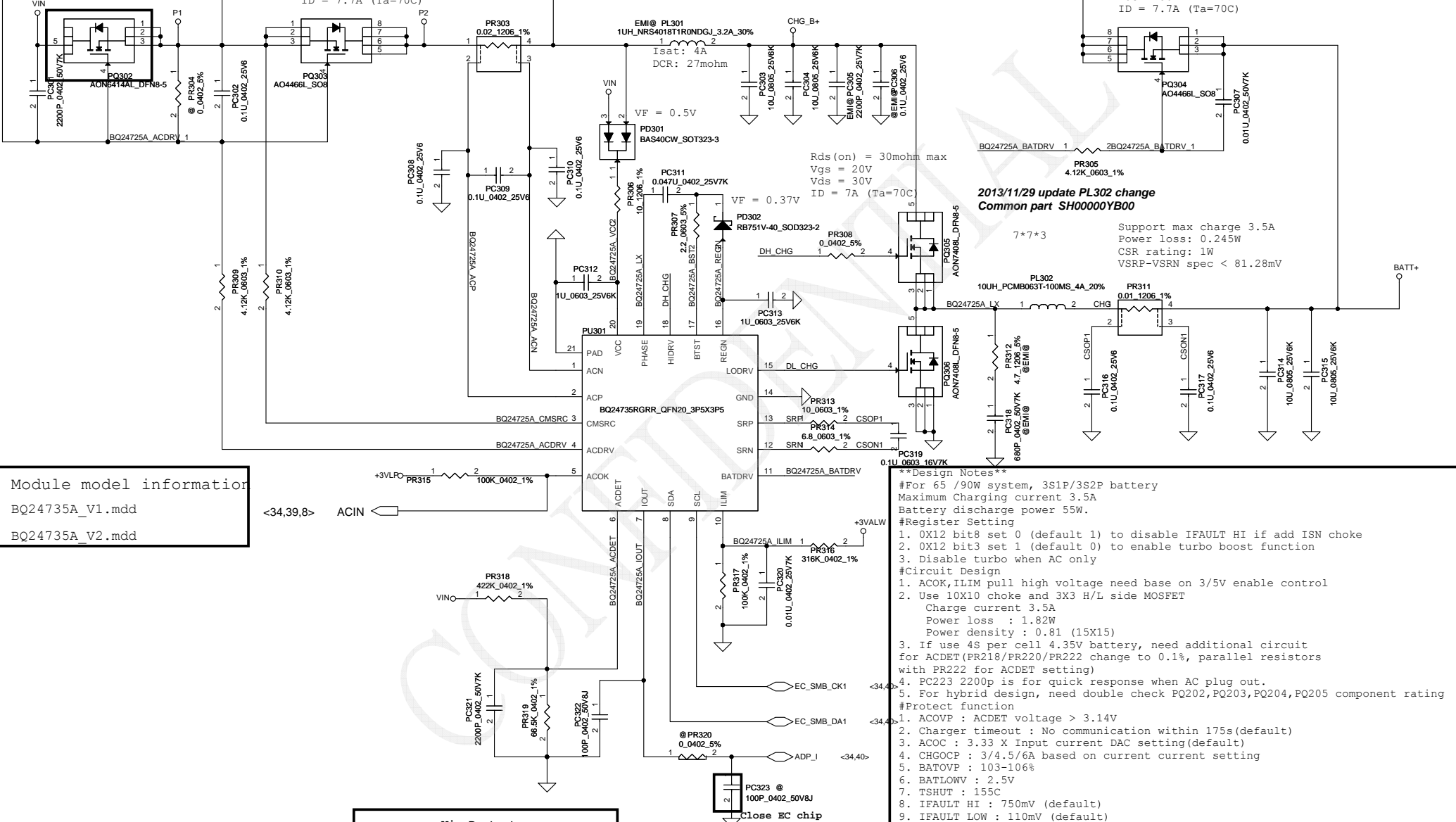
Protection for reverse input



2013/10/14
PR303 10m ohm chang -->20m ohm
SD0000S120

Rds(on) typ = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)

Rds(on) = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)



Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+107)/20/0.02
= 3.986 A

****Design Notes****

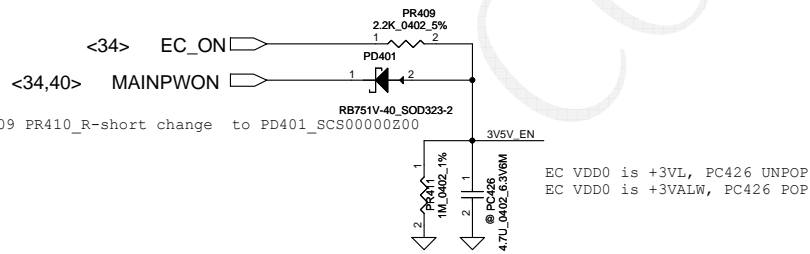
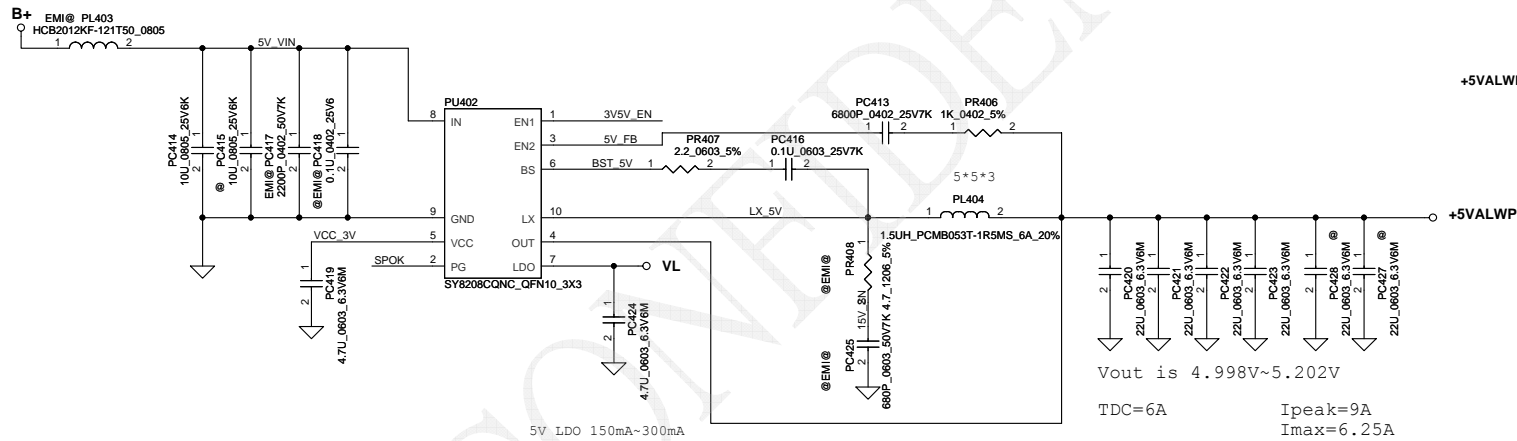
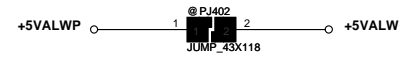
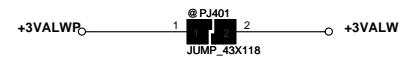
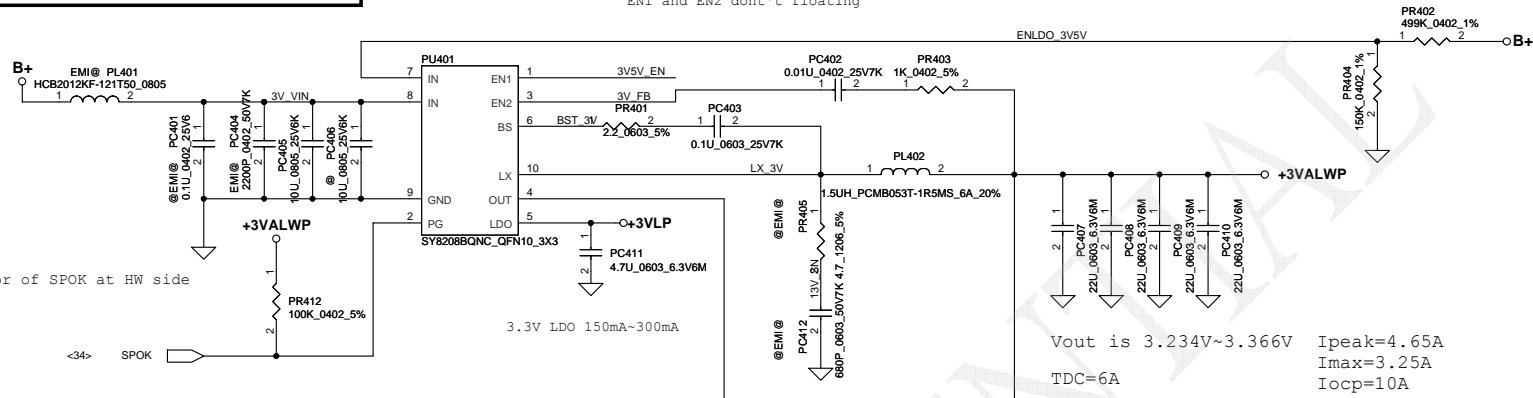
- #For 65 /90W system, 3S1P/3S2P battery
- Maximum Charging current 3.5A
- Battery discharge power 55W.
- #Register Setting
 - 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
 - 0X12 bit3 set 1 (default 0) to enable turbo boost function
 - Disable turbo when AC only
- #Circuit Design
 - ACOK,ILIM pull high voltage need base on 3/5V enable control
 - Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)
 - If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
 - PC223 2200p is for quick response when AC plug out.
 - For hybrid design, need double check PQ202, PQ203, PQ204, PQ205 component rating
- #Protect function
 - ACOVF : ACDET voltage > 3.14V
 - Charger timeout : No communication within 175s(default)
 - ACOC : 3.33 X Input current DAC setting(default)
 - CHGOCP : 3/4.5/6A based on current current setting
 - BATOVF : 103-106%
 - BATLOWV : 2.5V
 - TSHUT : 155C
 - IFault HI : 750mV (default)
 - IFault LOW : 110mV (default)

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Module model information

SY8208B_V2.mdd
SY8208C_V2.mdd

EN1 and EN2 dont't floating

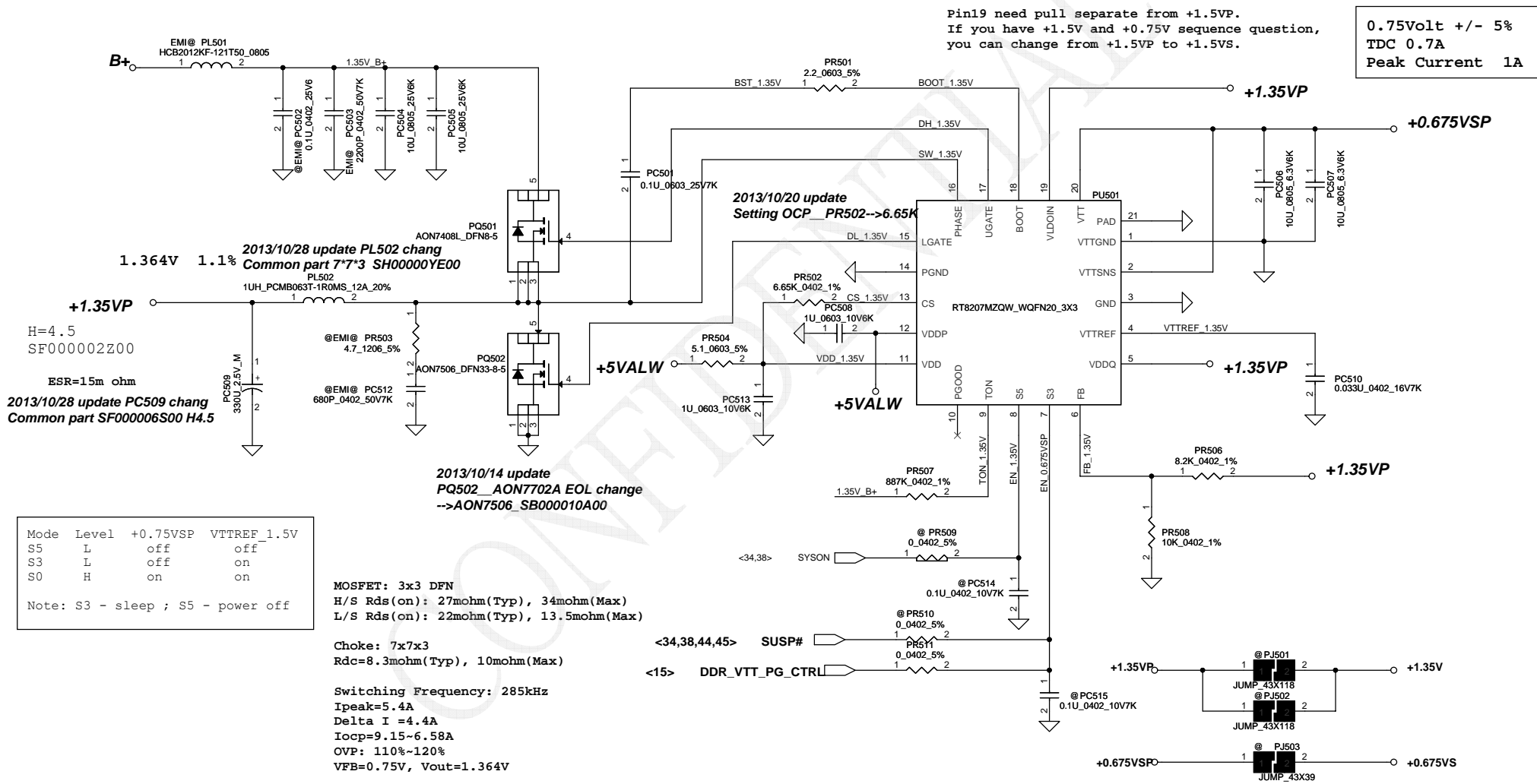


20131209 PR410_R-short change to PD401_SCS00000200

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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer



Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A

2013/10/28 update PL502 chang
Common part 7*7*3 SH00000YE00

2013/10/20 update
Setting OCP_PR502-->6.65K

2013/10/14 update
PQ502_AON7702A EOL change
-->AON7506_SB000010A00

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
L/S Rds(on): 22mohm(Typ), 13.5mohm(Max)

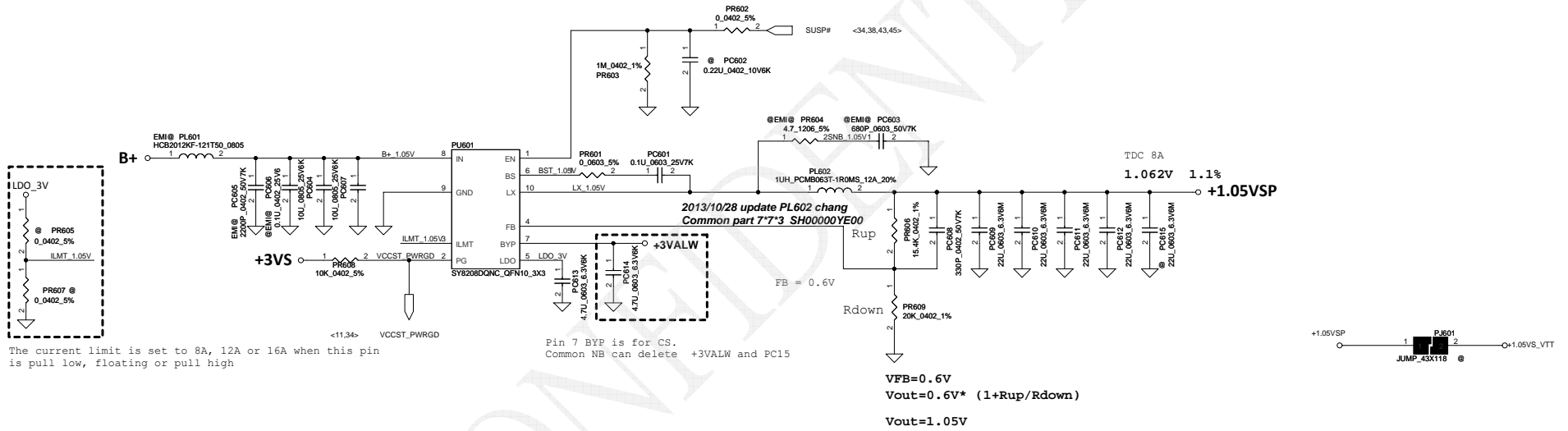
Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=5.4A
Delta I = 4.4A
Iocp=9.15~6.58A
OVP: 110%~120%
VFB=0.75V, Vout=1.364V

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Module model information
SY8208D_V1.mdd

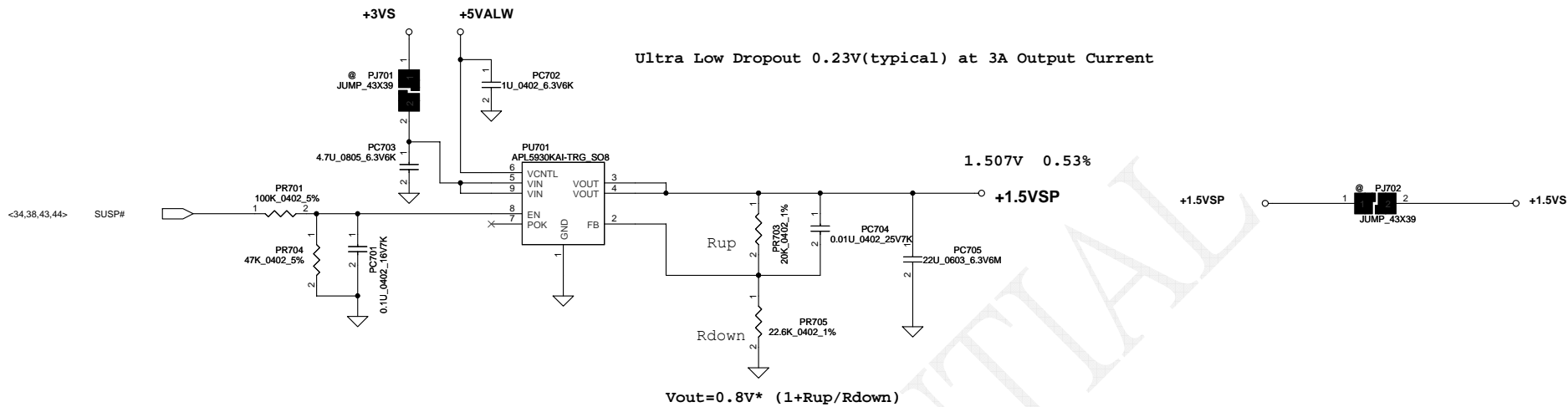
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

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Ultra Low Dropout 0.23V(typical) at 3A Output Current

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				Size	
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Module model information:
ISL95813 (for 15W & 28W CPU)

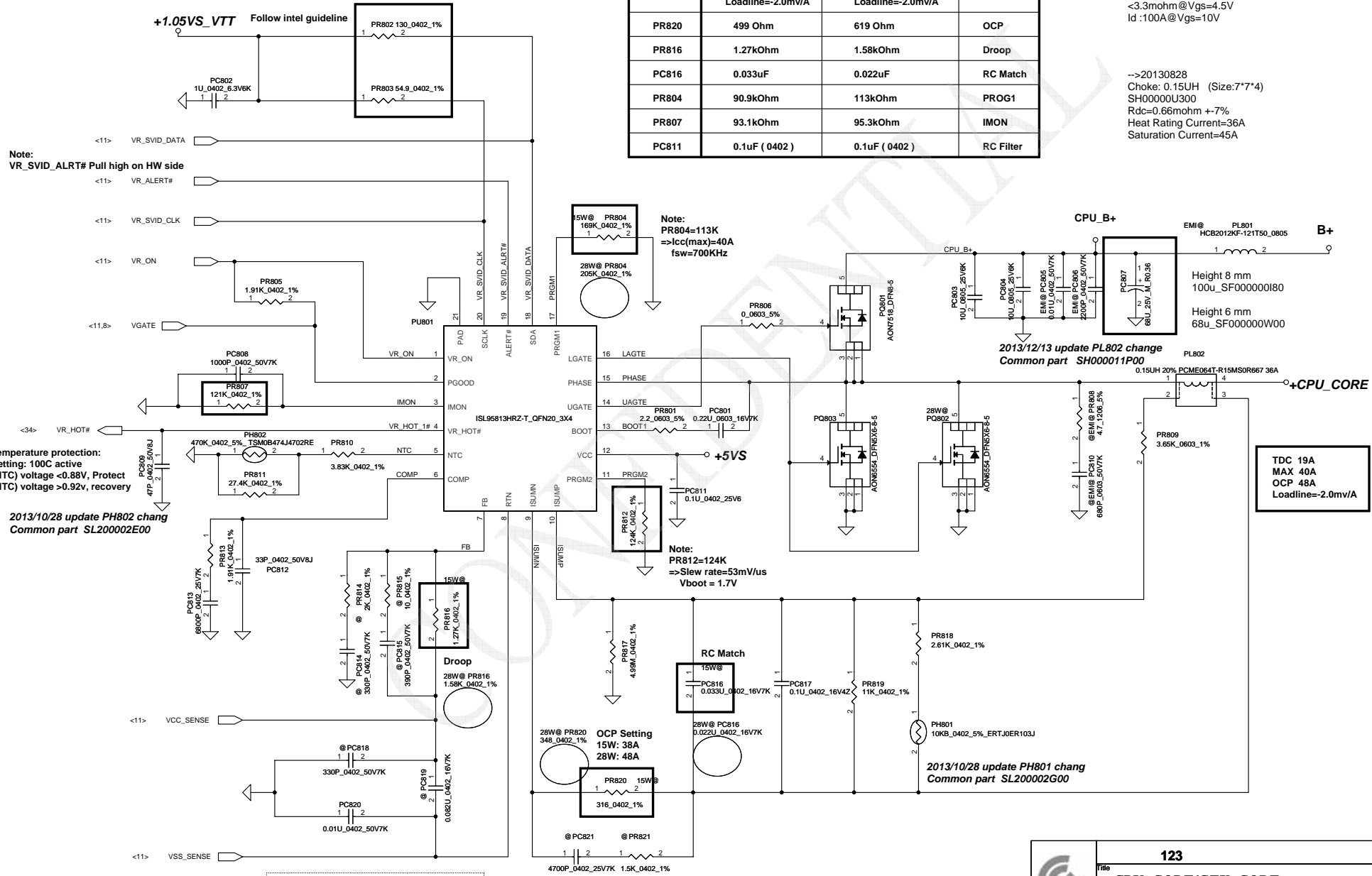
Base on BDW PDDG Rev_0_73

Location	15W	28W	Note
	TDC 14A		
MAX 32A		MAX 40A	
OCF 38.4A		OCF 48A	
Loadline=-2.0mv/A		Loadline=-2.0mv/A	
PR820	499 Ohm	619 Ohm	OCF
PR816	1.27kOhm	1.58kOhm	Droop
PC816	0.033uF	0.022uF	RC Match
PR804	90.9kOhm	113kOhm	PROG1
PR807	93.1kOhm	95.3kOhm	IMON
PC811	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

-->20130828
Choke: 0.15UH (Size:7*7*4)
SH00000U300
Rdc=0.66mohm +-7%
Heat Rating Current=36A
Saturation Current=45A



Note:
VR_SVID_ALERT# Pull high on HW side

Note:
PR804=113K
=>Icc(max)=40A
fsw=700KHz

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92V, recovery

2013/10/28 update PH802 chang
Common part SL200002E00

Droop
28W@ PR816
1.58K_0402_1%

Note:
PR812=124K
=>Slew rate=53mV/us
Vboot = 1.7V

RC Match
15W@
PC816
0.033U_0402_16V7K

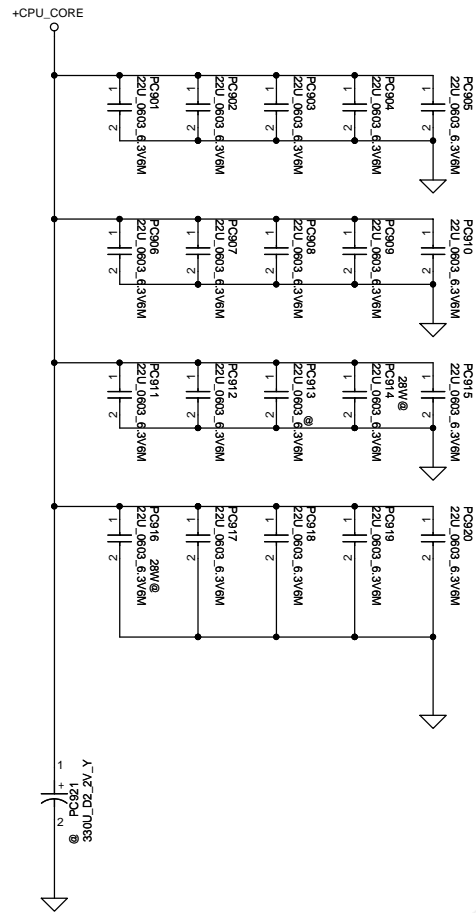
OCF Setting
15W: 38A
28W: 48A

2013/10/28 update PH801 chang
Common part SL200002G00

TDC 19A
MAX 40A
OCF 48A
Loadline=-2.0mv/A

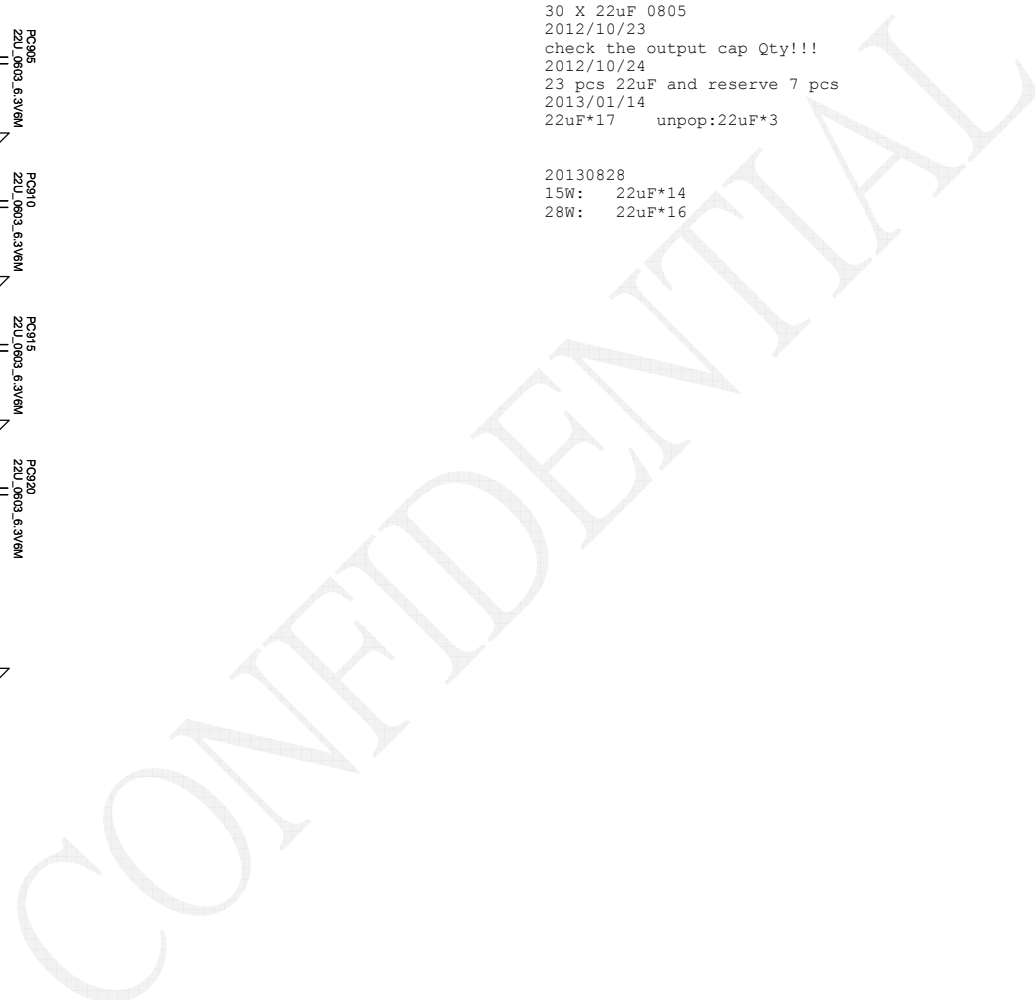
Local sense put on HW site

PWR Rule
需確認最新SPEC.
Modify 8/6.



30 X 22uF 0805
 2012/10/23
 check the output cap Qty!!!
 2012/10/24
 23 pcs 22uF and reserve 7 pcs
 2013/01/14
 22uF*17 unpop:22uF*3

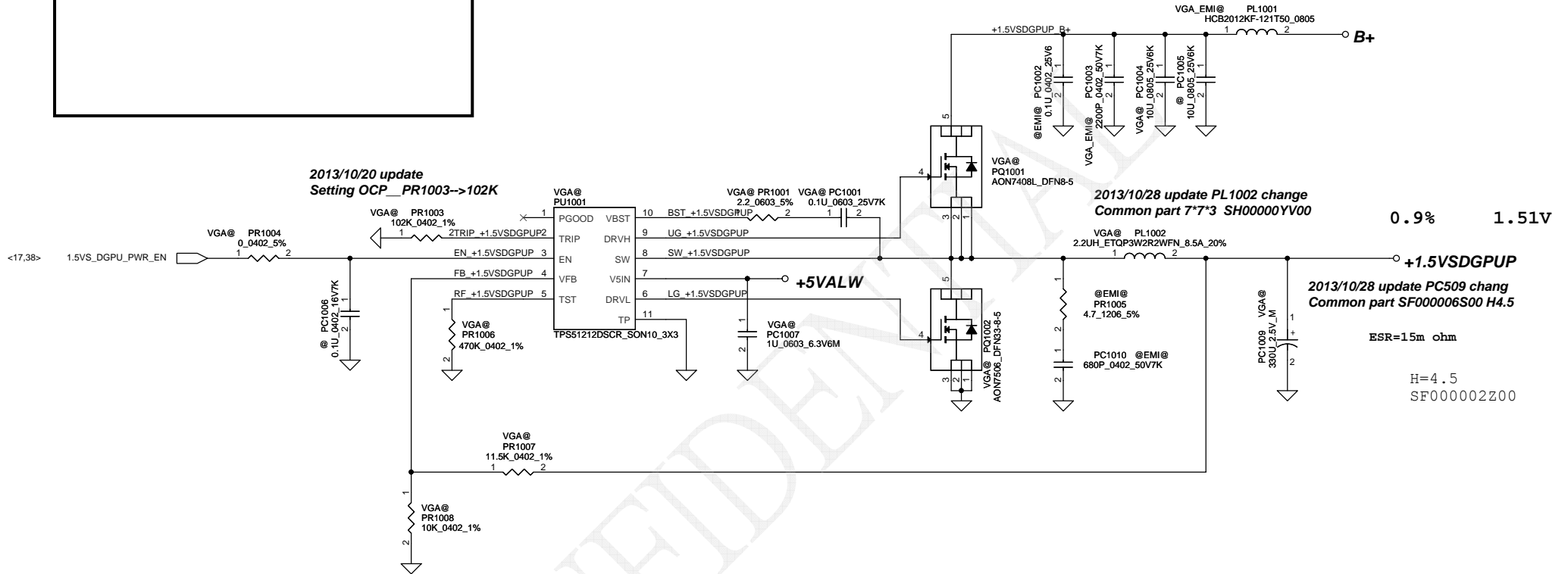
20130828
 15W: 22uF*14
 28W: 22uF*16



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Module model information

TPS51212_V1.mdd for Single layer
 TPS51212_V2.mdd for Dual layer



2013/10/20 update
 Setting OCP_PR1003-->102K

2013/10/28 update PL1002 change
 Common part 7*7*3 SH00000YV00

2013/10/28 update PC509 chang
 Common part SF000006S00 H4.5

0.9% 1.51V

ESR=15m ohm

H=4.5
 SF000002Z00

+1.2V

Switching Frequency: 290kHz
 I_{max}=8A
 OCP~10.5A
 OVP: 120%-130%
 VFB=0.704V, V_{out}=1.207V

+1.05V

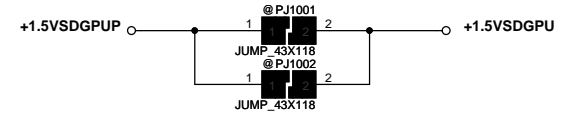
Switching Frequency: 290kHz
 I_{max}=5.4A
 I_{peak}=6.5A
 I_{ocp}=7.8A
 OVP: 120%-130%
 VFB=0.704V, V_{out}=1.055V

MOSFET: 3x3 DFN
 H/S R_{ds(on)}: 27mohm(Typ), 34mohm(Max)
 L/S R_{ds(on)}: 22mohm(Typ), 13.5mohm(Max)

Choke: 7x7x3
 R_{dc}=15.5mohm +/-15%

Switching Frequency: 290kHz
 I_{peak}=10A
 Delta I =2.16A
 I_{ocp}=12.14~16.67A
 OVP: 120%-130%
 VFB=0.704V, V_{out}=1.51V

Vout	PR1007	PR1008	PR1003
+1.5V	11.5k	10k	
+1.35V	9.31k	10k	
+1.2V	7.15k	10k	105K
+1.05V	4.99k	10k	93.1k



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Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

Vboot=Vvref*(Rref1+Rref2+Rboot)
 Rt=Rrefadj/(Rboot+Rref2)
 Vmin=Vvref*(Rref2/(Rref2+Rboot))*[Rt/(Rref1+Rt)]
 Vmax=Vvref*Rref2/((Rref1//Rrefadj)+Rboot+Rref2)
 Vout=Vmin+N*Vstep
 Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec	Config B	Config C	Config D
Vmin	0.6V	0.65V	0.9V
Vmax	1.2V	1.15V	1.15V
Vboot	0.9V	0.9V	1.028V
Voltage step	6.25mV	25mV	12.5mV
N of Voltage level	96	20	20
Rrefadj	PR1204 20K	39K	27K
Rref1	PR1204 20K	30K	7.5K
Rboot	PR1205 2K	3K	0
Rref2-PR1209	PR1209 18K	24K	6.2K
+PR1212	PR1212 0	3K	1.74K
C	PC1209 2.7nf	1.8nf	5.6nf

Current Limit setting
 Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA
 $I_{ripple} = (19.0 - 9.0) * 0.9 / (304.89KHz * 0.36uF * 19) = 7.811A$
 OCP=54A/2=27A per phase
 Ivalley=27A-7.811A/2=23.1A

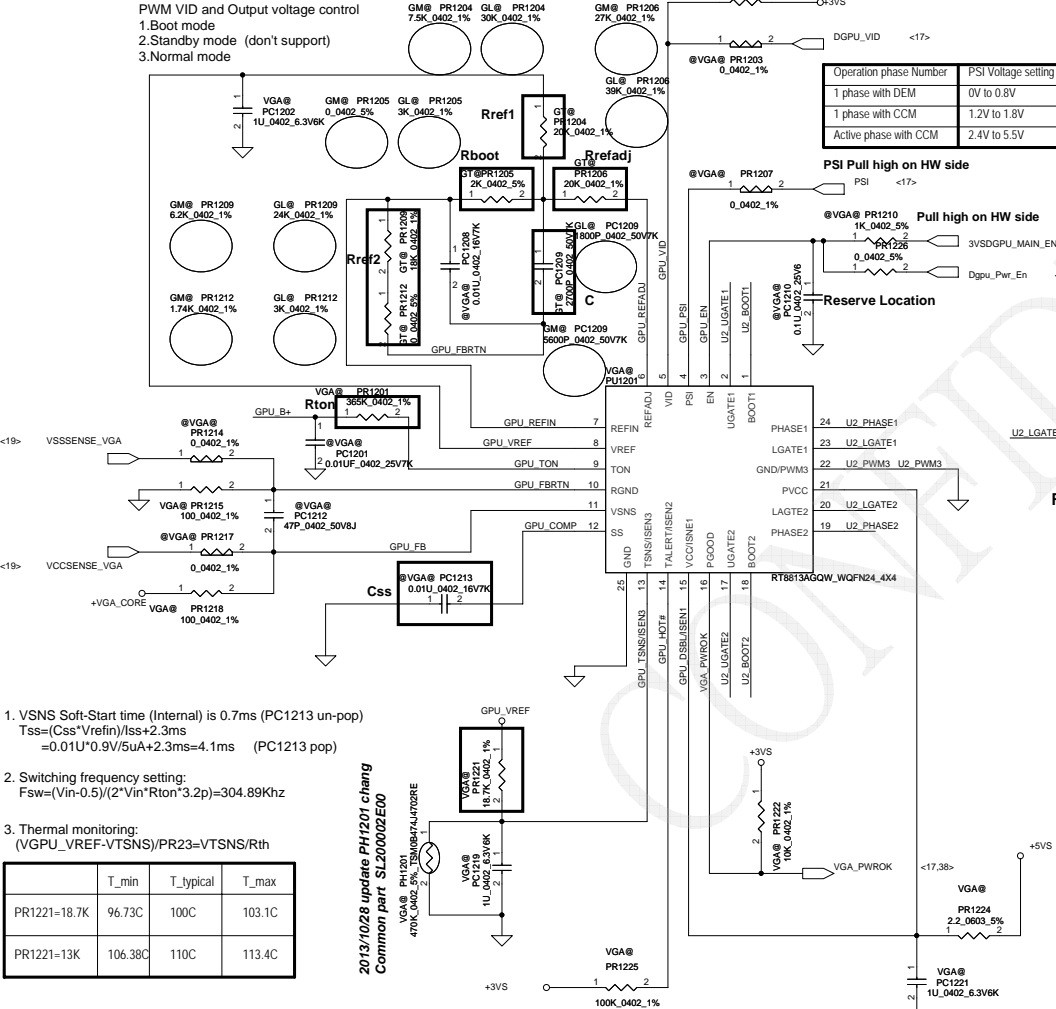
H-side MOS:AON6552 L-side MOS:AON6554
 Rds(on): 3.2mohm @ Vgs=10V
 5.6mohm @ Vgs=10V
 6.7mohm @ Vgs=4.5V
 3-3.8mohm @ Vgs=4.5V
 Id :20A @ Ta=25 degC Id :85A @ Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
 Rdc=0.97mohm +5%
 Heat Rating Current=34A
 Saturation Current=25A

C=3*330uF (9mohm)=990uF
 Vrripple=ripple*ESR(min)=7.811A*3mohm=23.4mV

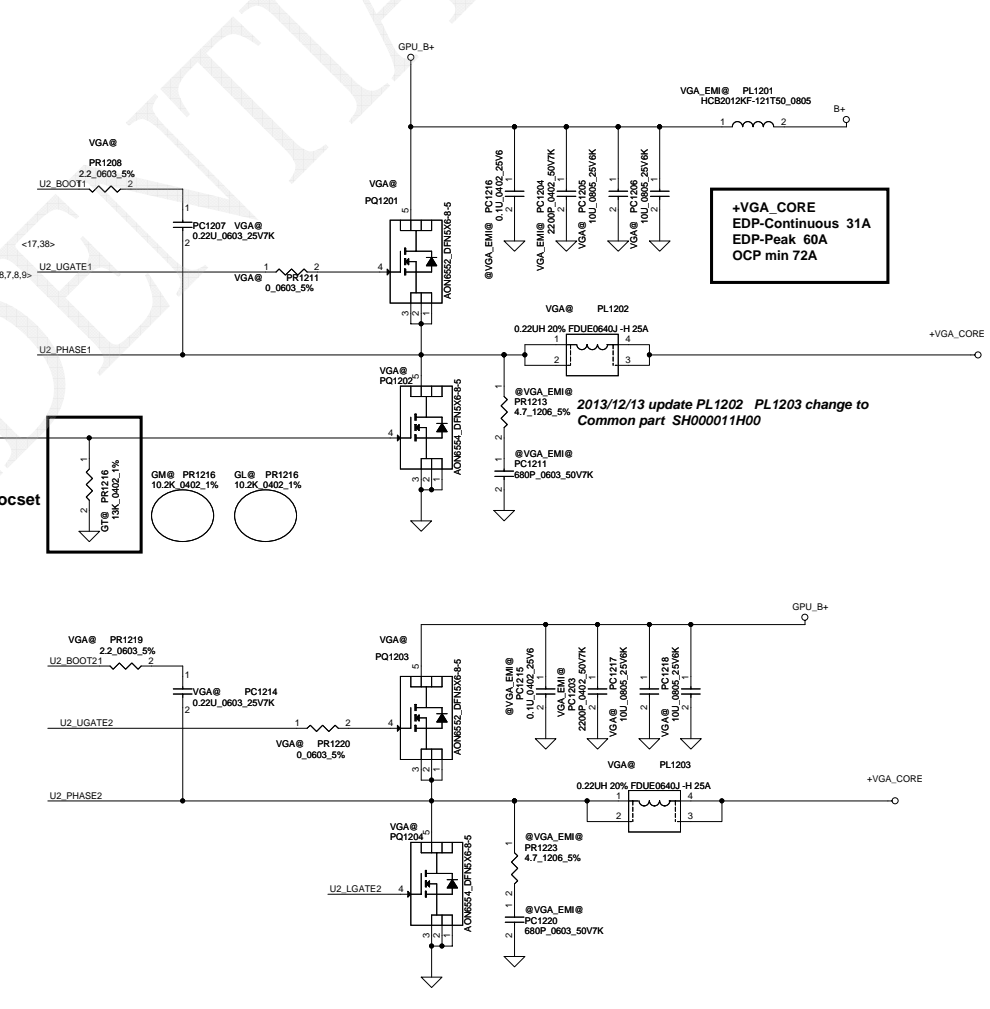
Different VGA Chip (different EDP-Max Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@

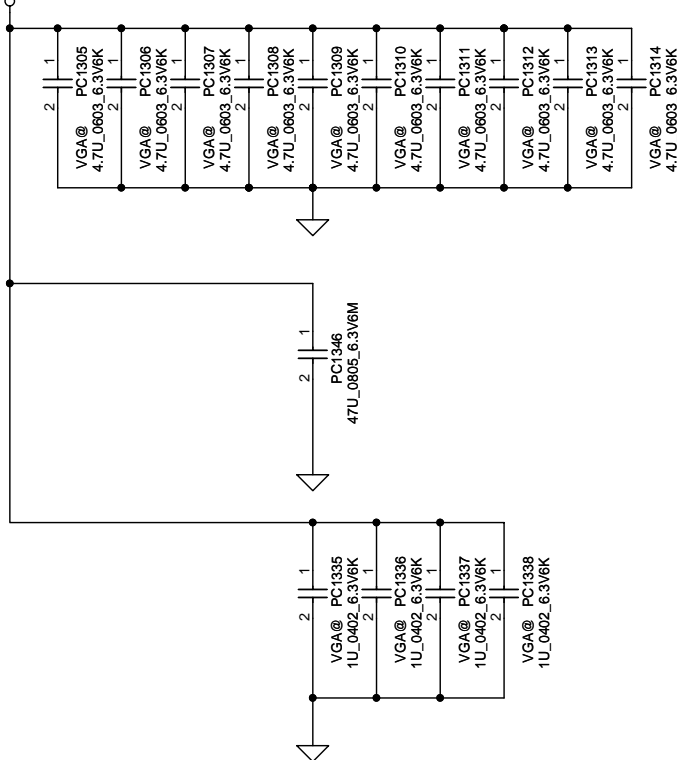


- VSNS Soft-Start time (Internal) is 0.7ms (PC1213 un-pop)
 $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} + 2.3ms = 0.01uF * 0.9V / 5uA + 2.3ms = 4.1ms$ (PC1213 pop)
- Switching frequency setting:
 $f_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p) = 304.89KHz$
- Thermal monitoring:
 $(V_{GPU_VREF} - V_{TSNS}) / PR23 = V_{TSNS} / R_{th}$

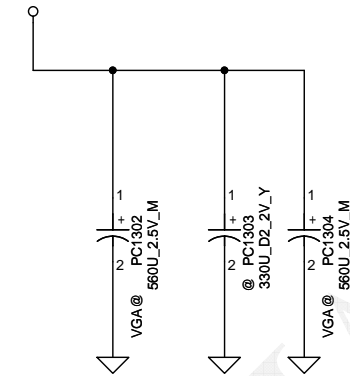
	T_min	T_typical	T_max
PR1221=18.7K	96.73C	100C	103.1C
PR1221=13K	106.38C	110C	113.4C



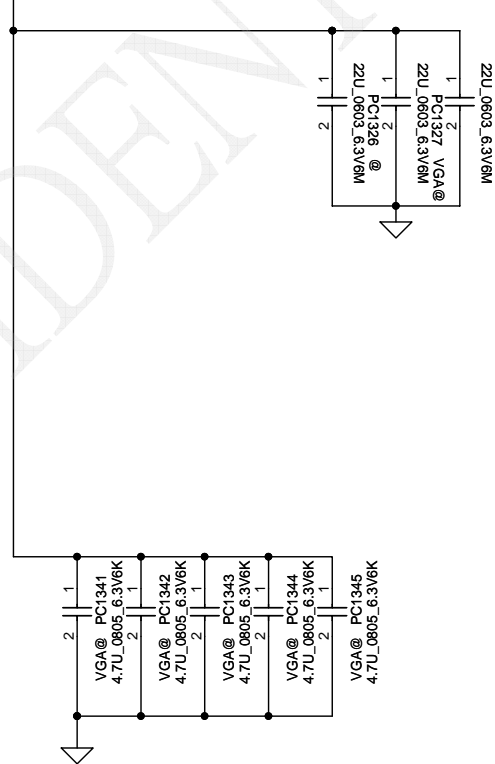
+VGA_CORE Under VGA Core



+VGA_CORE



+VGA_CORE
Near VGA Core



N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs(2PCS unpop)
4.7uF_0805_5pcs

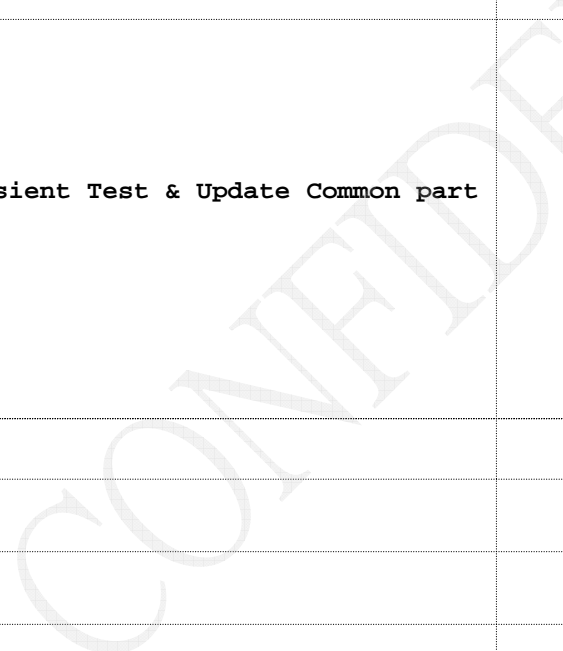
N15x2013/10/07
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	design update		P42 P44 P44 P46 P41	Add unpop PC428 PC427,22U_0603_6.3V6M_SE00000M000 Add unpop PC615,22U_0603_6.3V6M_SE00000M000 PC609 PC610,SE00000PL00 change to 0603_6.3V6M_SE00000M000 PL801 PC807,Swap positions. PL302,10uH_10104_SH000005Z80 change to 10uH_773_SH00000YB00	11/29	EVT
2	design update	Update Common part	P42	PR410 R-short change to PD401_SCS00000Z00	12/09	EVT
3	design update	VGA 29*29 change to 23*23	P50	ADD 1pcs PC1346_47U_0805_6.3V6M_SE00000PL00 Del 5pcs PC1315~PC1319 4.7U_0603_6.3V6K_SE107475K80 Del 4pcs PC1331~PC1334 1U_0402_6.3V6K_SE000000K80 Del 6pcs PC1322~1325&PC1329~1330_22U_0603_6.3V6M_SE00000M000	12/10	EVT
4	design update	VGA 29*29 change to 23*23 (GM config SPEC change)		PR1206_39K_0402_1% change to 27K_0402_1%(GL->GM) PR1204_30K_0402_1% change to 7.5K_0402_1%(GL->GM) PR1205_3K_0402_1% change to 0_0402_5%(GL->GM) PR1209_24K_0402_1% change to 6.2K_0402_1%(GL->GM) PR1212_3K_0402_1% change to 1.74K_0402_1%(GL->GM) PC1209_1800P_0402_50V7K change to 5600P_0402_50V7K(GL->GM)	12/12	EVT
5	design update	CPU Transient Test & Update Common part		PR820_274_0402_SD00000EI80 change to 316_0402_SD000003480 PR814_2K_0402_1%_SD034200180 change to unpop PC814_330P_0402_50V7K_SE074331K80 change to unpop PR813_5.9K_0402_SD034590180 change to 1.91K_0402_SD000009080 PR807_95.3K_0402_SD034953280 change to 121K_0402_SD034121380 PR817_Unpop change to 4.99M_0402_SD00000VO00 PL1202 PL1203_SH00000O200_7*7*4 change to Common part SH000011H00 PL802_SH00000U300 change to Common part SH000011P00 PC909 PC918 PC919 22U_0603_SE00000M000 SMT PC914 22U_0603_SE00000M000,SMT change to 28W@ PC913 22U_0603_SE00000M000 ,SMT change to @ PR227_30.9K_0402_1%_SD034309280 change to 30K_0402_1%_SD034300280 PR1210 1K_0402_5%_SD028100180change to unpop PR1226 0_0402_5%_SD028000080change to SMT	12/12	EVT



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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Module Design	Module Design change 3/5V solution	3/5V	Un-pop PR1	11/13	DVT
2						
12						
13						
14						
15						
16						
17						

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	material update		P28	L2503/2504/2505 Change P/N from SM01000GA00 to SM01000FH00	11/12	DVT
2	material update		P34	L31/L32 Change P/N from SM010030010 to SM010009U00	11/12	DVT
3	design update		P35	Delete D24, ON/OFF change to ON/OFFBTN#	11/12	DVT
4	schematics update	for TP_INT# wake function	P35	TP PIN1 VCC Connect to +3VALW, add R462, R463@, pop D22, R633, R453	11/12	DVT
5	design change		P10	Change USB port 5 for TS/port 6 for CCD / port 7 for CR(USB)_FP	11/12	DVT
6	design update		P6	reserve RTCRST# to EC pin 27 for clear CMOS add R490, and Q52 reserve to EC_RTCRST#	11/12	DVT
7	design update	EC board ID	P34	Pop R503(100K), R506(12K)	11/15	DVT
8	material update		P36	change C2135, C2136 to 0603 size	11/15	DVT
9	material update		P33	L24, L25 form SM070003Y00 to SM070003K00	11/15	DVT
10	material update		P7	pop share rom	11/15	DVT
11	design update	Co-lay TS_I2C and LVDS EDID	P25	R415, R433 for LVDS EDID R438, R439 for TS I2C	11/15	DVT
12	design update	for LVDS EP mode SMBus2 change to SMBus3	P24	Add R491 reserve for RTD2132 EP_MODE	11/18	DVT
13	design update	for TP_INT# wake function	P34	GPI055 change to GPI013	11/18	DVT
14	design update	for GC62.0 function	P17	R2055 change to Pull high +3VSDGPU_AON	11/20	DVT
15	design update	for +1.05VS VTT leakage issue	P38	+5VALW change to +3VLP add level shift(Q2501), R2503, R2502, R2549 Del R930	11/20	DVT
16	design update	for IT 6513 leakage issue	P27	IT6513 change to use 3VS	11/26	DVT
17	material update	for TXC recommend	P6	C153, C2, C3 to 15PF, C2004, C2005, C2558, C2559 to 10PF	11/27	DVT
18	design update	for wake on LAN function	P29	add R2550 10K pull high to +3V_LAN , PCH side pull high reserve	12/04	DVT
19	design update	for ESD request	P37	add C413 0.1u to +5VS	12/04	DVT
20	design update	for EMI request	P33	add choke(L29,L30) and R(R456, R457,R462,R463) co-lay for USB/B comm	12/04	DVT
21	design update	for ESD request	P36	add R2149, R2150(SM01000NH00), C2140, C2142(680PF) D2008(SCA00001B00) change to SOT23 R2135,R2138 chagne to 60 ohm	12/10	DVT
22	material update			SW3 SN100007700 chagne to SN100000K00 C408, C486 SF000002Y00 change to SF000006R00 C18, C118 SF000002Z00 change to SF000006S00	12/13	DVT
23	design update		P37	reserve R2551 0 ohm +3VALW to +3VLAN reserve R2540 for disable PHY	12/20	DVT

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	design issue		P28	U2052, U2503 change power rail to +HDMI_5V_OUT	12/31	PVT
2	material update	PVT board ID	P34	R506 change to 15K	12/31	PVT
3	design update	modify DQS P/N pin	P18		01/08	PVT
4	schematics update					
5	design change					
6	design update					
7	design update					
8	material update					
9	material update					
10	material update					
11	design update					
12	design update					
13	design update					
14	design update					
15	design update					
16	design update					
17	material update					
18	design update					
19	design update					
20	design update					
21	design update					
22	material update					
23	design update					

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