

KSKAA

Bradford 10M/10MG

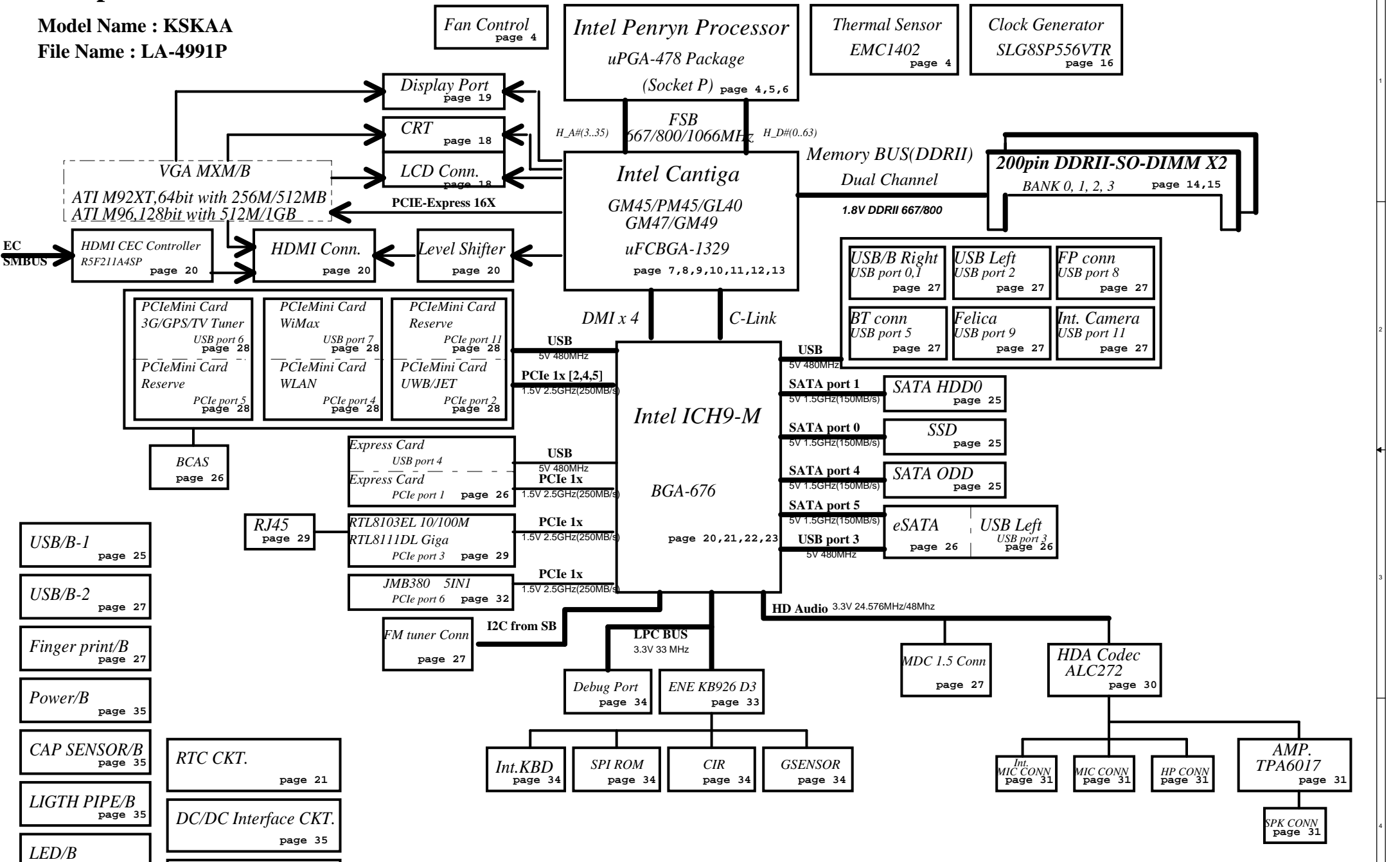
LA-4991P REV 1.0 Schematic

Intel Penryn/ Cantiga/ ICH9M
2008-05-07 Rev. 1.0

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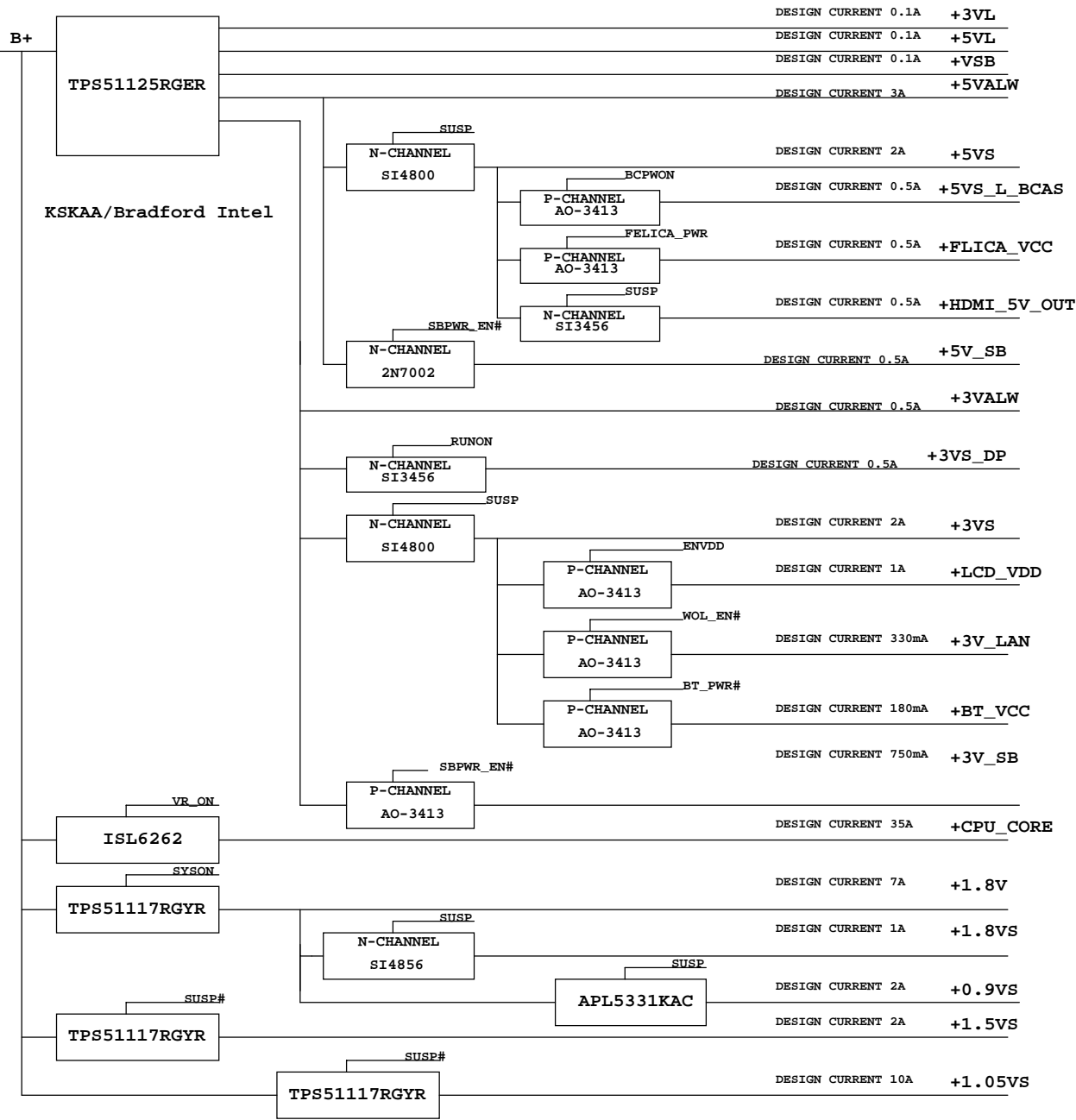
Model Name : KSKAA
File Name : LA-4991P



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DESIGN CURRENT 0.1A +3VL
 DESIGN CURRENT 0.1A +5VL
 DESIGN CURRENT 0.1A +VSB
 DESIGN CURRENT 3A +5VALW

DESIGN CURRENT 2A +5VS
 DESIGN CURRENT 0.5A +5VS_L_BCAS
 DESIGN CURRENT 0.5A +FLICA_VCC
 DESIGN CURRENT 0.5A +HDMI_5V_OUT
 DESIGN CURRENT 0.5A +5V_SB
 DESIGN CURRENT 0.5A +3VALW

DESIGN CURRENT 0.5A +3VS_DP
 DESIGN CURRENT 2A +3VS
 DESIGN CURRENT 1A +LCD_VDD
 DESIGN CURRENT 330mA +3V_LAN
 DESIGN CURRENT 180mA +BT_VCC
 DESIGN CURRENT 750mA +3V_SB

DESIGN CURRENT 35A +CPU_CORE
 DESIGN CURRENT 7A +1.8V
 DESIGN CURRENT 1A +1.8VS
 DESIGN CURRENT 2A +0.9VS
 DESIGN CURRENT 2A +1.5VS
 DESIGN CURRENT 10A +1.05VS

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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON		HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH		
S5 (Soft OFF)		LOW	LOW	LOW	LOW		
G3		LOW	LOW	LOW	LOW		

BTO Option Table

Function	HDMI			CRT	Display	LAN	
description	(Y)			(Q)	(Z)	(E)	(C)
explain	Intel(UMA)	ATI MXM/B	COMMON			10/100M	Giga
BTO	IHDMI@	NIHDMI@	HDMI@	H@	CRT@	DP@	8103EL@ 8111DL@

Function	3G SIM slot	Mini card	Felica	Finger printer	CIR	CAMERA & MIC	BLUE TOOTH
description	(3)	(D2)	(J)	(F)	(I)	(X)	(B)
explain		Two Cards				CAMERA	MIC
BTO	3G@	3G@	FLICA@	FP@	CIR@	CAM@	MIC@

External PCI Devices

EC SM Bus1 address

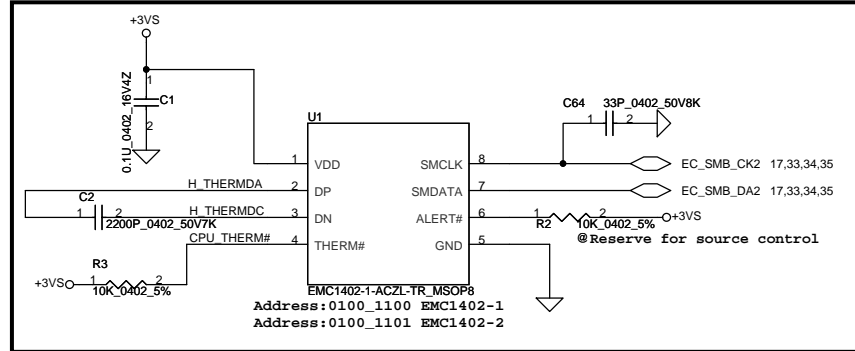
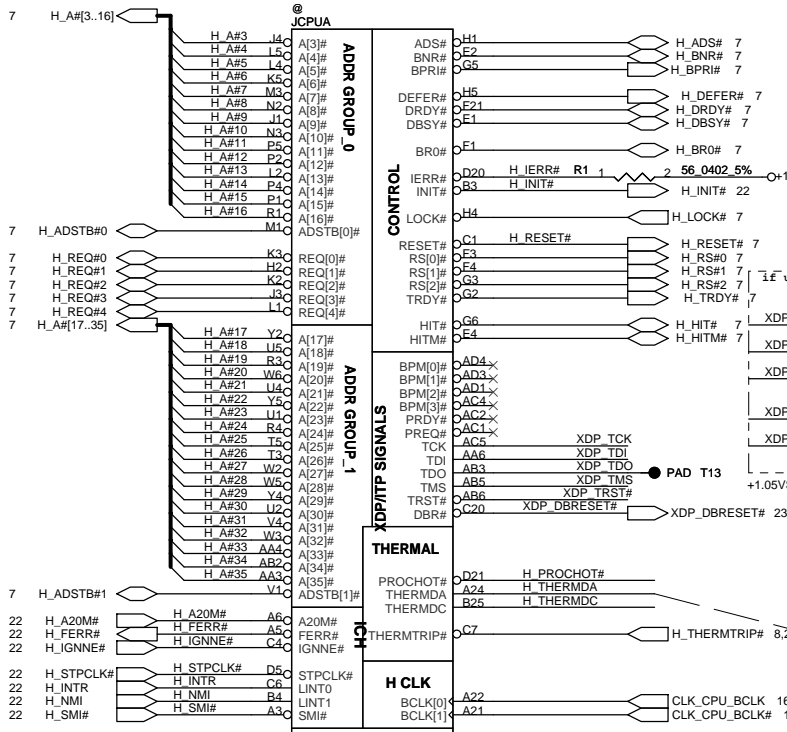
EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+5VL	Smart Battery	0001 01X b	+3VS	CPU THM Sen	
+5VL	HDMI-CEC	0011 010x b	+3VS	SMSC SMC1402	0100 110x b
+3VL	FUN/B (CAP Sensor)				

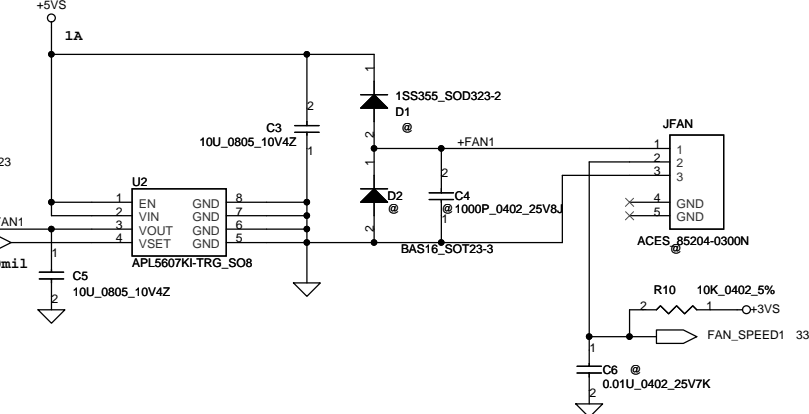
ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express	
+3VS	FM Module	

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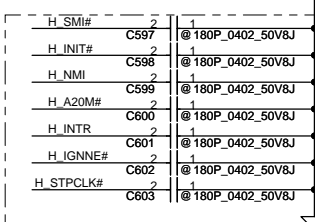
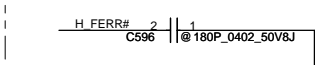
FAN Control Circuit



H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

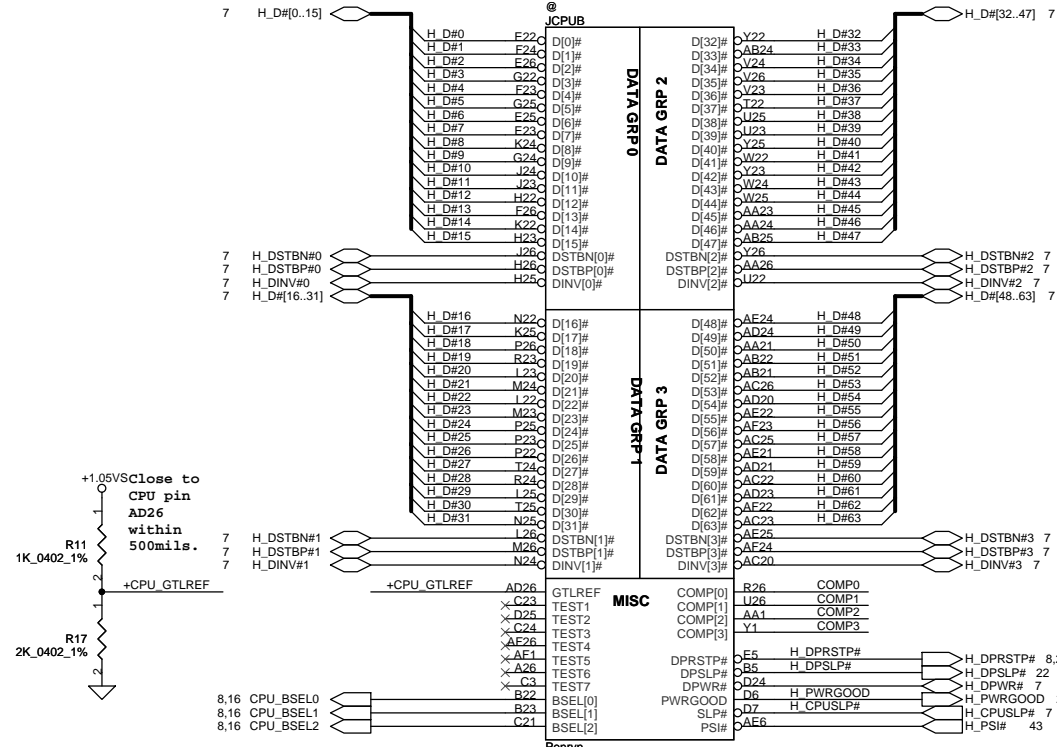
PROCHOT# PU: 680hm near CPU and MVP6. 560hm near CPU if no used.

Reserve for debug close to South Bridge

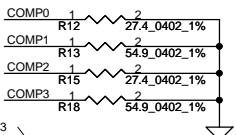


Reserve for debug close to CPU

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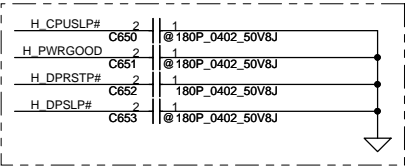
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



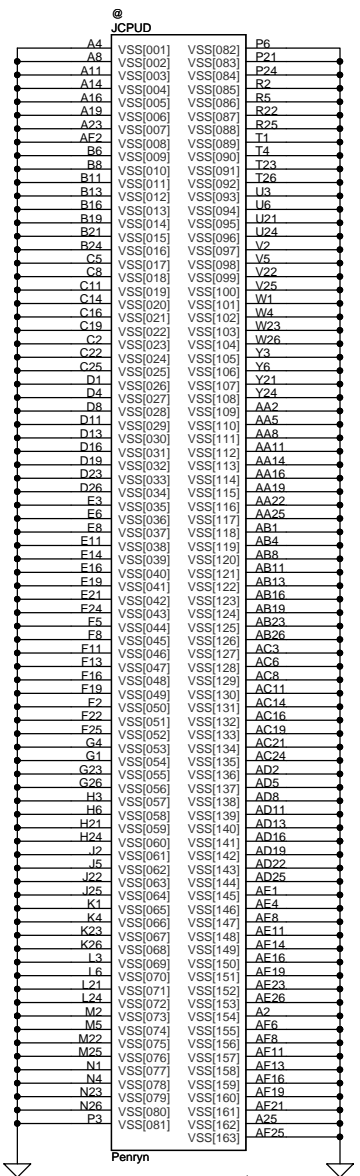
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

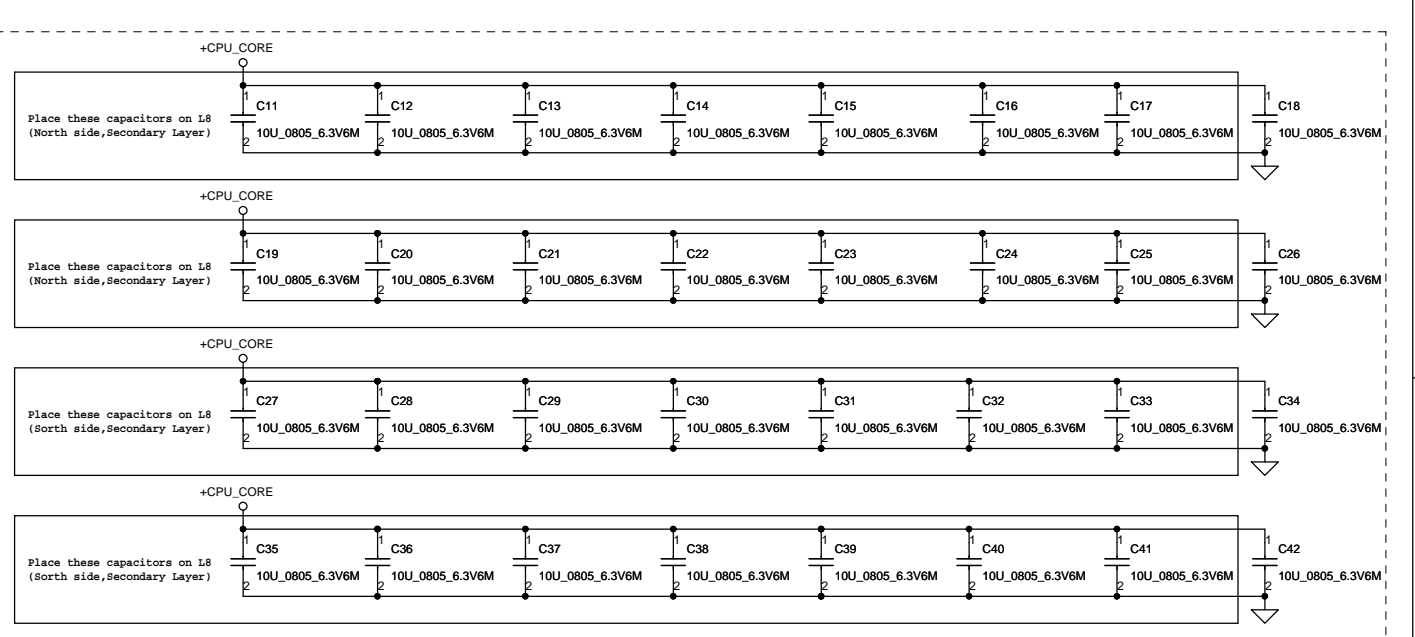
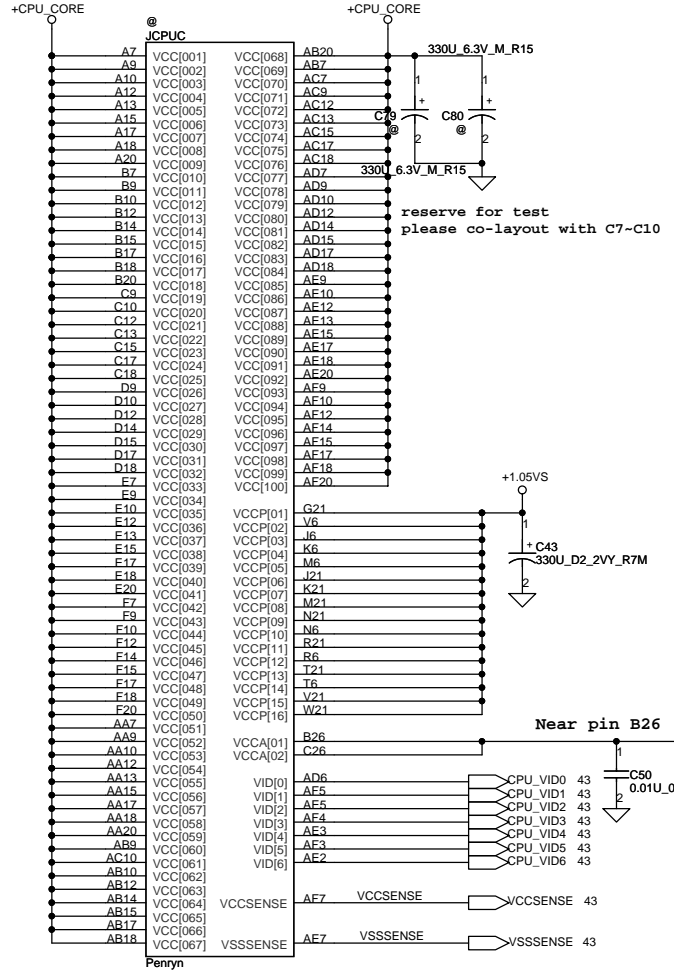
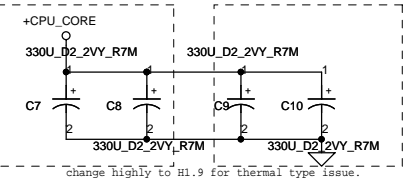


Reserve for debug close to CPU

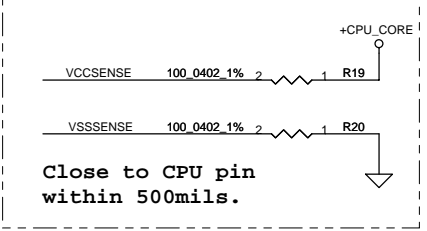
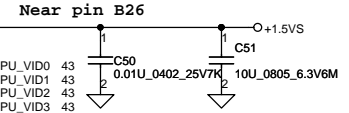
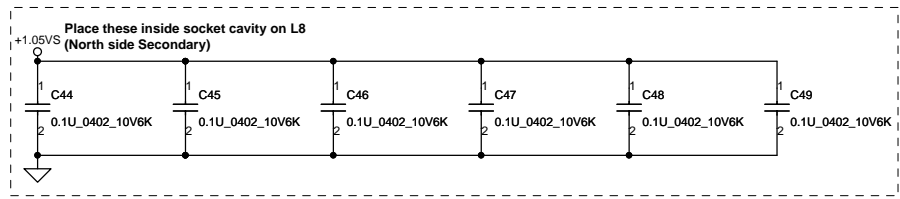


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



Mid Frequency Decoupling

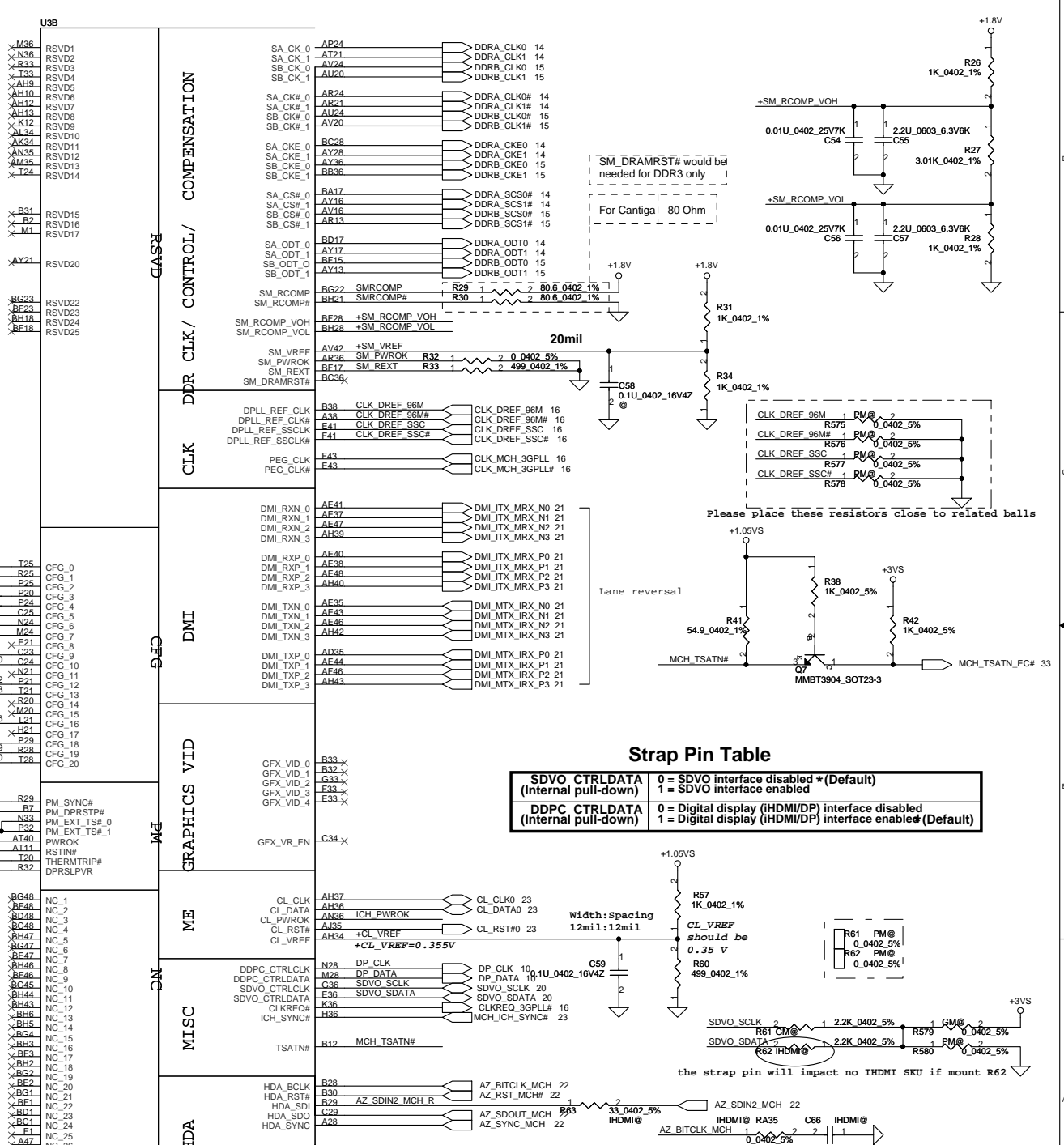
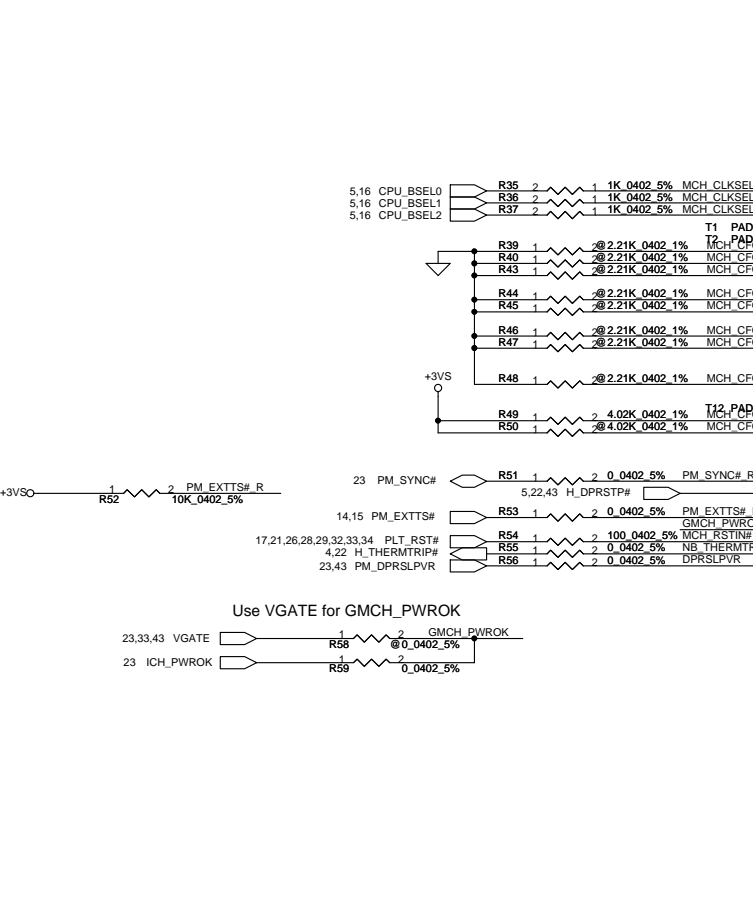


Length match within 25 mils.
The trace width/space/other is 14/7/25.

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Strap Pin Table

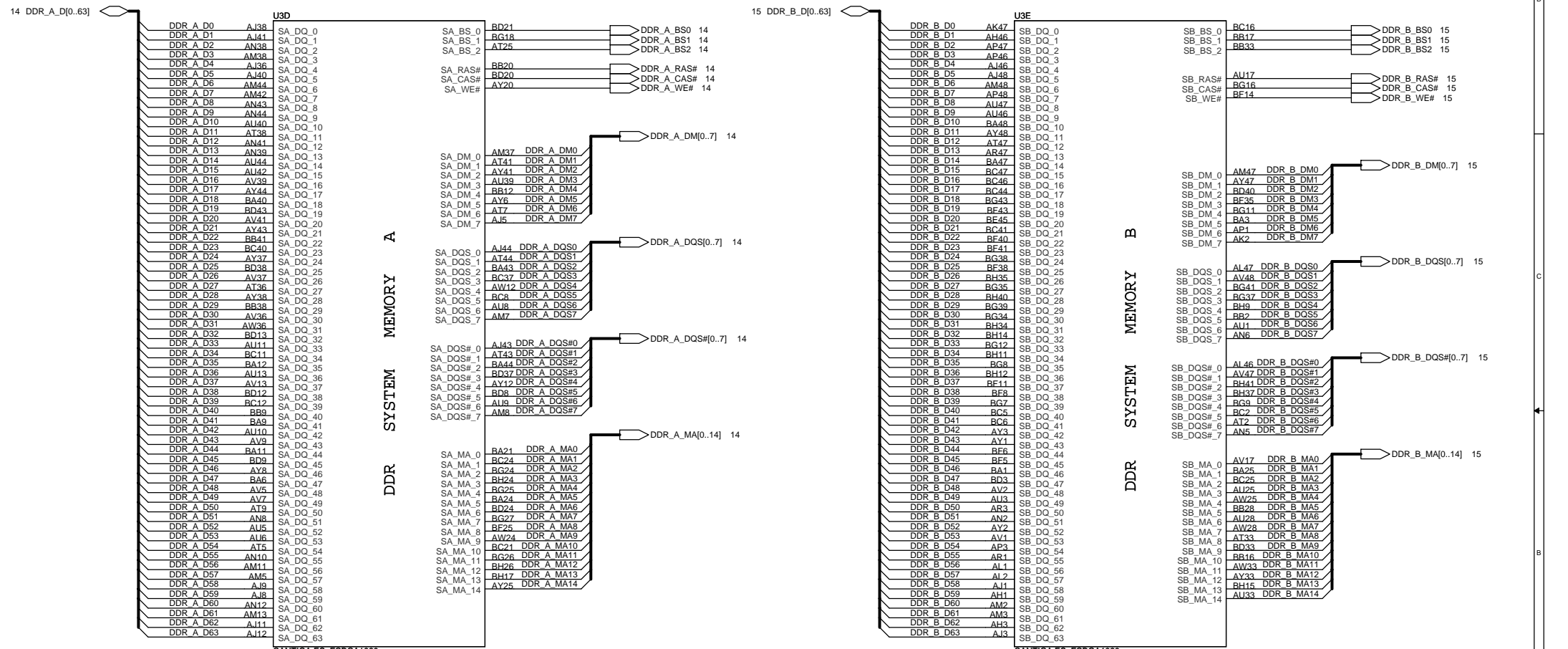
CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6 Internal pull-up	0 = iTPM Host Interface is enabled can support disable by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. *(Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.



SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled 1 = Digital display (iHDMI/DP) interface enable*(Default)

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G7R3@

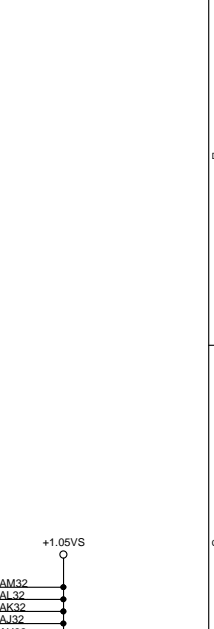
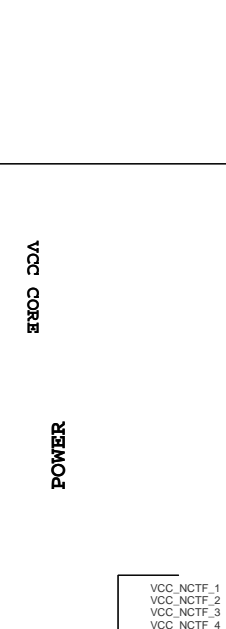
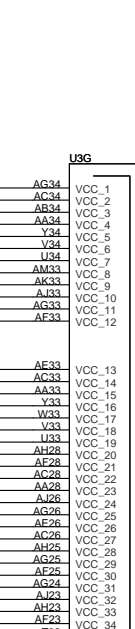
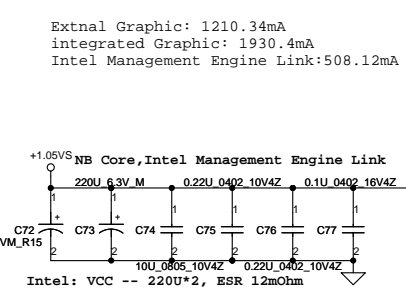
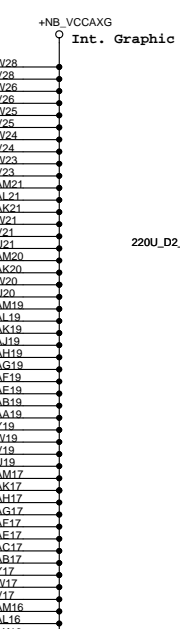
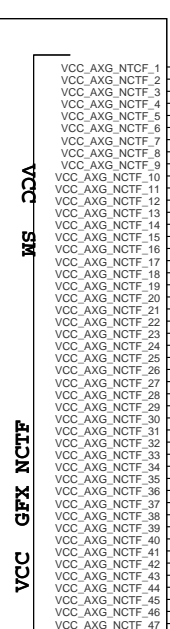
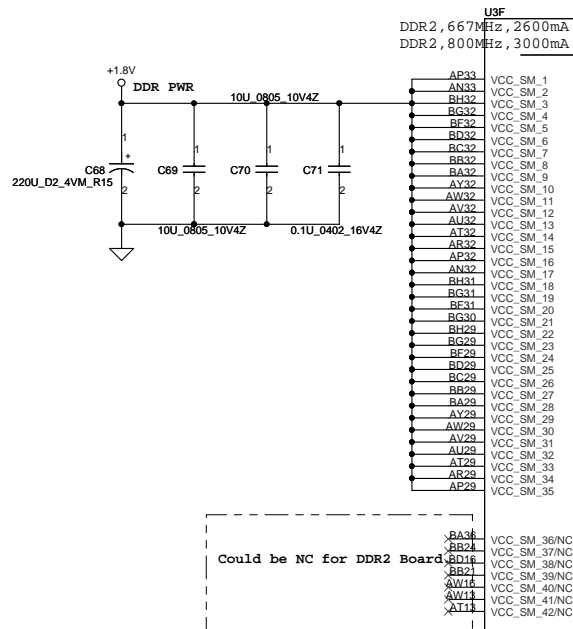
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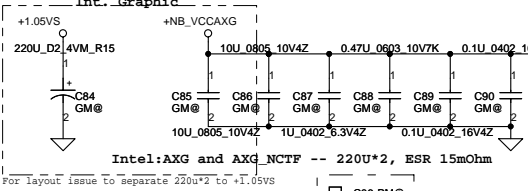
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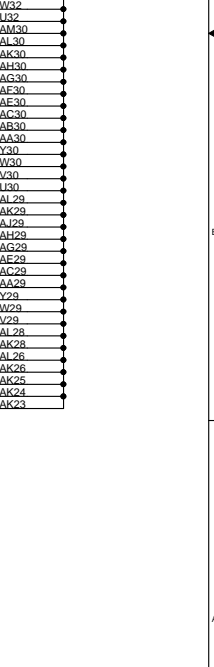
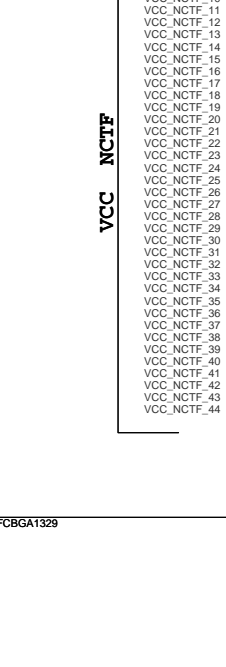
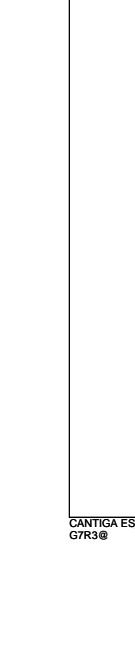
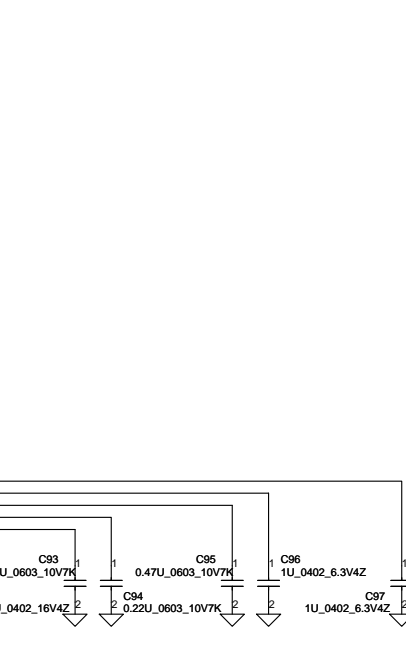
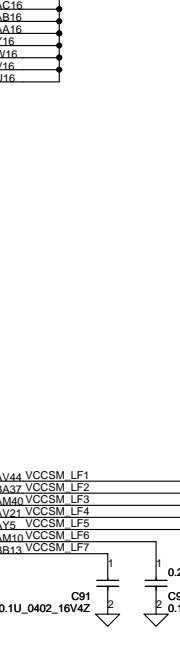
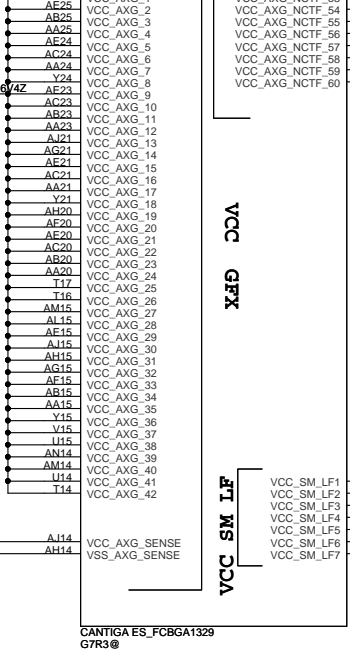
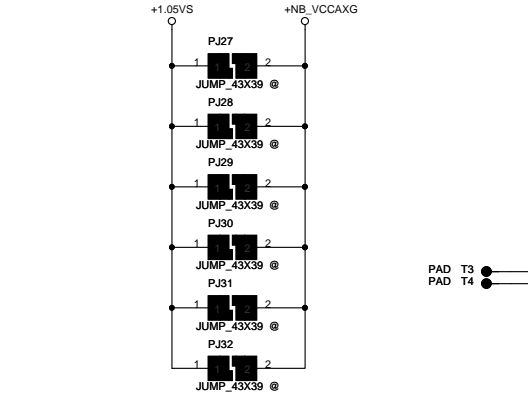
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For layout placement un-mound C123 and mound C84



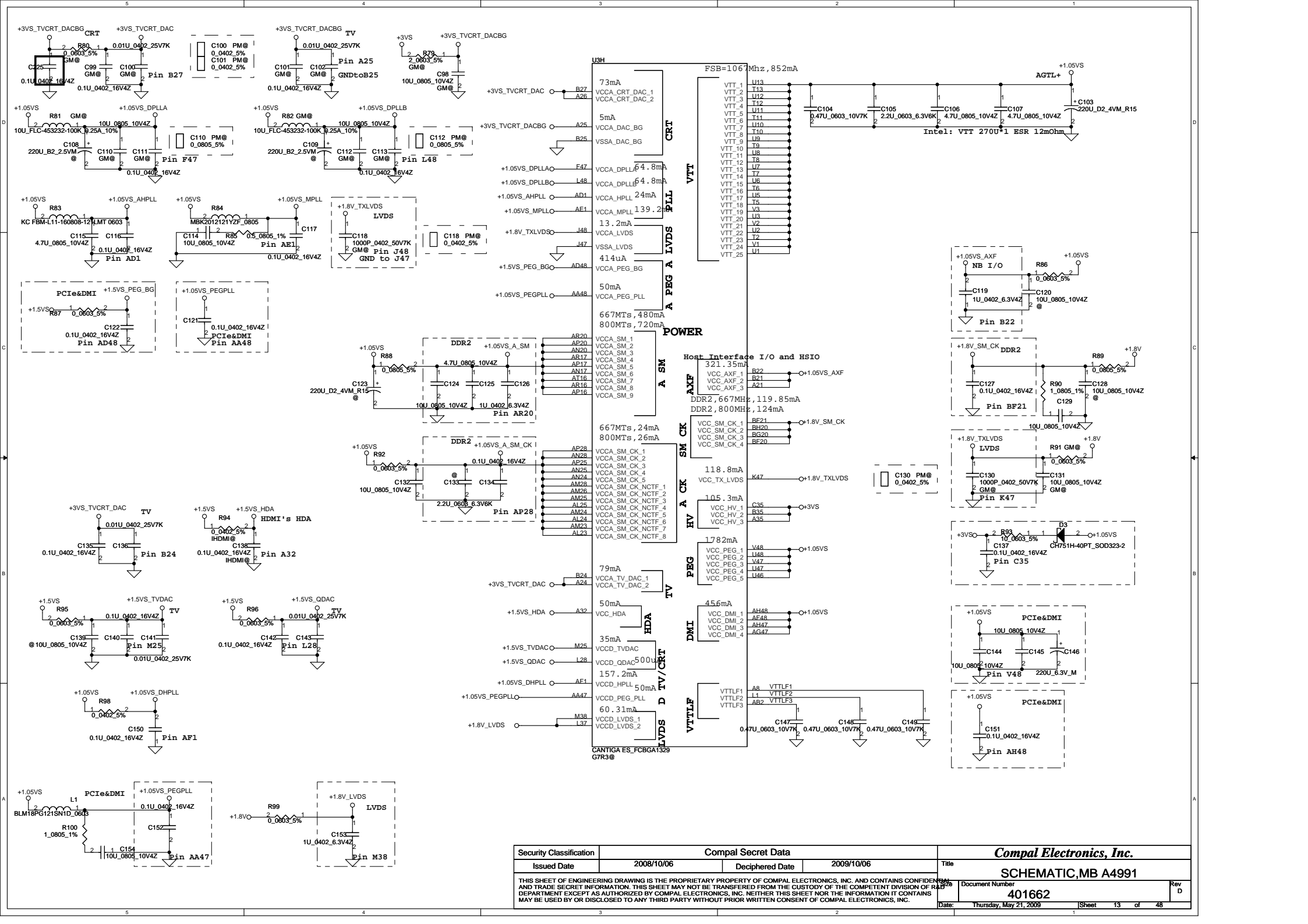
For layout issue to separate 220u*2 to +1.05vs



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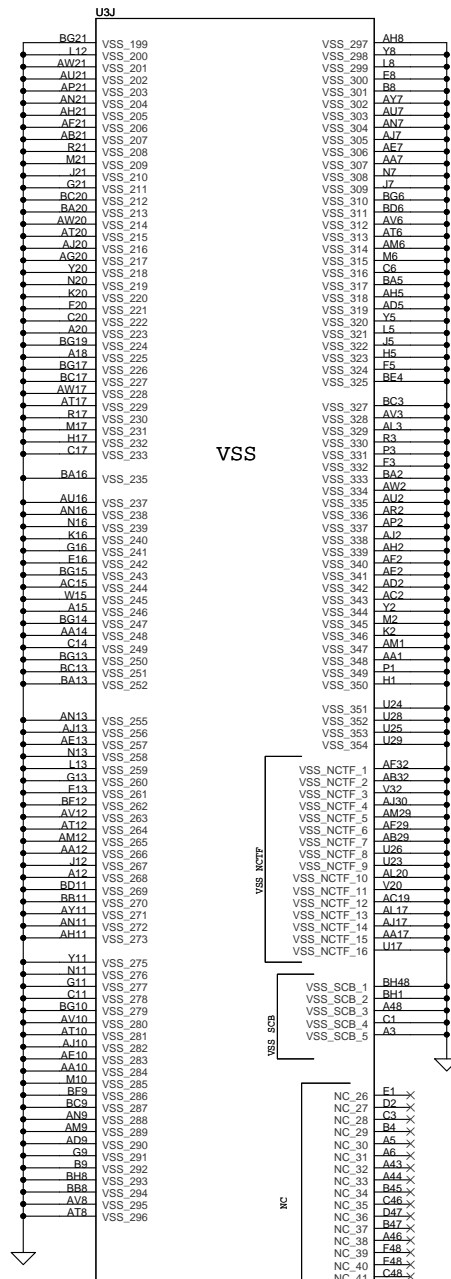
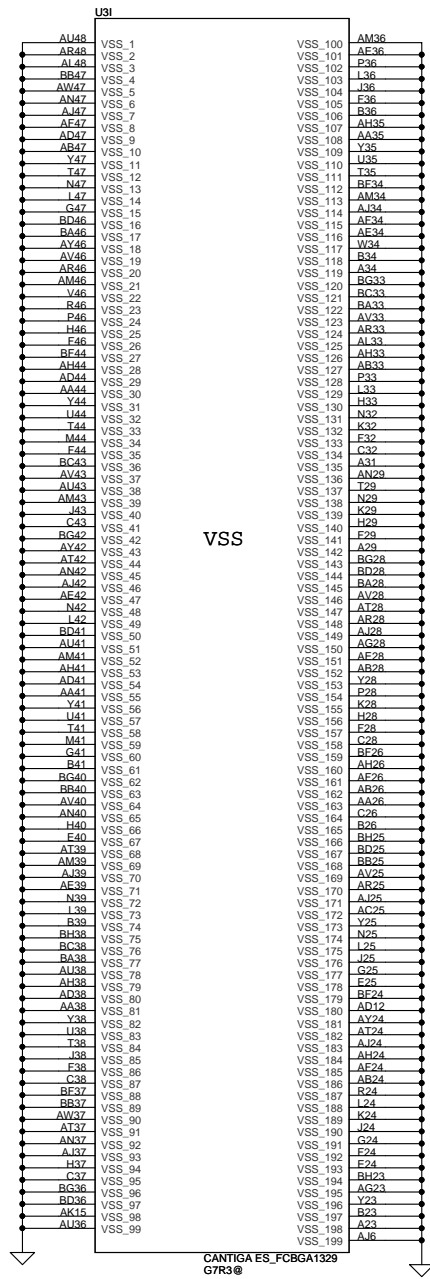
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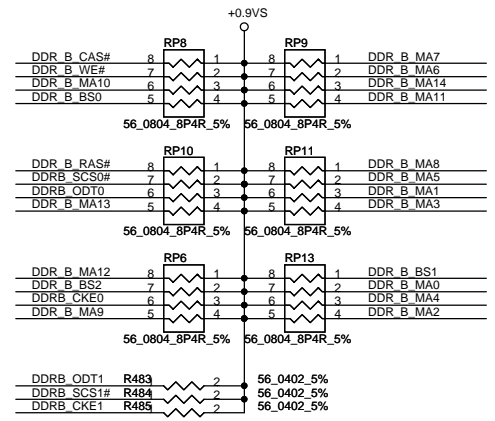
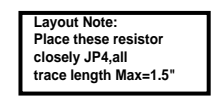
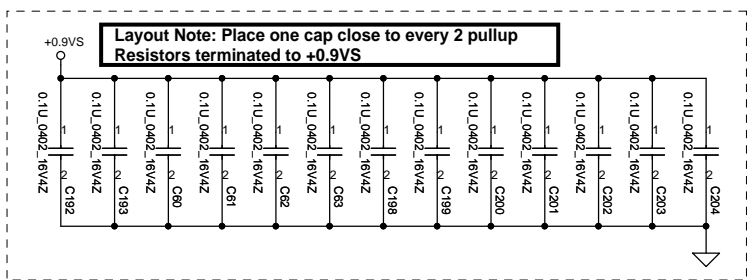
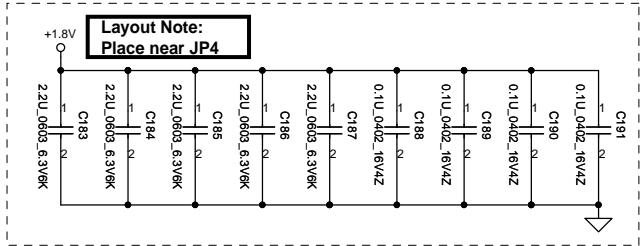
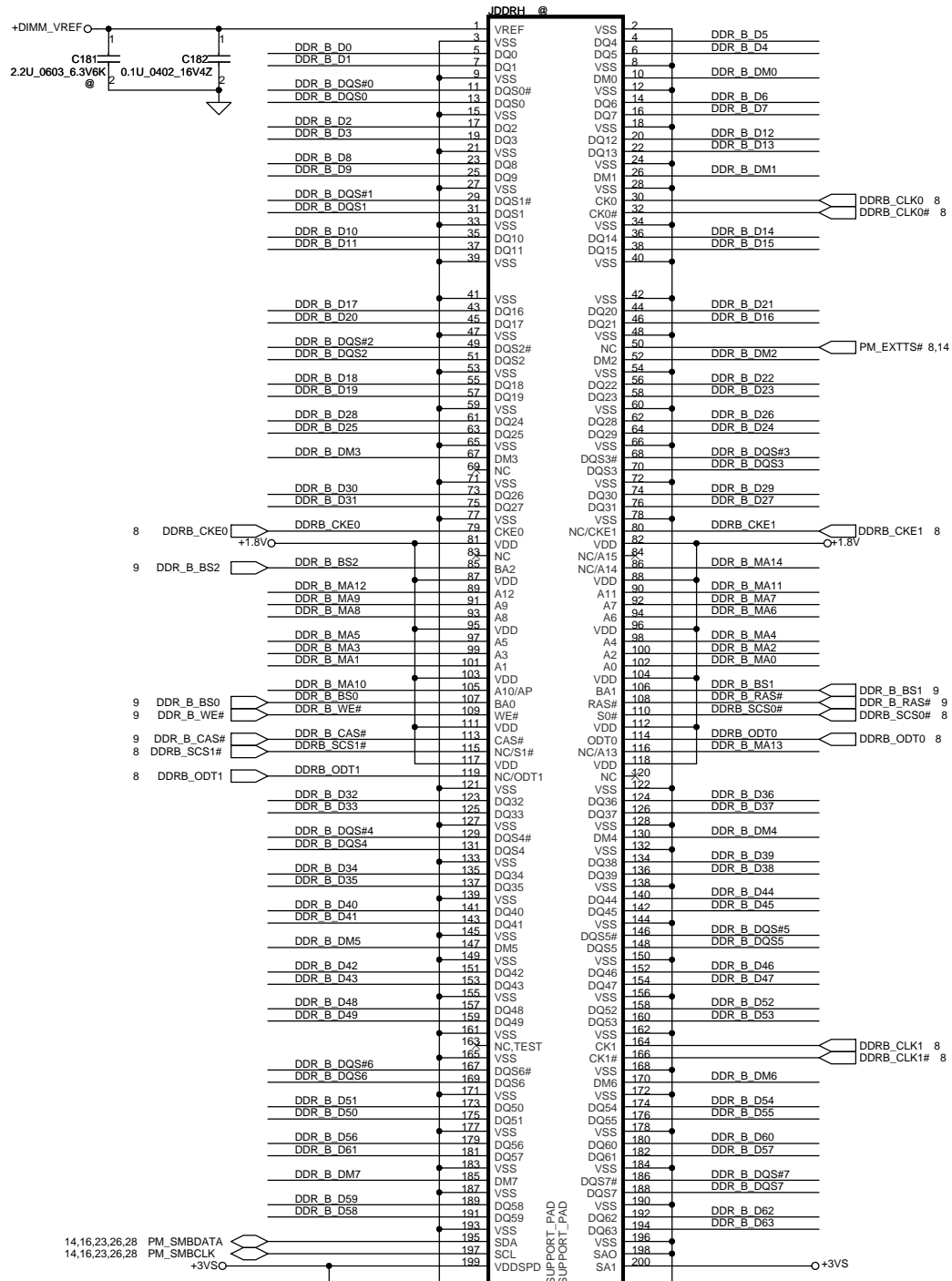


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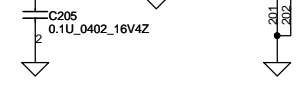
SCHEMATIC, MB A4991



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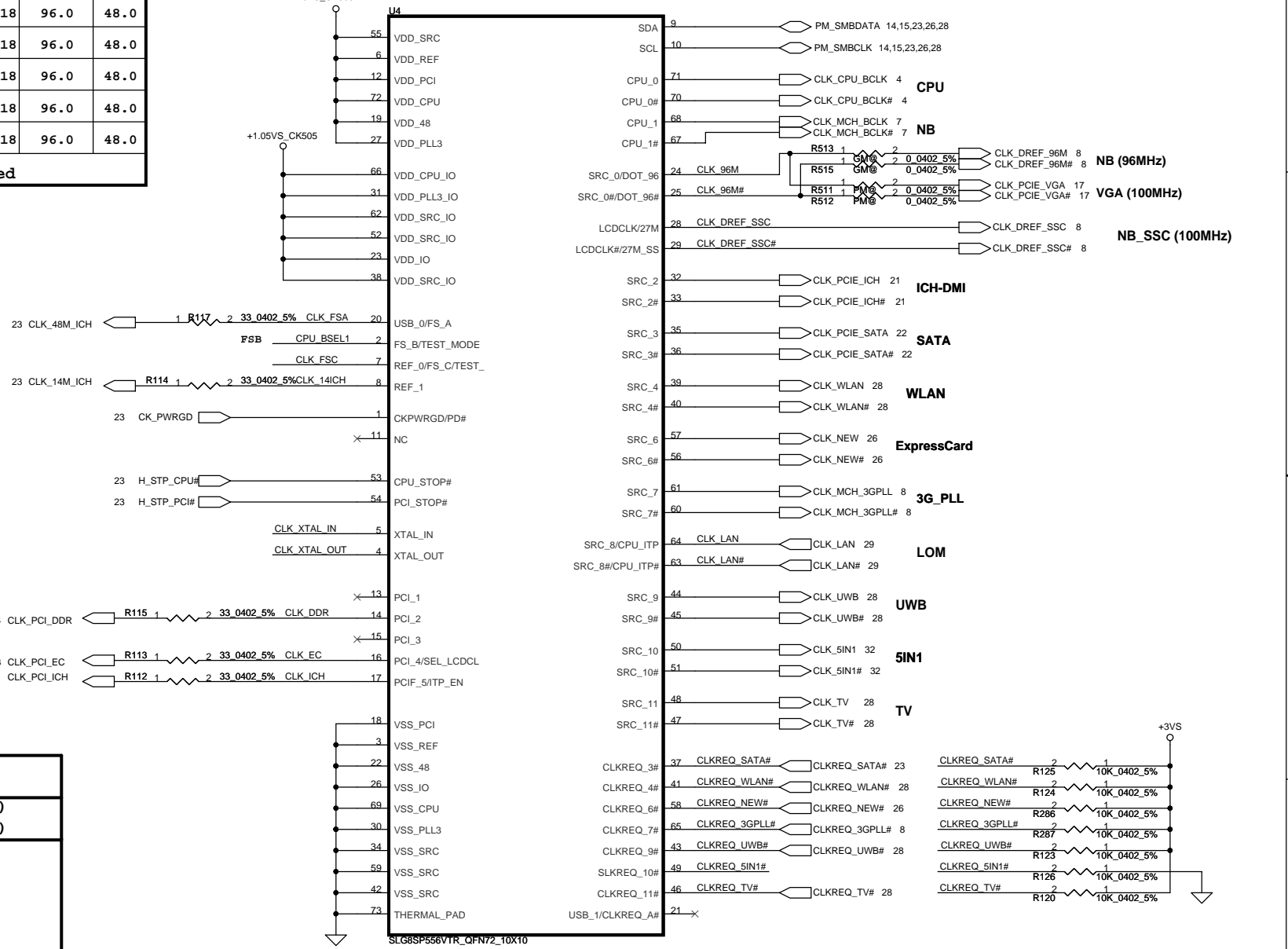
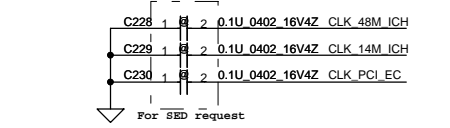
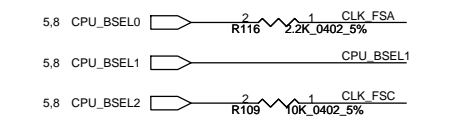
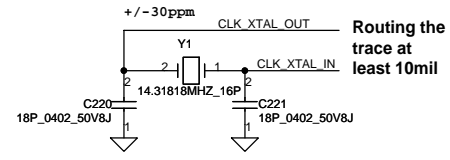
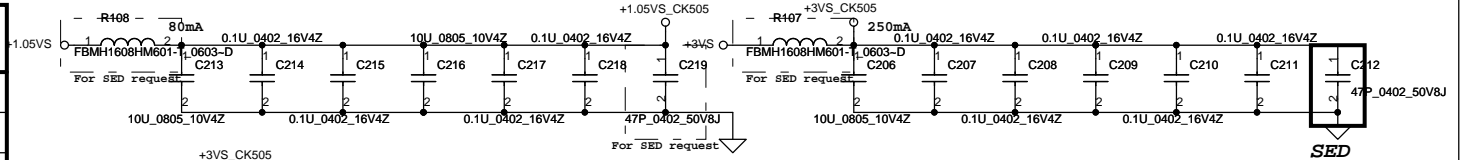


**SO-DIMM B
STANDARD
Bottom side**

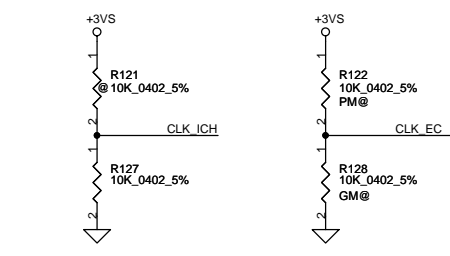


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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						

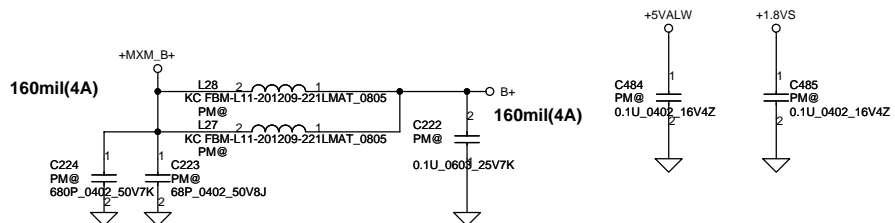
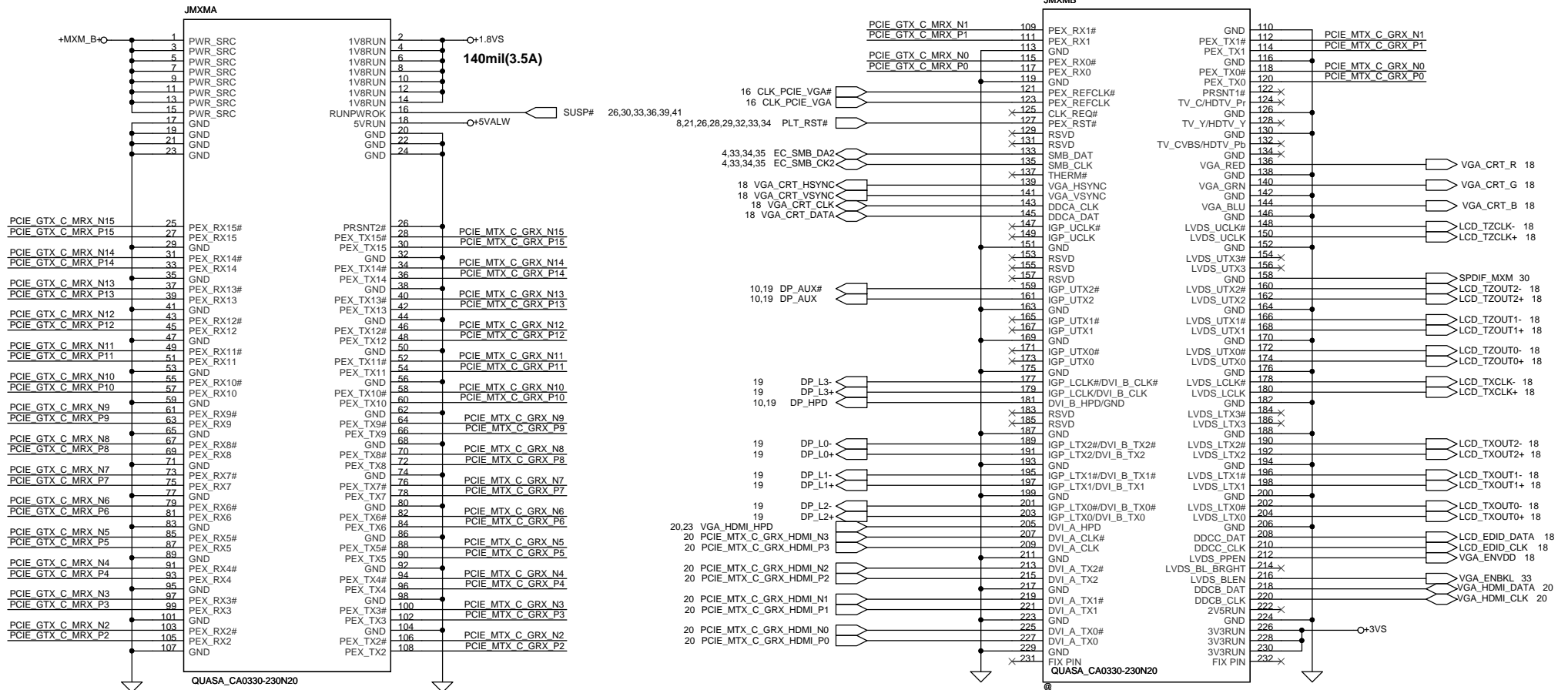


CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1 (UMA) 1 = Enable SRC0 & 27MHz (DIS)



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10,20 PCIE_MTX_C_GRX_N[0..15] ↔ PCIE_MTX_C_GRX_N[0..15] 10 PCIE_GTX_C_MRX_N[0..15] ↔ PCIE_GTX_C_MRX_N[0..15]
 10,20 PCIE_MTX_C_GRX_P[0..15] ↔ PCIE_MTX_C_GRX_P[0..15] 10 PCIE_GTX_C_MRX_P[0..15] ↔ PCIE_GTX_C_MRX_P[0..15]

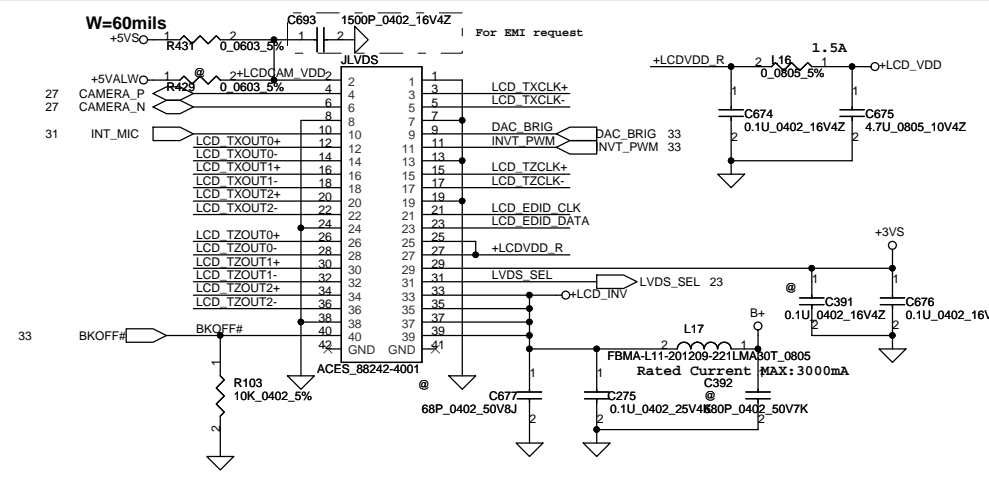


10 DP_L0+_NB	CV62	1	0.1U_0402_16V7K	DP_L0+
10 DP_L1+_NB	CV63	1	0.1U_0402_16V7K	DP_L1+
10 DP_L2+_NB	CV64	1	0.1U_0402_16V7K	DP_L2+
10 DP_L3+_NB	CV65	1	0.1U_0402_16V7K	DP_L3+
10 DP_L0+_NB	CV66	1	0.1U_0402_16V7K	DP_L0+
10 DP_L1+_NB	CV67	1	0.1U_0402_16V7K	DP_L1+
10 DP_L2+_NB	CV68	1	0.1U_0402_16V7K	DP_L2+
10 DP_L3+_NB	CV69	1	0.1U_0402_16V7K	DP_L3+

Close to MXM Connector

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LCD/PANEL BD. Conn.

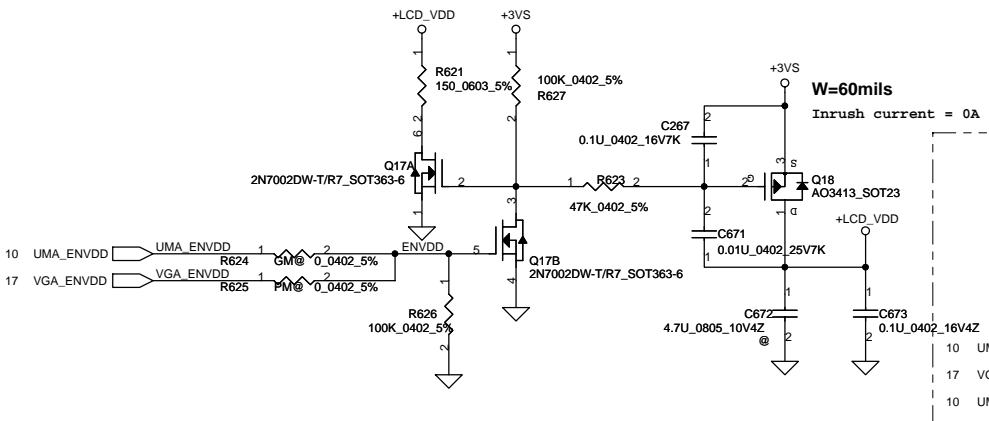
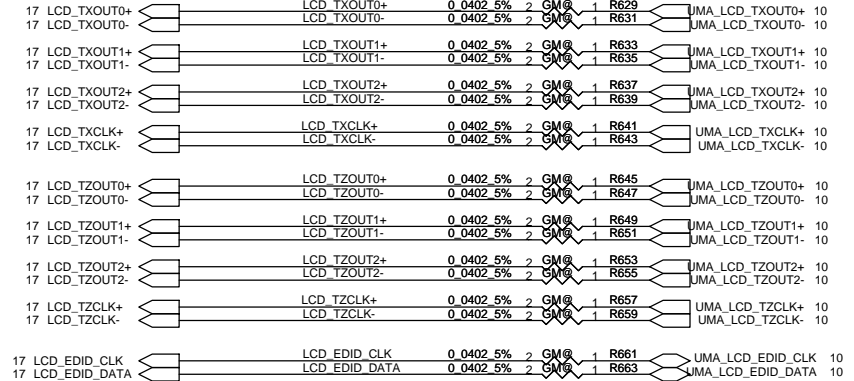


VGA side

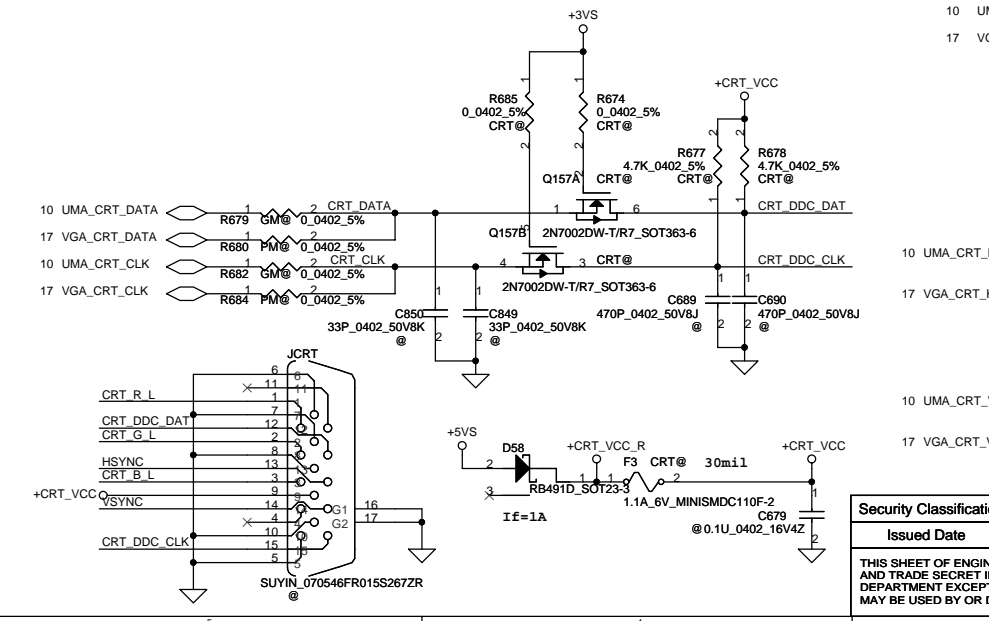
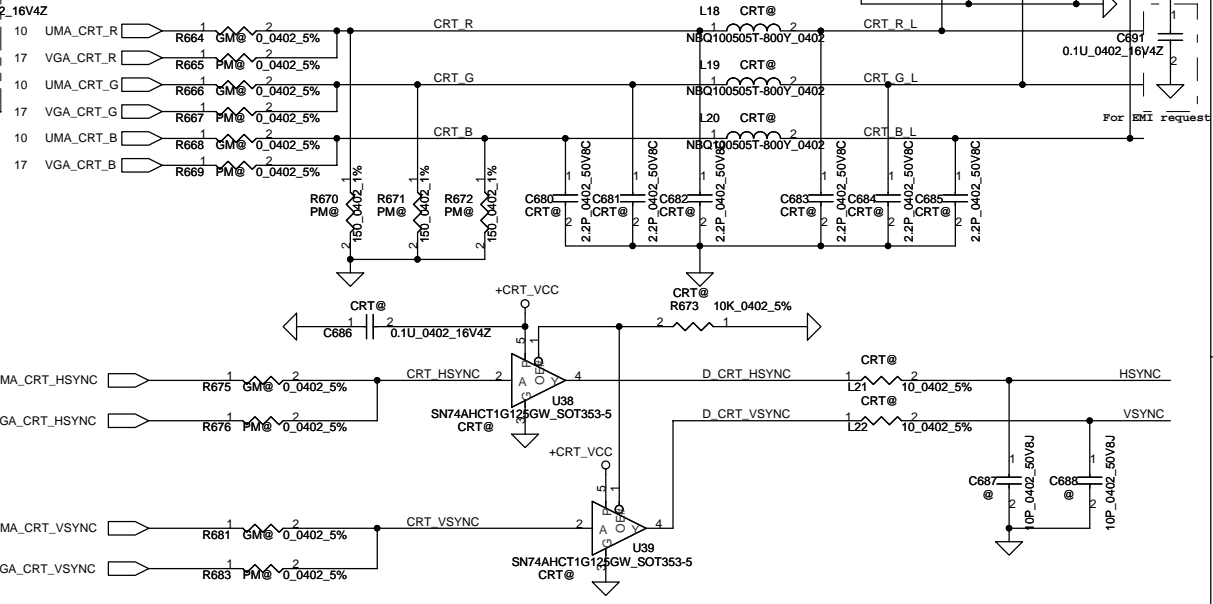
please link to VGA Conn. then link to LVDS Conn.

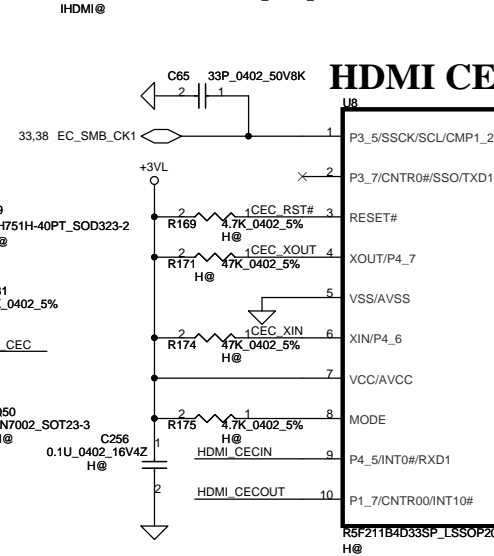
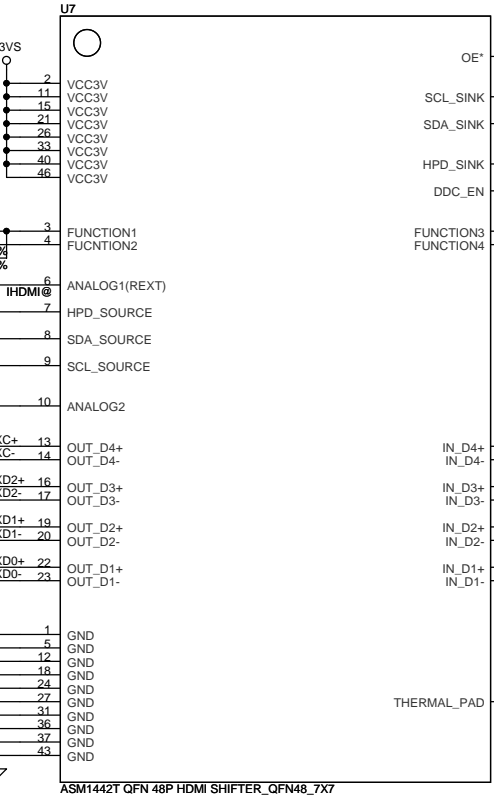
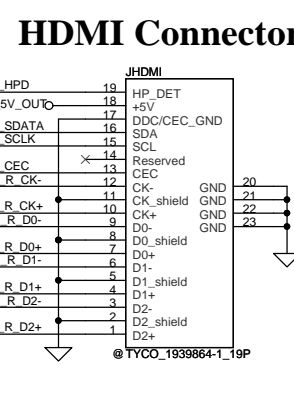
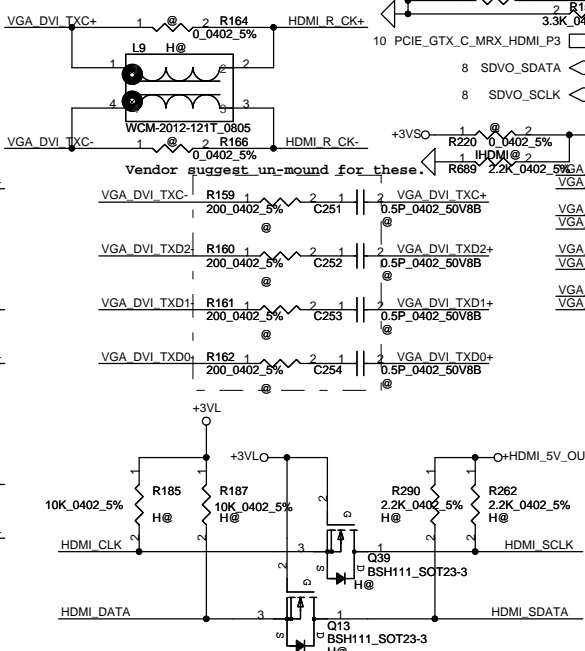
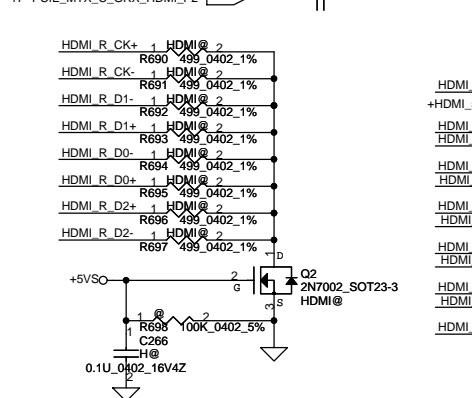
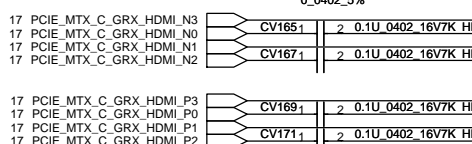
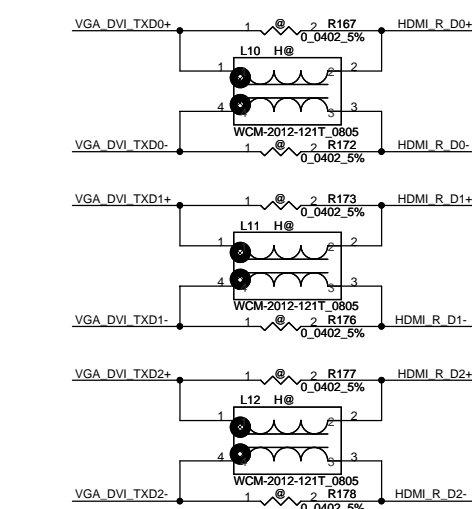
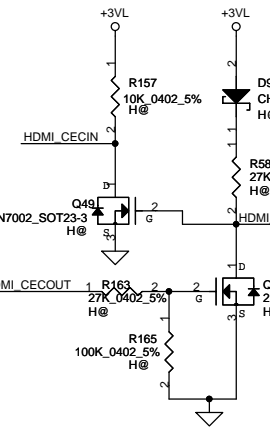
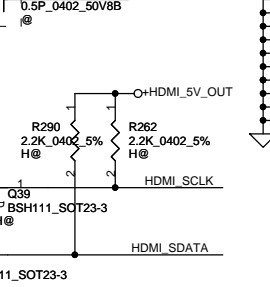
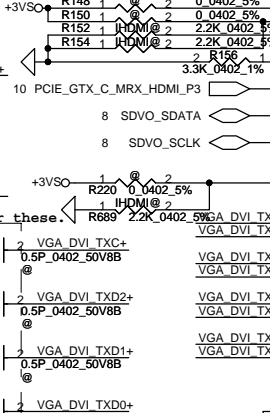
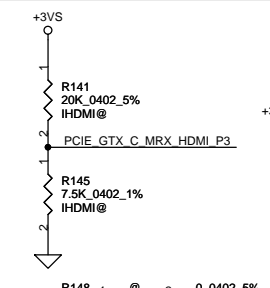
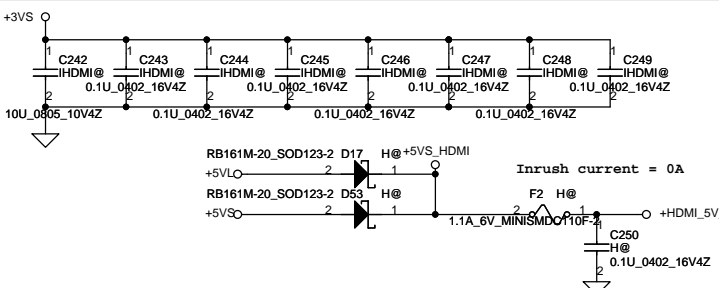
LVDS conn.

NB side

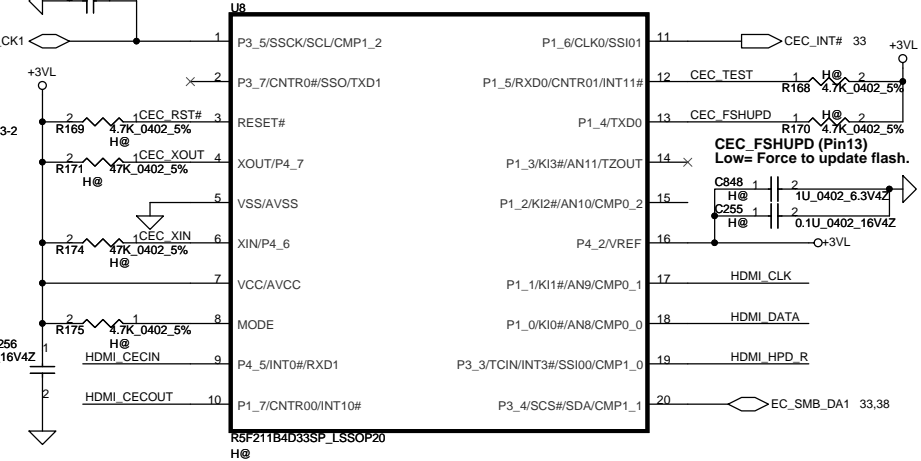


CRT CONNECTOR

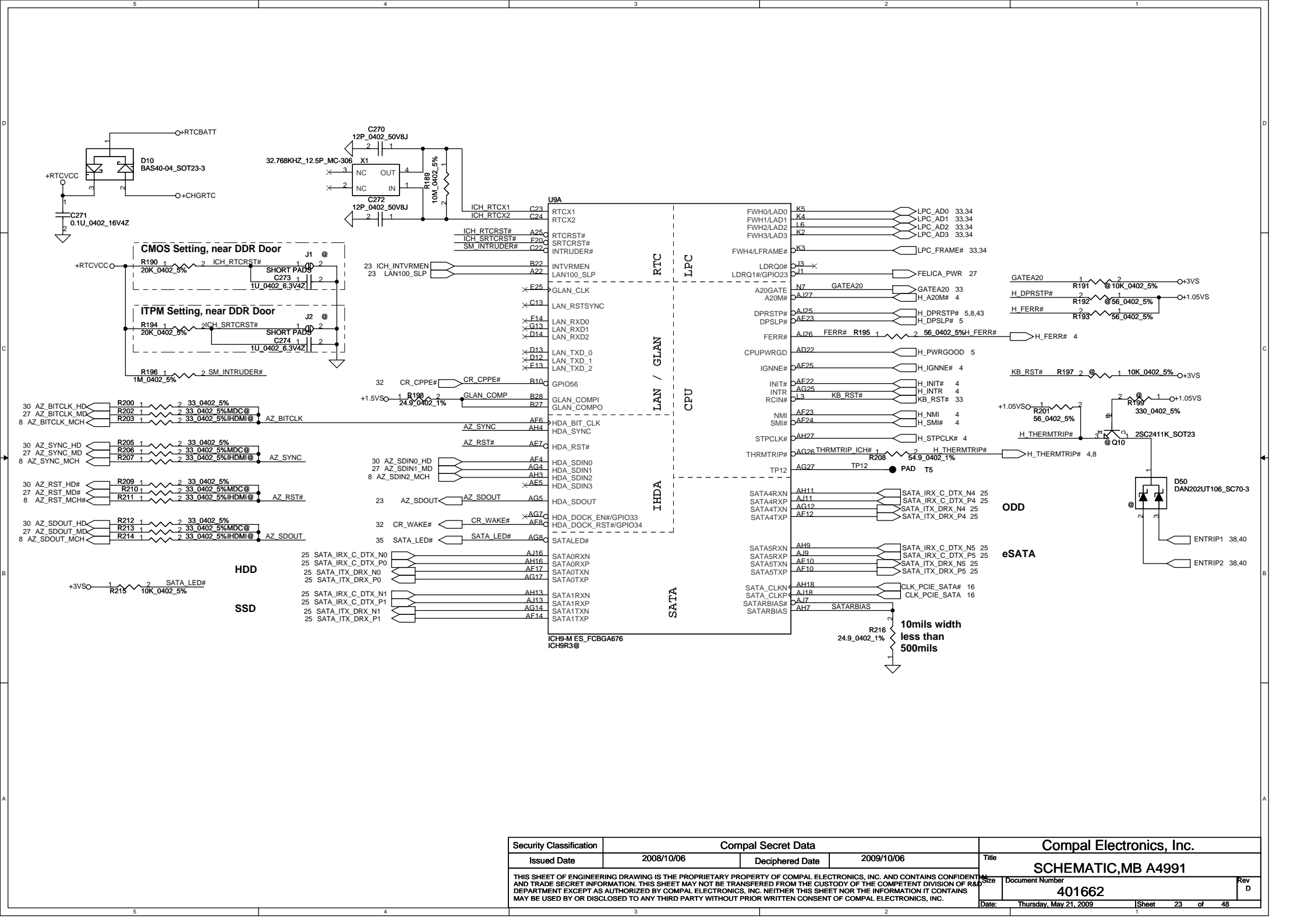




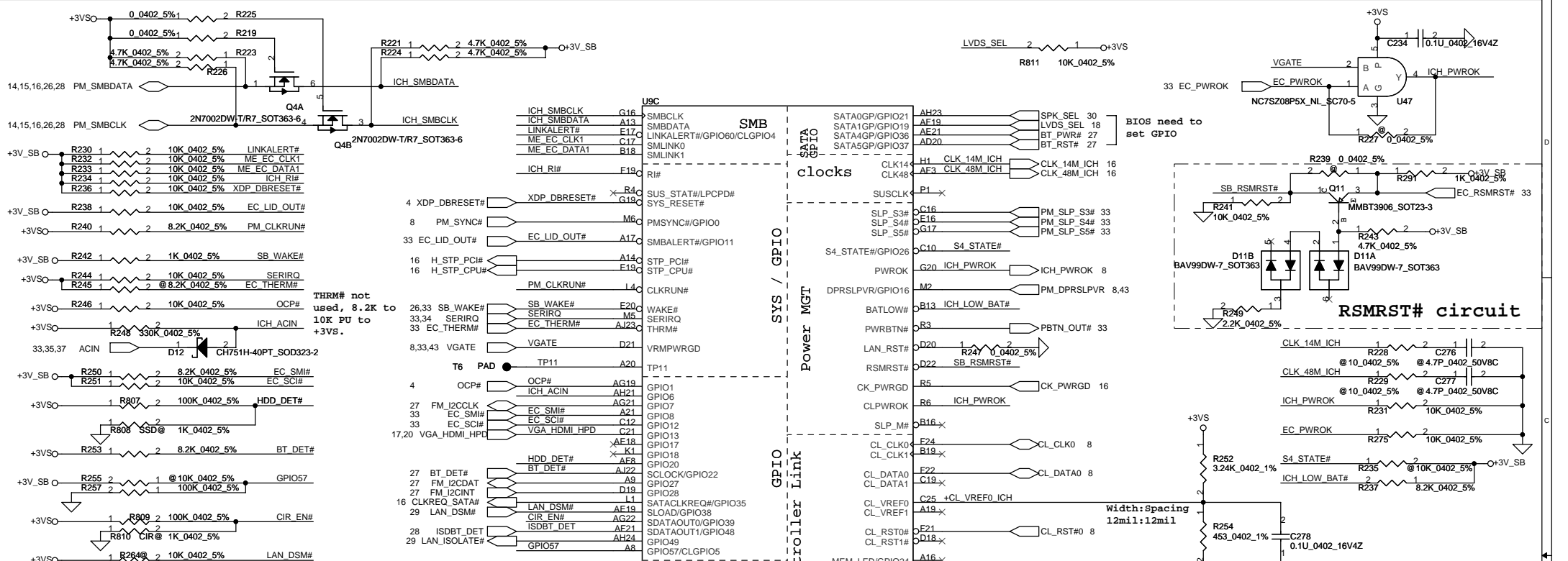
HDMI CEC Controller



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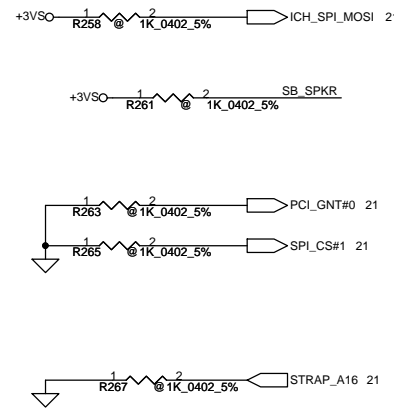


iTPM Physical Presence

CLGPIO5	Assert = iTPM Physical Presence Enable
Mobil Platform	De-assert = iTPM disable
	**Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

ICH9M Strap Pin



Internal TPM Strap (Internal pull-down)

SPI_MOSI	Low= Disable	High= iTPM enable by MCH strap*
----------	--------------	---------------------------------

No Reboot Strap (Internal pull-up)

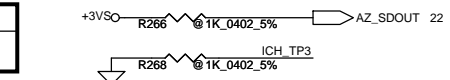
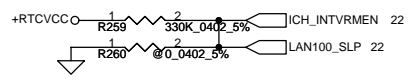
SB_SPKR	Low= "Default"	High= "No Reboot"
---------	----------------	-------------------

Boot BIOS Strap (Internal pull-up)

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable	High= Default* (Internal pull-up)
-----------	-------------------------------	-----------------------------------



Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled	High = Internal VR Enabled(Default)
--------------	----------------------------	-------------------------------------

Flash Descriptor Security Override Strap

GPIO33	Low= Descriptor Security override	High= Default* (Internal pull-up)
--------	-----------------------------------	-----------------------------------

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled	High = Internal VR Enabled(Default)
----------------	----------------------------	-------------------------------------

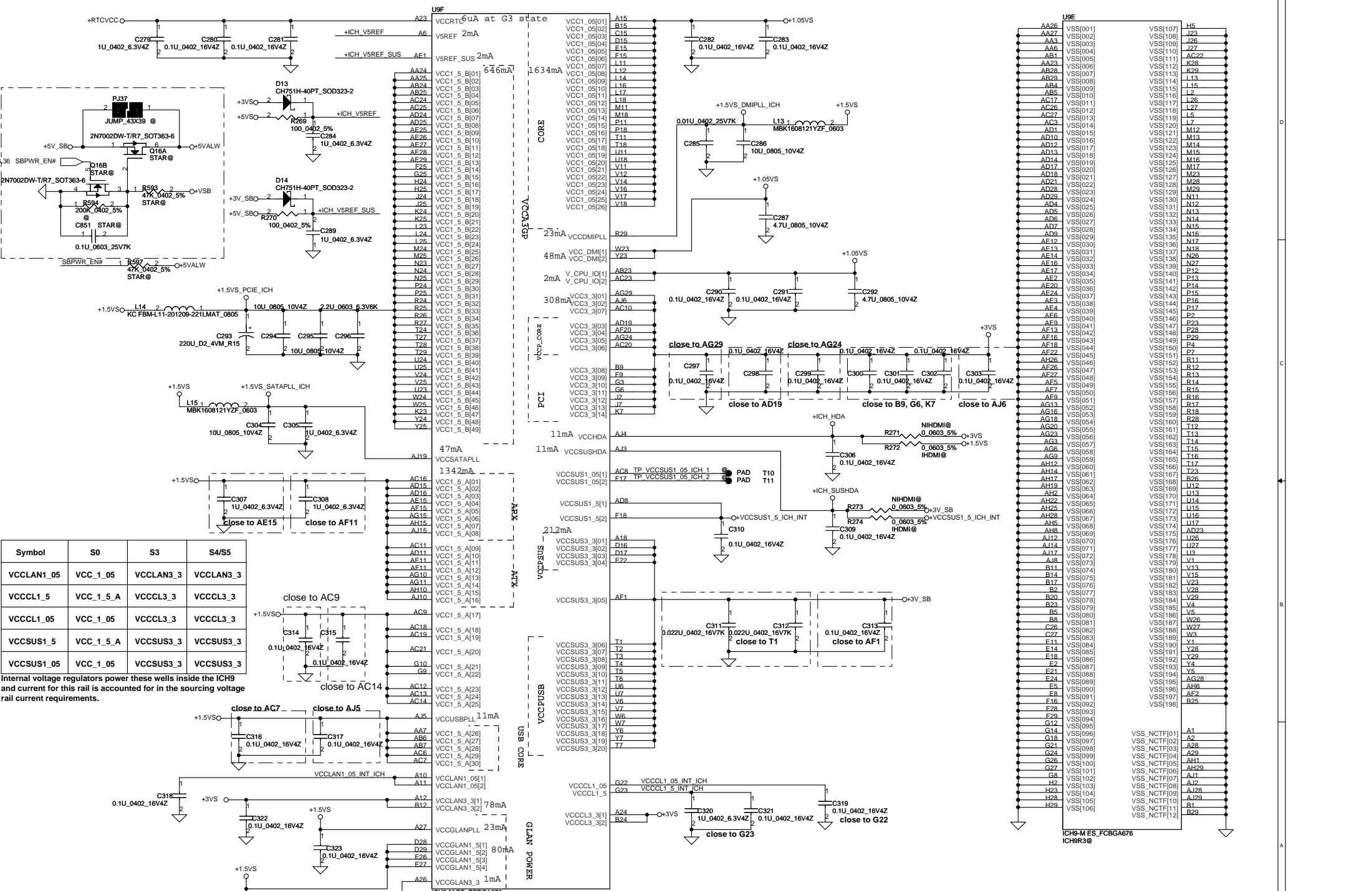
DMI Termination Voltage

GPIO49	Low= Desktop used	High= Mobile* (Internal pull-up)
--------	-------------------	----------------------------------

XOR Chain Entrance Strap

ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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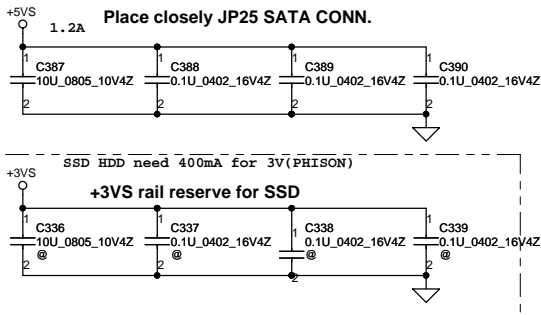


Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN_3_3	VCCLAN_3_3
VCCCL1_5	VCC_1_5_A	VCCCL_3_3	VCCCL_3_3
VCCCL1_05	VCC_1_05	VCCCL_3_3	VCCCL_3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS_3_3	VCCSUS_3_3
VCCSUS1_05	VCC_1_05	VCCSUS_3_3	VCCSUS_3_3

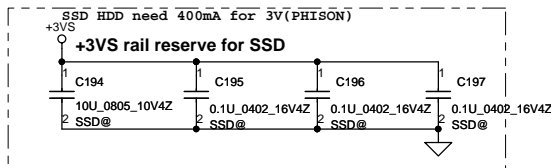
Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

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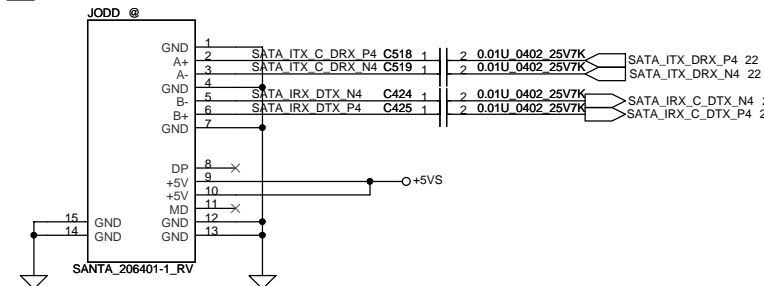
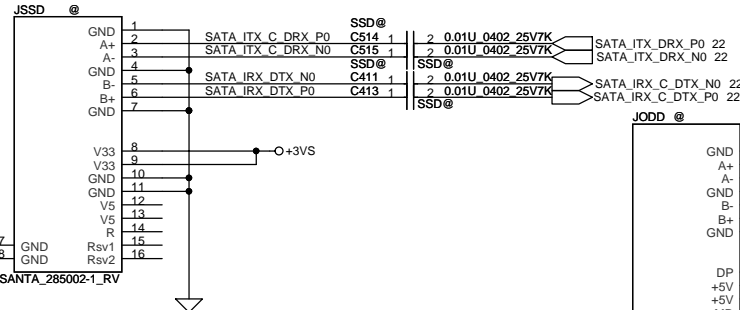
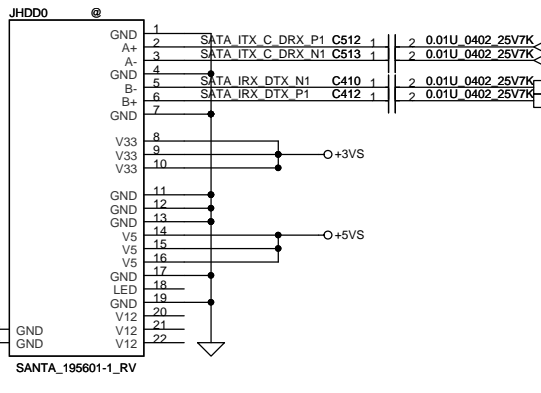
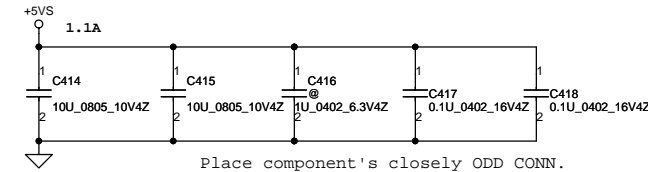
SATA HDD Conn.



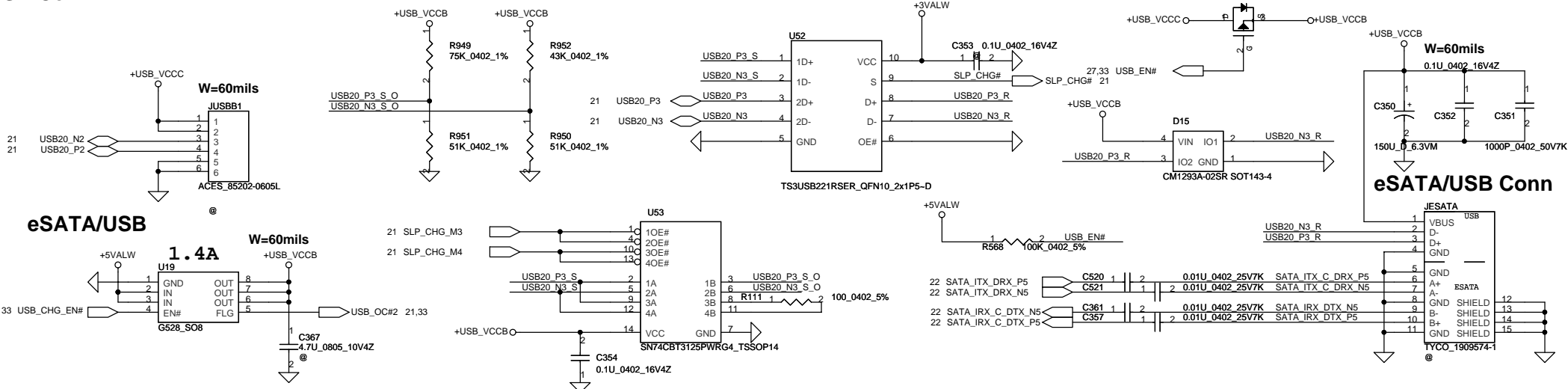
SSD Conn.



SATA ODD Conn



USB Conn.



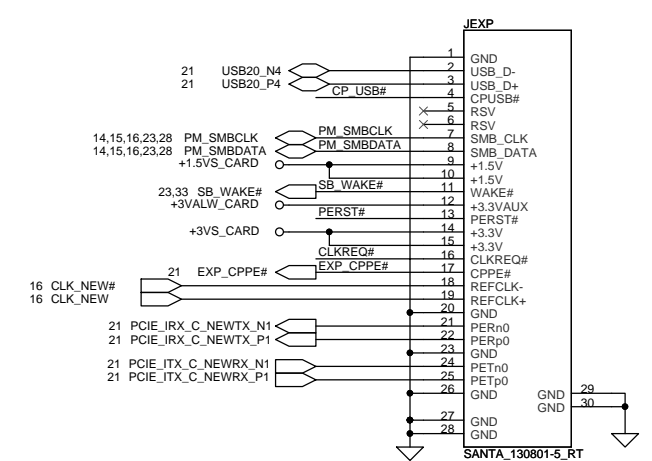
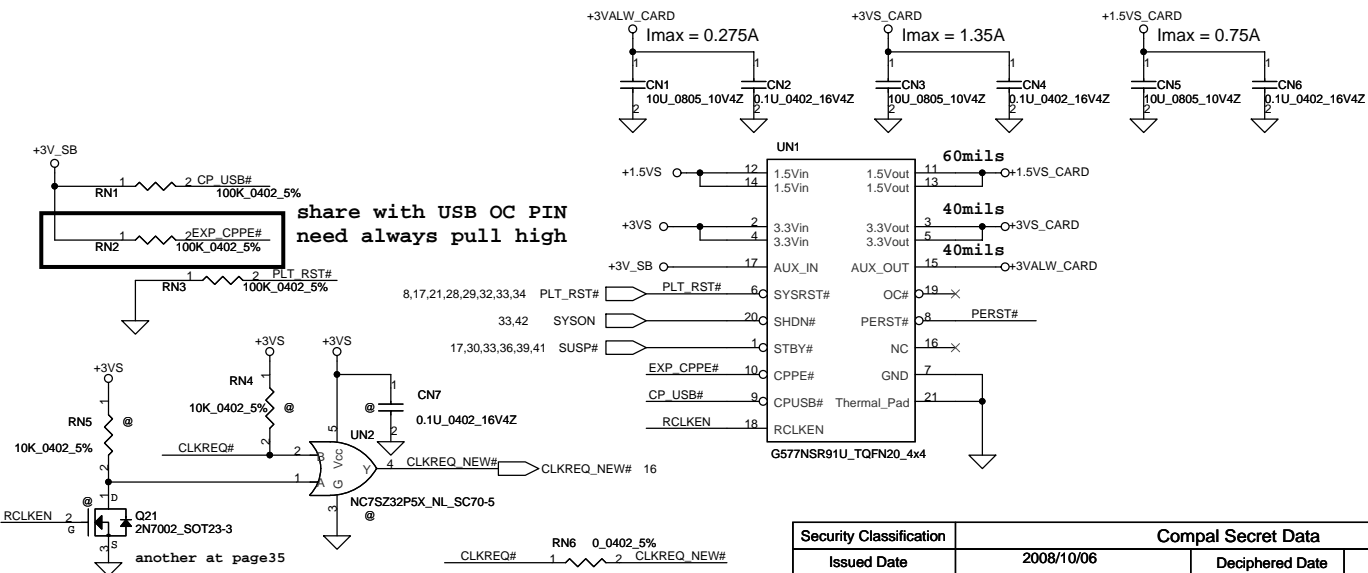
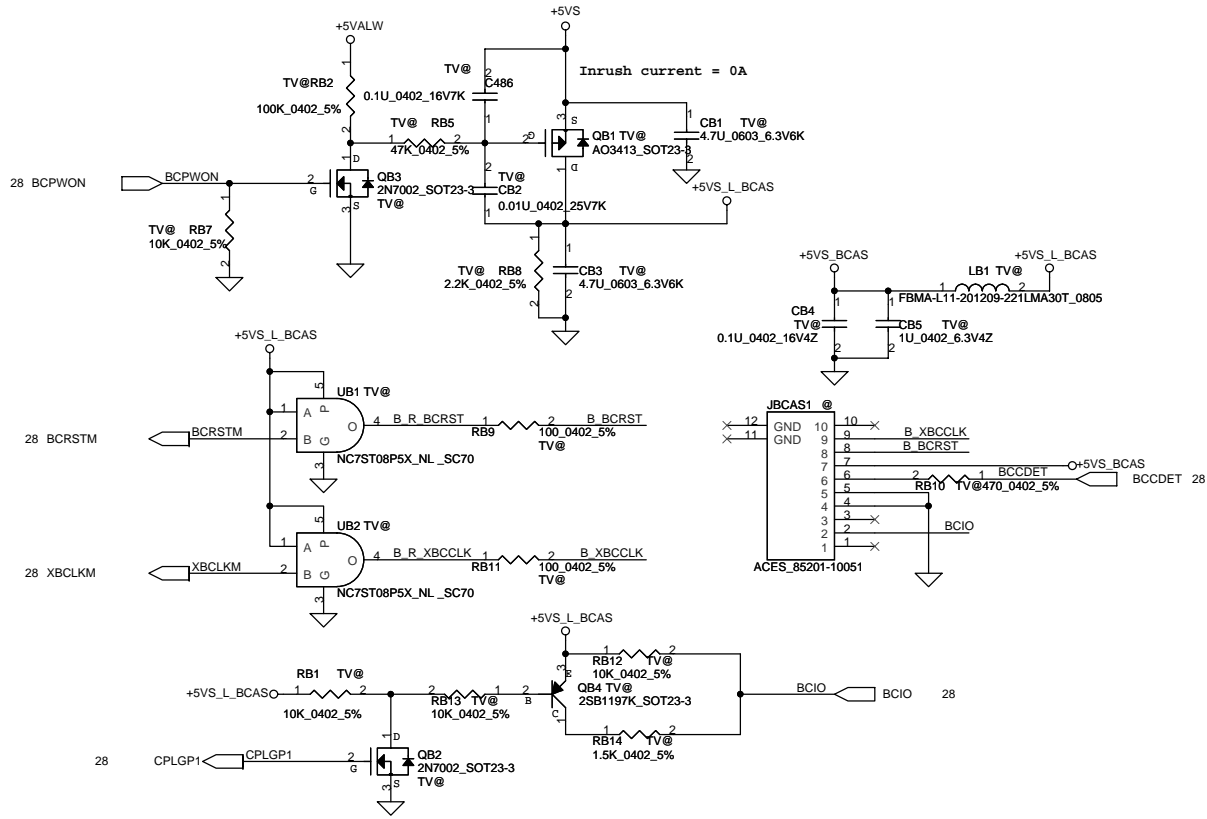
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

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B-CAS Circuit



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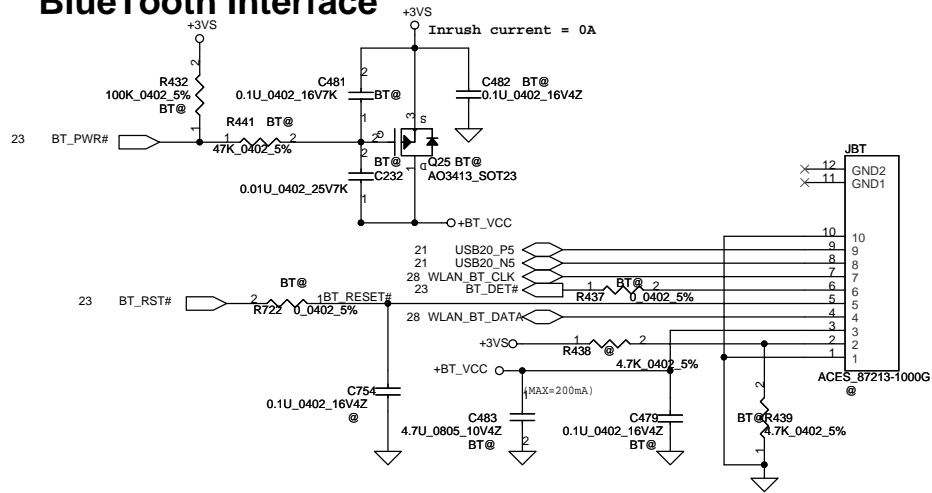
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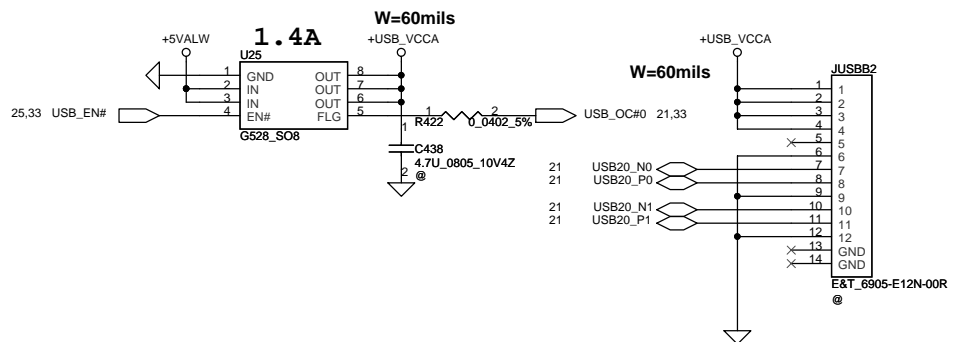
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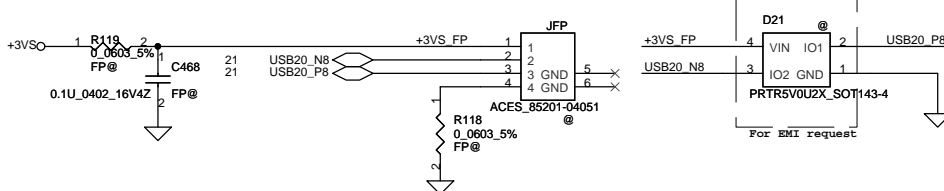
BlueTooth Interface



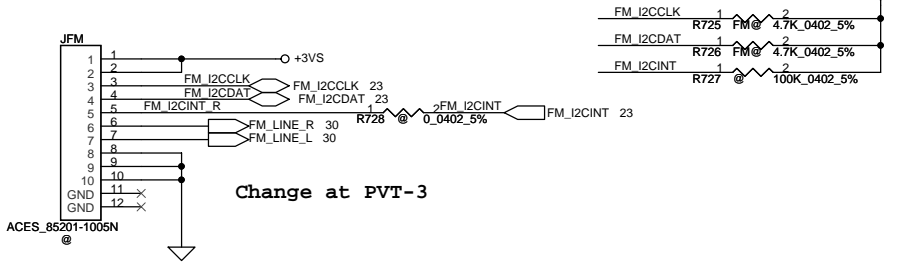
Right USB Board



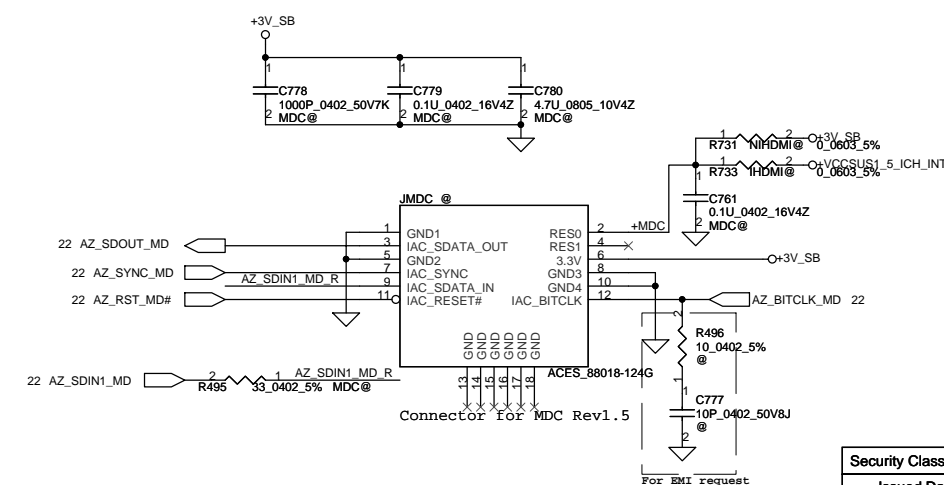
Finger printer



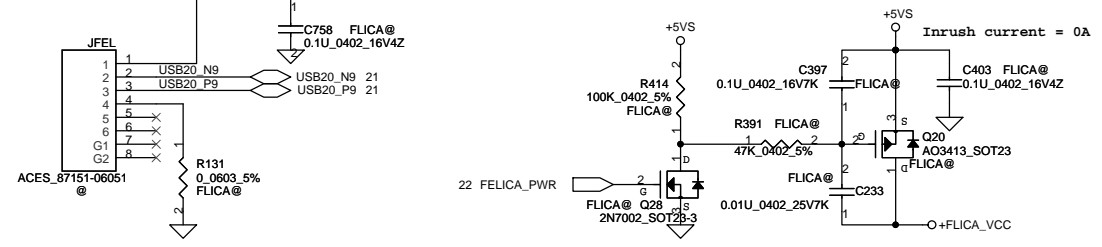
FM tuner



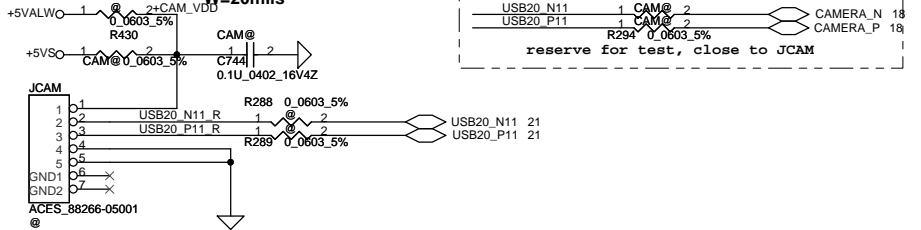
MDC 1.5 Conn.



Felica

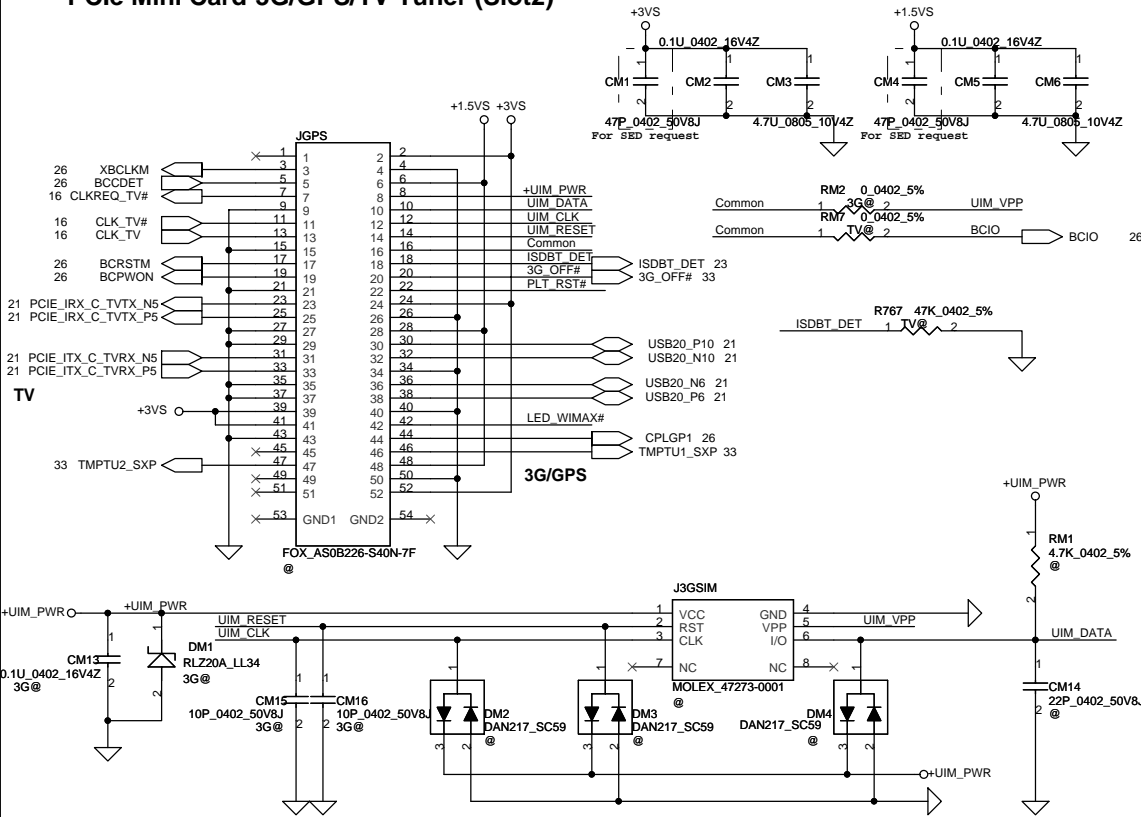


Int. Camera

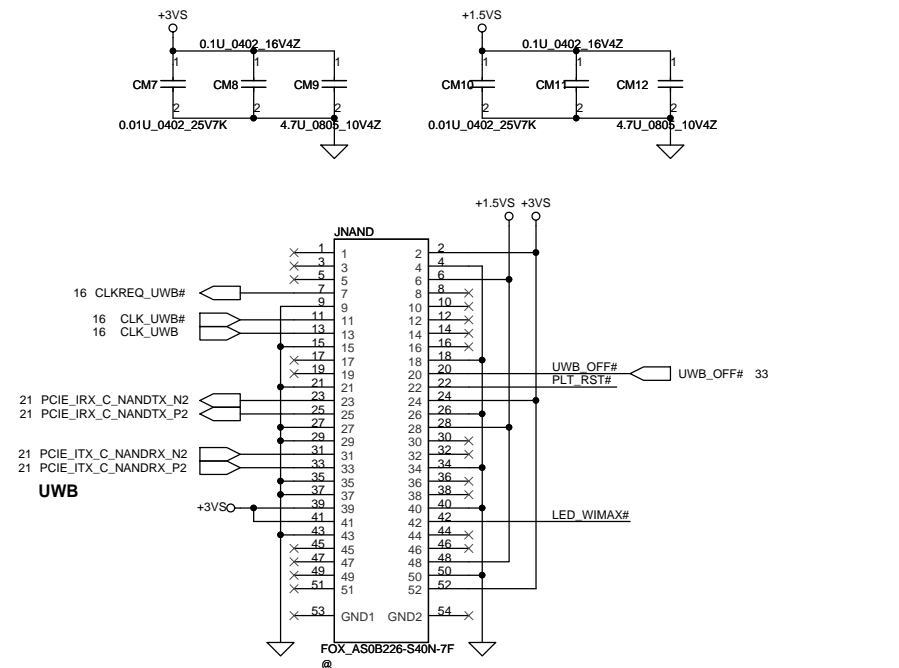


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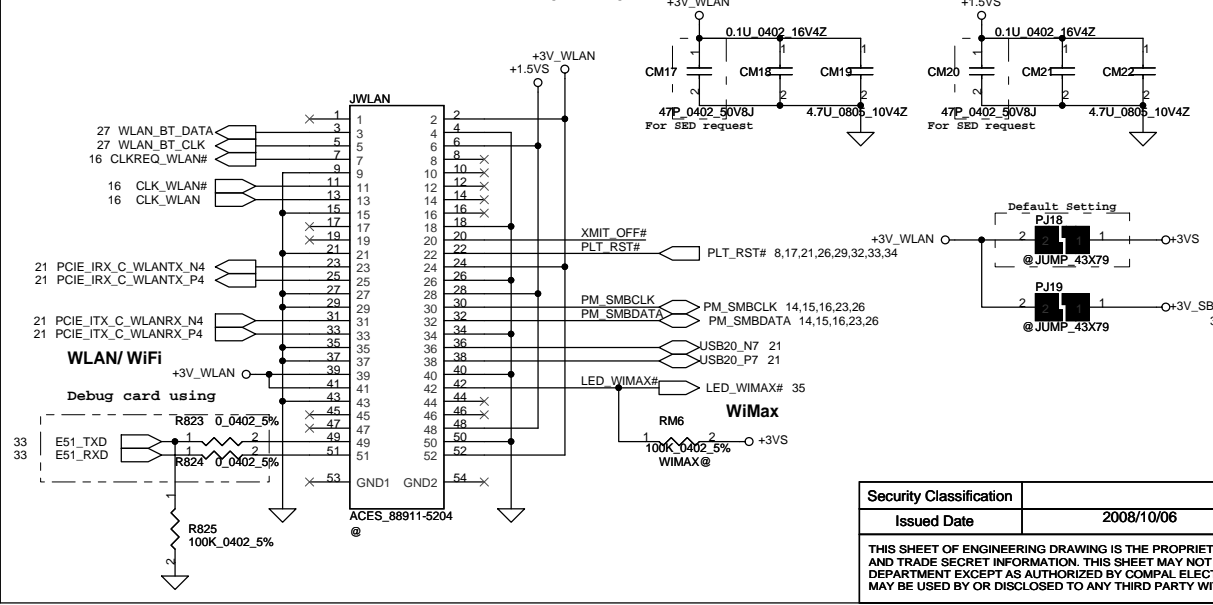
PCIe Mini Card-3G/GPS/TV Tuner (Slot2)



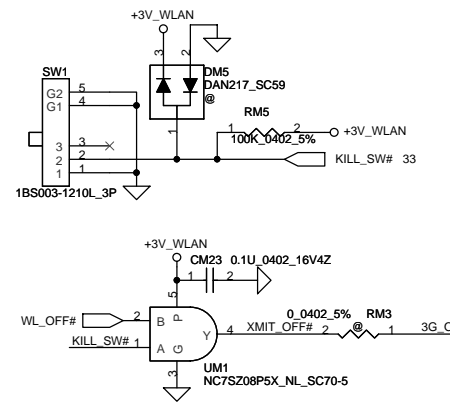
UWB/JET (Slot3)



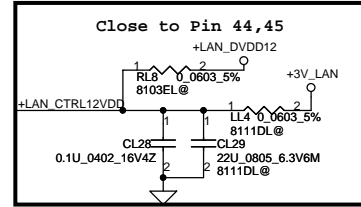
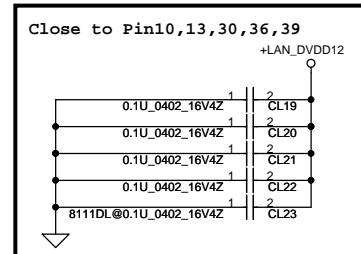
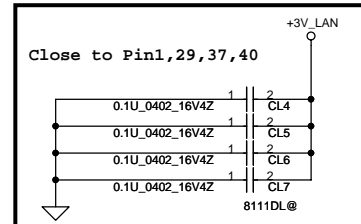
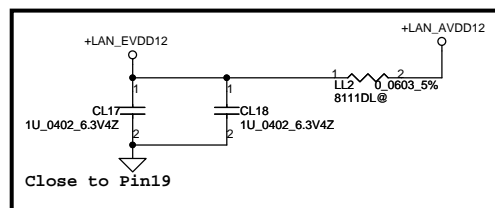
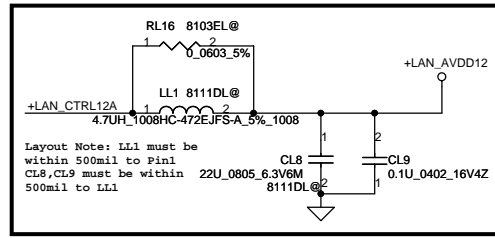
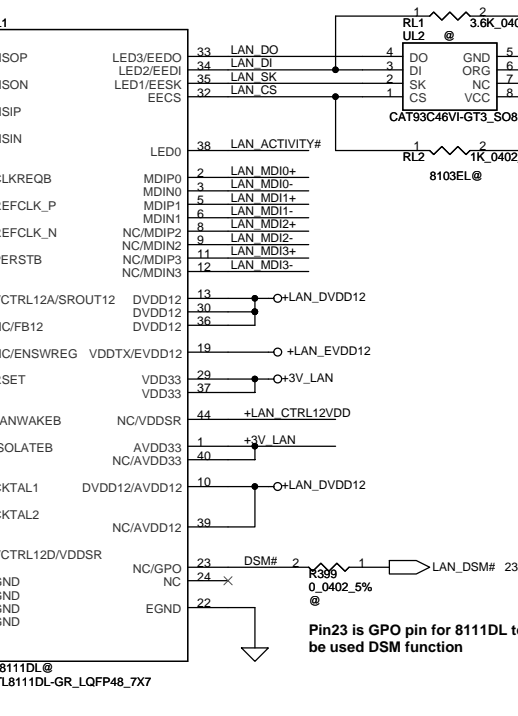
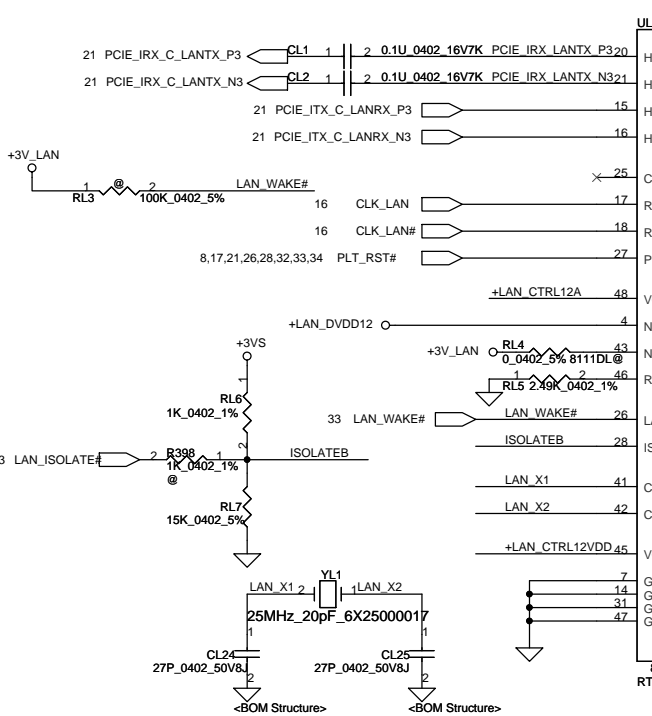
PCIe Mini Card-WLAN/WiMax (Slot1)



Kill SWITCH

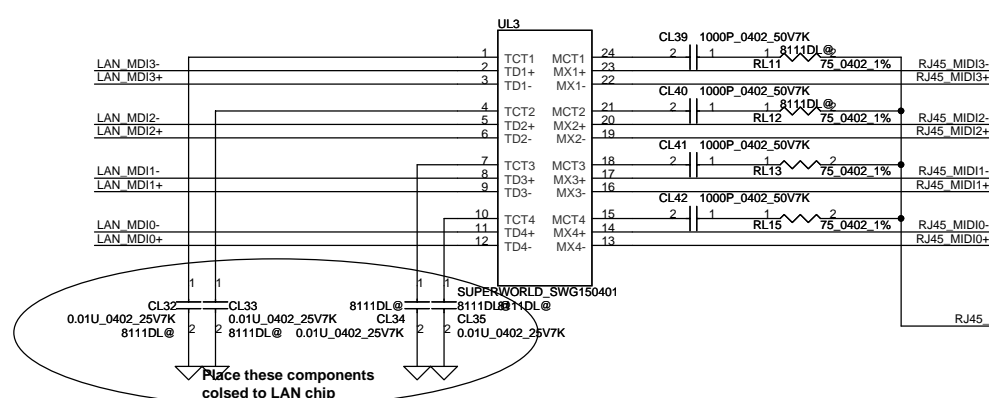


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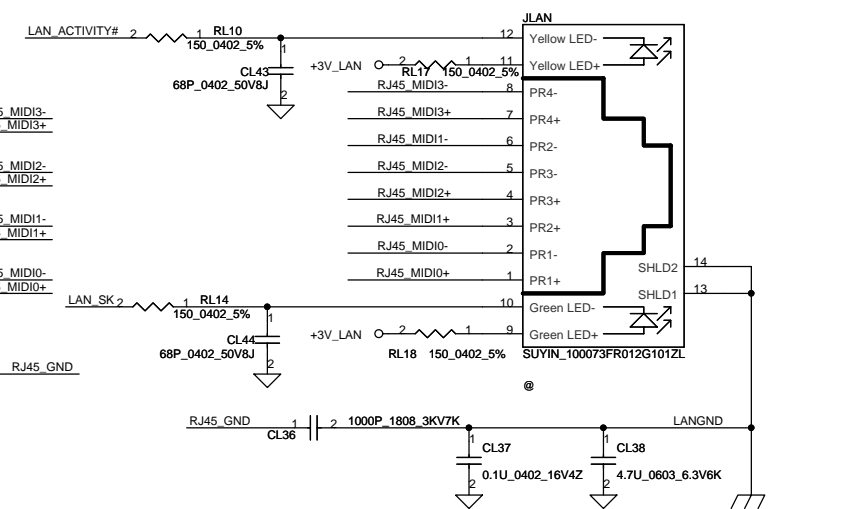


pin assignments table for difference

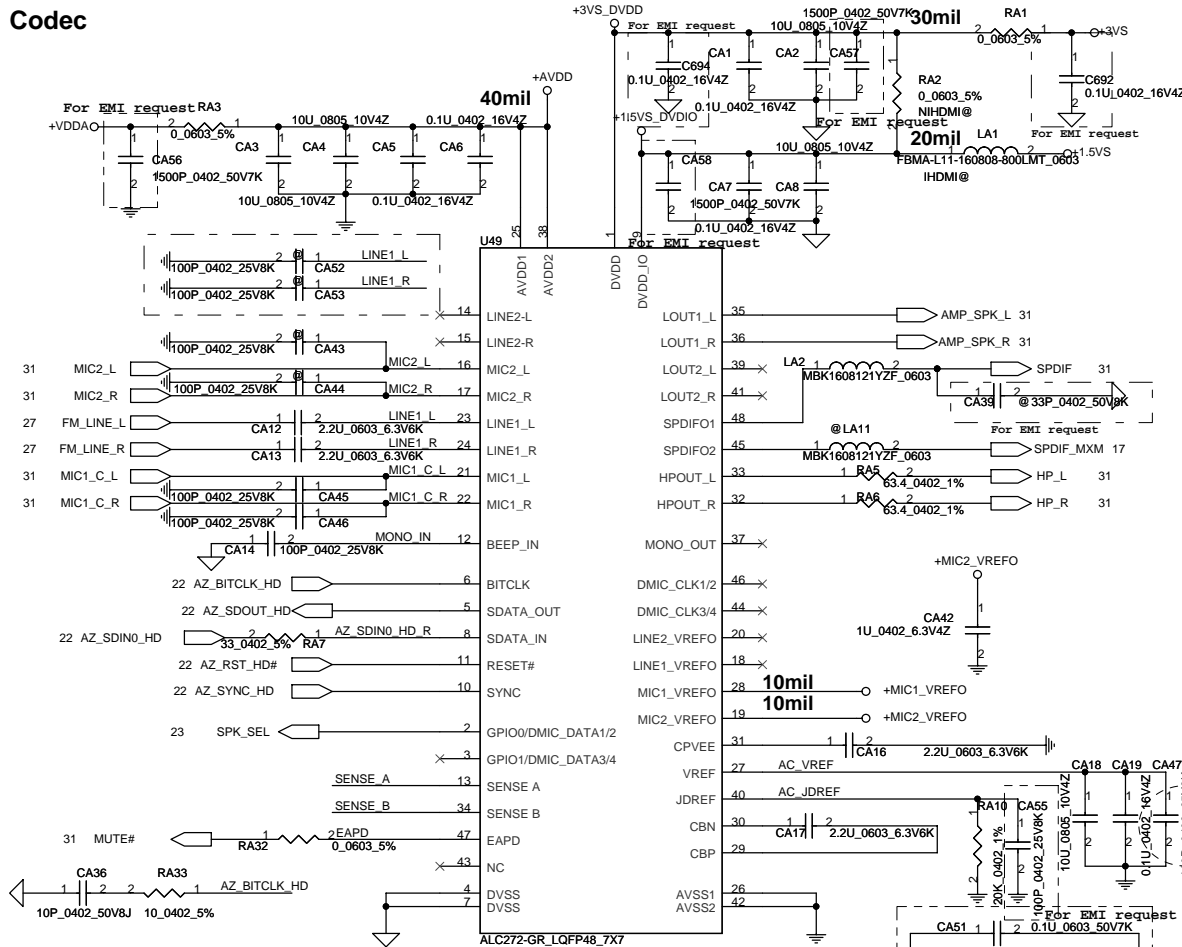
Pin	8111DL	8103EL
4	FBI2	NC
8	MDIP2	NC
9	MDIN2	NC
10	AVDD12	DVDD12
11	MDIP3	NC
12	MDIN3	NC
19	EVDD12	VDDTX
23	GPO	NC
33	EEDO	LED3
34	EEDI	LED2
35	EESK	LED1
39	AVDD12	NC
40	AVDD33	NC
43	ENSR	NC
44	VDDSR	NC
45	VDDSR	VCTRL12D
48	SROUT12	VCTRL12A



Place these components closed to LAN chip

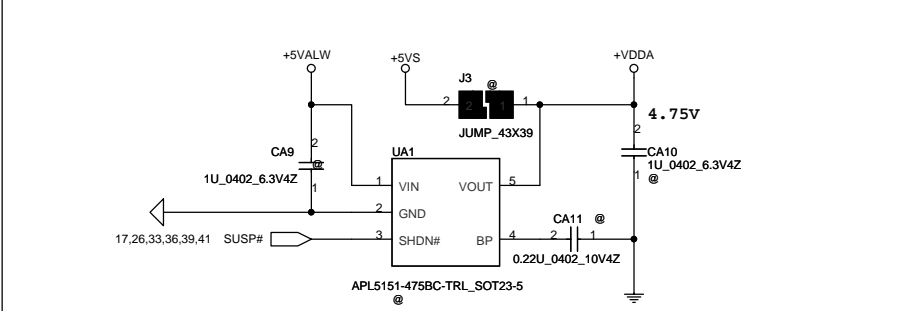


Codec

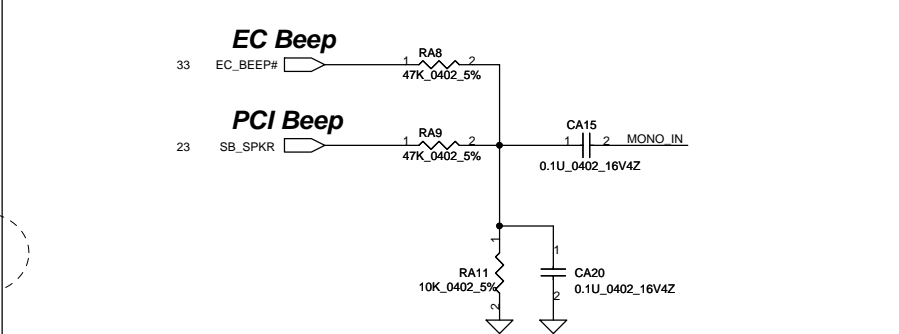


GPIO0-->SPK_SEL HIGH: HARMAN
LOW: NO-BRAND

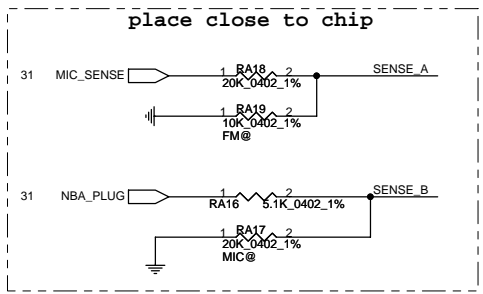
Audio regulator



Beep sound

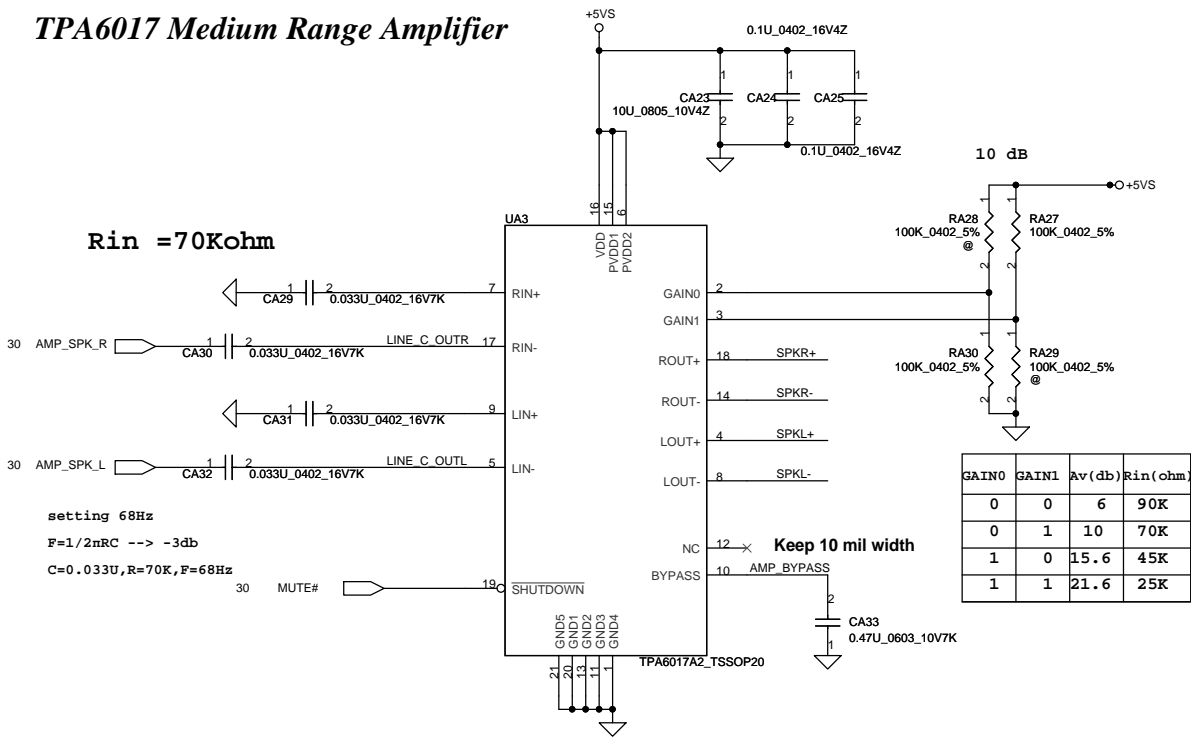


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

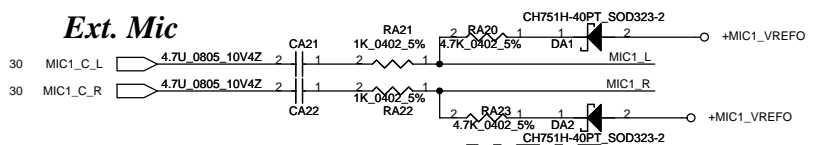


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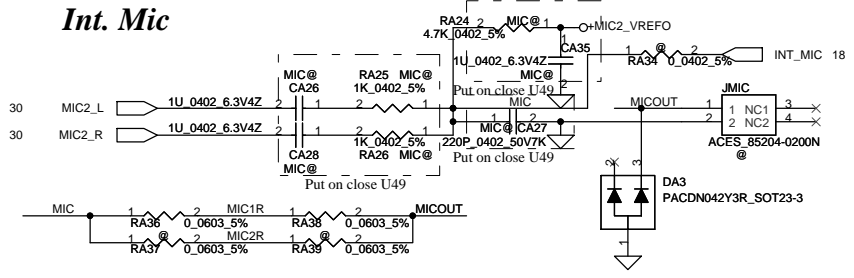
TPA6017 Medium Range Amplifier



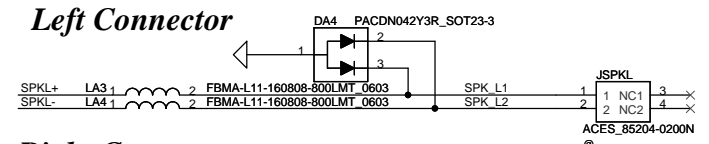
Ext. Mic



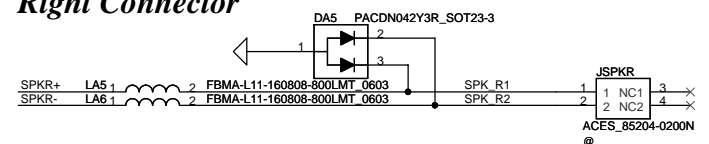
Int. Mic



Left Connector

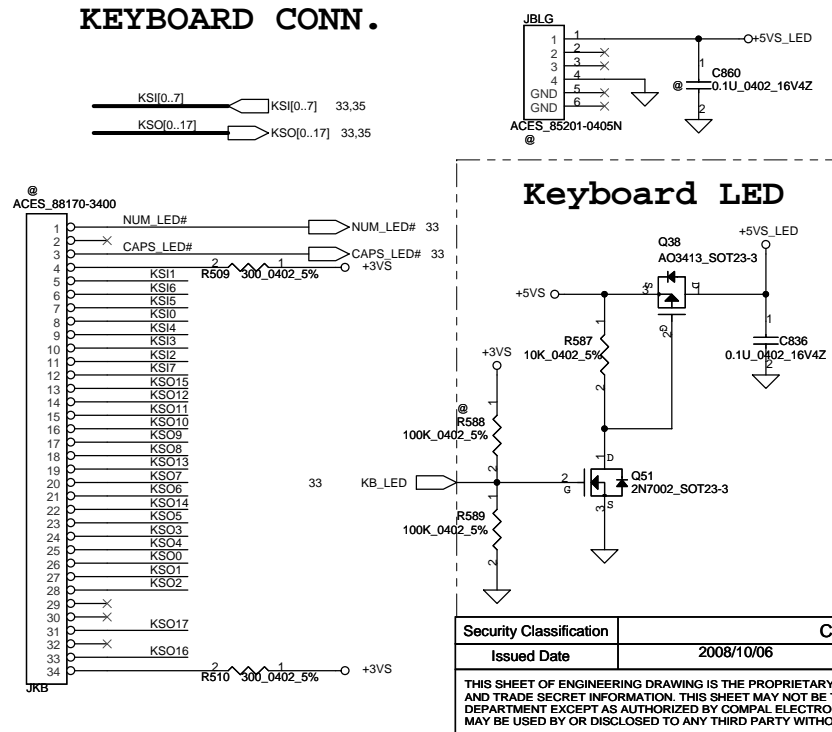


Right Connector

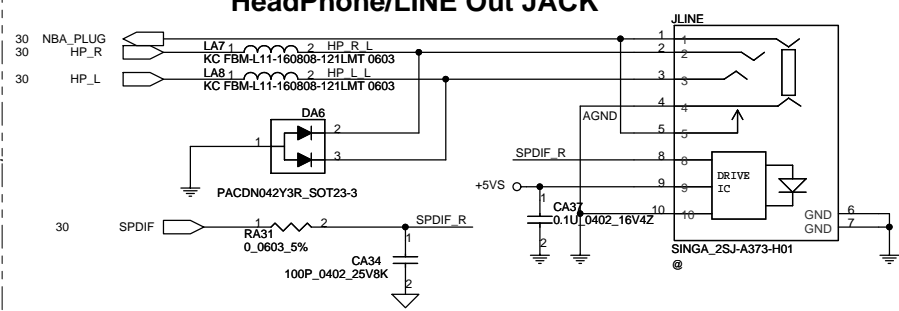


KSO10	C803	100P_0402_25V8K
KSO11	C804	100P_0402_25V8K
KSO12	C805	100P_0402_25V8K
KSO15	C807	100P_0402_25V8K
KSI7	C808	100P_0402_25V8K
KSI2	C810	100P_0402_25V8K
KSI3	C811	100P_0402_25V8K
KSI4	C812	100P_0402_25V8K
KSI0	C813	100P_0402_25V8K
KSI5	C814	100P_0402_25V8K
KSI6	C815	100P_0402_25V8K
KSI1	C816	100P_0402_25V8K
CAPS_LED#	C817	100P_0402_25V8K
NUM_LED#	C818	100P_0402_25V8K
KSO16	C809	100P_0402_25V8K
KSO17	C806	100P_0402_25V8K
KSO2	C793	100P_0402_25V8K
KSO1	C790	100P_0402_25V8K
KSO0	C791	100P_0402_25V8K
KSO4	C792	100P_0402_25V8K
KSO3	C795	100P_0402_25V8K
KSO5	C796	100P_0402_25V8K
KSO14	C797	100P_0402_25V8K
KSO6	C798	100P_0402_25V8K
KSO7	C799	100P_0402_25V8K
KSO13	C800	100P_0402_25V8K
KSO8	C801	100P_0402_25V8K
KSO9	C802	100P_0402_25V8K

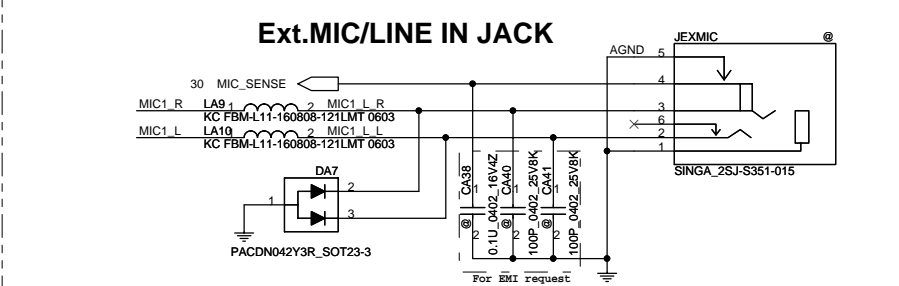
KEYBOARD CONN.



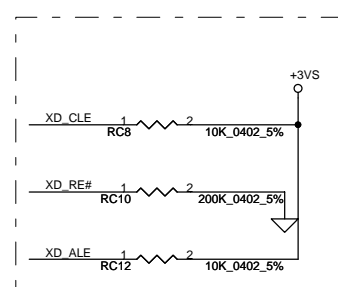
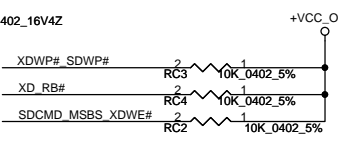
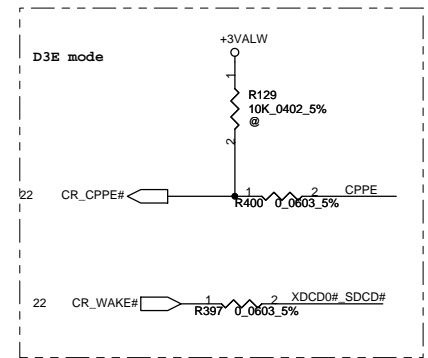
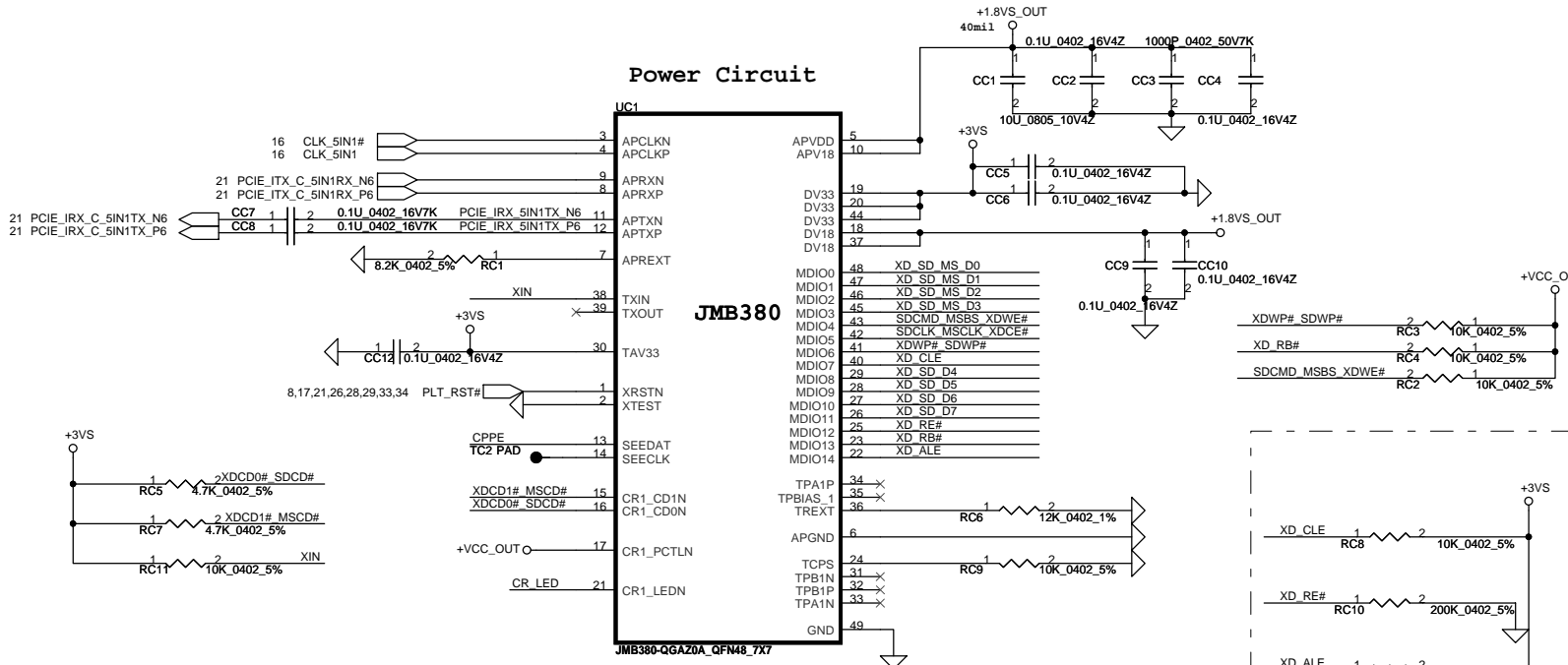
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



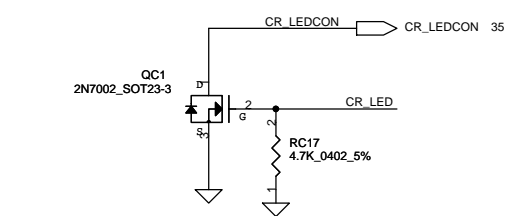
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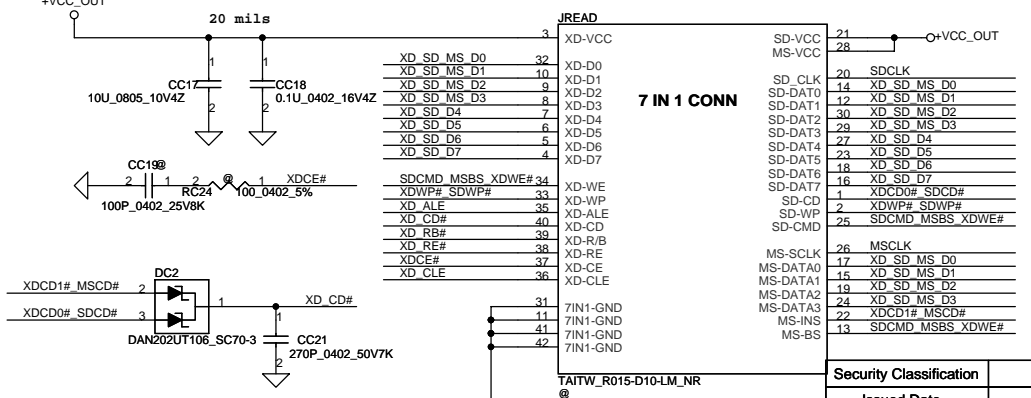
Strapping setting

Pin name	Description	
	High	low
MDIO7	on-board	add-in card
MDIO12	+VCC_OUT high active	+VCC_OUT low active
MDIO14	CR_LED high active	CR_LED low active

P.S CR1_PCTLN aslo can out 3V with 250mA for 5IN1 using.(MDIO12 can't be seted after MP IC)

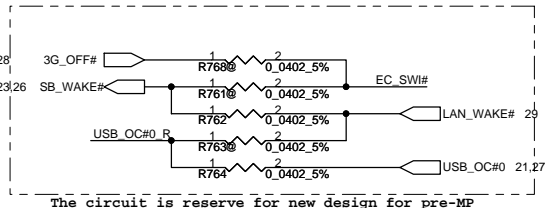
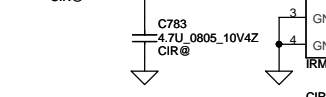
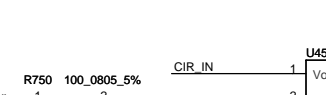
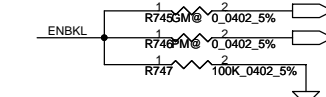
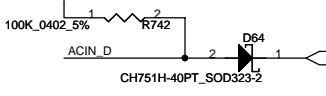
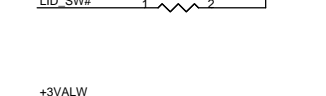
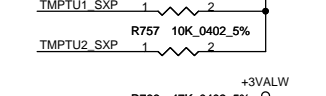
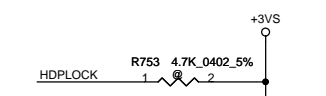
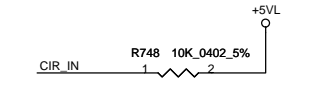
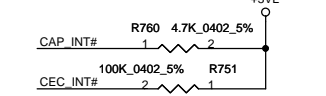
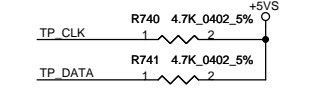
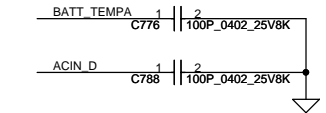
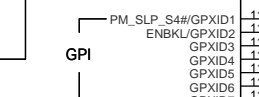
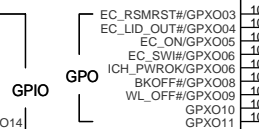
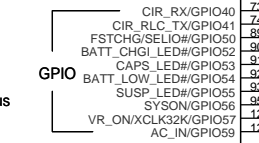
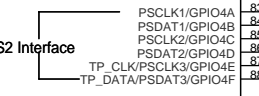
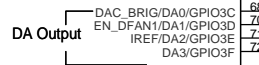
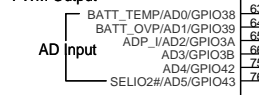
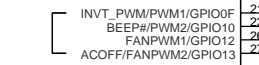
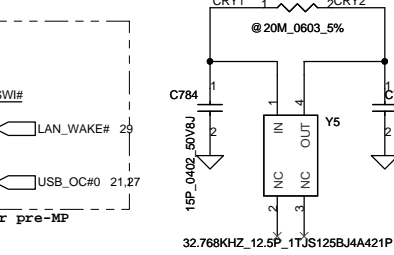
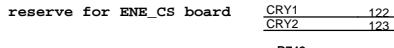
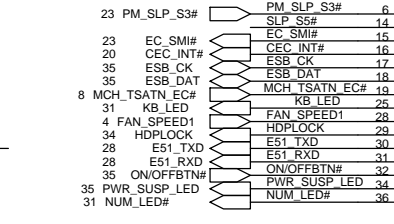
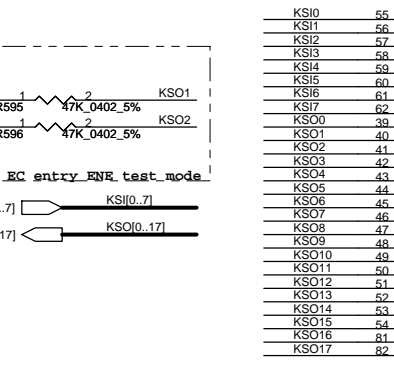
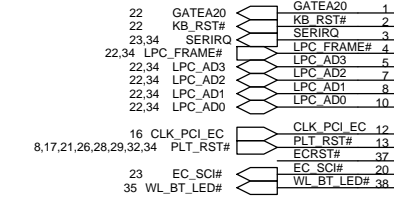
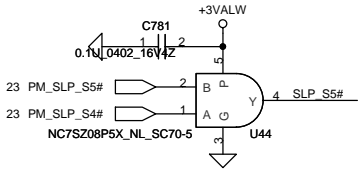
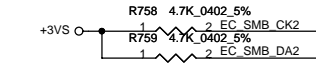
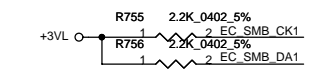
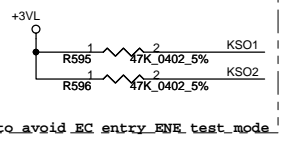
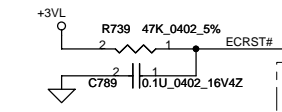
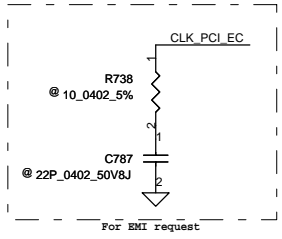
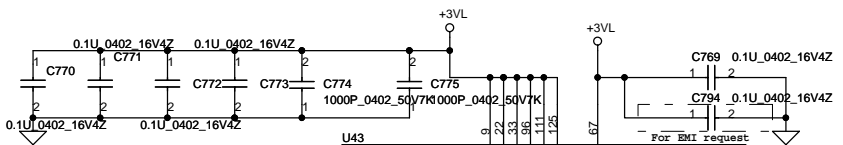


Card Reader Connector



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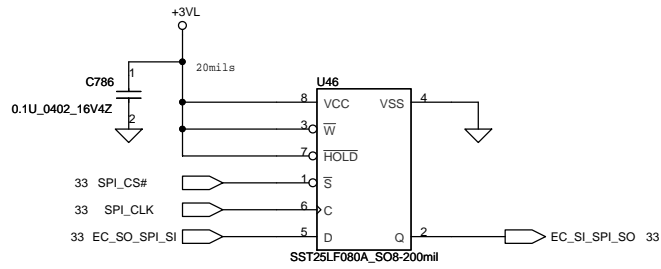


The circuit is reserve for new design for pre-MP

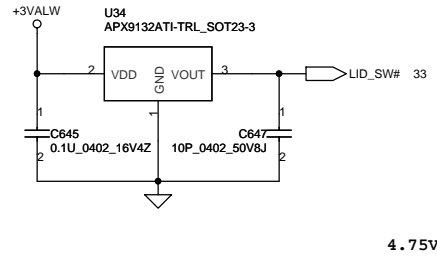
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SPI Flash (16Mb*1)

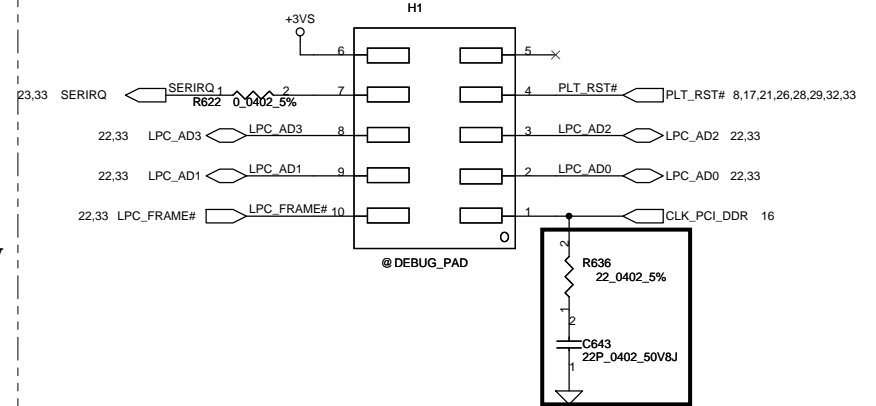


Lid SW

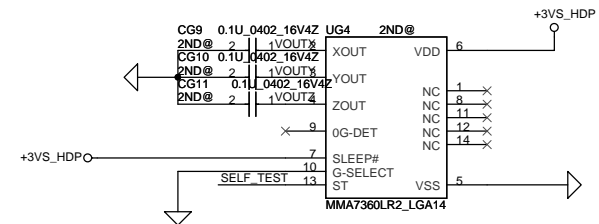
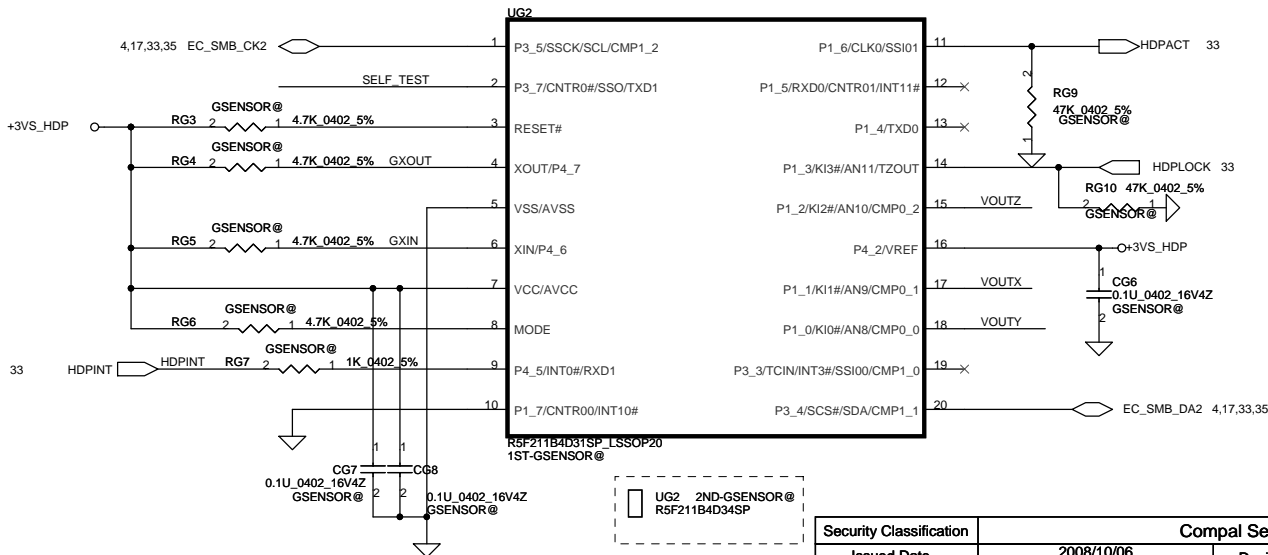
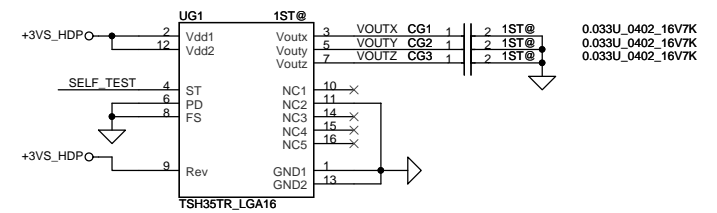
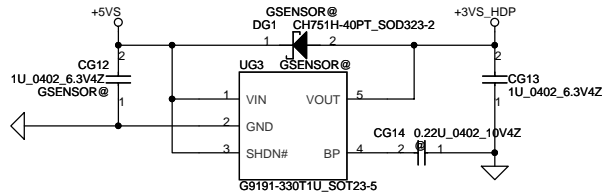
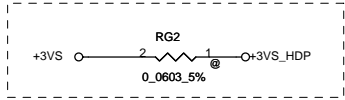


LPC Debug Port

Please place the PAD under DDR DIMM.

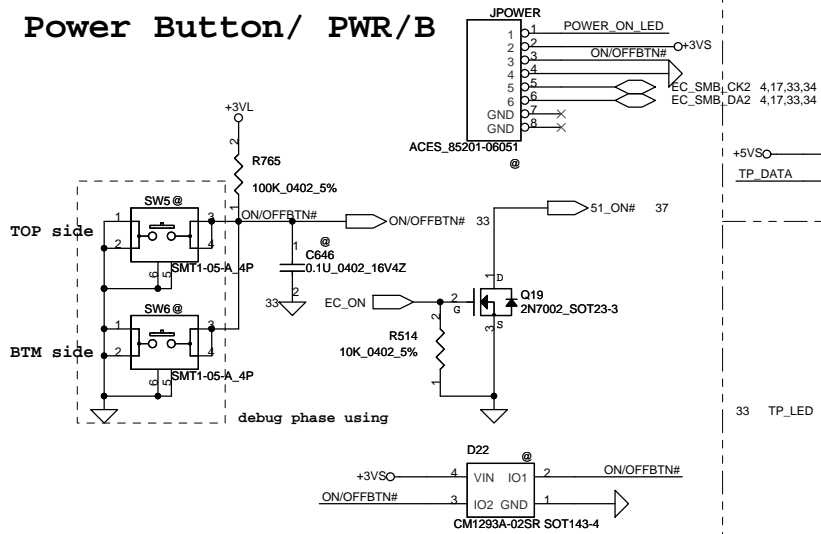


G-Sensor

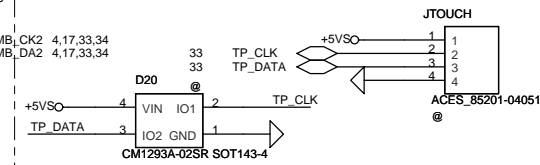


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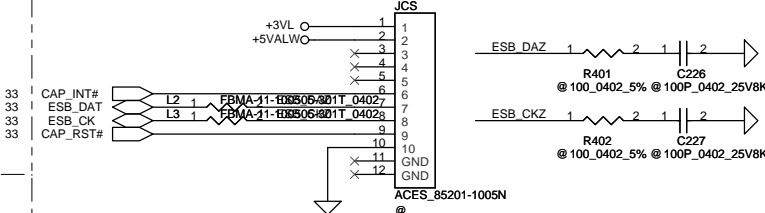
Power Button/ PWR/B



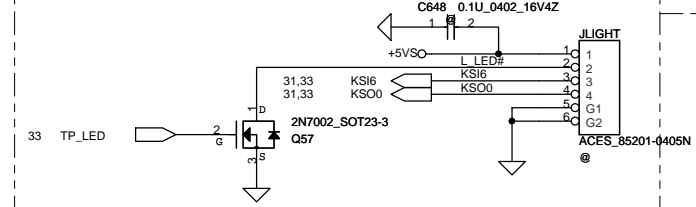
Touch/B Connector



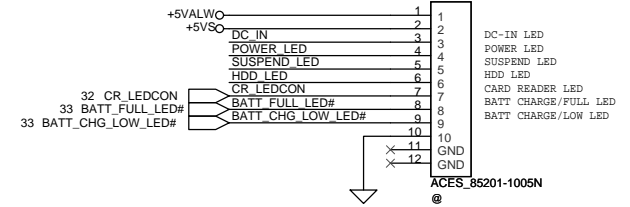
Caps Sensor Connector



Light Pipe Connector



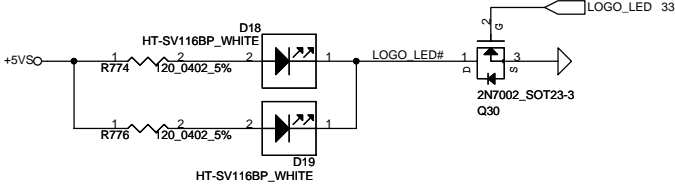
LED/B Connector



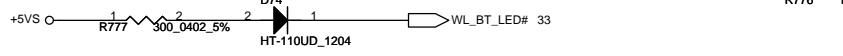
DC-IN LED



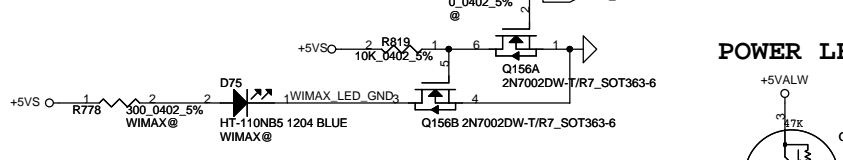
Satellite LED



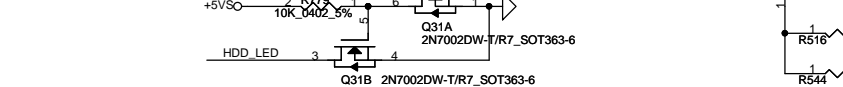
WL&BT LED



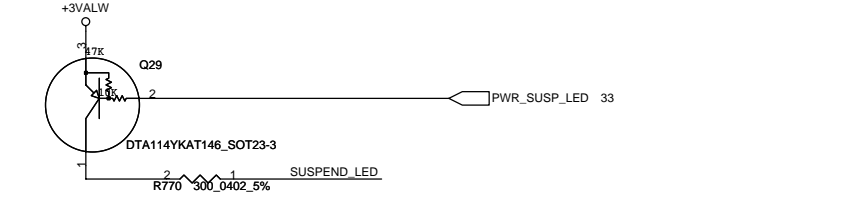
WiMAX LED



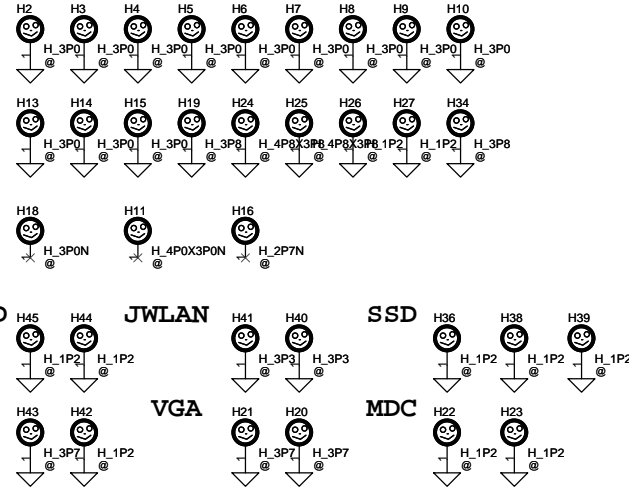
HDD LED



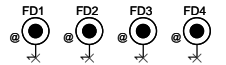
SUSPEND LED



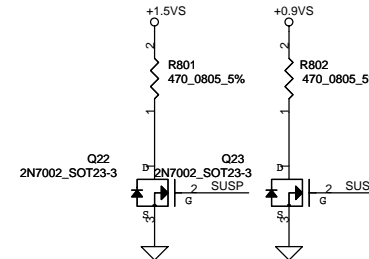
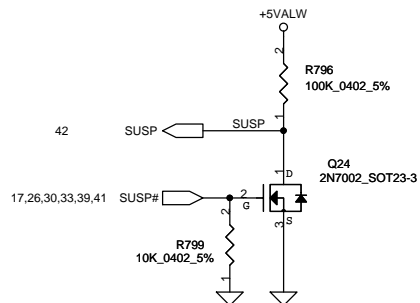
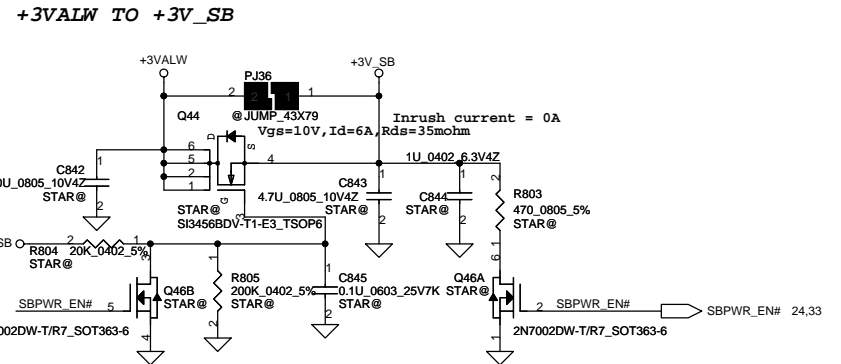
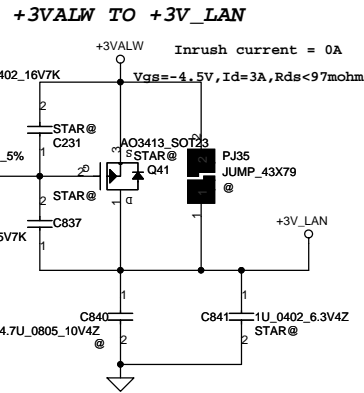
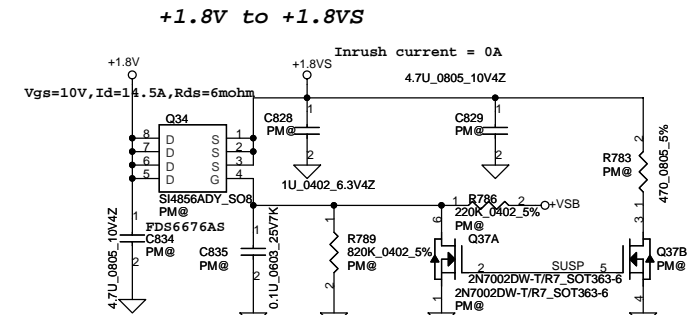
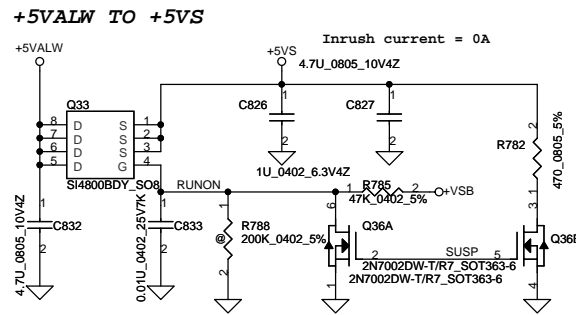
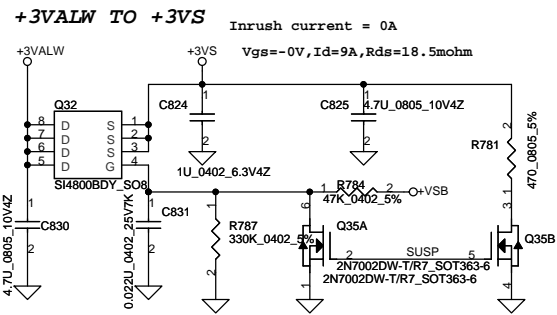
Screw Hole



PCB Federal Mark PAD

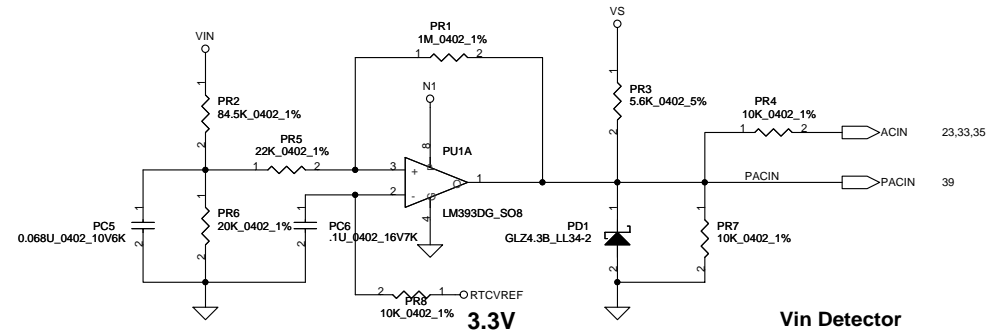
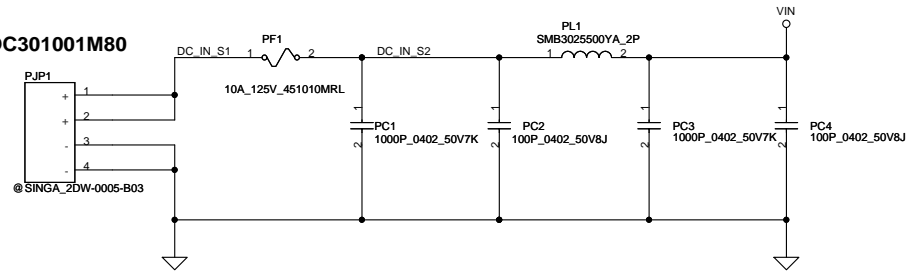


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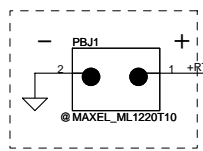
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DC301001M80

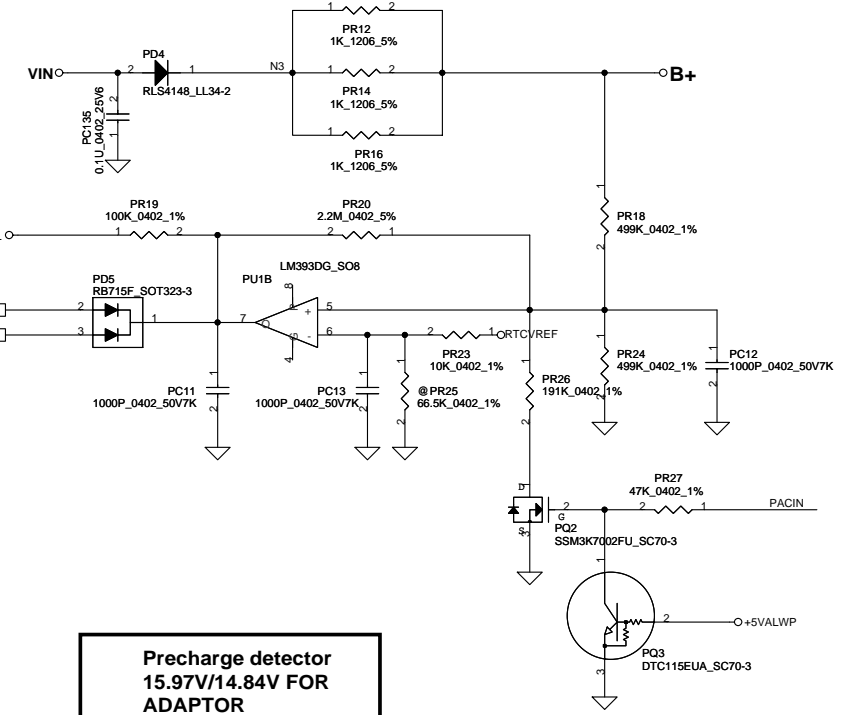
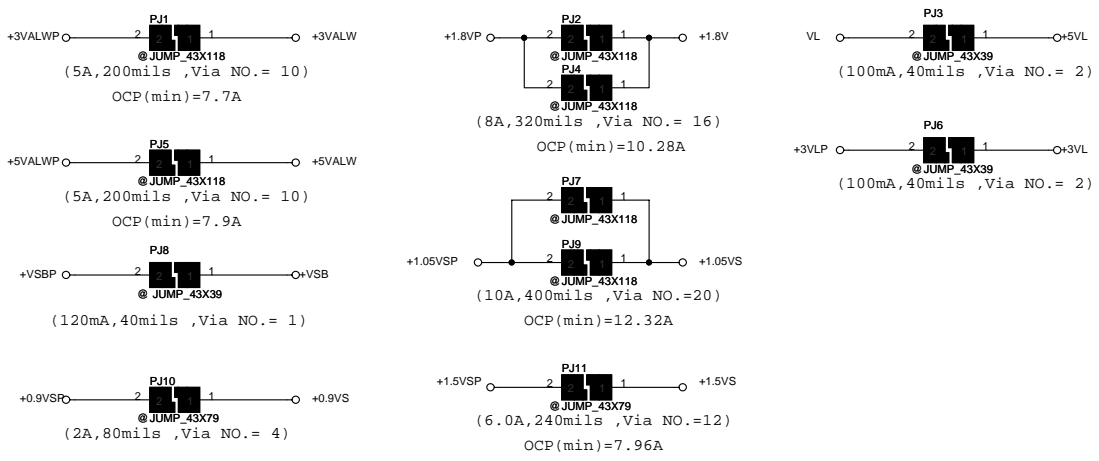
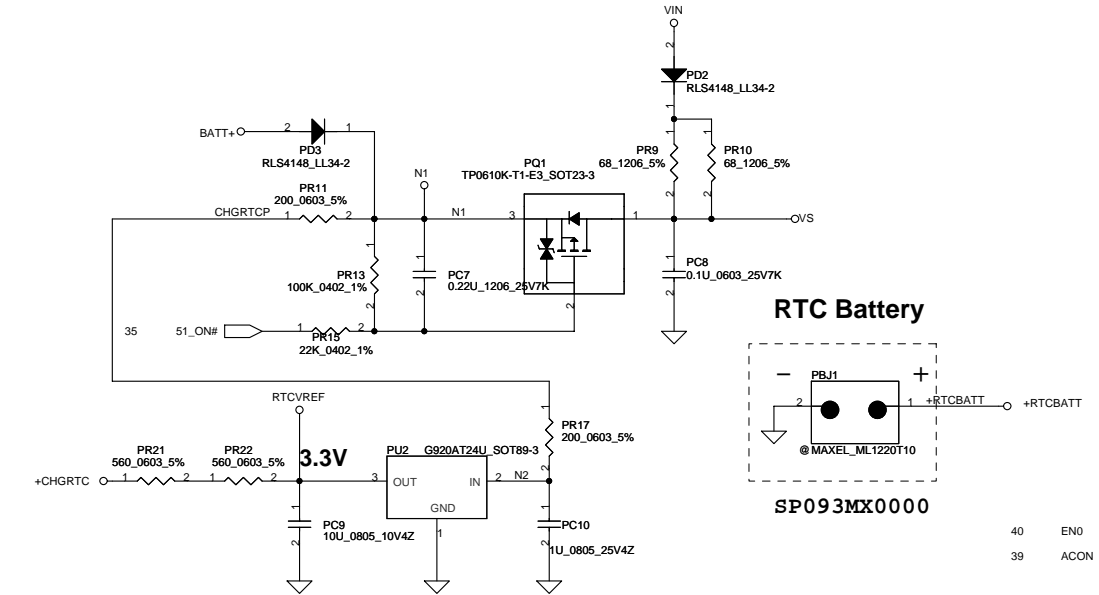


Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976

RTC Battery



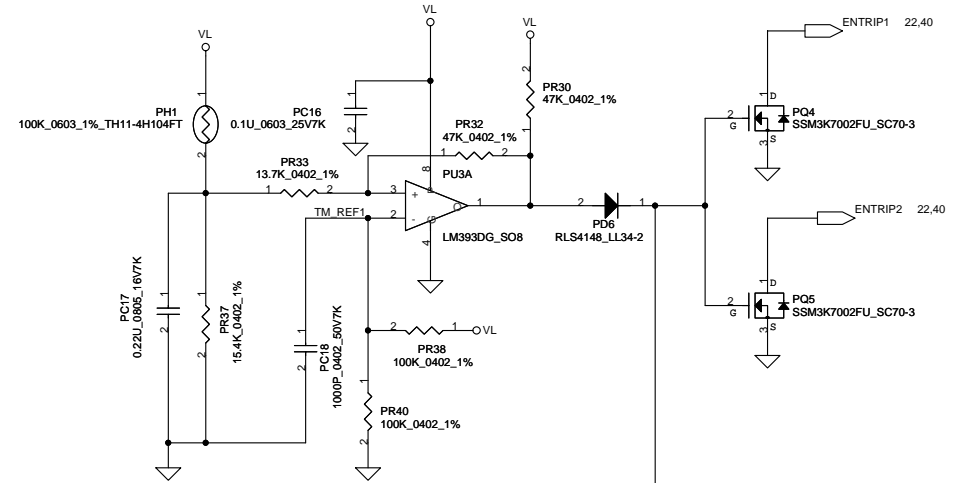
SP093MX0000



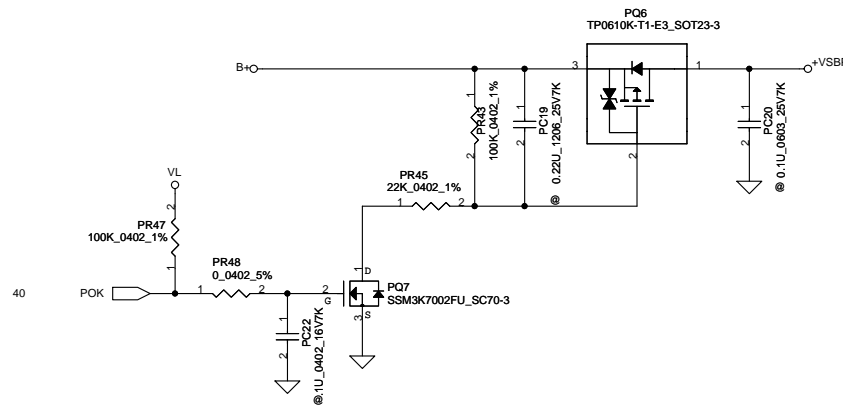
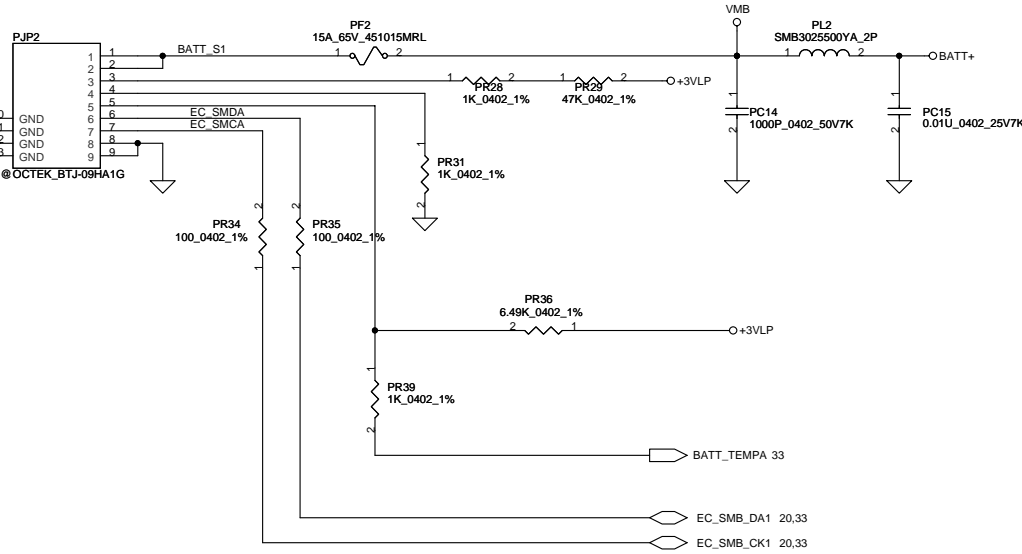
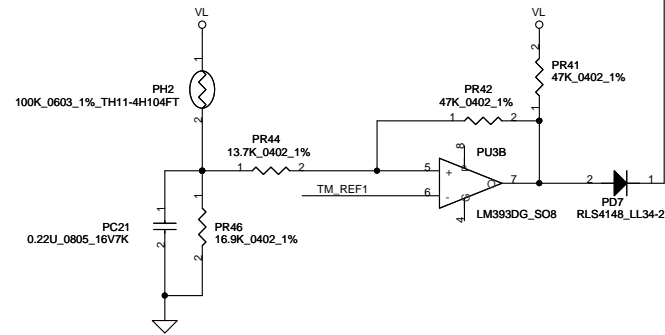
**Precharge detector
 15.97V/14.84V FOR
 ADAPTOR**

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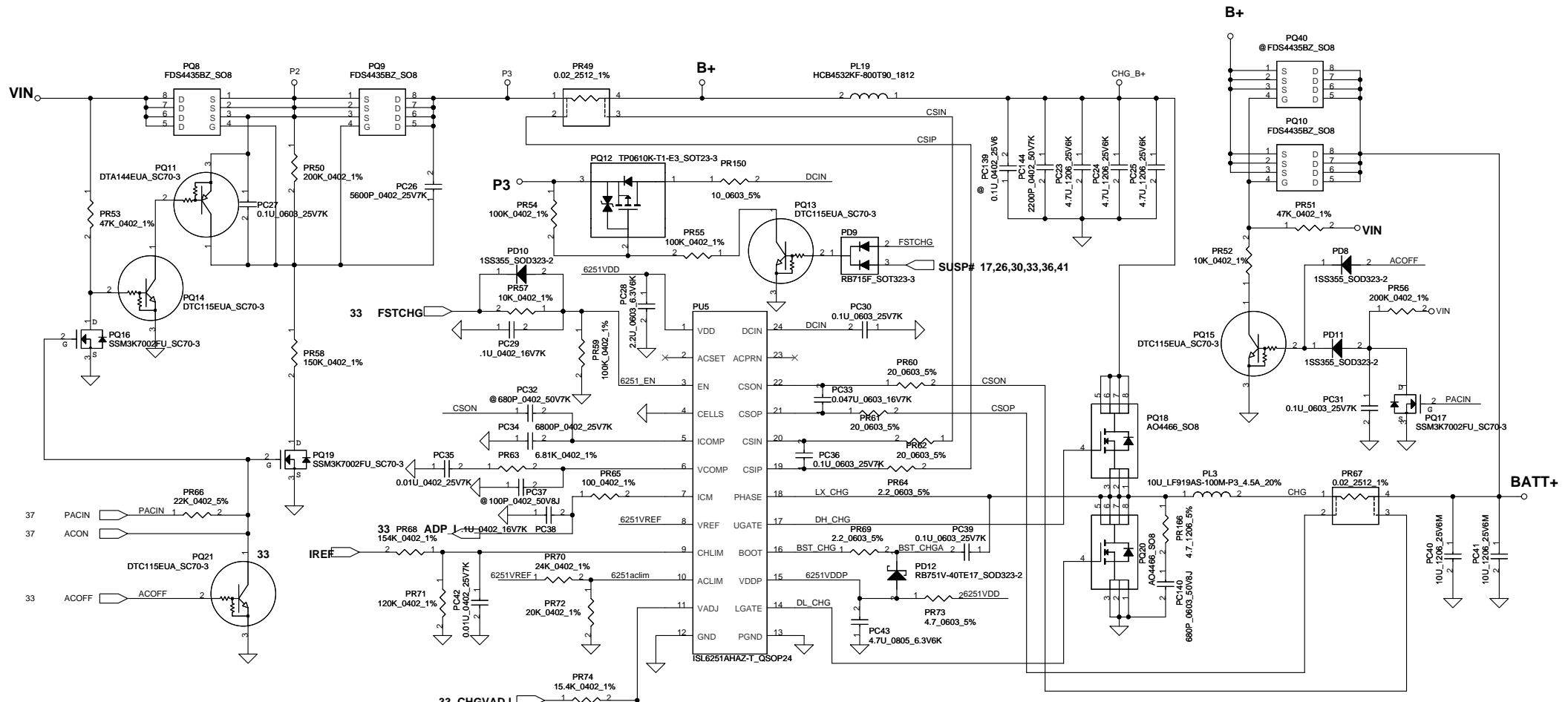
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 90 degree C
 Recovery at 53 degree C



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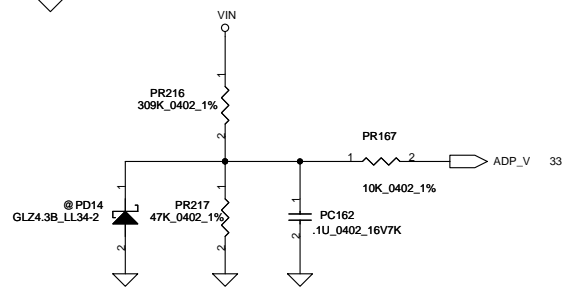
$I_{da} = 0 - 3.947A (75W) \quad CP = 92\% * I_{da}; \quad CP = 3.65A$

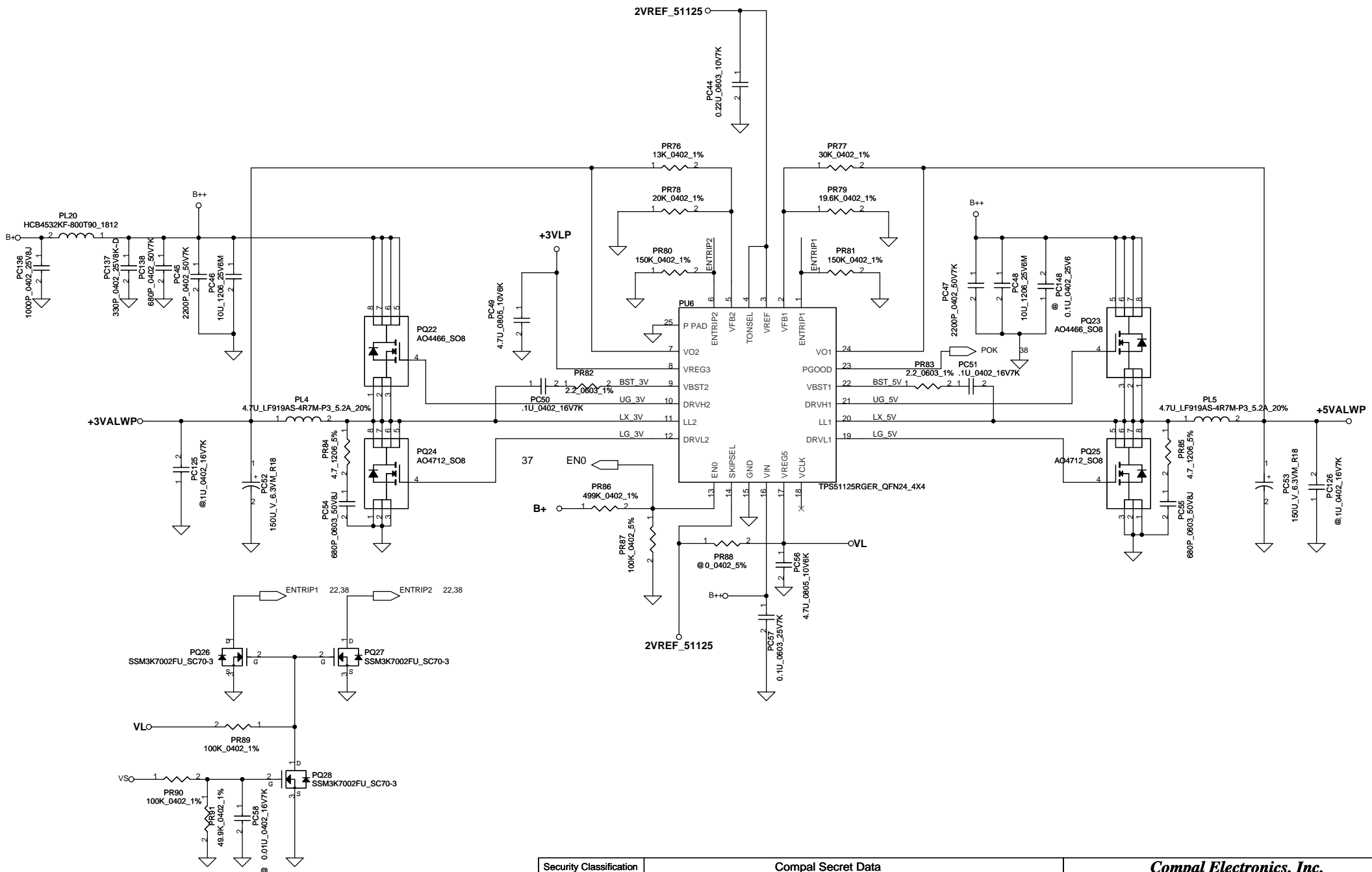
CP mode
 $V_{acLim} = 2.39 * (20K // 152K // (20K // 152K + 24K // 152K)) = 1.09986V$
 $I_{input} = (1/0.02) * ((0.05 * V_{acLim}) / 2.39 + 0.05)$
 where $V_{acLim} = 1.09986V, \quad I_{input} = 3.65A$

CC=0.25A-3A
 $I_{REF} = 1.016 * I_{charge}$
 $I_{REF} = 0.254V - 3.048V$
 VCHLIM need over 95mV

$CHGVADJ = (V_{cell} - 4) / 0.10627$	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2





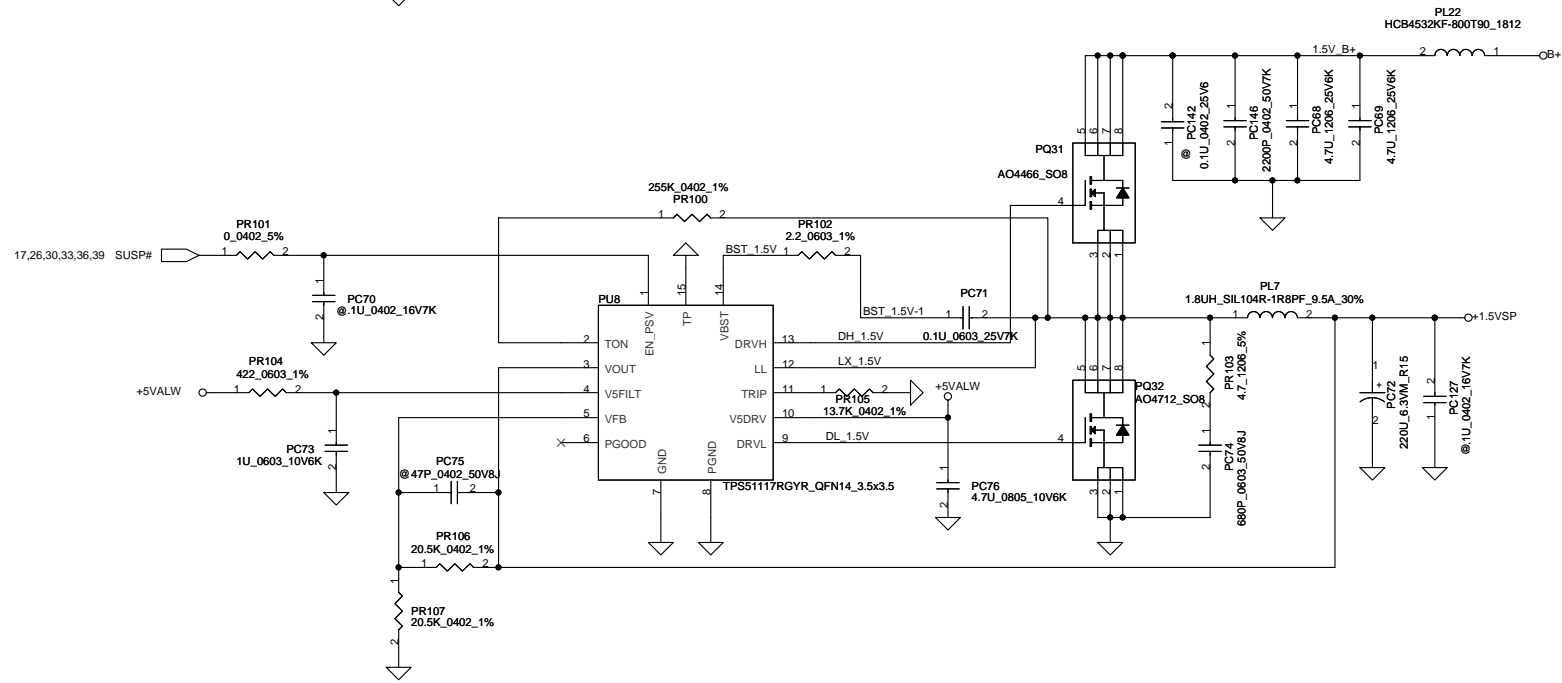
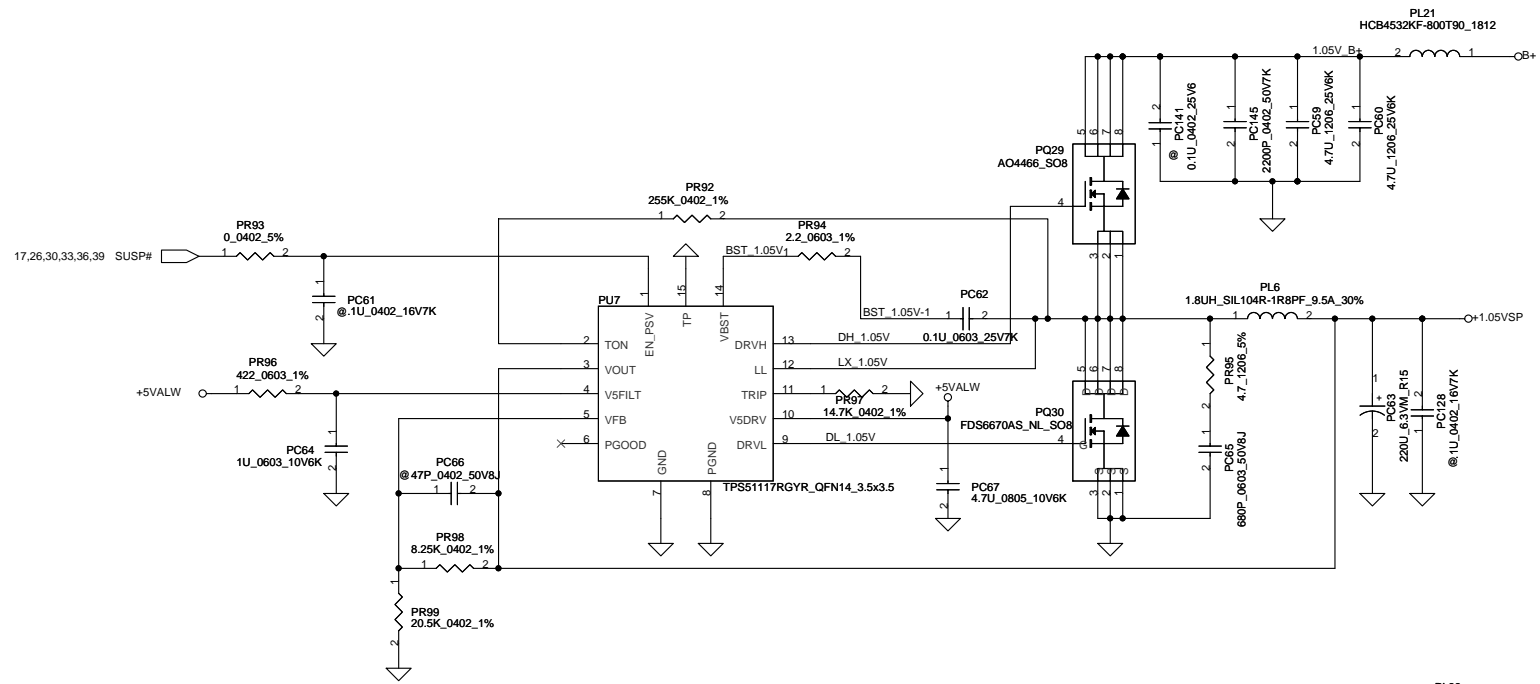
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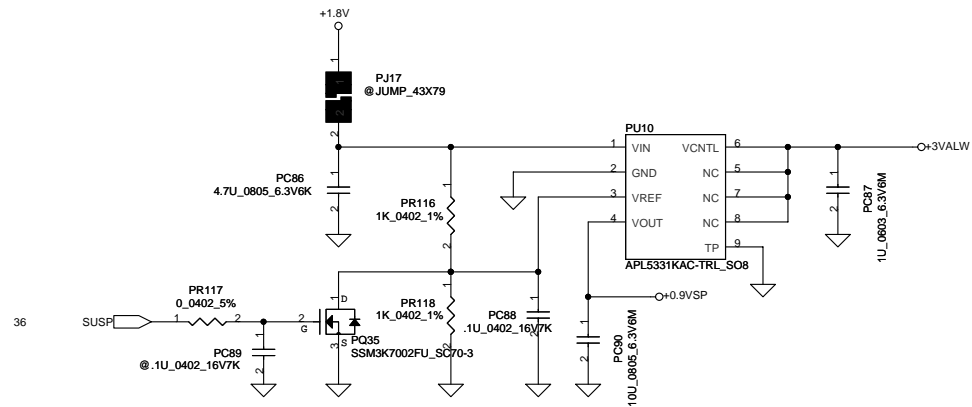
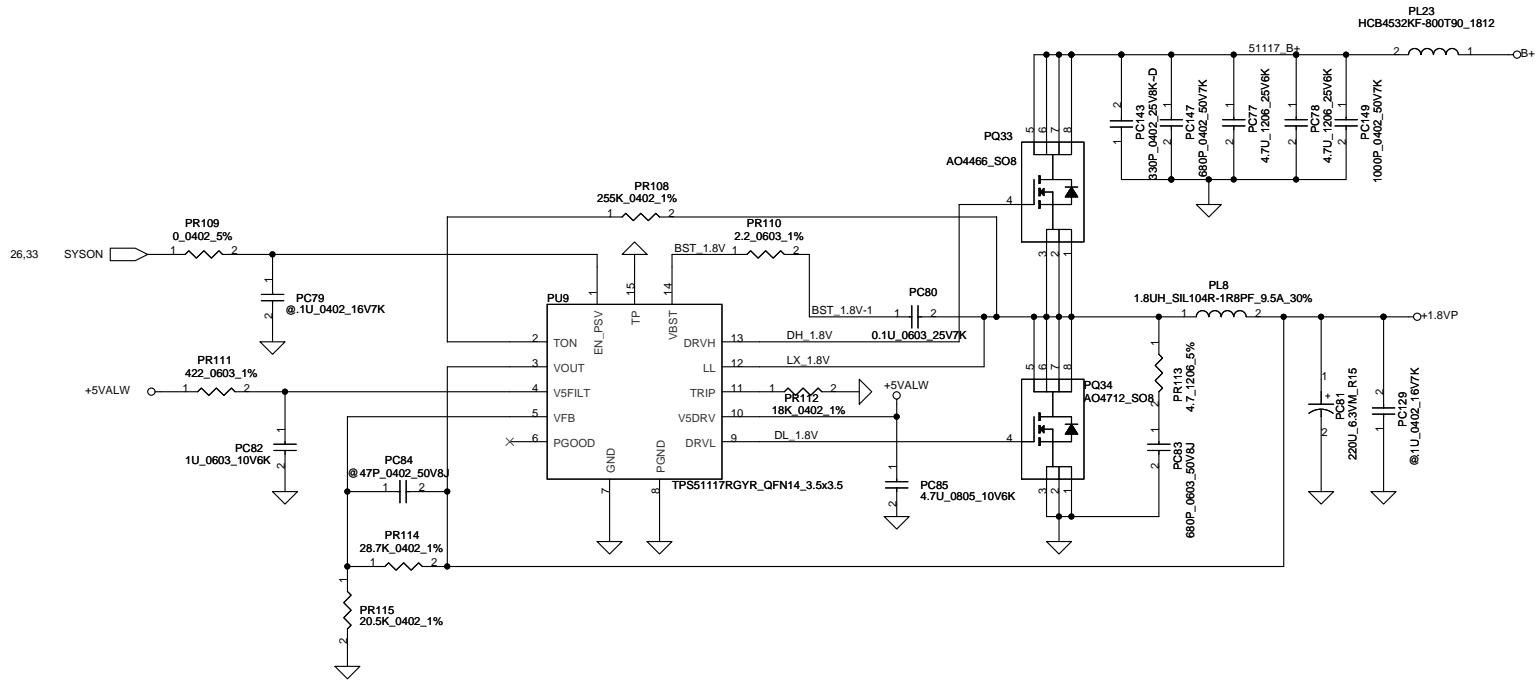
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		DCIN/DECTOR	Change location PU3A to PU1B Change ENTRIP1 to EN0 ,ENTRIP2 to ACON VL to RTCVREF in PR23 Pin6 Change PR23 to 10k ohm, PR25 to unpop Delete PD13	Circuit modify
EVT		BATTERY CONN/OTP	Change location PU4A to PU3A	Circuit modify
EVT		+CPU_CORE	Add PR137 0ohm_0402,PR154 0ohm_0402	Circuit modify
EVT		3VALWP/5VALWP	Change PR82 and PR83 to 2.2ohm Add PC136 1000P_0402,PC137 330P_0402, PC138 680P_0402	EMI request
EVT		1.8VP/0.9VSP	Change PR110 to 2.2ohm	EMI request
EVT		+CPU_CORE	Change PR140 and PR144 to 2.2ohm, PL9 to FBMA-L11-453215-121LMA90T_2 Add PC131 0.1U_00402,PC132 680P_0402, PC133 330P_0402, PC134 1000P_0402 PC102 680P_0603,PC111_680P_0603 PR134 4.7ohm_0402,PR146 4.7ohm_0402	EMI request
EVT		CHARGER	Change PR70 to 24k ohm	Circuit modify for 75W
EVT		CHARGER	Change PL3 to 10UH_4.5A_20%,PR71 to 120Kohm	Circuit modify
DVT		1.8VP/0.9VSP	Add PC143 330P_0402,PC147 680P_0402 PC149 680P_0402	EMI request
DVT		CHARGER	Add PC139 0.1U_0402, PC144 2200P_0402, PC140 680P_0603,PR166 4.7ohm_0603 Change PR69 to 2.2 ohm	SED request
DVT		3VALWP/5VALWP	Add PC148 0.1U_0402,PC54 680P_0603, PC55 680P_0603,PR84 4.7ohm_1206, PR85 4.7ohm_1206	SED request
DVT		1.05V/1.5V	Add PC141 0.1U_0402, PC142 0.1U_0402, PC145 2200P_0402,PC146 2200P_0402, PC65 680P_0603,PC74 680P_0603, PR95 4.7 ohm_0402,PR103 4.7 ohm_0402 Change PR94 and PR102 to 2.2 ohm	SED request
DVT		1.8VP/0.9VSP	Add PC143 0.1U_0402,PC147 2200P_0402, PC83 680P_0603,PR113 4.7 ohm_0402	SED request
DVT		CHARGER	Change PR71 to 120k ohm	Circuit modify
DVT		CHARGER	Change PR70 to 75k ohm	Circuit modify for 65W
DVT		+CPU_CORE	Change PR145 to 11.3k ohm	Circuit modify
PVT		DCIN/DECTOR	Change PU1 Pin8 from VS to N1	Circuit modify
PVT-3		DCIN/DECTOR	Change PC135 from 0.1U_0402_16V to 0.1U_0402_25V	Circuit modify
PVT-3		CHARGER	Change PR74 to 15.4k ohm Change PJ12 to PL19,add PR167 10K ohm	Circuit modify
PVT-3		3VALWP/5VALWP	Change PJ13 to PL20	Circuit modify
PVT-3		1.05V/1.5V	Change PJ14 to PL21,Change PJ15 to PL22	Circuit modify
PVT-3		1.8VP/0.9VSP	Change PJ16 to PL23	Circuit modify

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PIR (Product Improve Record)

KSKAA LA-4991P SCHEMATIC CHANGE LIST
REVISION CHANGE:

Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/12	4	Add R14	Spec requestion
2	12/12	8	Add U3.N28-->DP_CLK and U3.M28-->DP_DATA	support dongle
3	12/12	10	Add R97,Q27,U13,U14	support dongle
4	12/12	12	Add C225	For EMI reserv
5	12/12	23	Add J3	For cost down
6	12/12	19	Add Q160A/B,Q158A/B, Q159A/B,RV42,RV38,Rv45,CV59	Support dongle
7	12/12	19	Add RV107	
8	12/12	23	Change HDMI_HPD_R to VGA_HDMI_R from U9C.C21 to D58.2	power connect error
9	12/12	32	QC1 Stuff	For card reader LED display
10	12/12	33	Change R758 and R759 from 2.2K to 4.7K	Request reference voltage
11	12/12	34	Change Gsenser LDO solution==>UG1,DG1,CG11,CG12,CG13	For cost down
12	12/12	35	Change JPOWER from 4pin to 6pin	Add light sensor circuit for test
13	12/12	35	Change L2,L3 use FBMA-121-100505-301T_0402	Caps sensoe EMI reserve
14	12/12	35	Add R401,R402,C226,C227	Caps sensoe EMI reserve
15	12/12	36	Change C835 from 0.1uf to 0.22uf	For power sequence

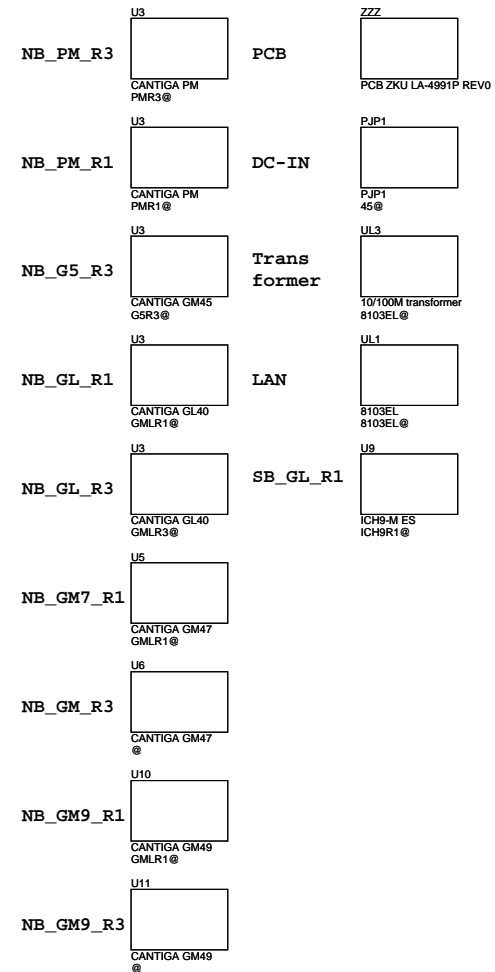
Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/24	16	Change R107,R108 use (FBMH1608HM601)BEAD	For SED team request
2	12/24	16	Change C212,C219 from 0.1uf to 47pf	For SED team request
3	12/24	16	Add C228,C229,C230	For SED team request
4	12/24	19	Add Q52	For UMA display port use
5	12/24	20	Add Q13,Q39,R290,R262,R204,R220,R958,C65	For CEC function
6	12/24	27	Delete Q26 and change R432 from 1M to 100K, R441 from 100K to 1K	Correct BT schematic
7	12/24	29	Change CM1,CM4,CM17,CM20 from 0.01uf to 47P	For SED team request
8	12/24	33	Change HDPDP netname to HDPLOCK and HDPACT to HDPINT	For customer request
9	12/24	34	Add RG2,RG10 and change 2ND source	For customer request
10	12/24	34	Change UG1.6 pull down and UG3.3 from GND to +5VS	For customer request

Revision Change: 0.3 to 0.4

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	02/02	35	Change Q29.3,Q42.3 from +5VALW to +3VALW	For suspend LED breathing concern
2	02/02	17	connect JMXMB.158 via a bead(SM010032020) to U49.45	For VGA SPDIF request
3	02/02	17	Reserve JMXMB.134 for HDA_RST	For VGA SPDIF request
4	02/02	34	UG2 from R5F211B4D23SP to R5F211B4D31SP(SA000037Y60)	For cost down request
5	02/02	20	U8 from R5F211A4C32SP to R5F211B4D33SP(SA000037Z70)	For cost down request
6	02/02	33	Change U43.79,U43.80 pull high from +3VS_HDP change to +3Vs	For G-Sensor issue
7	02/02	27	ADD R293 R294 for Camera output to LVDS	For Camera issue
8	02/02	20	Change Q39 , Q13 footprint	Due to footprint error
9	02/02	17	DELETE R185,R217,R218,R227,R275,R105,R187,R188,R790,R791	For Display port issue
		17	ADD CV62,CV63,CV64,CV65,CV66,CV67,CV68,CV69	
		19	ADD RV89	
10	02/02	34	ADD D16,R794	For ESATA surrport charge on S4/S5
11	02/02	31	CA35 Move to RA24 right side	For MIC issue
12	02/02	27	JFMI change to JFM	For common design request
13	02/02	28	JUWB change to JNAND	For common design request
14	02/04	19	DELETE D20 ,ADD Q162	For Display port change design

ISPD



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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Schematic, MB A4991	
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KSKAA LA-4991P SCHEMATIC CHANGE LIST
 REVISION CHANGE:

Revision Change: 0.3 to 0.4

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
15	02/04	18	ADD C267	For LVDS change PMOS Design
16	02/04	26	ADD C486	For B-CAS change PMOS Design
17	02/04	20	DELETE D8,D53 ,ADD Q161,R130,C876	Change HDMI design
18	02/04	27	ADD C232,C233	For Blue tooth and Felica change PMOS Design
19	02/04	34	unmount RG2 ; mount CG12,DG1,UG3,CG14,CG13	For G-Sensor Design change
20	02/04	36	ADD C837	For +3VALW -> +3V_LAN Change PMOS Design
21	02/04	26	unmount RN4,RN5,CN7,UN2,Q21 ; mount RN6	For cost down
22	02/04	30	DELETE UA1,CA11	For cost down
23	02/04	19	DELETE R134,R135,L6	For EMI Request
24	02/04	30	DELETE R204,R220	For HDMI issue
25	02/04	19	Modify JBLG footprint to ACES_85201-0405N_4P	For KB Bcaklight
26	02/05	33	exchange U43.25 , U43.26	For Backlight KB issue
27	02/05	26	JEXP USB20_N8,USB20_P8 Change to USB20_N4,USB20_P4	For design change
28	02/05	27	JFP USB20_N4,USB20_P4 Change to USB20_N8,USB20_P8	For design change
29	02/05	35	D20,D22	For EMI request
30	02/05	27	D21	For EMI request
31	02/05	31	C860	For EMI request
32	02/05	25	Change D15 PN to SC300000P00	For EMI request
33	02/05	31	Change DA4,DA5,DA6,DA7 PN to SCA00000G00	For EMI request
34	02/05	30	Change CA36 to 10p ,RA33 to 10 ohm	For EMI request
35	02/05	30	C694	For EMI request
36	02/05	20	HDMI CEC schematic modify	Cut-in New Design
37	02/06	10	ADD C644,C649,R204,R217,R218,R188,R135	For Display port issue
38	02/05	30	Modify J3 Footprint to JUMP_43X39	For Design request
39	02/05	28	Modify J3GSIM footprint to MOLEX_47273-0001_6P-S	For ME request
40	02/07	19	Remove RV45 ,RV81 Change to 1Mohm	For Display port issue
41	02/07	10	U13.2 Change DP_AUX_NB to DP_AUX U13.5 Change DP_AUX#_NB to DP_AUX#	For Display port issue
42	02/07	10	U14.2 Change DP_AUX_NB to DP_AUX U14.5 Change DP_AUX#_NB to DP_AUX#	For Display port issue
43	02/07	10	R797.2 Change DP_HPD_NB to DP_HPD	For Display port issue
44	02/10	26	change JBCAS1 connect method	For B-CAS issue
45	02/10	33	ADD D4	leakage electircity issue
46	02/10	28	Change JWLAN +3VS->+3V_LAN	For Design change
47	02/10	28	ADD PJ18,PJ19	For Design change
48	02/10	19	Remove RV37,RV79	For Display port issue
49	02/10	10	ADD R135	For Display port issue
50	02/10	8	ADD RA35,CA43	For HDMI noise issue
51	02/10	20	ADD R220,Q26,R558,C861	Cut-in New design
52	02/11	20	Change R156 to 4.12kohm	For HDMI issue
53	02/11	20	UV12.1,UV12.5 don't connect	For design issue
54	02/11	28	RM6.2 change to +3VS	For design issue
55	02/11	20	C861 footprint change to 0603	For design issue
56	02/11	29	UL3 PN -> SP050005L00	For EMI request
57	02/11	34	UG1 PN -> SA000039900	For customer request
58	02/11	32	Remove 1394 function	For customer request

Revision Change: 0.5 to 0.6

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01	04/01	32	Replace JMB380 to JMB385	Layout placement high limit
02	04/01	32	Remove RC11, add RC2,XC1,RC6,CC11,CC13	Replacement JMB380
03	04/01	32	Remove J1394,RC20,RC21,RC22,RC23,CC16,RC19,CC20	Remove 1394 , request from customer
04	04/01	19	Remove Q162, Add D23	Customer request
05	04/01	29	Change CL43 connect to JLAN pin12	For common design with KSKAE
06	04/01	29	Change CL44 connect to JLAN pin10	For common design with KSKAE
07	04/01	18	Change R673 from 0 to 10K	For common design with KSKAE
08	04/01	27	Change R722 from 0 to 100K	For common design with KSKAE
09	04/02	20	Remove Q161,Q26,R220,R558,C861, Add D53	For common design with KSKAE
10	04/02	28	Add R825	ES Status review
11	04/02	32	Remove CC11, CC13, XC1, RC2, RC6, RC9	For common design with KSKAE
12	04/03	30	Add CA56, CA57, CA58	FOR EMC status update
13	04/03	32	Add RC2, RC6, RC9, RC11	FOR JMB380 W/O 1394
14	04/06	20	Change U7 from STHDLS101TQT to CH7318C-BF	FOR HDMI fuction measure
15	04/06	20	Change L9,L10,L11,L12 from WCM-2012-900T to WCM-2012-121T	FOR EMI request
16	04/06	27	Change R722 from 10K ohm to 0ohm	Need meet Blue tooth spec

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KSKAA LA-4991P SCHEMATIC CHANGE LIST
 REVISION CHANGE:

Revision Change: 0.4 to 0.5

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01	03/14	18	Change R103 from 100K to 10K with BKOFF#	To solve some panel still have white screen when insert and un-insert AC adapter
02	03/14	18	Mount R431 and un-mount R429	For LVDS connector with camera power to +5VS For design change
03	03/14	20	Change U8 net for HDMI_SCLK/SDATA to HDMI CLK/DATA to CEC	For wrong connect impact leakage current
04	03/14	20	Change R570 from 100K to 10K	To avoid low voltage when insert HDMI device
05	03/14	20	Change C861 floorprint from 0603 to 0402	For common design with KSWAA
06	03/14	21	Change R794 connect to D16 pin1	For wrong pull-up rail of USB_OC#2
07	03/14	21	Exchange U9 USB port4 and port8	For customer request
08	03/14	23	Add U47,R227,C234 and remove D4	For CMOS discharge fail
09	03/14	25	Mount C350 and unmount C353	For USB power function
10	03/14	26	Change RN1 and RN2 pull high from +3VALW to +3V_SB	For common design with KSWAA
11	03/14	27	Add R428 with 0ohm for reserve +5VALW	For use module on camera connector & LVDS connector
12	03/14	27	JFM inverse connection	For pin no match with MB and cable
13	03/14	28	Connect to JGPS.49 and JGPS.51 reserve	To avoid some issue happen
14	03/14	28	Unmount RM3	For common design with KSKAE
15	03/14	28	un-mount RL3 with +3V_LAN for LAN_WAKE#	For common design with KSKAA
16	03/14	30	Add CA43,CA44,CA45,CA46,CA52,CA53 on codec input/power pins	For common design with KSKAE
17	03/14	31	Add R790,R791,R792,R798 with 100ohm	For speaker ouput voltage to high
18	03/14	31	Change Q38 from SI2301BDS to AO3413 and change R587 from 100K to 10K	For use module on camera connector & LVDS connector
19	03/14	32	Add RC9 with 10K	For common design with KSKAE
20	03/14	32	Change schematic design from JMB380 to JMB385	For customer change spec
21	03/14	33	R751 pull-up to +3VL of CEC_INT#	For common design with KSKAE
22	03/14	33	Change R755 and R756 from 4.7K to 2.2K and pull up +3VL	For common design with KSKAE
23	03/14	33	Exchange HDPINT and HDPACT	For G-sensor function work normal
24	03/14	33	un-mount R788 for +5VS power switch	For reduce inrush current
25	03/14	33	Add R761,R762,R763,R764	To prevent voltage leakage in S5
26	03/14	34	Change UG3 from APL5151 to G9191 and unmount CG13	For common design with KSKAE
27	03/14	35	Connect JLIGHT pin5,6 to GND	For common design with KSKAE
28	03/14	36	un-mount R594 for +5V_SB power switch	Let the power switch can get more Vgs voltage when battery low voltage state
29	03/14	36	change R789 from 330K to 820K and R786 from 100K to 220K	For +1.8VS power sequence For power question request
30	03/15	36	Remove R790,R791,R792,R798 with 100ohm	For speaker out voltage is normal
31	03/15	36	Add RA12 with 0ohm	For common desin with KSKAE

Revision Change: 0.6 to 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01	04/10	23	Add R811 and connect to U9C.AF18	For single and dual panel select
02	04/10	20	Change R156 from 4.12K to 976 ohm	For change level shifter IC of HDMI function
03	04/10	31	Add RA36, RA37, RA38, RA39 with 0ohm	For Int. MIC noise
04	04/10	35	Change Q42 power from +3VALW to +5VALW	For Power LED too dark issue
05	04/10	20	Add R220 with 0ohm	For use ASM1442T reserve.
06	04/20	20	Change U7 to ASM1442T	For HDMI signal quality bad issue
07	04/20	20	Delete R149,R159,R160,R161,R162,C251,C252,C253,C254	For HDMI signal quality bad issue
08	04/20	20	Change R151,R152,R153,R154,R689 to 2.2K and R156 to 3.3K	For HDMI signal quality bad issue
09	05/05	20		For HDMI signal quality bad issue

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