

Storm UMA Schematics Document Chief River Intel PCH

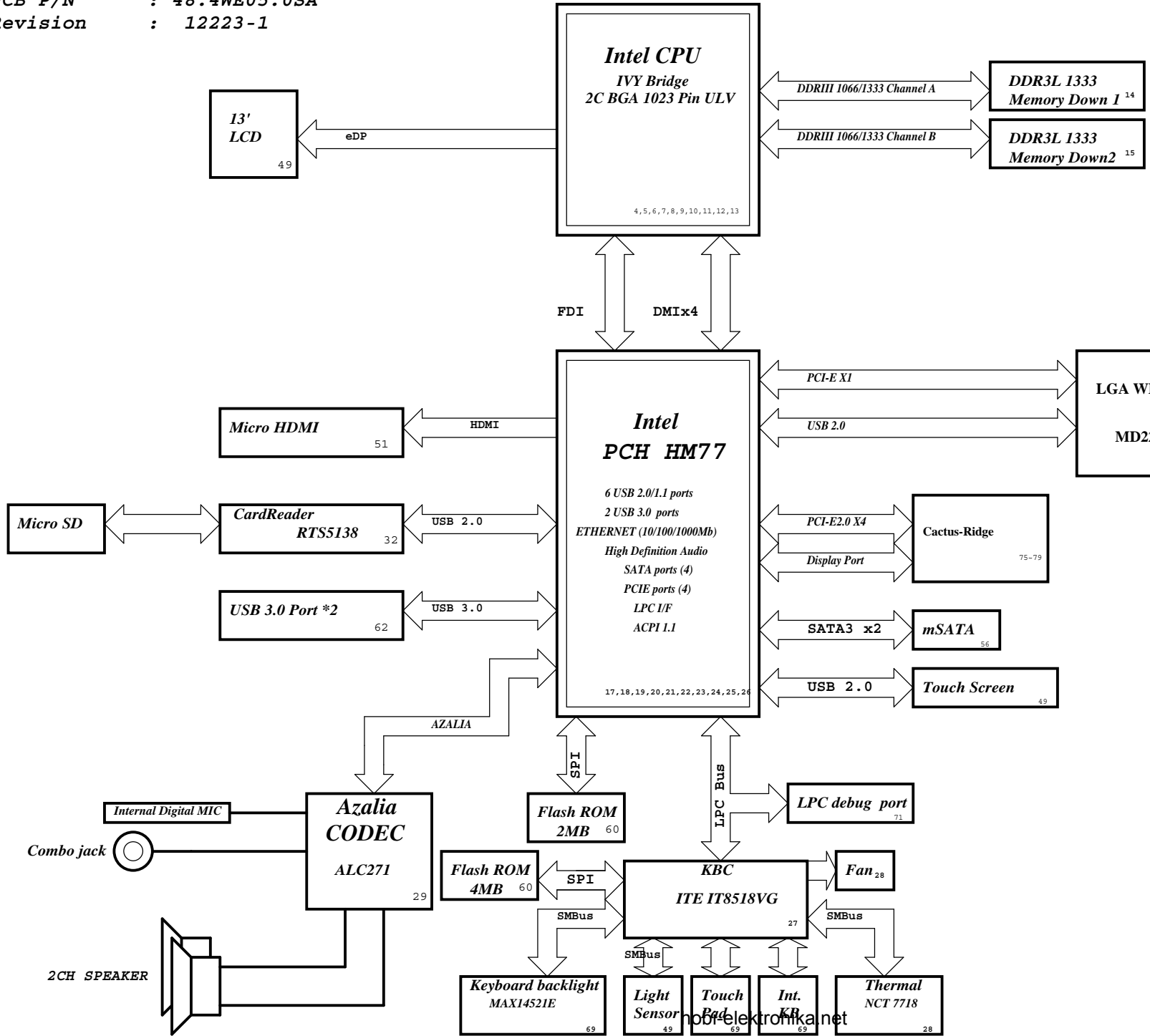
8G:FOR 8G DIMM

STORM

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Title			
Cover Page			
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Project code : 91.4WE01.001
 PCB P/N : 48.4WE05.0SA
 Revision : 12223-1

Storm Block Diagram



SYSTEM DC/DC APL5916KAI 48		CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE
SYSTEM DC/DC UP6128PQDD 45		SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT	DCBATOUT	3D3V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC UP6165BQKF 46		SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	DCBATOUT	VCC_GFXCORE_PWR
VGA RT8208BGQW 92		TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VGA_CORE	DCBATOUT	BT+
SYSTEM DC/DC RT9025 47		SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S0	1D8V_S0	1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0	3D3V_S5	1D8V_VGA_S0
Switches		Switches	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0	3D3V_S0	3D3V_VGA_S0
PCB LAYER			
L1:Top	L6:Signal	L7:GND	L8:Signal
L2:VCC	L3:Signal	L4:VCC	L5:Signal
L3:Signal	L4:VCC	L5:Signal	L6:Signal
L4:VCC	L5:Signal	L6:Signal	L7:GND
L5:Signal	L6:Signal	L7:GND	L8:Signal
L6:Signal	L7:GND	L8:Signal	L9:GND
L7:GND	L8:Signal	L9:GND	L10:Bottom

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0:	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	USB3.0 Ext. port 1
1	USB3.0 Ext. port 2
2	NC
3	NC
4	Card Reader
5	WLAN+BT
6	CCD
7	X
8	X
9	NC
10	NC
11	NC
12	NC

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB		
		Address	Hex	Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA		
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA		
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK		

PCIE Routing

LANE1	N/A
LANE2	N/A
LANE3	N/A
LANE4	WLAN
LANE5	Thunderbolt
LANE6	Thunderbolt
LANE7	Thunderbolt
LANE8	Thunderbolt

SATA Table

SATA	
Pair	Device
0	mSATA1
1	mSATA2
2	N/A
3	N/A
4	N/A
5	N/A

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

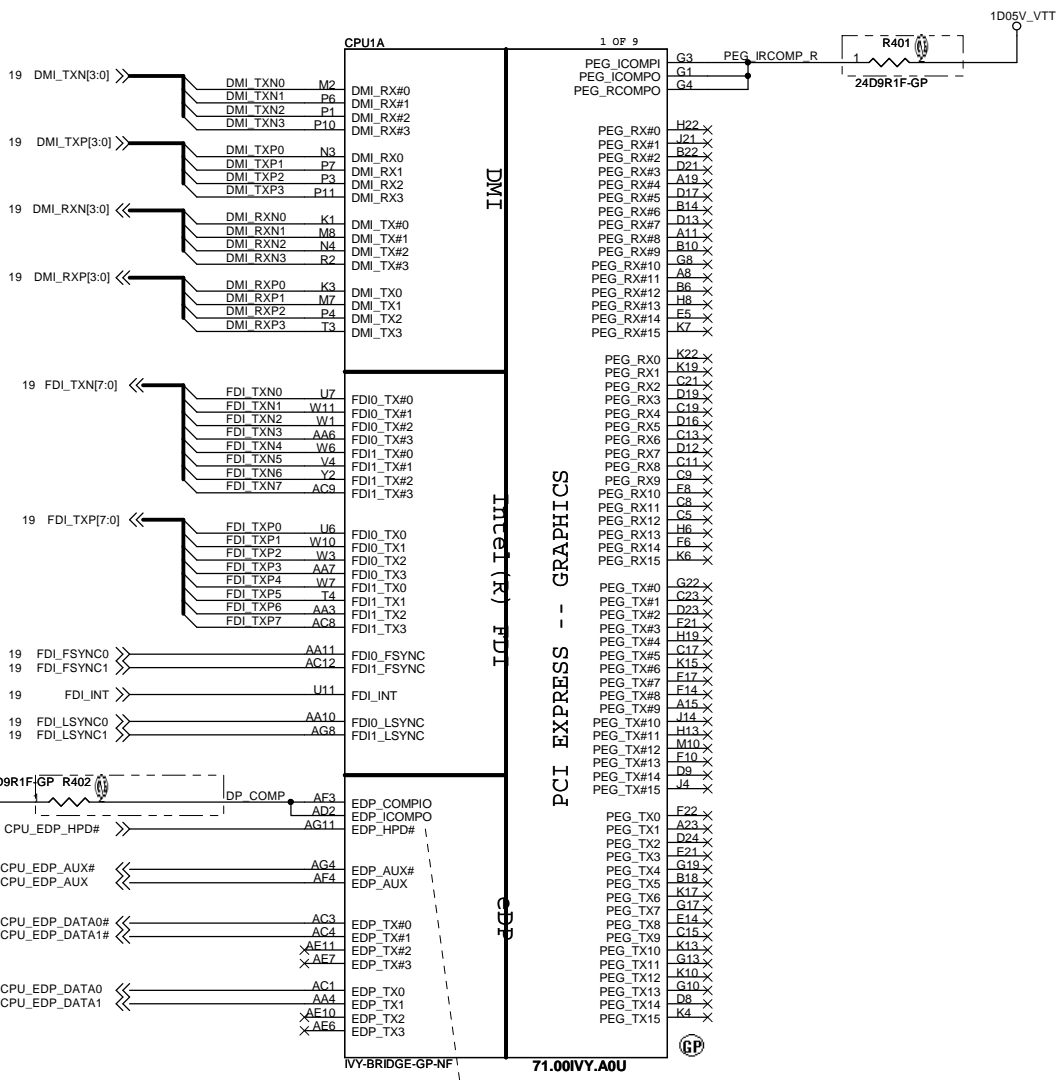
Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Impedance: 85 ohm

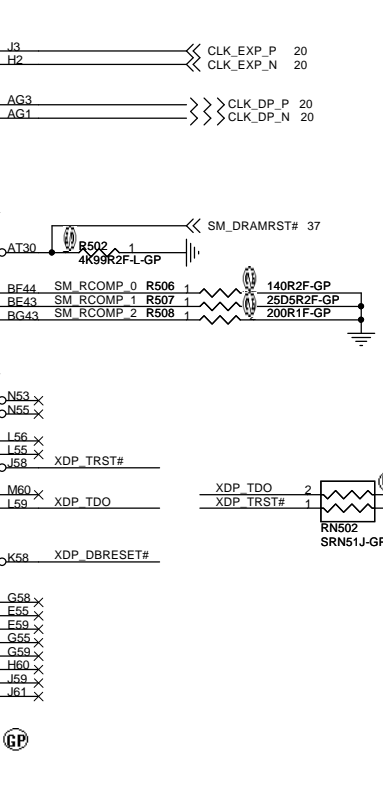
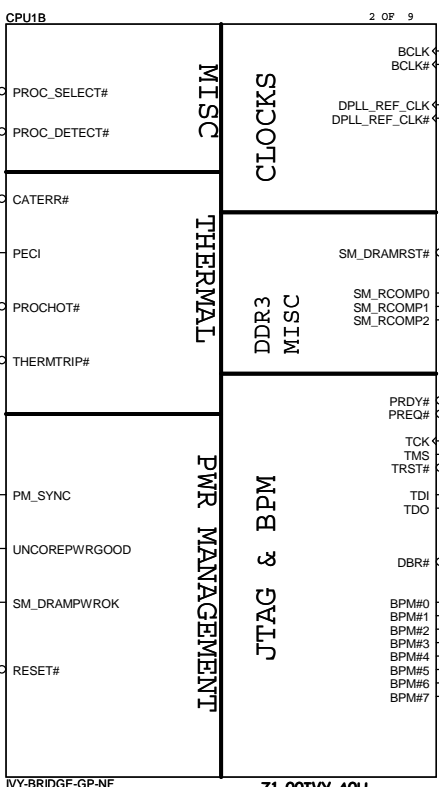
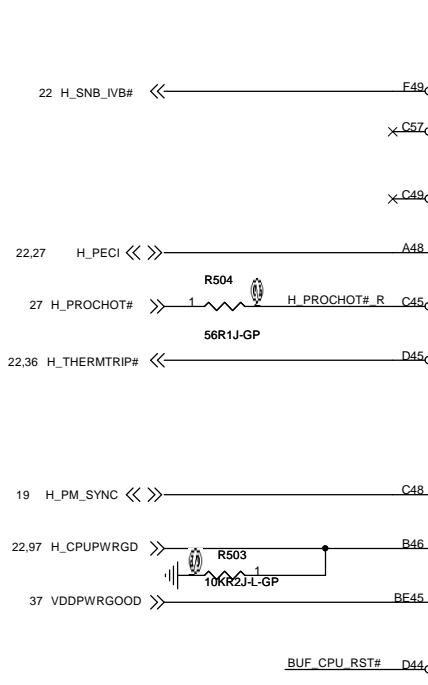
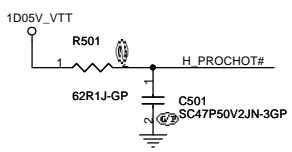
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.



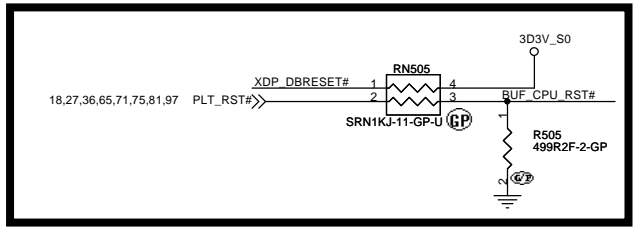
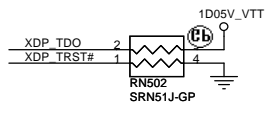
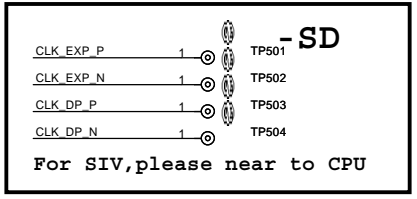
NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD# on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

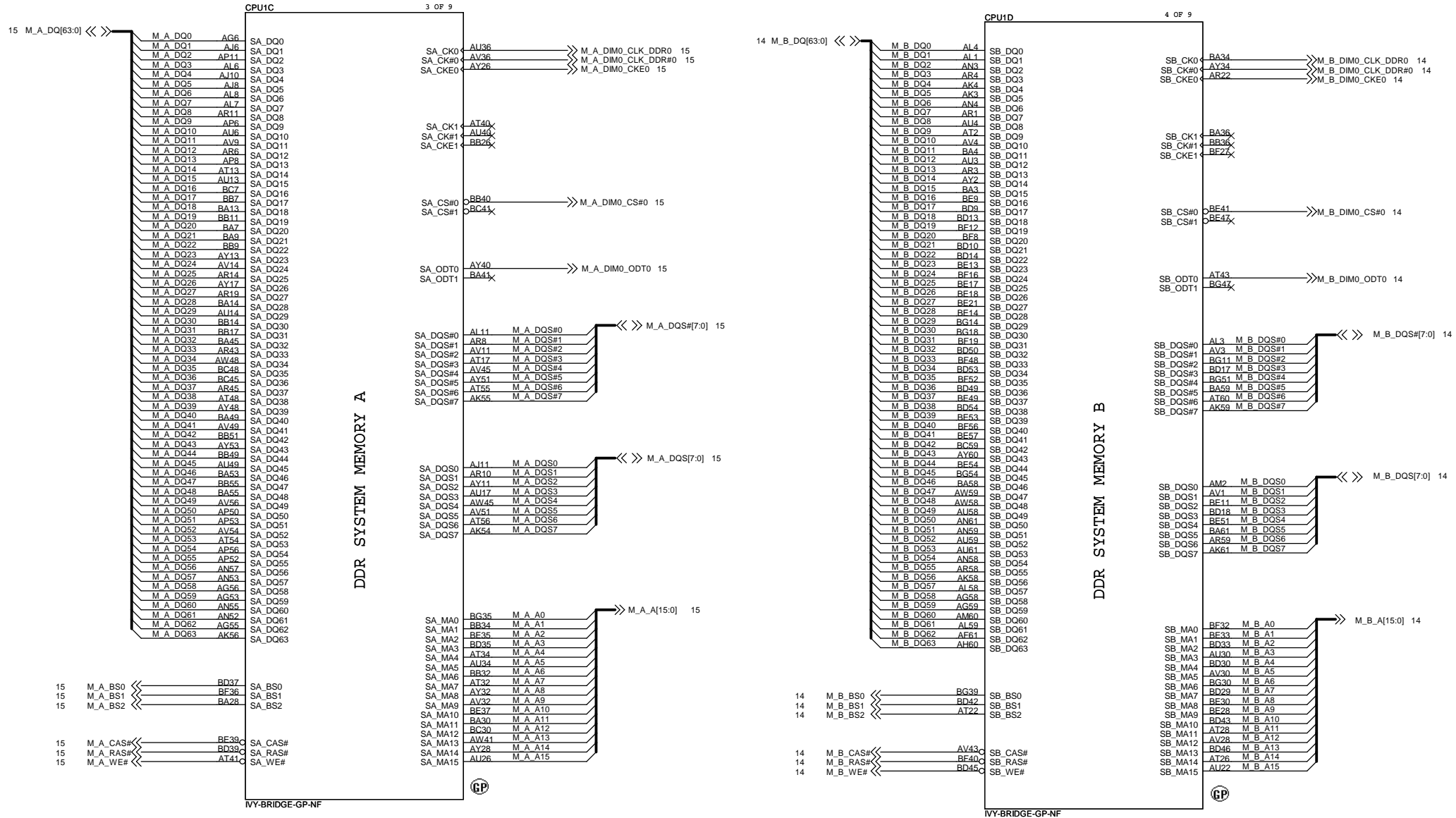
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Title: CPU (PCIe/DMI/FDI)
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SSID = CPU



Disabling Guidelines:
 If motherboard only supports external graphics or without eDP,
 Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5%
 resistor.
 Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5%
 resistor power (~15 mW) may be wasted.





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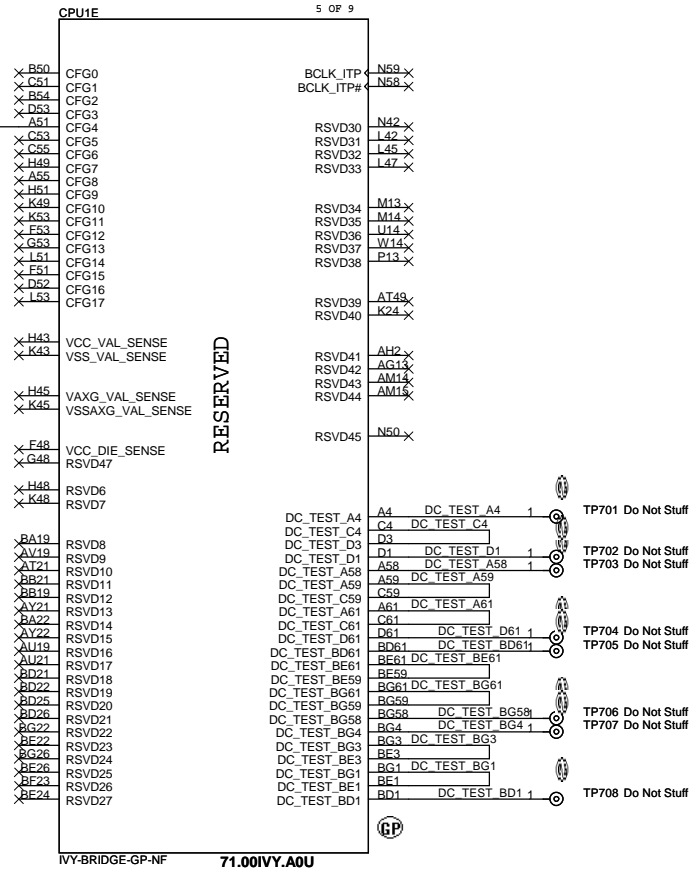
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SSID = CPU



Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	0
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable 0: Enabled - An external Display Port device is connected to the Embedded Display Port Pull-down to GND through a 1KΩ ± 5% resistor to enable port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	00
CFG[17:7]		Reserved configuration lands. A test point may be placed on the board for these lands.	

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Title: **CPU (RESERVED)**

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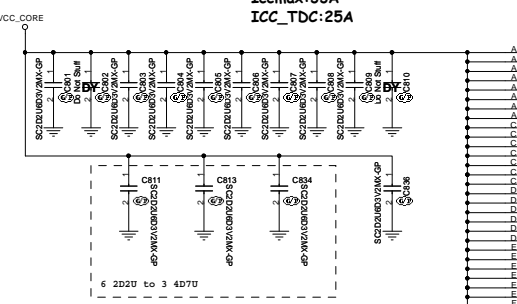
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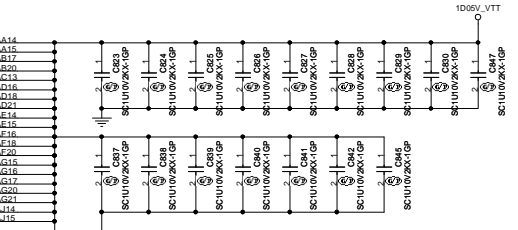
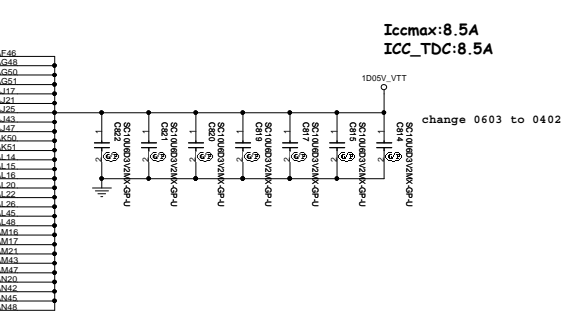
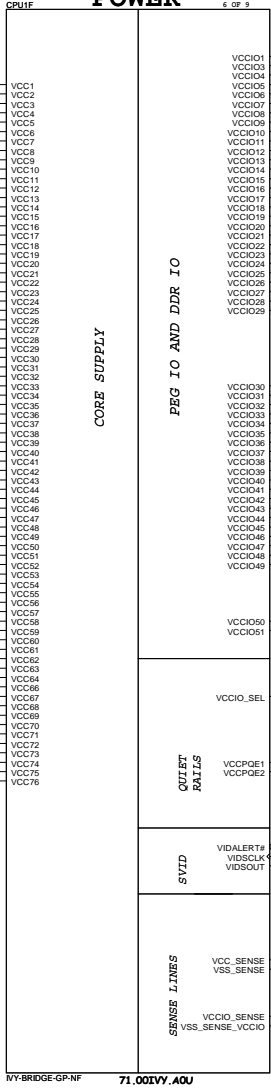
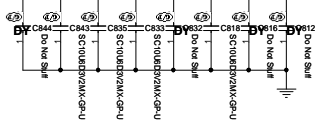
ULV:14W
Iccmax:33A
ICC_TDC:25A

POWER

Iccmax:8.5A
ICC_TDC:8.5A

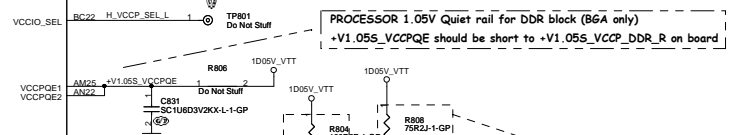


Layout Note: 2.2u Cap place under CPU

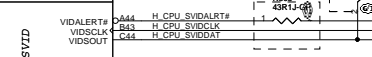


1.05V_VTT Power rail		PiN BC22 CPU	
1.05V	H	SNB	
1V	L	IVB	

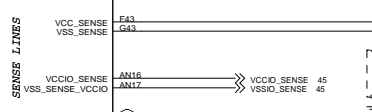
CPU EDS desig guide Rev change 1 V to 1.05V



PROCESSOR 1.05V Quiet rail for DDR block (B&A only)
+V1.05S_VCCPQE should be short to +V1.05S_VCCP_DDR_R on board



Place near processor



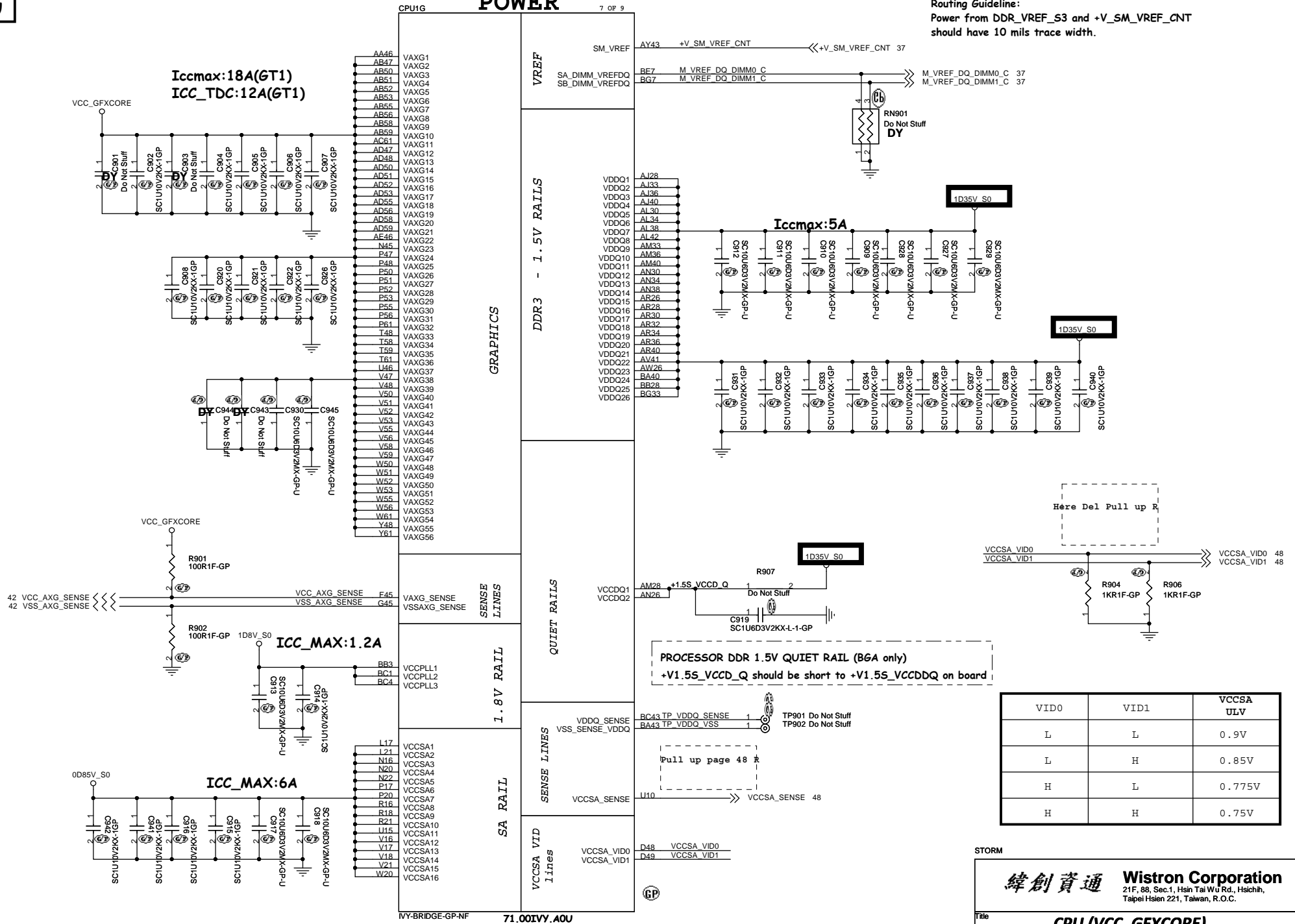
Place near processor

MY-BRIDGE-GP-NF 71.001VY.AOU

SSID = CPU

POWER

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.



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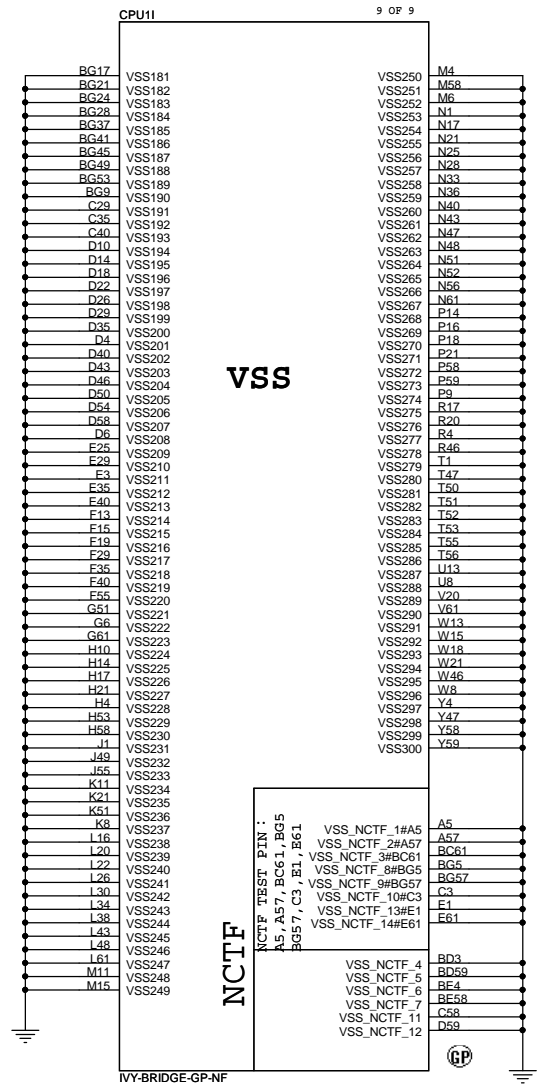
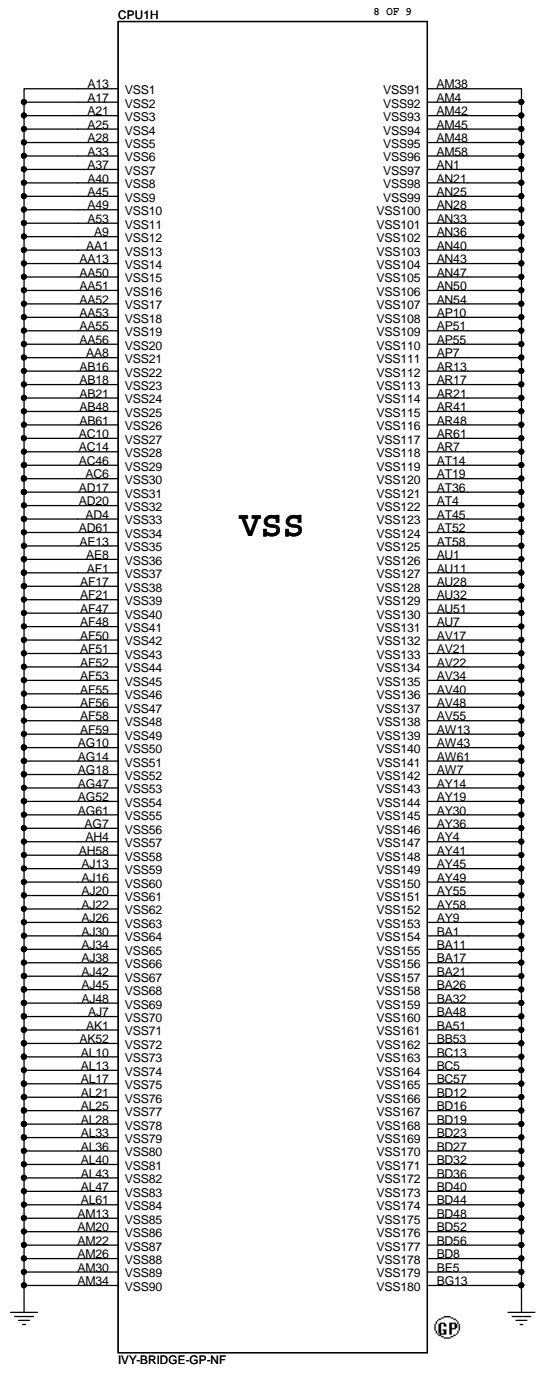
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Title CPU (VCC_GFXCORE)

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SSID = CPU



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reserve

JE40 delete XDP function

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Title

XDP

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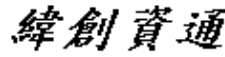
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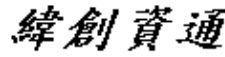
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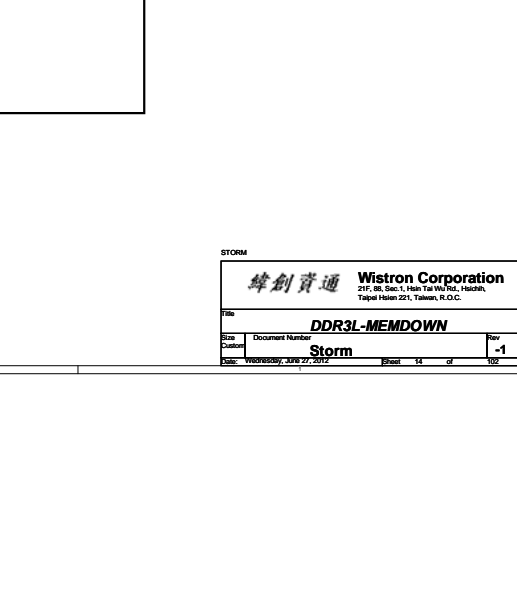
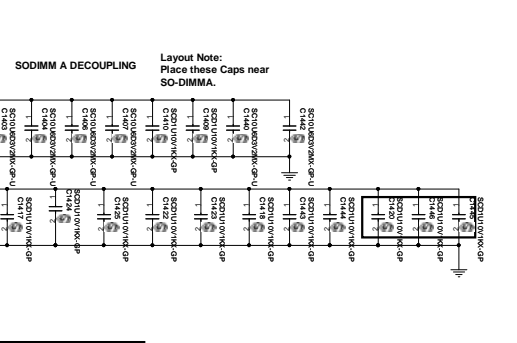
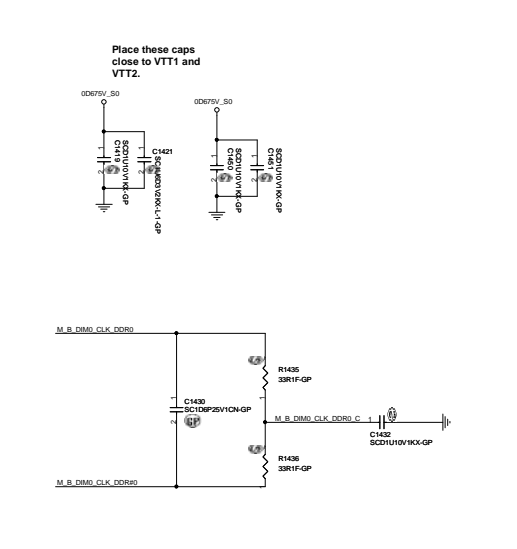
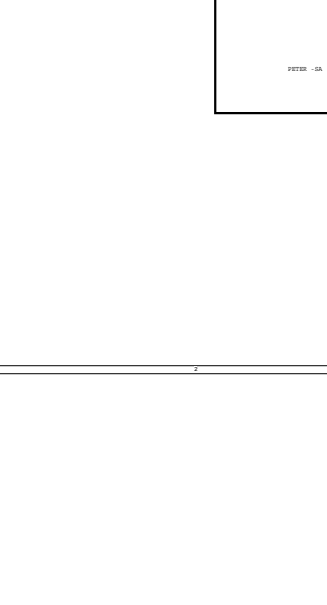
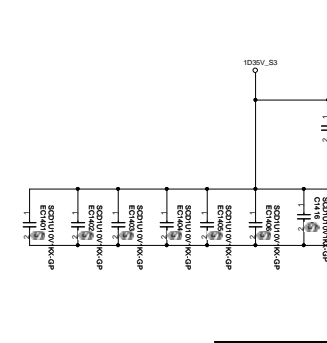
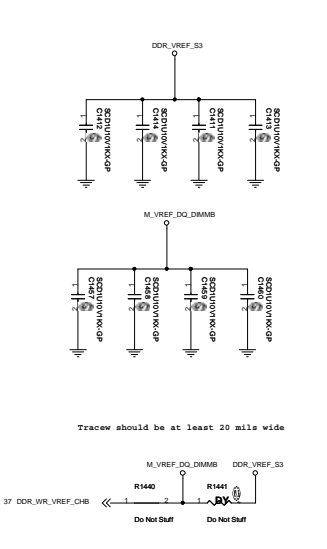
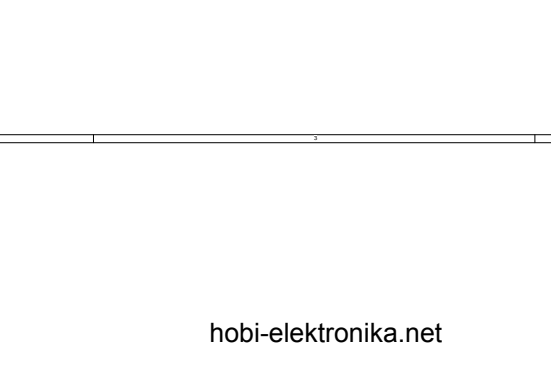
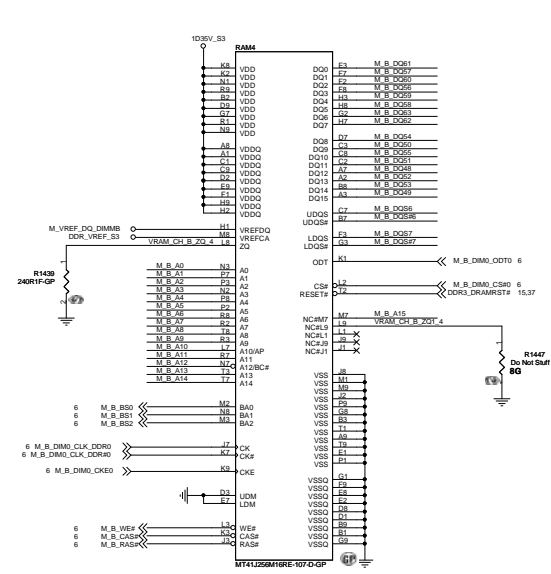
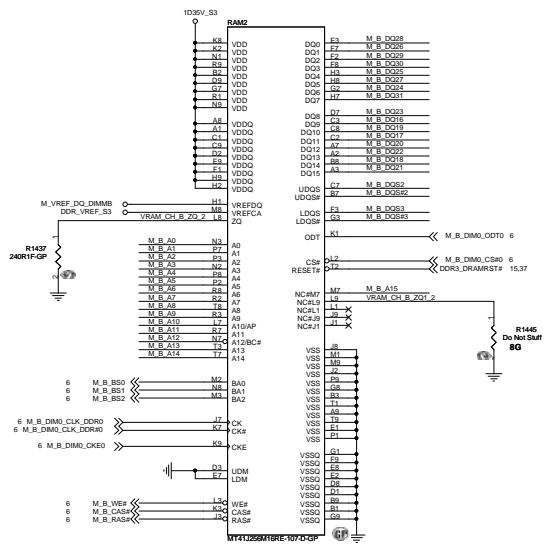
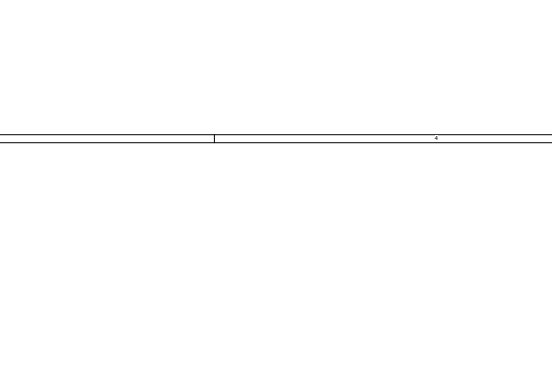
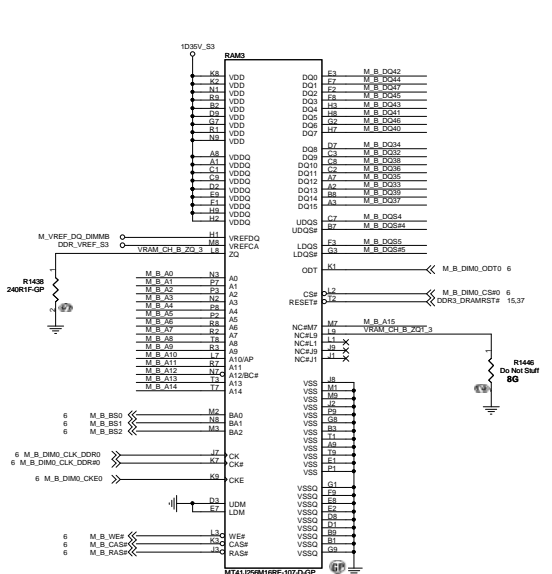
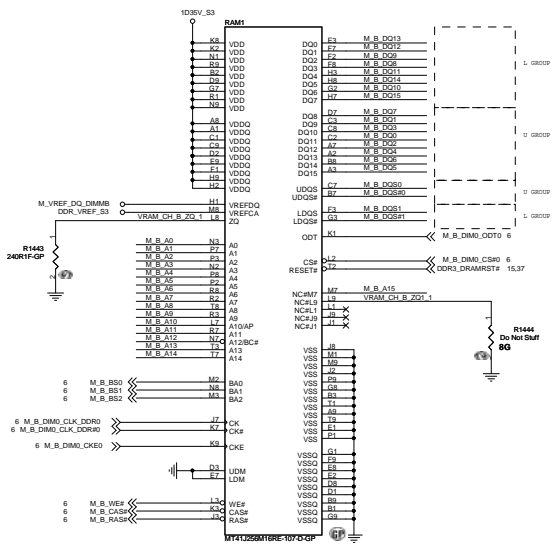
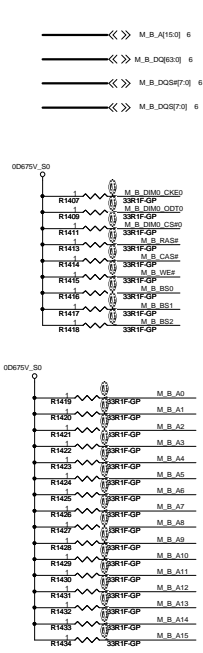
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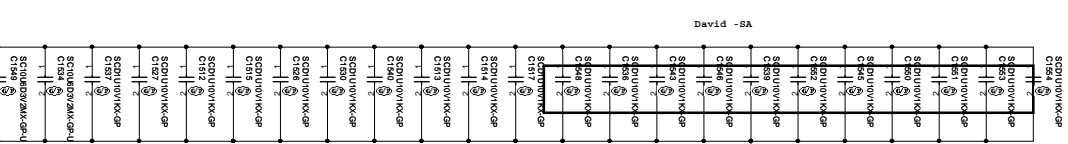
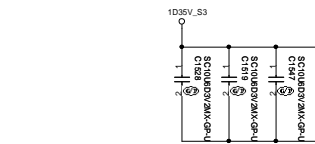
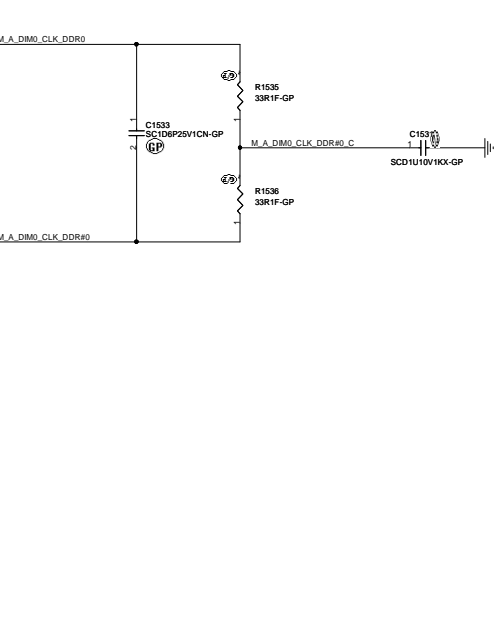
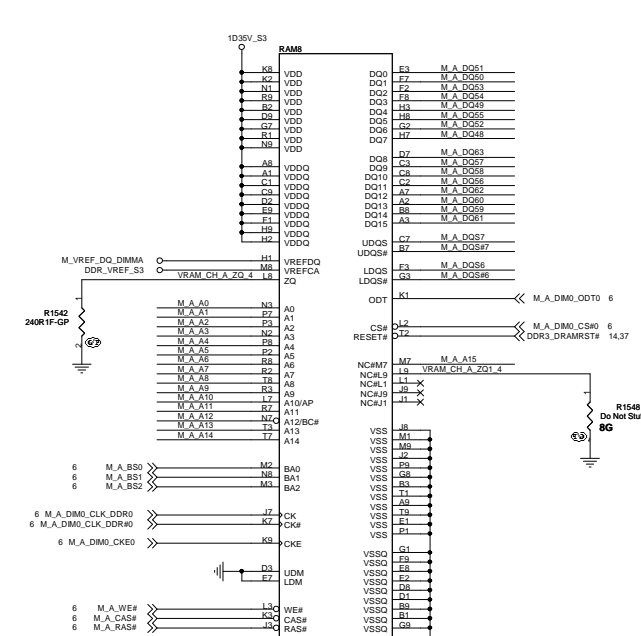
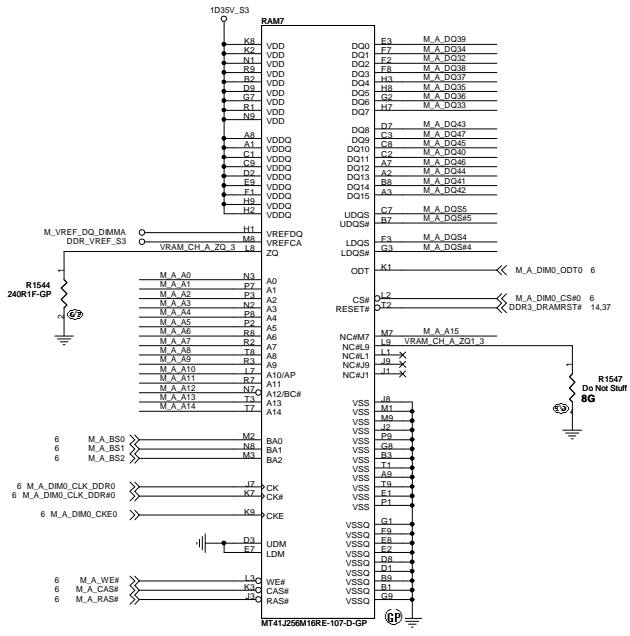
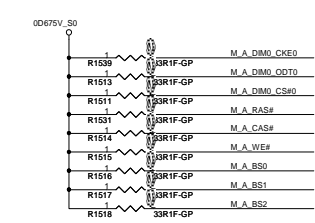
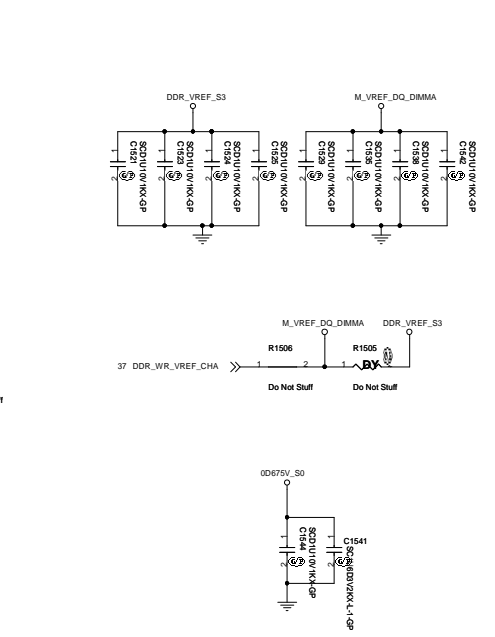
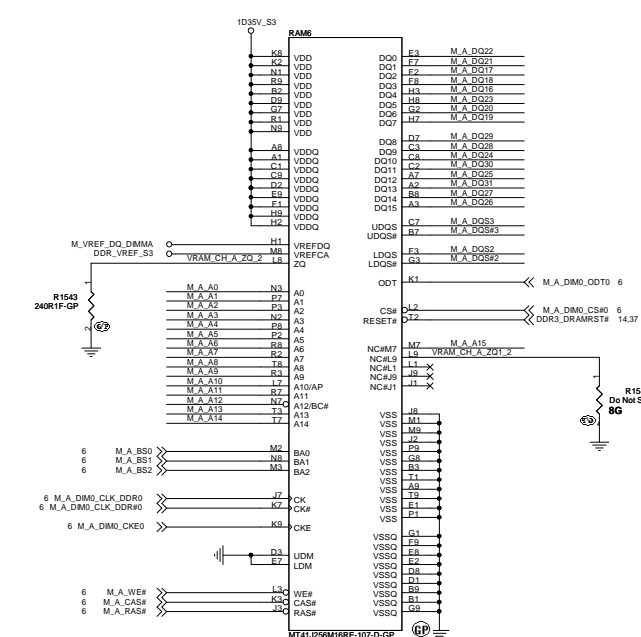
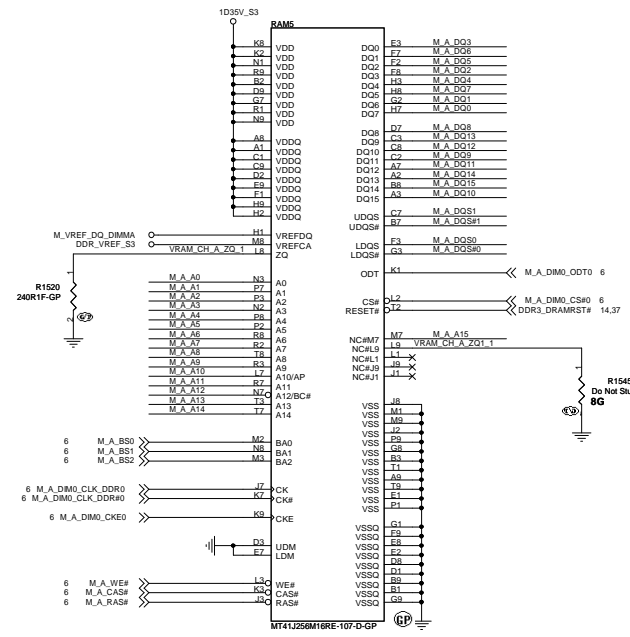
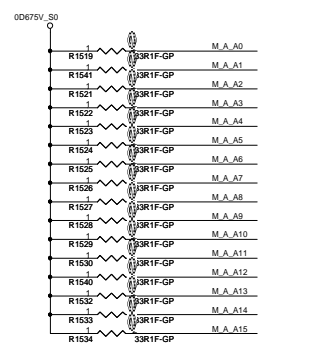
Size A4	Document Number Storm	Rev -1
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DDR3L-MEMDOWN
Storm
Rev -1

SSID = MEMORY

- 6 M_A_A[15:0] <<>>
- 6 M_A_DQ[63:0] <<>>
- 6 M_A_DQS[7:0] <<>>
- 6 M_A_DQS[7:0] <<>>



David -SA

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File: **DDR3L-MEMDOWN2**

Size: Document Number
Date: Monday, June 25, 2012 Sheet 15 of 102

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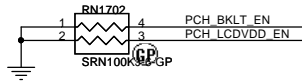
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Size A4	Document Number Storm	Rev -1
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Date: Monday, June 25, 2012	Sheet 16 of	102
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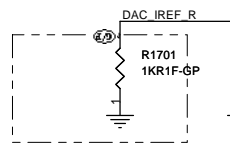
3.24.2 LVDS Disable Guidelines

Pin Name	System Pull-up/Pull-down	Schematic Notes	✓
Data/Clock/Control	.	All signals associated with the interface can be left as No Connect.	✓
Power Supply	.	The supply pins VCC_TX_LVDS, and VCCA_LVDS can be connected to GND.	✓

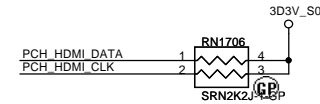
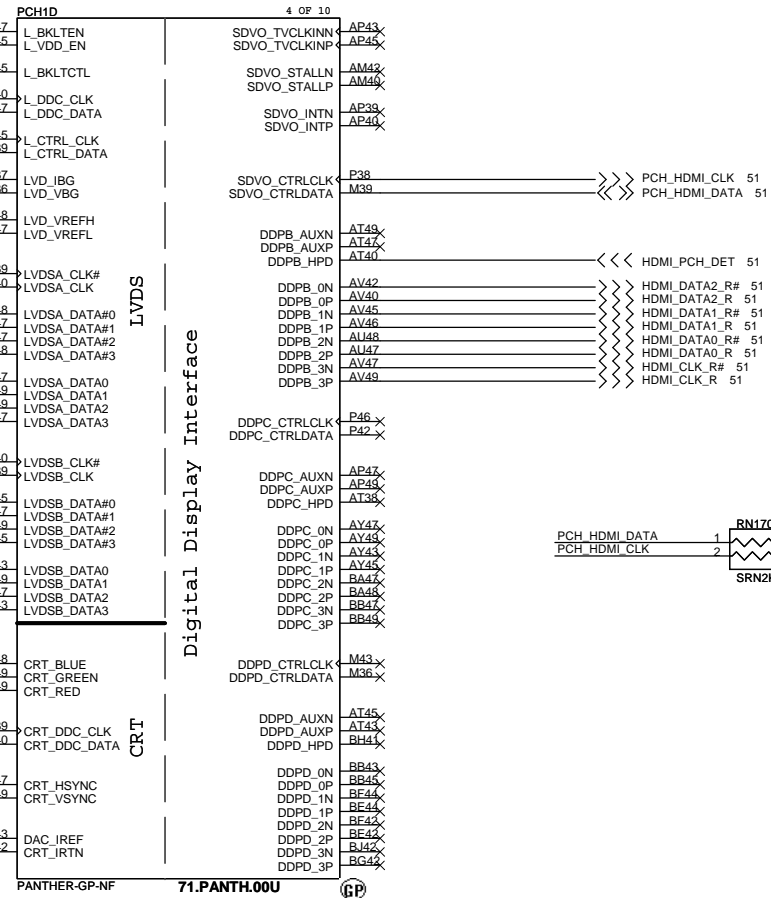


3.24.4 CRT Disable

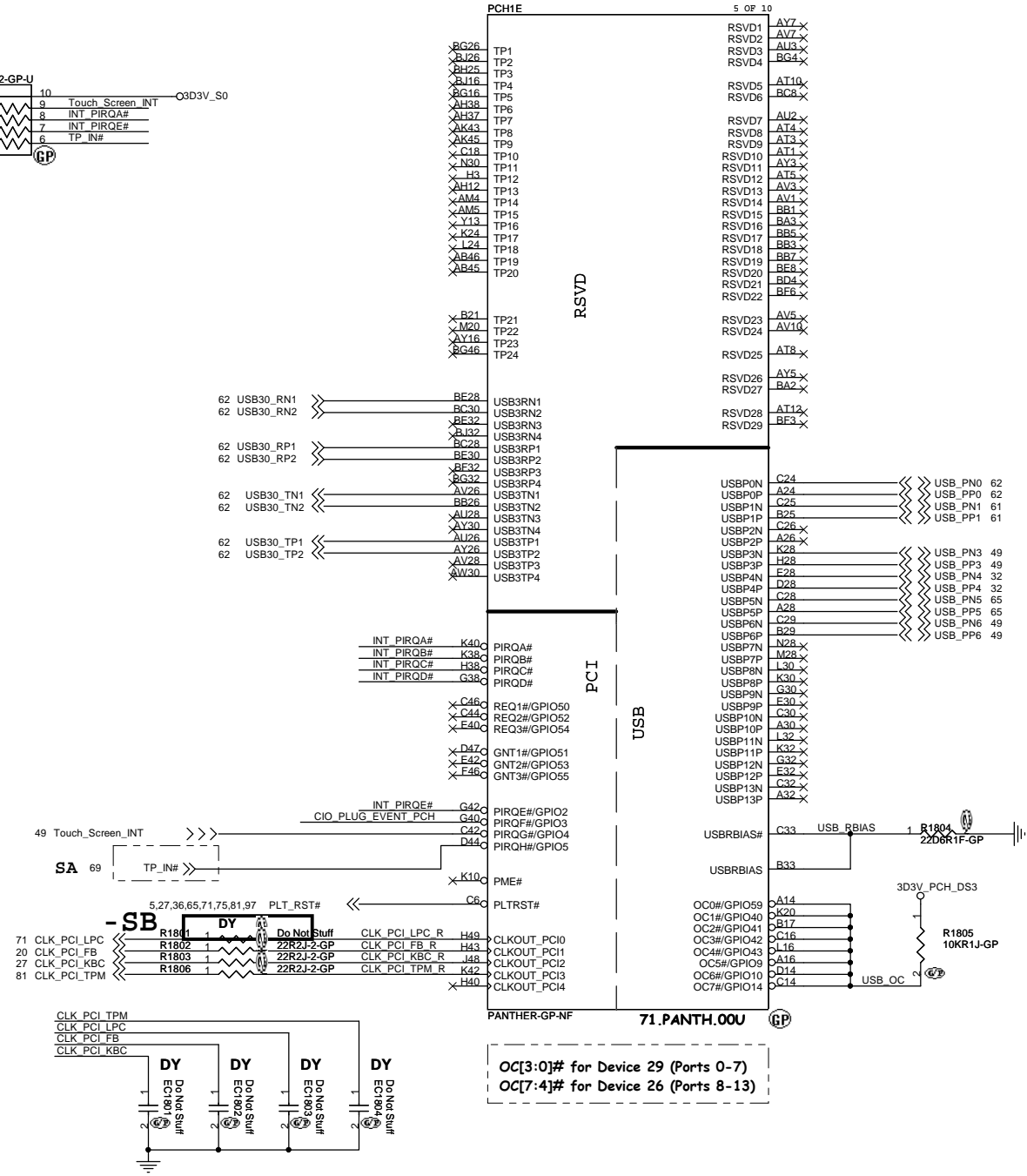
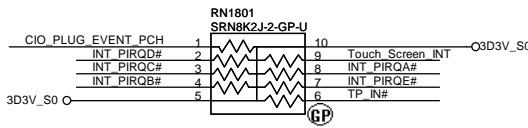
Name	System Pull-up/Pull-down	Schematic Notes	✓
CRT_RED CRT_GREEN CRT_BLUE CRT_HSYN CRT_VSYN	.	Leave as No Connect.	✓
CRT_IRTN	.	Connect directly to GND plane on the motherboard.	✓
DAC_IREF	1-kΩ ± 5% pull-down to GND.	.	✓
VCCADAC	Connect to +V3.3 power-rail.	.	✓



if use CRT change 1K to +/- 0.5% (64.10016.6DL)



SSID = PCH



USB Table

Pair	Device
0	USB3.0 Ext. port 1
1	USB3.0 Ext. port 2
2	NC
3	NC
4	Card Reader
5	Mini Card1 (WLAN)
6	CCD
7	X
8	X
9	NC
10	NC
11	NC
12	NC

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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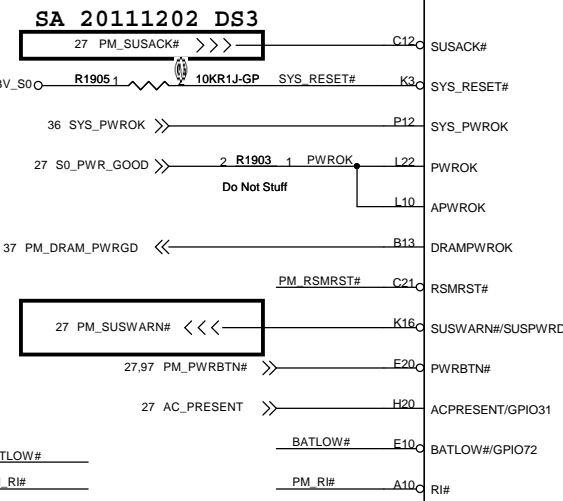
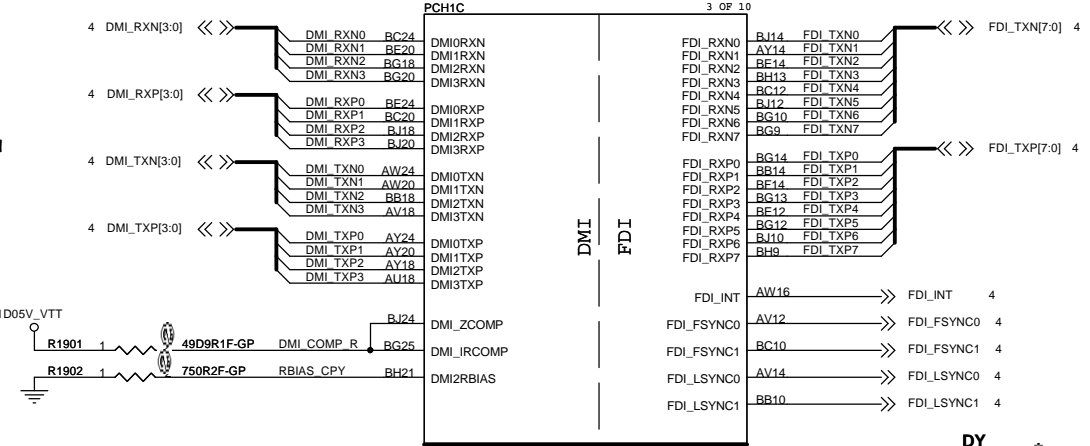
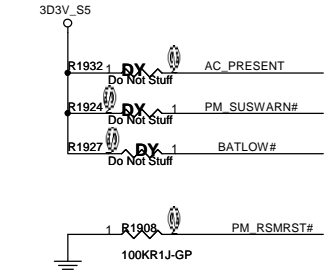
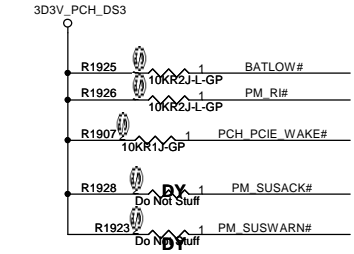
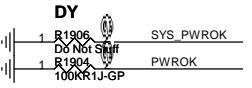
Title: **PCH (PCI/USB/NVRAM)**

Size A3 Document Number: **Storm** Rev: **-1**

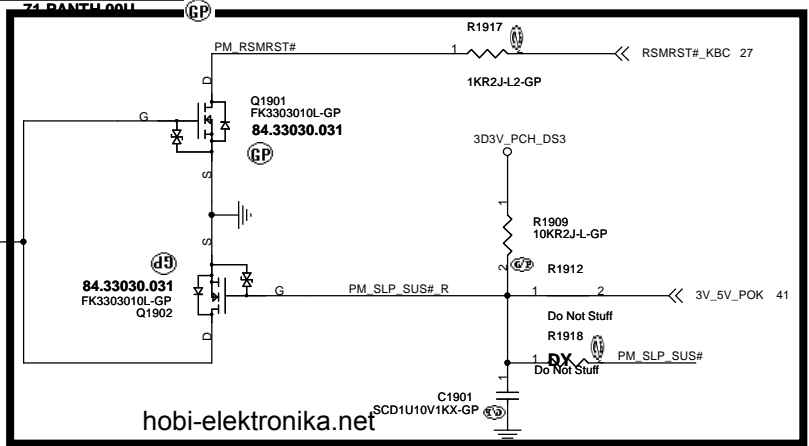
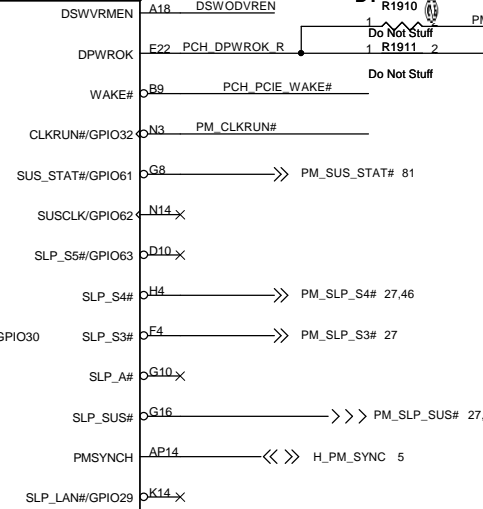
Date: Monday, June 25, 2012 Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

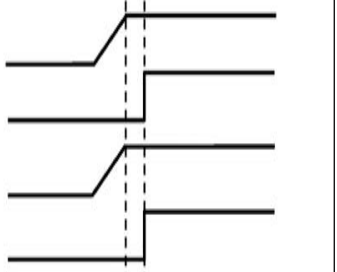
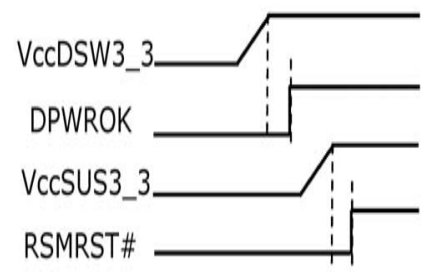


System Power Management



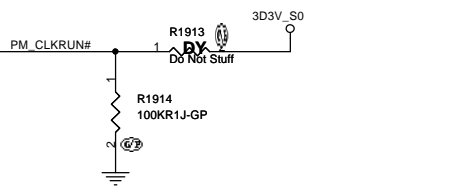
Deep S4/S5 Supported

Deep S4/S5 Not Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



STORM

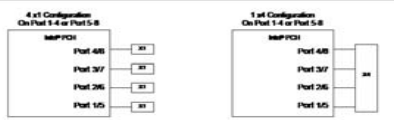
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Title: **PCH (DM I/FDI/PM)**

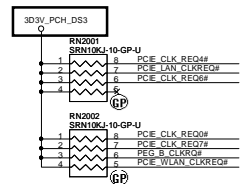
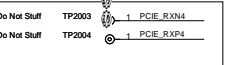
Size A3 Document Number: **Storm** Rev: **-1**

Date: Monday, June 25, 2012 Sheet 19 of 102

SSID = PCH

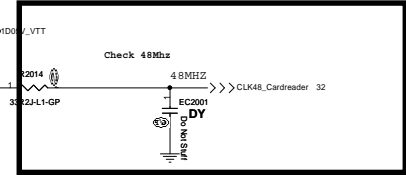
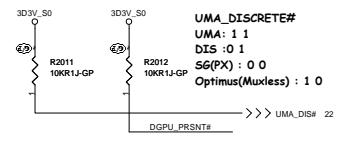
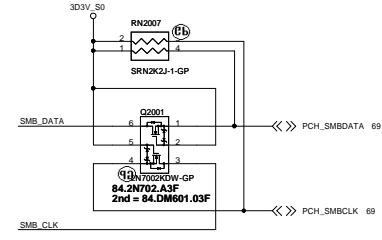
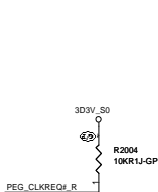
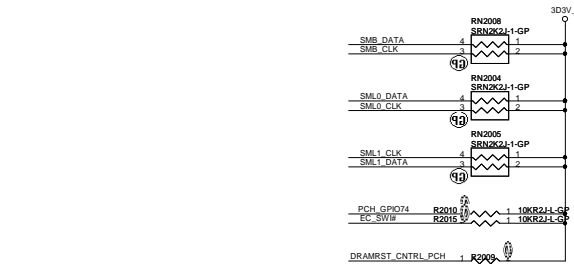
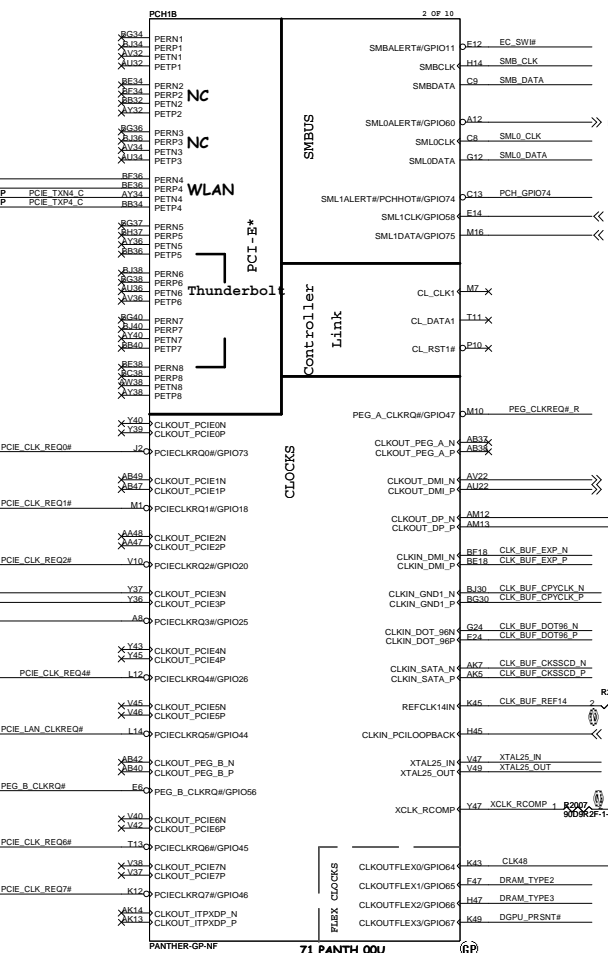
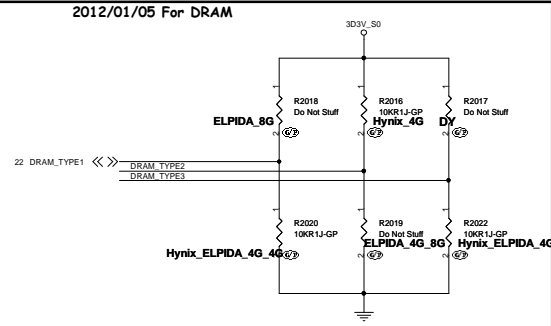


FOR SIV, PLS near PCH



PCIECLKRQ1# and PCIECLKRQ2# Support 80 power only

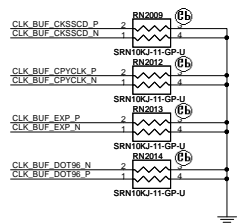
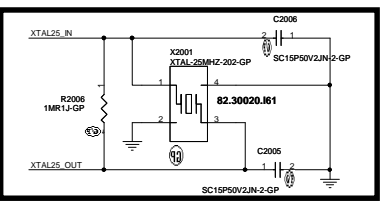
2012/01/05 For DRAM



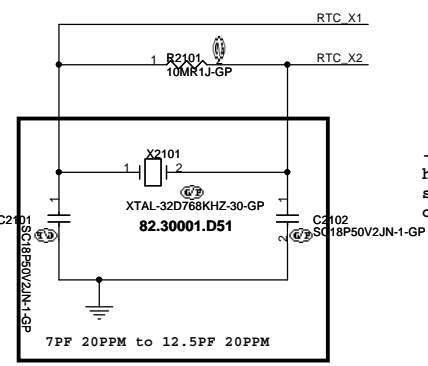
71.PANTH.000

As Flex clocks, can be configured as 48 MHz/ 24 MHz, 33 MHz, 27 MHz (Speed or Nonspread), 14,318 MHz. Refer to the PCB External Design Specification (EDS) for configuration options of Flex Clocks.

0	0	0	ELPIDA 2GB PER Channel(chip is 4Gbit RAM)
0	0	1	Hynix A 2GB PER Channel(chip is 4Gbit RAM)
0	1	0	
0	1	1	
1	0	0	ELPIDA 4GB PER Channel(chip is 8Gbit RAM)
1	0	1	
1	1	0	
1	1	1	



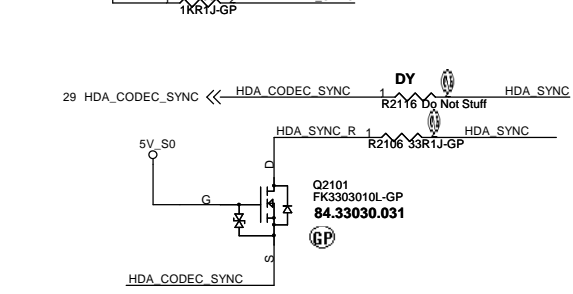
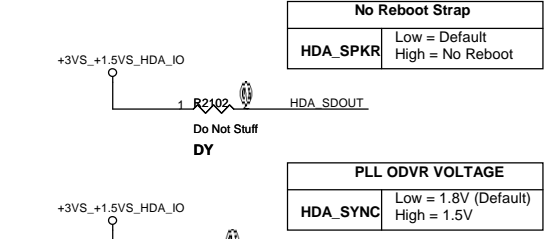
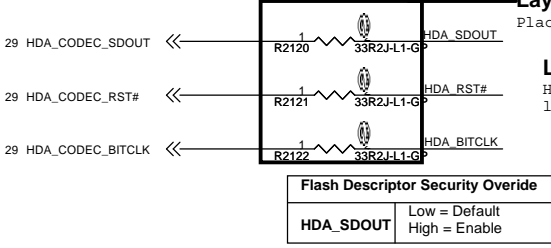
SSID = PCH



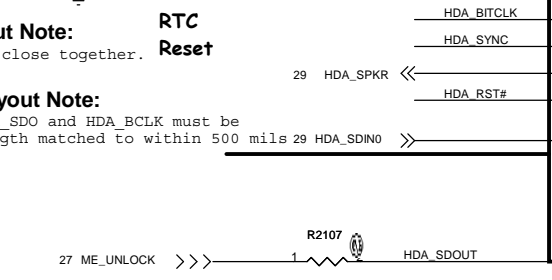
-SB height concern, do not change to 0603, so change C from 1uF to 0.1uF change R from 20K to 200K for AFR

Layout Note:
Place close together.

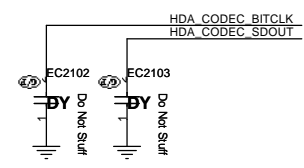
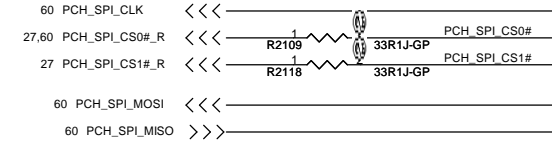
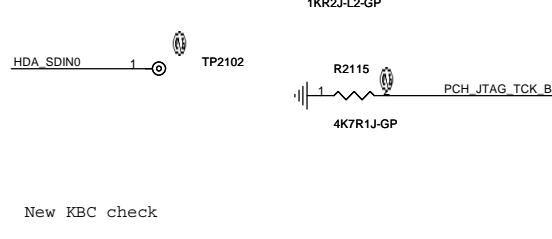
Layout Note:
HDA_SDO and HDA_BCLK must be length matched to within 500 mils



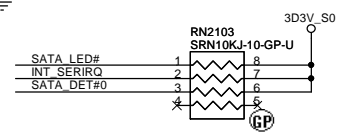
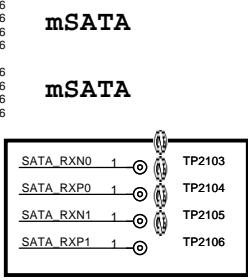
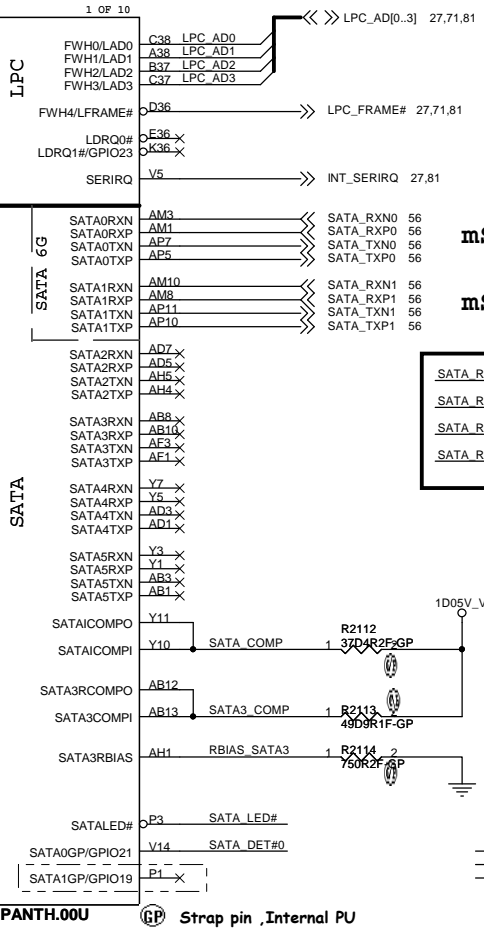
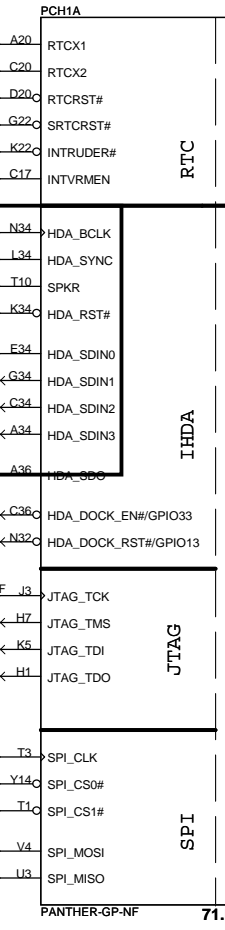
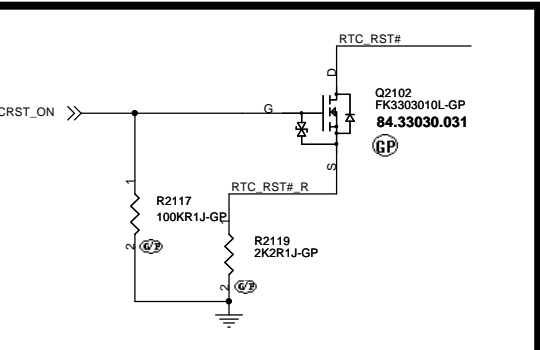
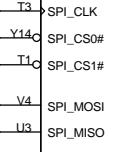
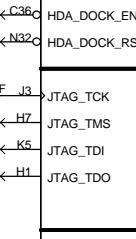
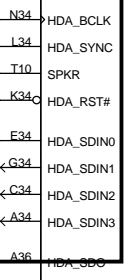
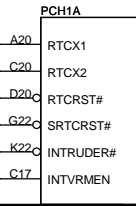
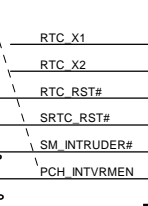
HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



RTC Reset



INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



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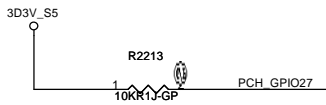
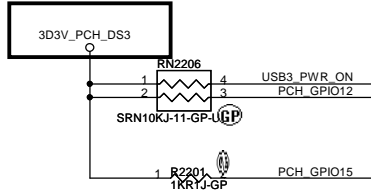
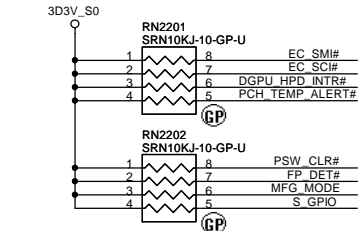
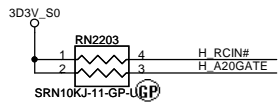
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size A3 Document Number Rev

Date: Tuesday, June 26, 2012 Sheet 21 of 102

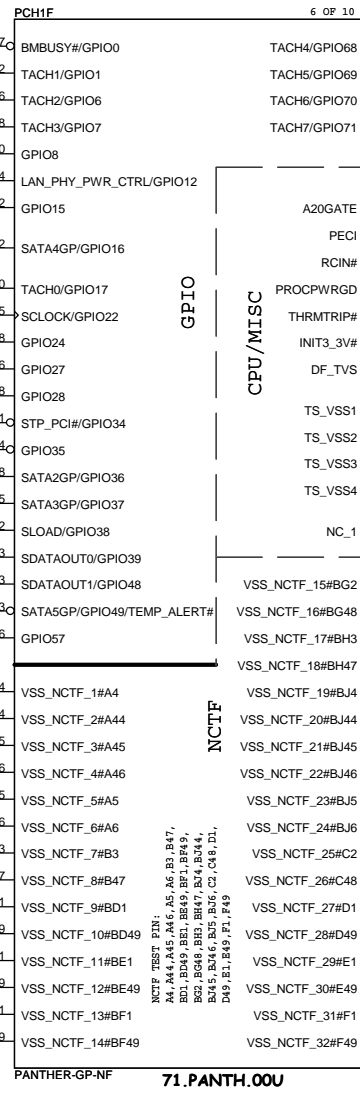
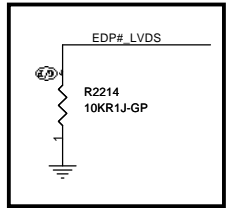
Storm **-1**

SSID = PCH



Pass Word Clear

20 DRAM_TYPE1 <<<



NCTF TEST PIN:
 PA, AA, A6, A7, A8, A9, B3, B4, B7, B8, B9, B10, B11, B14, B9, B10, B11, B14, B15, B16, B15, B16, C2, C4, D1, D9, B1, B4, B9, F1, F4, F9

PCH:no Turbo control via PECCI
 KBC (Recommended): EC collect all thermal data and Performs Turbo power control

Layout Note:

FDI TERMINATION VOLTAGE OVERRIDE (Reserved)	
FDI_OVRVLTG (GPIO37)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE (Reserved)	
DMI_OVRVLTG (GPIO36)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable (Reserved)	
ICC_EN# (GPIO8)	HIGH - DISABLED [DEFAULT] LOW - ENABLED

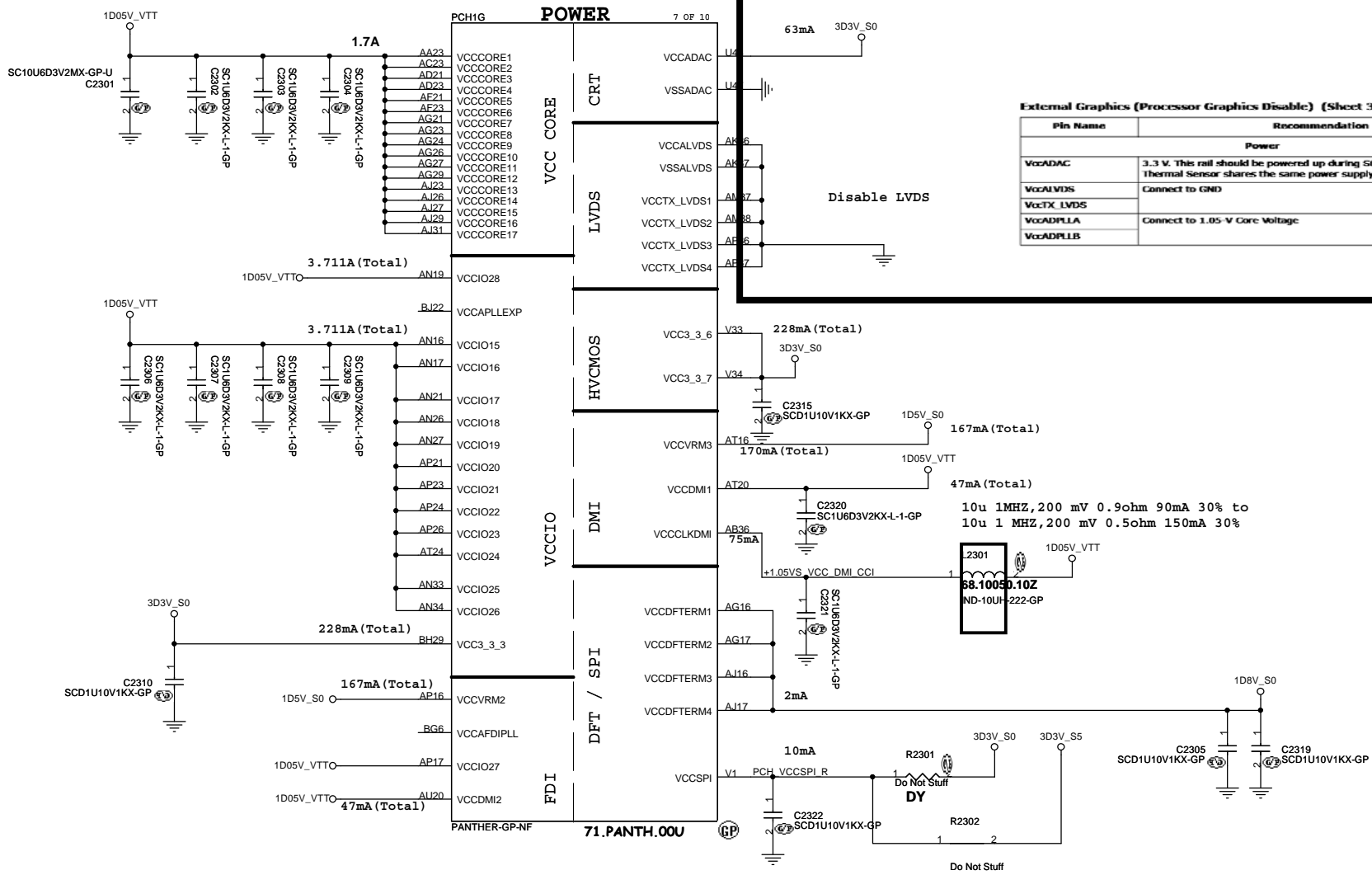
PLL ON DIE VR ENABLE	
PLL_ODVR_EN (GPIO28)	HIGH - DISABLED [DEFAULT] LOW - ENABLED

STORM

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Title: **PCH (GPIO/CPU)**

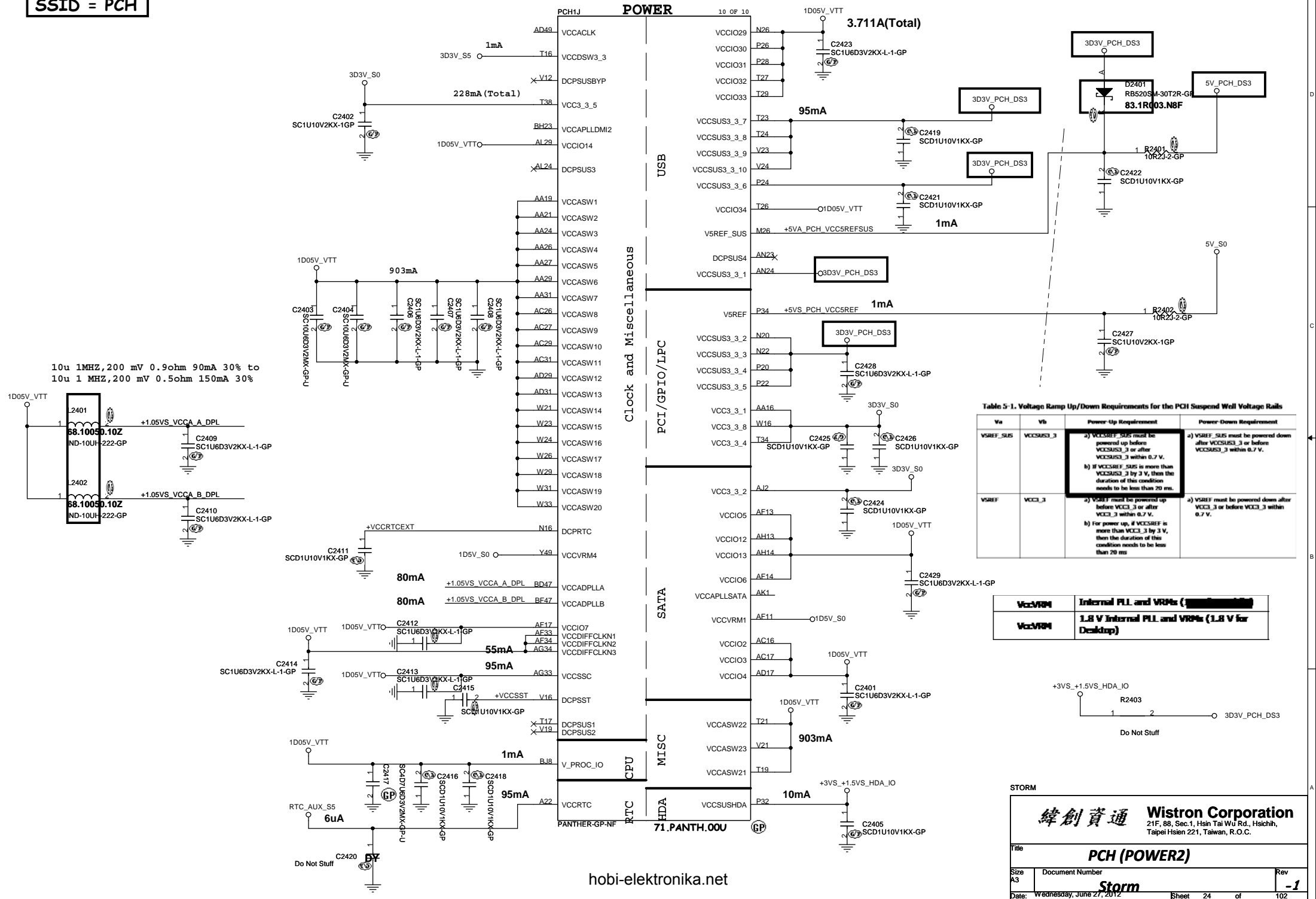
Size A3 Document Number Rev
 Date: Monday, June 25, 2012 Sheet 22 of 102 **Storm** **-1**



External Graphics (Processor Graphics Disable) (Sheet 3 of 3)

Pin Name	Recommendation
Power	
VccADAC	3.3 V. This rail should be powered up during S0 system state. Note that Thermal Sensor shares the same power supply rail with DAC.
VccALVDS	Connect to GND
VccCTX_LVDS	Connect to 1.05-V Core Voltage
VccADPLLA	
VccADPLLB	

SSID = PCH



STORM

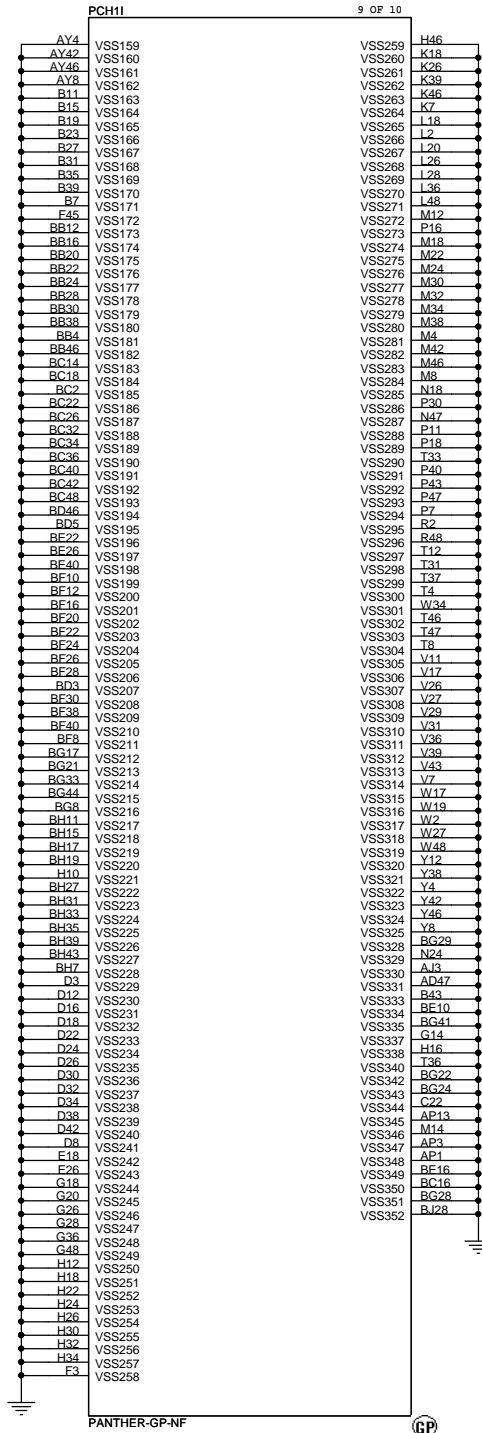
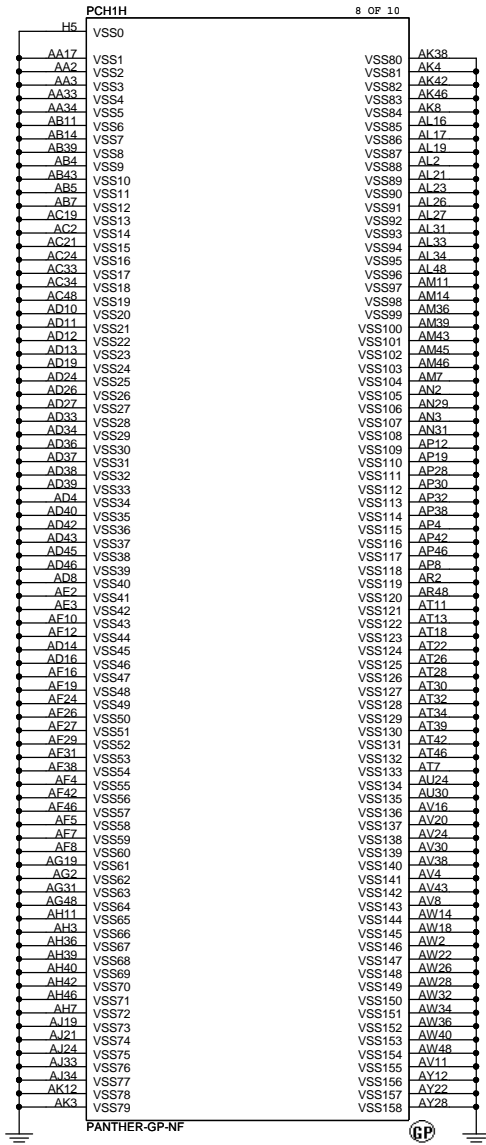
緯創資通 Wistron Corporation
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Title: PCH (POWER2)

Size A3 Document Number: Storm Rev: -1

Date: Wednesday, June 27, 2012 Sheet 24 of 102

SSID = PCH



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Title **PCH (VSS)**

Size A3	Document Number Storm	Rev -1
Date: Monday, June 25, 2012	Sheet 25 of 102	

5

4

3

2

1

D

D

C

C

B

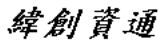
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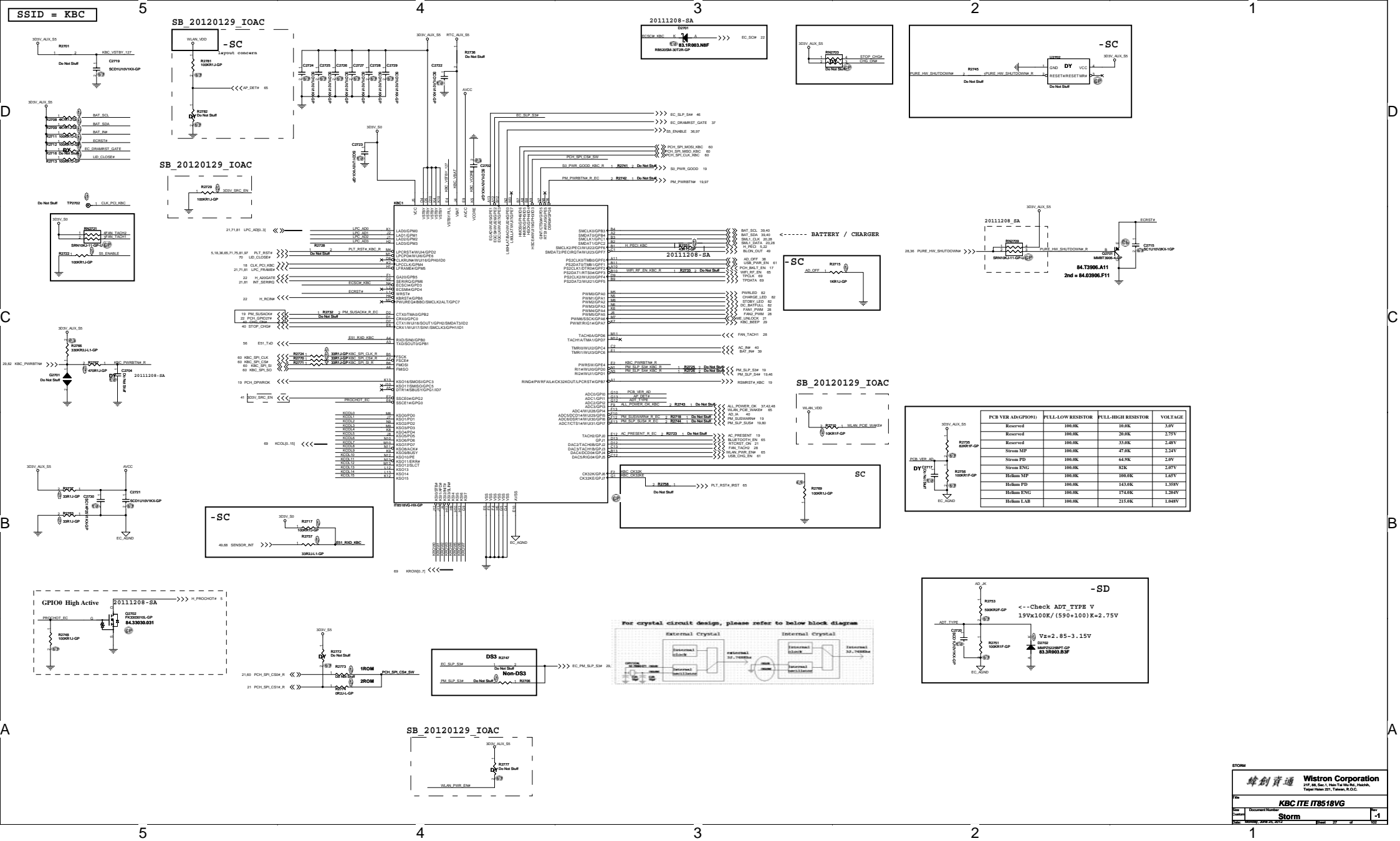
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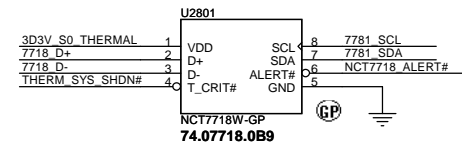
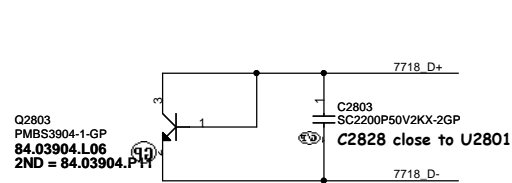
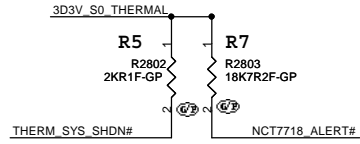
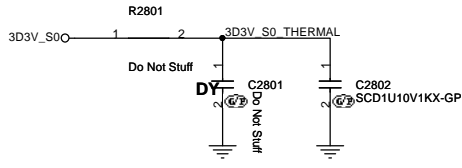
STORM

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Clock(colay)	
Size A3	Document Number Storm
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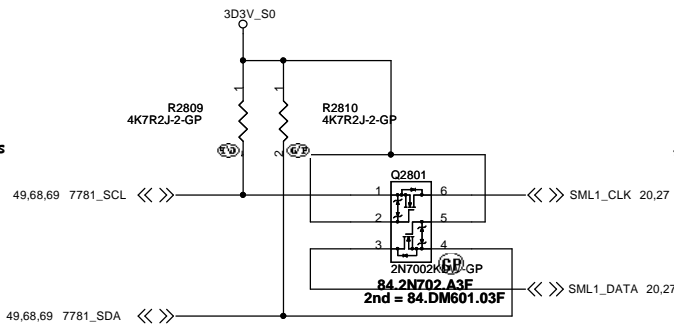
PCB VER AD(GPI0)	FULL-LOW RESISTOR	FULL-HIGH RESISTOR	VOLTAGE
Reserved	100.0K	10.0K	3.0V
Reserved	100.0K	35.0K	2.95V
Stream MP	100.0K	47.0K	2.24V
Stream PD	100.0K	64.9K	2.0V
Stream ENG	100.0K	81K	2.07V
HiBum MP	100.0K	100.0K	1.65V
HiBum PD	100.0K	122.0K	1.355V
HiBum ENG	100.0K	174.0K	1.284V
HiBum LAB	100.0K	215.0K	1.048V

SSID = Thermal



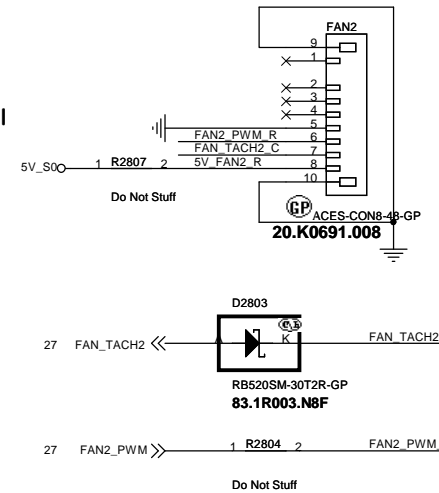
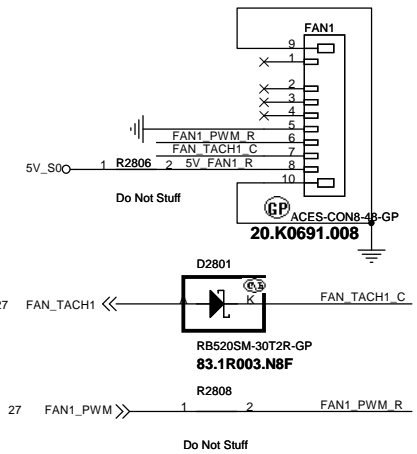
Layout notice :

- * Put the C1 2200pF to close the nct7718W
- * Add ground shielding for D+ and D- traces
- * D+/D- route has to be away from the high noise area
- * The recommended traces width and ground shielding spacing are 10mils



Layout 15 mil

Layout 15 mil



Setting 85°C

ALERT# /T CRIT#
Pull-up Resistor

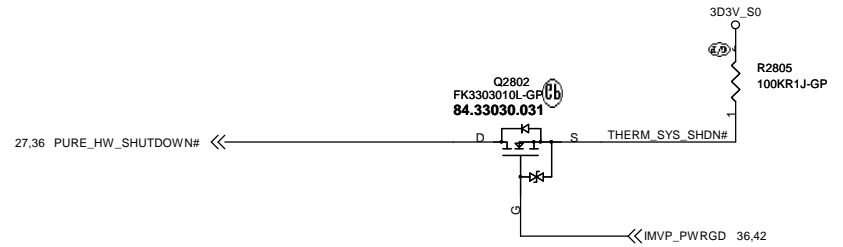
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	79°C	81°C	83°C	85°C	
87°C	89°C	91°C	93°C	95°C	
97°C	99°C	101°C	103°C	105°C	
107°C	109°C	111°C	113°C	115°C	
117°C	119°C	121°C	123°C	125°C	

T_CRIT temperature strapping point

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
77	79	81	83	85	
87	89	91	93	95	
97	99	101	103	105	
107	109	111	113	115	
117	119	121	123	125	

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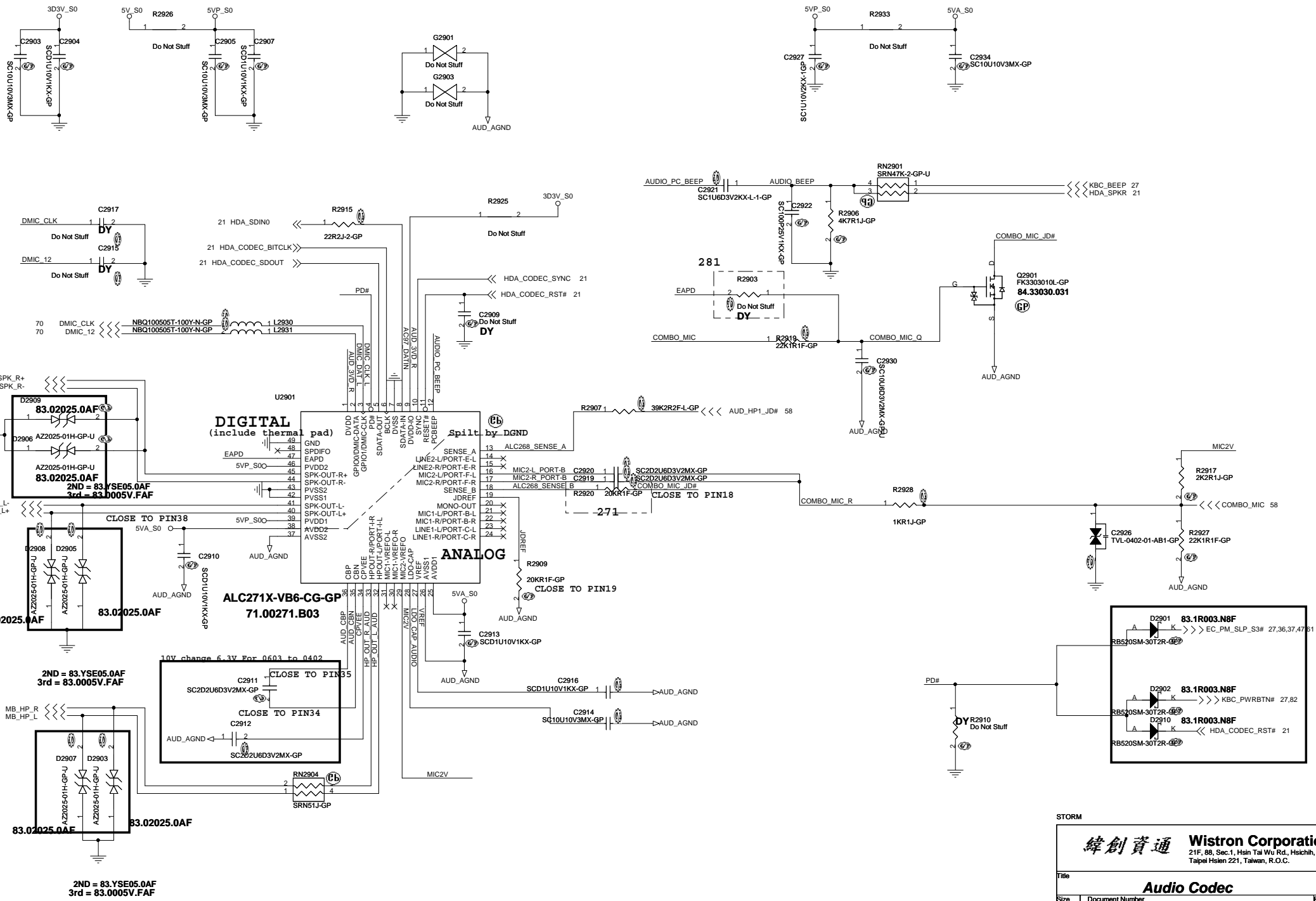
STORM

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Title: **NUVOTON_NCT7718W**

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AUDIO OP AMPLIFIER

JE40 delete AMP function

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Title

Audio AMP

Size
A4

Document Number

Storm

Rev

-1

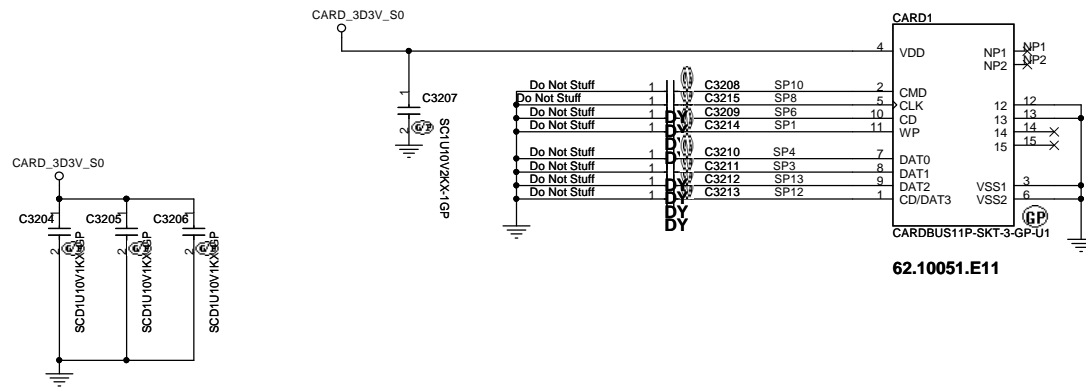
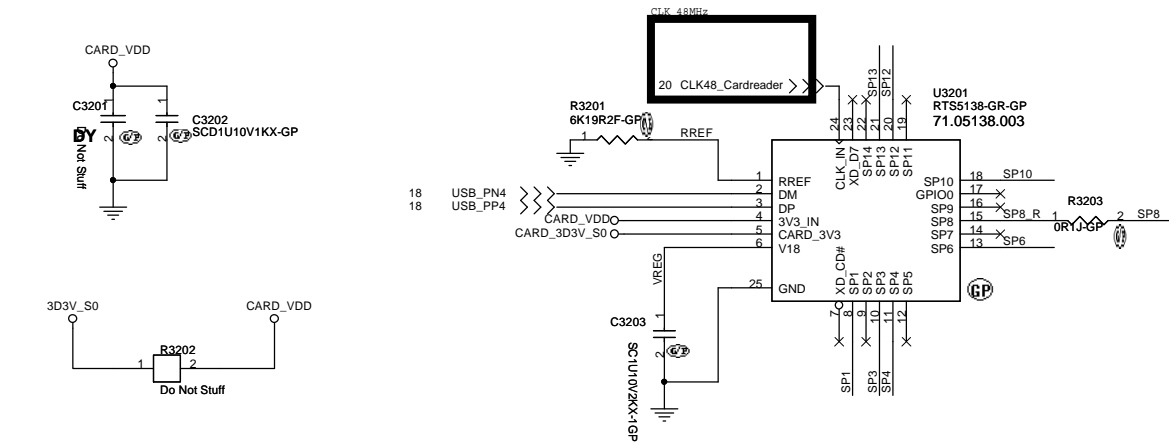
Date: Monday, June 25, 2012

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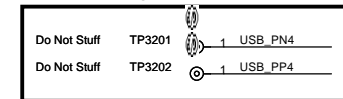
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AR8158			
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Near CARD1 Pin11, Pin18, Pin22

1	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	V18	O	Regulated supply voltage (1.8V ±10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected
7	XD_CD#	I	xD Card Detect (xD CD#)
8	SP1	I/O	xD Ready Signal (xD RDY), SD Write Protect (SD WP) and MS Check (MS CLK)
9	SP2	I/O	xD REF and MS Card Detect (MS INSP)
10	SP3	I/O	xD CE# and SD Data 1 (SD DAT1)
11	SP4	I/O	xD CLE, SD Data 0 (SD DAT0) and MS Data 7 (MS D7)
12	SP5	I/O	xD ALE, SD Data 7 (SD DAT7) and MS Data 3 (MS D3)
13	SP6	I/O	xD WE# and SD Card Detect (SD CD#)
14	SP7	I/O	xD Write Protect (xD WP), SD Data 6 (SD DAT6) and MS Data 6 (MS D6)
15	SP8	I/O	xD Data 0 (xD D0), SD Clock (SD CLK) and MS Data 2 (MS D2)
16	SP9	I/O	xD Data 1 (xD D1), SD Data 5 (SD D5) and MS Data 0 (MS D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD D2) and SD command signal (SD CMD#)
19	SP11	I/O	xD Data 3 (xD D3), SD Data 4 (SD DAT4) and MS Data 4 (MS D4)
20	SP12	I/O	xD Data 4 (xD D4), SD Data 3 (SD DAT3) and MS Data 1 (MS D1)
21	SP13	I/O	xD Data 5 (xD D5), SD Data 2 (SD DAT2) and MS Data 5 (MS D5)
22	SP14	I/O	xD Data 6 (xD D6) and MS RS
23	XD_D7	I/O	xD Data 7 (xD D7)
24	CLK_IN	I	48MHz clock directly input

FOR SIV, PLS near U3201



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CARDREADER	
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Reserved

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Title

Reserved

Size
A4

Document Number

Storm

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-1

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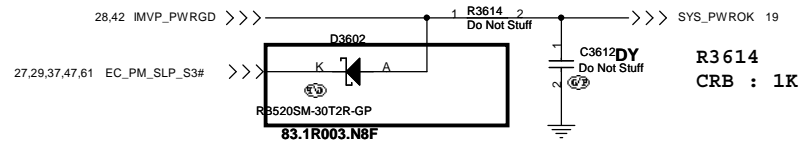
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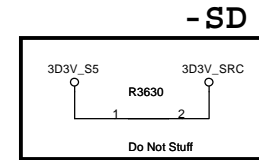
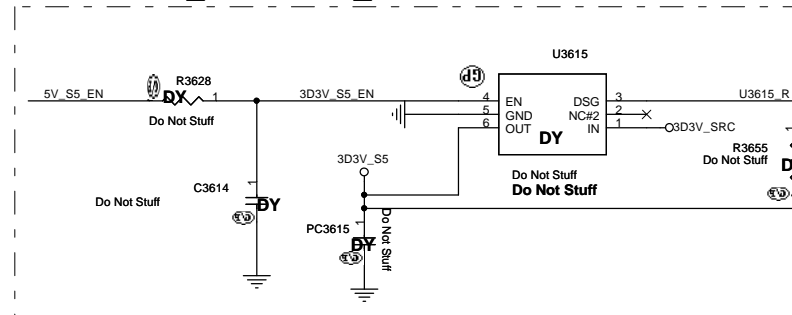
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Title			
USB 3.0 Controller			
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Power Sequence

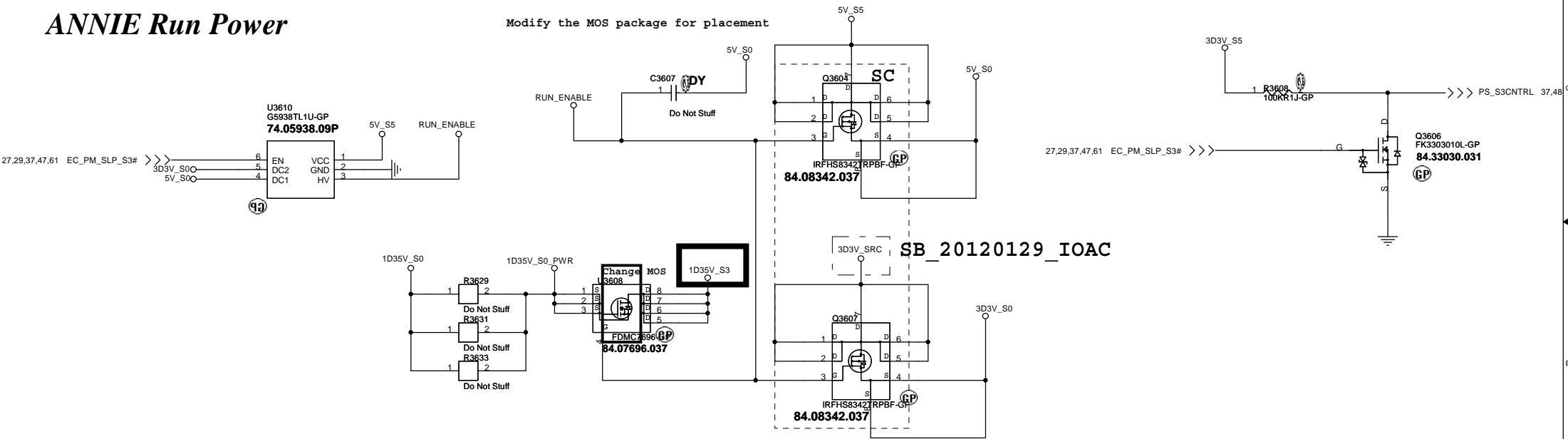


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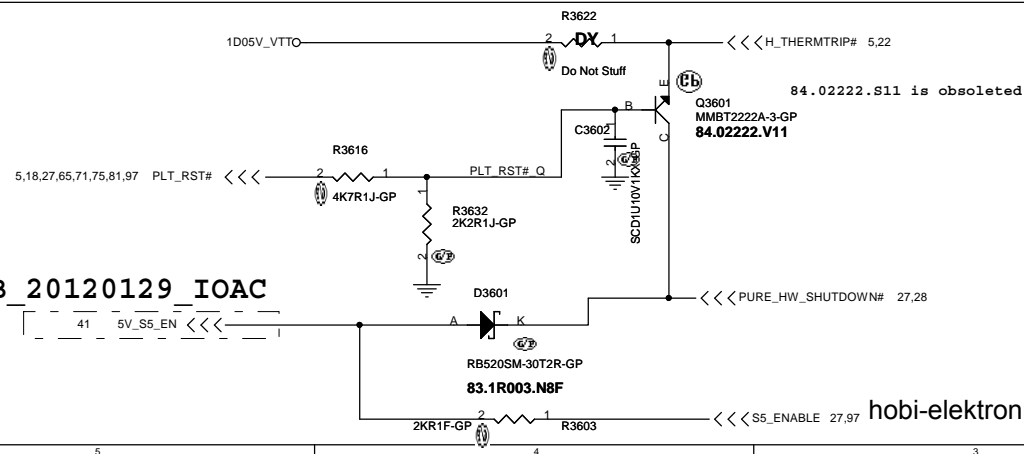


ANNIE Run Power

Modify the MOS package for placement



SB_20120129_IOAC

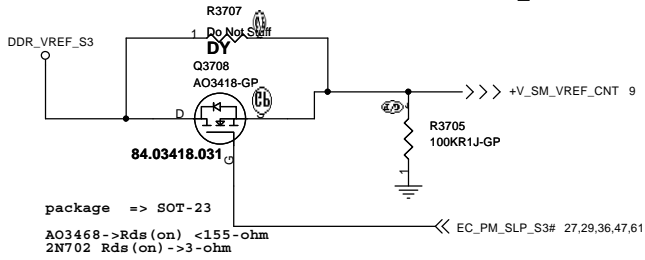


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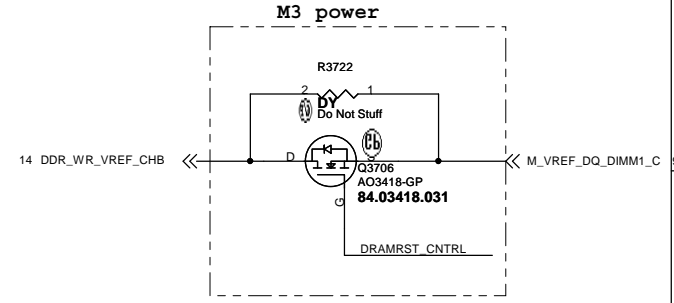
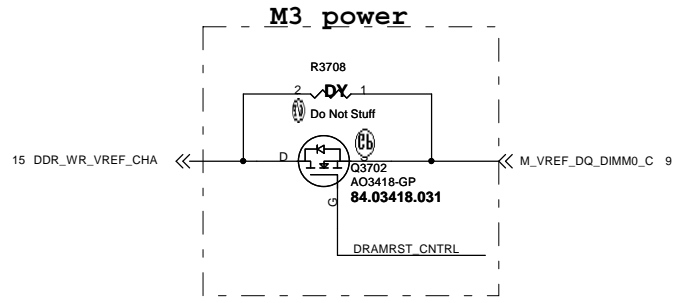
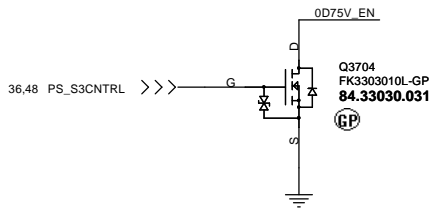
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Title Power Plane Enable		
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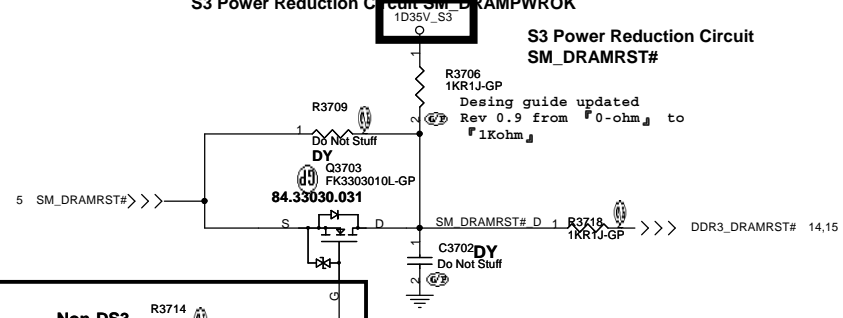
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



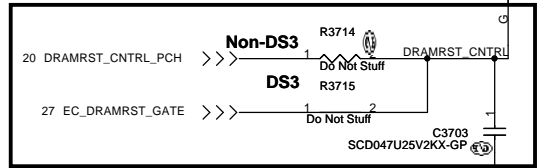
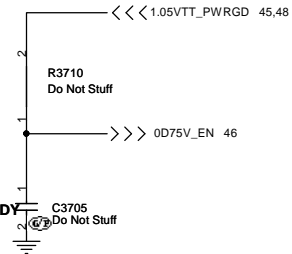
package => SOT-23
AO3468 -> Rds (on) <155-ohm
2N702 Rds (on) -> 3-ohm



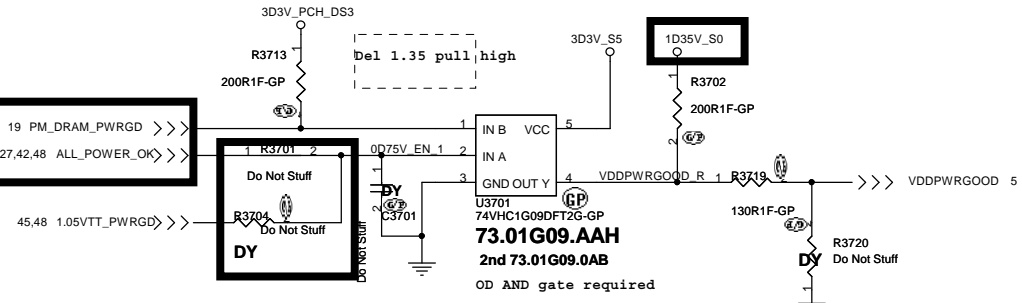
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMPWROK#
Desing guide updated
Rev 0.9 from '0-ohm' to
'1Kohm'



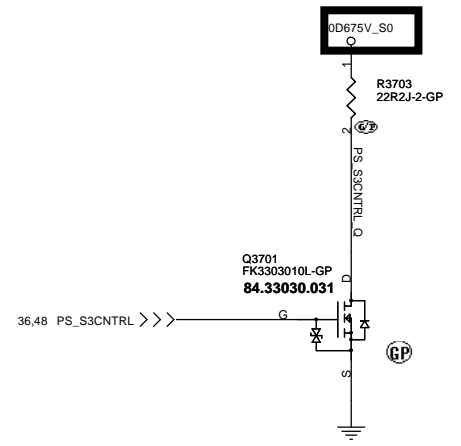
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Check DY R3701 or 04?

For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55 ± 200mV and the edge must be monotonic.

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Title: ADAPTER

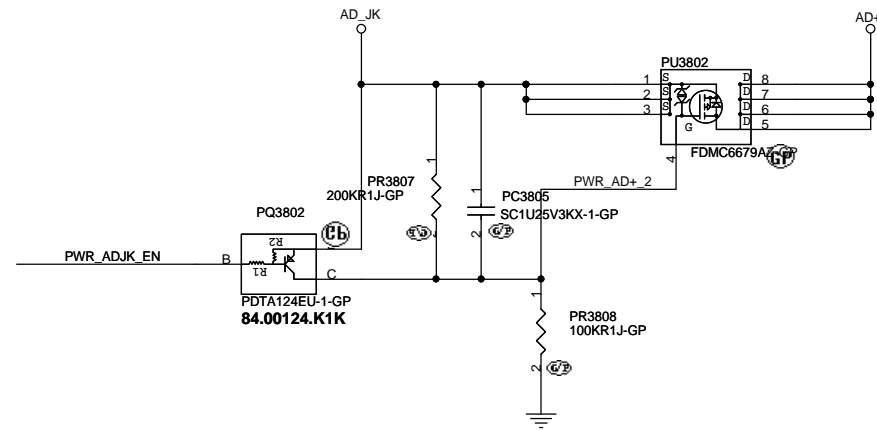
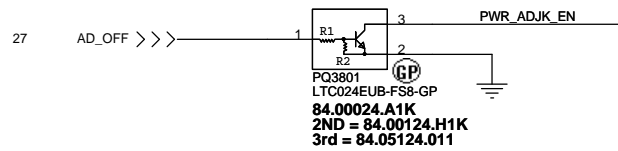
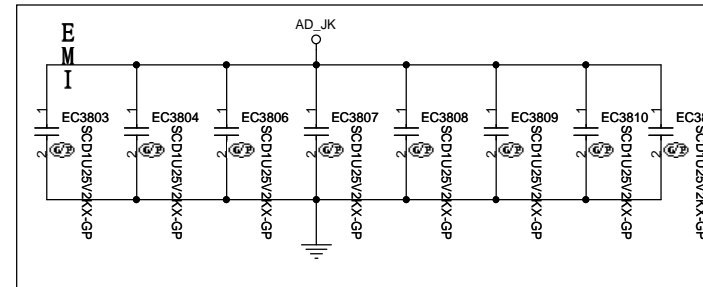
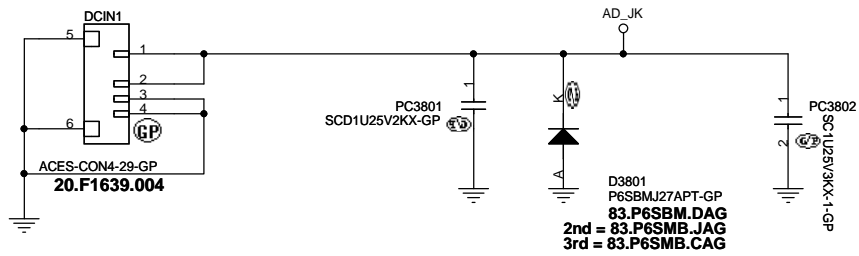
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ANNIE solution

1Pin=3A

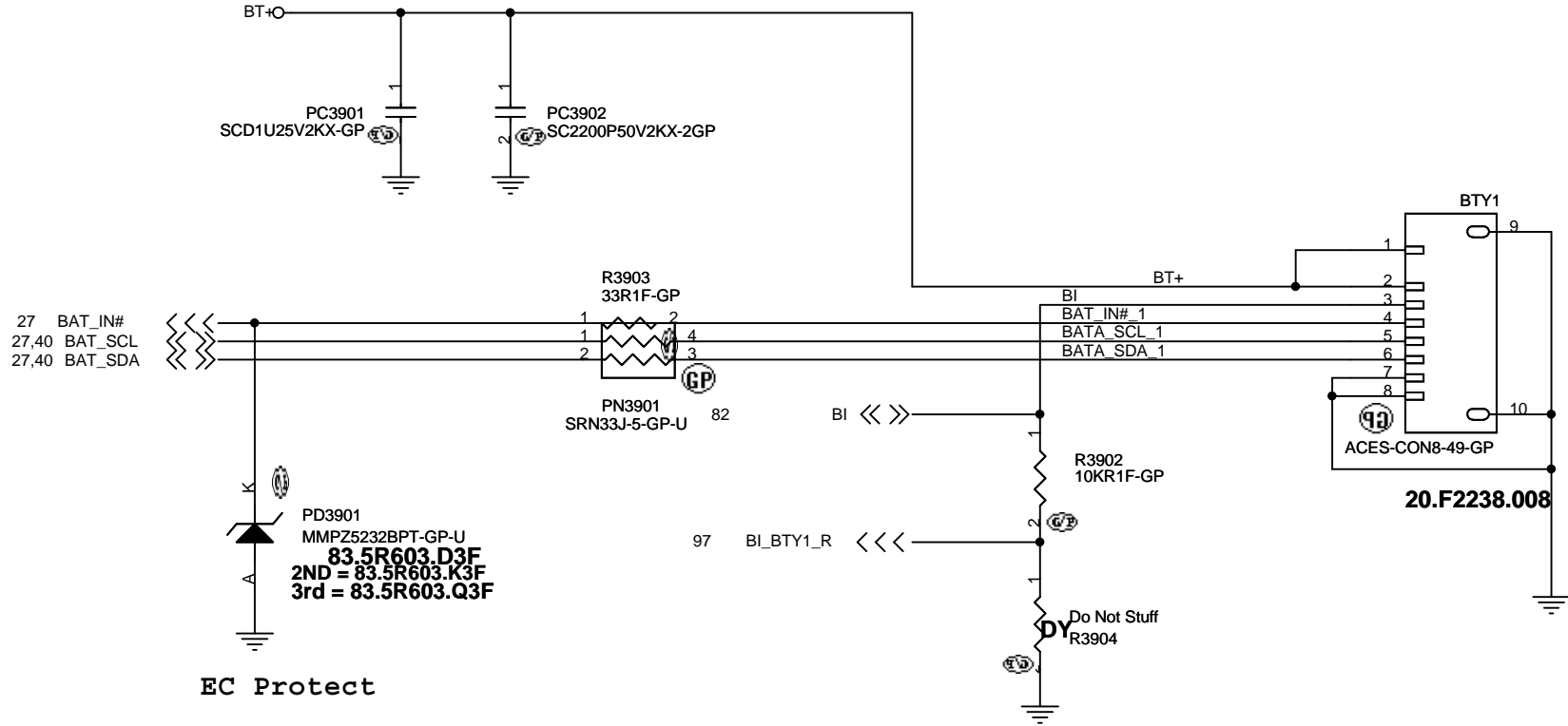
Adaptor in to generate DCBATOUT



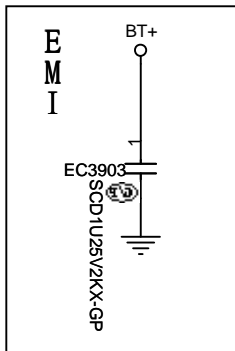
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Title			
DCIN JACK			
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BATTERY CONNECTOR



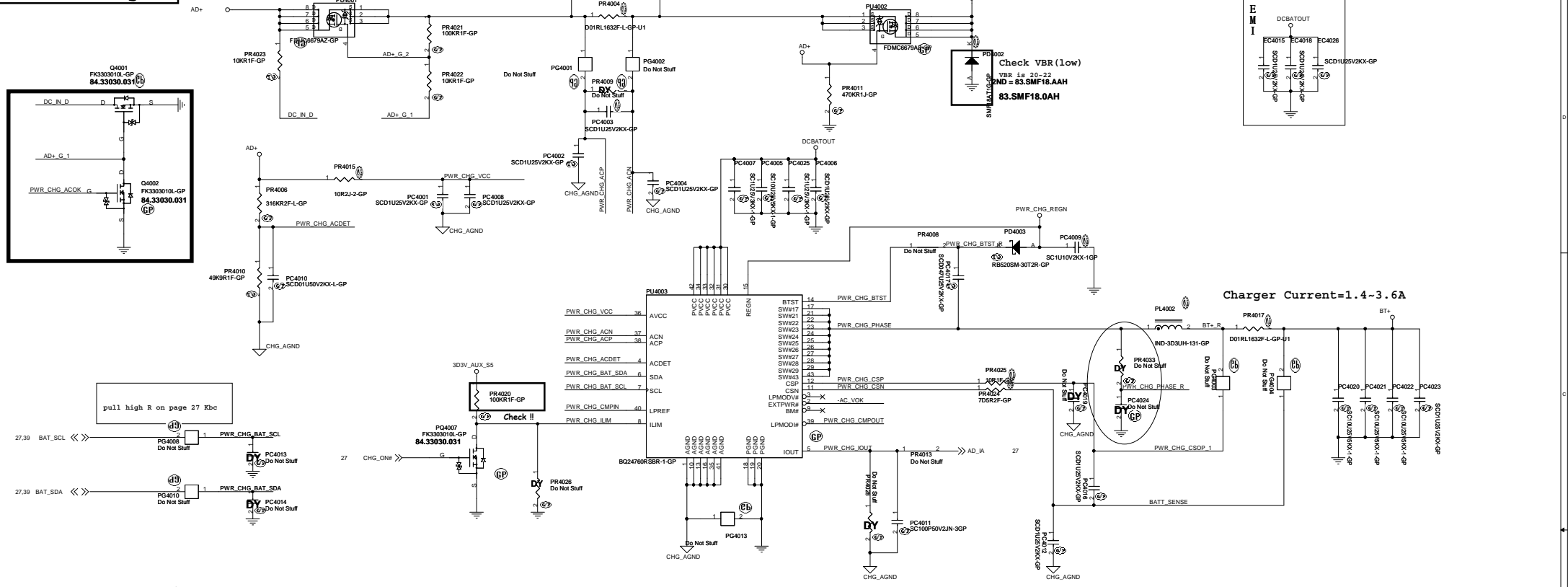
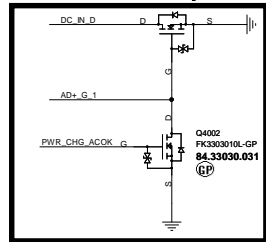
EC Protect



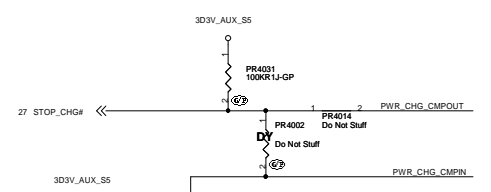
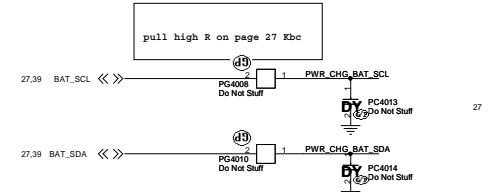
STORM

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Title BATT CONN			
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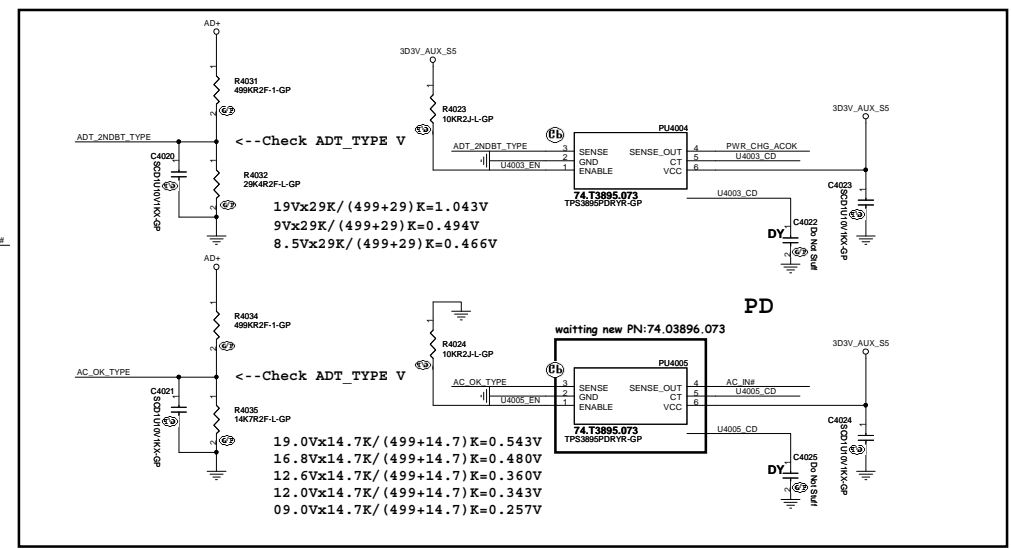
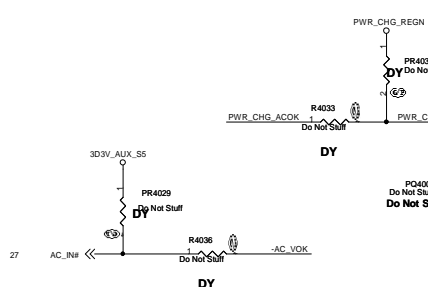
SSID = Charger



Charger Current=1.4-3.6A



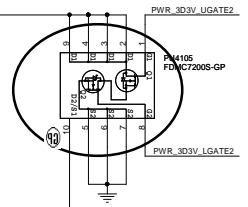
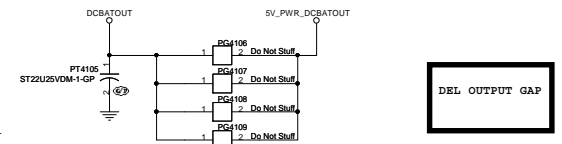
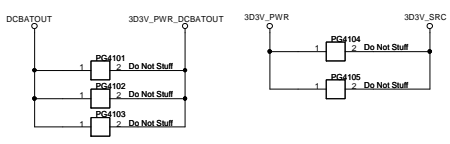
AD+ total power	R1	R2
45w	294k	49.9k
65w	187k	49.9k
90w	121k	49.9k



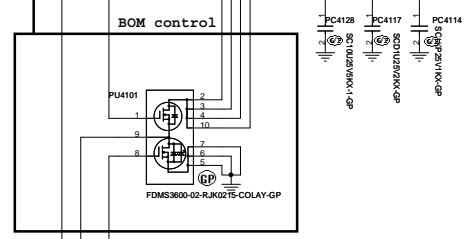
SSID = PWR.Plane.Regulator 3p3v5v

BOM control

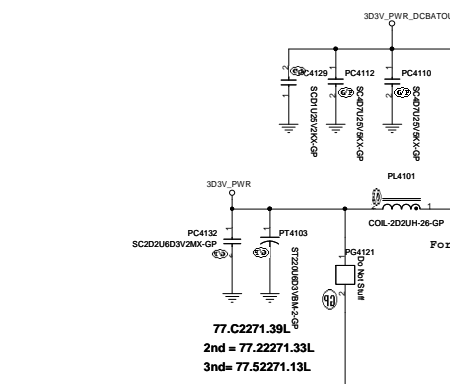
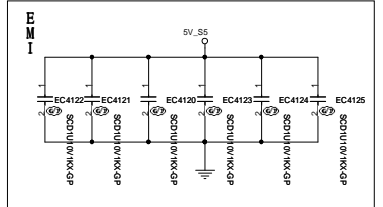
	Main source	2nd source
PU4101	84.03664.037 (FDM3664S)	84.00038.A37 (RJK03P8DPA)
	Mount	Mount



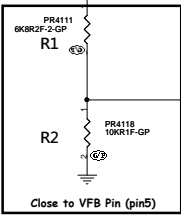
PU4103 need change to TP551275A
PN:74.51275.003
waiting for symbol



Design Current = 15A
25.1A < OCP < 29.3A



77.C2271.39L
2nd = 77.22271.33L
3nd = 77.52271.13L

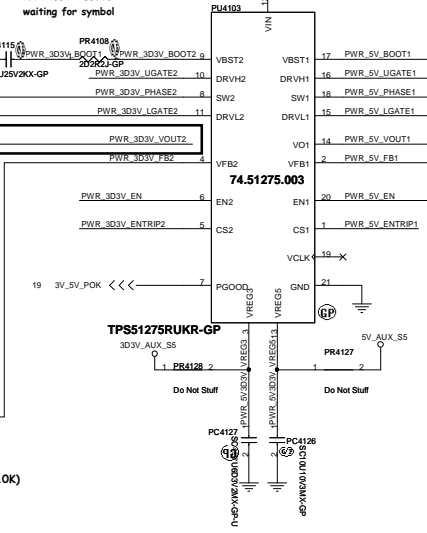


$$V_{out} = 2 * (1 + R1/R2)$$

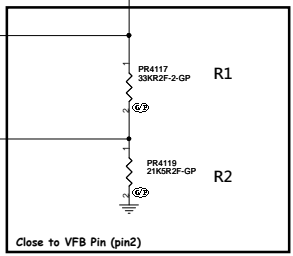
$$= 2 * (1 + 6.8K / 10K)$$

$$= 3.36V$$

I_{omaX} = 5A
OCP > 7.5A



See Table 1



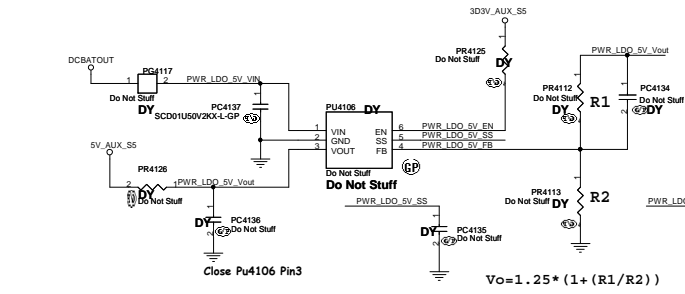
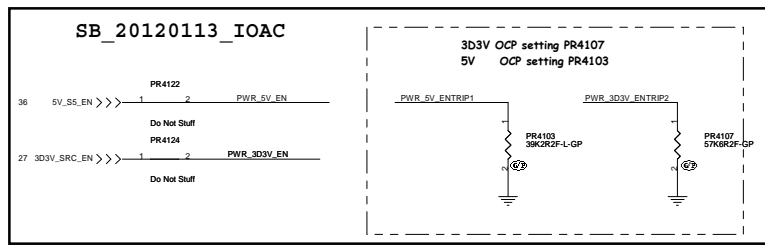
$$V_{out} = 2 * (1 + R1/R2)$$

$$= 2 * (1 + 33K / 21K)$$

$$= 5.14V$$

Table 1. SKIP mode operation (51275A)

	SKIPSEL	Skip mode operation
51275	n/a	Auto-skip
51275A	Hi	OOA
	Lo	Auto-skip



$$V_o = 1.25 * (1 + (R1/R2))$$

SSID = CPU.Regulator

Volterra's suggestion:
VCC 31x22uF(0603) for 1-PHASE VCC
VCCAXG 28x22uF(0603) for 1-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	825ohm	825ohm
1V	191ohm	191ohm

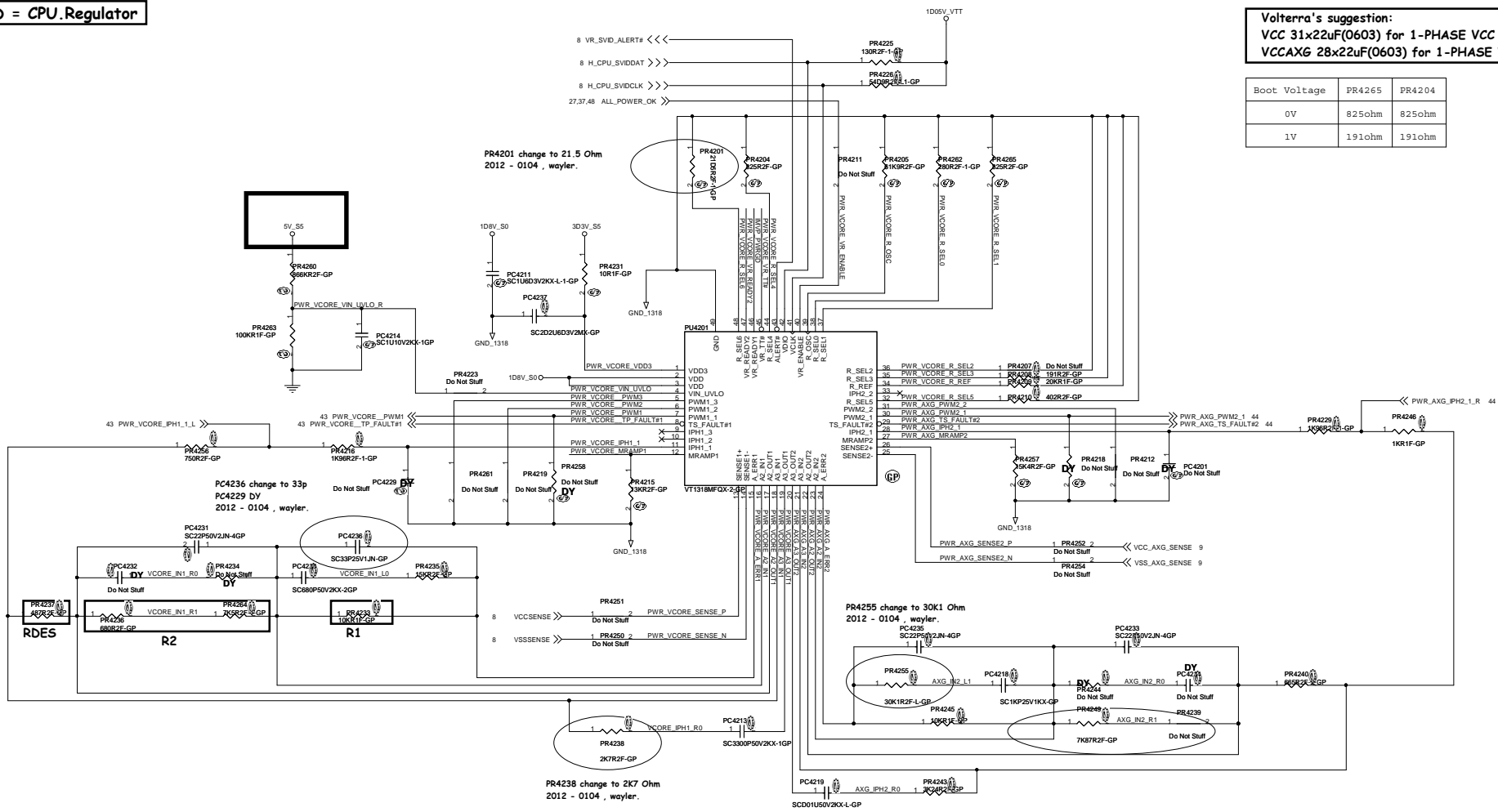


Table 1: R_{DES} Selection Table

1	20	1180
1	24	976
1	28	845
1	32	732
1	36	649
1	40	580
1	44	536
1	48	487
2	40	580
2	48	487
2	56	445
2	64	403
2	72	369
2	80	340
2	88	315
2	96	293
3	60	377
3	72	317
3	84	273
3	96	240
3	108	214
3	120	193
3	132	175
3	144	160

R₁ and R₂ Selection

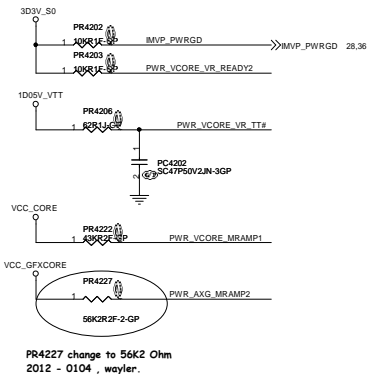
Along with R_{DES}, The values of R₁ and R₂ determine the load line according to Equation 4.

Equation 4

$$R_{LL}[\Omega] = \frac{R_1}{R_2} \cdot \frac{1}{2.2} \cdot R_{DES} \cdot \frac{1}{K_f}$$

With K_f being the slave current feedback gain and R₁ having a typical value of 10kΩ. Next, the required value of R₂ can be calculated to achieve the desired load line via Equation 4 and previously selected values for R₁ and R_{DES}.

→ R_{LL} is inverse proportion to R₂
 K_f=95000



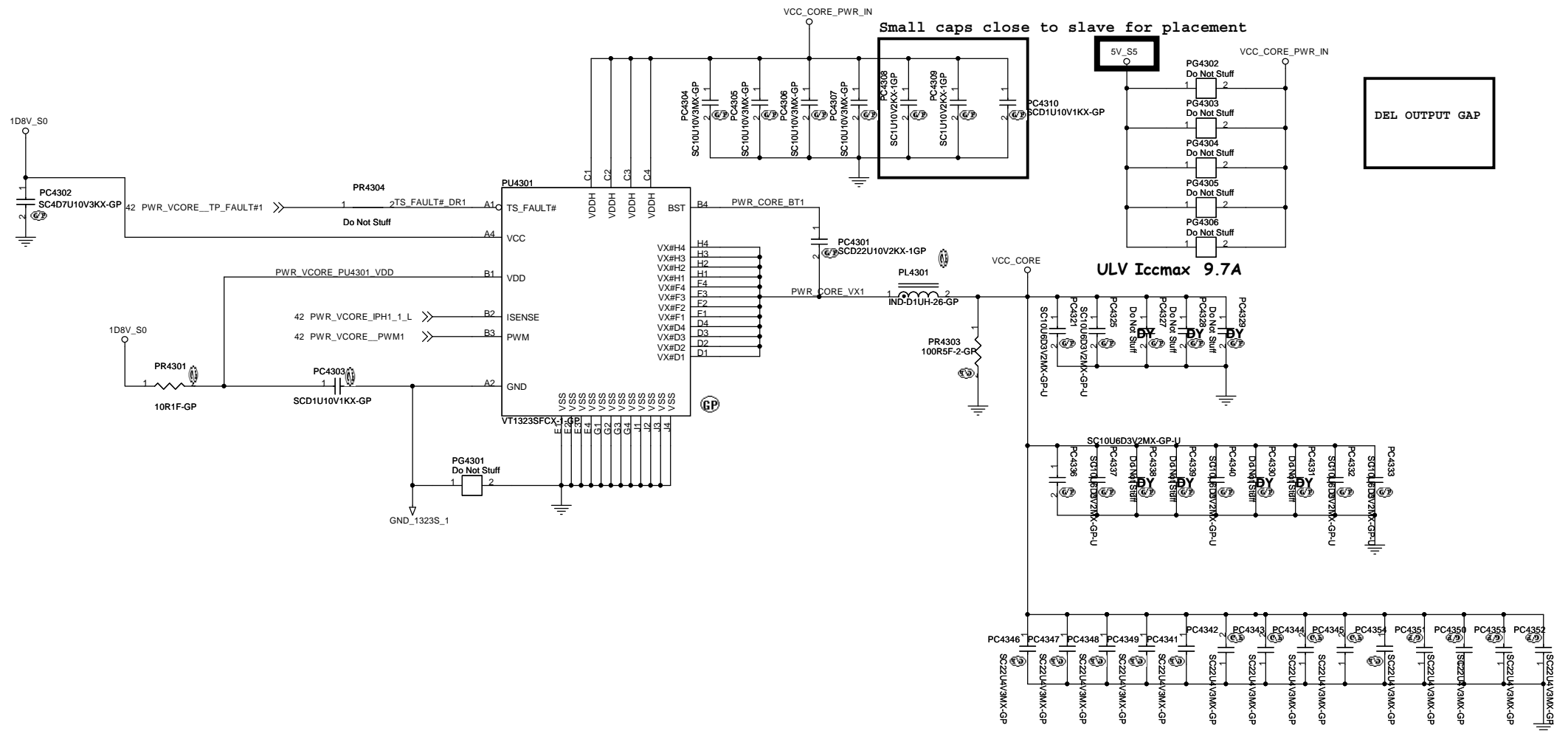
STORM

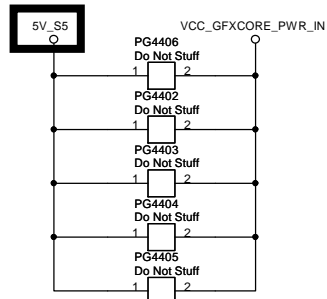
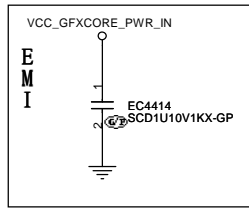
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.

Title: **VT1318+1323_CPU_CORE2+1(1/3)**

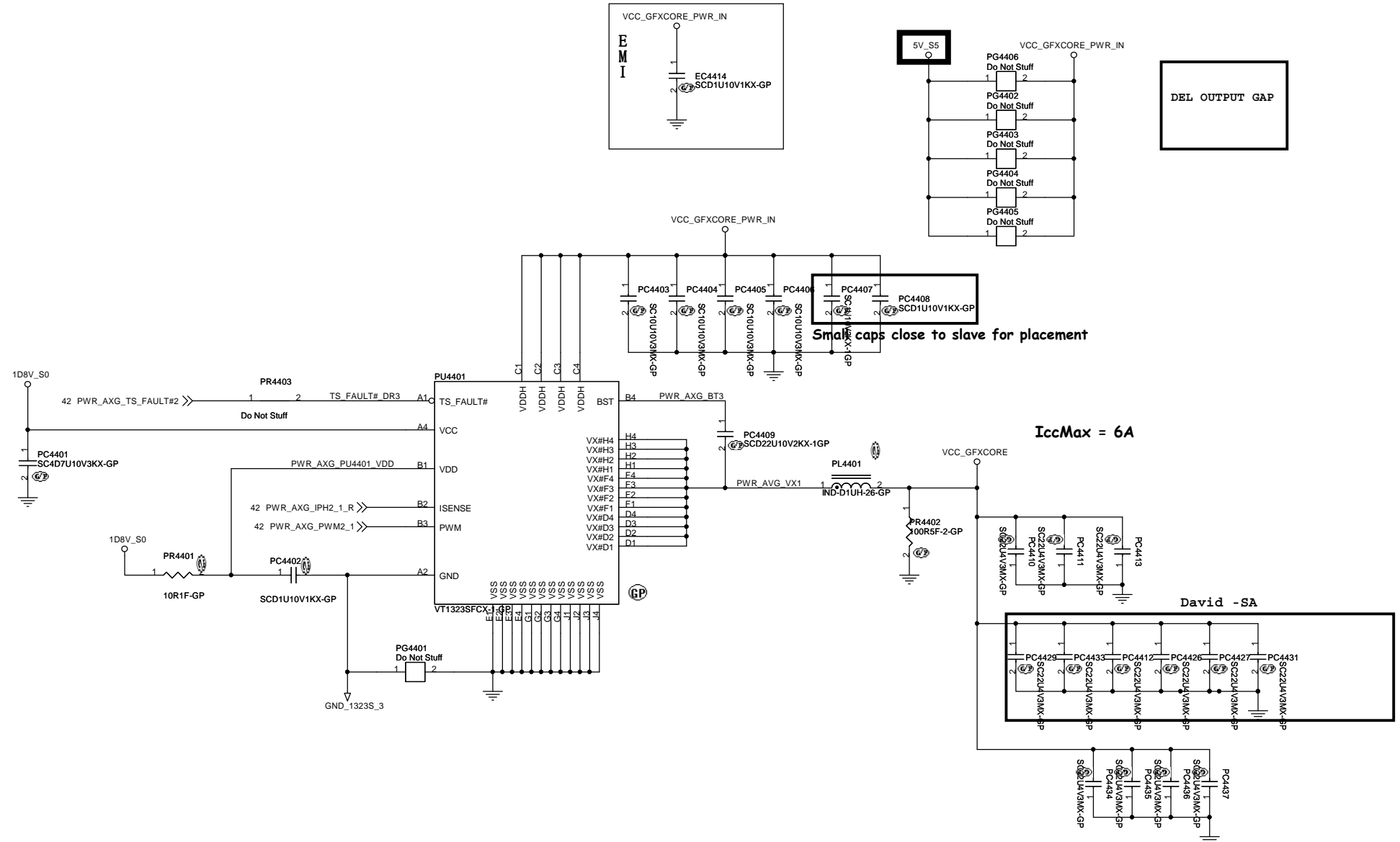
Size: Document Number Rev: -1

Date: Wednesday, June 27, 2012 Sheet: 42 of 102





DEL OUTPUT GAP



David -SA

STORM

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

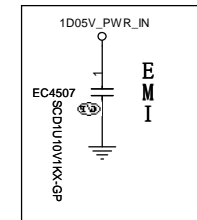
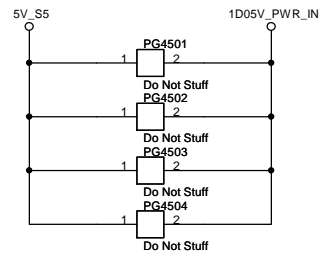
Title: **VT1318+1323_CPU_CORE2+1(3/3)**

Size	Document Number	Rev
	Storm	-1

Date: Monday, June 25, 2012 Sheet 44 of 102

Delete the old version VT386F circuit

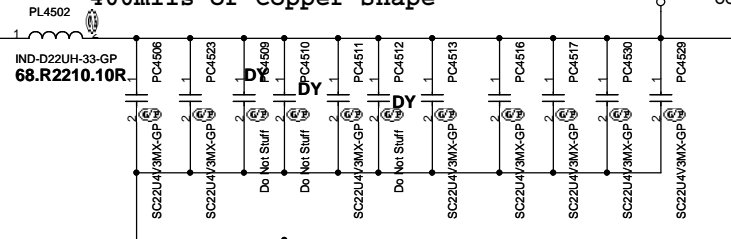
140mils or Copper Shape



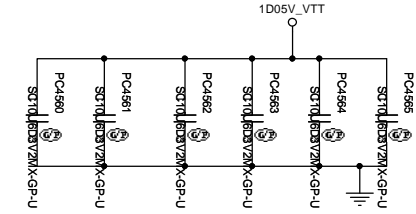
DEL OUTPUT GAP

PL4502 LAB2改為68.R2210.10R

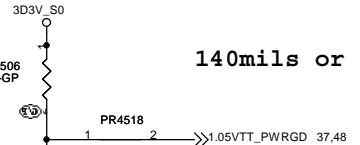
400mils or Copper Shape



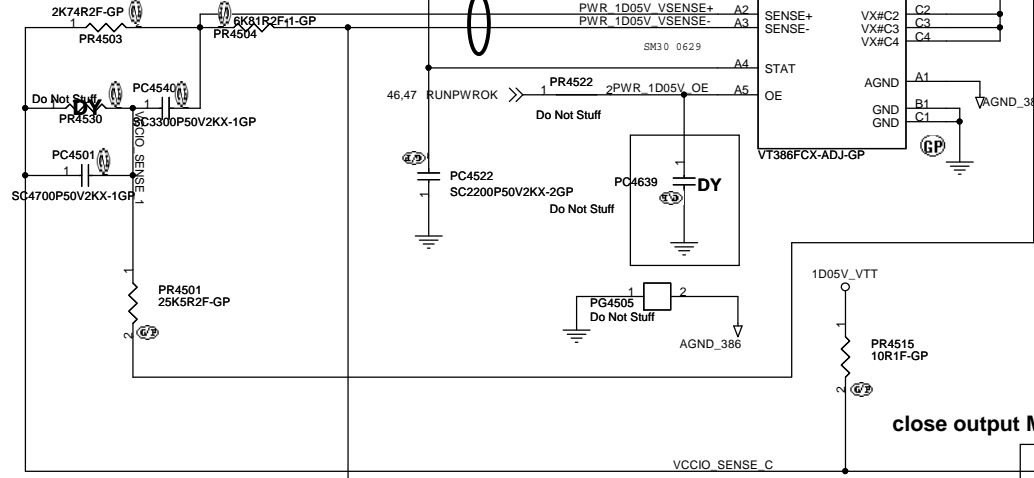
Design Current = 12A
OCP > 19.5A



Change to 0603_4V



Diff pair



VSENSE-TRACE
ROUTED DIFFERENTIALLY
PARALLEL TO VSENSE+

close output MLCC

PR4520 10R1F-GP

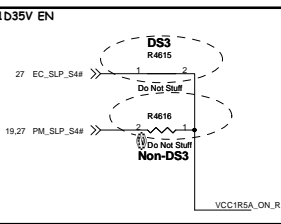
Change 0R PAD to 0R and DY

STORM

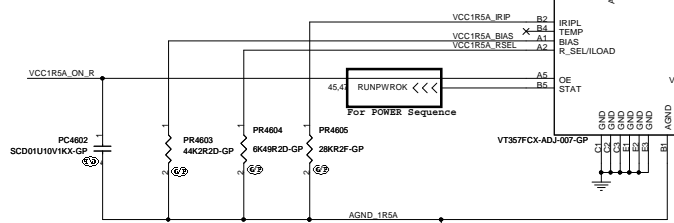
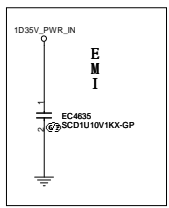
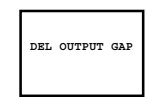
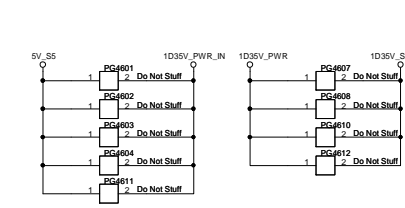
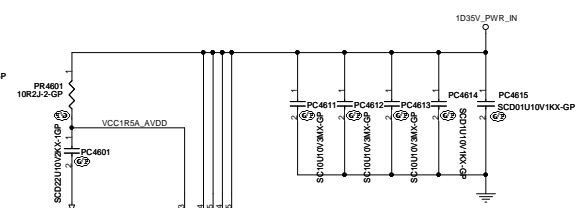
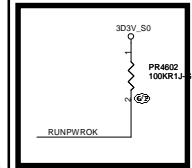
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VT386 +1.05V VTT**

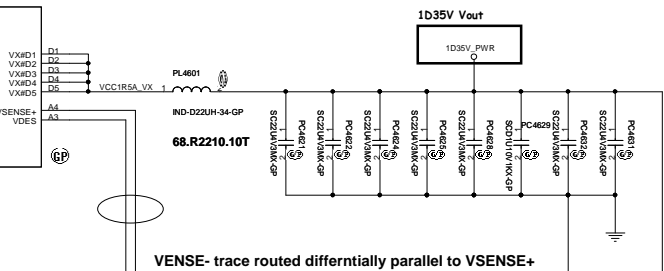
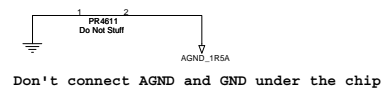
Size A3	Document Number	Rev
Date: Monday, June 25, 2012	Storm	-1
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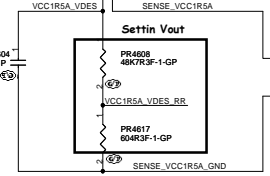
VT357 for 1D35V



collect all AGND referenced signals before dropping to GND

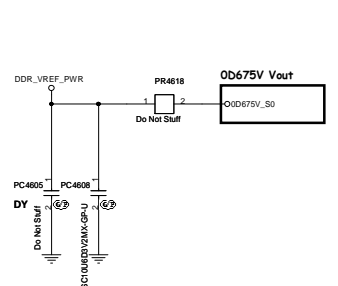
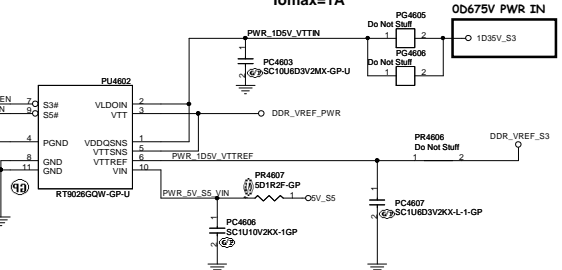
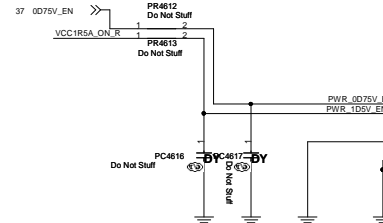


VENSE- trace routed differentially parallel to VSENSE+



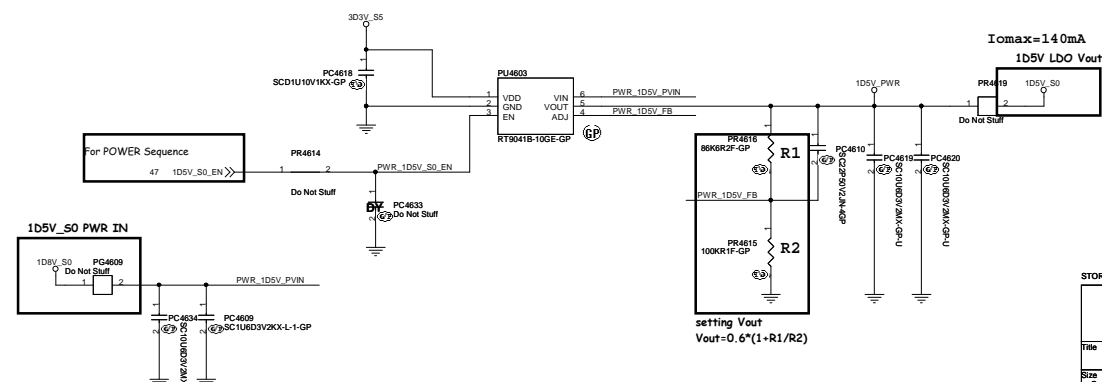
RT9026 for 0D675V_S0

0.675V Iomax=1A



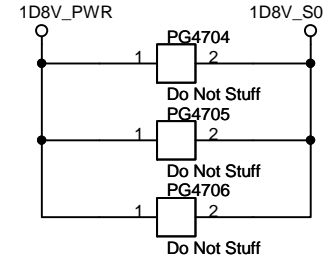
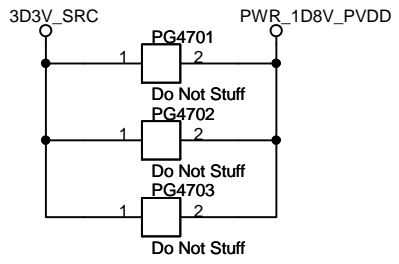
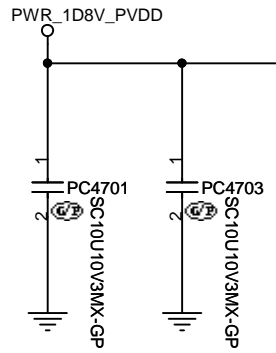
PT9041B for 1D5V_S0

Iomax = 140mA



setting Vout
Vout=0.6*(1+R1/R2)

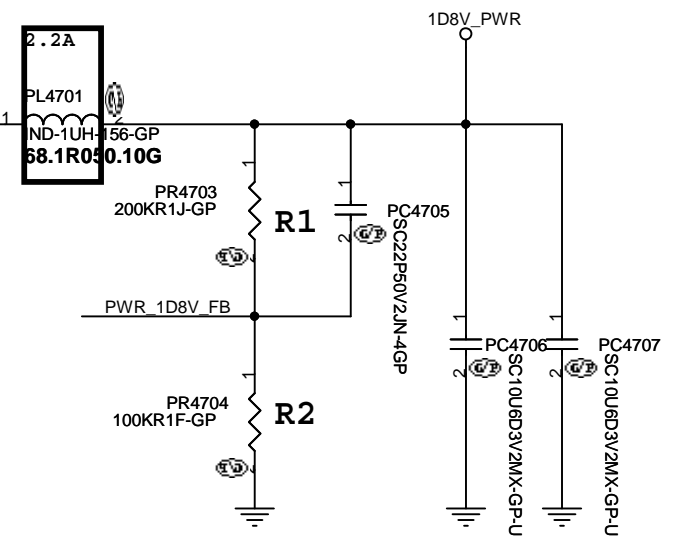
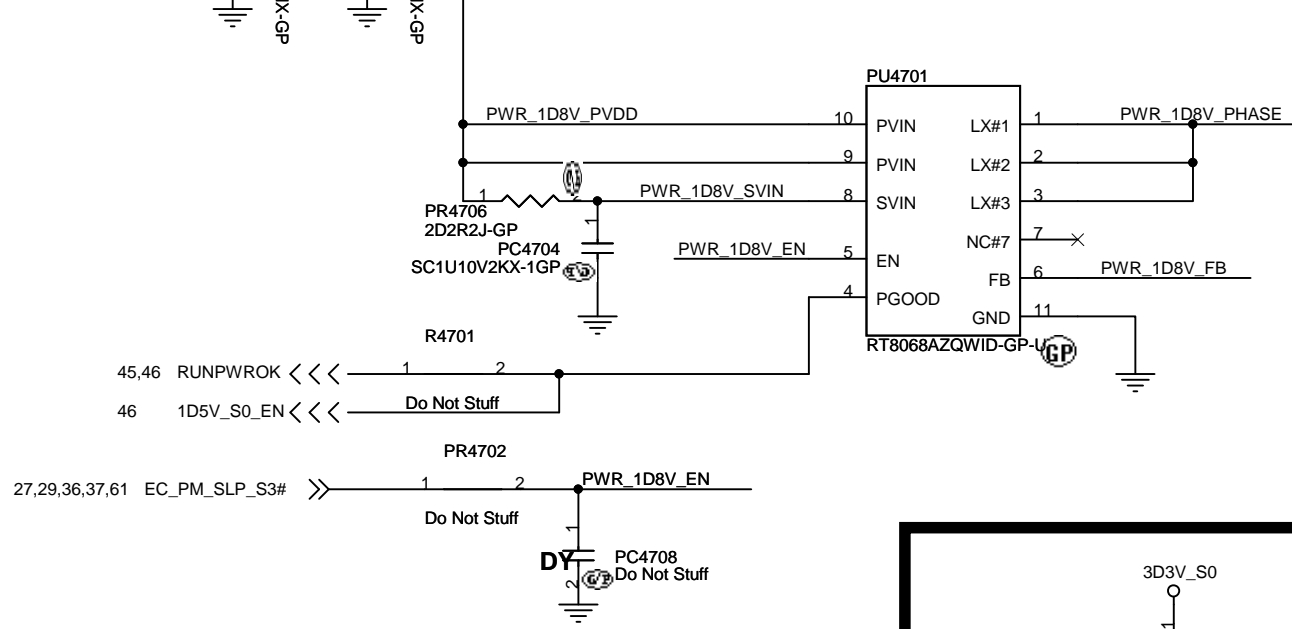
Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.		
DC-DC VCC1R5A		
Title	Document Number	Rev
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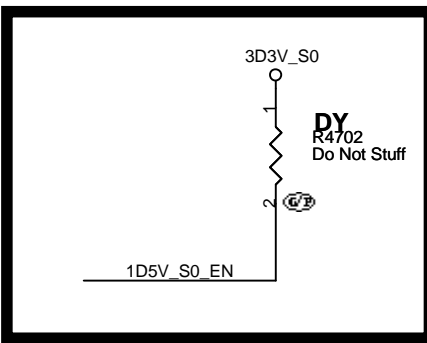
DEL OUTPUT GAP

I_{omax} = 1.242A
OCP > 5A

RT8068A for 1D8V_S0



$$V_o = 0.6 * (1 + (R1/R2))$$



STORM

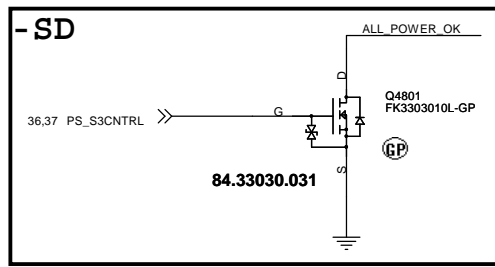
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **1D8V_S0 SYW231**

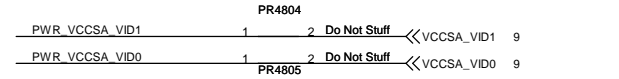
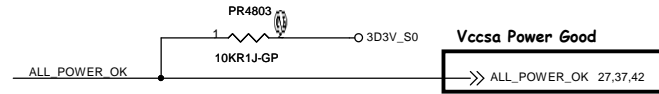
Size A4 Document Number **Storm** Rev -1

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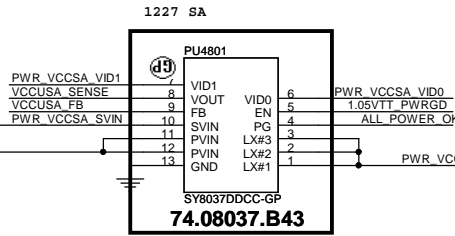
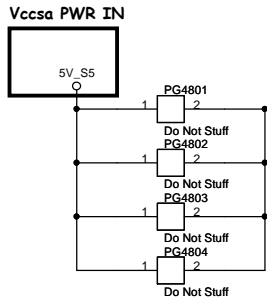
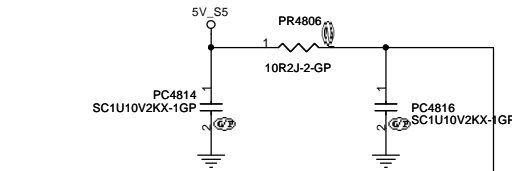
SY8037 for VCCSA



VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

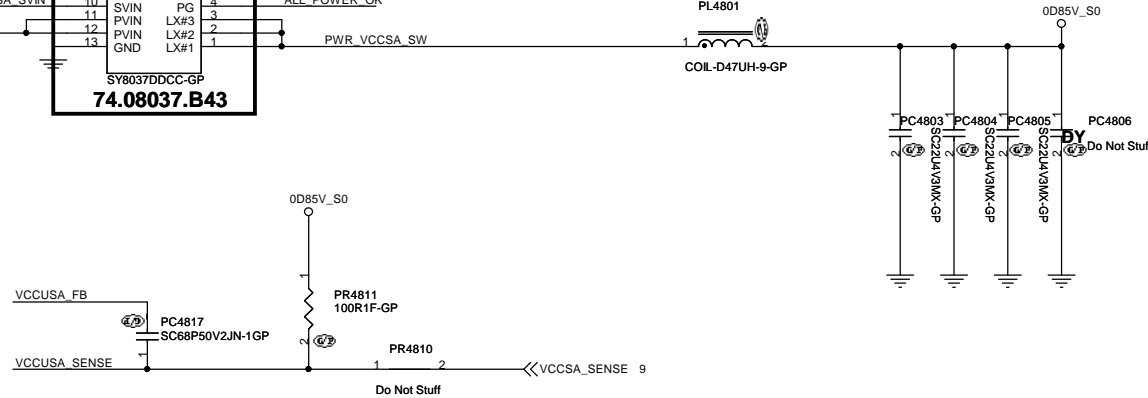


DEL OUTPUT GAP



CYNTEC - PCMB042T-R47MS
 package : 4.15 * 4 * 1.8
 ID 7 A ~ 9.5A
 DCR = 12.5 ~ 14mOhm

Design Current = 4 A
 6.6A < OCP < 7.8A



STORM

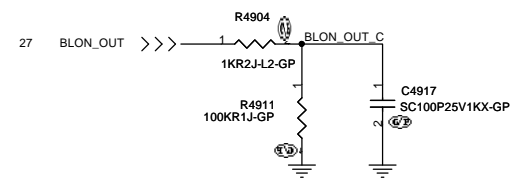
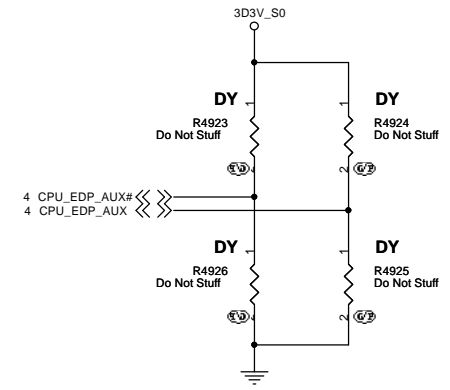
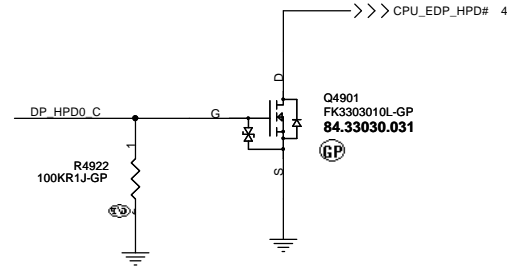
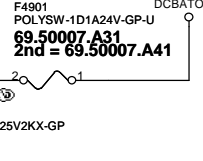
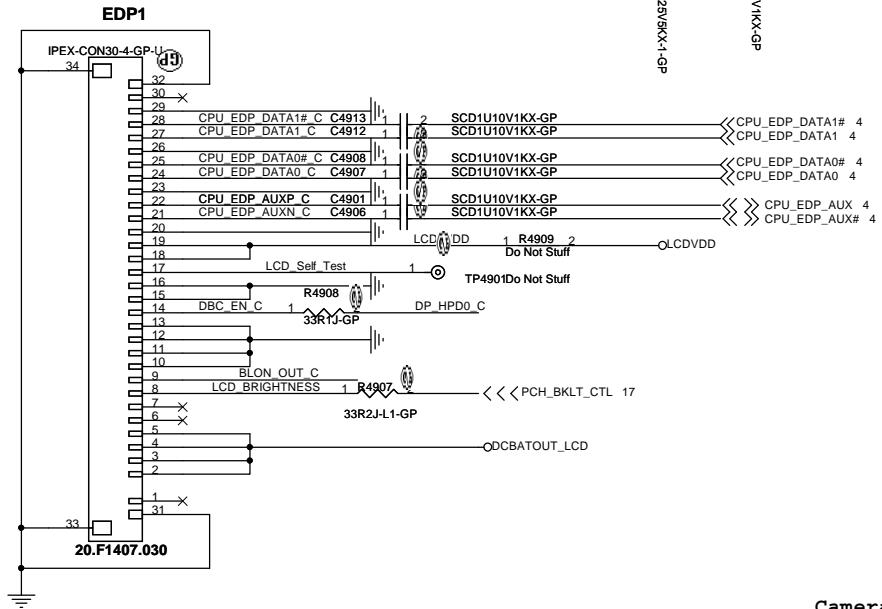
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **SY8037_VCCSA**

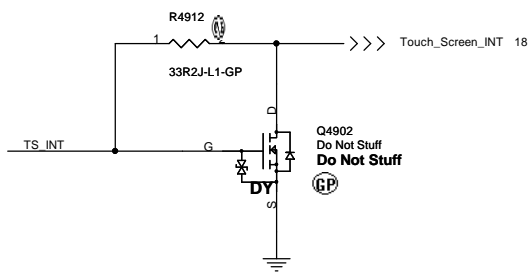
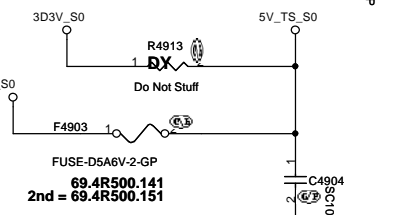
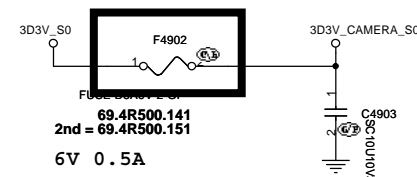
Size A3	Document Number	Rev -1
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SSID = VIDEO

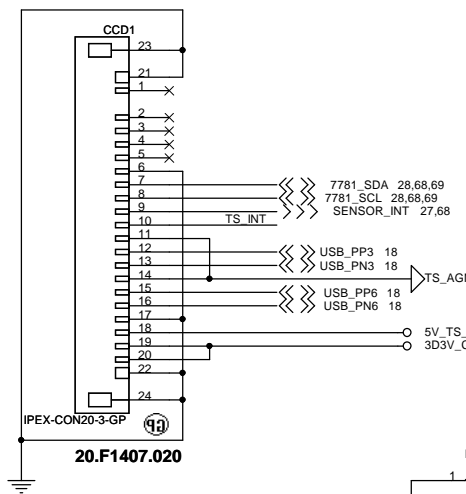
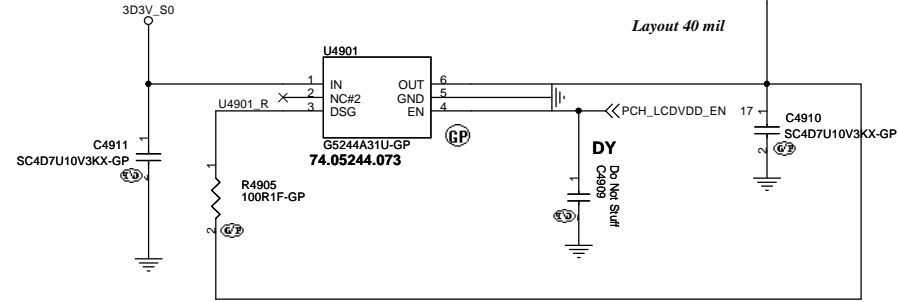
EDP CONNECTOR



Camera Power



output turn-On Rising Time:1.3ms~2.7ms
current limit:2~3.3A
Previous parts (74.05285.07F) rise time:1.5ms ~5ms
current limit:1.5ms~ 3.5ms



STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter CONN**

Size A3 Document Number: **Storm** Rev: **-1**

Date: Friday, June 29, 2012 Sheet 49 of 102

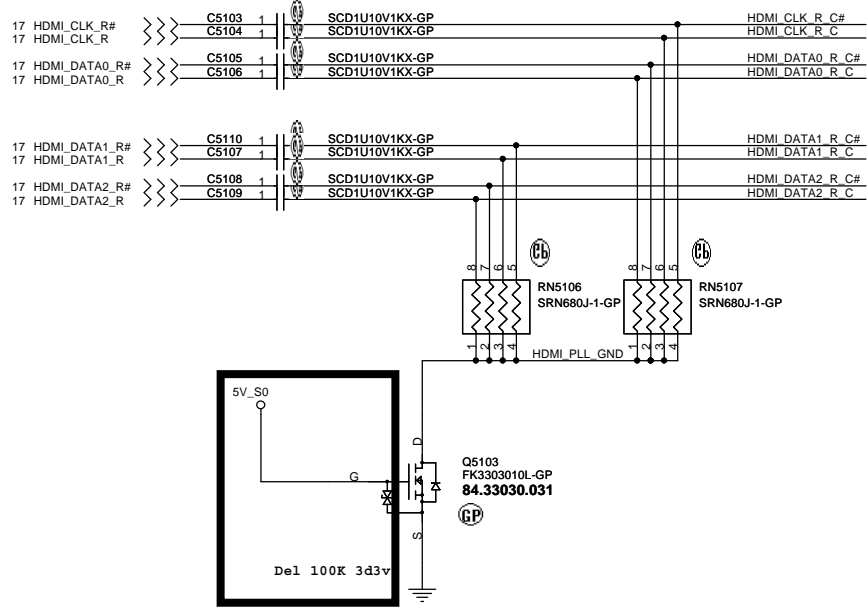
Pull High 5V Design on CRT Board
CRT DDCDATA & DDCCLK level shift

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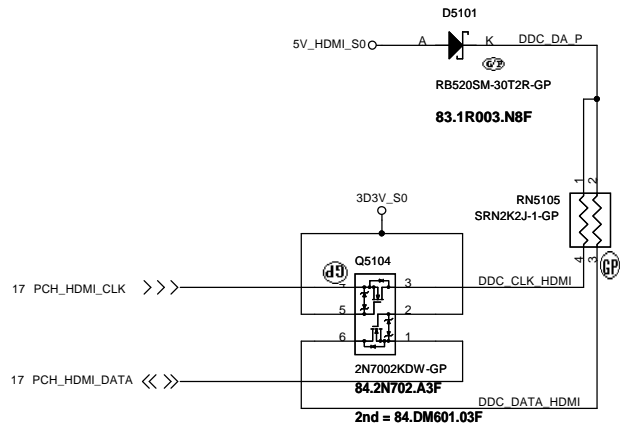
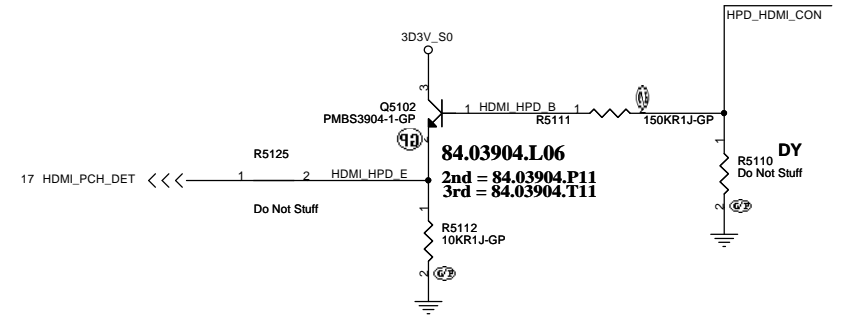
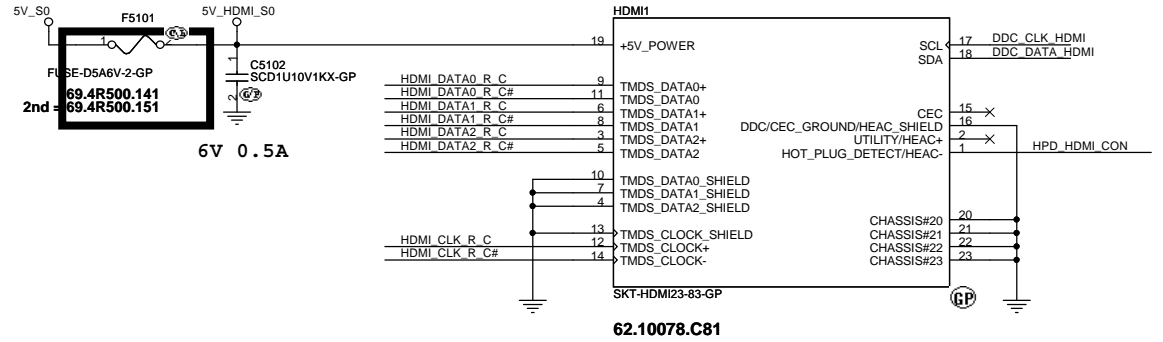
STORM

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CRT Connector			
Size A3	Document Number	Rev	
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HDMI Level Shifter



Micro HDMI CONN



Pin Defect

Pin	Signal Assignment
1	HPD_HDMI_CON
2	HPD_HDMI_CON
3	HPD_HDMI_CON
4	HPD_HDMI_CON
5	HPD_HDMI_CON
6	HPD_HDMI_CON
7	HPD_HDMI_CON
8	HPD_HDMI_CON
9	HPD_HDMI_CON
10	HPD_HDMI_CON
11	HPD_HDMI_CON
12	HPD_HDMI_CON
13	HPD_HDMI_CON
14	HPD_HDMI_CON
15	HPD_HDMI_CON
16	HPD_HDMI_CON
17	HPD_HDMI_CON
18	HPD_HDMI_CON
19	HPD_HDMI_CON
20	HPD_HDMI_CON
21	HPD_HDMI_CON
22	HPD_HDMI_CON
23	HPD_HDMI_CON
24	HPD_HDMI_CON
25	HPD_HDMI_CON
26	HPD_HDMI_CON
27	HPD_HDMI_CON
28	HPD_HDMI_CON
29	HPD_HDMI_CON
30	HPD_HDMI_CON
31	HPD_HDMI_CON
32	HPD_HDMI_CON
33	HPD_HDMI_CON
34	HPD_HDMI_CON
35	HPD_HDMI_CON
36	HPD_HDMI_CON
37	HPD_HDMI_CON
38	HPD_HDMI_CON
39	HPD_HDMI_CON
40	HPD_HDMI_CON
41	HPD_HDMI_CON
42	HPD_HDMI_CON
43	HPD_HDMI_CON
44	HPD_HDMI_CON
45	HPD_HDMI_CON
46	HPD_HDMI_CON
47	DDC_CLK HDMI
48	DDC_DATA HDMI
49	DDC_CLK HDMI
50	DDC_DATA HDMI
51	DDC_CLK HDMI
52	DDC_DATA HDMI
53	DDC_CLK HDMI
54	DDC_DATA HDMI
55	DDC_CLK HDMI
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72	DDC_DATA HDMI
73	DDC_CLK HDMI
74	DDC_DATA HDMI
75	DDC_CLK HDMI
76	DDC_DATA HDMI
77	DDC_CLK HDMI
78	DDC_DATA HDMI
79	DDC_CLK HDMI
80	DDC_DATA HDMI
81	DDC_CLK HDMI
82	DDC_DATA HDMI
83	DDC_CLK HDMI
84	DDC_DATA HDMI

Pin Defect

Pin 22 = Pin 21

Pin 23 = Pin 22

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STORM

STORM

緯創資通		Wistron Corporation	
<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
eDP			
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Date: Monday, June 25, 2012		of 102	

(Blanking)

STORM

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

S-VIDEO

Size
A4

Document Number

Storm

Rev
-1

Date: Monday, June 25, 2012

Sheet 53 of 102

(Blanking)

STORM

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Storm

Rev
-1

Date: Monday, June 25, 2012

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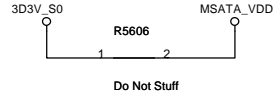
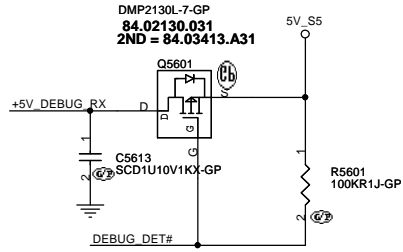
SSID = User.Interface

ITP Connector

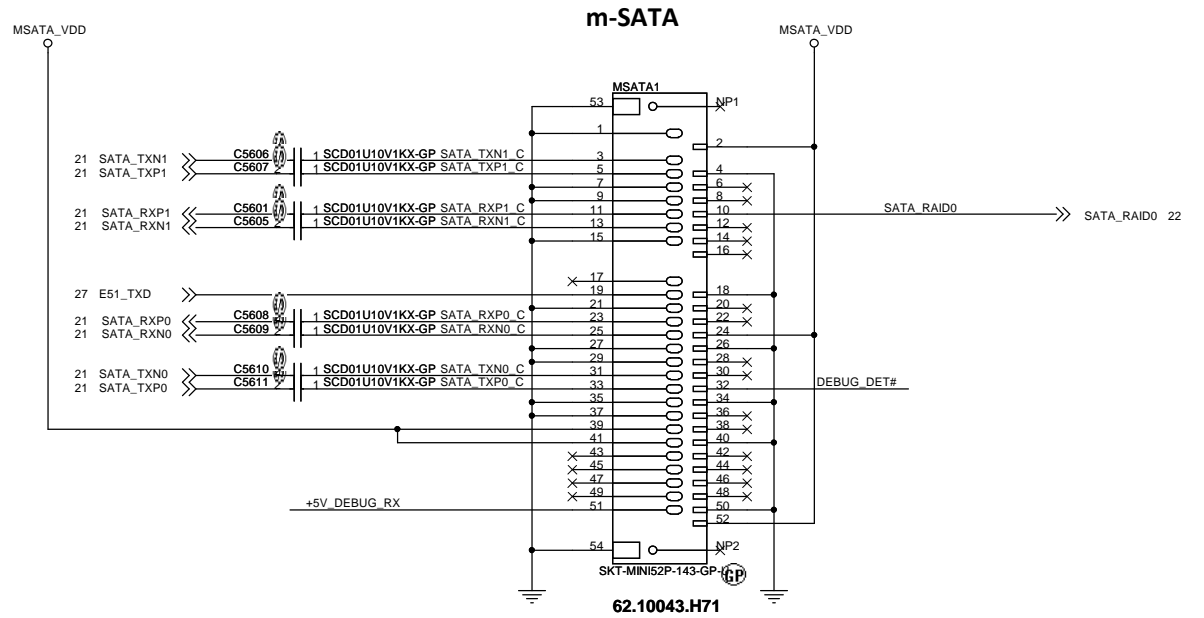
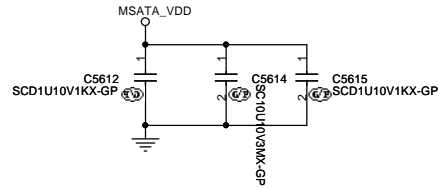
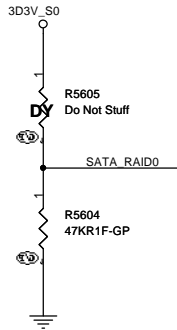
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

STORM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>ITP</i>			
Size	Document Number		Rev
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Date:	Monday, June 25, 2012	Sheet 55	of 102



DEBUG CARD



ESATA Power

USB CHARGER

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STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

E-SATA/USB CHARGER

Size
A3

Document Number

Storm

Rev

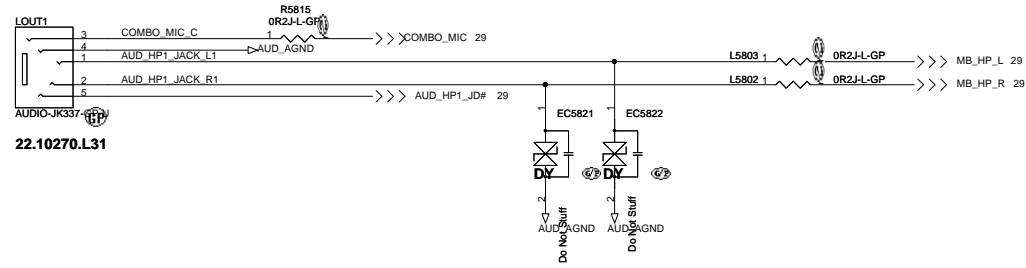
-1

Date: Monday, June 25, 2012

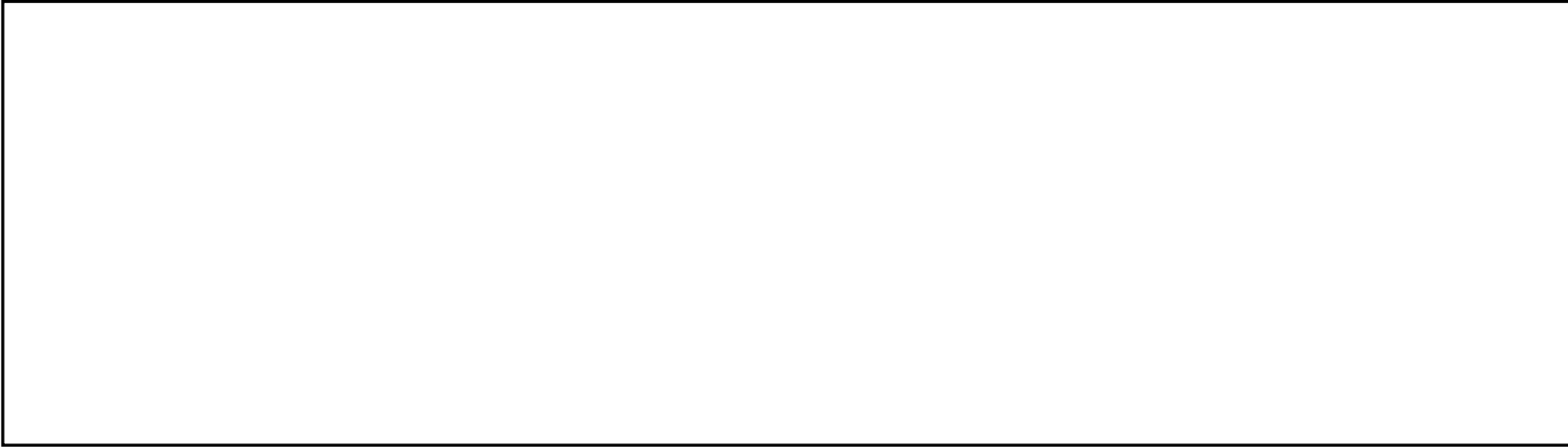
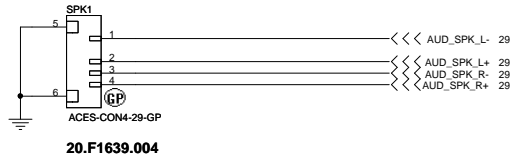
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SSID = AUDIO

LINE OUT



Speaker Connector



STORM

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title Audio Jack</p>		
Size Custom	Document Number Storm	Rev -1
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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

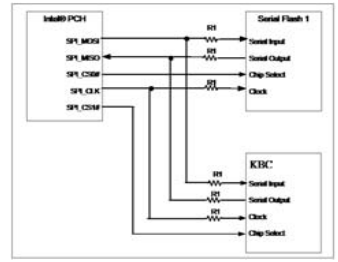
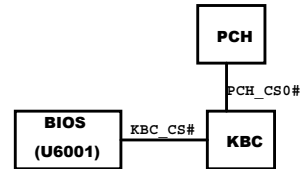
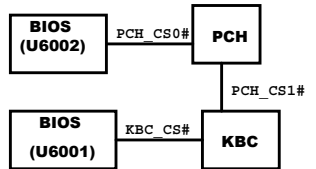
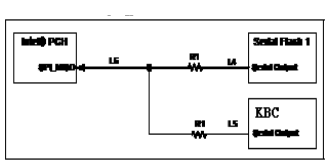
Without LAN

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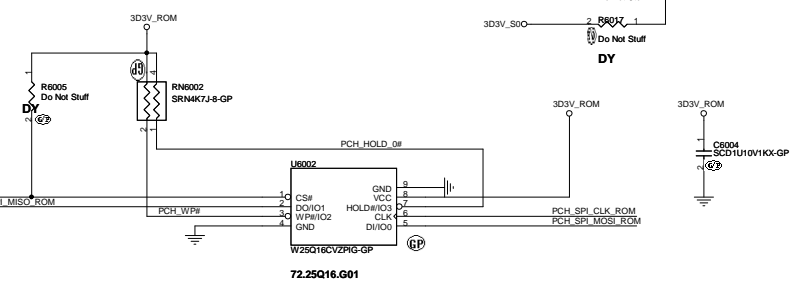
STORM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LAN CONNECTOR			
Size A4	Document Number Storm		Rev -1
Date: Monday, June 25, 2012		Sheet 59 of	102

SSID = Flash.ROM



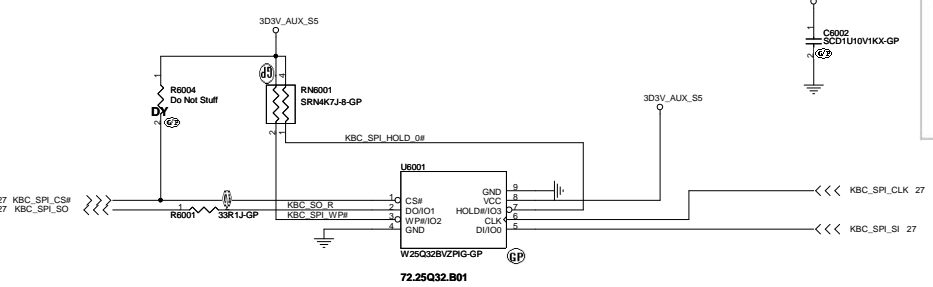
SPI Flash ROM(2M) for PCH



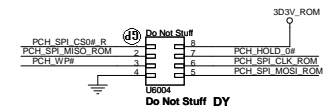
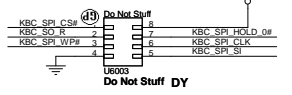
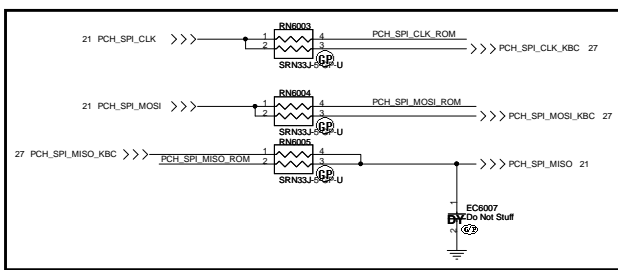
Flash ROM:72.25Q16.G01(2M)

SPI Flash ROM(4M) for KBC

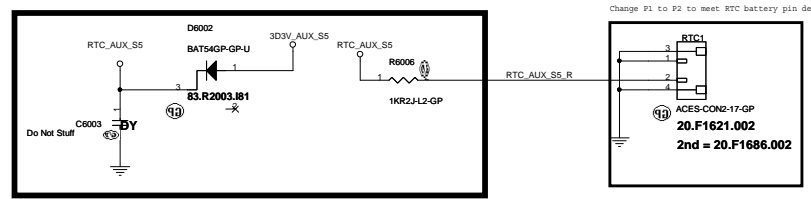
20111208-SA



Flash ROM:72.25Q32.B01(4M)



SSID = RBATT



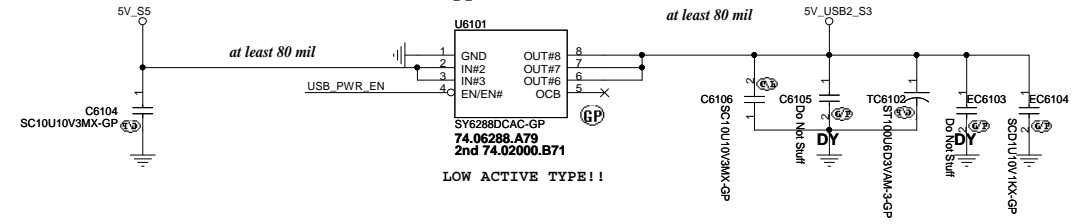
RTC battery charger circuit

STORM

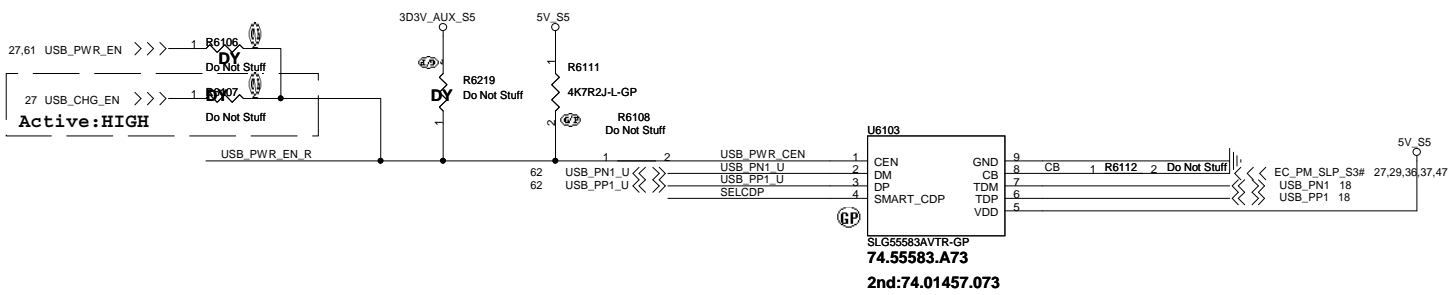
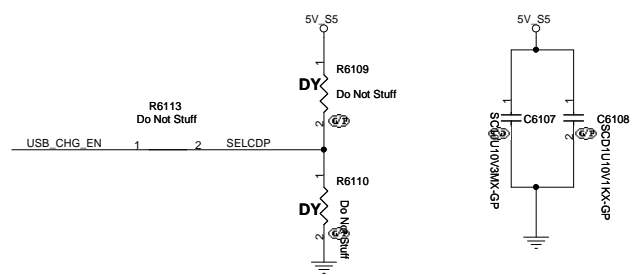
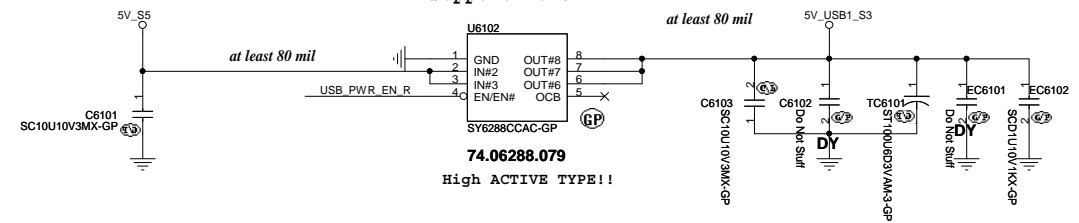
<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.</p>	
<p>Title Flash(KBC+PCH)/RTC</p>	
Size	Document Number
Chiltron	Storm
Date: Monday, June 25, 2012	Sheet 60 of 102

SSID = USB

Change Main source Support 2.45A



Change Main source Support 2.45A



Pin #	Name	Type	Description
1	CEN#	Output	P-FET Open Drain Output. Current Limit Switch (CLS) Control Output. CB changes from 0 to 1 or 1 to 0. CEN# will be high for 2 seconds (typ)
4	SMART-CDP	Input	Input Control logic (see truth table)
8	CB	Input	Switch Control Bit 0 = autodetection charger identification active 1 = charging downstream port with active USB2.0 data communication mode with 1.5A support

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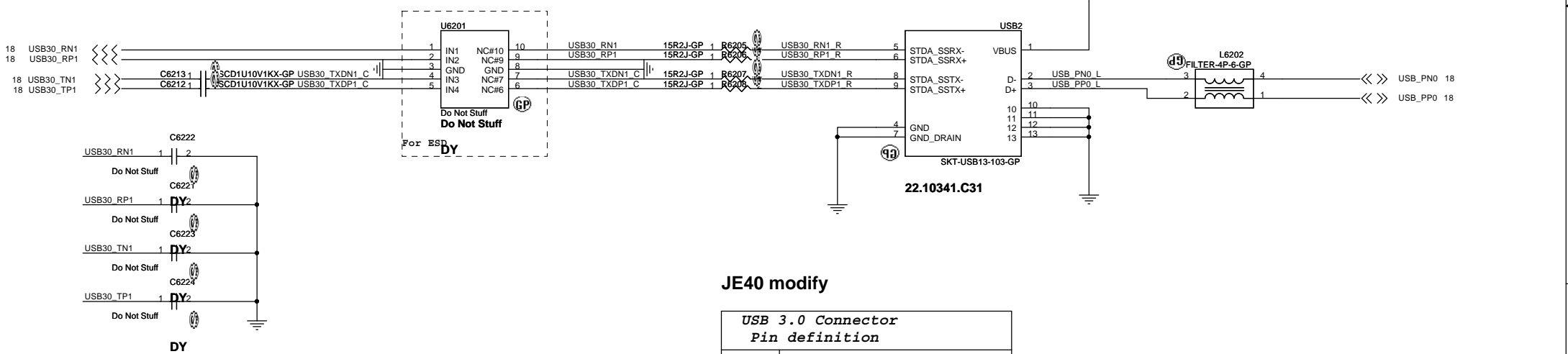
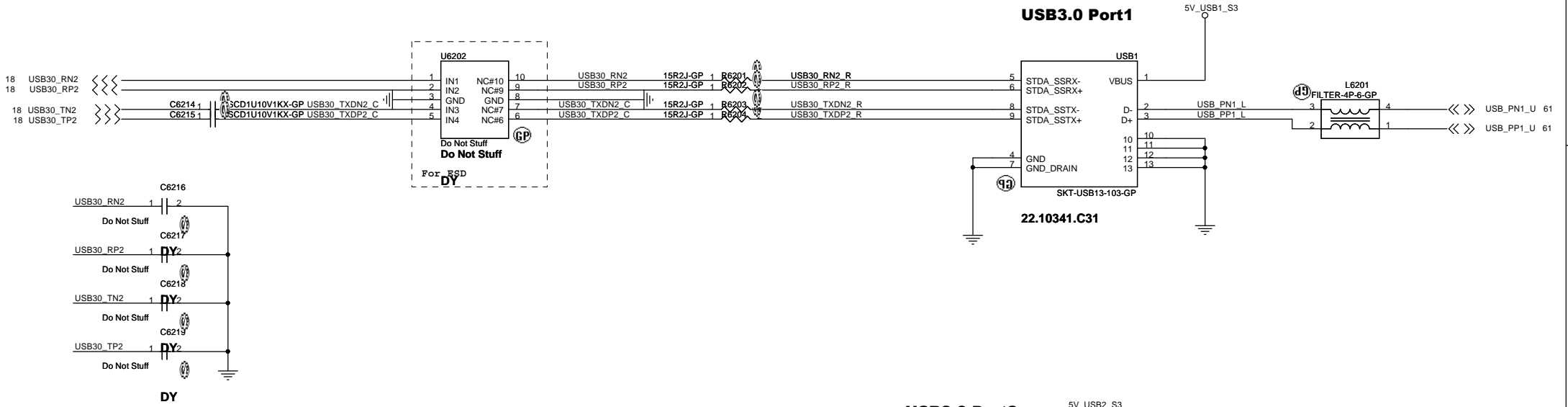
STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size: Custom
Document Number: **Storm**
Date: Monday, June 25, 2012

Rev: **-1**
Sheet 61 of 102



JE40 modify

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

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STORM

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Title: **USB 3.0 Port**

Size A3 Document Number **Storm** Rev **-1**

Date: Tuesday, June 26, 2012 Sheet 62 of 102

5 4 3 2 1

SSID = User.Interface
Bluetooth Module conn.

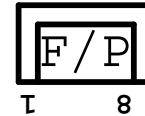
Without BT

STORM

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Bluetooth		
Size A4	Document Number Storm	Rev -1
Date: Monday, June 25, 2012	Sheet 63 of	102

Finger printer

JE40 delete FP function



STORM

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
A4

Document Number

Storm

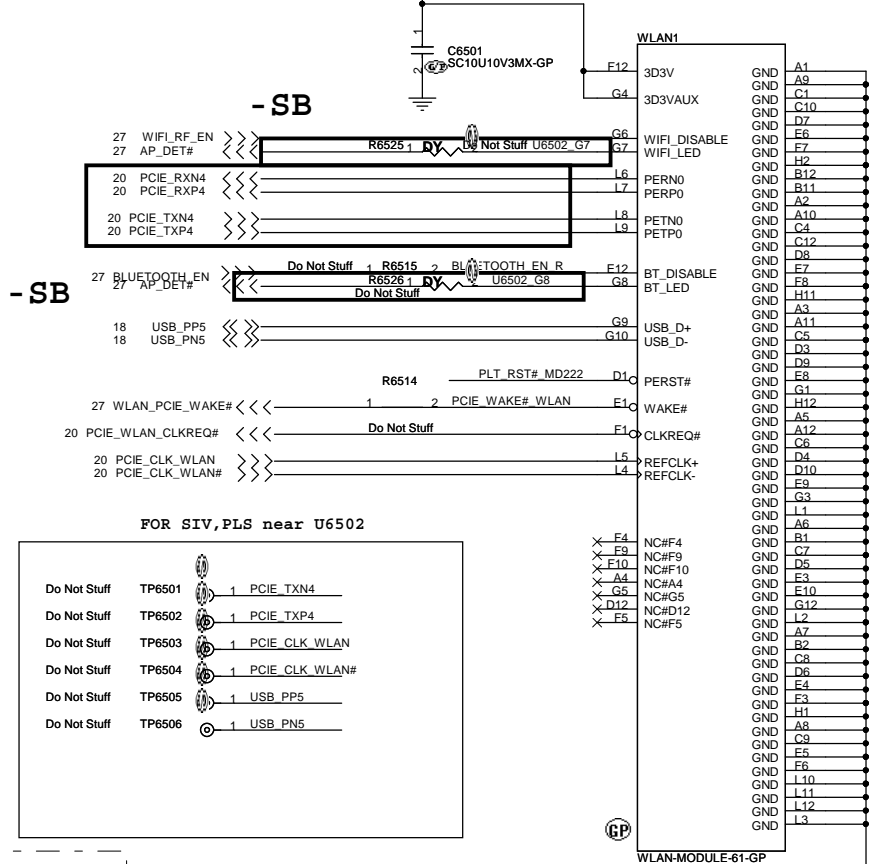
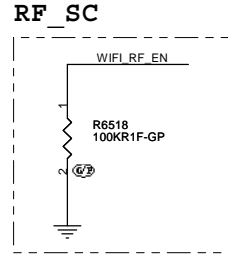
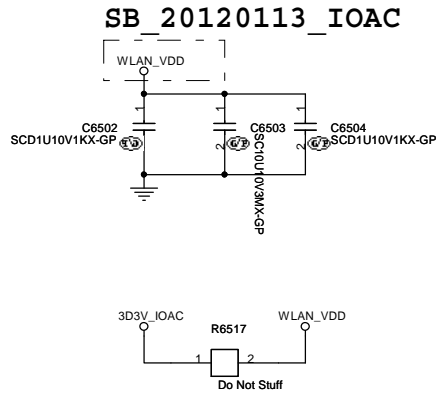
Rev
-1

Date: Monday, June 25, 2012

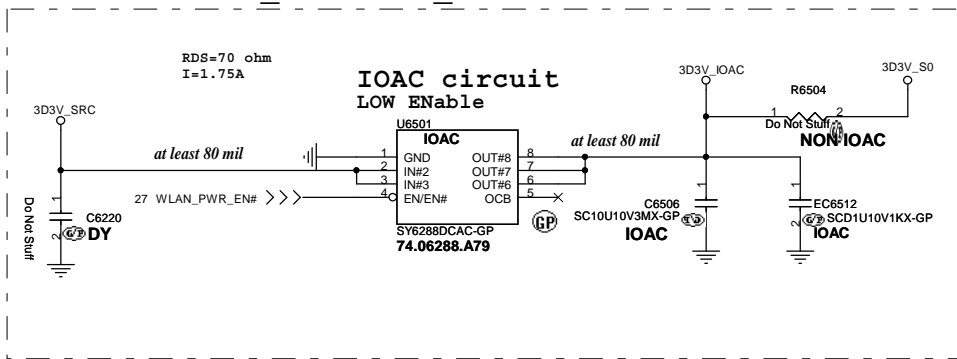
Sheet 64 of 102

SSID = Wireless Mini Card Connector(802.11a/b/g/n)

SB_20120113_IOAC



SB_20120129_IOAC



-SC



STORM

緯創資通 Wistron Corporation
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Title
MINICARD(WLAN)/TP CONN

Size A3	Document Number	Rev -1
Date: Monday, June 25, 2012	Storm	Sheet 65 of 102

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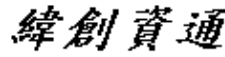
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STORM

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WWAN Connector(mSATA)		
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Size	Document Number	Rev
A4	Storm	-1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

M-SATA

Size
A4

Document Number

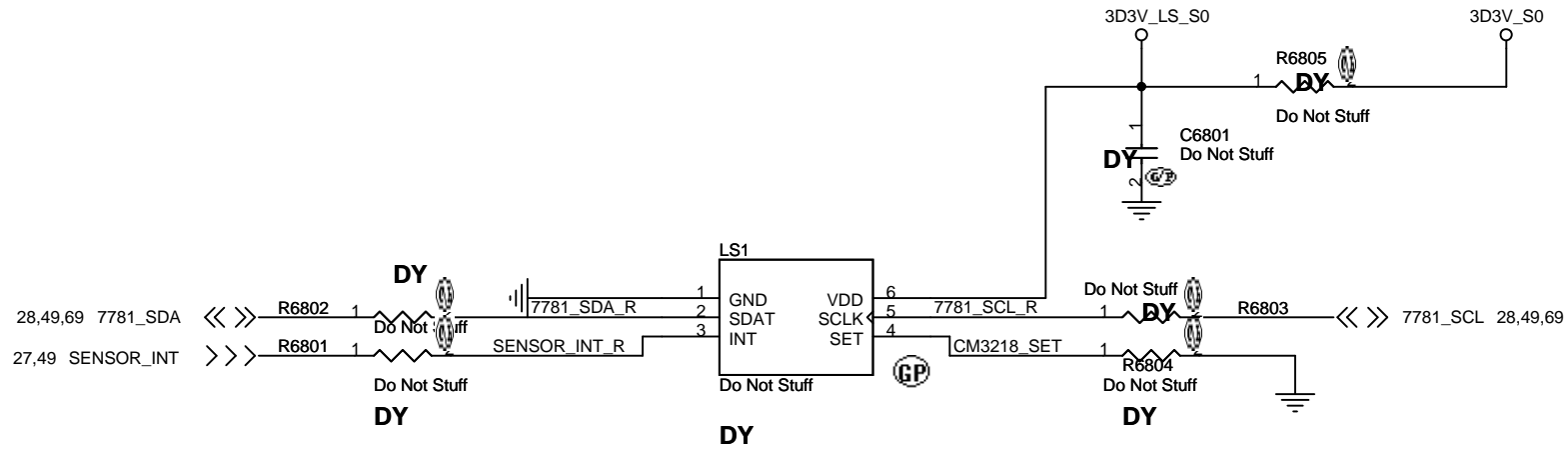
Storm

Rev
-1

Date: Monday, June 25, 2012

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SSID = User.Interface



STORM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <h3 style="margin: 0;">Light SENSOR</h3>			
Size A4	Document Number Storm		Rev -1
Date: Monday, June 25, 2012	Sheet 68	of 102	

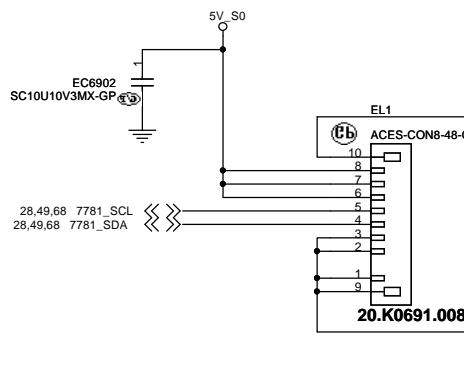
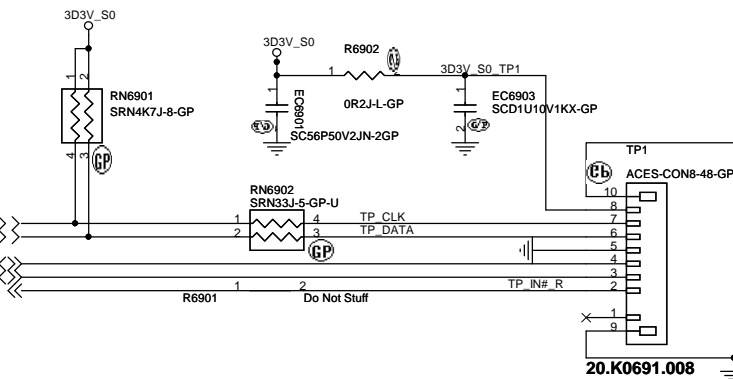
SSID = KBC

Pin number	Pin Define
1	VDDK(3.3V)
2	PCCLK
3	PCDt
4	DGND
5	NC*(SDA)
6	NC*(SCL)
7	NC*(INT)
8	NC

TOUCH PAD

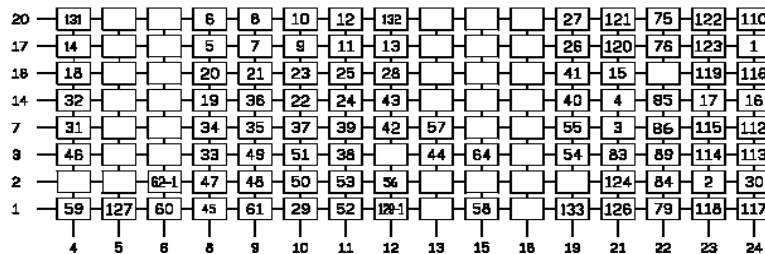
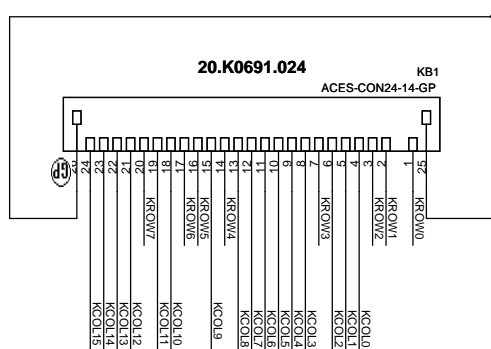
Note: Reserve for SMBus

27 TPCLK
27 TPDATA
20 PCH_SMBDATA
20 PCH_SMBCLK
18 TP_IN#



Internal Keyboard Connector

0.5 pitch



<<< KROW[0..7] 27
>>> KCOL[0..15] 27

R01 R02 R03 R04 R05 R06 R07 R08 R09 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26
 VIEW FROM TOP SIDE
 PIN NUMBER

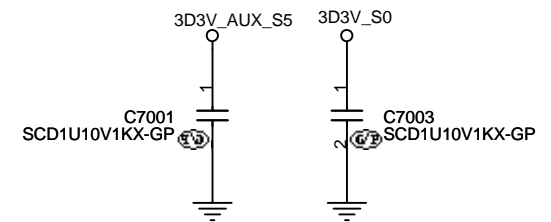
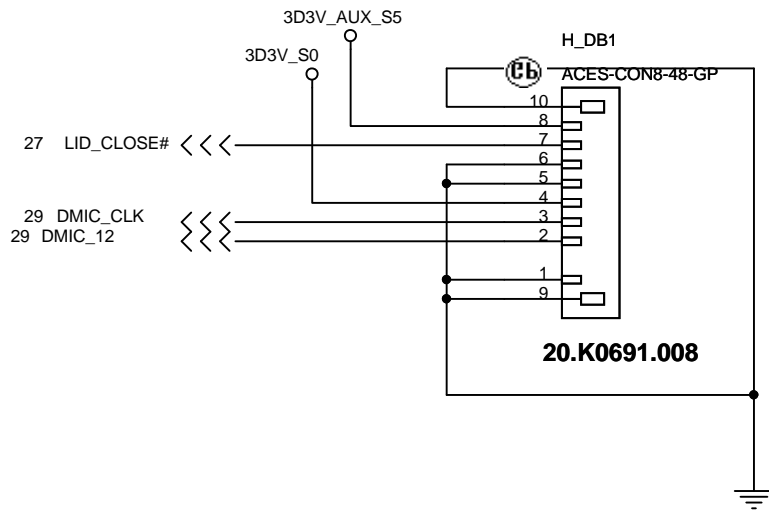
STORM

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size A3 Document Number: **Storm** Rev: **-1**

Date: Wednesday, June 27, 2012 Sheet 69 of 102

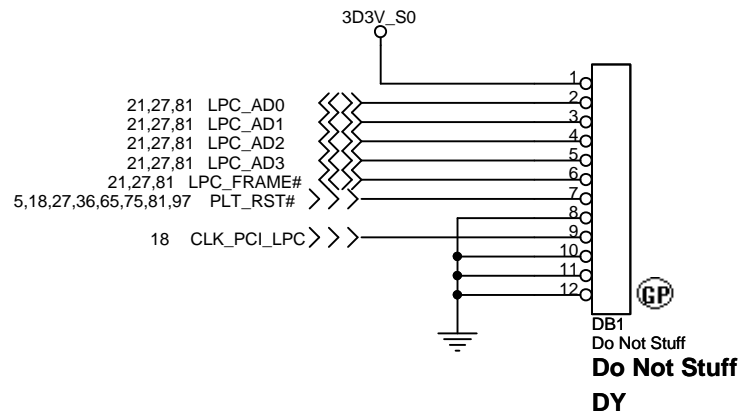


STORM

緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

Title **Hall Sensor/DMIC CONN**

Size A4 Document Number **Storm** Rev **-1**



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size
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Document Number

Storm

Rev

-1

Date: Monday, June 25, 2012

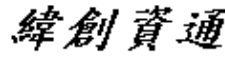
Sheet 71 of 102

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STORM

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Size	Document Number	Rev
A4	Storm	-1

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STORM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
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Document Number

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-1

Date: Monday, June 25, 2012

Sheet 73 of 102

Micro SD Card Reader

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STORM

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Title

Micro SD Card Reader

Size
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Date: Monday, June 25, 2012

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緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (1/4)

Size
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Date: Monday, June 25, 2012

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (2/4)

Size
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Document Number

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Rev

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Date: Monday, June 25, 2012

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緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (3/4)

Size
A4

Document Number

Storm

Rev

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Date: Monday, June 25, 2012

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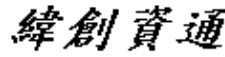
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STORM

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Thunderbolt (4/5)		
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Size A4	Document Number Storm	Rev -1
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STORM

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **Thunderbolt(5/5)**

Size A4	Document Number Storm	Rev -1
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Date: Monday, June 25, 2012 Sheet 79 of 102

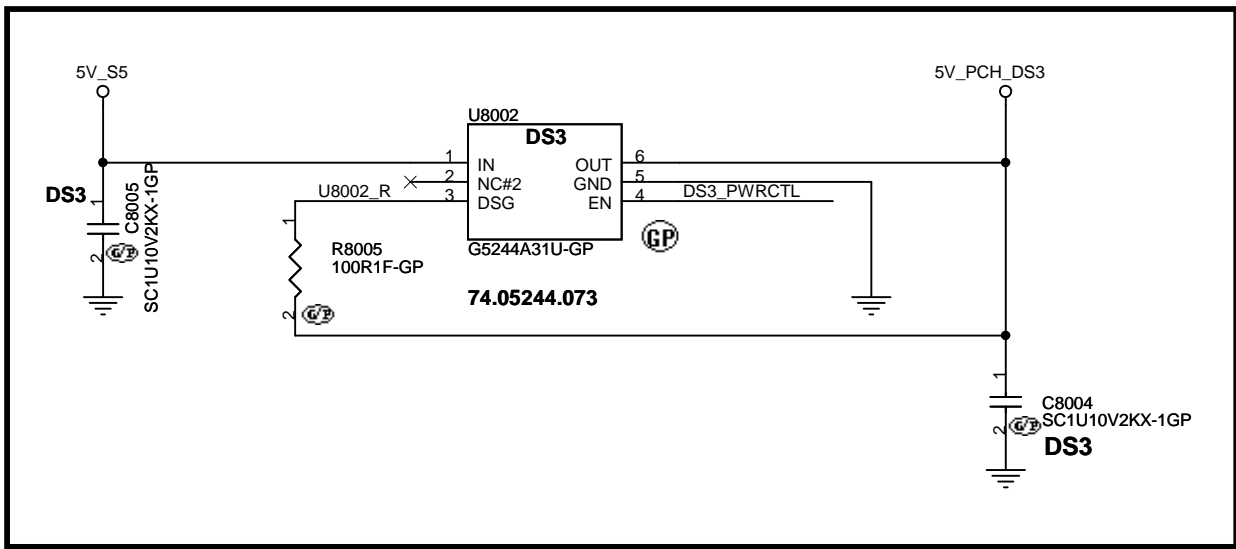
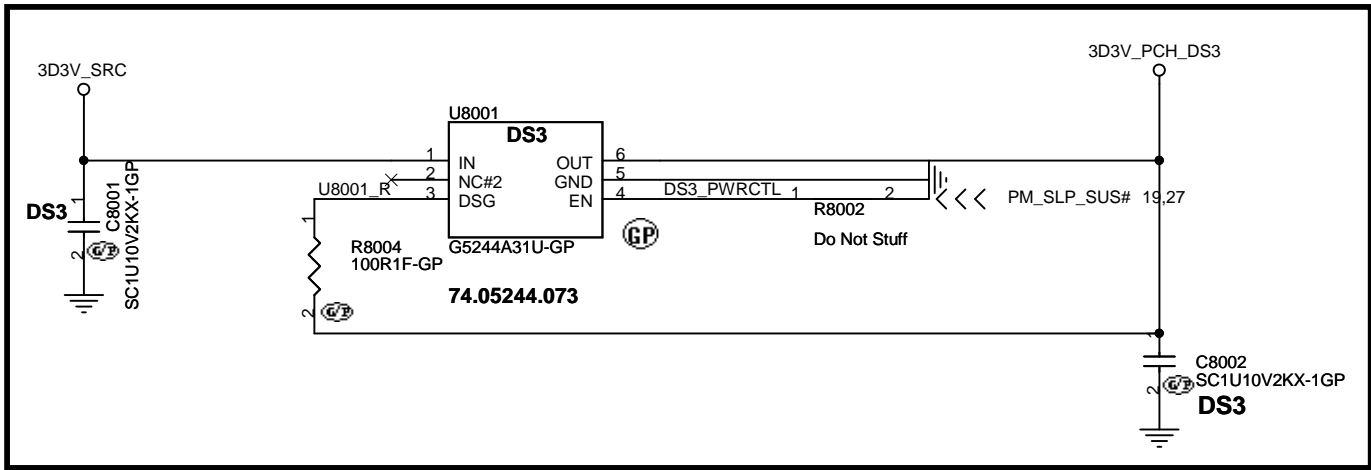
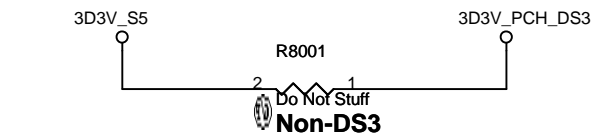
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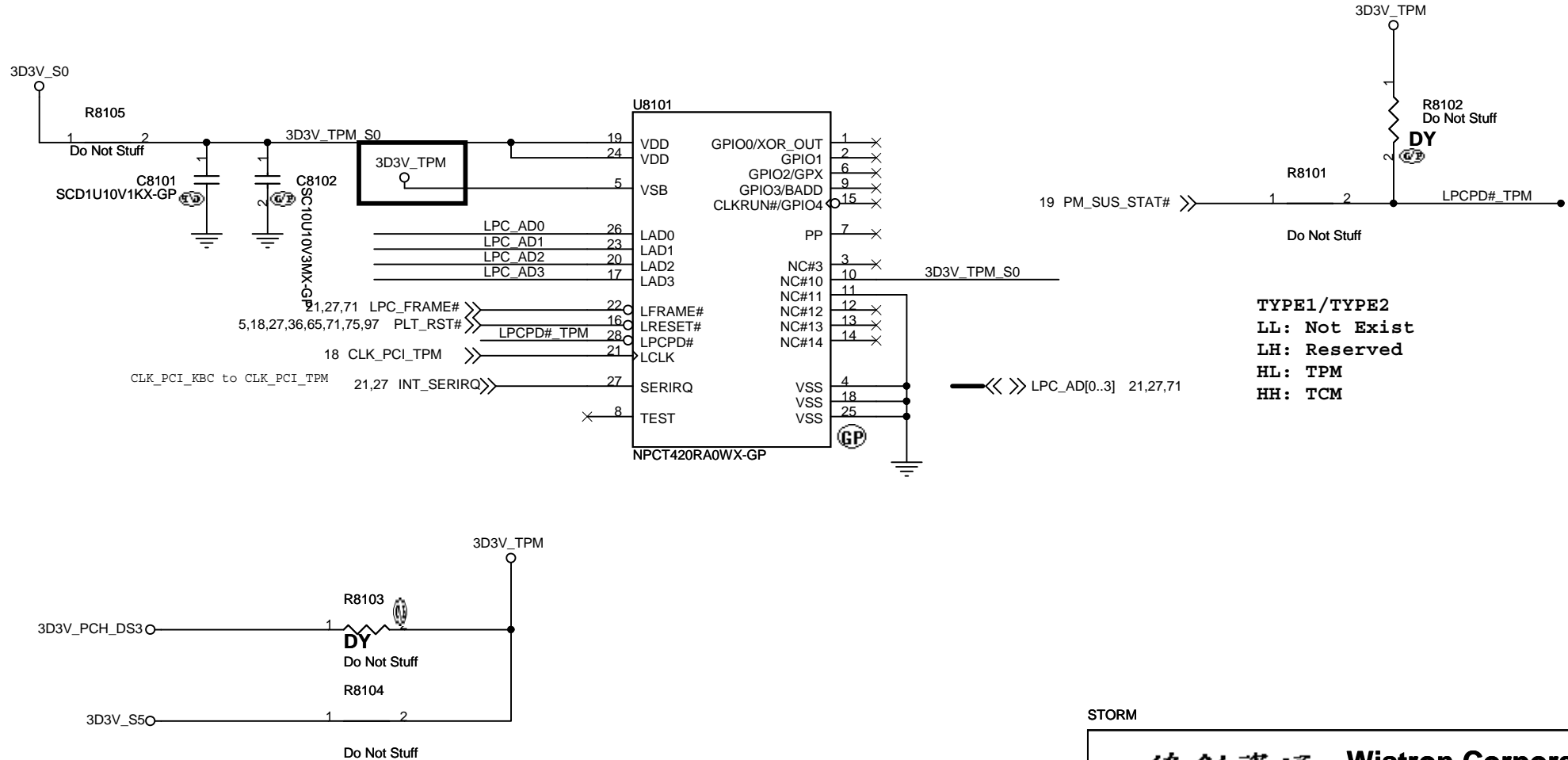
STORM

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **Deep Standby**

Size A4 Document Number **Storm** Rev **-1**

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STORM

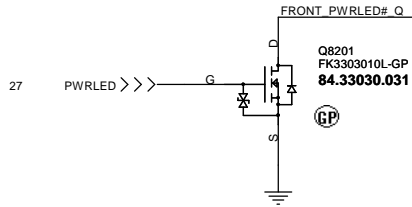
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

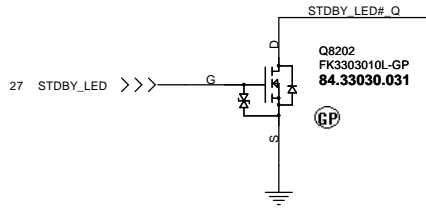
Size A4 Document Number **Storm** Rev **-1**

Date: Thursday, June 28, 2012 Sheet 81 of 102

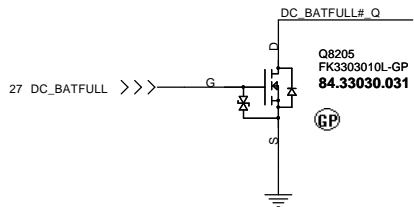
Power button LED



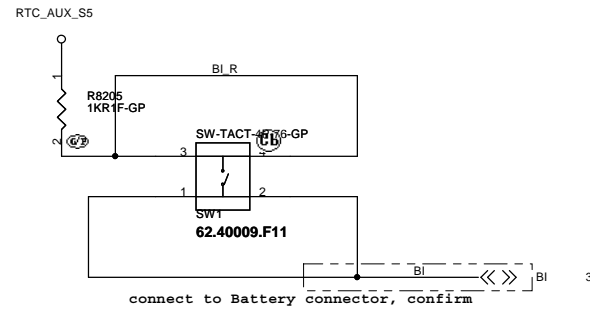
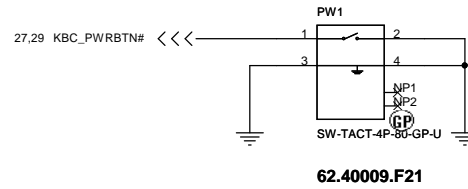
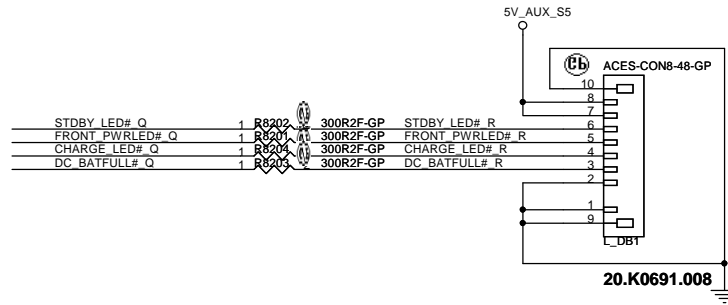
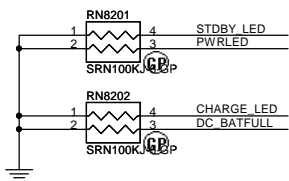
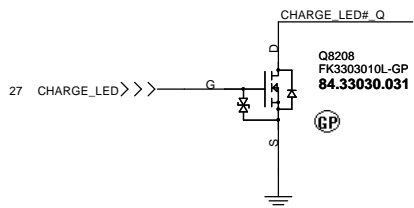
Power STDBY_LED



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)



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STORM

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

SYW231 1D8V(2)

Size
A4

Document Number

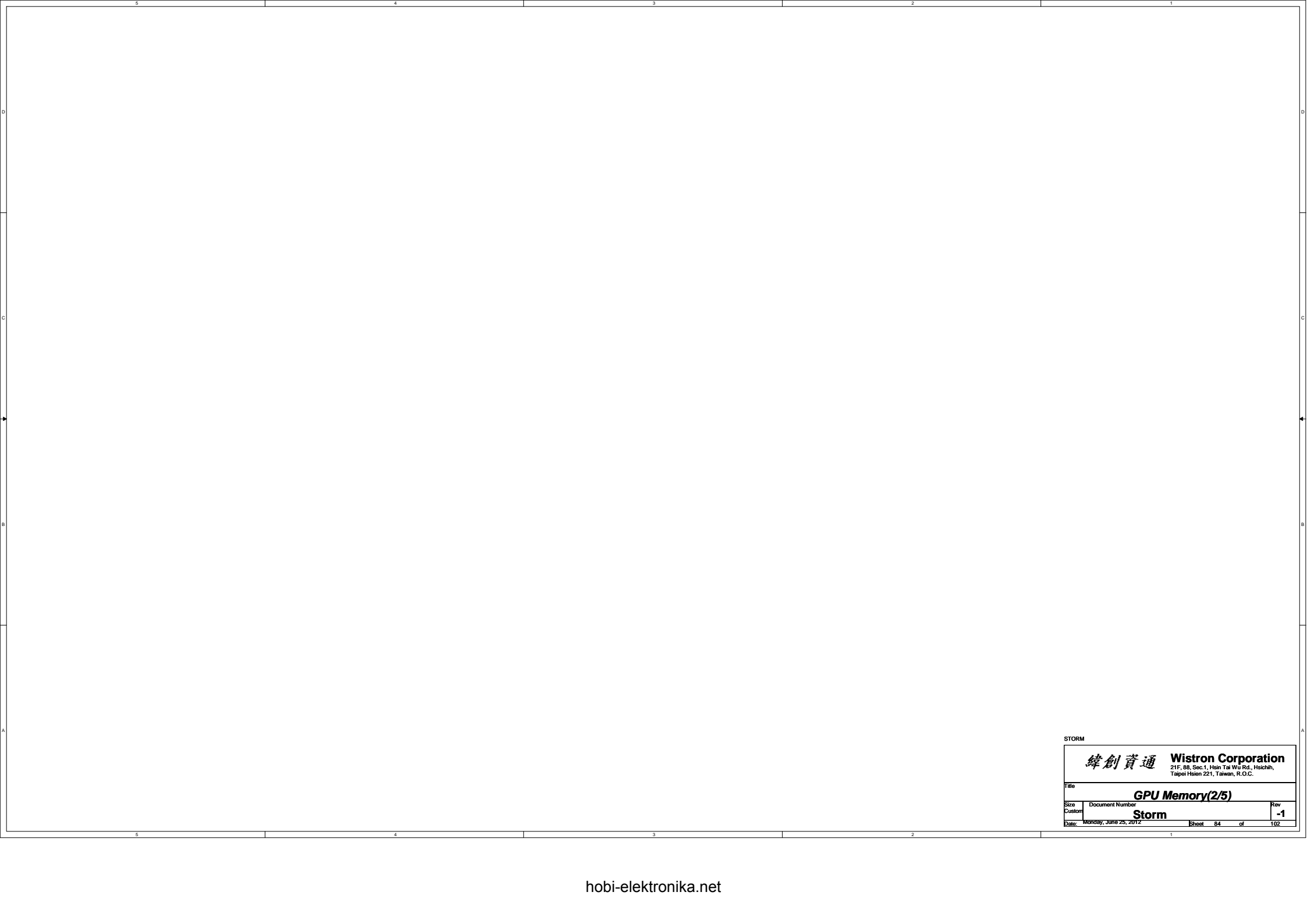
Storm

Rev

-1

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緯創資通 **Wistron Corporation**
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Title			GPU Memory(2/5)		
Size	Document Number				Rev
Custom	Storm				-1
Date:	Monday, June 25, 2012	Sheet	84	of	102

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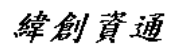
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STORM

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Title	
GPU DPPWR/GND(5/5)	
Size	Document Number
A3	Storm
Date: Monday, June 25, 2012	Rev
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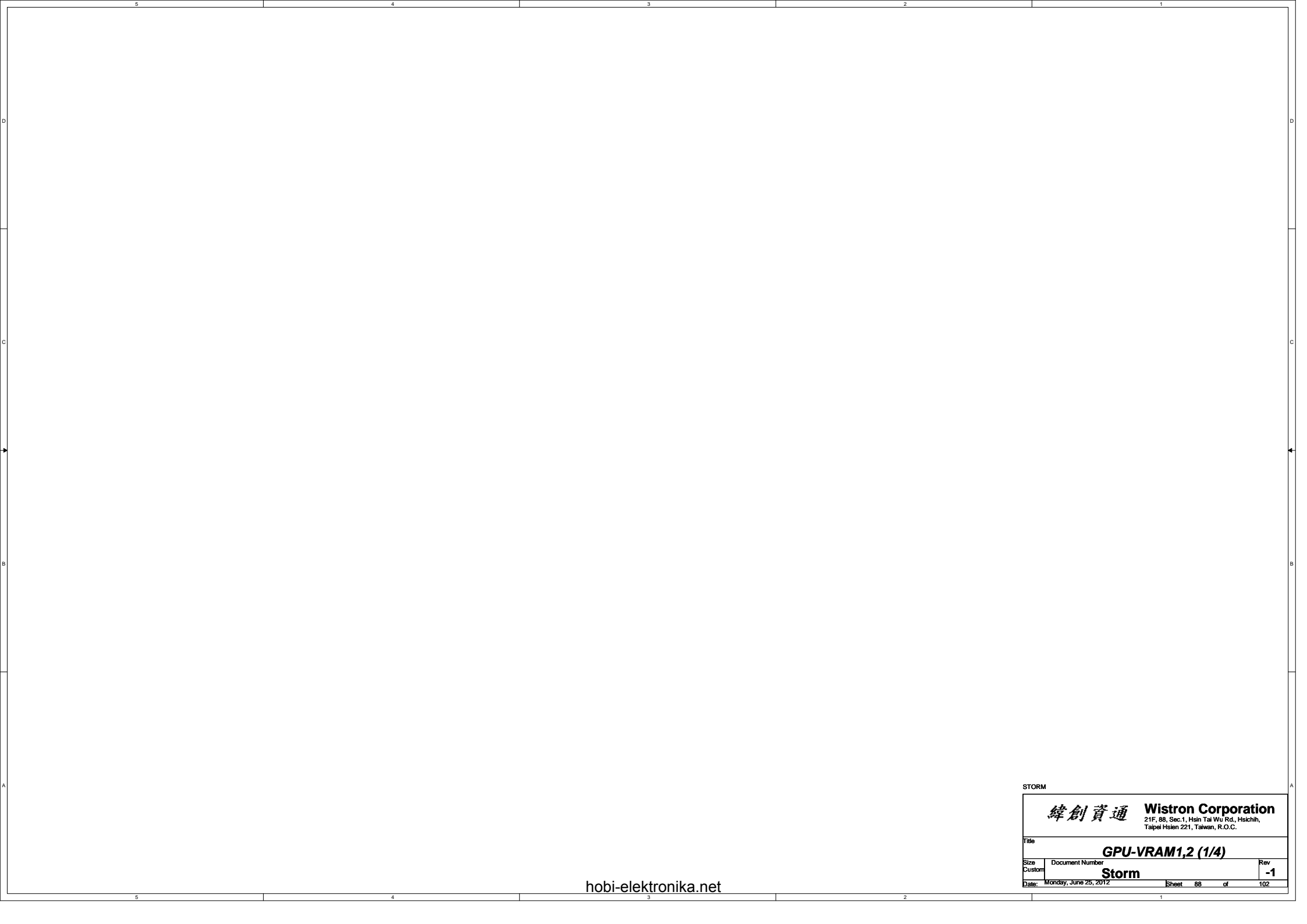
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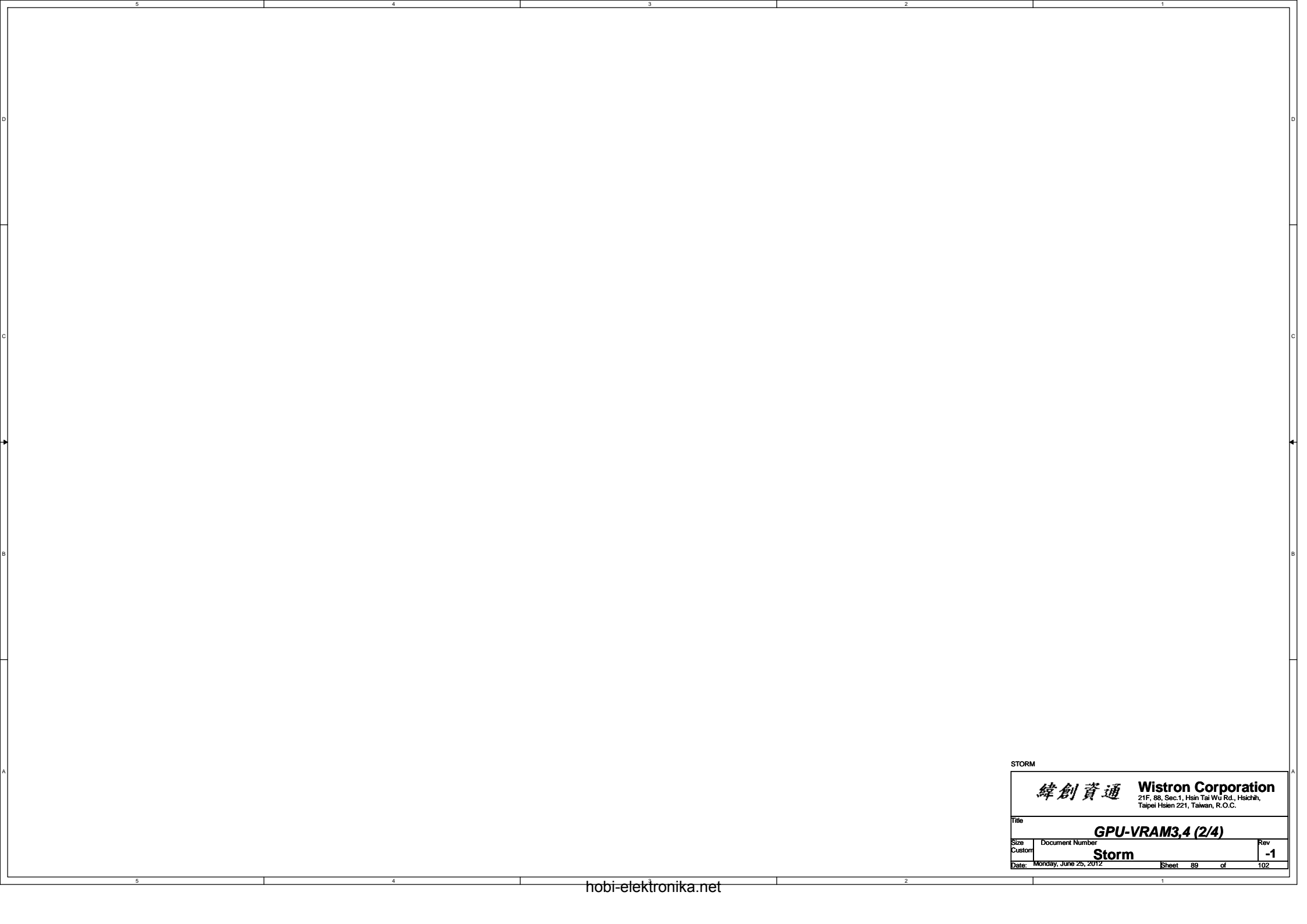
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STORM			
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipai Hsien 221, Taiwan, R.O.C.			
Title			
GPU-VRAM1,2 (1/4)			
Size	Document Number	Rev	
Custom	Storm	-1	
Date:	Monday, June 25, 2012	Sheet 88	of 102



STORM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM3,4 (2/4)			
Size	Document Number	Rev	
Custom	Storm	-1	
Date:	Monday, June 25, 2012	Sheet 89	of 102

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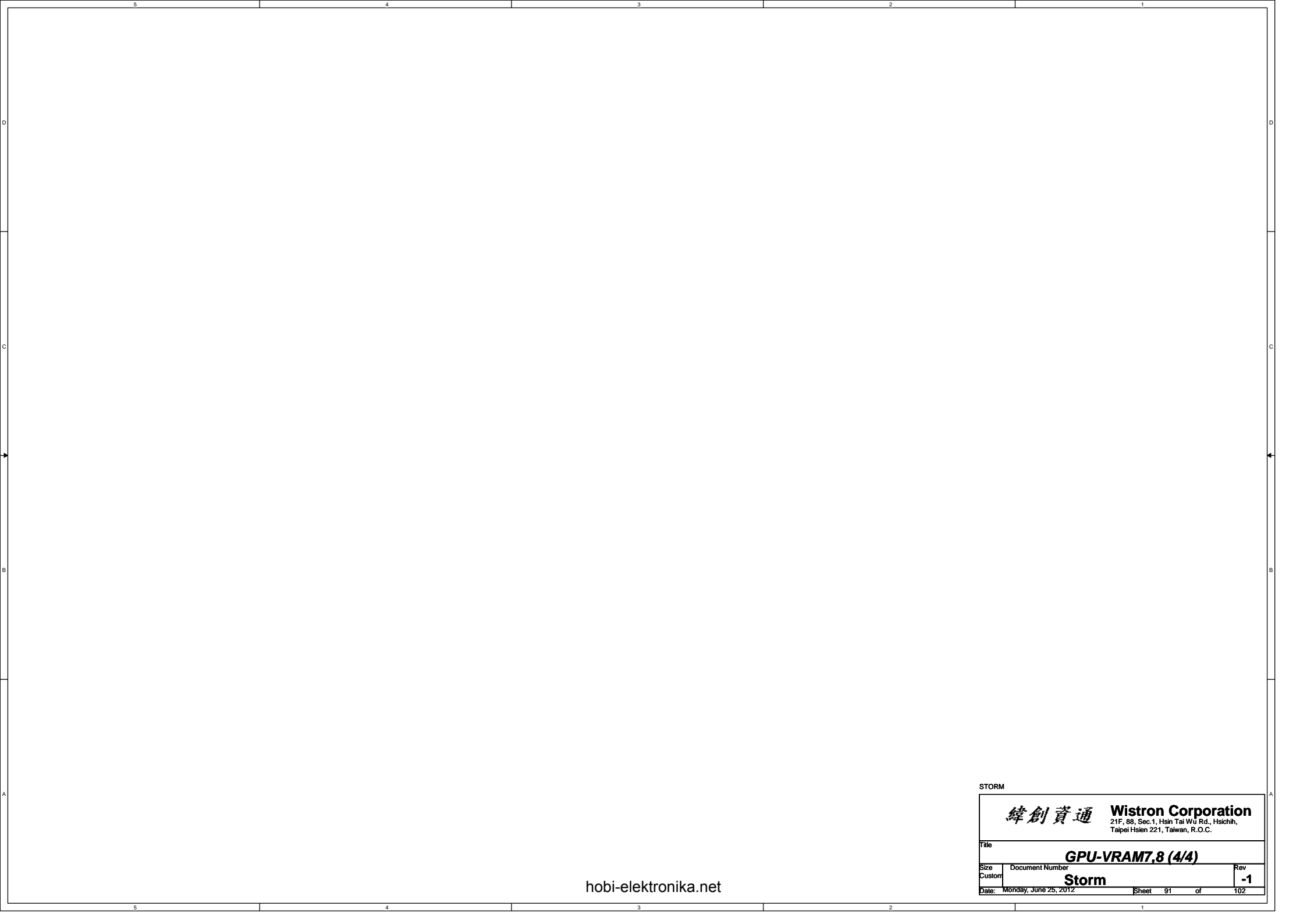
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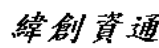
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GPU-VRAM5,6 (3/4)			
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		-1
GPU-VRAM7,8 (4/4)		Title
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Title		
RT8208B +VGA CORE		
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Title

DISCRETE VGA POWER

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LVDS Switch			
Size	Document Number		Rev
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Size A4 Document Number **Storm** Rev **-1**

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SSID = SDIO

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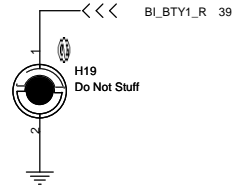
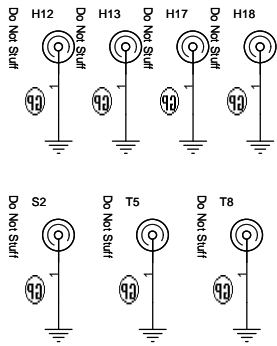
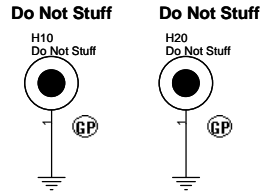
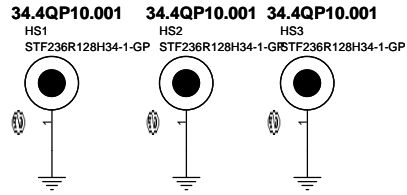
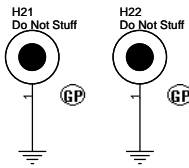
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title **TOUCH PANEL**

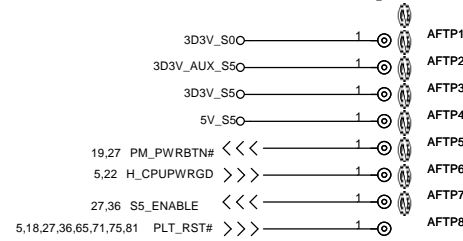
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Check test point

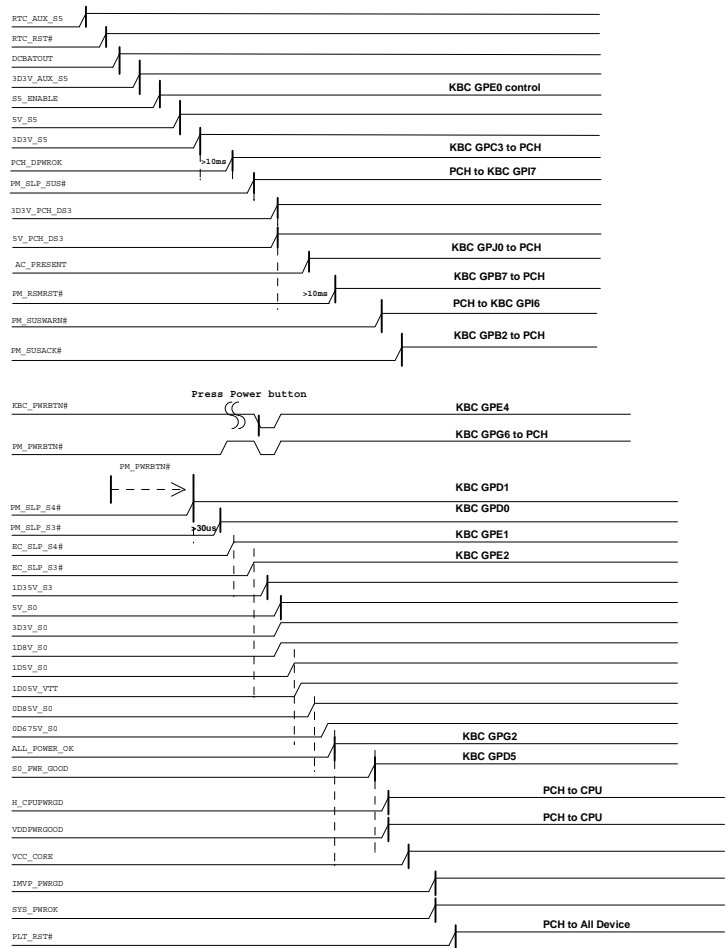


Test Point放在Dimm
Door打開可量測處

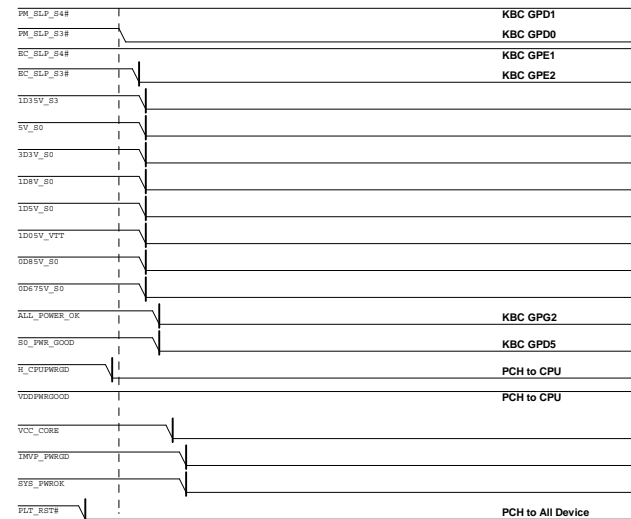
STORM

		Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>
UNUSED PARTS/EMI Capacitors		
Title Size A3	Document Number Storm	Rev -1
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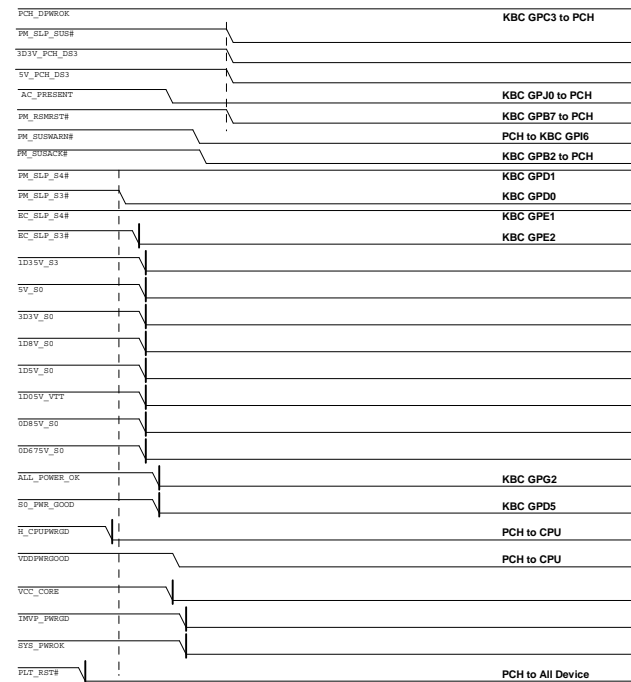
Intel Power Up Sequence



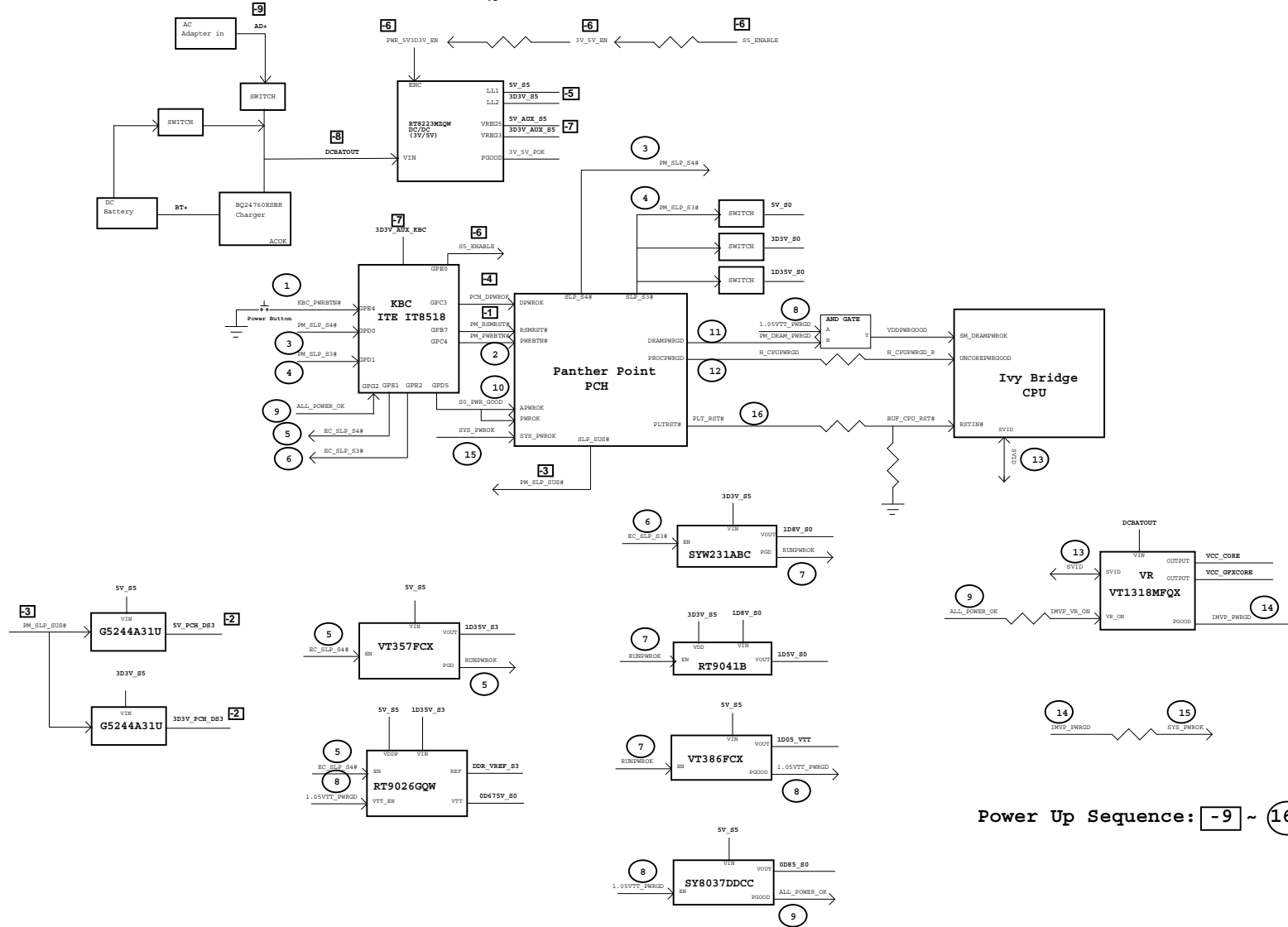
Intel S3 Sequence



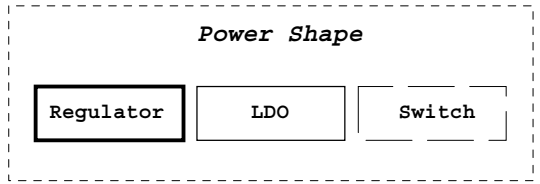
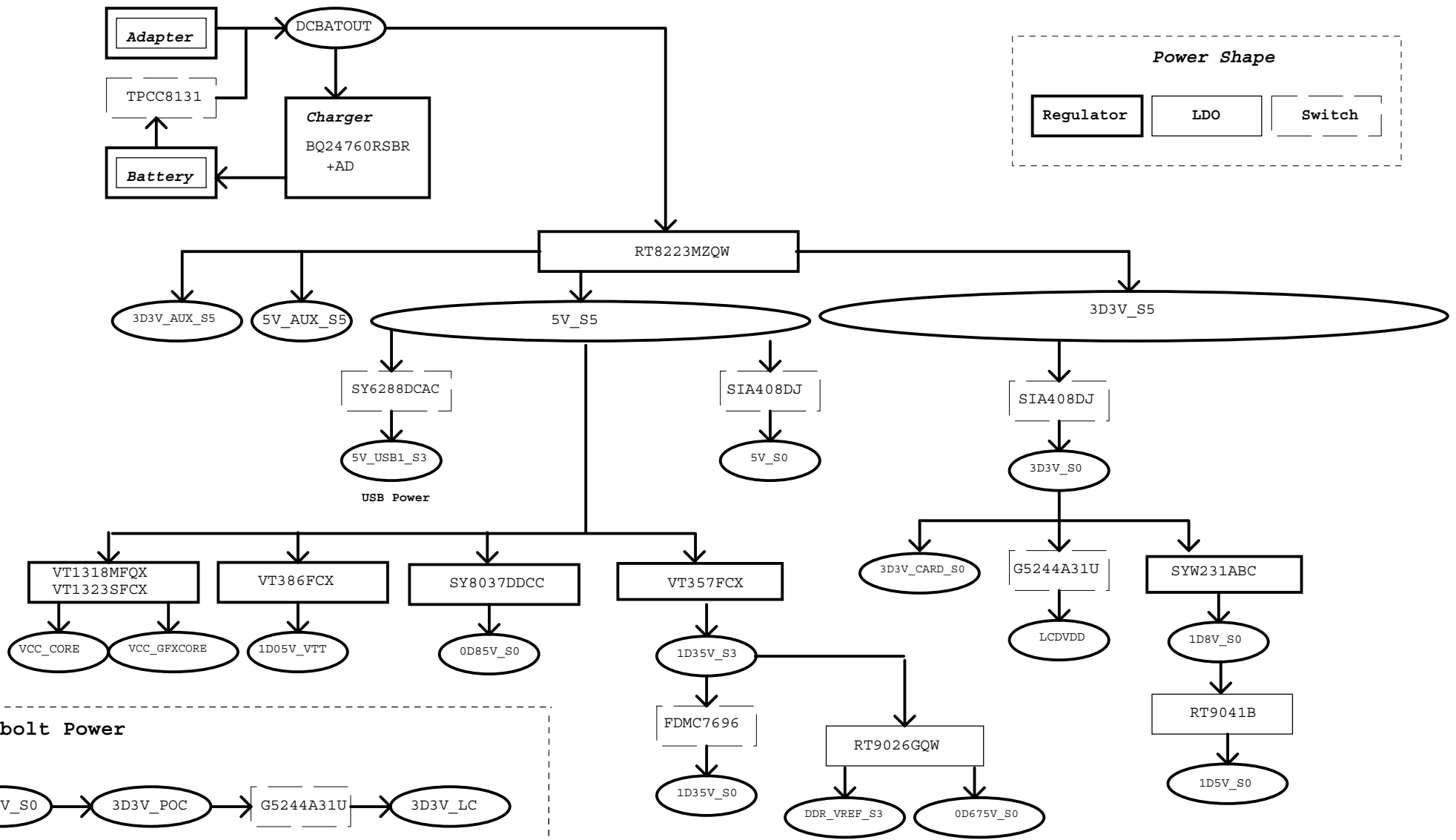
Intel Deep S3 Sequence



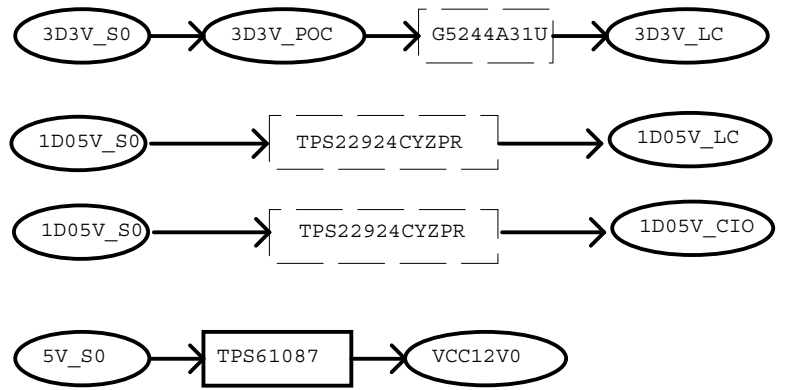
WISTRON CHIEF RIVER POWER UP SEQUENCE DIAGRAM



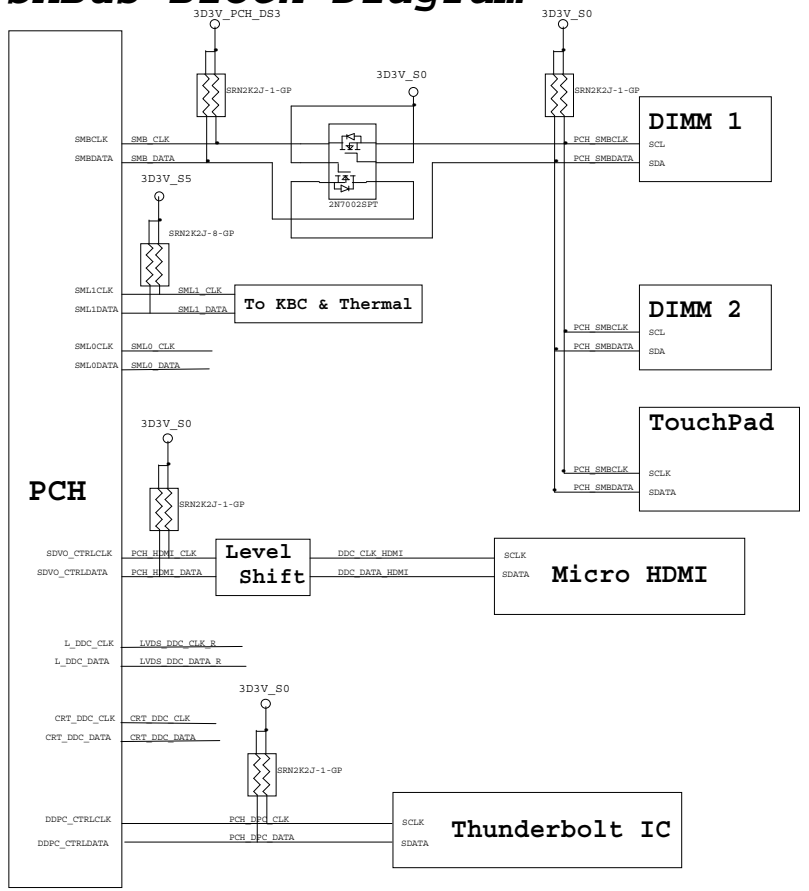
Power Up Sequence: [9] ~ (16)



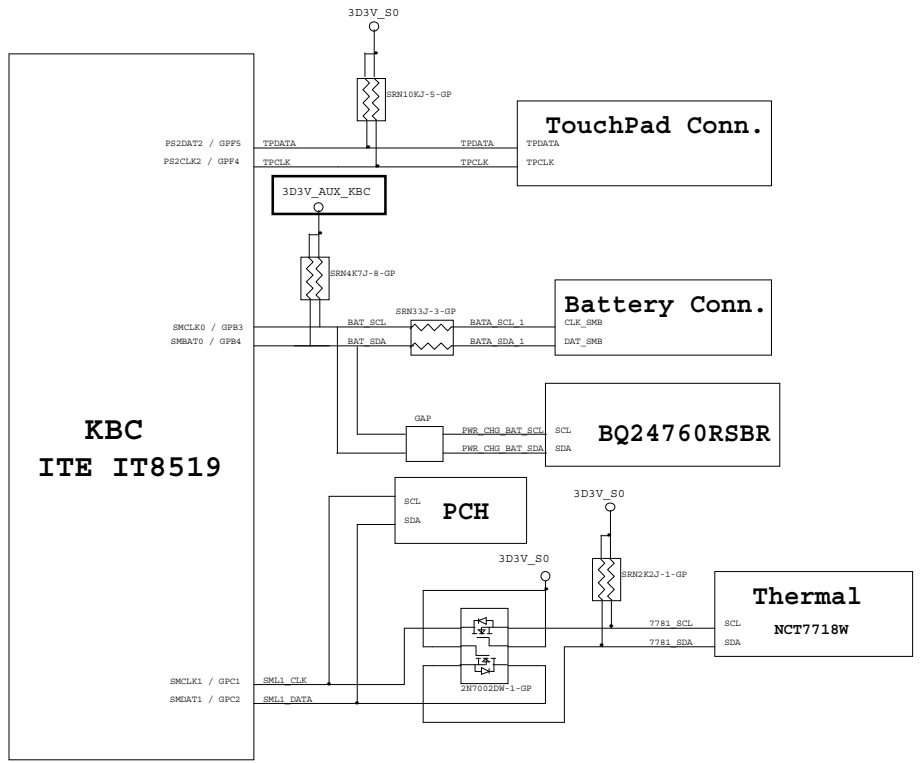
Thunderbolt Power



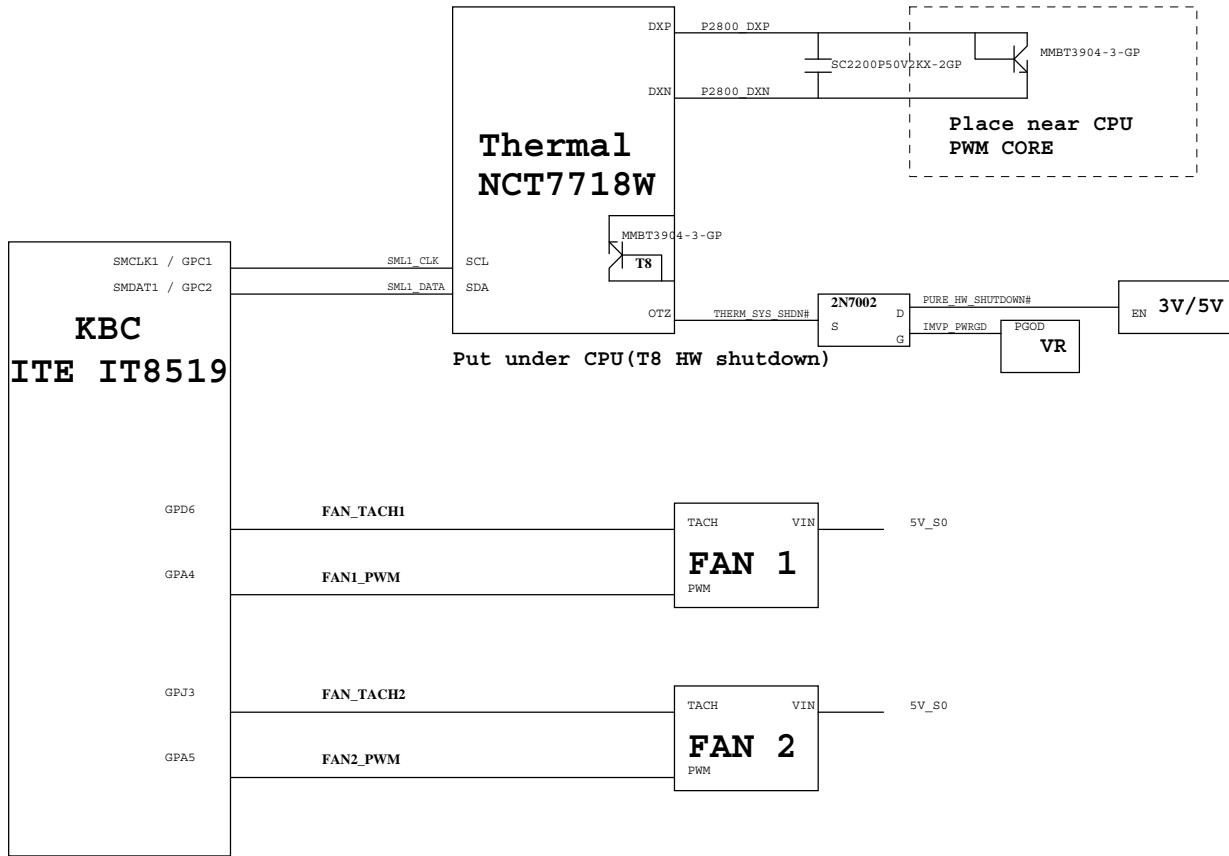
PCH SMBus Block Diagram



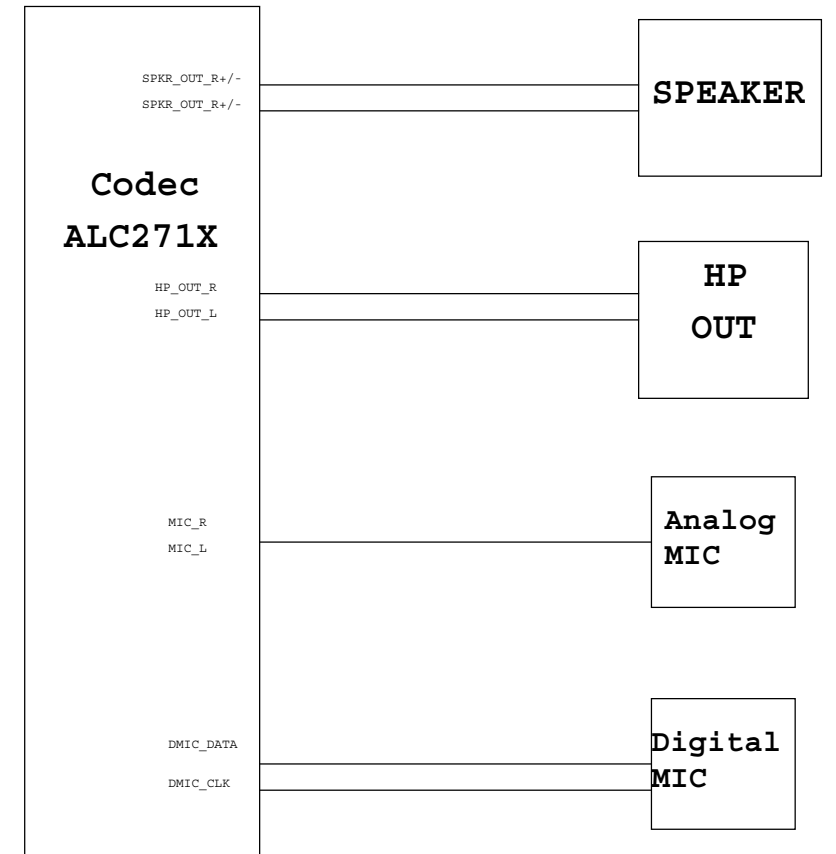
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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Thermal/Audio Block Diagram			
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