

PEGATRON CONFIDENTIAL

MODEL NAME :

PCB NO :

69- P/N :

AIC70 Schematic

Intel Arrandale rPGA-989

PCH BGA 1071

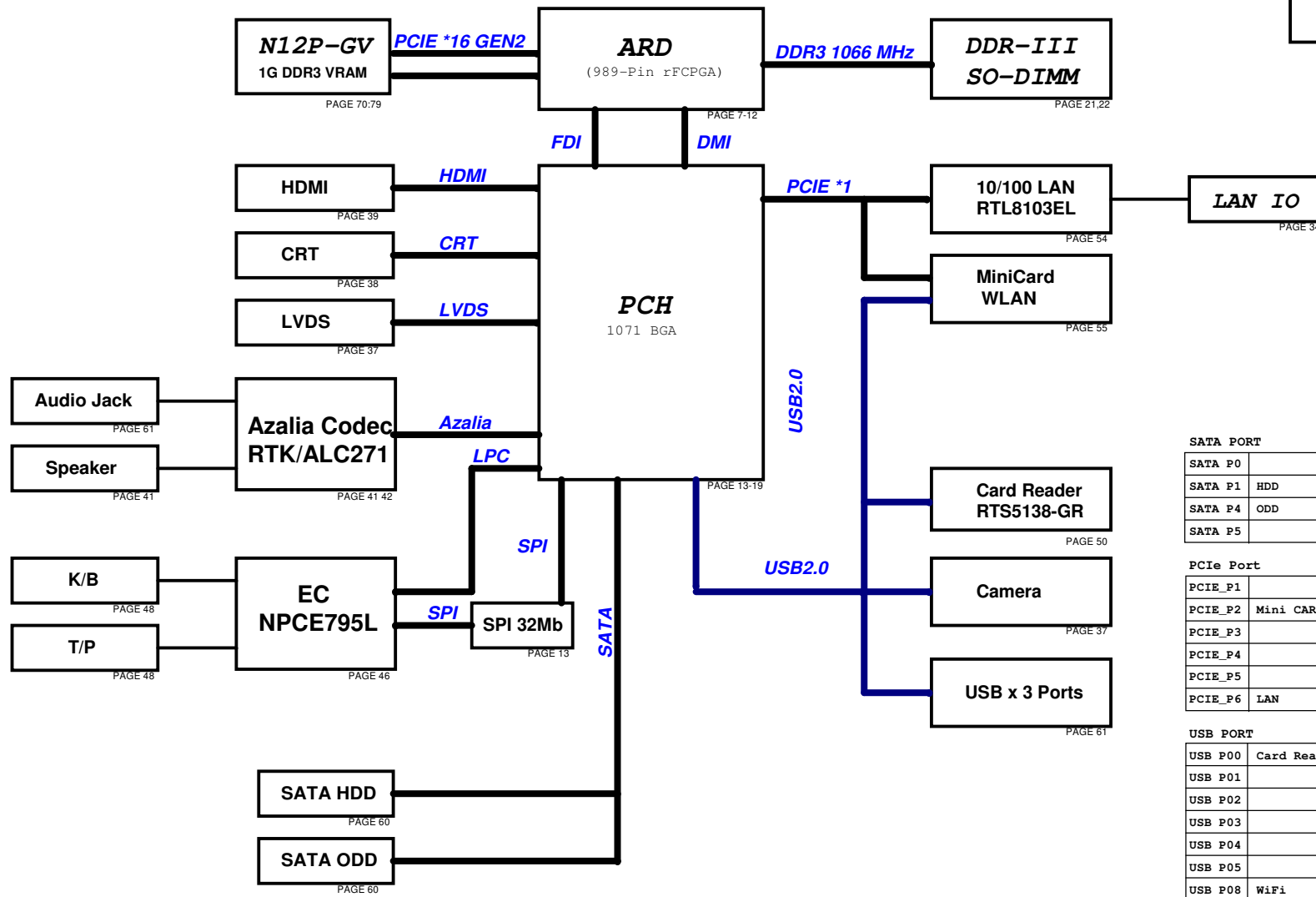
2011-05-04

REV : R2.0

PEGATRON Title : <i>Cover Page</i>		
BU1-RD Div.1-HW RD Dept.1 Engineer: <i>Johnson Huang</i>		
Size Custom	Project Name AIC70	Rev 2.0
Date: <i>Wednesday, May 04, 2011</i>		Sheet 1 of 77

AIC70 BLOCK DIAGRAM

CLOCK GEN.
SLG8SP585V
PAGE 24



POWER

CPU VCORE	PAGE 80
SYSTEM, +3V, +5V	PAGE 81
+VCCP	PAGE 82
DDR & VTT	PAGE 83
+VGFX_CORE	PAGE 86
+VGA_CORE	PAGE 87
SMART CHARGER	PAGE 88
POWER DETECT	PAGE 90
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

SATA PORT

SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	

PCIe Port

PCIe_P1	
PCIe_P2	Mini CARD (WLAN)
PCIe_P3	
PCIe_P4	
PCIe_P5	
PCIe_P6	LAN

USB PORT

USB P00	Card Reader
USB P01	
USB P02	
USB P03	
USB P04	
USB P05	
USB P08	WiFi
USB P09	
USB P10	Camera
USB P11	External
USB P12	External
USB P13	External

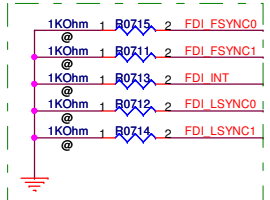
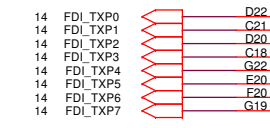
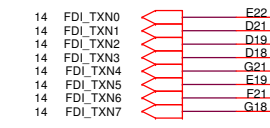
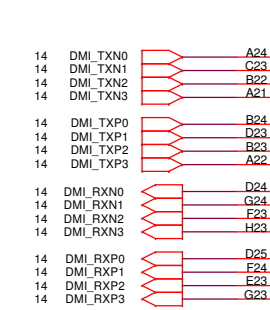
Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

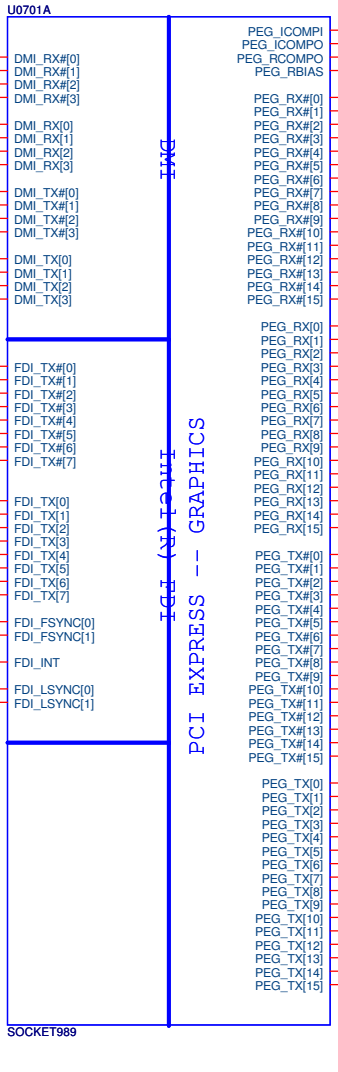
SCHEMATIC INDEX V1.2

PAGE#	Description	NOTE
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02	Block Diagram	
03	PAGE INDEX	
07-12	CPU	
13-19	PCH	
21-22	DDR3 SO-DIMM	
24	Clock Generator	
33-34	LAN	
37	LVDS CON	
38	RGB CON	
39	HDMI (Level shift for UMA)	
41-42	AUDIO CODEC & De-POP	
46-48	EC NPCE795L / KB / TP	
49	THERMAL / FAN	
50	CARD READER	
55	MINI CARD -WiFi & BT3.0	
60	SATA(HDD & ODD)	
61	USB & AUDIO CONN	
63	DC-IN / BATTERY CONN / Discharge	
65	PWR CONN & Debug CONN	
66	Led & Nut & ME Pad	
70-79	dGPU Schematics	
80-94	Power Schematics	
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96	ODD Board	
97	PWR Board	
98	TP SW Board & LID Switch	
99	AUDIO Board	

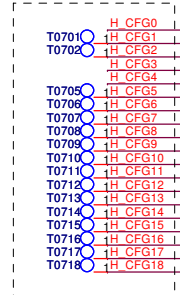
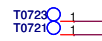
PAGE#	Description	NOTE



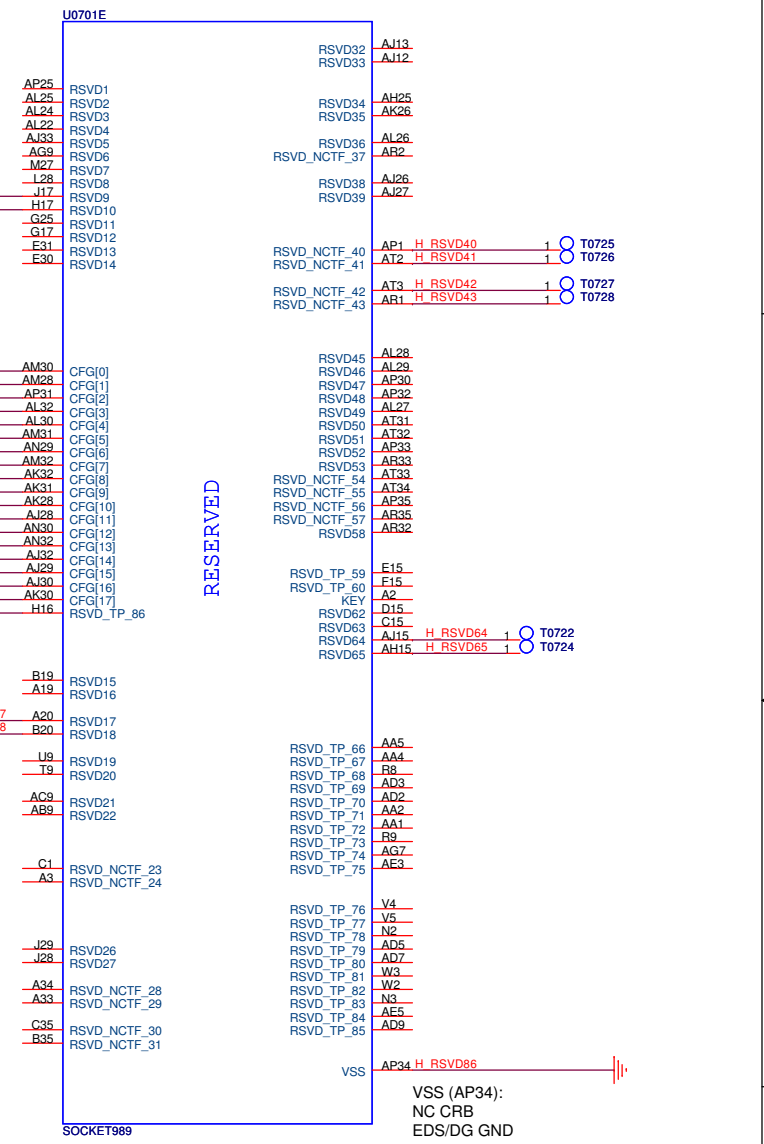
Default: DSC Only
 DSC only: Pop all resistors
 UMA only: Depop all resistors



M_VREFDQ_CHA/B for CFD only



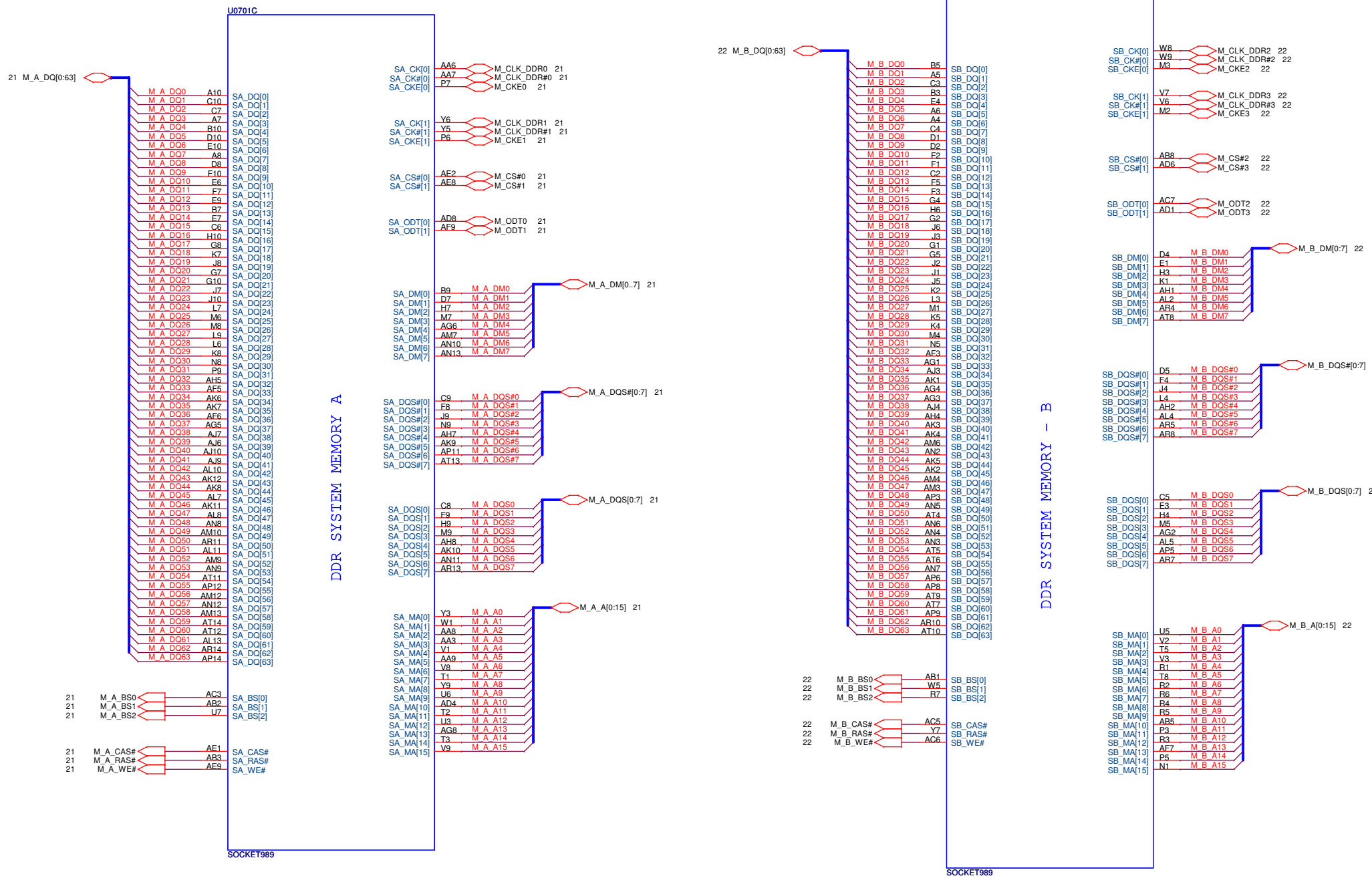
Place Near CON7501

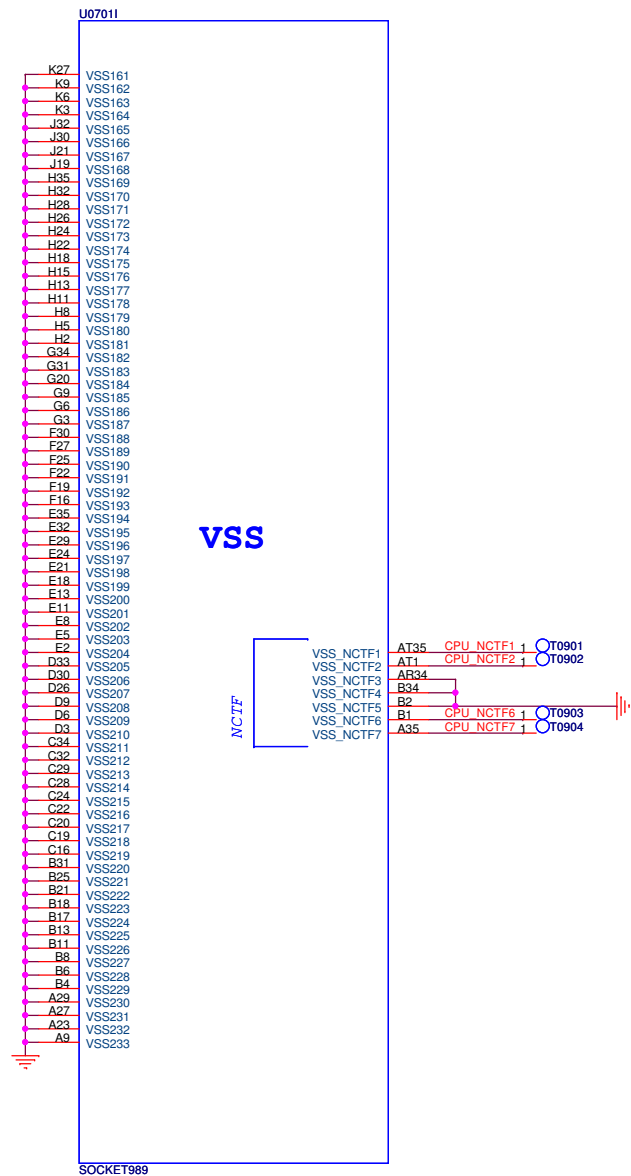
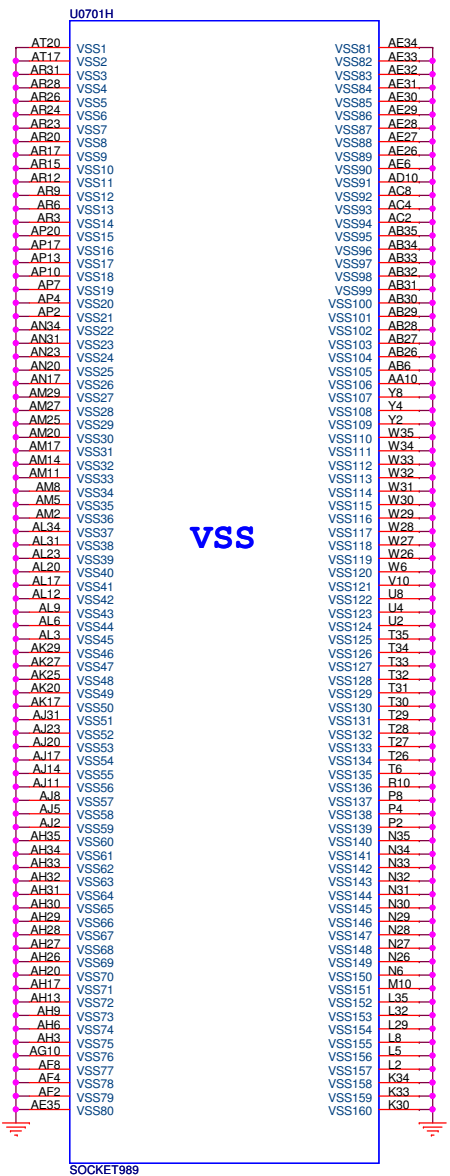


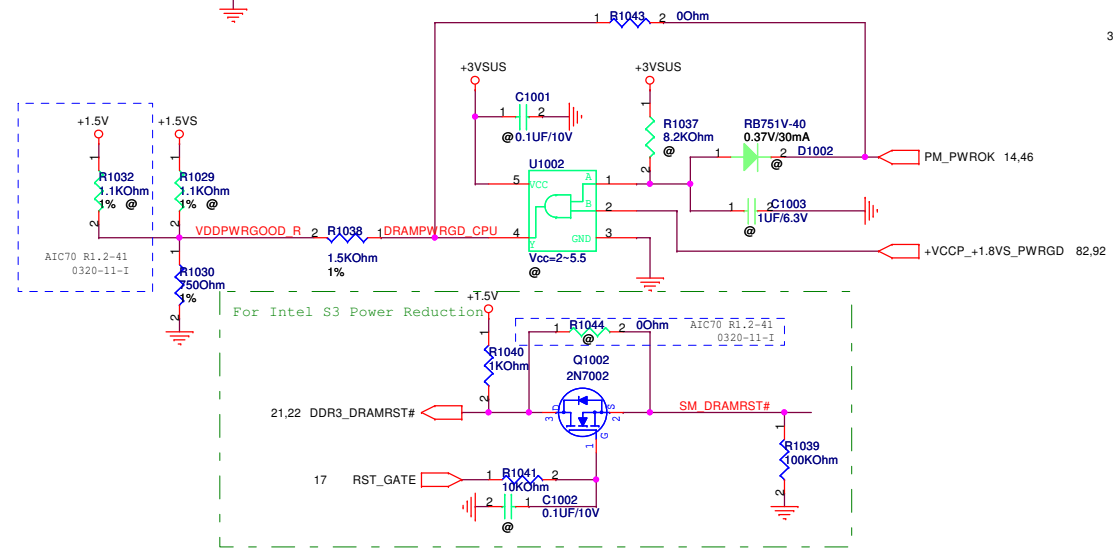
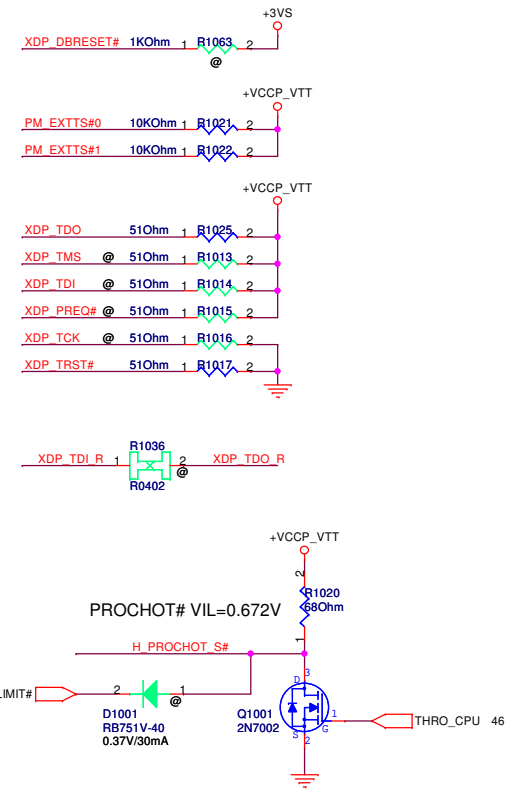
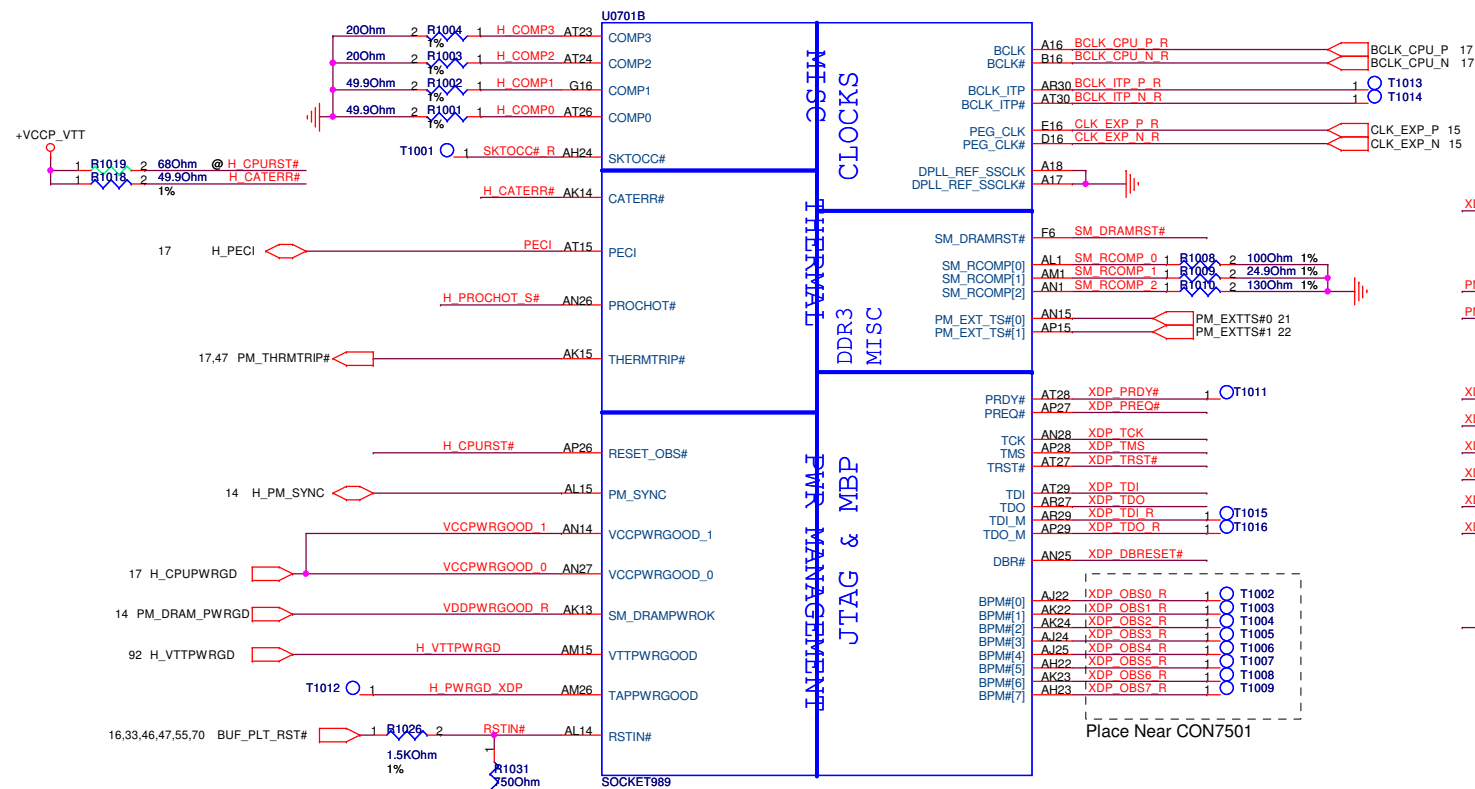
CFG0 : PCIE Config Strap
 H = Single PEG (Default)
 L = Bifurcation enabled

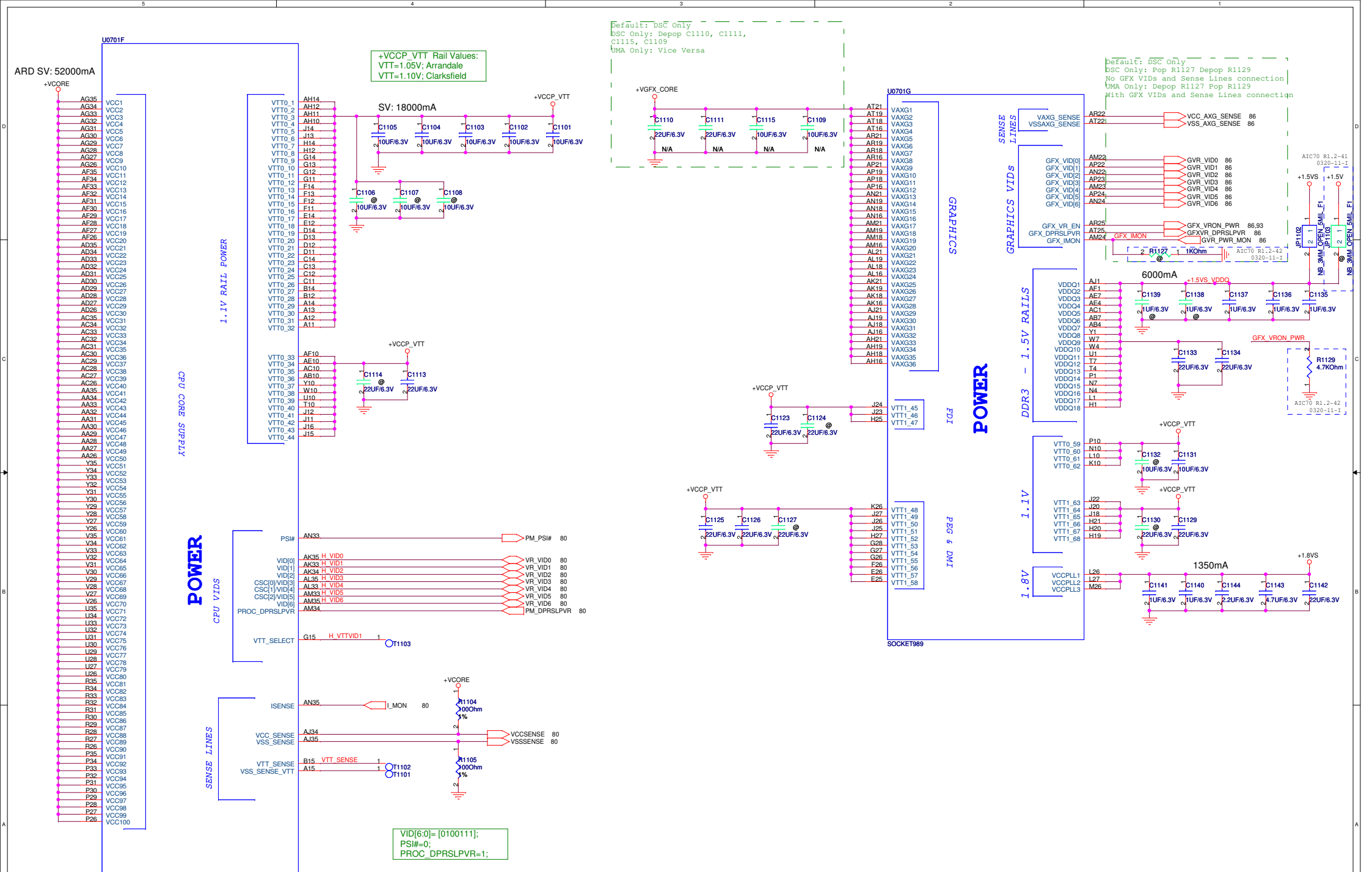
CFG3 : PCIE Lane Reversal
 H = Normal Operation (Default)
 L = Lane Numbers Reversed

CFG4 : eDP Presence
 H = Disable (Default)
 L = Enable



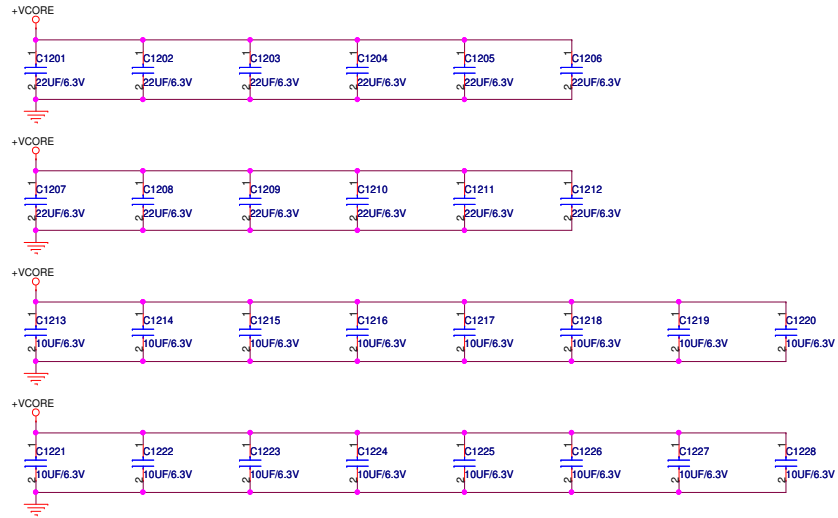


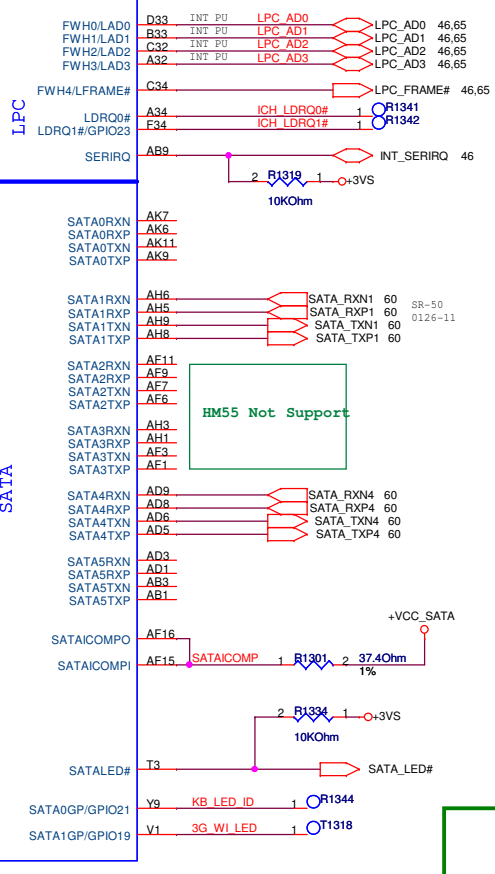
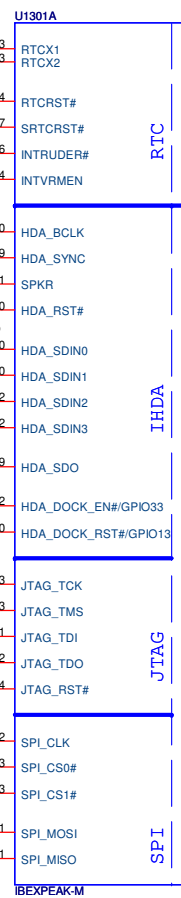
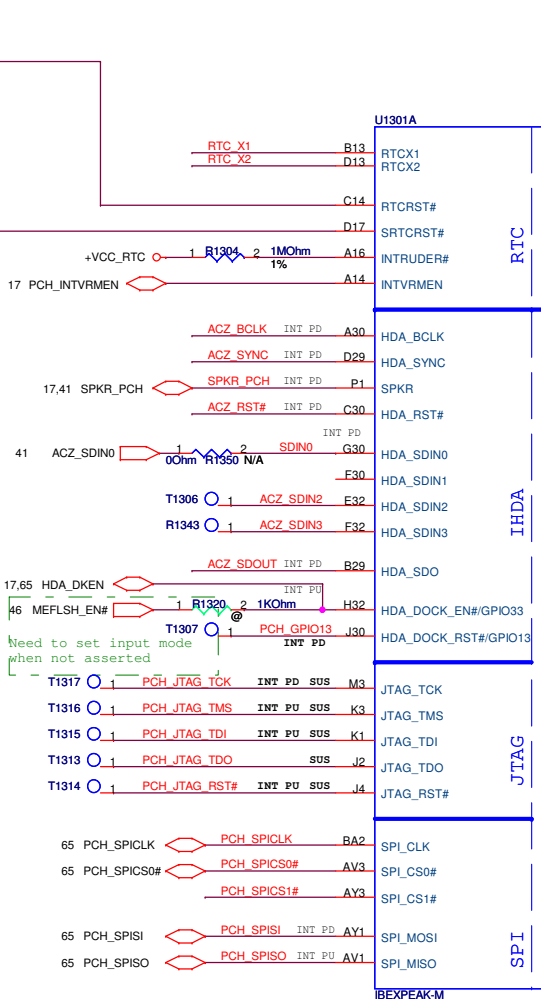
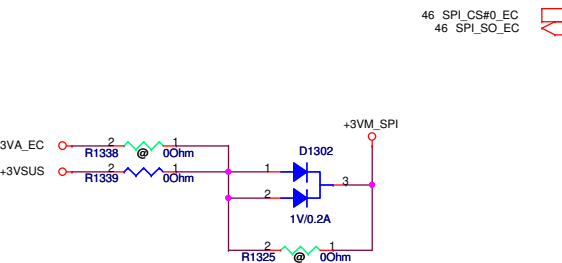
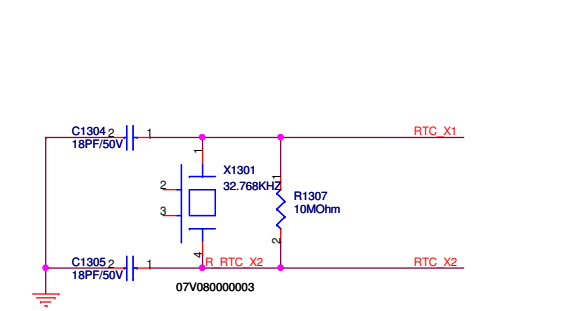
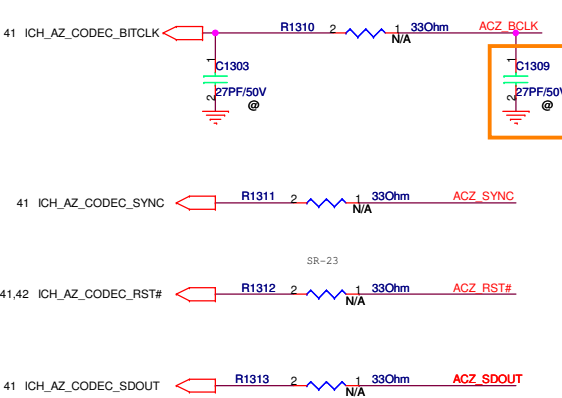
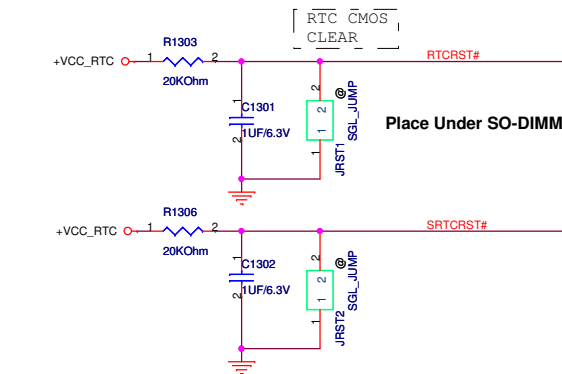




Decoupling guide from INTEL

VCORE 10uF x 16pcs
22uF x 12pcs

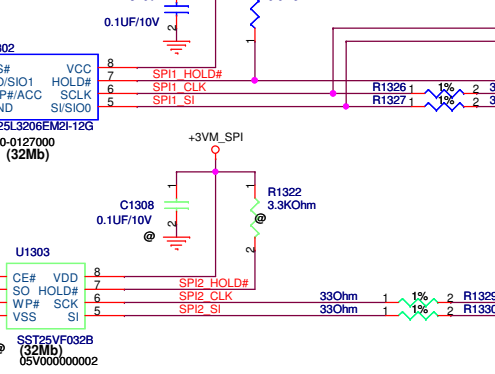
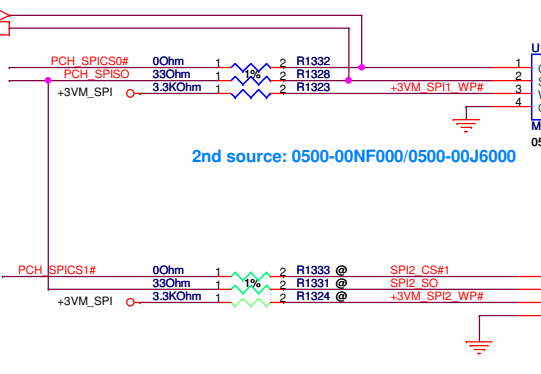
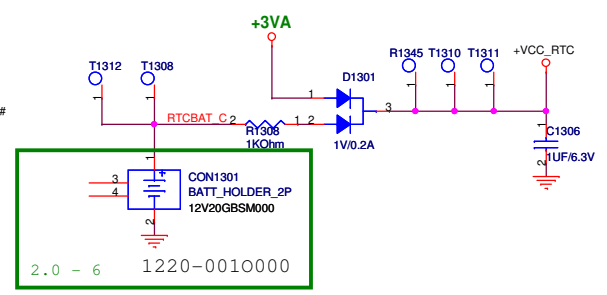




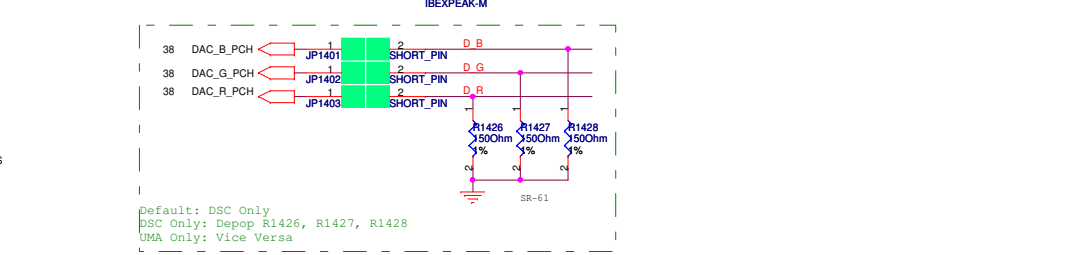
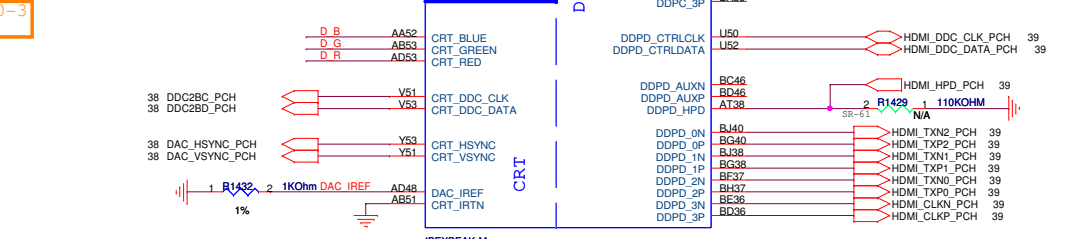
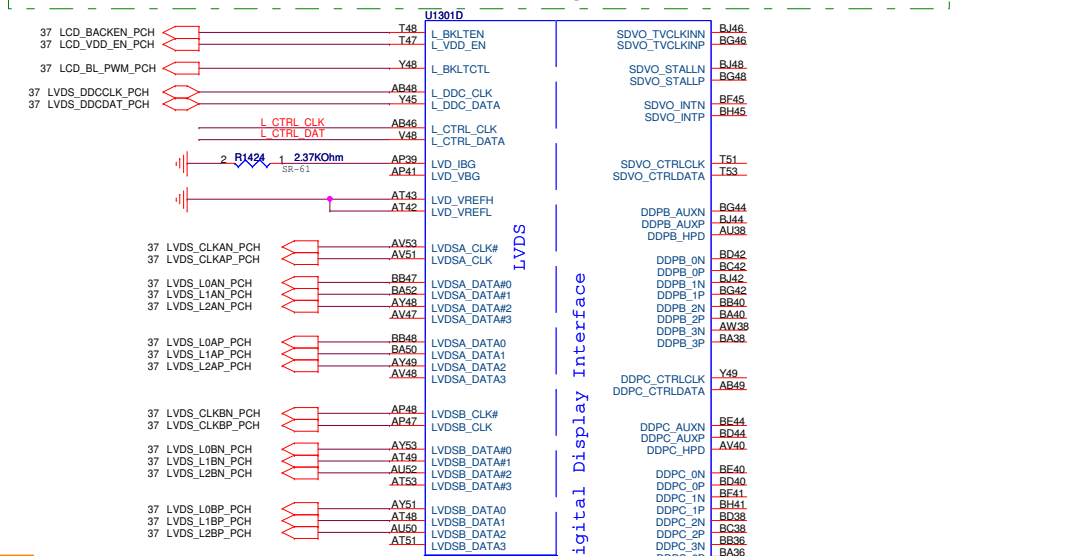
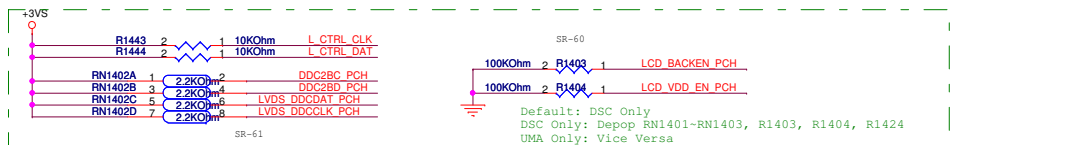
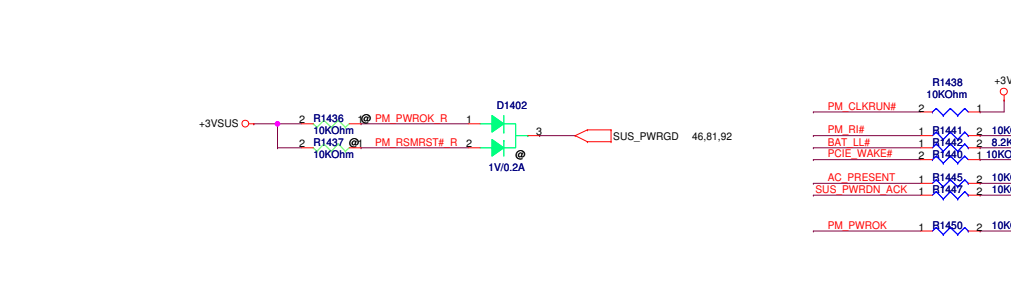
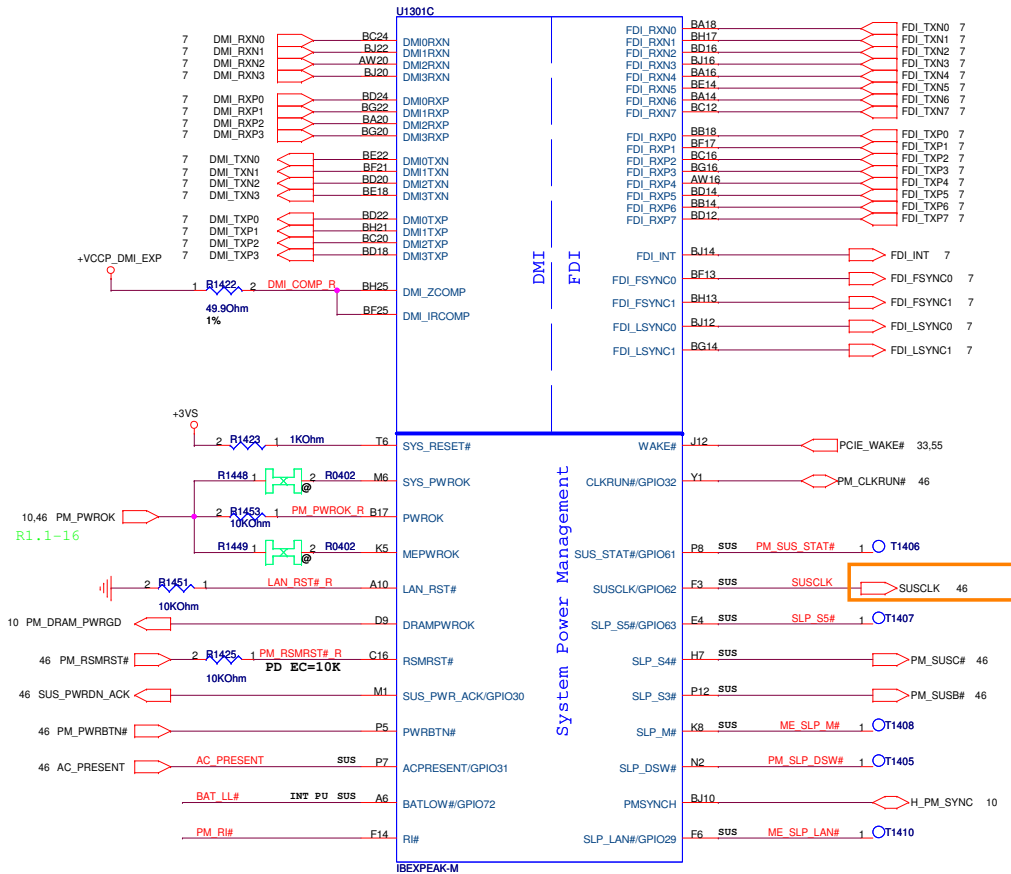
SATA PORT

SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	eSATA Removed

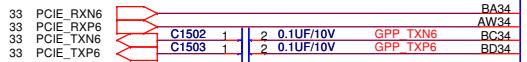
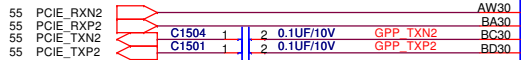
RTC BAT



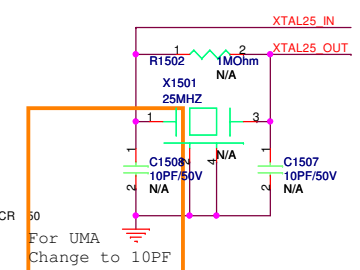
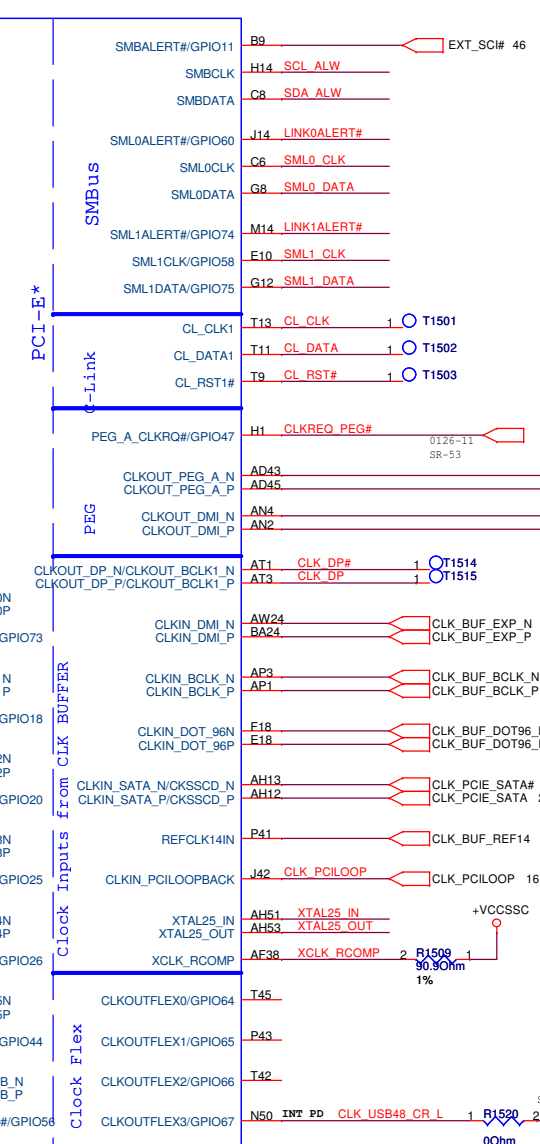
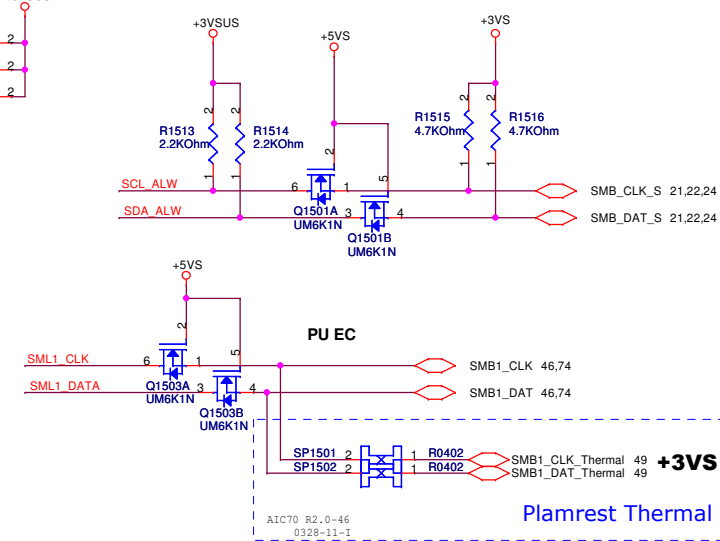
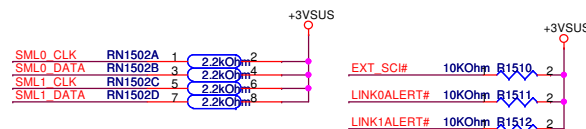
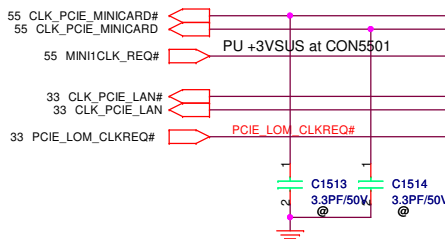
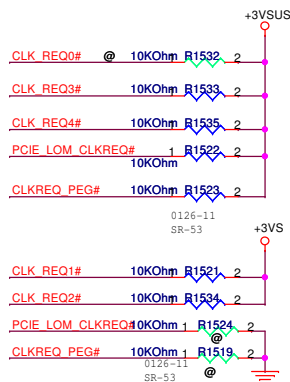
PEGATRON Title : PCH LPC/ SATA/ HDA
 BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang
 Size Project Name
 Custom AIC70
 Date: Wednesday, May 04, 2011 Sheet 13 of 77

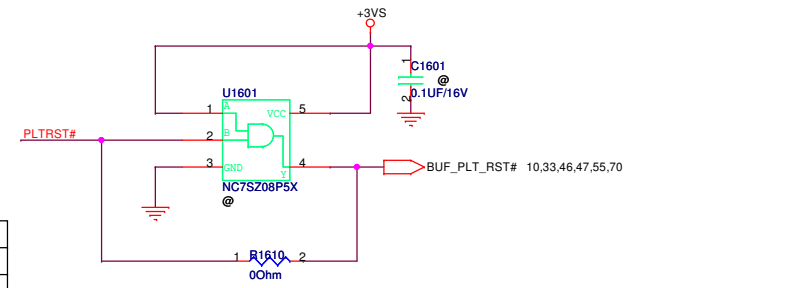
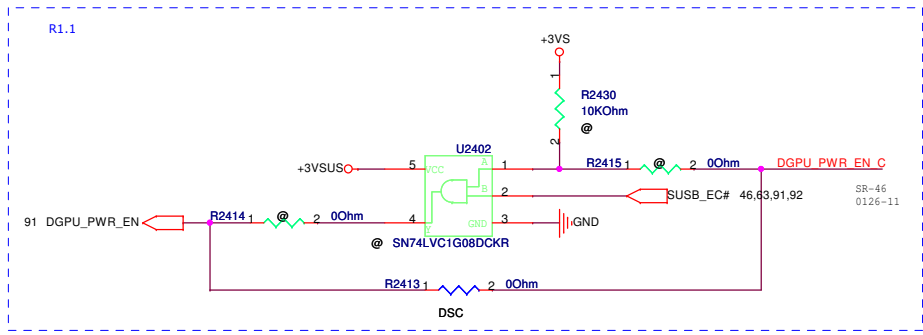
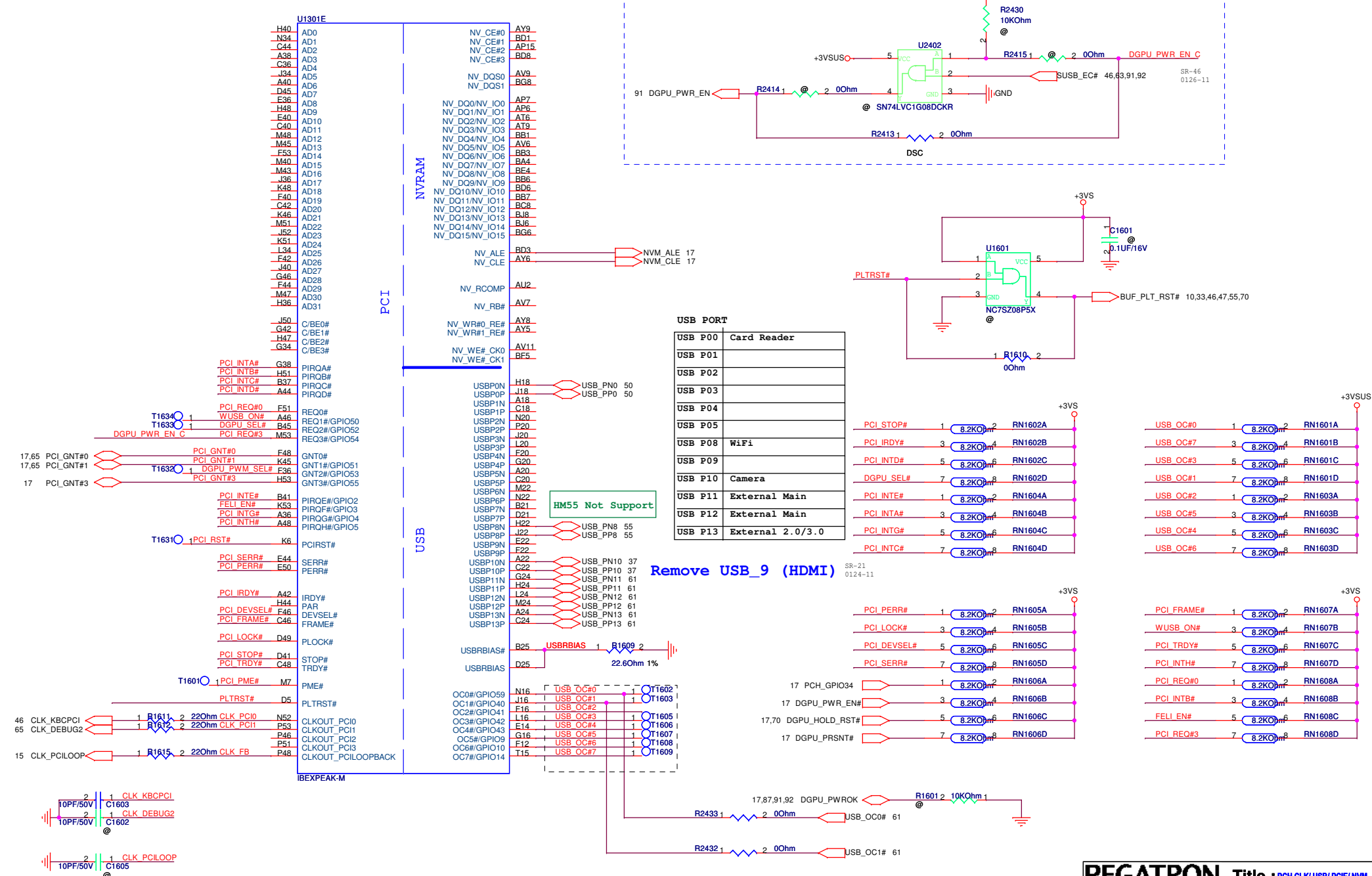


PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN



HM55 Not Support





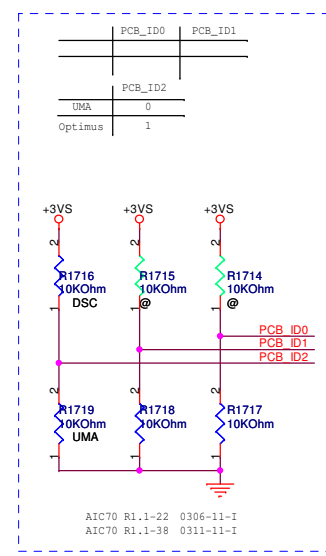
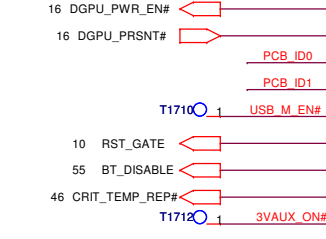
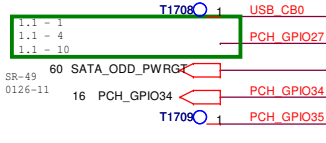
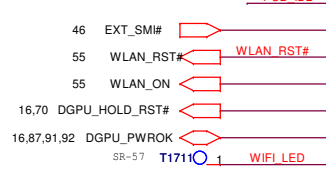
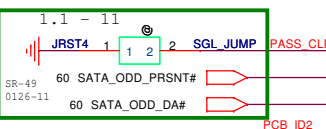
USB PORT

USB P00	Card Reader
USB P01	
USB P02	
USB P03	
USB P04	
USB P05	
USB P08	WiFi
USB P09	
USB P10	Camera
USB P11	External Main
USB P12	External Main
USB P13	External 2.0/3.0

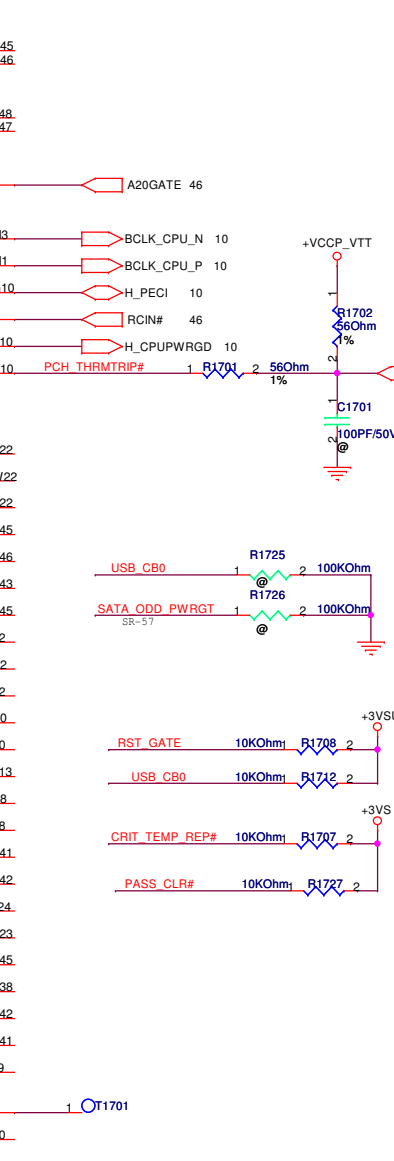
Remove USB_9 (HDMI) SR-21 0124-11

change USB power switch circuit

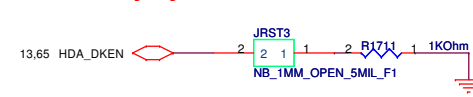
PEGATRON Title : PCH CLK/ USB/ PCIE/ NVM
 BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang
 Size Project Name
 Custom AIC70
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Pin	Signal	Function
Y3	PASS_CLR#	BMBUSY#/GPIO0
C38		TACH1/GPIO1
D37		TACH2/GPIO6
J32	PCB_ID2	TACH3/GPIO7
F10	EXT_SMI#	GPIO8
K9	WLAN_RST#	LAN_PHY_PWR_CTRL/GPIO12
T7	WLAN_ON	GPIO15
AA2	DGPU_HOLD_RST#	SATA4GP/GPIO16/CLKOUT_BCLK0_N/CLKOUT_PCIE8N
F38	DGPU_PWROK	TACH0/GPIO17 CLKOUT_BCLK0_P/CLKOUT_PCIE8P
Y7	WIFI_LED	SCLK/GPIO22
H10	USB_CB0	MEM_LED/GPIO24
V13		GPIO27
M11	PCH_GPIO34	GPIO28
V6	PCH_GPIO35	STP_PC#/GPIO34
AB7		SATA2GP/GPIO36
AB13		SATA3GP/GPIO37
V3	PCB_ID0	SLOAD/GPIO38
P3	PCB_ID1	SDATAOUT0/GPIO39
H3	USB_M_EN#	PCI_ECLKRQ6#/GPIO45
F1	RST_GATE	PCI_ECLKRQ7#/GPIO46
AB6	BT_DISABLE	SDATAOUT1/GPIO48
AA4	CRIT_TEMP_REP#	SATA5GP/GPIO49
F8	3VAUX_ON#	GPIO57
A4		Vss_NCTF1
A49		Vss_NCTF2
A5		Vss_NCTF3
A50		Vss_NCTF4
A52		Vss_NCTF5
A53		Vss_NCTF6
B2		Vss_NCTF7
B4		Vss_NCTF8
B52		Vss_NCTF9
B53		Vss_NCTF10
BE1		Vss_NCTF11
BE53		Vss_NCTF12
BF1		Vss_NCTF13
BE53		Vss_NCTF14
BH1		Vss_NCTF15
BH2		Vss_NCTF16
BH52		Vss_NCTF17
BH53		Vss_NCTF18
BJ1		Vss_NCTF19
BJ2		Vss_NCTF20
BJ4		Vss_NCTF21
BJ49		Vss_NCTF22
BJ5		Vss_NCTF23
BJ50		Vss_NCTF24
BJ52		Vss_NCTF25
BJ53		Vss_NCTF26
D1		Vss_NCTF27
D2		Vss_NCTF28
D53		Vss_NCTF29
E1		Vss_NCTF30
E53		Vss_NCTF31

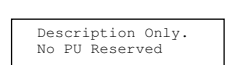


HDA_DKEN : Flash Descriptor Security Override
H = Disabled (Default)
L = Enabled
Note : Rising edge of PWROK

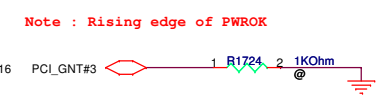


NOTE:
Assert the HDA_DKEN will halt and disable Intel ME.
This is a debug mode and must not asserted after manufacturing/debug.

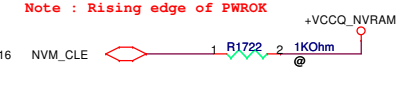
PCH_SPI1 : iTPM STRAP
H : Enable iTPM
L : Disable iTPM (Default)



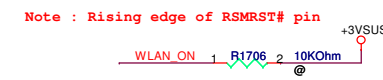
PCI_GNT#3 : A16 swap override
Strap/Top-Block Swap Override jumper
H : Default
L : A16 swap override/Top-Block Swap Override enabled



NVM_CLE : DMI Termination Voltage
H : Set to Vcc
L : Set to Vss



GPIO15/ WLAN_ON :
H = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality
L = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality



PCH_INTVRMEN : Integrated SUS 1.05V VRM Enable
H : Integrated VRM is enabled
L : Integrated VRM is disabled
Note : This signal should always be pulled high

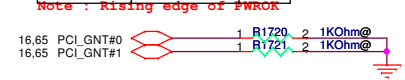


SPKR_PCH : NO REBOOT STRAP
H : Enable
L : Disable (Default)
Note : Rising edge of PWROK

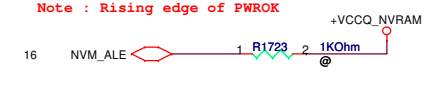


PCI_GNT#1, PCI_GNT#0 : Boot BIOS Strap

PCI_GNT#0	PCI_GNT#1	Function
0	0	LPC
0	1	PCI
1	1	SPI

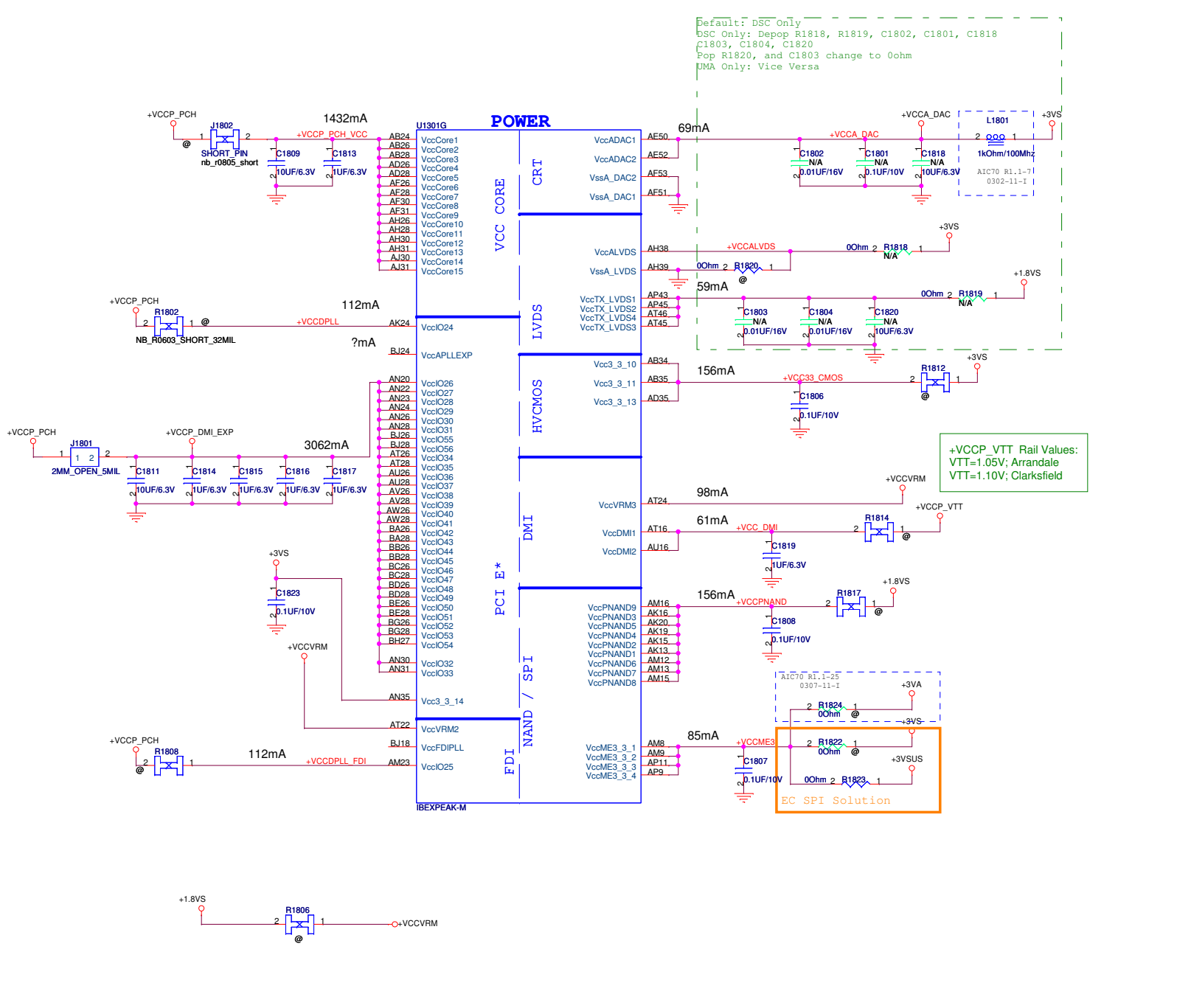


NVM_ALE : Danbury Technology Enabled
High--> Enable Intel Anti-Theft Technology.
Low--> Disable Intel Anti-Theft Technology.

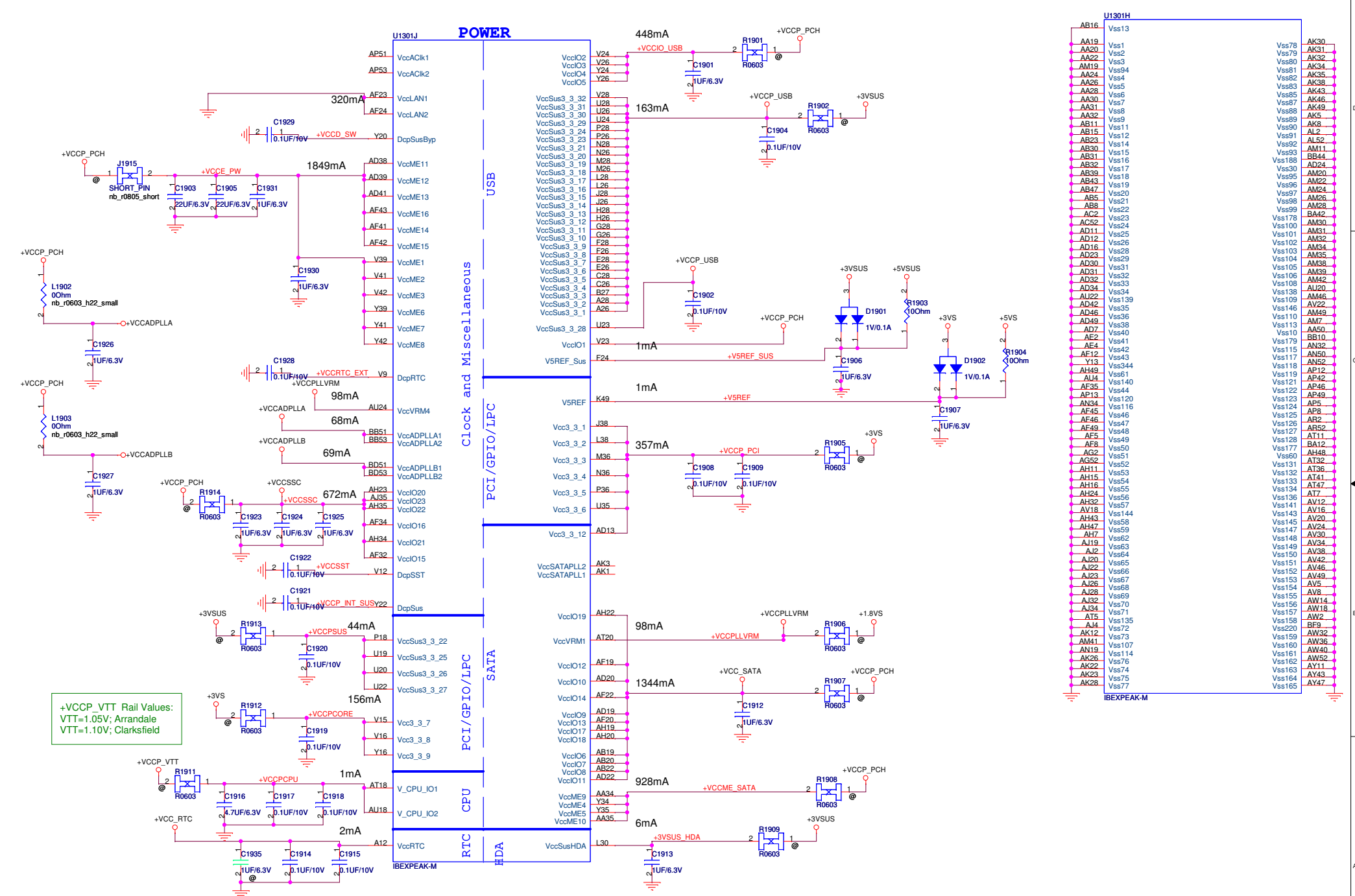


GPIO27/ USB_SW :
H = Enables the internal VccVRM. (Default)
L = Disables the VccVRM.
Note : Rising edge of RSMRST# pin

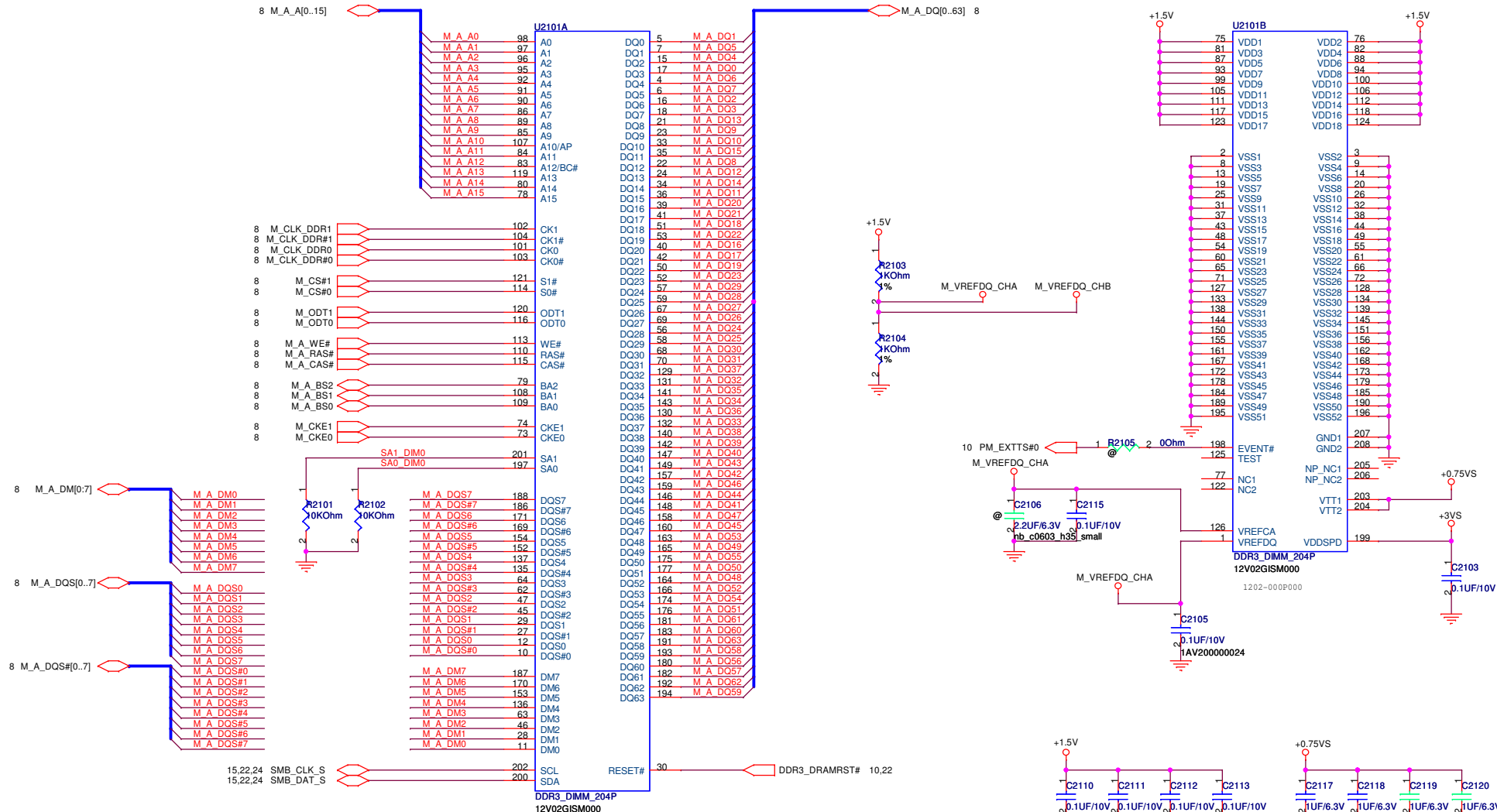




U1301I		H49	
AY7	Vss166	Vss270	H5
B11	Vss167	Vss271	J24
B15	Vss168	Vss272	K1
B23	Vss169	Vss273	K43
B31	Vss170	Vss274	K47
B35	Vss171	Vss275	K7
B39	Vss172	Vss276	L14
B43	Vss173	Vss277	L18
B47	Vss174	Vss278	L2
B7	Vss175	Vss279	L22
BG12	Vss176	Vss280	L32
BB12	Vss180	Vss282	L36
BB16	Vss181	Vss283	L40
BB20	Vss182	Vss285	L52
BB24	Vss183	Vss286	M12
BB30	Vss184	Vss287	M16
BB34	Vss185	Vss288	M20
BB38	Vss186	Vss289	M32
BB42	Vss187	Vss290	M38
BB49	Vss189	Vss291	M42
BB5	Vss190	Vss292	M46
BC10	Vss191	Vss293	M49
BC14	Vss192	Vss294	M5
BC18	Vss193	Vss295	M8
BC2	Vss194	Vss296	N24
BC22	Vss195	Vss297	P11
BC32	Vss196	Vss298	P15
BC36	Vss197	Vss299	P22
BC40	Vss198	Vss300	P30
BC44	Vss199	Vss302	P32
BC52	Vss200	Vss303	P34
BH9	Vss202	Vss304	P42
BD48	Vss203	Vss305	P45
BD49	Vss204	Vss306	P47
BD5	Vss205	Vss307	P52
BE12	Vss206	Vss308	R2
BE16	Vss207	Vss309	R52
BE24	Vss208	Vss310	T12
BE30	Vss209	Vss311	T4
BE34	Vss210	Vss312	T46
BE38	Vss211	Vss313	T49
BE42	Vss212	Vss314	T5
BE46	Vss213	Vss315	T8
BE48	Vss214	Vss316	T5
BE50	Vss215	Vss317	L30
BE6	Vss216	Vss318	U31
BE8	Vss217	Vss319	U32
BF3	Vss218	Vss320	U32
BF49	Vss219	Vss321	U34
BF51	Vss220	Vss322	P38
BG18	Vss221	Vss323	V19
BG24	Vss222	Vss324	V19
BG4	Vss223	Vss325	P16
BG50	Vss224	Vss326	V20
BH11	Vss225	Vss327	V30
BH15	Vss226	Vss328	V31
BH19	Vss227	Vss329	V32
BH23	Vss228	Vss330	V34
BH31	Vss229	Vss331	V35
BH35	Vss230	Vss332	V38
BH39	Vss231	Vss333	V43
BH43	Vss232	Vss334	V46
BH47	Vss233	Vss335	V47
BH7	Vss234	Vss336	V49
C12	Vss235	Vss337	V5
C12	Vss237	Vss338	V7
C50	Vss238	Vss339	V8
D51	Vss239	Vss340	W2
E16	Vss240	Vss341	W52
E20	Vss241	Vss342	Y11
E24	Vss242	Vss343	Y12
E30	Vss243	Vss344	Y15
E34	Vss244	Vss345	Y19
E38	Vss245	Vss346	Y23
E42	Vss246	Vss347	Y28
E46	Vss247	Vss348	Y30
E48	Vss248	Vss349	Y31
E8	Vss249	Vss350	Y32
F49	Vss250	Vss351	Y36
F5	Vss251	Vss352	Y43
G10	Vss252	Vss353	Y43
G14	Vss253	Vss354	Y46
G18	Vss254	Vss355	P49
G2	Vss255	Vss356	Y5
G2	Vss256	Vss357	Y6
G2	Vss257	Vss358	Y8
G22	Vss258	Vss359	P24
G32	Vss259	Vss360	T43
G36	Vss260	Vss361	AD51
G40	Vss261	Vss362	AT8
G44	Vss262	Vss363	AD47
G52	Vss263	Vss364	Y47
H16	Vss264	Vss365	AT12
H20	Vss265	Vss366	AM6
H30	Vss266	Vss367	AT13
H34	Vss267	Vss368	AM5
H38	Vss268	Vss369	Vss86
H42	Vss269	Vss370	AK39
			AV14

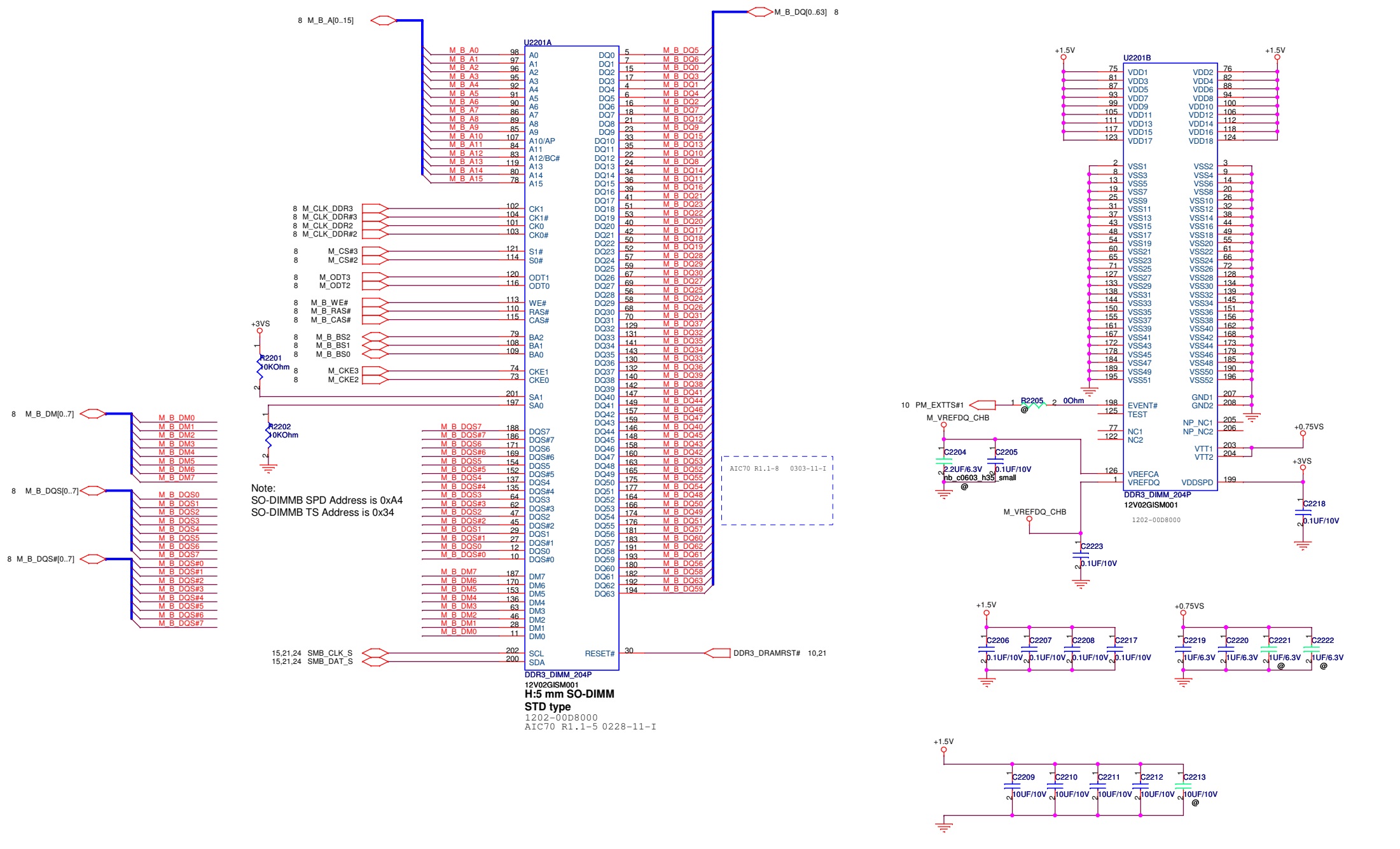


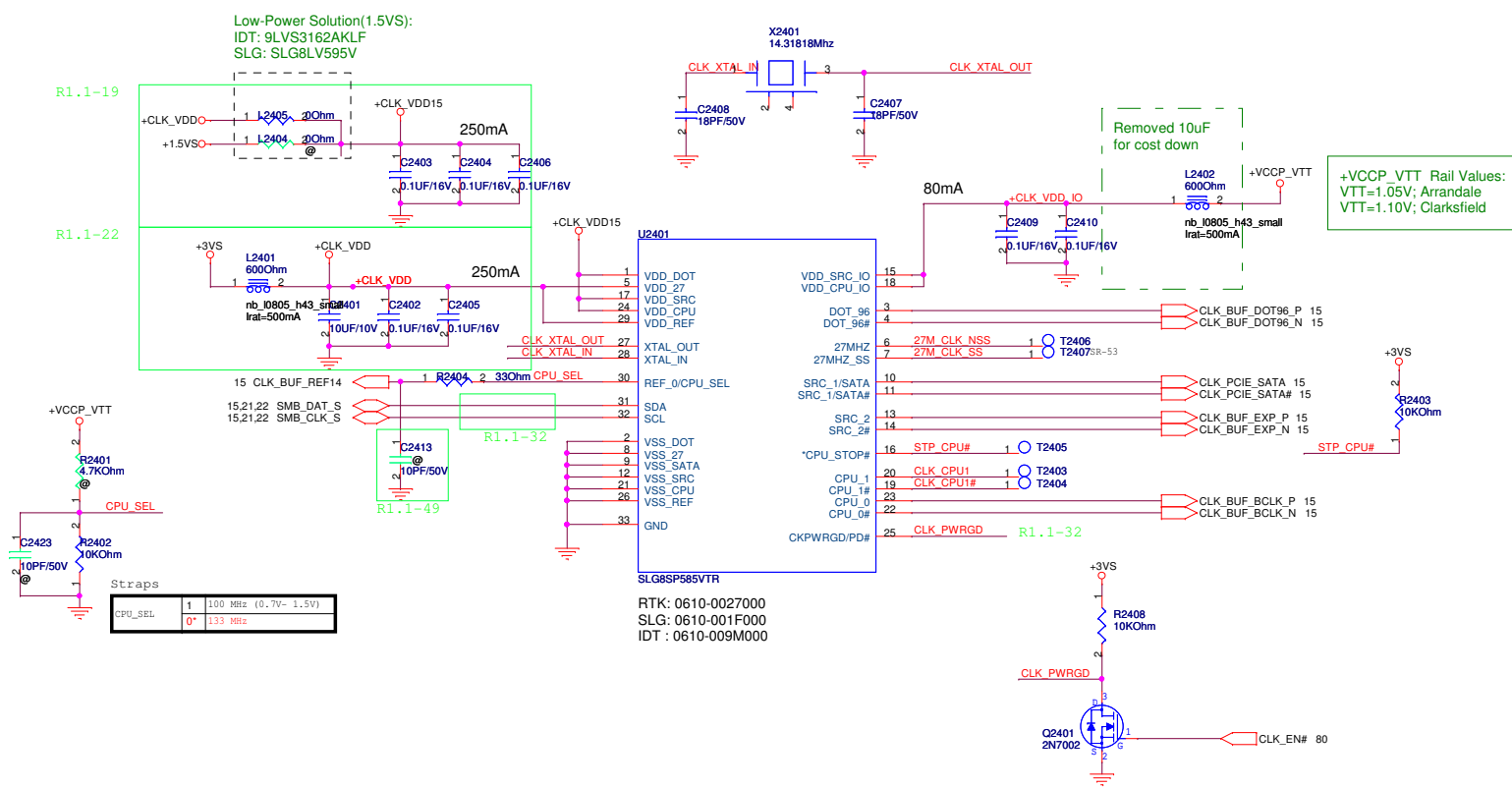
U1301H		IBEXPEAK-M	
AB16	Vss13	Vss78	AK30
AA19	Vss1	Vss79	AK31
AA20	Vss2	Vss80	AK32
AA22	Vss4	Vss81	AK33
AM19	Vss94	Vss82	AK34
AA24	Vss4	Vss83	AK35
AA28	Vss5	Vss84	AK38
AA28	Vss5	Vss85	AK43
AA30	Vss6	Vss87	AK46
AA31	Vss7	Vss88	AK49
AA32	Vss8	Vss89	AK5
AB11	Vss9	Vss90	AK8
AB15	Vss11	Vss91	AL2
AB23	Vss12	Vss92	AL52
AB30	Vss14	Vss93	AM11
AB30	Vss15	Vss99	AM22
AB31	Vss16	Vss100	AM24
AB32	Vss17	Vss102	AM30
AB39	Vss18	Vss103	AM31
AB43	Vss19	Vss104	AM32
AB47	Vss20	Vss105	AM34
AB5	Vss21	Vss106	AM38
AB5	Vss22	Vss107	AM39
AC2	Vss23	Vss108	AM42
AC52	Vss24	Vss109	AM44
AD11	Vss25	Vss110	AM46
AD12	Vss26	Vss111	AM49
AD16	Vss27	Vss112	AM7
AD23	Vss28	Vss113	AM7
AD30	Vss29	Vss114	AM7
AD31	Vss30	Vss115	AN32
AD32	Vss31	Vss116	AN50
AD34	Vss32	Vss117	AN52
AU22	Vss33	Vss118	AP2
AD42	Vss34	Vss119	AP42
Vss139	Vss35	Vss120	AP46
AD46	Vss36	Vss121	AP5
AD49	Vss37	Vss122	AP5
AD7	Vss38	Vss123	AP8
AE2	Vss39	Vss124	AP8
AE4	Vss40	Vss125	AR2
AF12	Vss41	Vss126	AR2
Vss43	Vss42	Vss127	AR52
AH49	Vss43	Vss128	AT11
AU4	Vss44	Vss129	AT11
Vss140	Vss45	Vss130	AT32
AF35	Vss46	Vss131	AT36
AP13	Vss47	Vss132	AT36
Vss120	Vss48	Vss133	AT41
AN34	Vss49	Vss134	AT47
Vss116	Vss50	Vss135	AT7
AF46	Vss51	Vss136	AV12
AF46	Vss52	Vss137	AV12
AF49	Vss53	Vss138	AV16
AF5	Vss54	Vss139	AV20
AF8	Vss55	Vss140	AV24
Vss49	Vss56	Vss141	AV30
AG52	Vss57	Vss142	AV34
AH11	Vss58	Vss143	AV38
AH15	Vss59	Vss144	AV38
AH16	Vss60	Vss145	AV42
AH24	Vss61	Vss146	AV44
AH32	Vss62	Vss147	AV49
AV18	Vss63	Vss148	AV5
AH43	Vss64	Vss149	AV8
Vss144	Vss65	Vss150	AW14
AH43	Vss66	Vss151	AW14
AH47	Vss67	Vss152	AW18
AH7	Vss68	Vss153	AW18
AH9	Vss69	Vss154	AW22
AJ	Vss70	Vss155	AW22
Vss65	Vss71	Vss156	AW32
AJ20	Vss72	Vss157	AW36
Vss66	Vss73	Vss158	AW36
AJ22	Vss74	Vss159	AW38
AJ23	Vss75	Vss160	AW40
AJ26	Vss76	Vss161	AW40
AJ28	Vss77	Vss162	AW52
AJ32	Vss78	Vss163	AY11
AJ34	Vss79	Vss164	AY43
Vss69	Vss80	Vss165	AY47
Vss70	Vss81		
Vss71	Vss82		
Vss72	Vss83		
Vss73	Vss84		
Vss74	Vss85		
Vss75	Vss86		
Vss76	Vss87		
Vss77	Vss88		
Vss78	Vss89		
Vss79	Vss90		
Vss80	Vss91		
Vss81	Vss92		
Vss82	Vss93		
Vss83	Vss94		
Vss84	Vss95		
Vss85	Vss96		
Vss86	Vss97		
Vss87	Vss98		
Vss88	Vss99		
Vss89	Vss100		
Vss90	Vss101		
Vss91	Vss102		
Vss92	Vss103		
Vss93	Vss104		
Vss94	Vss105		
Vss95	Vss106		
Vss96	Vss107		
Vss97	Vss108		
Vss98	Vss109		
Vss99	Vss110		
Vss100	Vss111		
Vss101	Vss112		
Vss102	Vss113		
Vss103	Vss114		
Vss104	Vss115		
Vss105	Vss116		
Vss106	Vss117		
Vss107	Vss118		
Vss108	Vss119		
Vss109	Vss120		
Vss110	Vss121		
Vss111	Vss122		
Vss112	Vss123		
Vss113	Vss124		
Vss114	Vss125		
Vss115	Vss126		
Vss116	Vss127		
Vss117	Vss128		
Vss118	Vss129		
Vss119	Vss130		
Vss120	Vss131		
Vss121	Vss132		
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Vss142	Vss153		
Vss143	Vss154		
Vss144	Vss155		
Vss145	Vss156		
Vss146	Vss157		
Vss147	Vss158		
Vss148	Vss159		
Vss149	Vss160		
Vss150	Vss161		
Vss151	Vss162		
Vss152	Vss163		
Vss153	Vss164		
Vss154	Vss165		
Vss155	Vss166		

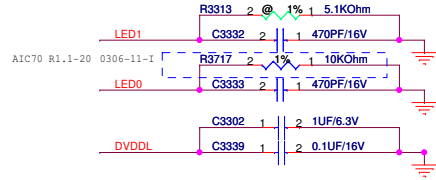
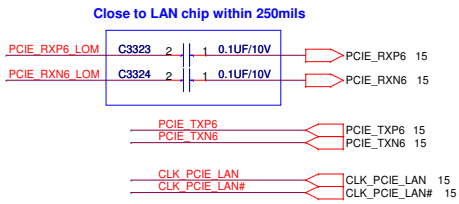


Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

H:8 mm SO-DIMM
STD type
 1202-000P000
 AIC70 R1.1-5 0228-11-1



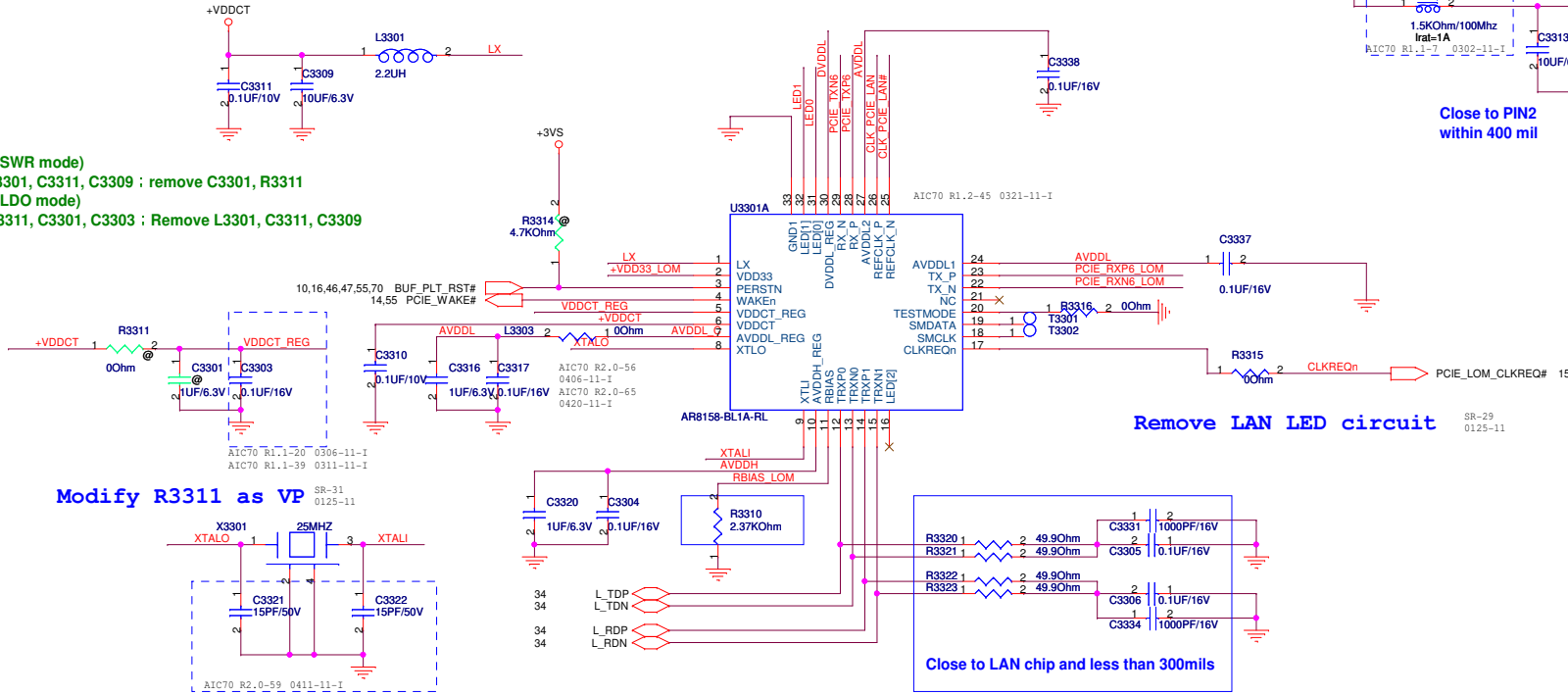
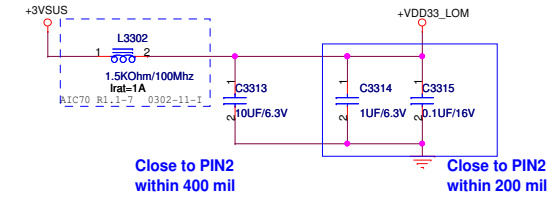




Modify H/W strap setting

- Pow-on strapping
- (1) LED[0]: enable overclocking
pull-high: overlocking (default)
stuff R3326, R3324; Remove R3317, R3325, R3327;
pull-low: un-overclocking
stuff R2, R3325, R3327; Remove R3326, R3324
 - (2) LED[1]: selection for AR8158's internal VDDCT (SWR/LDO)
pull-high: SWR mode
stuff R3330, R3332; Remove R3313, R3331, R3333;
pull-low: LDO mode
stuff R3313, R3331, R3333; Remove R3330, R3332

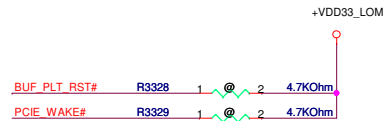
- AR8158 (SWR mode)
Stuff L3301, C3311, C3309 ; remove C3301, R3311
AR8158 (LDO mode)
Stuff R3311, C3301, C3303 ; Remove L3301, C3311, C3309



Modify R3311 as VP

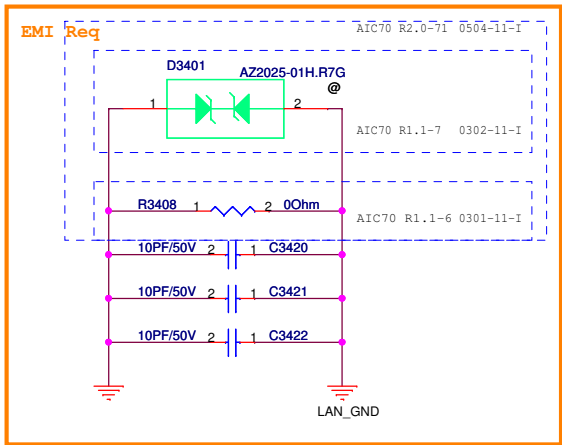
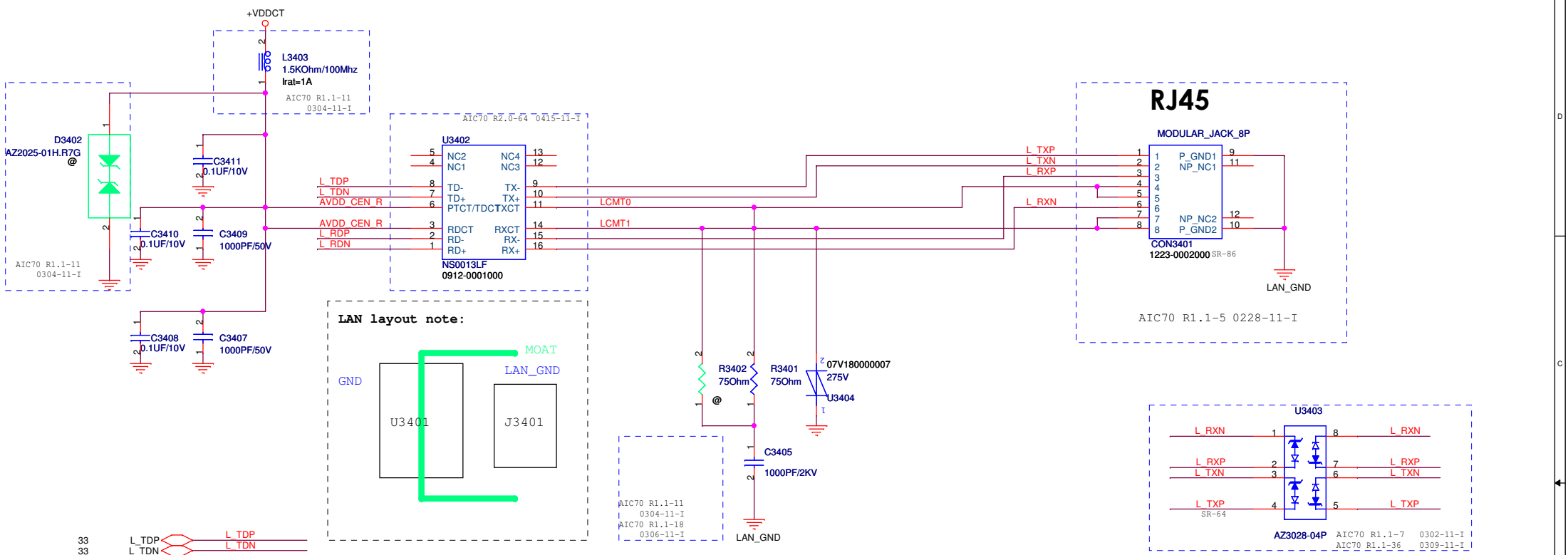
Remove LAN LED circuit

Close to LAN chip and less than 300mils



Modify LAN AR8158 circuit

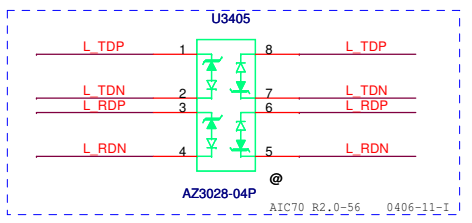
Change U3301 to AR8158 Part and remover SM BUS



Modify LAN AR8158 circuit SR-12 0121-11

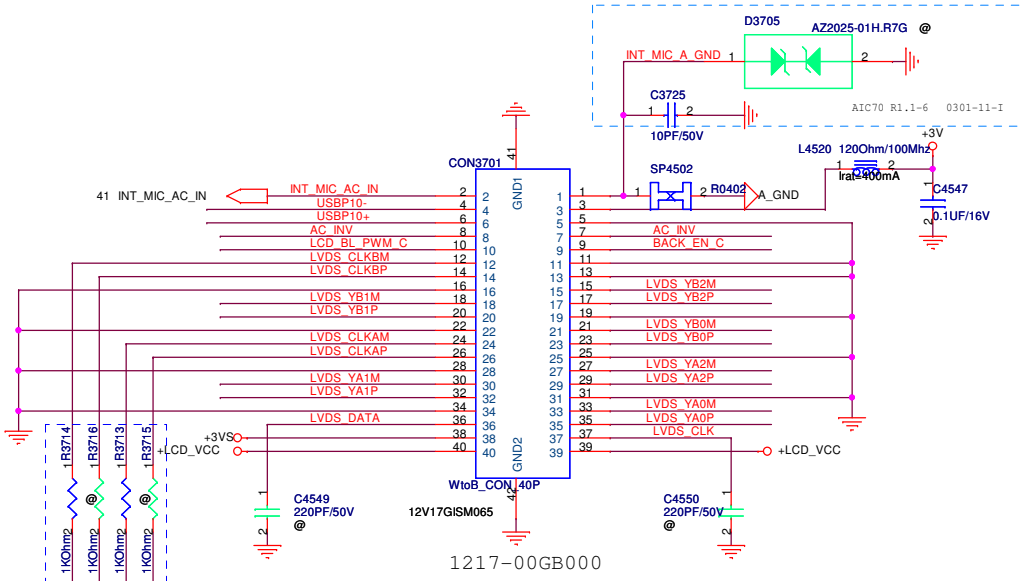
Modify Transformer circuit SR-40 0125-11 SR-45 SR-48 0125-11 0125-11

Modify LAN ESD circuit SR-33 0125-11



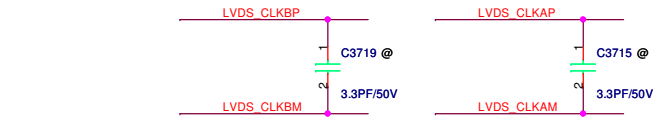
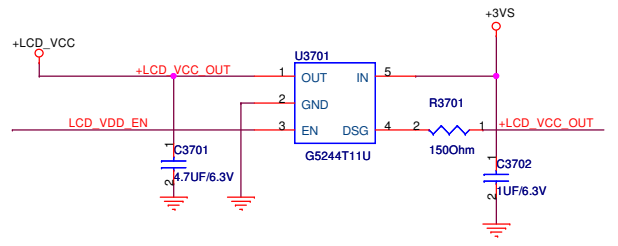
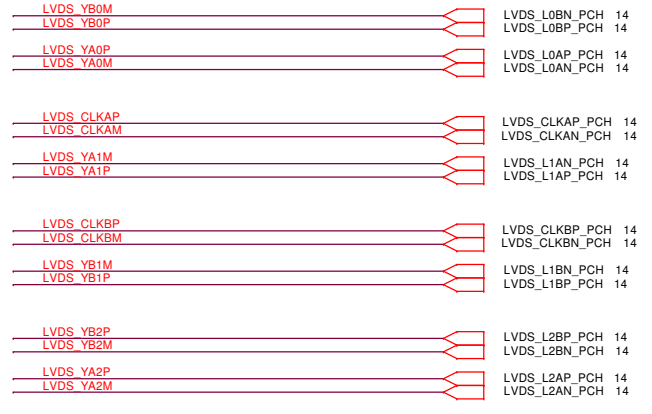
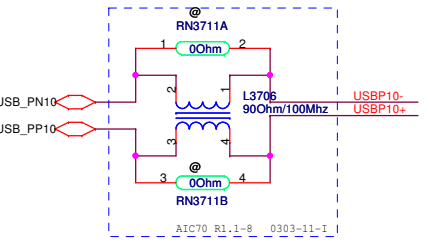
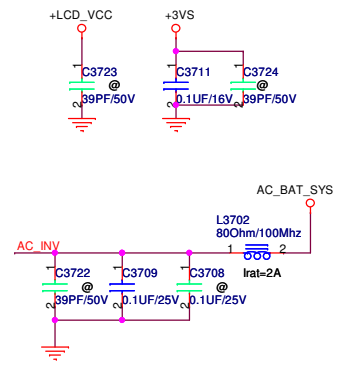
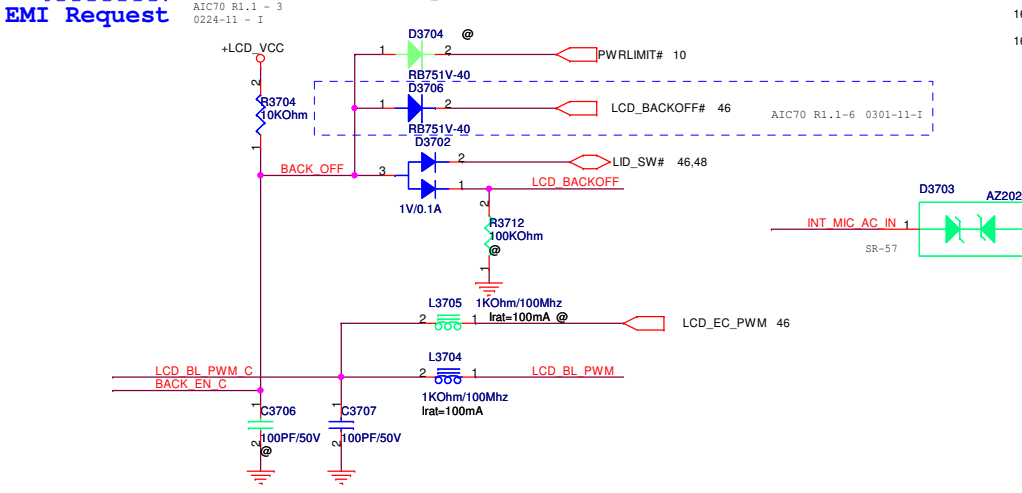
PEGATRON Title :R.J45		
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Johnson Huang		
Size B	Project Name AIC70	Rev 2.0
Date: Wednesday, May 04, 2011 Sheet 34 of 77		

LVDS Conn w/Camera Module & Int Mic

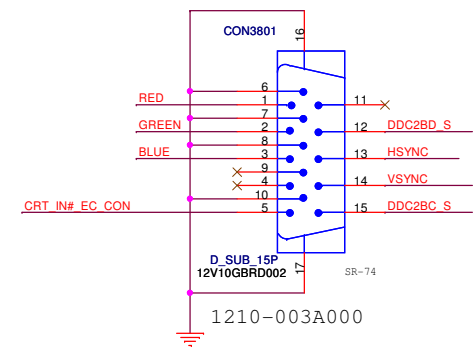
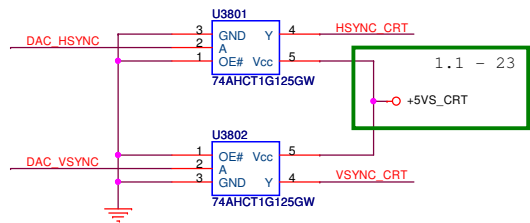
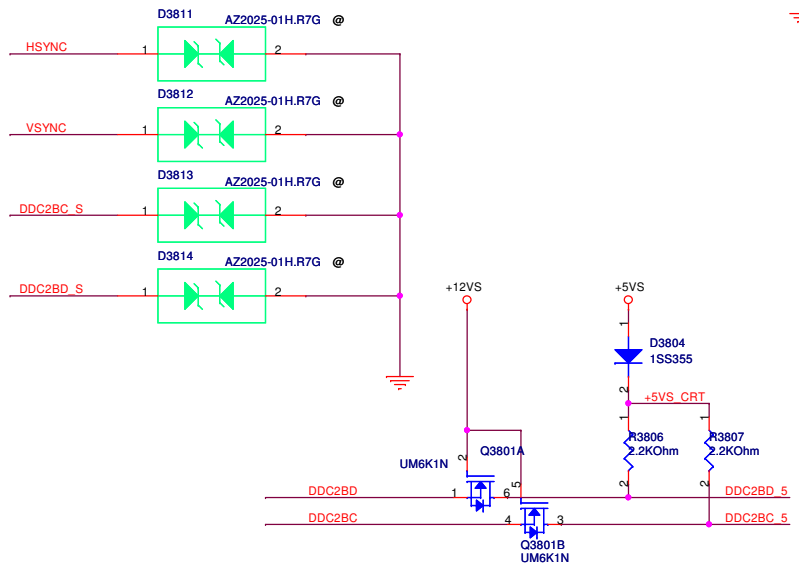
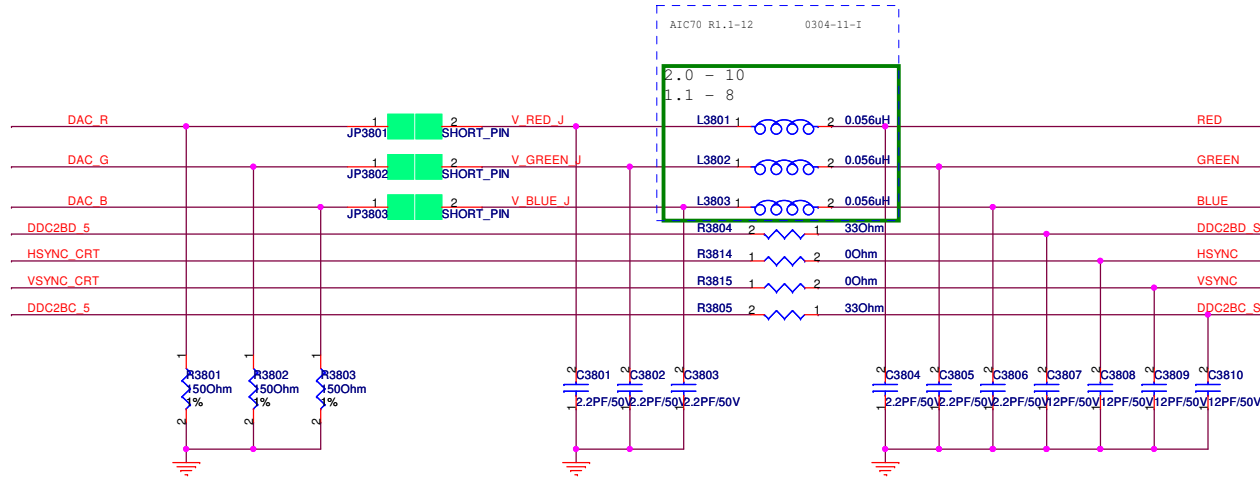


EMI Request

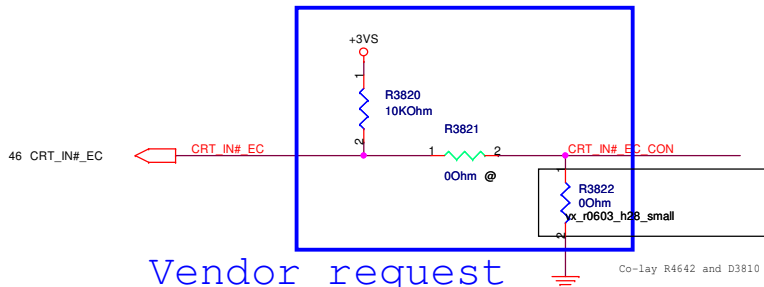
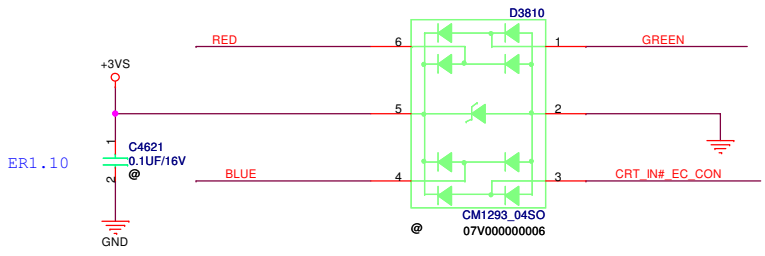
Modify LVDS Pin definition

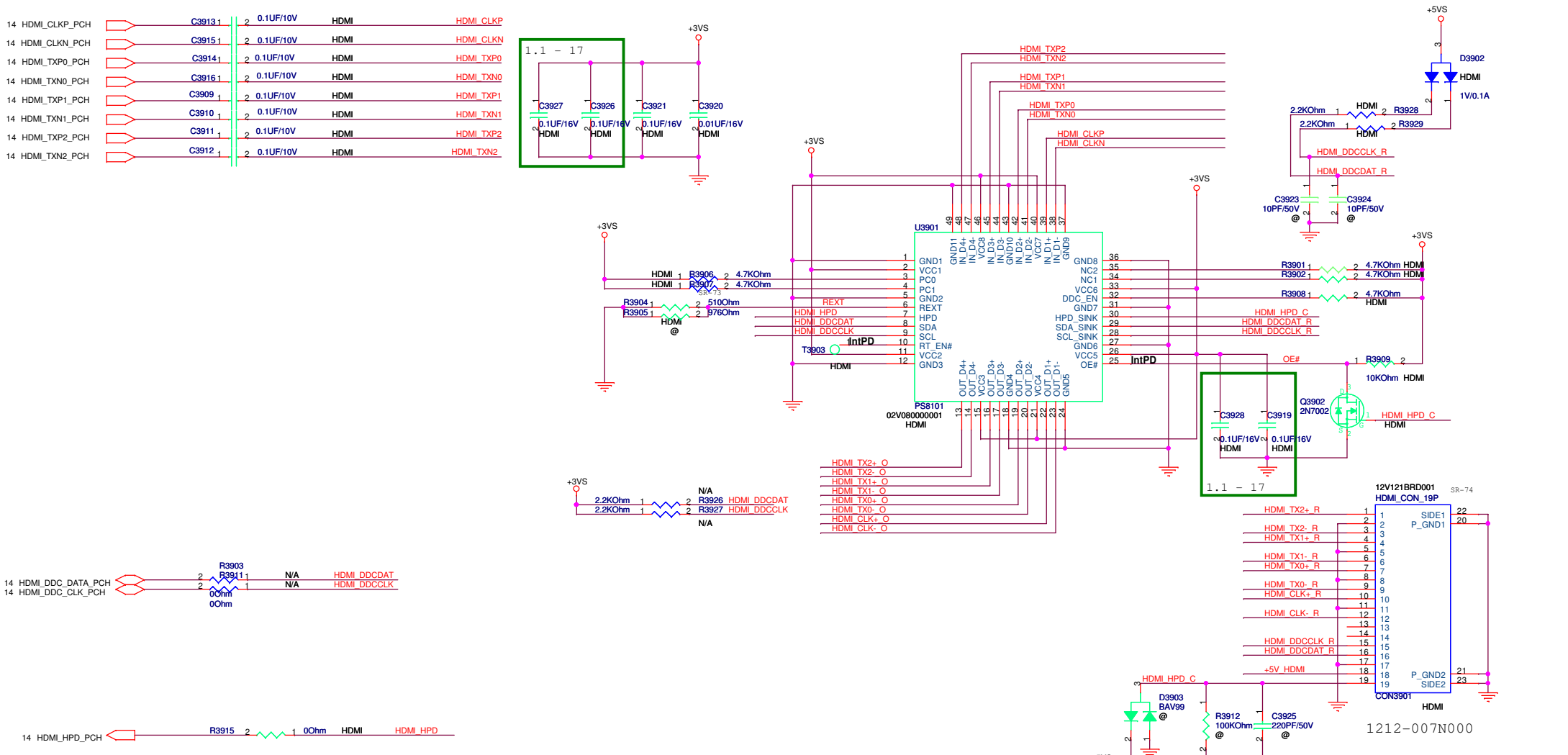


- 14 DAC_R_PCH → DAC_R
- 14 DAC_G_PCH → DAC_G
- 14 DAC_B_PCH → DAC_B
- 14 DAC_HSYNC_PCH → DAC_HSYNC
- 14 DAC_VSYNC_PCH → DAC_VSYNC
- 14 DDC2BD_PCH → DDC2BD
- 14 DDC2BC_PCH → DDC2BC

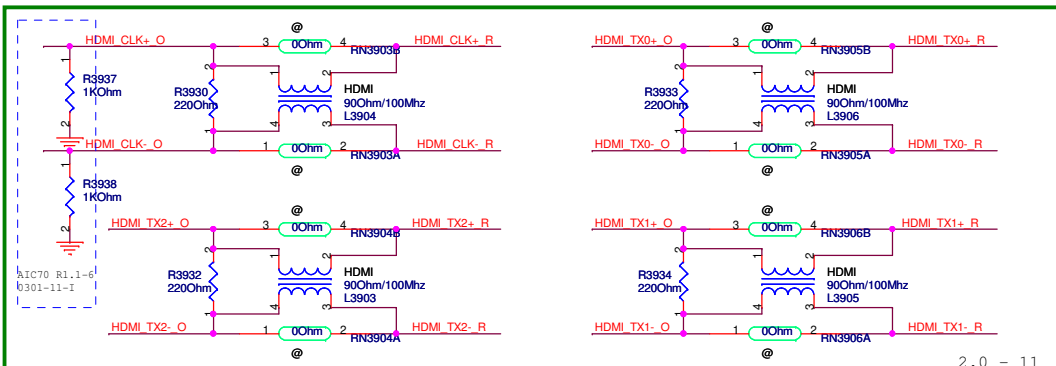


Del F3801, C3811 ADD CRT IN SR-36 0125-11

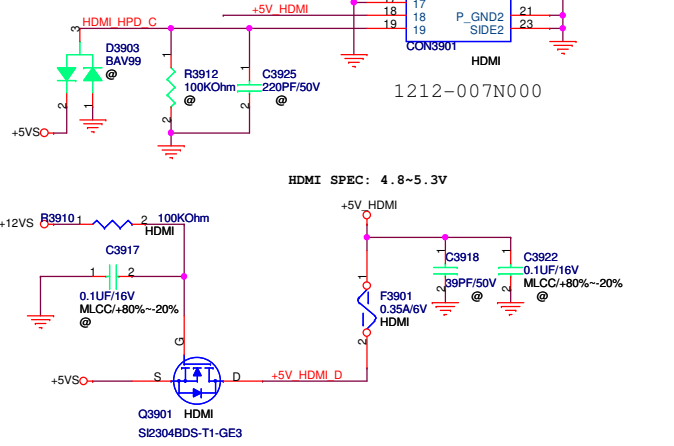




1.1 - 14



2.0 - 11



PEGATRON Title : **HDMI**
 BG1-HW RD Div.2-NB RD Dept.5 Engineer: **Johnson Huang**

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 39 of 77

5

4

3

2

1

D

D

C

C

B

B

A

A

PEGATRON		Title : <i>Display Port</i>	
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Johnson Huang</i>	
Size Custom	Project Name AIC70	Date: <i>Wednesday, May 04, 2011</i>	Rev 2.0
		Sheet	40 of 77

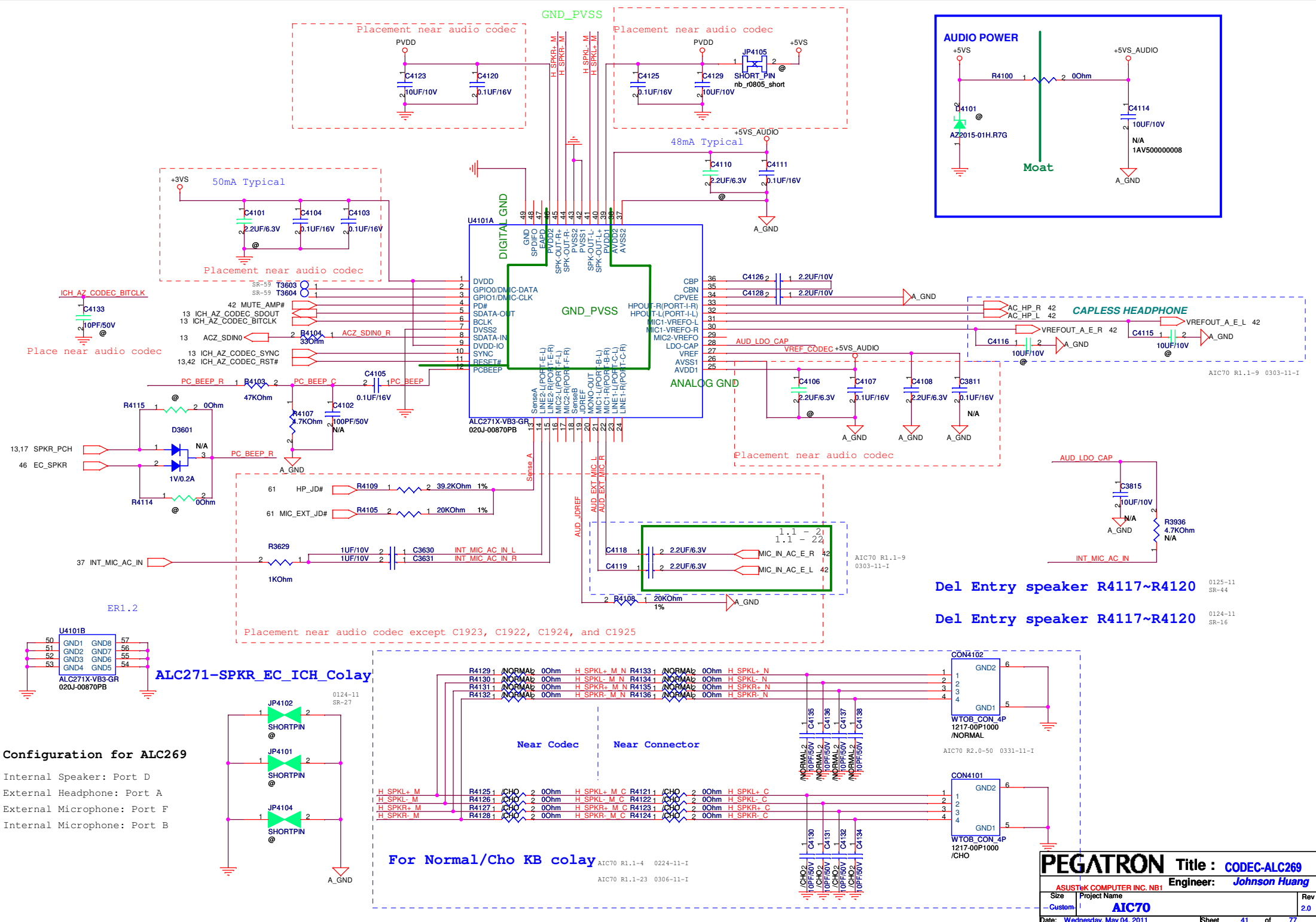
5

4

3

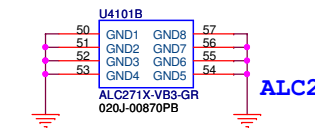
2

1

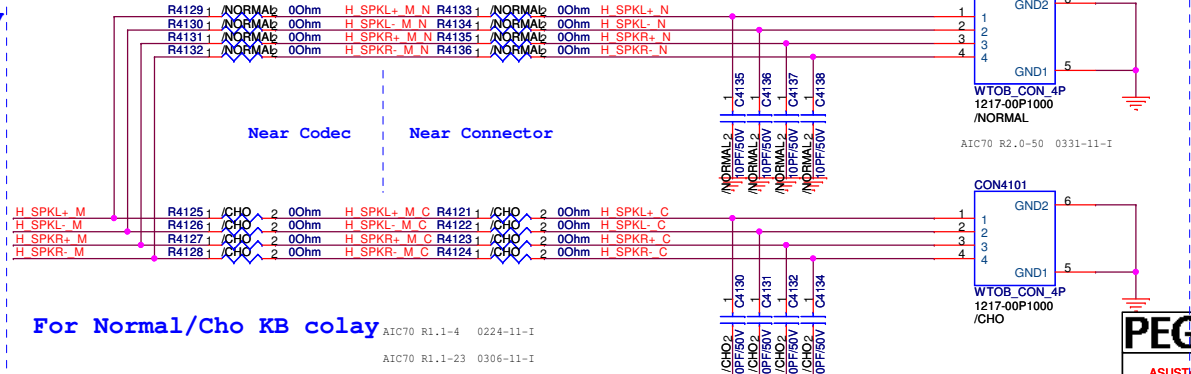
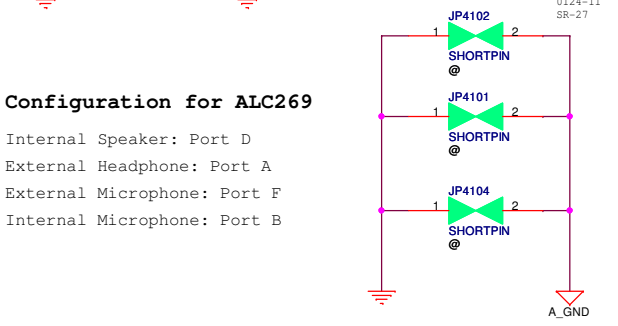


Configuration for ALC269

Internal Speaker: Port D
 External Headphone: Port A
 External Microphone: Port F
 Internal Microphone: Port B

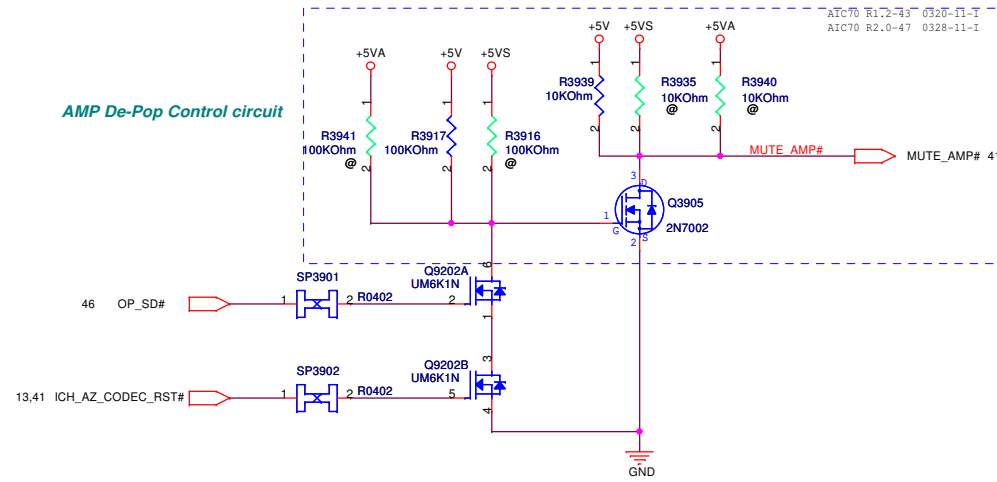


ALC271X-SPKR_EC_ICH Colay



PEGATRON Title : **CODEC-ALC269**
 ASUSTEK COMPUTER INC. NB1 Engineer: **Johnson Huang**
 Size Project Name
 - Custom **AIC70**
 Date: **Wednesday, May 04, 2011** Sheet **41** of **77**
 Rev **2.0**

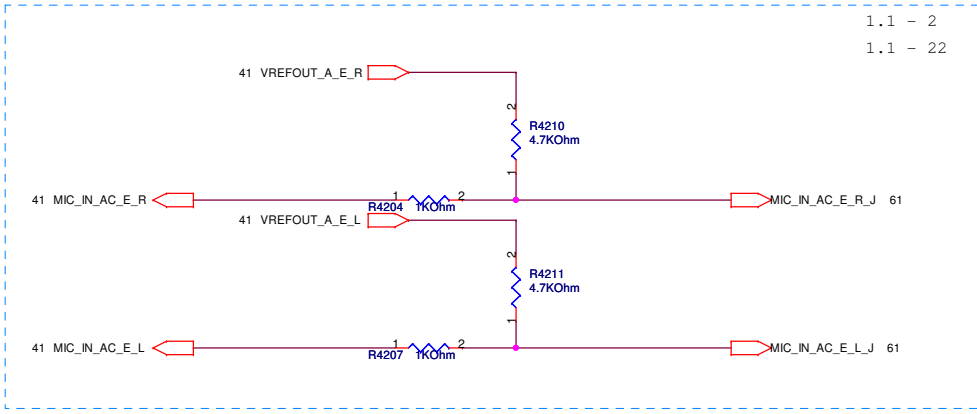
AMP De-Pop Control circuit



AIC70 R1.2-43 0320-11-I
AIC70 R2.0-47 0328-11-I

Modify De-Pop circuit

SR-43
0125-11



1.1 - 2
1.1 - 22



N/A
SR-58
N/A

5

4

3

2

1

D

D

C

C

B

B

A

A

PEGATRON		Title : MDC CONN	
BG1-HW RD Dw:2-NB RD Dept.5		Engineer: <i>Johnson Huang</i>	
Size	Project Name	Rev	
C	AIC70	2.0	
Date: <i>Wednesday, May 04, 2011</i>		Sheet	43 of 77

5

4

3

2

1

D

D

C

C

B

B

A

A

Del Entry audio circuit SR-8
0121-11

PEGATRON		Title : CODEC-ALC269	
ASUSTeK COMPUTER INC. NB1		Engineer: Johnson Huang	
Size Custom	Project Name AIC70	Date: Wednesday, May 04, 2011	Rev 2.0
		Sheet	44 of 77

5

4

3

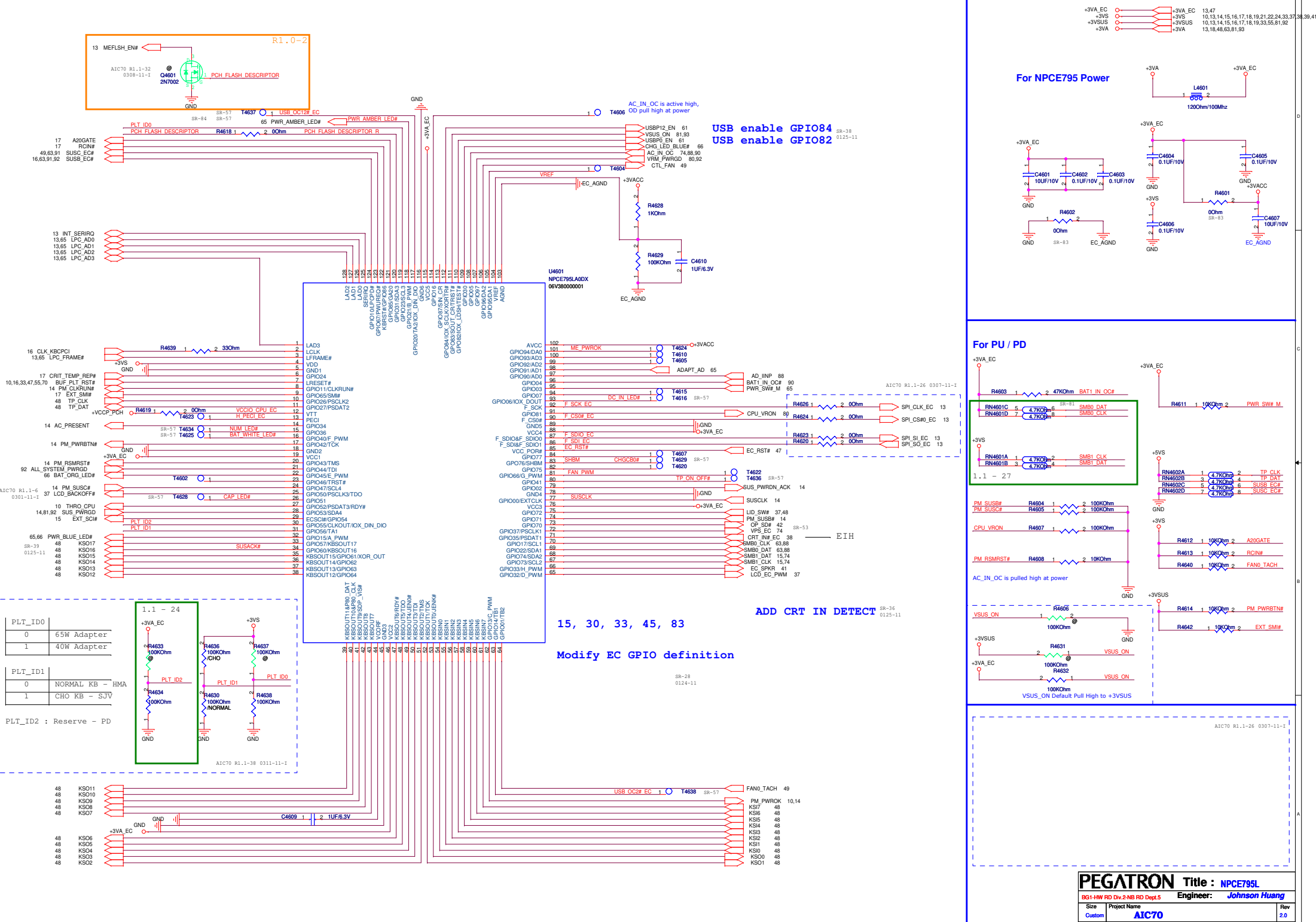
2

1

Del Entry audio circuit

SR-8
0121-11

PEGATRON		Title : AUDIO ALC269	
BU1-RD Div.1-HW RD Dept.1		Engineer: Johnson Huang	
Size Custom	Project Name AIC70	Date: Wednesday, May 04, 2011	Rev 2.0
Date: Wednesday, May 04, 2011		Sheet	45 of 77

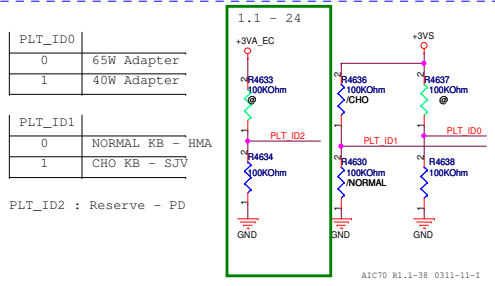
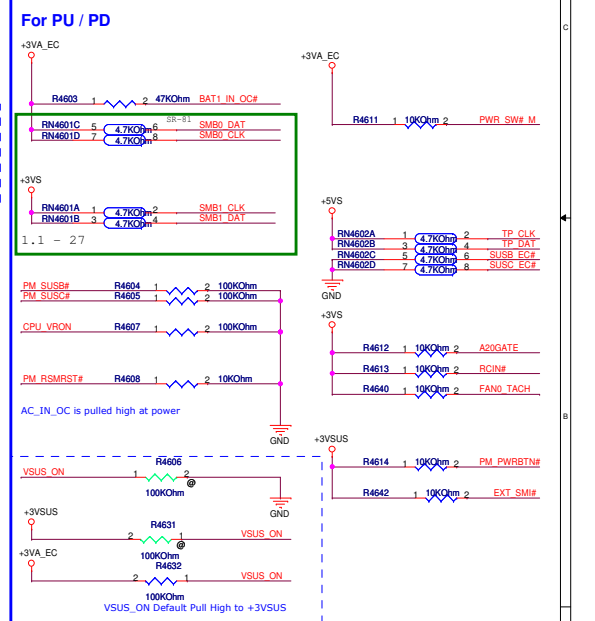
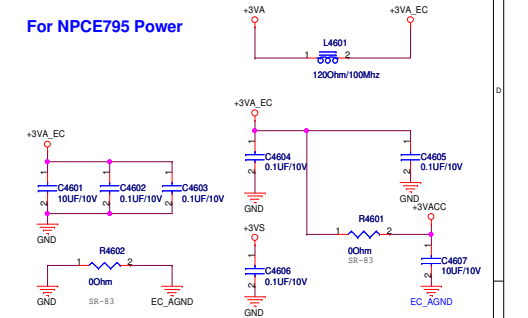
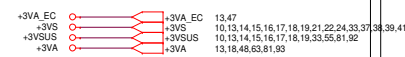


USB enable GPIO84
USB enable GPIO82

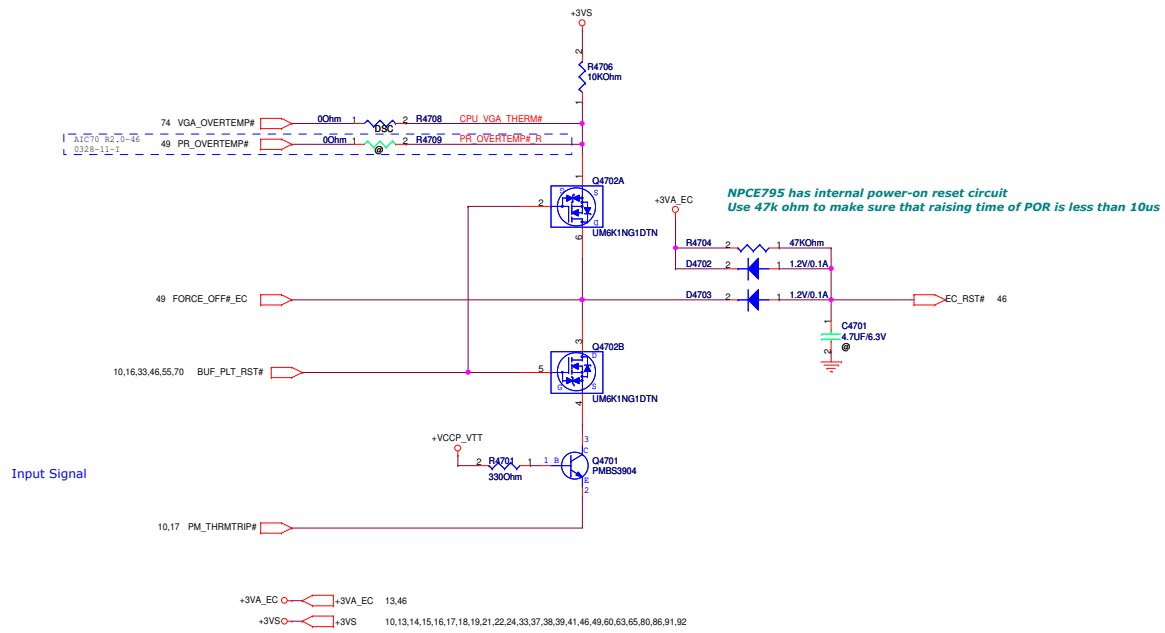
ADD CRT IN DETECT

15, 30, 33, 45, 83

Modify EC GPIO definition

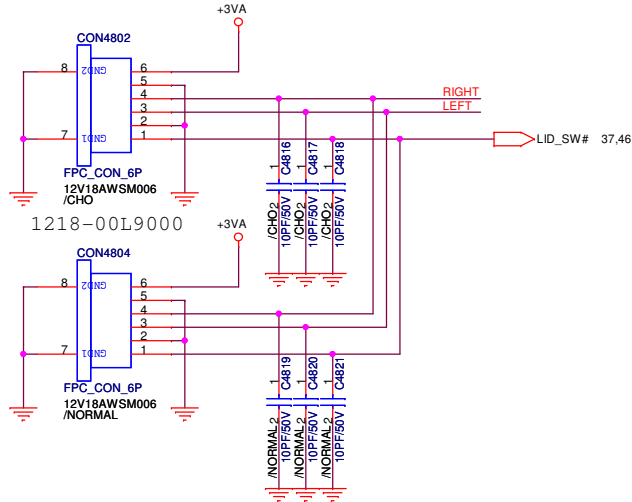


Thermal Policy

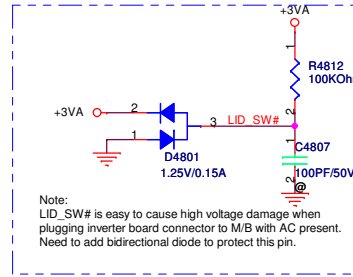


Touch Pad Button/ Hall Sensor

AIC70 R1.1-23 0306-11-I
AIC70 R1.1-35 0309-11-I

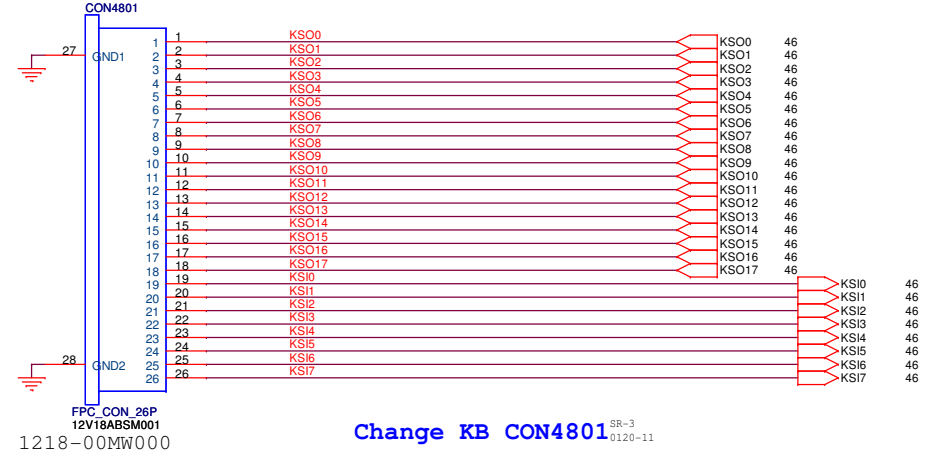


close to U4601



Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

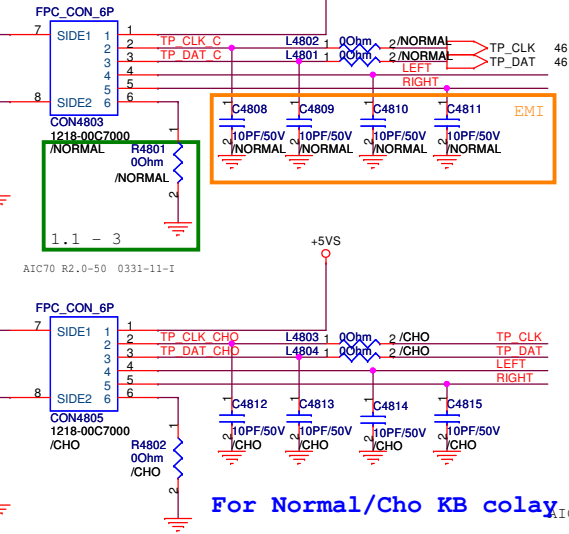
Keyboard FOR 17"



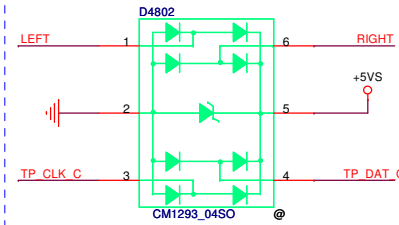
Change KB CON4801 SR-3 0120-11

Change KB CON4801 PIN definition SR-25 0124-11
Reverse KB CON4801 SR-19 SR-52 0124-11 0126-11

Touch Pad



For Normal/Cho KB colay 0224-11-I
AIC70 R1.1-4



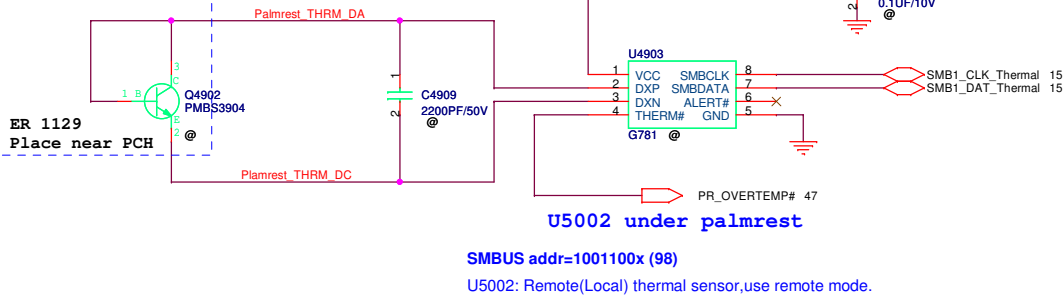
Remove 15'' KB connector AIC70 R1.1 - 1 0224-11 - I

Remove TP button circuit SR-22 0124-11

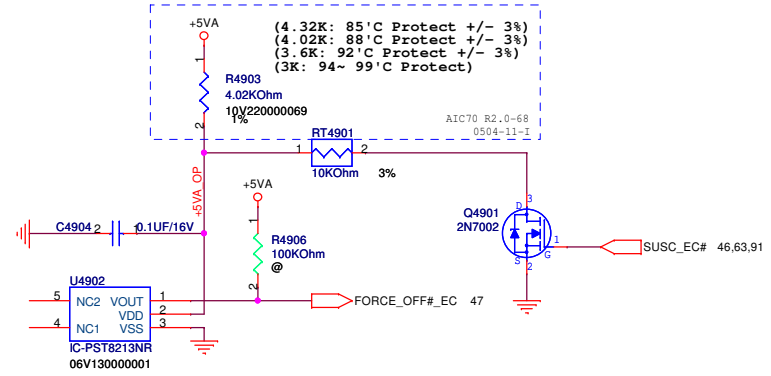
Palm Rest Thermal Sensor

PHILIP PMBS3904

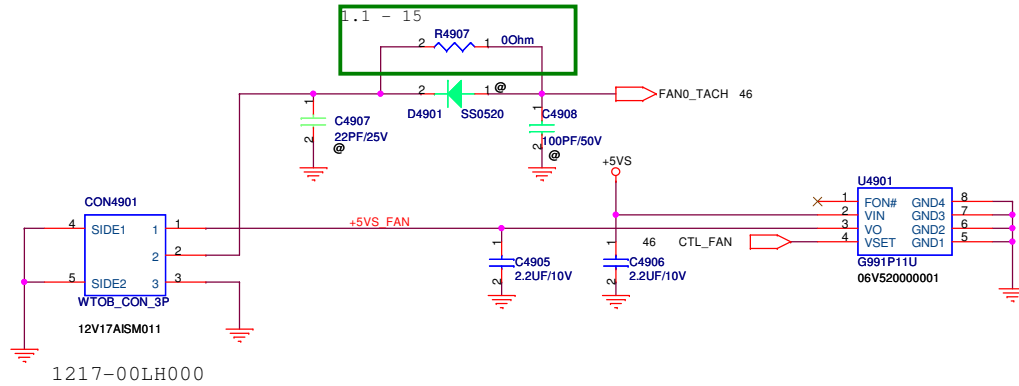
Place in the center of Plamrest.

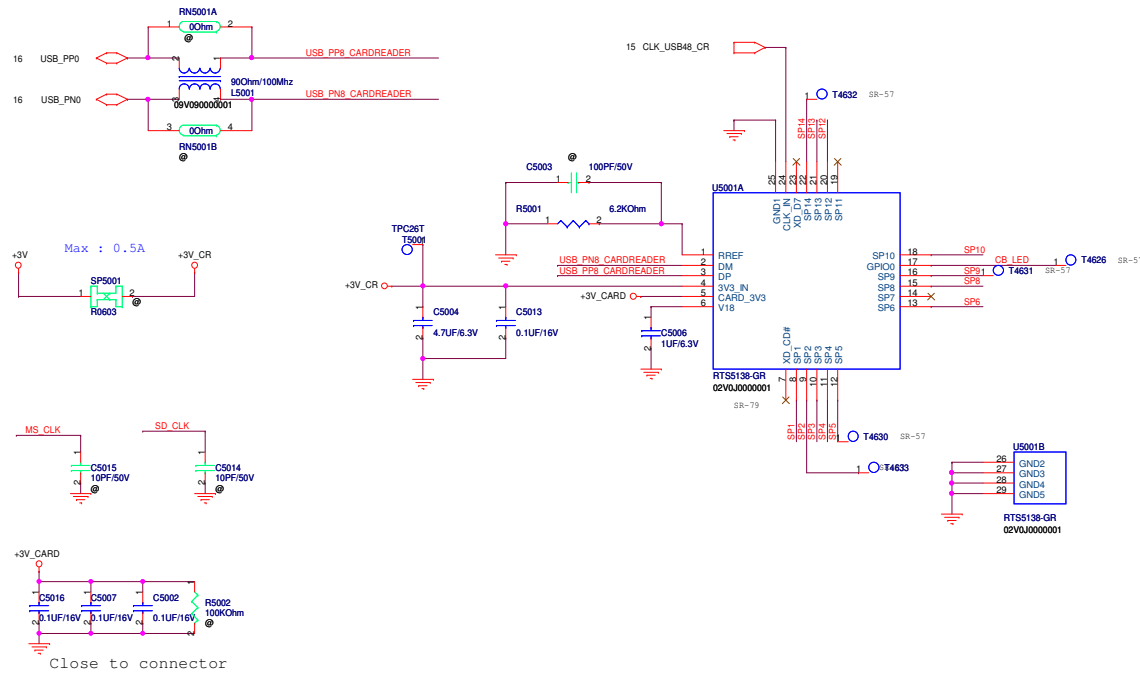


Thermister



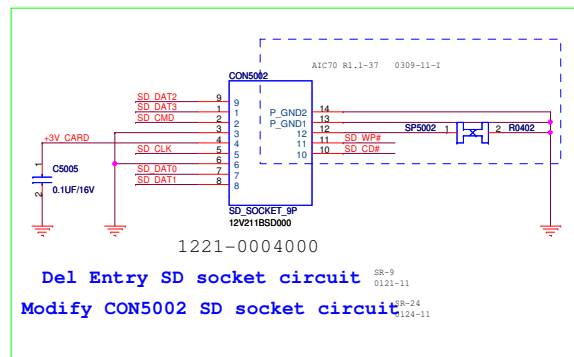
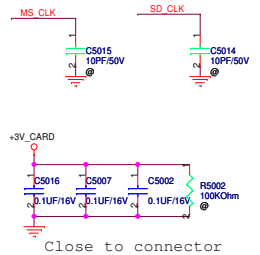
FAN





Pin Name	Description
SP1	SDWP# / MSCLK
SP2	MS_INS#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_BS

SP1	SD WP#	MS_CLK
SP2		MS_INS#
SP3	SD_DAT1	
SP4	SD_DAT0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_DAT3	MS_D1
SP13	SD_DAT2	
SP14		MS_BS



5

4

3

2

1

D

D

C

C

B

B

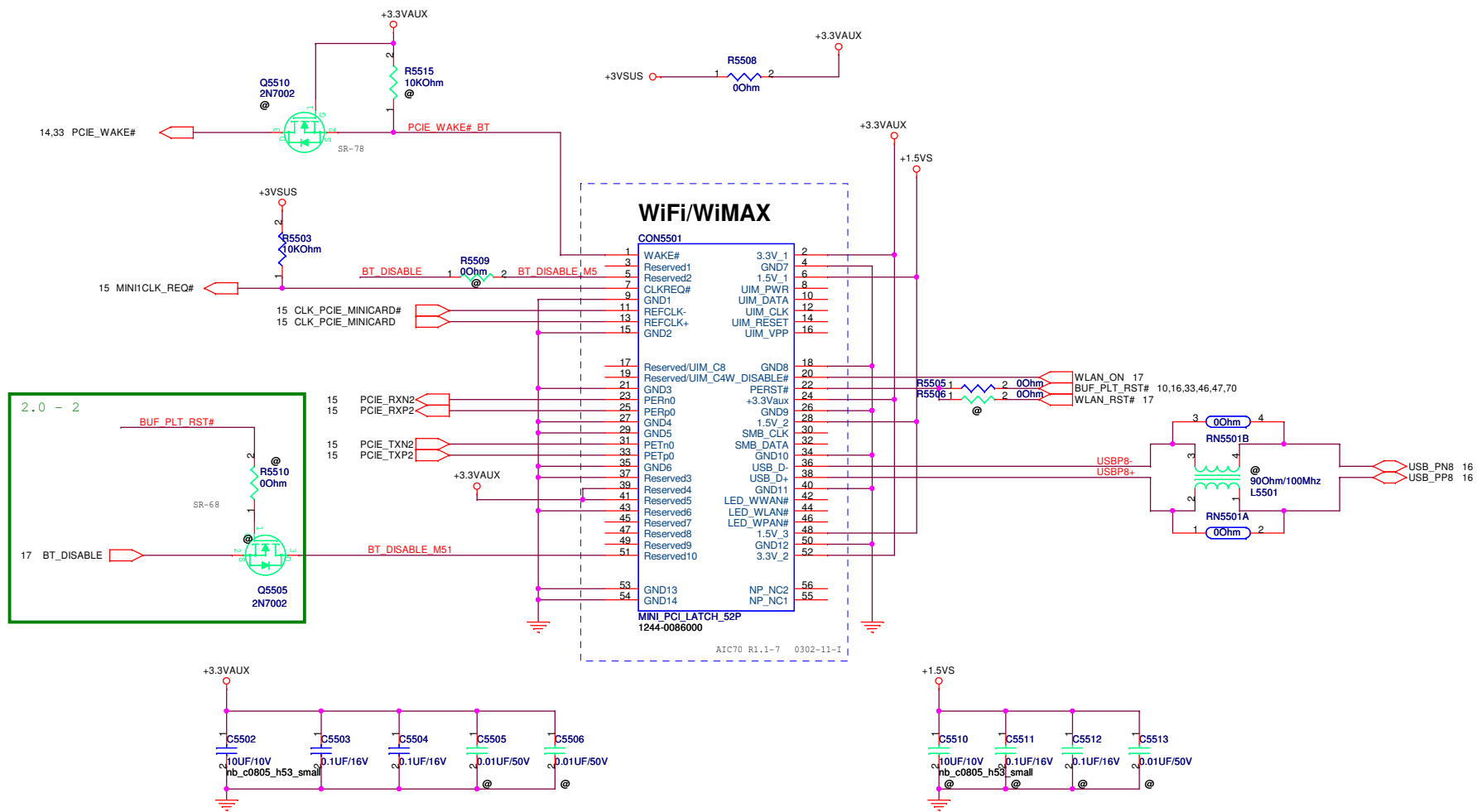
A

A

PEGATRON		Title : USB3.0 uPD720200	
BG11HW1		Engineer: <i>Johnson Huang</i>	
Size	Project Name	Rev	
C	AIC70	2.0	
Date: <i>Wednesday, May 04, 2011</i>		Sheet	53 of 77



PEGATRON		Title : PCIE NEW CARD	
BU1-RD Div.1-HW RD Dept.1		Engineer: Johnson Huang	
Size	Project Name		Rev
Custom	AIC70		2.0
Date: Wednesday, May 04, 2011		Sheet	54 of 77





PEGATRON		Title : MINICARD (WWAN)	
BU1-RD Div.1-HW RD Dept.1		Engineer:	
Size	Project Name		Rev
Custom			2.0
Date: Wednesday, May 04, 2011		Sheet	56 of 77

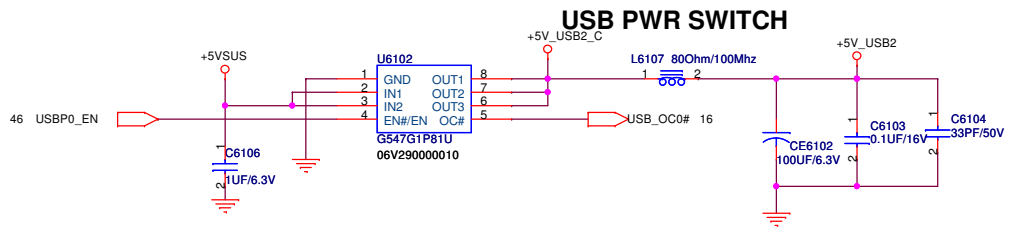


PEGATRON Title : **MINICARD (WUSB /UPCONVERT)**

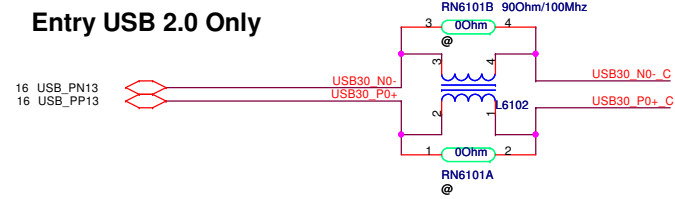
BU1-RD Div.1-HW RD Dept.1 Engineer: **Johnson Huang**

Size	Project Name	Rev
Custom	AIC70	2.0

Date: **Wednesday, May 04, 2011** Sheet **57** of **77**

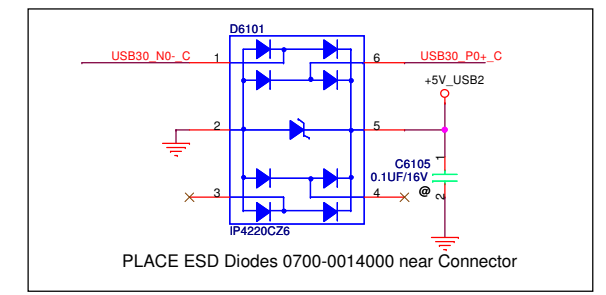
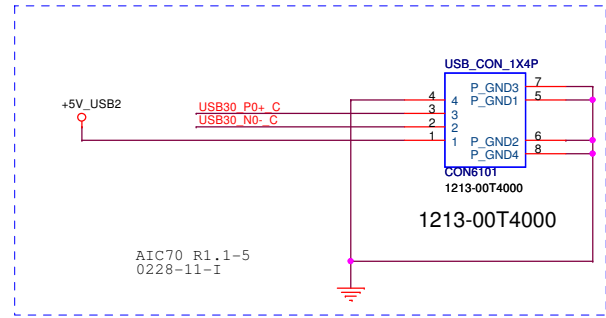


change USB power switch circuit SR-1 0120-11 SR-26 0124-11 SR-34 0125-11



Modify D6101, RN6101, RN6105, RN6106 SR-30 0125-11

USB 2.0

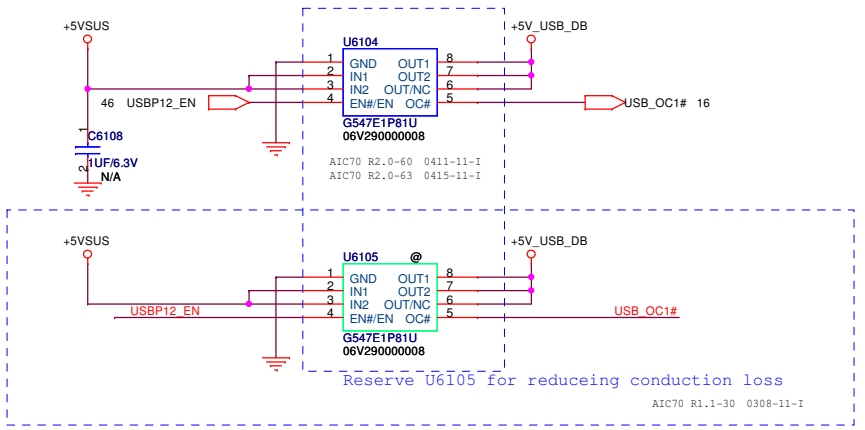


USB Conn. for Entry colay HDMI USB 2.0

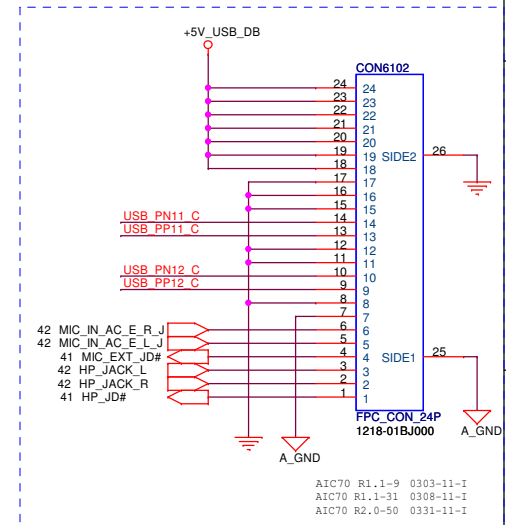
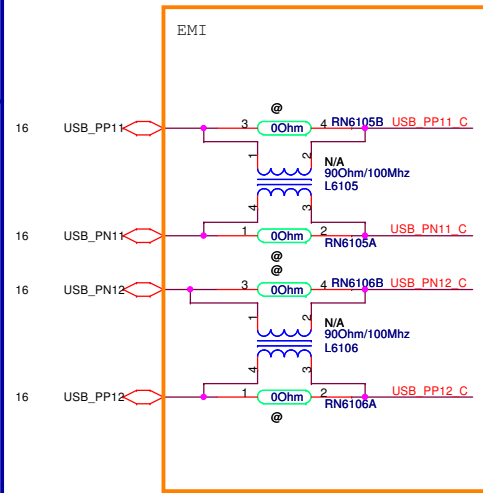
Remove USB_9 (HDMI) SR-21 0124-11

USB Power Switch for USB DB Main

change USB power switch circuit SR-26 0124-12 SR-38 0125-13



AUDIO BOARD/w USB2.0 x2



PEGATRON Title : USB PORTS/eSATA
 BU-1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang
 Size Custom Project Name AIC70 Rev 2.0
 Date: Wednesday, May 04, 2011 Sheet 61 of 77

TouchPanel CON

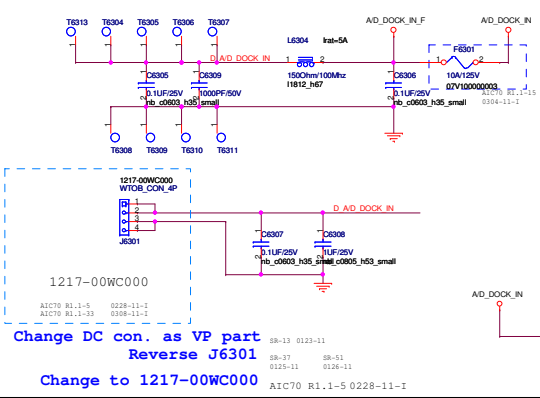
Camera Module CON

B/T MODULE

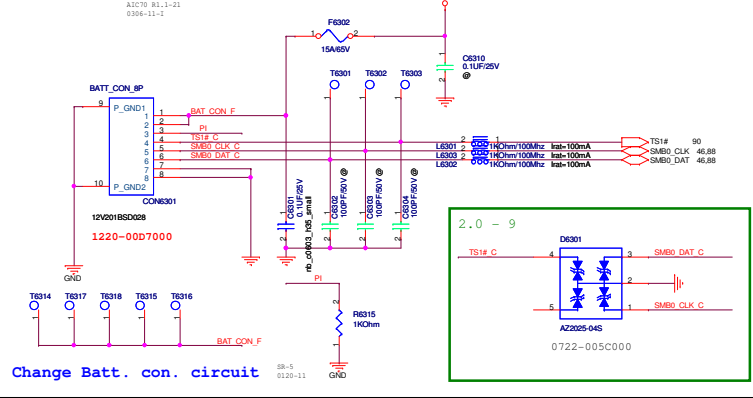
FELICA MODULE

PEGATRON		Title : <i>Camera/ BT/ FL CONN</i>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Johnson Huang</i>	
Size Custom	Project Name AIC70	Date: <i>Wednesday, May 04, 2011</i>	Rev 2.0
		Sheet	62 of 77

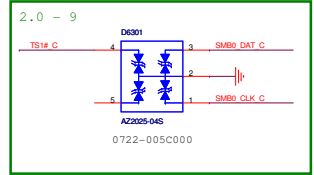
DC IN



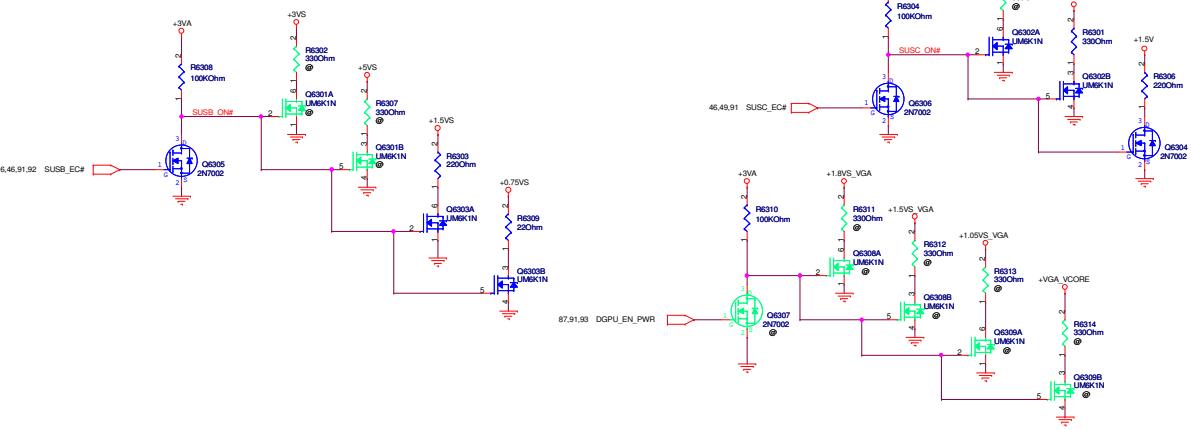
Battery Connector 17"



Remove 15" Battery connector



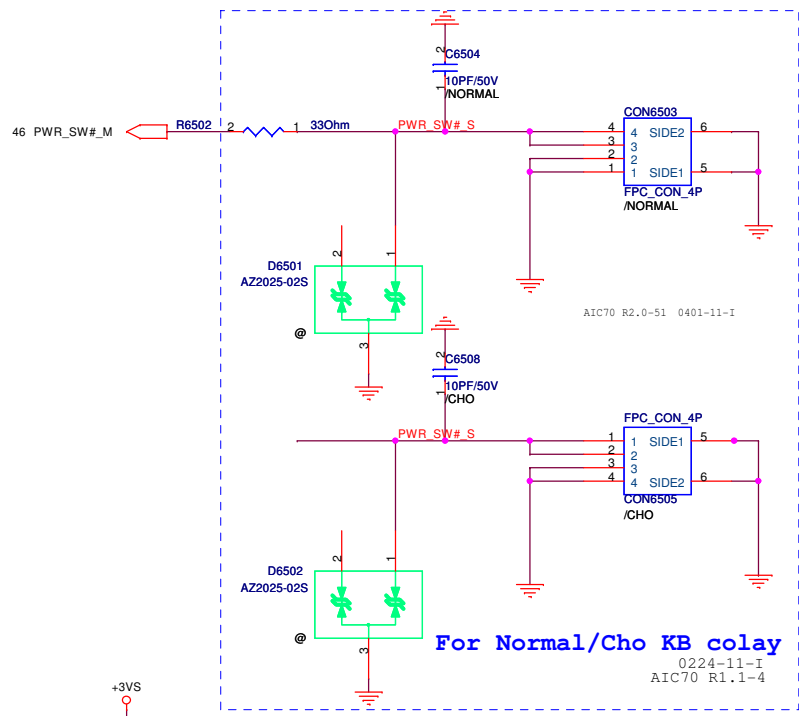
Discharge Circuit



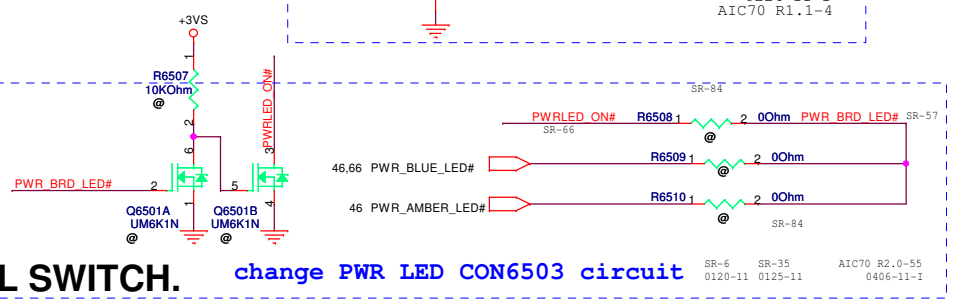
PAGATRON		Title : DC-IN DISCHARGE	
BUH-FD Dlx-1+HW FFD Dept.1		Engineer: Johnson Huang	
Size	Project Name	Rev	
Custom	AIC70	2.0	
Date: Wednesday, May 04, 2011	Sheet	65	of 77

Notes:
BRAIDWOOD right angled Connector (1.8V keyed)
Compatible BRAIDWOOD Modules
1.8V Mobile NVM 4GB 31.60mm x21.5mm
1.8V Mobile NVM 8GB 31.60mm x 21.5mm
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

PEGATRON Title : <i>NVM</i>		
BU1-RD Div.1-HW RD Dept.1 Engineer: <i>Johnson Huang</i>		
Size Custom	Project Name AIC70	Rev 2.0
Date: <i>Wednesday, May 04, 2011</i>		Sheet 64 of 77



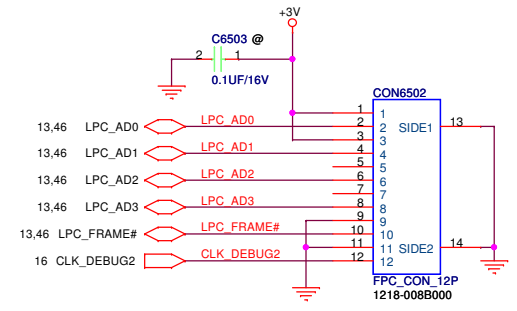
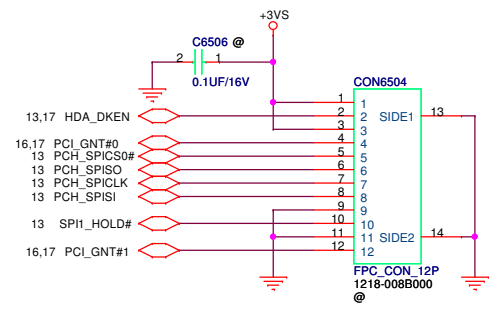
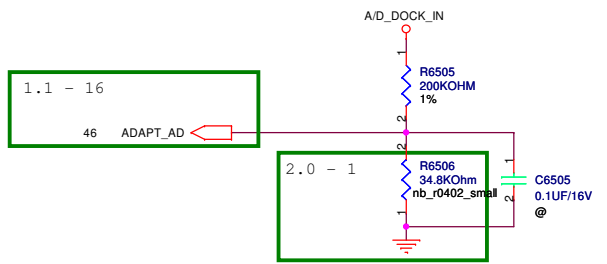
MODEM MODULE



KILL SWITCH. change PWR LED CON6503 circuit

DEBUG CARD CONN.

ADAPTOR VOLTAGE DETECTOR.



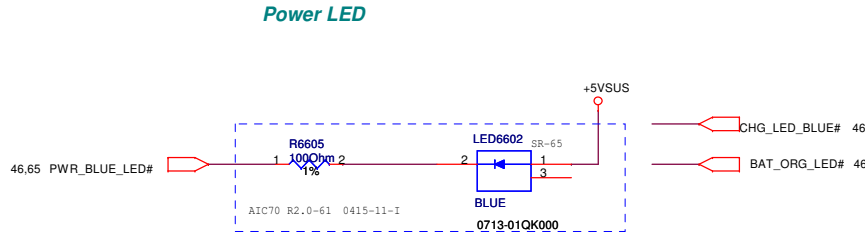
LED (Main)

Left → Right

- DC-IN
- Power
- Main Battery
- HDD/ODD
- Bridge Media
- WIFI

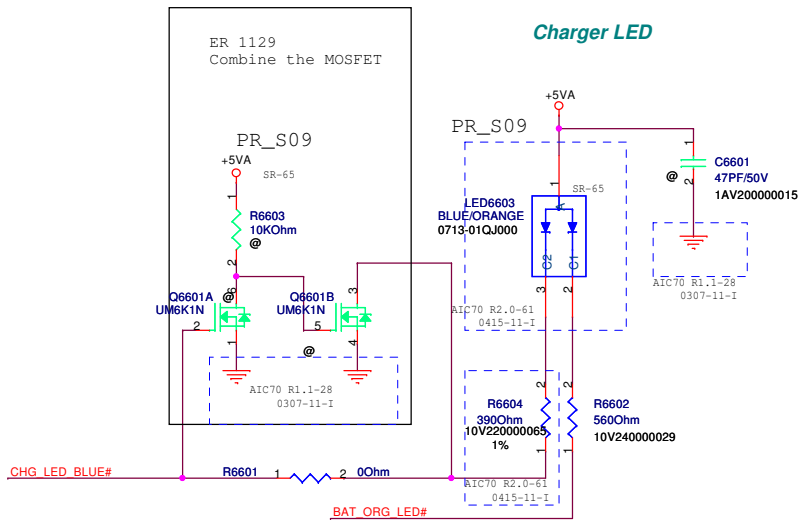
White White Amber (Blink) White Amber (Blink) White White Amber

Battery



Power LED

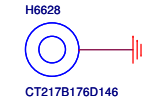
Charger LED



Remove LED circuit SR-18 0124-11

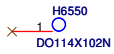
Modify LED circuit SR-28 0124-11 SR-39 0125-11

WLAN NUT



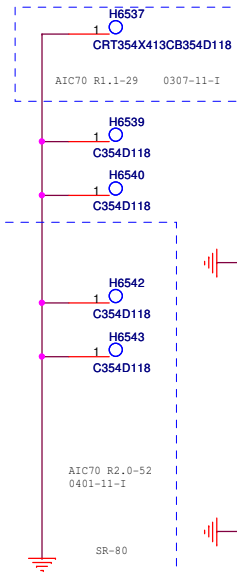
Fix hole

Detail C



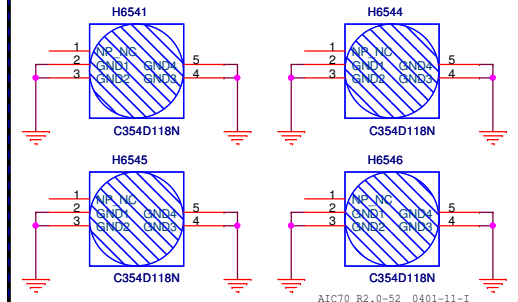
PCH Local Side Symbol

Screw Ax10

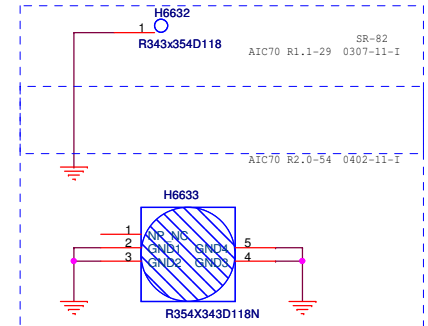


Screw Px4 CPU

Screw Cx2 VGA



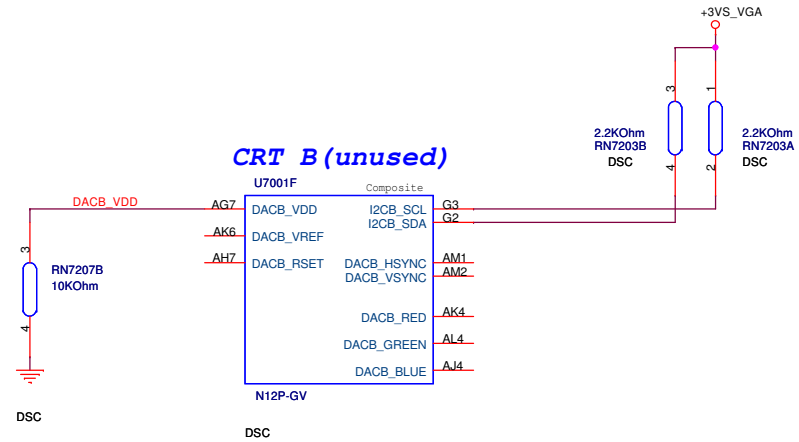
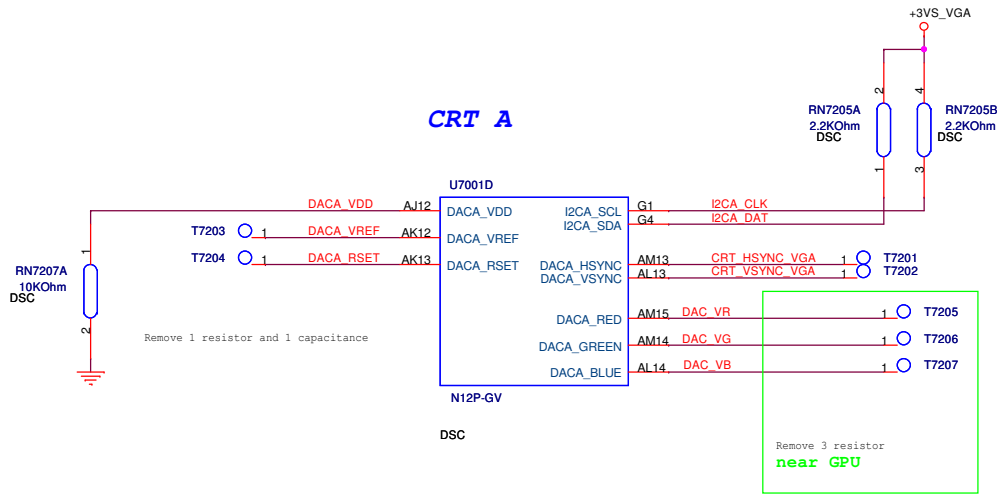
Screw Fx2



PEGATRON Title : LED/ CIR/ FW SCREW
 BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang
 Size Custom Project Name AIC70 Rev 2.0
 Date: Wednesday, May 04, 2011 Sheet 66 of 77

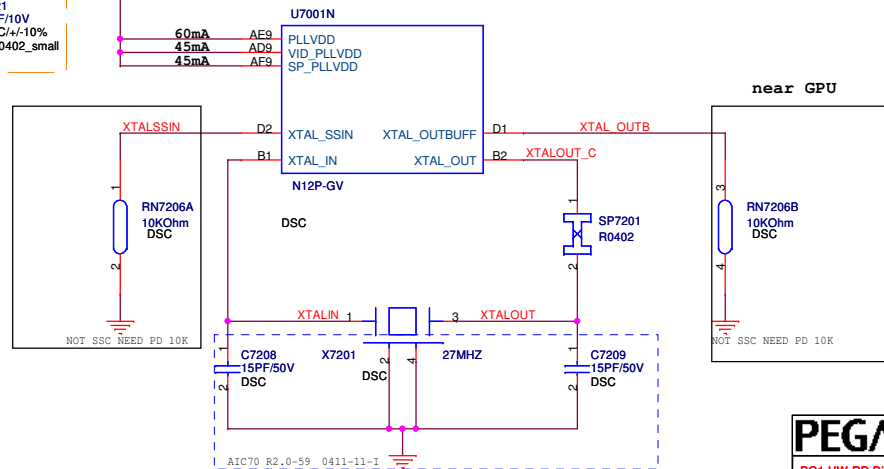
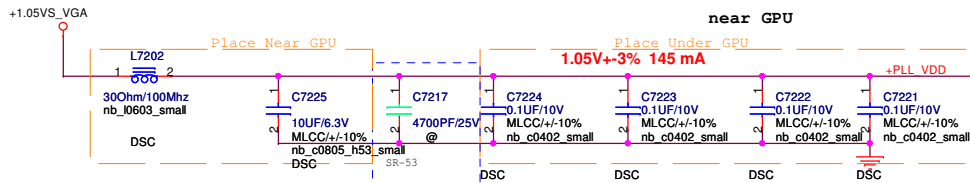


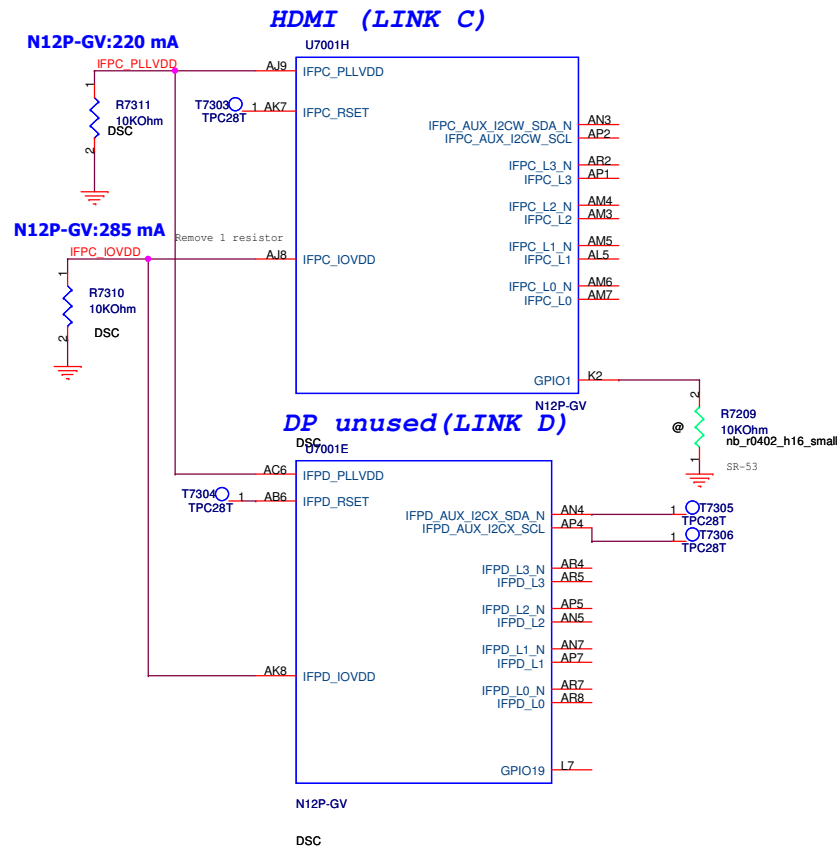
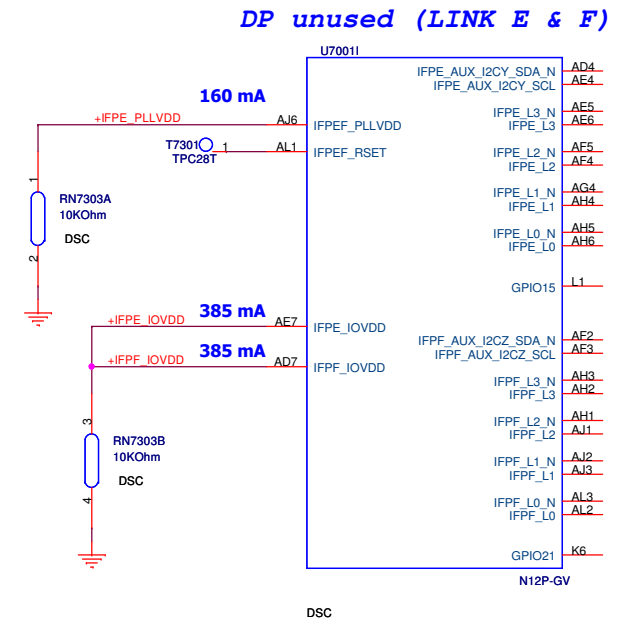
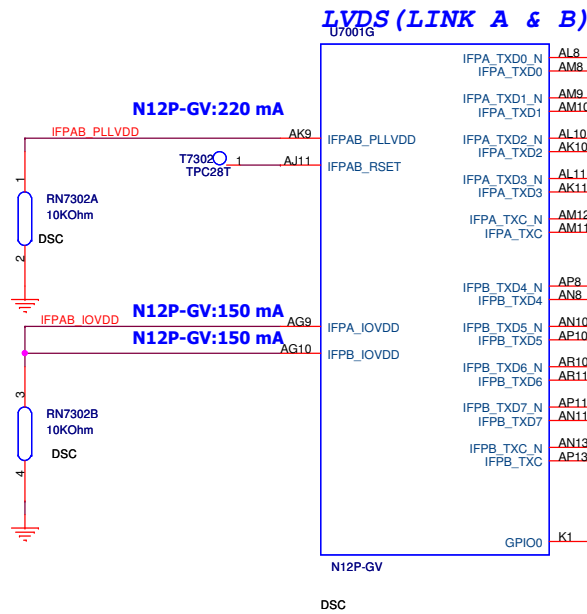
PEGATRON		Title : <i>G-Sensor TSH35TR</i>	
<i>BU1-RD Div.1+HW RD Dept.1</i>		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
Custom			2.0
Date:	<i>Wednesday, May 04, 2011</i>		Sheet 69 of 77



XTAL_IN, XTAL_OUT
 3.3V tolerance

correspondent BGA balls must be 12mils and 16 mil wide





IFP*	A	B	C	D	E	F
TURKEY	LVDS A	LVDS B	HDMI	unused		



PEGATRON Title : **LVDS, HDMI**

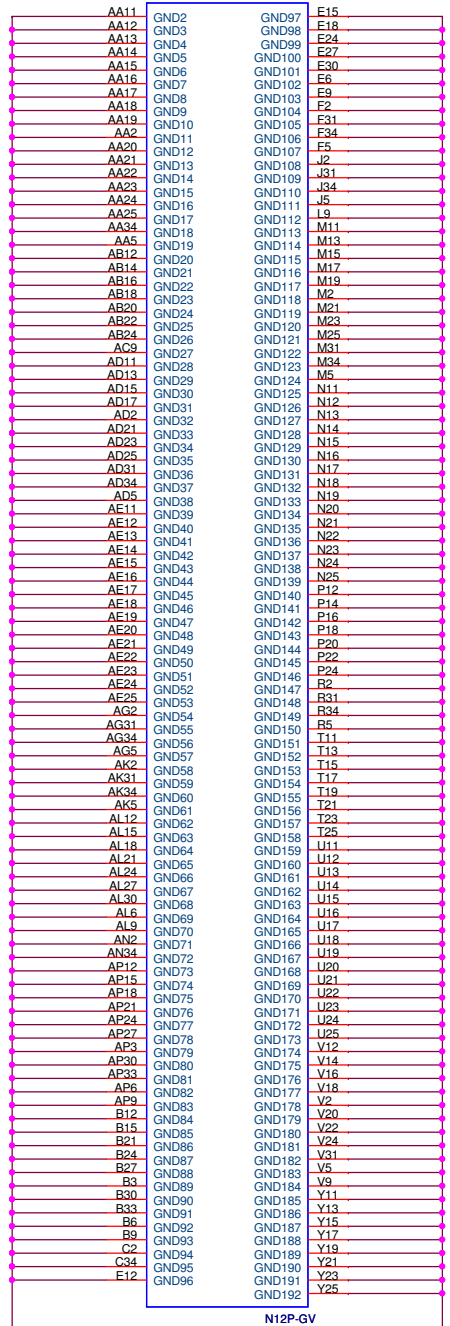
BG1-HW RD Div.2-NB RD Dept.5 Engineer: **Johnson Huang**

Size	Project Name	Rev
Custom	AIC70	2.0

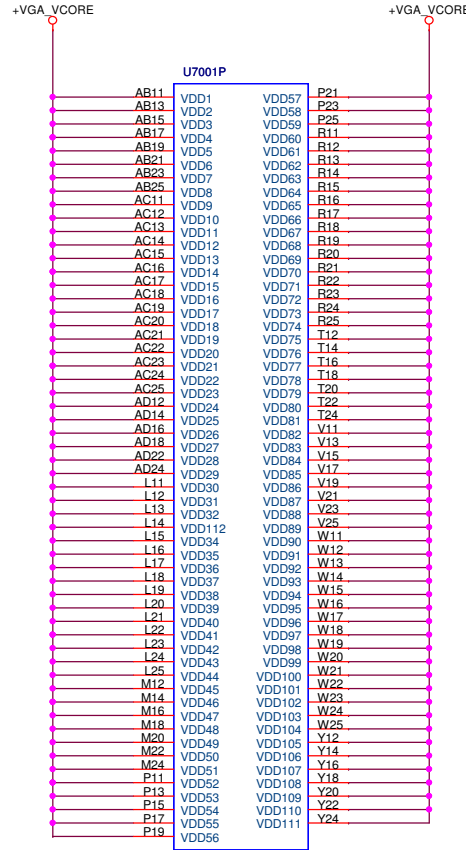
Date: **Wednesday, May 04, 2011** Sheet **73** of **77**

GND

U7001O



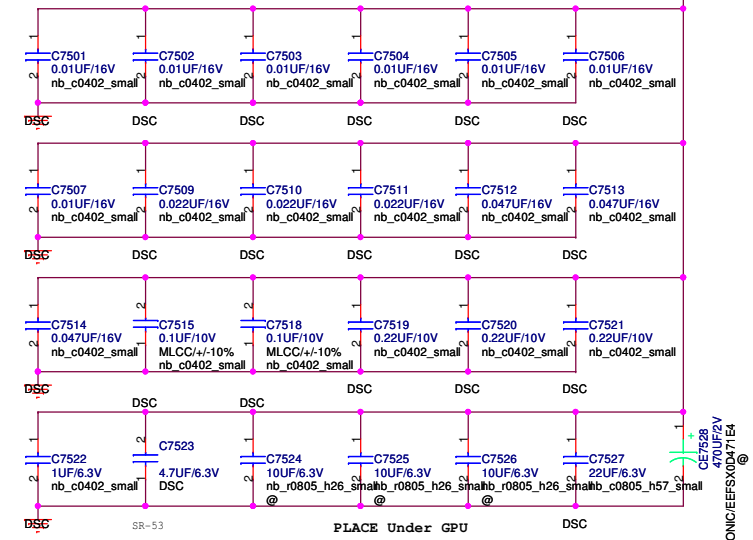
VAG_VCORE



N12P-GV

DSC

20.3 A



63.87 +VGA_VCORE ← +VGA_VCORE

PEGATRON Title : GPU PWR/GND

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 75 of 77

VRAM CH A

TOP SIDE

BOT SIDE

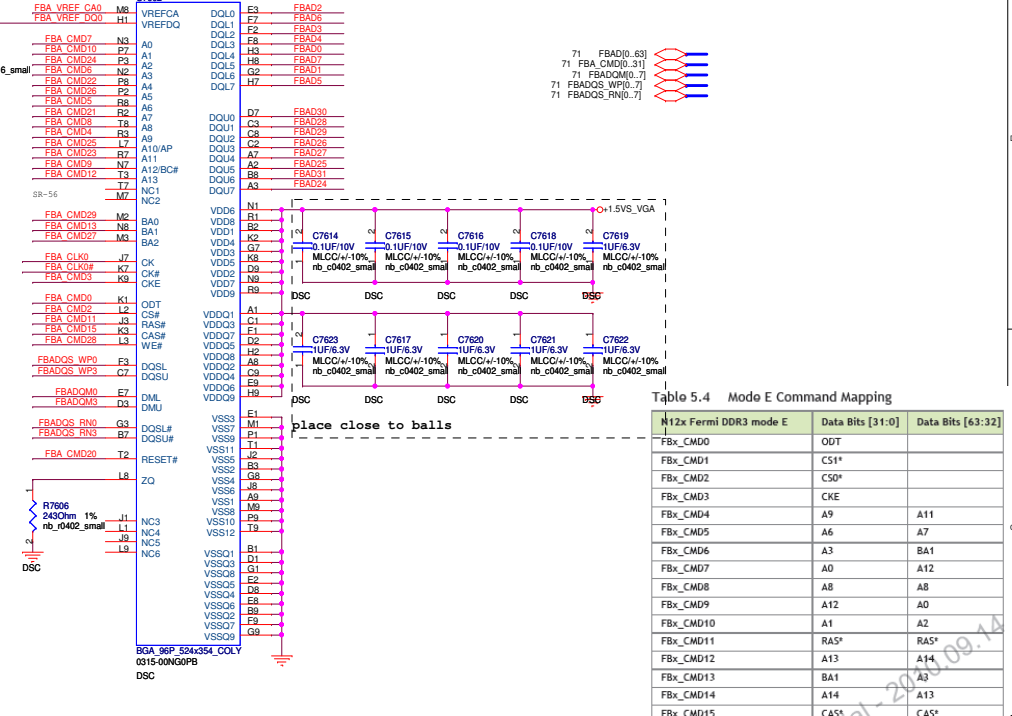
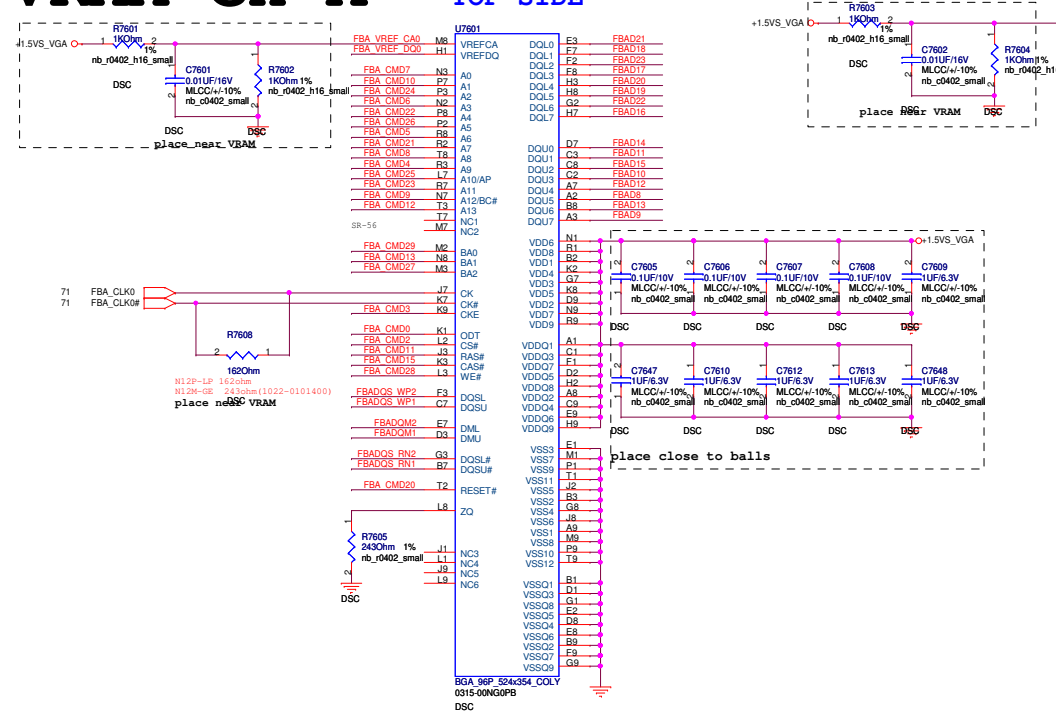
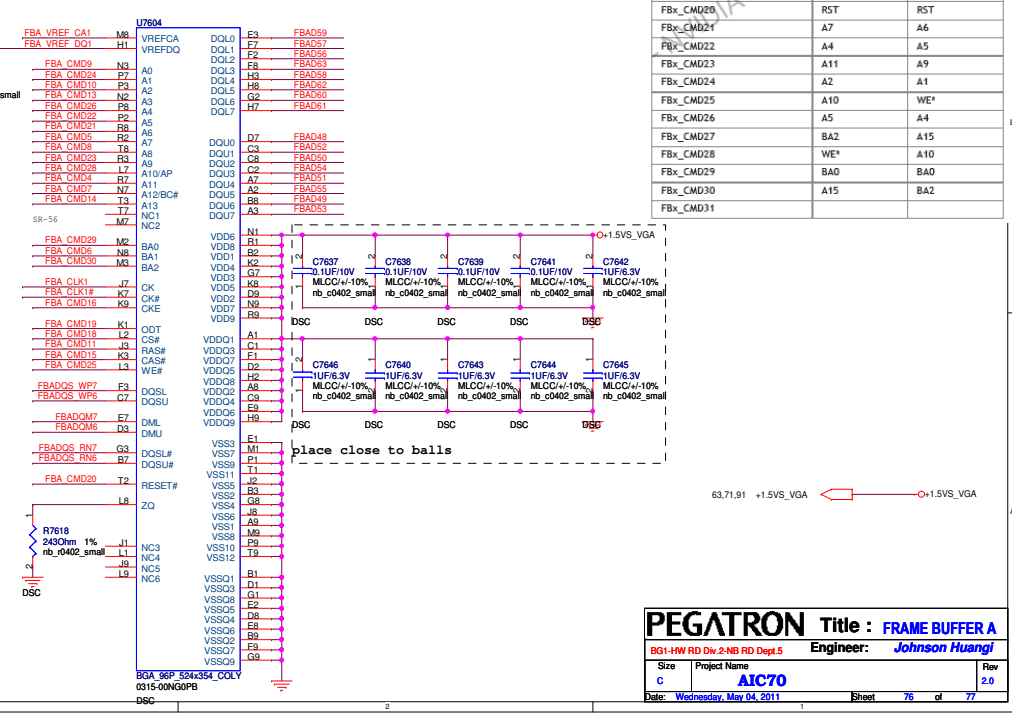
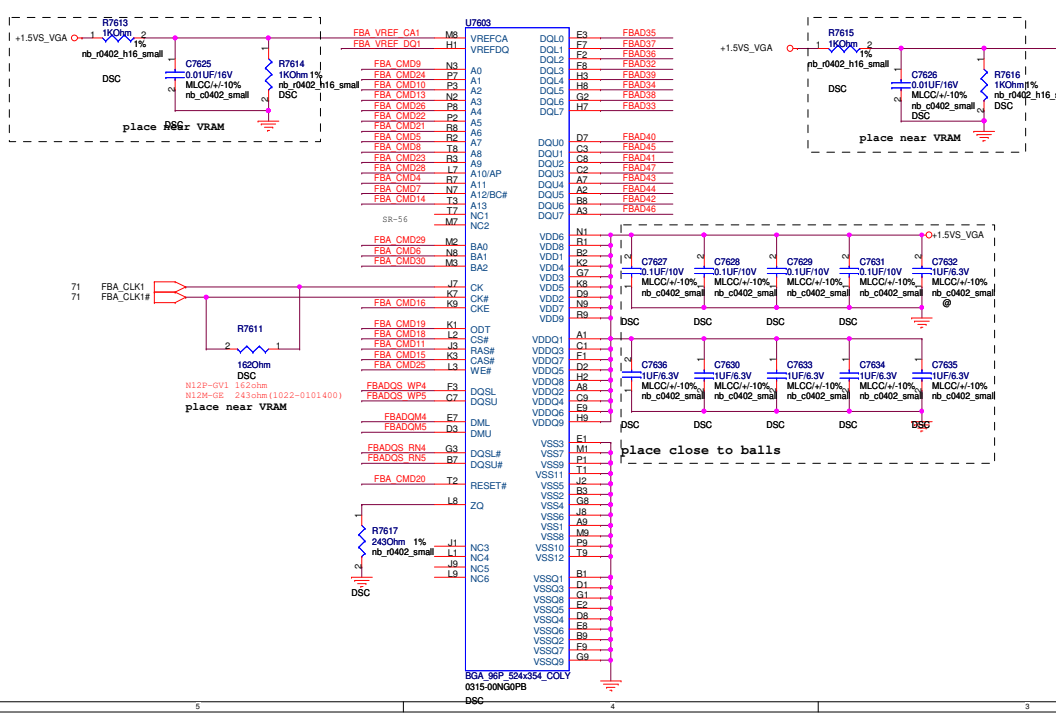


Table 5.4 Mode E Command Mapping

11x2x Fermi DDR3 mode E	Data Bits [31:0]	Data Bits [63:32]
Fbx_CMD0	ODT	
Fbx_CMD1	CS1*	
Fbx_CMD2	C50*	
Fbx_CMD3	CKE	
Fbx_CMD4	A9	A11
Fbx_CMD5	A6	A7
Fbx_CMD6	A3	BA1
Fbx_CMD7	A0	A12
Fbx_CMD8	A8	A8
Fbx_CMD9	A12	A0
Fbx_CMD10	A1	A2
Fbx_CMD11	RAS*	RAS*
Fbx_CMD12	A13	A14
Fbx_CMD13	BA1	A3
Fbx_CMD14	A14	A13
Fbx_CMD15	CAS*	CAS*
Fbx_CMD16	CKE	
Fbx_CMD17	CS1*	
Fbx_CMD18	C50*	
Fbx_CMD19	ODT	
Fbx_CMD20	RST	RST
Fbx_CMD21	A7	A6
Fbx_CMD22	A4	A5
Fbx_CMD23	A11	A9
Fbx_CMD24	A2	A1
Fbx_CMD25	A10	WE*
Fbx_CMD26	A5	A4
Fbx_CMD27	BA2	A15
Fbx_CMD28	WE*	A10
Fbx_CMD29	BA0	BA0
Fbx_CMD30	A15	BA2
Fbx_CMD31		

TOP SIDE

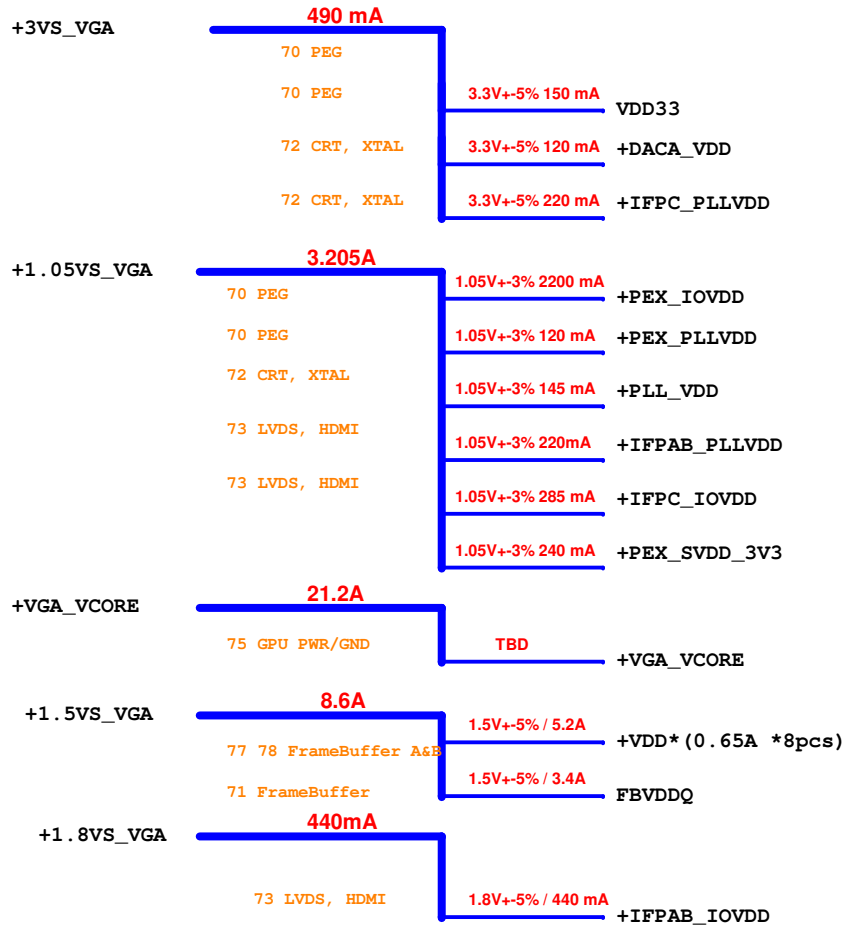
BOT SIDE



PEGATRON Title: **FRAME BUFFER A**
 BGI-HW RD Dw.2-NB RD Dept.5 Engineer: **Johnson Huang!**

Size	Project Name	Rev
	AIC70	2.0
Date: Wednesday, May 04, 2011	Sheet	76 of 77

Del B channel VRAM * 4 circuit SR-10
0121-11



N12P-LP Total:40W (w/VRAM)

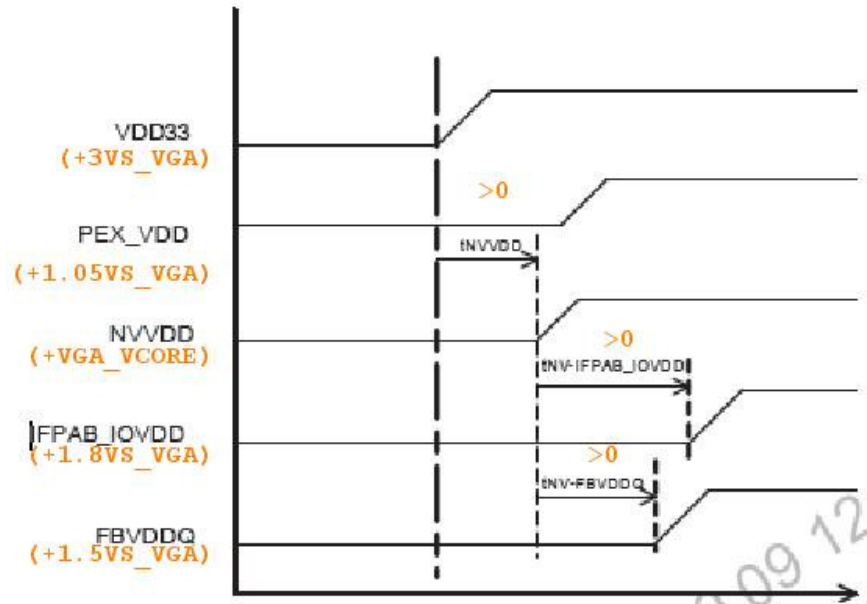
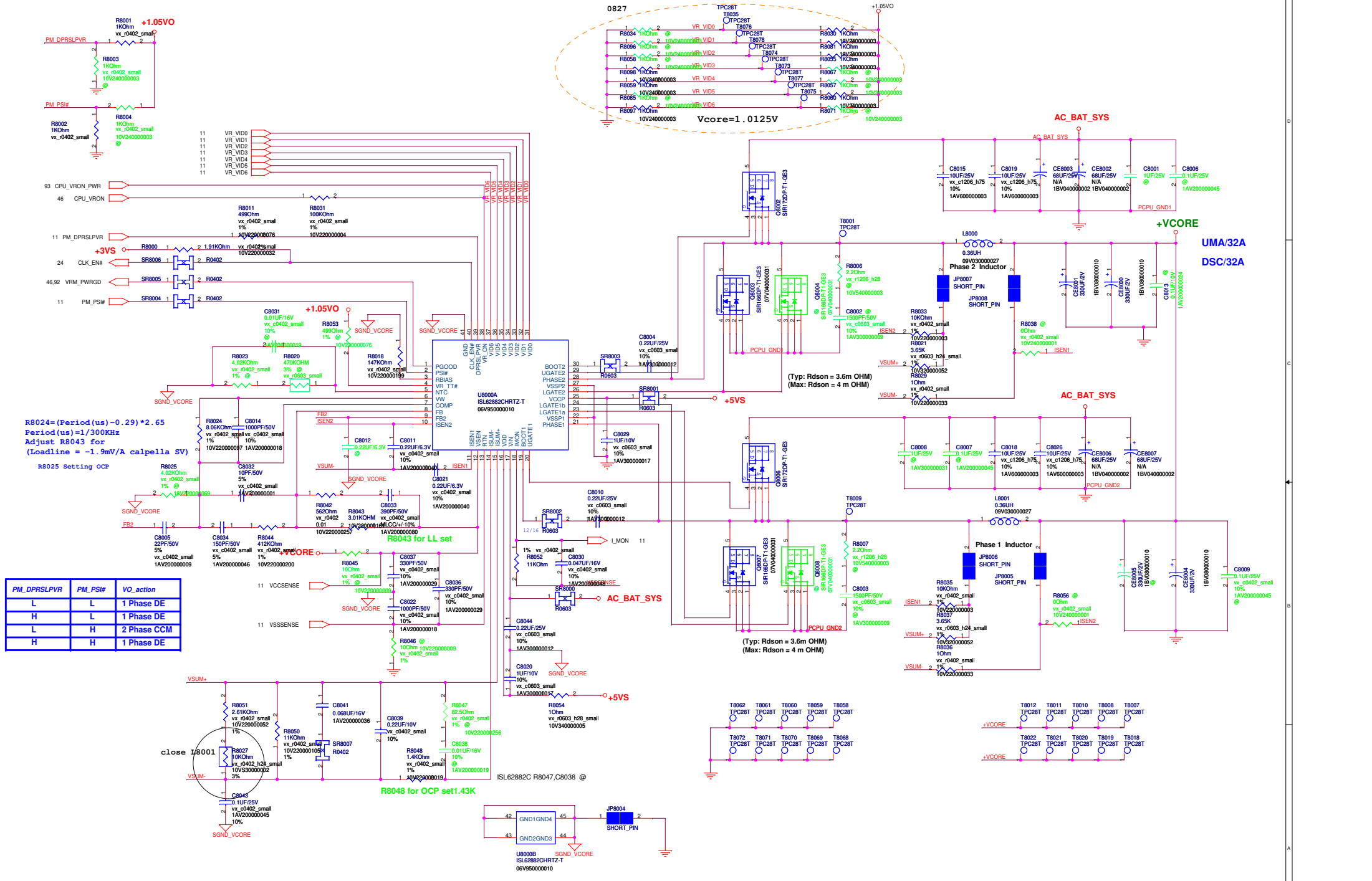


Figure 3.20 Recommended Power On Sequencing Order

Power Up Sequence :
+3VS_VGA -> +1.05VS_VGA -> +VGA_VCORE -> +1.5VS_VGA -> +1.8VS_VGA

Power Down Sequence :
+1.8VS_VGA -> +1.5VS_VGA -> +VGA_VCORE -> 1.05VS_VGA -> +3VS_VGA

according to Page 63, DG-05093-001_v02



R8024 = (Period(us) - 0.29) * 2.65
 Period(us) = 1/300KHz
 Adjust R8043 for
 (Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

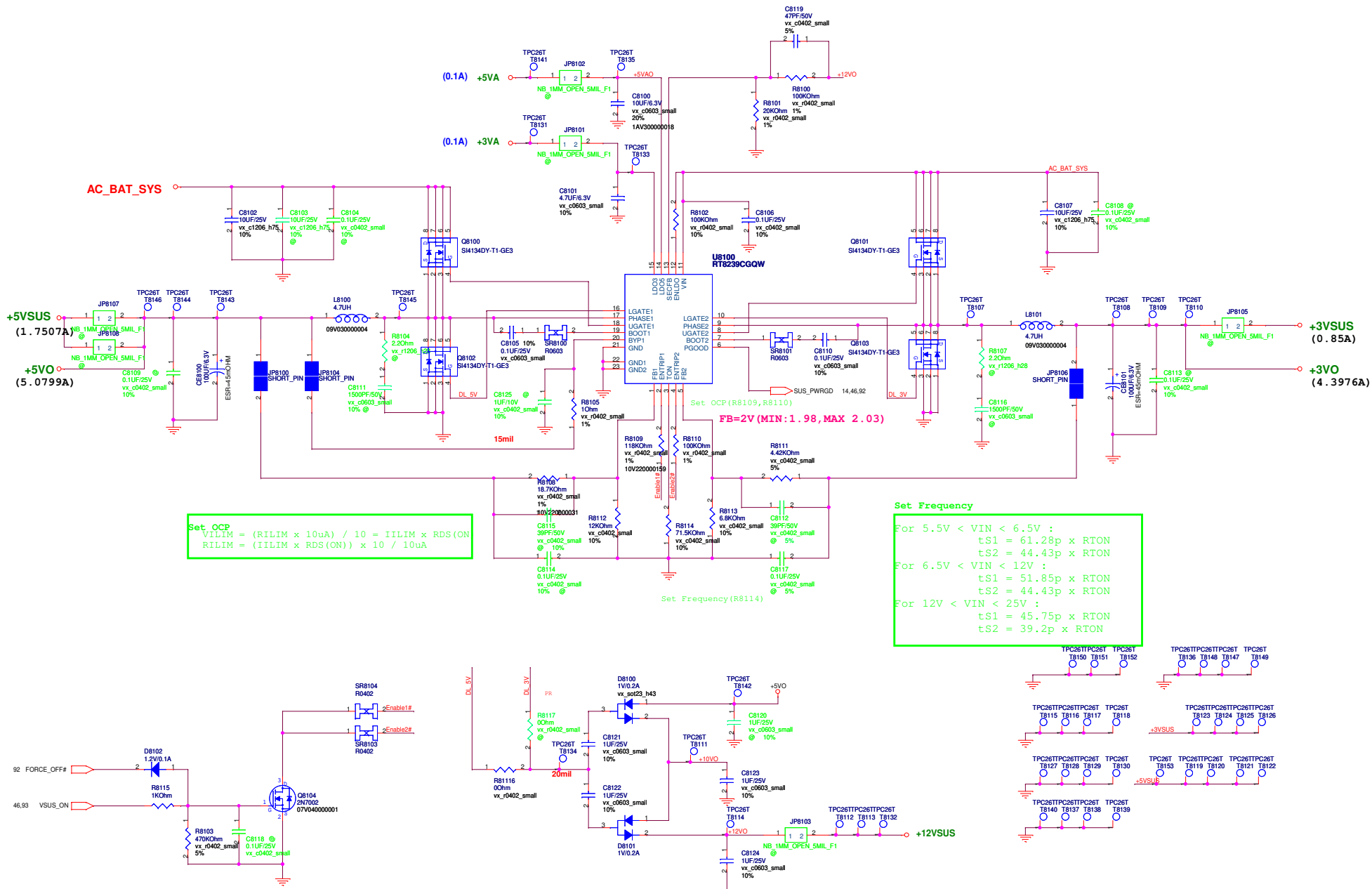
PM DPRSLPVR	PM_PSI#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

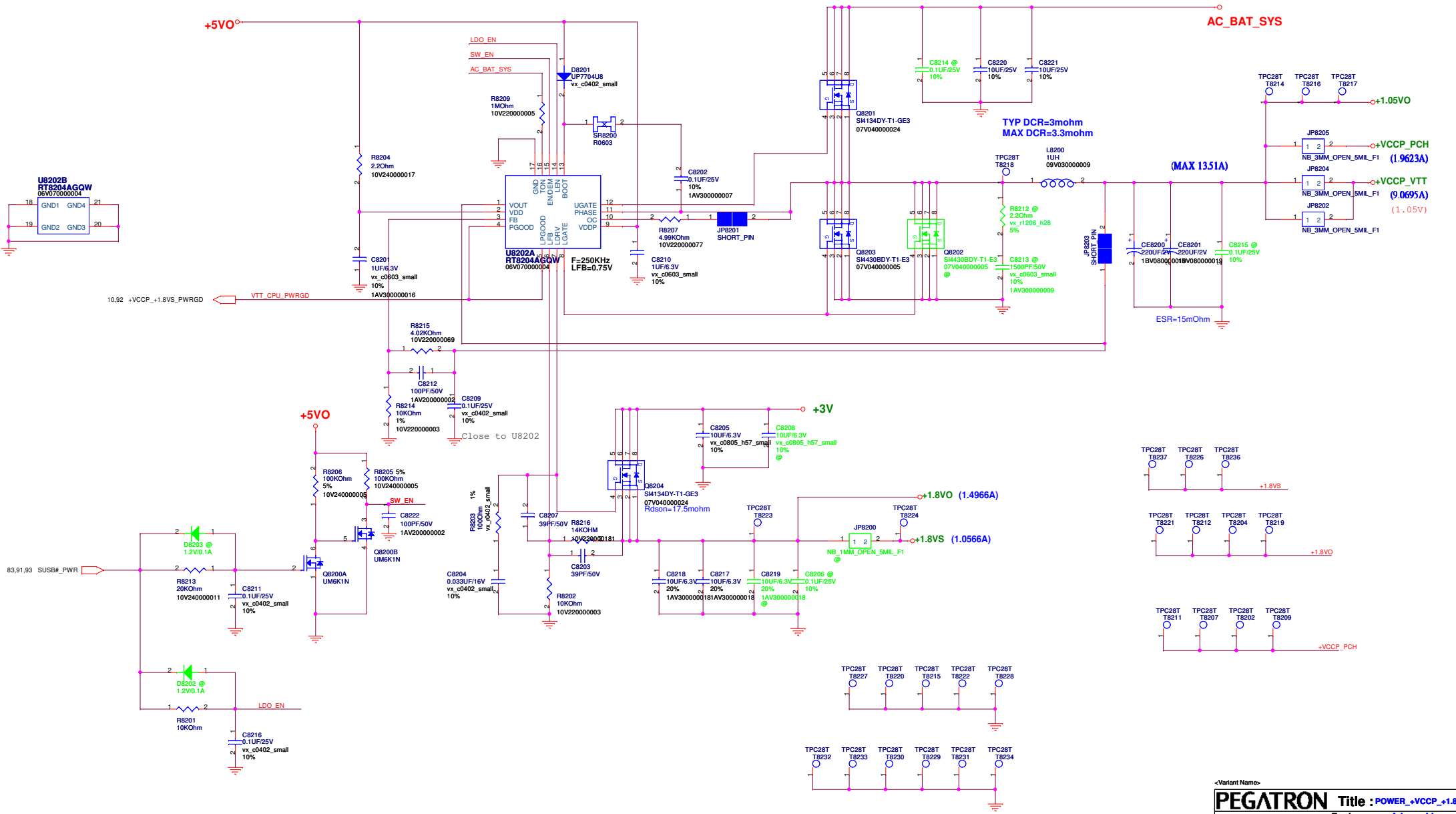
close I8001

R8048 for OCP set1.43K

(Typ: Rds(on) = 3.6m OHM)
 (Max: Rds(on) = 4 m OHM)

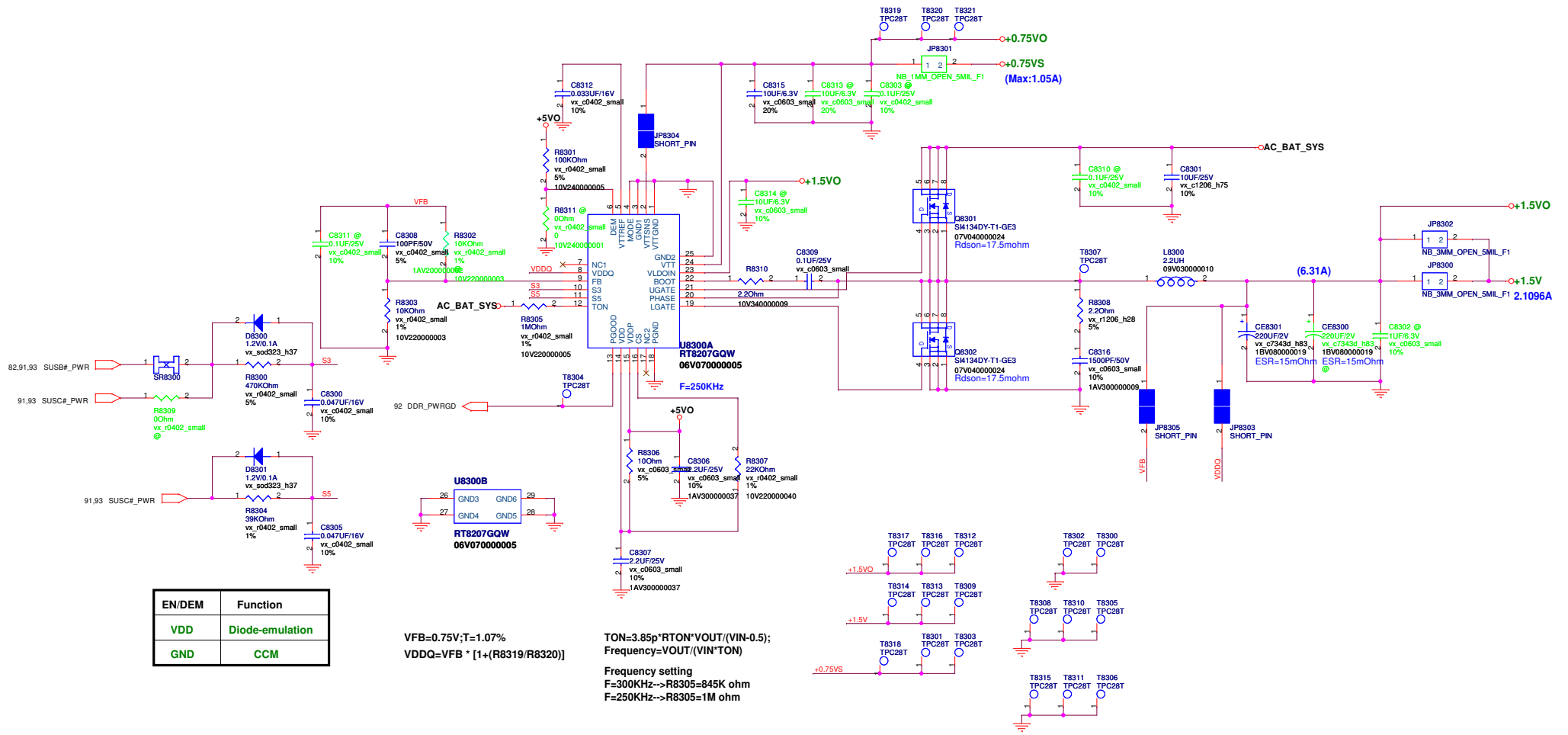
(Typ: Rds(on) = 3.6m OHM)
 (Max: Rds(on) = 4 m OHM)





<Variant Name>

PEGATRON		Title : POWER_+VCCP_+1.8VS	
		Engineer: Adams_Lin	
Size	Project Name		Rev
Custom	AIC70		1.0
Date: Wednesday, May 04, 2011		Sheet	82 of 77



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

$VFB=0.75V; T=1.07\%$
 $VDDQ=VFB * [1+(R8319/R8320)]$

$TON=3.85p \cdot RTON \cdot VOUT / (VIN-0.5);$
 $Frequency=VOUT / (VIN \cdot TON)$

Frequency setting
 $F=300KHz \rightarrow R8305=845K \text{ ohm}$
 $F=250KHz \rightarrow R8305=1M \text{ ohm}$

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

PEGATRON		Title : POWER_N/A	
		Engineer: Adams_Lin	
Size Custom	Project Name AIC70	Rev 1.0	
Date: Wednesday, May 04, 2011		Sheet	84 of 77

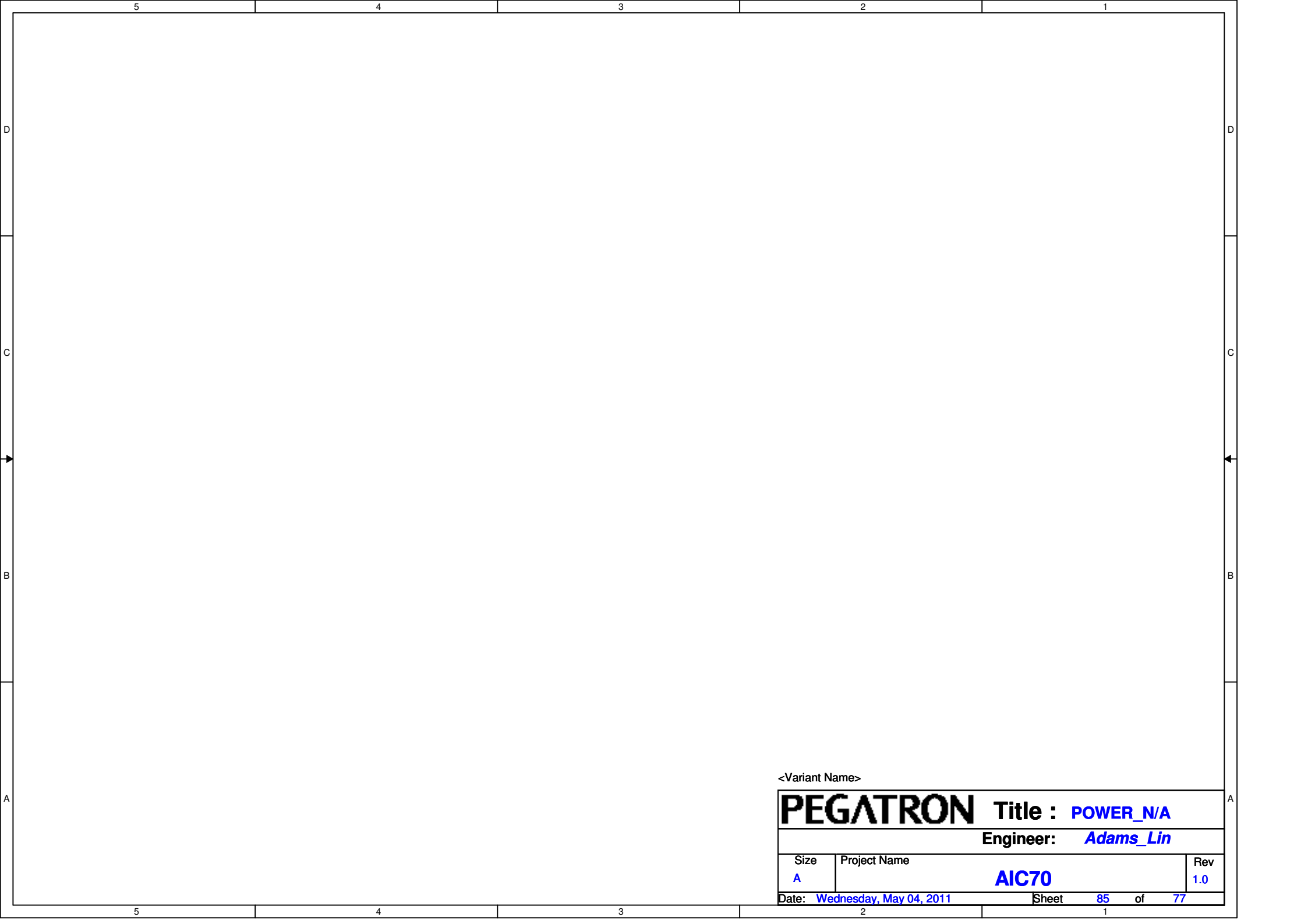
5

4

3

2

1

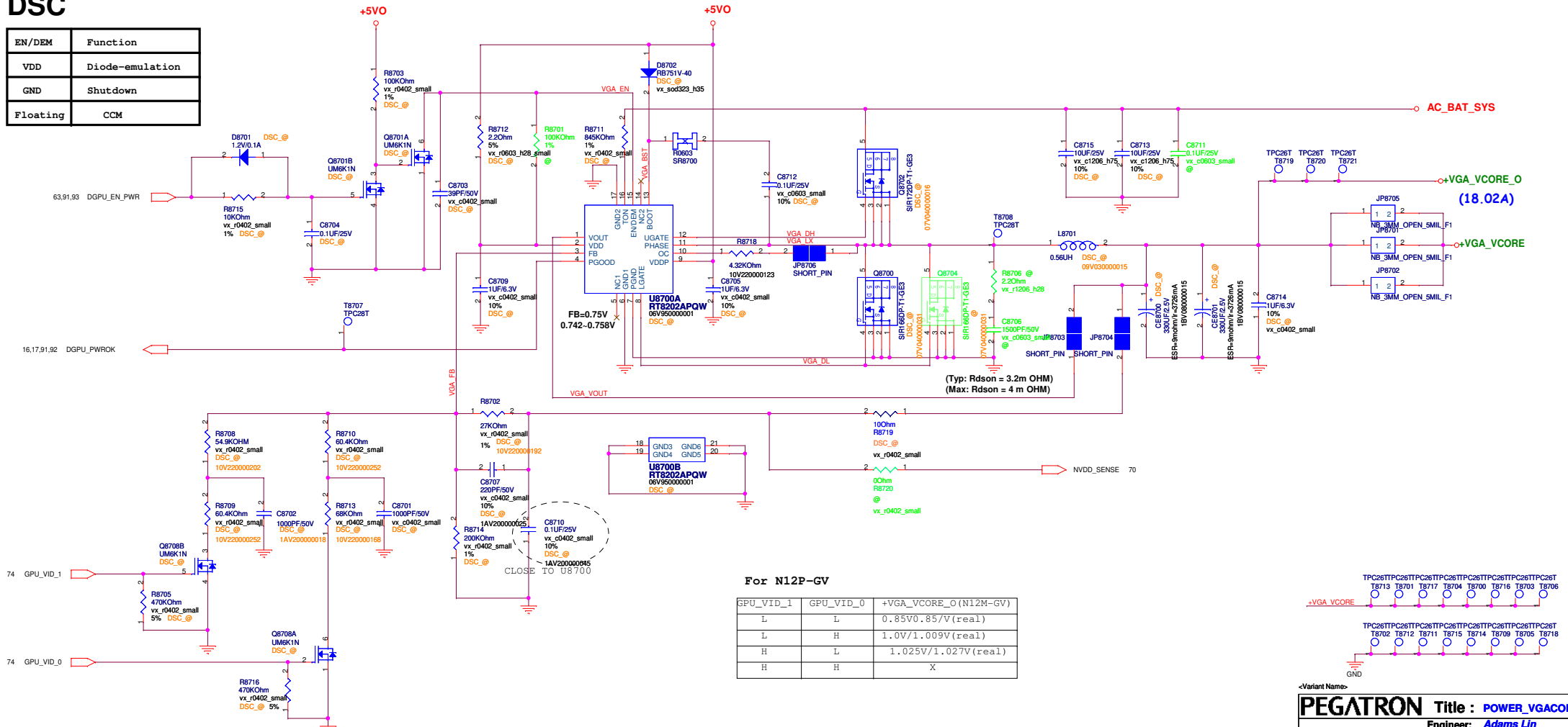


<Variant Name>

PEGATRON			Title : POWER_N/A		
			Engineer: Adams_Lin		
Size	Project Name			Rev	
A	AIC70			1.0	
Date: Wednesday, May 04, 2011			Sheet 85 of 77		

DSC

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



For N12P-GV

GPU_VID_1	GPU_VID_0	+VGA_VCORE_O (N12M-GV)
L	L	0.85V0, 85/V (real)
L	H	1.0V/1.009V (real)
H	L	1.025V/1.027V (real)
H	H	X



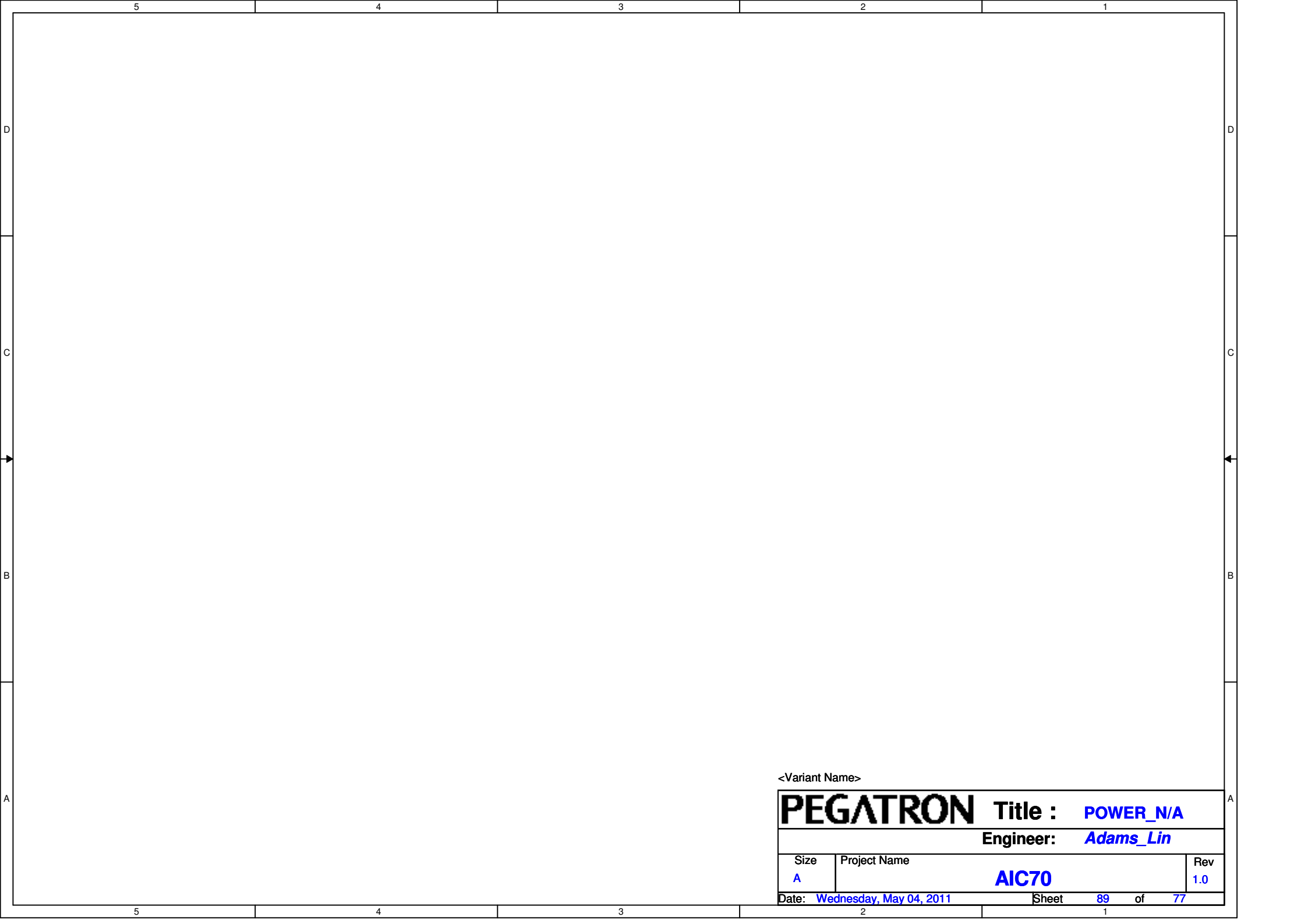
<Variant Name>

PEGATRON Title : **POWER_VGACORE**

Engineer: **Adams Lin**

Size	Project Name	Rev
Custom	AIC70	1.0

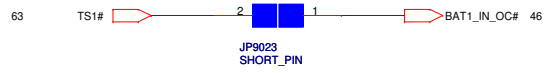
Date: **Wednesday, May 04, 2011** Sheet **87** of **77**



<Variant Name>

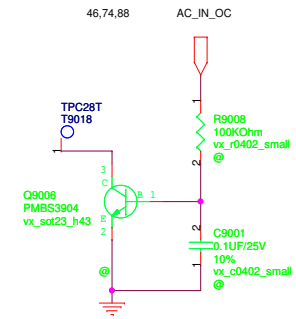
PEGATRON			Title :	POWER_N/A
			Engineer:	Adams_Lin
Size	Project Name			Rev
A	AIC70			1.0
Date: Wednesday, May 04, 2011			Sheet	89 of 77

BATTERY IN DETECT



ADAPTER IN DETECT

Use MAX17015 IC function to Cost down component

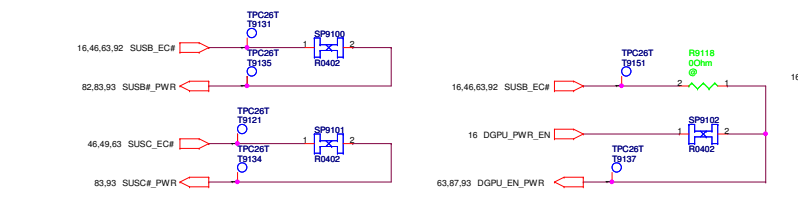
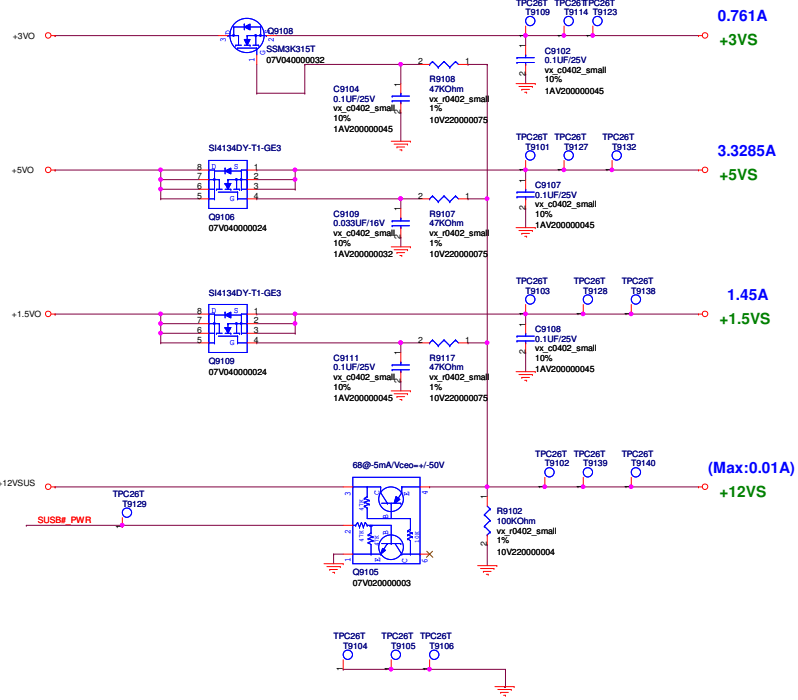


<Variant Name>

PEGATRON Title : **POWER_DETECT**
Engineer: **Adams_Lin**

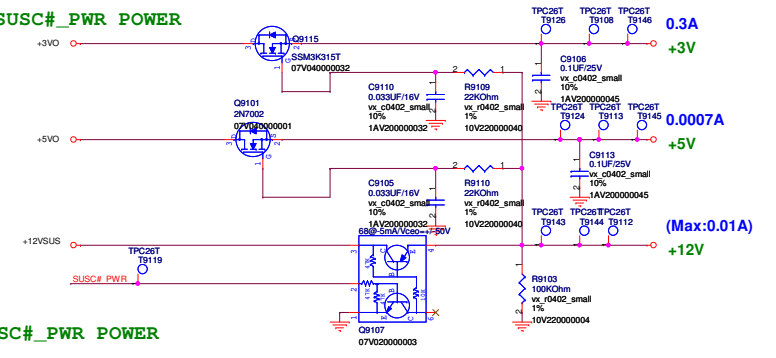
Size	Project Name	Rev
Custom	AIC70	1.0
Date: Wednesday, May 04, 2011		Sheet 90 of 77

SUSB#_PWR POWER

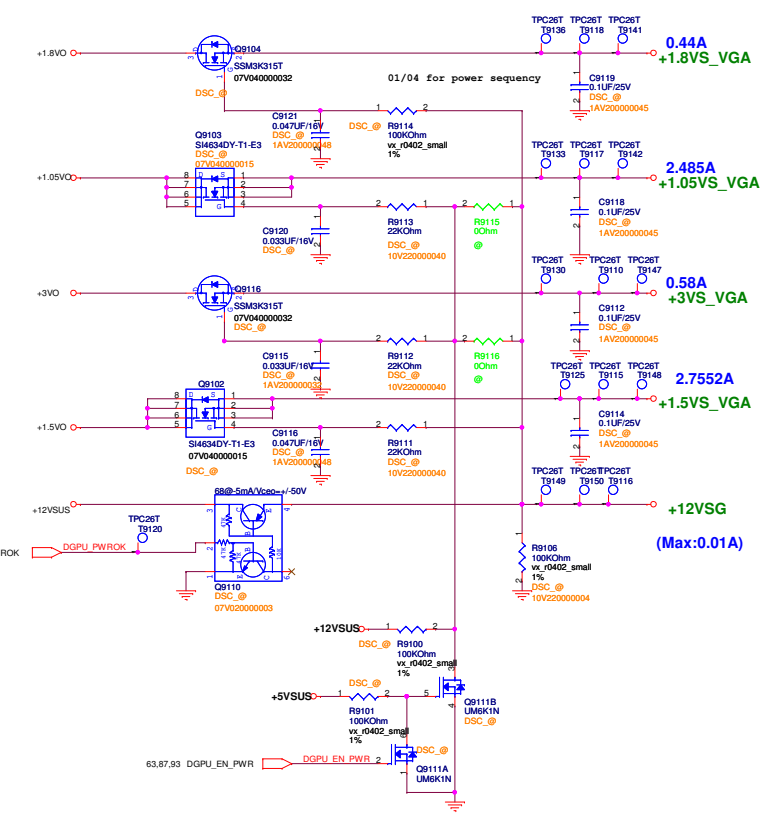


Ron = 41.5 mΩ (max) (RVS = 4.5 V)
 Ron = 27.6 mΩ (max) (RVS = 10 V)
 NOTE: +3V=0.3A(EE)+1.4978A(+3V Provide to 1.8V PWR)=1.7978A

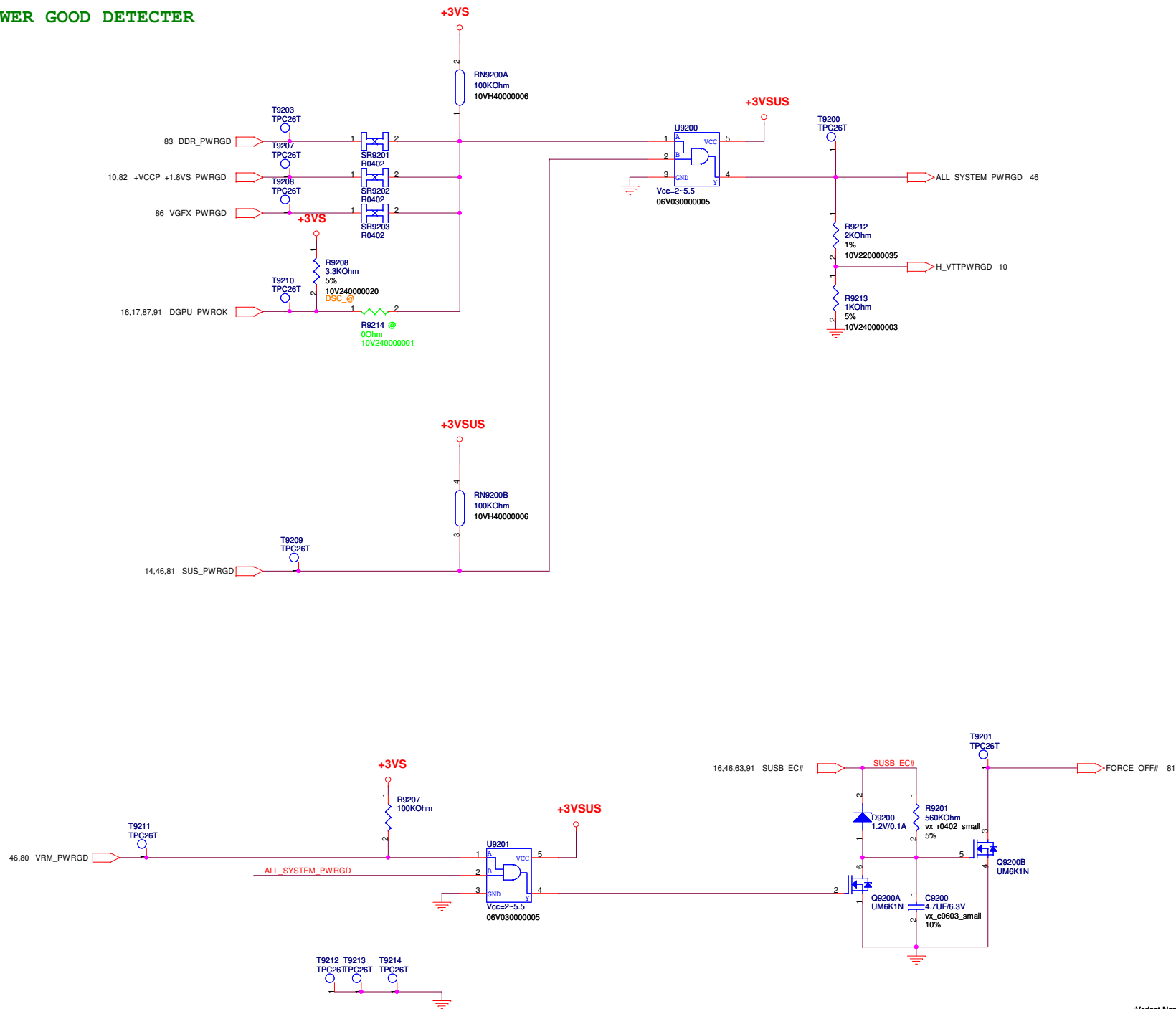
SUSC#_PWR POWER



DSC#_PWR POWER



POWER GOOD DETECTOR



AC_BAT_SYS ○ → AC_BAT_SYS 37,80,81,82,83,86,87,88
 BAT_CON ○ → BAT_CON 63,88
 BAT ○ → BAT 88

+5VA ○ → +5VA 42,49,66,81,88
 +3VA ○ → +3VA 13,18,46,48,63,81

+5VO ○ → +5VO 81,82,83,87,91
 +3VO ○ → +3VO 81,91
 +1.8VO ○ → +1.8VO 82,91
 +1.5VO ○ → +1.5VO 83,91
 +1.05VO ○ → +1.05VO 80,82,86,91
 +VGFX_CORE_O ○ → +VGFX_CORE_O 86
 +VGA_VCORE_O ○ → +VGA_VCORE_O 87
 +0.75VO ○ → +0.75VO 83

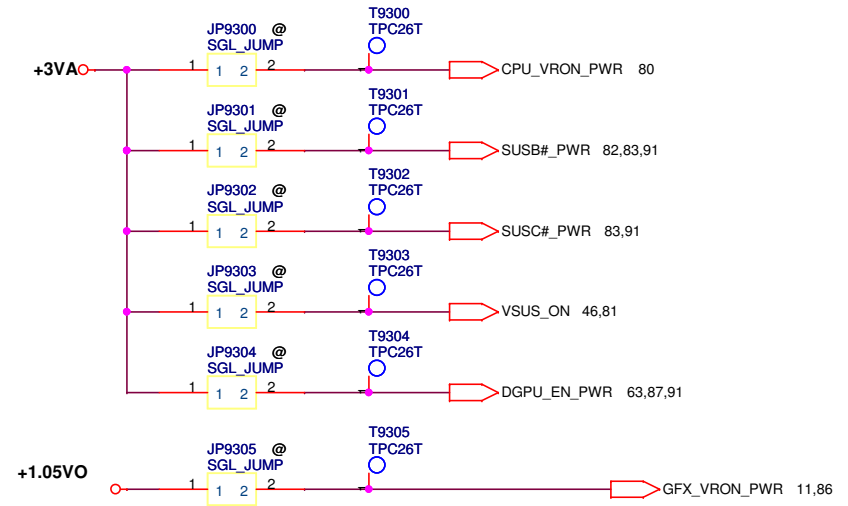
+12VS ○ → +12VS 38,39,91
 +5VS ○ → +5VS 15,19,38,39,41,42,46,48,49,60,63,80,86,91
 +3VS ○ → +3VS 10,13,14,15,16,17,18,19,21,22,24,33,37,38,39,41,46,47,49,60,63,65,80,86,91,92
 +1.8VS ○ → +1.8VS 11,18,19,82
 +1.5VS ○ → +1.5VS 10,11,24,55,63,91
 +0.75VS ○ → +0.75VS 21,22,63,83

+12VSUS ○ → +12VSUS 60,81,91
 +5VSUS ○ → +5VSUS 19,60,61,66,81,91
 +3VSUS ○ → +3VSUS 10,13,14,15,16,17,18,19,33,46,55,81,92

+12V ○ → +12V 91
 +5V ○ → +5V 42,63,91
 +3V ○ → +3V 37,50,63,65,82,91
 +1.5V ○ → +1.5V 10,11,21,22,63,83

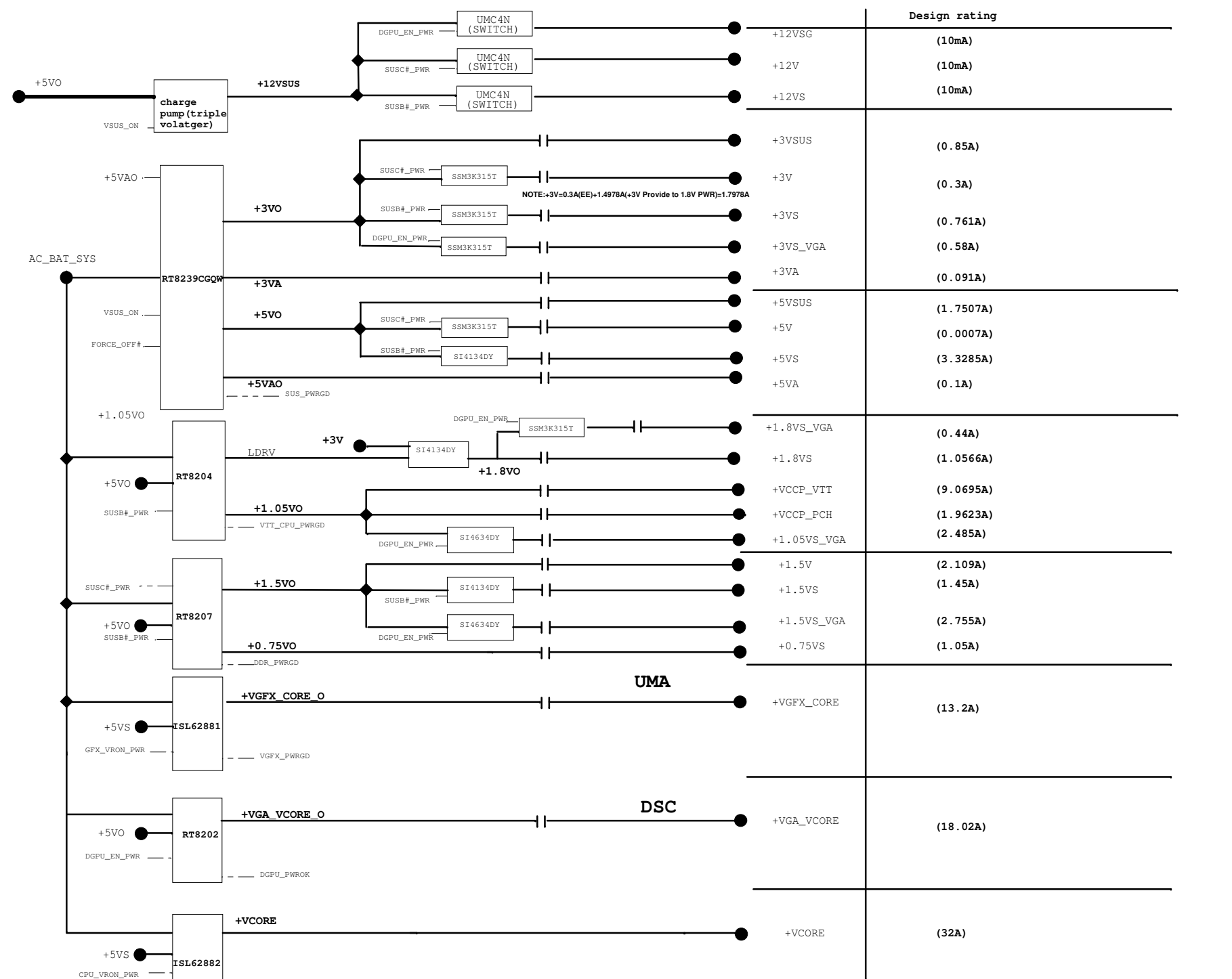
+VGA_VCORE ○ → +VGA_VCORE 63,75,87
 +VGFX_CORE ○ → +VGFX_CORE 11,86
 +VCORE ○ → +VCORE 11,12,80
 +12VSG ○ → +12VSG 91
 +3VS_VGA ○ → +3VS_VGA 70,72,74,91
 +1.8VS_VGA ○ → +1.8VS_VGA 63,91
 +1.5VS_VGA ○ → +1.5VS_VGA 63,71,76,91
 +1.05VS_VGA ○ → +1.05VS_VGA 63,70,71,72,91

FOR POWER TEST



<Variant Name>

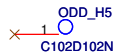
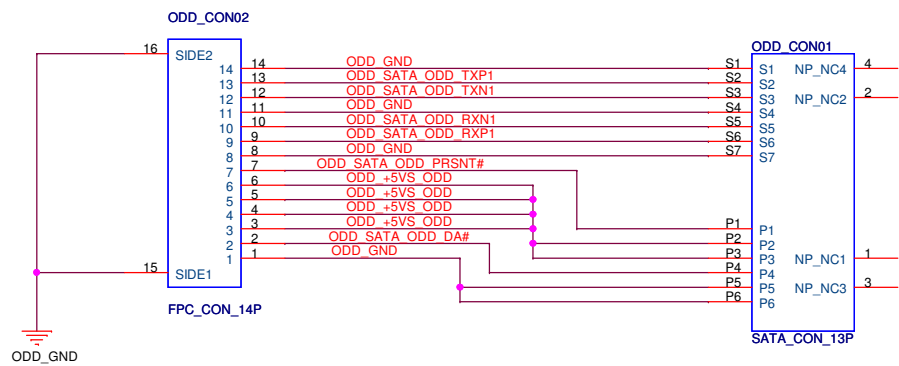
PEGATRON Title : POWER_SIGNAL		
Engineer: Adams_Lin		
Size Custom	Project Name AIC70	Rev 1.0
Date: Wednesday, May 04, 2011	Sheet 93 of 77	



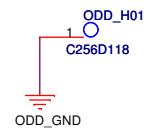
Design rating	
+12VSG	(10mA)
+12V	(10mA)
+12VS	(10mA)
+3VSUS	(0.85A)
+3V	(0.3A)
+3VS	(0.761A)
+3VS_VGA	(0.58A)
+3VA	(0.091A)
+5VSUS	(1.7507A)
+5V	(0.0007A)
+5VS	(3.3285A)
+5VA	(0.1A)
+1.8VS_VGA	(0.44A)
+1.8VS	(1.0566A)
+VCCP_VTT	(9.0695A)
+VCCP_PCH	(1.9623A)
+1.05VS_VGA	(2.485A)
+1.5V	(2.109A)
+1.5VS	(1.45A)
+1.5VS_VGA	(2.755A)
+0.75VS	(1.05A)
+VGFYX_CORE	(13.2A)
+VGA_VCORE	(18.02A)
+VCORE	(32A)

VR_VID0~VR_VID6, H_DPRSTP#, MCH_OK, PM_DPRSLPVR, PM_PSI#, VCCSENSE, VSSSENSE, STP_CPU#, PWR_MON

Item	Date	Description	Item	Date	Description	Item	Date	Description	
SR-1	0120-11	P61, A0410, change USB power switch circuit	SR-71	0128-11	P15. Add C1510 (22pF) for Clock fine-tune	AICTO R1-17 0306-11-1	P99. Add I0C7, S007	AICTO R2.0-0-41 0415-11-1	P66. Change LED602 to 0713-01Q600, LED603 to 0713-01Q200, R6605 to 100 ohm, R6604 to 390 ohm
SR-2	0120-11	Del P67, P68. Add P33, P34 for LAN	SR-72	0128-11	P33. change R325, R331 (4.7k ohm)	AICTO R1-18 0306-11-1	P94. Delete C346	AICTO R2.0-42 0415-11-1	P49. Change R4903 to 4.32k
SR-3	0120-11	P48. change KB CON4801	SR-73	0128-11	P39. Un-mount R3907 (HDMI)	AICTO R1-19 0306-11-1	P60. Add SPV002 and use /HDD_CABLE option for HDD cable	AICTO R2.0-43 0415-11-1	P61. Change U6104 to USB POWER SW. GS47R1P810: 06V25000008 , nostuff U6105
SR-4	0120-11	P34. change R445 CON4801	SR-74	0128-11	Change connector by list of 0128-11	AICTO R1-20 0306-11-1	P33. Change R3717 to 10k pull down for disable OC mode and nostuff C3303	AICTO R2.0-44 0415-11-1	P34. Change U3402 P/N to 0912-0001000 (only change P/N)
SR-5	0120-11	P79. change BATT. con. circuit	SR-75	0129-11	Change HDD CON601(1224-01N000)	AICTO R1-21 0306-11-1	P60. Delete /J7* option	AICTO R2.0-45 0420-11-1	P31. Change L3303 to 0 ohm
SR-6	0120-11	P65, A02 change PWR_LED CON6503 circuit	SR-76	0129-11	P97 (A02). Change Hotbar 6 Pad (PWR_U01)	AICTO R1-22 0306-11-1	P60. Delete /J7* option	AICTO R2.0-46 0421-11-1	P38. Reserve TP02
SR-7	0120-11	P60. change HDD CON6001	SR-77	0129-11	P41-P50 Change VP part	AICTO R1-23 0306-11-1	P60. Delete /J7* option	AICTO R2.0-47 0421-11-1	P38. Delete TP_SMC, TP_SMC
SR-8	0121-11	P44, P45 Del Entry audio circuit (Full)	SR-78	0129-11	P55. Add Q5510, R5515 for BT PCI-E wake up event	AICTO R1-24 0306-11-1	P48. Modify TP Button optional description	AICTO R2.0-48 0504-11-1	P49. Change R4903 to 4.02k
SR-9	0121-11	P50. Del Entry SD socket circuit	SR-79	0130-11	P50. change footprint for U5001 Card reader controller	AICTO R1-25 0306-11-1	P41. Modify speaker optional description and related net name	AICTO R2.0-49 0504-11-1	P66. Change H611, H612 to OSC optional
SR-10	0121-11	P77. Del B channel VRAM * 4 circuit	SR-80	0130-11	P66. change CPU4, GPU2, System screw hole*10	AICTO R1-26 0306-11-1	P1-P99. Hideify schematic optional	AICTO R2.0-50 0504-11-1	P61. Nostuff CON603
SR-11	0121-11	P46. Add EC GPIO35 DGPU_PWR_EN for Power	SR-81	0130-11	P46. change RN4601C (RN5202C)	AICTO R1-27 0307-11-1	P18. Add R1824 for PCM SPT *3VA power	AICTO R2.0-51 0504-11-1	P93. Nostuff I0C06
SR-12	0121-11	P34, P35. Modify LAN AR8158 (Full)	SR-82	0130-11	P66. change F screw hole *2	AICTO R1-28 0307-11-1	P46. Delete R4627, R4625, R4621, R4622, R4615, R4616, R4617, C4608, U4602	AICTO R2.0-70 0504-11-1	P34. Nostuff D1401, stuff R3408
SR-13	0123-11	P63. Change DC con. as VP part	SR-83	0130-11	P46. change SHORT PIN (R4601, R4602)	AICTO R1-29 0307-11-1	P60. Add R5109, R5110, R5111, R5112		
SR-14	0123-11	P60. change HDD CON6001	SR-84	0130-11	P46, P65. change EC GPIO21 (PWR_AMBER_LED*) for PWR Brd.	AICTO R1-30 0308-11-1	P66. Change ONL_LED08 to GND		
SR-15	0123-11	P7-P37 Change VP part	SR-85	0130-11	Modify Sub board screw hole	AICTO R1-31 0308-11-1			
SR-16	0124-11	P41 Del Entry speaker R4117-R4120	SR-86	0130-11	P34. Change R345 CON3401 1223-00B7000	AICTO R1-32 0308-11-1			
SR-17	0124-11	P38-P39 Change VP part	SR-87	0131-11	P74. Change Q7401B (Q9203B)	AICTO R1-33 0308-11-1			
SR-18	0124-11	P66 Remove LED circuit	SR-88	0131-11	P96, P99. Del Screw hole ODD_HOJ, change IOH3	AICTO R1-34 0309-11-1			
SR-19	0124-11	P48. Reverse KB CON4801	SR-89	0131-11	P97. Change Power Board LED_PWR_LED01	AICTO R1-35 0309-11-1			
SR-20	0124-11	P71. Remove GPU Channel B dummy NET	SR-90	0131-11	P60. Change 15* ODD CON505 as VP	AICTO R1-36 0309-11-1			
SR-21	0124-11	P16, P61. Remove USB_S (HDMI)	SR-91	0131-11	P99-P99. Copy from AAB70 (sub board)	AICTO R1-37 0309-11-1			
SR-22	0124-11	P49. Remove TP button circuit				AICTO R1-38 0311-11-1			
SR-23	0124-11	P13. Remove Entry Ar R1318, R1346, R1347, R1348, R1349				AICTO R1-39 0311-11-1			
SR-24	0124-11	P50. Modify CON5002 SD socket circuit				AICTO R1-40 0311-11-1			
SR-25	0124-11	P46. Change KB CON4801 PIN definition				AICTO R1-2 0320-11-1			
SR-26	0124-11	P16, P61. change USB power switch circuit				AICTO R1-3 0320-11-1			
SR-27	0124-11	P41, P46. AL0271-SPKR_EC_ICH_Coily				AICTO R1-4 0320-11-1			
SR-28	0124-11	P46, P65. Modify LED circuit and EC GPIO definition				AICTO R1-5 0320-11-1			
SR-29	0125-11	P33 Remove LAN LED circuit				AICTO R1-6 0320-11-1			
SR-30	0125-11	P61 Modify D6101, RN6101, RN6105, RN6106				AICTO R1-7 0320-11-1			
SR-31	0125-11	P33 Change R3311 as VP				AICTO R1-8 0320-11-1			
SR-32	0125-11	P33 Change U3301 to AR8158 and delete SM BUS				AICTO R1-9 0320-11-1			
SR-33	0125-11	P34 Modify LAN ESD circuit				AICTO R1-10 0320-11-1			
SR-34	0125-11	P61. Modify Q6101				AICTO R1-11 0320-11-1			
SR-35	0125-11	P65. Modify Q6501				AICTO R1-12 0320-11-1			
SR-36	0125-11	P38, P46. Del F3801, C3811 Add CRT IN Detect				AICTO R1-13 0320-11-1			
SR-37	0125-11	P63. Reverse J6301				AICTO R1-14 0320-11-1			
SR-38	0125-11	P61, P46. change USB power switch and GPIO				AICTO R1-15 0320-11-1			
SR-39	0125-11	P46, P66. change LED power and Met name				AICTO R1-16 0320-11-1			
SR-40	0125-11	P34. Modify Transformer circuit				AICTO R1-17 0320-11-1			
SR-41	0125-11	P33. Modify H/W strap setting				AICTO R1-18 0320-11-1			
SR-42	0125-11	P37. Modify LVDS PIN definition				AICTO R1-19 0320-11-1			
SR-43	0125-11	P42. Modify De-Pop circuit				AICTO R1-20 0320-11-1			
SR-44	0125-11	P41. Modify Audio Pin 14, 15, 27-31				AICTO R1-21 0320-11-1			
SR-45	0126-11	P34. Modify Transformer circuit				AICTO R1-22 0320-11-1			
SR-46	0126-11	P16. GPIO54 DGPU_PWR_EN				AICTO R1-23 0320-11-1			
SR-47	0126-11	U1301, U7001 Keypart no; U4602, F6302 Modify for BOM				AICTO R1-24 0320-11-1			
SR-48	0126-11	P34. Modify Transformer circuit				AICTO R1-25 0320-11-1			
SR-49	0126-11	P63, P60, P77, P48. Add 15* circuit BATT, ODD, Keyboard				AICTO R1-26 0320-11-1			
SR-50	0126-11	P13, P60 Rename SATA 0 to SATA 1				AICTO R1-27 0320-11-1			
SR-51	0126-11	P63. Reverse DC-IN J6301 PIN1 as GND				AICTO R1-28 0320-11-1			
SR-52	0126-11	P48. Reverse KB CON4801				AICTO R1-29 0320-11-1			
SR-53	0126-11	DGPU Dync with EHS11				AICTO R1-30 0320-11-1			
SR-54	0126-11	P.76. T7, M7 Setting				AICTO R1-31 0320-11-1			
SR-55	0126-11	Modify as OPT display output				AICTO R1-32 0320-11-1			
SR-56	0127-11	P.76. Cancel T7, M7 Setting				AICTO R1-33 0320-11-1			
SR-57	0127-11	P.46, P50 Modify single net				AICTO R1-34 0320-11-1			
SR-58	0127-11	P.42 Change R4205, R4206 = 51 ohm				AICTO R1-35 0320-11-1			
SR-59	0127-11	P.14 R1403, R1404 option N/A				AICTO R1-36 0320-11-1			
SR-60	0127-11	P.14 R1443, R1444, RN1402, R1424, R1426, R1427, R1428 option N/A; R1429 option /HDMI_LED_PCH				AICTO R1-37 0320-11-1			
SR-61	0127-11	P.71, P74. R7101, R7103, R7435, R7437 option 0				AICTO R1-38 0320-11-1			
SR-62	0127-11	P74. Del R7433, R7434, GPIO Test Pad				AICTO R1-39 0320-11-1			
SR-63	0128-11	P34. U3403.4 RNN				AICTO R1-40 0320-11-1			
SR-64	0128-11	P66. change R6603.1 (+5VA), LED602, LED603				AICTO R1-41 0320-11-1			
SR-65	0128-11	P65. change R6508.1 (PWR_LED_ON#), CON6503.6 (+5VSUS)				AICTO R1-42 0320-11-1			
SR-66	0128-11	P97. Modify A04 Pwr Board				AICTO R1-43 0320-11-1			
SR-67	0128-11	P55. Un-mount Q5505, R5510				AICTO R1-44 0320-11-1			
SR-68	0128-11	P66. Modify Screw Hole (Sync with AAB70)				AICTO R1-45 0320-11-1			
SR-69	0128-11	P63. Modify Battery CON6302, D6302 signal name				AICTO R1-46 0320-11-1			
SR-70	0128-11					AICTO R1-47 0320-11-1			
						AICTO R1-48 0320-11-1			
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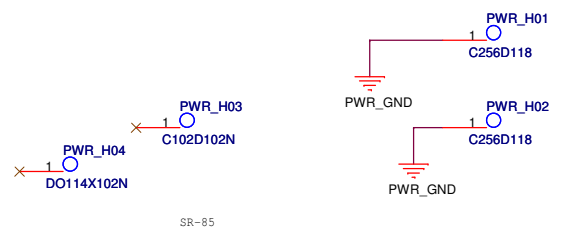
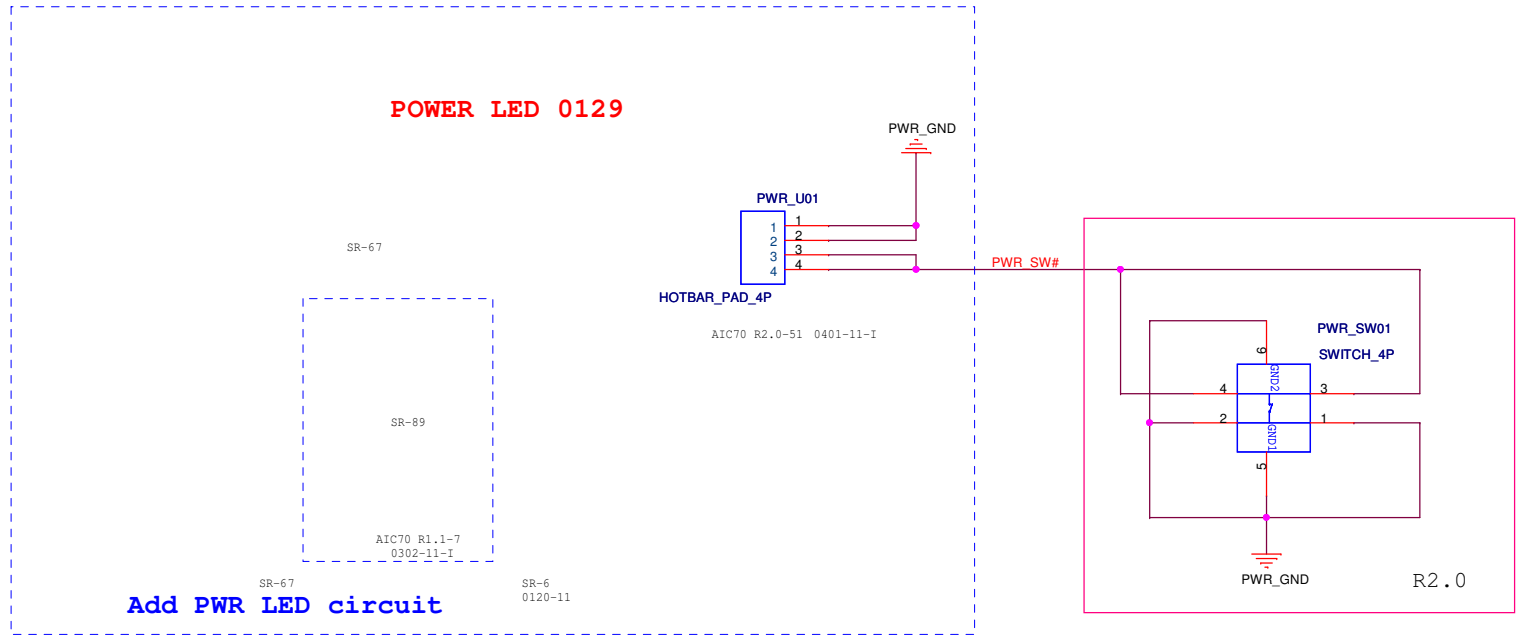


SR-88

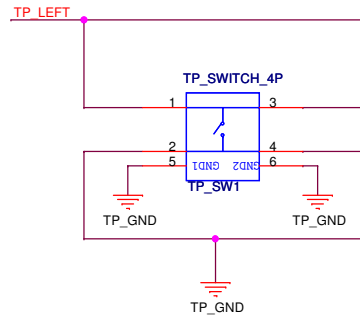
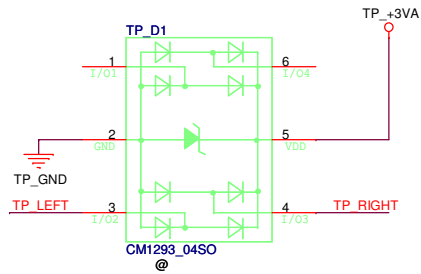
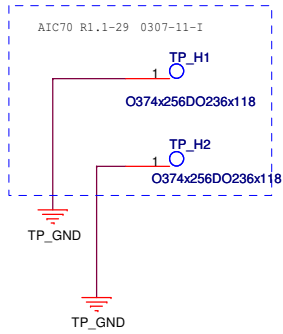
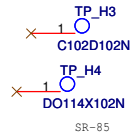


SR-85

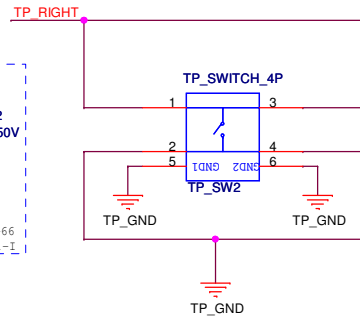
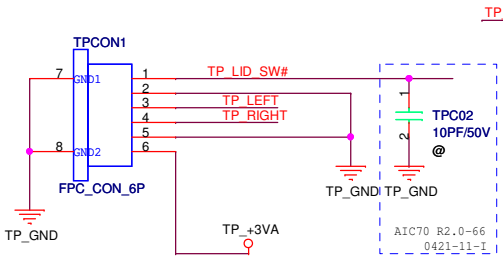
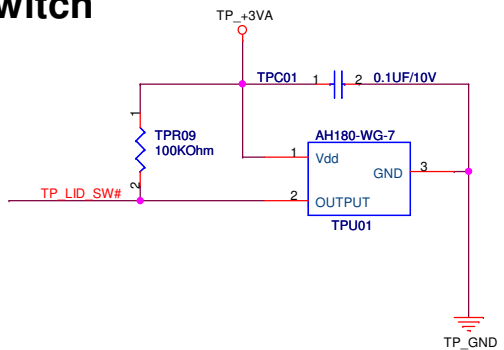
PEGATRON Title :ODD		Engineer: <i>Johnson Huang</i>
BU1-RD Div.1-HW RD Dept.1		
Size B	Project Name TOD ODD BOARD	Rev 2.0
Date: Wednesday, May 04, 2011	Sheet 96 of 77	



PEGATRON Title : PWR BTN		Rev
BU1-RD Div.1-HW RD Dept.1		2.0
Size	Project Name	
B	TOD POWER SW	
Date: Wednesday, May 04, 2011	Sheet 97 of 77	

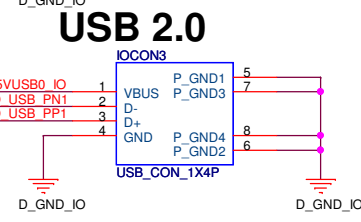
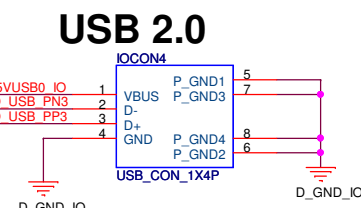
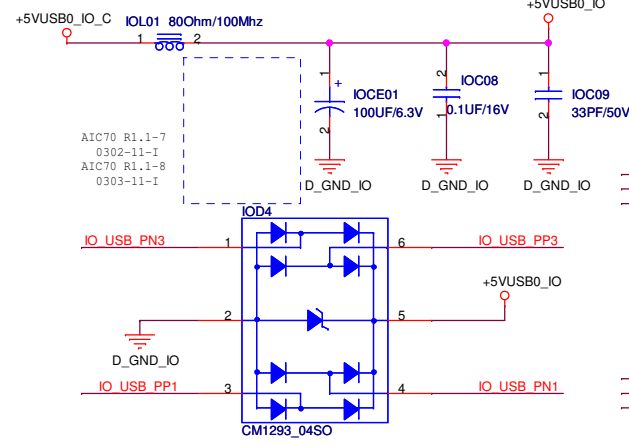
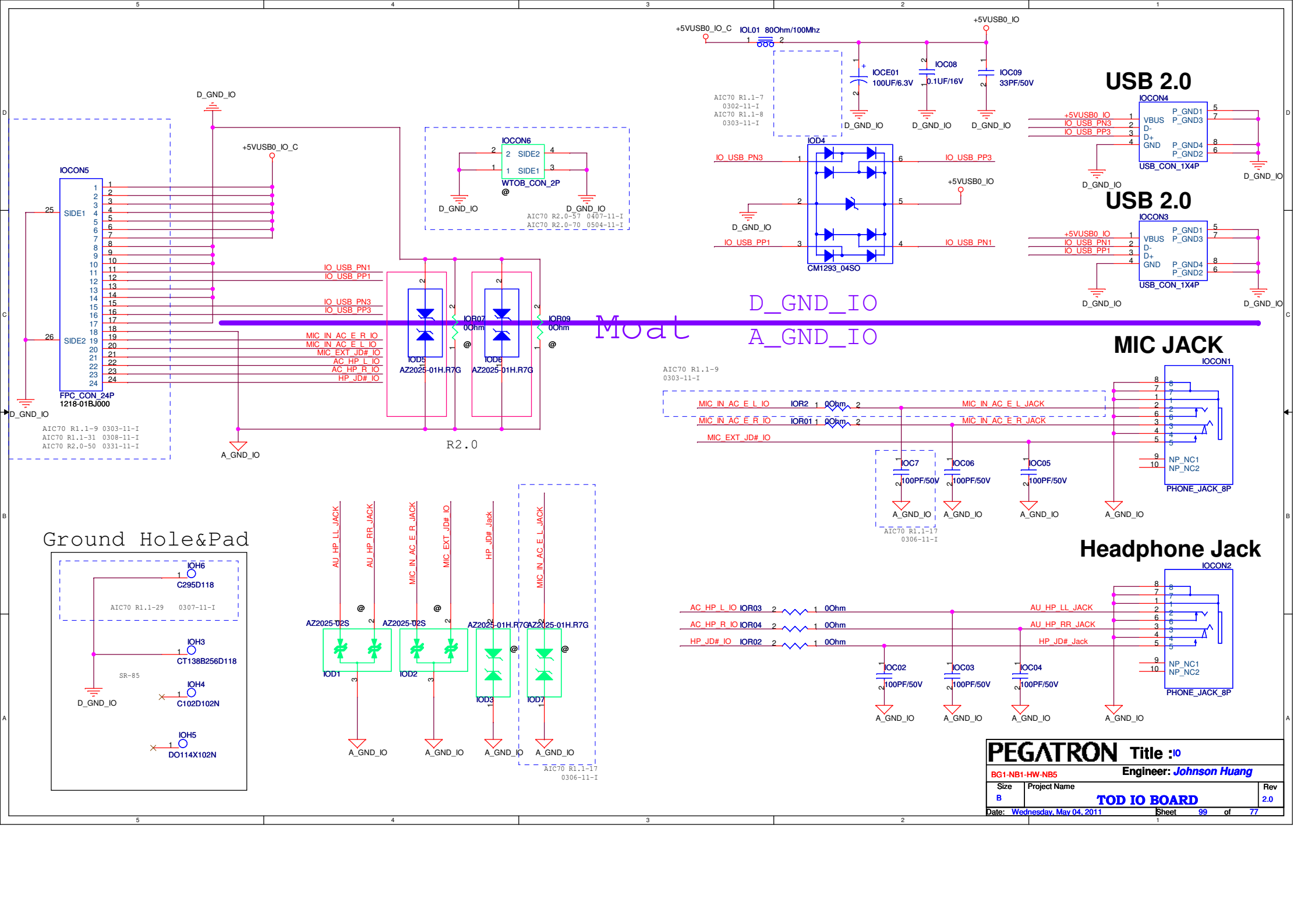


LID Switch



AIC70 R2.0-48 0330-11-I
AIC70 R2.0-67 0421-11-I

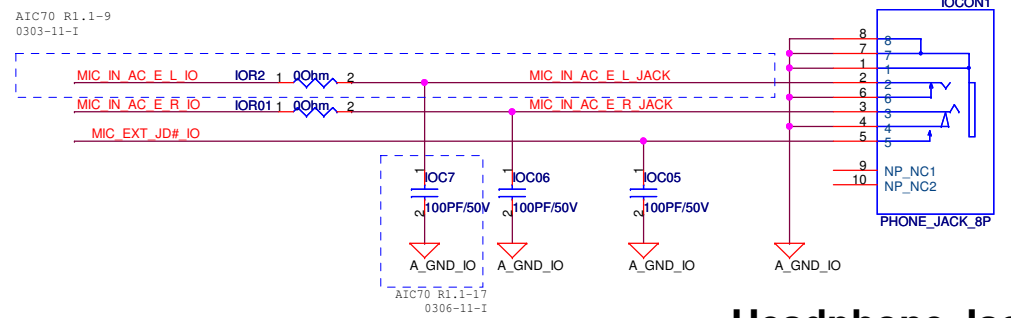
PEGATRON		Title : A03 TP	
<OrgName>		Engineer: Johnson Huang	
Size B	Project Name AIH70	Date: Wednesday, May 04, 2011	Rev 1.0
		Sheet 98 of 99	



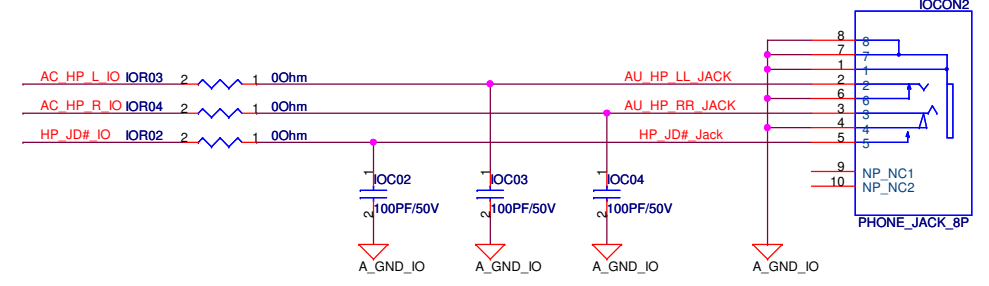
Moat

D_GND_IO
A_GND_IO

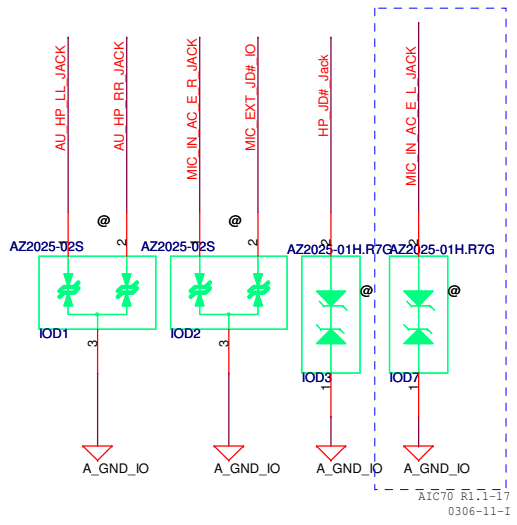
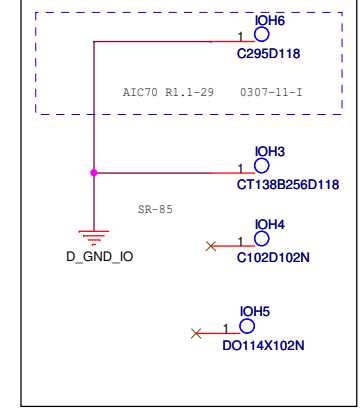
MIC JACK



Headphone Jack



Ground Hole&Pad



PEGATRON Title : IO		Engineer: Johnson Huang
BG1-NB1-HW-NB5		Rev 2.0
Size B	Project Name TOD IO BOARD	Date: Wednesday, May 04, 2011
Date: Wednesday, May 04, 2011		Sheet 99 of 77