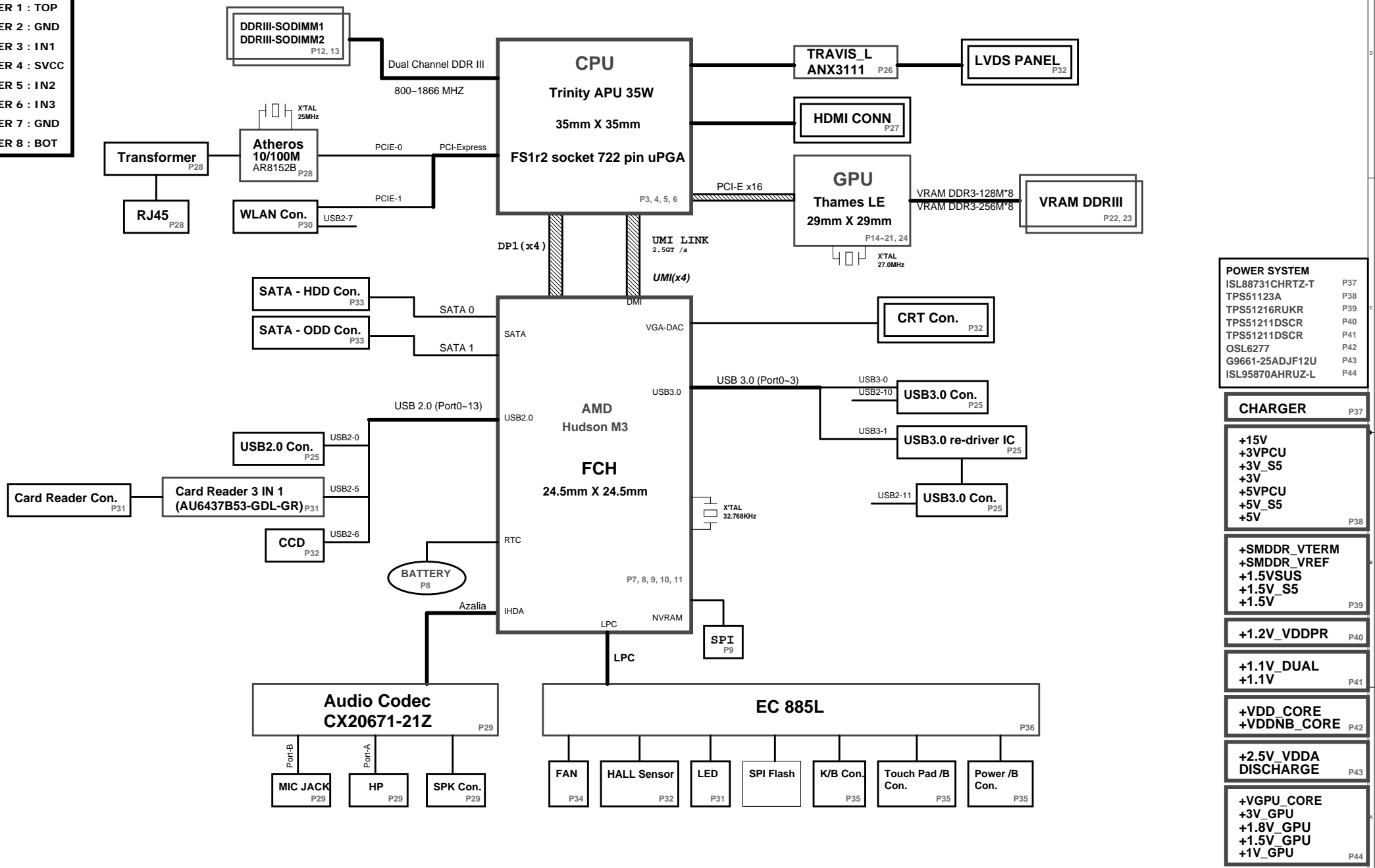


14" BY6/BY6D Comal Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



POWER SYSTEM

ISL88731CHRTZ-T	P37
TPS51123A	P38
TPS51216RUKR	P39
TPS51211DSCR	P40
TPS51211DSCR	P41
OSL6277	P42
G9661-25ADJF12U	P43
ISL95870AHRUZ-L	P44

CHARGER P37

+15V
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V

P38

+SMDDR_VTERM
+SMDDR_VREF
+1.5VSUS
+1.5V_S5
+1.5V

P39

+1.2V_VDDPR

P40

+1.1V_DUAL
+1.1V

P41

+VDD_CORE
+VDDNB_CORE

P42

+2.5V_VDDA DISCHARGE

P43






+VGPU_CORE
+3V_GPU
+1.8V_GPU
+1.5V_GPU
+1V_GPU

P44

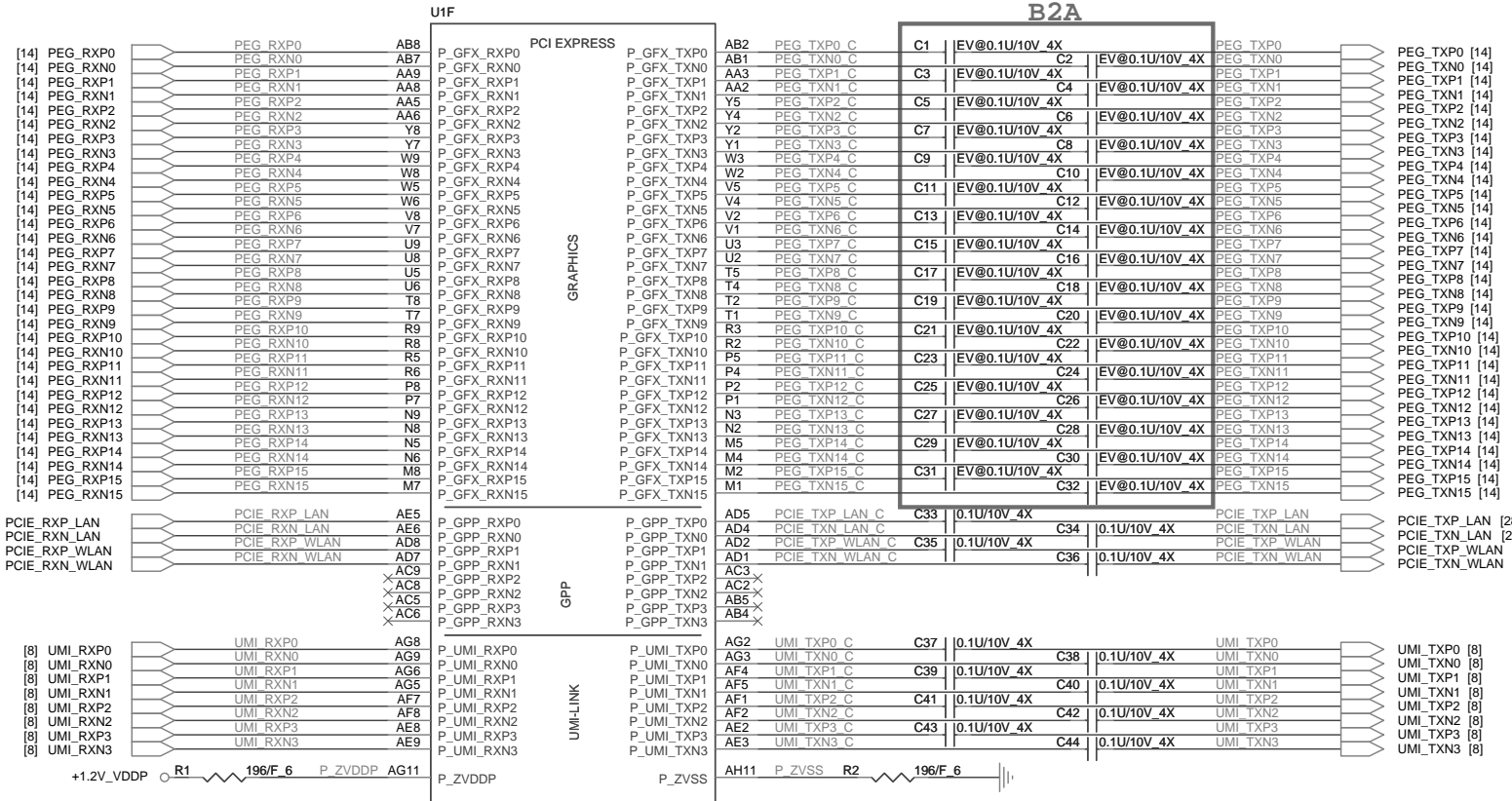
Table of Contents

PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3 - 6	Processor	CPU
7 - 11	FCH	CLG
8	RTC	RTC
12 - 13	DDRIII SO-DIMM	DDR
14 - 21	Thames/Seymour(M2)	VGA
22 - 23	VRAM - DDR3	VGA
24	PX	VGA
25	USB Connector	USB
	USB 3.0 Redriver	U3B
	USB Sleep Charger	SLC
26	TRAVIS Decoder	LDS
27	HDMI comm part	HDM
	CEC	CEC
28	Atheros LAN	LAN
29	Codec (CX20671-21Z)	ADO
30	MINI Card (Wi-Fi & WIMAX)	MNW
31	Card reader	MMC
	LED	LED
32	VGA Connector	VGA
	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
33	HDD	HDD
	ODD	ODD
34	Thermal	THC
	FAN	THC
35	KeyBoard	KBC
	TP&FP board	TPD,FPD
	Power SW	PSW
36	EC NPCE885LA0DX	KBC
37	Charger (ISL88731CHRTZ-T)	PWM
38	System 5V/3V	PWM
39	DDR 1.5V	PWM
40	+1.2V_VDDPR	PWM
41	+1.1V_DUAL	PWM
42	+VCC_CORE 2+1	PWM
43	Discharge	PWM
44	GPU_CORE	PWM
45	Power Sequence	
46	Change List	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V--+19V		S0-S5
+VCCRTC	+3.0V--+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3VPCU	+3.3V	AC/DC Insert enable	S0-S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P	S0
+1.5VSUS	+1.5V	S5_ON	S0-S3
+1.5V	+1.5V	MAIN_ON	S0
+1.2V_VDDPR	+1.2V	VDDA_PWRGD	S0
+1.1V_DUAL	+1.1V	+1.1V_DUAL_EN	S0-S5
+1.1V	+1.1V	MAIN_ON	S0
+VDD_CORE	~	VDDA_PWRGD	S0
+VDDNB_CORE	~	VDDA_PWRGD	S0
+VGPU_CORE		PX_MODE	S0
+1.8V_GPU	+1.8V	PE_GPIO1	S0
+1V_GPU	+1V	DGPU_PWREN	S0
+3V_GPU	+3.3V	PE_GPIO1	S0
+1.5V_GPU	+1.5V	PX_MODE_D	S0
+2.5V_VDDA	+2.5V	MAIN_ON	S0

GND PLANE	PAGE
 GND_SIGNAL	32
 8769GND	36
	28
 GND	ALL
 ADOGND	29

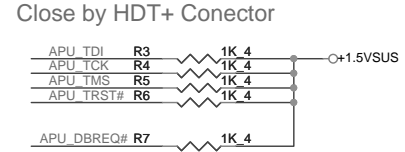
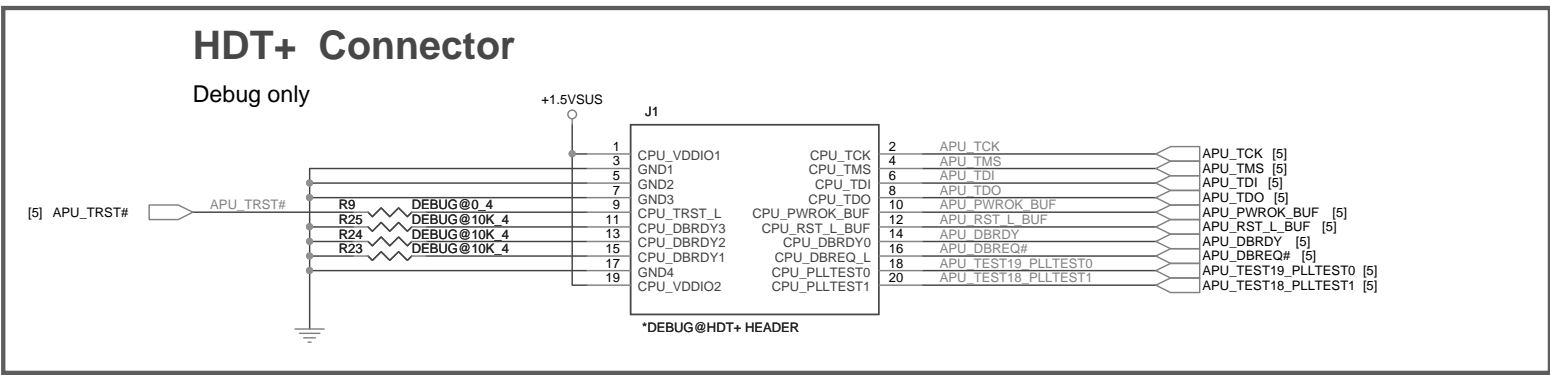
ITEM	Value Code	FUNCTIONS
1	CEC@	CEC
2	Debug@	HDT+ Debug
3	EV@	DISCRETE
4	IV@	UMA
5	U3@	Internal USB 3.0
6	1G4@	VRAM 1Gb*4
7	1G8@	VRAM 1Gb*8
8	2G@	VRAM 2Gb
9	AMD@	AMD VRAM
10	DIS@	DISCRETE
11	M2@	M2 FCH
12	M3@	M3 FCH
13	NMP@	LPC Debug Card
14	PX4@	PX4 Mode
15	PX5@	PX5 Mode
16	Sam@	Samsung VRAM
17	U2@	USB 2.0 (colay W USB 3.0)



PEG X 16

TO PCIE-LAN
TO WLAN

TO PCIE-LAN
TO WLAN

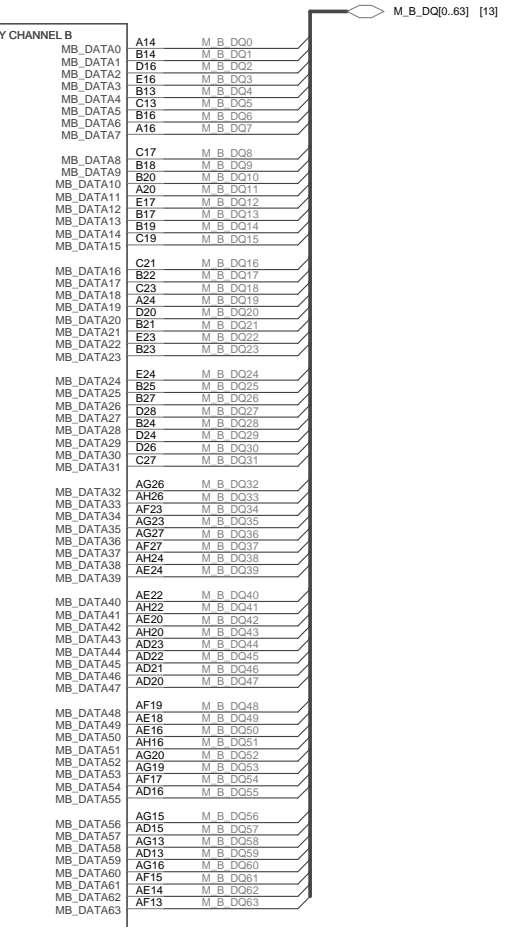
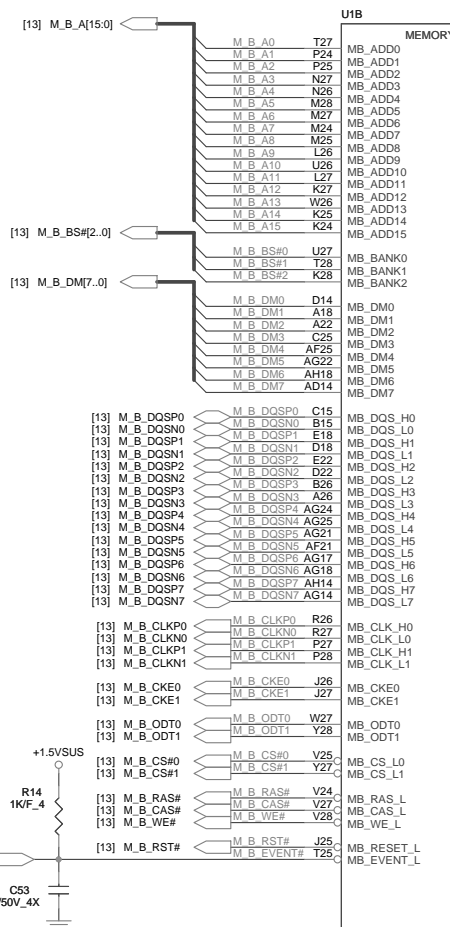
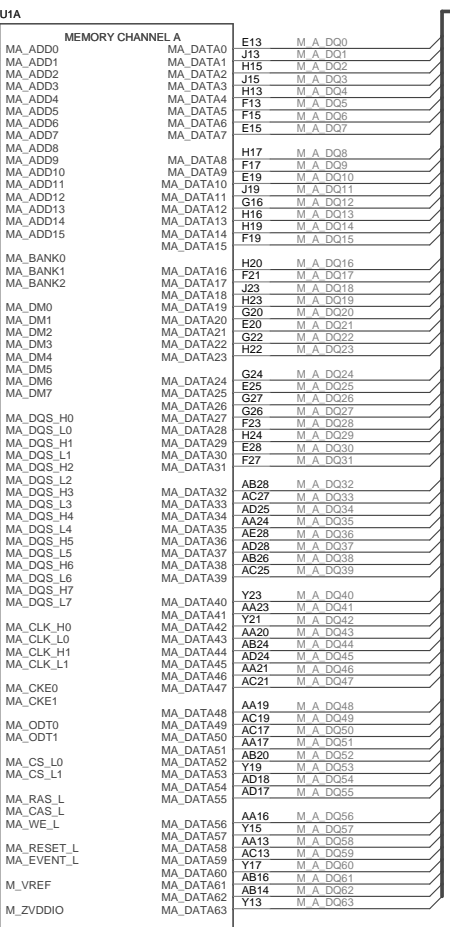
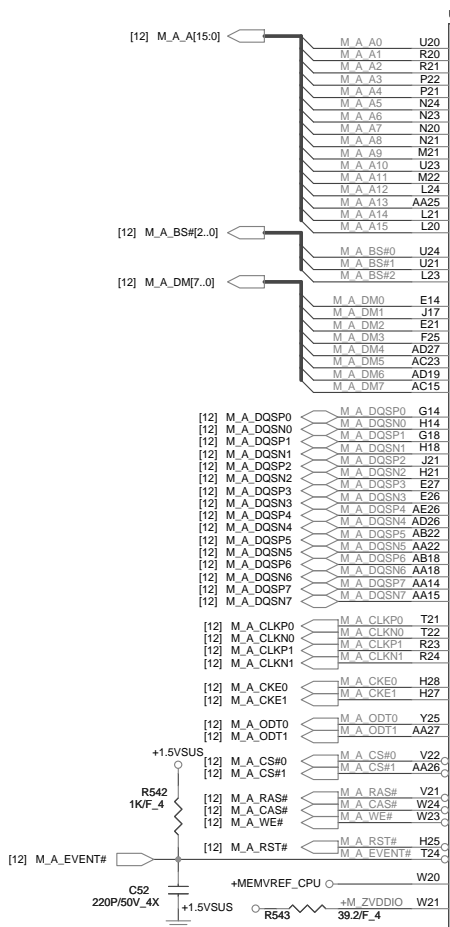


Quanta Computer Inc.

PROJECT : BY6/BY6D

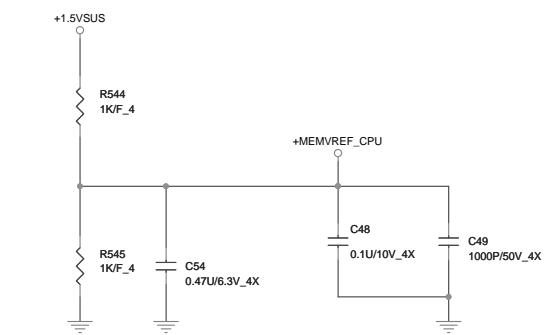
Size Document Number **APU 1/4(PCIE/UMI/GPP/HDT)** Rev 1A

Date: Tuesday, February 14, 2012 Sheet 3 of 47



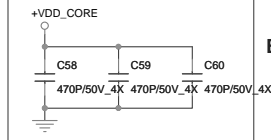
Trinity APU Soldermask openings for all bottom side vias/TTPs under FS1

Trinity APU

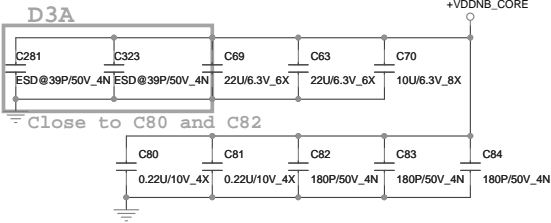


APU POWER TABLE

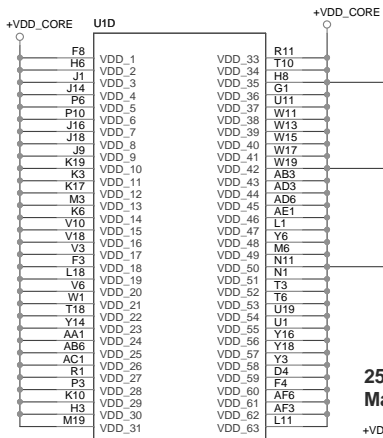
PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



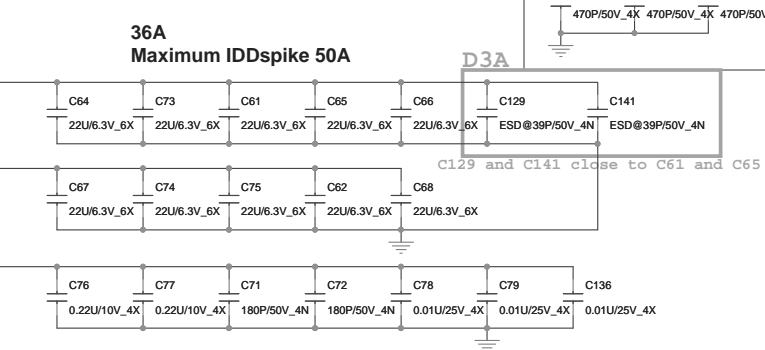
EMI



Close to C80 and C82

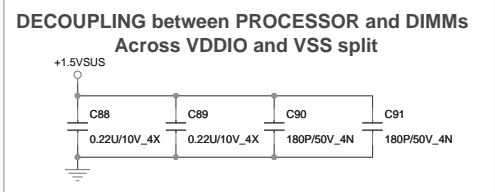


36A Maximum IDDspike 50A



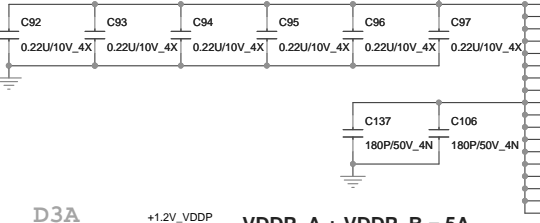
c129 and c141 close to C61 and C65

25A Maximum IDDNBspike 33A



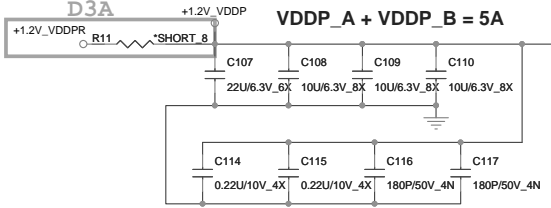
DECOUPLING between PROCESSOR and DIMMs Across VDDIO and VSS split

VDDIO=4.6A (Up to DDR3_1600 @ 1.5V)

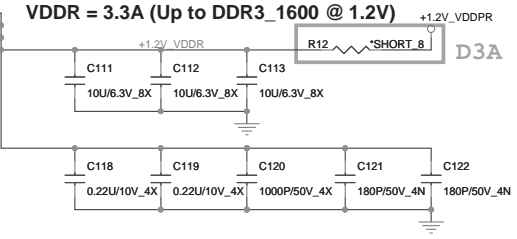


Trinity APU

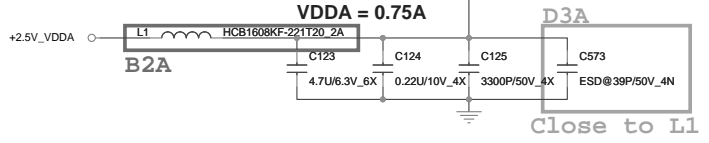
VDDP_A + VDDP_B = 5A



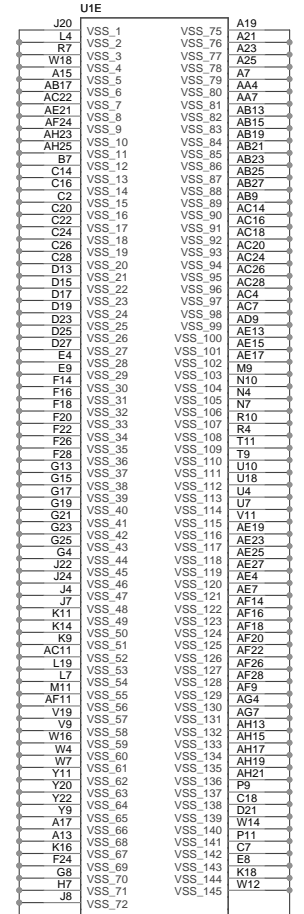
VDDR = 3.3A (Up to DDR3_1600 @ 1.2V)



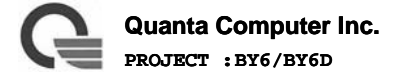
VDDA = 0.75A

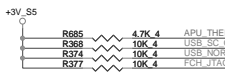
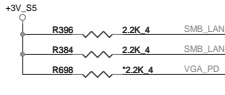
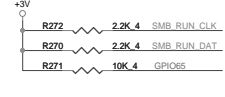
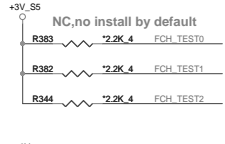


Close to L1



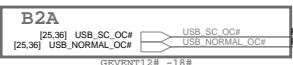
Trinity APU



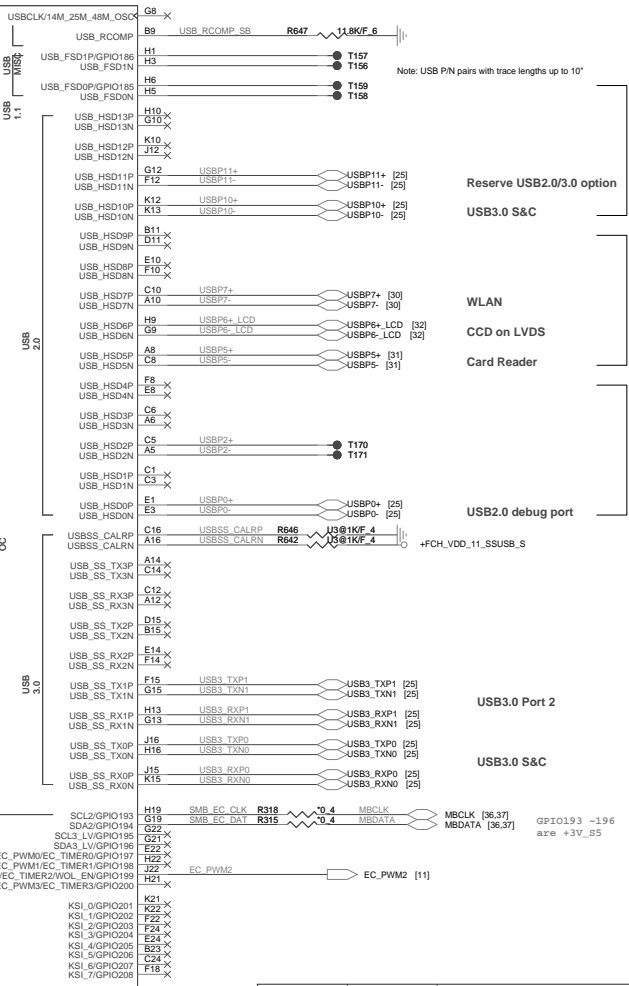
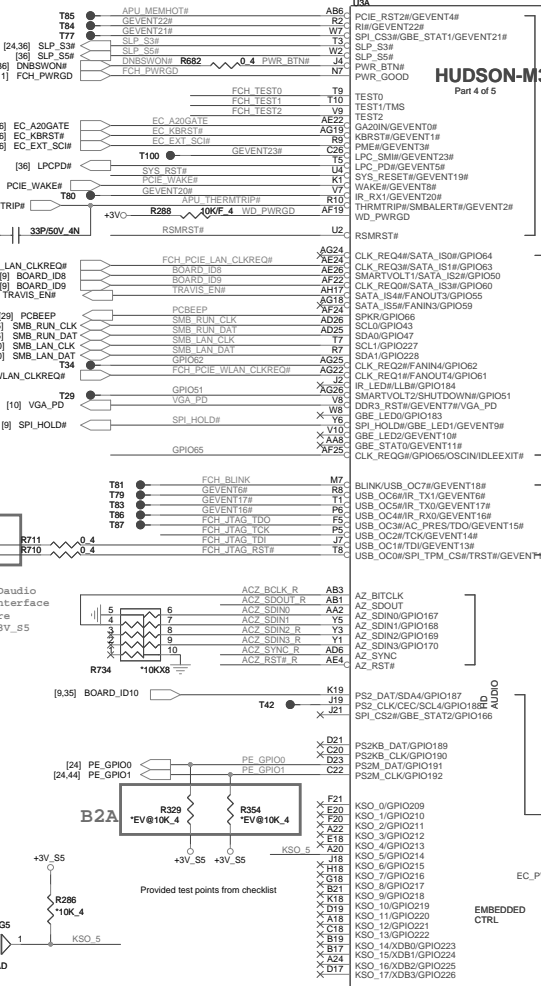
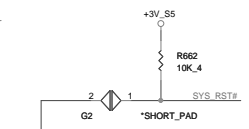


For Dimm
For Lan&WiFi

Integrated 8.2-kΩ PU



Note: LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported



HUB3
HUB2
HUB1

Reserve USB2.0/3.0 option
 USB3.0 S&C

WLAN
 CCD on LVDS
 Card Reader

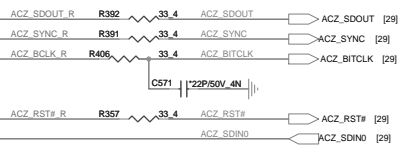
USB2.0 debug port

USB3.0 Port 2

USB3.0 S&C

Hudson-M3

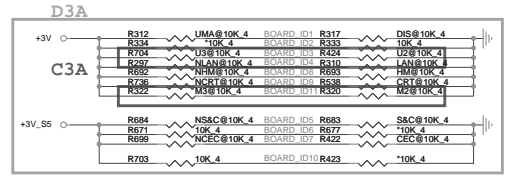
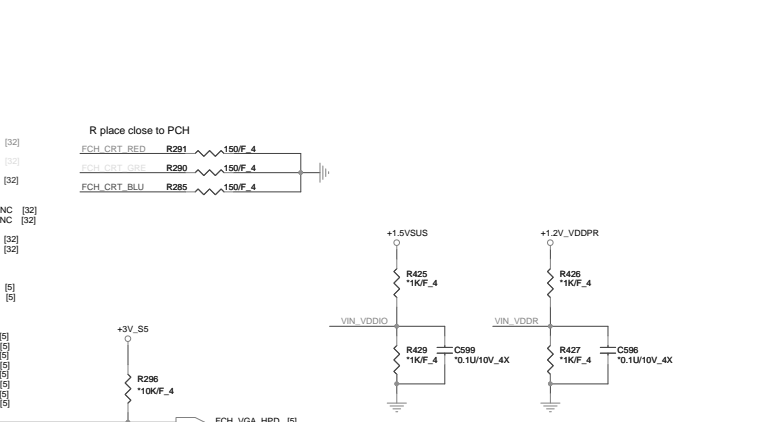
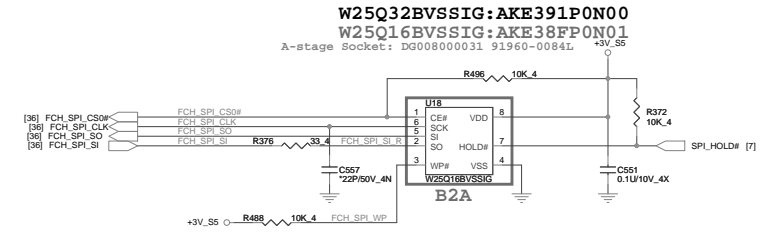
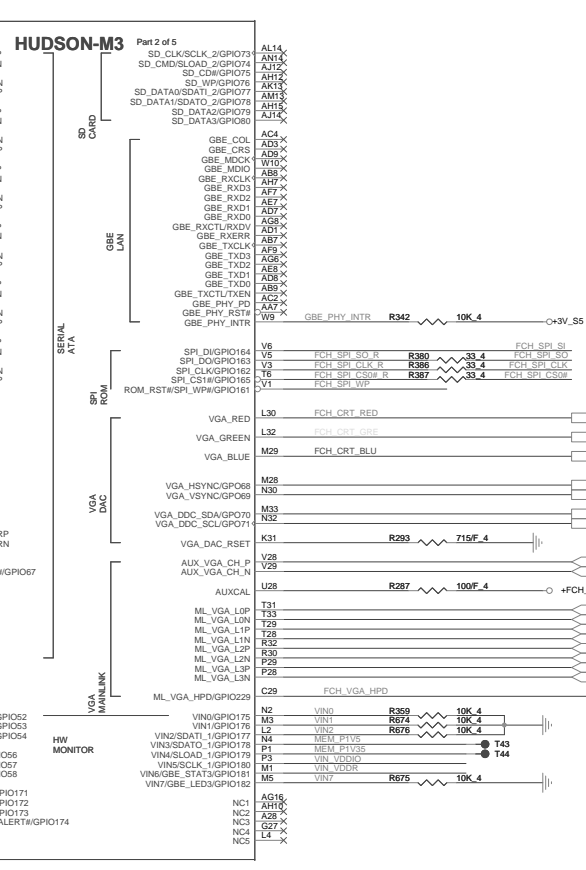
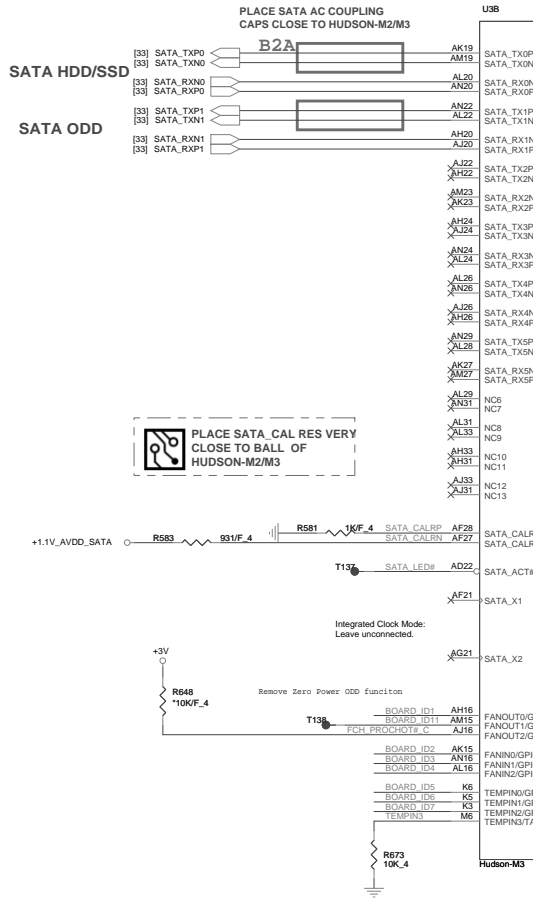
To Azalia



EC	FCH	Device	I2C_Device(S)
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery
I2Ce_2(M)		EEPROM	APU
I2Ce_3(M)		VGA Thermal	
	I2Cf_3(M)		APU
	I2Cf_1(M)	Lan	Wlan
	I2Cf_0(M)	Dimm	Clk Gen

EC will Conflict with FCH, did not mount R315&R318

Quanta Computer Inc.
PROJECT : BY6/BY6D
 Size Document Number **FCH 1/5(GPIO/USB/AZ)** Rev 1A
 Date: Tuesday, February 14, 2012 Sheet 7 of 47



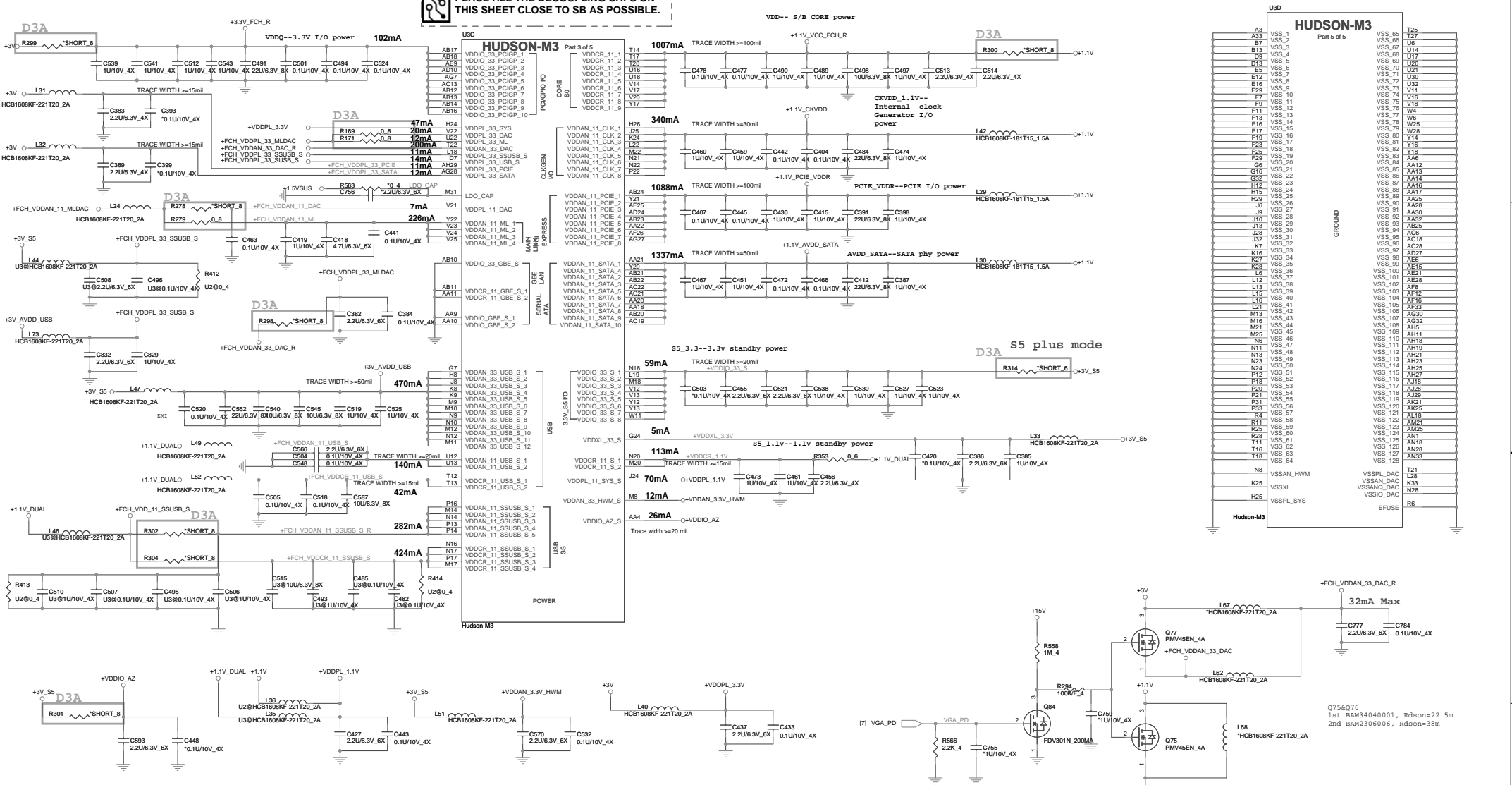
BOARD ID SETTING

	Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11
	UMA SKU		H	L								
	VGA SKU											
	VRAM 900M			H	L							
	VRAM 800M											
C3A	USB3_0				H	L						
	USB2_0											
B2A	W/O LAN					H	L					
	W/O S&C						H	L				
	W/O BT							H	L			
	W/O CEC								H	L		
B2A	W/O HDMI									H	L	
	W/O CRT										H	L
	Metal/IMR										H	L
	TEXTURE											H
C3A B2A	PCH-M3											H
	PCH-M2											L

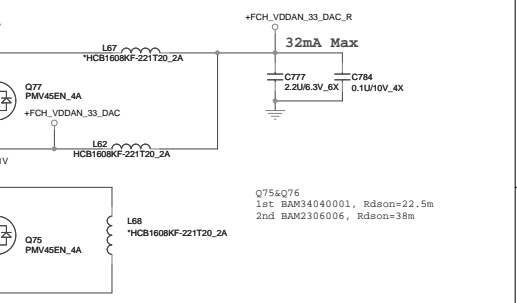


Quanta Computer Inc.
 PROJECT :BY6/BY6D
 FCH 3/5(SATA/VGA/GND/SPI)
 Date: Tuesday, February 14, 2012 Sheet 9 of 47

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

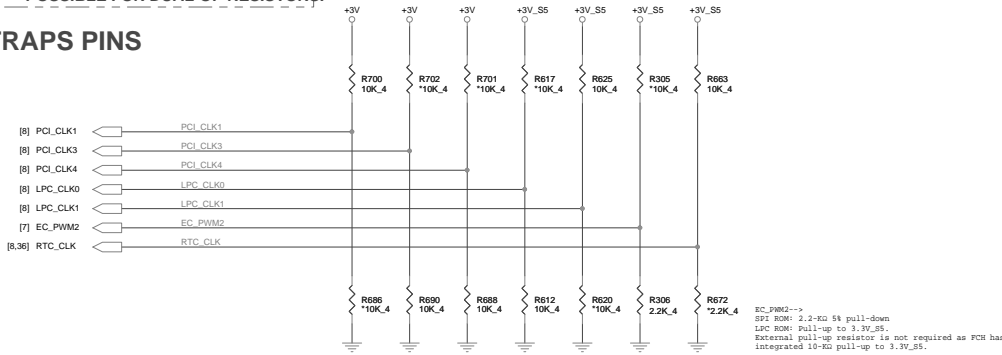


HUDSON-M3 Part 5 of 5	
A3	VSS_1
A3	VSS_2
B7	VSS_3
B13	VSS_4
D8	VSS_5
D13	VSS_6
E7	VSS_7
E12	VSS_8
E16	VSS_9
F7	VSS_10
F11	VSS_11
F15	VSS_12
F19	VSS_13
F19	VSS_14
F19	VSS_15
F19	VSS_16
F19	VSS_17
F26	VSS_18
F26	VSS_19
F26	VSS_20
G16	VSS_21
G16	VSS_22
H12	VSS_23
H15	VSS_24
H29	VSS_25
J6	VSS_26
J9	VSS_27
J10	VSS_28
J13	VSS_29
J28	VSS_30
J32	VSS_31
K27	VSS_32
K18	VSS_33
K29	VSS_34
K29	VSS_35
L6	VSS_36
L12	VSS_37
L13	VSS_38
L16	VSS_39
L16	VSS_40
L21	VSS_41
M3	VSS_42
M16	VSS_43
M21	VSS_44
M25	VSS_45
N6	VSS_46
N11	VSS_47
N13	VSS_48
N15	VSS_49
N23	VSS_50
P12	VSS_51
P16	VSS_52
P20	VSS_53
P21	VSS_54
P31	VSS_55
P33	VSS_56
R8	VSS_57
R11	VSS_58
R25	VSS_59
R25	VSS_60
T11	VSS_61
T16	VSS_62
T16	VSS_63
T16	VSS_64
N8	VSSAN_HWM
K25	VSSAN_DAC
H25	VSSXL
H25	VSSPL_SYS
T25	VSS_1
VSS_66	VSS_66
U14	VSS_67
U17	VSS_68
U17	VSS_69
U17	VSS_70
U20	VSS_71
U32	VSS_72
U32	VSS_73
U32	VSS_74
U32	VSS_75
U32	VSS_76
U32	VSS_77
U32	VSS_78
U32	VSS_79
U32	VSS_80
U32	VSS_81
U32	VSS_82
U32	VSS_83
U32	VSS_84
U32	VSS_85
U32	VSS_86
U32	VSS_87
U32	VSS_88
U32	VSS_89
U32	VSS_90
U32	VSS_91
U32	VSS_92
U32	VSS_93
U32	VSS_94
U32	VSS_95
U32	VSS_96
U32	VSS_97
U32	VSS_98
U32	VSS_99
U32	VSS_100
U32	VSS_101
U32	VSS_102
U32	VSS_103
U32	VSS_104
U32	VSS_105
U32	VSS_106
U32	VSS_107
U32	VSS_108
U32	VSS_109
U32	VSS_110
U32	VSS_111
U32	VSS_112
U32	VSS_113
U32	VSS_114
U32	VSS_115
U32	VSS_116
U32	VSS_117
U32	VSS_118
U32	VSS_119
U32	VSS_120
U32	VSS_121
U32	VSS_122
U32	VSS_123
U32	VSS_124
U32	VSS_125
U32	VSS_126
U32	VSS_127
U32	VSS_128
T21	VSSPL_DAC
L28	VSSAN_DAC
K33	VSSANO_DAC
N28	VSSIO_DAC
R6	EFUSE



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

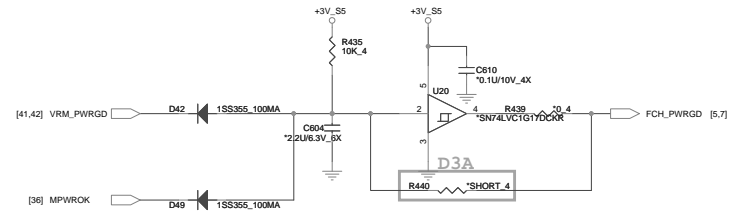
STRAPS PINS



Remove PCI_CLK2 function

REQUIRED STRAPS

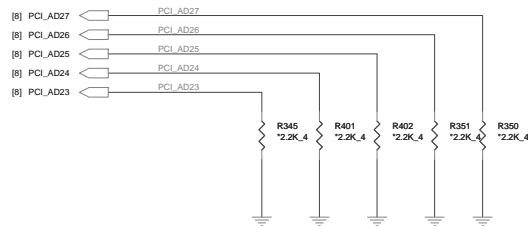
	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



FCH PWRGD CKT

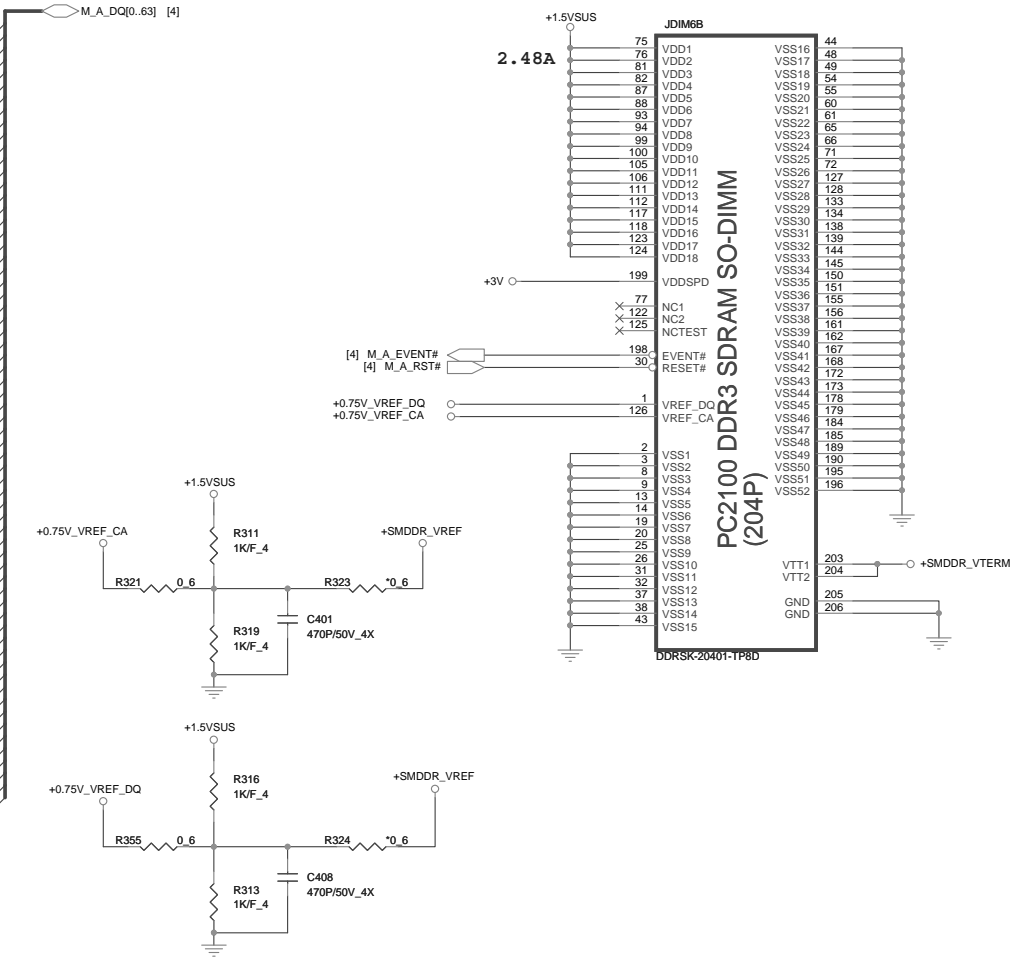
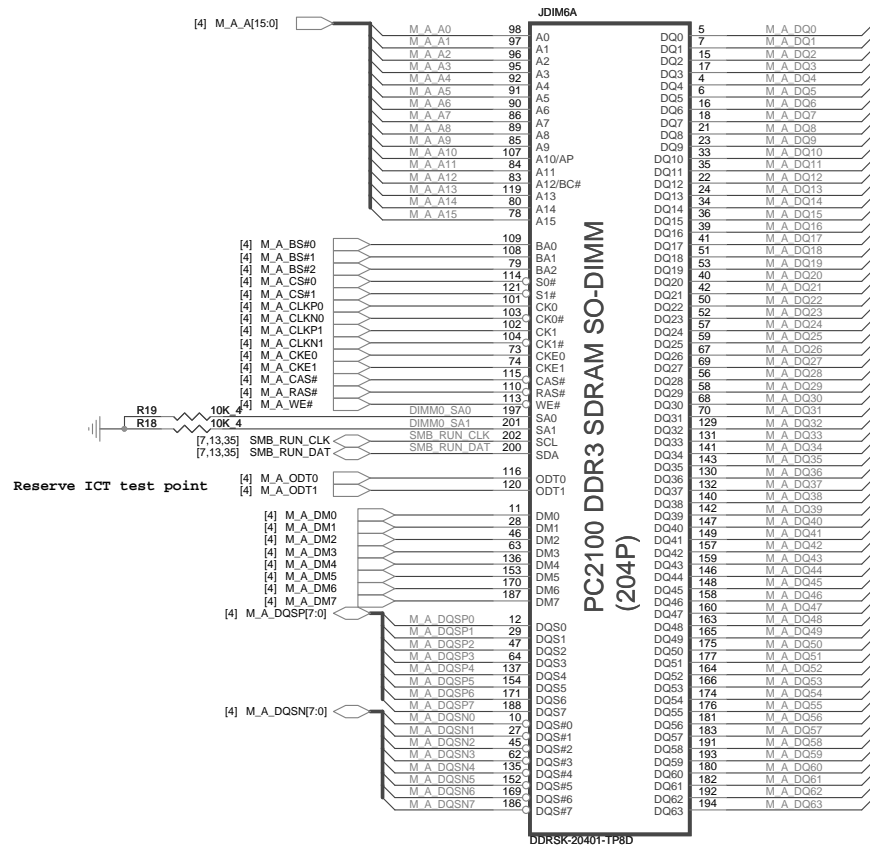
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

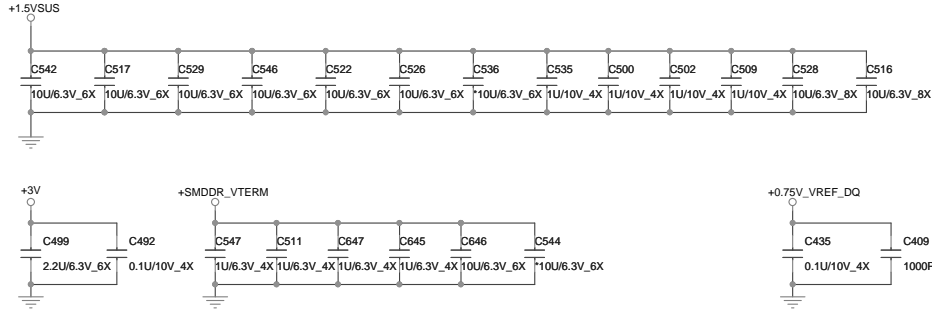


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

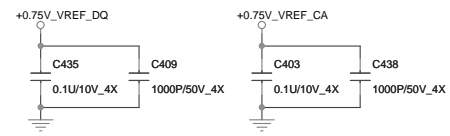
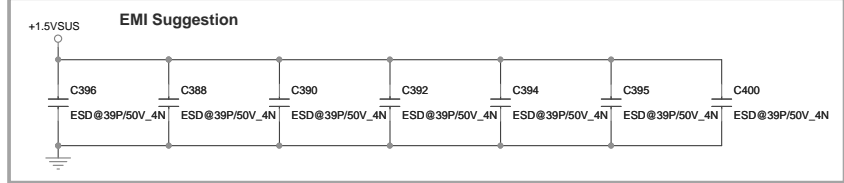
Quanta Computer Inc.
 PROJECT : BY6/BY6D
 Document Number: **FCH 5/5(STRAP & PWRGD)**
 Date: Tuesday, February 14, 2012 Sheet 11 of 47



Place these Caps near So-Dimm0.



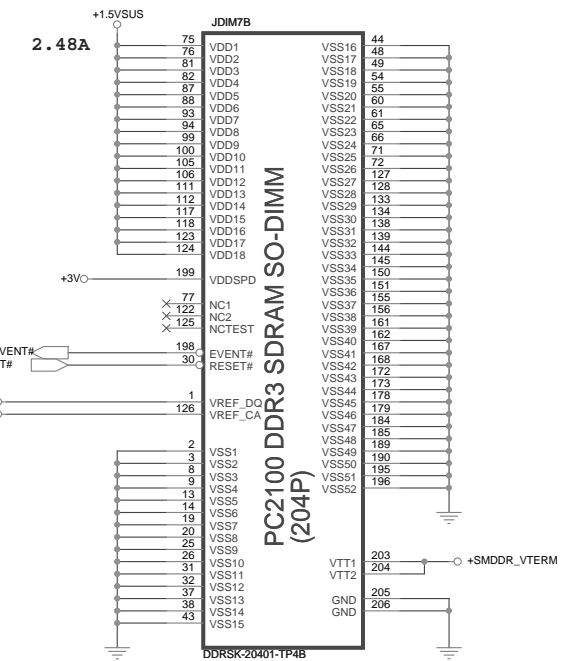
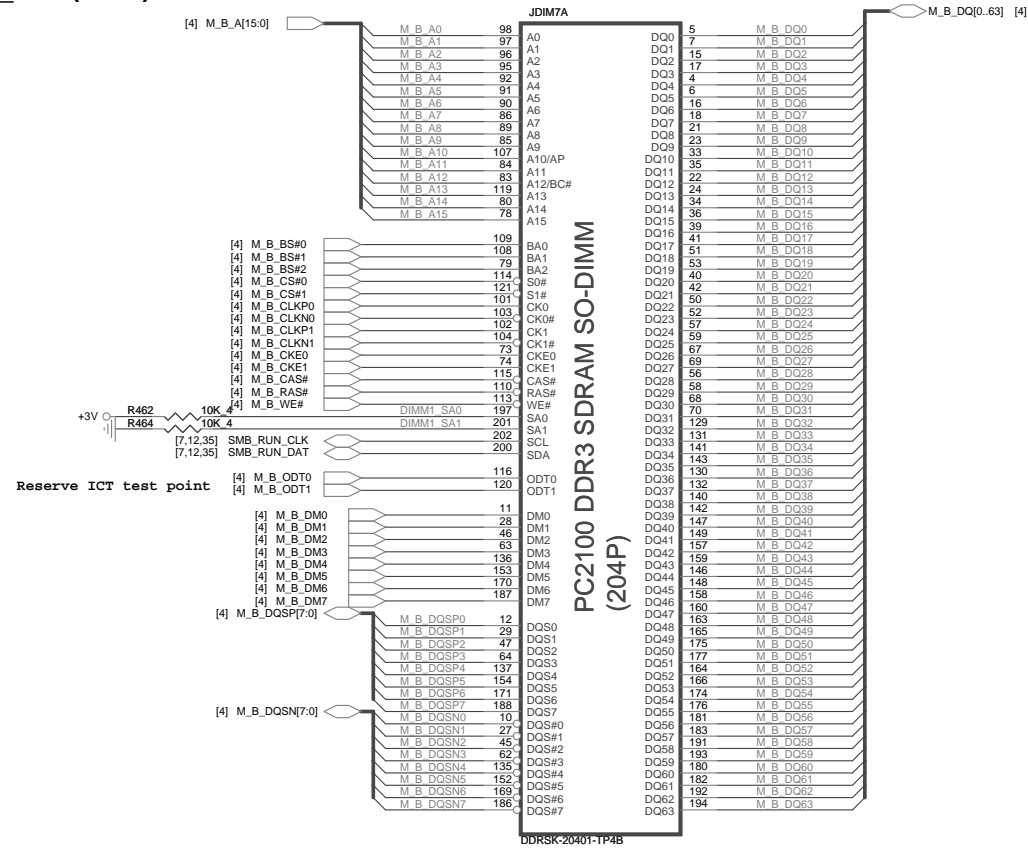
D3A



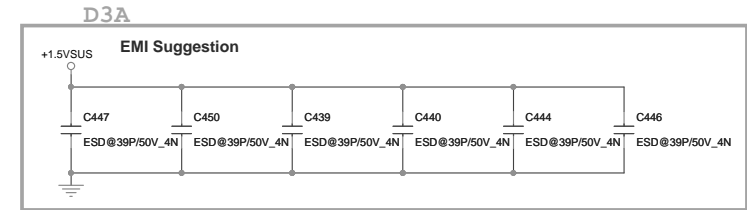
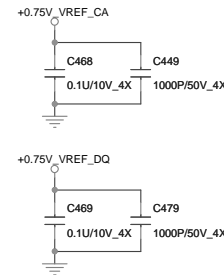
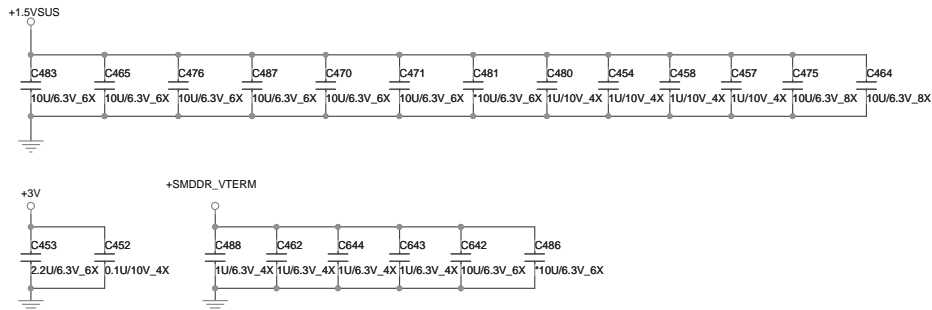
Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	DDR3 DIMM-1	1A
Date:	Tuesday, February 14, 2012	Sheet 12 of 47

DDR_RVS (DDR)



Place these Caps near So-Dimm1.



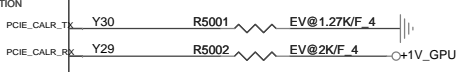
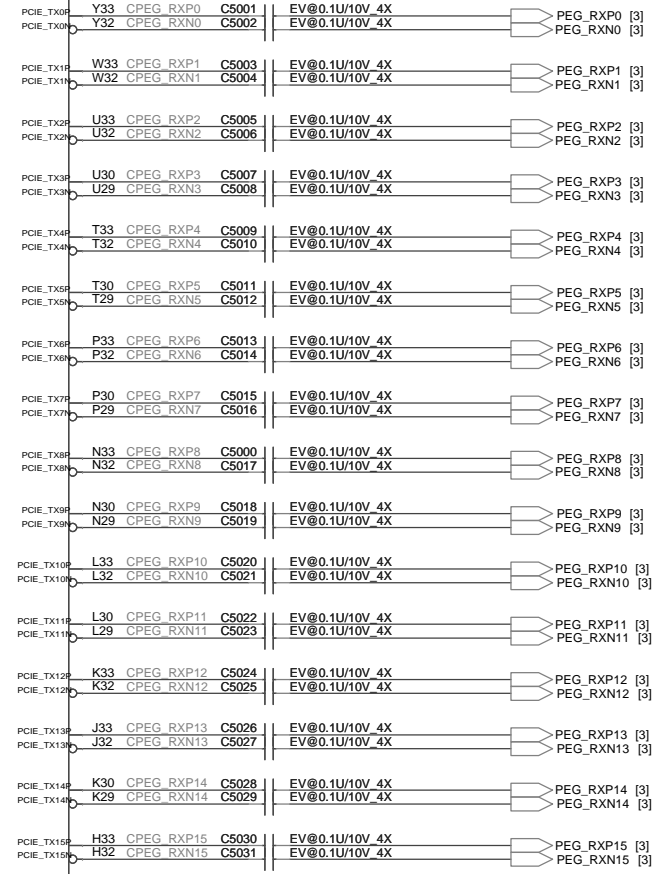
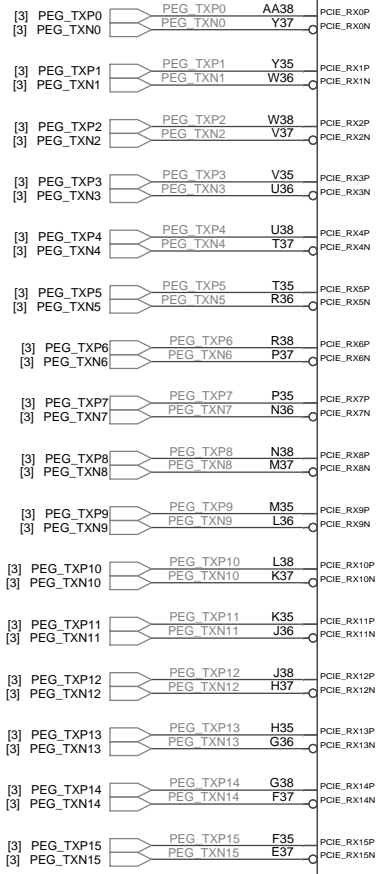
<VGA>

U6000A

PART 1 OF 9

PCI EXPRESS INTERFACE

EV@HEATHROW M2



Thames and Seymour Power-on sequence

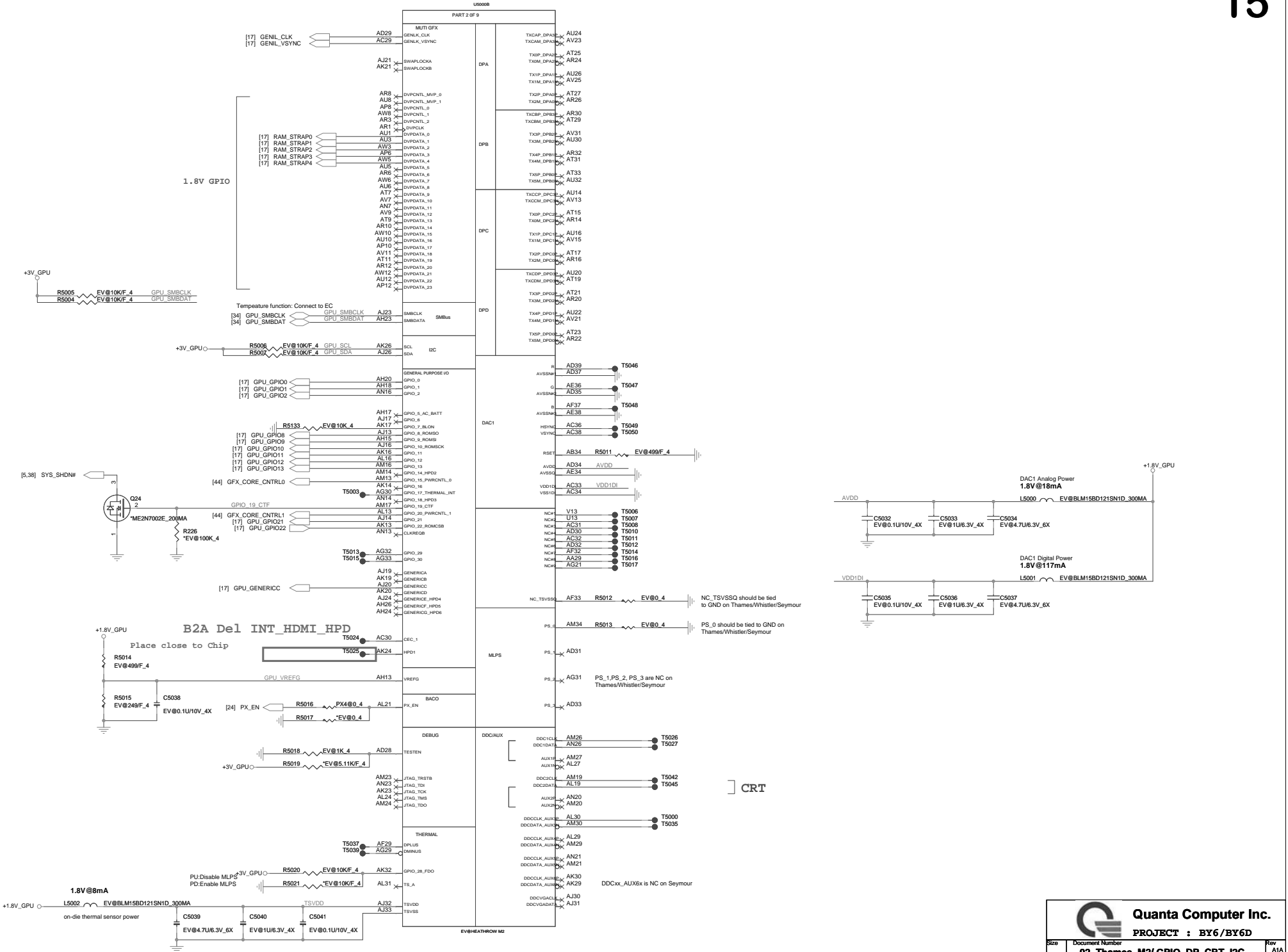
- 1 => +1V_GPU
- 2 => +3V_GPU
- 3 => +VGPU_CORE,+1.5V_GPU
- 4 => +1.8V_GPU

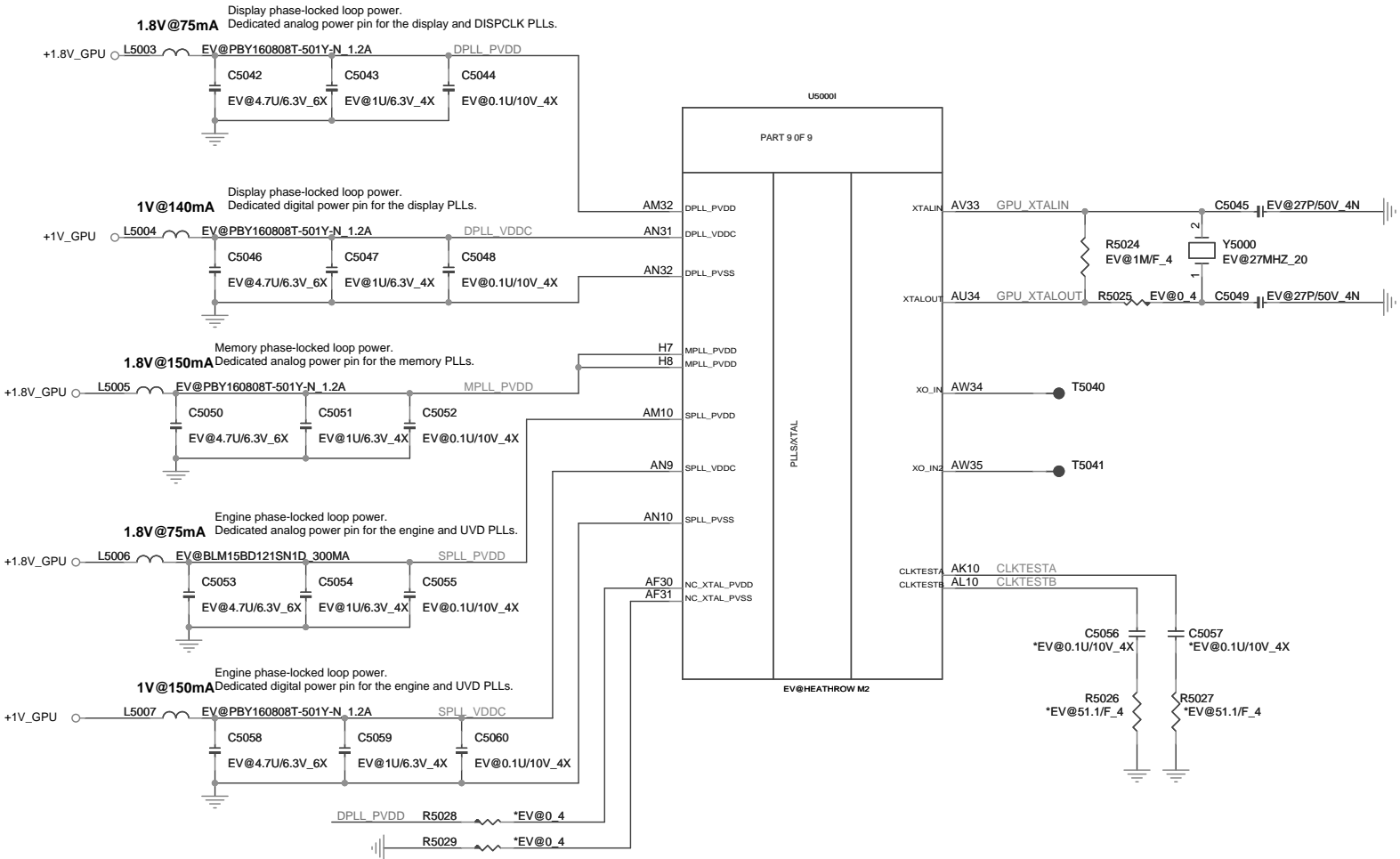
PEG

Intel platform: Lane0 ~ Lane15
 Brazos platform: Lane12 ~ Lane15
 Comal and Sabine platform: Lane8 ~Lane15

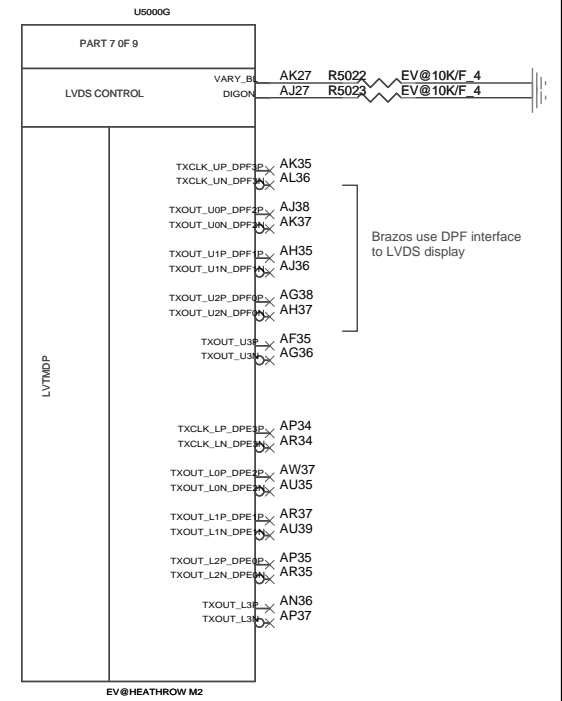
Quanta Computer Inc.
 PROJECT : BY6/BY6D


Size	Document Number	Rev
	Thames_M2/PEG*16	A1A
Date:	Monday, February 13, 2012	Sheet 14 of 47



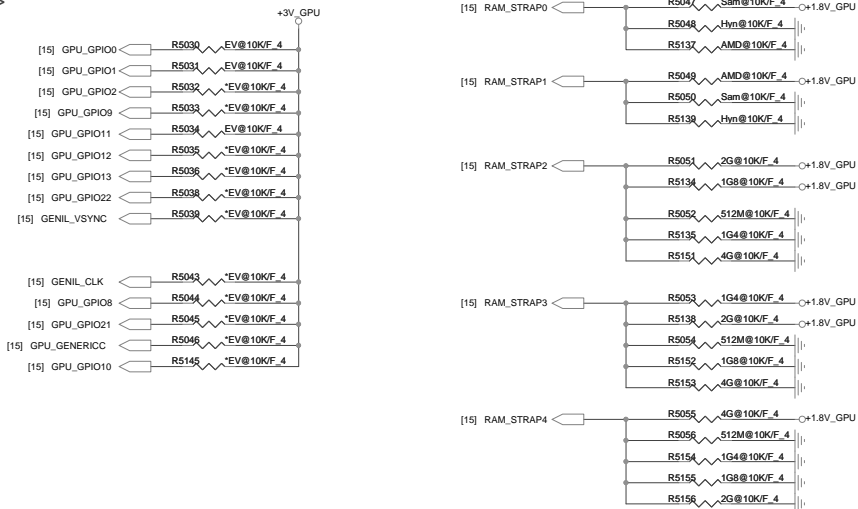


DPE/DPF/LVDS



		
Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number	Rev
	Thames M2/ XTAL_LVDS	A1A
Date:	Monday, February 13, 2012	Sheet 16 of 47

<VGA>



DDR3 Memory TYPE

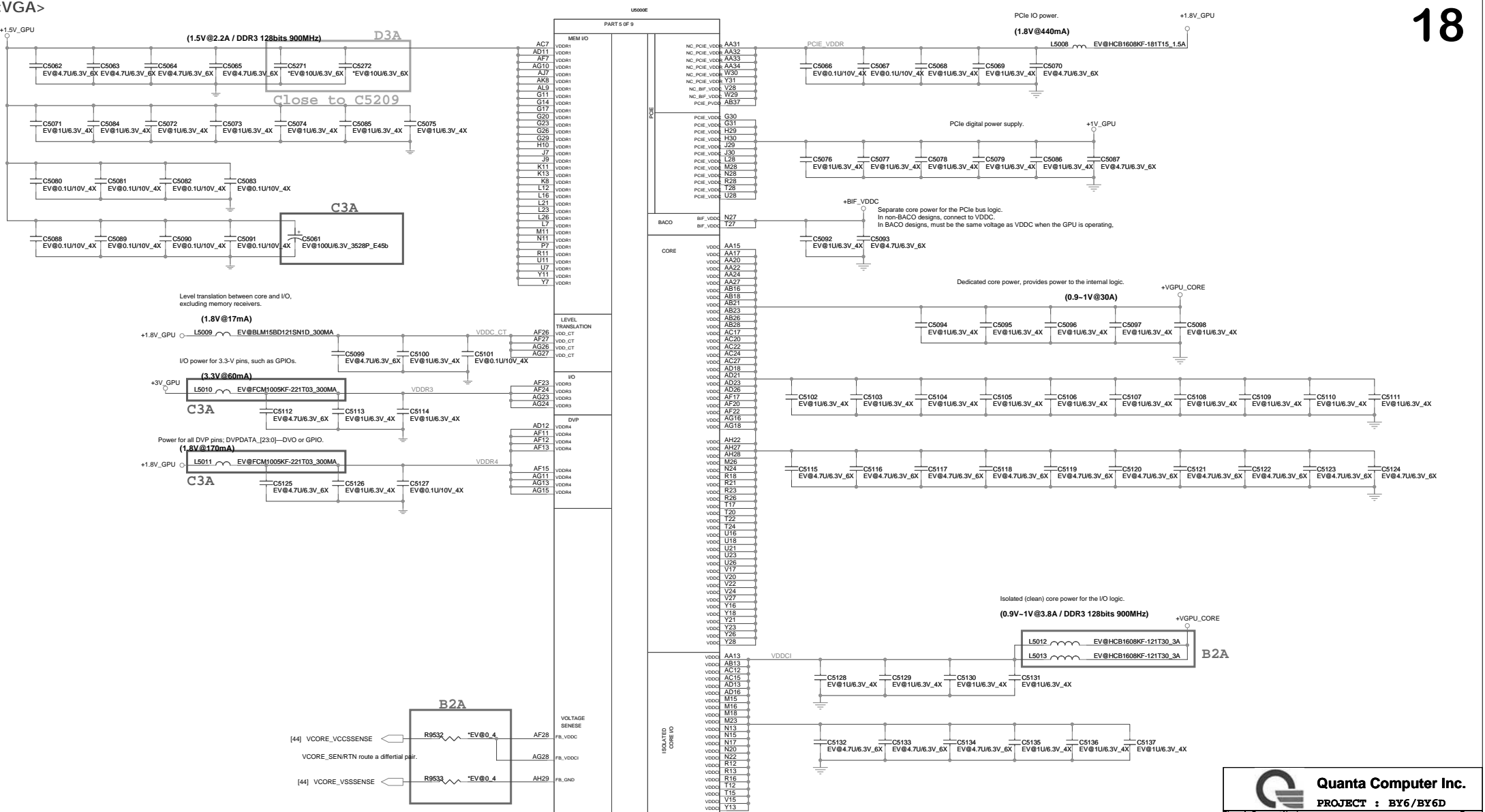
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP4 DVPDATA_4	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZWTW02 * 4	512MB	0	0	0	0	0
		AKD5LZWTW02 * 8	1GB	0	0	1	0	0
	H5TQ2G63BFR-11C (128M*16)	AKD5MGWTW00 * 4	1GB	0	1	0	0	0
		AKD5MGWTW00 * 8	2GB	0	1	1	0	0
	H5TQ4G***** (256M*16)	AK***** * 8	4GB	1	0	0	0	0
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 4	512MB	0	0	0	0	1
		AKD5EGGT500 * 8	1GB	0	0	1	0	1
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 4	1GB	0	1	0	0	1
		AKD5MGWT500 * 8	2GB	0	1	1	0	1
	K4W4G***** (256M*16)	AK***** * 8	4GB	1	0	0	0	1
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 4	512MB	0	0	0	1	0
		AKD5EZWT700 * 8	1GB	0	0	1	1	0
	23EY4187MC11 (128M*16)	AKD5DZWT700 * 4	1GB	0	1	0	1	0
		AKD5DZWT700 * 8	2GB	0	1	1	1	0
		23EY***** (256M*16)	AK***** * 4	4GB	1	0	0	1

CONFIGURATION STRAPS - SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS. NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3:1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512bit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA	GENLK_CLK GPIO6 GPIO1 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

System Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1

EEPROM



Quanta Computer Inc.
PROJECT : BY6/BY6D

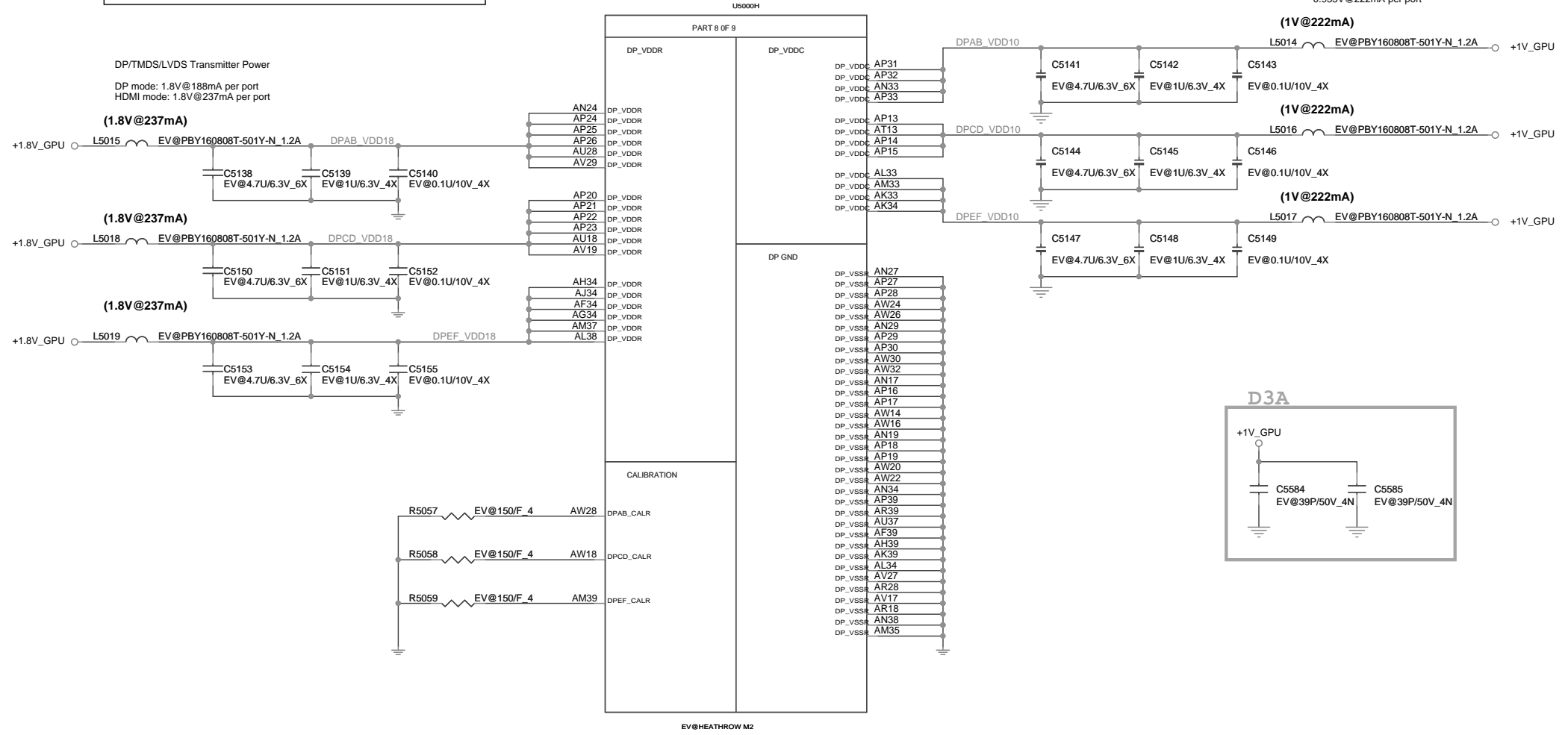
Size	Document Number	Rev
	Thames_M2/ MainPower	A1A
Date:	Monday, February 13, 2012	Sheet 18 of 47

<VGA>

For Thames/Whistler/Seymour
 a dedicated BEAD is required
 for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

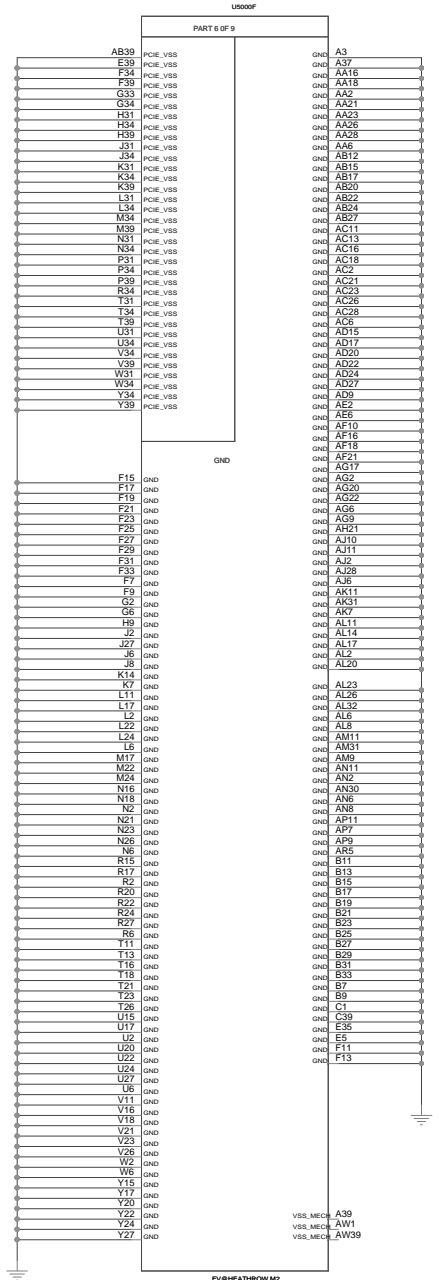
For Thames/Whistler/Seymour
 a dedicated BEAD is required
 for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
 0.935V@222mA per port



Quanta Computer Inc.
 PROJECT : BY6/BY6D

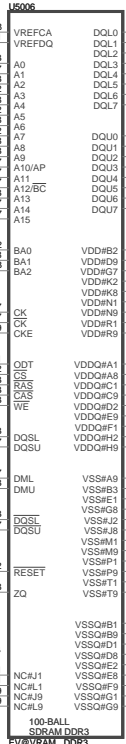
Size	Document Number	Rev
	Thames M2/ DP_Powers	A1A
Date:	Monday, February 13, 2012	Sheet 19 of 47



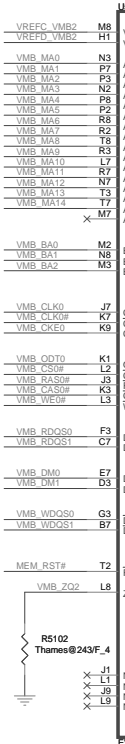
CHANNEL B: 512MB DDR3 (64M*16*4pcs) <VGA>

- [21] VMB_DQ[63..0] VMB_DQ[63..0]
- [21] VMB_DM[7..0] VMB_DM[7..0]
- [21] VMB_RDQS[7..0] VMB_RDQS[7..0]
- [21] VMB_WDQS[7..0] VMB_WDQS[7..0]
- [21] VMB_MA[14..0] VMB_MA[14..0]

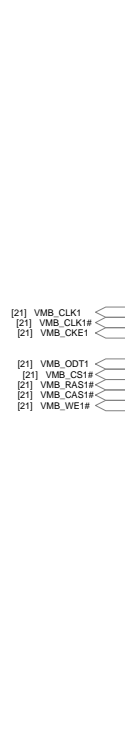
QSA# [7..0]
QSA# [7..0]



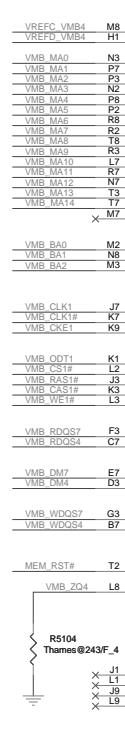
BOT Down



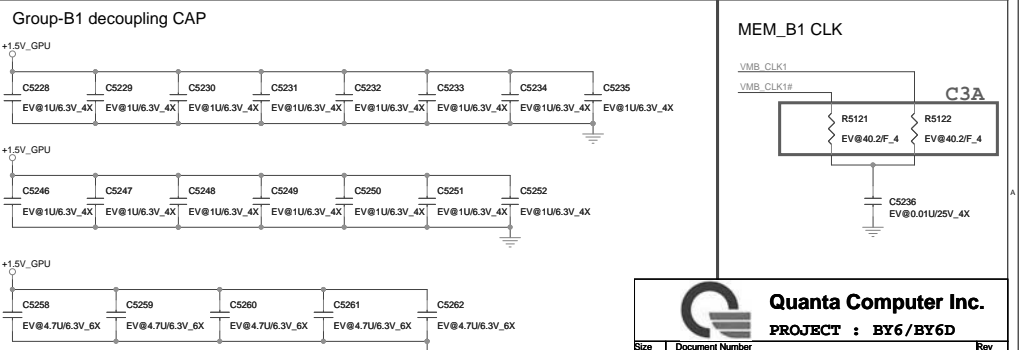
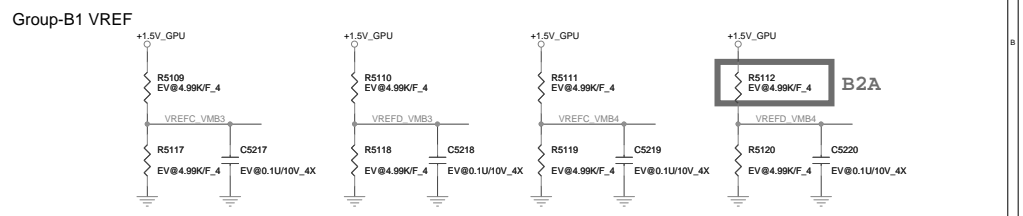
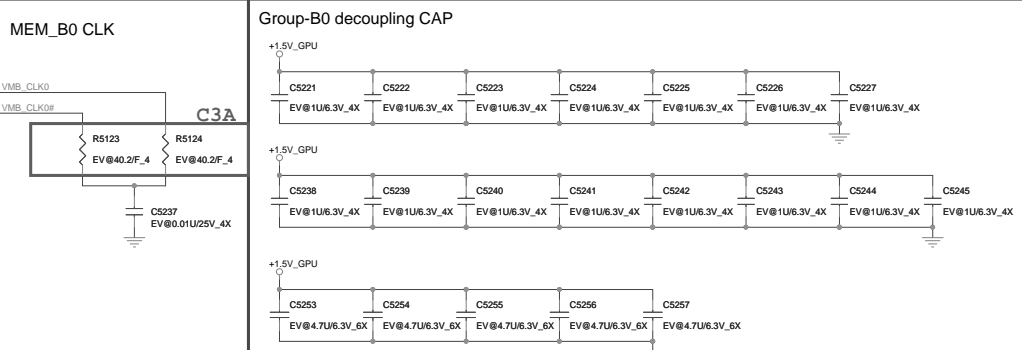
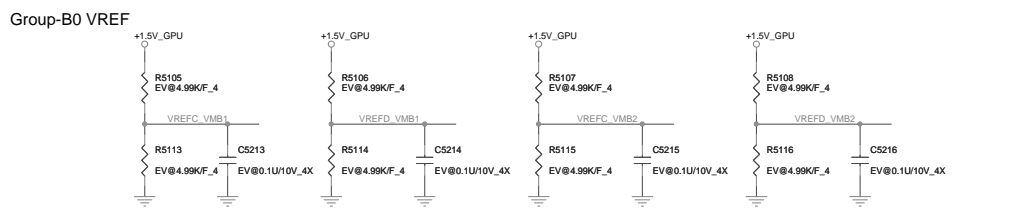
TOP Down

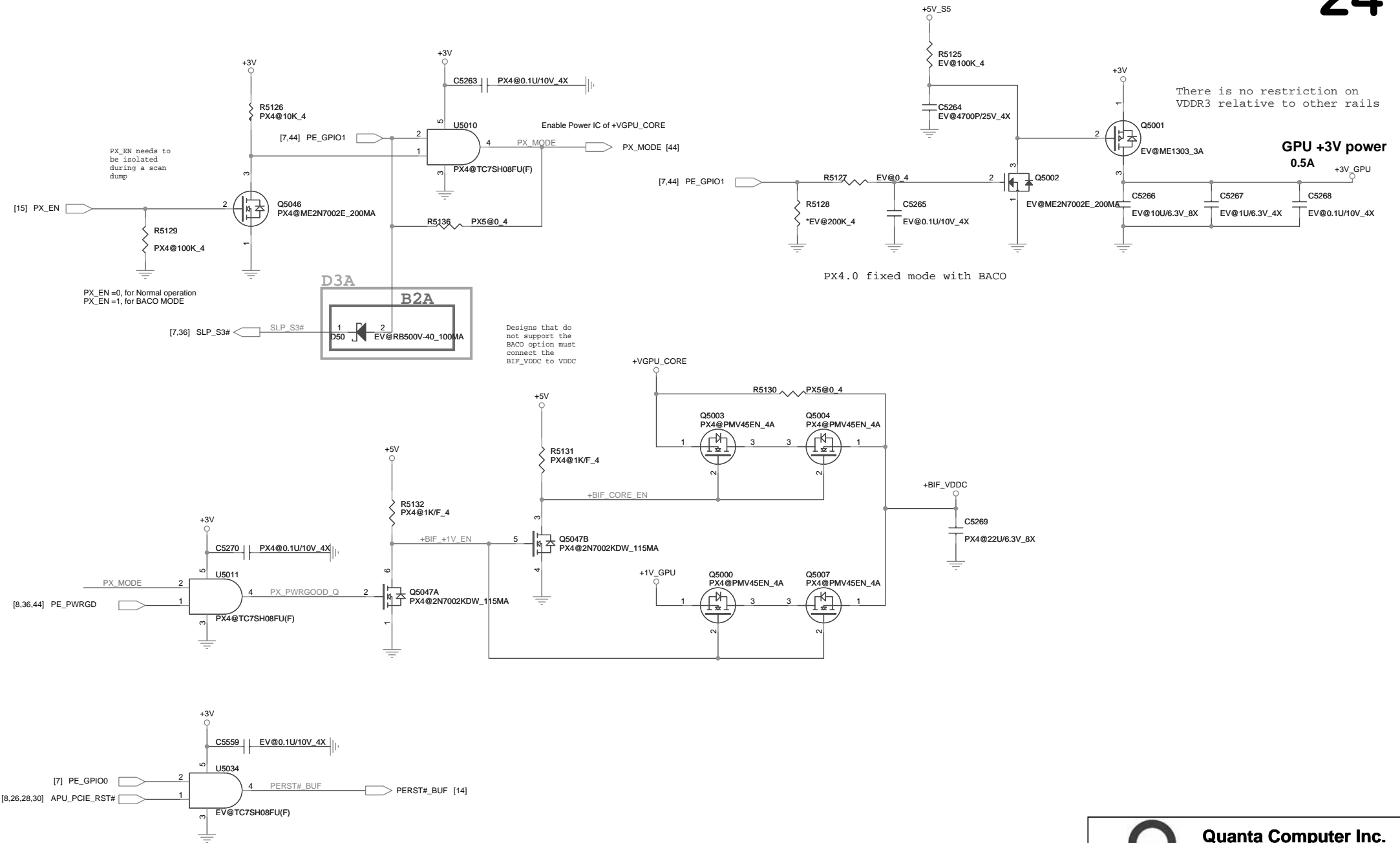


TOP Up

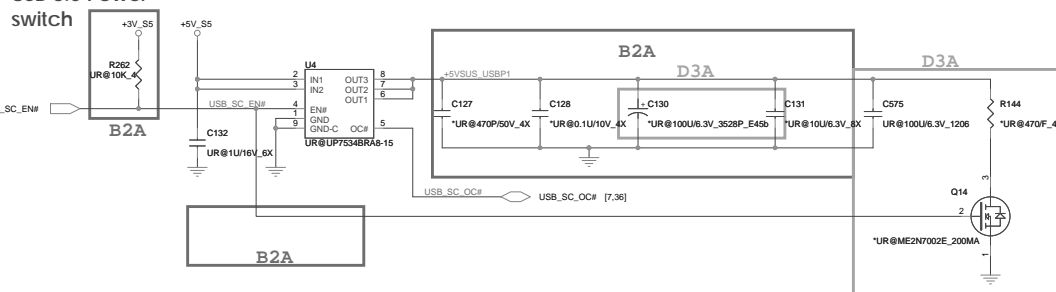


BOT Up

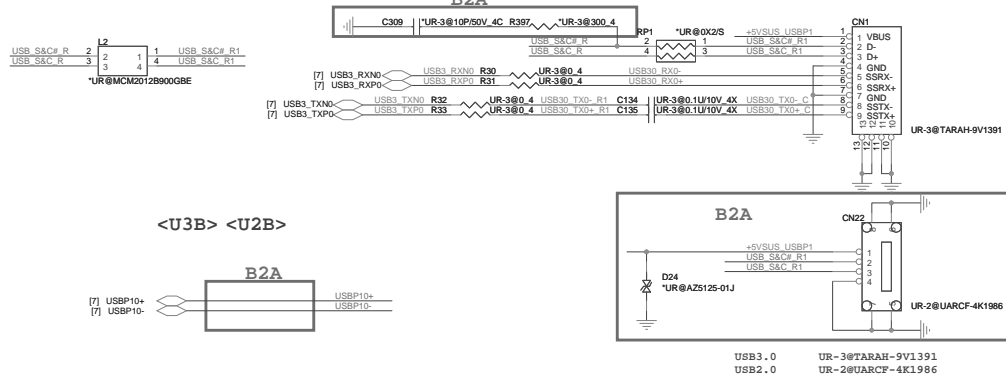




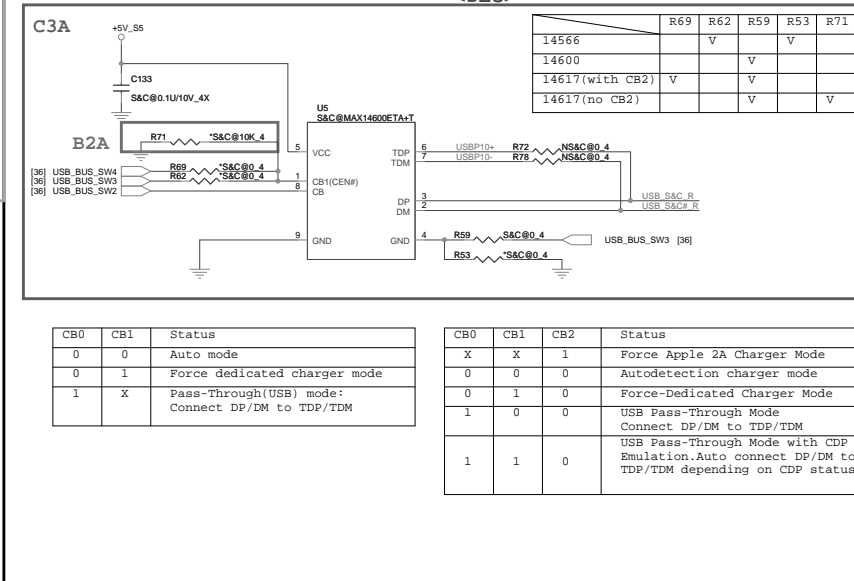
USB 3.0 Power switch <USB> <U3B>



USB 3.0 CONN <U3B> <USB> <EMI>



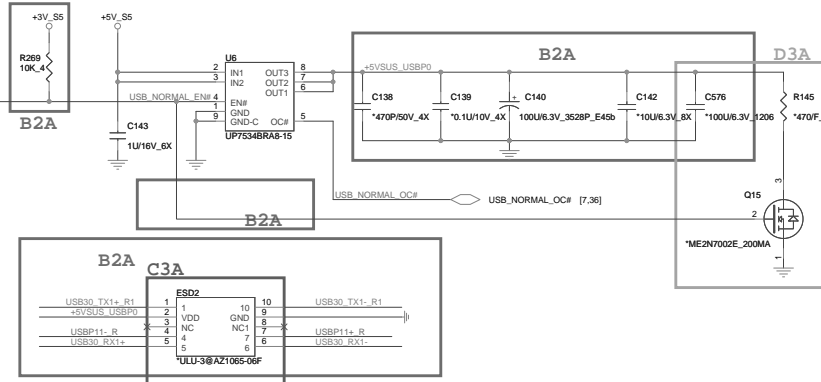
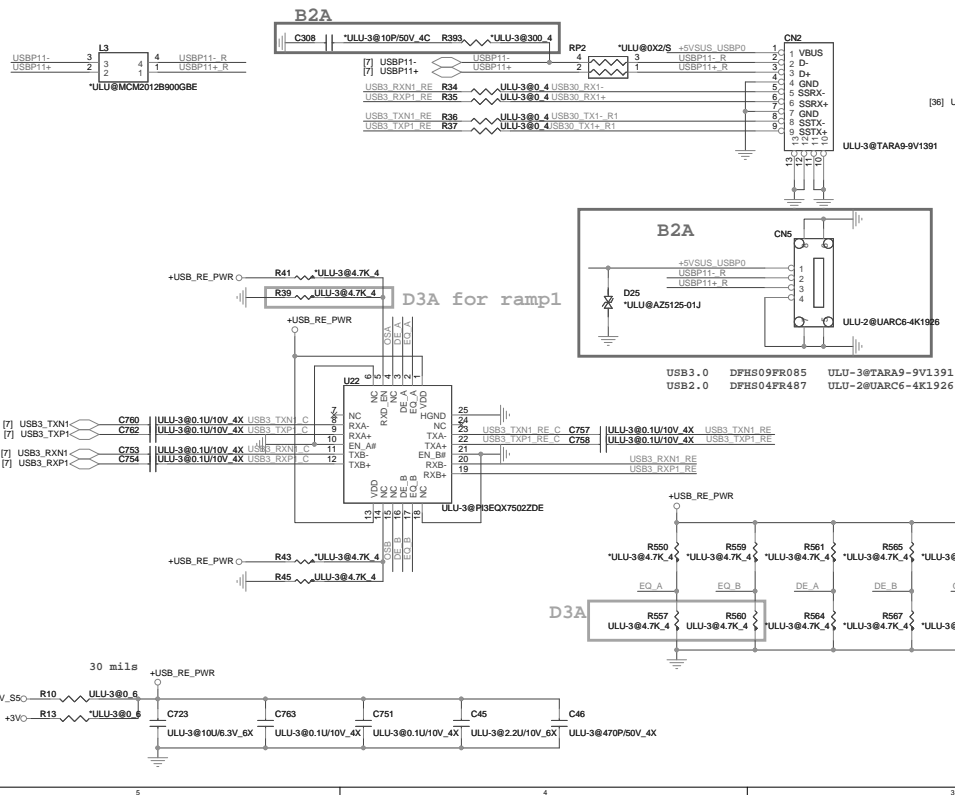
USB w S&C MAXIM solution <SLC>



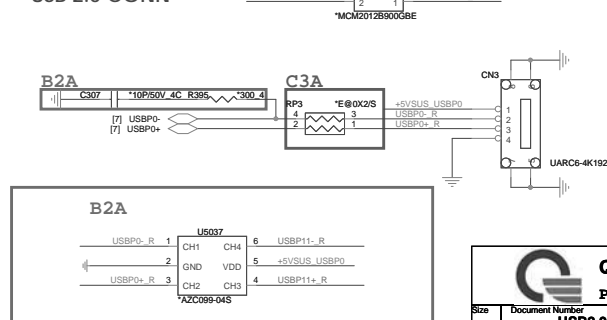
14566	R69	R62	R59	R53	R71
14600		V	V	V	
14617(with CB2)	V		V		
14617(no CB2)			V		V

CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

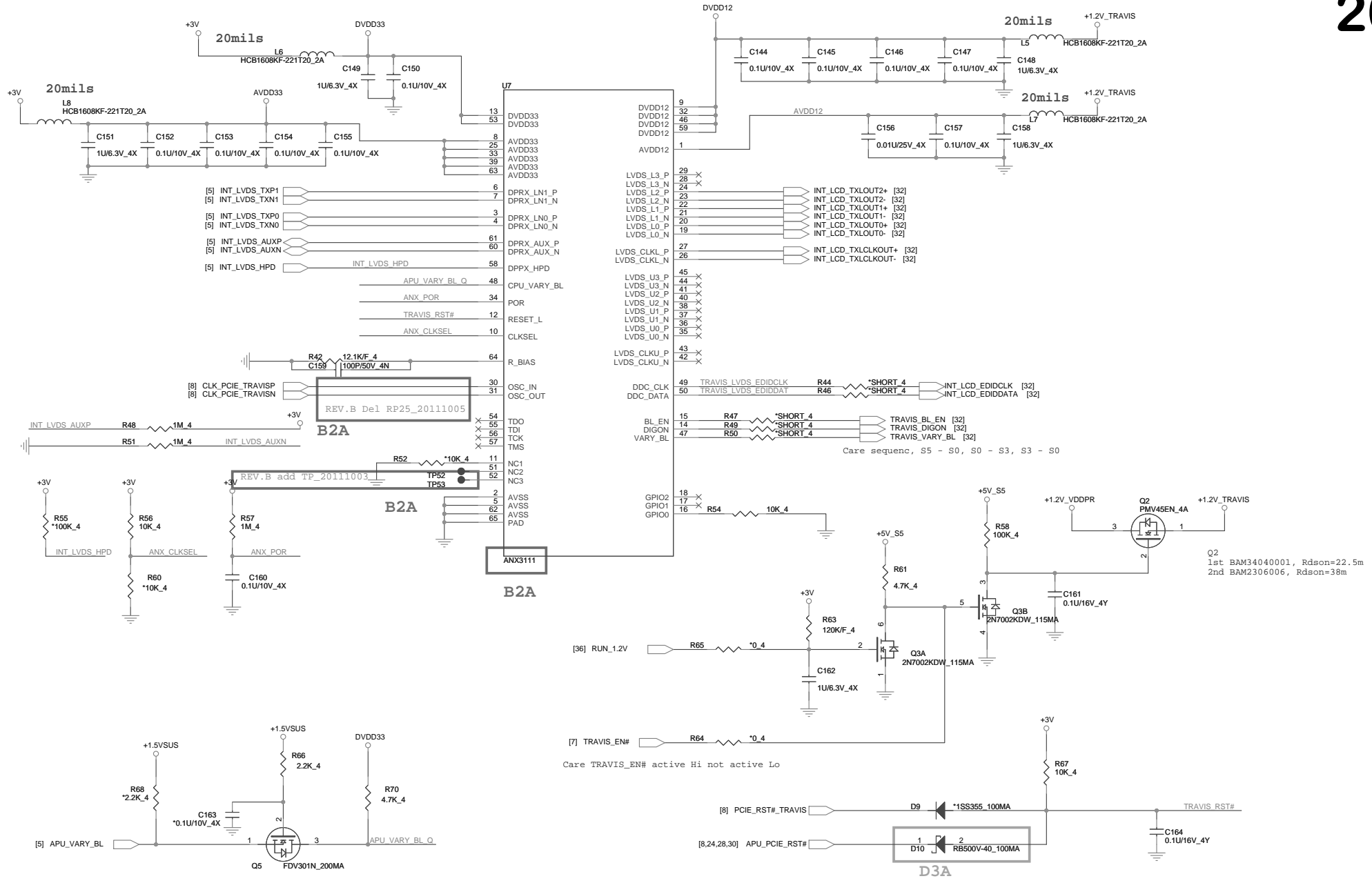
CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status



USB 2.0 CONN



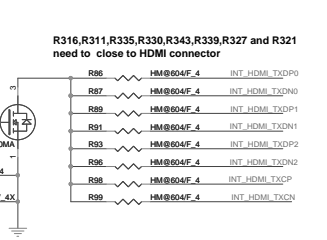
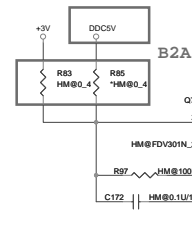
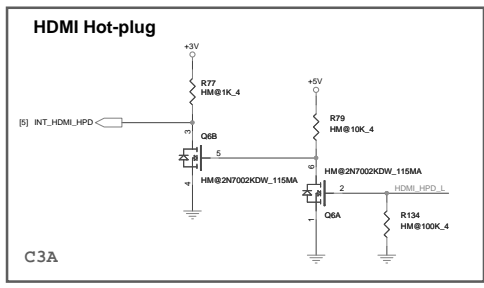
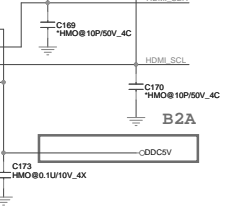
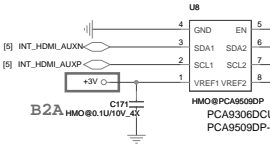
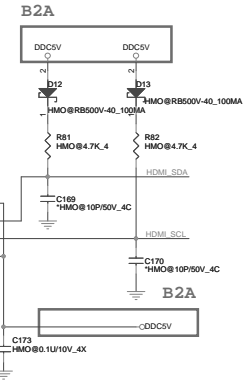
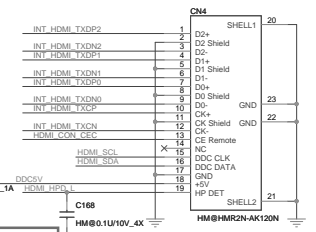
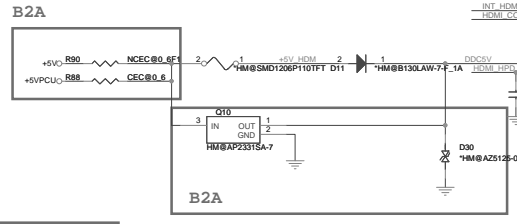
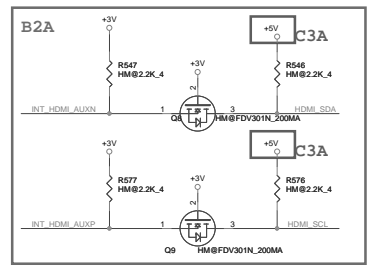
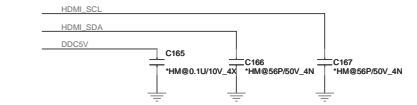
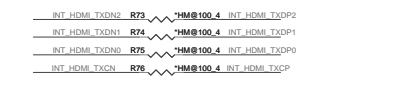
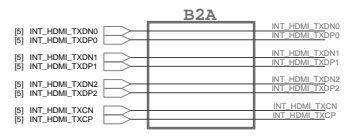
Quanta Computer Inc.
PROJECT :BY6/BY6D
USB2.0/USB3.0
 Size: _____ Document Number: _____ Rev: 1A
 Date: Tuesday, February 14, 2012 Sheet 25 of 47



Quanta Computer Inc.
PROJECT : BY6/BY6D

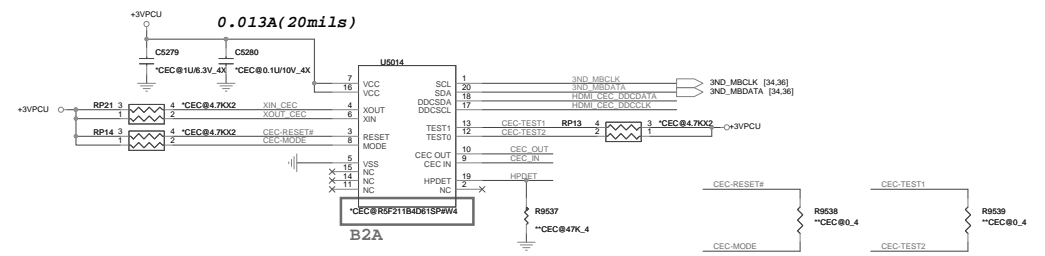
Size	Document Number	Rev
	TRAVIS ANX3110	1A
Date:	Tuesday, February 14, 2012	Sheet 26 of 47

HDMI

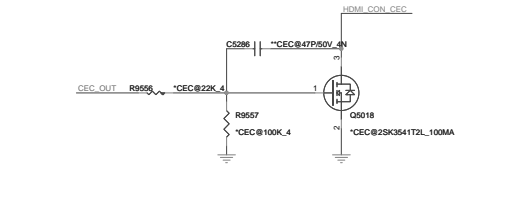


R316, R311, R335, R330, R343, R339, R327 and R321 need to close to HDMI connector

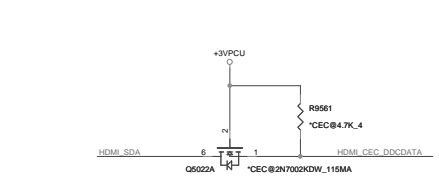
HDMI CEC <CEC>



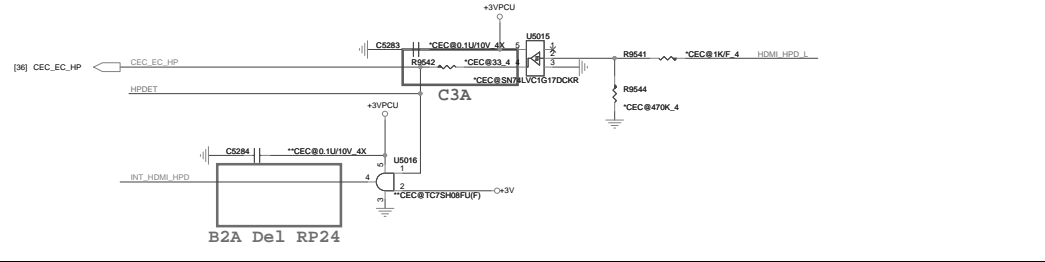
CEC Output <CEC> (To Connect)



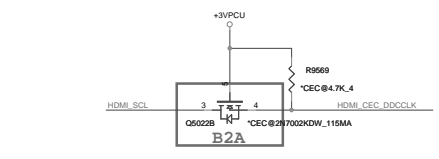
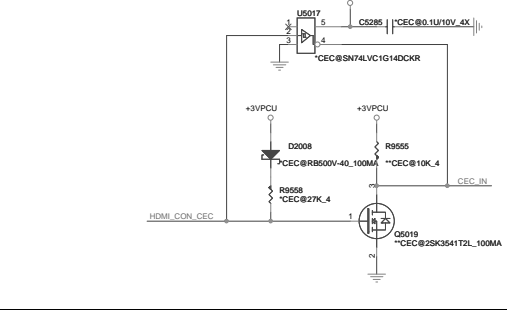
CEC SMBus Level <CEC> (To CECC)



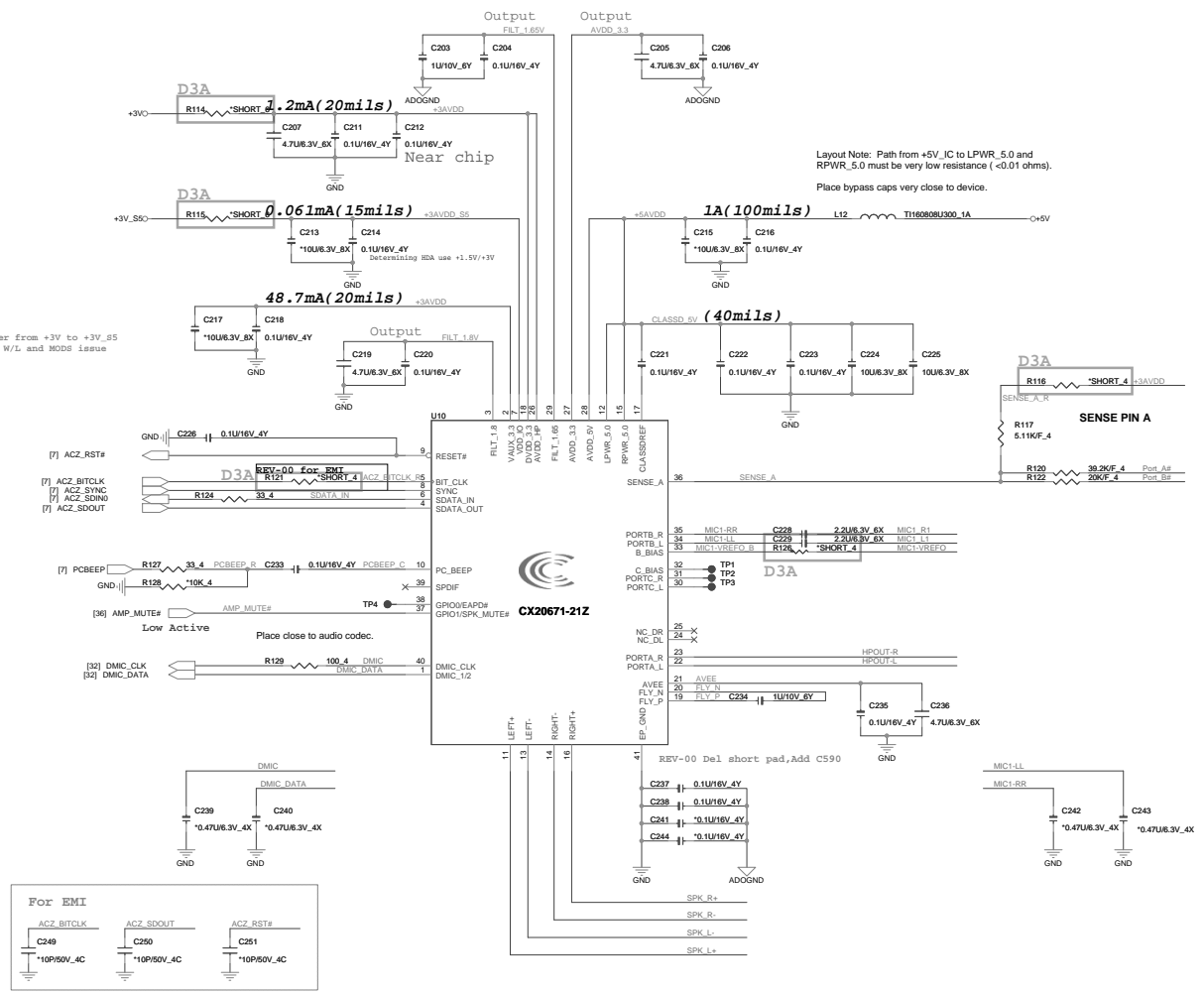
CEC HotPlug <CEC>



CEC Input <CEC> (To CECC)

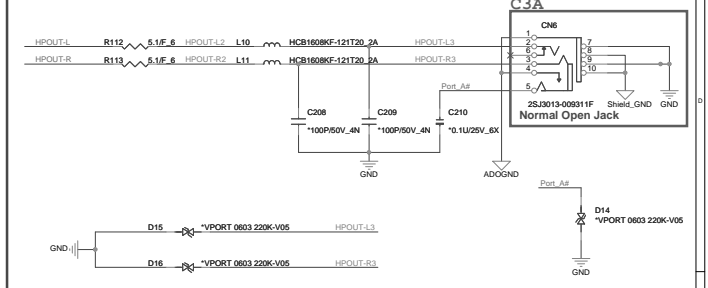


Codec (CX20671-21Z) <ADO> <EMI>

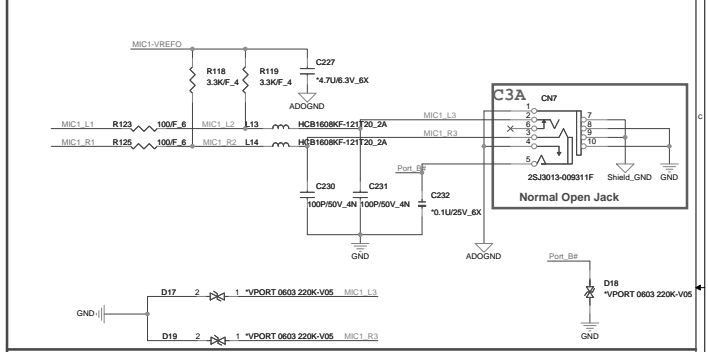


Modify Power From +3V to +3V_S5
for fixing W/L and MODS Issue

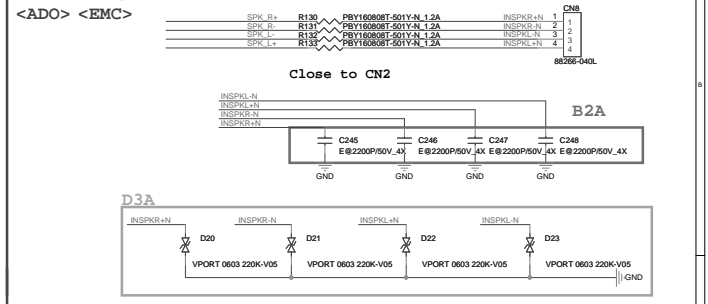
HP <ADO> <EMC>



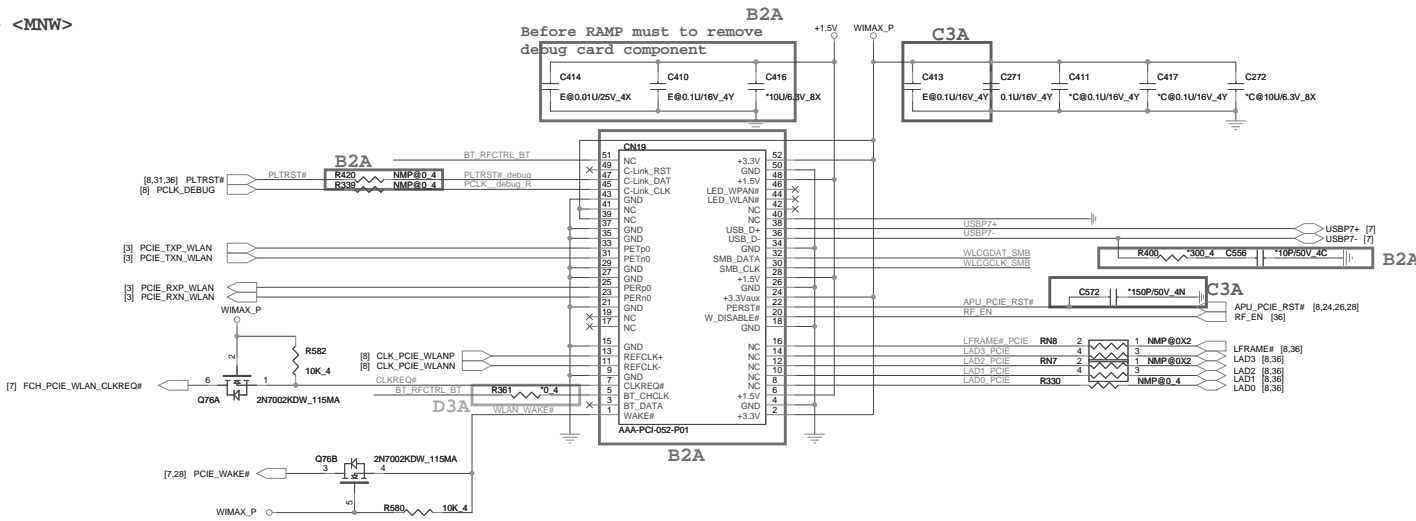
External MIC <ADO> <EMC>



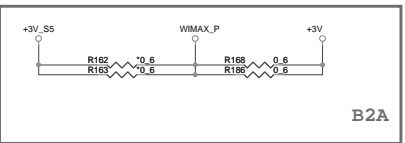
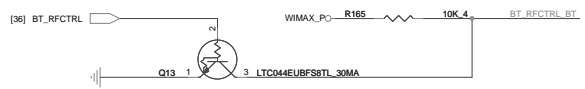
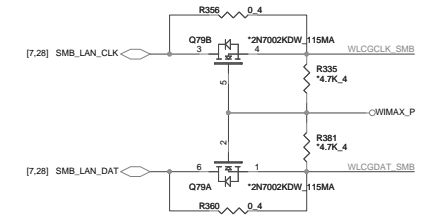
Internal Speaker <ADO> <EMC>



MINI Card Slot#1 <MNW>
(WiFi)

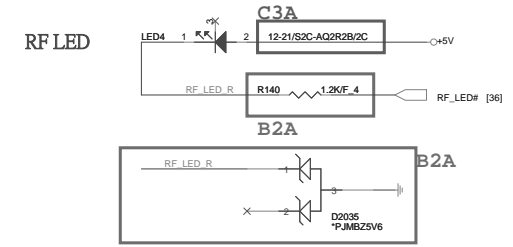
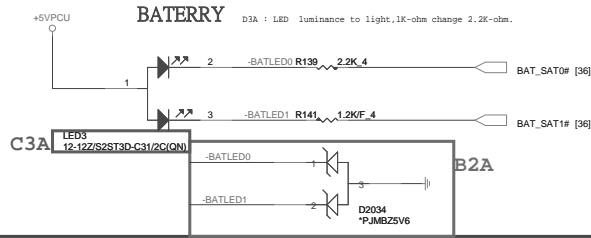
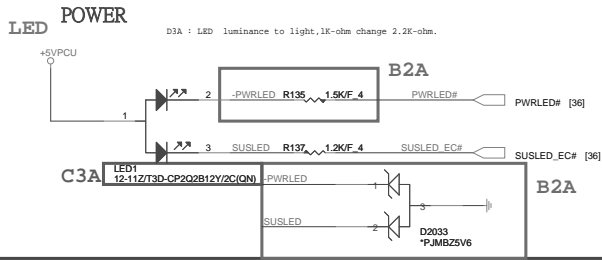


SMBus(DDR3/WLAN/3G)



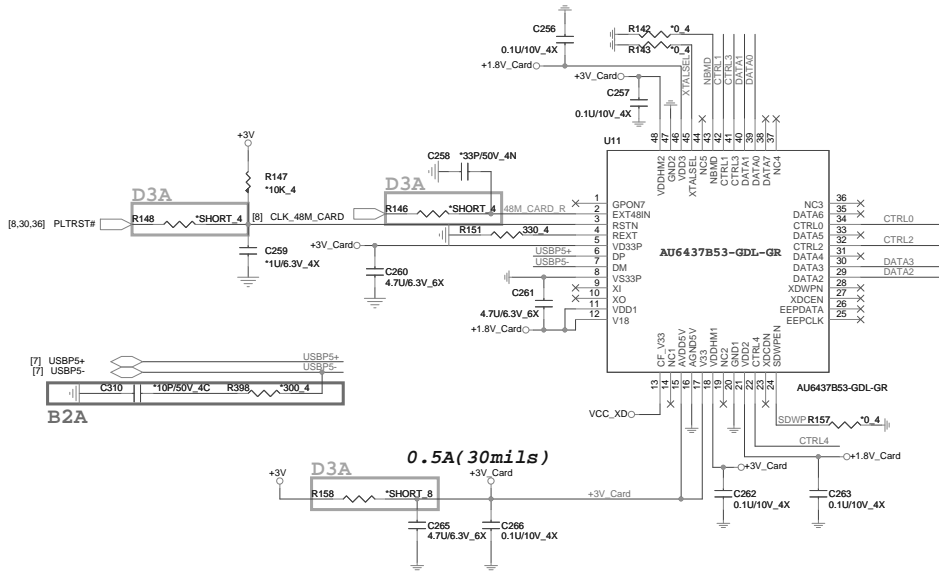
Quanta Computer Inc.
PROJECT : BY6/BY6D

Size: Document Number: MINI CARD Rev: 1A
Date: Tuesday, February 14, 2012 Sheet: 30 of 47



3 IN 1 CARD READER (Type: MS/MMC/SD) <MMC>

Card Reader (AU6437B53-GDL-GR)



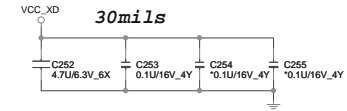
Clock input selection
 1 : 48MHz input (default)
 0 : 12MHz input

NBMD Power saving mode enable
 1 : enable (default)
 0 : disable

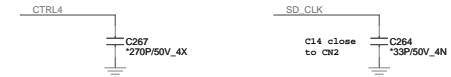
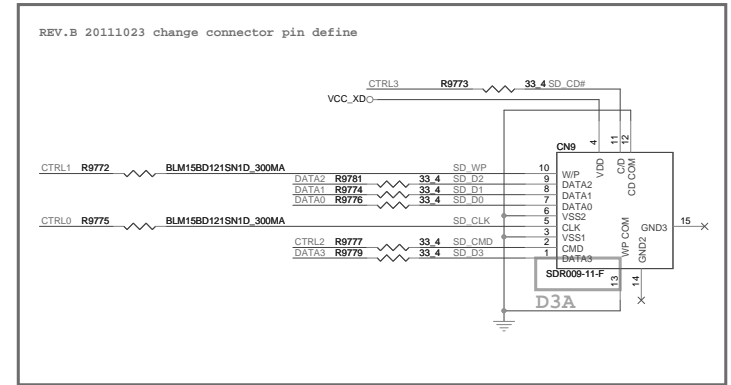
CTRL0 trace surround with GND

	SD	XD	MS
CTRL0	SDCLK	XDALE	MSBS
CTRL1	SDWP	XDCLE	MSCLK
CTRL2	SDCMD	XDRBD	
CTRL3	SDCDN	XDRWN	
CTRL4		XDRDN	MSINS

SD write protect enable
 1 : decided by SDWP(default)
 0 : SD always write-able



B2A



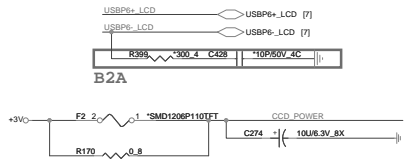
Quanta Computer Inc.

PROJECT : BY6/BY6D

Size	Document Number	Rev
	CARD READER/LED	1A

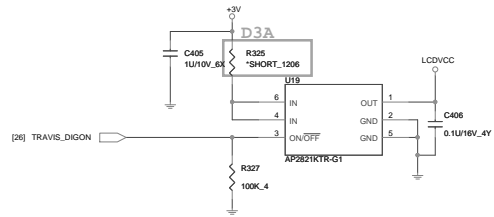
Date: Tuesday, February 14, 2012 Sheet 31 of 47

CCD [CCD]



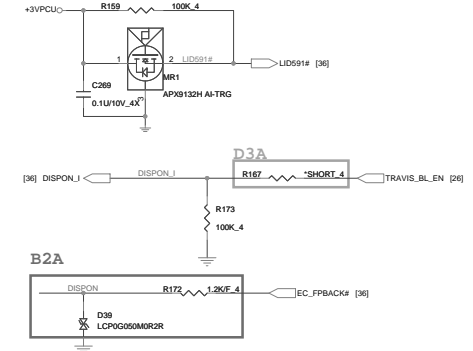
LCD POWER SWITCH

<LDS>

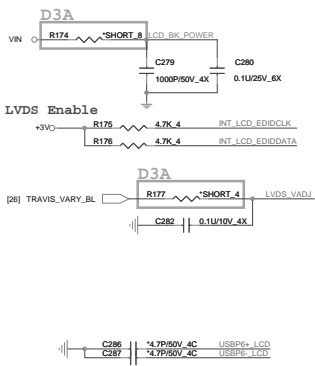


HALL SENSOR&BACK LIGHT SWITCH

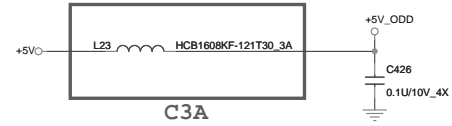
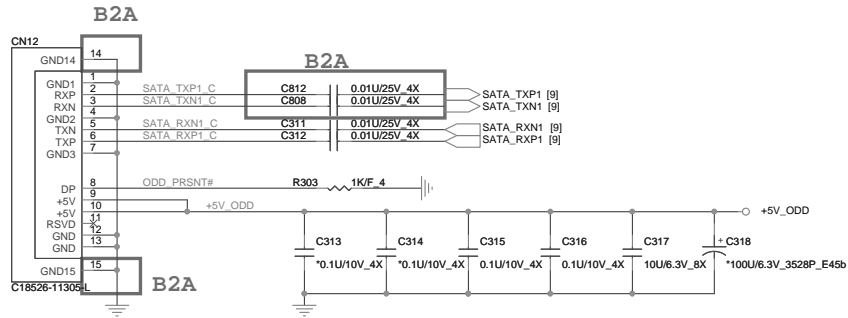
<HSR>



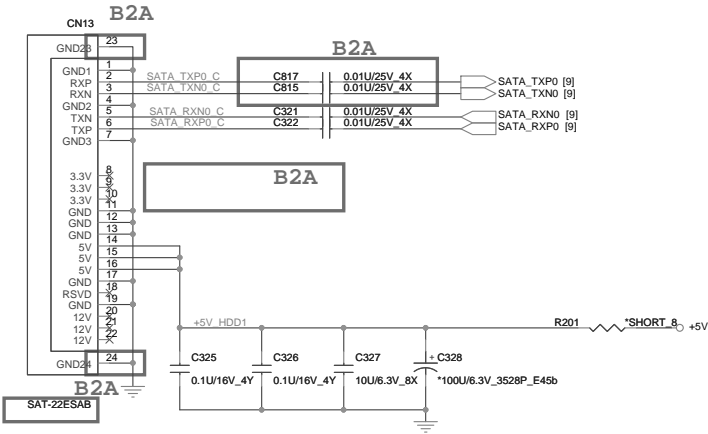
LCD Panel Module [LDS]



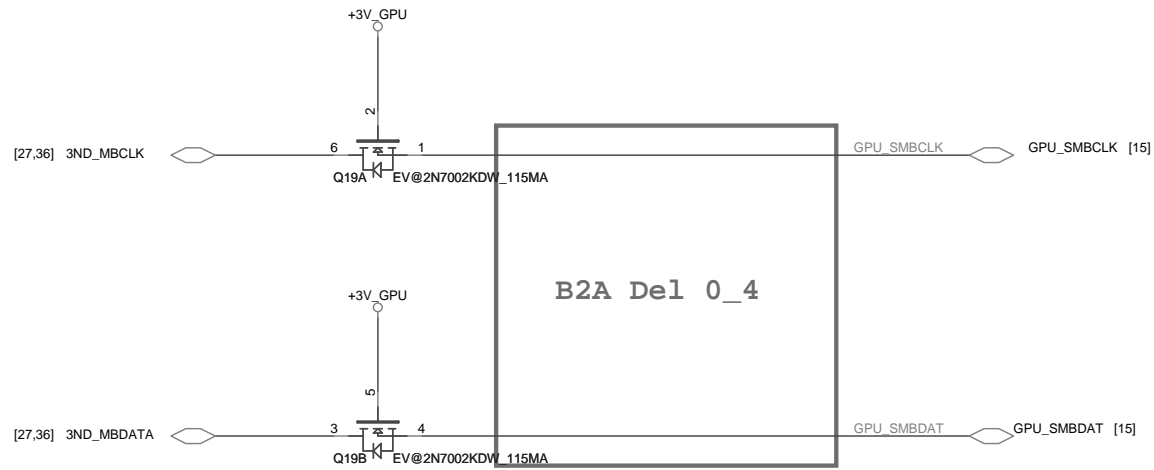
SATA ODD [ODD]



SATA HDD [HDD]

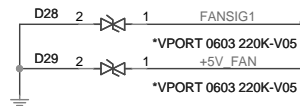
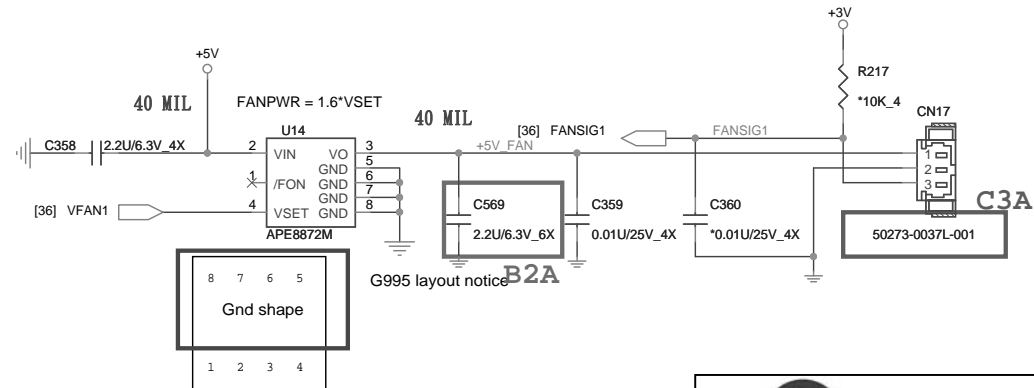


Thermal Sensor <THC>



Thermal	Ext Thermal	dGPU Int Thermal
EC(M) 3ND_SMB	U13	
EC(M) 3ND_SMB		dGPU int SMBUS
dGPU(M) SMB	U13	dGPU int SMBUS

FAN Control <THC>



Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	THERMAL	1A

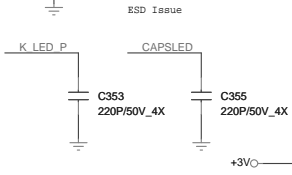
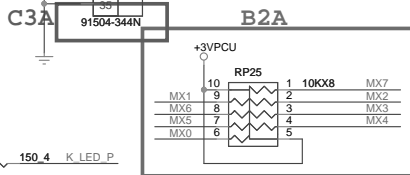
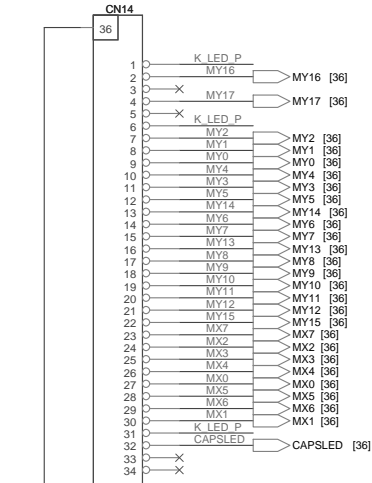
Date: Tuesday, February 14, 2012 Sheet 34 of 47

KEY BOARD Connector <KBC> <EMI>

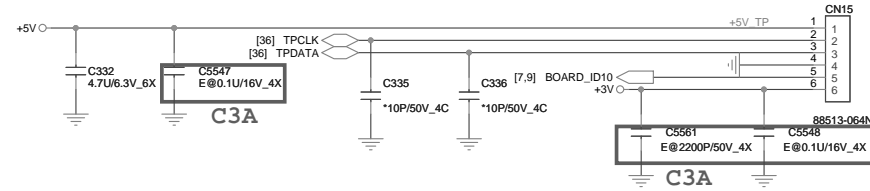
INT KeyBoard

D3A

C329	ESD@39P/50V_4N	MX7
C330	ESD@39P/50V_4N	MX2
C331	ESD@39P/50V_4N	MX3
C333	ESD@39P/50V_4N	MX4
C337	ESD@39P/50V_4N	MX0
C338	ESD@39P/50V_4N	MX5
C339	ESD@39P/50V_4N	MX6
C340	ESD@39P/50V_4N	MX1
C341	ESD@39P/50V_4N	MY7
C342	ESD@39P/50V_4N	MY13
C343	ESD@39P/50V_4N	MY12
C344	ESD@39P/50V_4N	MY15
C345	ESD@39P/50V_4N	MY3
C346	ESD@39P/50V_4N	MY5
C347	ESD@39P/50V_4N	MY14
C348	ESD@39P/50V_4N	MY6
C349	ESD@39P/50V_4N	MY2
C350	ESD@39P/50V_4N	MY1
C351	ESD@39P/50V_4N	MY0
C352	ESD@39P/50V_4N	MY4
C357	ESD@39P/50V_4N	MY16
C373	ESD@39P/50V_4N	MY17

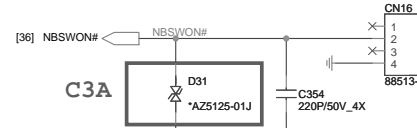


TOUCH PAD BOARD <TPD> <EMI>

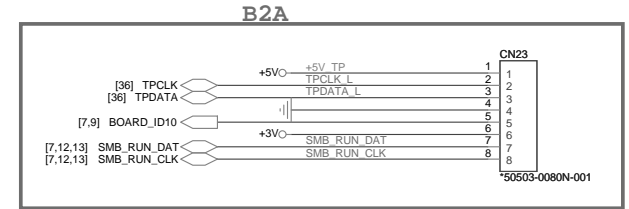


ID_Detect	default
Metal/IMR	H
TEXTURE	L

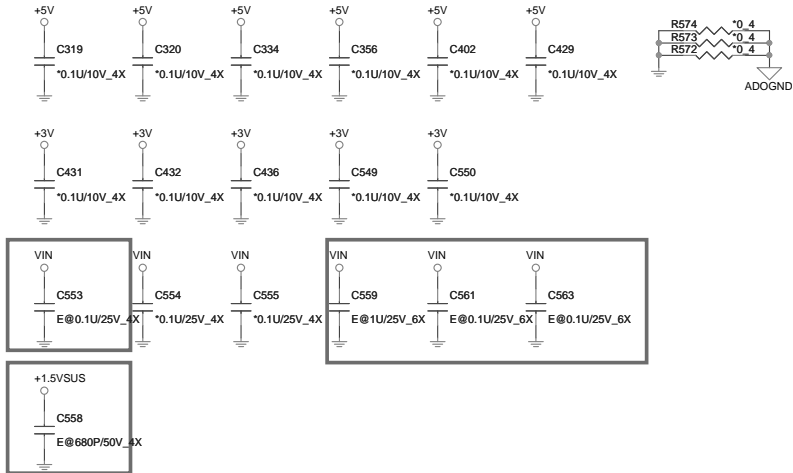
Power Board (UIF) <PSW>



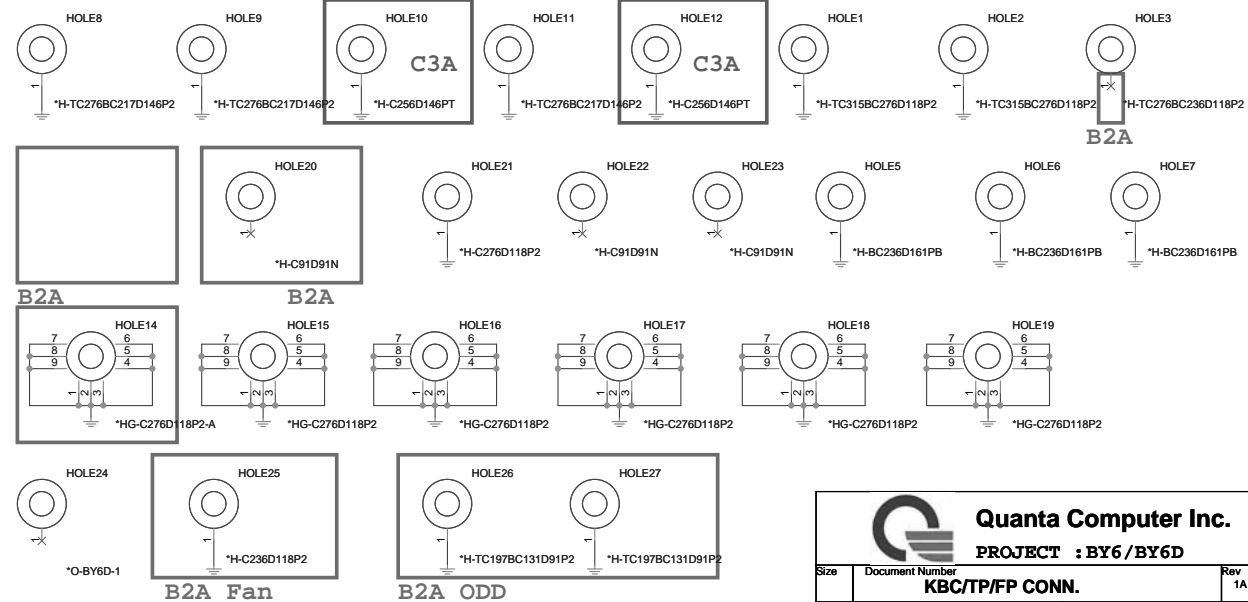
TP board <TPD>



EMI PAD <EMI>



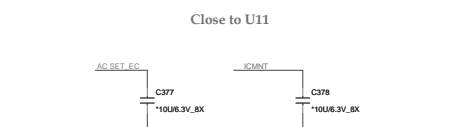
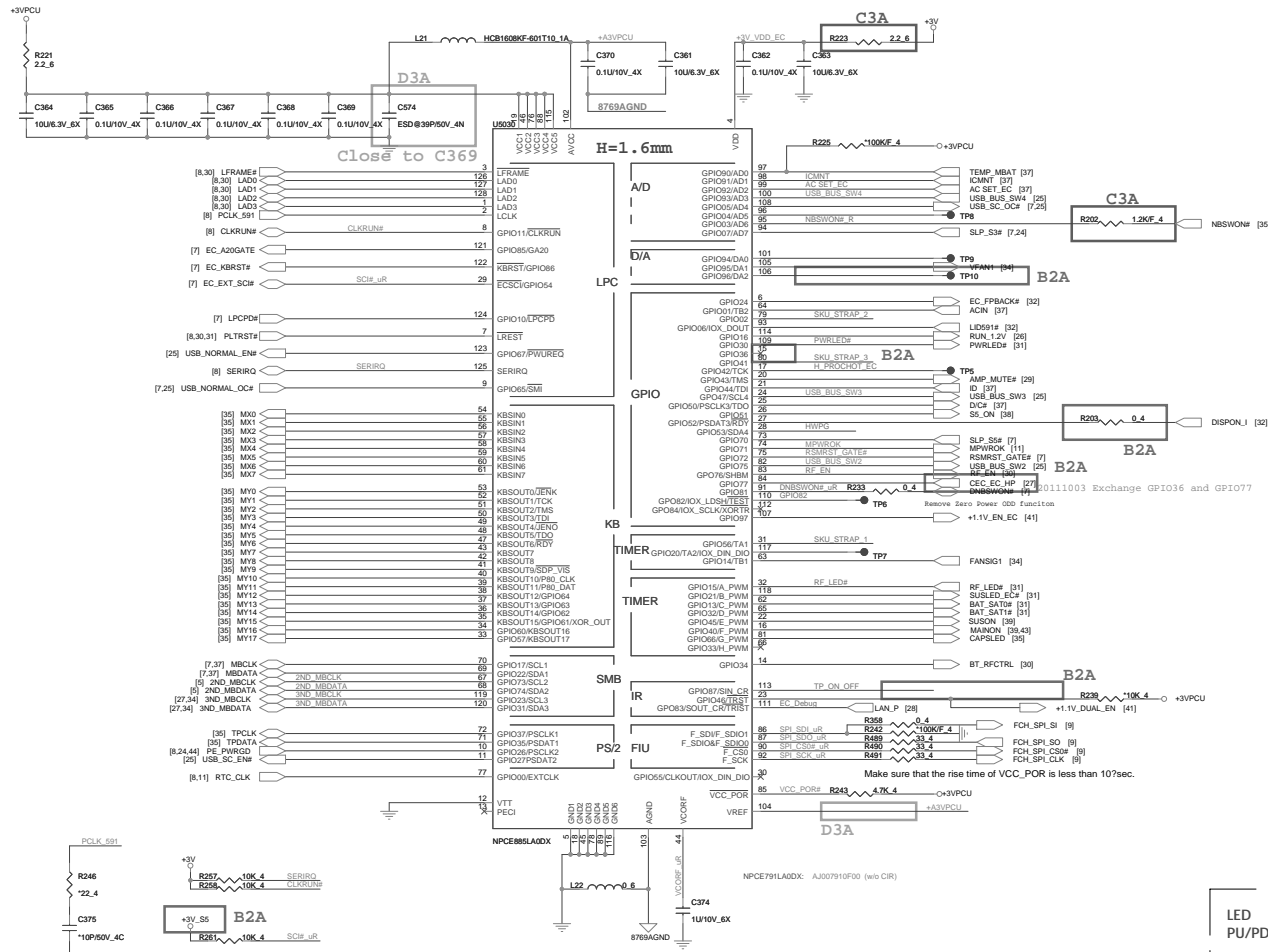
HOLE <OTH>



Quanta Computer Inc.
PROJECT : BY6/BY6D
KBC/TP/FP CONN.

Size	Document Number	Rev
		1A

Date: Tuesday, February 14, 2012 Sheet 35 of 47



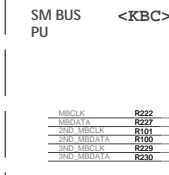
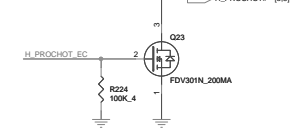
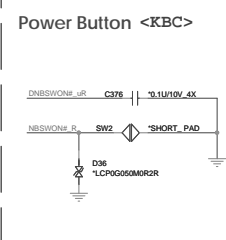
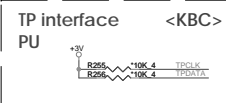
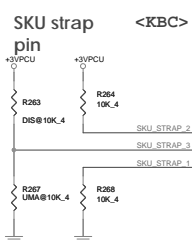
SKU STRAPPING:

Pull H SKU_STRAP_3 For Discrete

Pull L SKU_STRAP_3 For UMA

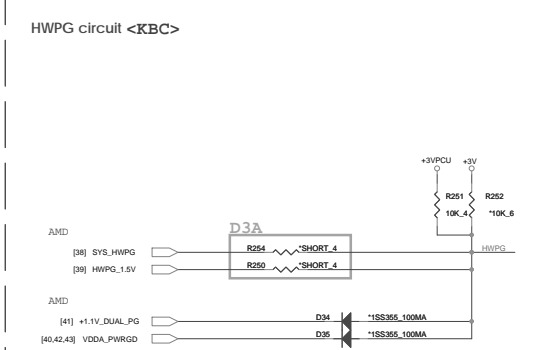
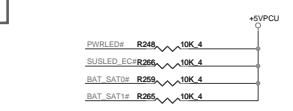
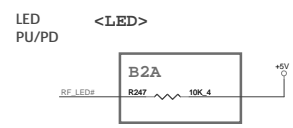
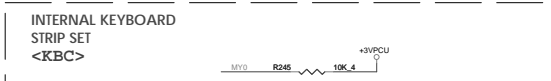
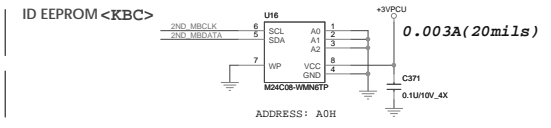
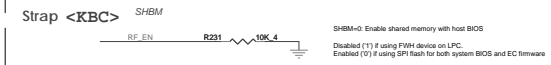
Pull SKU_STRAP_1=Lo&SKU_STRAP_2=Hi For 14"

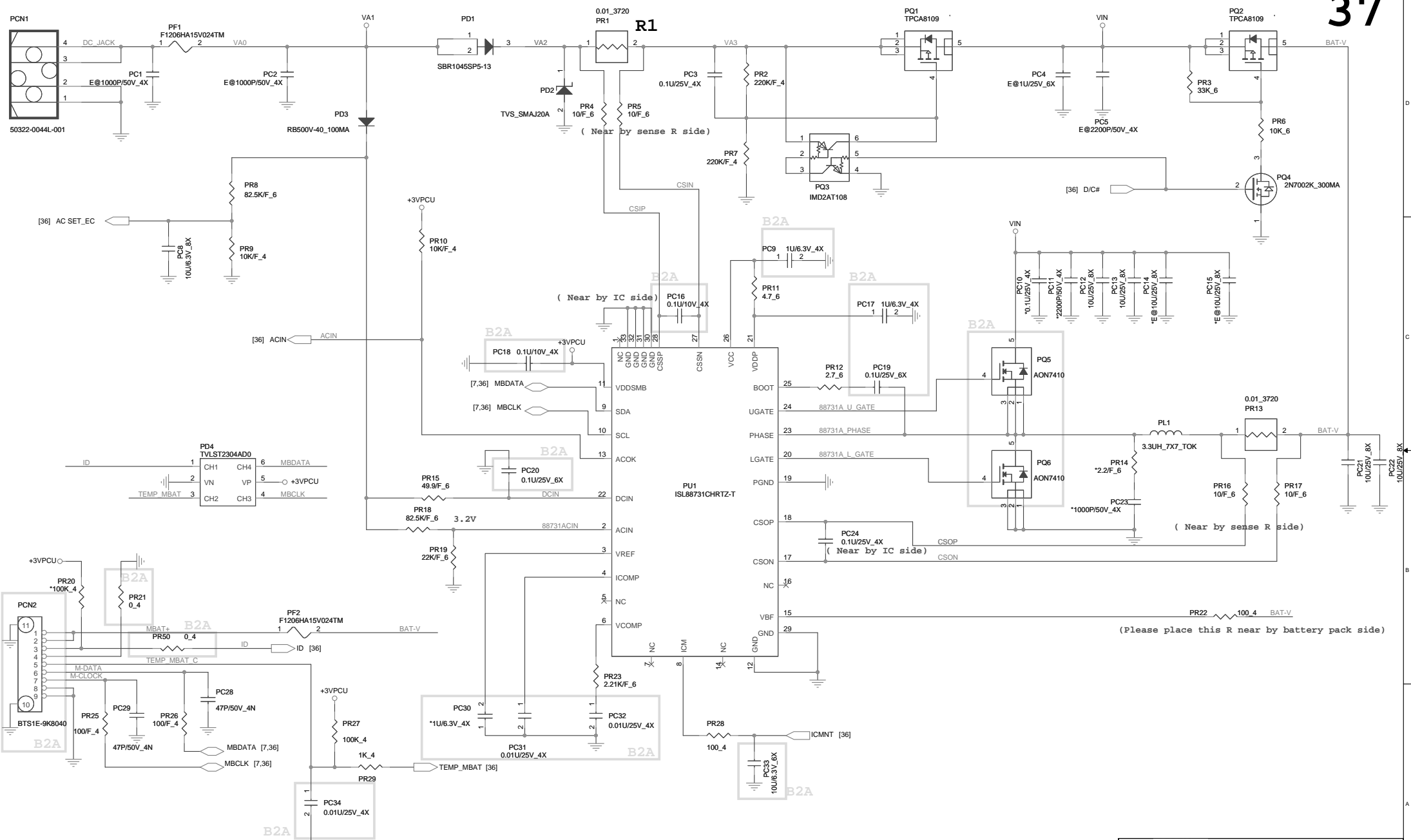
SKU_STRAP_1 (GPIO56)	SKU_STRAP_2 (GPIO02)	SKU_STRAP_3 (GPIO41)	SKU
0	0	0	Brazos UMA
0	0	1	Brazos DIS
0	1	0	COMAL UMA
0	1	1	COMAL DIS
1	0	0	Deccan UMA
1	0	1	Deccan DIS



SMBUS Table

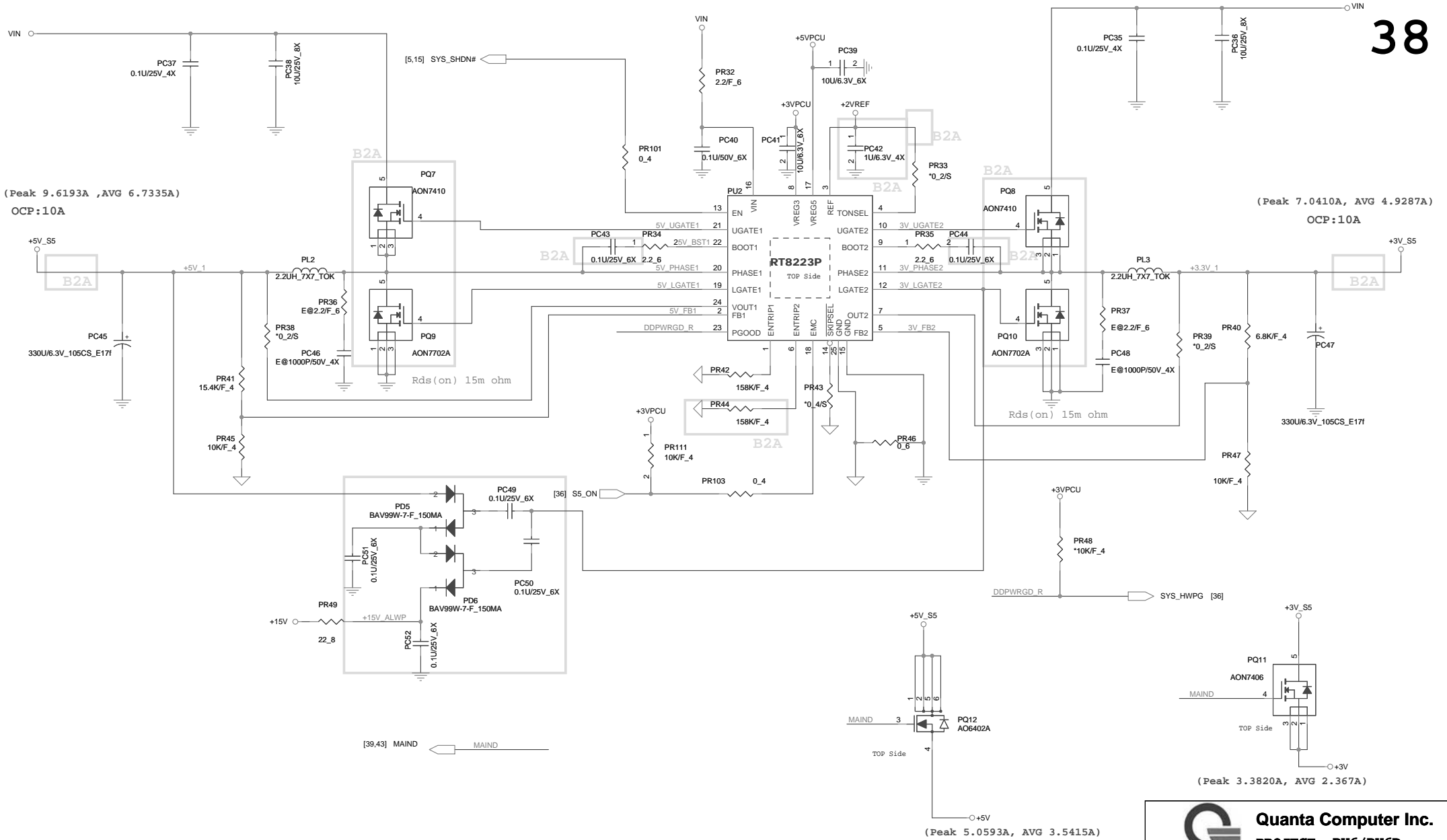
SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H





Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	CHARGER (ISL88731C)	1A
Date:	Tuesday, February 14, 2012	Sheet 37 of 47



(Peak 9.6193A ,AVG 6.7335A)
OCP:10A

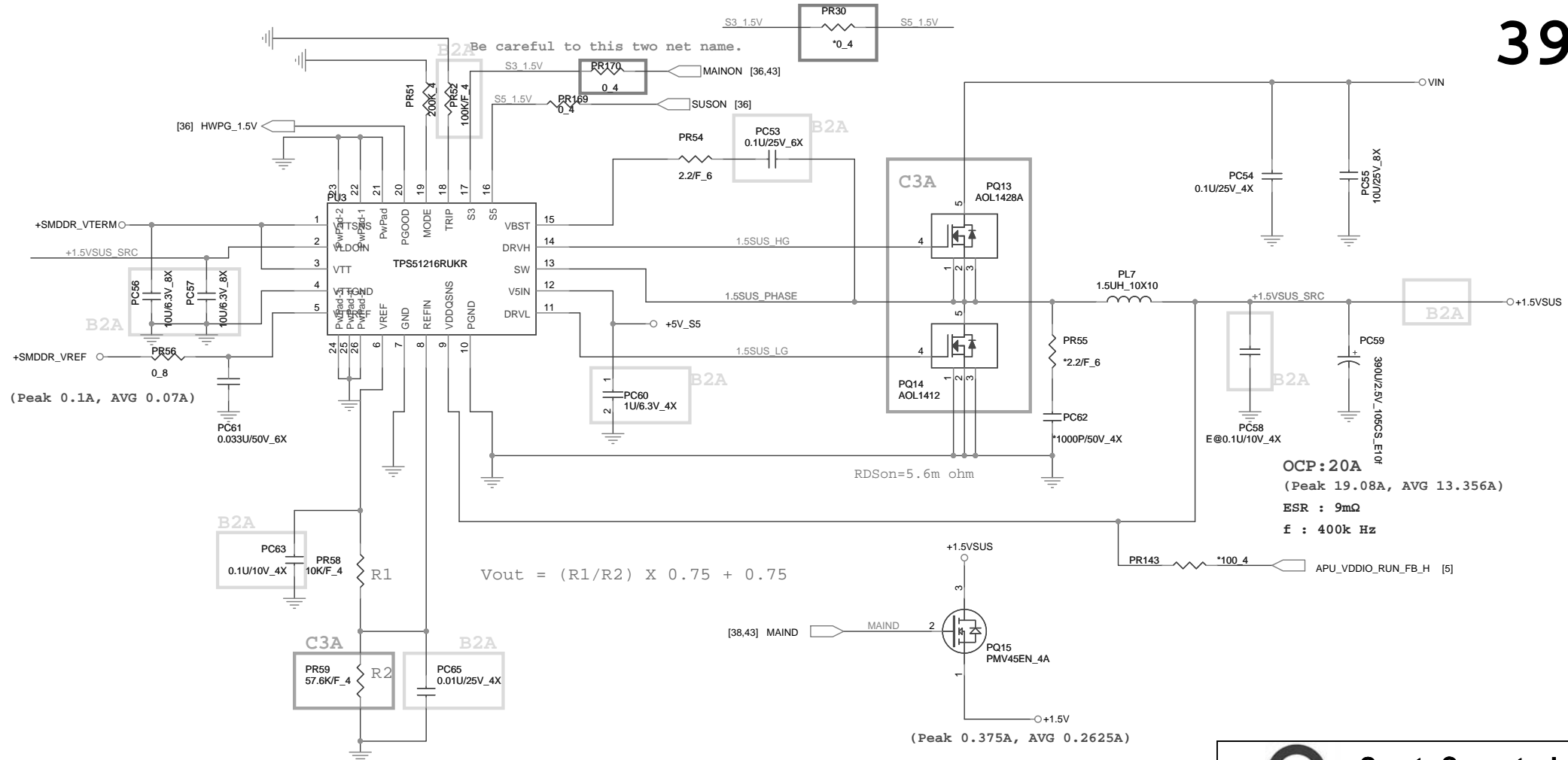
(Peak 7.0410A, AVG 4.9287A)
OCP:10A


(Peak 5.0593A, AVG 3.5415A)

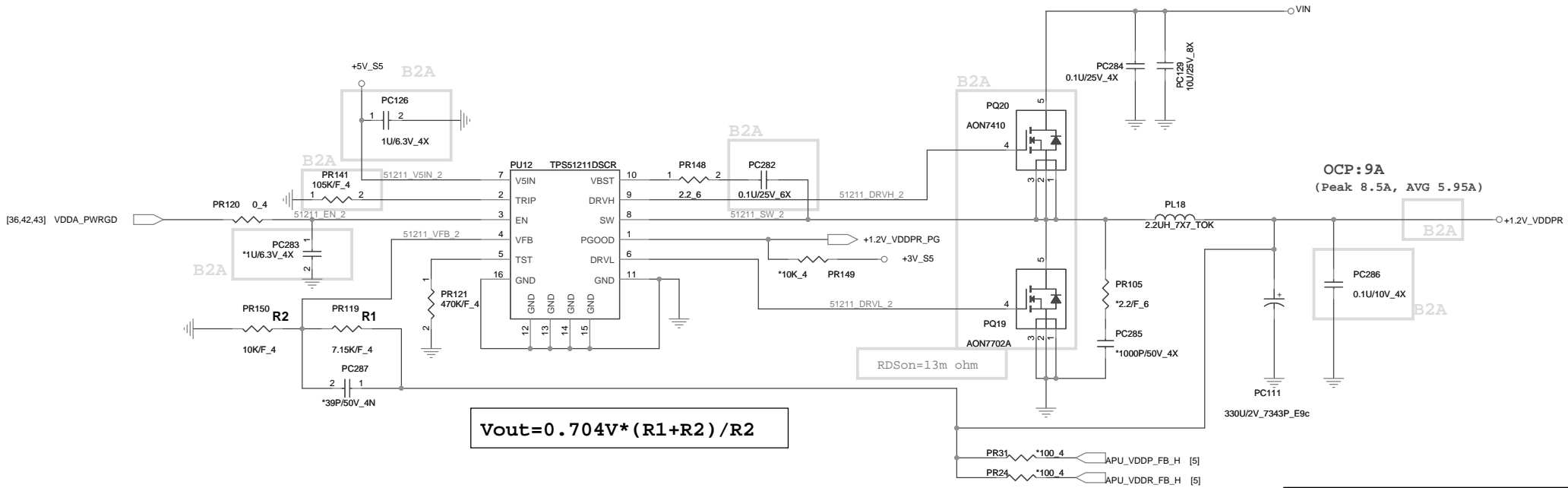
(Peak 3.3820A, AVG 2.367A)

Quanta Computer Inc.
PROJECT :BY6/BY6D

Size	Document Number	Rev
	System 3V/5V(RT8223P)	1A
Date:	Tuesday, February 14, 2012	Sheet 38 of 47

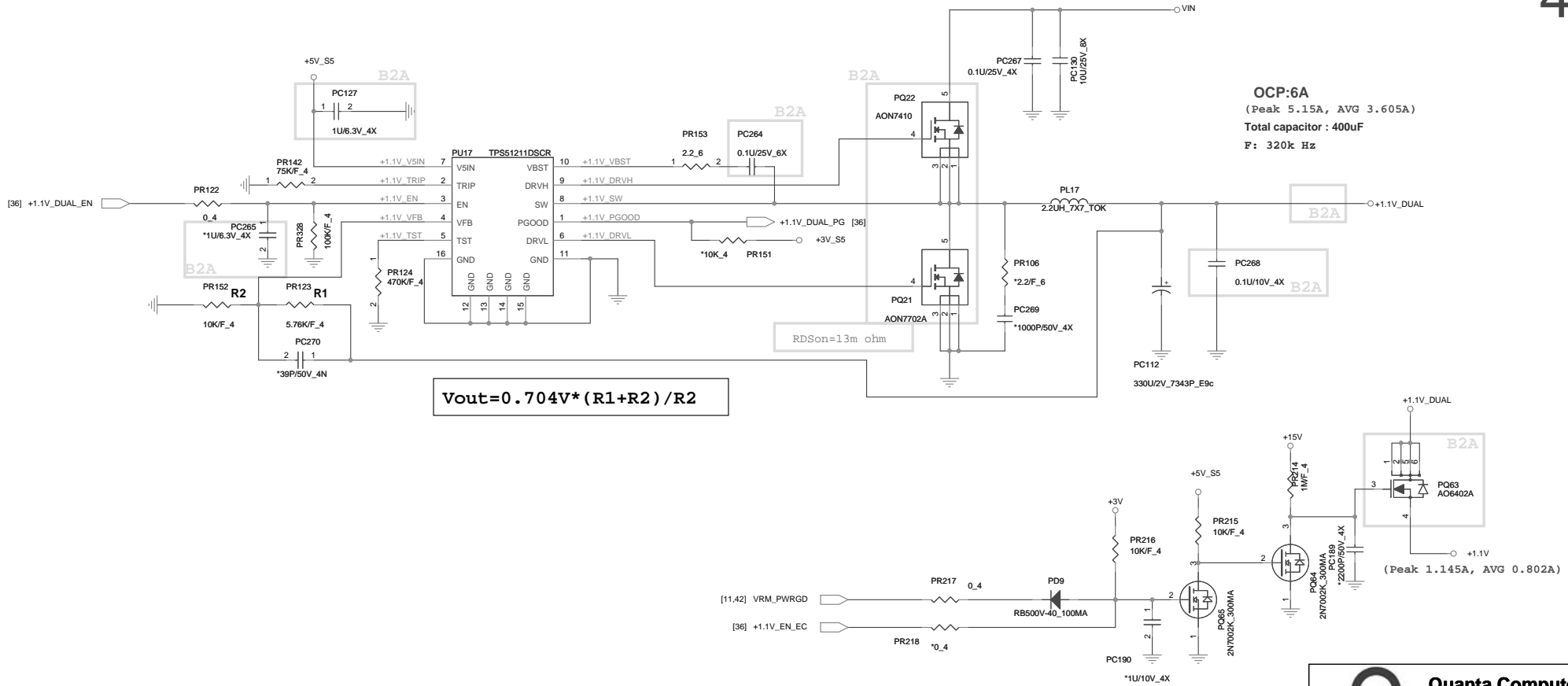


 Quanta Computer Inc. PROJECT : BY6/BY6D		Size	Document Number	Rev
			+1.5VSUS (TPS51216RUKR)	1A
Date: Tuesday, February 14, 2012		Sheet 39 of 47		



Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	+1.2V_VDDPR (TPS51211DSCR)	1A
Date:	Tuesday, February 14, 2012	Sheet 40 of 47



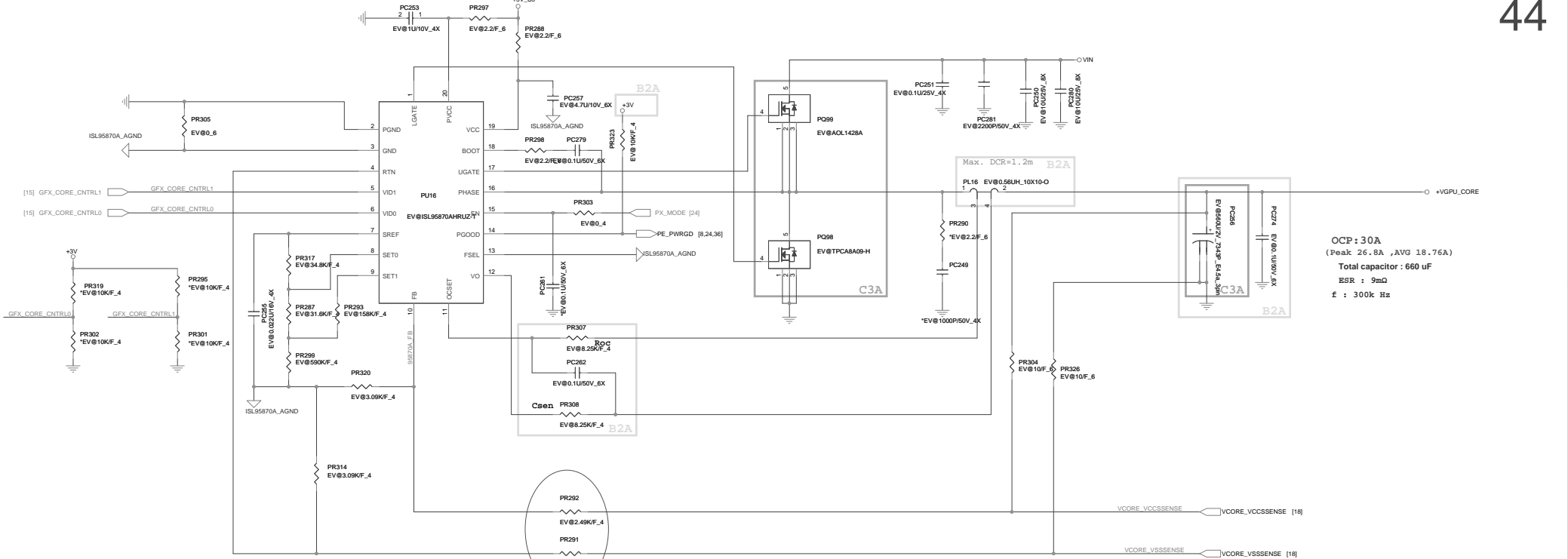
$$V_{out} = 0.704V * (R1 + R2) / R2$$

OCP:6A
 (Peak 5.15A, AVG 3.605A)
 Total capacitor : 400uF
 F: 320k Hz

(Peak 1.145A, AVG 0.802A)

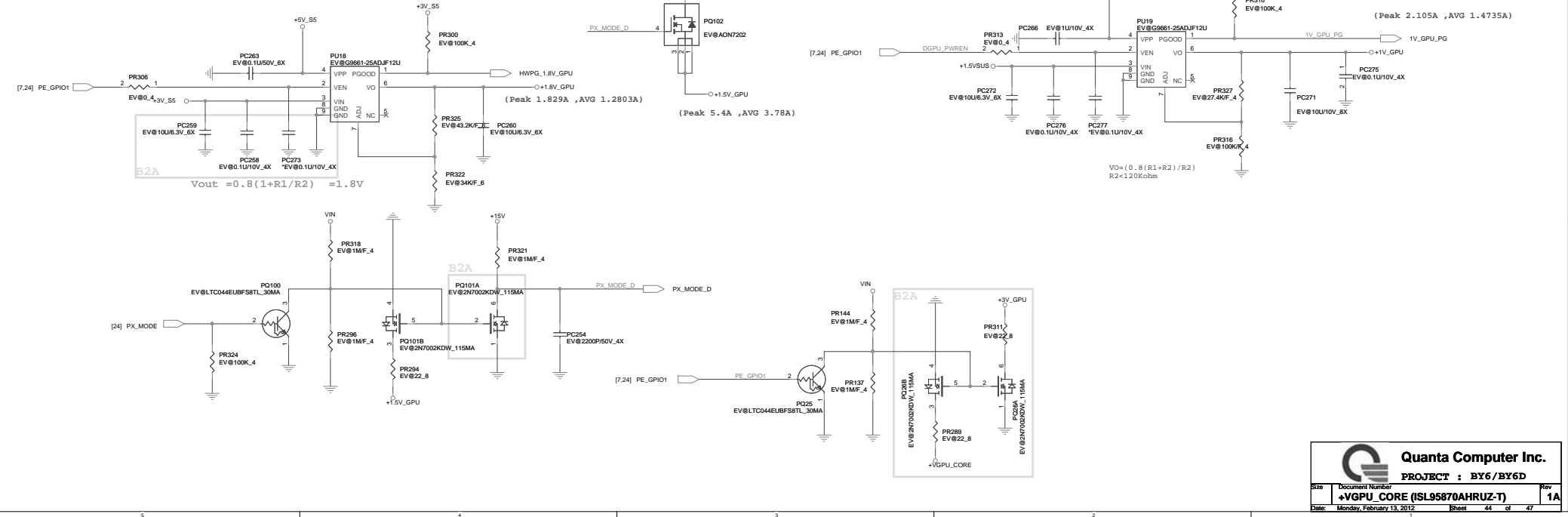
Quanta Computer Inc.
 PROJECT : BY6/BY6D

Size	Document Number	Rev
	+1.1V_DUAL (TPS51211DSCR)	1C
Date:	Tuesday, February 14, 2012	Sheet 41 of 47



OCP: 30A
 (Peak 26.8A ,AVG 18.76A)
 Total capacitor: 660 uF
 ESR : 9mΩ
 f : 300k Hz

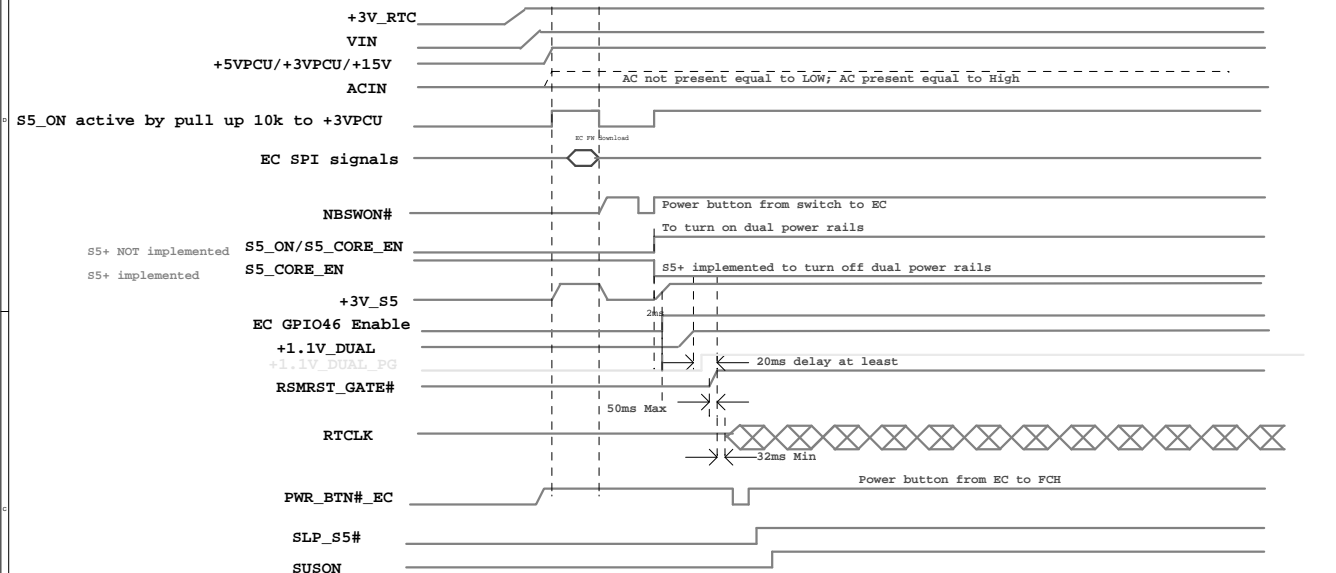
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.0V
0	0	1.1V



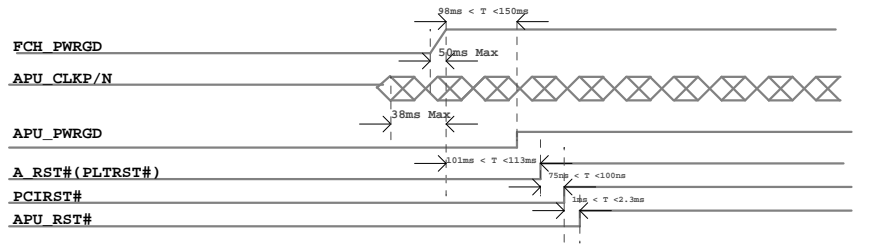
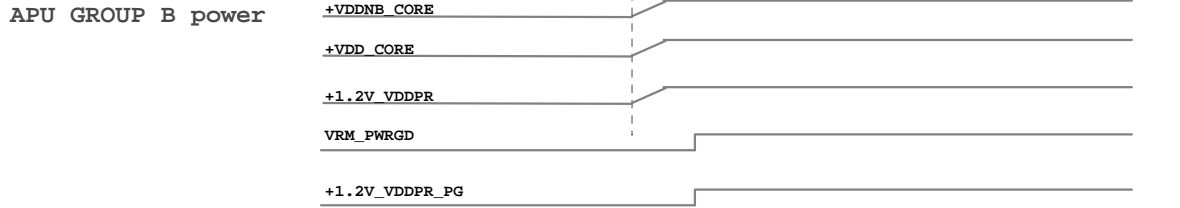
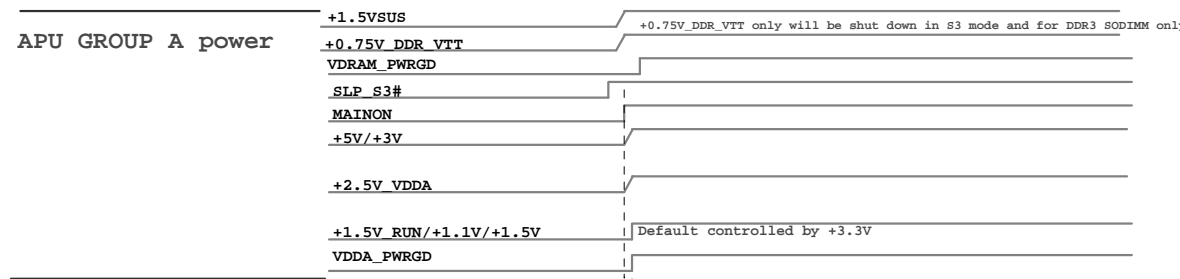
$V_{out} = 0.8 \cdot (1 + R1/R2) = 1.8V$

$V_O = (0.8 \cdot (R1 + R2) / R2)$
 $R2 < 1.2 \Omega kOhm$

BY6/BY6D Power On Sequence: S5 > S0



APU Power on sequence required:
 Llano APU:
 1.Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)
 HUDSON-M2/M3:
 1.+3V_S5 ramp before +1.1V_DUAL
 2.+3V ramp before +1.1V
 3.+3V_RTC must ramp at least 5 secs before the +3V_S5



Model		REV	CHANGE LIST				MODEL BY6D	
BY6D MB	A1A					PAGE	FROM	
						1	A1A	
						2	A1A	
						3	A1A	
						4	A1A	
						5	A1A	
						6	A1A	
						7	A1A	
						8	A1A	
						9	A1A	
						10	A1A	
						11	A1A	
						12	A1A	
						13	A1A	
						14	A1A	
						15	A1A	
						16	A1A	
						17	A1A	
						18	A1A	
						19	A1A	
						20	A1A	
						21	A1A	
						22	A1A	
						23	A1A	
						24	A1A	
						25	A1A	
						26	A1A	
						27	A1A	
						28	A1A	
						29	A1A	
						30	A1A	
						31	A1A	
						32	A1A	
						33	A1A	
						34	A1A	
						35	A1A	
						36	A1A	
						37	A1A	
						38	A1A	
						39	A1A	
						40	A1A	
						41	A1A	
						42	A1A	
						43	A1A	
						44	A1A	
						45	A1A	
						46	A1A	

DOC NO. 204	PROJECT MODEL :	BY6D	APPROVED BY:		DATE:	2011/10/02
	PART NUMBER:		DRAWING BY:	Wei-Sheng	REVISION:	A1A