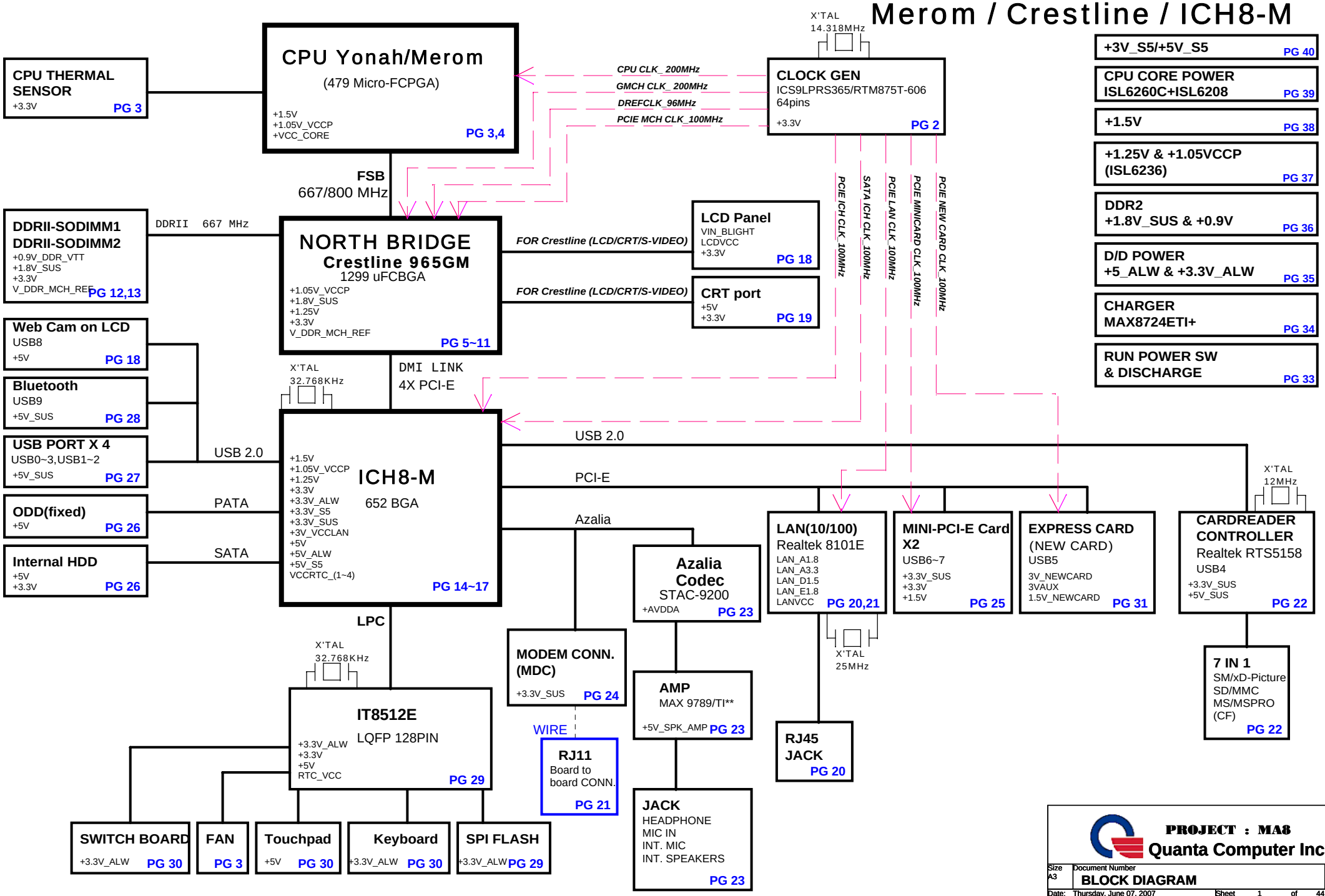
MA8 BLOCK DIAGRAM

Merom / Crestline / ICH8-M

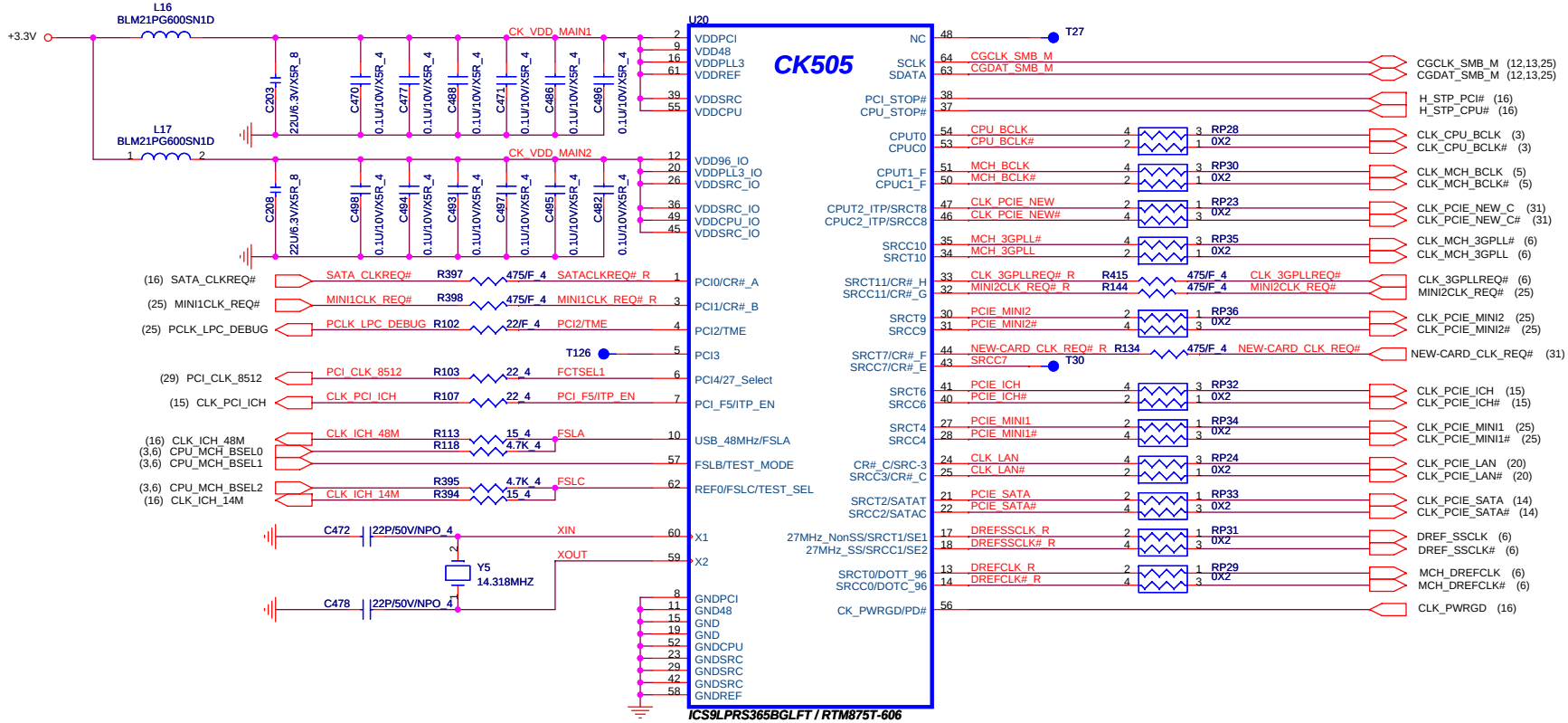


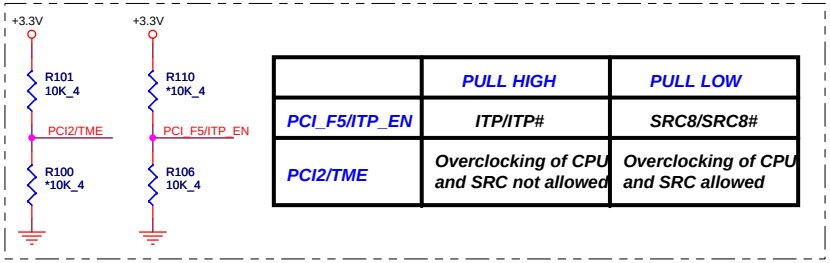
PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A3	BLOCK DIAGRAM	1A

Date: Thursday, June 07, 2007 Sheet 1 of 44

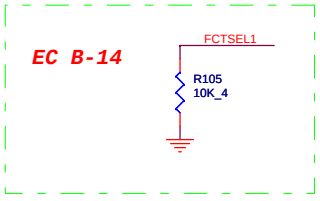


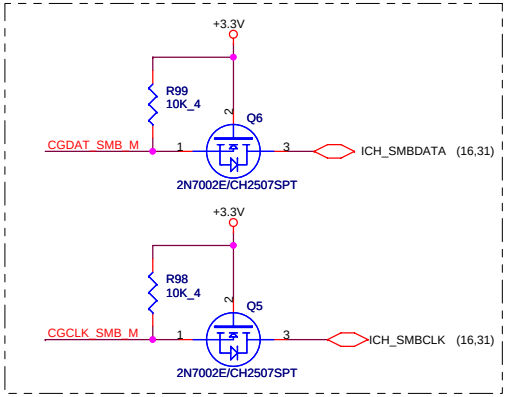


	PULL HIGH	PULL LOW
PCI_F5/ITP_EN	ITP/ITP#	SRC8/SRC8#
PCI2/TME	Overclocking of CPU and SRC not allowed	Overclocking of CPU and SRC allowed

GCLK_SEL = FCTSEL1

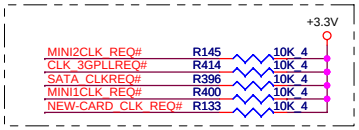
FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS





CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100.00	100	33
0	0	1	133.33	100	33
0	1	1	166.66	100	33
0	1	0	200.00	100	33
0	0	0	266.66	100	33
1	0	0	333.33	100	33
1	1	0	400.00	100	33
1	1	1	200.00	100	33



EMI CAP

C181	27P/50V/NPO_4	CLK_ICH_48M
C466	27P/50V/NPO_4	CLK_ICH_14M
C177	27P/50V/NPO_4	PCI_CLK_8512
C176	27P/50V/NPO_4	PCLK_LPC_DEBUG
C178	27P/50V/NPO_4	CLK_PCI_ICH

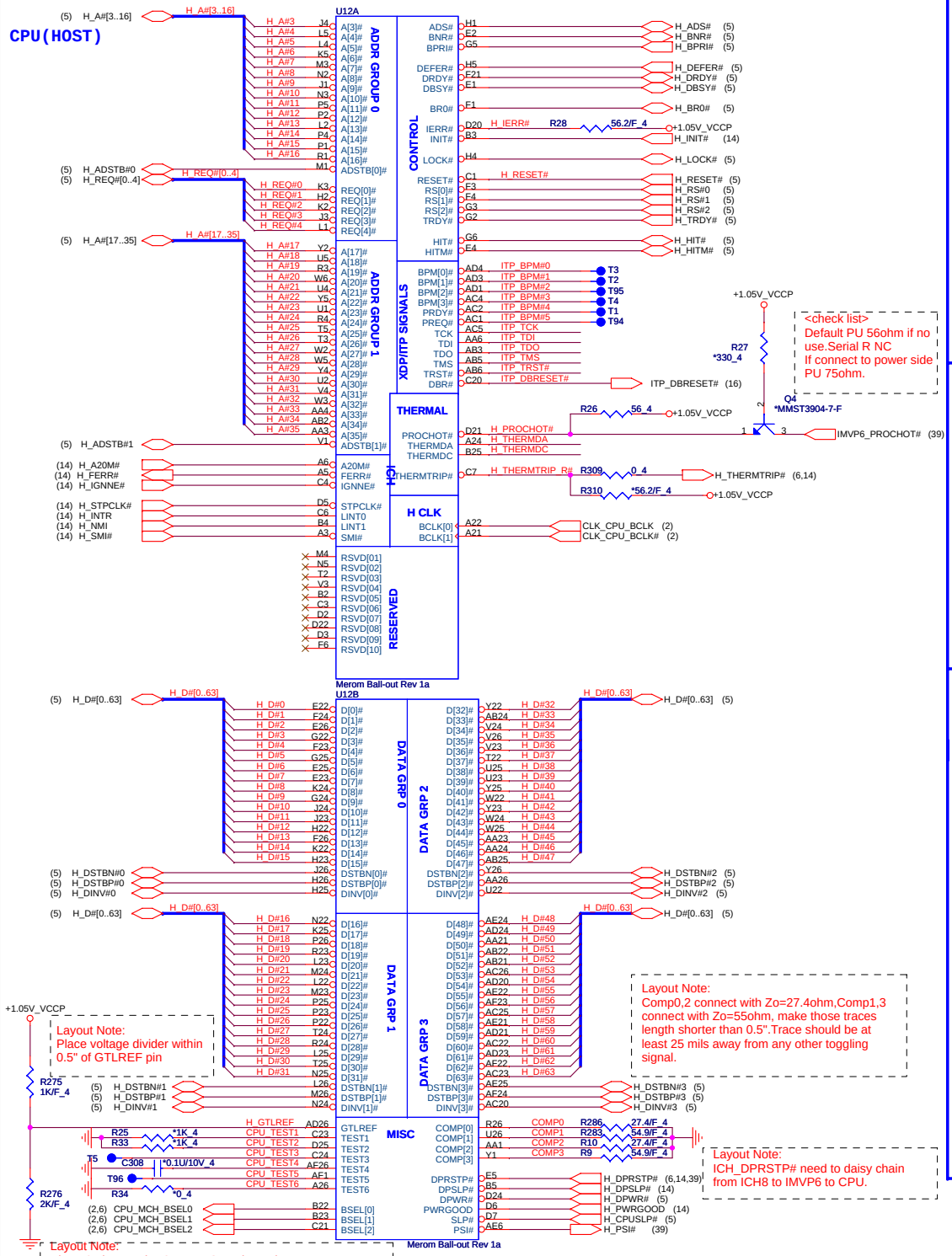
PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A3	CLOCK GENERATOR	1A

Date: Saturday, June 23, 2007 Sheet 2 of 44

CPU(HOST)



<check list>
Default PU 56ohm if no use.Serial R NC
If connect to power side PU 75ohm.

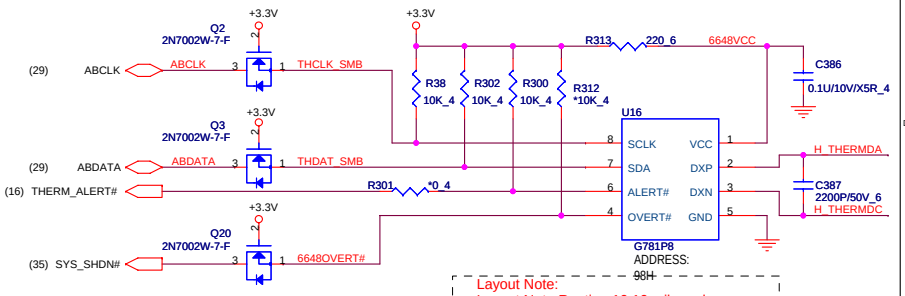
Layout Note:
Place voltage divider within 0.5" of GTLREF pin

Layout Note:
Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Layout Note:
ICH_DPRSTP# need to daisy chain from ICH8 to IMVP6 to CPU.

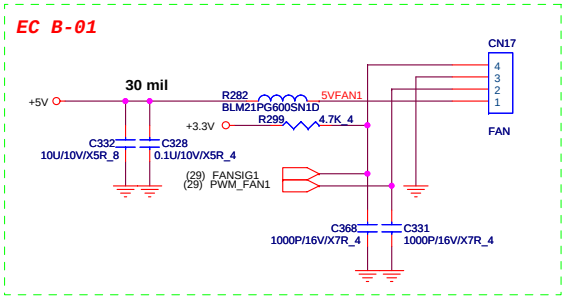
Layout Note:
Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

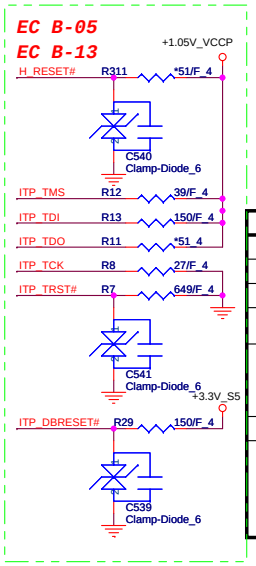
CPU Thermal monitor



Layout Note:
Layout Note:Routing 10:10 mils and away from noise source with ground gard

CPU FAN





Populate ITP700Flex for bringup

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-up near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near CPU
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

PROJECT : MA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU(1 of 2)/FAN/Thermal	1A
Date: Saturday, June 23, 2007	Sheet 3 of 44	

03

CPU(Power)

All use 10U 4V(+-20%,X6S,0805)Pb-Free.

+VCC_CORE

C340 10U/6.3V/X5R_8, C341 10U/6.3V/X5R_8, C46 10U/6.3V/X5R_8, C363 10U/6.3V/X5R_8, C362 10U/6.3V/X5R_8

C336 10U/6.3V/X5R_8, C338 10U/6.3V/X5R_8, C361 10U/6.3V/X5R_8, C364 10U/6.3V/X5R_8, C47 10U/6.3V/X5R_8

8 inside cavity, north side, secondary layer.

C337 10U/6.3V/X5R_8, C21 10U/6.3V/X5R_8, C24 10U/6.3V/X5R_8, C23 10U/6.3V/X5R_8, C366 10U/6.3V/X5R_8

C22 10U/6.3V/X5R_8, C25 10U/6.3V/X5R_8, C29 10U/6.3V/X5R_8, C45 10U/6.3V/X5R_8, C339 10U/6.3V/X5R_8

8 inside cavity, south side, secondary layer.

C28 10U/6.3V/X5R_8, C38 10U/6.3V/X5R_8, C37 10U/6.3V/X5R_8, C19 10U/6.3V/X5R_8, C18 10U/6.3V/X5R_8, C20 10U/6.3V/X5R_8

6 inside cavity, north side, primary layer.

C40 10U/6.3V/X5R_8, C41 10U/6.3V/X5R_8, C42 10U/6.3V/X5R_8, C43 10U/6.3V/X5R_8, C365 10U/6.3V/X5R_8, C44 10U/6.3V/X5R_8

6 inside cavity, south side, primary layer.

<REV.NO. 0.5/REF.NO.19343>
Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA

U12C

VCC[001] A7, VCC[002] A9, VCC[003] A10, VCC[004] A12, VCC[005] A13, VCC[006] A15, VCC[007] A17, VCC[008] A18, VCC[009] A20, VCC[010] B7, VCC[011] B9, VCC[012] B10, VCC[013] B12, VCC[014] B14, VCC[015] B15, VCC[016] B17, VCC[017] B18, VCC[018] B20, VCC[019] C9, VCC[020] C10, VCC[021] C12, VCC[022] C13, VCC[023] C15, VCC[024] C17, VCC[025] C18, VCC[026] D9, VCC[027] D10, VCC[028] D12, VCC[029] D14, VCC[030] D15, VCC[031] D17, VCC[032] D18, VCC[033] E7, VCC[034] E9, VCC[035] E10, VCC[036] E12, VCC[037] E13, VCC[038] E15, VCC[039] E17, VCC[040] E18, VCC[041] E20, VCC[042] F7, VCC[043] F9, VCC[044] F10, VCC[045] F12, VCC[046] F14, VCC[047] F15, VCC[048] F17, VCC[049] F18, VCC[050] F20, VCC[051] AA7, VCC[052] AA9, VCC[053] AA10, VCC[054] AA12, VCC[055] AA13, VCC[056] AA15, VCC[057] AA17, VCC[058] AA18, VCC[059] AA20, VCC[060] AB9, VCC[061] AC10, VCC[062] AB10, VCC[063] AB12, VCC[064] AB14, VCC[065] AB15, VCC[066] AB17, VCC[067] AB18

VCC[068] AB20, VCC[069] AB7, VCC[070] AC7, VCC[071] AC9, VCC[072] AC12, VCC[073] AC13, VCC[074] AC15, VCC[075] AC17, VCC[076] AC18, VCC[077] AD7, VCC[078] AD9, VCC[079] AD10, VCC[080] AD12, VCC[081] AD14, VCC[082] AD15, VCC[083] AD17, VCC[084] AD18, VCC[085] AE9, VCC[086] AE10, VCC[087] AE12, VCC[088] AE13, VCC[089] AE15, VCC[090] AE17, VCC[091] AE18, VCC[092] AE20, VCC[093] AF9, VCC[094] AF10, VCC[095] AF12, VCC[096] AF14, VCC[097] AF15, VCC[098] AF17, VCC[099] AF18, VCC[100] AF20

VCCP[01] G21, VCCP[02] V6, VCCP[03] J6, VCCP[04] K6, VCCP[05] M6, VCCP[06] J21, VCCP[07] K21, VCCP[08] M21, VCCP[09] N21, VCCP[10] N6, VCCP[11] R21, VCCP[12] R6, VCCP[13] T21, VCCP[14] T6, VCCP[15] V21, VCCP[16] W21

VCCA[01] B26, VCCA[02] C26

VID[0] AD6, VID[1] AE5, VID[2] AE5, VID[3] AE4, VID[4] AE3, VID[5] AE3, VID[6] AE2

VCCSENSE AF7

VSSSENSE AE7

Merom Ball-out Rev 1a

+1.05V_VCCP

C358 0.1U/10V/X5R_4, C345 0.1U/10V/X5R_4, C344 0.1U/10V/X5R_4, C348 0.1U/10V/X5R_4, C360 0.1U/10V/X5R_4, C351 0.1U/10V/X5R_4

Layout out:
Place these inside socket cavity on North side secondary.

+1.05V_VCCP

C335 330U/2V_7343

+1.5V

C68 0.01U/16V/X7R_4, C64 10U/6.3V/X5R_8

Layout Note:
Place C68,C64 near PIN B26.

+VCC_CORE

R279 100/F_6

VID0 (39), VID1 (39), VID2 (39), VID3 (39), VID4 (39), VID5 (39), VID6 (39)

VCCSENSE (39)

VSSSENSE (39)

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

R280 100/F_6

U12D

VSS[001] A4, VSS[002] A8, VSS[003] A11, VSS[004] A14, VSS[005] A16, VSS[006] A19, VSS[007] A23, VSS[008] AE2, VSS[009] B6, VSS[010] B8, VSS[011] B11, VSS[012] B13, VSS[013] B16, VSS[014] B19, VSS[015] B21, VSS[016] B24, VSS[017] C5, VSS[018] C8, VSS[019] C11, VSS[020] C14, VSS[021] C16, VSS[022] C19, VSS[023] C2, VSS[024] C22, VSS[025] C25, VSS[026] D1, VSS[027] D4, VSS[028] D8, VSS[029] D11, VSS[030] D13, VSS[031] D16, VSS[032] D19, VSS[033] D23, VSS[034] D26, VSS[035] E3, VSS[036] E6, VSS[037] E8, VSS[038] E11, VSS[039] E14, VSS[040] E16, VSS[041] E19, VSS[042] E21, VSS[043] E24, VSS[044] F5, VSS[045] F8, VSS[046] F11, VSS[047] F13, VSS[048] F16, VSS[049] F19, VSS[050] F2, VSS[051] F22, VSS[052] F25, VSS[053] G4, VSS[054] G1, VSS[055] G23, VSS[056] G26, VSS[057] H3, VSS[058] H6, VSS[059] H21, VSS[060] H24, VSS[061] J2, VSS[062] J5, VSS[063] J22, VSS[064] J25, VSS[065] K1, VSS[066] K4, VSS[067] K23, VSS[068] K26, VSS[069] L3, VSS[070] L6, VSS[071] L21, VSS[072] L24, VSS[073] M2, VSS[074] M5, VSS[075] M22, VSS[076] M25, VSS[077] N1, VSS[078] N4, VSS[079] N23, VSS[080] N26, VSS[081] P3

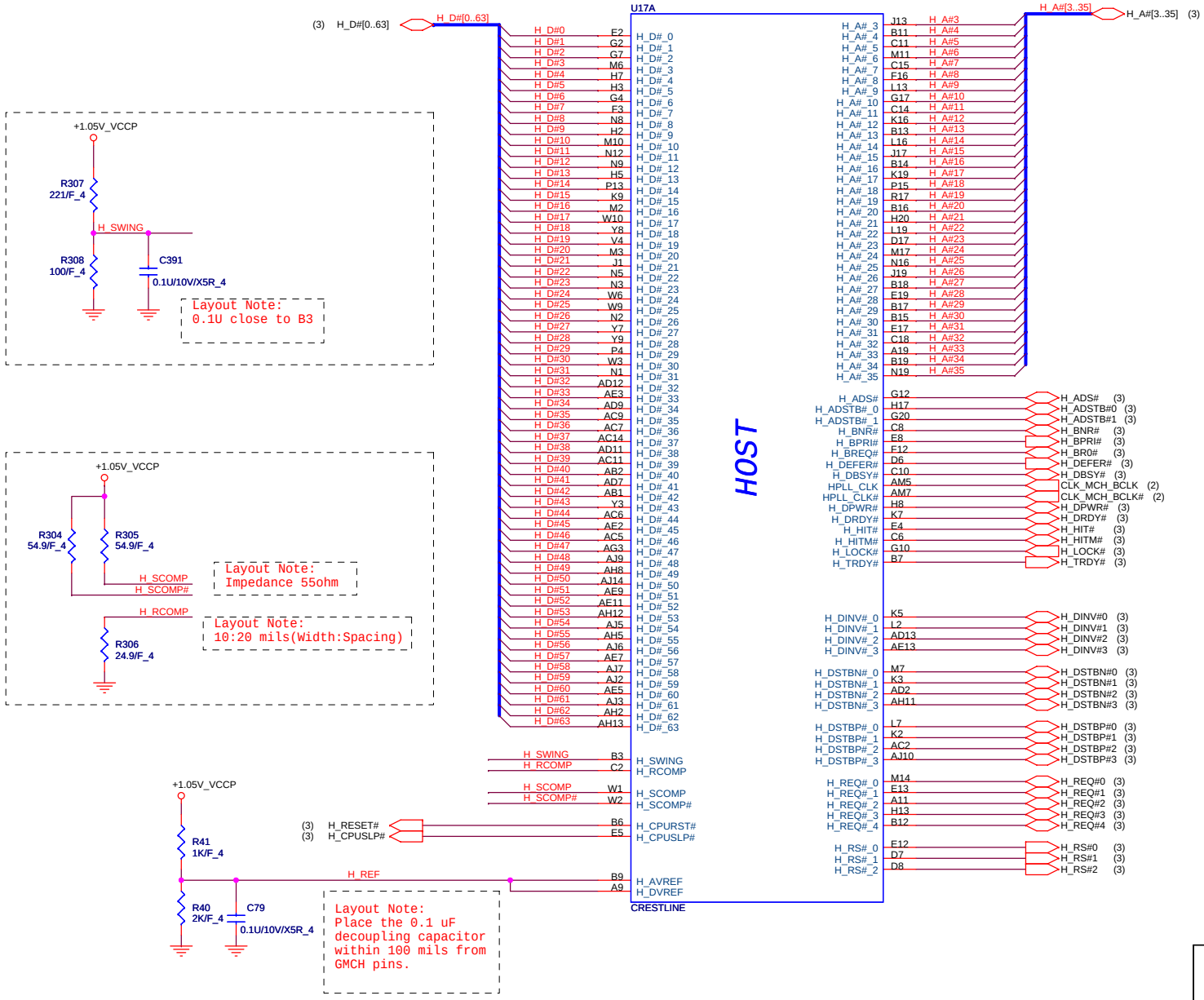
VSS[082] P6, VSS[083] P21, VSS[084] P24, VSS[085] R2, VSS[086] R5, VSS[087] R22, VSS[088] R25, VSS[089] T1, VSS[090] T4, VSS[091] T23, VSS[092] T26, VSS[093] U3, VSS[094] U6, VSS[095] U21, VSS[096] U24, VSS[097] V2, VSS[098] V5, VSS[099] V22, VSS[100] V25, VSS[101] W1, VSS[102] W4, VSS[103] W23, VSS[104] W26, VSS[105] Y3, VSS[106] Y6, VSS[107] Y21, VSS[108] Y24, VSS[109] AA2, VSS[110] AA5, VSS[111] AA8, VSS[112] AA11, VSS[113] AA14, VSS[114] AA16, VSS[115] AA19, VSS[116] AA22, VSS[117] AA25, VSS[118] AB1, VSS[119] AB4, VSS[120] AB8, VSS[121] AB11, VSS[122] AB13, VSS[123] AB16, VSS[124] AB19, VSS[125] AB23, VSS[126] AB26, VSS[127] AC3, VSS[128] AC6, VSS[129] AC8, VSS[130] AC11, VSS[131] AC14, VSS[132] AC16, VSS[133] AC19, VSS[134] AC21, VSS[135] AC24, VSS[136] AD2, VSS[137] AD5, VSS[138] AD8, VSS[139] AD11, VSS[140] AD13, VSS[141] AD16, VSS[142] AD19, VSS[143] AD22, VSS[144] AD25, VSS[145] AE1, VSS[146] AE4, VSS[147] AE8, VSS[148] AE11, VSS[149] AE14, VSS[150] AE16, VSS[151] AE19, VSS[152] AE23, VSS[153] AE26, VSS[154] A2, VSS[155] AF6, VSS[156] AF8, VSS[157] AF11, VSS[158] AF13, VSS[159] AF16, VSS[160] AF19, VSS[161] AF21, VSS[162] A25, VSS[163] AF25

Merom Ball-out Rev 1a

PROJECT : MA8
Quanta Computer Inc.

Size	Document Number	Rev
A3	CPU(2 of 2)	1A

Date: Saturday, June 23, 2007 Sheet 4 of 44

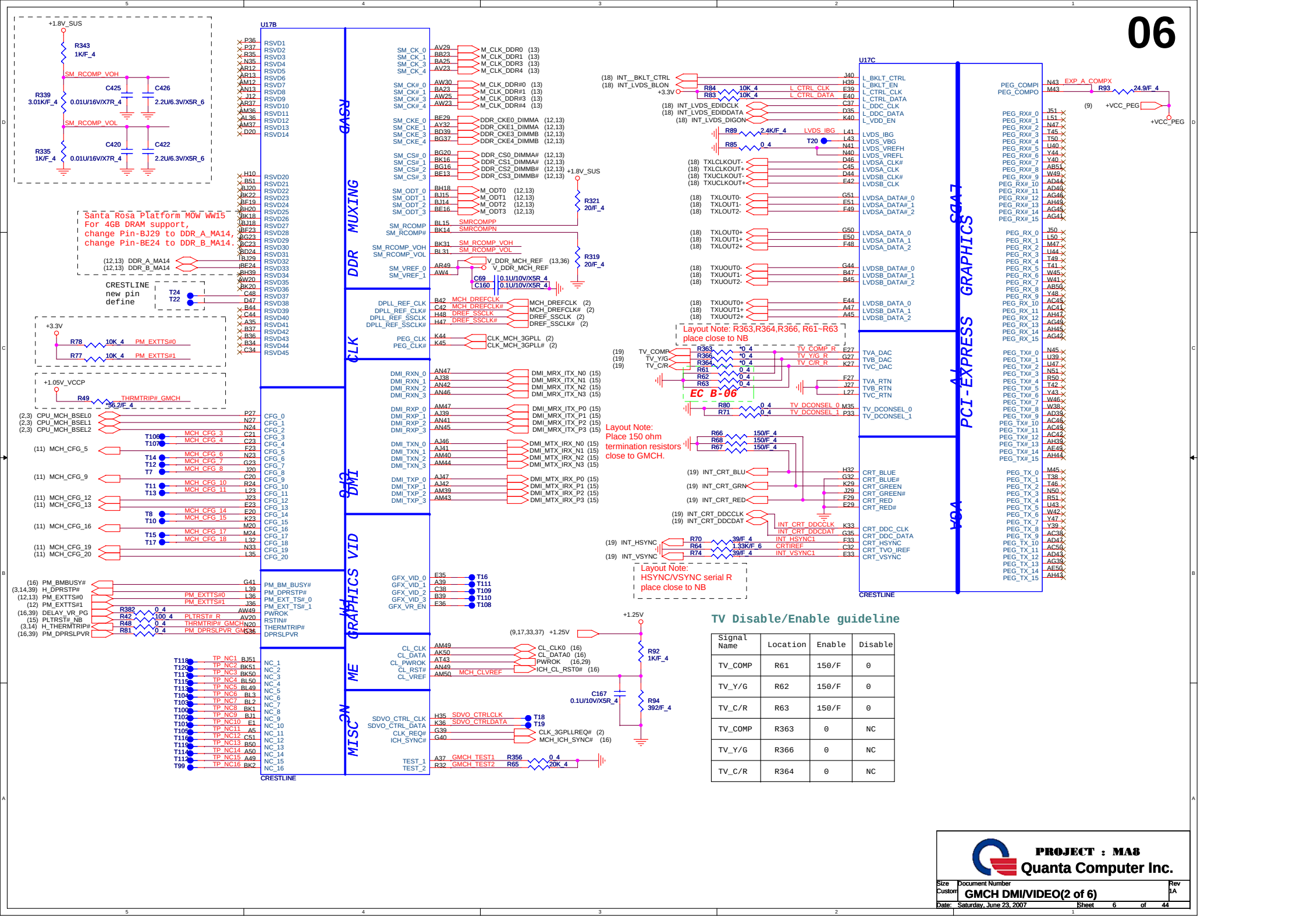


PROJECT : MA8

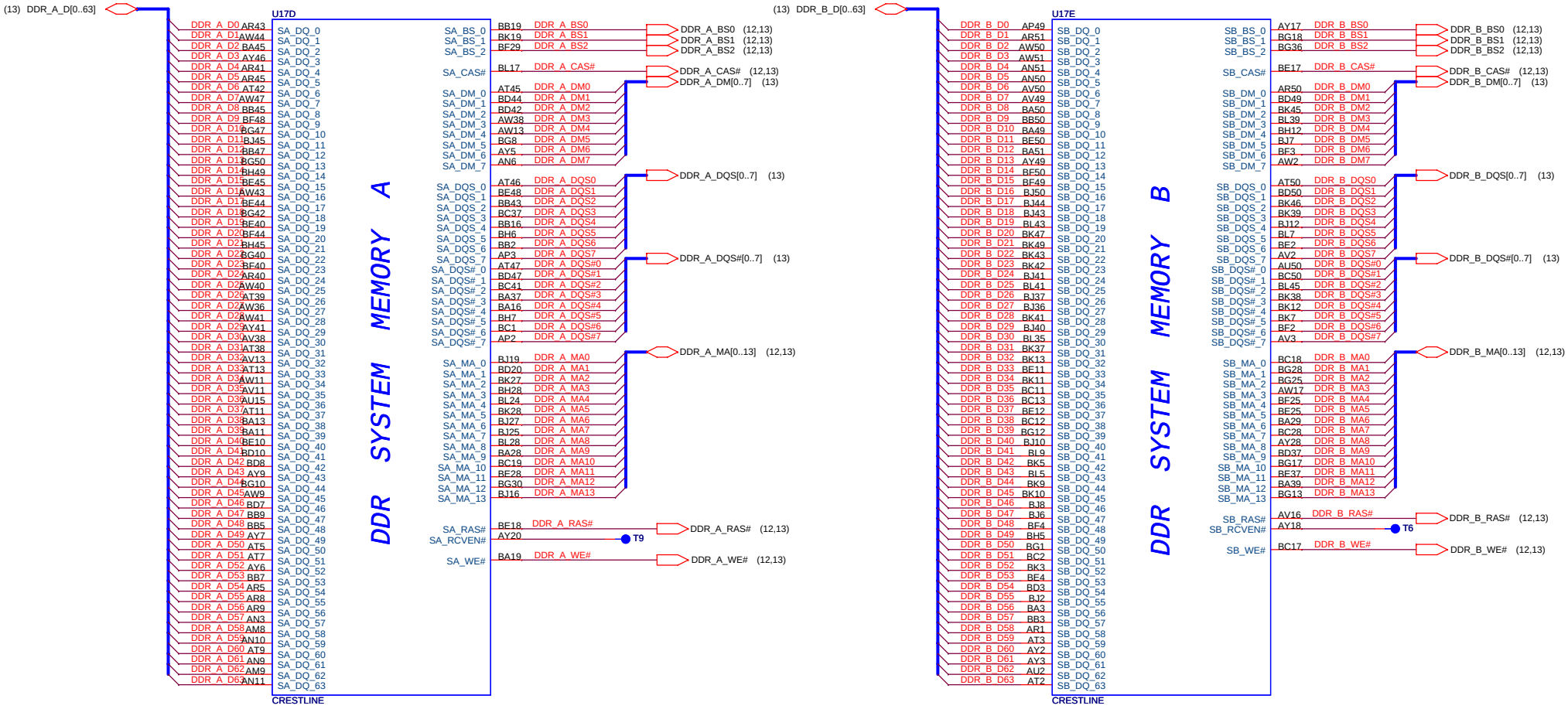
Quanta Computer Inc.

Size	Document Number	Rev
A3	GMCH HOST(1 of 6)	1A

Date: Saturday, June 23, 2007 Sheet 5 of 44



Signal Name	Location	Enable	Disable
TV_COMP	R61	150/F	0
TV_Y/G	R62	150/F	0
TV_C/R	R63	150/F	0
TV_COMP	R363	0	NC
TV_Y/G	R366	0	NC
TV_C/R	R364	0	NC



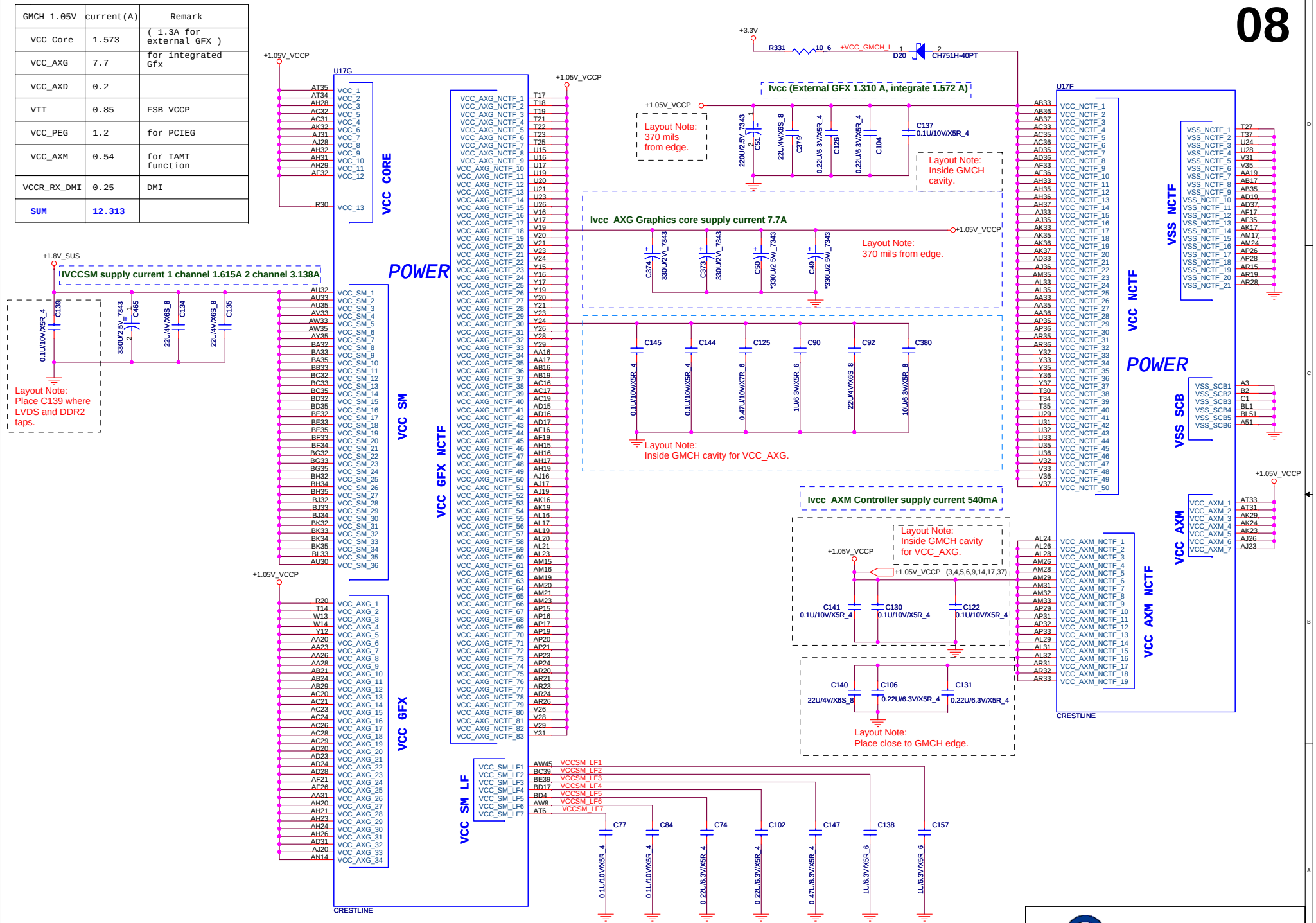
PROJECT : MA8

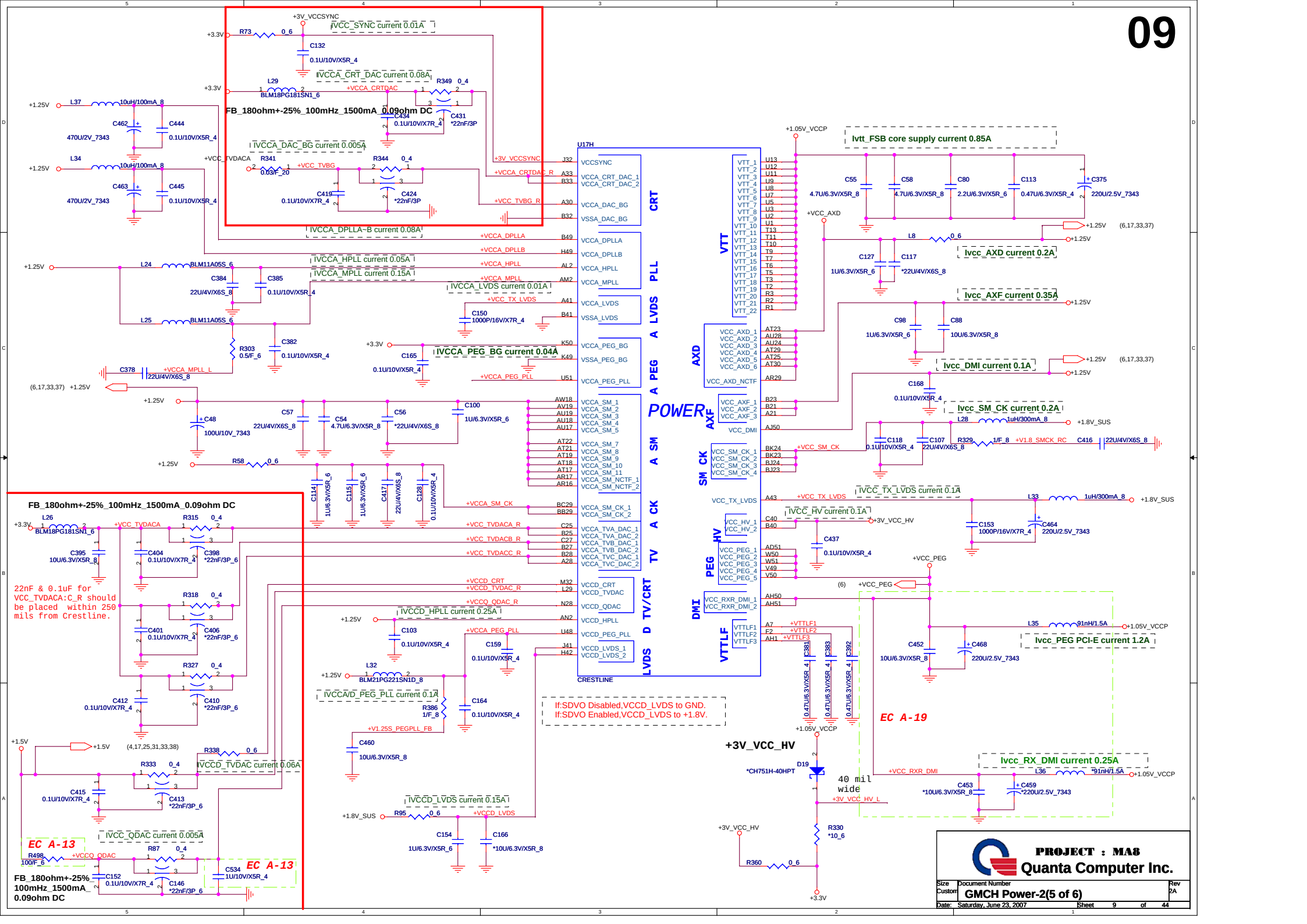
Quanta Computer Inc.

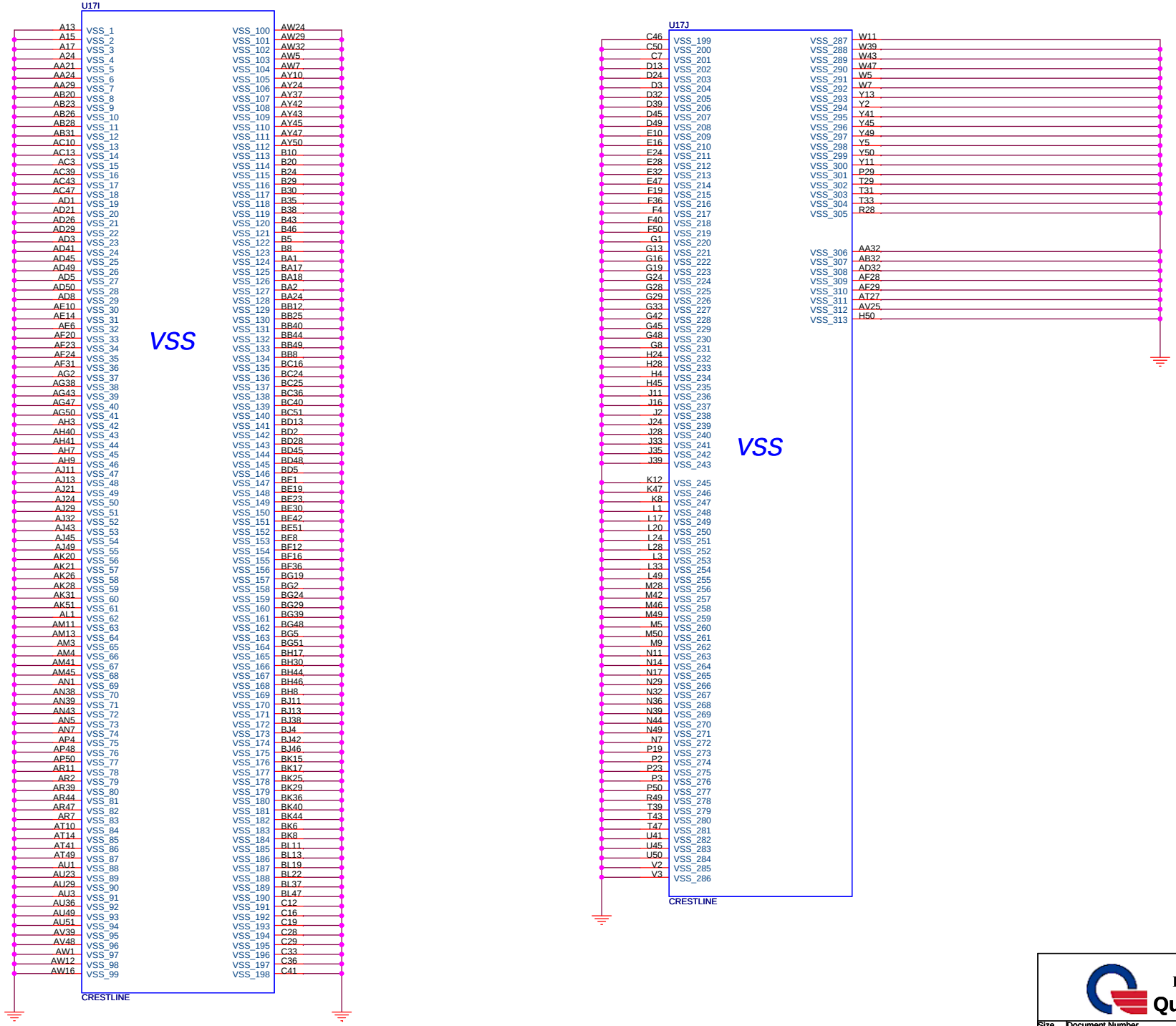
Size	Document Number	Rev
A3	GMCH DDR/Strap(3 of 6)	1A

Date: Saturday, June 23, 2007 Sheet 7 of 44

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	12.313	




09
POWER
U17H
CRESTLINE
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
IVCC_SYNC current 0.01A
IVCCA_CRT_DAC current 0.08A
IVCCA_DAC_BG current 0.005A
IVCCA_DPLLA~B current 0.08A
IVCCA_HPLL current 0.05A
IVCCA_MPLL current 0.15A
IVCCA_LVDS current 0.01A
IVCCA_PEG_BG current 0.04A
IVCCD_HPLL current 0.25A
IVCCA/D_PEG_PLL current 0.1A
IVCCD_TVDAC current 0.06A
IVCCD_LVDS current 0.15A
IVCC_QDAC current 0.005A
Ivtt_FSB core supply current 0.85A
Ivcc_AXD current 0.2A
Ivcc_AXF current 0.35A
Ivcc_DMI current 0.1A
Ivcc_SM_CK current 0.2A
IVCC_TX_LVDS current 0.1A
IVCC_HV current 0.1A
Ivcc_PEG PCI-E current 1.2A
Ivcc_RX_DMI current 0.25A
22nF & 0.1uF for VCC_TVDACA:C_R should be placed within 250 mils from Crestline.
If:SDVO Disabled,VCCD_LVDS to GND.
If:SDVO Enabled,VCCD_LVDS to +1.8V.
+3V_VCC_HV
40 mil wide
EC A-19
EC A-13
PROJECT : MA8
Quanta Computer Inc.
GMCH Power-2(5 of 6)
Size Custom
Document Number
Rev 2A
Date: Saturday, June 23, 2007
Sheet 9 of 44



PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A3	GMCH Power-3(6 of 6)	1A

Date: Thursday, June 07, 2007 Sheet 10 of 44

Strap table

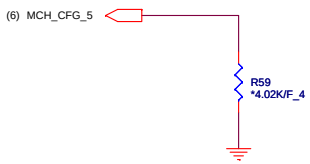
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

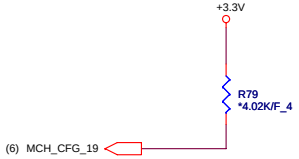
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



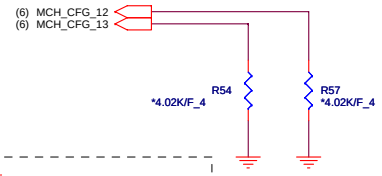
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



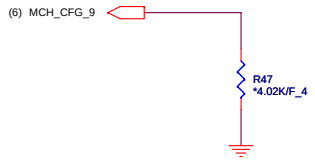
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

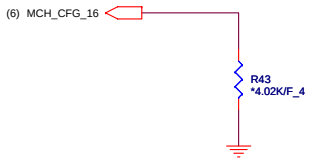


SDVO Present

Strap define at External DVI control page

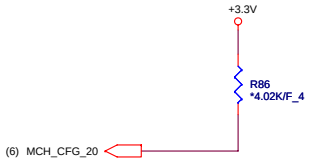
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

PROJECT : MA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH Strap Table	1A
Date: Saturday, June 23, 2007	Sheet 11 of 44	

DDR2 Dual channel A/B PU

DDRII A CHANNEL

+0.9V_DDR_VTT

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

C99 C73 C63 C83 C95 C124 C121 C60 C66 C91 C65 C89 C105 C116

0.1U/10V/X5R_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C61 C123 C97 C108 C112 C85 C109 C62 C94 C59 C70 C78 C86 C75

0.1U/10V/X5R_4

(7,13) DDR_A_MA[0..13]

+0.9V_DDR_VTT

+0.9V_DDR_VTT (33,36)

DDR_B_MA[0..13] (7,13)

DDR_A_MA7 / DDR_A_MA11	RP19	56X2	RP16	56X2	DDR_B_MA11 / DDR_B_MA7
DDR_A_MA4 / DDR_A_MA6	RP15	56X2	RP13	56X2	DDR_B_MA6 / DDR_B_MA4
(7,13) DDR_A_RAS# / (7,13) DDR_A_BS1	RP9	56X2	RP6	56X2	DDR_B_RAS# (7,13) / DDR_B_BS1 (7,13)
(6,13) M_ODT0 / DDR_A_MA13	RP2	56X2	RP1	56X2	DDR_B_MA13 / M_ODT2 (6,13)
DDR_A_MA12 / (7,13) DDR_A_BS2	RP20	56X2	RP10	56X2	DDR_B_MA3 / DDR_B_MA5
DDR_A_MA8 / DDR_A_MA9	RP17	56X2	RP18	56X2	DDR_B_MA9 / DDR_B_MA12
DDR_A_MA5 / DDR_A_MA3	RP12	56X2	RP14	56X2	DDR_B_MA1 / DDR_B_MA8
DDR_A_MA10 / DDR_A_BS0	RP7	56X2	RP5	56X2	DDR_B_MA10 / DDR_B_BS0 (7,13)
(7,13) DDR_A_WE# / (7,13) DDR_A_CAS#	RP4	56X2	RP3	56X2	DDR_B_WE# (7,13) / DDR_B_CAS# (7,13)
DDR_A_MA0 / DDR_A_MA2	RP11	56X2	RP8	56X2	DDR_B_MA2 / DDR_B_MA0

(6,13) M_ODT1 / DDR_A_MA1	R31 R39 R37 R35 R53 R56 R51	56_4	R30 R45 R36 R32 R50 R46 R44	56_4

(6,13) DDR_CS0_DIMMA#
(6,13) DDR_CS1_DIMMA#
(6,13) DDR_CKE0_DIMMA
(6,13) DDR_CKE1_DIMMA
(6,13) DDR_A_MA14

M_ODT3 (6,13)
DDR_B_BS2 (7,13)
DDR_CS2_DIMMB# (6,13)
DDR_CS3_DIMMB# (6,13)
DDR_CKE3_DIMMB (6,13)
DDR_CKE4_DIMMB (6,13)
DDR_B_MA14 (6,13)

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall

+3.3V

+3.3V (2,3,6,8,9,11,13,14,15,16,17,18,19,20,23,25,26,29,30,31,33)

C370 *0.1U/10V/X5R_4

R298 *220_6

U13

(2,13,25) CGCLK_SMB_M	8	SCLK	VCC 1 — LM86_3V
(2,13,25) CGDAT_SMB_M	7	SDA	DXP 2 — DDR_THERMDA
(6,13) PM_EXTTS#0	6	ALERT#	DXN 3 — DDR_THERMDC
(6) PM_EXTTS#1 — R290 *0_4	4	OVERT#	GND 5

*LM86CIMM

*MMBT3904_NL Q19

Quanta Computer Inc.	PROJECT : MA8	
Size: Custom	Document Number: DDR RES. ARRAY	Rev: 1A
Date: Saturday, June 23, 2007	Sheet 12 of 44	

A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN

PC4800 DDR2 SDRAM SO-DIMM (200P)

CN19 — DIMM1_9.2

CKE 0,1
CLOCK 0,1

SMbus address A0

CN20 — DIMM2_5.2

CKE 2,3
CLOCK 3,4

SMbus address A4

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

PROJECT : MA8

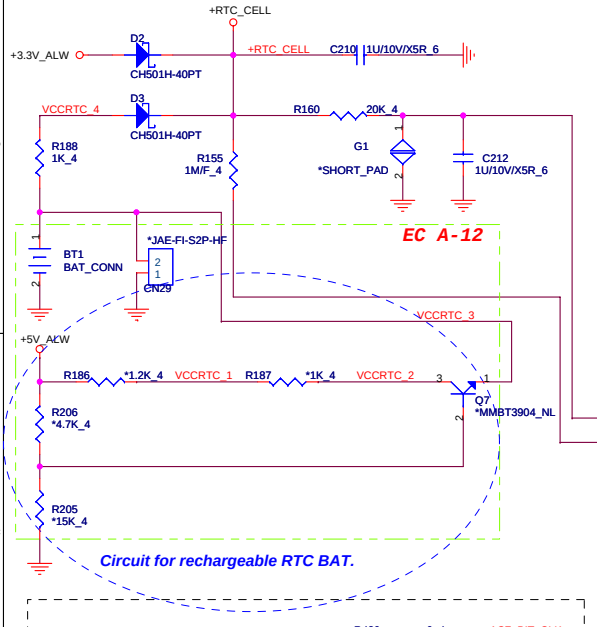
Quanta Computer Inc.

DDR SO-DIMM(200P)

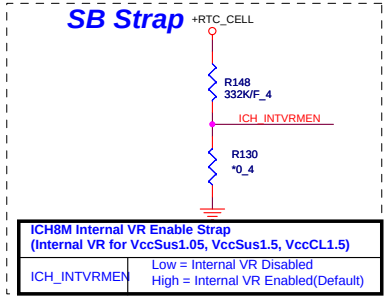
Size: Custom | Document Number | Rev: 1A

Date: Saturday, June 23, 2007 | Sheet 13 of 44

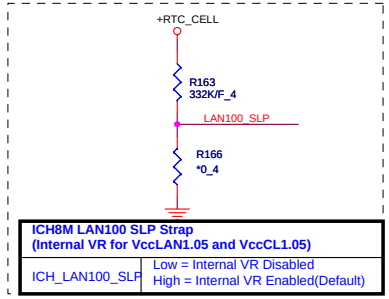
RTC



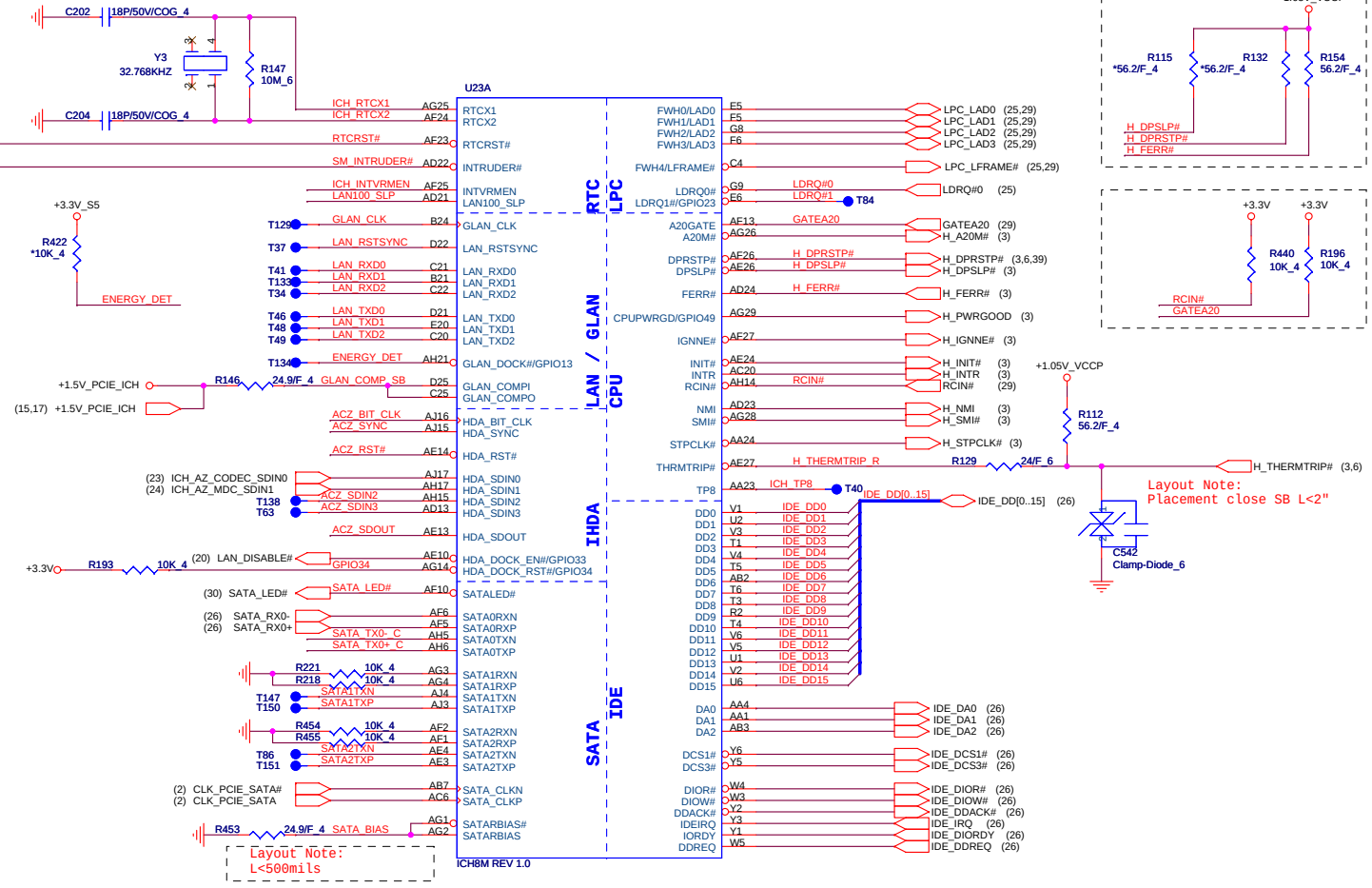
SB Strap

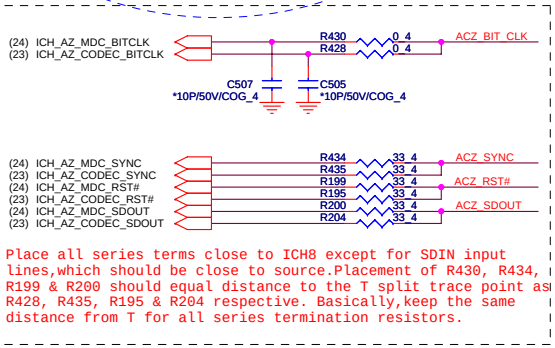


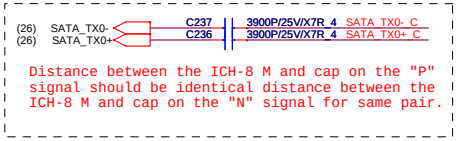
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

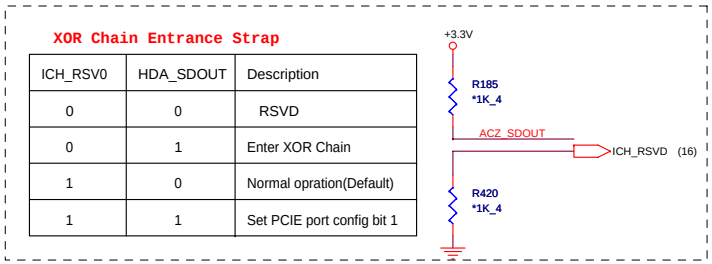


ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)









PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8M HOST(1 of 4)	2A
Date: Saturday, June 23, 2007	Sheet 14 of 44	

Place TX DC blocking caps close ICH8.

MiniCard-1 (WLAN)
(25) PCIE_RX1-
(25) PCIE_RX1+
(25) PCIE_TX1-
(25) PCIE_TX1+
C184 0.1U/10V/X5R_4 PCIE_TXN1_C
C183 0.1U/10V/X5R_4 PCIE_TXP1_C

MiniCard-2
(25) PCIE_RX2-
(25) PCIE_RX2+
(25) PCIE_TX2-
(25) PCIE_TX2+
C186 *0.1U/10V/X5R_4 PCIE_TXN2_C
C185 *0.1U/10V/X5R_4 PCIE_TXP2_C
EC A-09

Express Card (NEWCARD)
(31) PCIE_RXN3
(31) PCIE_RXP3
(31) PCIE_TXN3
(31) PCIE_TXP3
C188 0.1U/10V/X5R_4 PCIE_TXN3_C
C187 0.1U/10V/X5R_4 PCIE_TXP3_C

U23D

PCI-Express Direct Media Interface

PERN1 P27
PERP1 P26
PETN1 N29
PETP1 N28
PERN2 M27
PERP2 M26
PETN2 L29
PETP2 L28
PERN3 K27
PERP3 K26
PETN3 J29
PETP3 J28
PERN4 H27
PERP4 H26
PETN4 G29
PETP4 G28
PERN5 F27
PERP5 F26
PETN5 E29
PETP5 E28
PERN6/GLAN_RXN D27
PERP6/GLAN_RXP D26
PETN6/GLAN_TXN C29
PETP6/GLAN_TXP C28

DMI0RXN V27
DMI0RXP V26
DMI0TXN U29
DMI0TXP U28
DMI1RXN Y27
DMI1RXP Y26
DMI1TXN W29
DMI1TXP W28
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA29
DMI2TXP AA28
DMI3RXN AD27
DMI3RXP AD26
DMI3TXN AC29
DMI3TXP AC28
DMI_CLKN T26
DMI_CLKP T25
DMI_ZCOMP Y23
DMI_IRCOMP Y24

DMI_MTX_IRX_N0 (6)
DMI_MTX_IRX_P0 (6)
DMI_MRX_ITX_N0 (6)
DMI_MRX_ITX_P0 (6)
DMI_MTX_IRX_N1 (6)
DMI_MTX_IRX_P1 (6)
DMI_MRX_ITX_N1 (6)
DMI_MRX_ITX_P1 (6)
DMI_MTX_IRX_N2 (6)
DMI_MTX_IRX_P2 (6)
DMI_MRX_ITX_N2 (6)
DMI_MRX_ITX_P2 (6)
DMI_MTX_IRX_N3 (6)
DMI_MTX_IRX_P3 (6)
DMI_MRX_ITX_N3 (6)
DMI_MRX_ITX_P3 (6)
CLK_PCIE_ICH# (2)
CLK_PCIE_ICH (2)

+1.5V_PCIE_ICH
R158 24.9/F_4
DMI_IRCOMP_R

Layout Note:
DMI_IRCOMP_R<500mils

SPI

SPI_CLK C23
SPI_CS0# B23
SPI_CS1# E22
SPI_MOSI D23
SPI_MISO F21

T35
T13
T38 SPI_CS1# R
T36
T45

USB

OC0# AJ19
OC1#/GPIO40 AG16
OC2#/GPIO41 AG15
OC3#/GPIO42 AE15
OC4#/GPIO43 AF15
OC5#/GPIO29 AG17
OC6#/GPIO30 AD12
OC7#/GPIO31 AJ18
OC8# AD14
OC9# AH18

USBP0N G3
USBP0P G2
USBP1N H5
USBP1P H4
USBP2N H2
USBP2P H1
USBP3N J3
USBP3P J2
USBP4N K5
USBP4P K4
USBP5N K2
USBP5P K1
USBP6N L3
USBP6P L2
USBP7N M5
USBP7P M4
USBP8N M2
USBP8P M1
USBP9N N3
USBP9P N2
USBRBIAS# F2
USBRBIAS F3

USBP0- (27)
USBP0+ (27)
USBP1- (27)
USBP1+ (27)
USBP2- (27)
USBP2+ (27)
USBP3- (27)
USBP3+ (27)
USBP4- (22)
USBP4+ (22)
USBP5- (31)
USBP5+ (31)
USBP6- (25)
USBP6+ (25)
USBP7- (25)
USBP7+ (25)
USBP8- (18)
USBP8+ (18)
USBP9- (28)
USBP9+ (28)

System
System
System
System
CARDREADER
NEWCARD
MiniCard-1 (WLAN)
MiniCard-2(reserved)
WEB CAM
BLUETOOTH

USB_RBIAS_PN
R225 22.6/F_6

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH8M REV 1.0

(20) PCIE_RX6-/GLAN_RX-
(20) PCIE_RX6+/GLAN_RX+
(20) PCIE_TX6-/GLAN_TX-
(20) PCIE_TX6+/GLAN_TX+
C190 0.1U/10V/X5R_4 GLAN_TXN_C
C189 0.1U/10V/X5R_4 GLAN_TXP_C

(27) USB_OC0#
(27) USB_OC1#
(27) USB_OC2#
(27) USB_OC3#
(25,30) WLAN_RF_OFF#
T136
USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#
USB_OC4#
USB_OC5#
WLAN_RF_OFF#
GPIO31
OC8#
OC9#

+3.3V_SUS
RP25
USB_OC2# 6
USB_OC5# 7
OC9# 8
USB_OC0# 9
+3.3V_SUS 10
5 USB_OC3#
4 OC8#
3 WLAN_RF_OFF#
2 USB_OC4#
1
10KX8

ICH8 Boot BIOS select

Boot BIOS Strap			
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

SPI_CS1# R R165 *1K_4
PCI_GNT0# R214 *1K_4

A16 SWAP Override strap

PCI_GNT3#	Low = A16 swap override enabled High = Default

PCI_GNT3# R201 *1K_4

EC A-04
+3.3V_SUS R322 10K_4 GPIO31
+3.3V_SUS R182 10K_4 USB_OC1#

SB-PCI

U23B

PCI

AD0 D20
AD1 E19
AD2 D19
AD3 A20
AD4 D17
AD5 A21
AD6 A19
AD7 C19
AD8 A18
AD9 B16
AD10 A12
AD11 E16
AD12 A14
AD13 G16
AD14 A15
AD15 B6
AD16 C11
AD17 A9
AD18 D11
AD19 B12
AD20 C12
AD21 D10
AD22 C7
AD23 F13
AD24 E11
AD25 E13
AD26 E12
AD27 D8
AD28 A6
AD29 E8
AD30 D6
AD31 A3

REQ0# A4 PCI_REQ0# T148
GNT0# D7 PCI_GNT0#
REQ1#/GPIO50 E18 BOARD_ID1 BOARD_ID1 (16)
GNT1#/GPIO51 C18 BOARD_ID2 BOARD_ID2 (16)
REQ2#/GPIO52 B19 PCI_REQ2# T135
GNT2#/GPIO53 E18 PCI_GNT2# T58
REQ3#/GPIO54 A11 PCI_REQ3# T140
GNT3#/GPIO55 C10 PCI_GNT3#

C/BE0# C17
C/BE1# E15
C/BE2# F16
C/BE3# E17

IRDY# C8 PCI_IRDY# T74
PAR D9
PCIRST# G6 PCIRST# (19)
DEVSEL# D16 PCI_DEVSEL# T61
PERR# A7 PCI_PERR# T145
PLOCK# B7 PCI_PLOCK# T144
SERR# E10 PCI_SERR# T69
STOP# C16 PCI_STOP# T60
TRDY# C9 PCI_TRDY# T72
FRAME# A17 PCI_FRAME# T137

PLTRST# AG24 PLTRST#_NB
PCICLK B10 CLK_PCI_ICH CLK_PCI_ICH (2)
PME# G7

Interrupt I/F

T78 PCI_PIRQA# F9 PIRQA#
T146 PCI_PIRQB# B5 PIRQB#
T85 PCI_PIRQC# C5 PIRQC#
T142 PCI_PIRQD# A10 PIRQD#

PIRQE#/GPIO2 F8 GPIO2
PIRQF#/GPIO3 G11 GPIO3 T82
PIRQG#/GPIO4 E12 ICH_GPIO4_PIRQG# T64
PIRQH#/GPIO5 B3 ICH_GPIO5_PIRQH# T66 T149

CLK_PCI_ICH
R446 *10_4
C509 *10P/50V/COG_4
Reserved for EMI. Place resister and cap close to ICH.

PLTRST#_NB (6)

+3.3V
C191 0.1U/10V/X5R_4
U4 TC7SH08FU(F)
PLTRST# (16,20,25,26,31)
R114 100K_4

PCI Pullups

+3.3V
PCI_REQ2# R429 8.2K_4
PCI_REQ3# R442 8.2K_4
PCI_FRAME# R433 8.2K_4

RP26
PCI_SERR# 6
PCI_TRDY# 7
PCI_IRDY# 8
PCI_PIRQD# 9
+3.3V 10
5 ICH_GPIO4_PIRQG#
4 GPIO3
3 PCI_DEVSEL#
2 PCI_STOP#
1
8.2KX8

RP27
PCI_PERR# 6
PCI_PLOCK# 7
PCI_PIRQA# 8
GPIO2 9
+3.3V 10
5 PCI_PIRQC#
4 ICH_GPIO5_PIRQH#
3 PCI_REQ0#
2 PCI_PIRQB#
1
8.2KX8

PROJECT : MA8
Quanta Computer Inc.

Size	Document Number	Rev
A3	ICH8M PCIE(2 of 4)	2A

Date: Saturday, June 23, 2007 Sheet 15 of 44

+3.3V_S5
R184 10K_4 ICH_RI#
R164 10K_4 SCI#
R167 1K_4 ICH_PCIE_WAKE#
R168 10K_4 ICH_CL_RST1#

+3.3V_S5
R413 2.2K_4 ICH_SMBCLK
R177 2.2K_4 ICH_SMBDATA
R181 10K_4 AMT_SMBCLK
R170 10K_4 AMT_SMBDATA

+3.3V
R447 8.2K_4
CLKRUN#
R448 *10K_4
Option to " Disable " clkrun. Pulling it down will keep the clks running.

Place these close to ICH8.
CLK_ICH_48M → R224 *10_4 → C246 *10P/50V/COG_4
CLK_ICH_14M → R215 *33_4 → C235 *10P/50V/COG_4

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

U23C
ICH8M REV 1.0

SMB
(2,31) ICH_SMBCLK → ICH_SMBCLK → AJ26 SMBCLK
(2,31) ICH_SMBDATA → ICH_SMBDATA → AD19 SMBDATA
T42 → ICH_CL_RST1# → AG21 LINKALERT#
AMT_SMBCLK → AC17 SMLINK0
AMT_SMBDATA → AE19 SMLINK1
ICH_RI# → AF17 RI#

SATA GPIO
SATA0GP/GPIO21 AJ12 → R444 8.2K_4 → +3.3V
SATA1GP/GPIO19 AJ10 → R449 8.2K_4 → +3.3V
SATA2GP/GPIO36 AE11 → R208 8.2K_4 → +3.3V
SATA3GP/GPIO37 AG11 → R207 8.2K_4 → +3.3V

Clocks
CLK14 AG9 ← CLK_ICH_14M → CLK_ICH_14M (2)
CLK48 G5 ← CLK_ICH_48M → CLK_ICH_48M (2)
SUSCLK D3 ← ICH_SUSCLK → T87

SYS GPIO
(25) LPC_PD# → F4 SUS_STAT#/LPCPD#
(3) ITP_DBRESET# → AD15 SYS_RESET#
(6) PM_BMBUSY# → AG12 BMBUSY#/GPIO0
(29) SCI# → SCI# → AG22 SMBALERT#/GPIO11
(2) H_STP_PCI# → AE20 STP_PCI#/GPIO15
(2) H_STP_CPU# → AG18 STP_CPU#/GPIO25
(25) CLKRUN# → CLKRUN# → AH11 CLKRUN#/GPIO32
(20,25,31) ICH_PCIE_WAKE# → ICH_PCIE_WAKE# → AE17 WAKE#
(25,29) IRQ_SERIRQ → IRQ_SERIRQ → AE12 SERIRQ
(3) THERM_ALERT# → THERM_ALERT# → AC13 THRM#
VR_PWRGD_CLKEN → AJ20 VRMPWRGD
T132 → TP7 → AJ22 TP7

Power MGT
SLP_S3# AG23 → SLP_S3# → R127 100/F_4 → SUSB# (29)
SLP_S4# AE21 → SLP_S4# → R131 100/F_4 → SUSC# (29)
SLP_S5# AD18 → SLP_S5# → T57
S4_STATE#/GPIO26 AH27 → S4_STAT# (29)
PWROK AE23 ← ICH_PWROK
DPRSLPVR/GPIO16 AJ14 ← PM_DPRSLPVR_R ← R438 100/F_4 ← PM_DPRSLPVR → PM_DPRSLPVR (6,39)
BATLOW# AE21 ← PM_BATLOW#_R
PWRBTN# C2 ← DNBSWON# → DNBSWON# (29)
LAN_RST# AH20 ← PM_LAN_ENABLE_R ← R425 *0_4 / R111 0_4 / R116 *0_4 / R117 100/F_4 ← RSMRST# → PM_LAN_RST# (20,29) / PLTRST# (15,20,25,26,31)
RSMRST# AG27 ← PM_RSMRST#_R → RSMRST# (29)
CK_PWRGD E1 → CLK_PWRGD (2)
CLPWROK E3 ← PWROK → PWROK (6,29)
SLP_M# AJ25 → SUSM# (29)

GPIO Controller Link
CL_CLK0 F23 → CL_CLK0 (6)
CL_CLK1 AE18 ← CL_CLK1 → T55
CL_DATA0 F22 → CL_DATA0 (6)
CL_DATA1 AF19 ← CL_DATA2 → T47
CL_VREF0 D24 ← CL_VREF0_SB
CL_VREF1 AH23 ← CL_VREF1_SB
CL_RST# AJ23 → ICH_CL_RST0# (6)

MISC
GPIO0 T133 → GPIO1 AJ8
(18) FPBACK# → FPBACK# → RSVD_GPIO7 AJ9
(29) KBSMI# → KBSMI# → AE16
T44 → GPIO12 → AC19
BOARD_ID0 AG8
(23) MIC_DET → MIC_DET → BOARD_ID3 AH12
T79 → GPIO22 → AE11
(28) BT_ON# → BT_ON# → AG10
T56 → GPIO28 → AH25
(2) SATA_CLKREQ# → AD16
T80 → GPIO38 → AG13
T14 → GPIO39 → AF9
T81 → GPIO48 → AJ11
(23) ACZ_SPKR → ACZ_SPKR → AD10 SPKR
(6) MCH_ICH_SYNC# → R443 0_4 → MCH_ICH_SYNC#_R → AD9 MCH_SYNC#
(14) ICH_RSVD → AJ13 TP3
AJ21
MEM_LED/GPIO24 AJ27 ← GPIO24
ME_EC_ALERT/GPIO10 AJ24 ← ME_EC_ALERT → T130
EC_ME_ALERT/GPIO14 AF22 ← EC_ME_ALERT
WOL_EN/GPIO9 AG19 ← LAN_WOL_EN

+3.3V_S5
R157 10K_4 PM_BATLOW#_R
R190 10K_4 KBSMI#
R436 10K_4 GPIO28
R421 10K_4 BT_ON#
R456 10K_4 DNBSWON#
R173 *10K_4 EC_ME_ALERT
R418 10K_4 ME_EC_ALERT

+3.3V
R189 8.2K_4 THERM_ALERT#
R441 *10K_4 MCH_ICH_SYNC#_R
R202 10K_4 IRQ_SERIRQ
R432 *2.2K_4 VR_PWRGD_CLKEN#
R450 10K_4 RSVD_GPIO7
R451 10K_4 FPBACK#

+3.3V_S5 → R417 3.24K/F_4 → R416 453/F_4 → C501 0.1U/10V/X5R_4
+3.3V → R152 3.24K/F_4 → R151 453/F_4 → C206 0.1U/10V/X5R_4

(39) VR_PWRGD_CLKEN# → VR_PWRGD_CLKEN → U22 NL17SZ14DFT2G
+3.3V → C506 0.1U/10V/X5R_4
VR_PWRGD_CLKEN → R424 100K_4

No Reboot strap
+3.3V → *10K_4 R203 ACZ_SPKR
HDA_SPKR: Low = Default, High = No Reboot

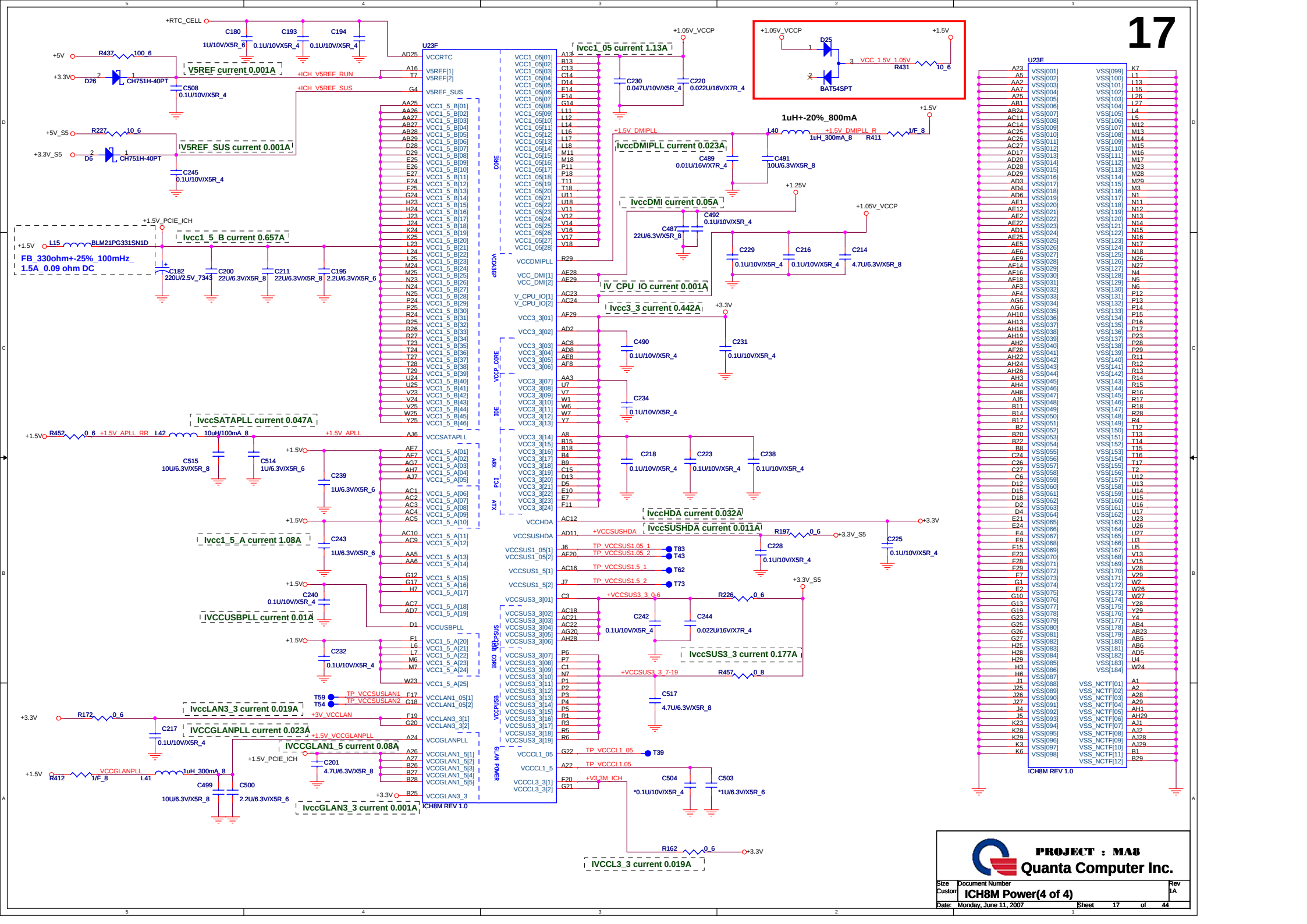
PM_DPRSLPVR R439 *100K_4
RSMRST# R109 10K_4
PM_LAN_ENABLE_R R423 *1M_4
LAN_WOL_EN R176 100K_4

+3.3V +3.3V_SUS
From Core , GMCH → R427 2K_4 → C502 0.1U/10V/X5R_4
(6,39) DELAY_VR_PG →
(6,29) PWROK →
U21 TC7SH08FU(F) → ICH_PWROK
From EC , GMCH → R426 100K_4
R419 10K_4

Board ID	ID3	ID2	ID1	ID0	Remark
1.Default(C-test)	1	1	1	1	
2.RSV	1	0	0	0	
3.RSV	1	0	0	1	
4.RSV	1	0	1	0	
5.RSV	1	0	1	1	
6.RSV	1	1	0	0	
7.RSV	1	1	0	1	
8.RSV	1	1	1	0	

GPIO[20]--Integrated Pull-Down 20K.
+3.3V → R212 1K_4 → R213 *10K_4
+3.3V → R175 10K_4 → R174 *10K_4
+3.3V → R179 10K_4 → R180 *10K_4
+3.3V → R217 10K_4 → R216 *10K_4
BOARD_ID0
BOARD_ID1 → BOARD_ID1 (15)
BOARD_ID2 → BOARD_ID2 (15)
BOARD_ID3

PROJECT : MA8
Quanta Computer Inc.
Size: Custom | Document Number: ICH8M GPIO(3 of 4) | Rev: 1A
Date: Saturday, June 23, 2007 | Sheet 16 of 44


+RTC_CELL
C180 1U/10V/X5R_6
C193 0.1U/10V/X5R_4
C194 0.1U/10V/X5R_4
+5V
R437 100_6
+3.3V
D26 CH751H-40PT
V5REF current 0.001A
+ICH_V5REF_RUN
C508 0.1U/10V/X5R_4
+ICH_V5REF_SUS
+5V_S5
R227 10_6
+3.3V_S5
D6 CH751H-40PT
V5REF_SUS current 0.001A
C245 0.1U/10V/X5R_4
+1.5V_PCIE_ICH
+1.5V
L15 BLM21PG331SN1D
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
Ivcc1_5_B current 0.657A
C182 220U/2.5V_7343
C200 22U/6.3V/X5R_8
C211 22U/6.3V/X5R_8
C195 2.2U/6.3V/X5R_6
U23F
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
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VCC1_5_B[45]
VCC1_5_B[46]
CORE
VCCA3GP
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCC3_3[01]
VCC3_3[02]
VCC3_3[03]
VCC3_3[04]
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VCC3_3[08]
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IDE
AGP
PCI
ATX
VCCHDA
VCCSUSHDA
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
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VCCSUS3_3[19]
SUS_CORE
VCCSUS3_3
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
GLAN POWER
VCCSUS3_3
IvccSATAPLL current 0.047A
R452 0_6
+1.5V_APLL_RR
L42 10uH/100mA_8
+1.5V_APLL
C515 10U/6.3V/X5R_8
C514 1U/6.3V/X5R_6
VCCSATAPLL
VCC1_5_A[01]
VCC1_5_A[02]
VCC1_5_A[03]
VCC1_5_A[04]
VCC1_5_A[05]
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VCC1_5_A[24]
VCC1_5_A[25]
C239 1U/6.3V/X5R_6
C243 1U/6.3V/X5R_6
C240 0.1U/10V/X5R_4
C232 0.1U/10V/X5R_4
Ivcc1_5_A current 1.08A
IVCCUSBPLL current 0.01A
VCCUSBPLL
TP_VCCSUSLAN1
TP_VCCSUSLAN2
VCCLAN1_05[1]
VCCLAN1_05[2]
IvccLAN3_3 current 0.019A
R172 0_6
+3.3V
+3V_VCCLAN
VCCLAN3_3[1]
VCCLAN3_3[2]
C217 0.1U/10V/X5R_4
IVCCGLANPLL current 0.023A
+1.5V_VCCGLANPLL
VCCGLANPLL
IVCCGLAN1_5 current 0.08A
+1.5V_PCIE_ICH
C201 4.7U/6.3V/X5R_8
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN1_5[5]
VCCGLAN3_3
IvccGLAN3_3 current 0.001A
+1.5V
R412 1/F_8
VCCGLANPLL
L41 1uH_300mA_8
C499 10U/6.3V/X5R_8
C500 2.2U/6.3V/X5R_6
ICH8M REV 1.0
Ivcc1_05 current 1.13A
+1.05V_VCCP
C230 0.047U/10V/X5R_4
C220 0.022U/16V/X7R_4
D25 BAT54SPT
VCC_1.5V_1.05V
R431 10_6
+1.5V
1uH+-20%_800mA
L40 1uH_300mA_8
+1.5V_DMIPLL_R
R411 1/F_8
IvccDMIPLL current 0.023A
C489 0.01U/16V/X7R_4
C491 10U/6.3V/X5R_8
IvccDMI current 0.05A
+1.25V
C492 0.1U/10V/X5R_4
C487 22U/6.3V/X5R_8
C229 0.1U/10V/X5R_4
C216 0.1U/10V/X5R_4
C214 4.7U/6.3V/X5R_8
IV_CPU_IO current 0.001A
Ivcc3_3 current 0.442A
+3.3V
C490 0.1U/10V/X5R_4
C231 0.1U/10V/X5R_4
C234 0.1U/10V/X5R_4
C218 0.1U/10V/X5R_4
C223 0.1U/10V/X5R_4
C238 0.1U/10V/X5R_4
IvccHDA current 0.032A
IvccSUSHDA current 0.011A
+VCCSUSHDA
R197 0_6
+3.3V_S5
C228 0.1U/10V/X5R_4
C225 0.1U/10V/X5R_4
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
T83
T43
T62
T73
+3.3V_S5
+VCCSUS3_3_0-6
R226 0_6
C242 0.1U/10V/X5R_4
C244 0.022U/16V/X7R_4
IvccSUS3_3 current 0.177A
+VCCSUS3_3_7-19
R457 0_8
C517 4.7U/6.3V/X5R_8
TP_VCCCL1_05
TP_VCCCL1.05
T39
+V3.3M_ICH
C504 *0.1U/10V/X5R_4
C503 *1U/6.3V/X5R_6
R162 0_6
+3.3V
IVCCL3_3 current 0.019A
U23E
VSS[001]
VSS[002]
VSS[003]
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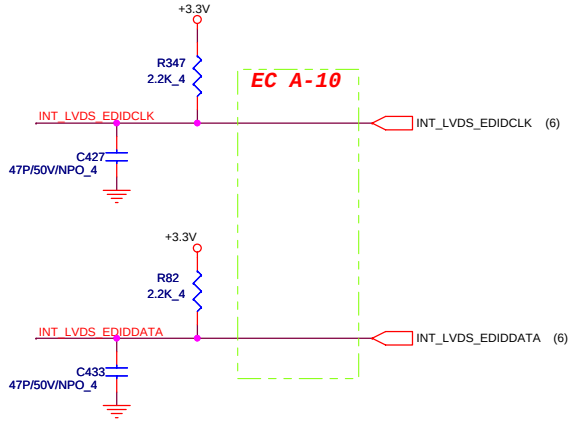
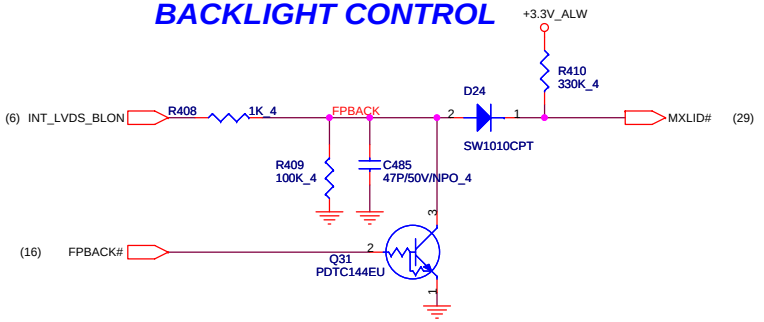
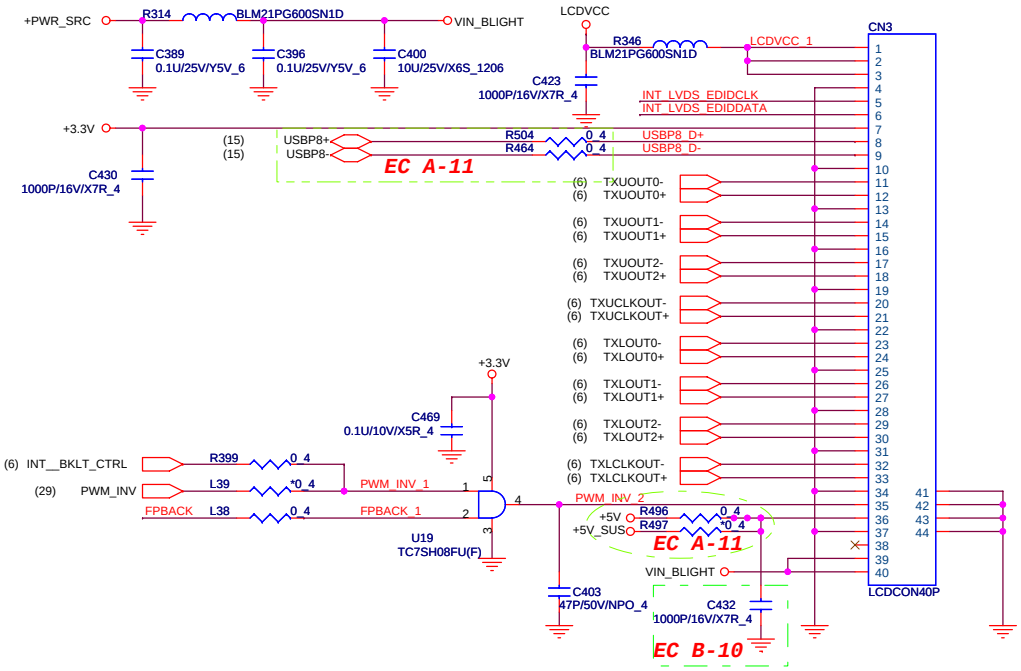
ICH8M REV 1.0
PROJECT : MA8
Quanta Computer Inc.
Size: Custom
Document Number: ICH8M Power(4 of 4)
Rev: 1A
Date: Monday, June 11, 2007
Sheet 17 of 44



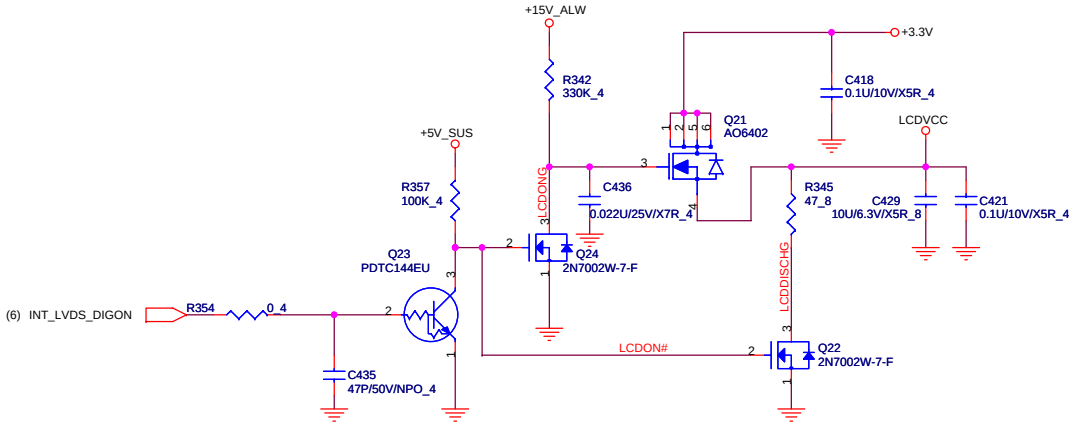
BACKLIGHT CONTROL



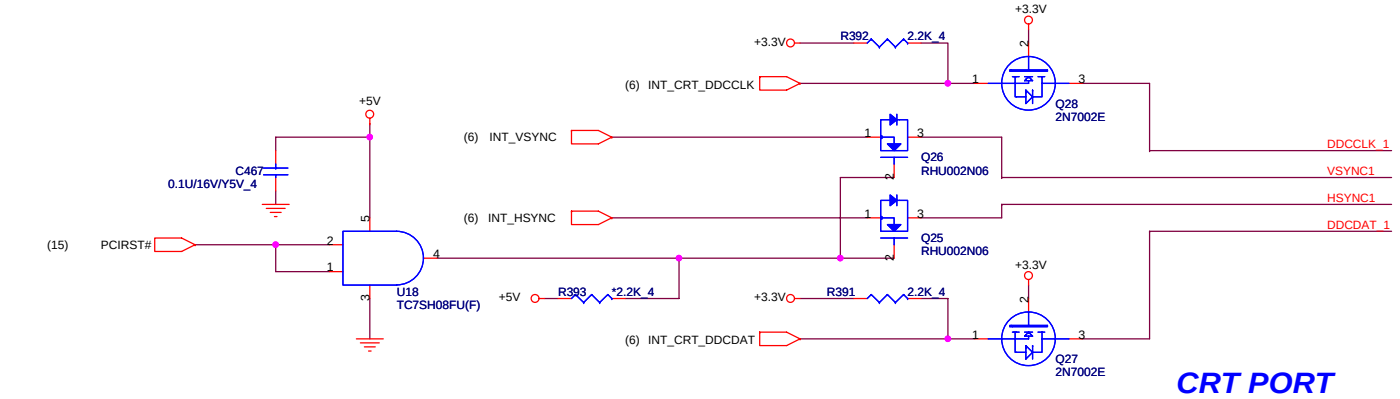
LCD CONNECTOR(Include WEB CAM function)



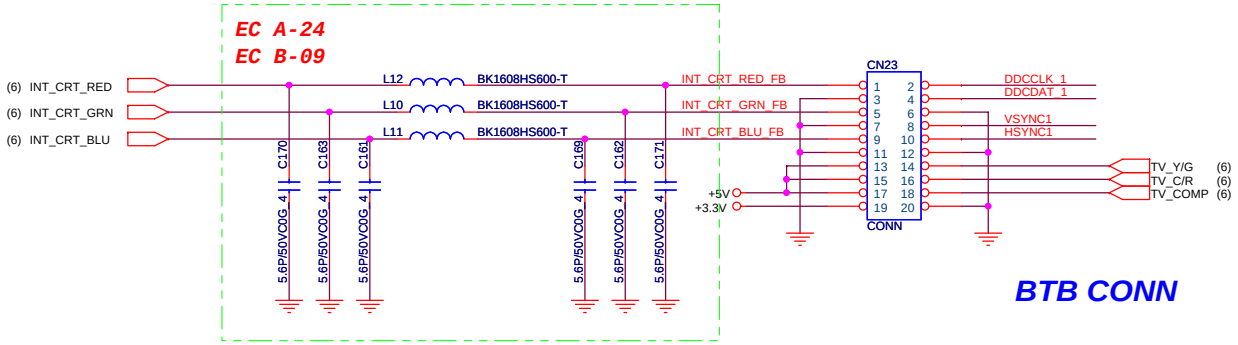
PANEL VCC CONTROL



PROJECT : MA8		
Quanta Computer Inc.		
Size: A3	Document Number: LVDS/LCD CONN/LID/WEB CAM	Rev: 2A
Date: Saturday, June 23, 2007	Sheet 18 of 44	



CRT PORT



BTB CONN

PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A3	CRT PORT,TV	1A

Date: Saturday, June 23, 2007 Sheet 19 of 44

E : Stuffed for 8101E(10/100)

EC A-17

EC A-21

EC A-20

EC B-08

TOP view		Orange LED		Green LED	
O		Solid	Link	Solid	100Mb Link
G		Blink	Data Transfer	Off	>100Mb Link
		Off	No Link		

RJ45

8101E pop 2K depop 2.49K
8111B depop 2K pop 2.49K

RTL8101E/8111B

U11

for 93C56 used. NC if 93C46 is used.

U14 93C46-3GR

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

NS892403/2405

U1 NS892405:10/100

BLOCK A is only for RTL8101E application.

Block A

PARTS REFRENCE	RTL8101E	RTL8111B
R14 R15 R16 R17	ASM	NoASM

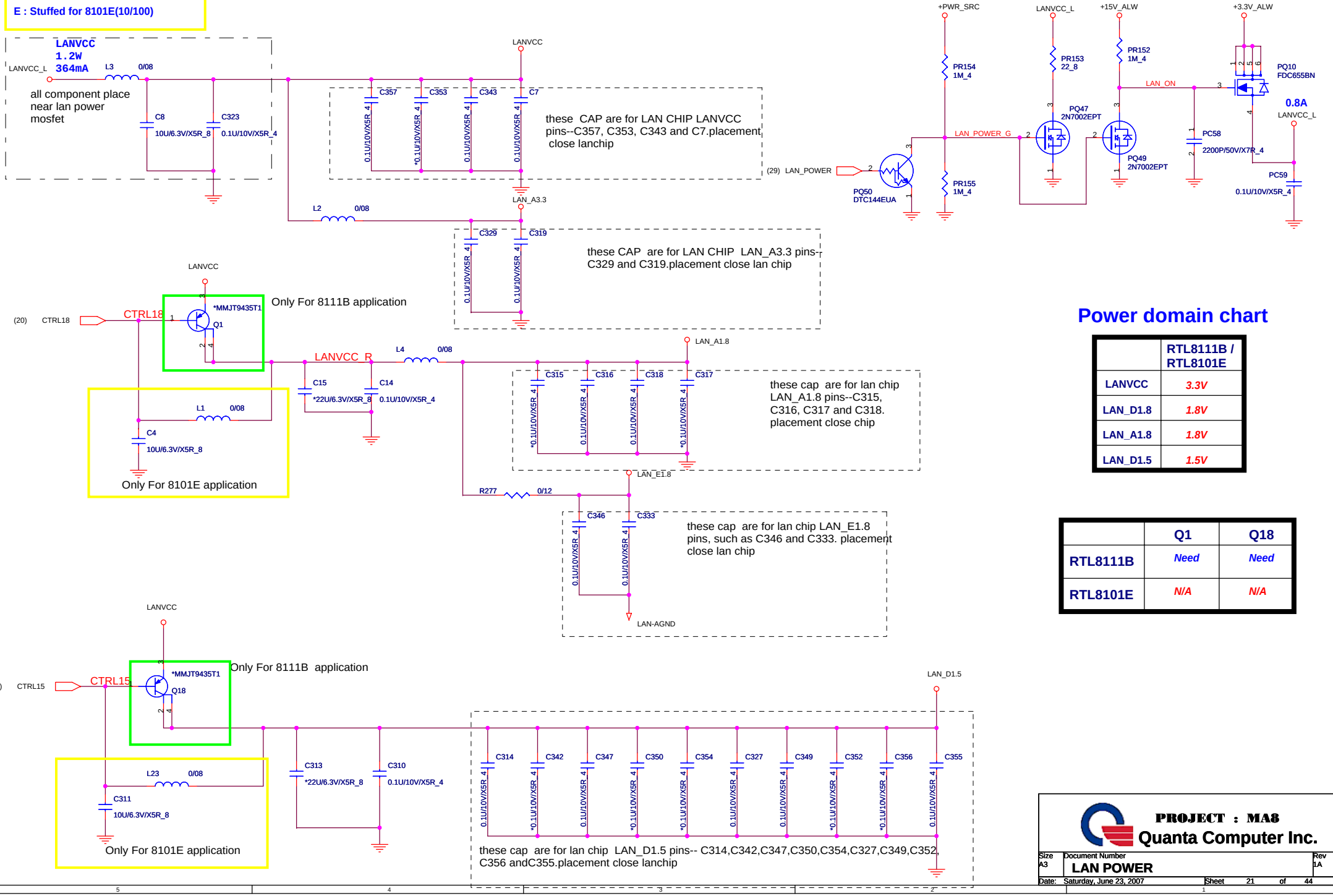
PROJECT : MA8
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN-REALTEK 8101E	2A

Date: Saturday, June 23, 2007 Sheet 20 of 44

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	*3.3V*
LAN_D1.8	*1.8V*
LAN_A1.8	*1.8V*
LAN_D1.5	*1.5V*

	Q1	Q18
RTL8111B	*Need*	*Need*
RTL8101E	*N/A*	*N/A*

PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN POWER	1A

Date: Saturday, June 23, 2007 Sheet 21 of 44

Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

EC B-07

U2

CF_CD# 13, GPIO0 14, CF_D10 15, CF_D9 16, CF_D2 17, CF_D8/SM_CD# 18, CF_D1/XD_CD# 19, CF_D0/SM_WPM#/SD_WP 20, CF_A0/SD_CD# 21, CF_DMACK# 22, CF_A1/XD_D4 23, CF_DMARQ 24

XD_CLE/CF_D3 43, XD_CE#/CF_D11 42, XD_ALE/CF_D4 41, SD_DAT2/XD_RE#/CF_D12 40, SD_DAT3/XD_WE#/CF_D5 39, XD_RDY/CF_D13 38, SD_DAT4/XD_WP#/CF_D6 37, SD_CMD 36, SD_DAT5/XD_D0/CF_D14 35, SD_CLK/XD_D1/MS_CLK/CF_D7 34, SD_DAT6/XD_D7/MS_D3/CF_D15 33, CF_CS0# 30, MS_INS#/CF_IORD# 29, SD_DAT7/XD_D2/MS_D2/CF_IOWR# 28, SD_DAT0/XD_D6/MS_D0/CF_RST# 27, SD_DAT1/XD_D3/MS_D1/CF_IORDY 26, XD_D5/MS_BS/CF_A2 25

SP0 18, SP1 19, SP2 20, SP3 21, SP4 23

R69 6.25K/F_4 RREF 2 RREF

(15) USBP4- R72 0_4 DM 4 DM

(15) USBP4+ R75 0_4 DP 5 DP

20P/50V/NPO_6 C110 XTLO 48 XTLO

R60 270k_6 Y1 12MHz/30PPM

20P/50V/NPO_6 C111 XTLI 47 XTLI

EC B-03

MODE_SEL 45 MODE_SEL

R52 10K_4 C120 *0.1U/10V/X5R_4

+3.3V_SUS R55 100K_4 RST# 44 RST#

C119 1U/6.3V/X5R_6

Realtek RTS5158

AV_PLL_IN 1 AV_PLL C155 0.1U/10V/X5R_4 R90 0_4 C156 1U/6.3V/X5R_6

VREG_OUT 10 VREG

5V_IN 8 5V_IN

A3V3_IN 3

D3V3_OUT 33 C136 0.1U/10V/X5R_4 C142 0.1U/10V/X5R_4 D3V3

11 C158 0.1U/10V/X5R_4 C133 4.7U/10V/X5R_8

5V to 3V3 as digital power

C149 0.1U/10V/X5R_4 R88 0_6 C148 4.7U/10V/X5R_8 +5V_SUS

A3V3_OUT 7 C129 C143 A3V3

CARD_3V3_OUT 9 CARD_3V3 C151 1U/6.3V/X5R_6

3.3V Power for all cards

AG33 6, AG_PLL 46, DGND2 32, DGND1 12

0.1U/10V/X5R_4, 4.7U/6.3V/X5R_8

5V to 3V3 as analog power

CARD_3V3 C414 C428 C440 0.1U/10V/X5R_4

7 IN1 CARD-READER (PUSH-PUSH)

Support MMC/SD/MS/xD/CF/SM Cards

EC B-07

SP0	R742	33_4	SM_CD#	T23
SP1	R748	33_4	XD_CD#	
SP2	R737	33_4	SD_WP	
SP3	R753	33_4	SD_CD#	
SP4	R744	33_4	XD_D4	
SP5	R746	33_4	XD_D5/MS_BS	
SP6	R756	33_4	SD_DAT1/XD_D3/MS_D1	
SP7	R745	33_4	SD_DAT0/XD_D6/MS_D0	
SP8	R755	33_4	SD_DAT7/XD_D2/MS_D2	
SP9	R754	33_4	MS_INS#	
SP10	R752	33_4	MS_D3/SD_DAT6/XD_D7	
SP11	R741	33_4	XD_D1/SD_CLK/MS_SCLK	
SP12	R743	33_4	SD_DAT5/XD_D0	
SP13	R740	33_4	SD_DAT4/XD_WP#	
SP14	R747	33_4	XD_R/B#	
SP15	R739	33_4	SD_DAT3/XD_WE#	
SP16	R751	33_4	SD_DAT2/XD_RE#	
SP17	R738	33_4	XD_ALE	
SP18	R749	33_4	XD_CE#	
SP19	R750	33_4	XD_CLE	

CN21

SD_CD# 1, SD_WP 2, CARD_3V3 3, 4, SD_DAT1/XD_D3/MS_D1 5, MS_D3/SD_DAT6/XD_D7 6, SD_DAT0/XD_D6/MS_D0 7, SD_DAT0/XD_D6/MS_D0 8, XD_D5/MS_BS 9, SD_DAT7/XD_D2/MS_D2 10, XD_D4 11, SD_DAT1/XD_D3/MS_D1 12, MS_D3/SD_DAT6/XD_D7 13, XD_D5/MS_BS 14, XD_D1/SD_CLK/MS_SCLK 15, SD_DAT1/XD_D3/MS_D1 16, SD_DAT7/XD_D2/MS_D2 17, SD_DAT0/XD_D6/MS_D0 18, CARD_3V3 19, SD_DAT7/XD_D2/MS_D2 20, XD_D1/SD_CLK/MS_SCLK 21

SD_CD, SD_WP, 7IN1_GND1, XD_VCC, SD_DAT1, XD_DAT7, XD_DAT6, SD_DAT0, XD_DAT5, MMC_DAT7, XD_DAT4, XD_DAT3, MMC_DAT6, MS_BS, SD_CLK, MS_DAT1, XD_DAT2, MS_DAT0, SD_VCC, MS_DAT2, XD_DAT1

XD_DAT0 22, MS-INS 23, MMC_DAT5 24, MS_DAT3 25, SD_CMD 26, MS_SCLK 27, MMC_DAT4 28, MS_VCC 29, SD_DAT3 30, SD_DAT2 31, XD_WP 32, XD_WE 33, XD_ALE 34, XD_CLE 35, XD_CE 36, XD_RE 37, XD_R/B 38, 7IN1_GND2 39, XD_CD 40, 7IN1_GND3 41, 7IN1_GND4 42

SD_DAT5/XD_D0 22, MS_INS# 23, SD_DAT5/XD_D0 24, MS_D3/SD_DAT6/XD_D7 25, SD_CMD 26, XD_D1/SD_CLK/MS_SCLK 27, SD_DAT4/XD_WP# 28, CARD_3V3 29, SD_DAT3/XD_WE# 30, SD_DAT2/XD_RE# 31, SD_DAT4/XD_WP# 32, SD_DAT3/XD_WE# 33, XD_ALE 34, XD_CLE 35, XD_CE# 36, SD_DAT2/XD_RE# 37, XD_R/B# 38, XD_CD# 40

*10K_4 R332 CARD_3V3

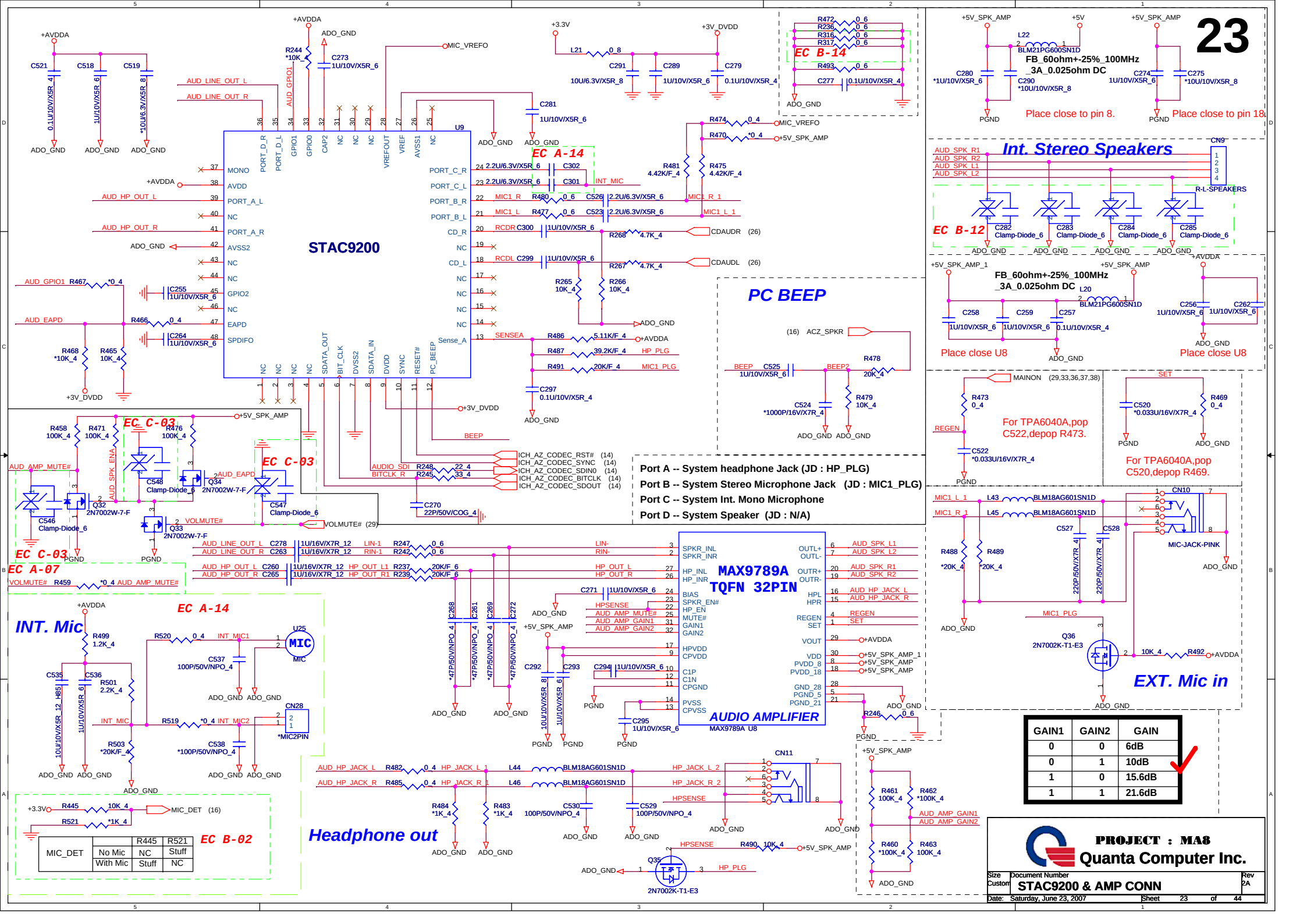
R015-610-NM

PROJECT : MA8

Quanta Computer Inc.

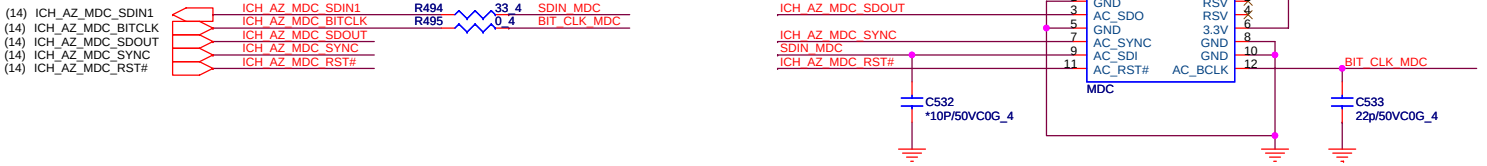
Size	Document Number	Rev
A3	RTS5158 CONTROLLER	1A

Date: Saturday, June 23, 2007 Sheet 22 of 44


23
STAC9200
MAX9789A
TQFN 32PIN
AUDIO AMPLIFIER
MAX9789A U8
PC BEEP
Int. Stereo Speakers
R-L-SPEAKERS
INT. Mic
Headphone out
EXT. Mic in
EC A-14
EC B-12
EC C-03
EC A-07
EC B-02
Port A -- System headphone Jack (JD : HP_PLG)
Port B -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port C -- System Int. Mono Microphone
Port D -- System Speaker (JD : N/A)
Place close to pin 8.
Place close to pin 18.
Place close U8
Place close U8
For TPA6040A,pop C522,depop R473.
For TPA6040A,pop C520,depop R469.
MIC_DET
No Mic
With Mic
R445 NC Stuff
R521 NC NC
GAIN1 GAIN2 GAIN
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
PROJECT : MA8
Quanta Computer Inc.
STAC9200 & AMP CONN
Size Custom
Document Number
Rev 2A
Date: Saturday, June 23, 2007
Sheet 23 of 44

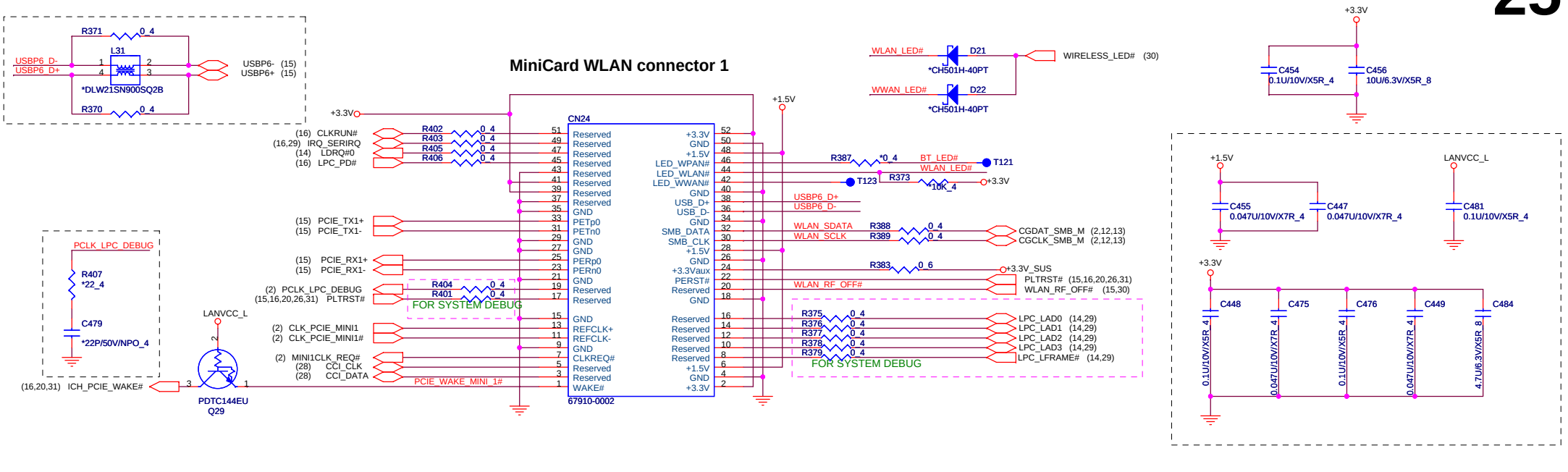
EC A-05

For MDC Module



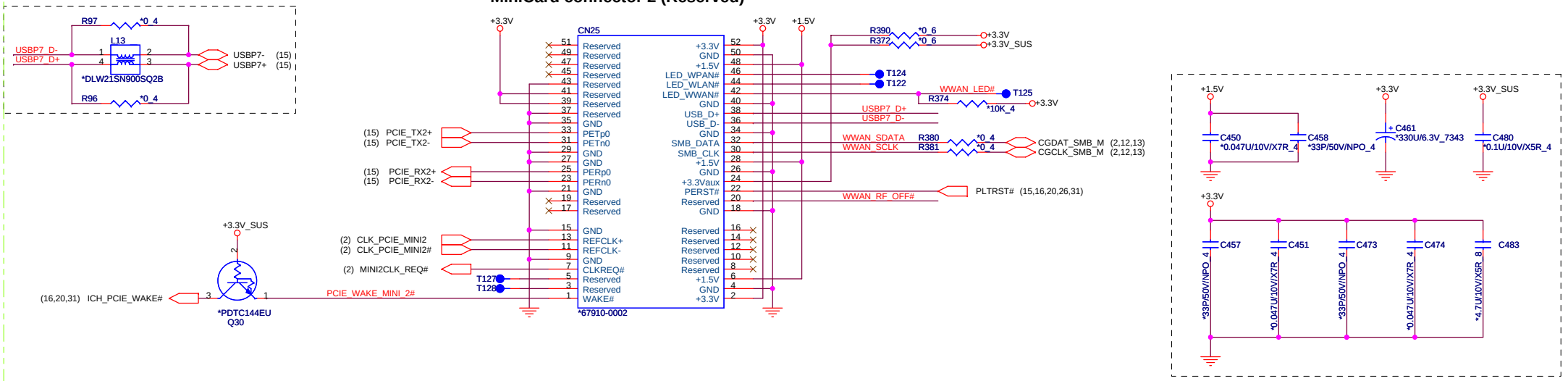
PROJECT : MA8		
Quanta Computer Inc.		
Size: A3	Document Number: MODEM(MDC)	Rev: 2A
Date: Saturday, June 23, 2007	Sheet 24 of 44	

MiniCard WLAN connector 1



EC A-09

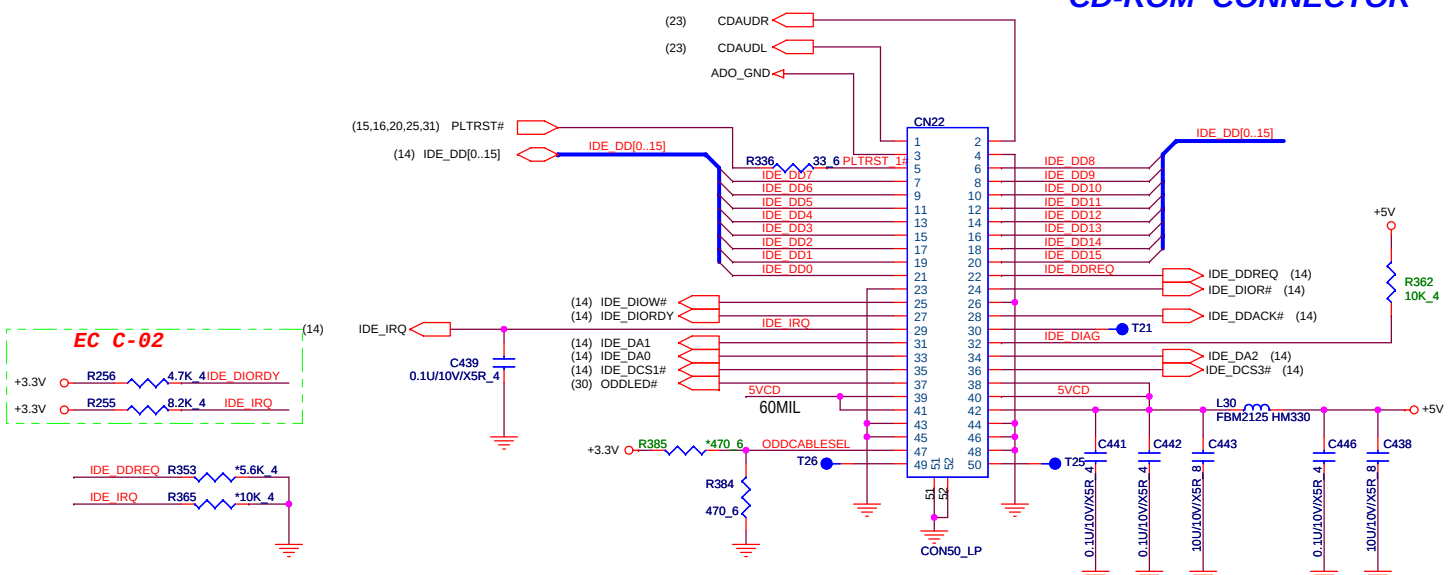
MiniCard connector 2 (Reserved)



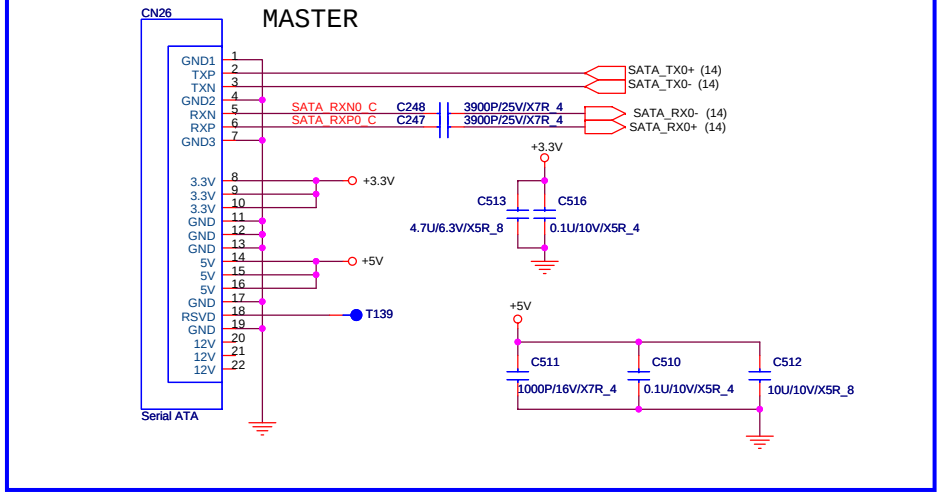
PROJECT : MA8		
Quanta Computer Inc.		
Size: A3	Document Number: MiniCard connector	Rev: 2A
Date: Saturday, June 23, 2007	Sheet 25 of 44	

For fix ODD

CD-ROM CONNECTOR



SATA CONNECTOR



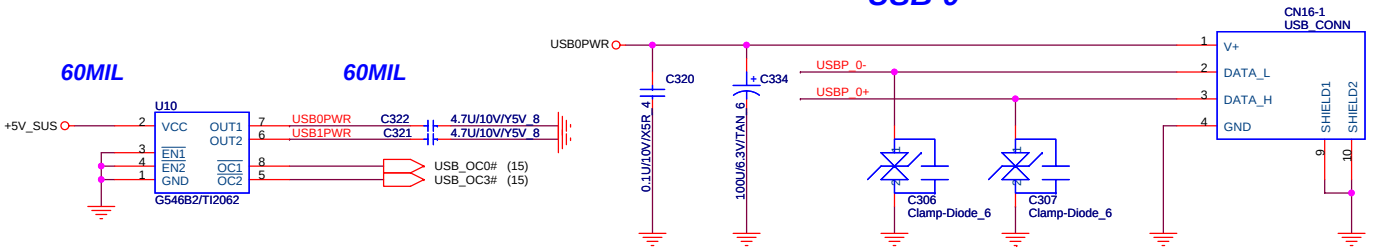
PROJECT : MA8

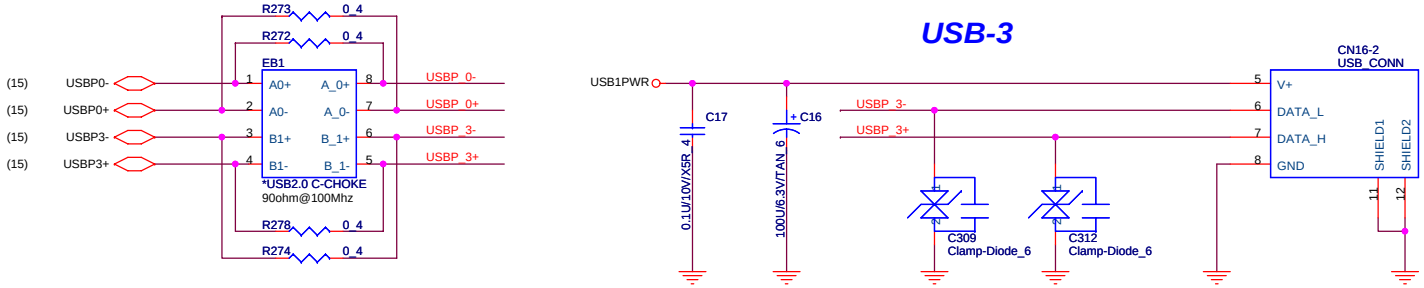
Quanta Computer Inc.

Size	Document Number	Rev
A3	SATA HDD,ODD,USB	1A

Date: Saturday, June 23, 2007 Sheet 26 of 44

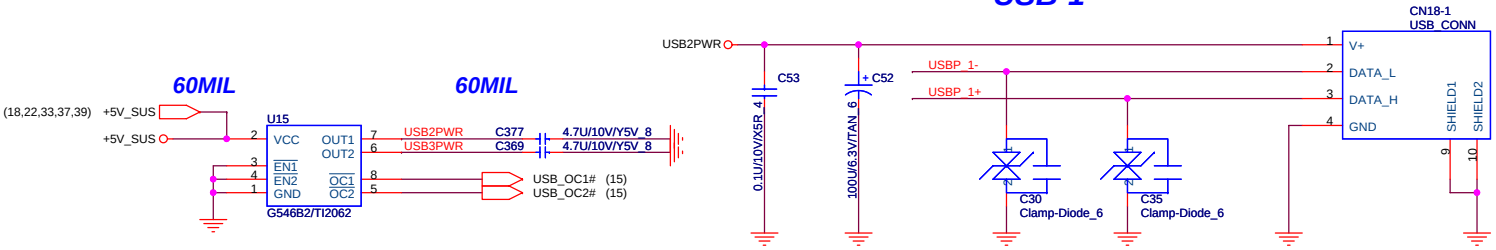
USB-0

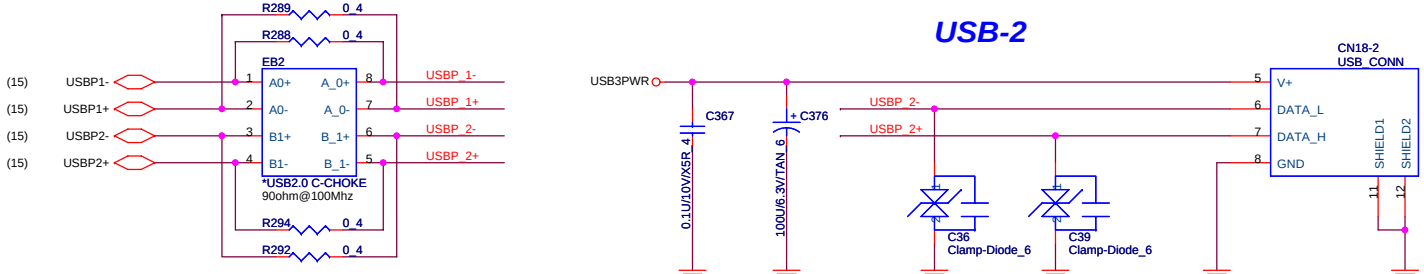




USB-3

USB-1





USB-2

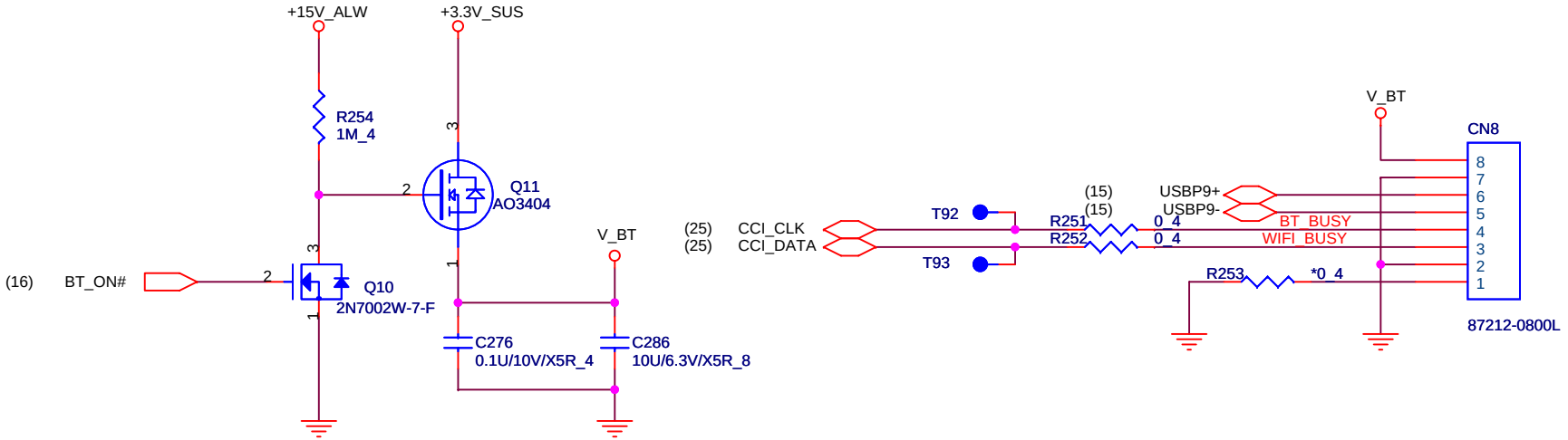
PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A3	USB PORT	1A

Date: Saturday, June 23, 2007 Sheet 27 of 44

BLUETOOTH CONNECTOR



PROJECT : MA8		
Quanta Computer Inc.		
Size: A4	Document Number: BLUETOOTH	Rev: 1A
Date: Saturday, June 23, 2007	Sheet 28 of 44	

IT8512

(For PLL Power)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

RF ON/OFF SWITCH(reserved)

8Mbit (1M Byte), SPI

Layout Note:
Place R119,R135,R128 within 500 mils from SPI Flash.

Please reserve this connector
for serial debug port & KBS download usage.

Place close to EC,

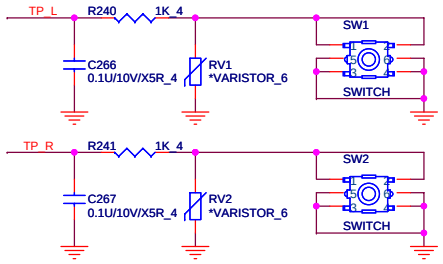
EC B-16

PROJECT : MA8
Quanta Computer Inc.

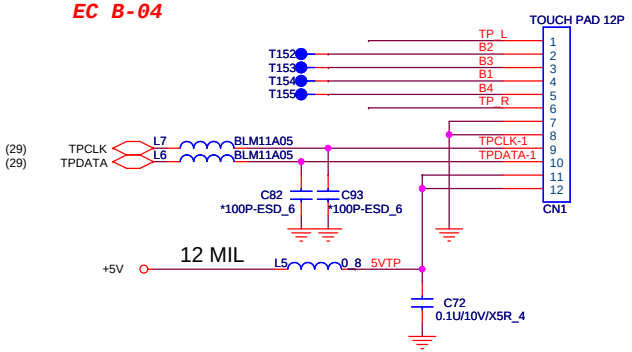
Size	Document Number	Rev
Custom	KBC-IT8512	1A

Date: Saturday, June 23, 2007 Sheet 29 of 44

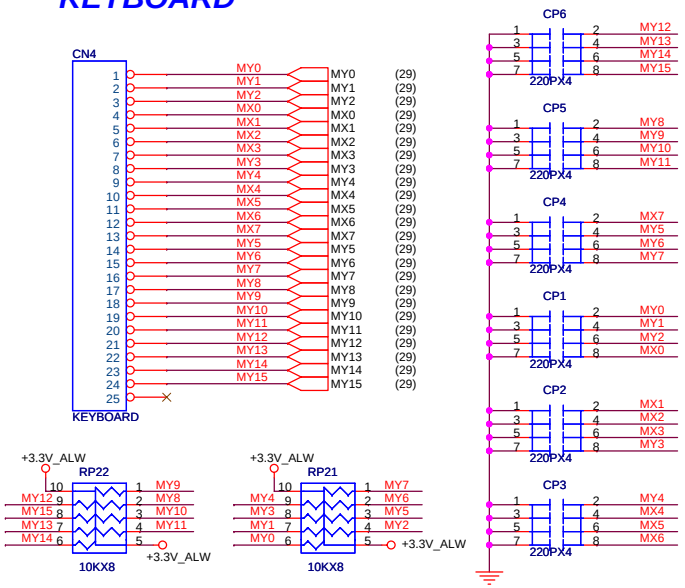
TOUCHPAD SWITCH CONN



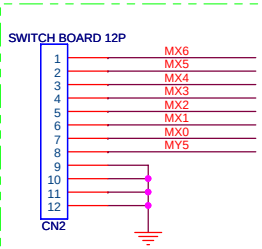
EC A-16
EC B-04



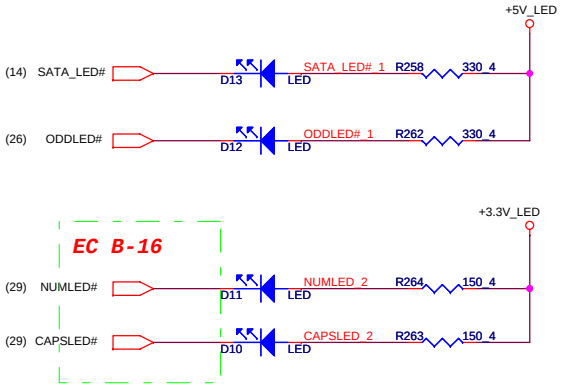
KEYBOARD



SWITCH BOARD

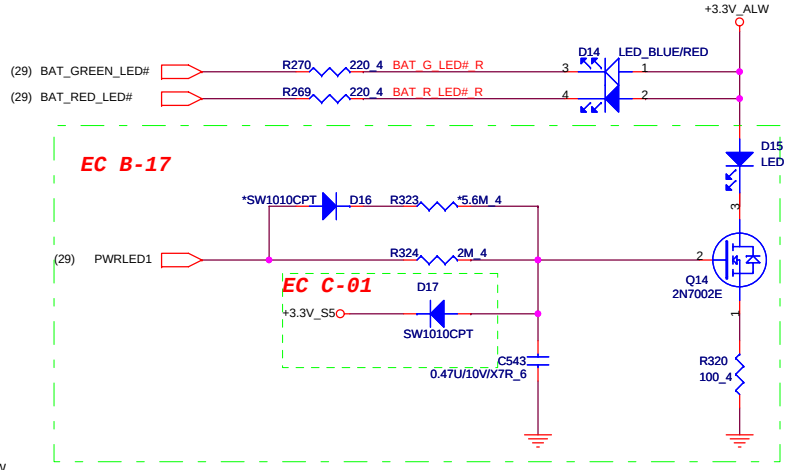


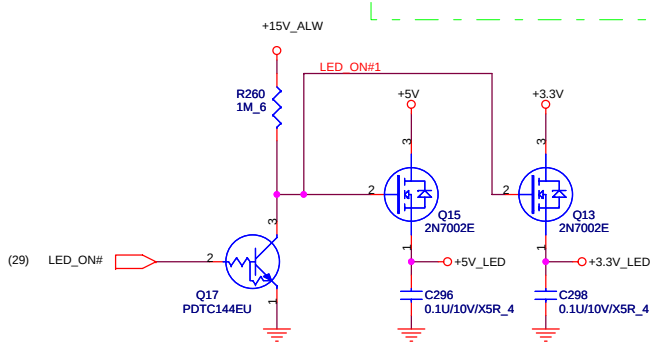
EC A-18



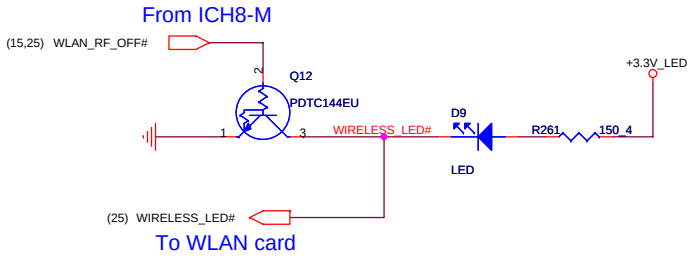
EC B-16

LED INDICATOR





WIRELESS LED

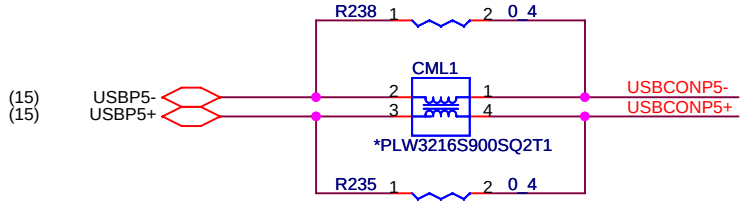


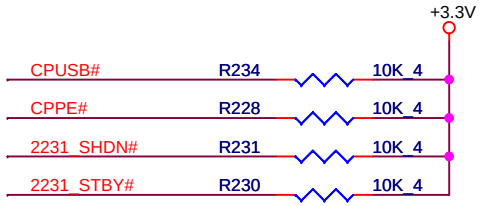
PROJECT : MA8
Quanta Computer Inc.

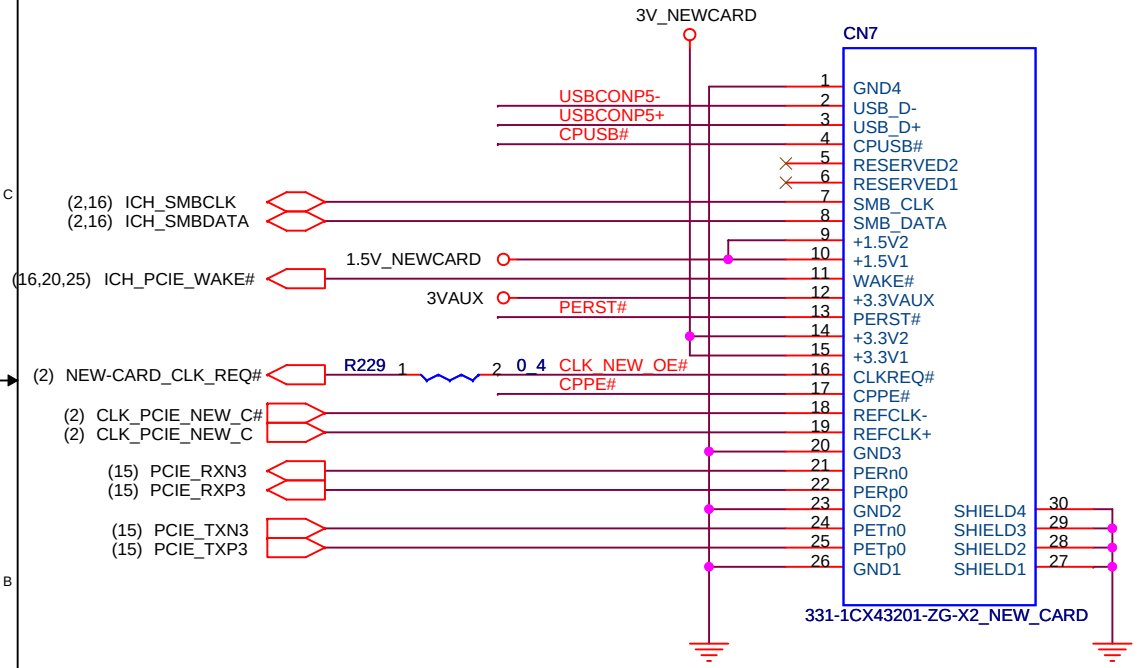
Size	Document Number	Rev
A3	TP/KB/LED/SW. BOARD	2A

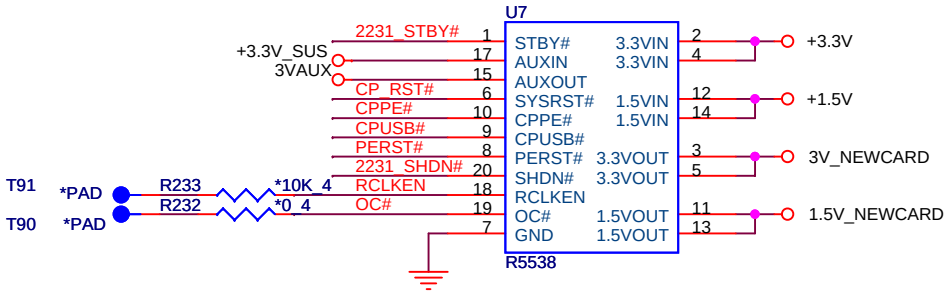
Date: Saturday, June 23, 2007 Sheet 30 of 44

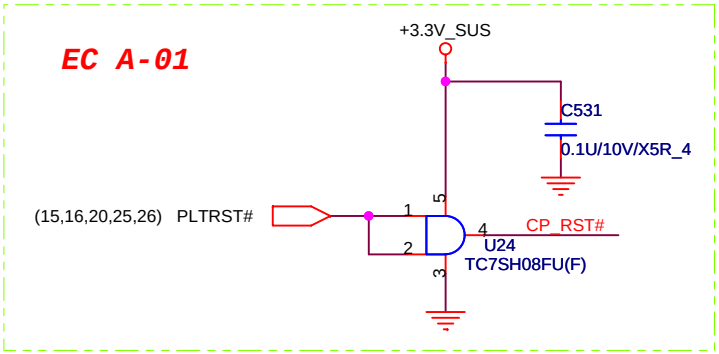
NEWCARD

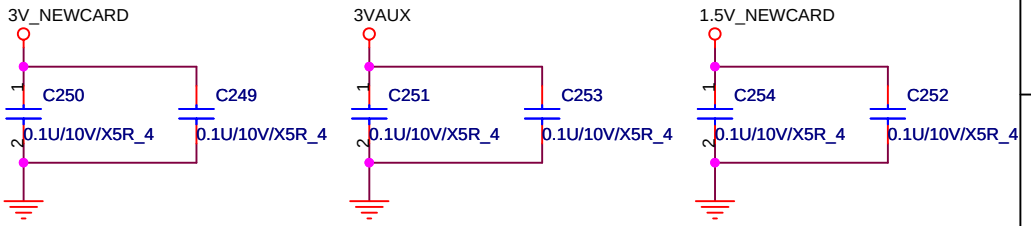












PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A4	NEW CARD	2A
Date: Saturday, June 23, 2007	Sheet 31 of 44	

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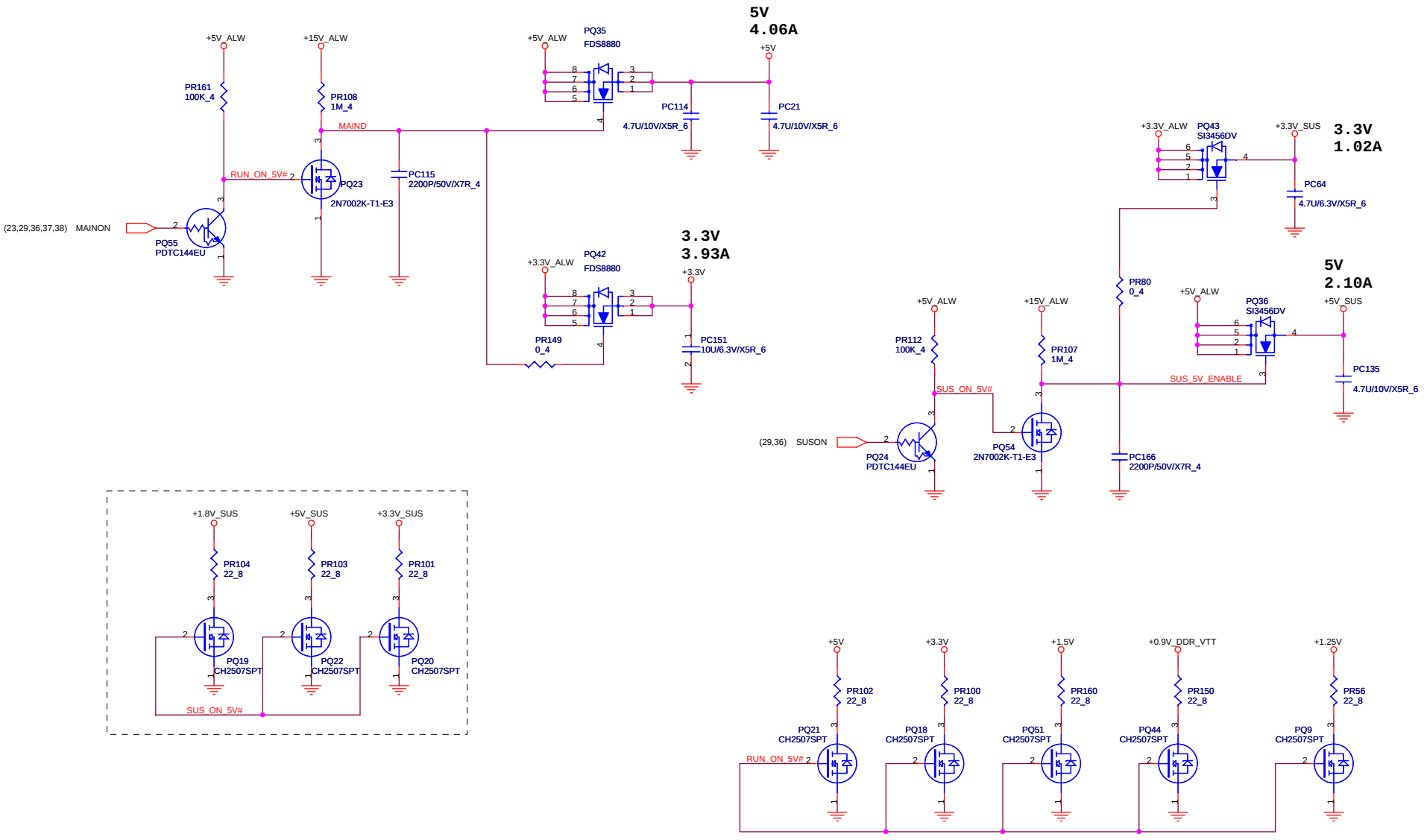
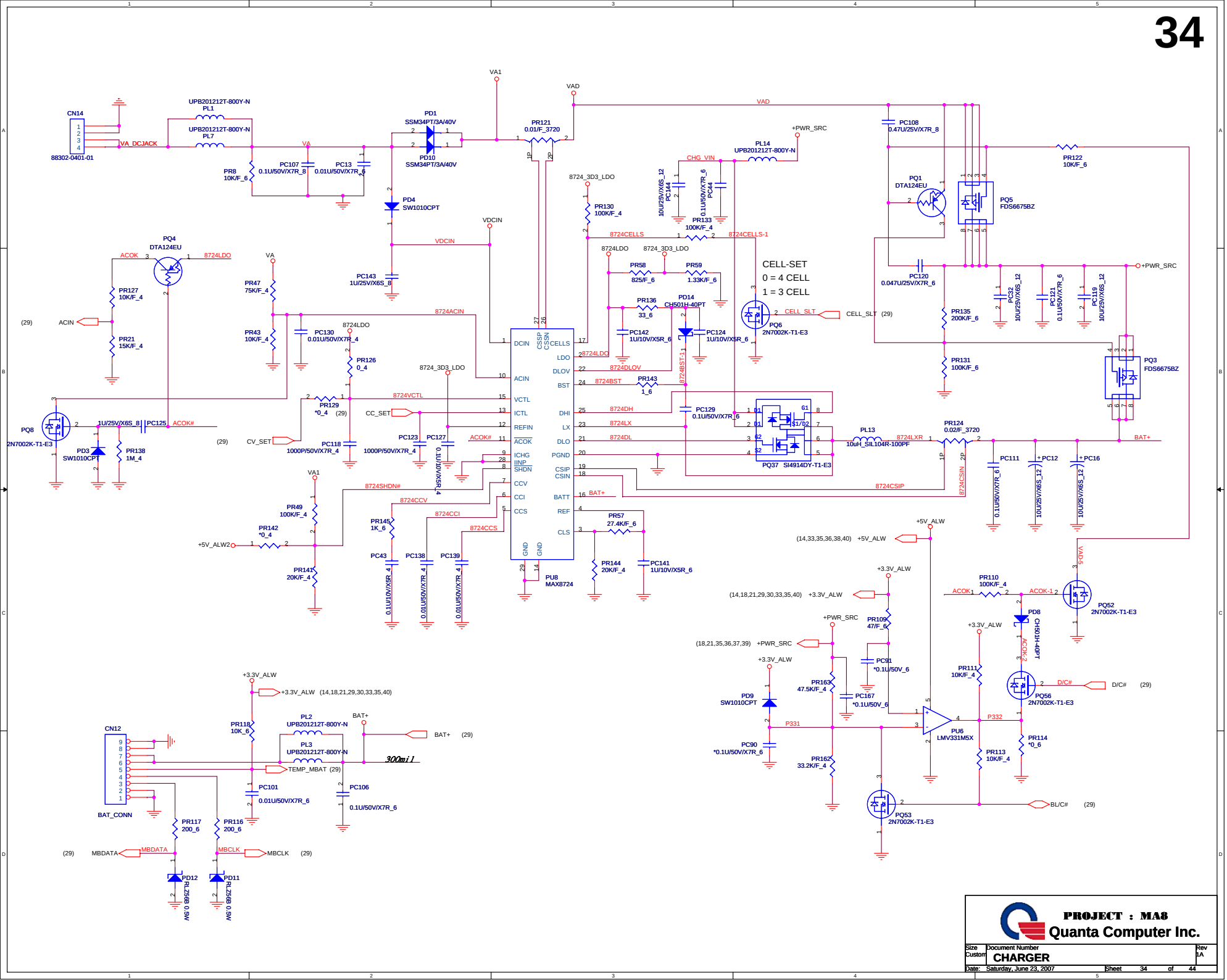


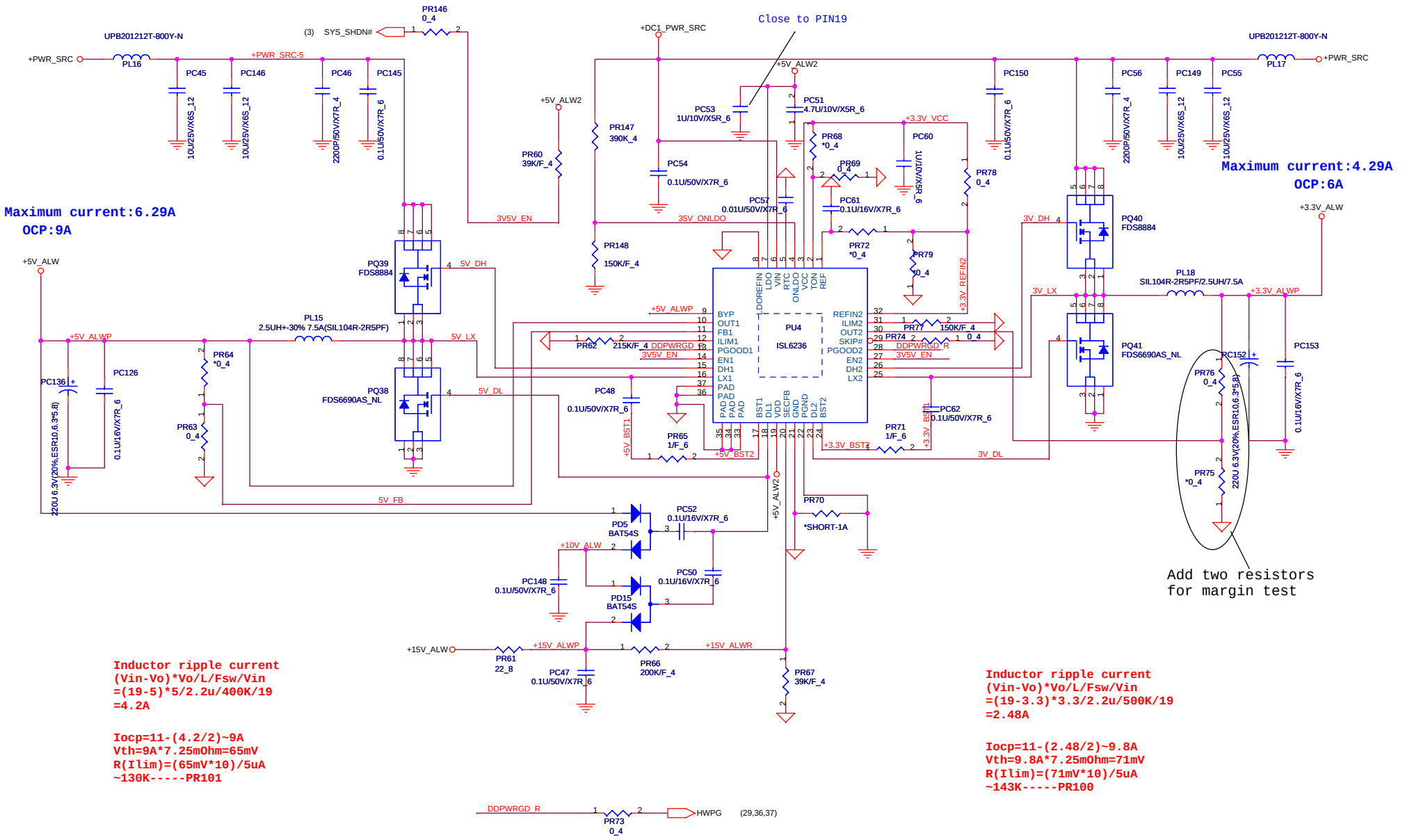
PROJECT : MA8

Quanta Computer Inc.

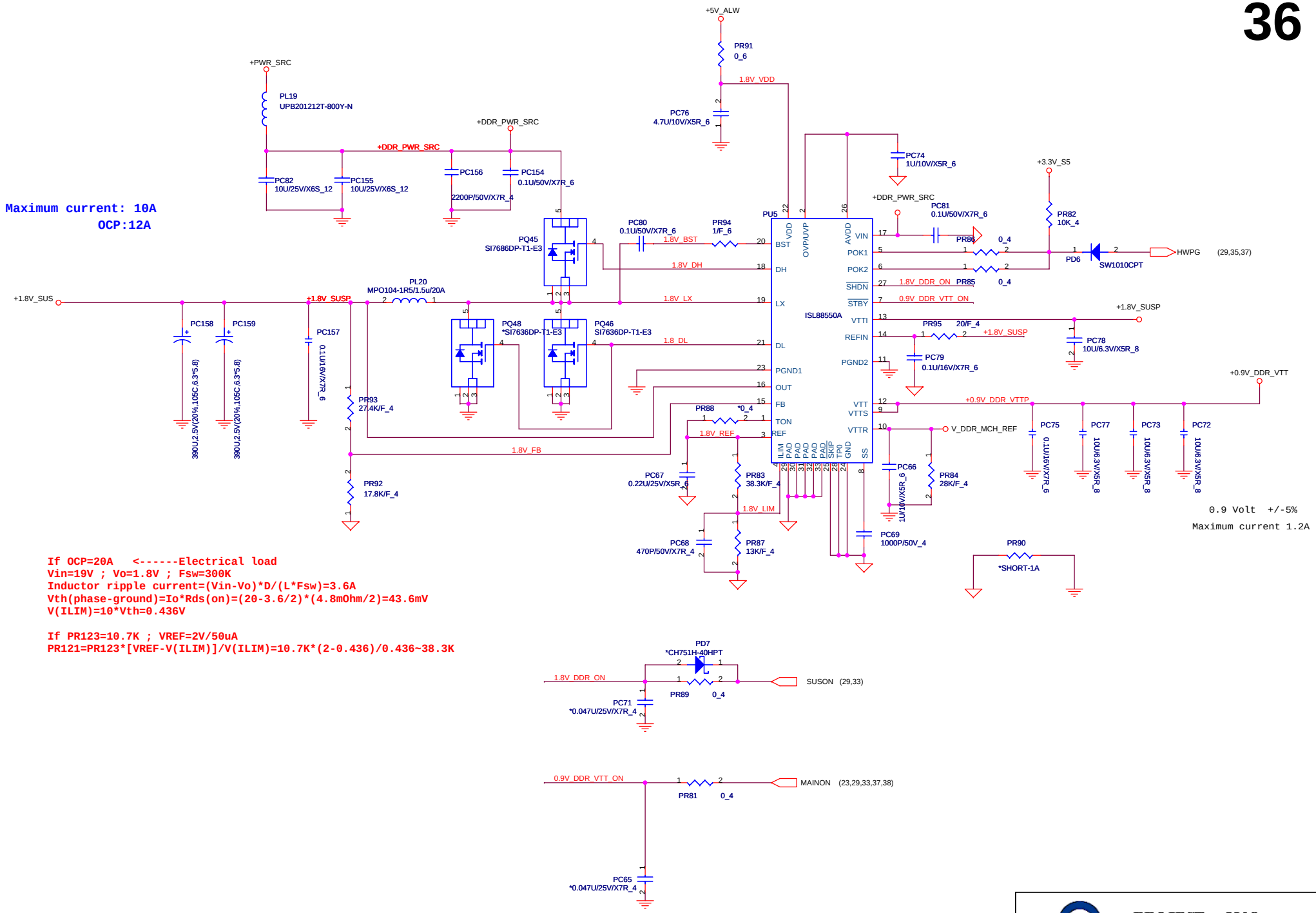
Size	Document Number	Rev
Custom	RUN POWER SW & DISCHARGE	1A

Date: Saturday, June 23, 2007 Sheet 33 of 44


CELL-SET
0 = 4 CELL
1 = 3 CELL
PROJECT : MA8
Quanta Computer Inc.
CHARGER
Saturday, June 23, 2007
Sheet 34 of 44



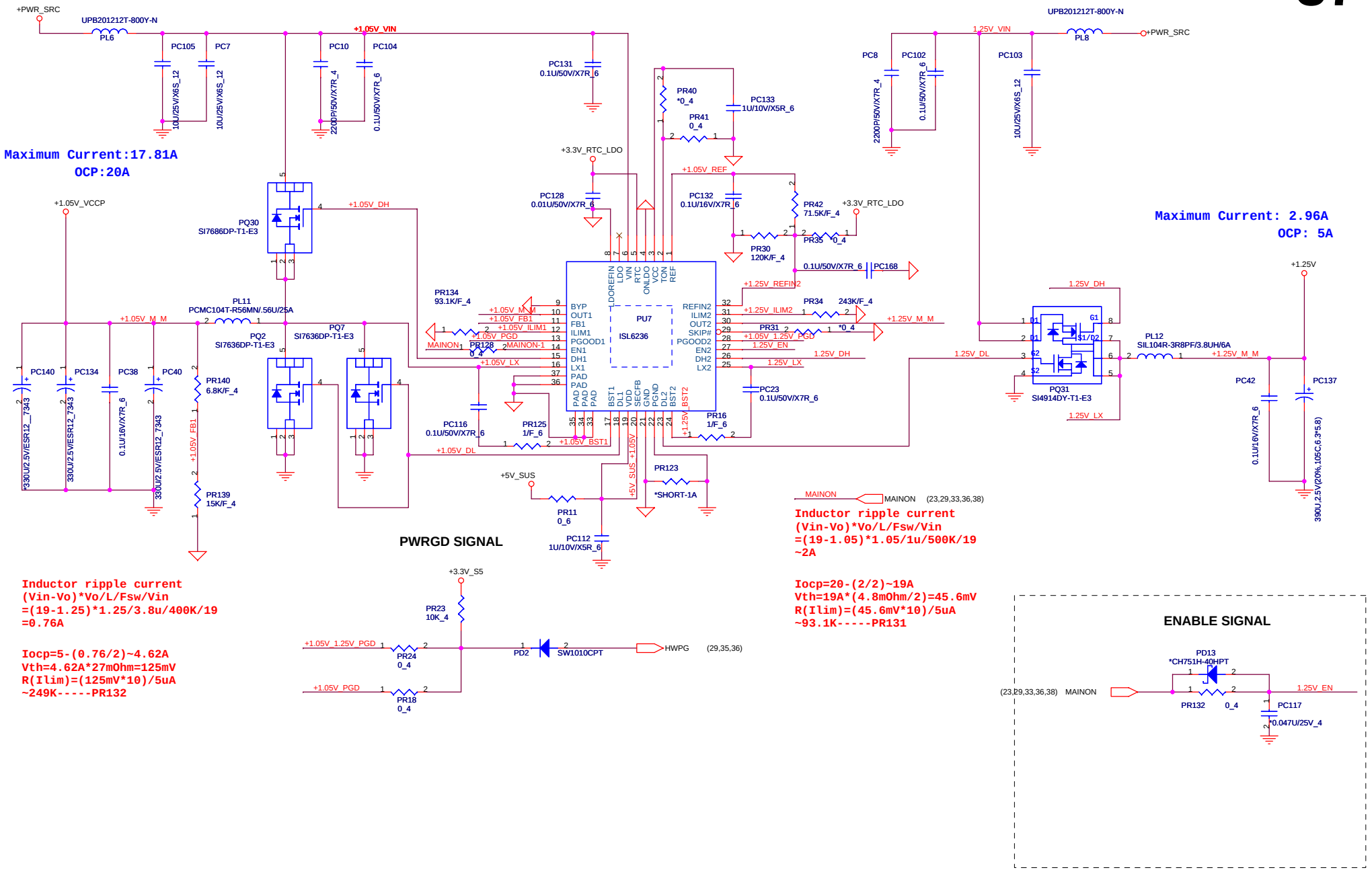
PROJECT : MA8			
Quanta Computer Inc.			
Size: Custom	Document Number: D/D POWER		Rev: 1A
Date: Saturday, June 23, 2007		Sheet 35 of 44	



PROJECT : MA8

Quanta Computer Inc.

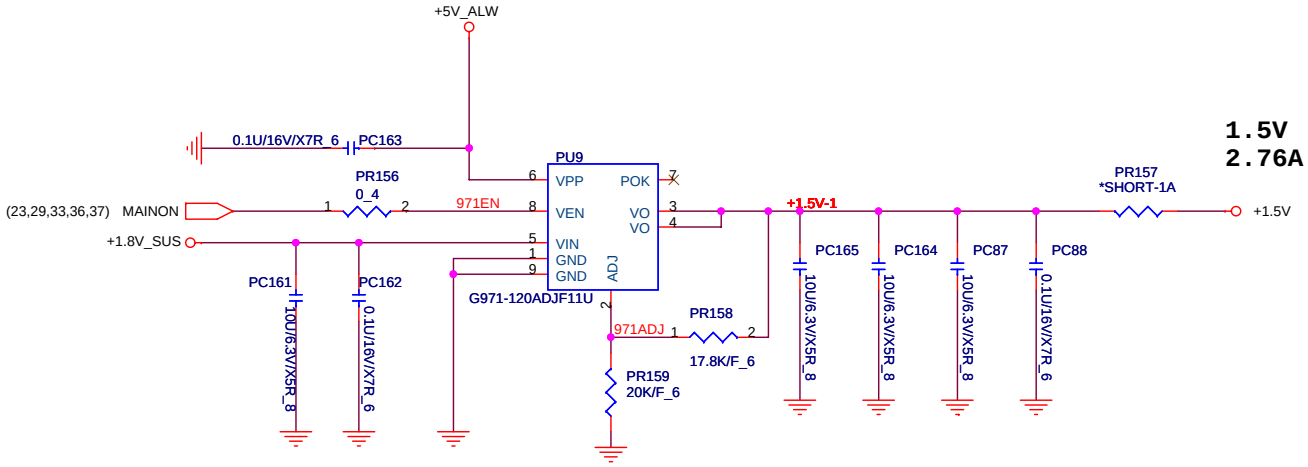
Size	Document Number	Rev
Custom	+1.8V_SUS & +0.9V_DDR_VTT	1A
Date: Saturday, June 23, 2007	Sheet 36 of 44	



PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.25V & +1.05VCCP	1A
Date: Saturday, June 23, 2007	Sheet 37 of 44	

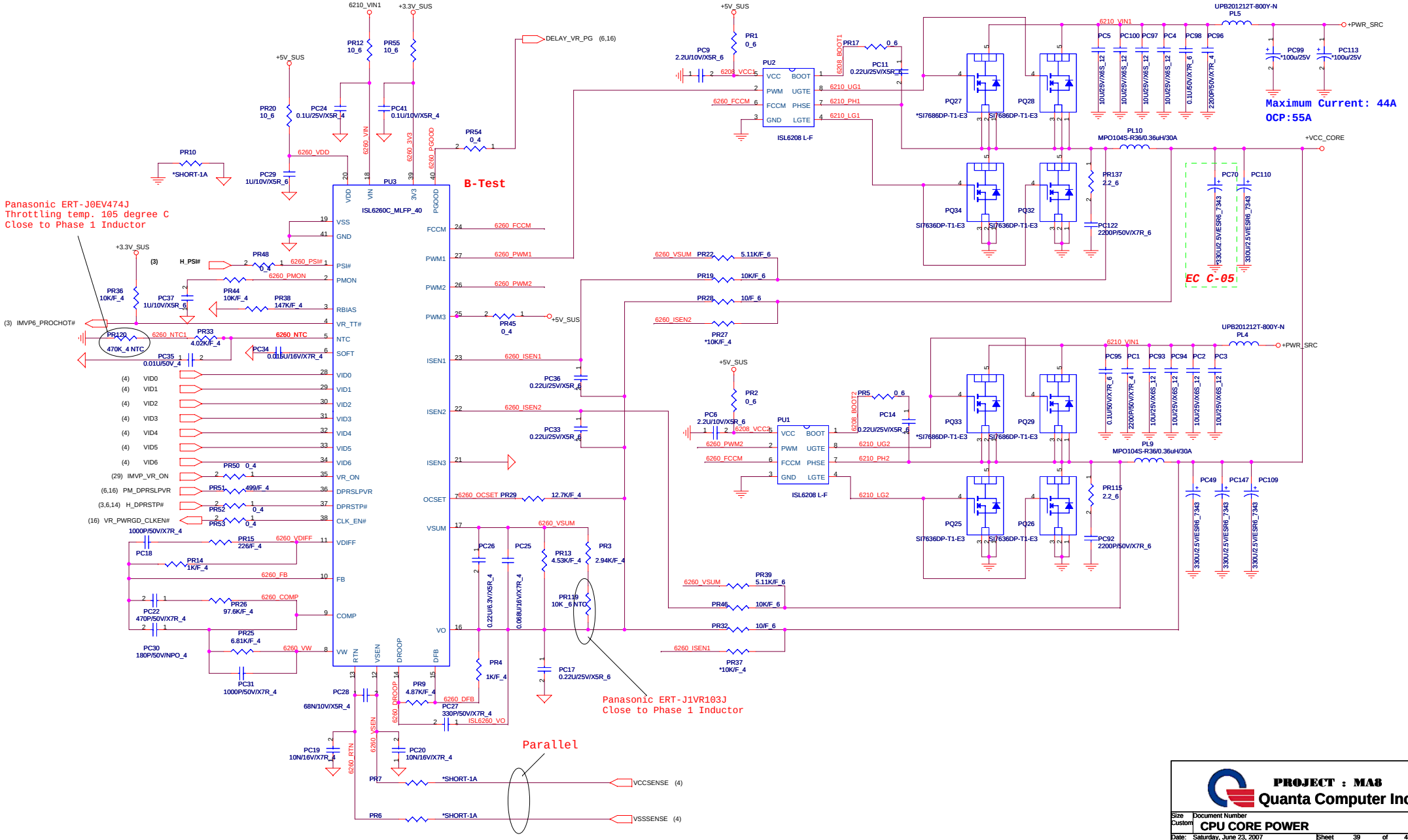


1.5V
2.76A

Vout =0.8(1+R1/R2) = 0.8(1+17.8K/20K) = 1.512V

PROJECT : MA8
Quanta Computer Inc.

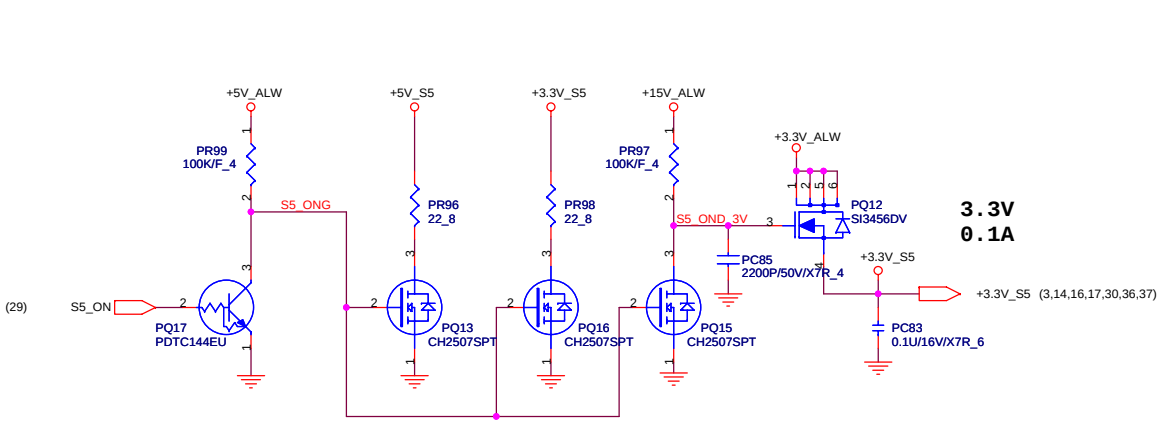
Size	Document Number	Rev
Custom	+1.5V	1A
Date: Saturday, June 23, 2007	Sheet 38 of 44	

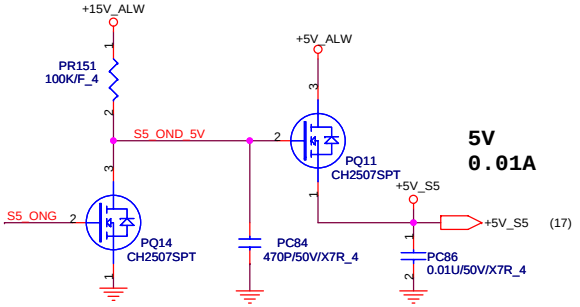


PROJECT : MA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU CORE POWER	1A

Date: Saturday, June 23, 2007 Sheet 39 of 44





PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
B	+3V_S5/+5V_S5	1A

Date: Saturday, June 23, 2007 Sheet 40 of 44

EC A-23 EC B-11

CPU SCREW HOLE

HOLE6 H-C236D154P2
HOLE7 *H-C236D154P2
HOLE8 *H-C236D154P2
HOLE9 *H-C236D154P2
HOLE17 H-C236D154P2

EC A-08

MINI PCI-E SCREW HOLE 2

HOLE12 *H-C236D142P2
HOLE13 *H-C236D142P2

MINI PCI-E SCREW HOLE 1

HOLE10 H-C236D142P2
HOLE11 H-C236D142P2

EC A-06

MDC SCREW HOLE

HOLE28 h-c146d146n
HOLE29 h-c146d146n

HOLE15 *H-C236D118P2
HOLE16 *H-C236D118P2
HOLE2 *H-S354D118P2
HOLE4 *H-TC236BC354D118P2
HOLE19 *H-R394X354D118P2
HOLE26 *H-R394X354D118P2

HOLE27 *H-C236D118P2
HOLE25 *H-R346X374D118P2
HOLE24 *H-TC314BR394X433P2
HOLE14 *H-C276D276N
HOLE20 *H-C118D118N
HOLE3 *H-TS335X315BC236D118p2
HOLE31 *H-C118D118N

EC A-15

HOLE30 *H-c236d118p2

EC C-04

HOLE32 *H-C315D118P2

HOLE21 *H-TC236BR329X335D118P2
HOLE23 *H-C315D118P2
HOLE5 *H-C315D118P2
HOLE1 *H-C315D118P2
HOLE18 *H-C315D118P2

HOLE22 *H-C236D118P2

MODEM

PAD17 FDBF1006
PAD18 FDBF1006
PAD19 FDBF1006
PAD20 *FDBF1006

PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
A3	EMI PAD & Hole	2A

Date: Wednesday, June 13, 2007 Sheet 41 of 44

A-test to B-test EC list

MA8 Schematic EC Tracking Record A (for A --> B) JAN. 22, 2007

EC #/Page/Description/Part Affected

EC A-01 /31/ Add C531 & U24 to prevent leakage of current.

EC A-02 /30/ Remove CN2,L27,R322,R323 to eliminate Finger Print function according to latest hardware spec. from customer.

EC A-03 /18/ Remove resistor array chip RN2-RN9(0 Ohm) for LVDS

EC A-04 /15/ Add pull high resistor R322(10K_4) to OC#7

EC A-05 /24/ Change MODEM from MOM(modem on motherboard) to MDC(modem daughter card).So replace whole page of SILICON SI3054+SI3080(MODEM) with MDC board to board Conn. schematic. R494,R495,C532,C533,CN27 were added in this schematic.

EC A-06 /41/ Add MDC SCREW HOLE==>HOLE28,HOLE29.

EC A-07 /23/ Remove R464 & depop R459 to normalize VOLMUTE# function

EC A-08 /41/ Depop 2 MINI PCI-E SCREW HOLE ==>HOLE12,HOLE13.

EC A-09 /25&15/ Depop MiniCard connector 2 and related parts as following list CN25,R96,R97,Q30,R380,R381,R390,C451,C457,C473,C474,C483,C450,C458,C480,D23,C185,C186

EC A-10 /18/ Remove R76 & R350 which connect to INT_LVDS_EDIDDATA & INT_LVDS_EDIDCLK respectively.

EC A-11 /18/ Remove C432, add R504,R464,R496,R497 for camera function

EC A-12 /14/ Change RTC from rechargeable to NON rechargeable.So, disable charging circuit by depop Q7,R186,R187,R205,R206 & replace CN5(Wire type) by BT1(Socket type).

EC A-13 /09/ Replace L9 with R498 & add C534(CRT signal quality)

EC A-14 /23/ Change the value of C301 & C302 from 1U/10V/X5R_6 to 2.2U/6.3V/X5R_6 for internal MIC function. Add internal MIC shcematic including following parts,R499,C536,R501,C535,C538,R503,CN28,R519,R520,C537,U25.

EC A-15 /41/ Add HOLE30 for keyboard

EC A-16 /30/ Change touchpad from TM61~G307 to TM61~G372 for cost down reason. But reserve schematic of G307 ,so add R505-R518 for the convenience of making option between G307 & G372.

EC A-17 /20/ Remove D16-D18,C2,C5 and add R194 for cost down reason.

EC A-18 /30/ Add CN2 for switch board.

EC A-19 /09/ Connect Pin AH50 & AH51 of U17 to +VCC_PEG, depop C542,C468,L35

EC A-20 /20/ Change U1 from NS892405 to NS892404 for layout

EC A-21 /20/ Add C600 for better signal intergrity due to PCIE_TX6-/GLAN_TX- & PCIE_TX6+/GLAN_TX+ change refrence plane on MB.

EC A-22 /20/ Delete CHASSIS_GND which connect with RJ45 for ESD. Remove C1,C11,C303,C305

EC A-23 /41/ Change Hole6,Hole7,Hole8,Hole9 to non-PTH hole to improve ESD.

EC A-24 /19/ Change L10,L11,L12 to 0 Ohm, depop C161,C162,C163,C169,C170,C171 to improve CRT performance.

B-test to C-test EC list

MA8 Schematic EC Tracking Record B (for B --> C) MAR. 20, 2007

EC #/Page/Description/Part Affected

EC B-01 /03/ Reverse pin define of CN17 for layout.

EC B-02 /23/ Add R521(1K ohm) to pull down MIC_DET for no MIC sku

EC B-03 /22/ Change the Y1, 12MHz (foot print: XTAL-3_2X2_5-2_3X1_9) to the big size (Y5: FSX-7B) for cost down reason.

EC B-04 /30/ Remove R505-R518 which provide the option between TM61~G307 & TM61~G372 on B-test. C-test will use only TM61~G372.

EC B-05 /03/ Stuff ITP resistor R7,R8,R12,R13,R29.

EC B-06 /06/ R61,R62,R63 change to 0 Ohm for cost down.

EC B-07 /22/ Change R737-R756 from 0ohm to 33ohm.

EC B-08 /20/ Connect pin13-16 of CN13 to GND to improve ESD.

EC B-09 /19/ Change L10,L11,L12 to BK1608HS600-T, pop up C161,C162,C163,C169,C170,C171 to improve EMI.

EC B-10 /18/ Add C432(1000p) to +5V at pin32 of CN3.

EC B-11 /41/ Connect Hole6-9 to GND to improve ESD.

EC B-12 /23/ C282,C283,C284,C285 change from capacitor to varistor.

EC B-13 /03/ Add varistor C539,C540,C541 in parallel to ITP_DBRESET#,H_RESET# & ITP_TRST# respectively.

EC B-14 /23/ Add R316 & R317 both 0ohm resistor between analog GND plane and digital GND.

EC B-15 /02/ Remove R104(GCLK_SEL) due to MA8 don't support external VGA

EC B-16 /29/30/ Remove Q14,Q16 and change NUMLED#/CAPLED# to low active for cost down reason.

EC B-17 /30/ Change PWRLED schematic for cost down reason.

C-test to FAI EC list

MA8 Schematic EC Tracking Record C (for C --> FAI) June. 01, 2007

EC #/Page/Description/Part Affected

EC C-01 /30/ Add D17 to discharge C543 when power off.So, D15 will not light up at the beginning of power turn on.

EC C-02 /26/ Add pull high R256(4.7K) & R255(8.2K) separately to IDE_IRQ & IDE_DIORDY according to intel DSGL.

EC C-03 /23/ Add C546,C547,C548 for ESD solution.

EC C-04 /41/ Add Hole32.

EC C-05 /39/ Add back PC70 for +VCC_CORE

PROJECT : MA8

Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC list	3A

Date: Tuesday, June 12, 2007 Sheet 44 of 44