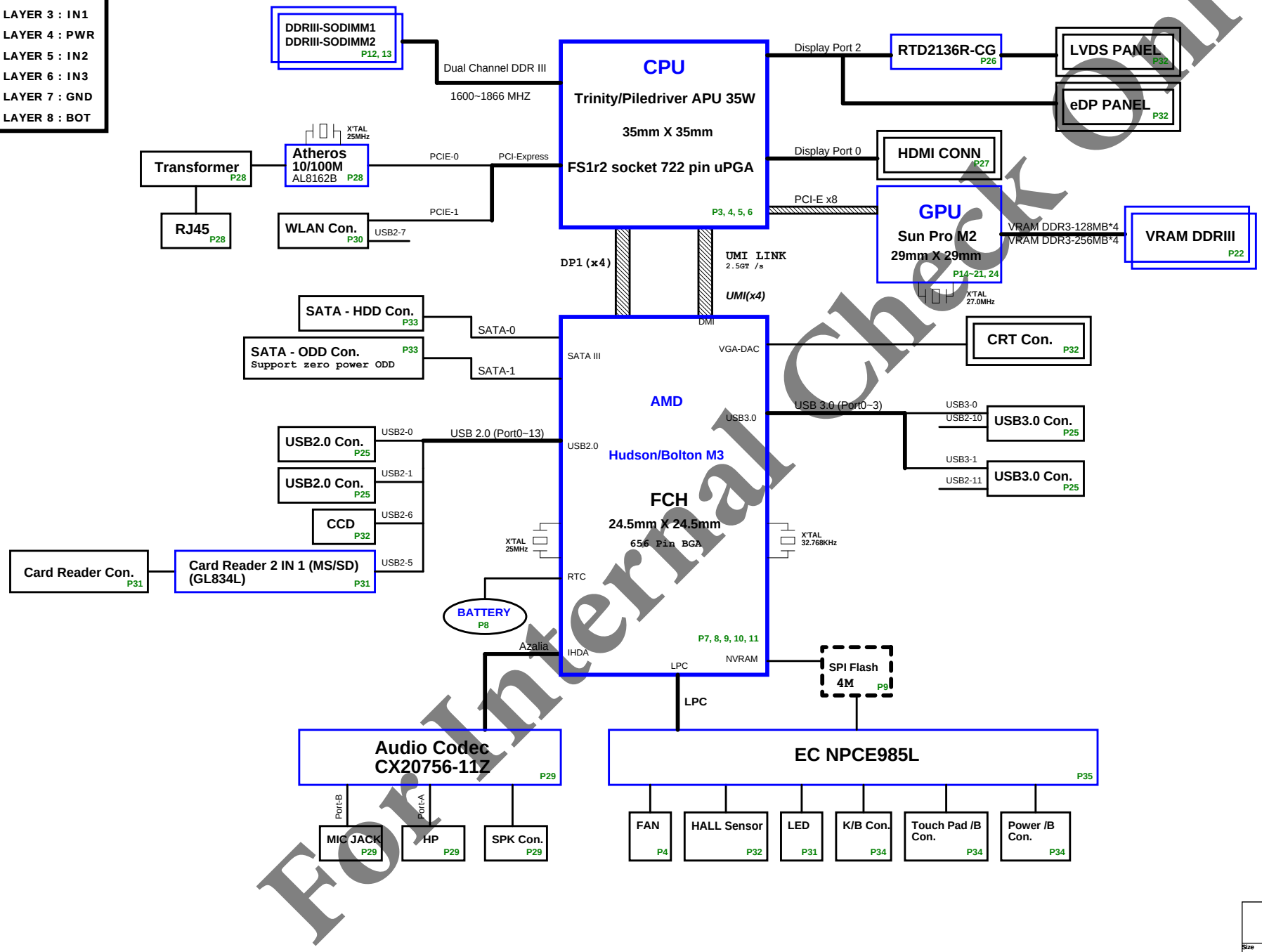
BD8 Richland/Comal Block Diagram

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : PWR
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



POWER SYSTEM

ISL88731CHRTZ-T
TPS51123A
TPS51216RUKR
TPS51211DSCR
TPS51211DSCR
OSL6277
G9661-25ADJF12U
ISL95870AHRUZ-L

- CHARGER P36
- +15V, +3VPCU, +3V_S5, +3V, +5VPCU, +5V_S5, +5V — P37
- +SMDDR_VTERM, +SMDDR_VREF, +1.5VSUS, +1.5V_S5, +1.5V — P38
- +1.2V_VDDPR — P39
- +1.1V_DUAL, +1.1V — P40
- +VDD_CORE, +VDDNB_CORE — P41
- +2.5V_VDDA DISCHARGE — P42
- +VGPU_CORE, +3V_GPU, +1.8V_GPU, +1.5V_GPU, +1V_GPU — P43,P44

Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	Block Diagram	1A

Date: Saturday, January 26, 2013 Sheet 1 of 47

Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
+VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P	S0
+1.5VSUS	+1.5V	S5_ON	S0~S3
+1.5V	+1.5V	MAIN_ON	S0
+1.2V_VDDPR	+1.2V	VDDA_PWRGD	S0
+1.1V_DUAL	+1.1V	+1.1V_DUAL_EN	S0~S5
+1.1V	+1.1V	MAIN_ON	S0
+VDD_CORE	~	VDDA_PWRGD	S0
+VDDNB_CORE	~	VDDA_PWRGD	S0
+VGPU_CORE		PX_MODE	S0
+1.8V_GPU	+1.8V	PE_GPIO1	S0
+1V_GPU	+1V	DGPU_PWREN	S0
+3V_GPU	+3.3V	PE_GPIO1	S0
+1.5V_GPU	+1.5V	PX_MODE_D	S0
+2.5V_VDDA	+2.5V	MAIN_ON	S0

GND PLANE	PAGE
GND_SIGNAL	32
8769GND	36
	28
GND	ALL
ADOGND	29

ITEM	Value Code	FUNCTIONS
1	CEC@	CEC
2	Debug@	HDT+ Debug
3	EV@	DISCRETE
4	IV@	UMA
5	U3@	Internal USB 3.0
6	1G4@	VRAM 1Gb*4
7	1G8@	VRAM 1Gb*8
8	2G@	VRAM 2Gb
9	AMD@	AMD VRAM
10	DIS@	DISCRETE
11	M2@	M2 FCH
12	M3@	M3 FCH
13	NMP@	LPC Debug Card
14	PX4@	PX4 Mode
15	PX5@	PX5 Mode
16	Sam@	Samsung VRAM
17	U2@	USB 2.0 (colay W USB 3.0)
18	E@	EMI

Quanta Computer Inc.

PROJECT : Richland

Size	Document Number	Rev
	POWER STAGE & BOI-FUNCTION	1A

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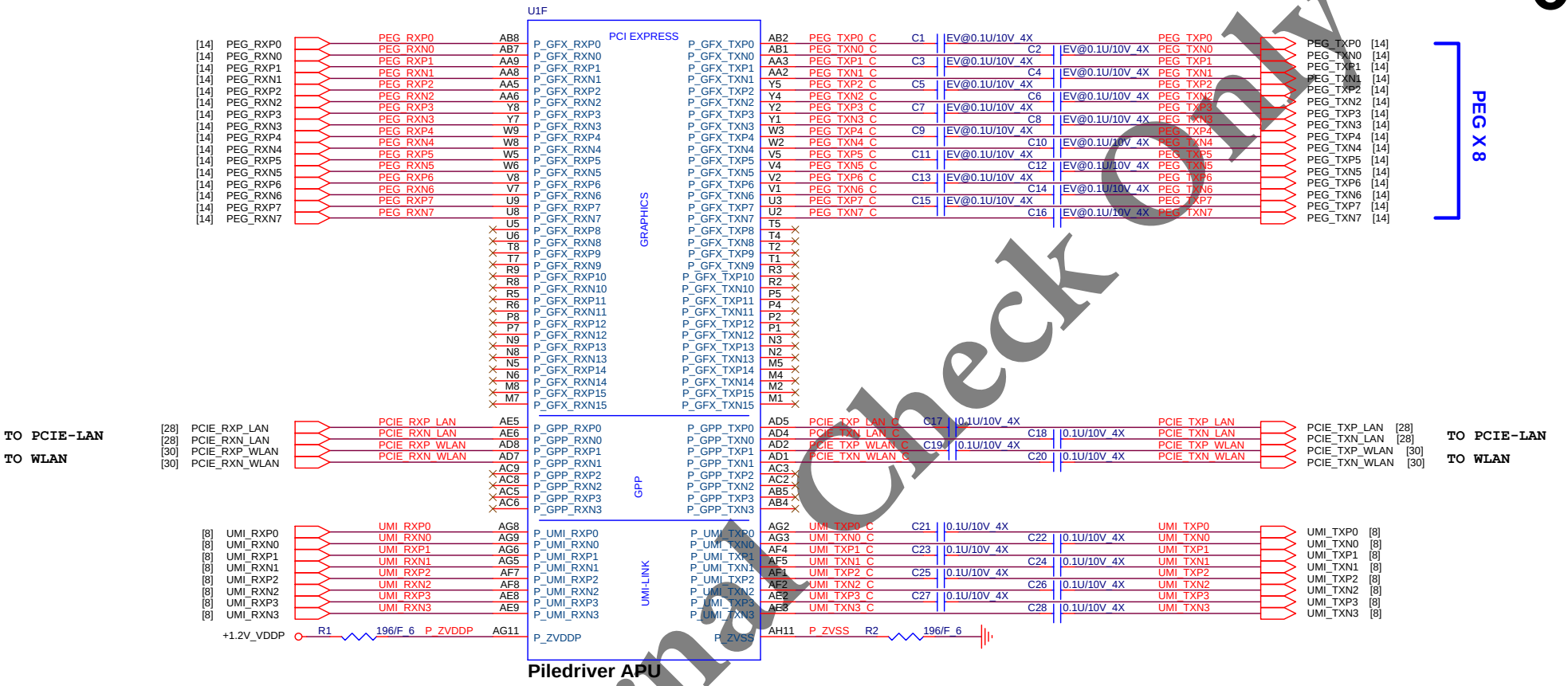
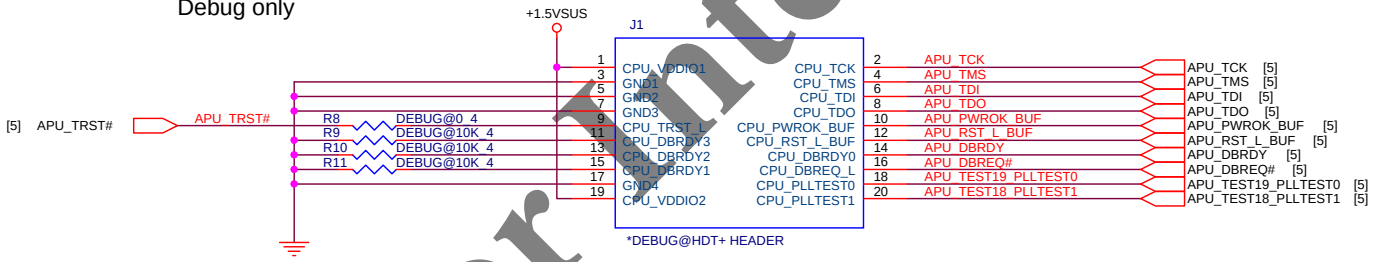


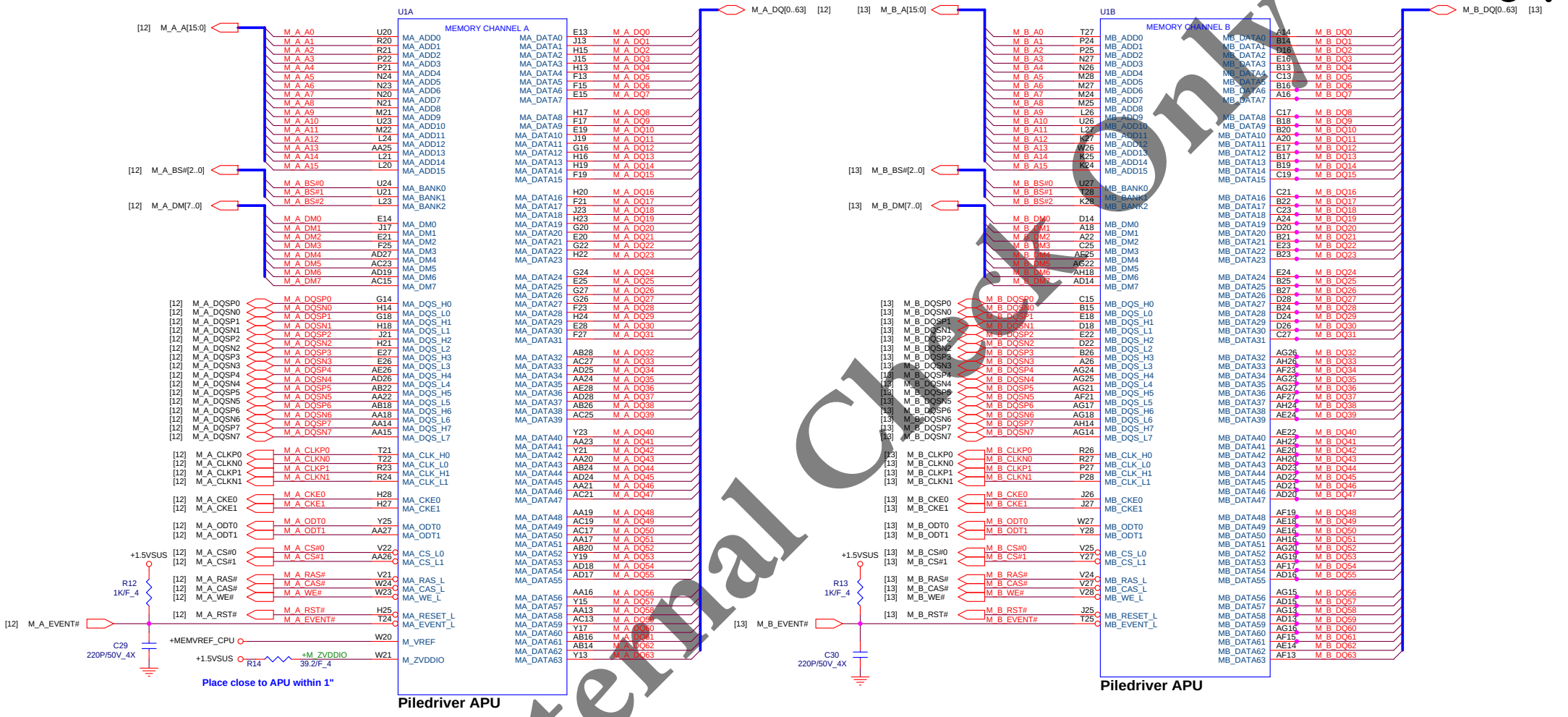
HDT+ Connector

Debug only

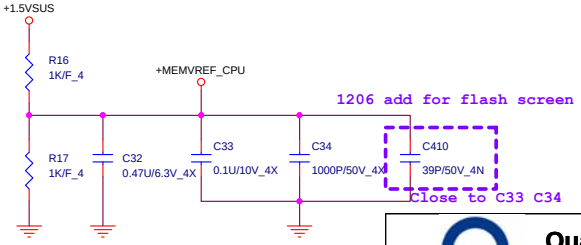


Close by HDT+ Conector

Quanta Computer Inc.		
PROJECT :Richland		
Size	Document Number: APU 1/4(PCIE/UMI/GPP/HDT)	Rev 1A
Date: Saturday, January 26, 2013	Sheet 3 of 47	



FAN Control <THC>



Quanta Computer Inc.		
PROJECT : Richland		
Size	Document Number	Rev
	APU 2/4(DDR3 MEM I/F)	1A
Date: Saturday, January 26, 2013	Sheet 4 of 47	

1017 AMD FAE suggest(DG_1.05)

DP0 HDMI

DP1 Hudson-M3 VGA output

DP2 LVDS

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

Piledriver APU

HDMI

FCH VGA

LVDS

For eDP Panel

FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP

DMAACTIVE_L controls entry and exit from the sleep and power states

SVC	SVD	BOOT VOLTAGE VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID,Remove Rd, Re, Rf, install Rc set VID via SVC & SVD option RES.

APU_PWRGD have pull up 300ohm to +1.5V on page 4

for normal operation open Ra , Rb,Rc

Fan
APU Core Power
EC

Debug only

CPU Thermal sensor / MB Local TEMP

Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 76dgree
Hysteresis is 30C

Quanta Computer Inc.
PROJECT : Richland

Size	Document Number	Rev
	APU 3/4(DISPLAY/MISC)	1A

Date: Saturday, January 26, 2013 Sheet 5 of 47

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

B2A add for ESD

C91 ESD@39P/50V_4N, C77 ESD@39P/50V_4N, C92 22U/6.3V_6X, C93 22U/6.3V_6X, C78 10U/6.3V_6X

1026 change for EOD

+VDDNB_CORE

C98 0.22U/10V_4X, C99 0.22U/10V_4X, C100 180P/50V_4N, C101 180P/50V_4N, C102 180P/50V_4N

+VDDNB_CAP

C103 22U/6.3V_6X, C104 22U/6.3V_6X, C105 180P/50V_4N

+VDD_CORE

U1D

VDD_1 F8, VDD_2 H6, VDD_3 J1, VDD_4 J14, VDD_5 P6, VDD_6 P10, VDD_7 J16, VDD_8 J18, VDD_9 J9, VDD_10 K19, VDD_11 K3, VDD_12 K17, VDD_13 M3, VDD_14 K6, VDD_15 V10, VDD_16 V18, VDD_17 V3, VDD_18 F3, VDD_19 L18, VDD_20 V6, VDD_21 W1, VDD_22 T18, VDD_23 Y14, VDD_24 AA1, VDD_25 AB6, VDD_26 AC1, VDD_27 R1, VDD_28 P3, VDD_29 K10, VDD_30 H3, VDD_31 M19

VDD_33 R11, VDD_34 T10, VDD_35 H8, VDD_36 G1, VDD_37 U11, VDD_38 W11, VDD_39 W13, VDD_40 W15, VDD_41 W17, VDD_42 W19, VDD_43 AB3, VDD_44 AD3, VDD_45 AD6, VDD_46 AE1, VDD_47 L1, VDD_48 Y6, VDD_49 M6, VDD_50 N11, VDD_51 N1, VDD_52 T3, VDD_53 T6, VDD_54 U19, VDD_55 U1, VDD_56 Y16, VDD_57 Y18, VDD_58 Y3, VDD_59 D4, VDD_60 F4, VDD_61 AF6, VDD_62 AF3, VDD_63 L11

36A
Maximum IDDspike 50A

C79 22U/6.3V_6X, C74 22U/6.3V_6X, C75 22U/6.3V_6X, C76 22U/6.3V_6X, C80 22U/6.3V_6X, C88 ESD@39P/50V_4N, C81 ESD@39P/50V_4N

C82 22U/6.3V_6X, C83 22U/6.3V_6X, C89 22U/6.3V_6X, C84 22U/6.3V_6X, C90 22U/6.3V_6X

C94 0.22U/10V_4X, C95 0.22U/10V_4X, C96 180P/50V_4N, C85 180P/50V_4N, C86 0.01U/25V_4X, C97 0.01U/25V_4X, C87 0.01U/25V_4X

25A
Maximum IDDNBspike 33A

+VDDNB_CORE

C8, D10 VDDNB_1, B8 VDDNB_2, B12 VDDNB_3, C9 VDDNB_4, A9 VDDNB_5, A10 VDDNB_6, A8 VDDNB_7, A11 VDDNB_8, E10 VDDNB_9, E11 VDDNB_10, C10 VDDNB_11, VDDNB_12

VDDNB_13 C11, VDDNB_14 C12, VDDNB_15 D9, VDDNB_16 D8, VDDNB_17 D12, VDDNB_18 D11, VDDNB_19 B11, VDDNB_20 A12, VDDNB_21 B10, VDDNB_22 E12, VDDNB_23 B9

+VDDNB_CAP

VDDNB_CAP K13, VDDNB_CAP K12

DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split

+1.5VSUS

C106 0.22U/10V_4X, C107 0.22U/10V_4X, C108 180P/50V_4N, C109 180P/50V_4N

VDDIO=4.6A (Up to DDR3_1600 @ 1.5V)

+1.5VSUS

C110 0.22U/10V_4X, C111 0.22U/10V_4X, C112 0.22U/10V_4X, C113 0.22U/10V_4X, C114 0.22U/10V_4X, C115 0.22U/10V_4X

C124 180P/50V_4N, C125 180P/50V_4N

VDDIO_1 H26, VDDIO_2 K20, VDDIO_3 J28, VDDIO_4 K23, VDDIO_5 K26, VDDIO_6 L22, VDDIO_7 L25, VDDIO_8 L28, VDDIO_9 M20, VDDIO_10 M23, VDDIO_11 M26, VDDIO_12 N22, VDDIO_13 N25, VDDIO_14 N28, VDDIO_15 P20, VDDIO_16 P23, VDDIO_17 P26, VDDIO_18 AA28

VDDIO_19 T23, VDDIO_20 T26, VDDIO_21 U22, VDDIO_22 U25, VDDIO_23 U28, VDDIO_24 Y26, VDDIO_25 T20, VDDIO_26 R28, VDDIO_27 R25, VDDIO_28 R22, VDDIO_29 V20, VDDIO_30 V23, VDDIO_31 V26, VDDIO_32 W22, VDDIO_33 W25, VDDIO_34 W28, VDDIO_35 Y24, VDDIO_36 G28

+1.5VSUS

C116 22U/6.3V_6X, C117 22U/6.3V_6X, C118 22U/6.3V_6X, C119 22U/6.3V_6X, C120 4.7U/6.3V_6X, C121 4.7U/6.3V_6X, C122 4.7U/6.3V_6X, C123 4.7U/6.3V_6X

+1.2V_VDDP

+1.2V_VDDPR R80 0_8

VDDP_A + VDDP_B = 5A

C126 22U/6.3V_6X, C127 10U/6.3V_6X, C128 10U/6.3V_6X, C129 10U/6.3V_6X

1026 change for EOD

C133 0.22U/10V_4X, C134 0.22U/10V_4X, C135 180P/50V_4N, C136 180P/50V_4N

VDDP AH6, AH5, AH4, AH3, AH7

VDDA AB10

VDDR AG10, AH8, AH9, AH10

VDDR = 3.3A (Up to DDR3_1600 @ 1.2V)

+1.2V_VDDR

R81 0_8

+1.2V_VDDPR

C130 10U/6.3V_6X, C131 10U/6.3V_6X, C132 10U/6.3V_6X

1026 change for EOD

C137 0.22U/10V_4X, C138 0.22U/10V_4X, C139 1000P/50V_4X, C140 180P/50V_4N, C141 180P/50V_4N

VDDA = 0.75A

+2.5V_VDDA L1 HCB1608KF-221T20_2A

C142 4.7U/6.3V_6X, C143 0.22U/10V_4X, C144 3300P/50V_4X, C145 ESD@39P/50V_4N

B2A add for ESD

Piledriver APU

EMI

+VDD_CORE

C71 470P/50V_4X, C72 470P/50V_4X, C73 470P/50V_4X

U1E

VSS_1 J20, VSS_2 L4, VSS_3 R7, VSS_4 W18, VSS_5 A15, VSS_6 AB17, VSS_7 AC22, VSS_8 AE21, VSS_9 AF24, VSS_10 AH23, VSS_11 AH25, VSS_12 B7, VSS_13 C14, VSS_14 C16, VSS_15 C2, VSS_16 C20, VSS_17 C22, VSS_18 C24, VSS_19 C26, VSS_20 C28, VSS_21 D13, VSS_22 D15, VSS_23 D17, VSS_24 D19, VSS_25 D23, VSS_26 D25, VSS_27 D27, VSS_28 E4, VSS_29 E9, VSS_30 F14, VSS_31 F16, VSS_32 F18, VSS_33 F20, VSS_34 F22, VSS_35 F26, VSS_36 F28, VSS_37 G13, VSS_38 G15, VSS_39 G17, VSS_40 G19, VSS_41 G21, VSS_42 G23, VSS_43 G25, VSS_44 G4, VSS_45 J22, VSS_46 J24, VSS_47 J4, VSS_48 J7, VSS_49 K11, VSS_50 K14, VSS_51 K9, VSS_52 AC11, VSS_53 L19, VSS_54 L7, VSS_55 M11, VSS_56 AF11, VSS_57 V19, VSS_58 V9, VSS_59 W16, VSS_60 W4, VSS_61 W7, VSS_62 Y11, VSS_63 Y20, VSS_64 Y22, VSS_65 Y9, VSS_66 A17, VSS_67 A13, VSS_68 K16, VSS_69 F24, VSS_70 G8, VSS_71 H7, VSS_72 J8

VSS_75 A19, VSS_76 A21, VSS_77 A23, VSS_78 A25, VSS_79 A7, VSS_80 AA4, VSS_81 AA7, VSS_82 AB13, VSS_83 AB15, VSS_84 AB19, VSS_85 AB21, VSS_86 AB23, VSS_87 AB25, VSS_88 AB27, VSS_89 AB9, VSS_90 AC14, VSS_91 AC16, VSS_92 AC18, VSS_93 AC20, VSS_94 AC24, VSS_95 AC26, VSS_96 AC28, VSS_97 AC4, VSS_98 AC7, VSS_99 AD9, VSS_100 AE13, VSS_101 AE15, VSS_102 AE17, VSS_103 M9, VSS_104 N10, VSS_105 N4, VSS_106 N7, VSS_107 R10, VSS_108 R4, VSS_109 T11, VSS_110 T9, VSS_111 U10, VSS_112 U18, VSS_113 U4, VSS_114 U7, VSS_115 V11, VSS_116 AE19, VSS_117 AE23, VSS_118 AE25, VSS_119 AE27, VSS_120 AE4, VSS_121 AE7, VSS_122 AF14, VSS_123 AF16, VSS_124 AF18, VSS_125 AF20, VSS_126 AF22, VSS_127 AF26, VSS_128 AF28, VSS_129 AF9, VSS_130 AG4, VSS_131 AG7, VSS_132 AH13, VSS_133 AH15, VSS_134 AH17, VSS_135 AH19, VSS_136 AH21, VSS_137 P9, VSS_138 C18, VSS_139 D21, VSS_140 W14, VSS_141 P11, VSS_142 C7, VSS_143 E8, VSS_144 K18, VSS_145 W12

Piledriver APU

Quanta Computer Inc.
PROJECT : Richland

Size	Document Number	Rev
	APU 4/4(POWER/GND)	1A

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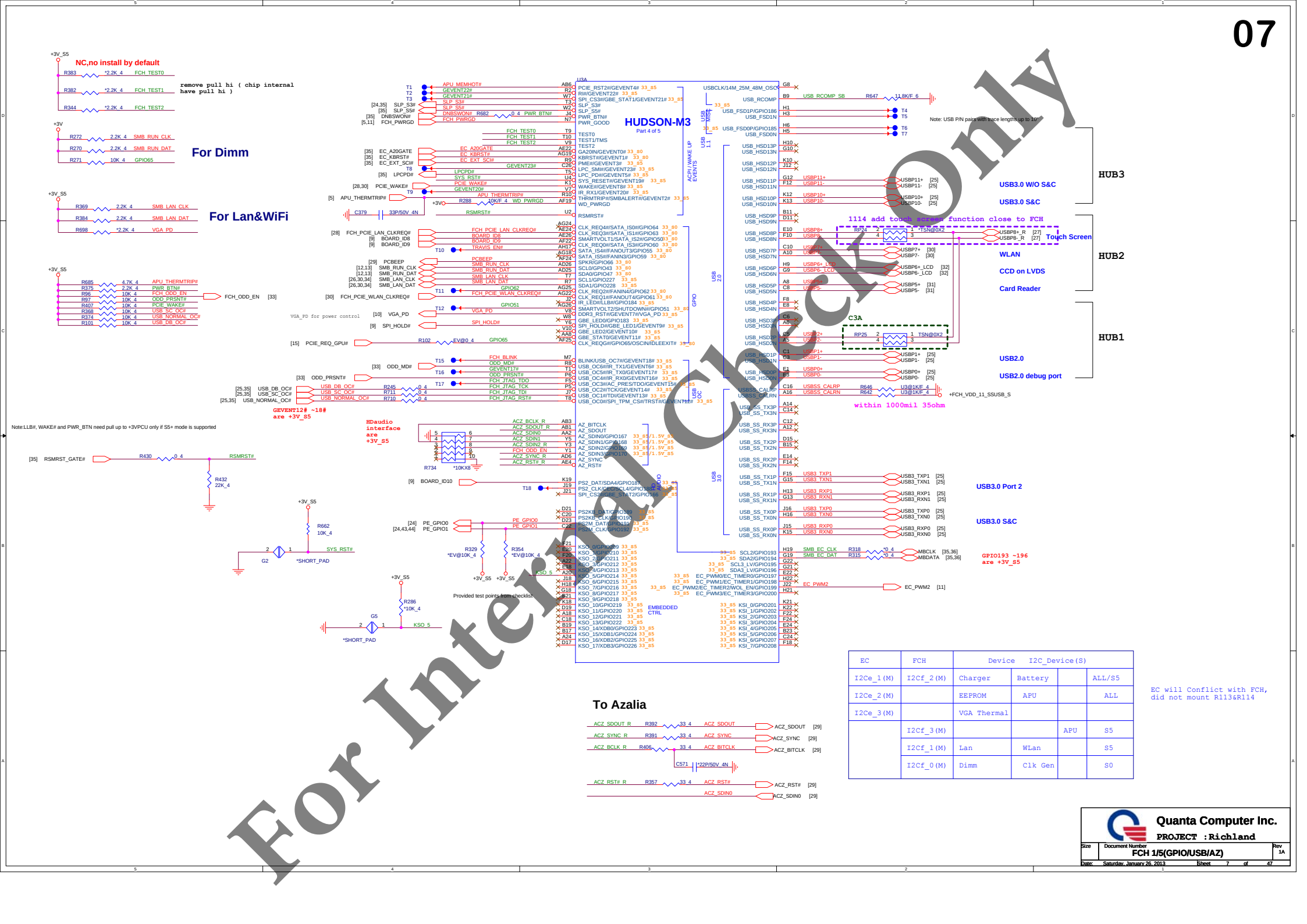

EC	FCH	Device	I2C_Device(S)		
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		EEPROM	APU		ALL
I2Ce_3(M)		VGA Thermal			
	I2Cf_3(M)			APU	S5
	I2Cf_1(M)	Lan	WLan		S5
	I2Cf_0(M)	Dimm	Clk Gen		S0

Quanta Computer Inc.
PROJECT : Richland

Size	Document Number	Rev
	FCH 1/5(GPIO/USB/AZ)	1A

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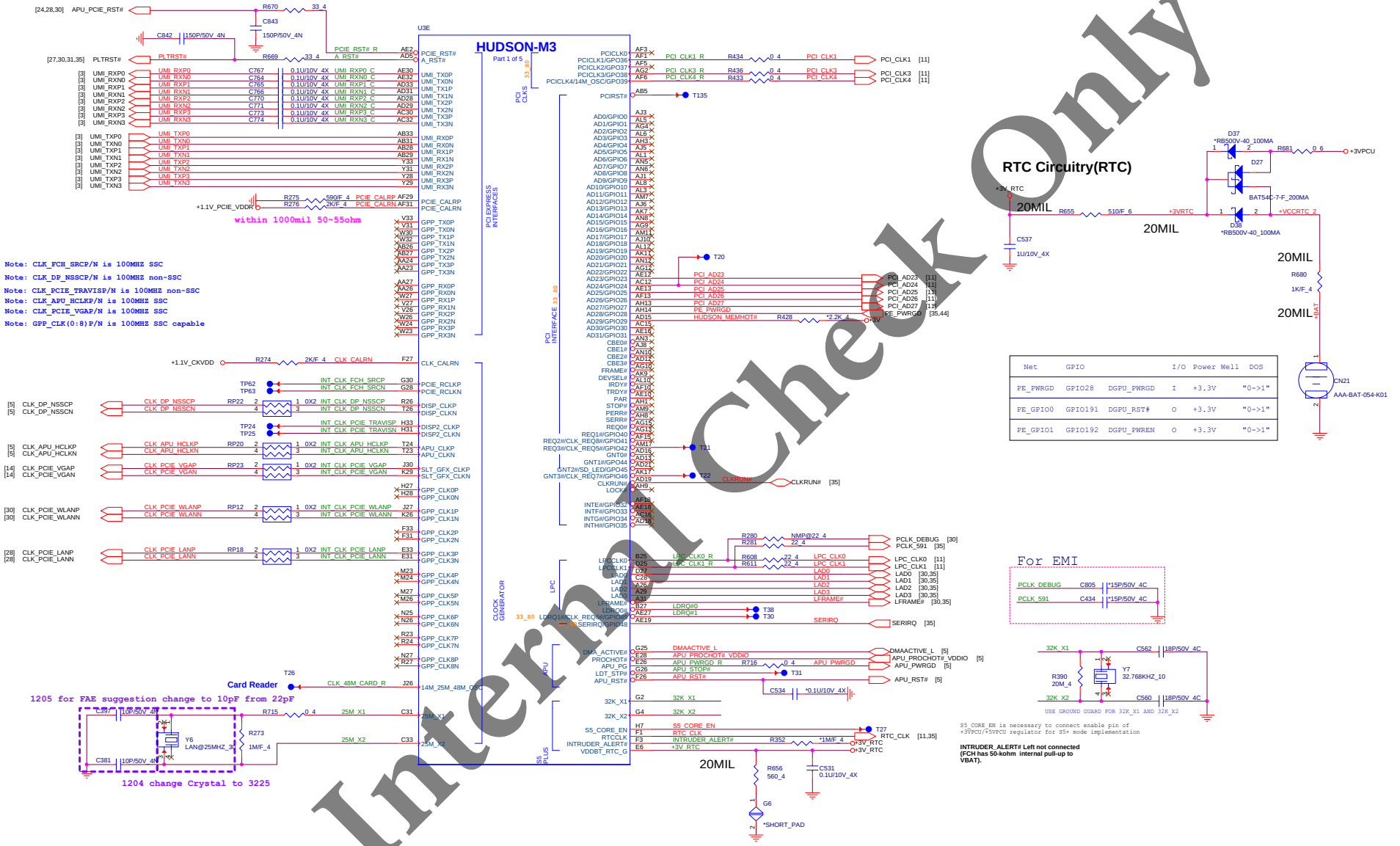

Net	GPIO		I/O	Power Well	DOS
PE_PWRGD	GPIO28	DGPU_PWRGD	I	+3.3V	"0->1"
PE_GPIO0	GPIO191	DGPU_RST#	O	+3.3V	"0->1"
PE_GPIO1	GPIO192	DGPU_PWREN	O	+3.3V	"0->1"

Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	FCH 2/5(ACPI/PCI/CLK)	1A

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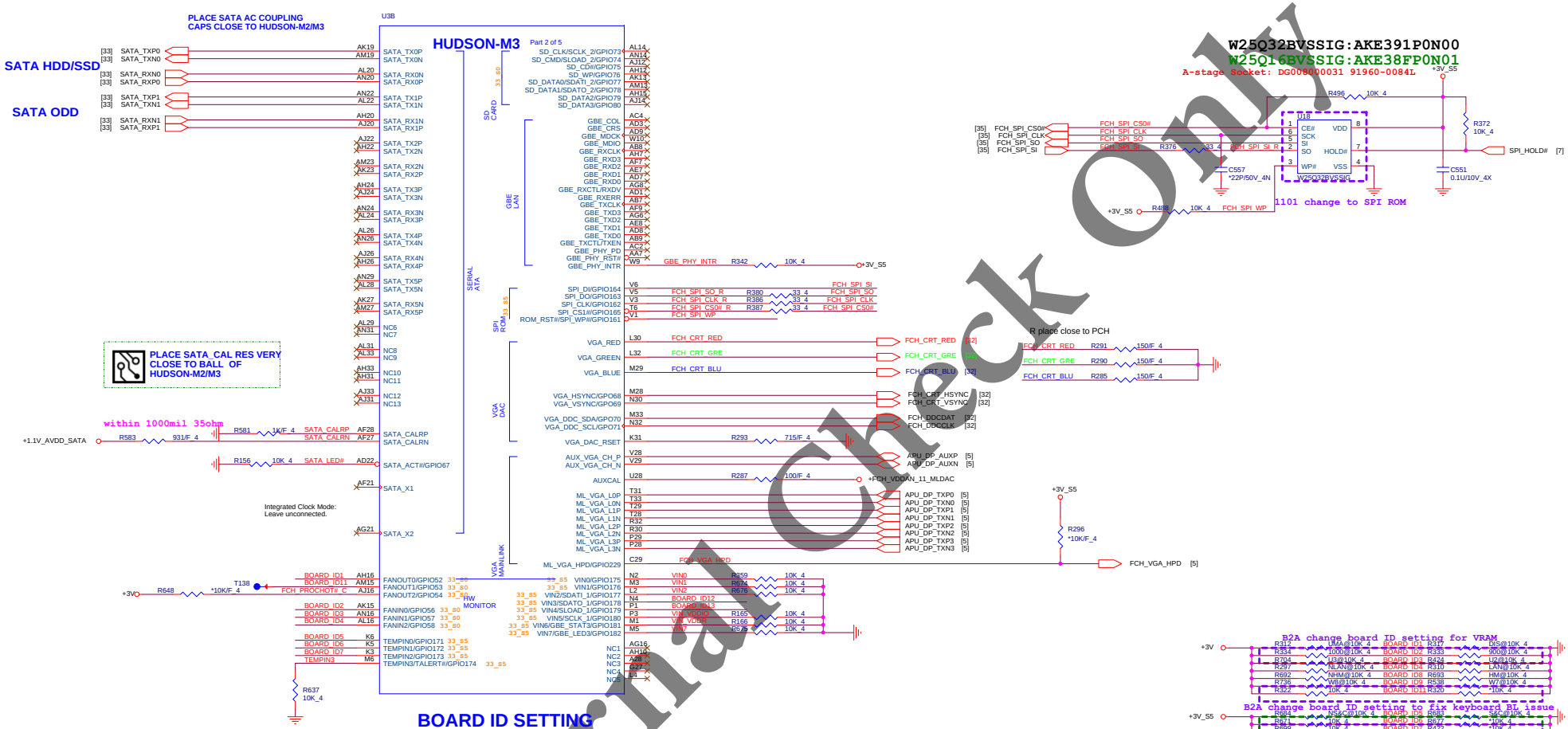


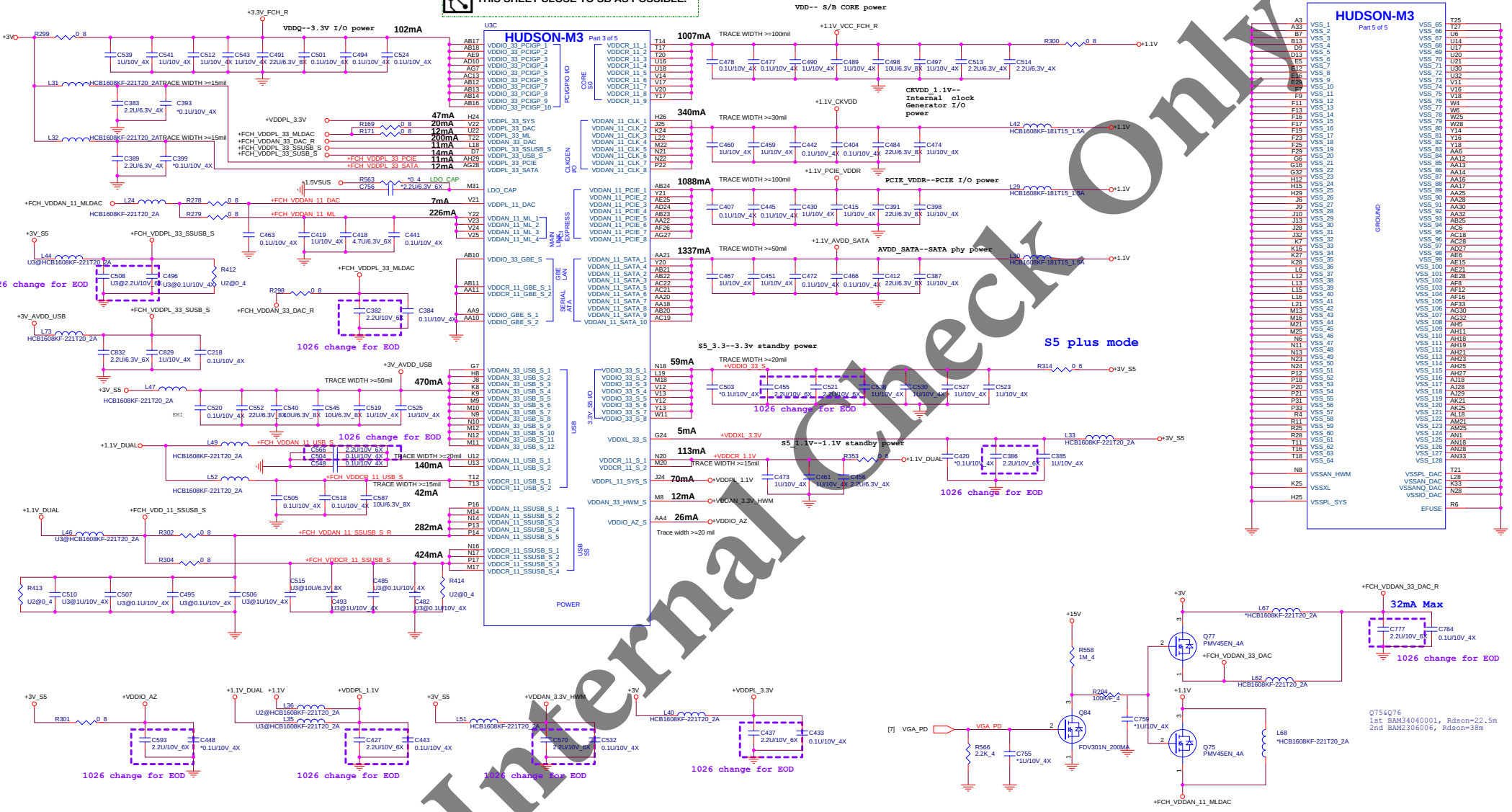
BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12	ID13
UMA SKU VGA SKU	H L												
1205 Change Board ID 1000 900		H L											
USB3.0 USB2.0			H L										
W/O LAN W LAN				H L									
W/O S&C W S&C					H L								
0111 change setting N-Brand Brand(Harman/Kardon)						H L							
1101 change setting N-METAL(W/O KBPLED) METAL(W KBPLED)							H L						
W/O HDMI W HDMI								H L					
W/O WLAN WLAN									H L				
1101 change setting Non-TEXTURE(BOX) TEXTURE(NBOX)										H L			
1029 change setting N-Brand Brand(ONKYO)											H L		
1120 Add Board ID Sun Mars												H L	
W/O CRT W CRT													H L

		Board ID10		Board ID11	Board ID6	Board ID7
		Speaker	Touch Pad	Box Vendor	Box Vendor	KB Backlight
H	Metal	Box	+3.3V	ONKYO/Harman Kardon/Others		V
	IMR					X
L	Texture	Boxless	+5V	X	X	X

Quanta Computer Inc.
PROJECT :Richland
Size | Document Number | Rev
FCH 3/5(SATA/VGA/GND/SPI) | 1A
Date: Saturday, January 26, 2013 | Sheet 9 of 47

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

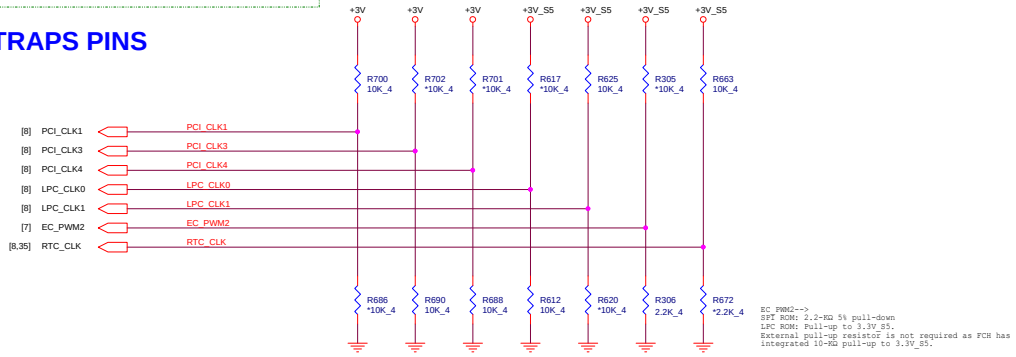


Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	FCH 4/5(POWER)	1A
Date: Saturday, January 26, 2013	Sheet 10 of 47	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

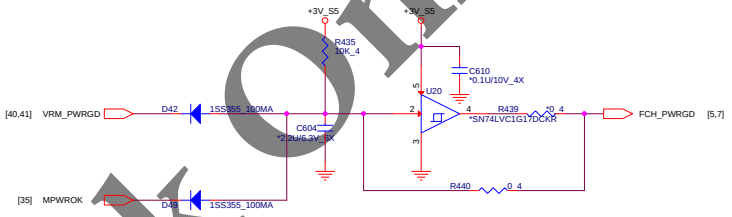
STRAPS PINS



Remove PCI_CLK2 function

REQUIRED STRAPS

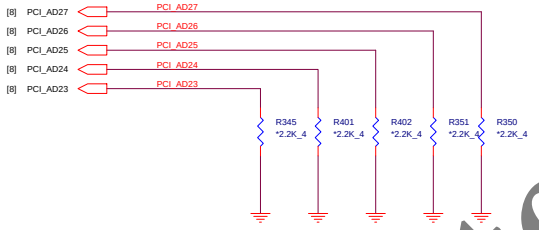
	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



FCH PWRGD CKT

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

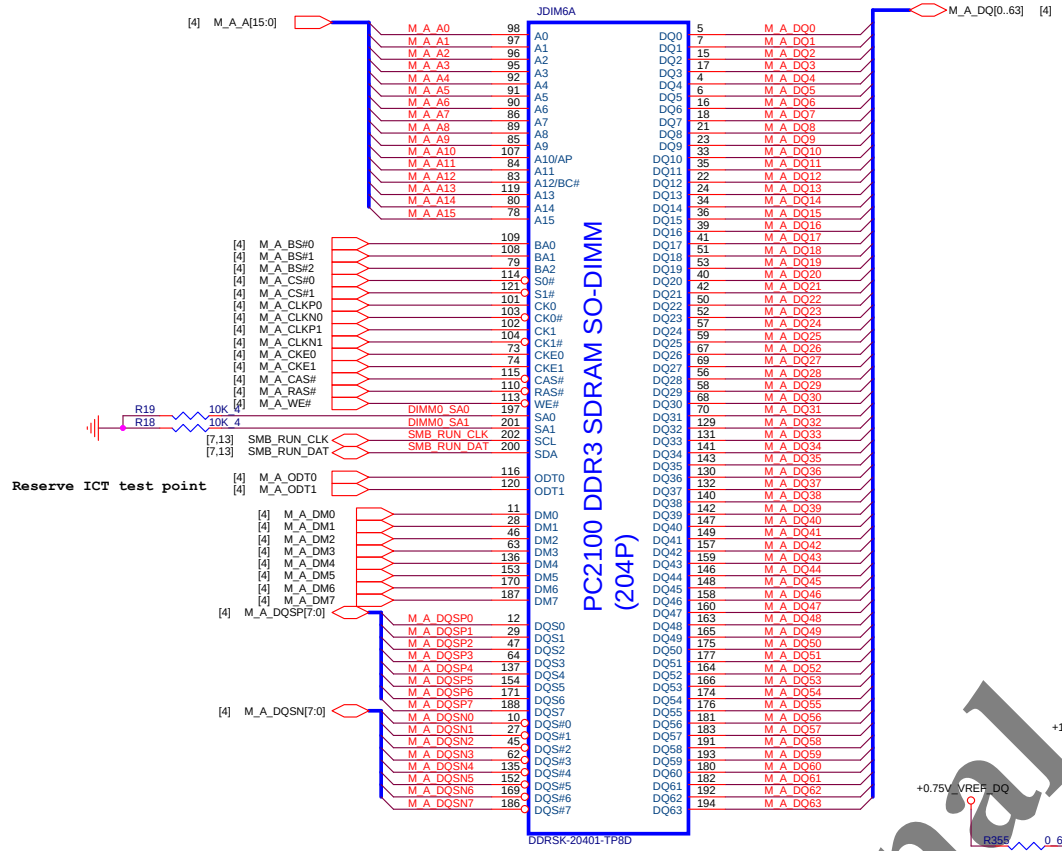


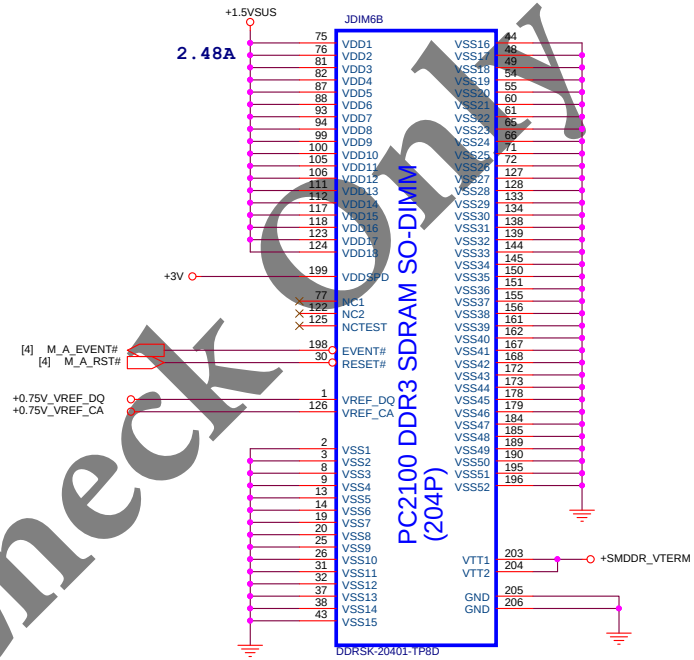
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

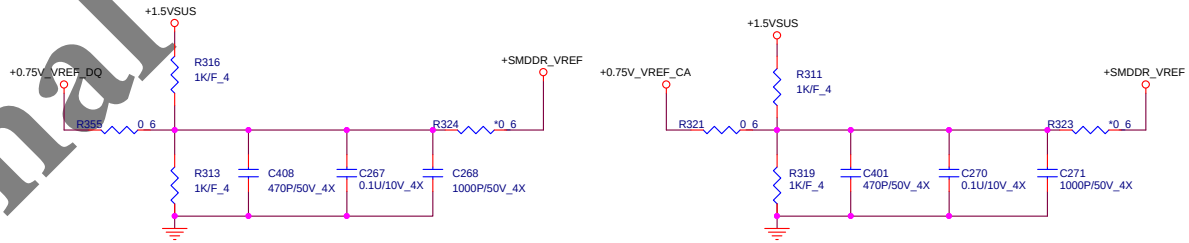
Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	1A
Date: Saturday, January 26, 2013	Sheet 11 of 47	

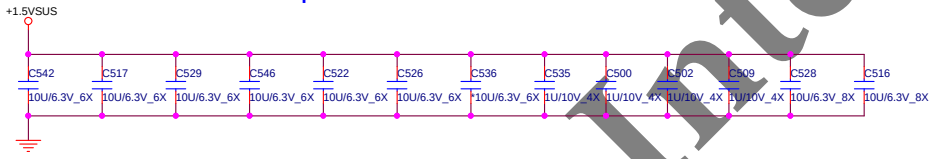
JDIM_1 close to APU, CLK Min=1016 mils



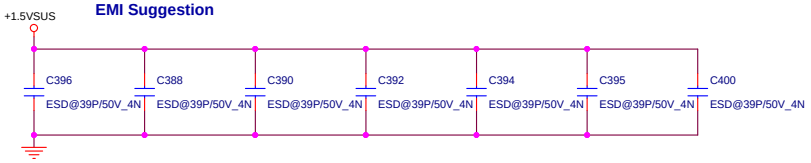


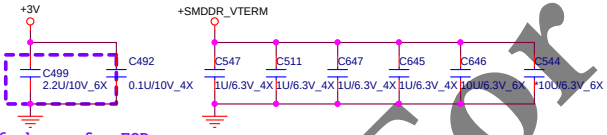


Place these Caps near So-Dimm0.

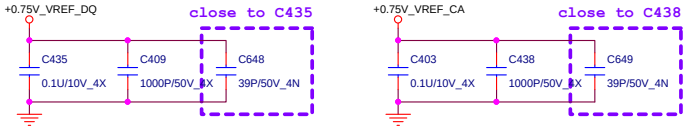


EMI Suggestion





1026 change for EOD



1206 Add 39pF for flash screen

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PROJECT :Richland

Size	Document Number	Rev
	DDR3 DIMM-1	1A

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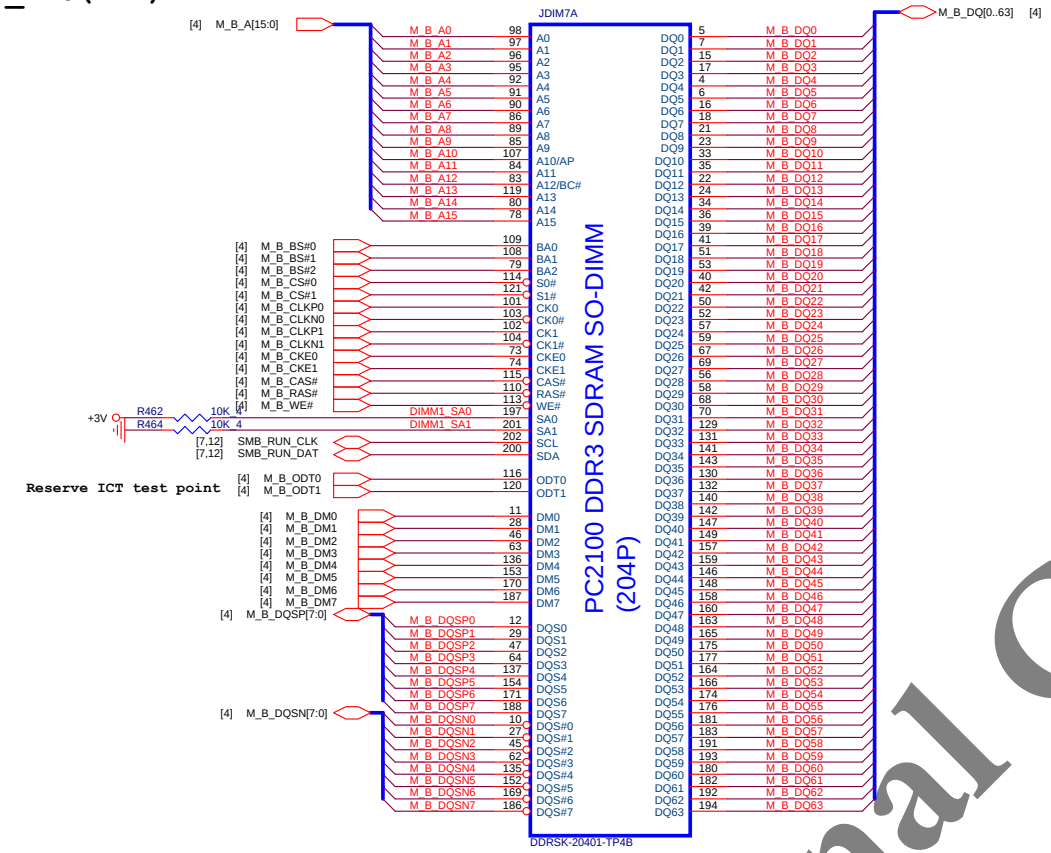
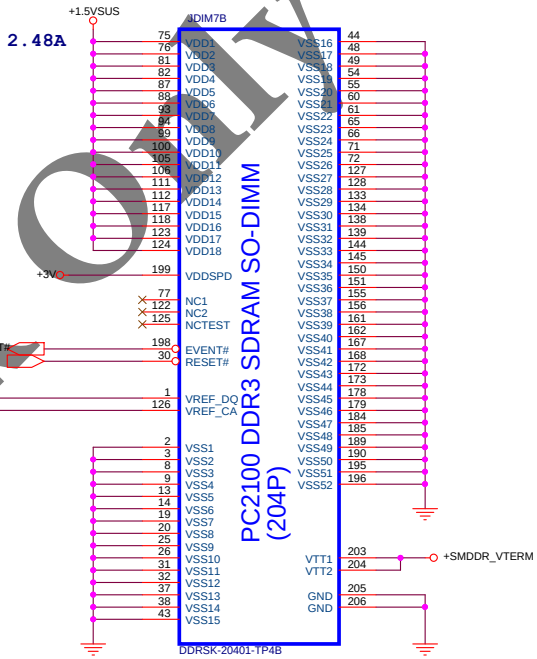
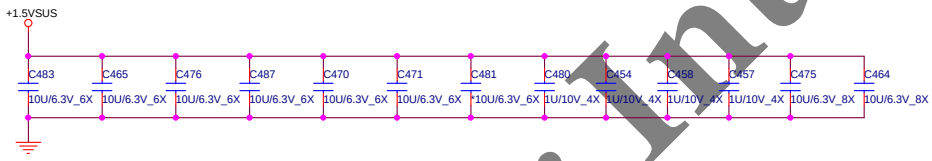
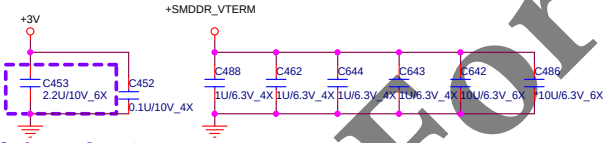
DDR_RVS (DDR)



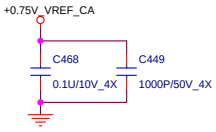


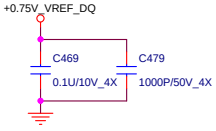
Place these Caps near So-Dimm1.



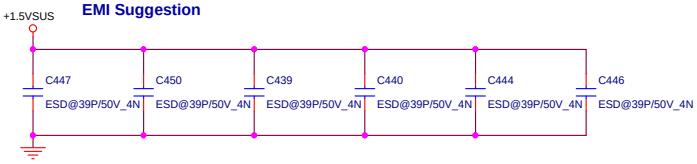


1026 change for EOD





EMI Suggestion



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PROJECT :Richland

Size	Document Number	Rev
	DDR3 DIMM-2	1A

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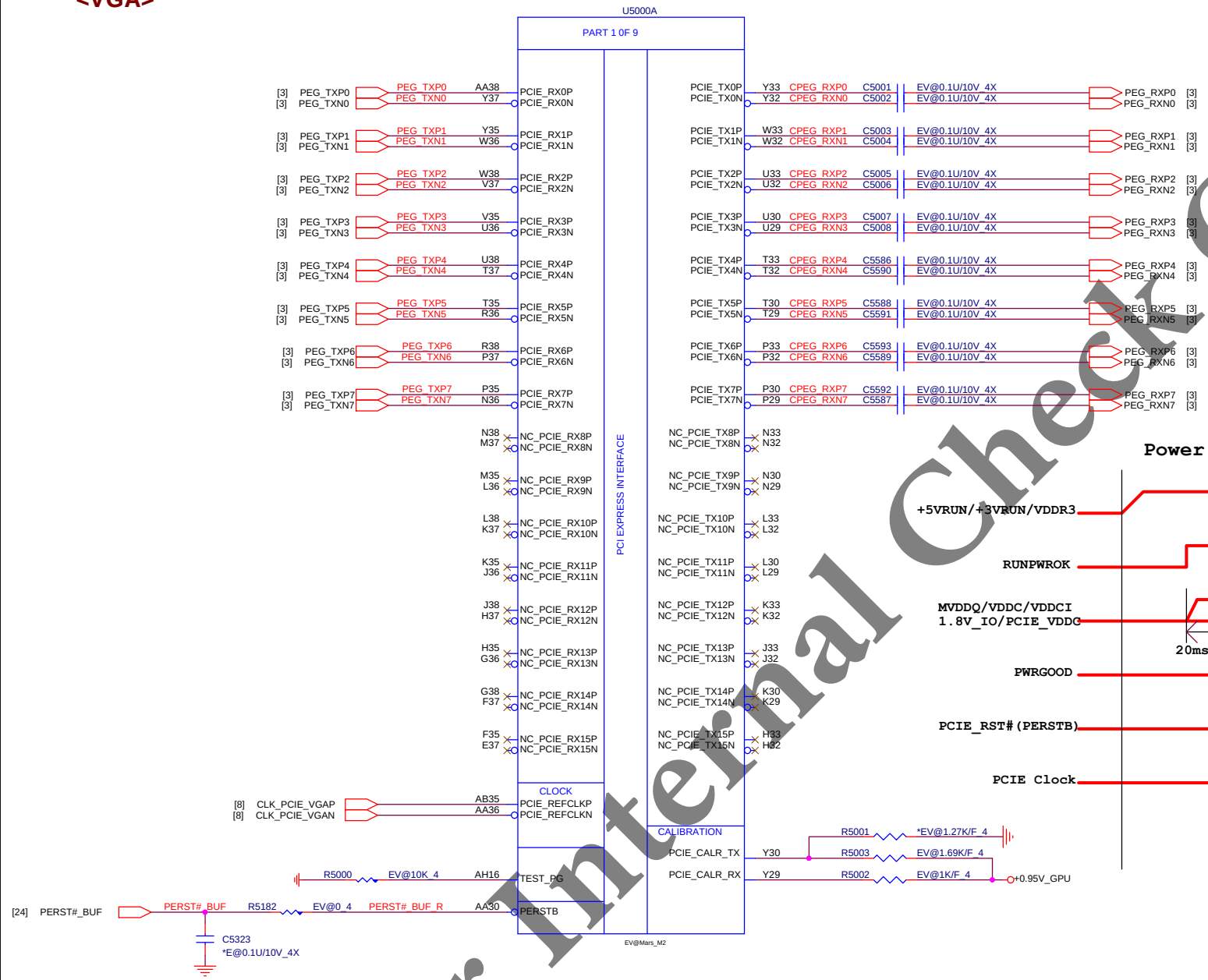
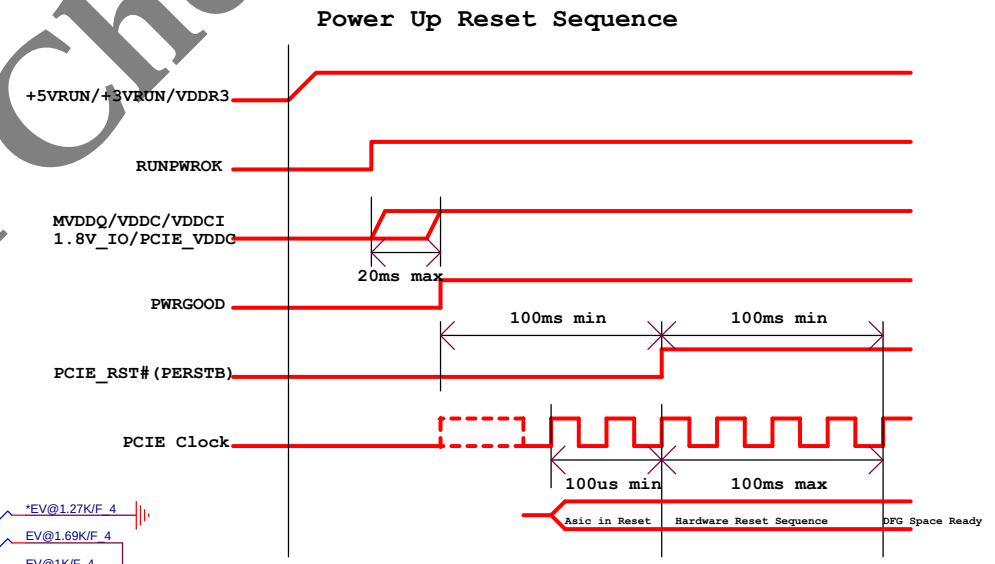


Mars Power-on sequence

1 => +3V_GPU
2 => +VDDC,+VDDCI,+1.5V_GPU,+0.95V_GPU
3 => +1.8V_GPU

PEG

Intel platform: Lane0 ~ Lane15
Brazos platform: Lane12 ~ Lane15
Comal and Sabine platform: Lane8 ~Lane15
Richland and Kabini platform: Lane0 ~ Lane7



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PROJECT : Richland

Size	Document Number	Rev
	Mars_M2/ PEG*8	A1A

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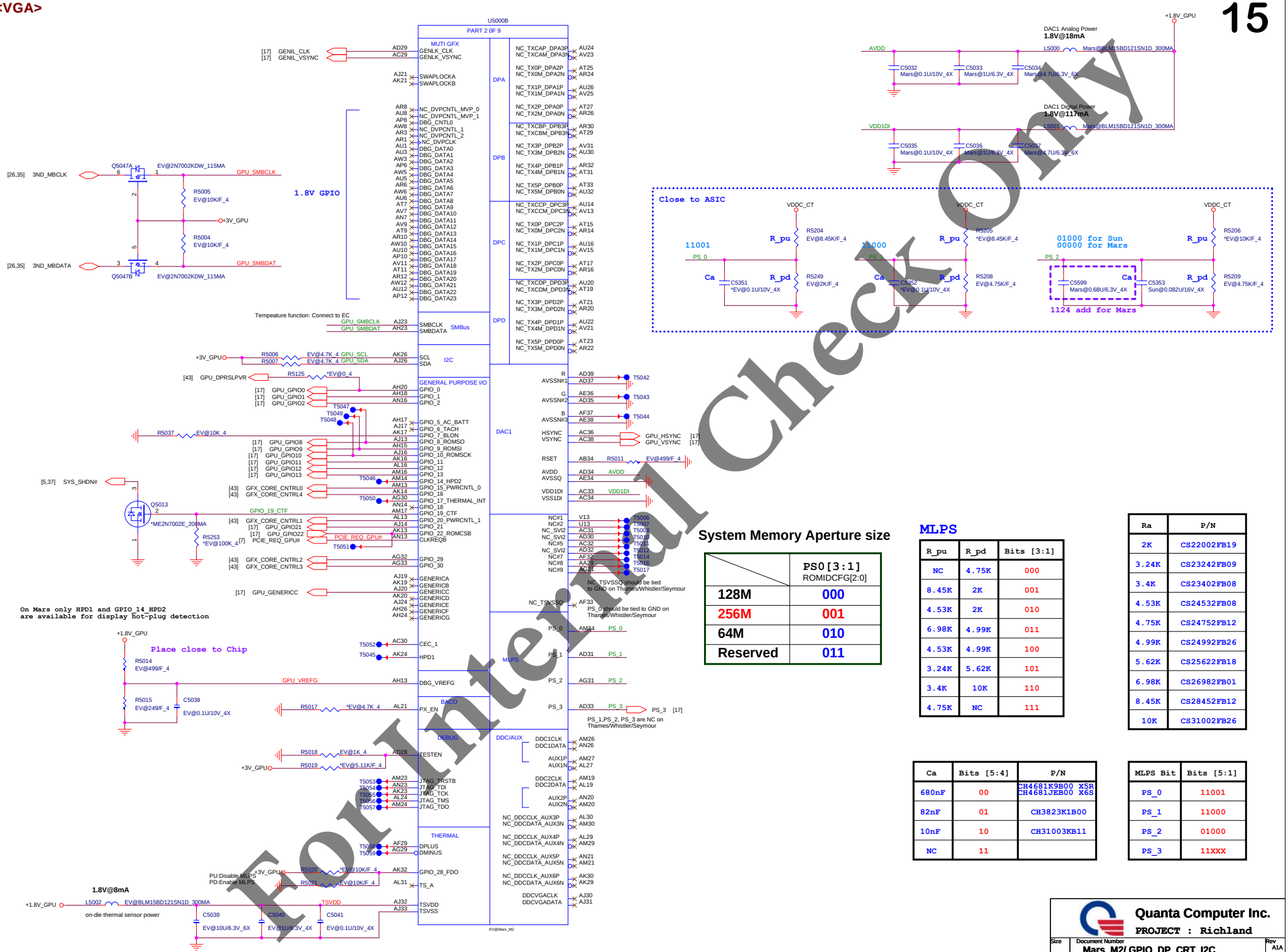

System Memory Aperture size

	PS0[3:1] ROMIDCFG[2:0]
128M	000
256M	001
64M	010
Reserved	011

MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00 X5R CH4681JEB00 X6S
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	01000
PS_3	11XXX

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Size	Document Number	Rev
	Mars_M2/ GPIO_DP_CRT_I2C	A1A

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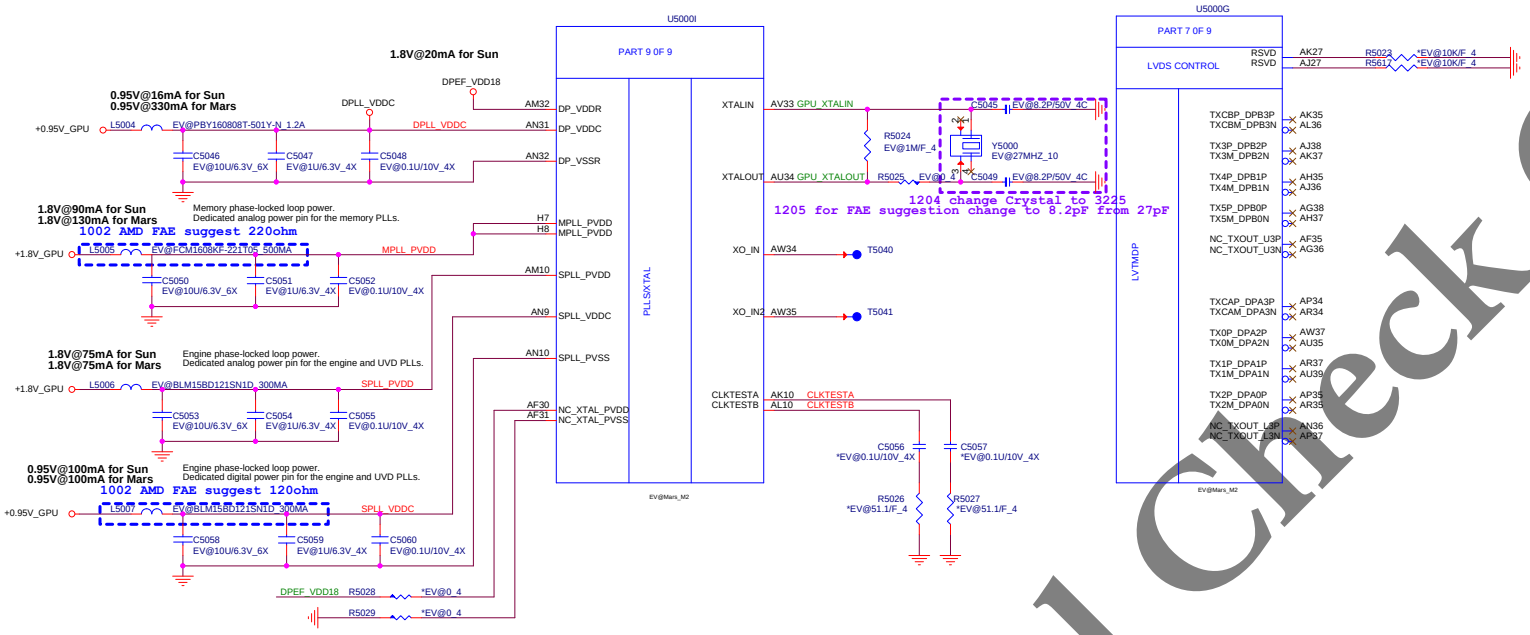
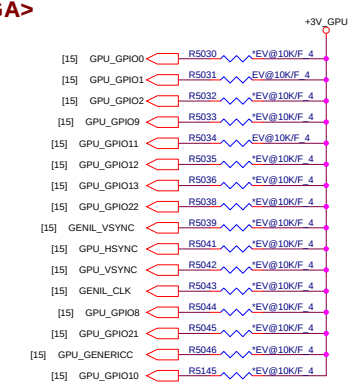
DPE/DPF/LVDS

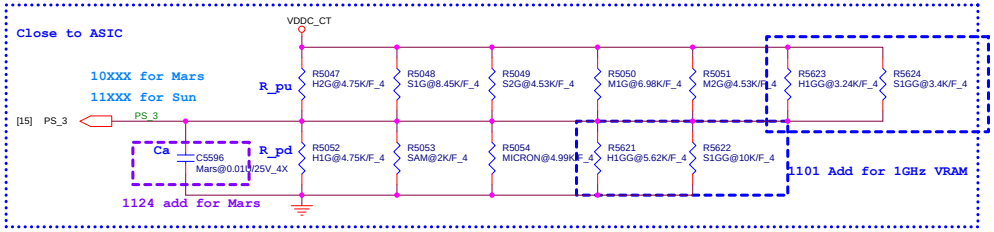


Quanta Computer Inc.
PROJECT : Richland

Size	Document Number	Rev
	Mars_M2/ XTAL_LVDS	A1A
Date: Saturday, January 26, 2013	Sheet 16 of 47	

<VGA>





MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

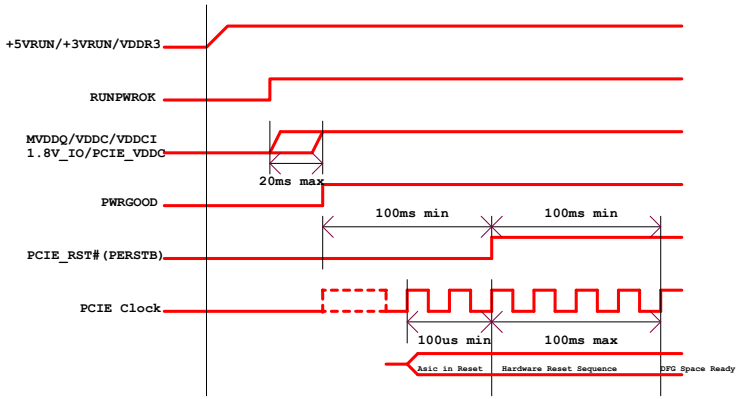
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
STRAP_TX_CFG_DRV_FULL_SWING	PS_1[4]		Control the transmitter full-/half- swing mode 0: 50% Tx output swing 1: Full Tx output swing	1
STRAP_TX_DEEMPH_EN	PS_1[5]		PCIe transmitter, de-emphasis enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
STRAP_BIF_GEN3_EN_A	PS_1[1]		PCIe GEN3 Capability 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	0 for Kabini
STRAP_BIF_VGA_DIS	PS_2[4]		VGA disable determines whether or not the card will be recognized as the system's VGA controler (through the SUBCLASS field in the PCI configuration space) 0: VGA controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
ROM_CONFIG[2:0]	PS_0[3..1]		Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
STRAP_BIOS_ROM_EN	PS_2[3]		Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
N/A	PS_0[4]		Reserved for internal use only. Must be 1 at reset	1
N/A	PS_1[3]	GENLK_CLK	Reserved	0
STRAP_BIF_CLK_PM_EN	PS_1[2]	GPIO8	PCIe reference clock power management capability is reported in the PCI 0: The CLKREQB power management capability is disabled 1: The CLKREQB power management capability is enabled	0
RESERVED RESERVED	NA NA	GPIO21 GENERICC	Reserved Reserved (for Thames/Whistler/Seymour only)	0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

DDR3 Memory TYPE

Vendor	Vendor P/N	B/S P/N (QCI P/N)	Size	MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)(900MHz)	AKD5MGWTW16 * 4	1GB	000
	H5TC4G63AFR-11C (256M*16)(900MHz)	AKD5PGWTW05 * 4	2GB	111
	H5TQ2G63DFR-N0C (128M*16)(1GHz)	AKD5MGDTW01 * 4	1GB	101
Micron	MT41J128M16JT-107G:K (128M*16)(900MHz)	AKD5DGSTL00 * 4	1GB	011
	MT41K256M16HA-107G:E (256M*16)(900MHz)	AKD5PGSTL00 * 4	2GB	100
Samsung	K4W2G1646E-BC11 (128M*16)(900MHz)	AKD5MGGT520 * 4	1GB	001
	K4W4G1646B-HC11 (256M*16)(900MHz)	AKD5MGWT516 * 4	2GB	010
	K4W2G1646B-BC1A (128M*16)(1GHz)	AKD5MGGT532 * 4	1GB	110

Power Up Reset Sequence



Quanta Computer Inc.
PROJECT : Richland

Size	Document Number	Rev
	Mars_M2/ STRAPS_Thermal	A1A

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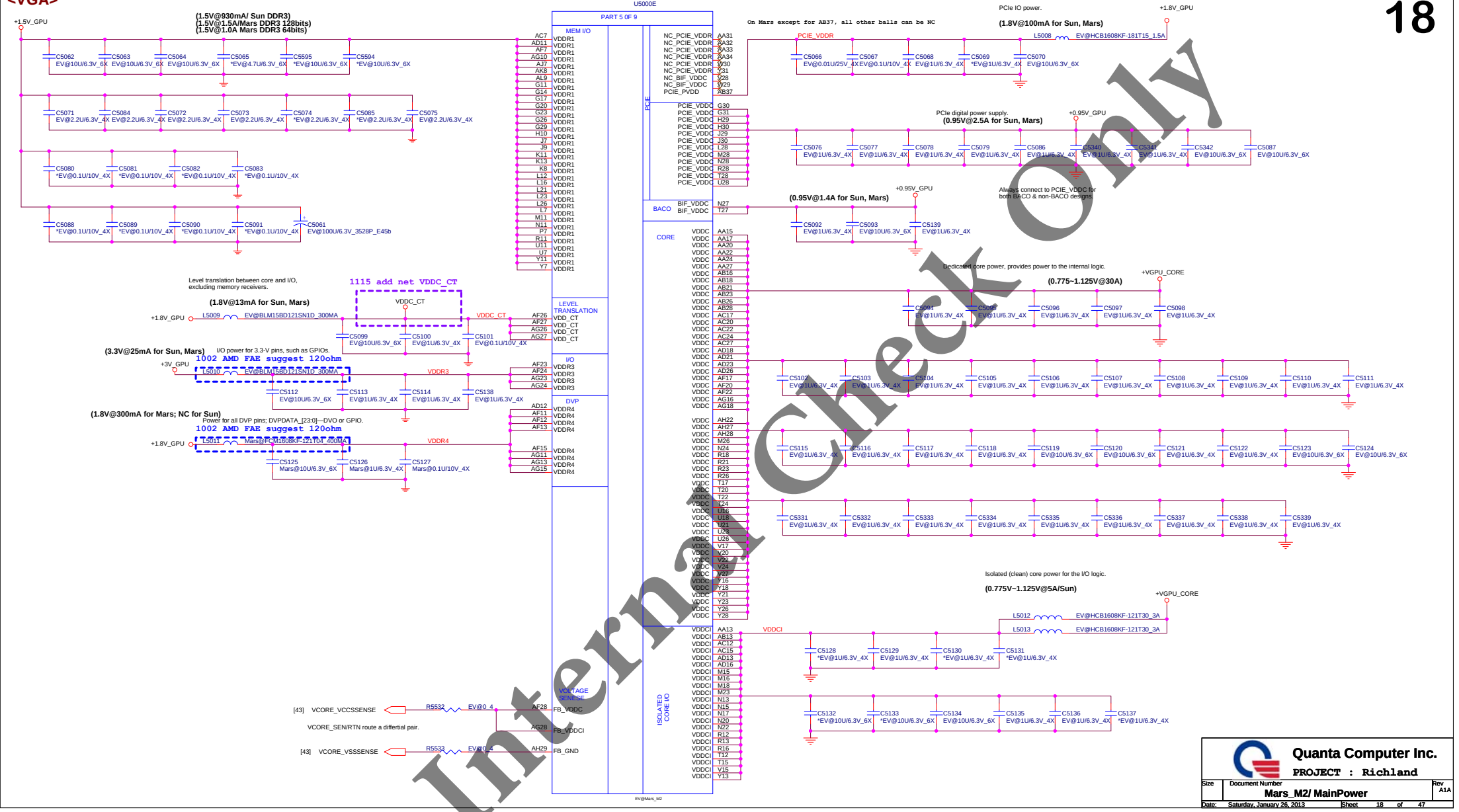
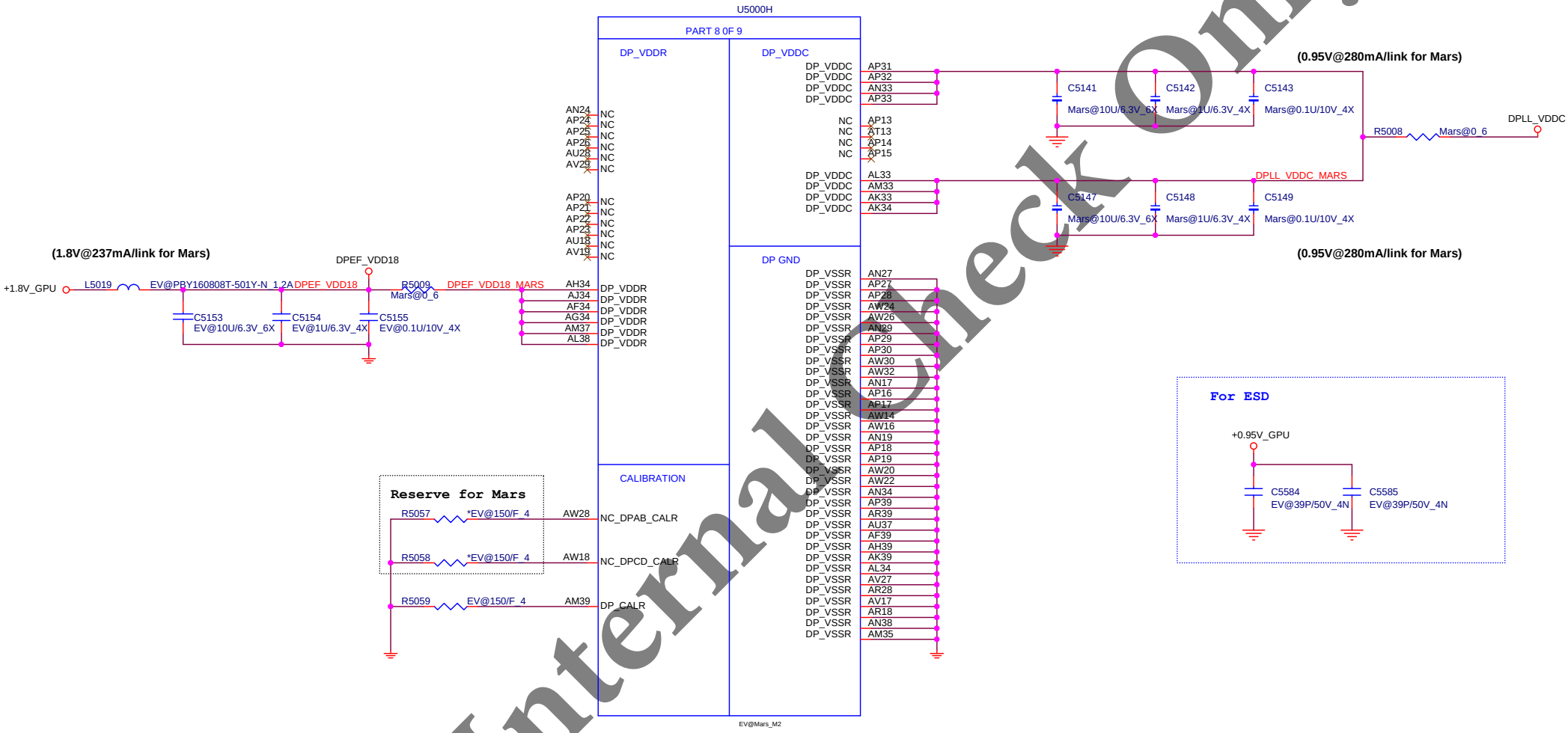
<VGA>



Quanta Computer Inc.		
PROJECT : Richland		
Size	Document Number: Mars_M2/ MainPower	Rev: A1A
Date: Saturday, January 26, 2013	Sheet 18 of 47	



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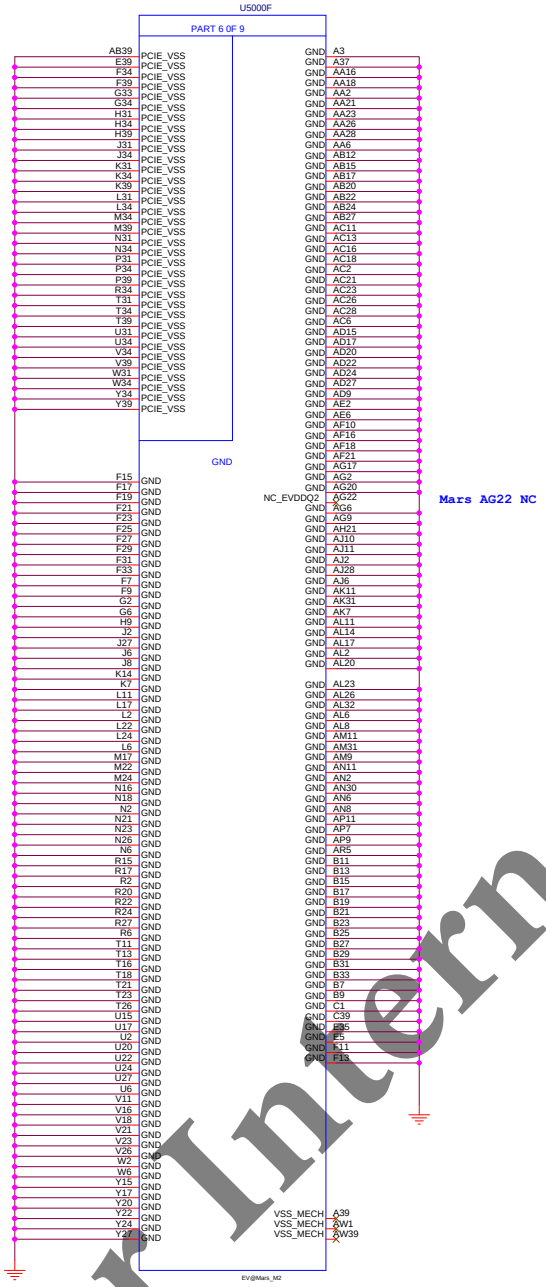
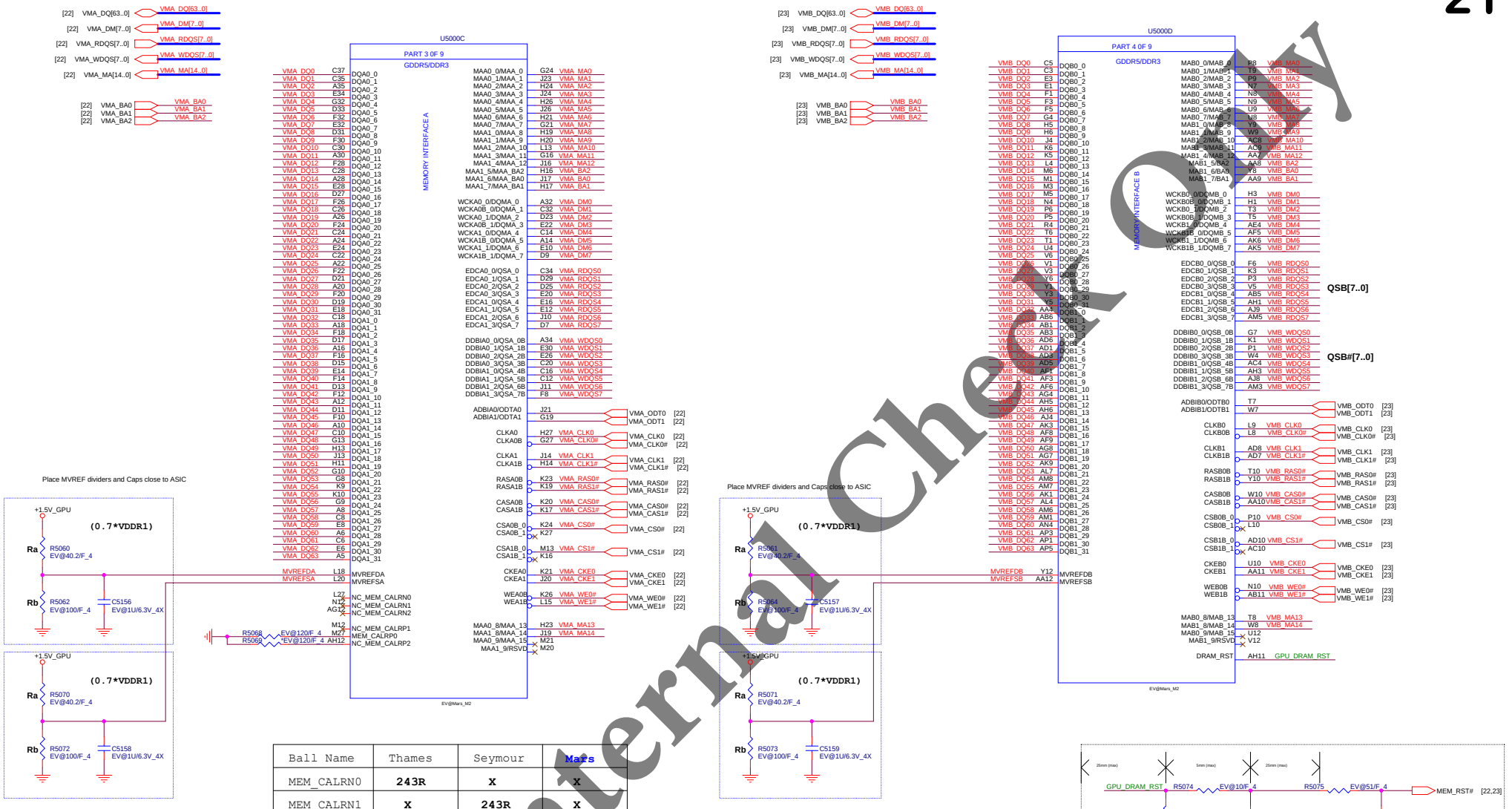
PROJECT : Richland

Size	Document Number	Rev
	Mars_M2/ DP_Powers	A1A
Date: Saturday, January 26, 2013	Sheet 19 of 47	

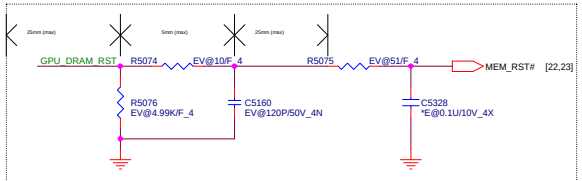


Mars AG22 NC

Quanta Computer Inc.			
PROJECT : Richland			
Size	Document Number		Rev
	Mars_M2/ GND		A1A
Date: Saturday, January 26, 2013	Sheet 20 of 47		



Ball Name	Thames	Seymour	Mars
MEM_CALRN0	243R	X	X
MEM_CALRN1	X	243R	X
MEM_CALRN2	243R	X	X
MEM_CALRP0	243R	X	120R
MEM_CALRP1	X	243R	X
MEM_CALRP2	243R	X	X



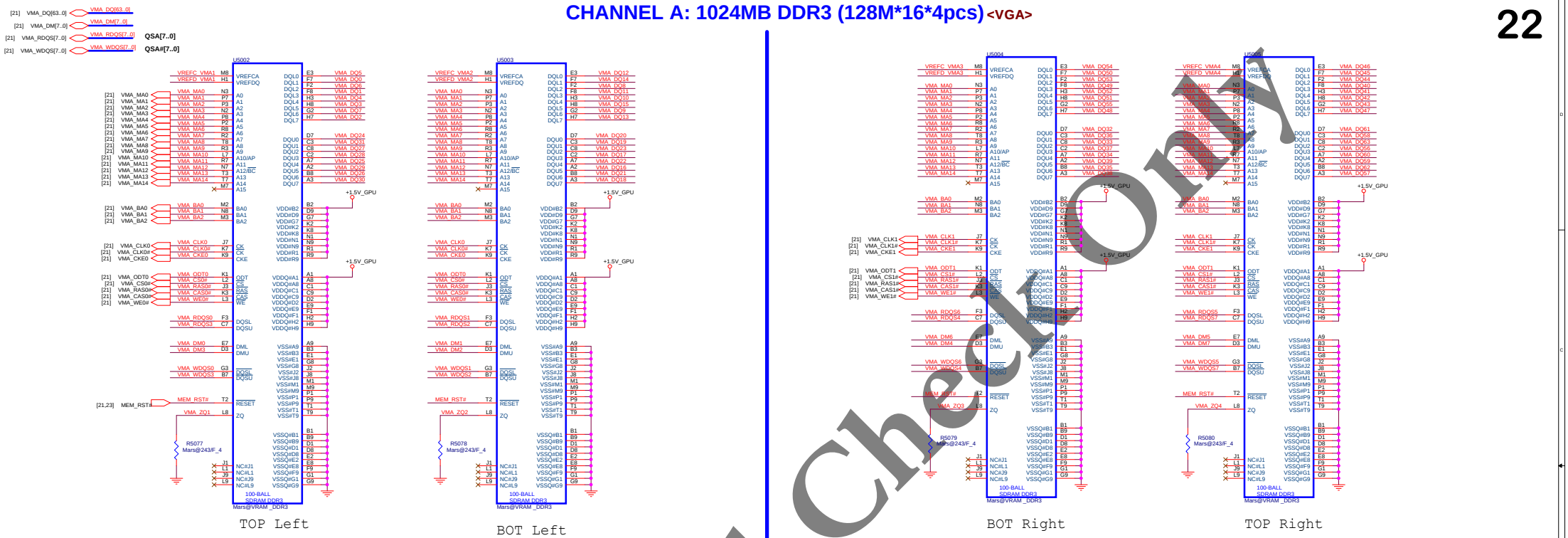
Place all these componets very close to GPU (within 25mm)
and keep all components close to each other
** This basic topology should be used for DRAM_RAT for DDR3/GDDR5

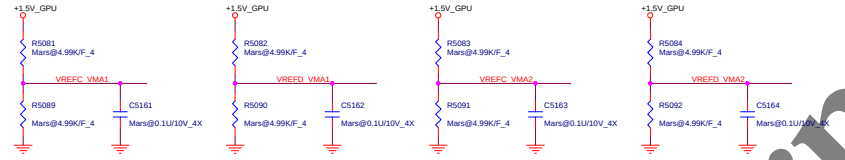
These Capacitors and Resistor values arre an example only
The series R and || cap values will depend on the DRAM loads
and will have to be calculated for differrent Memory, DRAM loads and board
to pass Reset Signal Spec

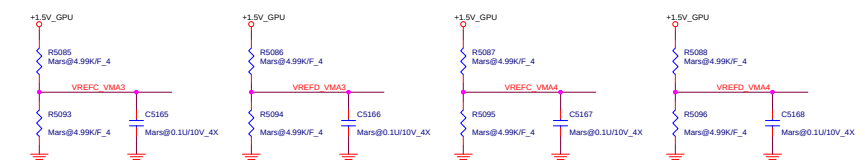
Quanta Computer Inc.
PROJECT : Richland

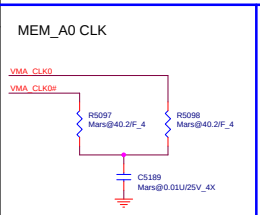
Size	Document Number	Rev
	Mars_M2/ MEM Interface	A1A
Date: Saturday, January 26, 2013	Sheet 21 of 47	

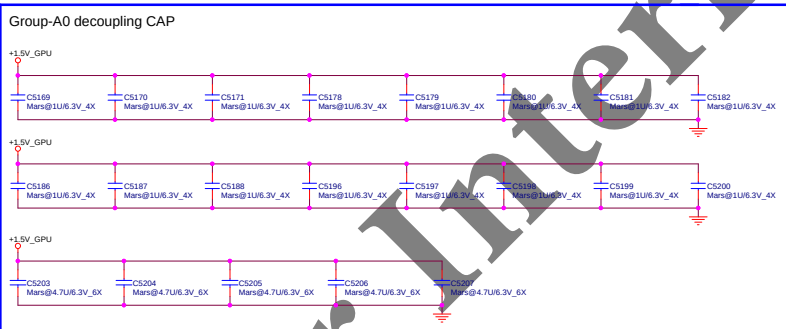
CHANNEL A: 1024MB DDR3 (128M*16*4pcs) <VGA>

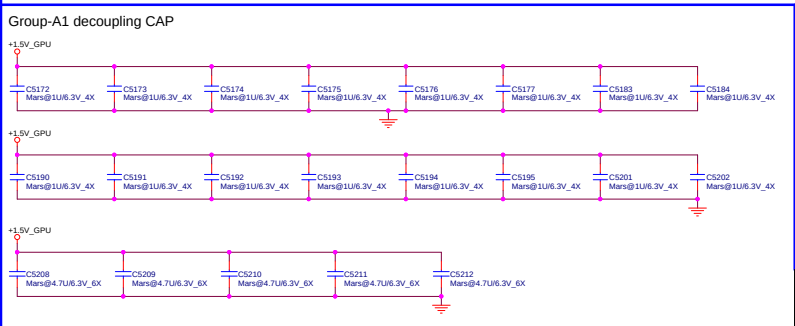


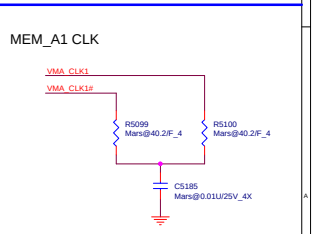












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PROJECT : Richland

Size	Document Number	Rev
	VRAM_A: DDR3*4PCS	A1A

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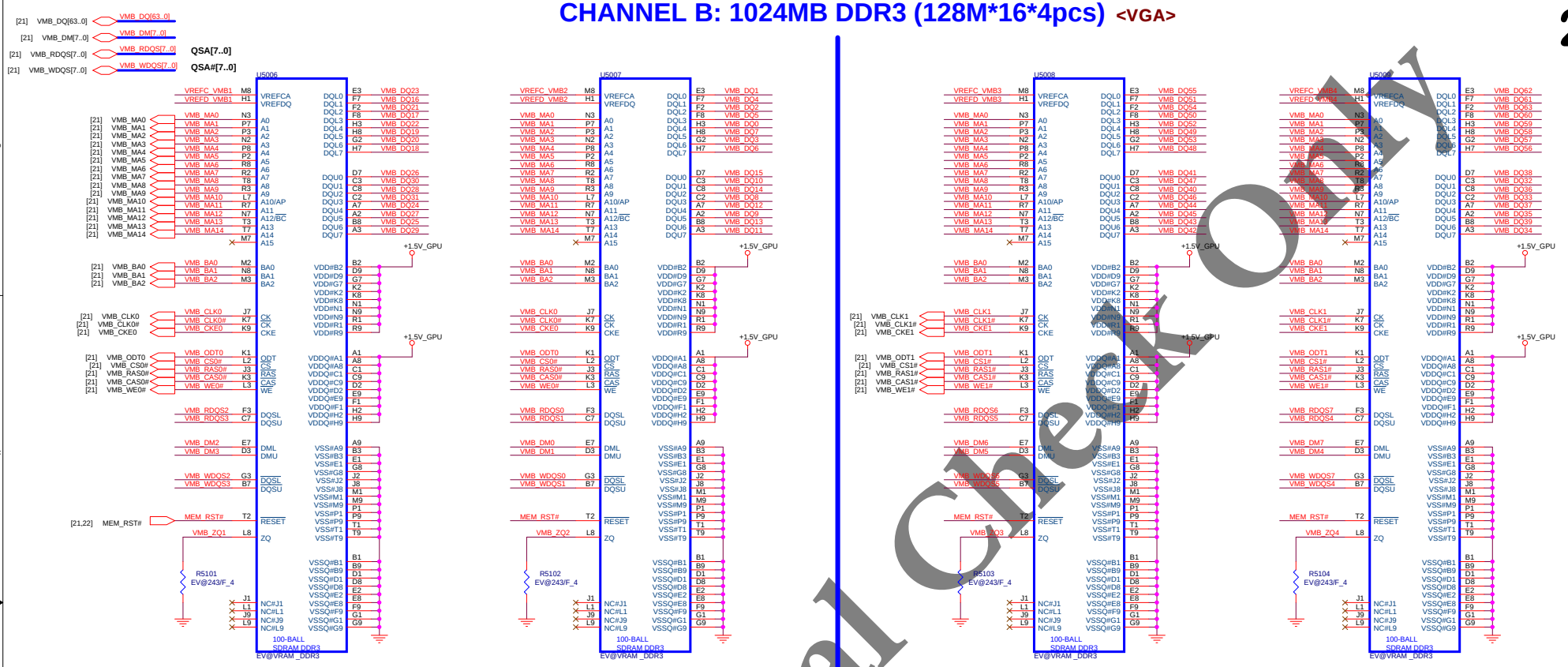
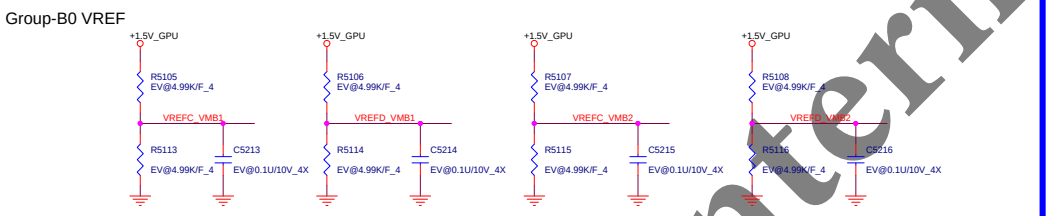
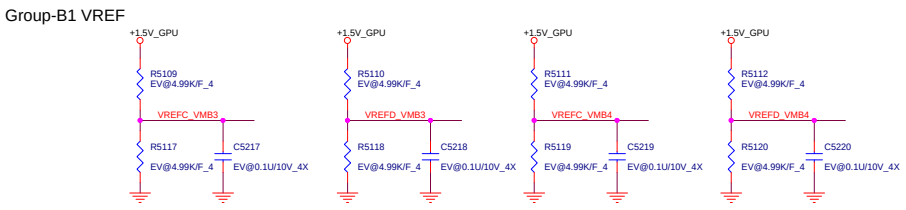
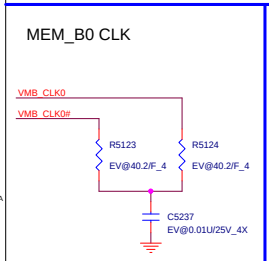
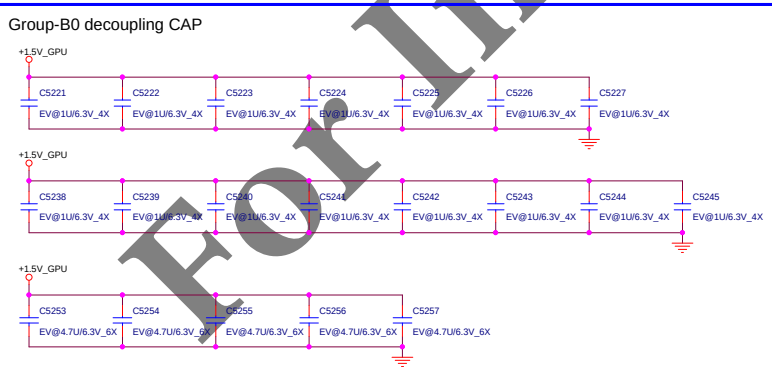
CHANNEL B: 1024MB DDR3 (128M*16*4pcs) <VGA>

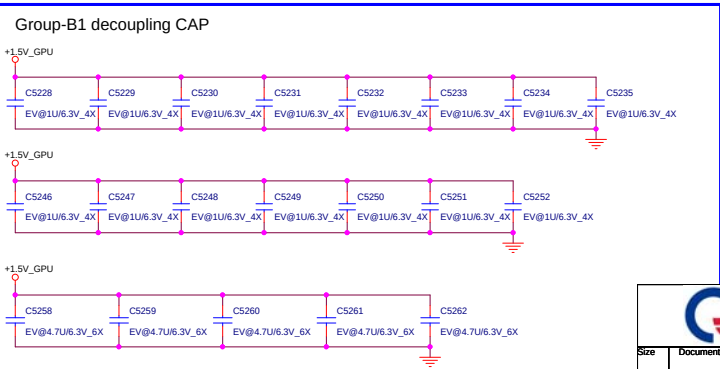


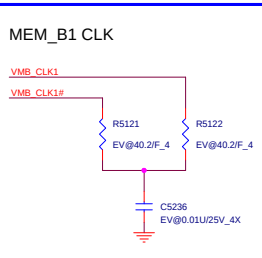












Quanta Computer Inc.
PROJECT : Richland

Size	Document Number	Rev
	VRAM_B: DDR3*4PCS	A1A

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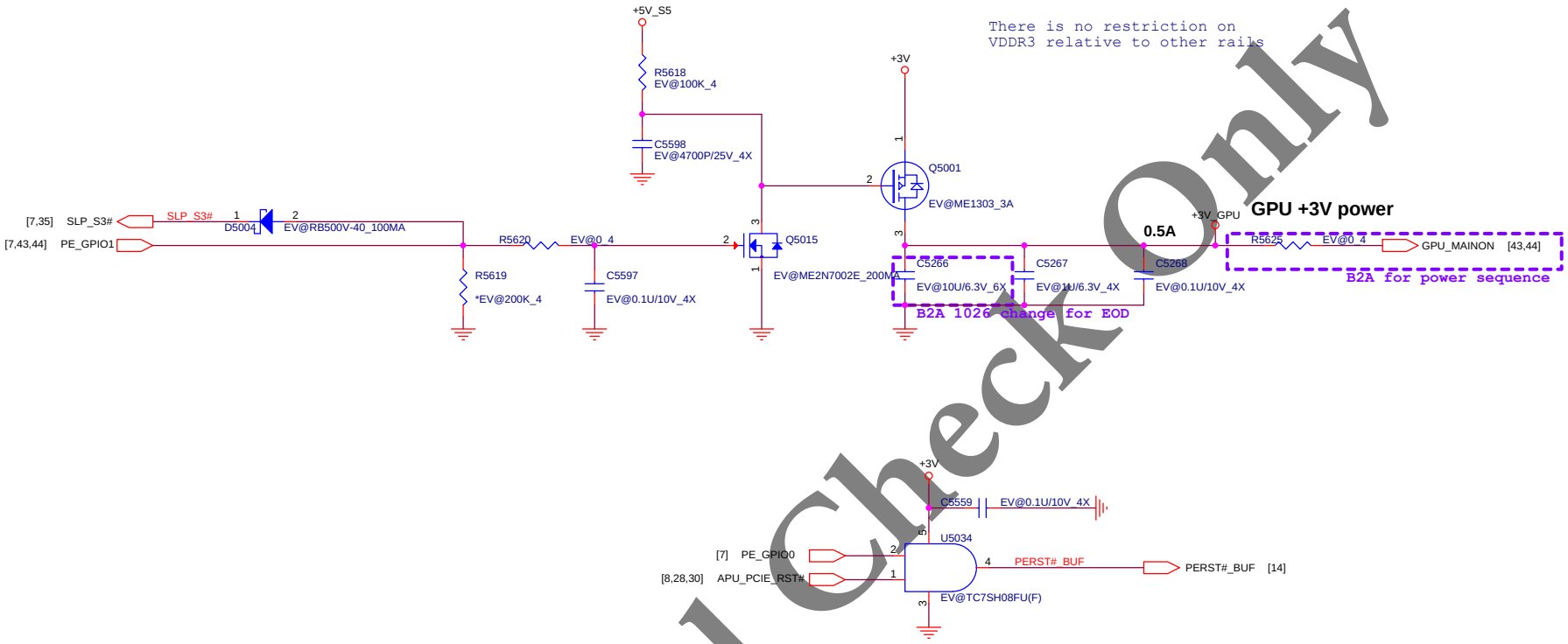
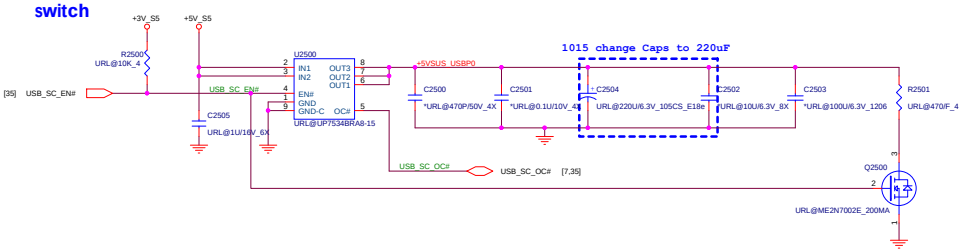


Quanta Computer Inc.		
PROJECT : Richland		
Size	Document Number: Mars_M2/ PX5	Rev: A1A
Date: Saturday, January 26, 2013	Sheet 24 of 47	

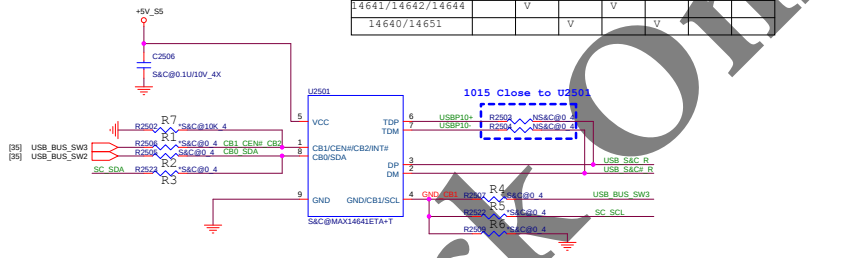
USB 3.0 Power switch <USB> <U3B>



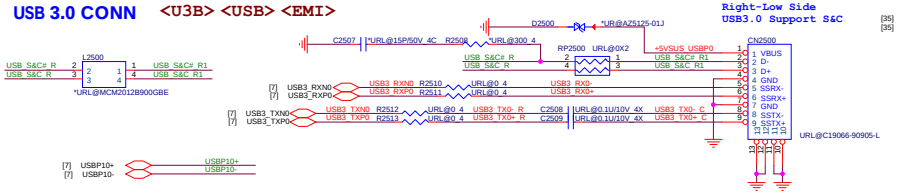
USB w S&C MAXIM solution <SLC>

14566/14600/14617

	R1	R2	R3	R4	R5	R6	R7
14566	V	V				V	
14600		V		V			
14617(no CB2)		V		V			V
14641/14642/14644		V		V			
14640/14651			V		V		



USB 3.0 CONN <U3B> <USB> <EMI>



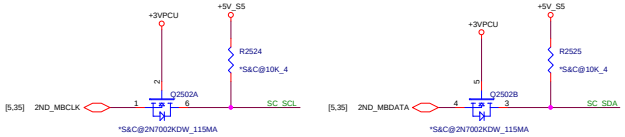
SW2	SW3	14600	
CB0	CB1	Status	
0	0	Auto mode	Charger , AM
0	1	Force dedicated charger mode	Charger , FM
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

C&S update OSC table

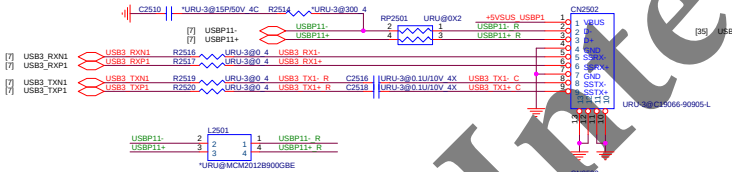
SW2	SW3	14641	
CB0	CB1	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
0	1	Force 1A for Apple device	Charger , AP1
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14644	
CB0	CB1	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
0	1	Force dedicated charger mode	Charger , FM
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14642	
CB0	CB1	Status	
0	X	2A Auto mode for Apple device	Charger , AM2
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM



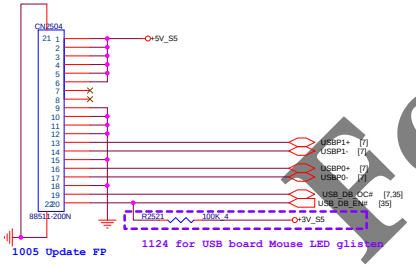
USB 3.0 CONN <U3B> <U2B> <EMI>

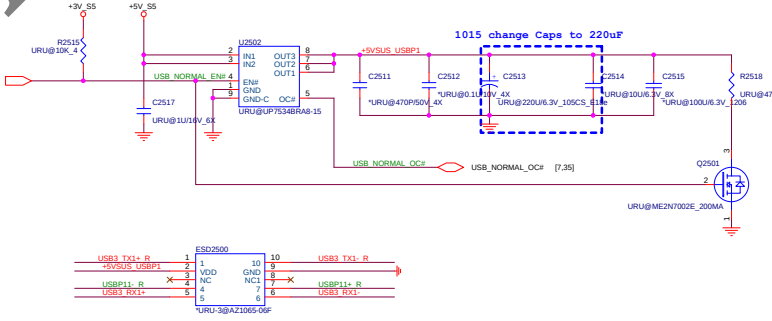


Confirm

USB3.0	DFHS09FR085	ULU-3@TARA9-9V1391
USB2.0	DFHS04FR487	ULU-2@UARC6-4K1926

USB 2.0 CONN





Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	USB2.0/USB3.0	1A

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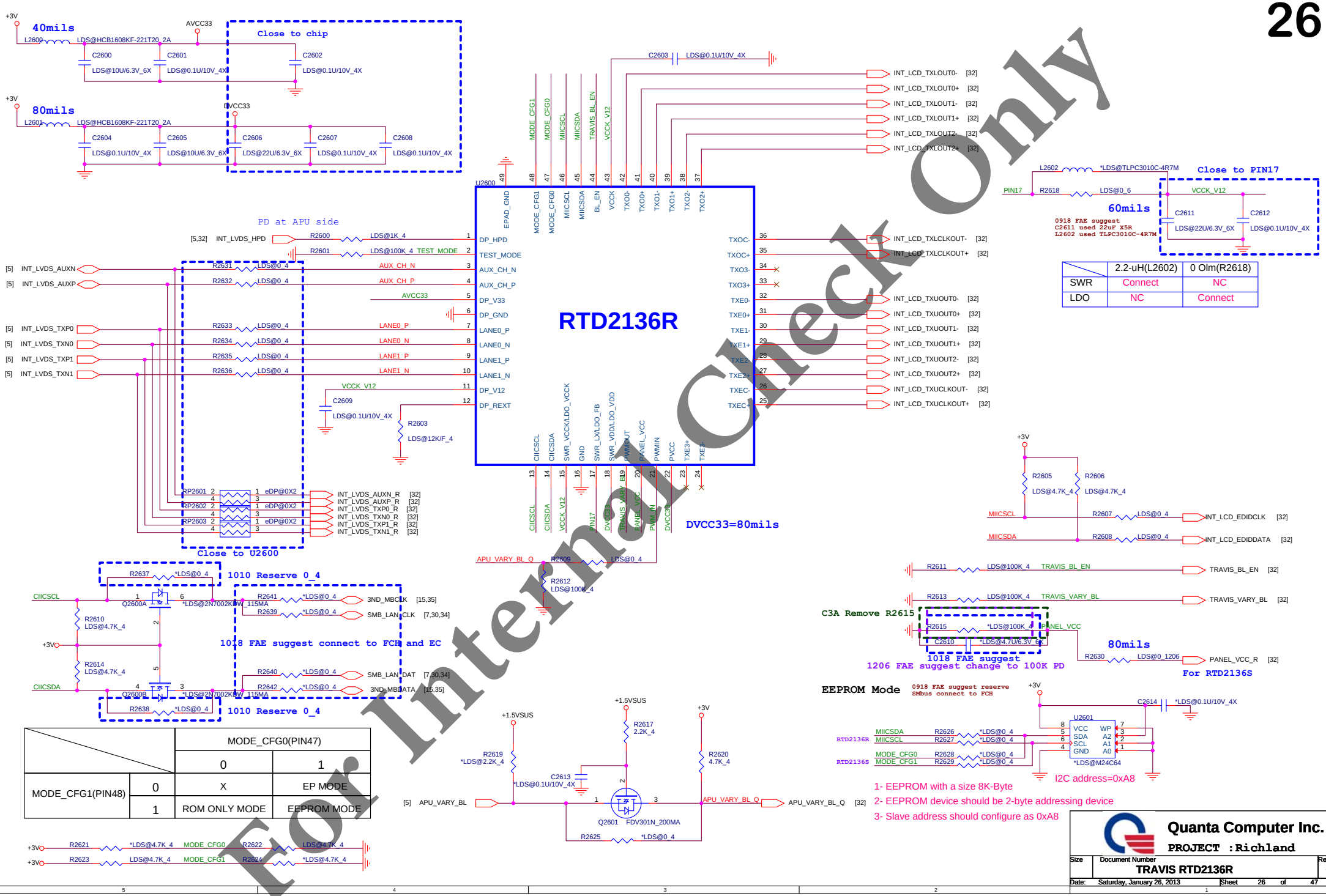

	2.2-uH(L2602)	0 Olm(R2618)
SWR	Connect	NC
LDO	NC	Connect

	MODE_CFG0(PIN47)	
	0	1
MODE_CFG1(PIN48) 0	X	EP MODE
MODE_CFG1(PIN48) 1	ROM ONLY MODE	EEPROM MODE

Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	TRAVIS RTD2136R	1A
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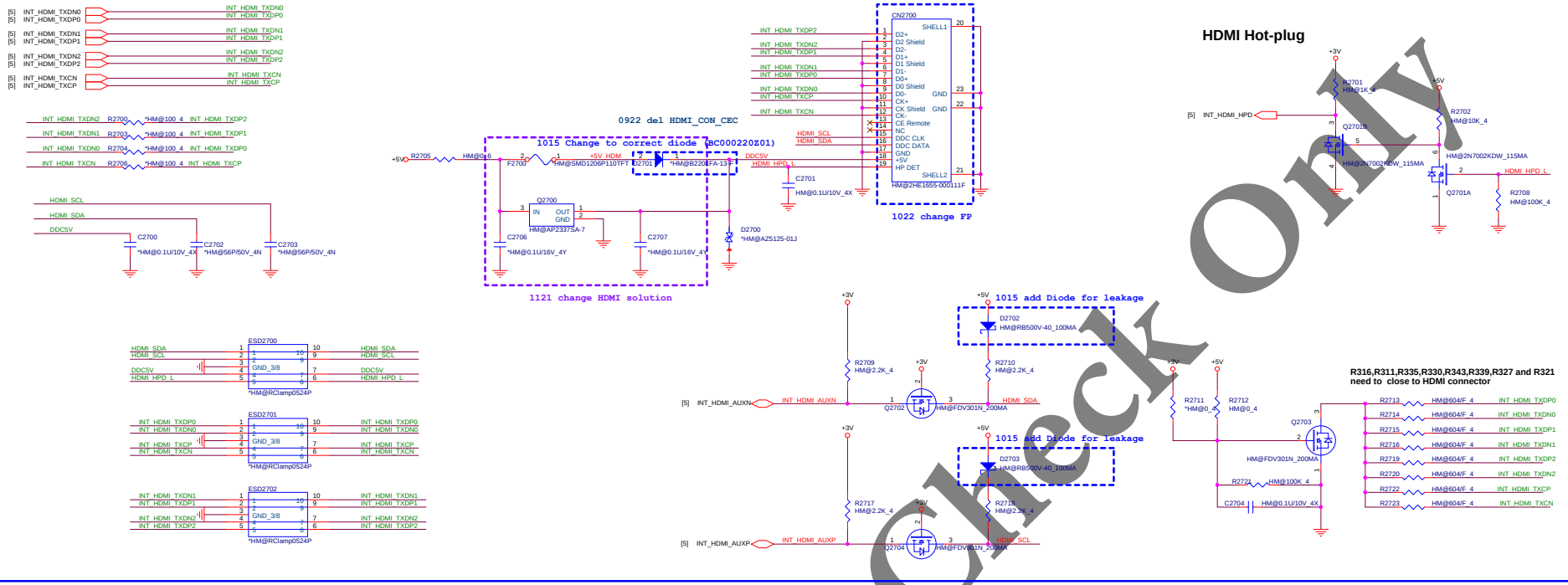
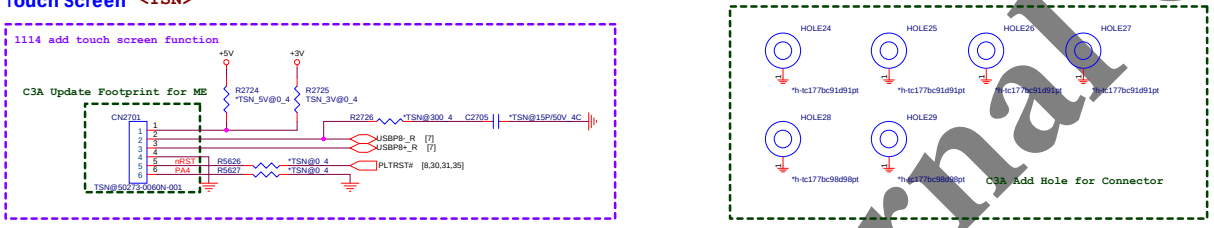
HDMI



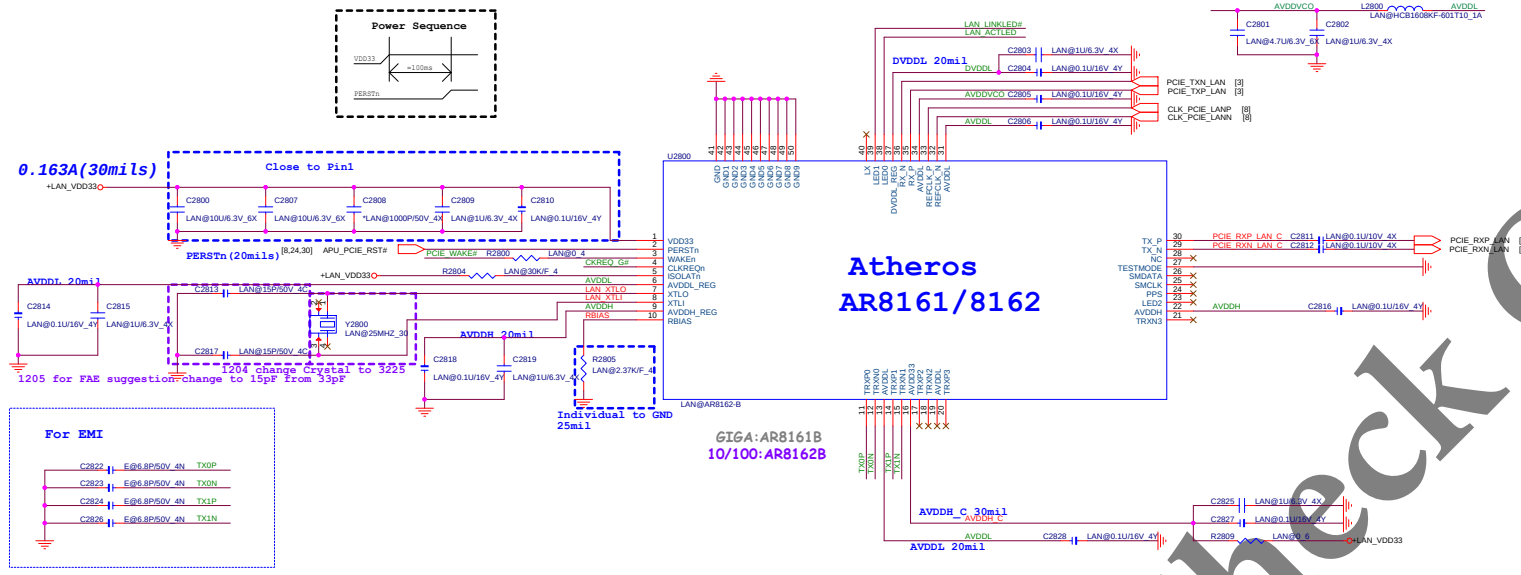
Touch Screen <TSN>



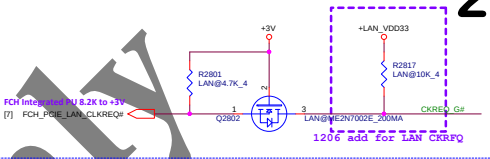
Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	HDMI/CEC	1A
Date: Saturday, January 26, 2013	Sheet 27 of 47	

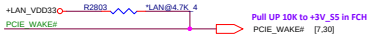
Atheros Lan <LAN> <LNG>



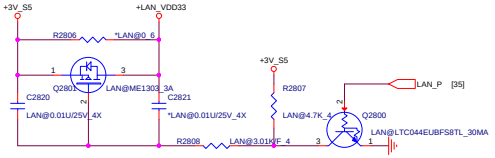
<LAN> <LNG> <LN1>



LAN-Wake up function <LAN>



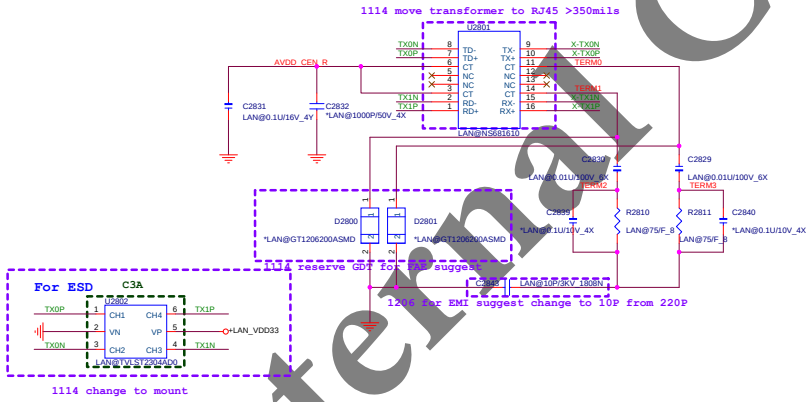
Wake on LAN function <LAN>



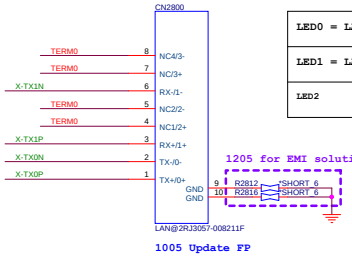
PLACE NEAR LAN IC SIDE <LAN> <LNG>

0920 FAE suggest remove 49.9K, 0.1u and 1000p

TRANSFORMER CONN <LAN> <LNG>



RJ45 <LAN> <LNG> <LN1>



LED0 = LAN_ACTLED	1	High core voltage(default=1)
	0	Low core voltage
LED1 = LAN_LINKLED#	1	Switch mode regulator (SWR) select
	0	Linear regulator (LDO) select
LED2	1	25 MHz external clock input
	0	48 MHz external clock input

Power on Strapping pin

Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	ATHEROS LAN (AR8152B)	1A
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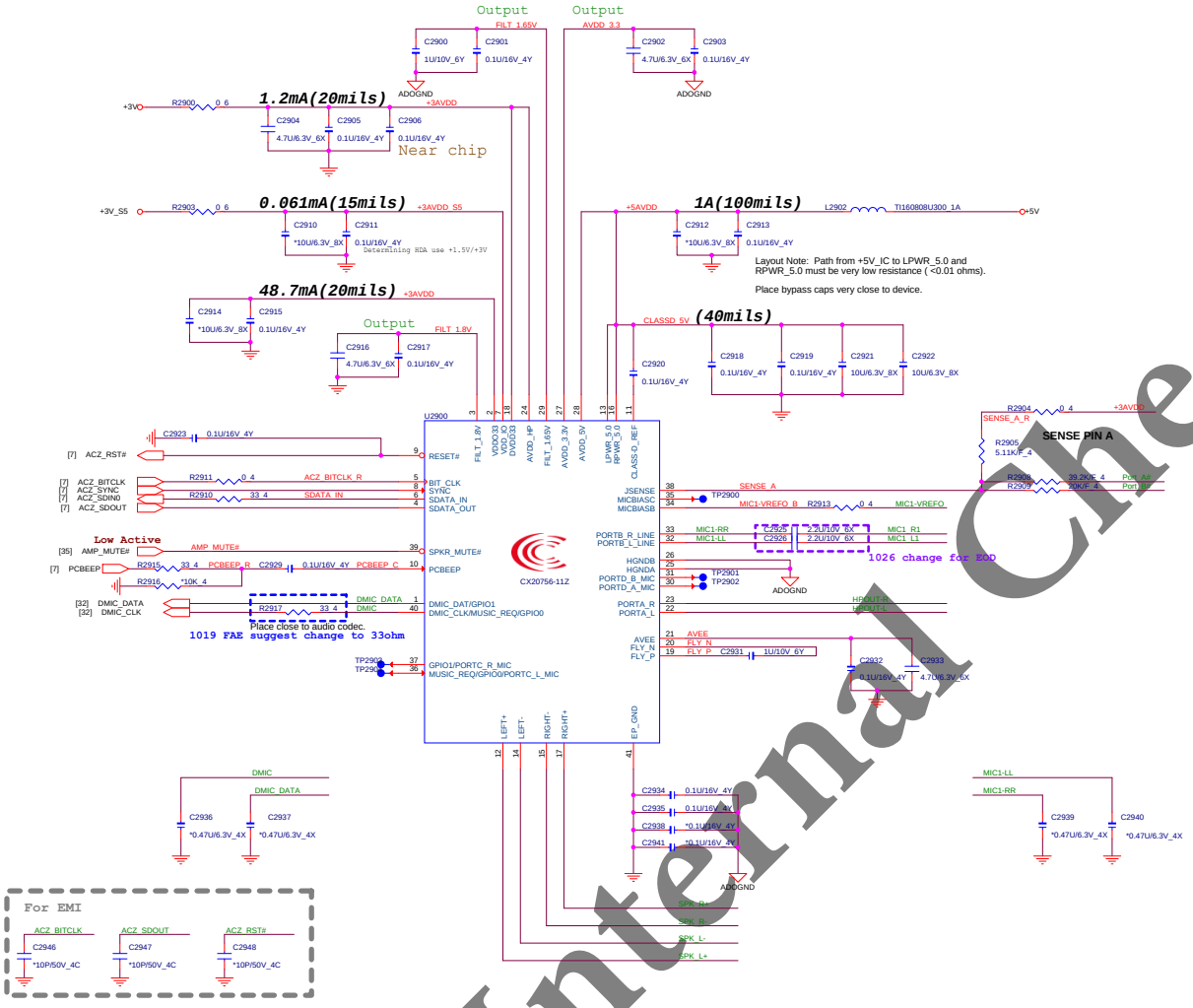
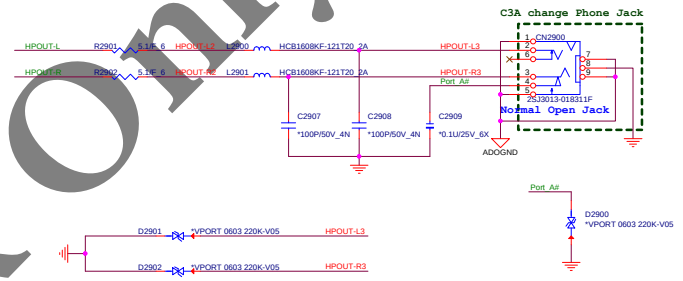
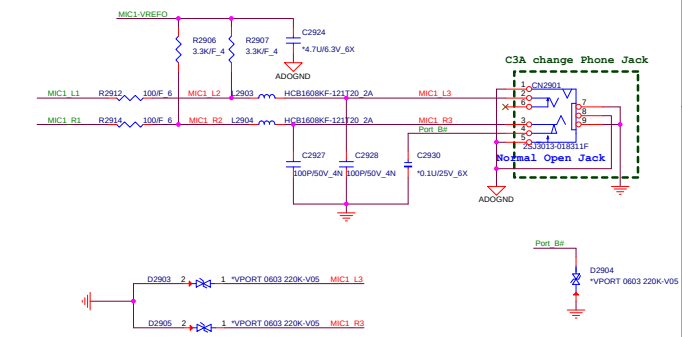
Codec (CX20756-11Z) <ADO> <EMI>



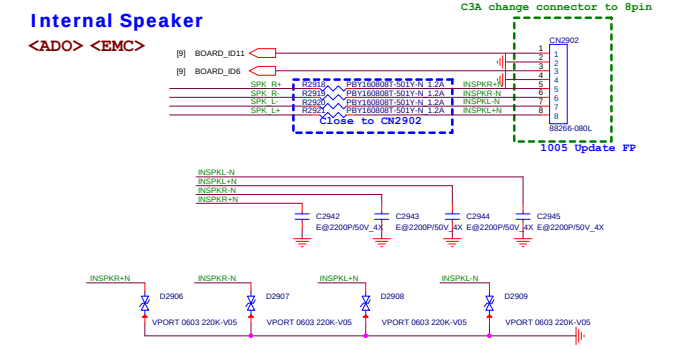
HP <ADO> <EMC>



External MIC <ADO> <EMC>



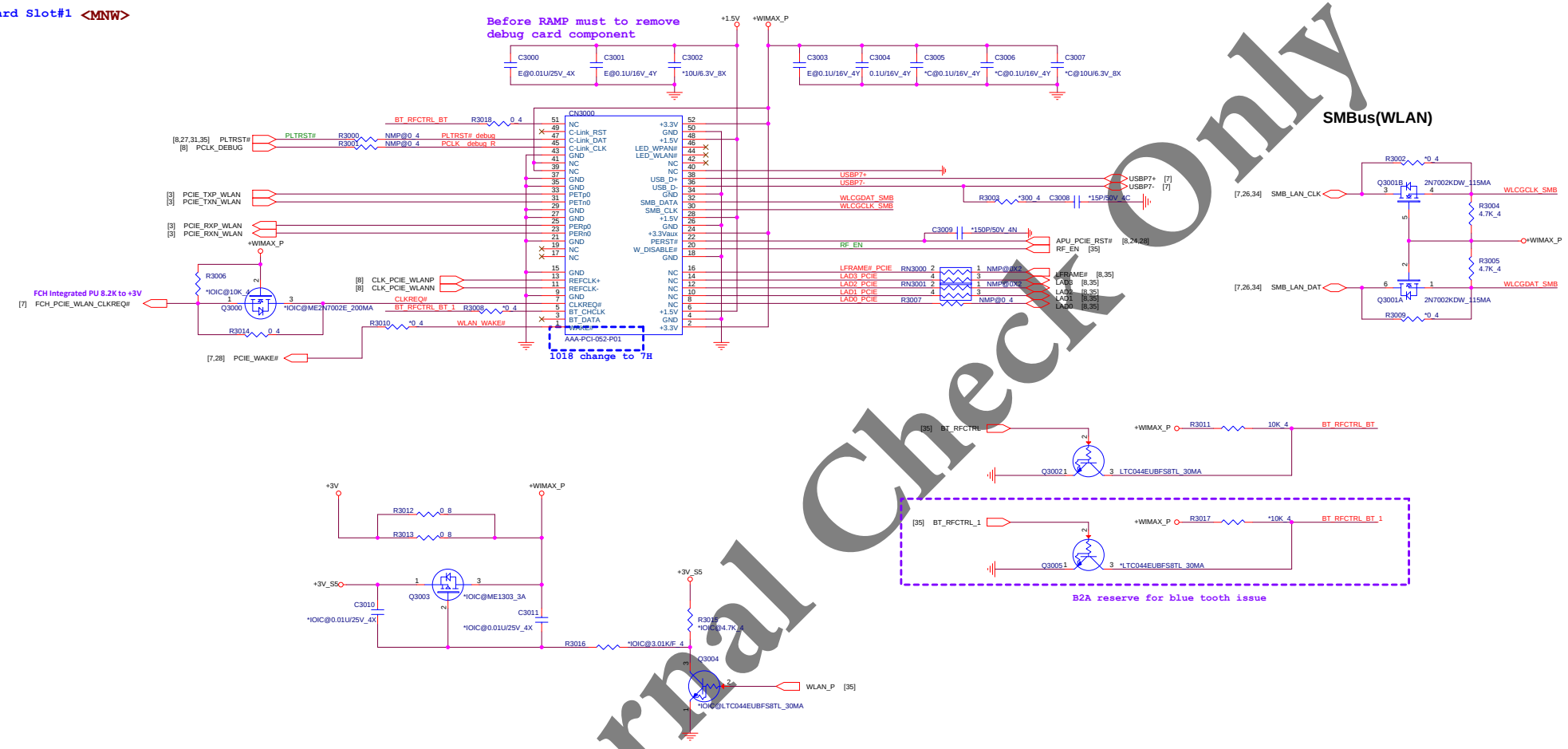
Internal Speaker <ADO> <EMC>



Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	AUDIO CODEC (CX20756-11Z)	1A
Date: Saturday, January 26, 2013	Sheet 29 of 47	

MINI Card Slot#1 <MNW>
(WiFi)



Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	MINI CARD	1A

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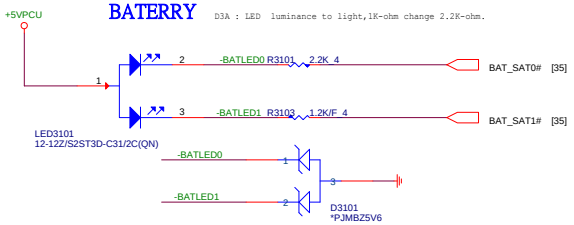
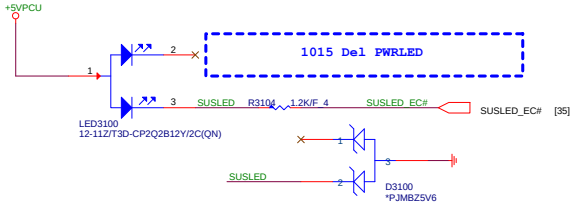
BATERRY

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

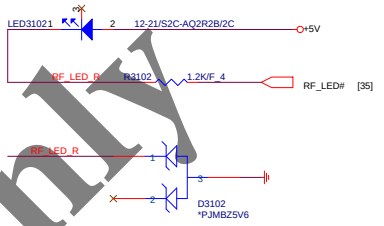


LED POWER

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

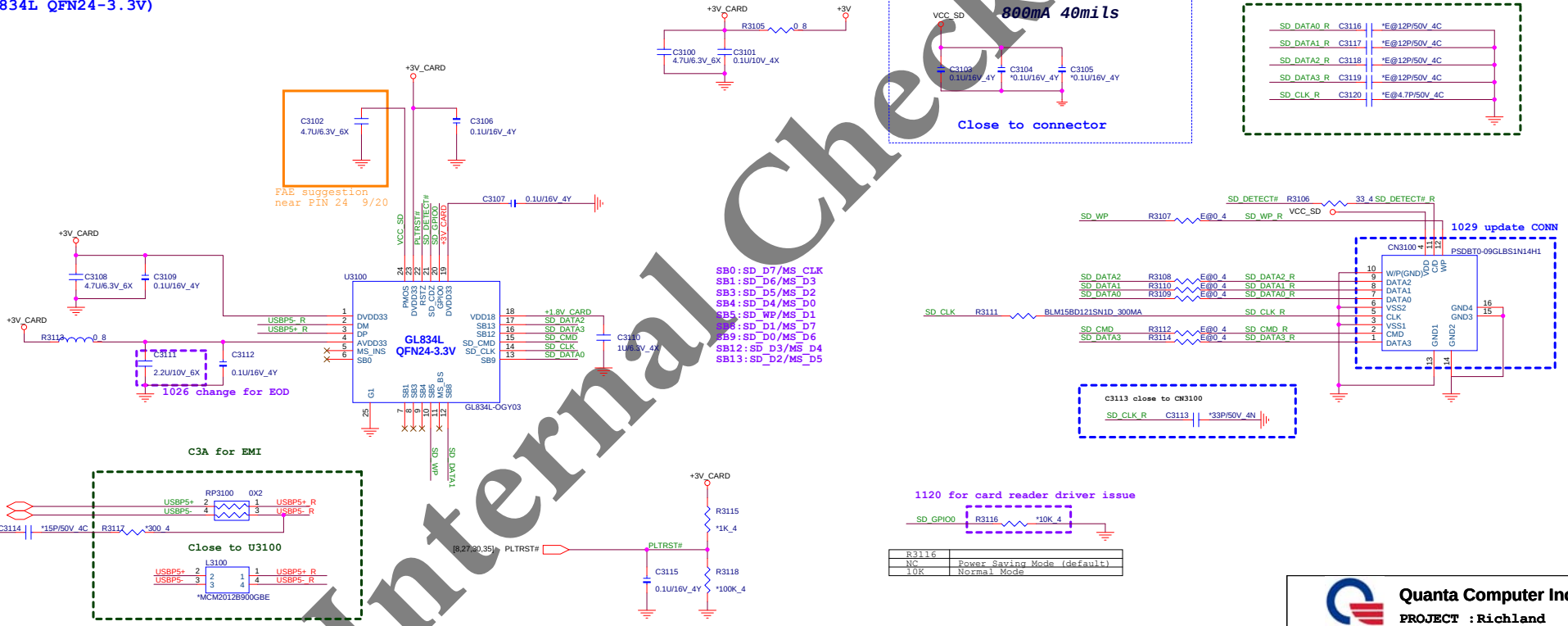


RF LED



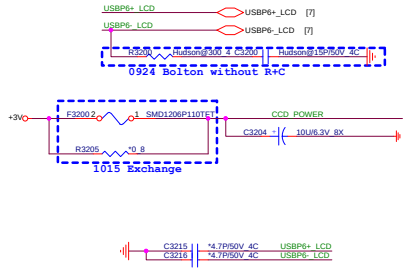
2 IN 1 CARD READER (Type: MS/SD) <MMC>

Card Reader (GL834L QFN24-3.3V)

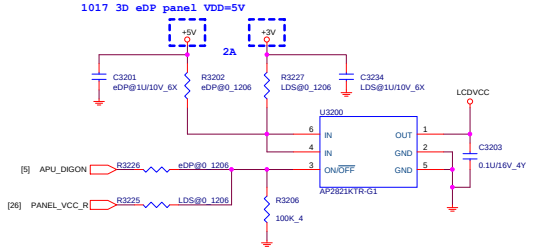


Quanta Computer Inc.		
PROJECT : Richland		
Size	Document Number: CARD READER/LED	Rev: 1A
Date: Saturday, January 26, 2013	Sheet 31 of 47	

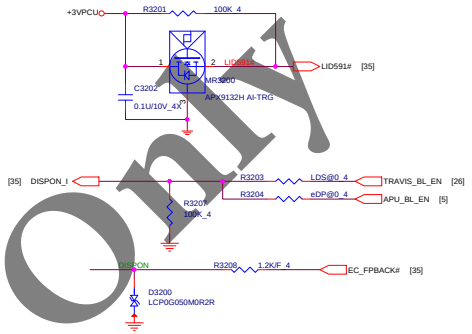
CCD [CCD]



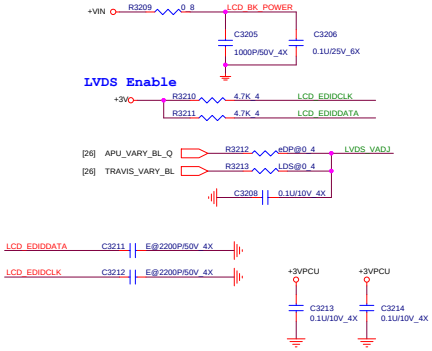
LCD POWER SWITCH <LDS>

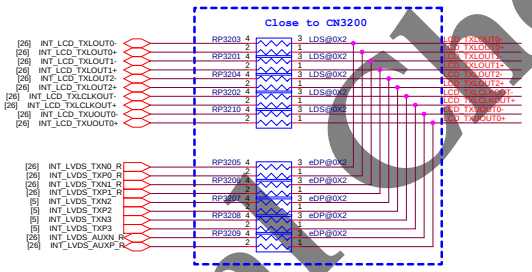


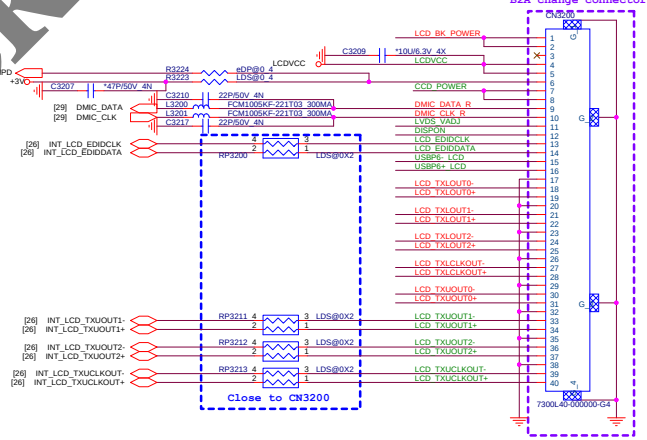
HALL SENSOR&BACK LIGHT SWITCH <HSR>



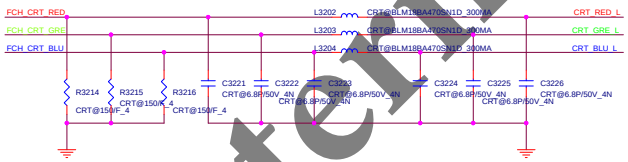
LCD Panel Module [LDS]

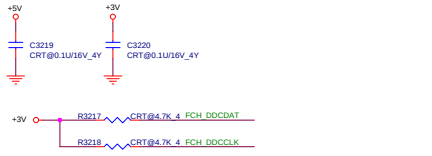


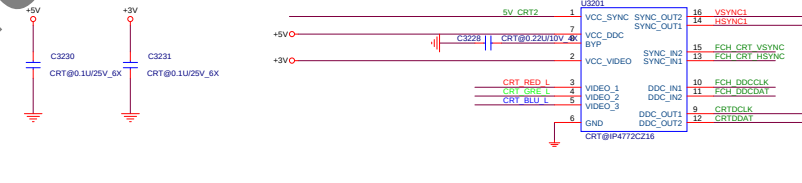




CRT [CRT]



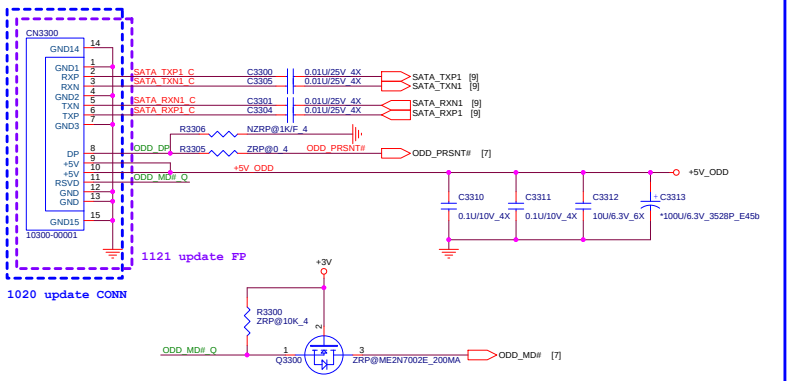




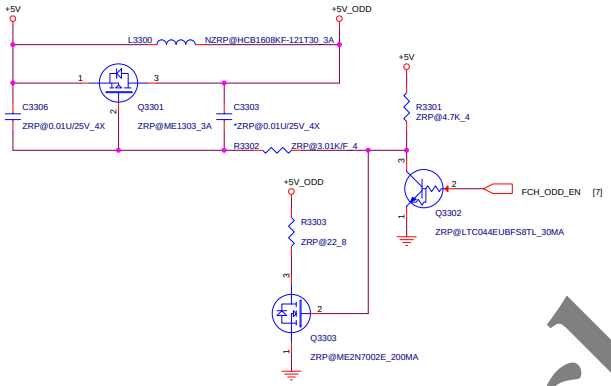
Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	LVDS/CCD/DRT	1A
Date: Saturday, January 26, 2013	Sheet 32 of 47	

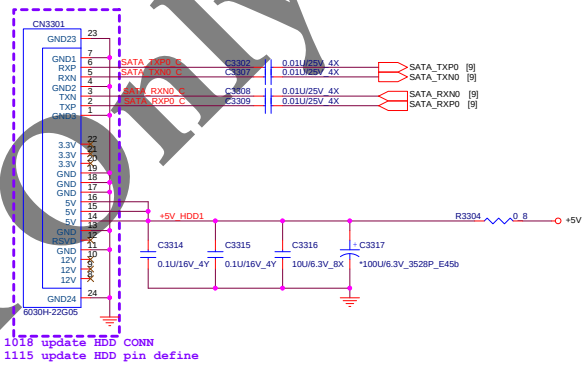
SATA ODD [ODD]



ODD Zero power <OZP>



SATA HDD [HDD]



3D-LDO Power <GSR>

3D-u-micro P <GSR>

3D-SMBus <GSR>

3D-Sensor IC <GSR>

Quanta Computer Inc.
PROJECT :Richland

Size	Document Number	Rev
	HDD/ODD	1A
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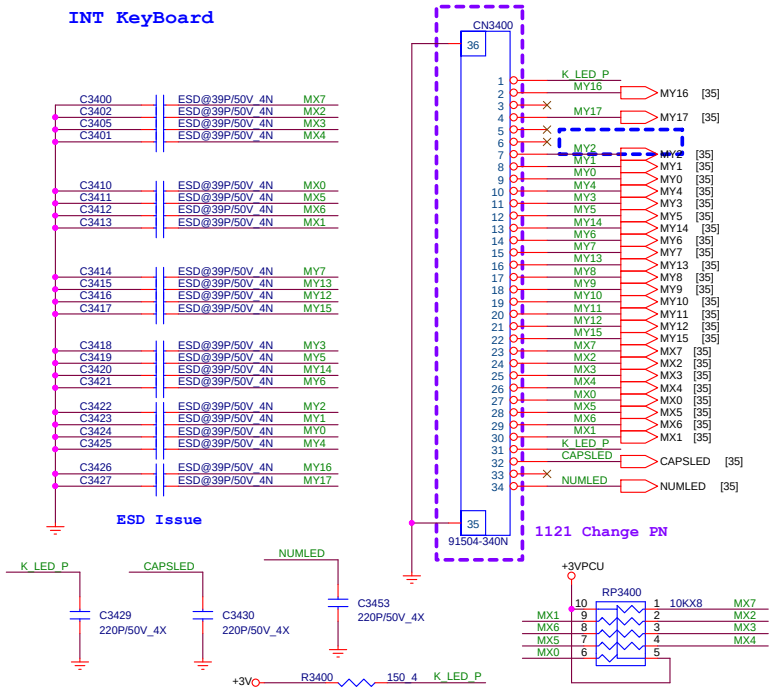
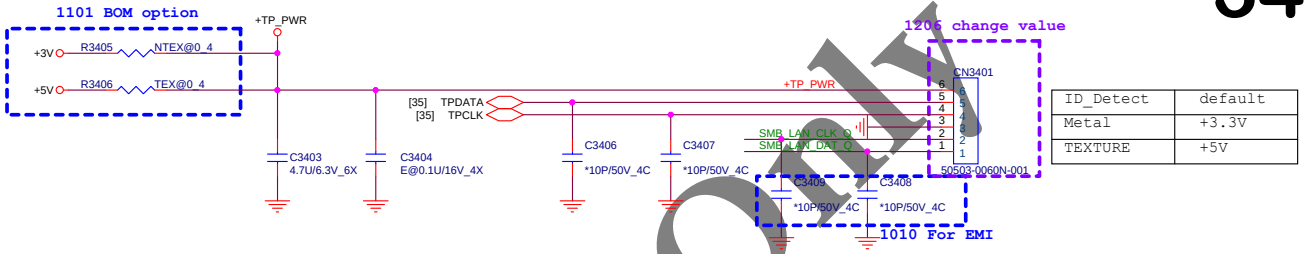
KEY BOARD Connector <KBC> <EMI>

INT KeyBoard

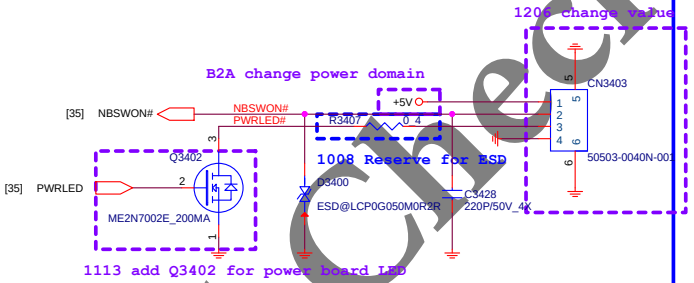


TOUCH PAD BOARD <TPD> <EMI>

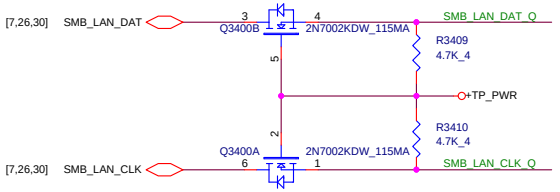


ID_Detect	default
Metal	+3.3V
TEXTURE	+5V

Power Board (UIF) <PSW>

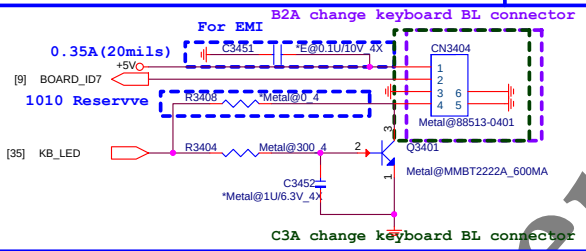


TP board <TPD>

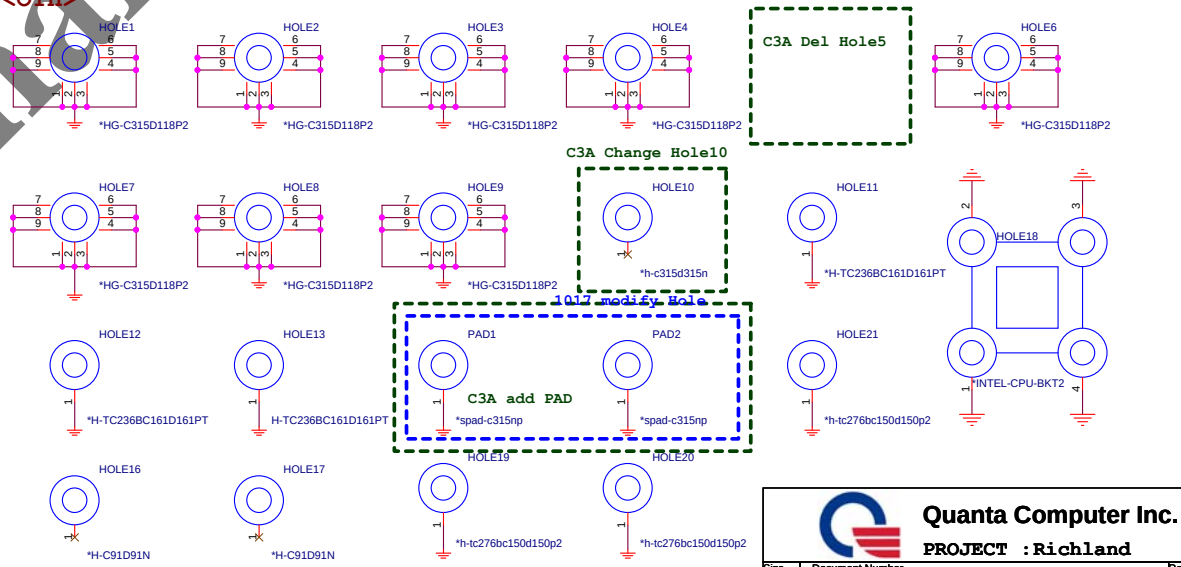


KEY BOARD LED

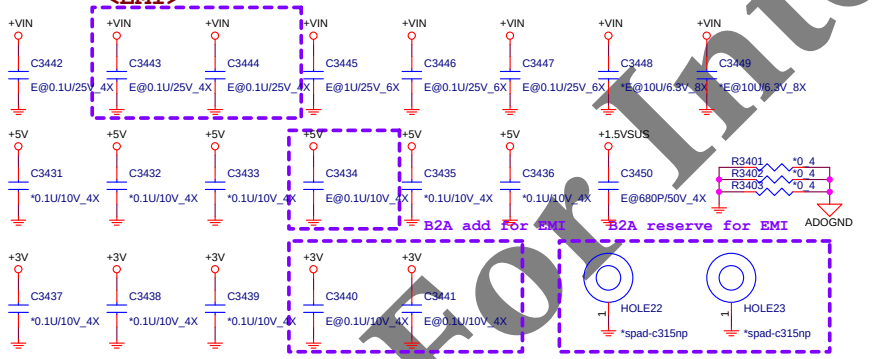
<KBP> <EMI>



HOLE <OTH>



EMI PAD <EMI> B2A add for EMI



Quanta Computer Inc.

PROJECT :Richland

Size	Document Number	Rev
	KBC/TP/FP CONN.	1A

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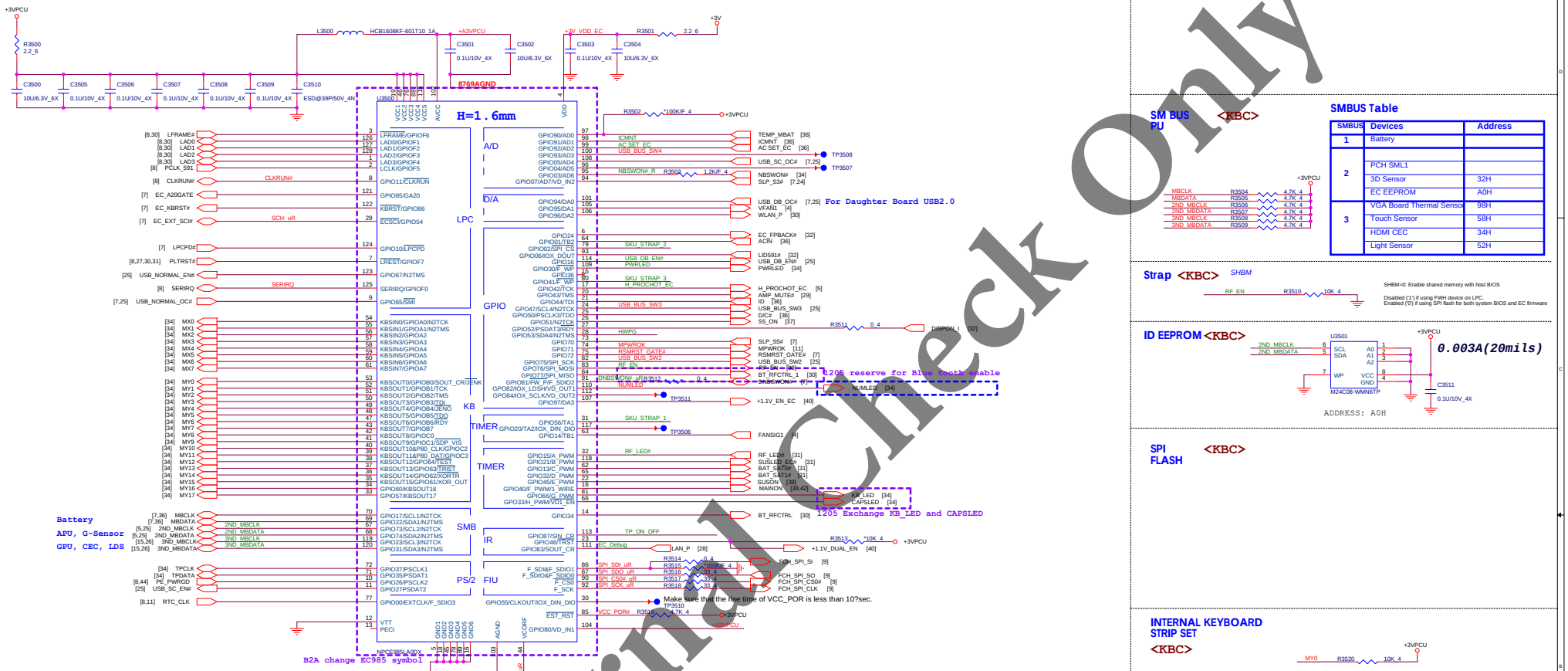
EC <KBC>



SKU_STRAP_1(GPIO56)	SKU_STRAP_2(GPIO02)	SKU_STRAP_3(GPIO41)	SKU
0	0	0	Kabini UMA
0	0	1	Kabini DIS
0	1	0	Richland UMA
0	1	1	Richland DIS
1	0	0	Brazos UMA
1	0	1	Brazos DIS

SM BUS PU <KBC>

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

Strap <KBC> SHBM

SHBM=0: Enable shared memory with host BIOS

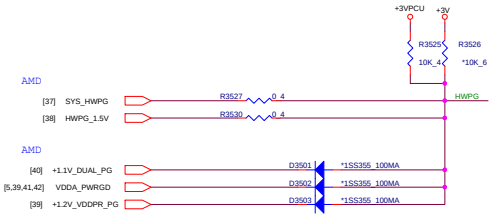
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID EEPROM <KBC>

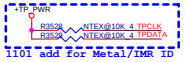
SPI FLASH <KBC>

INTERNAL KEYBOARD STRIP SET <KBC>

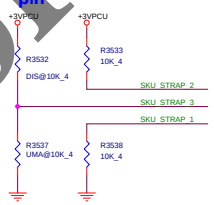
HWPG circuit <KBC>



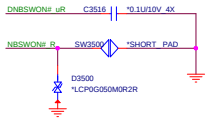
TP interface PU <KBC>



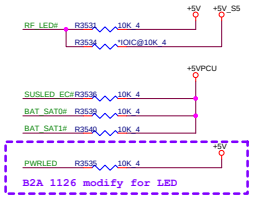
SKU strap pin <KBC>



Power Button <KBC>



LED PU/PD <LED>



Quanta Computer Inc.	PROJECT : Richland		
Size	Document Number		Rev
	EC NPCE795CA0DX		1A
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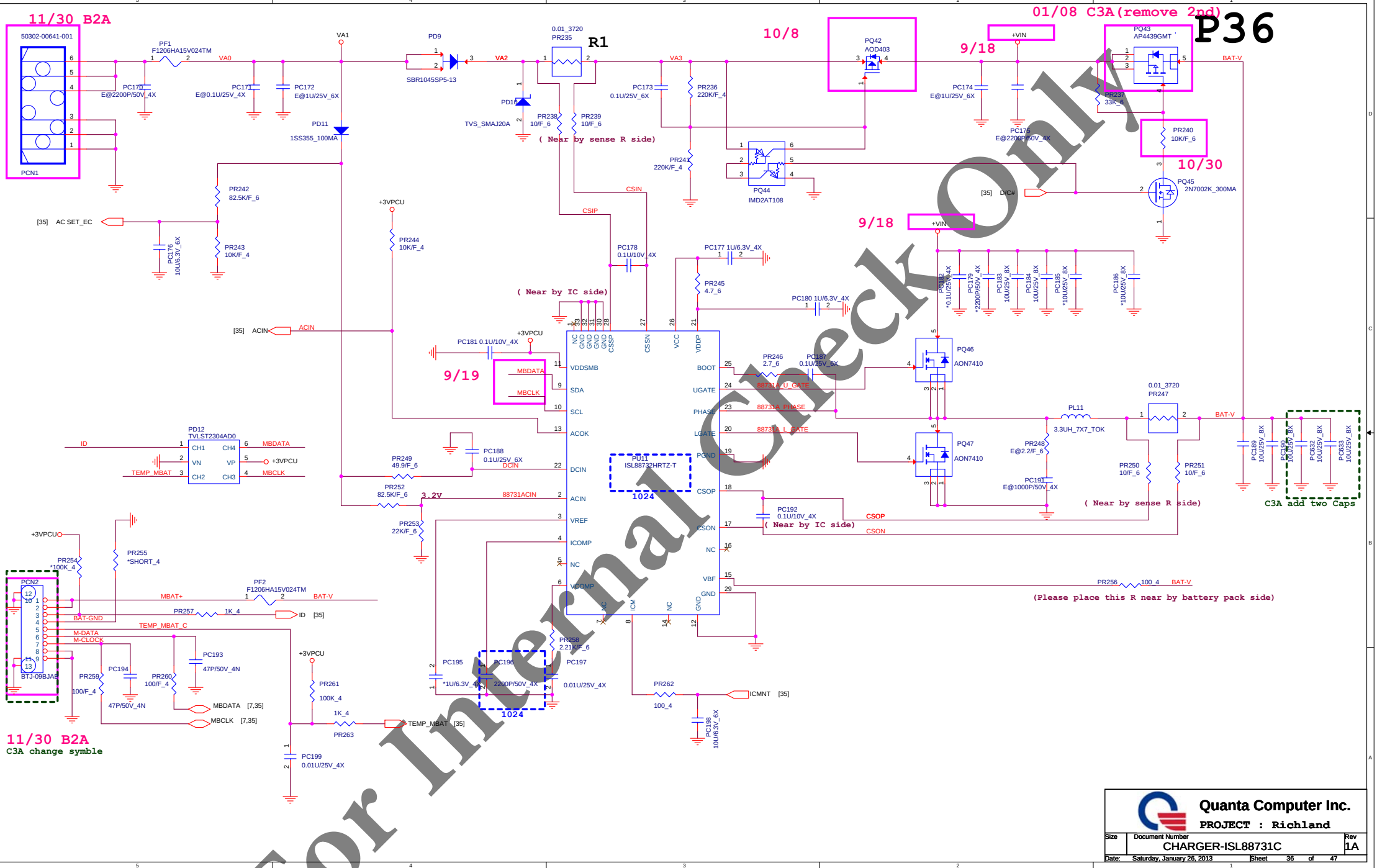
11/30 B2A
01/08 C3A(remove 2nd)
P36
10/8
9/18
10/30
9/19
50302-00641-001
PCN1
PF1
F1206HA15V024TM
VA0
VA1
VA2
VA3
PD9
SBR1045SP5-13
PD10
TVS_SMAJ20A
PD11
1SS355_100MA
0.01_3720
PR235
R1
PR238
10/F_6
PR239
10/F_6
(Near by sense R side)
PC170
E@2200P/50V_4X
PC171
E@0.1U/25V_4X
PC172
E@1U/25V_6X
PC173
0.1U/25V_6X
PR236
220K/F_4
PR241
220K/F_4
PQ42
AOD403
PQ44
IMD2AT108
+VIN
PC174
E@1U/25V_6X
PC175
E@2200P/50V_4X
PQ43
AP4439GMT
BAT-V
PR237
33K_6
PR240
10K/F_6
PQ45
2N7002K_300MA
[35] D/C#
PR242
82.5K/F_6
[35] AC SET_EC
PC176
10U/6.3V_6X
PR243
10K/F_4
+3VPCU
PR244
10K/F_4
CSIN
CSIP
PC178
0.1U/10V_4X
PC177 1U/6.3V_4X
PR245
4.7_6
PC180 1U/6.3V_4X
(Near by IC side)
[35] ACIN
ACIN
PC181 0.1U/10V_4X
MBDATA
MBCLK
PU11
ISL88732HRTZ-T
1024
NC
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
IMN
PR246
2.7_6
PC187
0.1U/25V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ46
AON7410
PQ47
AON7410
PL11
3.3UH_7X7_TOK
0.01_3720
PR247
PR248
E@2.2/F_6
PC191
E@1000P/50V_4X
PR250
10/F_6
PR251
10/F_6
(Near by sense R side)
C3A add two Caps
PC188
0.1U/25V_6X
PR249
49.9/F_6
PR252
82.5K/F_6
3.2V
88731ACIN
PR253
22K/F_6
PC192
0.1U/10V_4X
(Near by IC side)
CSOP
CSON
PR256
100_4
BAT-V
(Please place this R near by battery pack side)
PD12
TVLST2304AD0
ID
TEMP_MBAT
MBDATA
+3VPCU
MBCLK
PR254
*100K_4
PR255
*SHORT_4
PCN2
BTJ-09BJAB
PF2
F1206HA15V024TM
MBAT+
BAT-V
PR257
1K_4
ID [35]
BAT-GND
TEMP_MBAT_C
M-DATA
M-CLOCK
PC193
47P/50V_4N
PR259
100/F_4
PC194
47P/50V_4N
PR260
100/F_4
MBDATA [7,35]
MBCLK [7,35]
PR258
2.21K/F_6
PC195
*1U/6.3V_4X
PC196
2200P/50V_4X
PC197
0.01U/25V_4X
1024
PR262
100_4
ICMNT [35]
PC198
10U/6.3V_6X
PR261
100K_4
1K_4
PR263
TEMP_MBAT [35]
PC199
0.01U/25V_4X
11/30 B2A
C3A change symble
For Internal Check Only
Quanta Computer Inc.
PROJECT : Richland
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Document Number
CHARGER-ISL88731C
Rev
1A
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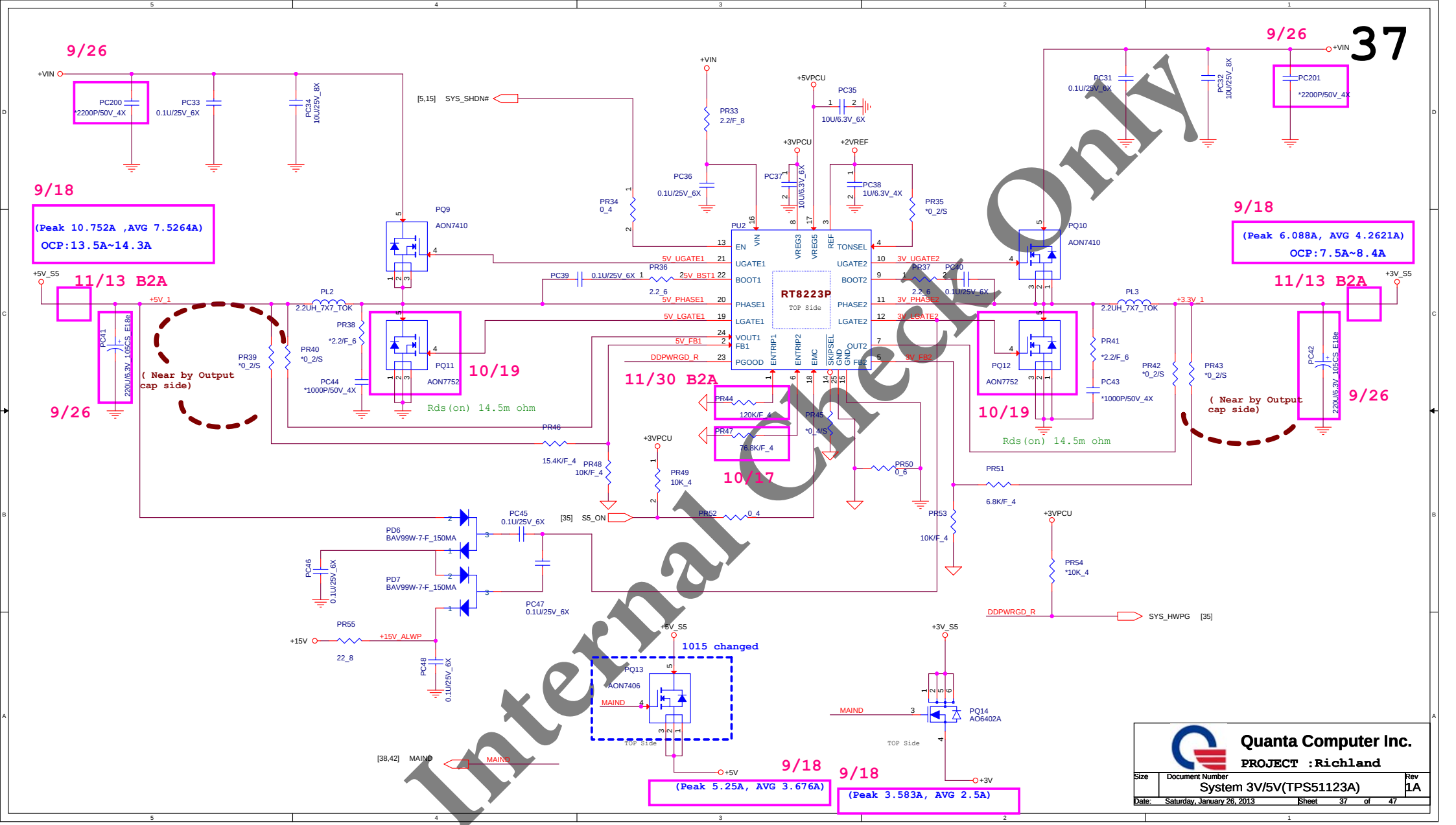

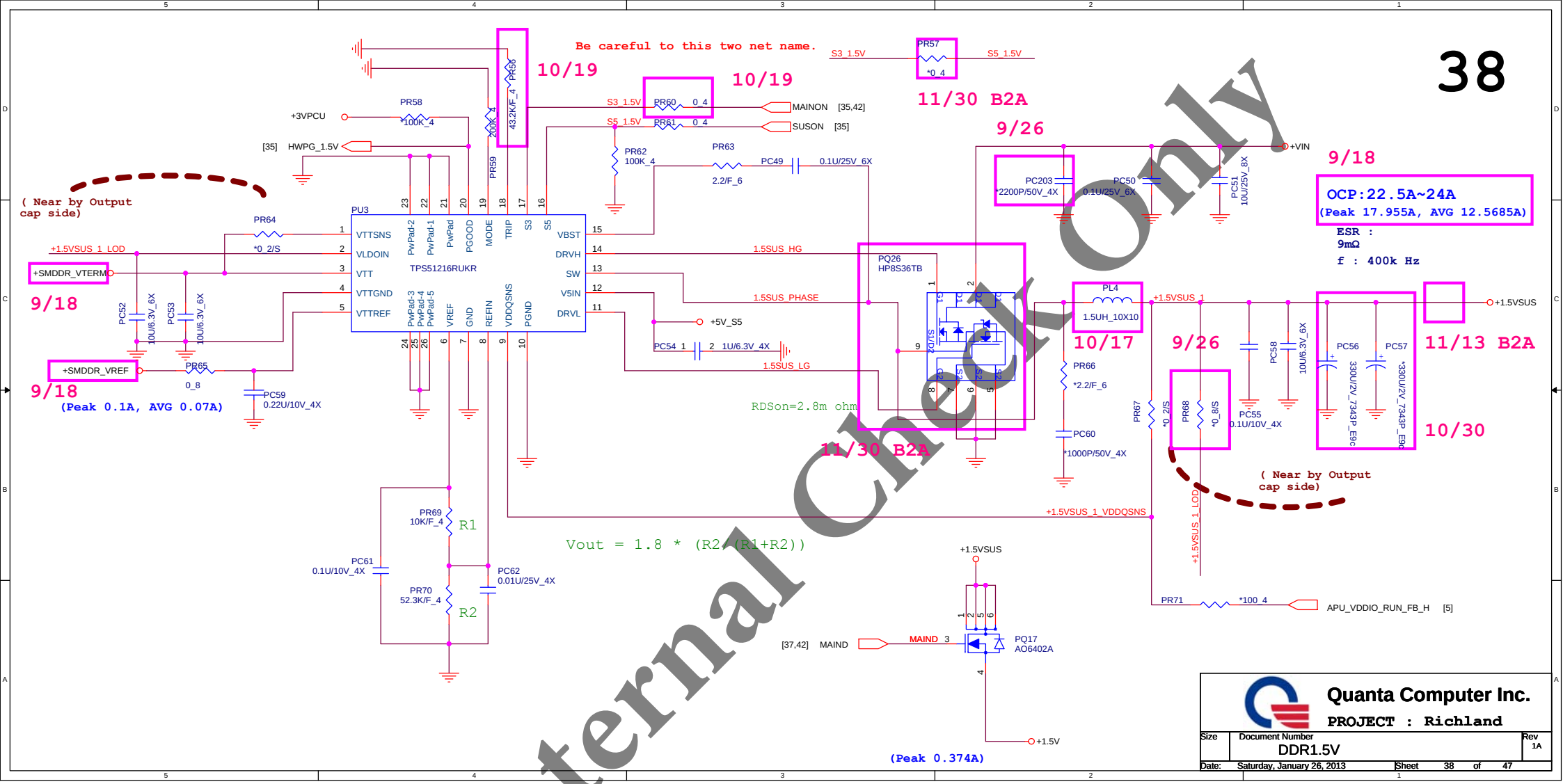

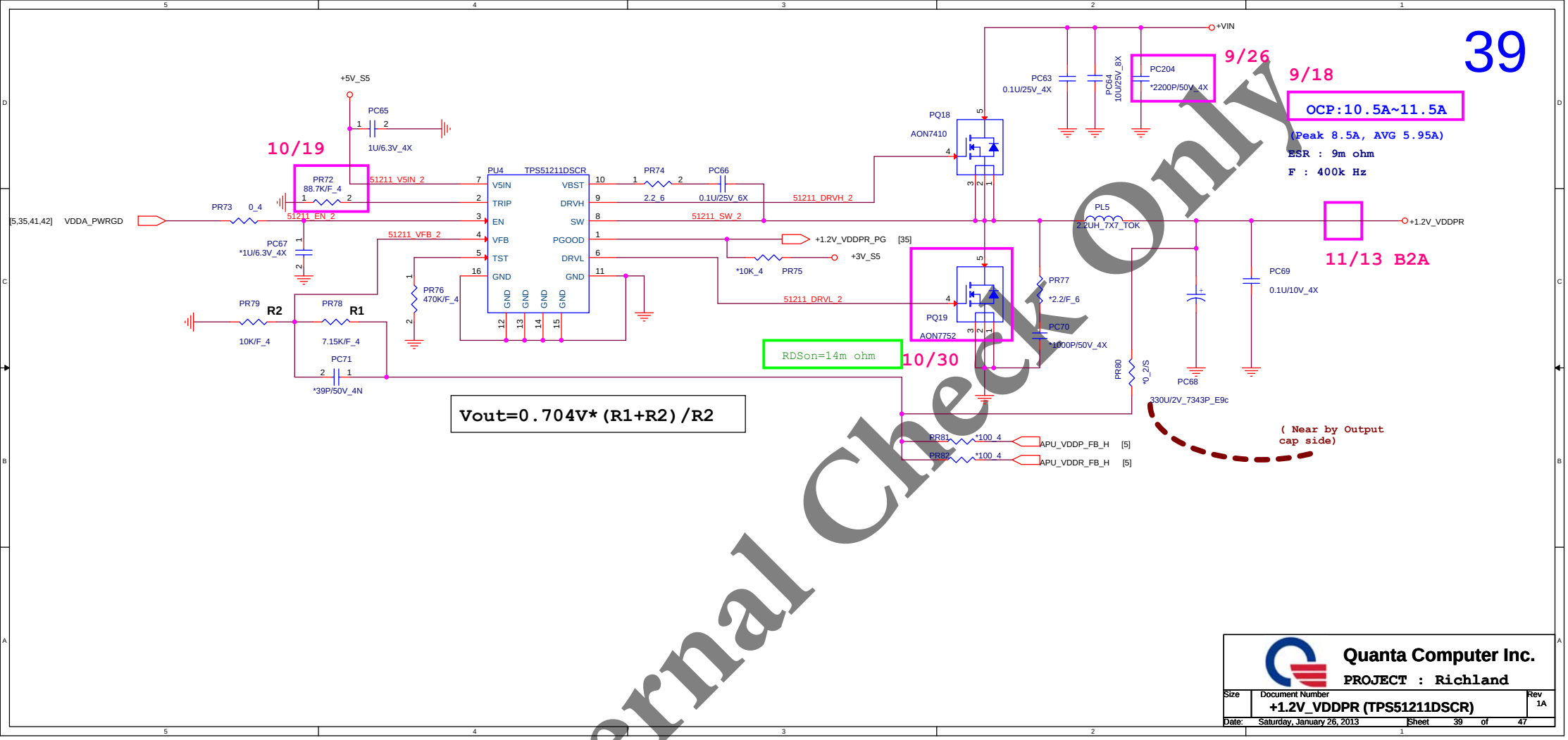

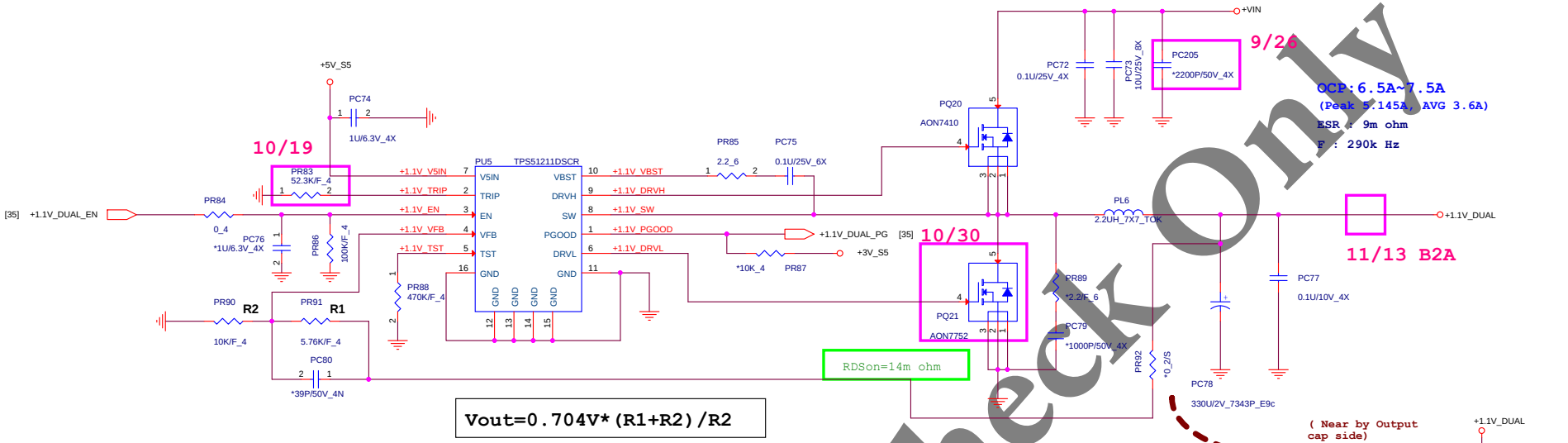

Quanta Computer Inc.		
PROJECT : Richland		
Size	Document Number: +1.1V_DUAL (TPS51211DSCR)	Rev: 1A
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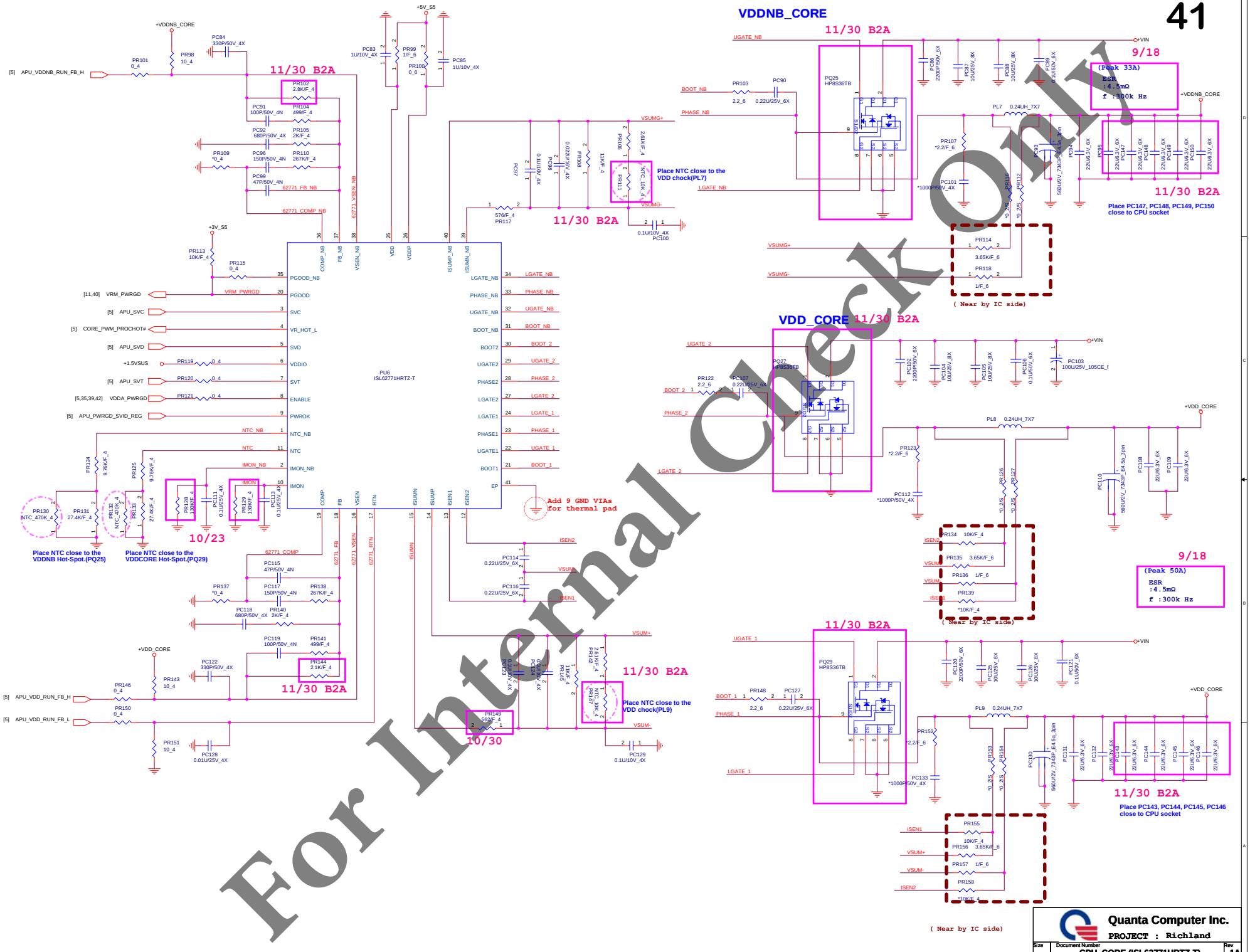

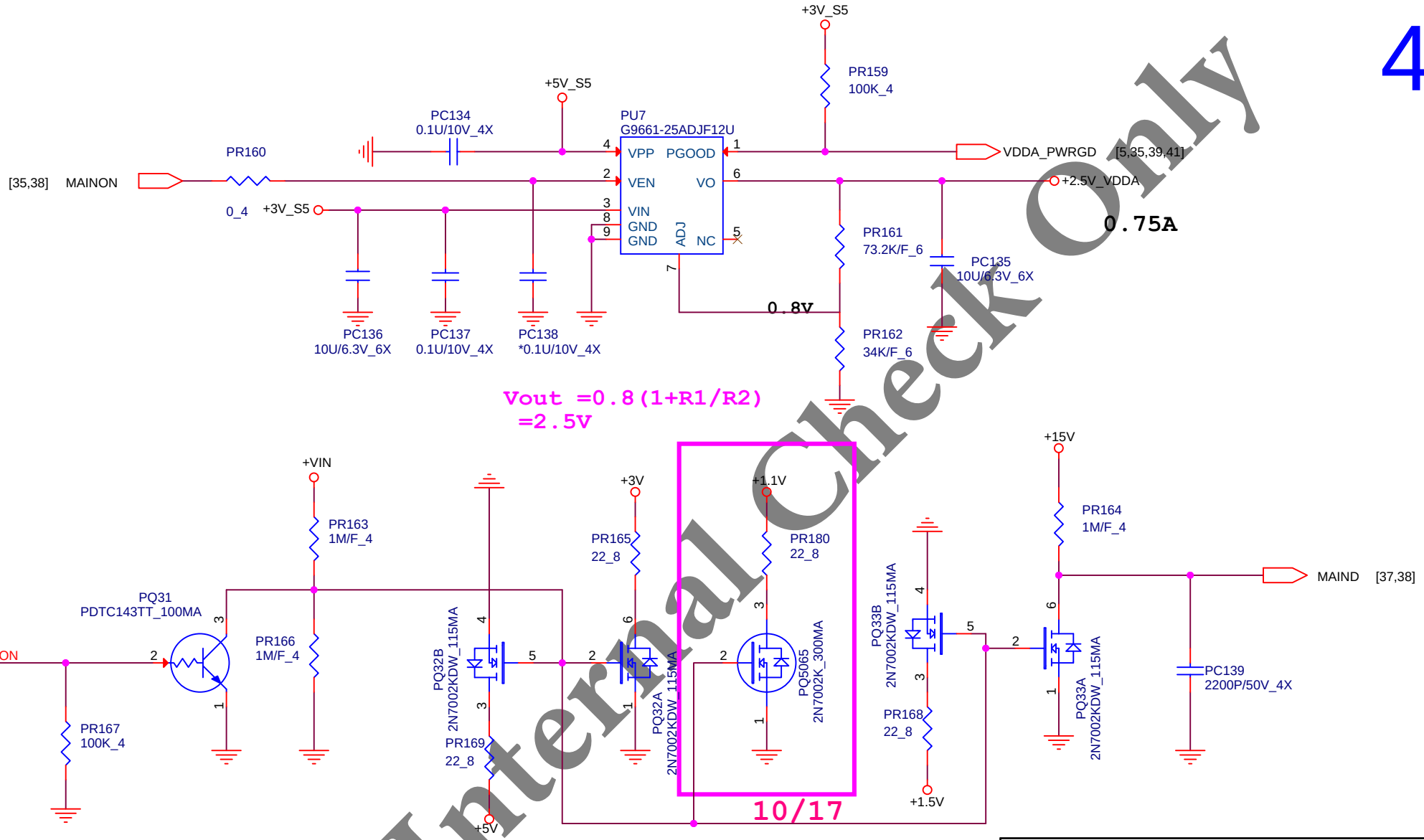

Quanta Computer Inc.

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	DISCHARGE	1A

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Int_VGA [PWM]

Mars VDDC VID TABLE

VDDC (V)	GFX_CORE_CNTRL4 (VID5) (GPIO_6)	GFX_CORE_CNTRL3 (VID4) (GPIO_30)	GFX_CORE_CNTRL2 (VID3) (GPIO_29)	GFX_CORE_CNTRL1 (VID2) (GPIO_20)	GFX_CORE_CNTRL0 (VID1) (GPIO_15)
1.125	0	1	1	1	1
1.100	1	0	0	0	0
1.075	1	0	0	0	1
1.050	1	0	0	1	0
1.025	1	0	0	1	1
1.000	1	0	1	0	0
0.975	1	0	1	0	1
0.950	1	0	1	1	0
0.925	1	0	1	1	1
0.900	1	1	0	0	0
0.875	1	1	0	0	1
0.850	1	1	0	1	0
0.825	1	1	0	1	1
0.800	1	1	1	0	0
0.775	1	1	1	0	1

12/03 B2A
10/16
11/30 B2A
12/03 B2A
01/08 C3A
10/16
11/30 B2A
10K NTC put close with Inductor
Parallel
11/09 B2A
10/22

Countinue current:14.7A
Peak current:21A
OCP:27A~28A

+VGPU_CORE

Quanta Computer Inc.
PROJECT : Richland
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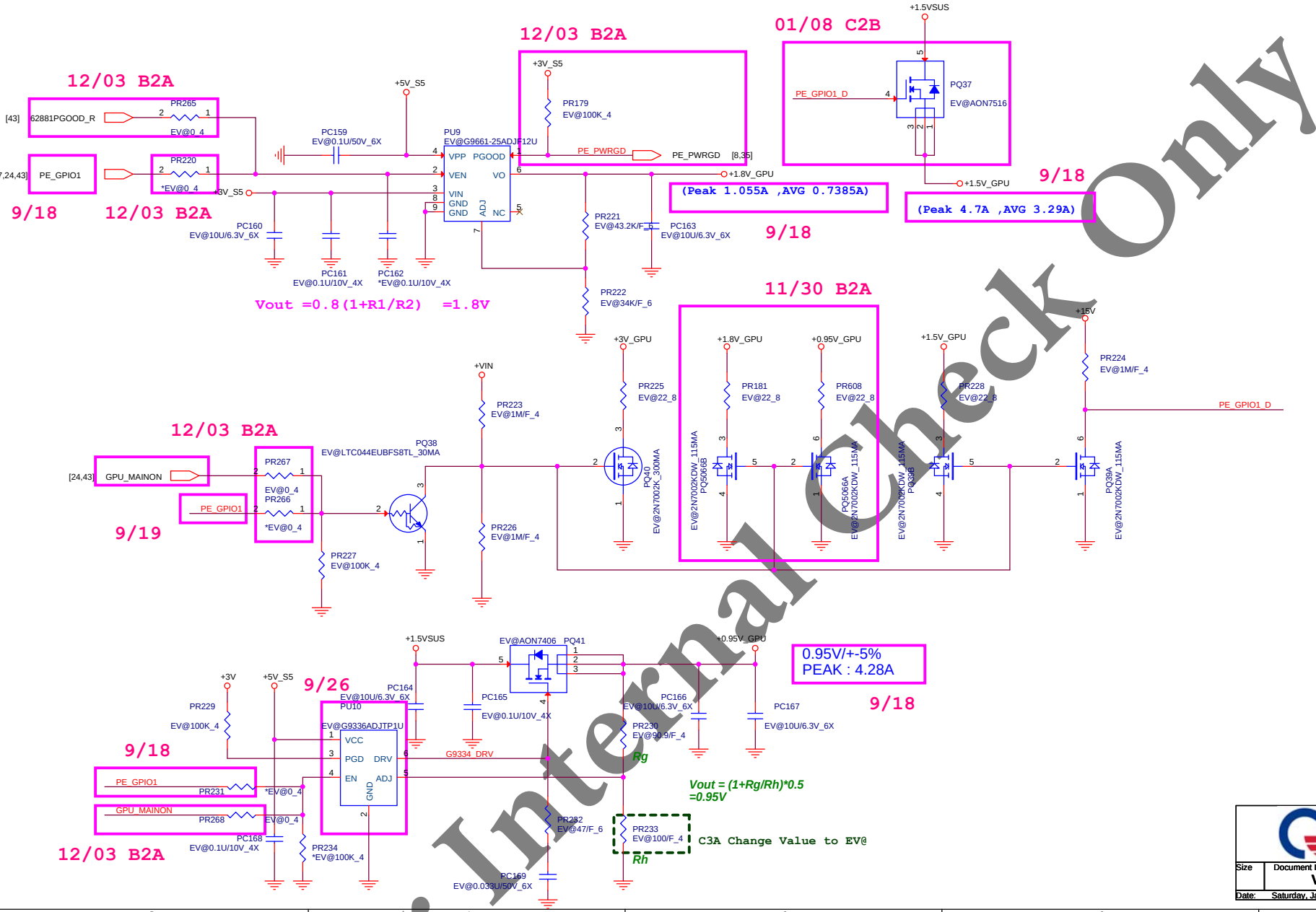

Quanta Computer Inc.
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Size	Document Number	Rev
	VGA_DIS	1A
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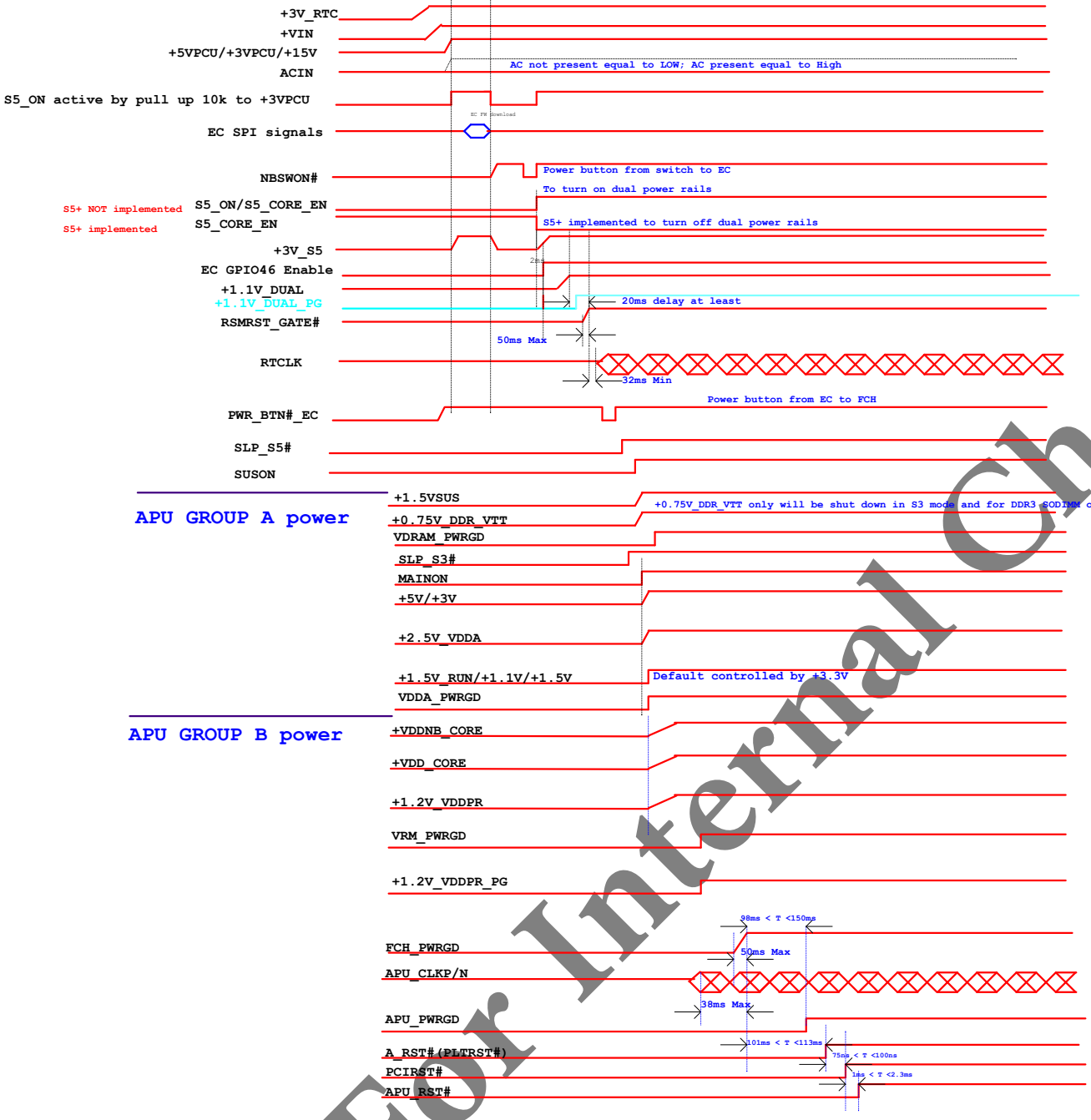
BD8/BD8D Power On Sequence: S5 > S0

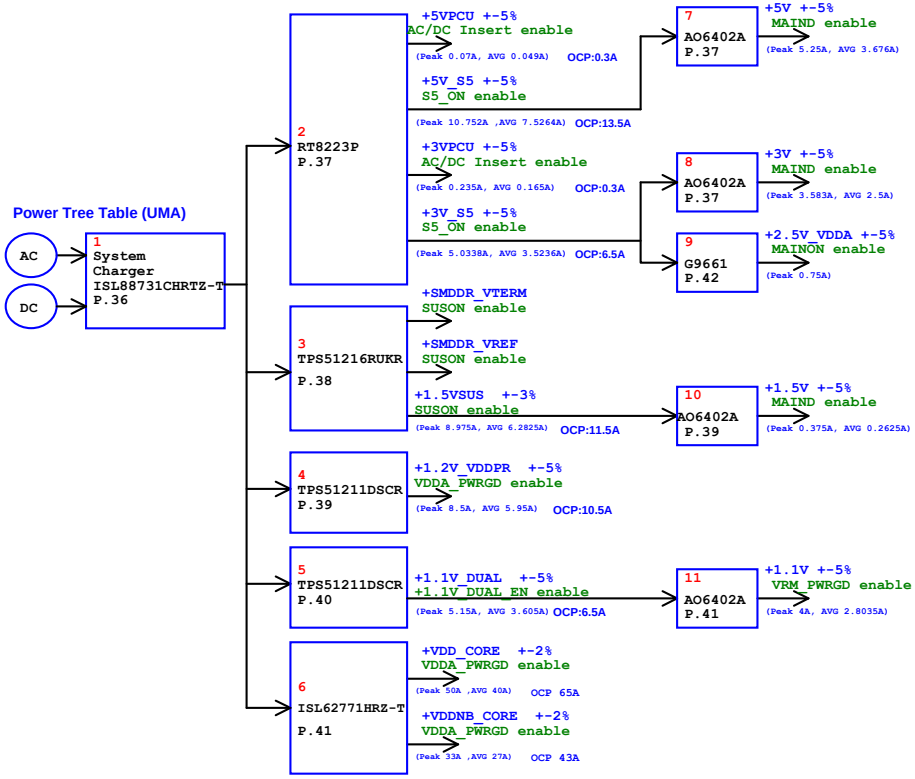


APU Power on sequence required:

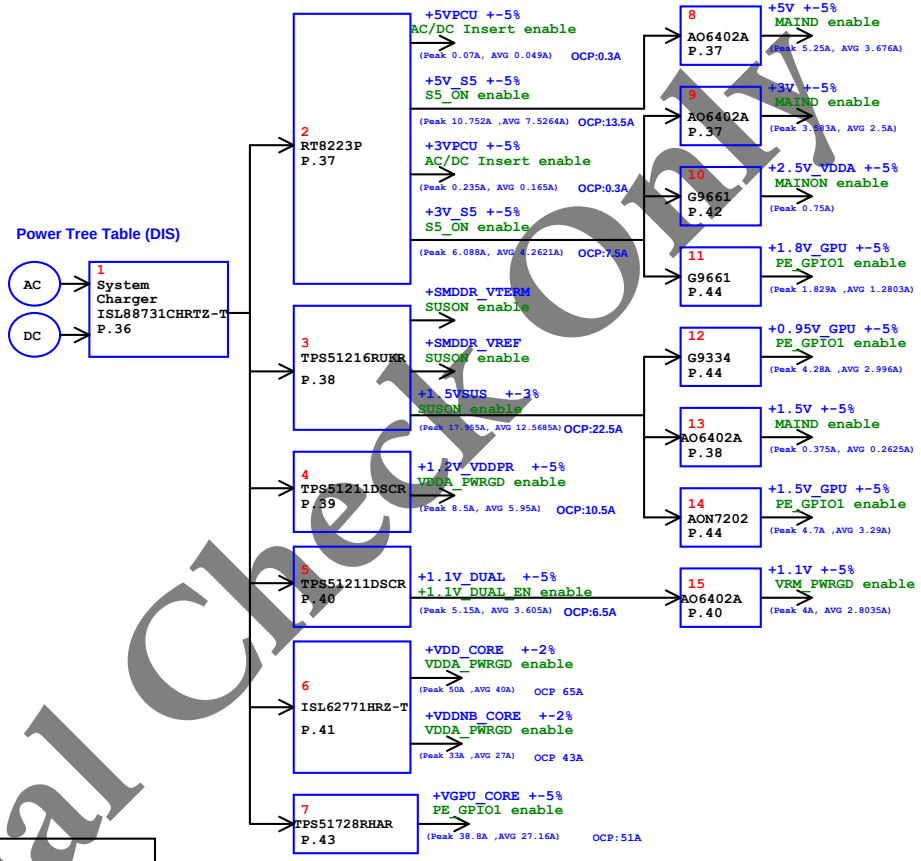
Llano APU:
1.Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR).

HUDSON-M2/M3:
1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Power Tree Table (UMA)



Power Tree Table (DIS)



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : Richland
Size | Document Number: POWER TREE TABLE | Rev: 1A
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Model	REV	CHANGE LIST
BY6D MB	A1A	

MODEL	BY6D	
PAGE	FROM	
1	A1A	
2	A1A	
3	A1A	
4	A1A	
5	A1A	
6	A1A	
7	A1A	
8	A1A	
9	A1A	
10	A1A	
11	A1A	
12	A1A	
13	A1A	
14	A1A	
15	A1A	
16	A1A	
17	A1A	
18	A1A	
19	A1A	
20	A1A	
21	A1A	
22	A1A	
23	A1A	
24	A1A	
25	A1A	
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27	A1A	
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36	A1A	
37	A1A	
38	A1A	
39	A1A	
40	A1A	
41	A1A	
42	A1A	
43	A1A	
44	A1A	
45	A1A	
46	A1A	

DOC NO. 204	PROJECT MODEL :	BY6D	APPROVED BY:		DATE:	2011/10/02
	PART NUMBER:		DRAWING BY:	Wei-Sheng	REVISON:	A1A

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