



Compal Confidential

Gx00/Gx00 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

AMD Mars XT / SUN Pro

2013-02-27

LA-9631P

REV: 1.0

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				Customer	LA-9631P	
				Date:	Wednesday, February 27, 2013	Sheet 1 of 60

Chief River

AMD MARS XT M2 128 bits
/ **SUN PRO M2 64 bits**

VRAM 512MB/1GB/2GB
MARS XT : DDR3 x 8
SUN PRO : DDR3 x 4

Page 23~32

PEG 8x
Gen2 / Gen3

Intel Processor Ivy Bridge

rPGA989
37.5mm x 37.5mm

Page 5~11

Memory Bus
Dual Channel

DDR3 1600MHz
DDR3 1333MHz
DDR3 1066MHz

204pin DDRIII-SO-DIMM X2

BANK 0, 1, 2

Page 12, 13

FDI *8
2.7GT/s

DMI2 *4
5GT/s

- LVDS Conn. Page 33
- HDMI Conn. Page 35
- CRT Conn. Page 34

RJ45 Conn. Page 38

LAN
PCIe Port 0
Atheros
AR8162/QCA8172 (10/100)

Page 37

PCIe x1

PCIe Mini Card WLAN
PCIe Port 1

Page 36

PCIe x1

Intel PCH Panther Point

FCBGA 989Balls
25mm x 25mm

Page 14~22

USB30 x2

Left USB3.0 x2
USB30 Port 0,1 Page 45

Right USB2.0
USB20 Port 9 Page 45

Int. Camera
USB20 Port 3 Page 33

Touch Screen
USB20 Port 2 Page 45

Card Reader
Realtek RTS5170
USB20 Port 11 page 28

USB20 x6

SATA Gen3

HDD Conn.
SATA Port 0 Page 40

SATA

ODD Conn.
SATA Port 2 Page 40

AZALIA

Audio Codec
CONEXANT
CX20757 Page 41

Int. MIC Conn.
Page 41

Int. Speaker Conn.
Page 41

Audio Combo Jacks
HP & MIC Page 41

SPI ROM
2MB + 4MB
Page 14

EC
ENE KB9012
Page 42

Thermal Sensor
Page 39

Touch Pad
Page 43

Int. KBD
Page 43

Sub-board

15"
14"

Power/B (LID)
LS9631

USB/B
LS9632

IO/B (Card Reader)
LS9633

ODD/B
LS9634

Switch/B (LED, LID)
LS9635

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			Sheet 2 of 60	Rev 1.0

Voltage Rails

power plane	State	+B	+5VALW	+3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	○	○	○	○	○	○
S3	○	○	○	○	○	✗
S5 S4/AC	○	○	○	✗	✗	✗
S5 S4/ Battery only	○	✗	✗	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗	✗	✗

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V	Board ID / SKU ID Table for AD channel						
R694	100K +/- 1%	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD			
0	0	0 V	0 V	0 V	0x00 - 0x0B	MP		
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT		
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	DVT		
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	EVT		

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
DDR_JDIMM2	1010 010x A4h

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	0100 0001 41h

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) _{USB3.0}
		1	USB Port (Left Side) _{USB3.0}
		2	Touch Screen
	UHCI1	3	Camera
		4	
		5	
		6	
EHCI2	UHCI3	7	
		8	
	UHCI4	9	USB Port (Right Side USB-BD)
		10	Mini Card(WLAN)
		11	Card Reader
		12	
UHCI6	13		

BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76, HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

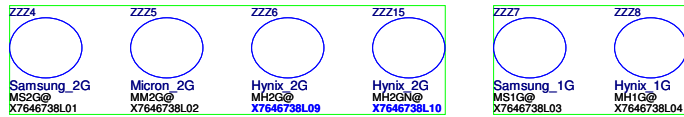
SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	V	X	X	X	X	V	V
SMB_EC_DA2	+3VS	+3VGS					+3VS	+3VALW
PCH_SMBCLK	PCH	X	X	X	V	V	X	X
PCH_SMBDATA	+3VALW				+3VS	+3VS		
PCH_SMLCLK	PCH	X	X	X	X	X	X	X
PCH_SMLDATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VGS		+3VS			+3VS	

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Date: Wednesday, February 27, 2013				Rev 1.0
Sheet 3 of 60				

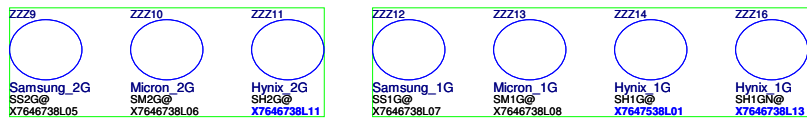
Mars XT VRAM STRAP

		X76@			X76@				
	Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27		
2GBytes	ZZZ4 MS2G@ Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	0	NC	4.75K		
2GBytes	ZZZ5 MM2G@ Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K		
2GBytes	ZZZ6 MH2G@ Hynix 2048Mbits SA000065300 128M16 H5TQ2G63DFR-N0C	2	0	1	0	4.53K	2K		
1GBytes	ZZZ7 MS1G@ Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	3	0	1	1	6.98K	4.99K		
2GBytes	ZZZ15 MH2GN@ Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	4	1	0	0	4.53K	4.99K		
1GBytes	ZZZ8 MH1G@ Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	7	1	1	1	4.75K	NC		



Sun PRO VRAM STRAP

		X76@			X76@				
	Vendor UV9, UV10, UV11, UV12	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27		
2GBytes	ZZZ9 SS2G@ Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	0	NC	4.75K		
2GBytes	ZZZ10 SM2G@ Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-107G:E	1	0	0	1	8.45K	2K		
2GBytes	ZZZ11 SH2G@ Hynix 4096Mbits SA00006DG00 256Mx16 H5TQ4G63MFR-11C	2	0	1	0	4.53K	2K		
1GBytes	ZZZ12 SS1G@ Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	3	0	1	1	6.98K	4.99K		
1GBytes	ZZZ16 SH1GN@ Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	4	1	0	0	4.53K	4.99K		
1GBytes	ZZZ13 SM1G@ Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	6	1	1	0	3.4K	10K		
1GBytes	ZZZ14 SH1G@ Hynix 2048Mbits SA000065300 128M16 H5TQ2G63DFR-N0C	7	1	1	1	4.75K	NC		



Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(3.3VGS)

PCIE_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

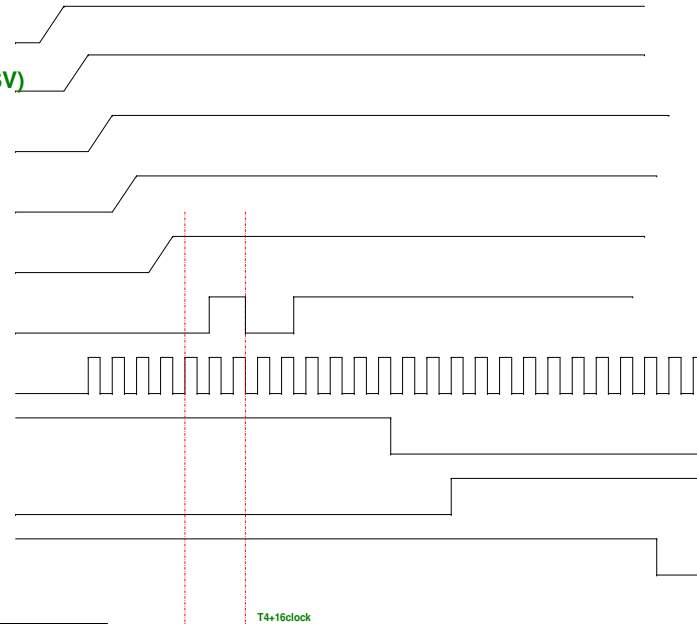
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset



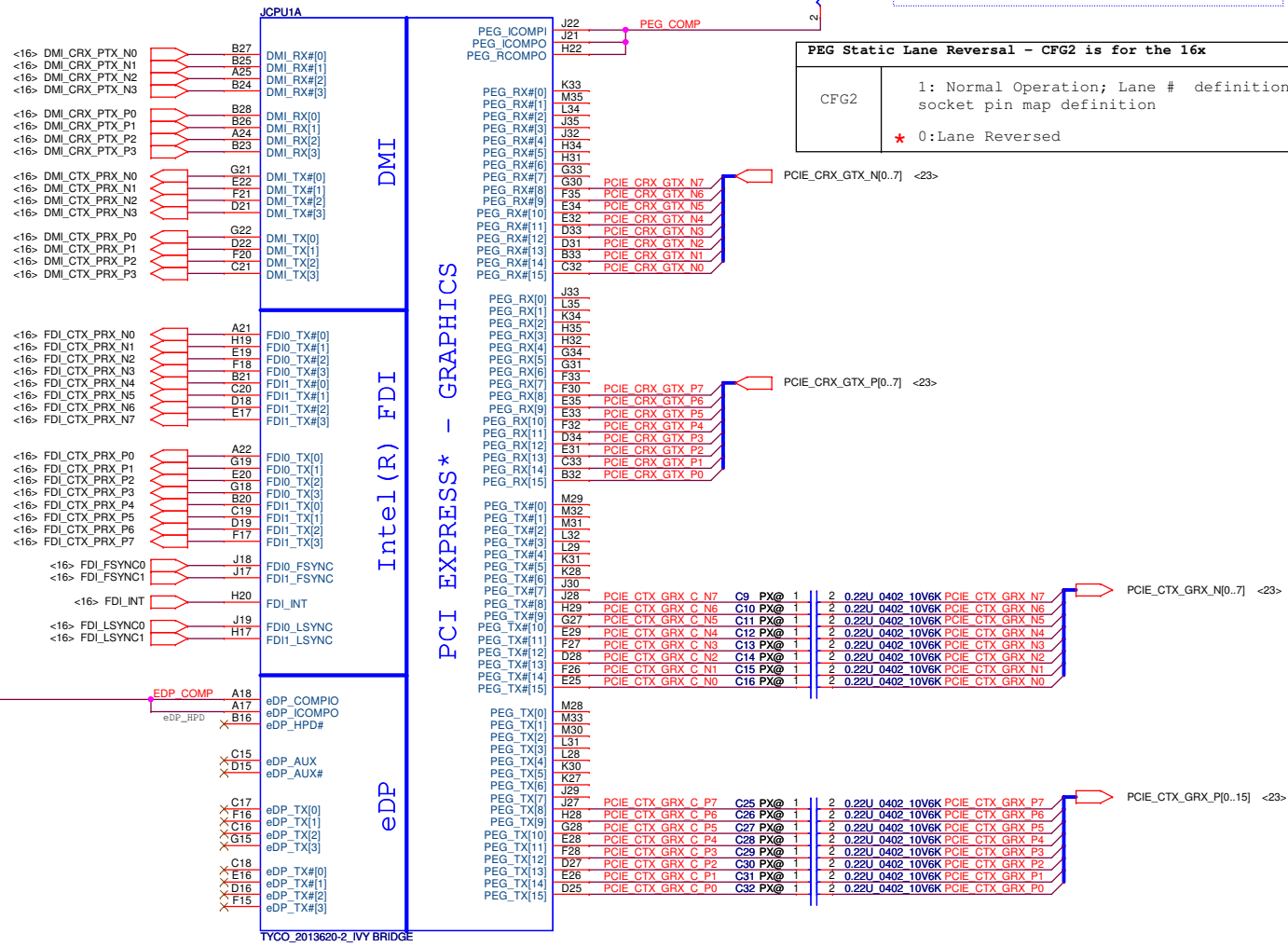
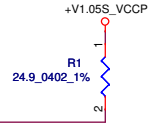
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

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				VGA Notes List
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				LA-9631P
				Rev 1.0
				Date: Wednesday, February 27, 2013 Sheet 4 of 60



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



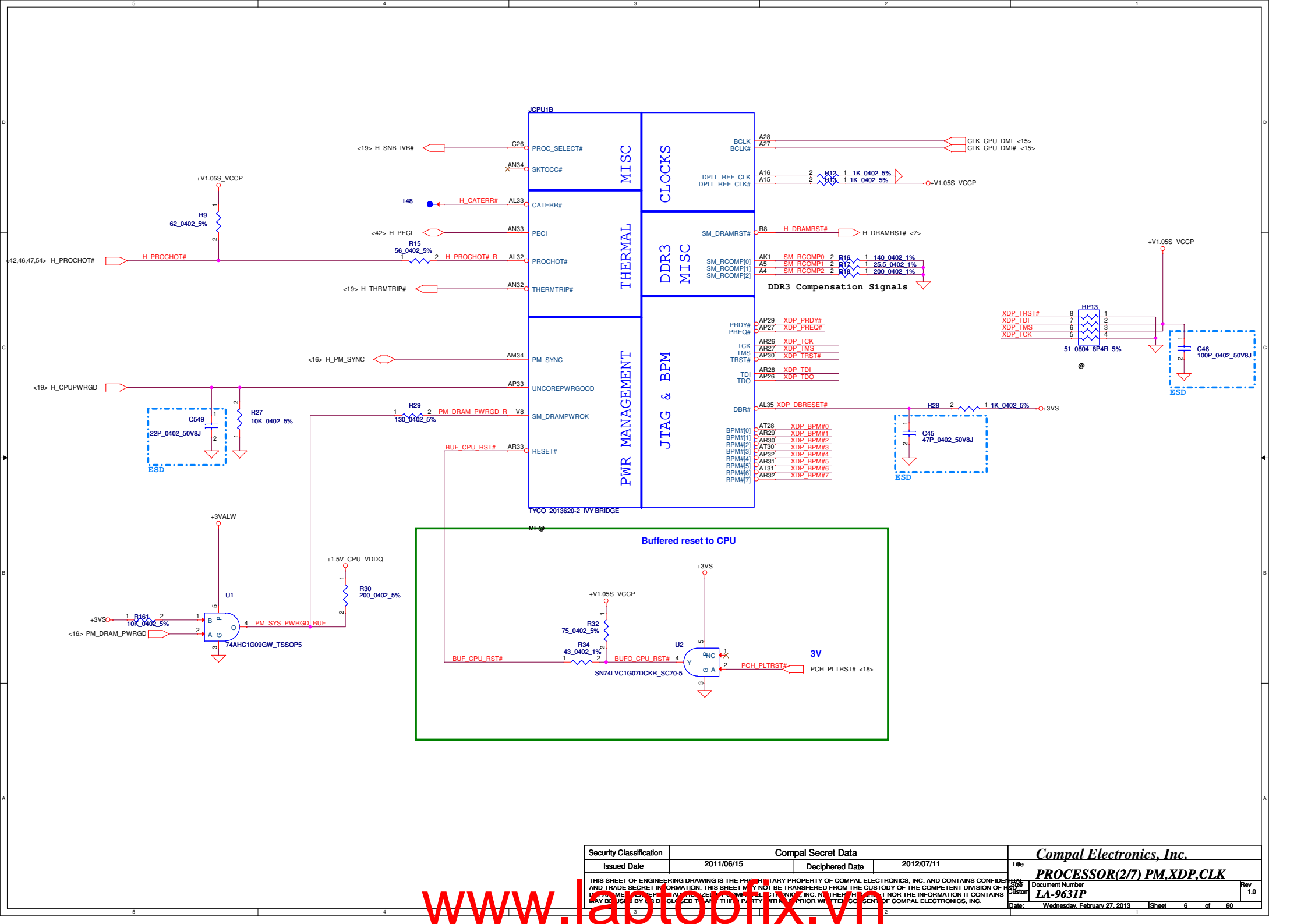
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
*	0: Lane Reversed

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

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Compal Electronics, Inc.	
PROCESSOR(17) DMI,FDI,PEG	
Size	Document Number
Custom	LA-9631P
Date	Wednesday, February 27, 2013
Sheet	5 of 60
Rev	1.0



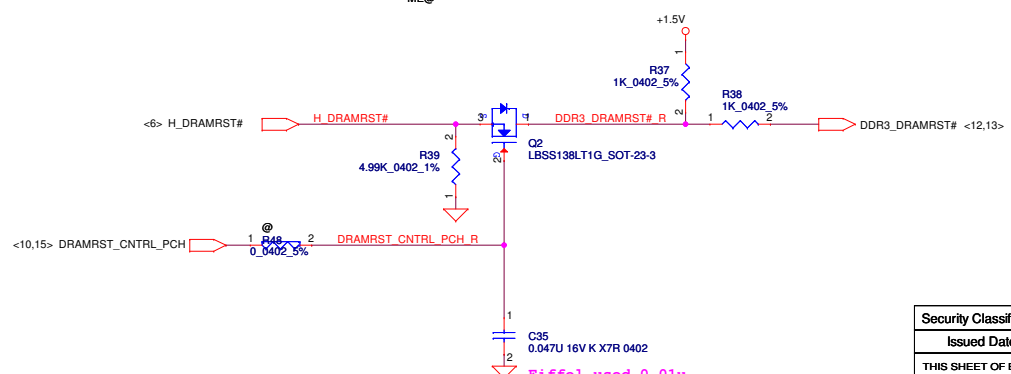
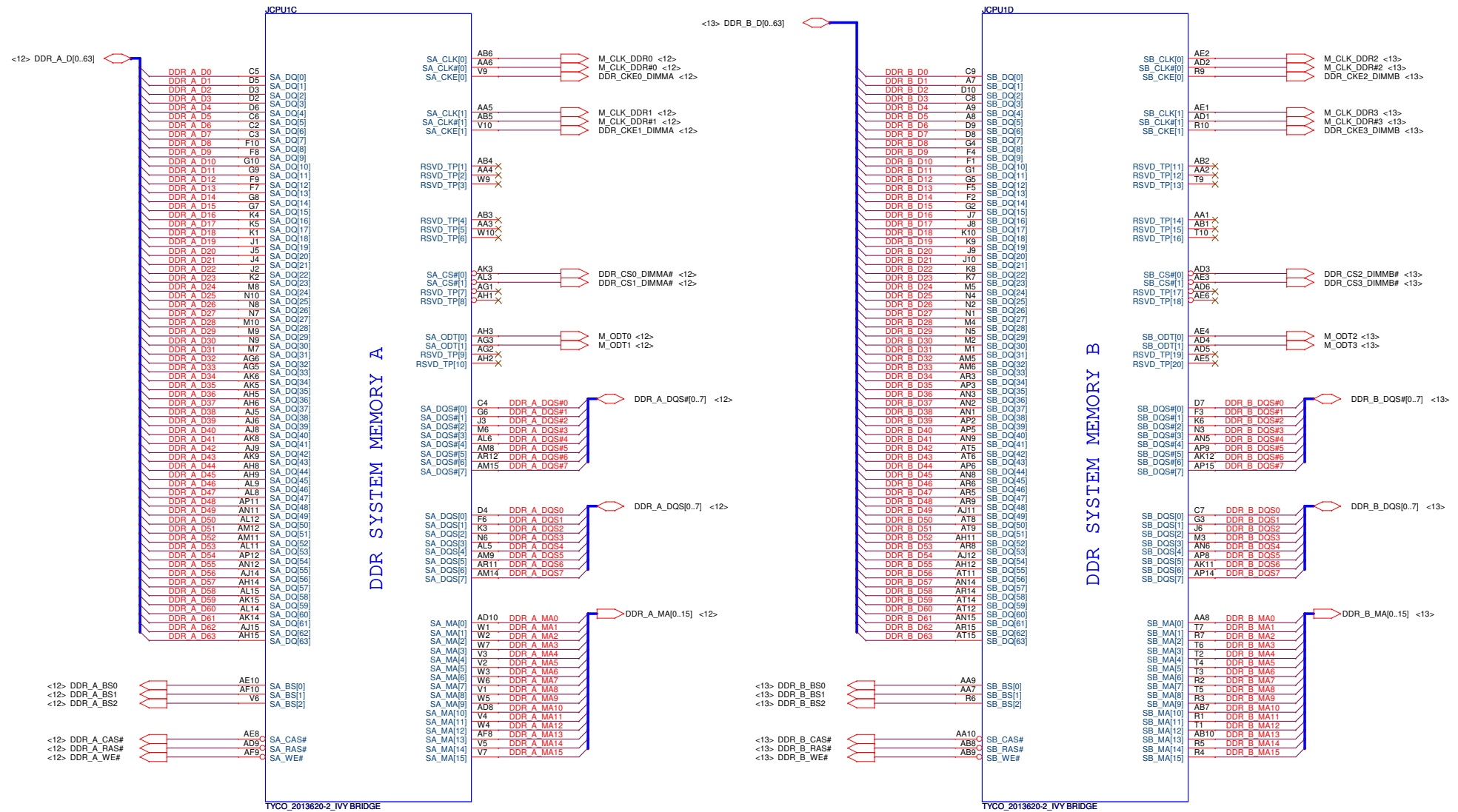
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Title **Compal Electronics, Inc.**
PROCESSOR(2/7) PM,XDP,CLK

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Document Number	Rev
LA-9631P	1.0
Date: Wednesday, February 27, 2013	Sheet 6 of 60

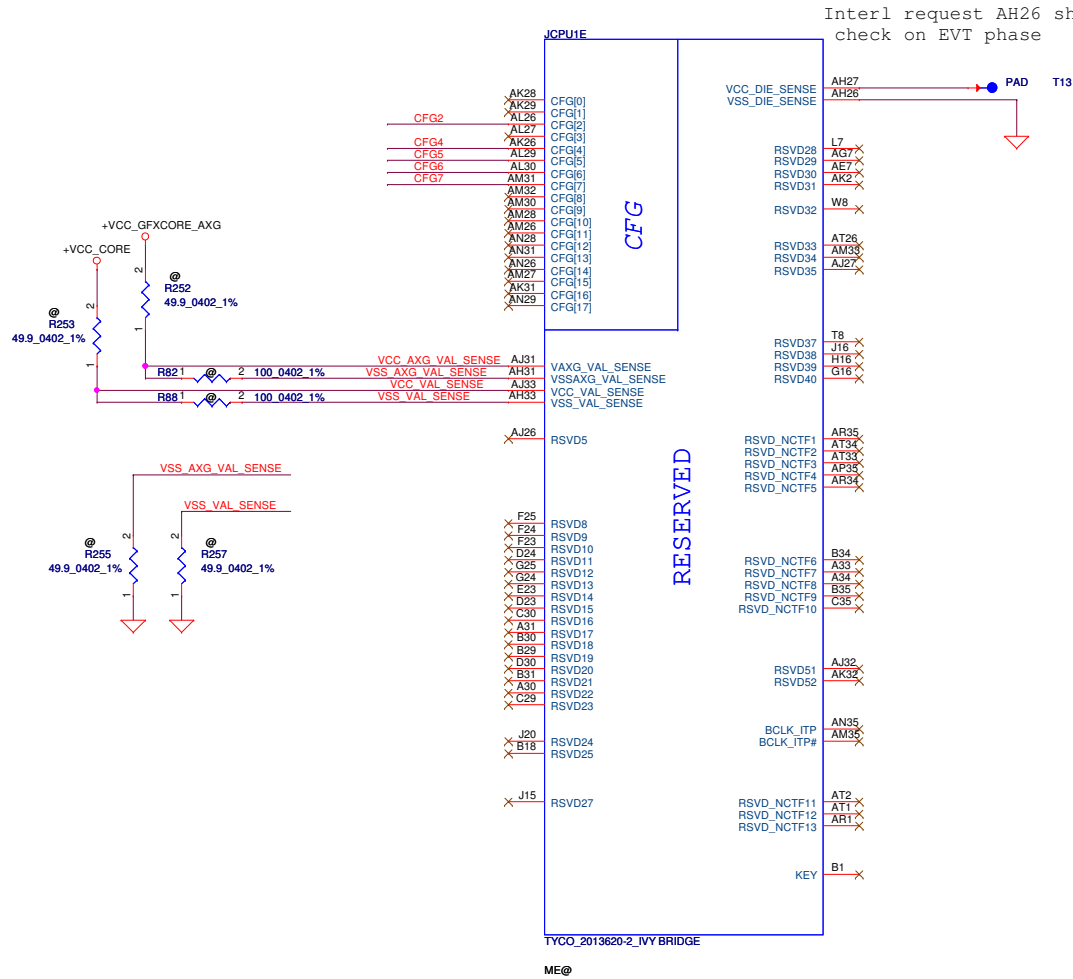
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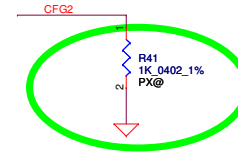
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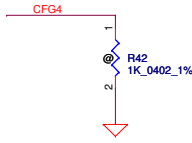
CFG Straps for Processor



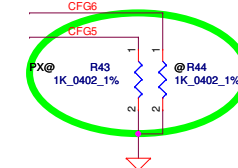
Interl request AH26 short GND
check on EVT phase



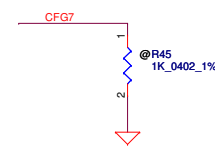
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

POWER

+VCC_CORE
QC=94A
DC=53A

JCPU1F

+V1.05S_VCCP
8.5A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
VCC29
VCC30
VCC31
VCC32
VCC33
VCC34
VCC35
VCC36
VCC37
VCC38
VCC39
VCC40
VCC41
VCC42
VCC43
VCC44
VCC45
VCC46
VCC47
VCC48
VCC49
VCC50
VCC51
VCC52
VCC53
VCC54
VCC55
VCC56
VCC57
VCC58
VCC59
VCC60
VCC61
VCC62
VCC63
VCC64
VCC65
VCC66
VCC67
VCC68
VCC69
VCC70
VCC71
VCC72
VCC73
VCC74
VCC75
VCC76
VCC77
VCC78
VCC79
VCC80
VCC81
VCC82
VCC83
VCC84
VCC85
VCC86
VCC87
VCC88
VCC89
VCC90
VCC91
VCC92
VCC93
VCC94
VCC95
VCC96
VCC97
VCC98
VCC99
VCC100

VCCI01
VCCI02
VCCI03
VCCI04
VCCI05
VCCI06
VCCI07
VCCI08
VCCI09
VCCI10
VCCI11
VCCI12
VCCI13
VCCI14
VCCI15
VCCI16
VCCI17
VCCI18
VCCI19
VCCI20
VCCI21
VCCI22
VCCI23
VCCI24
VCCI25
VCCI26
VCCI27
VCCI28
VCCI29
VCCI30
VCCI31
VCCI32
VCCI33
VCCI34
VCCI35
VCCI36
VCCI37
VCCI38
VCCI39
VCCI40

VIDALERT#
VIDSCLK
VIDSOUT

VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSS_SENSE_VCCIO

AH13
AH10
AG10
AC10
Y10
U10
P10
L10
J14
J13
J12
J11
H14
H12
H11
G14
G13
G12
F14
F13
F12
F11
E14
E12
E11
D14
D13
D12
D11
C14
C13
C12
C11
B14
B12
A14
A13
A12
A11

AJ29
AJ30
AJ28

AJ35
AJ34
B10
A10

+V1.05S_VCCP

R46
75_0402_5%

VR_SVID_CLK series-resistors close to VR

R50 2 1 130 0402 5%
V1.05S_VCCP 0.1uF on power side

VCC_SENSE 100ohm +-1% pull-up to VCC near processor

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

+VCC_CORE

R51
100_0402_1%

VCCSENSE <54>
VSSSENSE <54>

R54
100_0402_1%

R74
10_0402_1%

VSS_SENSE 100ohm +-1% pull-down to GND near processor

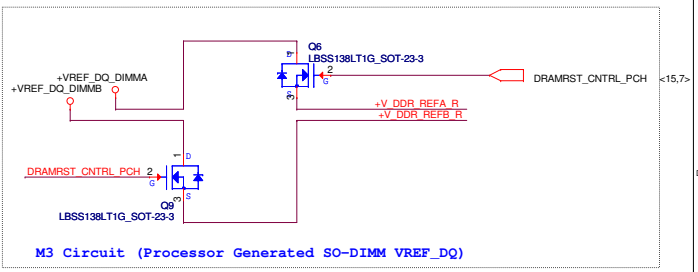
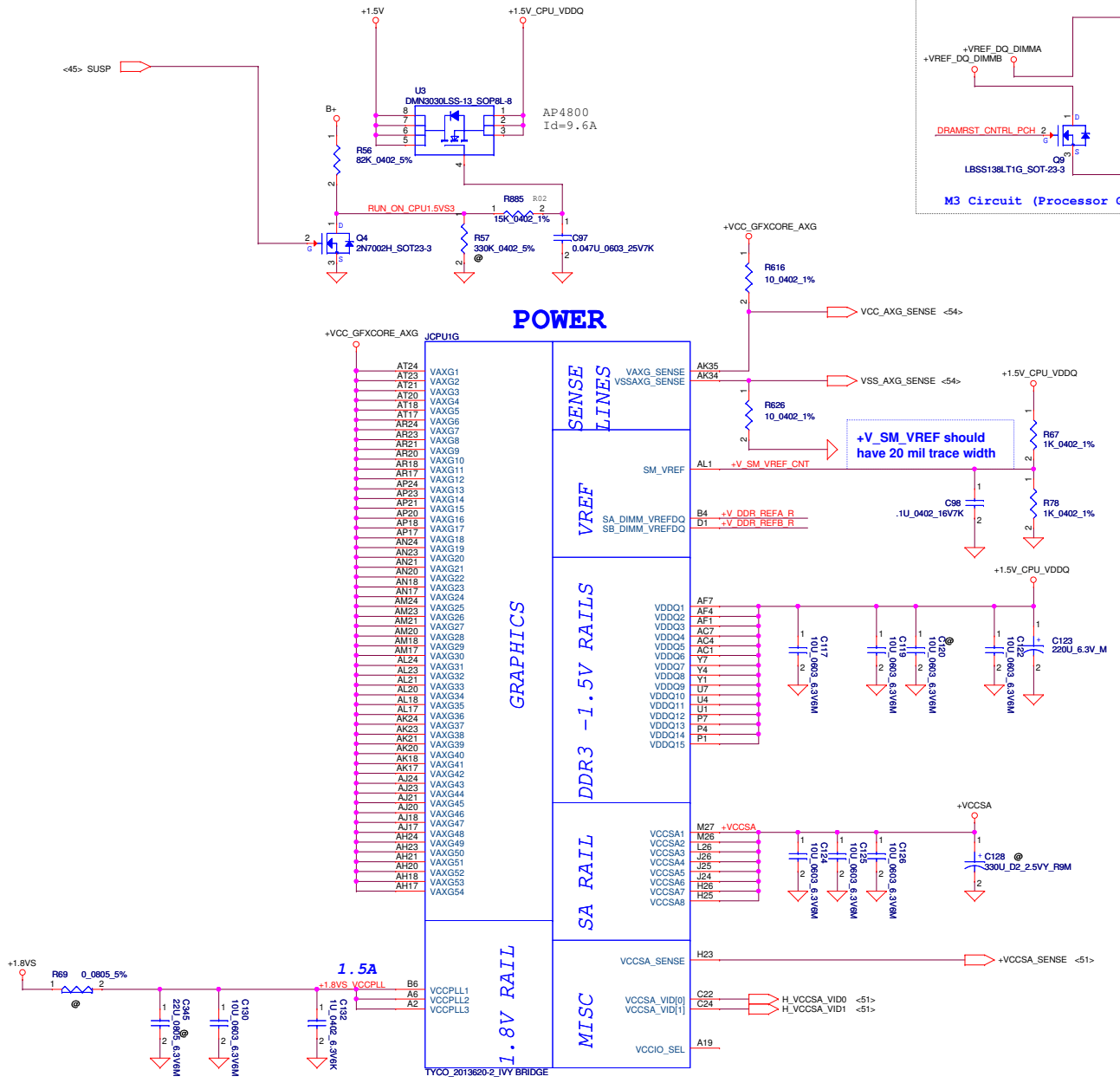
R79
10_0402_1%

TYCO_2013620-2_IVY BRIDGE

ME@

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				Sheet 9 of 60 Rev 1.0

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POWER

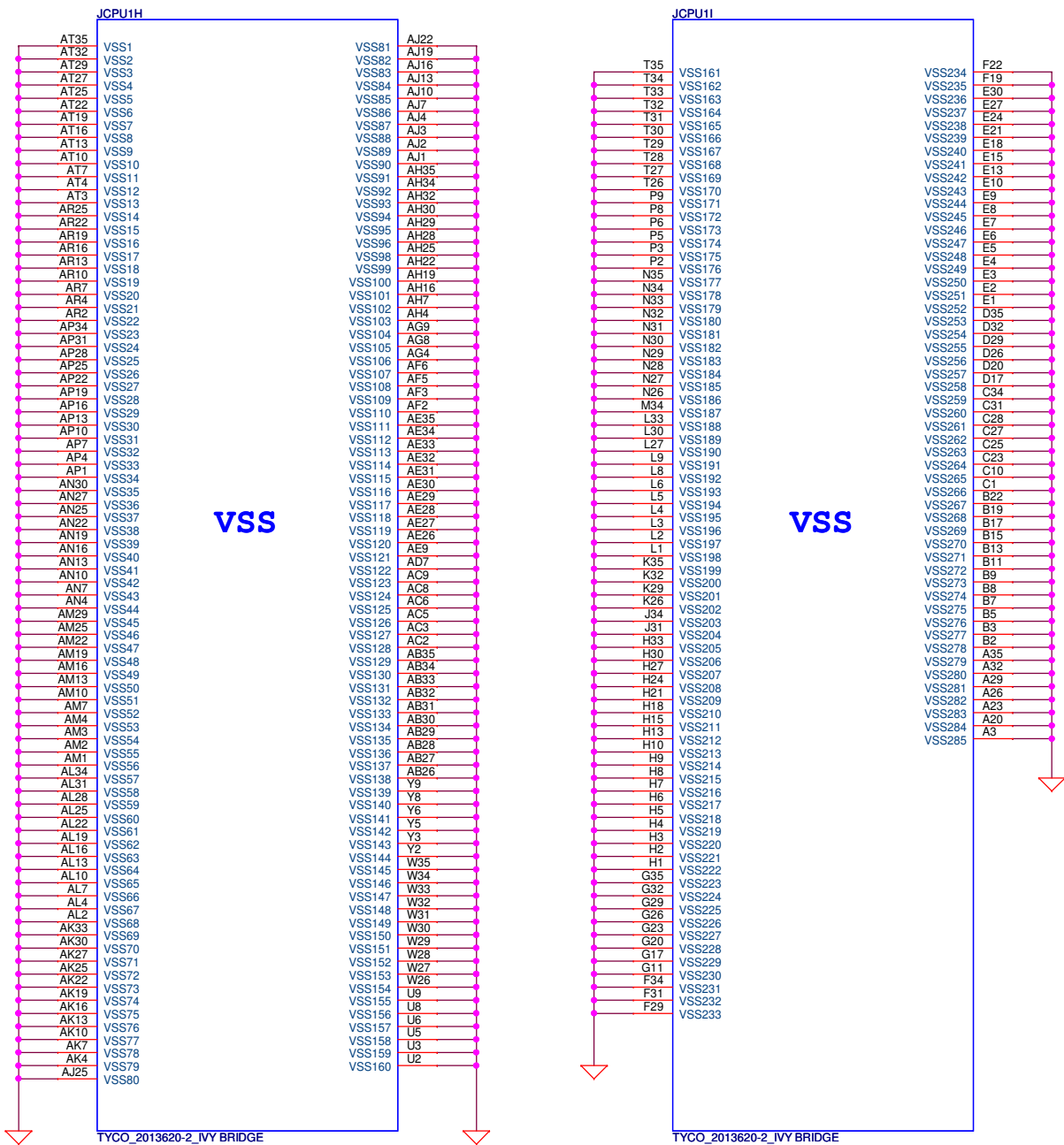
GRAPHICS

1.8V RAIL

IVY Bridge drives VCCIO_SEL low
 VCCP_PWRCTRL:0
 Sandy Bridge is NC for A19
 VCCP_PWRCTRL:1

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Date: Wednesday, February 27, 2013			Sheet 10 of 60

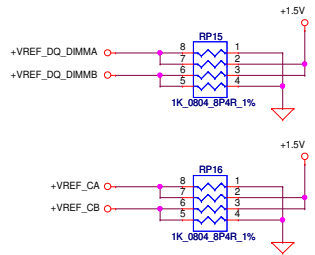
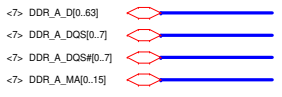
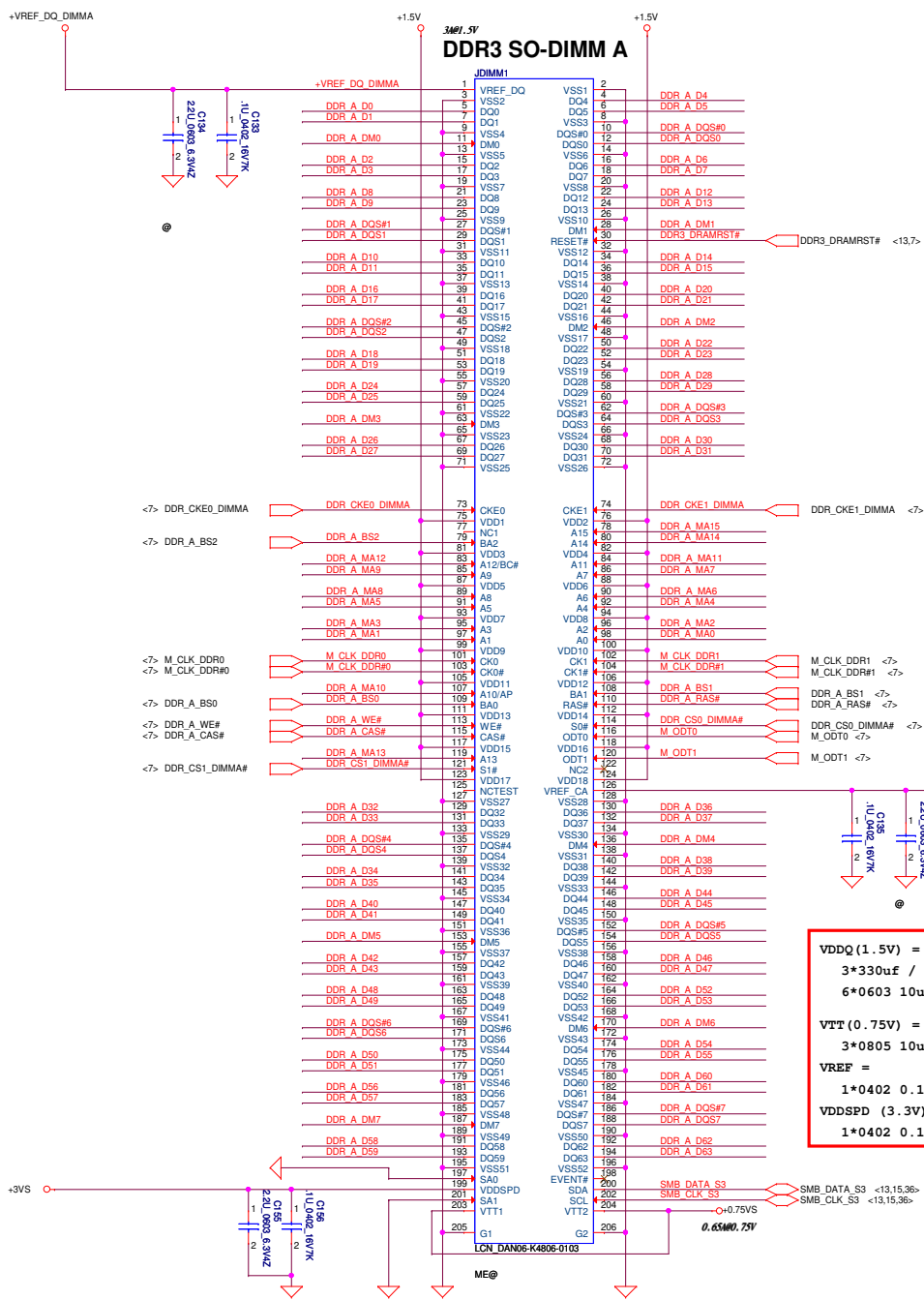
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ME@

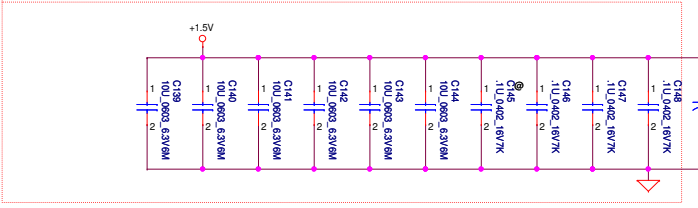
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Size Custom LA-9631P	Document Number LA-9631P	Rev 1.0
Date:	Wednesday, February 27, 2013	Sheet 11 of 60



OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
 (10uF_0603_6.3V)*8
 (0.1uF_402_10V)*4

Layout Note:
Place near DIMM



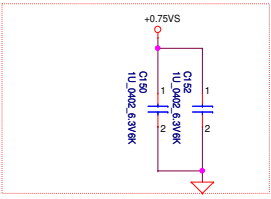
Layout Note:
Place near DIMM

VDDQ (1.5V) =
 $3 \times 330\mu\text{f} / 12\text{m ohm}$ (TOTAL FOR 2 SO-DIMM's)
 6×0603 10uF (PER CONNECTOR)

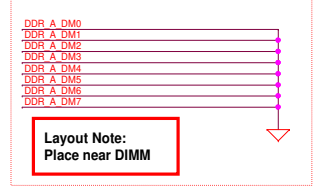
VTT (0.75V) =
 3×0805 10uF 4×0402 1uF

VREF =
 1×0402 0.1uF 1×0402 2.2uF

VDDSPD (3.3V) =
 1×0402 0.1uF 1×0402 2.2uF

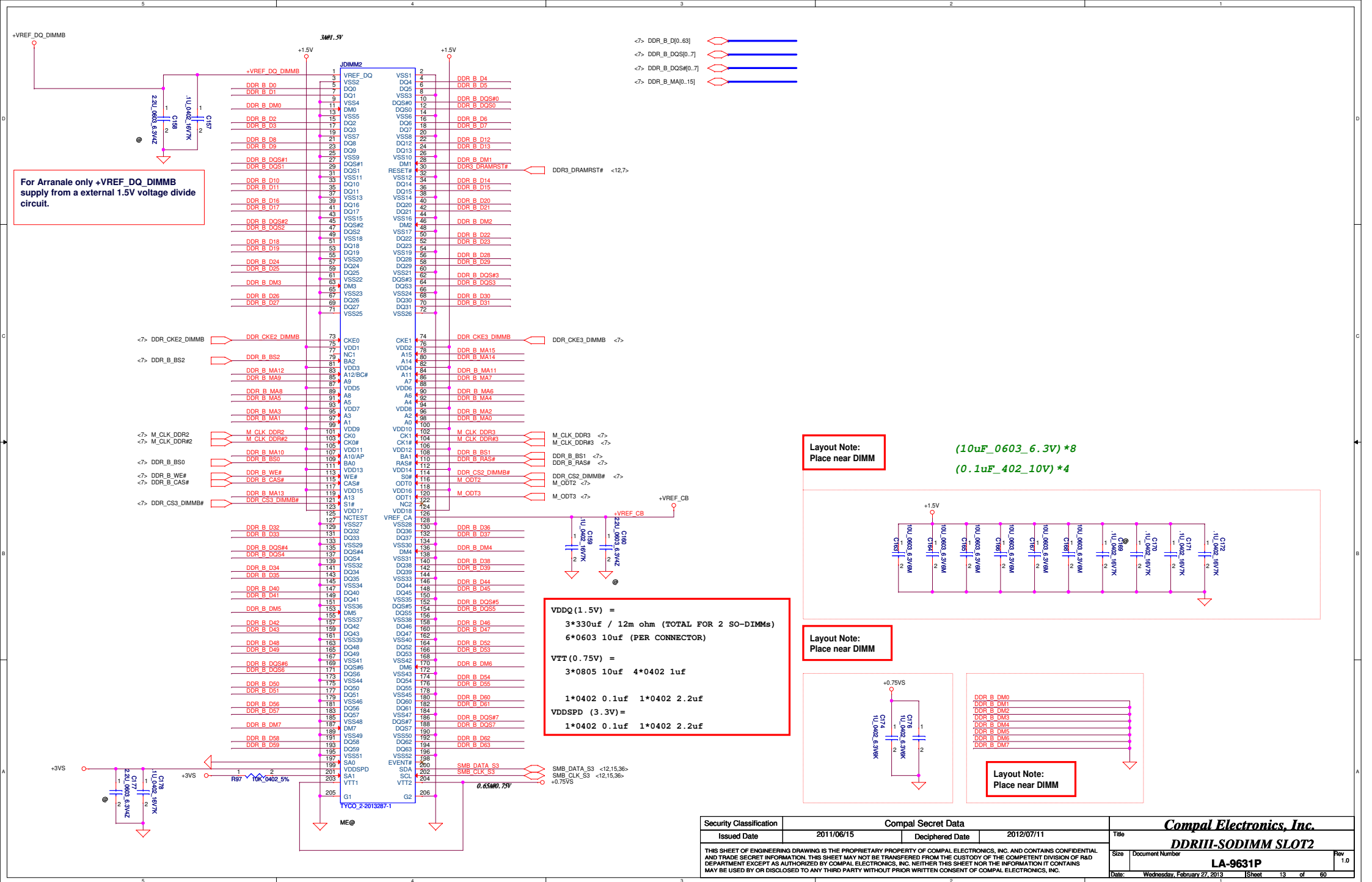


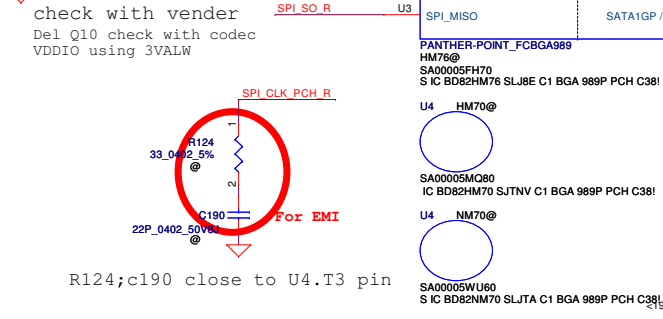
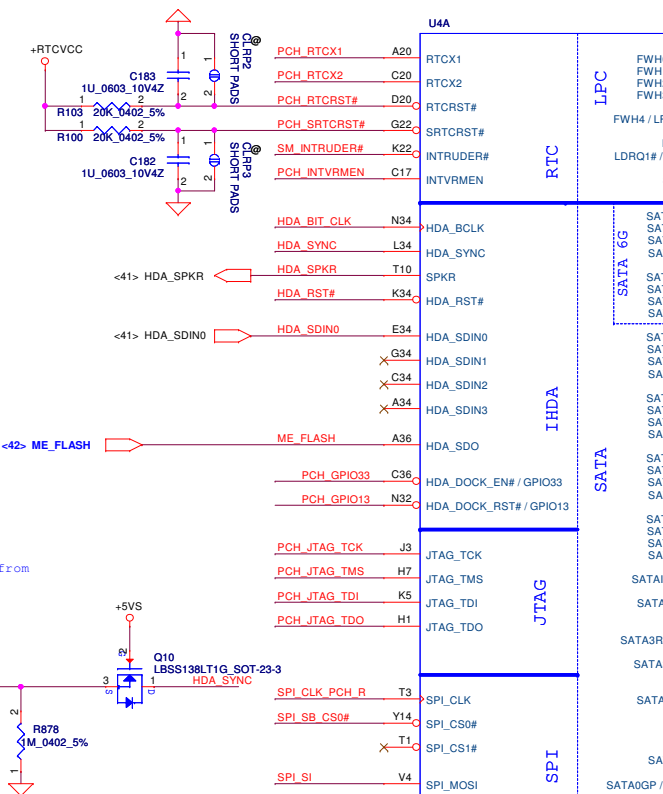
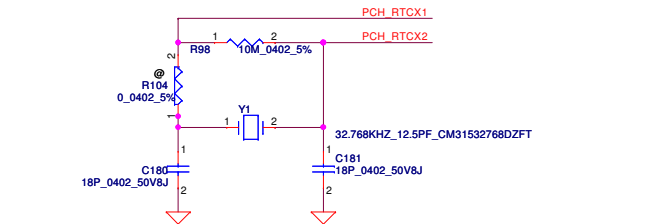
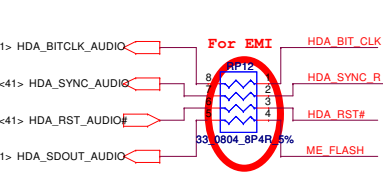
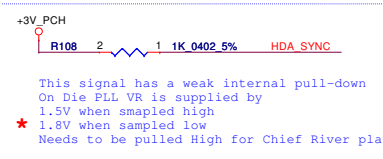
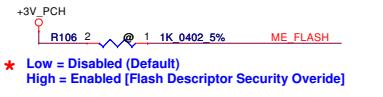
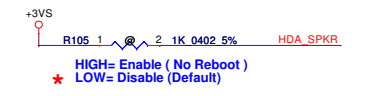
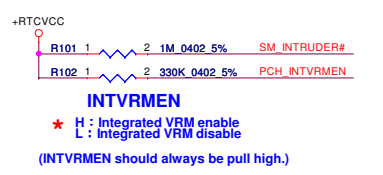
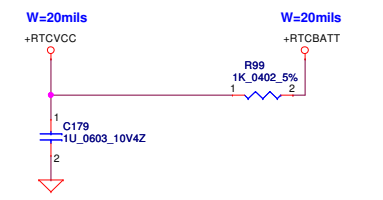
7/28 Update connect GND directly



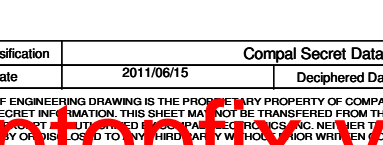
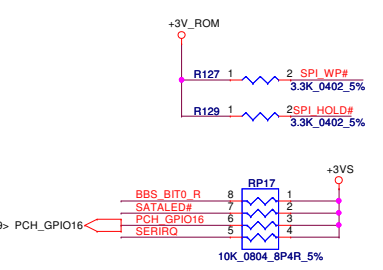
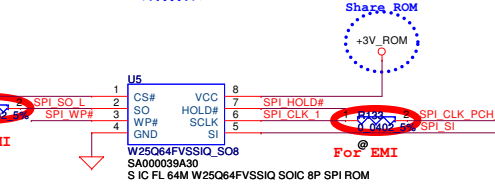
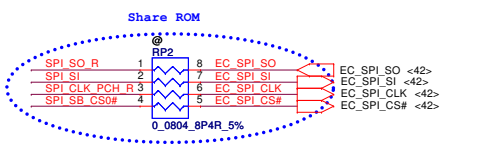
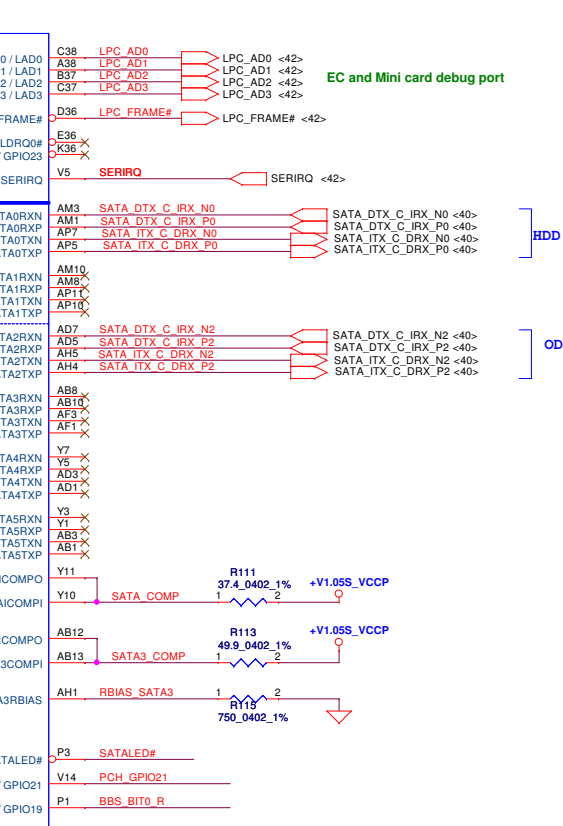
Layout Note:
Place near DIMM

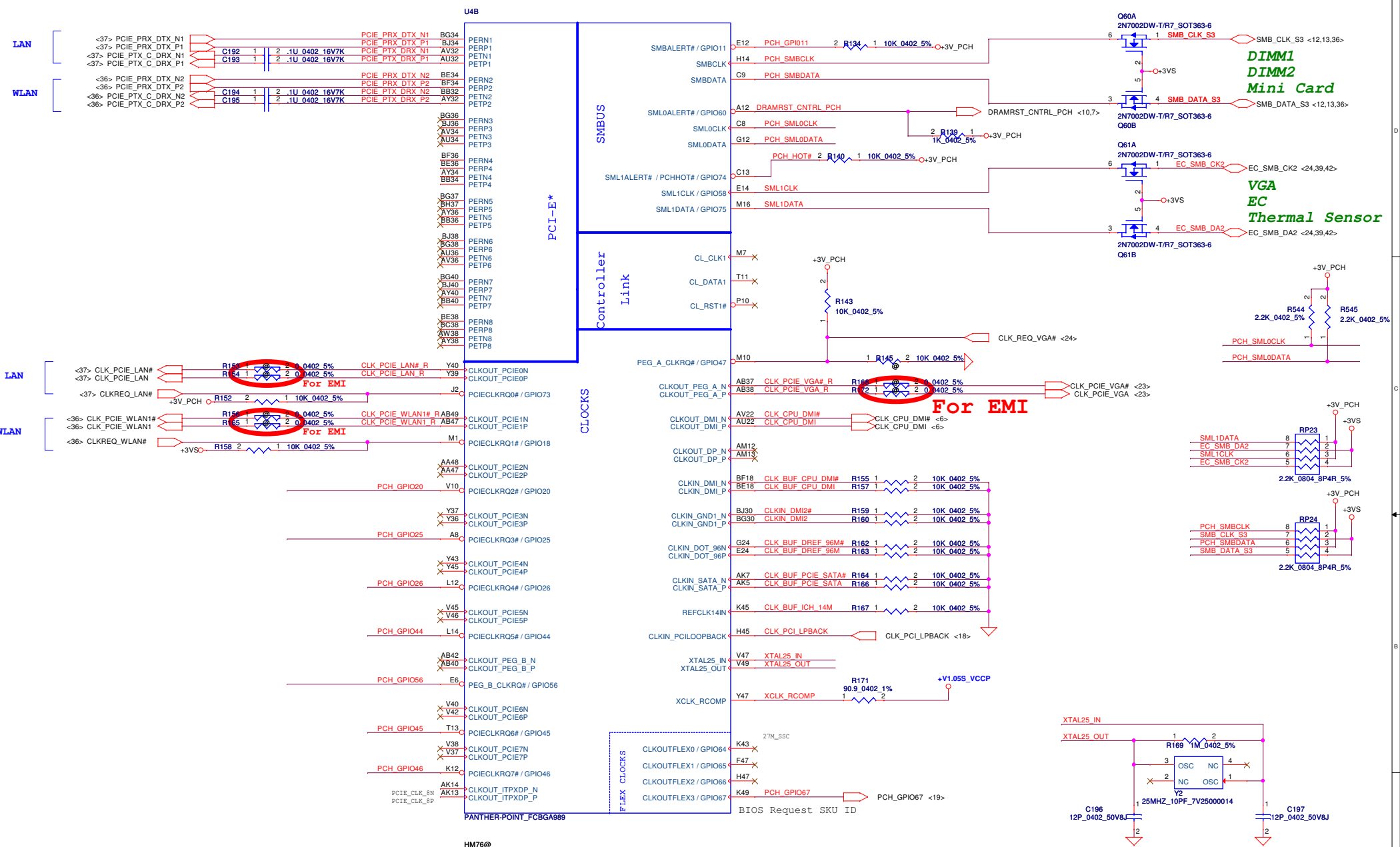
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			LA-9631P		0
			Date:	Wednesday, February 27, 2013	Sheet 12 of 60





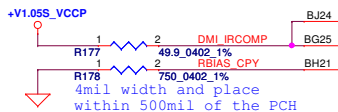
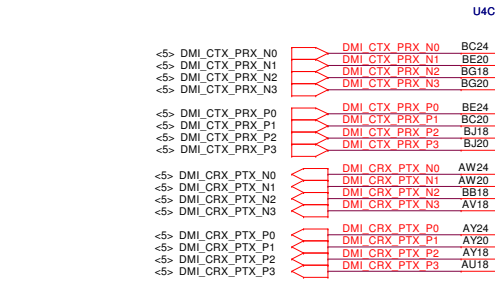
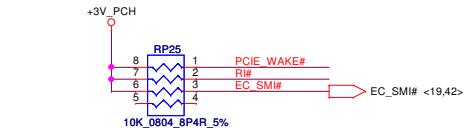
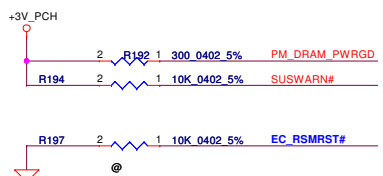
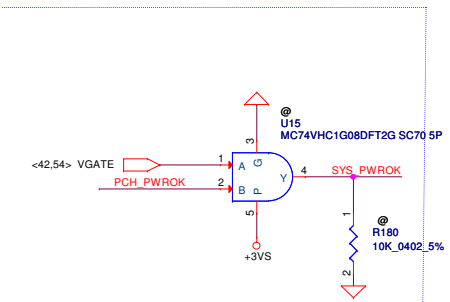
CLR2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS
CLR3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



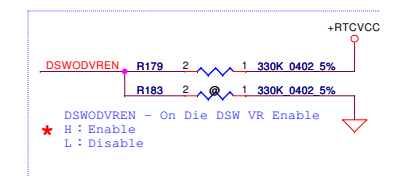
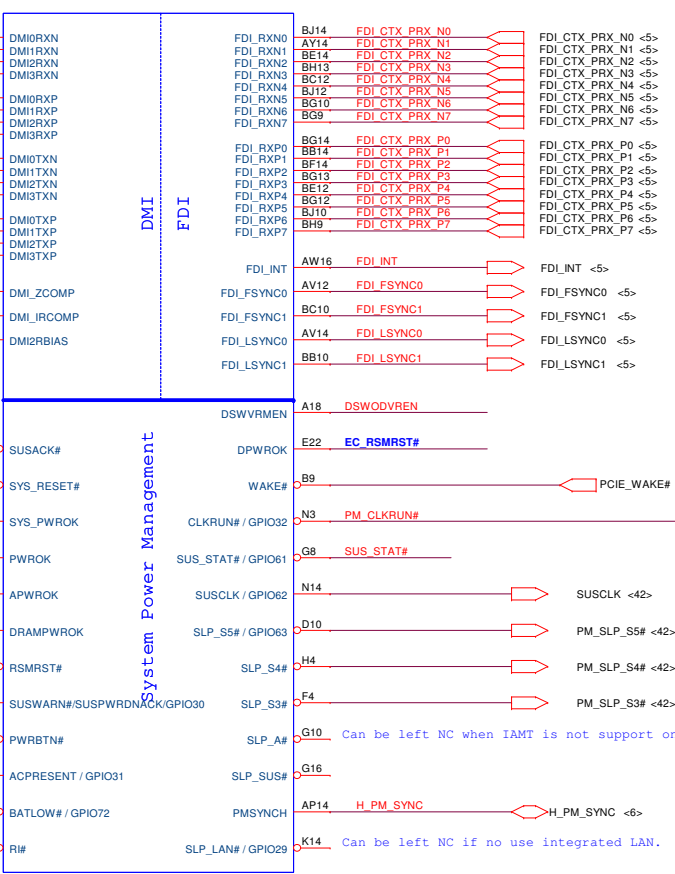
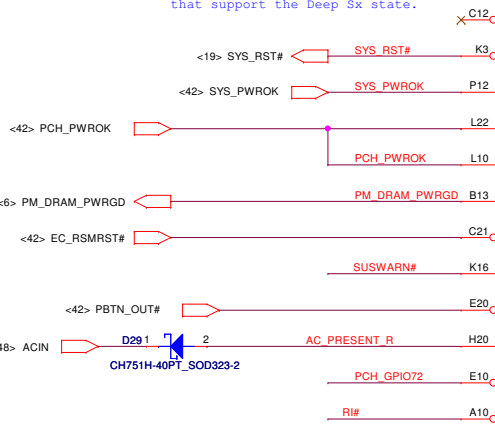


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PCH (2/9) PCIE, SMBUS, CLK				Rev
LA-9631P				1.0
Date:	Wednesday, February 27, 2013	Sheet	15	of 60

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SUSACK# is only used on platform that support the Deep Sx state.

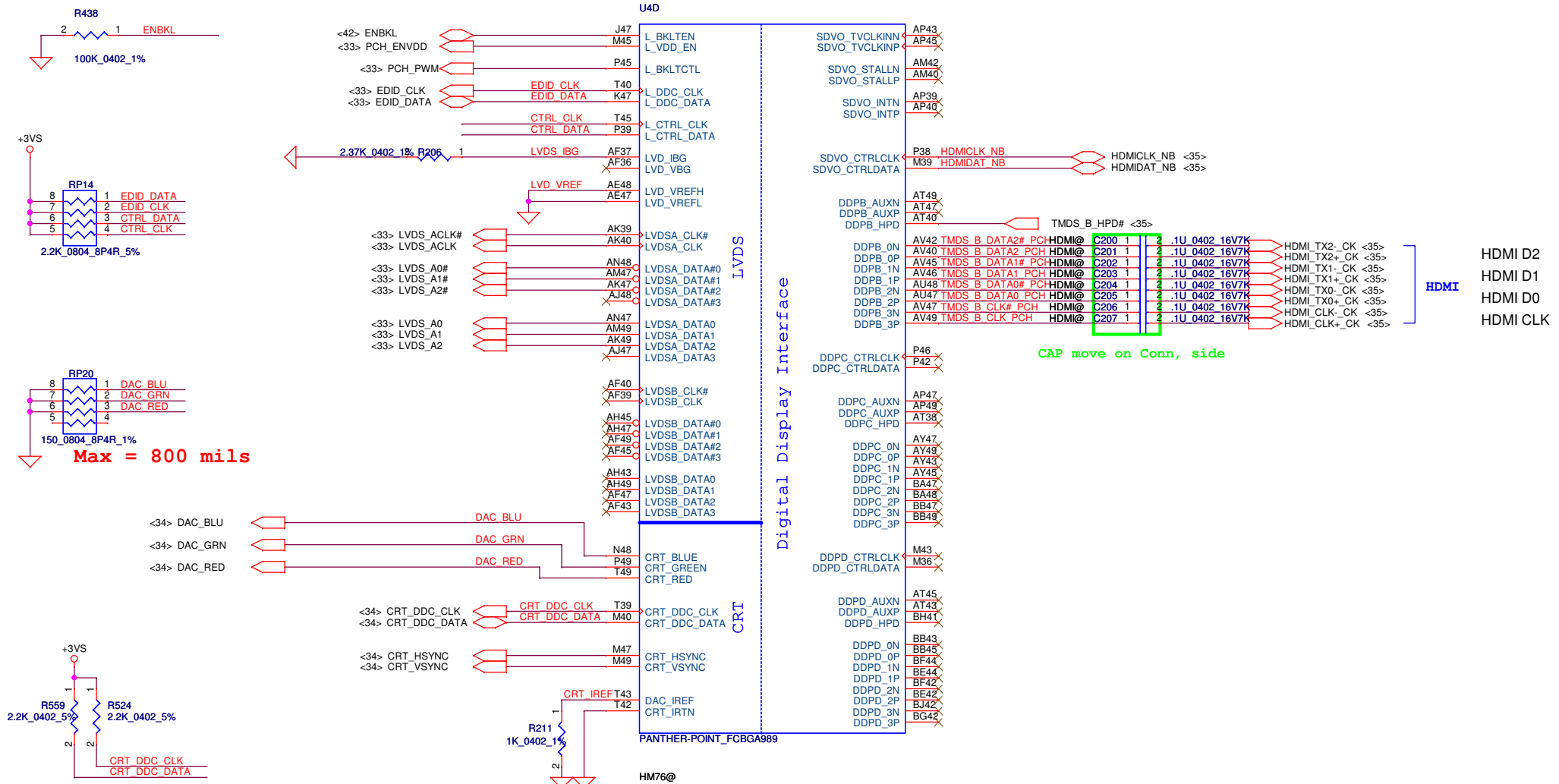


DSOWDVREN - On Die DSW VR Enable
 * H : Enable
 L : Disable

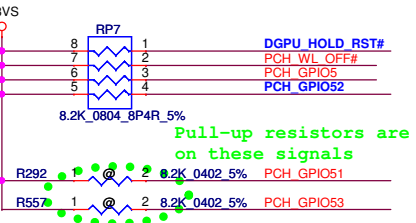
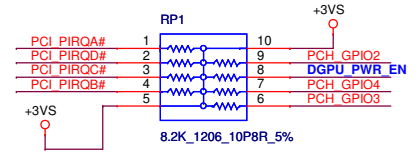
HM76@

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				LA-9631P	1.0
				Date: Wednesday, February 27, 2013	Sheet 16 of 60

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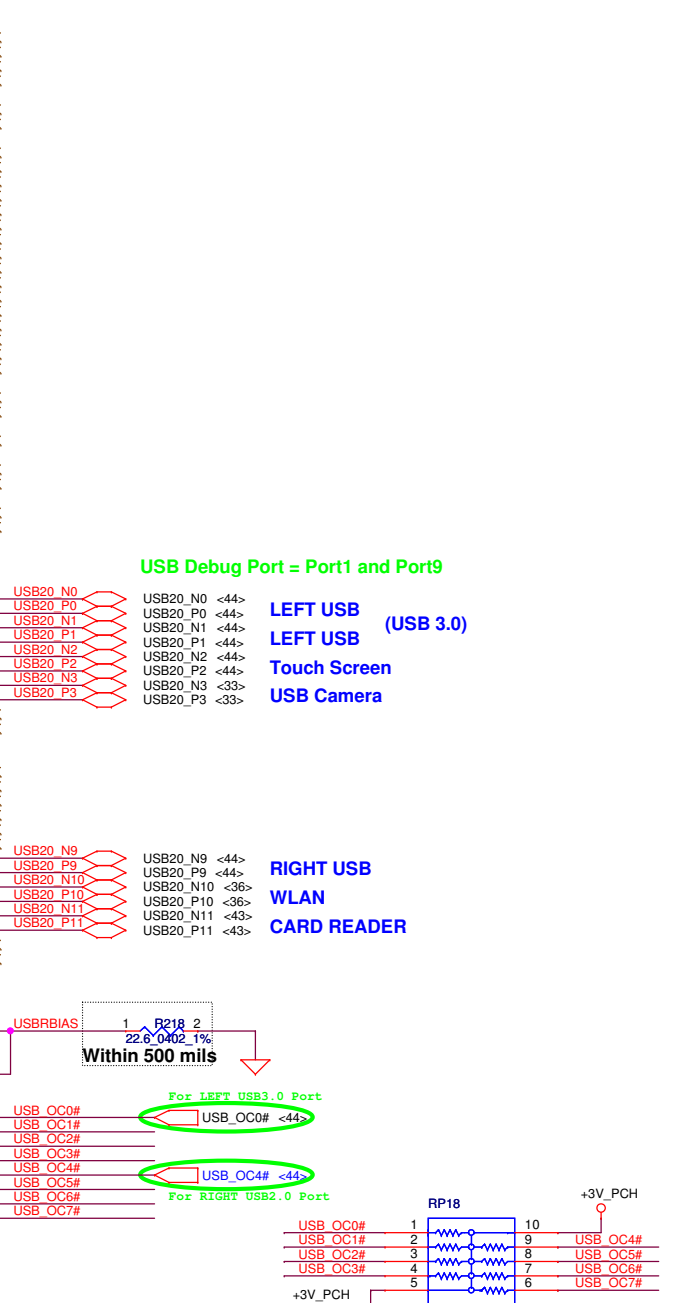
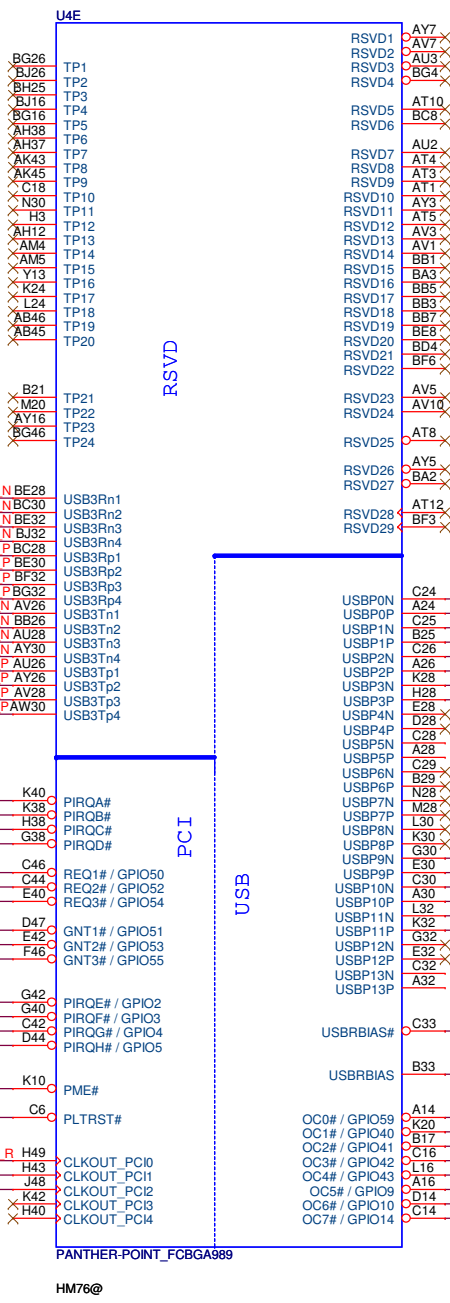
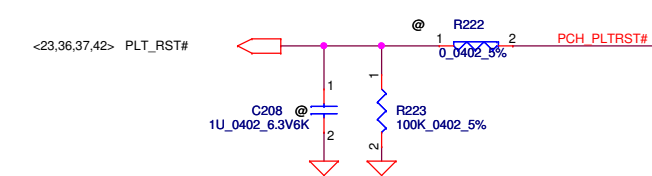
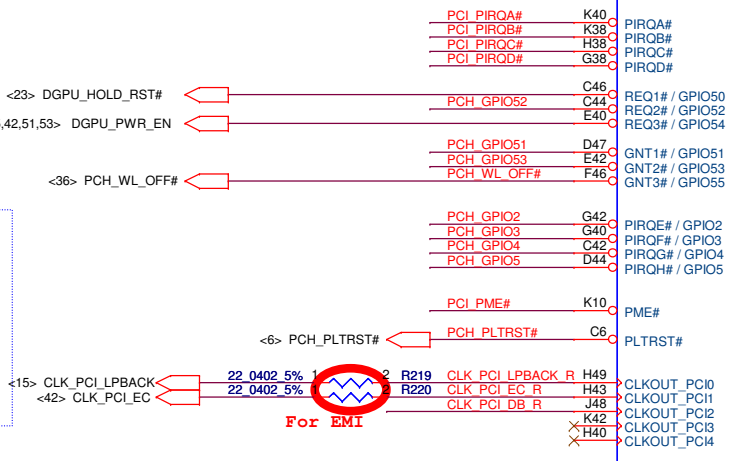
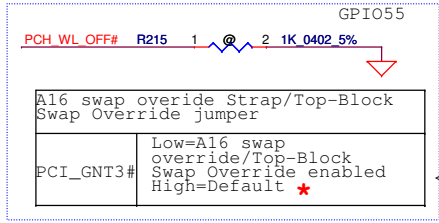
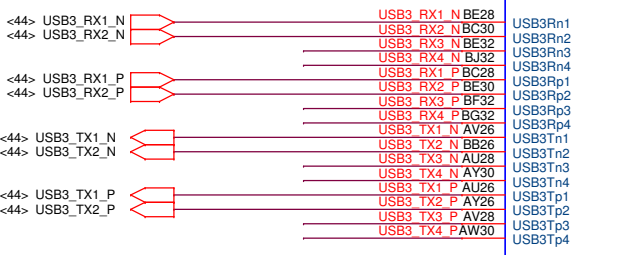


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Date: Wednesday, February 27, 2013				Sheet 17 of 60



Pull-up resistors are not required on these signals

Boot BIOS Strap bit1 BBS1		
Bit11	Bit10	Boot BIOS Destination
0	1	Reserved
1	0	Reserved
1	1	★ SPI (Default)
0	0	LPC



USB Debug Port = Port1 and Port9

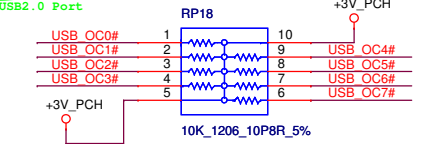
LEFT USB (USB 3.0)
LEFT USB
Touch Screen
USB Camera

RIGHT USB
WLAN
CARD READER

Within 500 mils

For LEFT USB3.0 Port

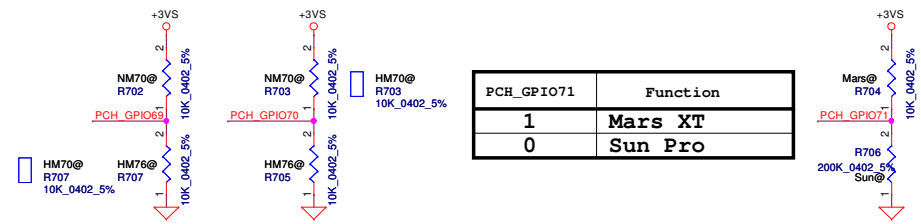
For RIGHT USB2.0 Port



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Date: Wednesday, February 27, 2013			Sheet 18 of 60

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PCH_GPIO69	PCH_GPIO70	Function
1	1	NM70
1	0	Reserved
0	1	HM70
0	0	HM76

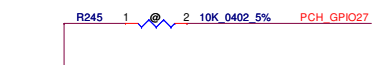


PCH_GPIO71	Function
1	Mars XT
0	Sun Pro

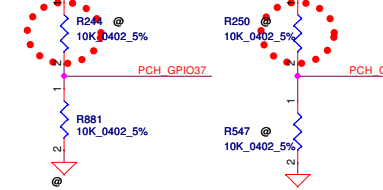
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



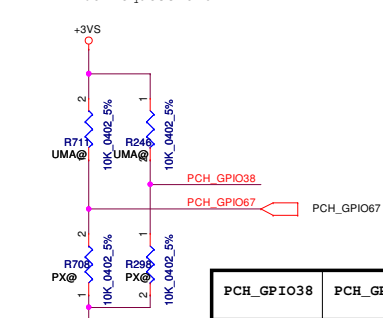
* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



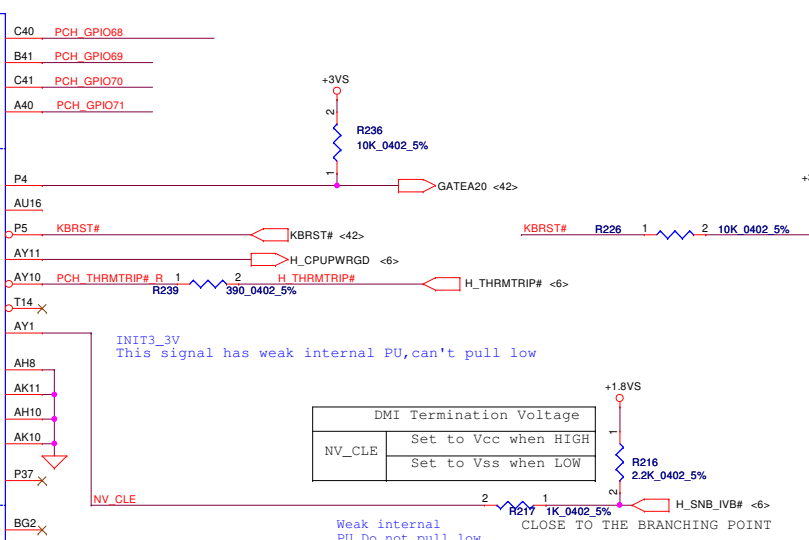
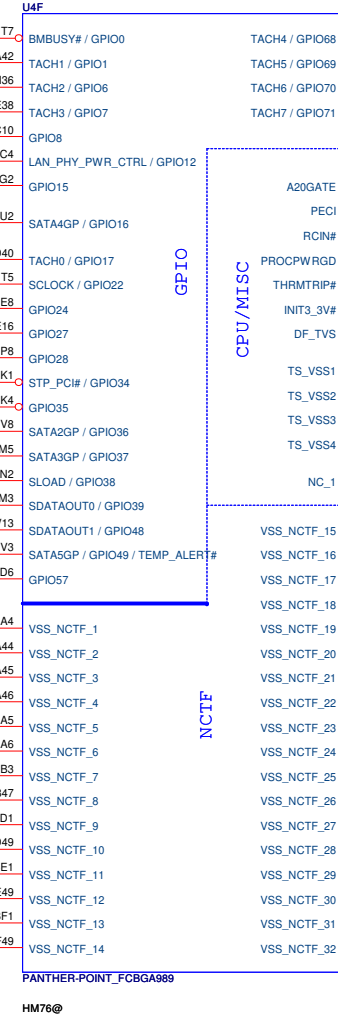
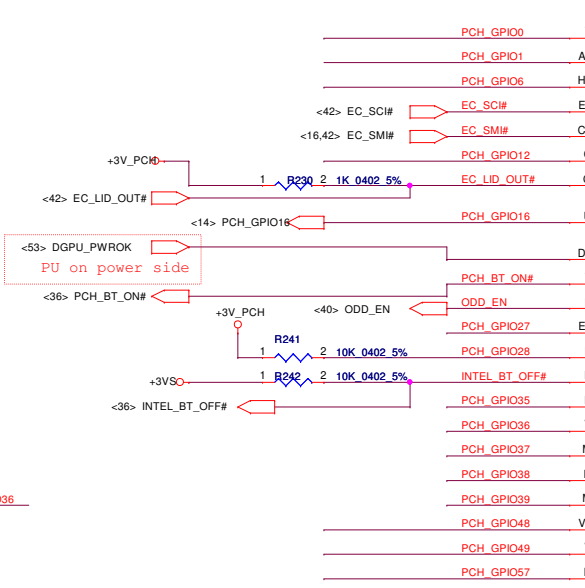
GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.



BIOS Request SKU ID



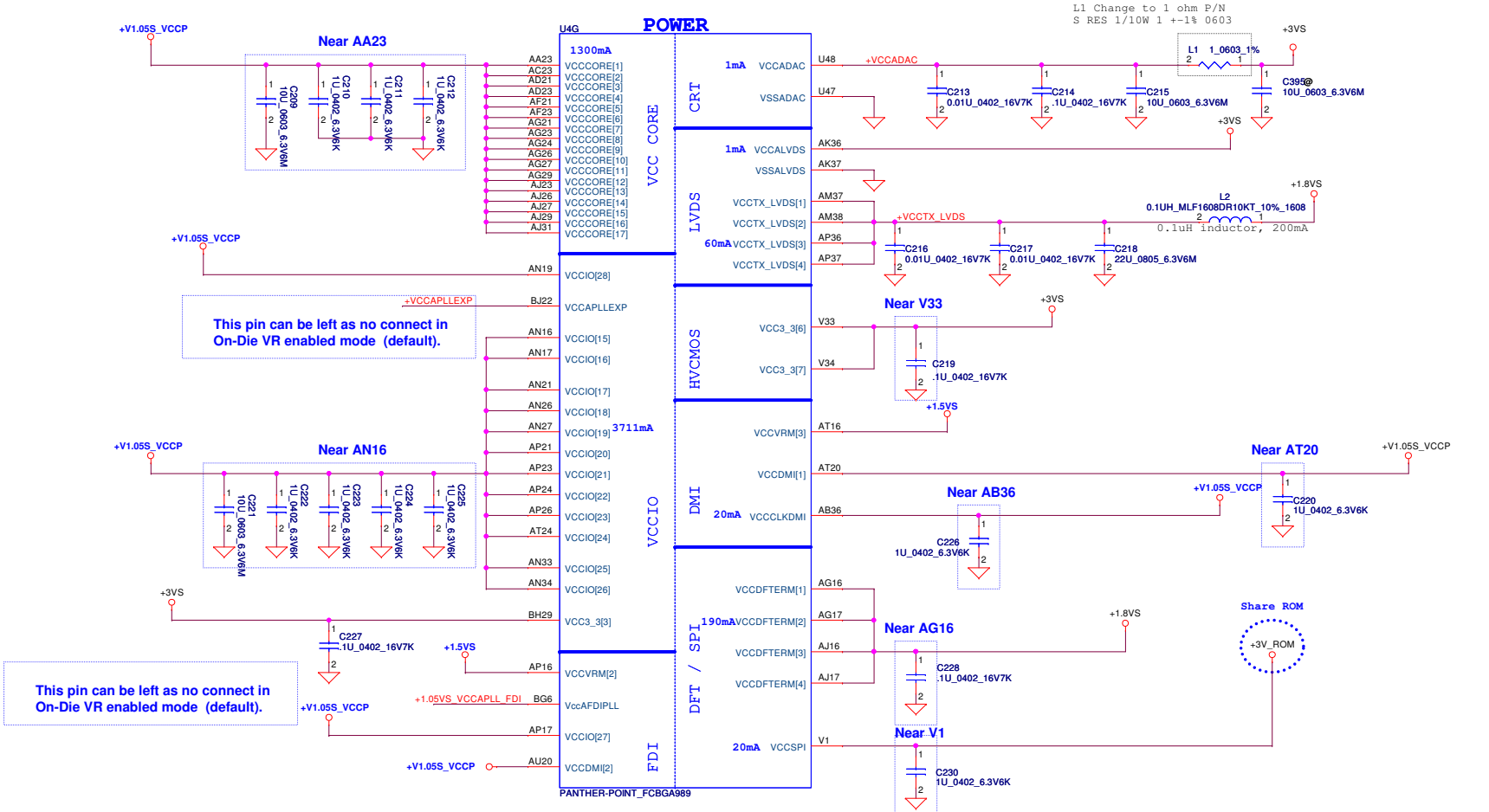
PCH_GPIO38	PCH_GPIO67	Function
0	0	SG(Optimus / PX)
0	1	Reserved
1	0	DIS
1	1	UMA



DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
NV_CLE	Set to Vss when LOW

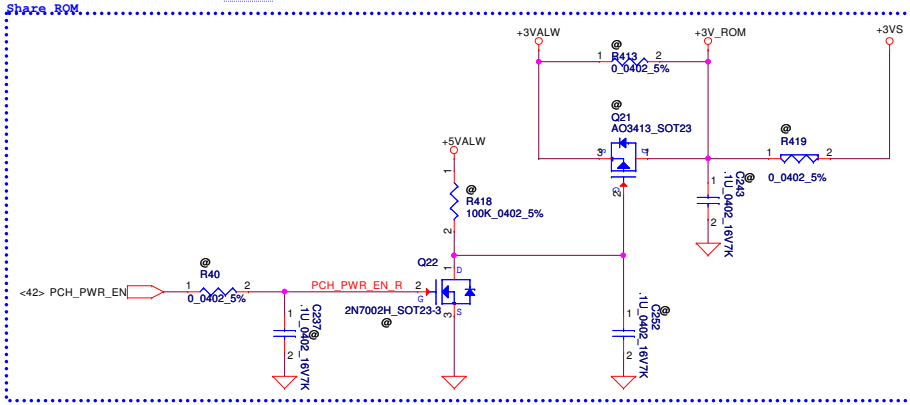
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Date:	Wednesday, February 27, 2013	Sheet	19 of 60

PCH Power Rail Table		
Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



This pin can be left as no connect in On-Die VR enabled mode (default).

This pin can be left as no connect in On-Die VR enabled mode (default).

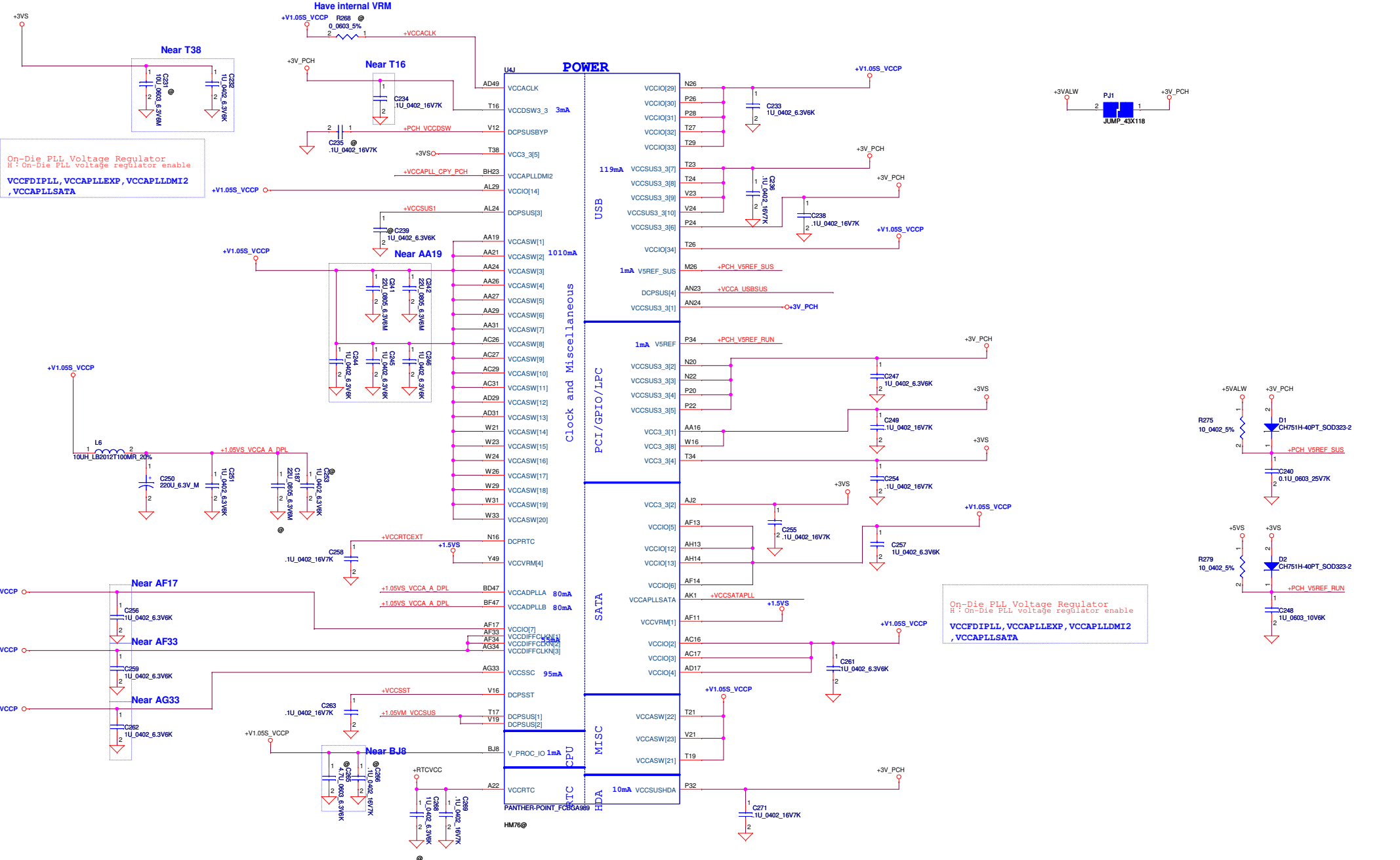


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PCH (719) PWR	
Document Number	LA-9631P
Date:	Wednesday, February 27, 2013
Sheet	20 of 60

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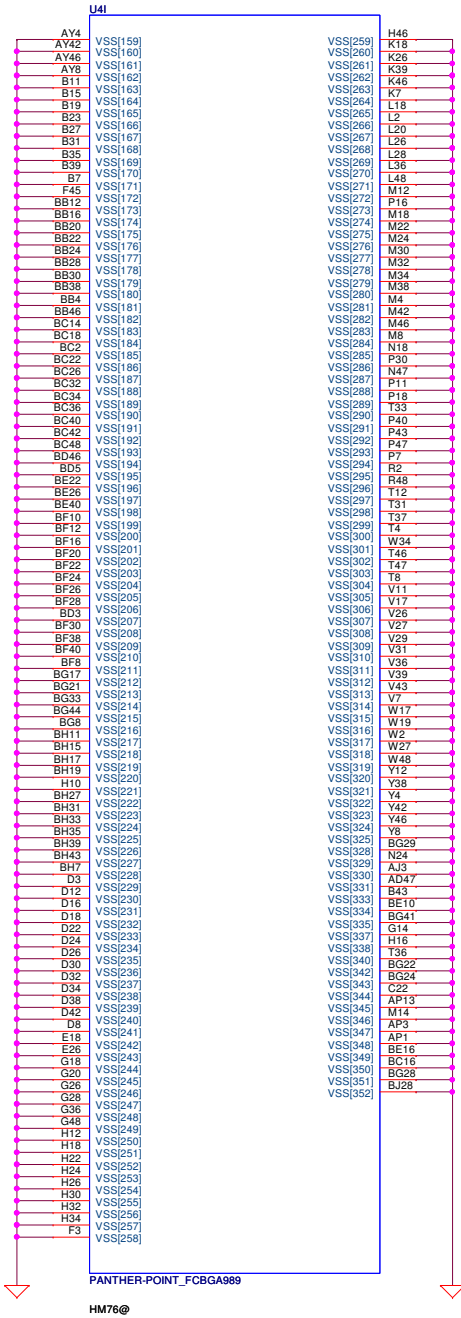
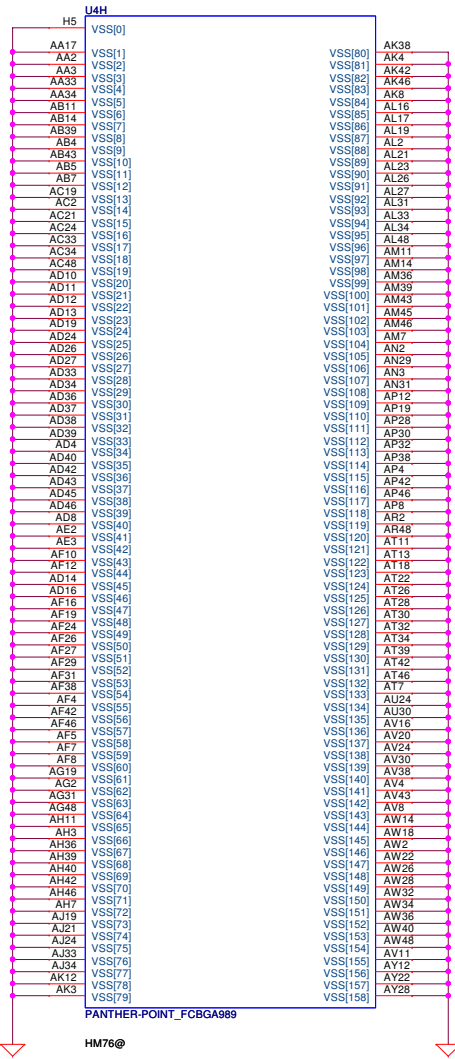
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On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
**VCCFDIPLL, VCCAPLEXP, VCCAPLLDMI2
 ,VCCAPLLSATA**

On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
**VCCFDIPLL, VCCAPLEXP, VCCAPLLDMI2
 ,VCCAPLLSATA**

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Size	Document Number	Date		Sheet	Rev
Custom	LA-9631P	Wednesday, February 27, 2013		21	1.0
			of 60		



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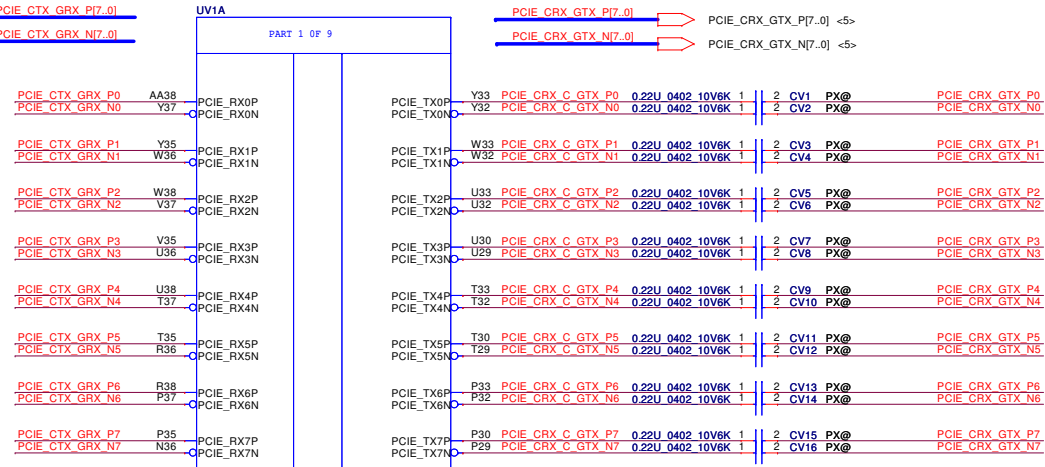
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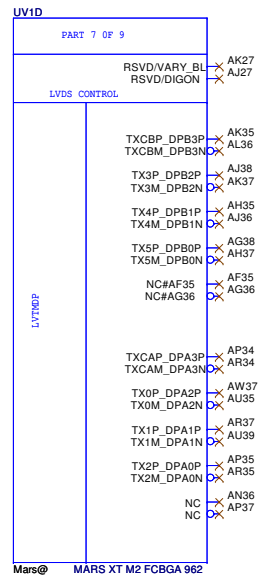
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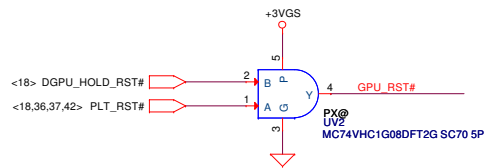
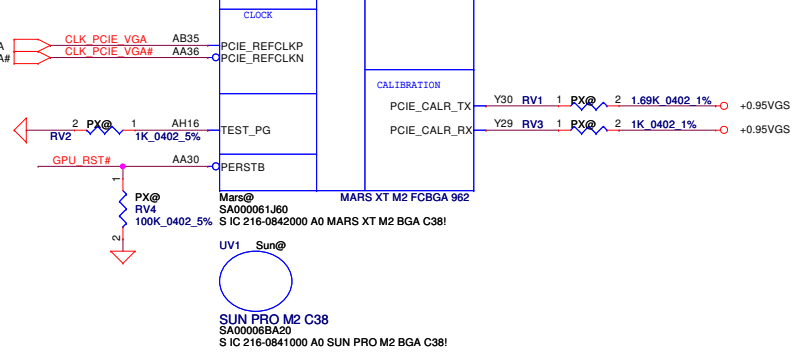


LVDS Interface



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<15> CLK_PCIE_VGA# CLK_PCIE_VGA#

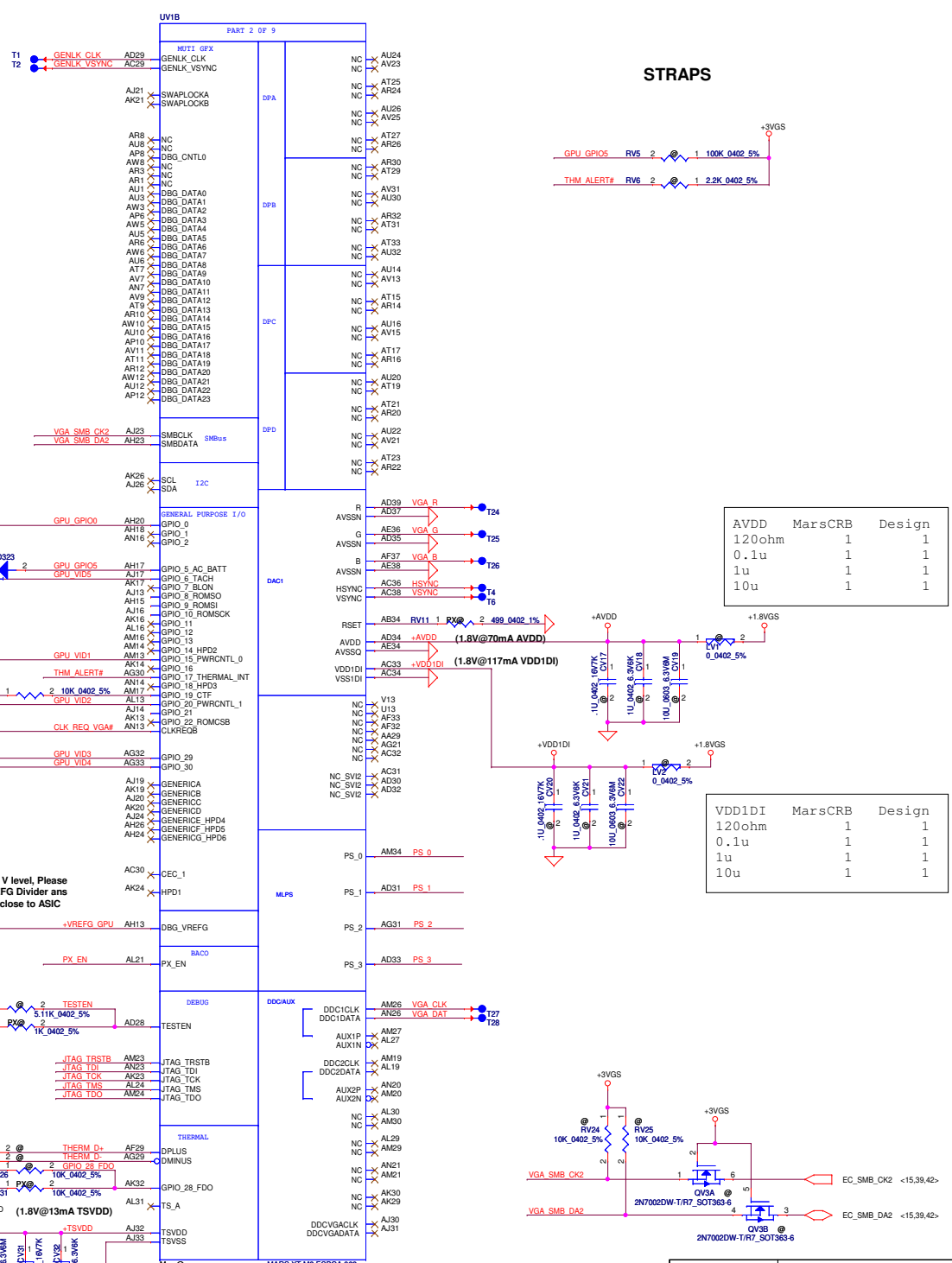


Mars@ SA000061J80 S IC 216-0842000 A0 MARS XT M2 BGA C38!

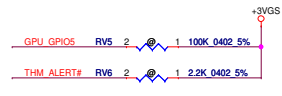
SUN PRO M2 C38 SA00006BA20 S IC 216-0841000 A0 SUN PRO M2 BGA C38!

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Date								Wednesday, March 06, 2013					
Sheet								23 of 60					

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STRAPS



AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

GPIO 28 FDO	MLPS
H	Disable
L	Enable

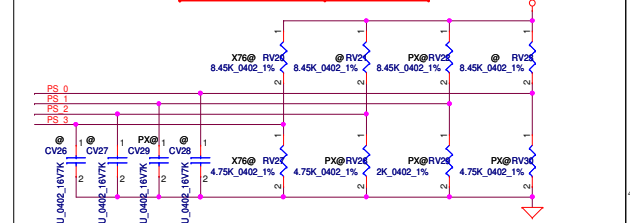
TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRs_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M2SP05A (ST) 101 - 1Mbit M2SP10A (ST) 101 - 2Mbit M2SP20 (ST) 101 - 4Mbit M2SP40 (ST) 101 - 8Mbit M2SP80 (ST) 100 - 512Kbit Pm2SLV010 (Chingss) 101 - 1Mbit Pm2SLV010 (Chingss)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1]	NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	11	000	NC	NC	4.75k
PS_1[5:1]	01	001	82nF	8.45k	2k
PS_2[5:1]	11	000	NC	NC	4.75k
PS_3[5:1]	11	XXX	NC	X	X

Mapping to VRAM type please refer to page 4

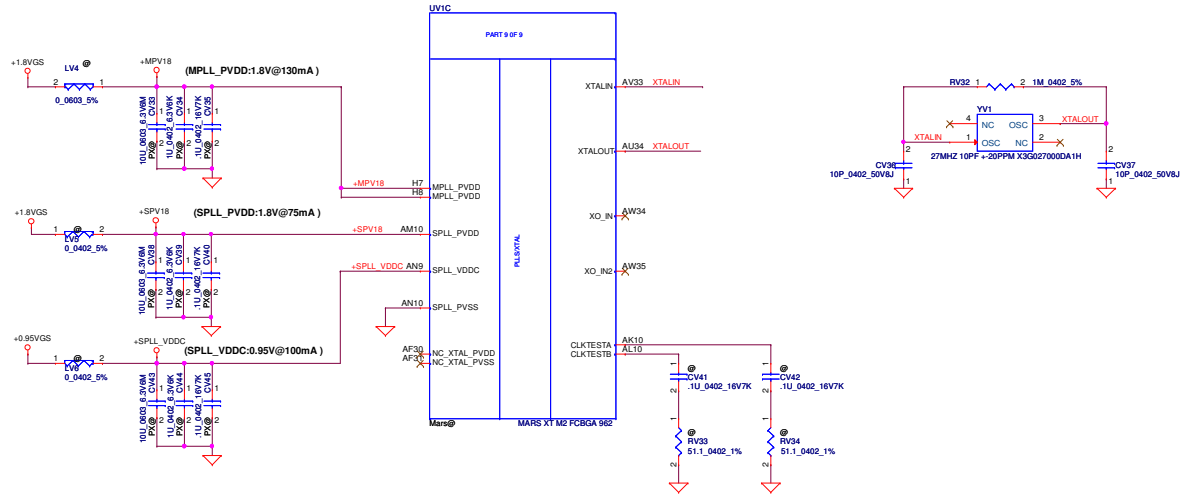


Place CLOSE VGA CHIP

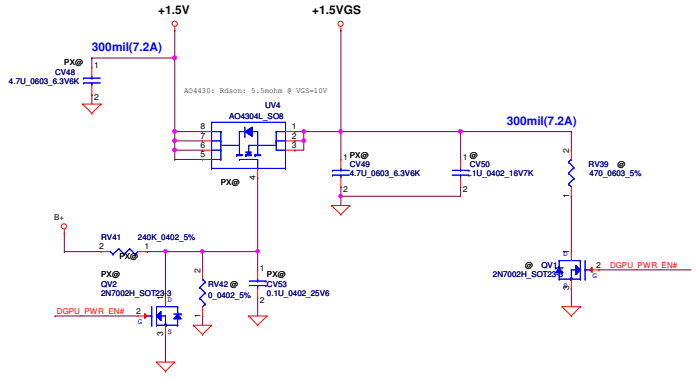
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

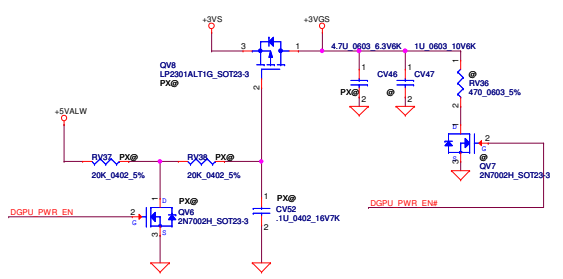
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



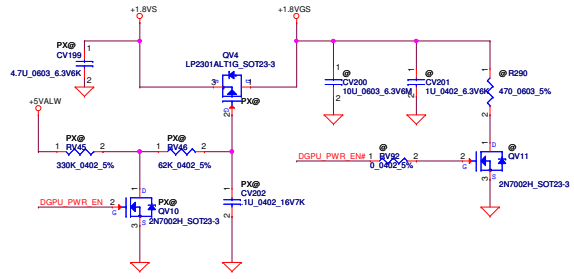
+1.5V to +1.5VGS



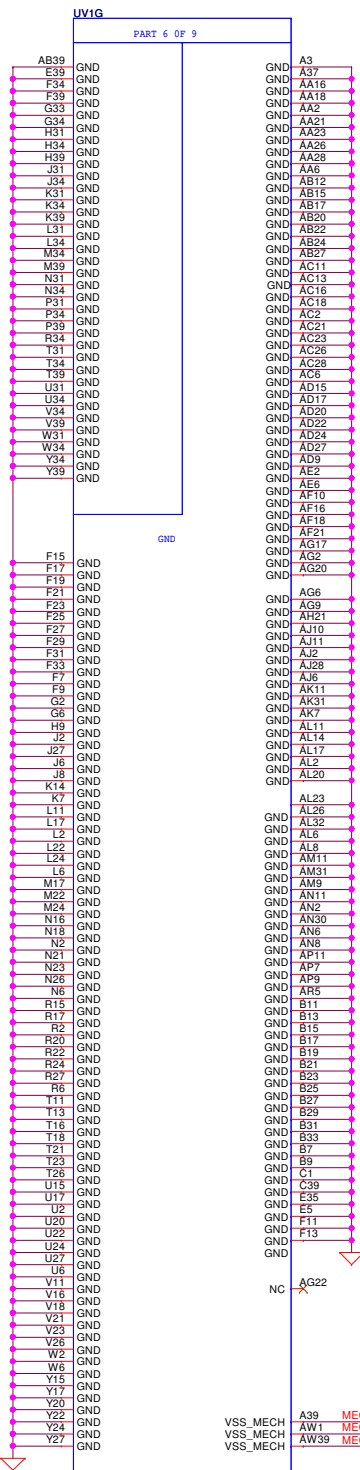
+3VS to +3VGS



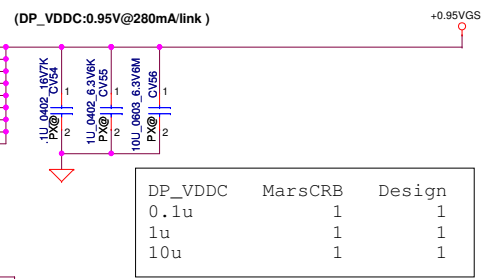
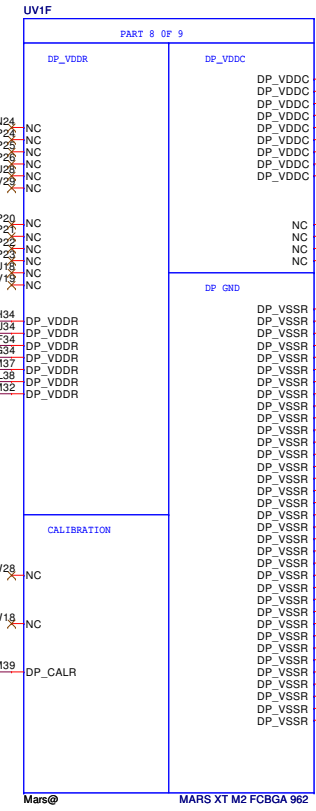
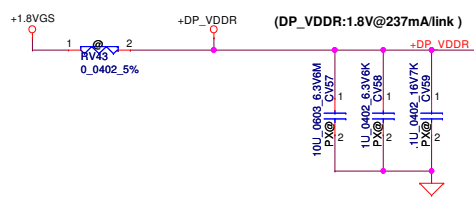
+1.8VS to +1.8VGS



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www.laptopfix.vn		Document Number	Rev. 1.0
		Issue Date	February 27, 2012
		Page	2 of 80



DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1



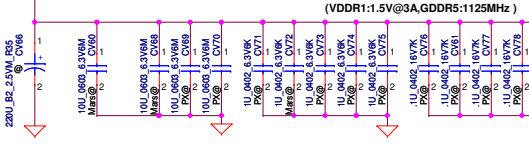
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AT1 MarsXTX M2 PWR GND		Document Number	
LA-9631P		Rev 1.0	
Date: Wednesday, February 27, 2013		Sheet 26 of 60	

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For GDDR5, MVDDQ = 1.5V
(VDDR1:1.5V@3A,GDDR5:1125MHz)

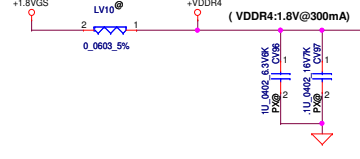
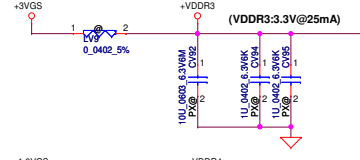
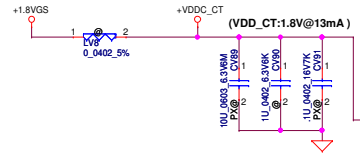


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

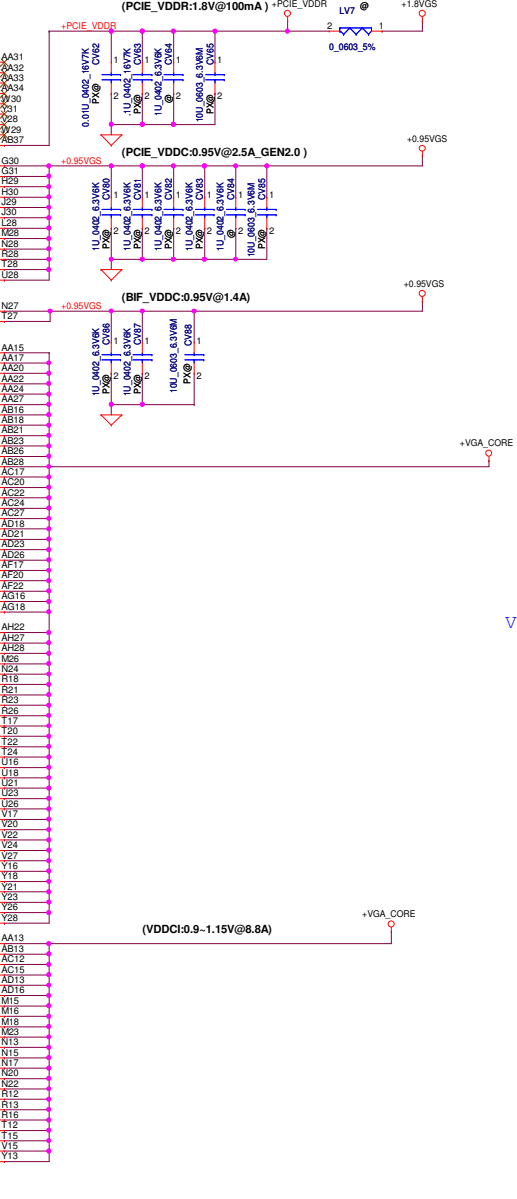
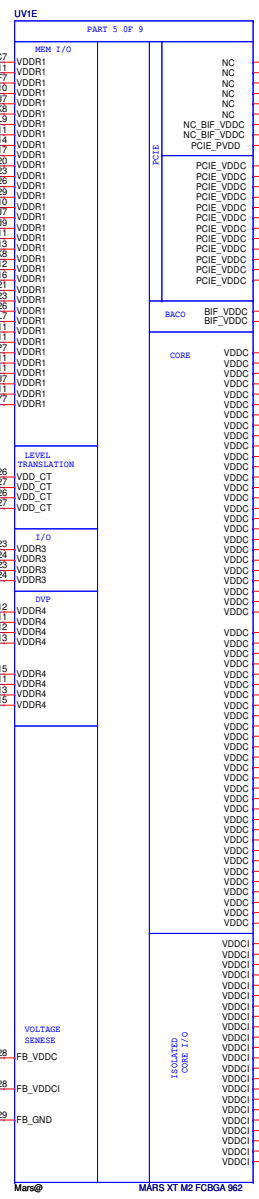
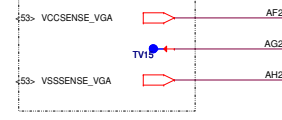
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



Route as differential pair



PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

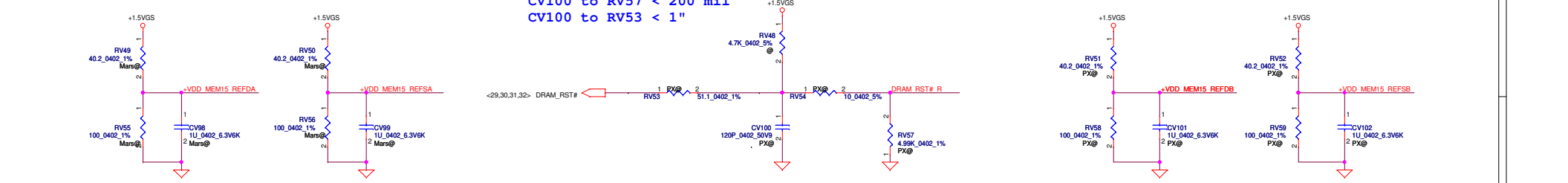
PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VGA_CORE Cap in power side sheet

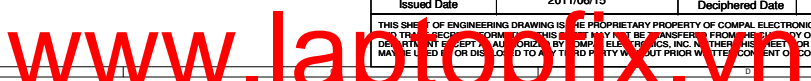
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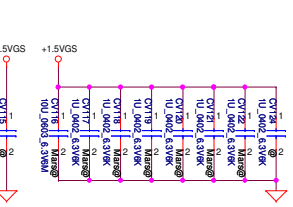
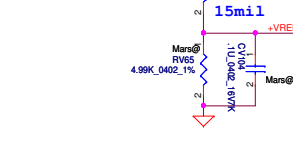
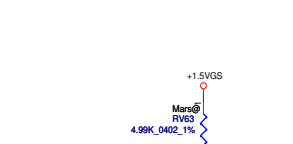
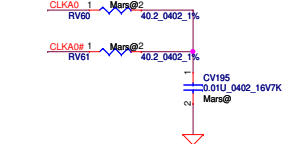
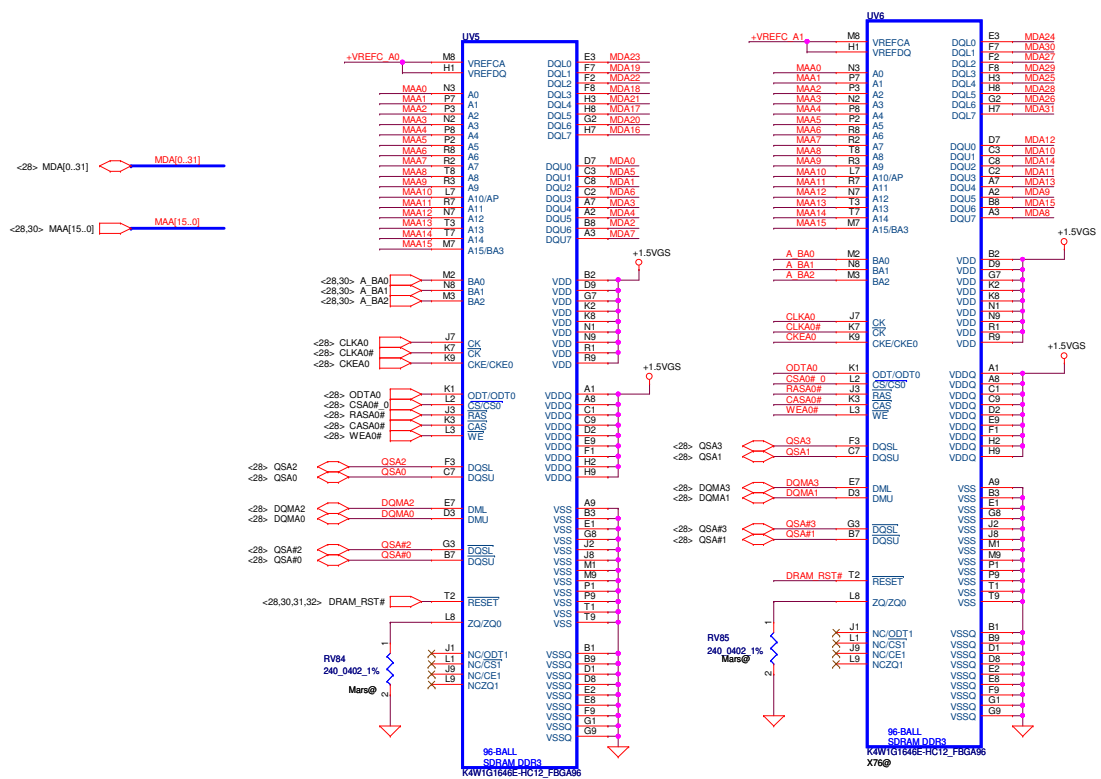


Ball to RV57 < 1"
 CV100 to RV53 < 200 mil
 CV100 to RV53 < 1"



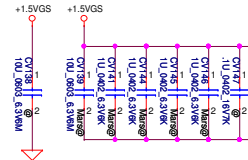
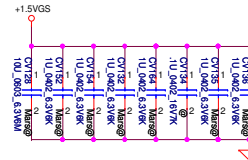
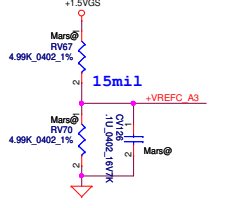
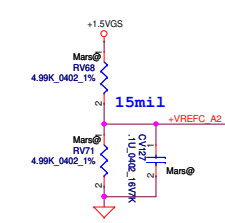
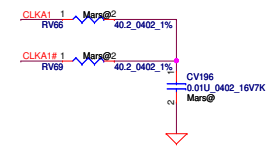
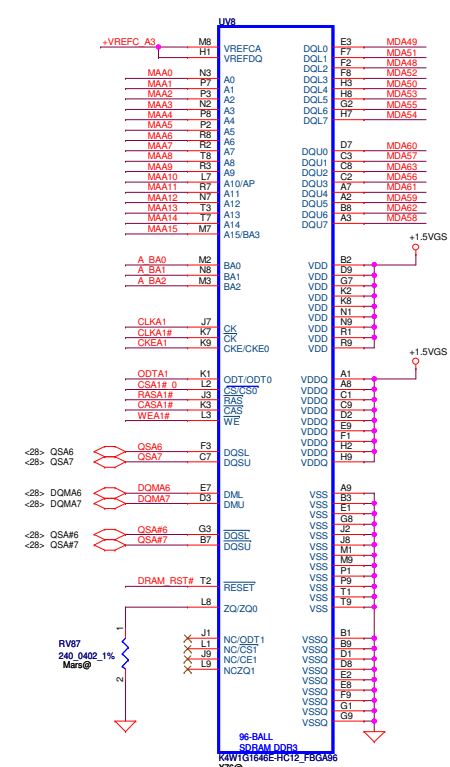
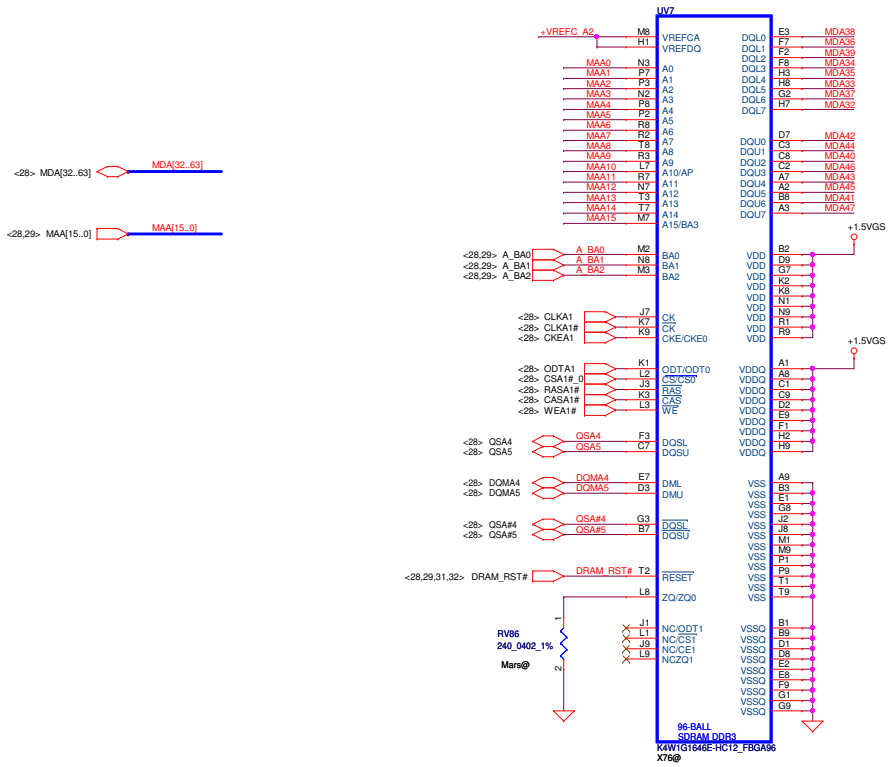
DRAM_RST# is a daisy-chain net that connects to all VRAM
 This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and |I| Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.
 Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2





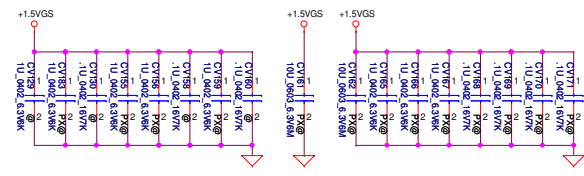
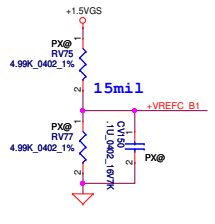
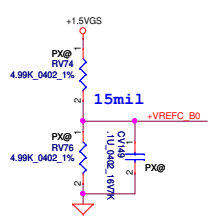
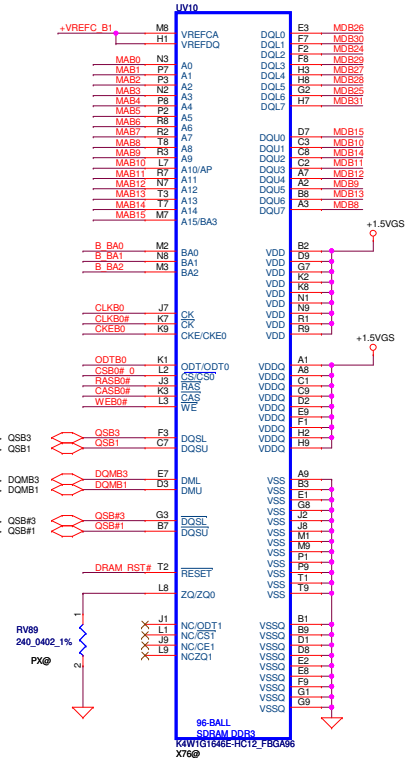
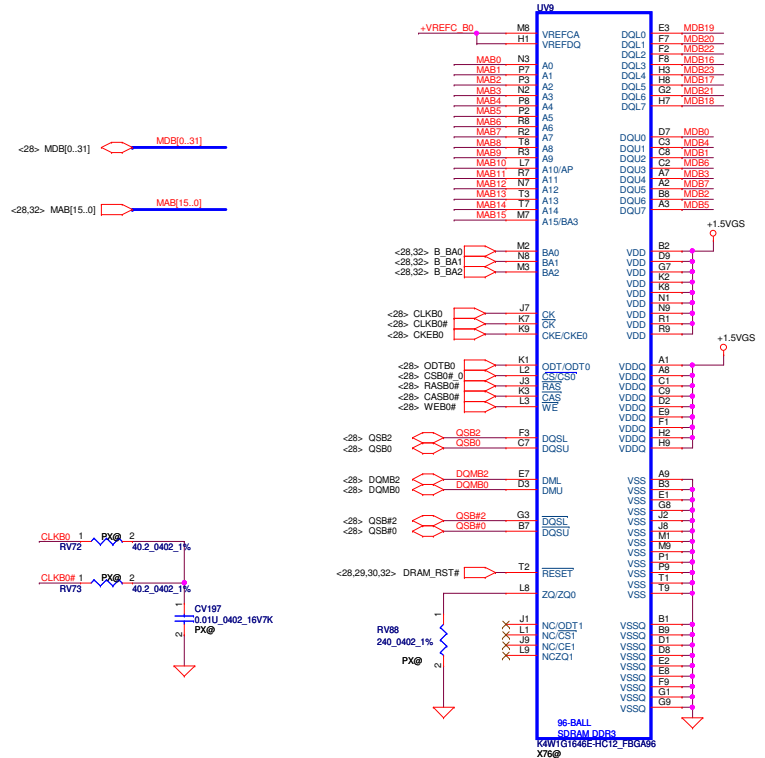
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Size	Document Number	Rev	1.0
Date:	Wednesday, February 27, 2013	Sheet	29 of 60

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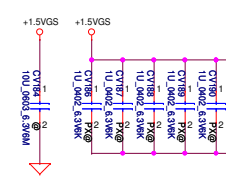
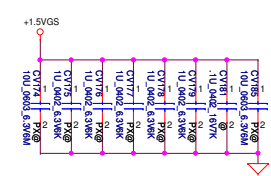
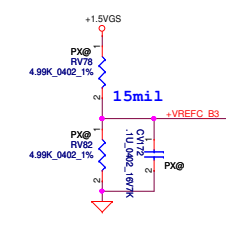
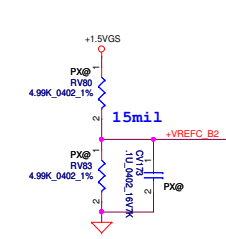
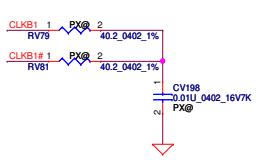
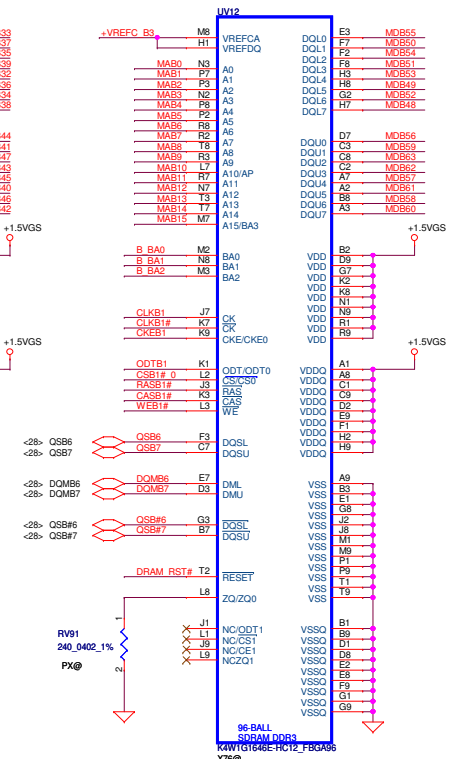
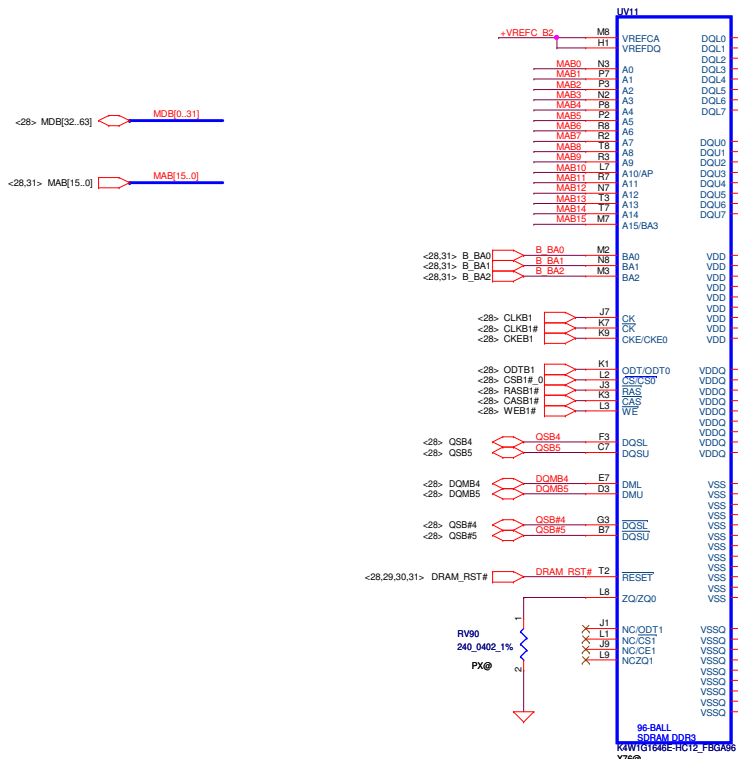
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Size	C	Document Number	LA-9631P
Date:	Wednesday, February 27, 2013	Sheet	30 of 60

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Title			ATI Whistler M2 VRAM B
Document Number			LA-9631P
Date:			Wednesday, February 27, 2013
Sheet			31 of 60

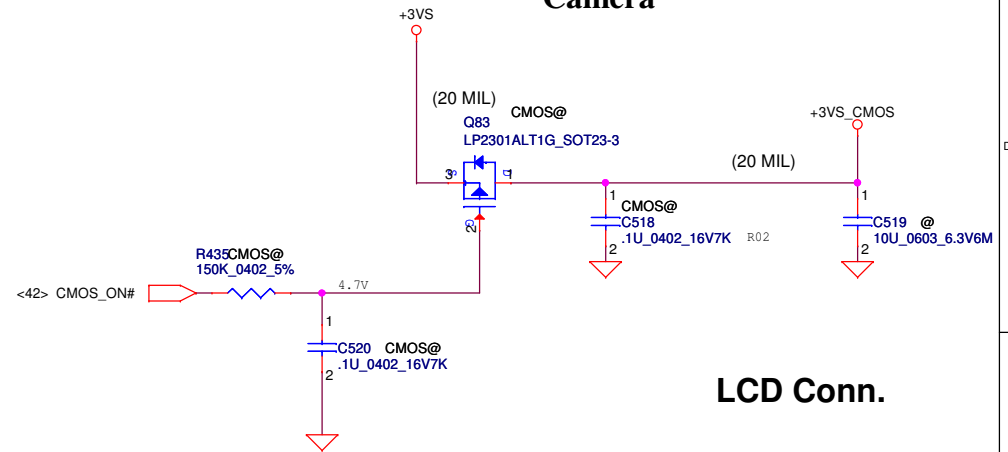
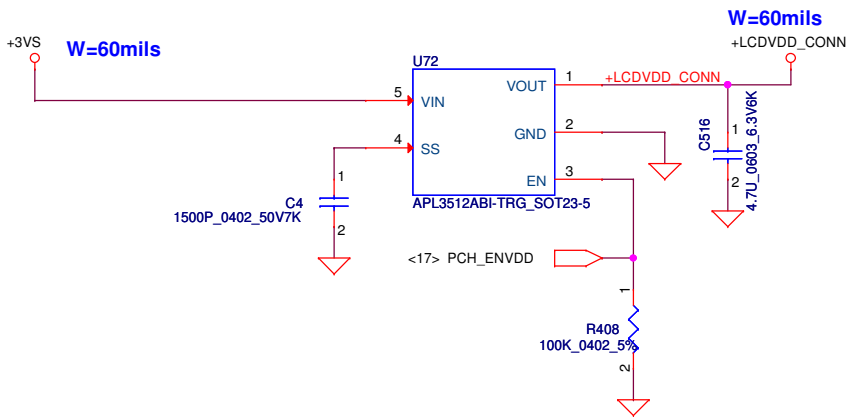
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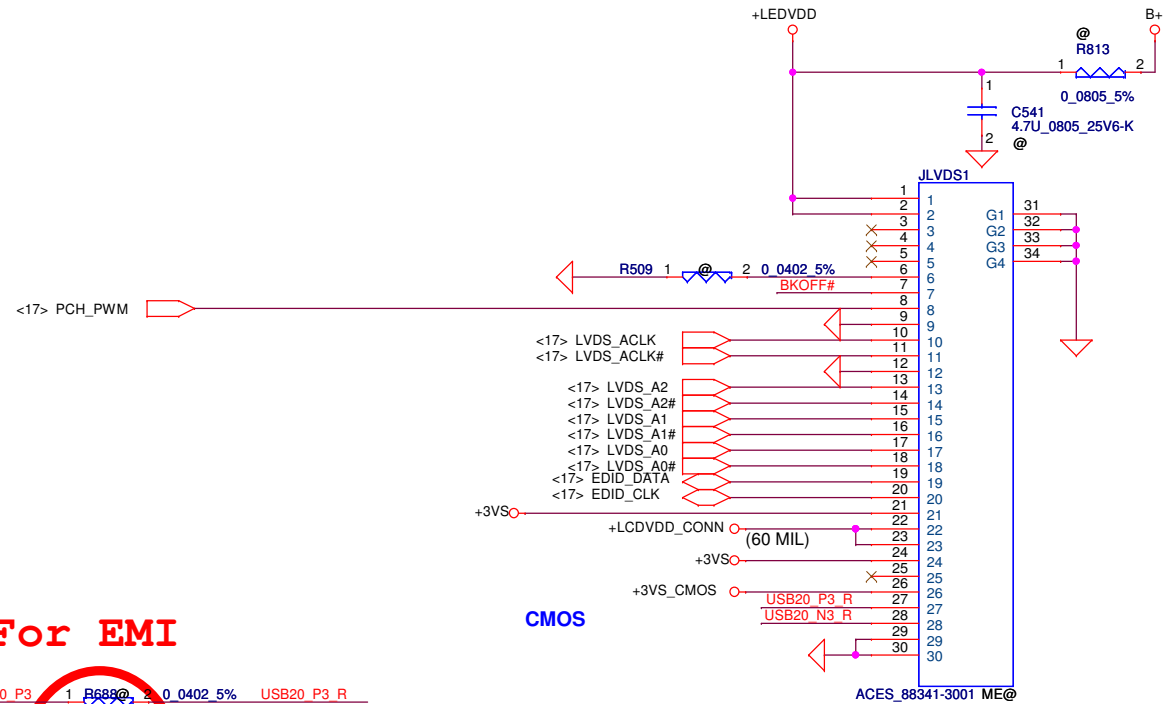
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Size	LA-9631P		Date:	Wednesday, February 27, 2013	Sheet	32 of 60

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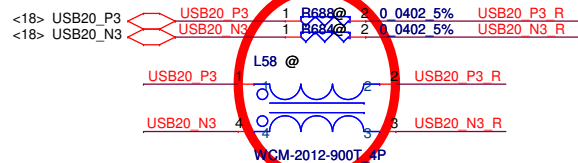
LCD POWER CIRCUIT



LCD Conn.

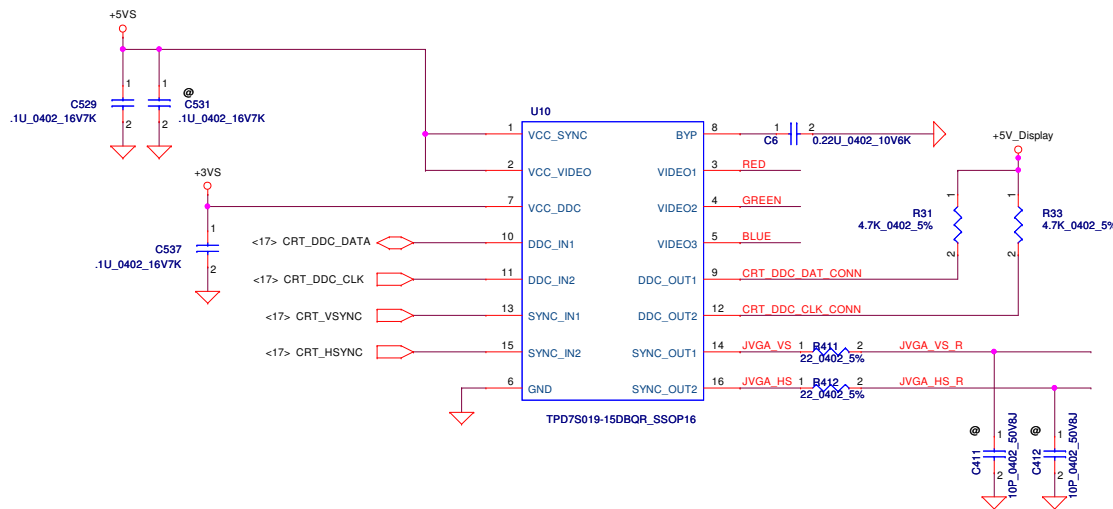
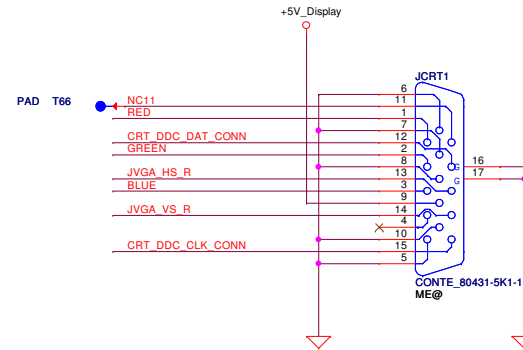
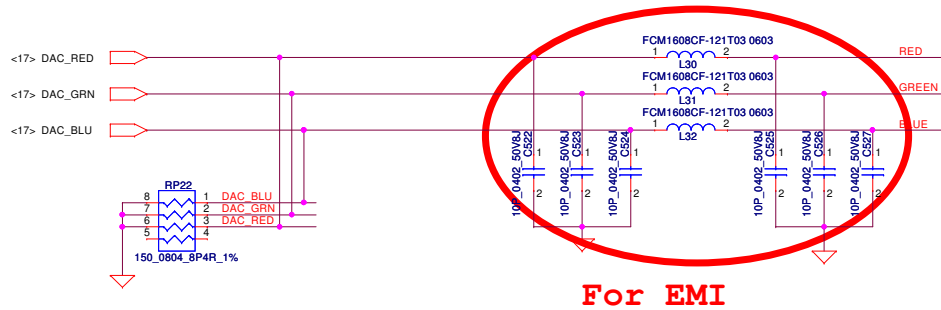


For EMI



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				Custom	LA-9631P		1.0
Date:	Wednesday, February 27, 2013	Sheet	33	of	60		

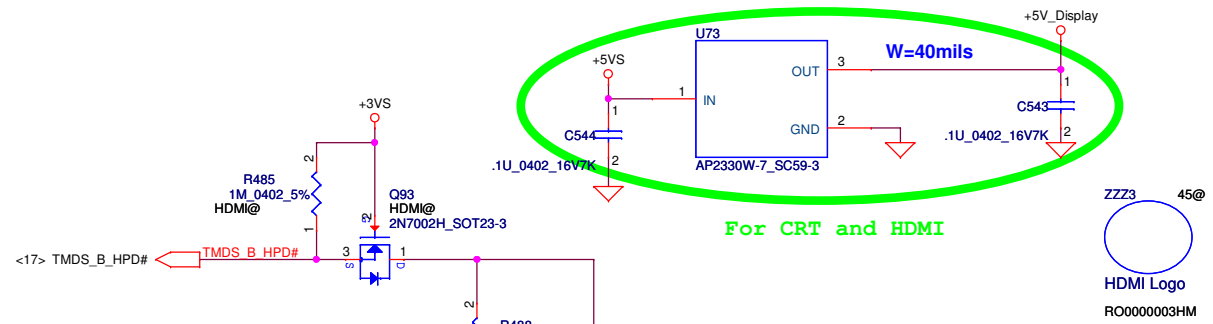
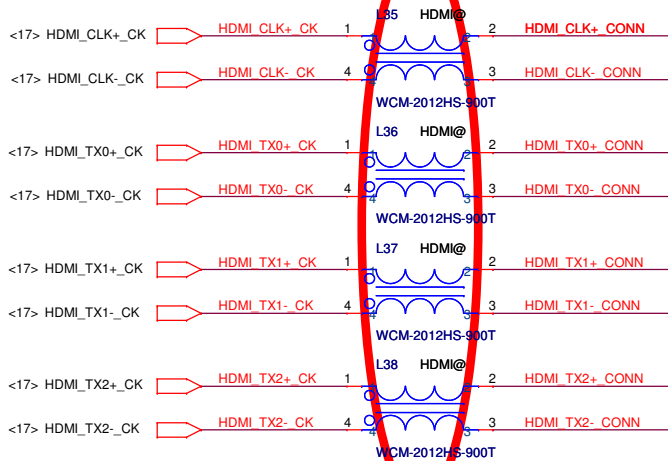
www.laptopfix.vn



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				LA-9631P	1.0
				Date:	Wednesday, February 27, 2013
				Sheet	34 of 60

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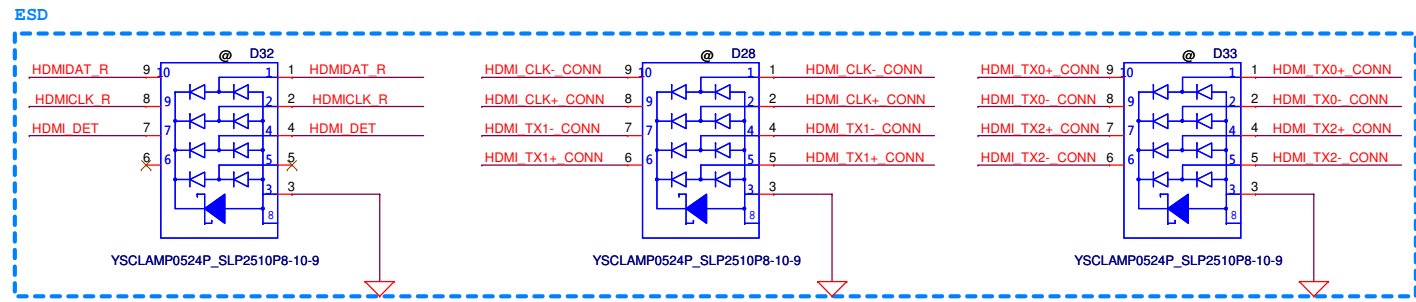
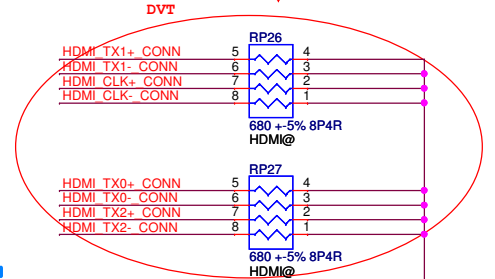
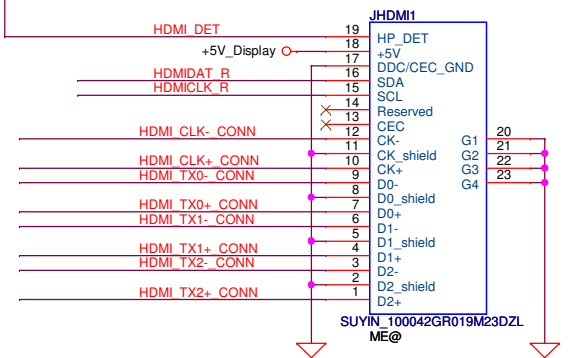
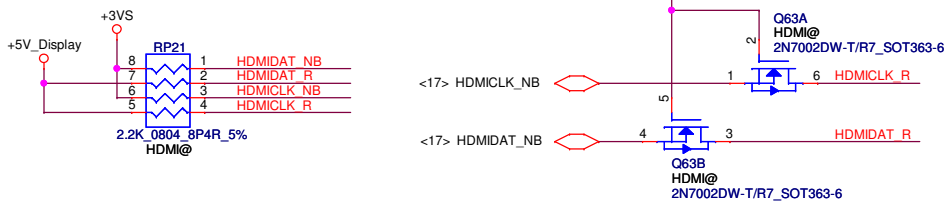
For EMI



For CRT and HDMI

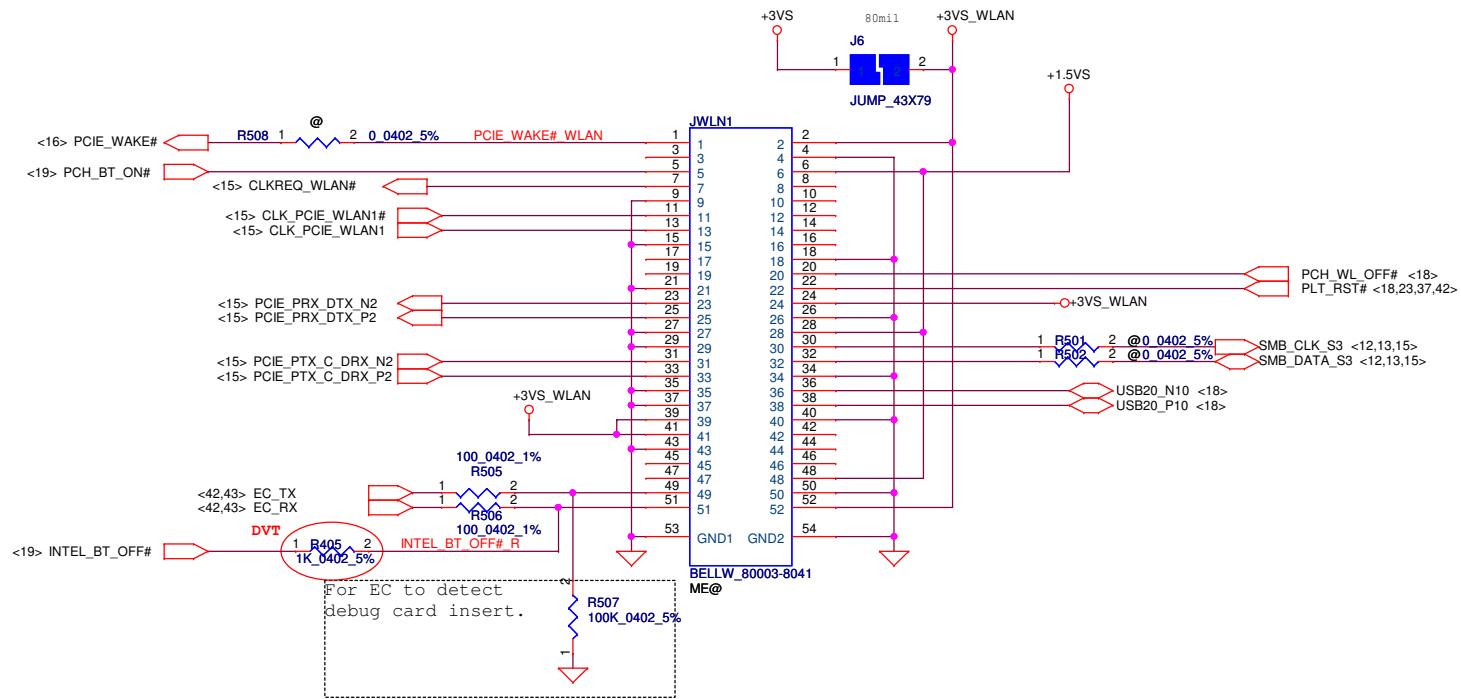


Pull up R for PCH OR VGA SIDE



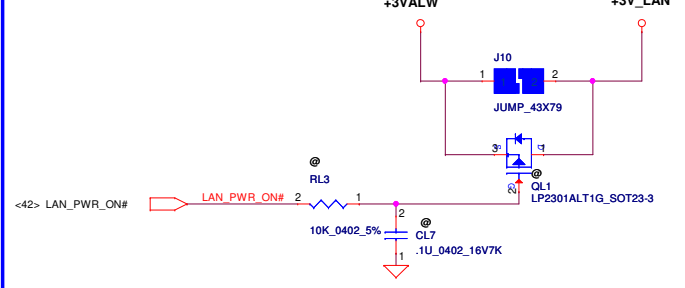
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				HDMI CONN	
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				LA-9631P	1.0
				Date: Wednesday, February 27, 2013	Sheet 35 of 60

Mini Card for WLAN/WiMAX(Half)

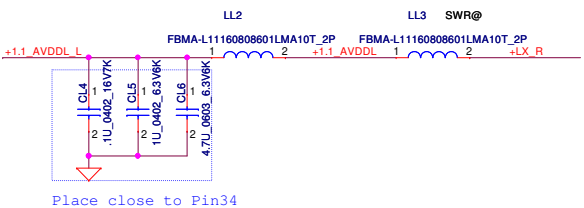
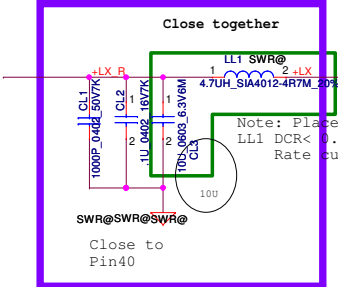
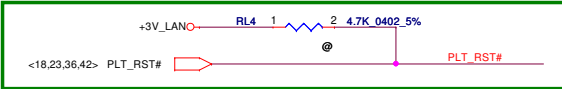


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title Mini-Card/NEW Card/SIM	
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				Date	Wednesday, February 27, 2013
				Sheet	36 of 60
				Rev	1.0

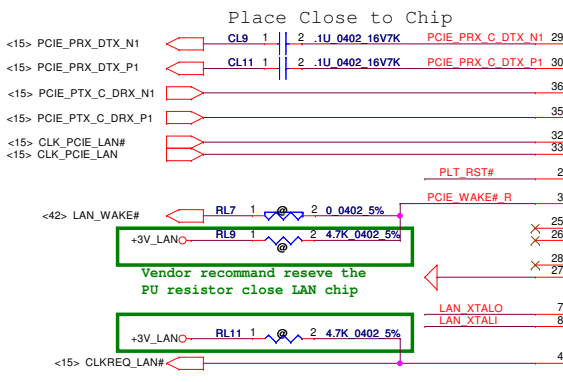
For LAN & Green CLK



Vendor recommend reseve the PU resistor close LAN chip

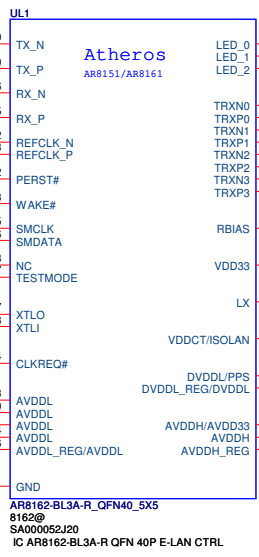


UL1 8172@
QCA8172-BL3A-R
 SA000065410
 S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL

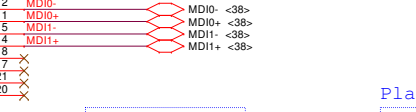


Vendor recommend reseve the PU resistor close LAN chip

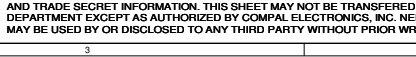
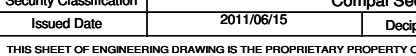
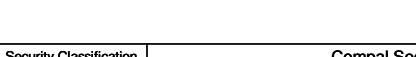
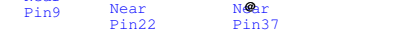
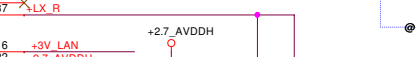
Near Pin13
 Near Pin19
 Near Pin31



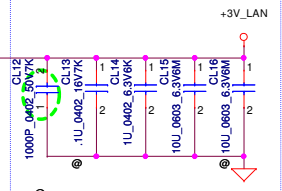
Atheros
 AR8151/AR8161



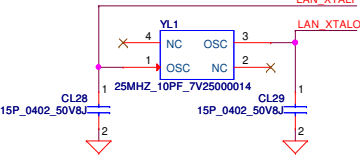
mount RL12 if use LDO modue



Place Close to PIN1



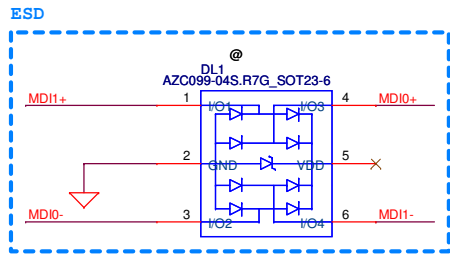
don't @ (could be B C cost done)



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Custom	LA-9631P	Wednesday, February 27, 2013		Sheet	37 of 60

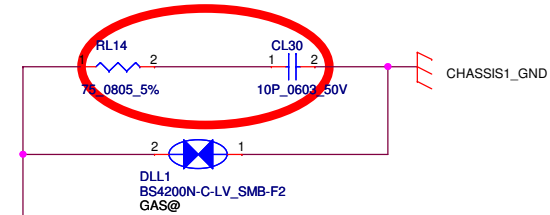
DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

Place Close to TL1



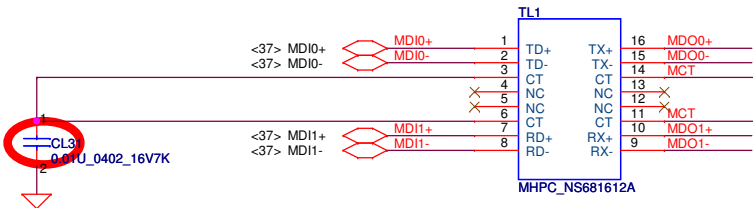
Reserve gas tube for EMI go rural solution

For EMI

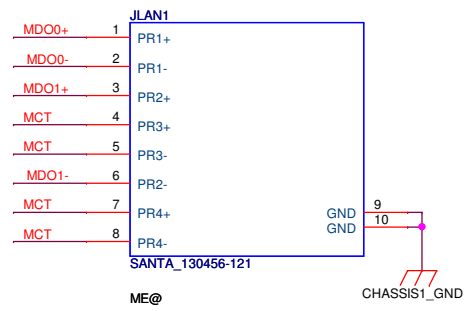
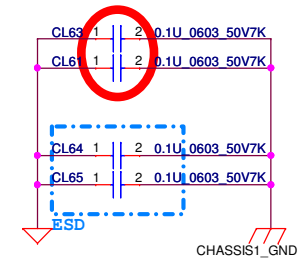


Place Close to TL1

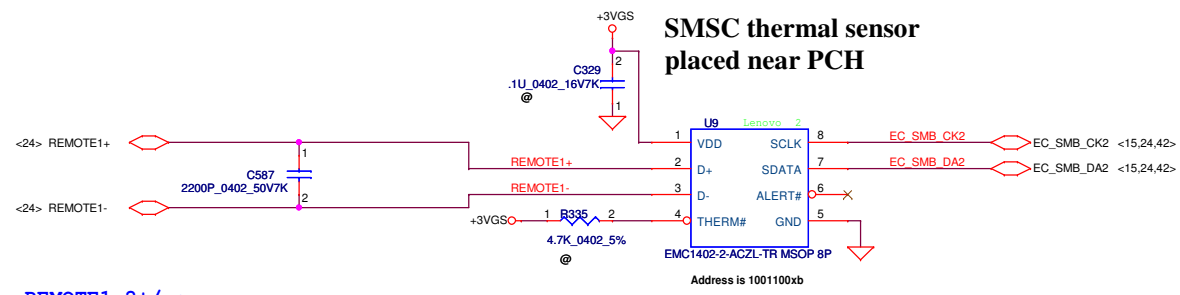
For EMI



For EMI



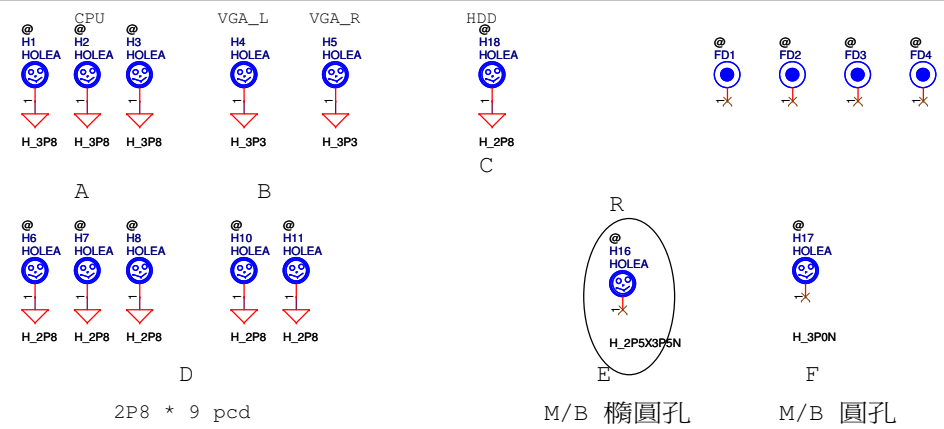
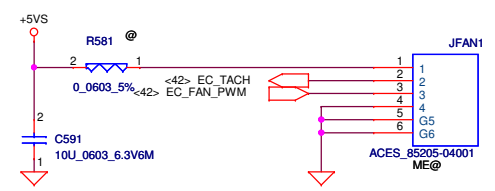
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				LA-9631P	
				Date:	Wednesday, February 27, 2013
				Sheet	38 of 60



SMSC thermal sensor placed near PCH

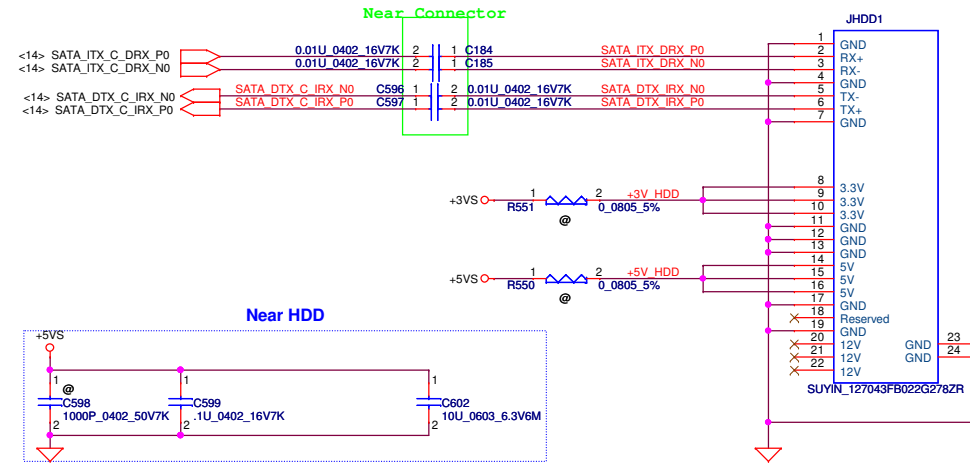
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

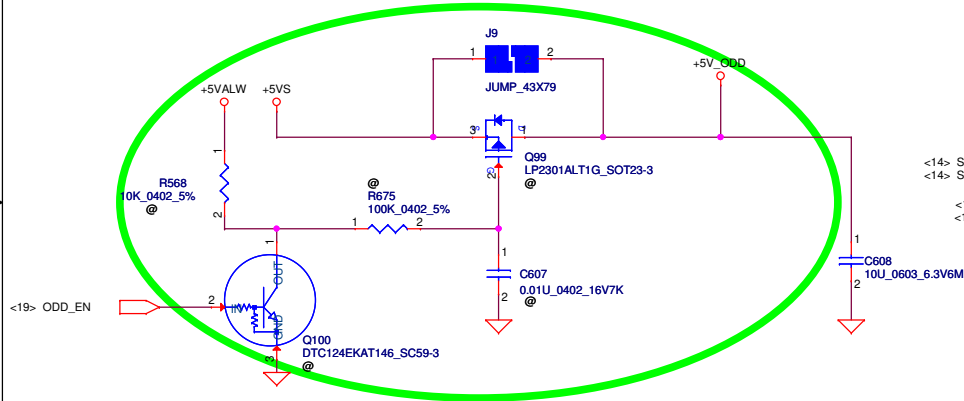


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				Rev	1.0
				Date	Wednesday, February 27, 2013
				Sheet	39 of 60

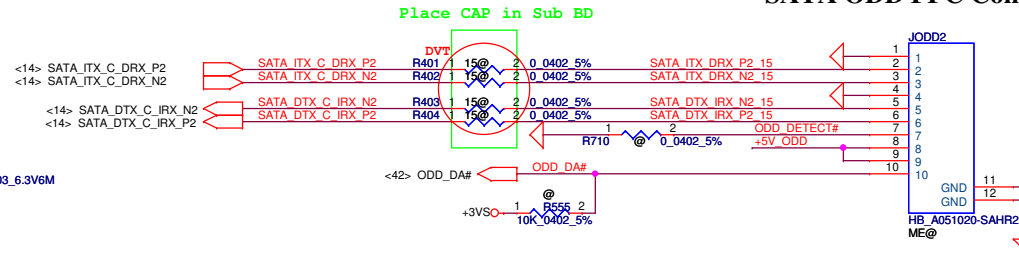
SATA HDD Conn.



ODD Power Control

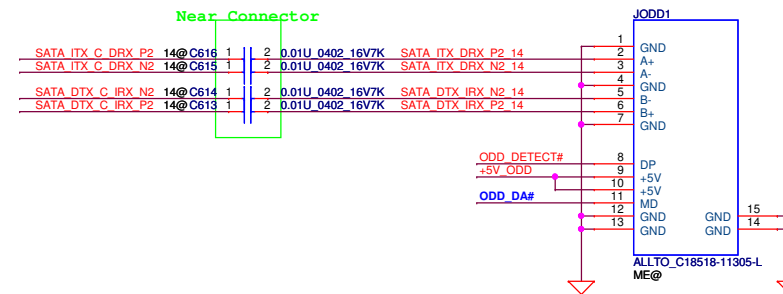


FOR 15" SATA ODD FFC Conn.



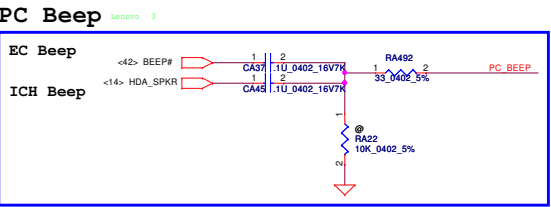
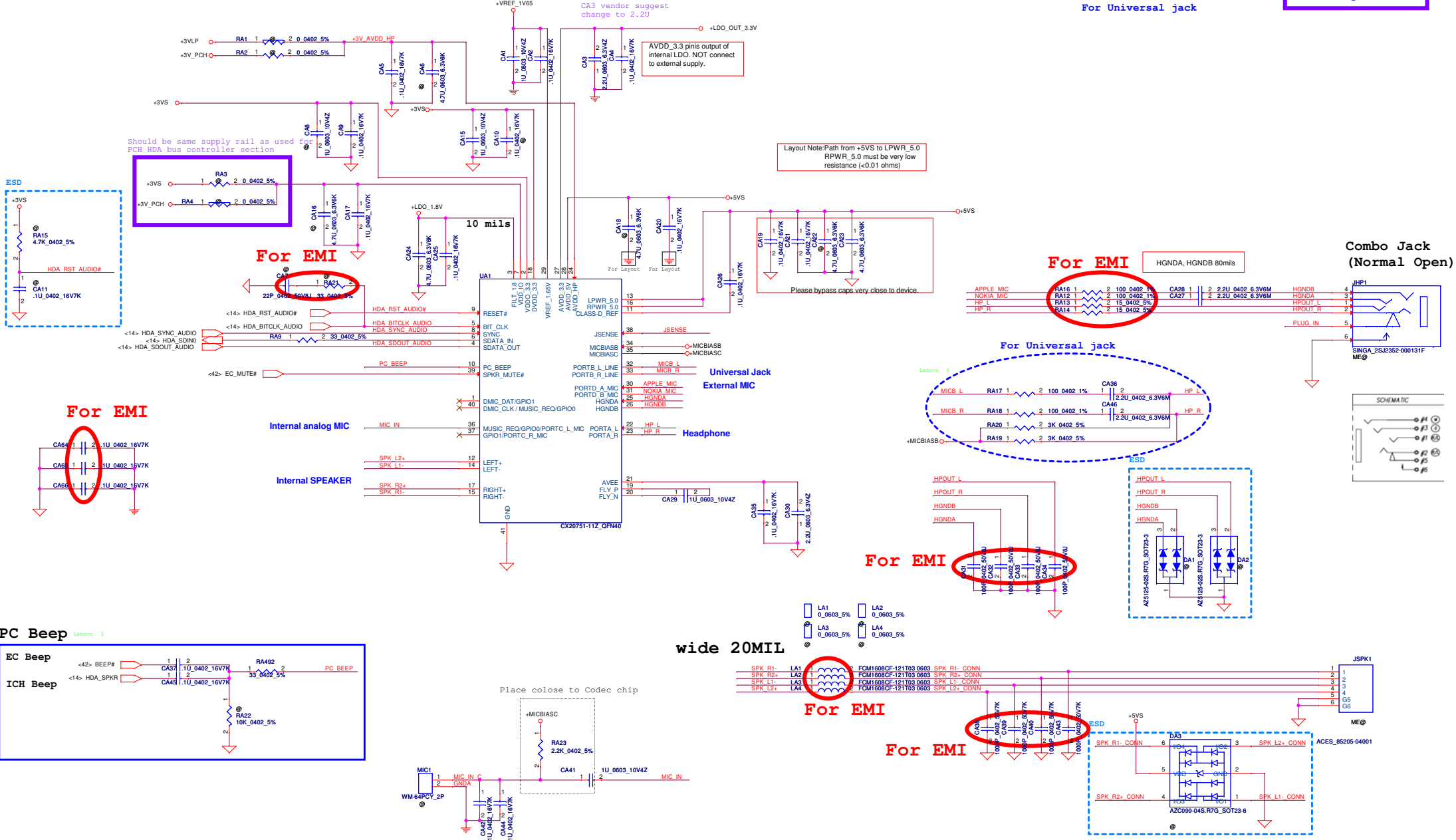
Co-lay

FOR 14" SATA ODD Conn.

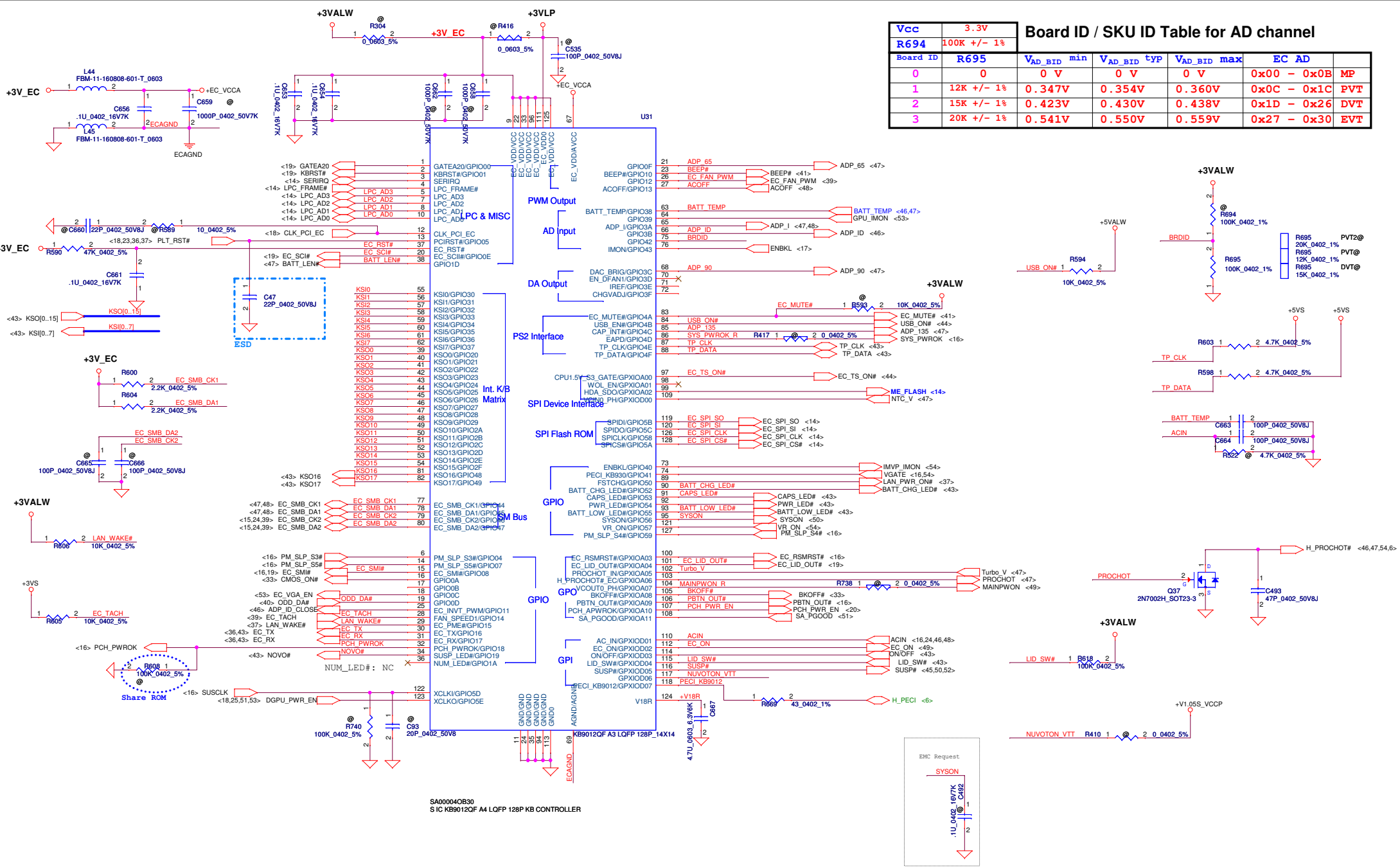


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				Document Number
				Custom
				LA-9631P
				Rev
				1.0
				Date
				Wednesday, February 27, 2013
				Sheet
				40 of 60

CX20751
 High Definition Audio Codec SoC
 With Integrated Class-D Stereo
 Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).

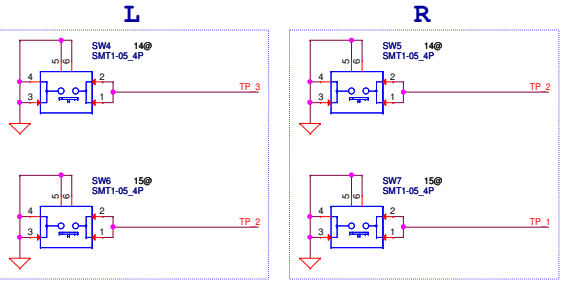
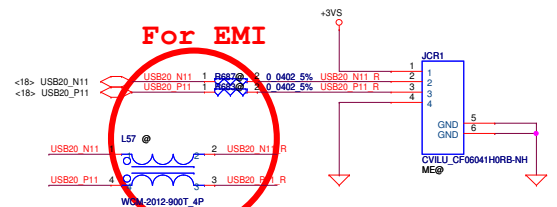
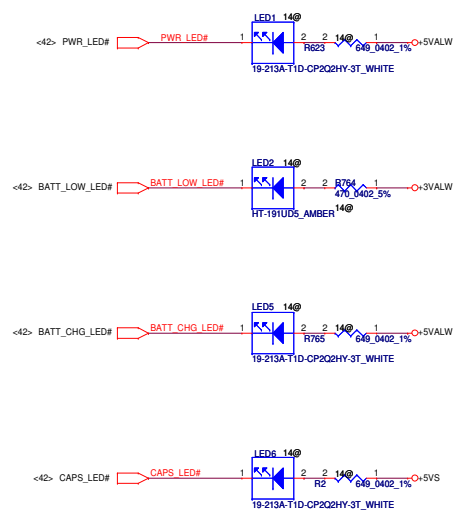
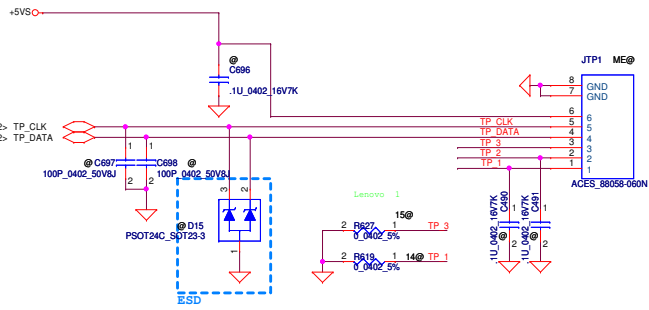
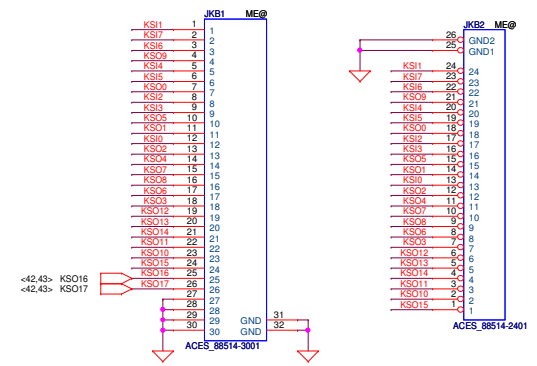
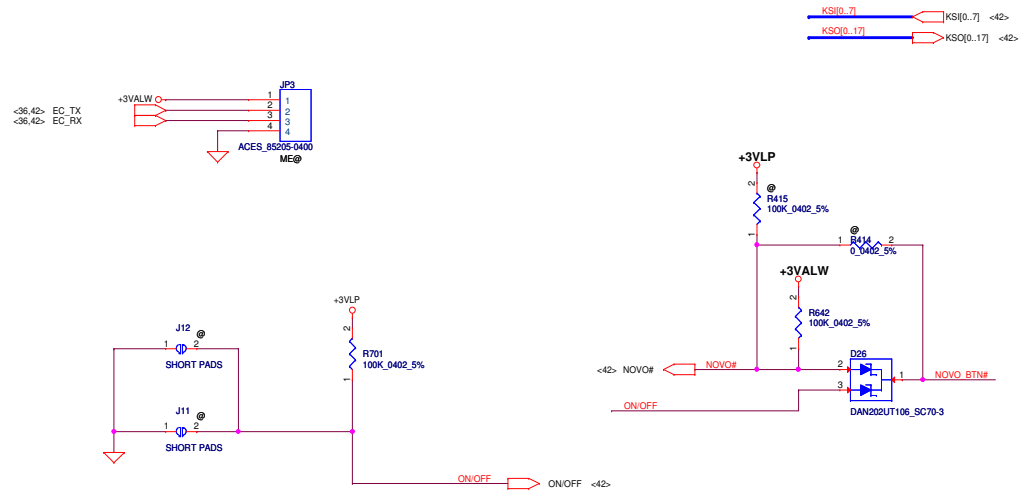


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				LA-9631P
				Rev 1.0
				Date: Tuesday, March 05, 2013
				Sheet 41 of 60

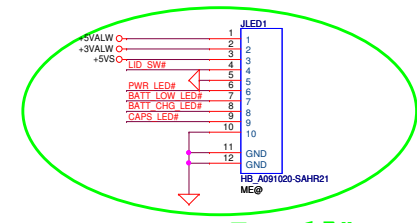
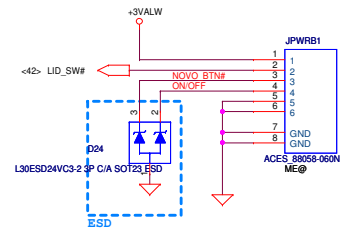


Vcc		3.3V			Board ID / SKU ID Table for AD channel		
R694	R695	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD		
0	0	0 V	0 V	0 V	0x00 - 0x0B	MP	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	DVT	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	EVT	

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Customer		Rev	1.0	LA-9631P	
Date:	Wednesday, March 06, 2013	Sheet	42	of 60	

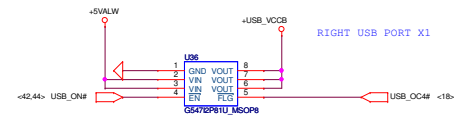


15/17"		14"	
1	VCC	1	VCC
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	L
5	L	5	R
6	R	6	GND

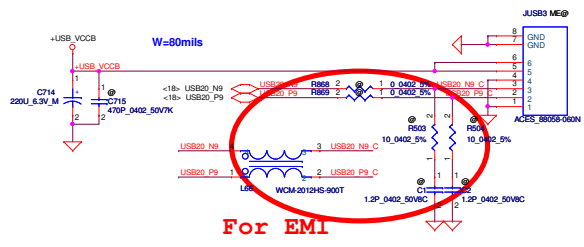


For 15"

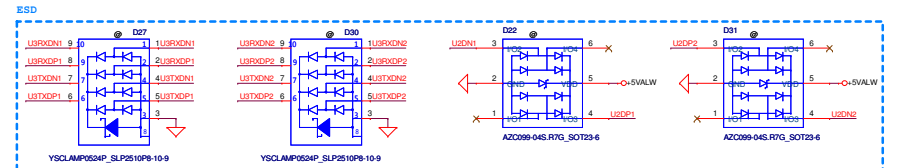
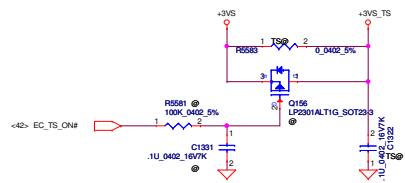
Ext. USB2.0



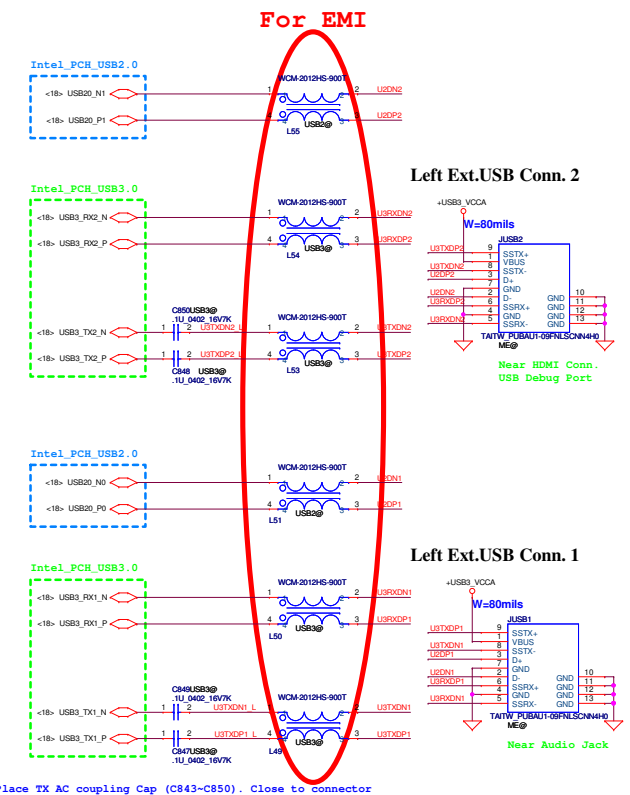
Right Ext.USB Conn.



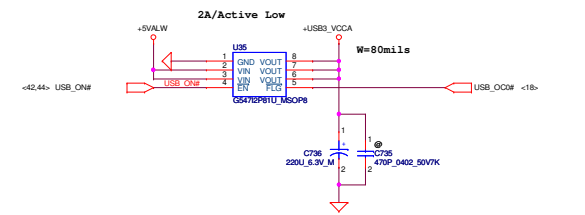
Touch Screen



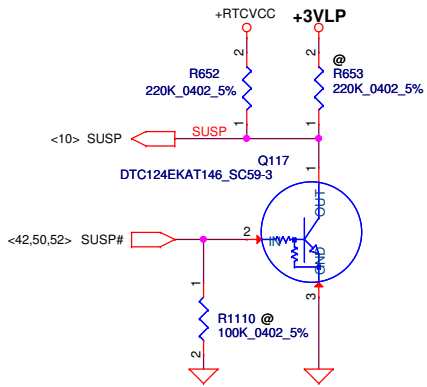
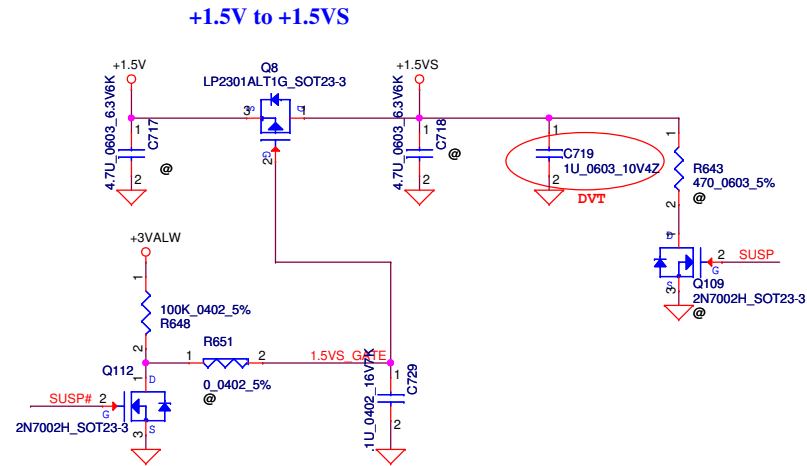
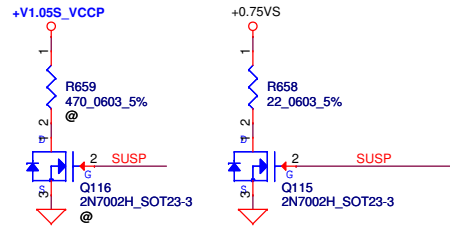
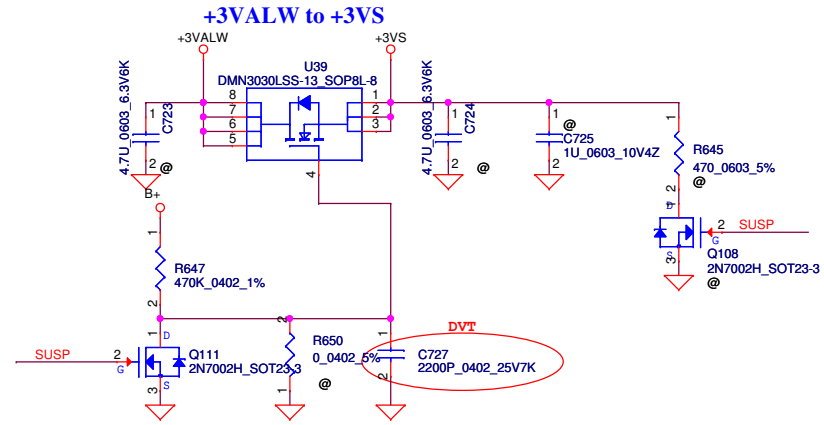
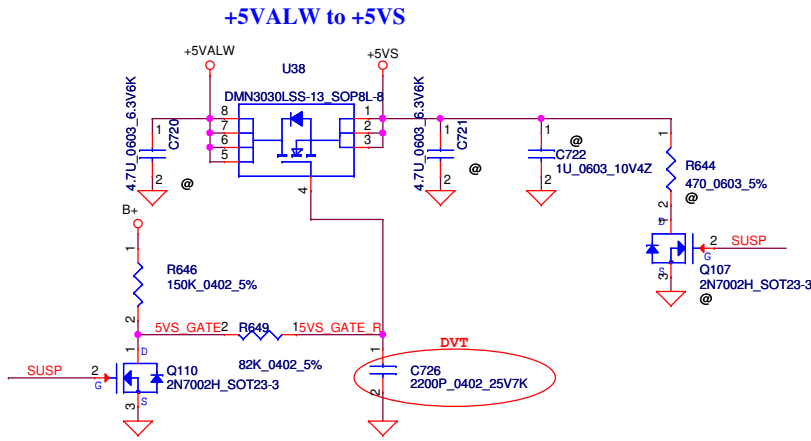
USB3.0



Place TX AC coupling Cap (C843-C850). Close to connector

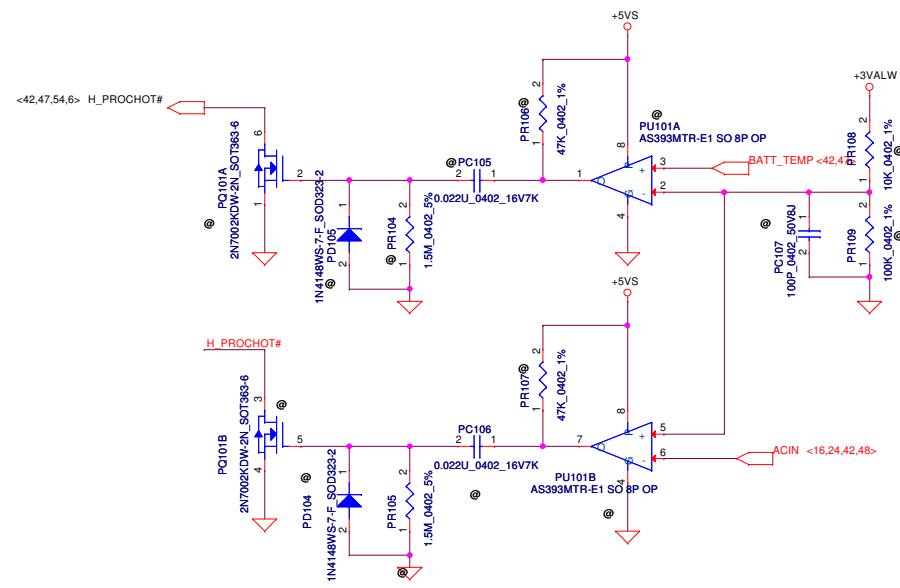
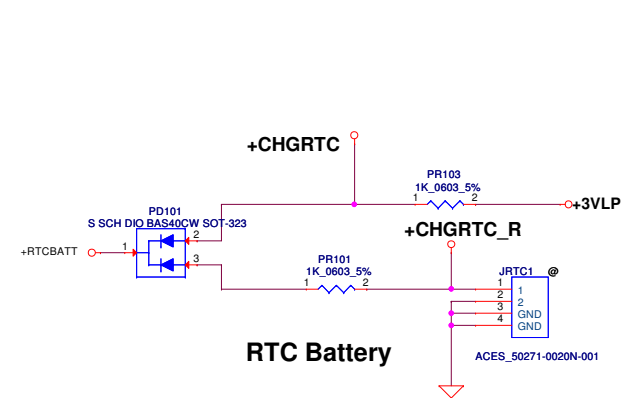
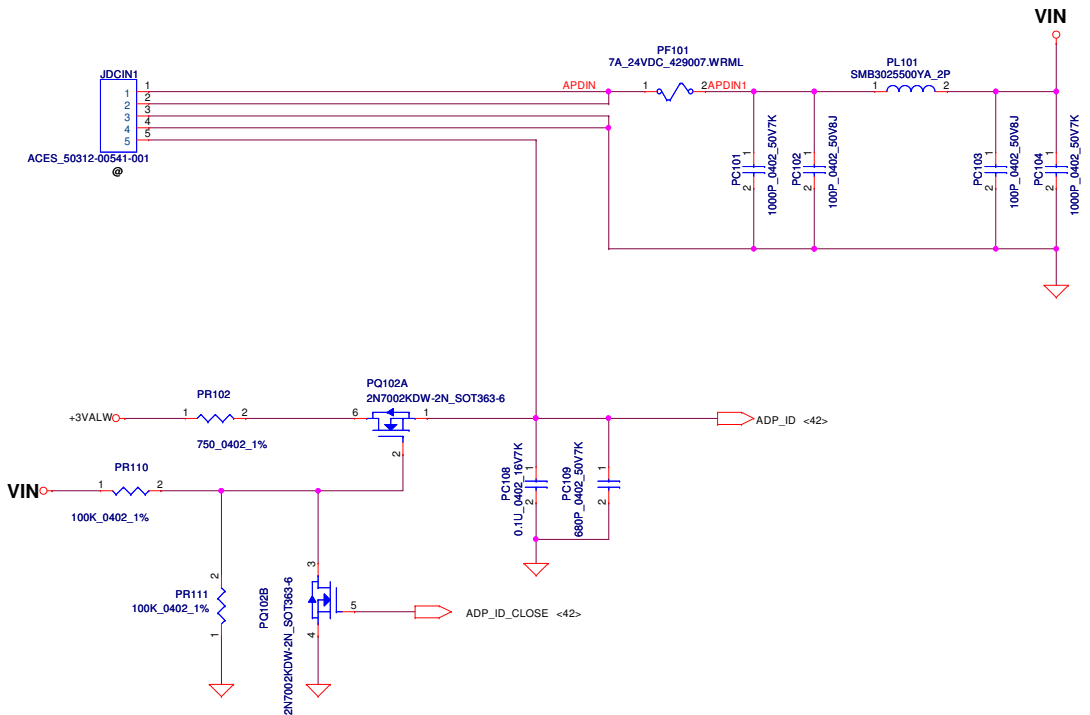


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Date: Wednesday, February 27, 2013				Sheet	45 of 60
Document Number				Rev	1.0
LA-9631P					

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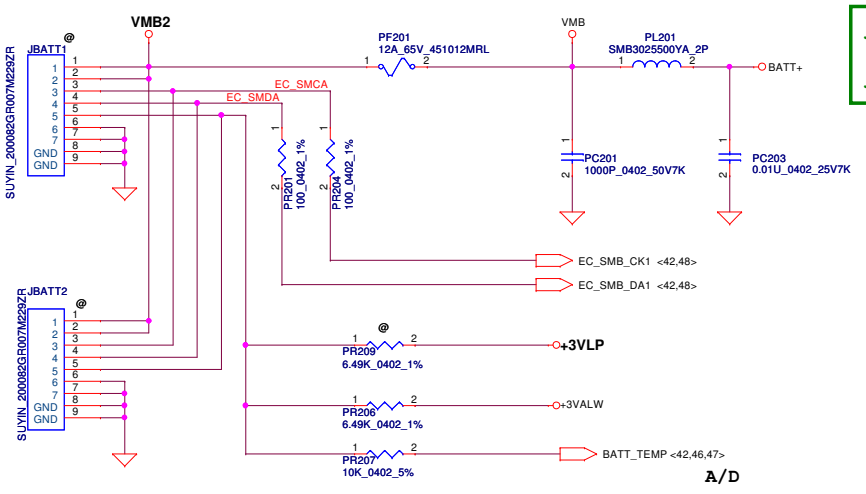


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Compal Electronics, Inc. PWR DCIN / RTC Battery	
Document Number	Rev
Gx00	1.0
Date: Wednesday, February 27, 2013	Sheet 46 of 60

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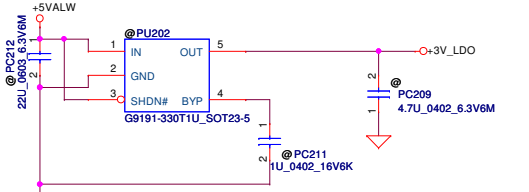
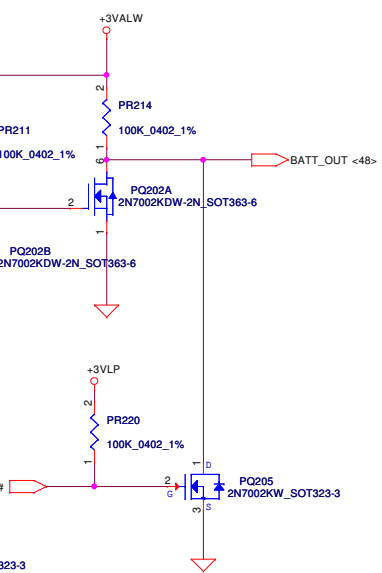
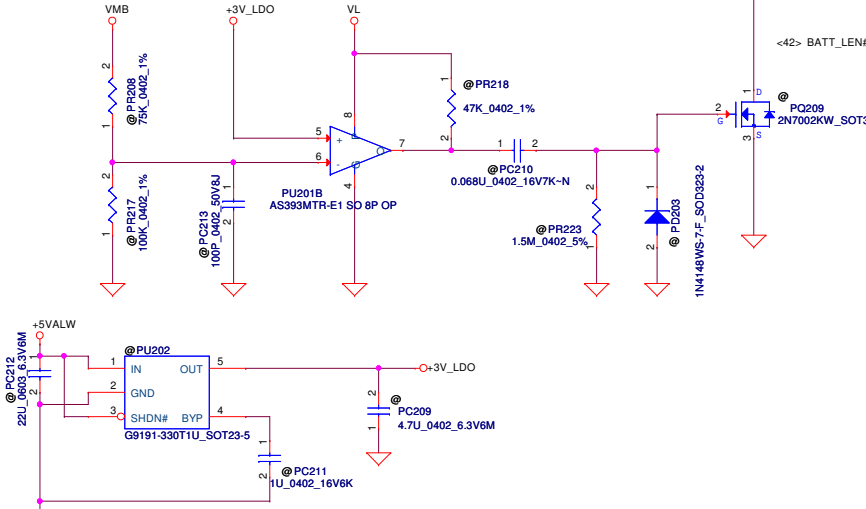
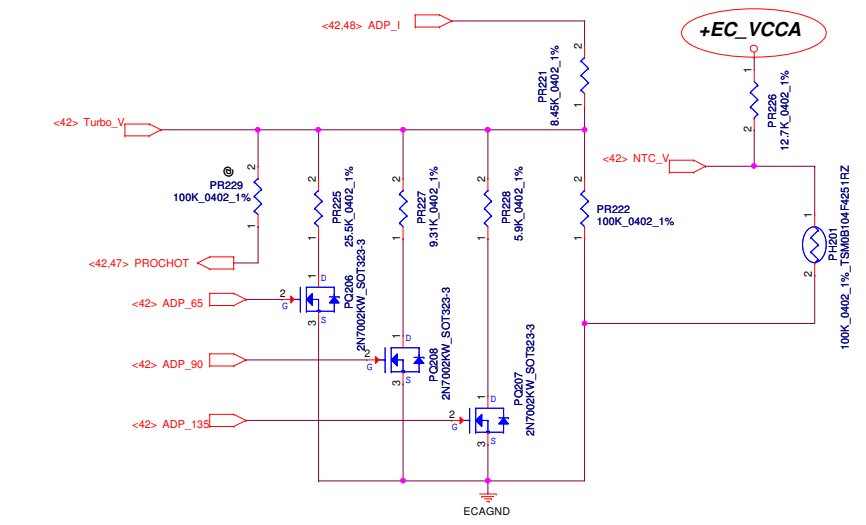
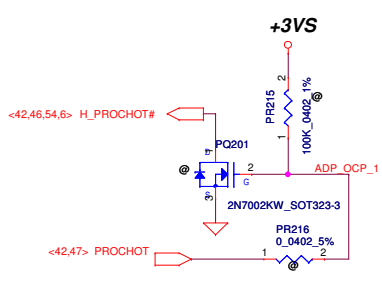
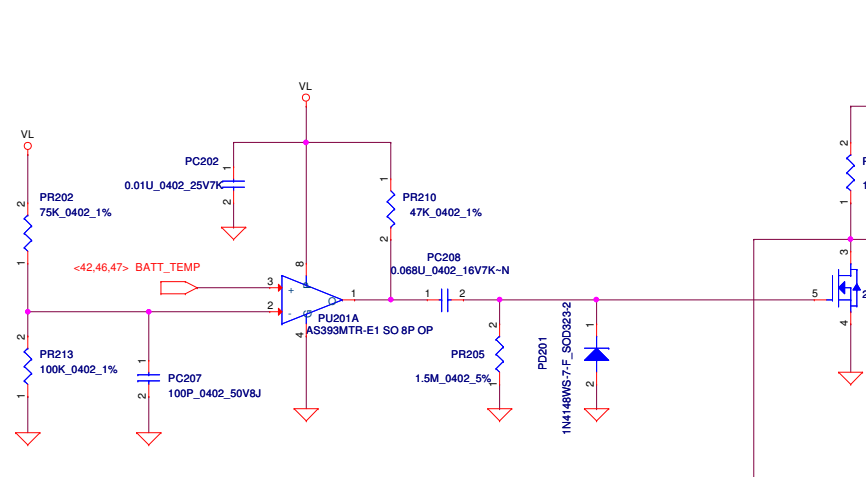


JBATT1 ---> 15"
JBATT2 ---> 14"

PH201 under CPU bottom side :
CPU thermal protection at 93 +/-3 degree C
Recovery at 56 +/-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA) : 1.65K 70W active 65W recovery

20120314
Change to +EC_VCCA from +3VLP

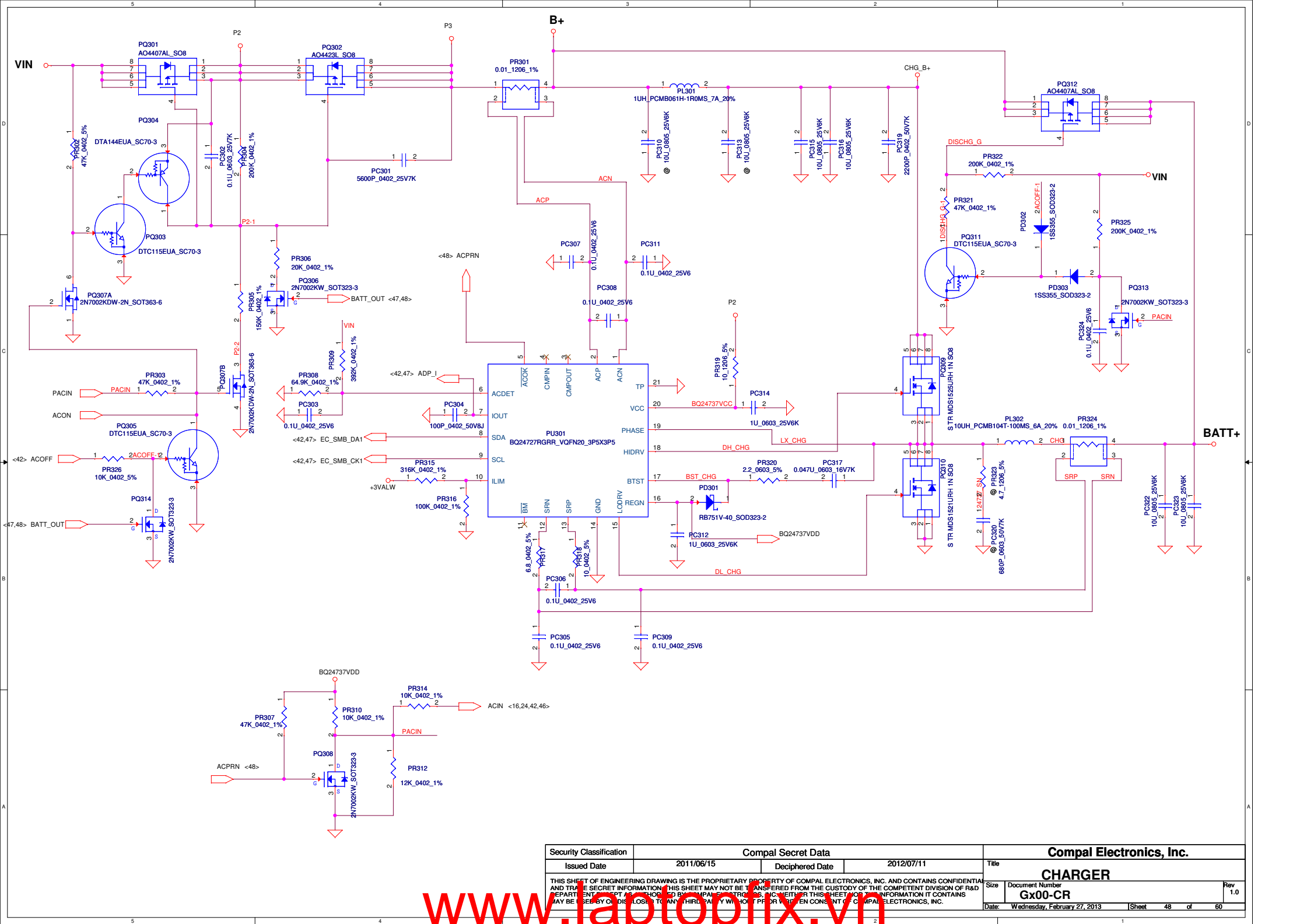


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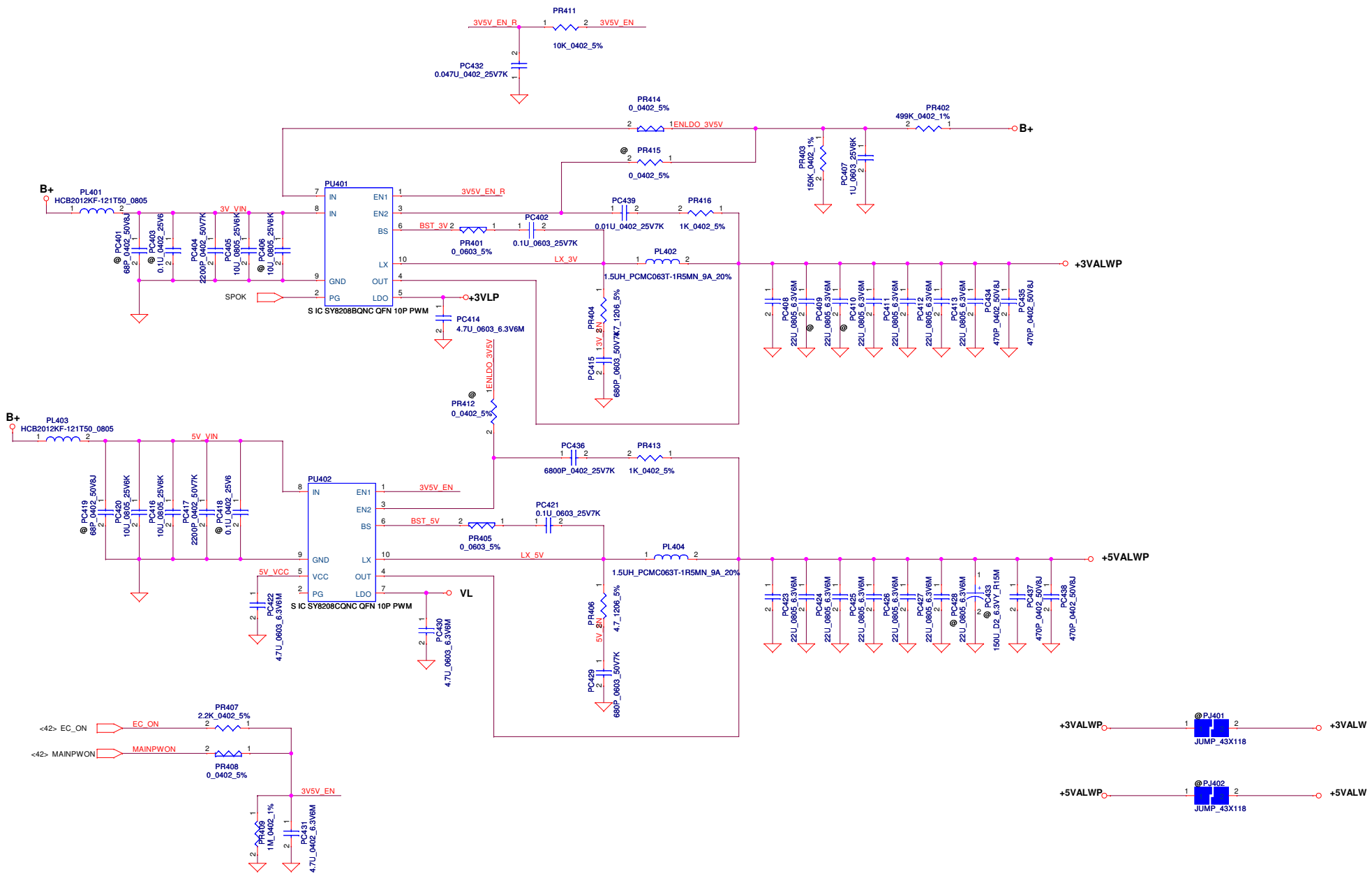
Compal Electronics, Inc.	
PWR-BATTERY CONN/OTP	
Document Number	Gx00-CR
Date	Wednesday, March 08, 2013

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Sheet 47 of 60



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					Gx00-CR	1.0
				Date:	Wednesday, February 27, 2013	Sheet 48 of 60

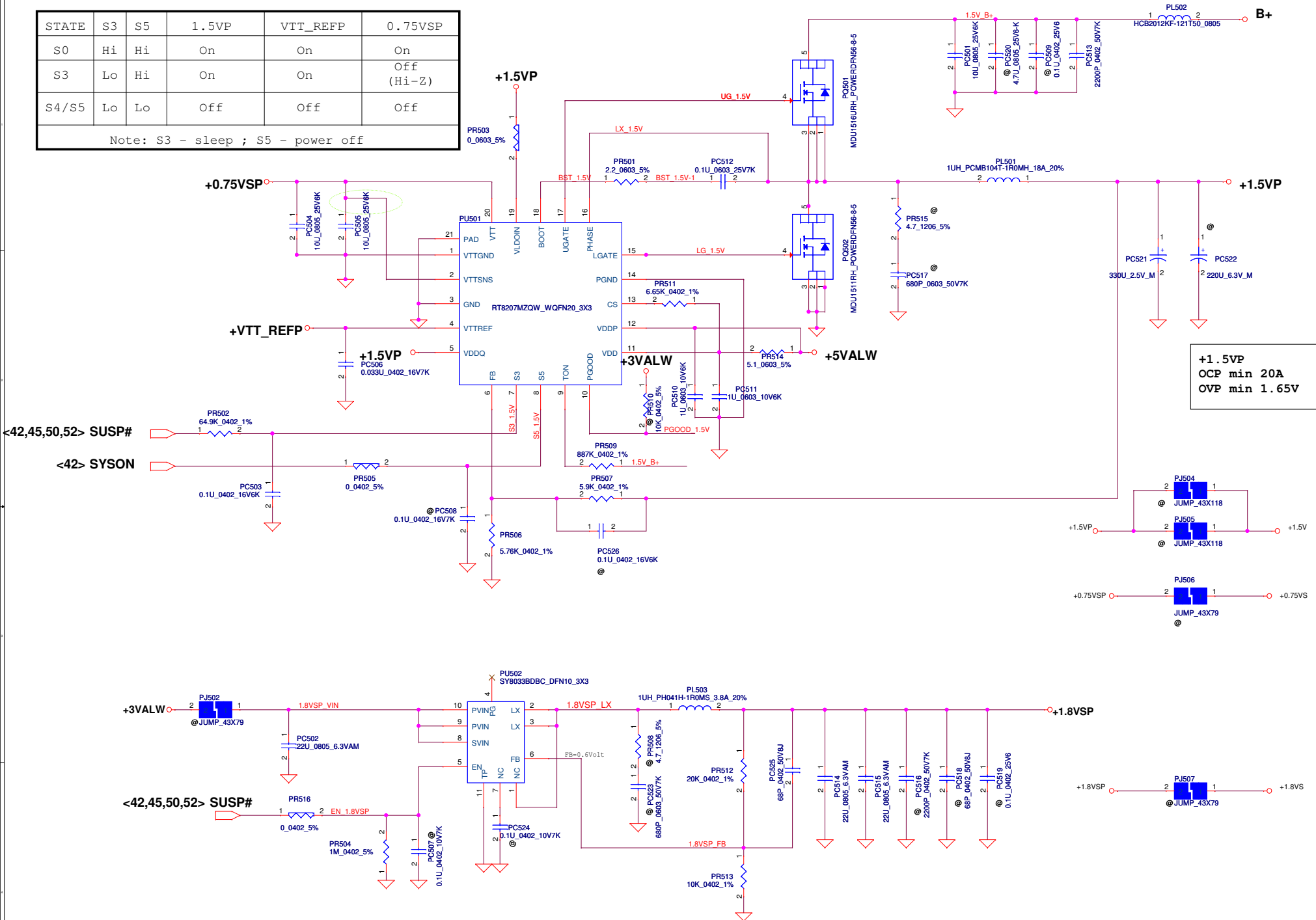


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				Gx00-CR	1.0
				Date: Wednesday, February 27, 2013	Sheet 49 of 60

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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



+1.5VP
 OCP min 20A
 OVP min 1.65V

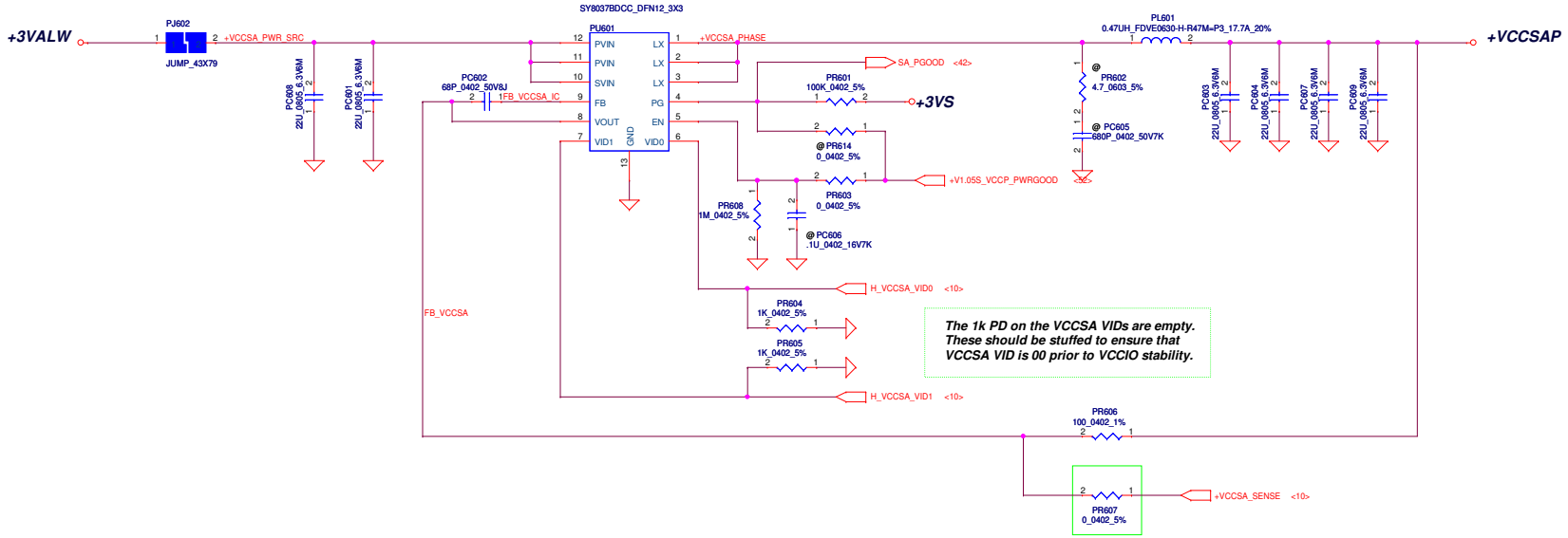
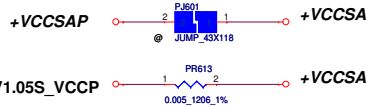
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		2012/07/11

Compal Electronics, Inc.	
+1.5VP/+1.8VSP	
Size	Document Number
Custom	Gx00-CR
Date:	Wednesday, February 27, 2013
Sheet	50 of 60

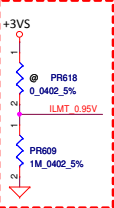
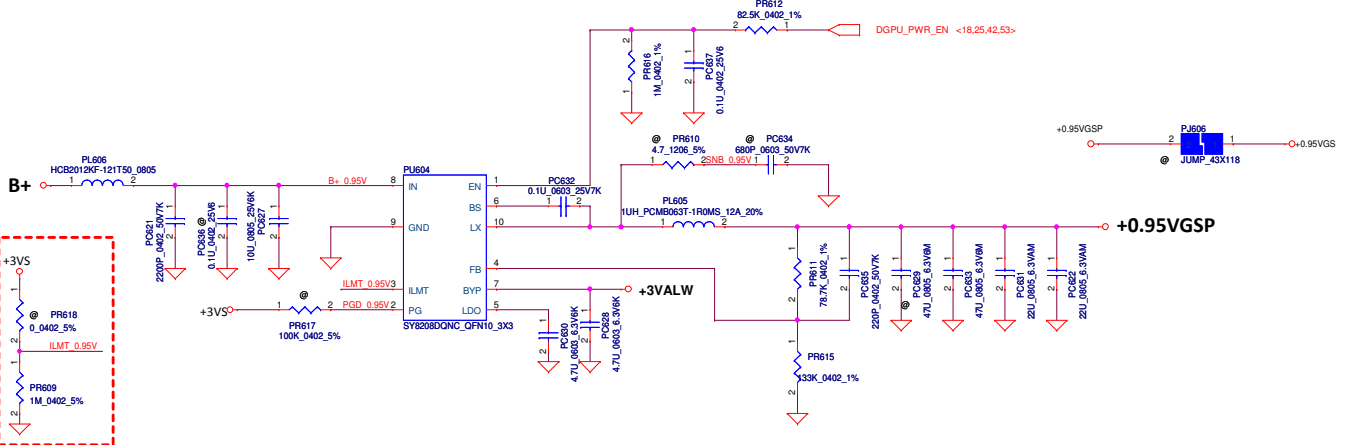
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

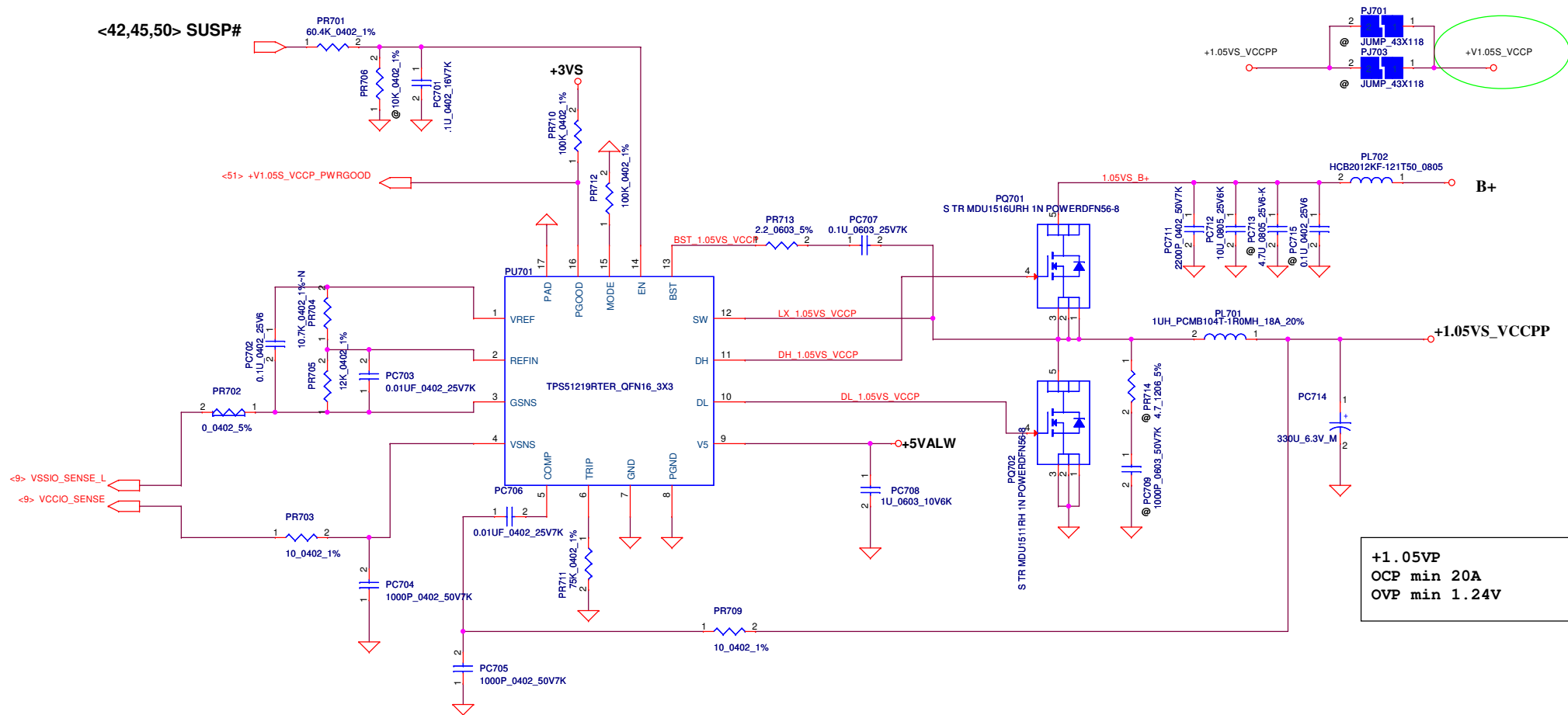
output voltage adjustable network



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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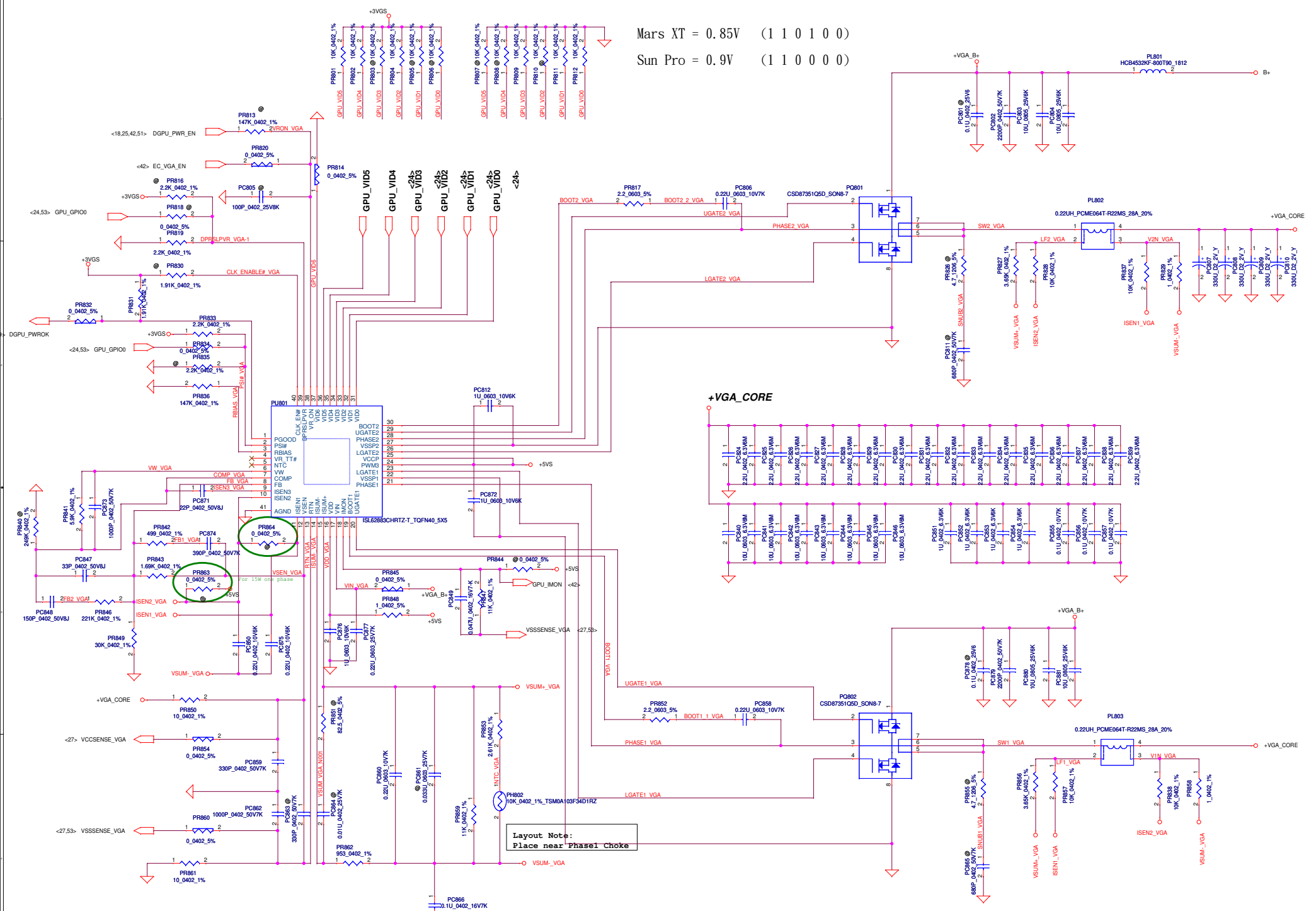


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				Custom	1.0
				Date:	Wednesday, February 27, 2013
				Sheet	52 of 60

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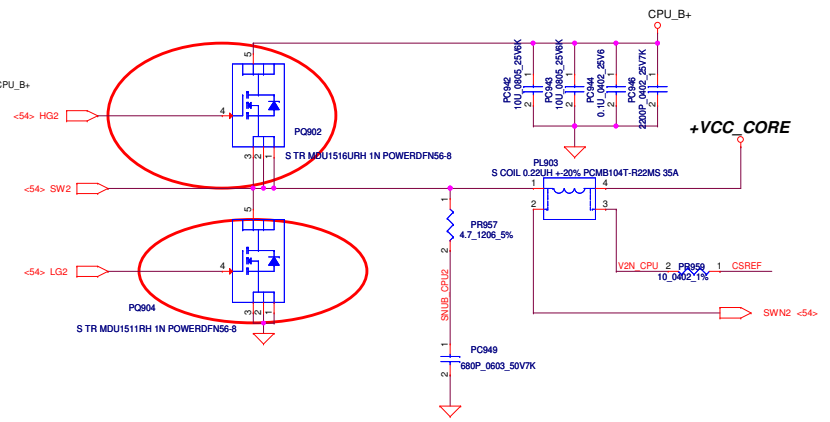
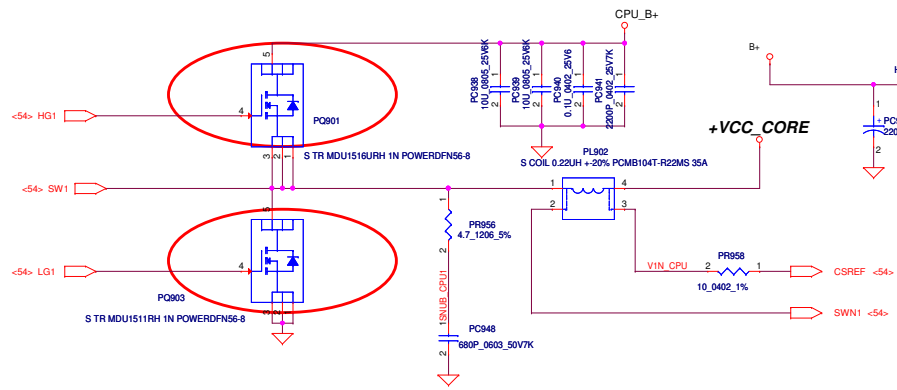
Mars XT = 0.85V (1 1 0 1 0 0)

Sun Pro = 0.9V (1 1 0 0 0 0)



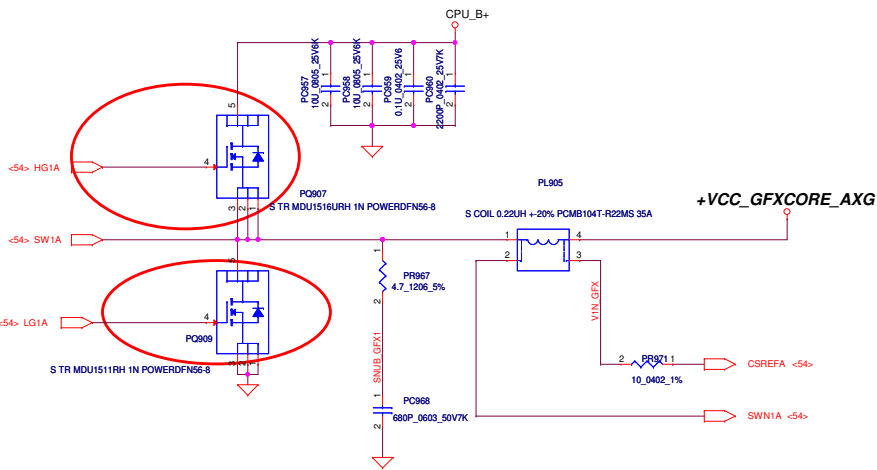
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Size	Document Number	Gx00-CR		Rev	1.0
Date	Wednesday, February 27, 2013			Sheet	53 of 60

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QC 45W CPU
 VID1=0.9V
 IccMax=94A
 Icc_Dyn=66A
 Icc_TDC=52A
 R_LL=1.9m ohm
 OCP-110A

DC 35W CPU
 VID1=1.05V
 IccMax=53A
 Icc_Dyn=43A
 Icc_TDC=36A
 R_LL=1.9m ohm
 OCP-65A

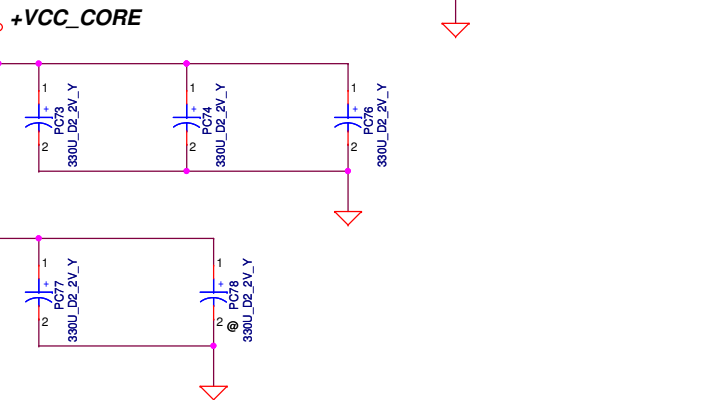
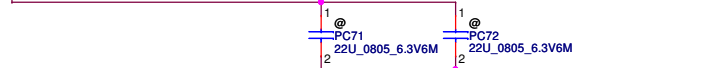
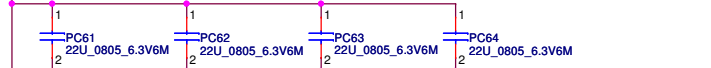
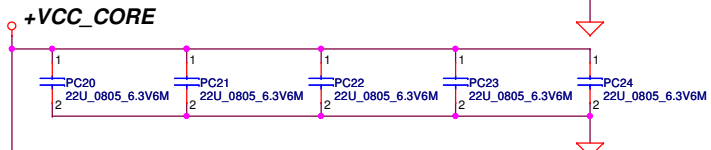
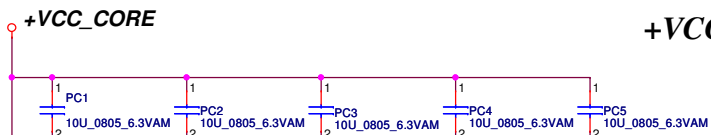


QC 45W GT2
 VID1=1.23V
 IccMax=46A
 Icc_Dyn=37A
 Icc_TDC=38A
 R_LL=3.9m ohm
 OCP-55A

DC 35W GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm
 OCP-40A

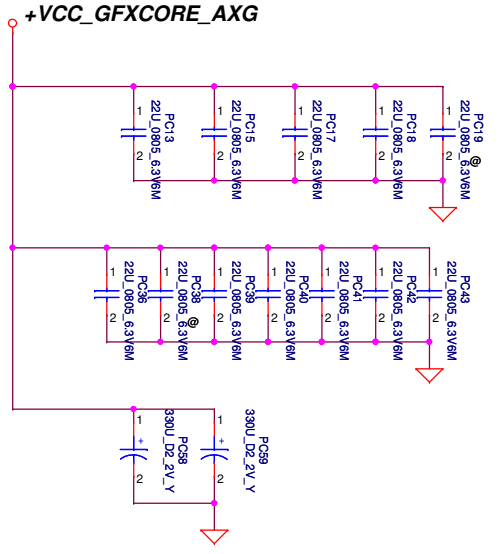
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PWR-CPU CORE	
Document Number	Gx00-CR
Rev	1.0
Date	Wednesday, February 27, 2013
Sheet	55 of 60



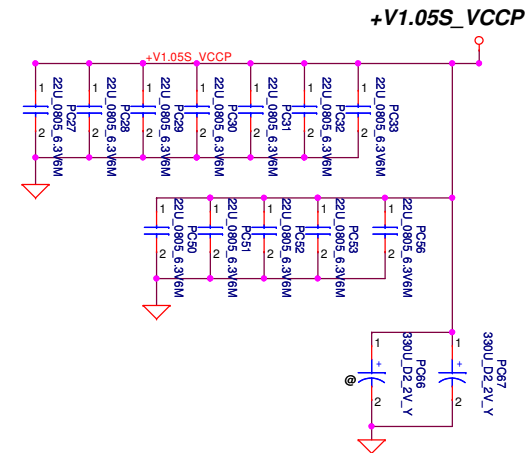
+VCC_CORE

+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



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Size	Document Number	Date		Sheet	Rev
	LA-963IP	Wednesday, February 27, 2013		56 of 60	1.0

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VIWGP/R PWR PIR List

Item	Page	MODIFICATION LIST	PURPOSE	
1	P. 46	Add PR102, PC108, PC109	For ADP_ID pin detect	EVT TO DVT
2	P. 47	Add PR225, PR227, PR228, PQ206, PQ207, PQ208	For protect adapter function	
3	P. 49	Add PR410, PC433	For 3VALWP/5VALWP sequence	
4	P. 49	Add PC434, PC435, PC436, PC437	For EMI solution	
5	P. 49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple	
6	P. 50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence	
7	P. 51	Add PC637	For +0.95VGSP sequence	
8	P. 54	Change PC907, PR912, PR927, PC928	For CPU Transient Compensation	

9	P. 48	Add PR326 and PQ314	For battery health function	PVT TO PVT2
10	P. 49	Add PR411, PC432	To delay +3VALW enable. PR411 change to 10K and PC432 change to 0.047uF	
11	P. 49	Change PC439 from 4700P to 10nF , PC436 from 47nF to 6.8nF	Adjust +3VALW and +5VALW rising time.	
12	P. 51	Add PR614	For Celeron CPU SA_PGOOD	
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				

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				Date:	Wednesday, February 27, 2013
				Sheet	57 of 60

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VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 46	Change C726, C727 to 2.2nF	For Sequence
2	P. 36	Add R405	For Intel Combo Card
3	P. 35	Delete RP19. Add RP26, RP27	Because ME modify MIC location
4	P. 14	Add R406, R407, R408, R409	Reserve for improvement factory processes
5	P. 42	Add EC_SPI_S0, EC_SPI_S1, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
6	P. 42	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
7	P. 42	Reserve R410	Reserve Pull-high for GPIO
8	P. 5-32	Change footprint of JCPU1, U4, UV1, UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	For Lenovo rule
9	P. 25	Change RV41 to 240K. Change CV53 to 0.1uF	For VGA sequence
10	P. 21	Add Q21, R40, C237, R225, C243	Reserve for power consumption
11	P. 34	Add R411, R412, C411, C412	Reserve for EMI
12	P. 25	Change CV36, CV37 to 8.2pF	For Crystal fine-tune
13	P. 42	Add ADP_65 to EC Pin.21	For adapter protection
14	P. 42	Add ADP_90 to EC Pin.68	For adapter protection
15	P. 42	Add ADP_135 to EC Pin.85	For adapter protection
16	P. 42	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
17	P. 42	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
18	P. 42	Add ADP_ID to EC Pin.66	For adapter
19	P. 42	Change PCH_ENBKL from EC Pin.73 to EC Pin.76	For common design
20	P. 42	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
21	P. 42	Add VGATE to EC Pin.74	Reserve for sequence
22	P. 42	Add SYS_PWROK to EC Pin.86	Reserve for sequence
23	P. 42	Change EC_TS_ON# from EC Pin.85 to EC Pin.97	For common design
24	P. 42	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
25	P. 42	Change SUSCLK from EC Pin.123 to EC Pin.122	For common design

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				LA-9631P	1.0
				Date:	Wednesday, February 27, 2013
				Sheet	59 of 60

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VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 40	Delete R416, Add J9	No need Zero ODD Function
2	P. 36	Reserve R508	For leakage current issue of Atheros WLAN
3	P. 33	Add R509	protect BKOFF# damage
4	P. 42	Reserve R416	Reserve +3VLP power rail to EC
5	P. 42	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.
6	P. 42	Change EC_SMB_CK1 & EC_SMB_DAI power rail to +3V_EC	Using power rail which the same with EC.
7	P. 14	Change U5 from 4MB to 8MB ROM	Follow common design
8	P. 14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it
1	P. 41	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5
2	P. 42	Reserve resistance in EC for share ROM.	Follow common design
3	P. 51	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU

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				LA-9631P	1.0
				Date:	Wednesday, February 27, 2013
				Sheet	60 of 60

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