

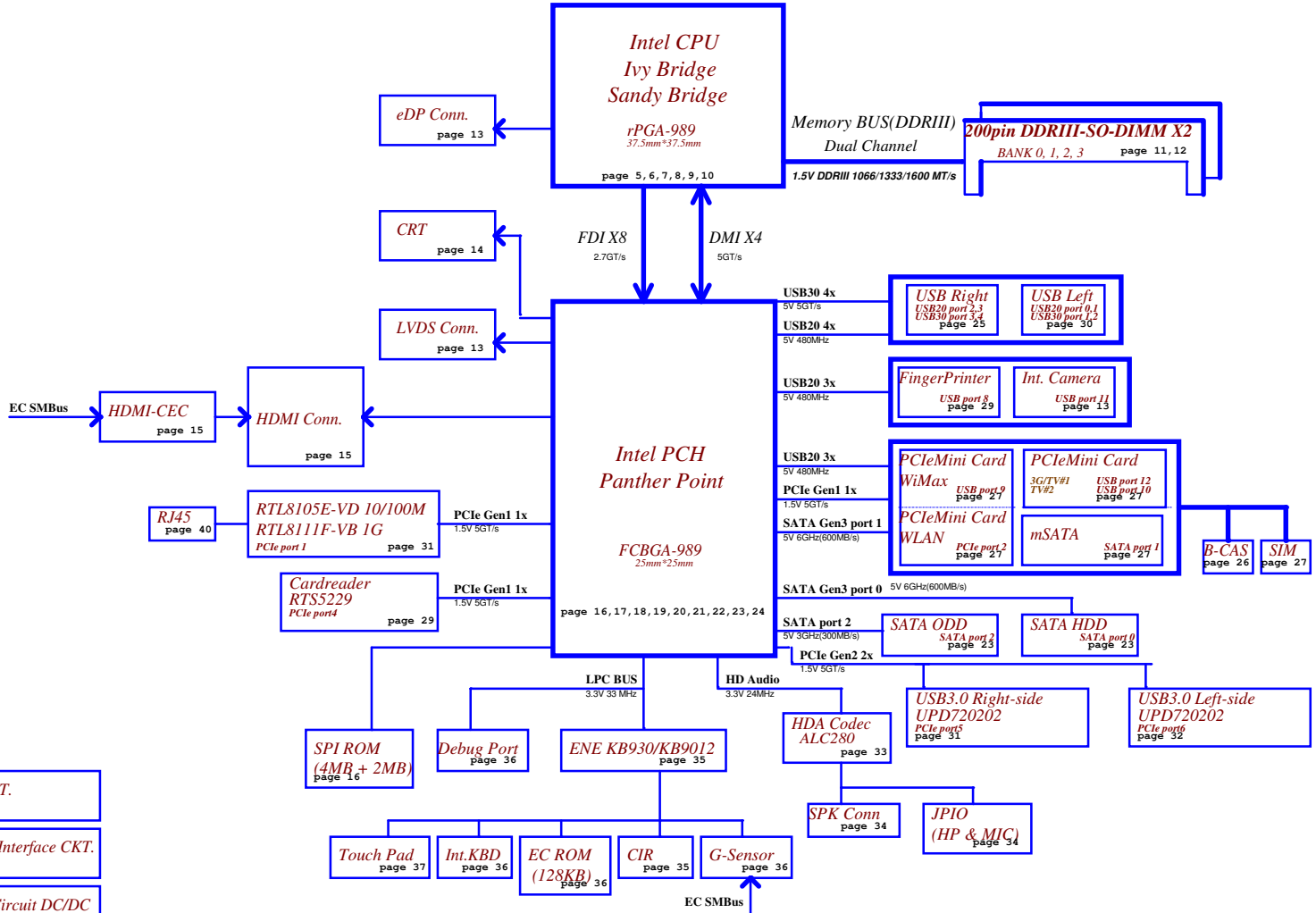
# QCLA4,5

*Eureka 14" & 15"*

## LA-8862P REV 0.2 Schematic

Intel Processor (Ivy Bridge / Sandy Bridge) PCH (Panther Point) 2011-11-24 Rev 0.2
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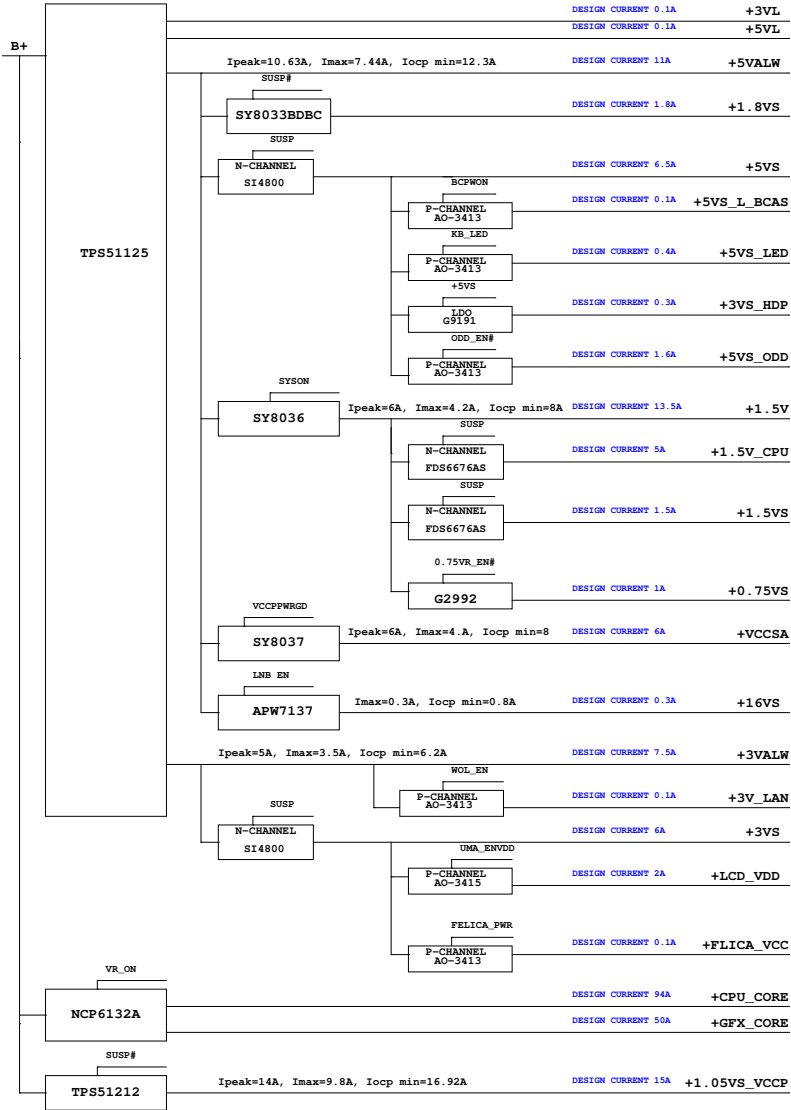
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				QCLA4,5	0.2
Date: Thursday, February 16, 2012				Sheet 1 of 48	



- RTC CKT. page 16
- DC/DC Interface CKT. page 38
- Power Circuit DC/DC page 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49
- Power On/Off CKT. page 37

- Finger Printer/B page 26
- Power/B page 37

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				Document Number
				Block Diagram
				QCLA4,5
				Rev 0.2
				Date: Thursday, February 16, 2012
				Sheet 2 of 48



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				Document Number
				Rev
				0.2
				Date
				Thursday, February 16, 2012
				Sheet
				3 of 48

**Voltage Rails**

( O MEANS ON X MEANS OFF )

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTF +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

**BTO Option Table**

Function	HDMI	Camera & Mic	TPM	MINI PCI-E SLOT
description	HDMI	Camera & Mic	TPM	Half Card
explain	HDMI	Digital MIC	Analog MIC	SLB 9635 SLB 9655
BTO	HDMI@	CAM@	AMIC@	TPM9635@ TPM9655@ WIMAX@

Function	SPI ROM	Green CLK	USB 3.0	Sleep & Charge	LAN
description	SPI ROM <td>Green CLK</td> <td>USB 3.0</td> <td>Sleep &amp; Charge</td> <td>LAN</td>	Green CLK	USB 3.0	Sleep & Charge	LAN
explain	WIN8	Green CLK	NOGCLK	Internal	10/100M Giga
BTO	WIN8@	GCLK@	NOGCLK@	IUSB30@	8105ELDO@ 8111FVB@

**PCH SM Bus Address**

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

**EC SM Bus1 Address**

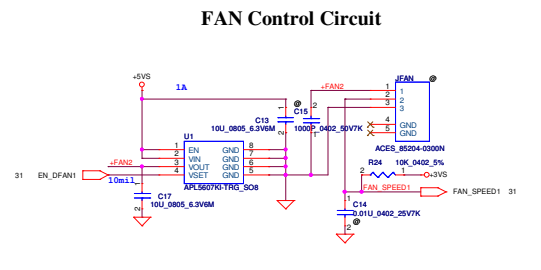
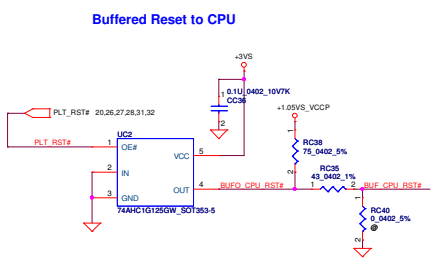
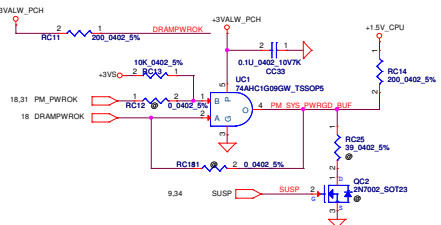
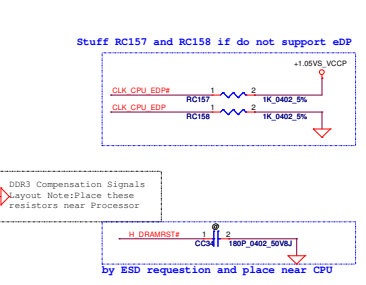
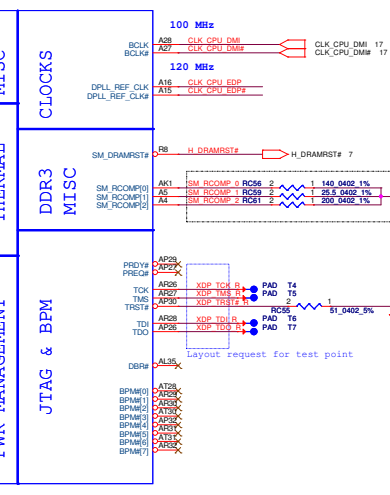
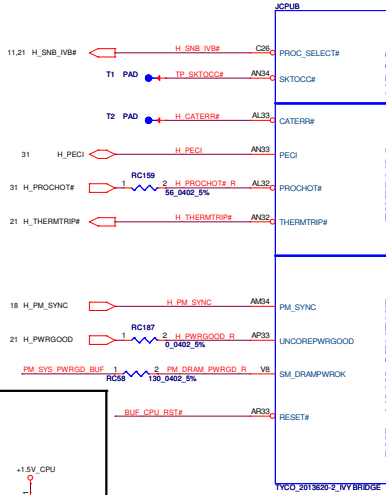
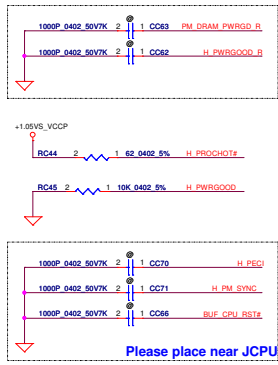
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
+3VL	Cap. Sensor		Virtual I2C

**EC SM Bus2 Address**

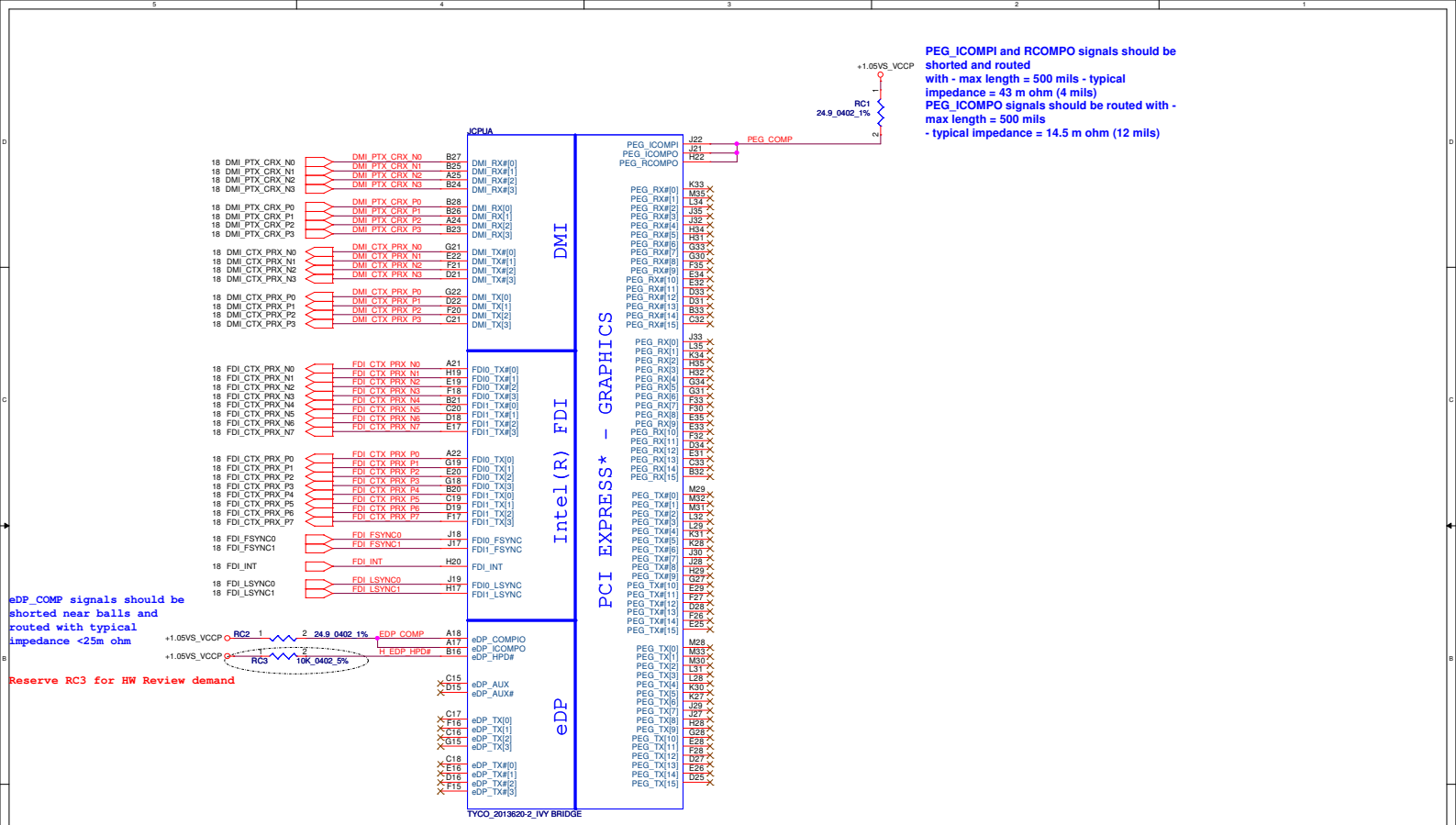
Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

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Date	Thursday, February 15, 2012	Sheet	5	of	48



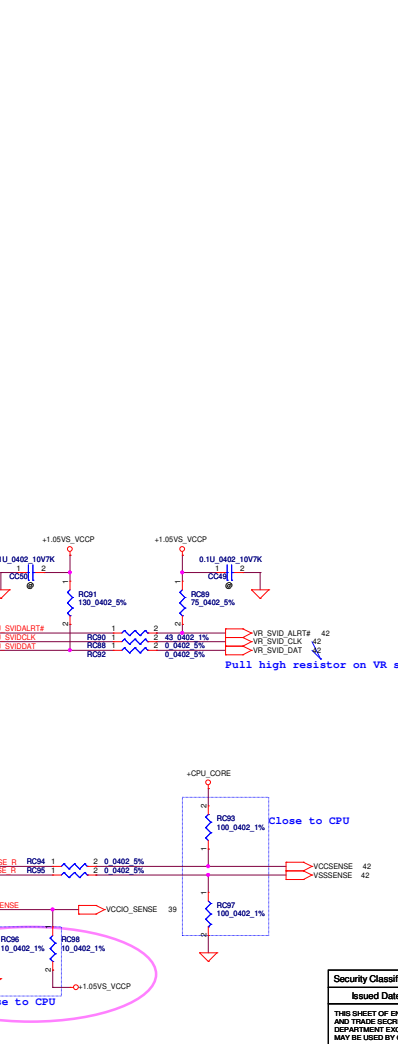
eDP\_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

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				QFKAA	0.2
Date: Thursday, February 16, 2012				Sheet	6 of 48

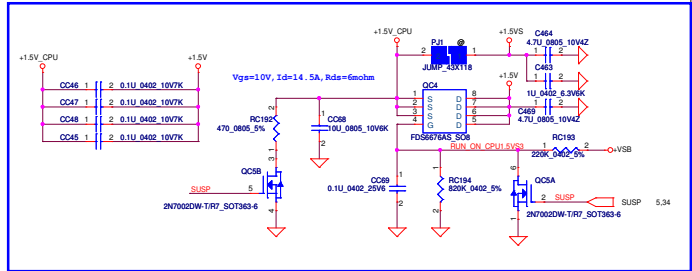
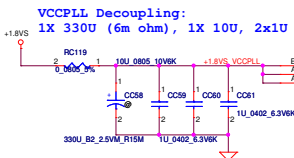
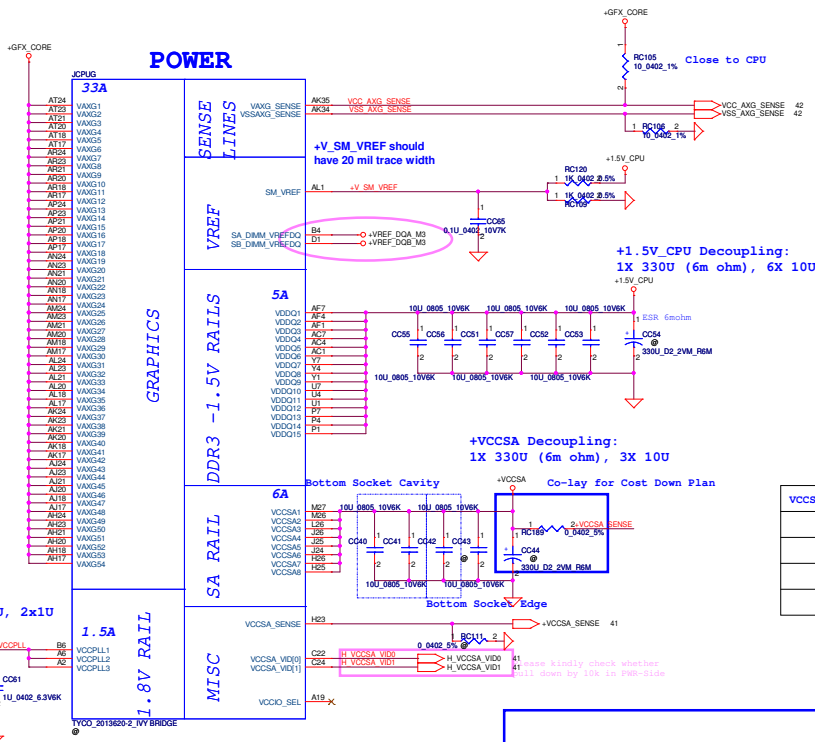


Pin	Signal	Power	Current
AG35	VCC1	POWER	8.5A
AG34	VCC2	POWER	
AG33	VCC3	POWER	
AG32	VCC4	POWER	
AG31	VCC5	POWER	
AG30	VCC6	POWER	
AG29	VCC7	POWER	
AG28	VCC8	POWER	
AG27	VCC9	POWER	
AG26	VCC10	POWER	
AG25	VCC11	POWER	
AG24	VCC12	POWER	
AG23	VCC13	POWER	
AG22	VCC14	POWER	
AG21	VCC15	POWER	
AG20	VCC16	POWER	
AG19	VCC17	POWER	
AG18	VCC18	POWER	
AG17	VCC19	POWER	
AG16	VCC20	POWER	
AG15	VCC21	POWER	
AG14	VCC22	POWER	
AG13	VCC23	POWER	
AG12	VCC24	POWER	
AG11	VCC25	POWER	
AG10	VCC26	POWER	
AG9	VCC27	POWER	
AG8	VCC28	POWER	
AG7	VCC29	POWER	
AG6	VCC30	POWER	
AG5	VCC31	POWER	
AG4	VCC32	POWER	
AG3	VCC33	POWER	
AG2	VCC34	POWER	
AG1	VCC35	POWER	
AG0	VCC36	POWER	
AG35	VCC37	POWER	
AG34	VCC38	POWER	
AG33	VCC39	POWER	
AG32	VCC40	POWER	
AG31	VCC41	POWER	
AG30	VCC42	POWER	
AG29	VCC43	POWER	
AG28	VCC44	POWER	
AG27	VCC45	POWER	
AG26	VCC46	POWER	
AG25	VCC47	POWER	
AG24	VCC48	POWER	
AG23	VCC49	POWER	
AG22	VCC50	POWER	
AG21	VCC51	POWER	
AG20	VCC52	POWER	
AG19	VCC53	POWER	
AG18	VCC54	POWER	
AG17	VCC55	POWER	
AG16	VCC56	POWER	
AG15	VCC57	POWER	
AG14	VCC58	POWER	
AG13	VCC59	POWER	
AG12	VCC60	POWER	
AG11	VCC61	POWER	
AG10	VCC62	POWER	
AG9	VCC63	POWER	
AG8	VCC64	POWER	
AG7	VCC65	POWER	
AG6	VCC66	POWER	
AG5	VCC67	POWER	
AG4	VCC68	POWER	
AG3	VCC69	POWER	
AG2	VCC70	POWER	
AG1	VCC71	POWER	
AG0	VCC72	POWER	
AG35	VCC73	POWER	
AG34	VCC74	POWER	
AG33	VCC75	POWER	
AG32	VCC76	POWER	
AG31	VCC77	POWER	
AG30	VCC78	POWER	
AG29	VCC79	POWER	
AG28	VCC80	POWER	
AG27	VCC81	POWER	
AG26	VCC82	POWER	
AG25	VCC83	POWER	
AG24	VCC84	POWER	
AG23	VCC85	POWER	
AG22	VCC86	POWER	
AG21	VCC87	POWER	
AG20	VCC88	POWER	
AG19	VCC89	POWER	
AG18	VCC90	POWER	
AG17	VCC91	POWER	
AG16	VCC92	POWER	
AG15	VCC93	POWER	
AG14	VCC94	POWER	
AG13	VCC95	POWER	
AG12	VCC96	POWER	
AG11	VCC97	POWER	
AG10	VCC98	POWER	
AG9	VCC99	POWER	
AG8	VCC100	POWER	



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Date:	Thursday, February 16, 2012	Sheet	8	of 48



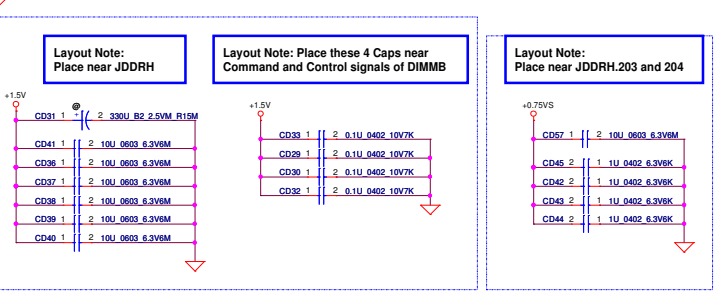
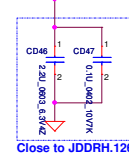
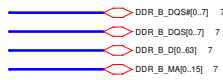
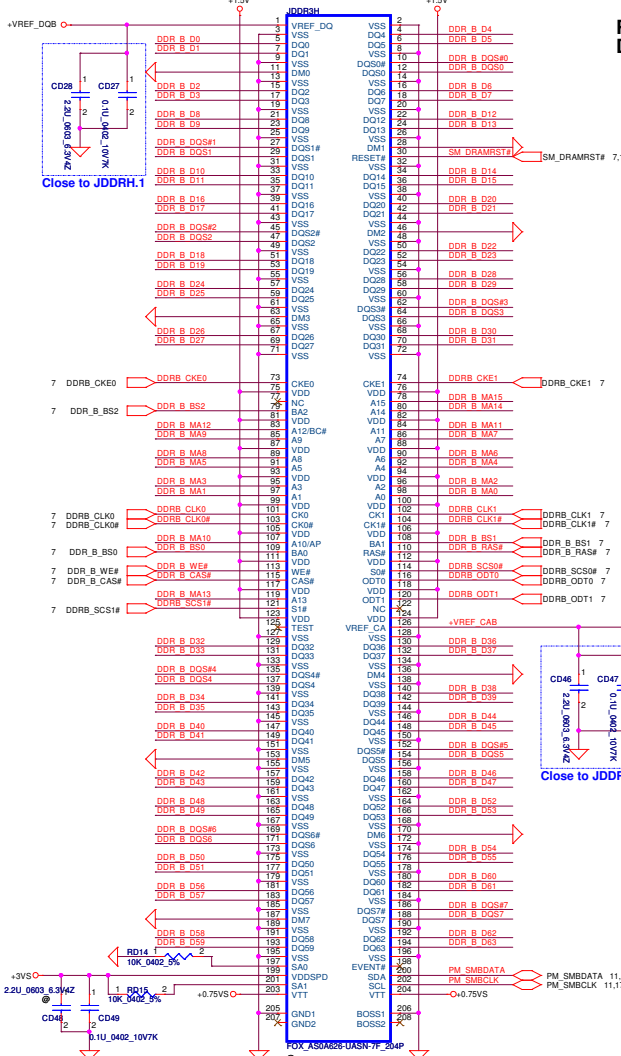


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			Sheet	9 of 48



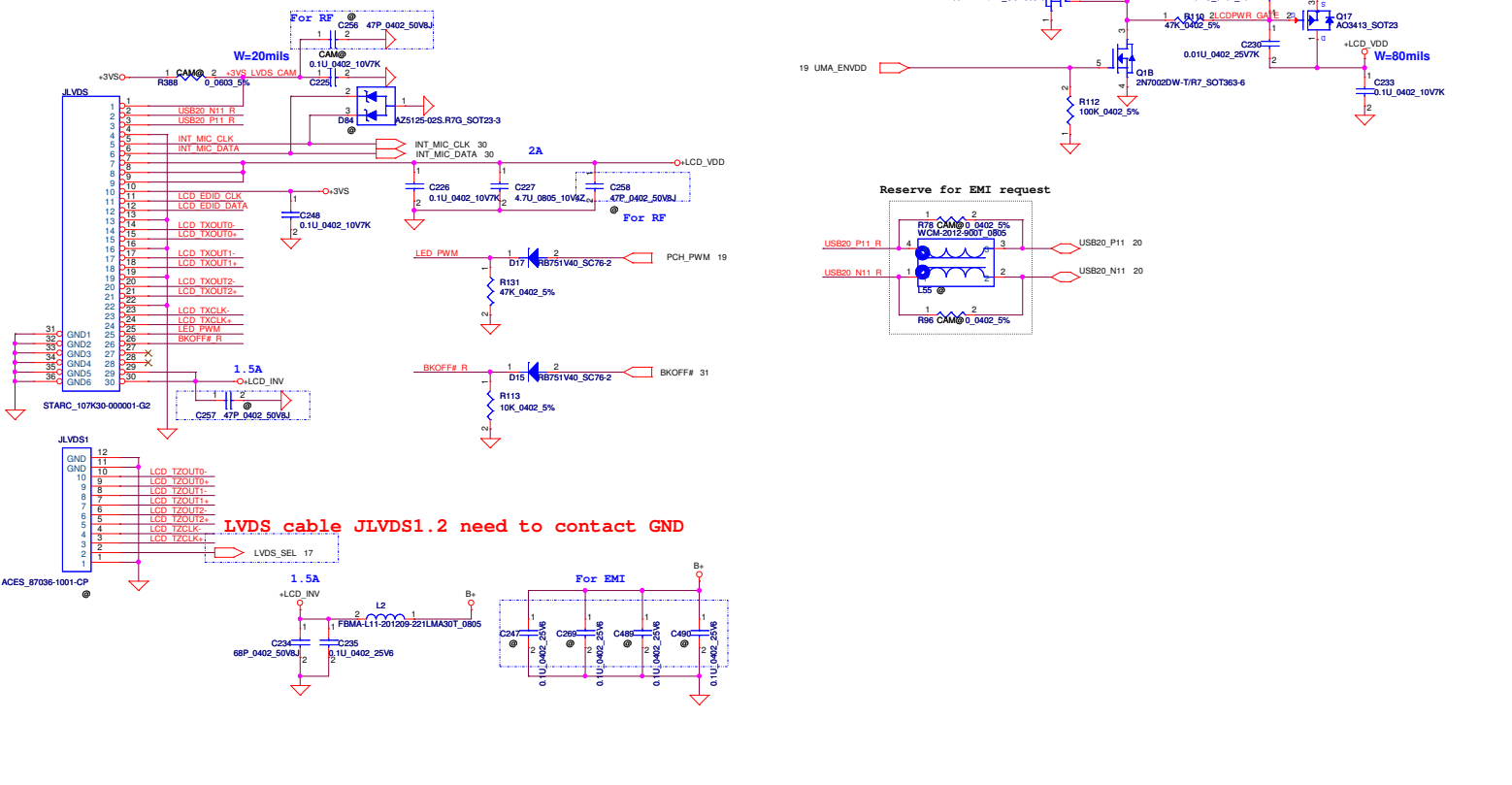


# Reverse Type DDR3 SO-DIMM B



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				Custom	QFKAA
				Date:	Thursday, February 16, 2012
				Sheet	12 of 48

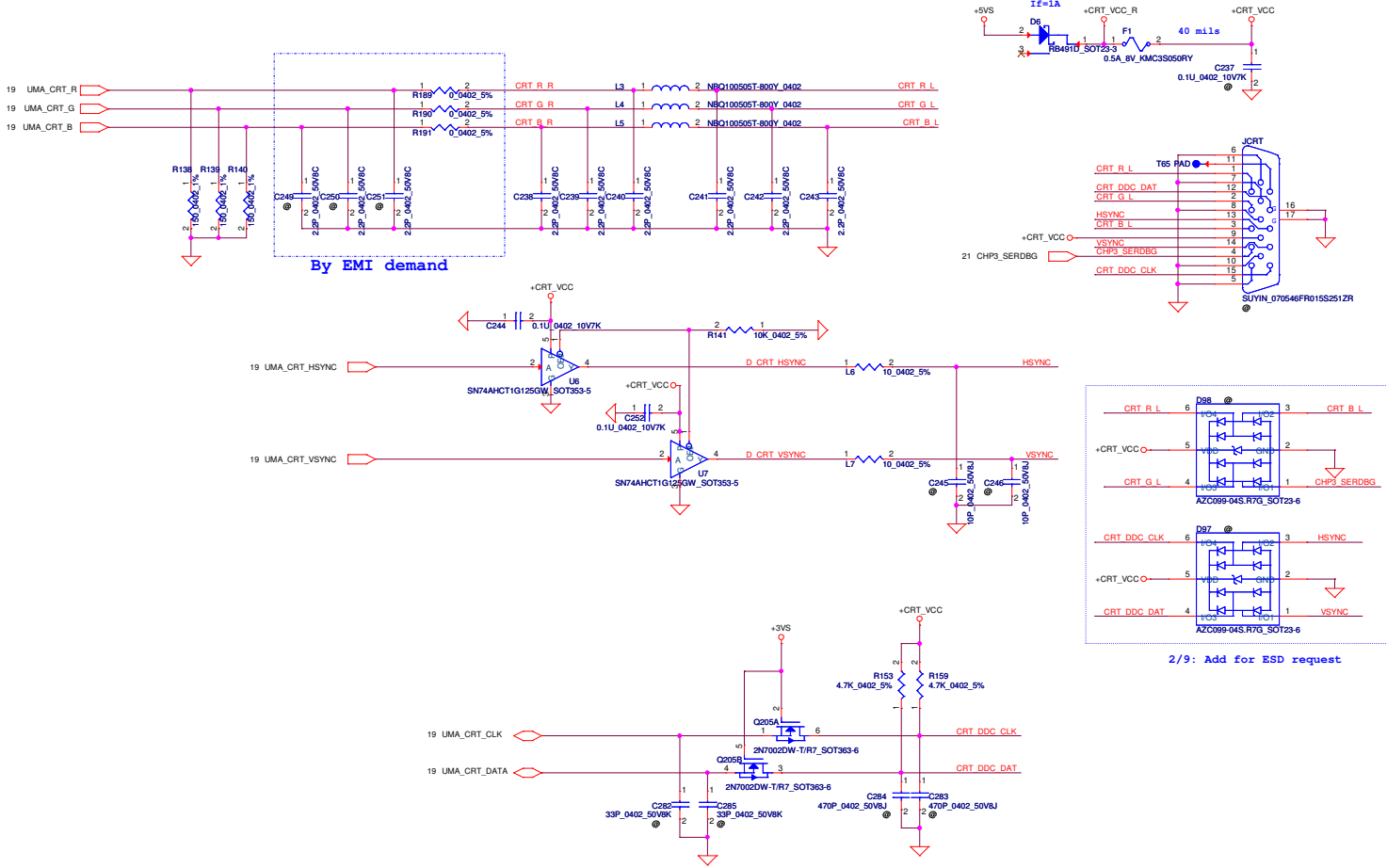
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- 19 LCD\_TXOUT2+ LCD\_TXOUT2+
- 19 LCD\_TXOUT2- LCD\_TXOUT2-
- 19 LCD\_TXCLK+ LCD\_TXCLK+
- 19 LCD\_TXCLK- LCD\_TXCLK-
- 19 LCD\_EDID\_CLK LCD\_EDID\_CLK
- 19 LCD\_EDID\_DATA LCD\_EDID\_DATA
- 19 LCD\_TZOUT0+ LCD\_TZOUT0+
- 19 LCD\_TZOUT0- LCD\_TZOUT0-
- 19 LCD\_TZOUT1+ LCD\_TZOUT1+
- 19 LCD\_TZOUT1- LCD\_TZOUT1-
- 19 LCD\_TZOUT2+ LCD\_TZOUT2+
- 19 LCD\_TZOUT2- LCD\_TZOUT2-
- 19 LCD\_TZCLK+ LCD\_TZCLK+
- 19 LCD\_TZCLK- LCD\_TZCLK-



LVDS cable JLVDS1.2 need to contact GND

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				Date	Thursday, February 16, 2012	Sheet 19 of 48

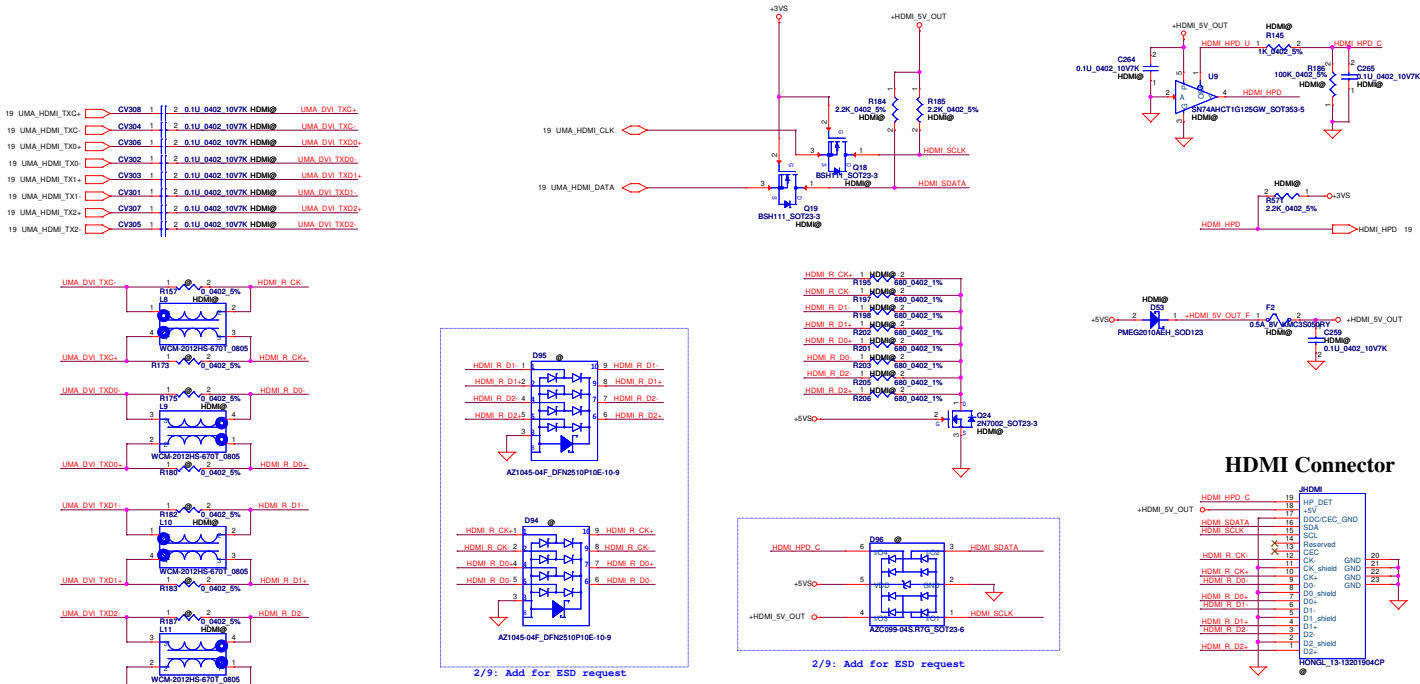
# CRT CONNECTOR



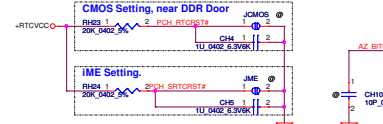
By EMI demand

2/9: Add for ESD request

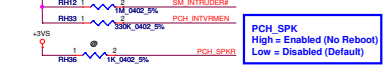
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Date: Thursday, February 16, 2012				Sheet 14 of 48 Rev 0.2



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				<b>QFKAA</b>
				Date: Thursday, February 15, 2012 Sheet 18 of 48

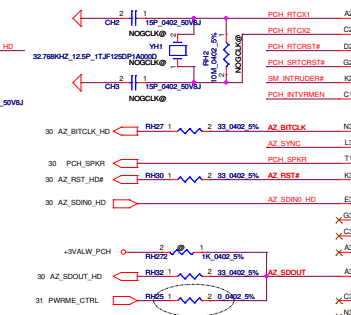
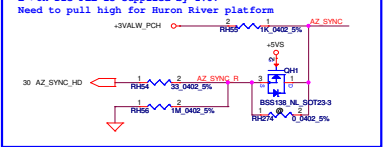


**Integrated SUS 1.05V VRM Enable**  
 High = Enable Internal VRs (must be always pulled high)  
 PCH\_INTRVME#

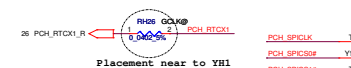


**HDA\_SDO**  
 MB debug mode, this signal has a weak internal pull down  
 \*Low = Disable (default)  
 High = Enable (flash descriptor security override)

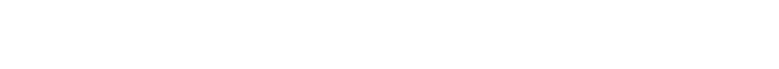
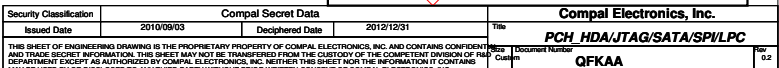
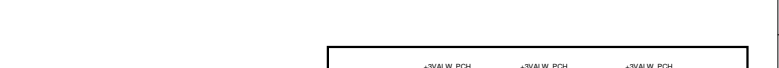
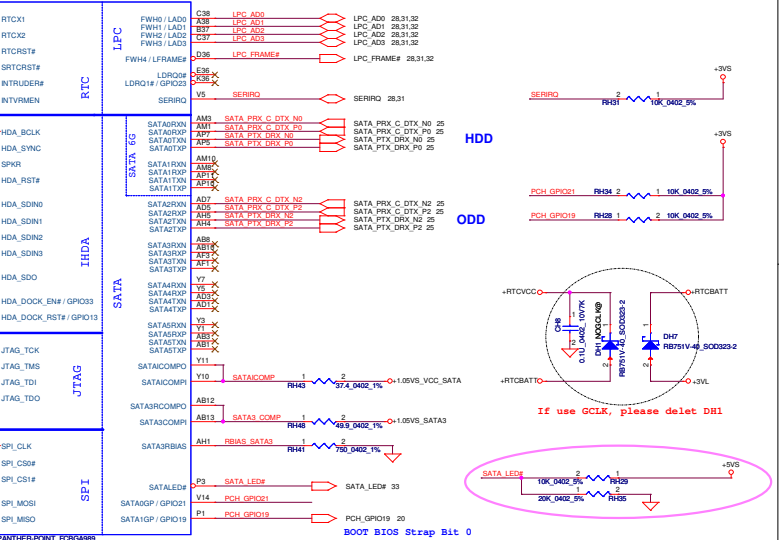
**HDA\_SYNC**  
 \*This signal has a weak internal pull down  
 H=On Die PLL is supplied by 1.5V  
 L=On Die PLL is supplied by 1.5V  
 Need to pull high for Huron River platform



8/30 Change PWRME\_CTRL# to HDA\_SDO by PCH EDS

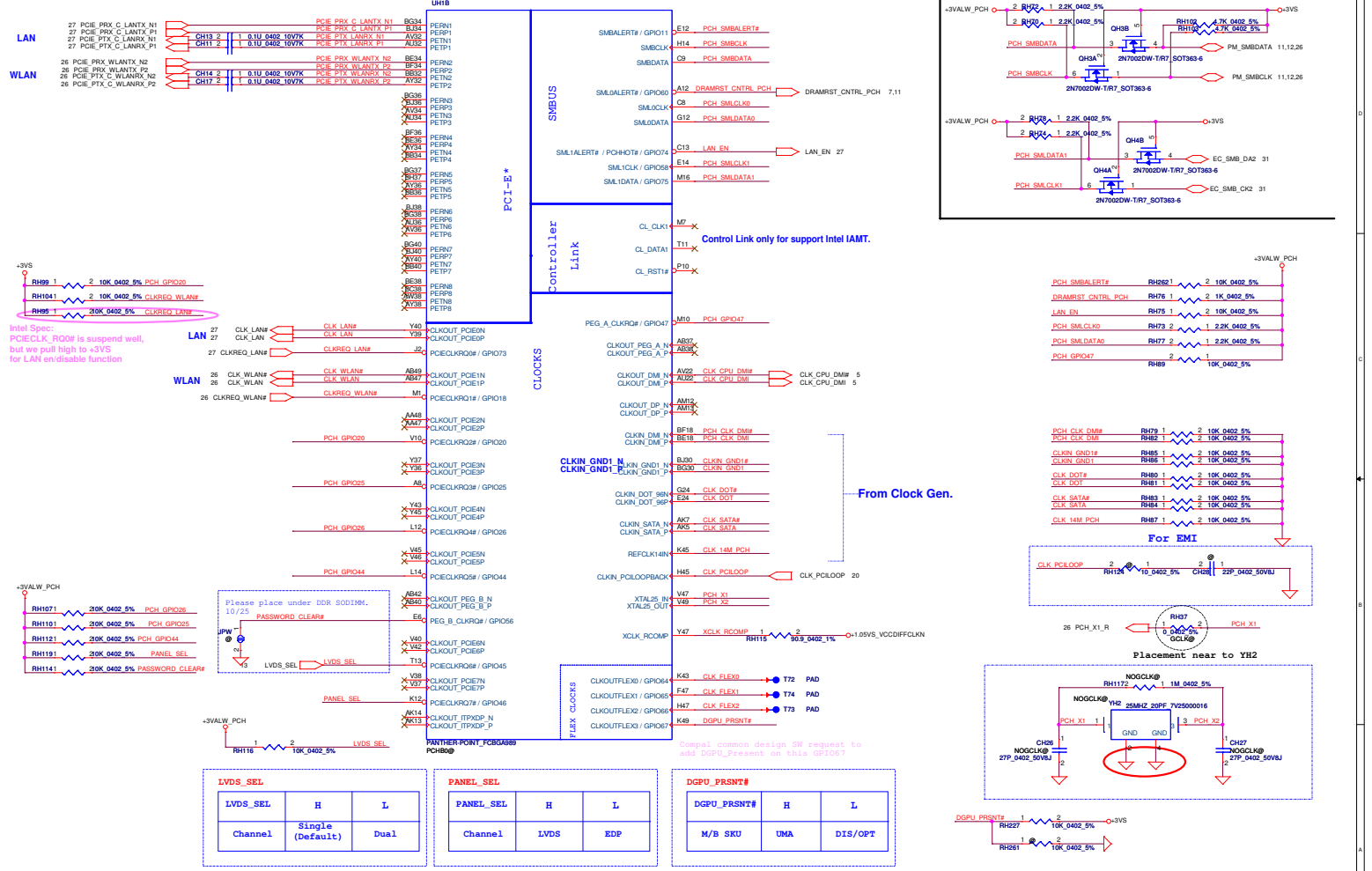


Socket: SP07000F500/SP07000H900  
 Please place U13 & U4 close to U2 PCH,  
 Please place RH66, RH67, RH68 near UH3  
 Please place RH267 near RH66, Please place RH271 near RH67,  
 Please place RH269 near RH68.



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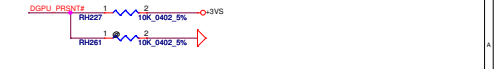
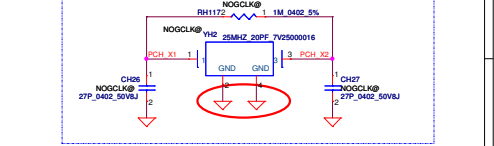
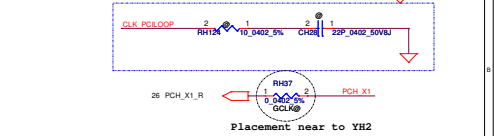
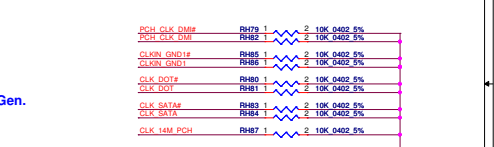
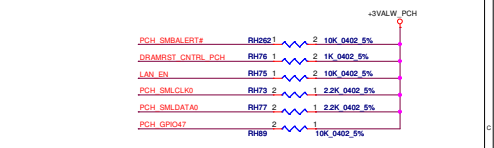
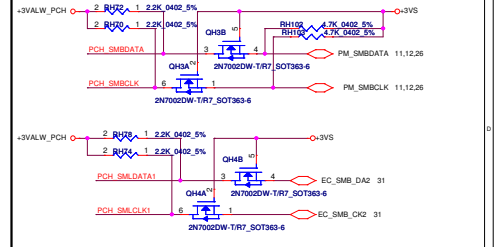
Intel Spec: PCIeCLK\_ROOT is suspend well, but we pull high to +3VS for LAN enable/disable function

Original common design SW request to add DGPU\_Present on USB GP1067

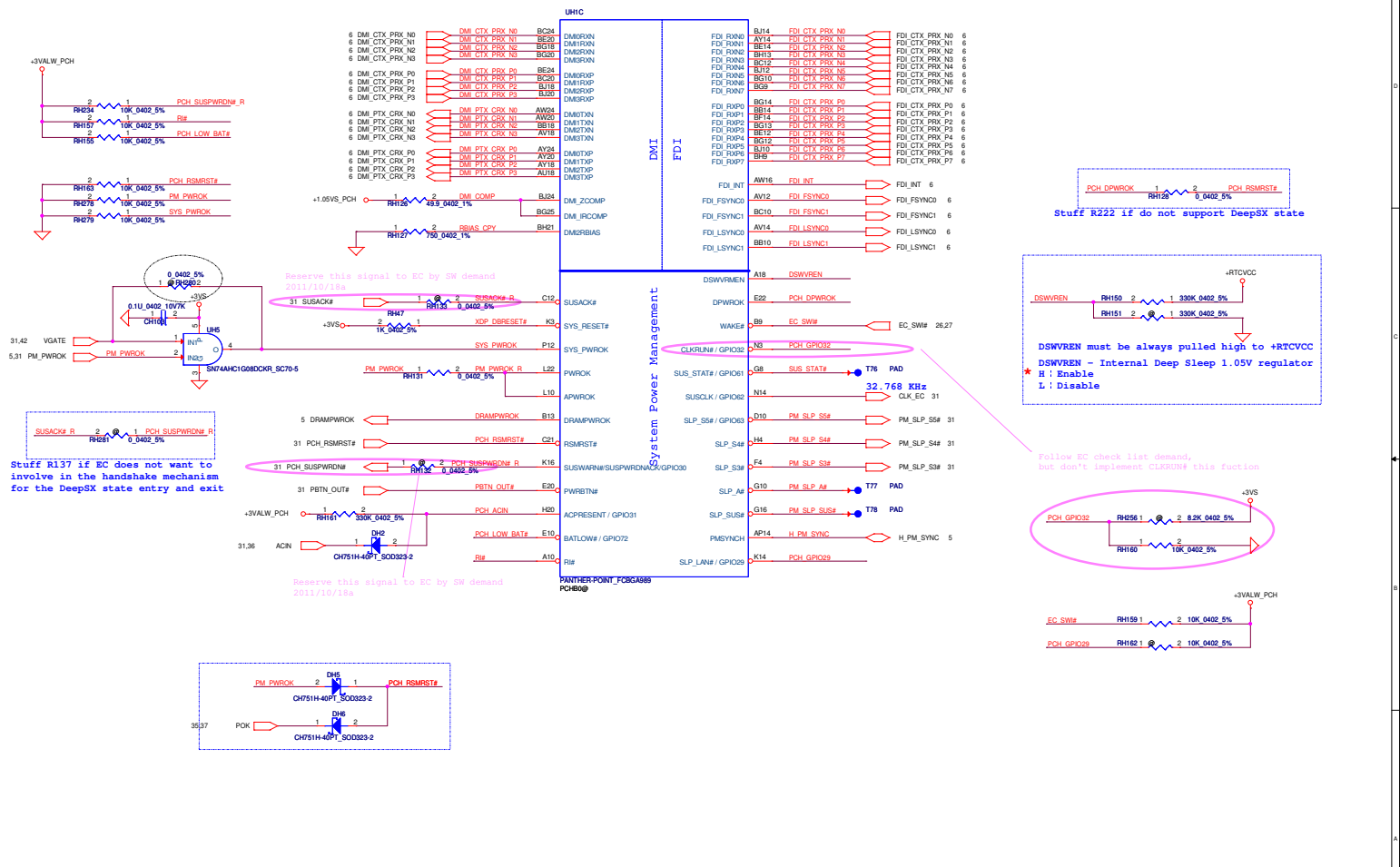
LVDS_SEL	H	L
Channel	Single (Default)	Dual

PANEL_SEL	H	L
Channel	LVDS	EDP

DGPU_PRSN#	H	L
M/B SKU	UMA	DIS/OPT

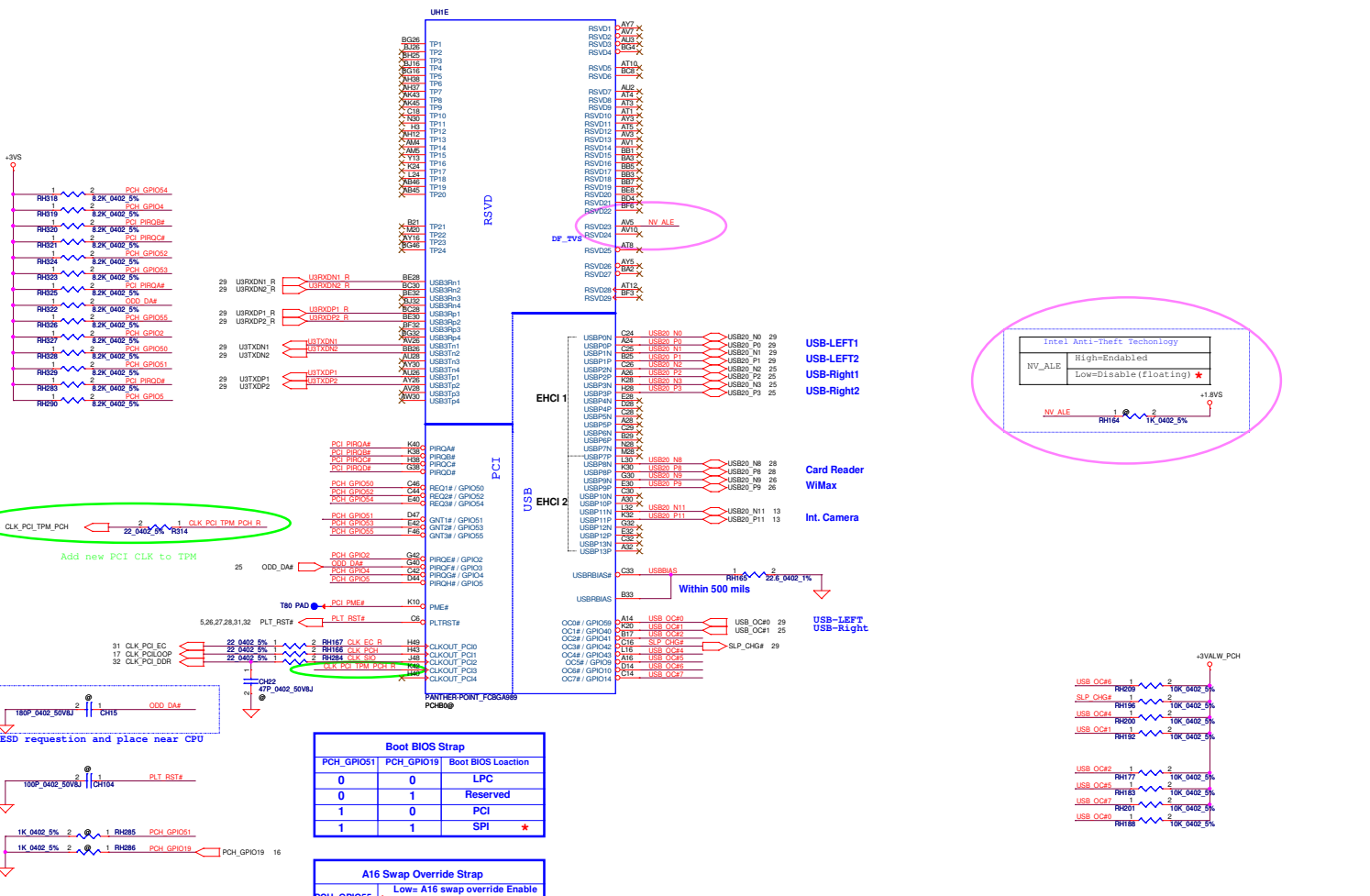


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Doc. Control		Document Number	QFKAA	Rev	0.2
Date	Thursday, February 15, 2012	Sheet	17	of	48



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Doc Number	PCH_DMI/FDI/PM			Rev
Doc Name	QFKAA			0.2
Date	Thursday, February 16, 2012			Sheet 18 of 48



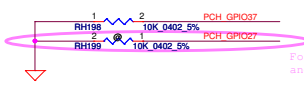
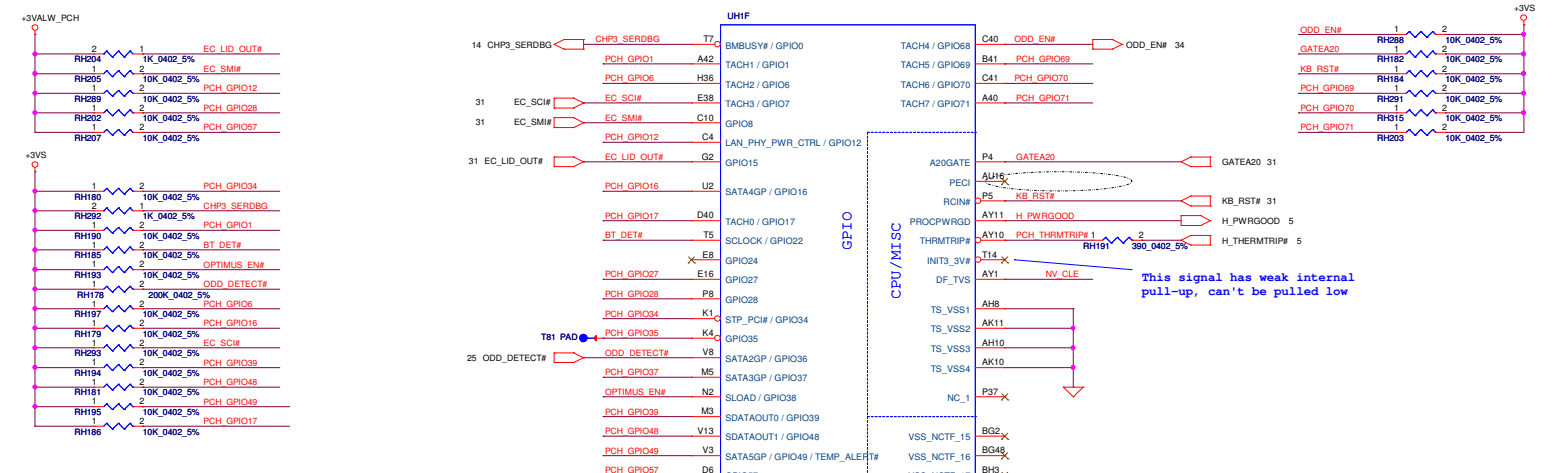


29 CLK\_PCI\_TPM\_PCH ← 22\_0402 5% R314  
 Add new PCI CLK to TPM

PCH_GPIO51	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

PCH_GPIO55	Low= A16 swap override Enable	High= A16 swap override Disable
*		

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Docu	QFKAA	Sheet	20 of 48
Date:	Thursday, February 16, 2012		



Follow Compal ORB and Intel Check list 466063 V1.5

**GPIO28**  
 On-Die PLL Voltage Regulator  
 H: Enable  
 L: Disable

RH206 1 2 1K 0402 5% PCH\_GPIO28

**3D\_DET#**

3D_DET#	H	L
SKU	Non3D	3D

**GPIO8**  
 Integrated Clock Chip Enable (Removed)  
 H: Disable  
 L: Enable

RH2981 1 2 1K 0402 5% EC\_SMI#

Integrated clock enable functionality is achieved by soft-strap. The current default is clock enable

**OPTIMUS\_EN#**

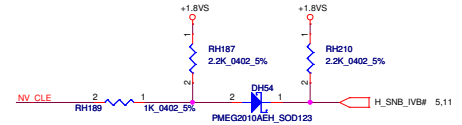
OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

**HDD2\_DET#**

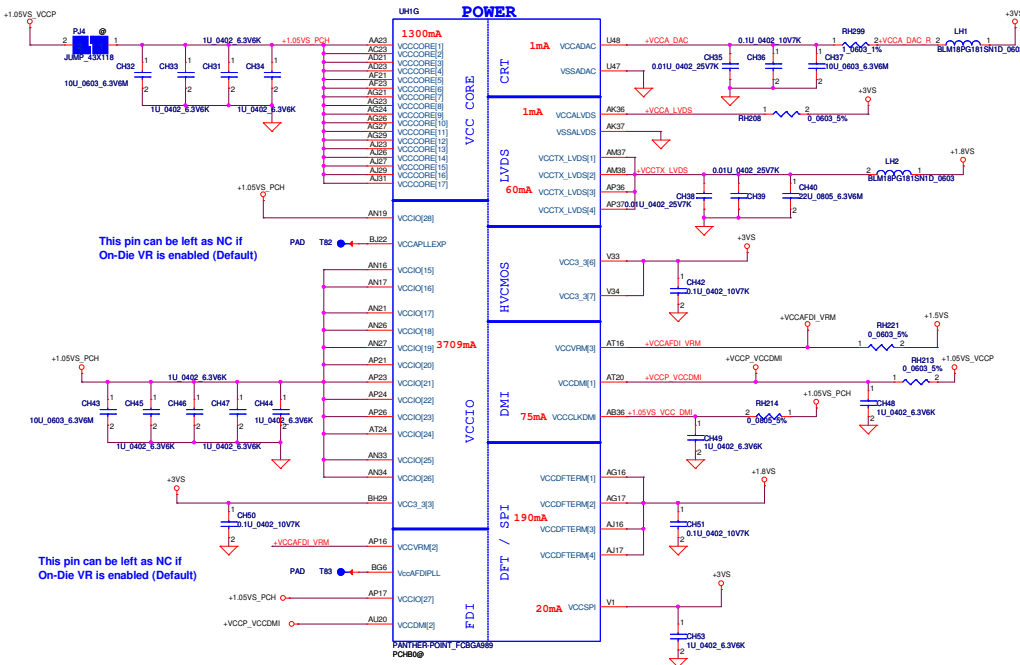
HDD2_DET#	H	L
SKU	ONE HDD	TWO HDD

**DMI & FDI Termination Voltage**

NV\_CLE Set to VCC when HIGH  
 Set to VSS when LOW



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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Part Number	PCH_CPU/GPIO	
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				Customer		
				Date	Thursday, February 16, 2012	Sheet 21 of 48



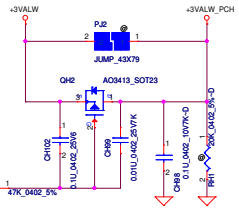
PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	50 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADP1LLA	1.05	0.08
VccADP1LLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDPTERM	1.8	0.002
VccRTC	3.3	N/A
VccBus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSDMI	1.05	0.095
VccDIFFCLKM	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

This pin can be left as NC if On-Die VR is enabled (Default)

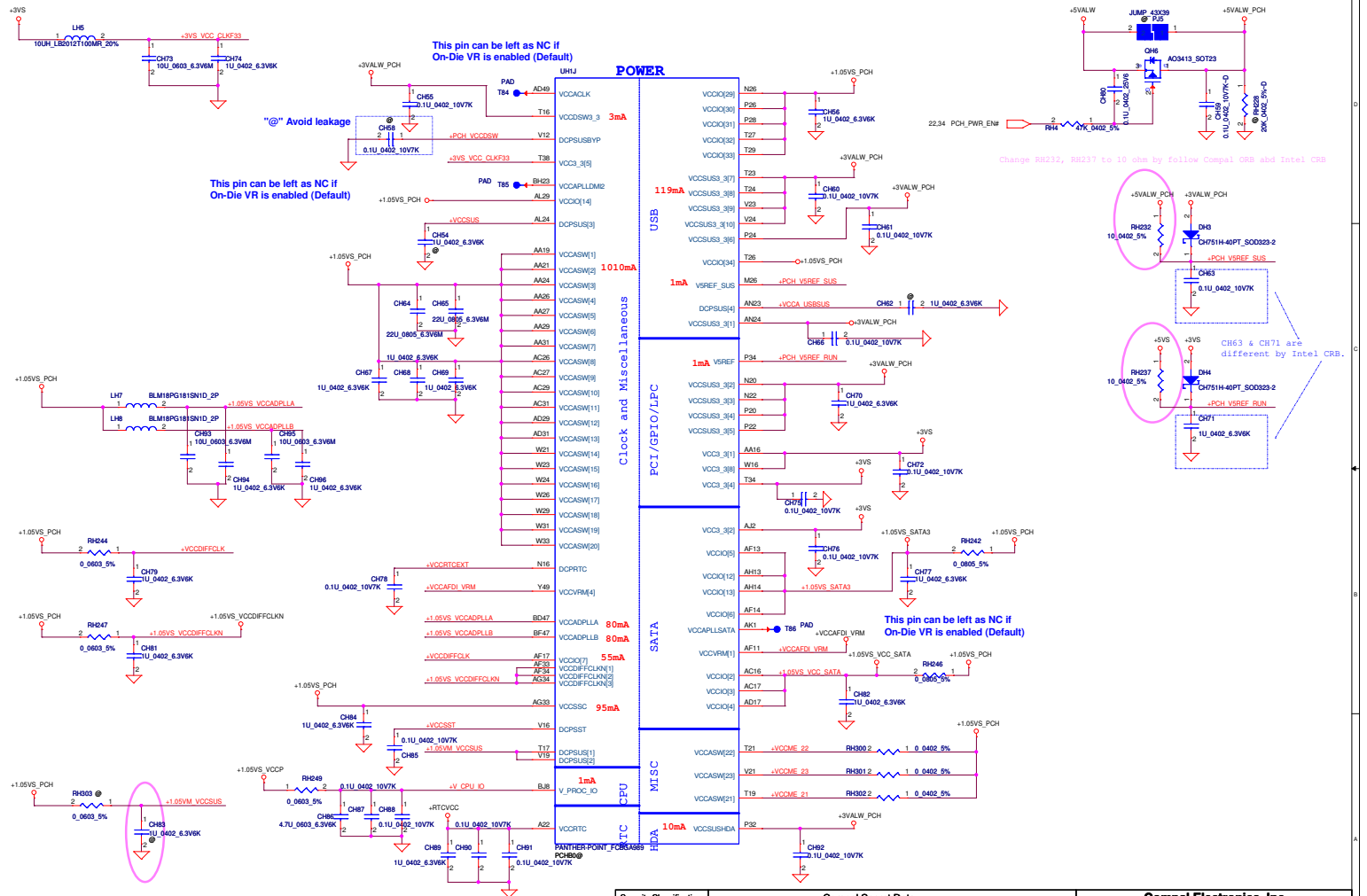
This pin can be left as NC if On-Die VR is enabled (Default)

**+3VALW to +3V\_PCH**

Vgs = -4.5V, Id = 3A, Rds = 97mOhm



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Sheet	22	of	48



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				0.2
Date: Thursday, February 16, 2012				Sheet 23 of 48

Compal Electronics, Inc.  
**PCH\_POWER-2**  
**QFKAA**

**UHH**

VSS[0]	
AA17	VSS[1]
AA2	VSS[2]
AA3	VSS[3]
AA33	VSS[4]
AA34	VSS[5]
AA11	VSS[6]
AA14	VSS[7]
AA15	VSS[8]
AA4	VSS[9]
AA1	VSS[10]
AA5	VSS[11]
AA7	VSS[12]
AA13	VSS[13]
AA2	VSS[14]
AA21	VSS[15]
AA3	VSS[16]
AA34	VSS[17]
AA8	VSS[18]
AA10	VSS[19]
AA11	VSS[20]
AA12	VSS[21]
AA13	VSS[22]
AA15	VSS[23]
AA16	VSS[24]
AA24	VSS[25]
AA3	VSS[26]
AA33	VSS[27]
AA34	VSS[28]
AA38	VSS[29]
AA39	VSS[30]
AA38	VSS[31]
AA39	VSS[32]
AA4	VSS[33]
AA40	VSS[34]
AA4	VSS[35]
AA43	VSS[36]
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AA45	VSS[38]
AA46	VSS[39]
AA8	VSS[40]
AA2	VSS[41]
AA3	VSS[42]
AA10	VSS[43]
AA14	VSS[44]
AA16	VSS[45]
AA18	VSS[46]
AA19	VSS[47]
AA2	VSS[48]
AA26	VSS[49]
AA28	VSS[50]
AA27	VSS[51]
AA29	VSS[52]
AA31	VSS[53]
AA36	VSS[54]
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AA45	VSS[56]
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AA47	VSS[58]
AA48	VSS[59]
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AA3	VSS[68]
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AA34	VSS[70]
AA39	VSS[71]
AA19	VSS[72]
AA21	VSS[73]
AA4	VSS[74]
AA4	VSS[75]
AA43	VSS[76]
AA34	VSS[77]
AA12	VSS[78]
AA3	VSS[79]

PANTHER POINT\_FCBGA389

PCH@P

**UHI**

AA4	VSS[169]
AA22	VSS[169]
AA46	VSS[169]
AA6	VSS[169]
AA1	VSS[169]
AA11	VSS[169]
AA19	VSS[169]
AA2	VSS[169]
AA3	VSS[169]
AA4	VSS[169]
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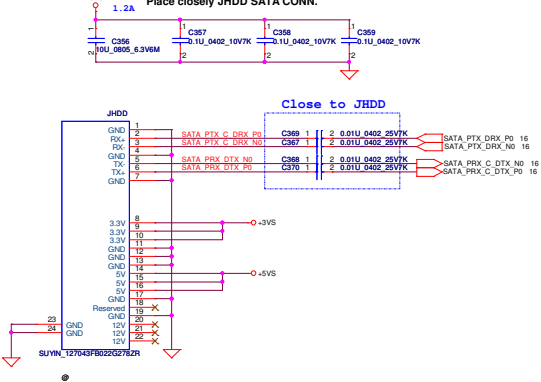
PANTHER POINT\_FCBGA389

PCH@P

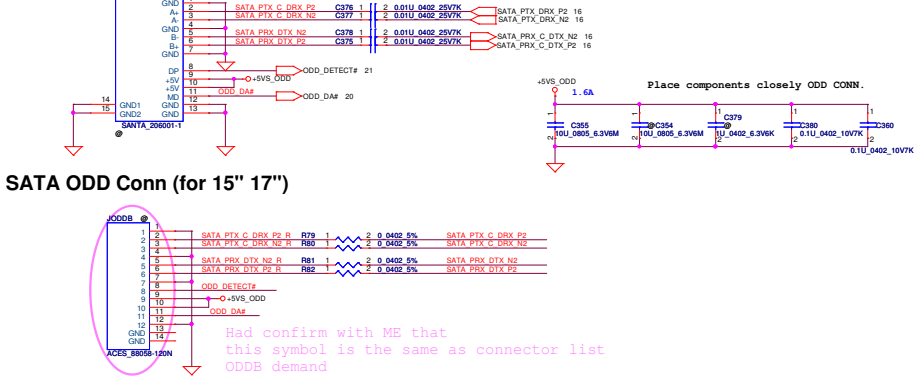
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Date:	Thursday, February 16, 2012	Sheet	24	of	48



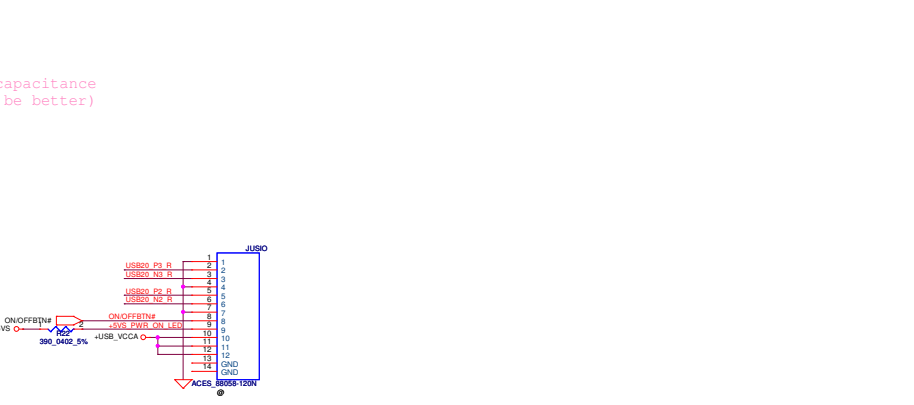
**SATA HDD Conn.**



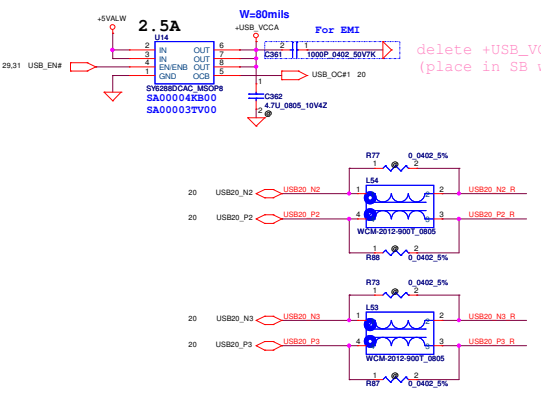
**SATA ODD Conn (for 14")**



**SATA ODD Conn (for 15" 17")**

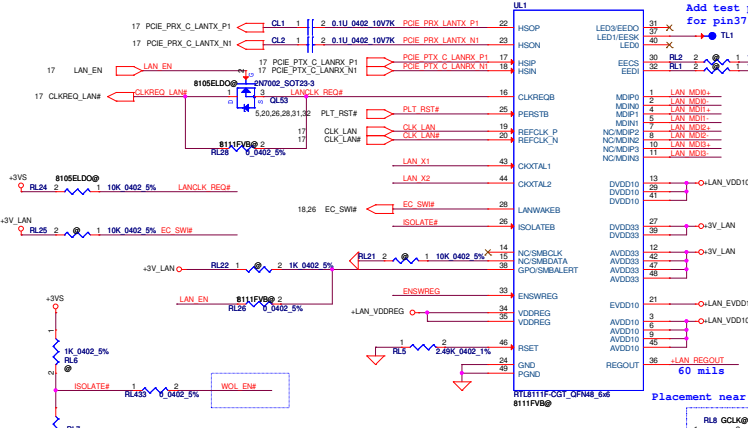


**Power Button & RUSB connector**

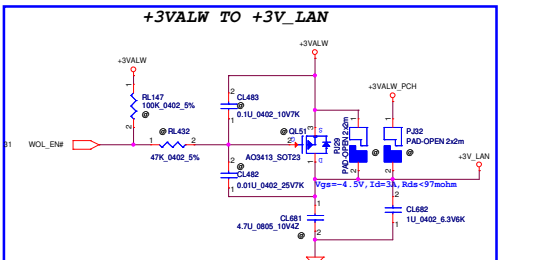


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/03	Deciphered Date	2012/12/31	Title	SATA-HDD/ODD/USB
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Size	Document Number	Date	Thursday, February 18, 2012	Sheet	25 of 48
	QFKAA				Rev 0.2





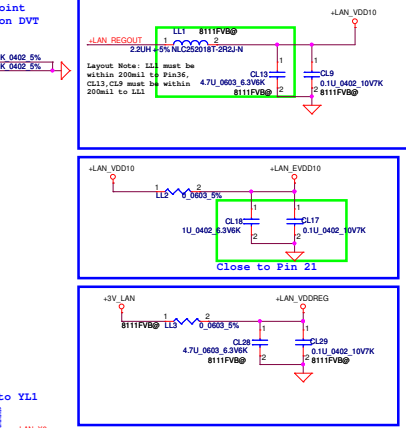
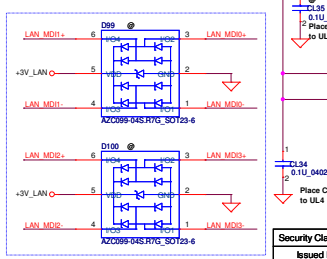
WOL_EN	LOW	HIGH	HIGH
Sx Enable			
Wake up			
Sx Disable			
Wake up			



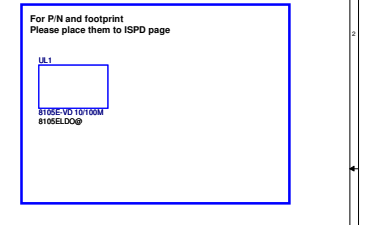
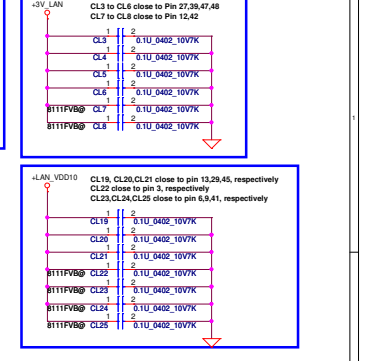
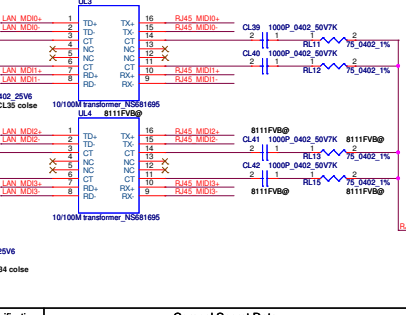
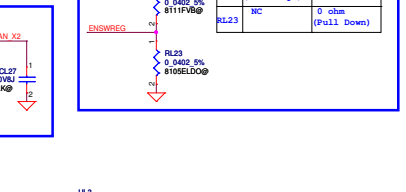
**+3V\_LAN rising time (10%-90%) need > 1ms and <100ms.**

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

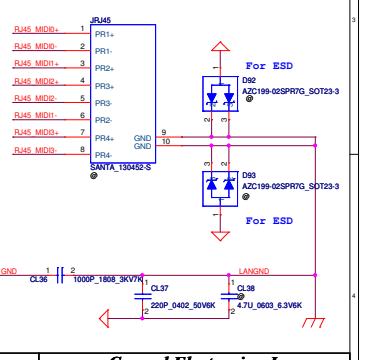
\* S3: after SUSP# assert low over 100ms  
S4/S5: after SYSON assert low over 100ms



B105E-VL/VD	B105E-VL/VD	
B111F-VB	B111F-VB	
Input Mode	LDO Mode	
RL4	0 ohm	NC
RL23	NC	0 ohm (Pull Down)



For P/N and footprint  
Please place them to ISPD page



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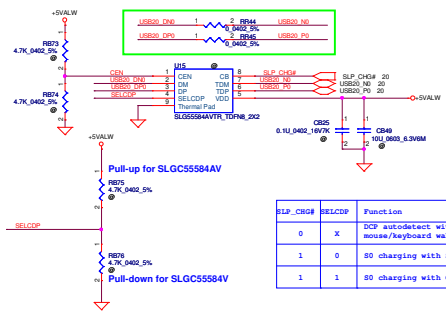
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Custom	QMLE4 LA-8864P	02

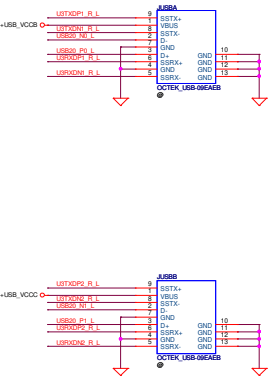
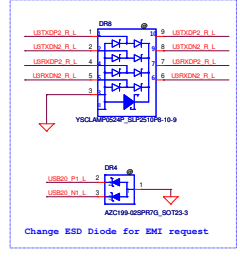
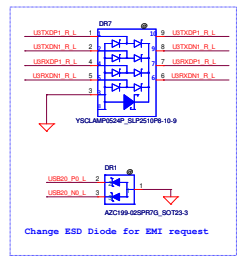
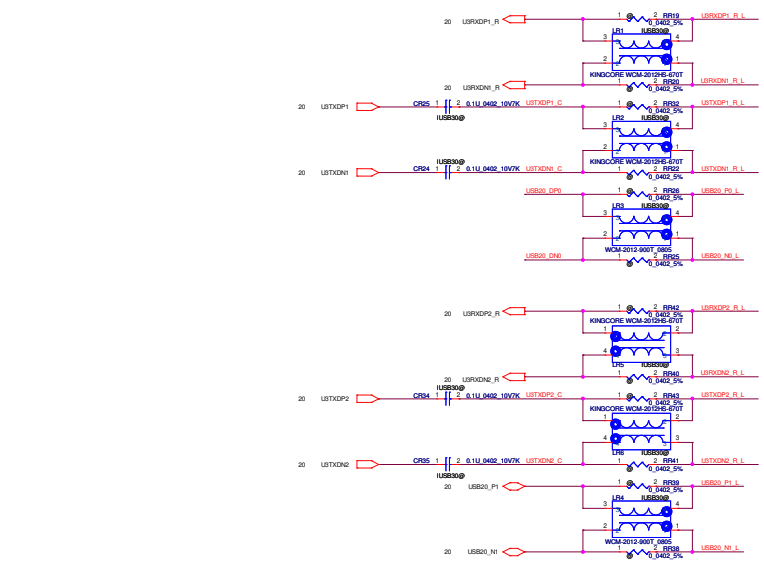
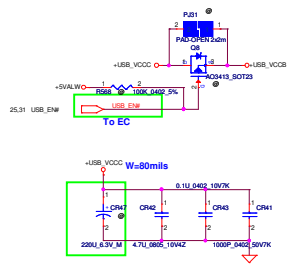
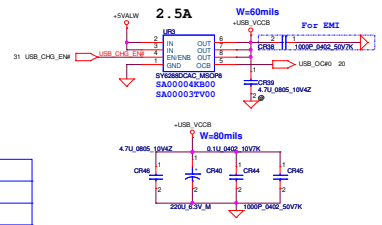
Date: Thursday, February 16, 2012 Sheet 27 of 48



# Sleep & Charge Function

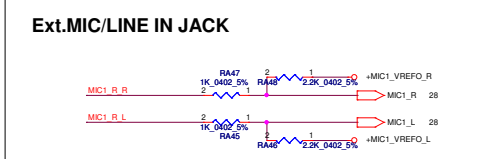
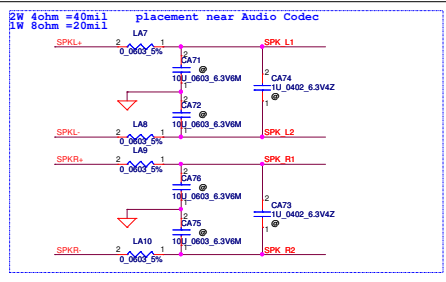
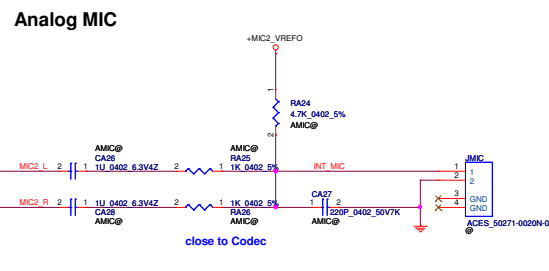
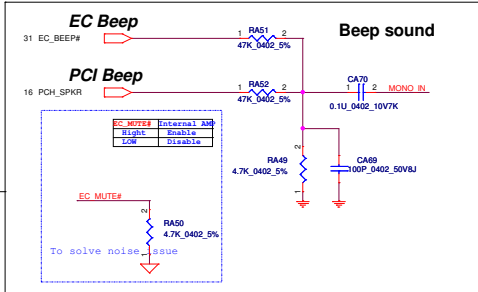
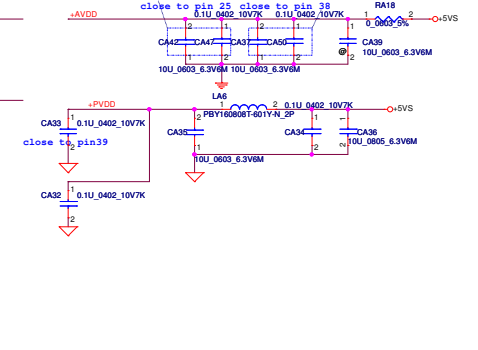
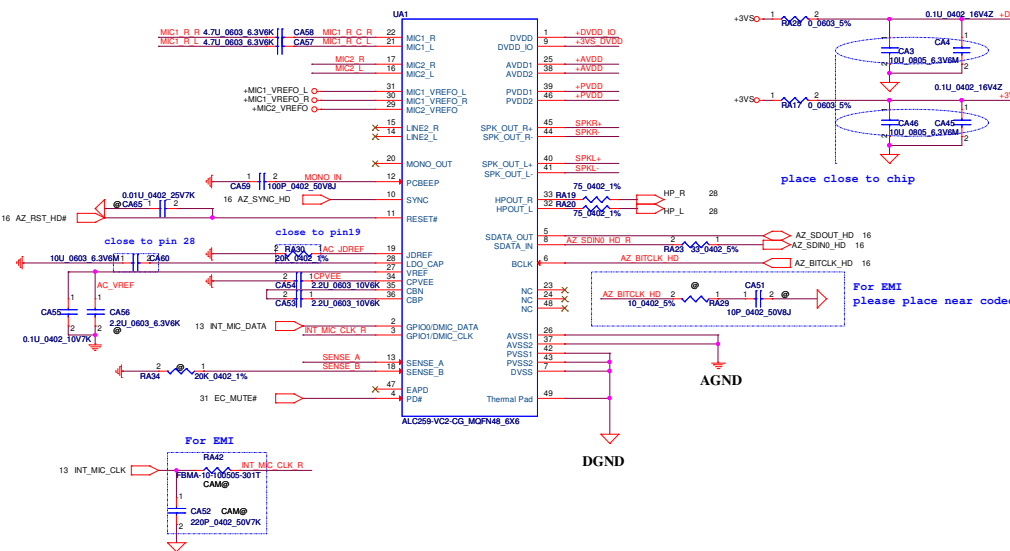


SLEEP_CS#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	SD charging with SDP only
1	1	SD charging with CDP or SDP only

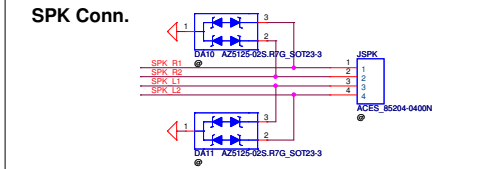
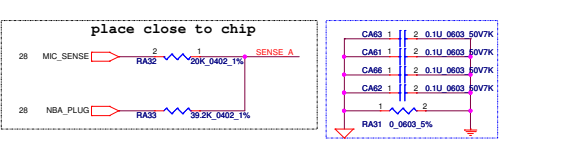


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			Page: 22 of 22

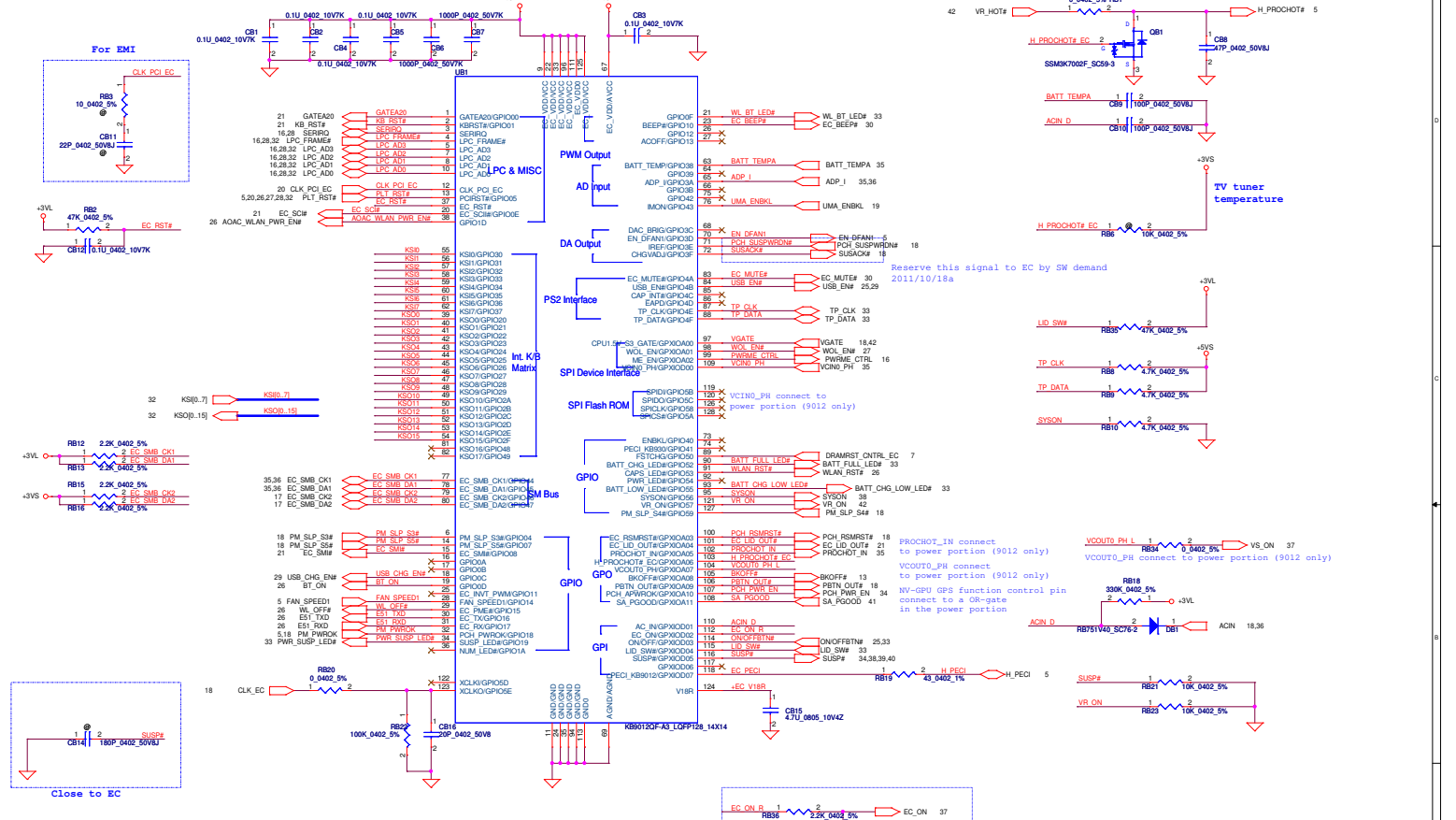
35mA for 3.3V level



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	10K	PORT-F (PIN 20)	

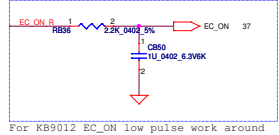


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Date:	Thursday, February 16, 2012	Sheet	30	of 48	



**Voltage Comparator Pins FOR 9012 A3**

VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



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Date	Thursday, February 16, 2012	Sheet	31	of 48	

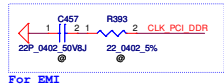
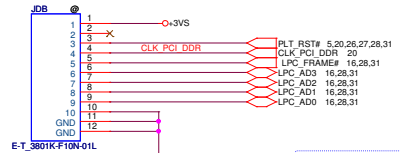
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Compal Electronics, Inc.

SPI Flash (128KB)

Lid SW

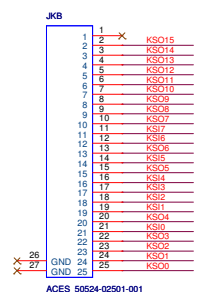
LPC Debug Port Place the JDB under DDR DIMM.



For EMI

KEYBOARD CONN.

G-Sensor



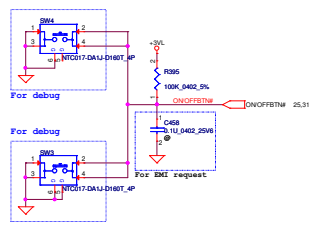
KSO0	C406	100P_0402_50VBJ
KSO1	C406	100P_0402_50VBJ
KSO2	C404	100P_0402_50VBJ
KSO3	C408	100P_0402_50VBJ
KSO4	C425	100P_0402_50VBJ
KSO5	C407	100P_0402_50VBJ
KSO6	C431	100P_0402_50VBJ
KSO7	C422	100P_0402_50VBJ
KSO8	C423	100P_0402_50VBJ
KSO9	C424	100P_0402_50VBJ
KSO10	C409	100P_0402_50VBJ
KSO11	C427	100P_0402_50VBJ
KSO12	C411	100P_0402_50VBJ
KSO13	C428	100P_0402_50VBJ
KSO14	C421	100P_0402_50VBJ
KSO15	C412	100P_0402_50VBJ
KSO16	C415	100P_0402_50VBJ
KSO17	C416	100P_0402_50VBJ
KSO18	C417	100P_0402_50VBJ
KSO19	C418	100P_0402_50VBJ
KSO20	C419	100P_0402_50VBJ
KSO21	C413	100P_0402_50VBJ
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KSO23	C420	100P_0402_50VBJ

For EMI  
Close to KKB

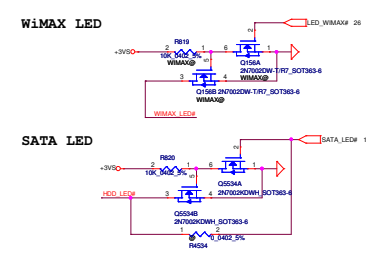
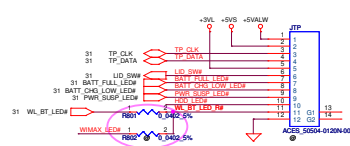
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Date	Thursday, February 18, 2011	Sheet	32	of	48



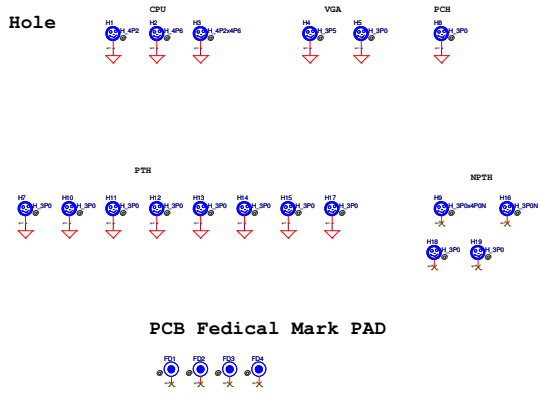
**Power Button**



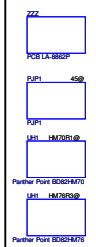
**Touchpad Connector**



**Screw Hole**



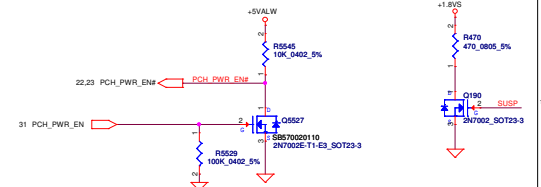
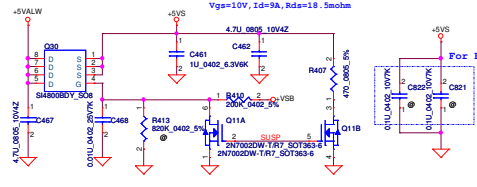
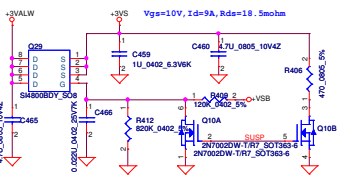
**ISPD**



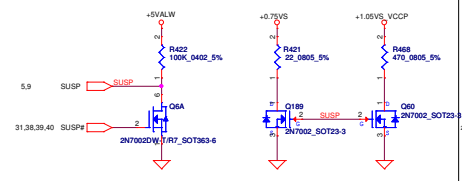
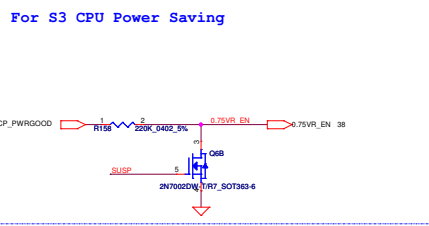
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**+3VALW TO +3VS**

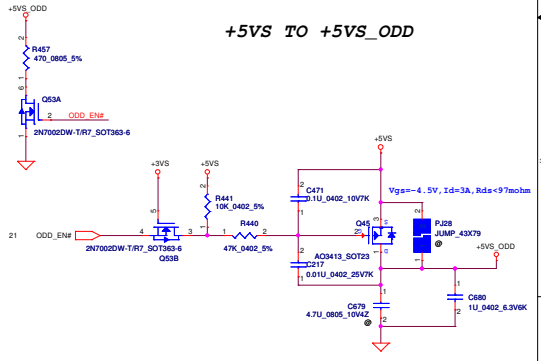
**+5VALW TO +5VS**



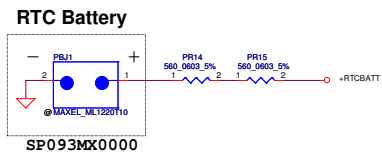
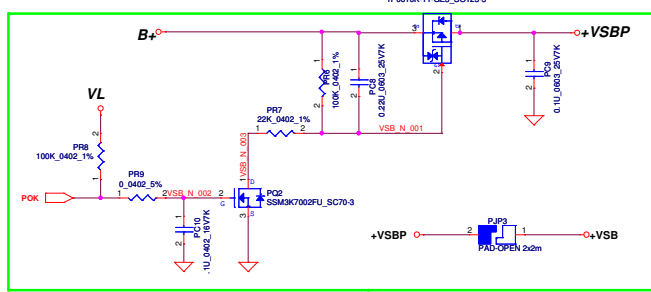
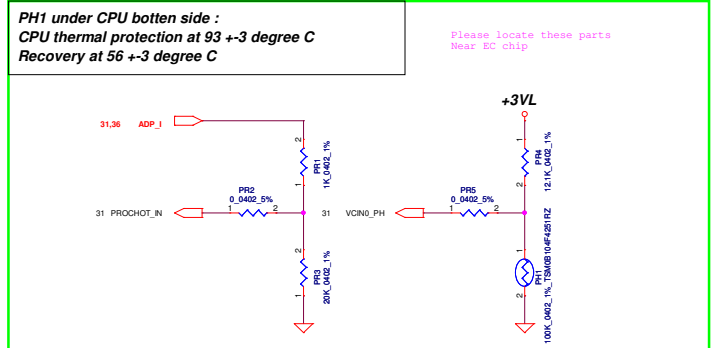
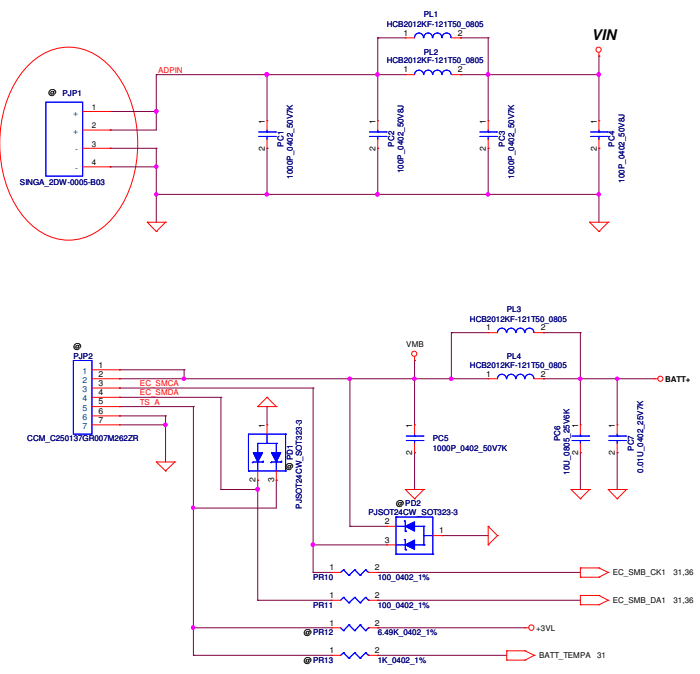
Un-used Dual MOS



**+5VS TO +5VS\_ODD**

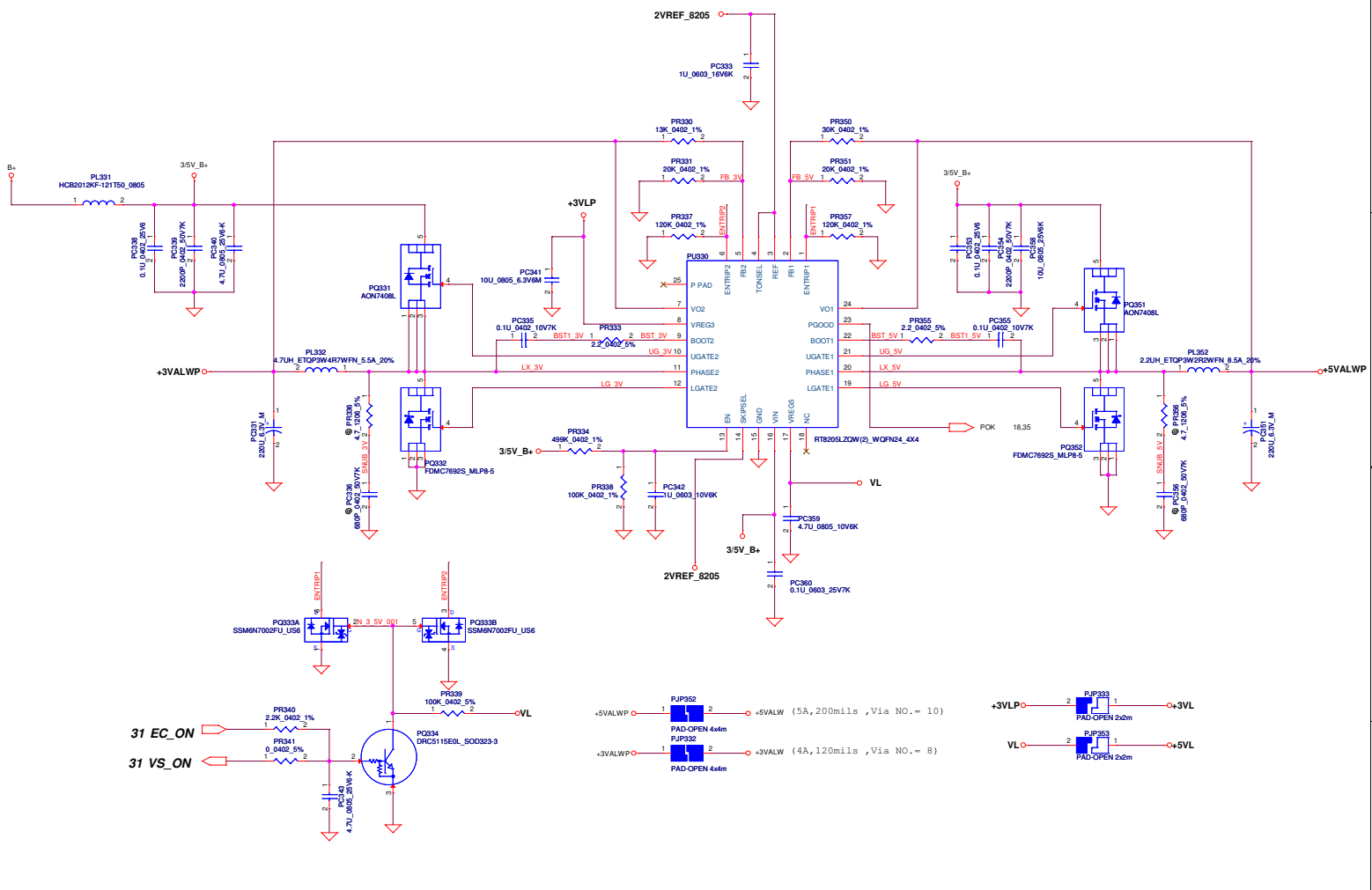


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Thursday, February 16, 2012	Sheet	35	of	48

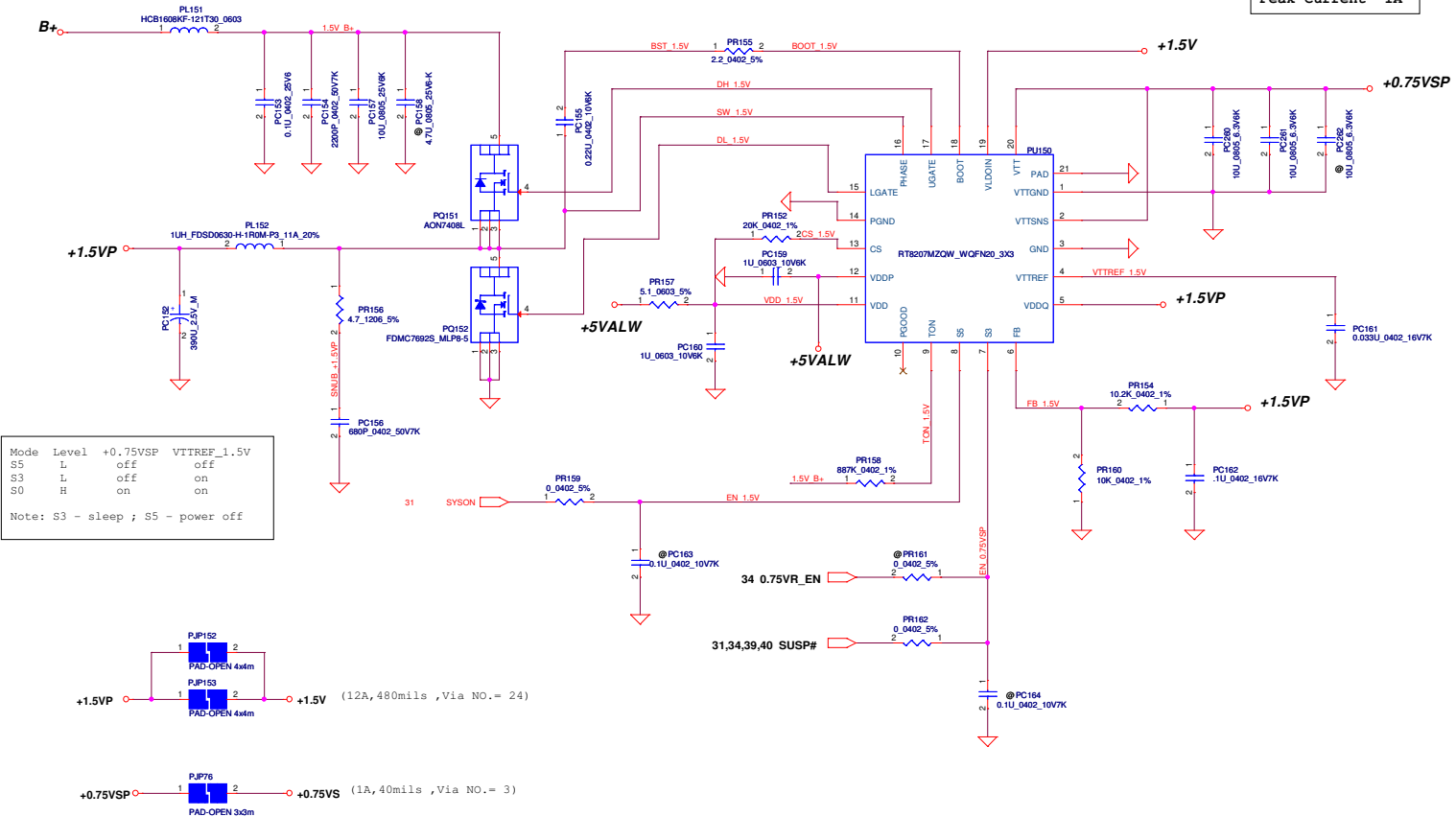




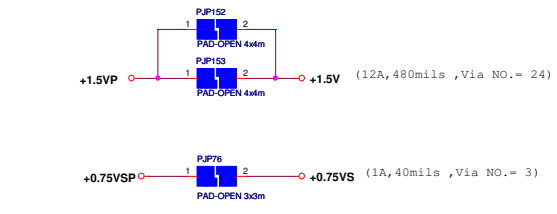
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				Date	Thursday, February 16, 2012
				Sheet	37 of 48

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**PWR-3.3VALWP/SVALWP**  
 QCLA4 LA-8861P M/B

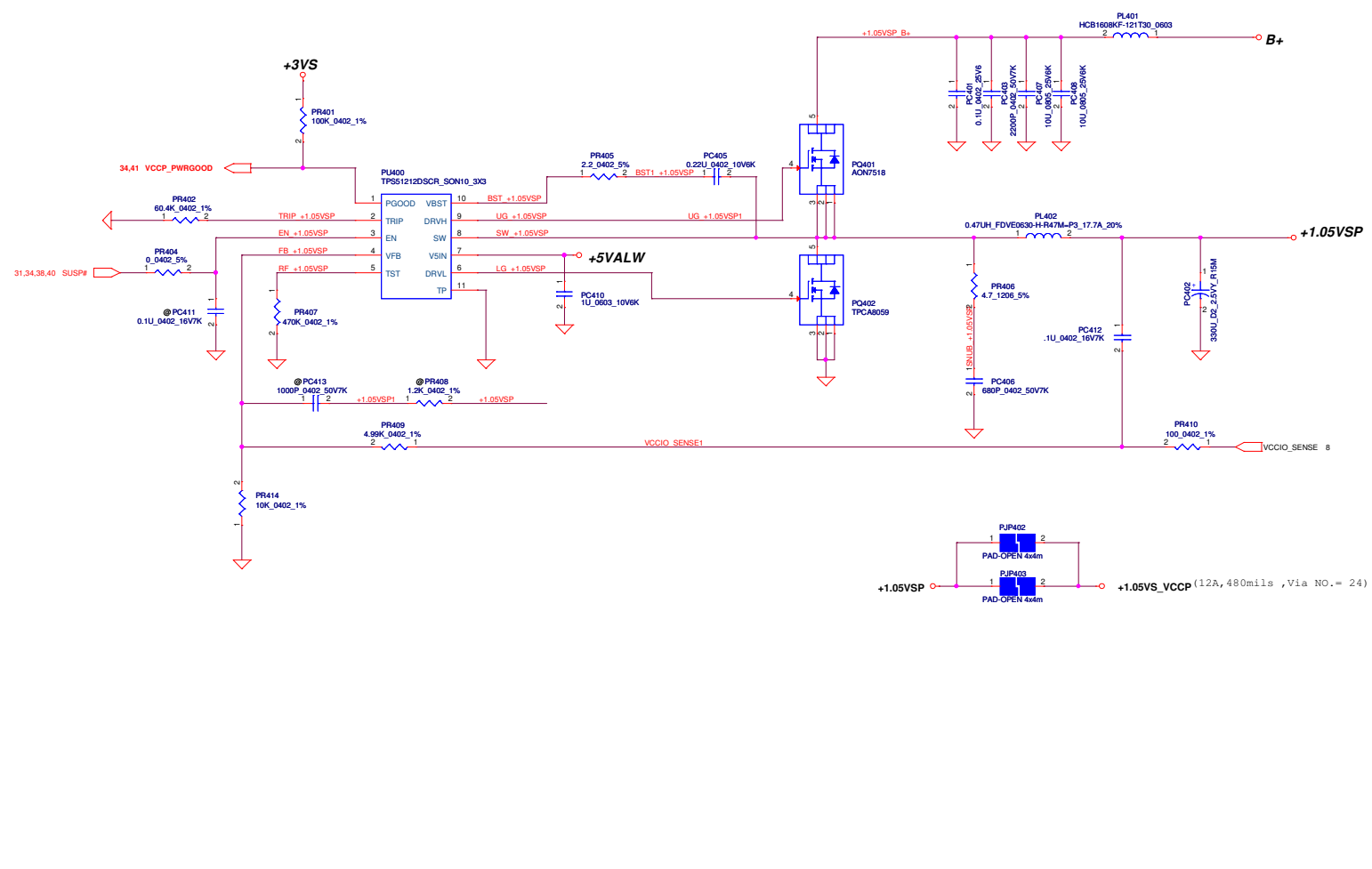
0.75Volt +/- 5%  
TDC 0.7A  
Peak Current 1A



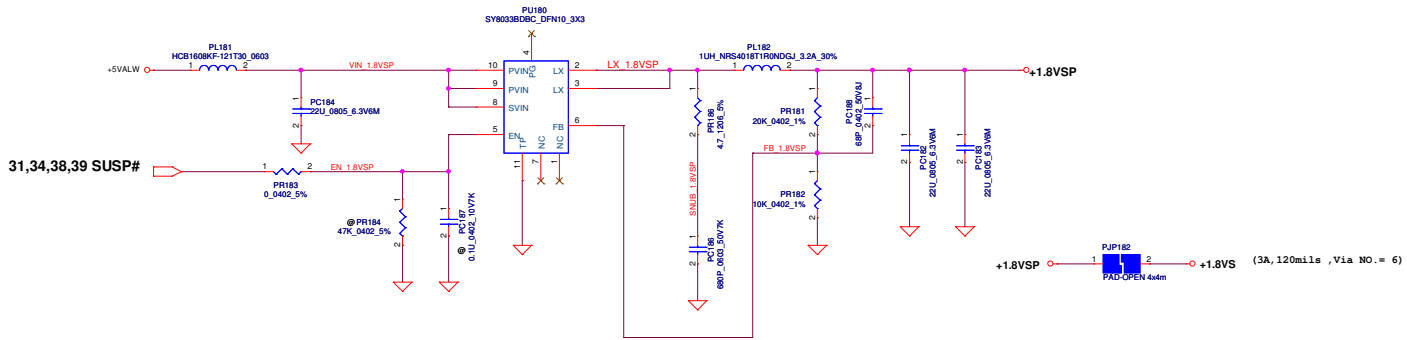
Mode Level +0.75VSP VITREF\_1.5V  
S5 L off off  
S3 L off on  
S0 H on on  
Note: S3 - sleep ; S5 - power off



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				Rev
				0.2
				Date: Thursday, February 16, 2012
				Sheet 38 of 48



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				Rev	0.2
Date:	Thursday, February 16, 2012	Sheet	39	of	48



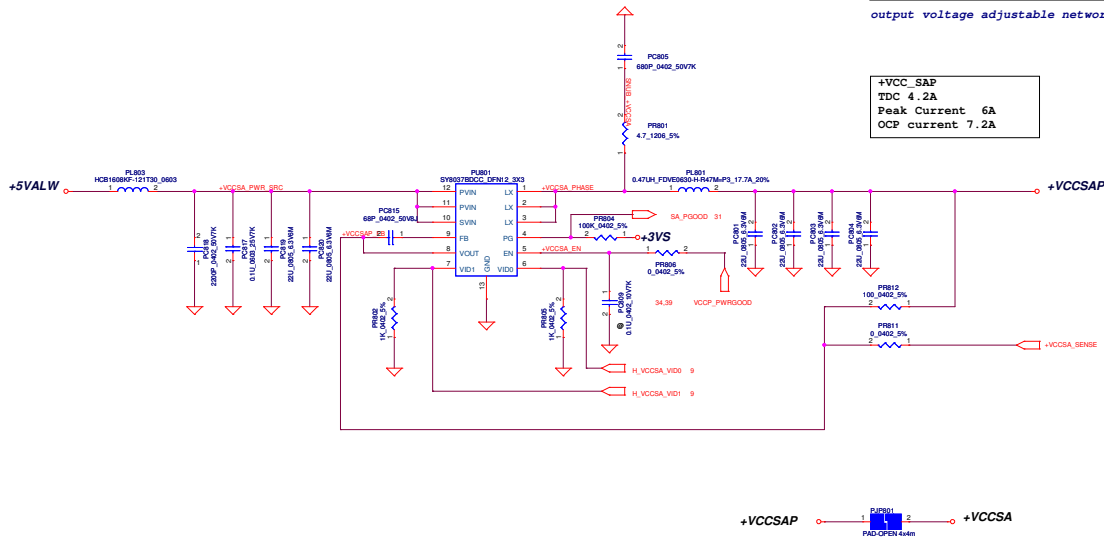
Security Classification	Compal Secret Data		Title	
Issued Date	2009/01/23	Deciphered Date	2012/12/31	<b>Compal Electronics, Inc.</b>
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				Size
				SAMSUNG
				02
				Date: Thursday, February 16, 2012
				Sheet 40 of 48



The 1k PD on the VCCSA VID's are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

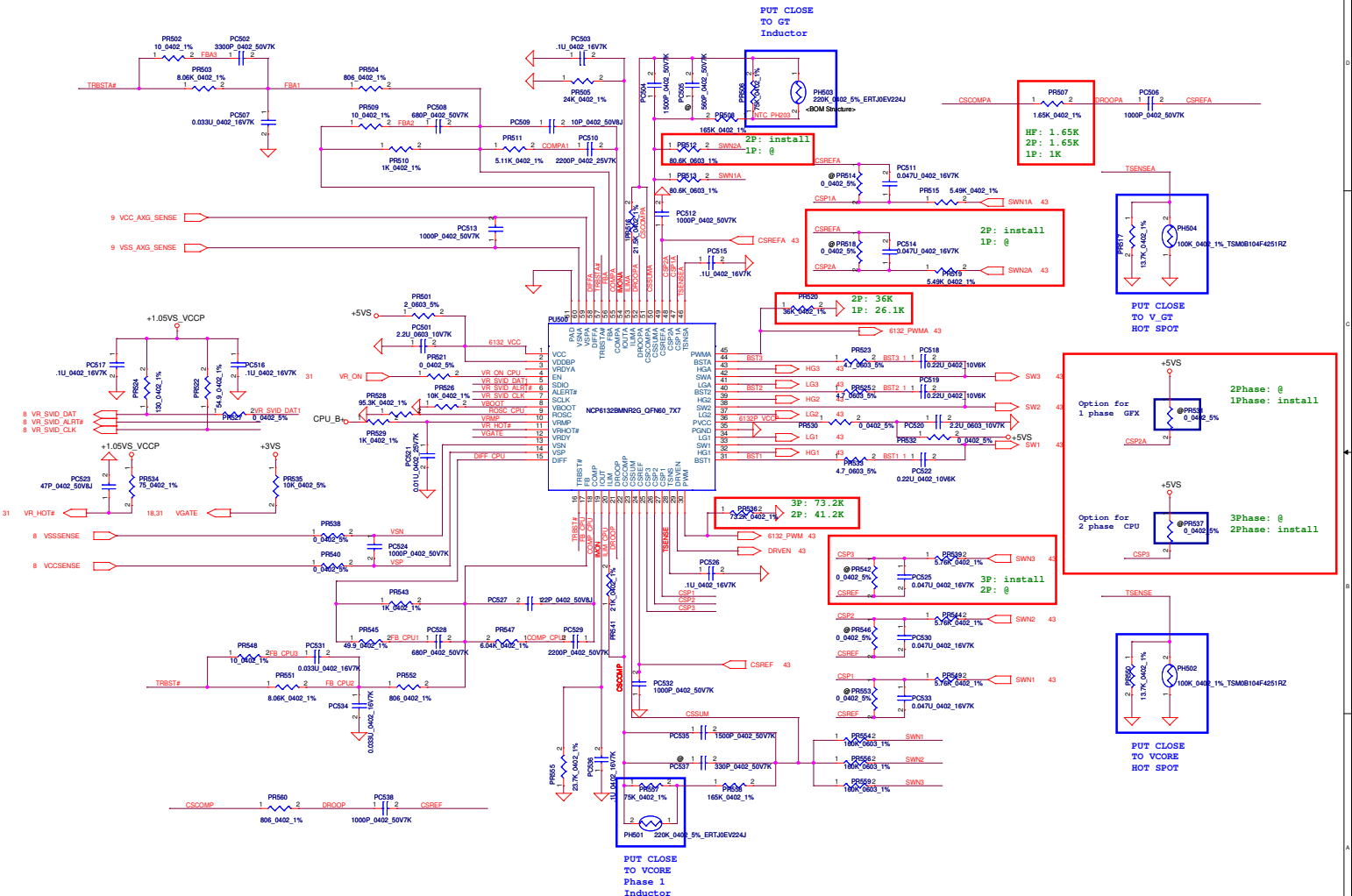
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



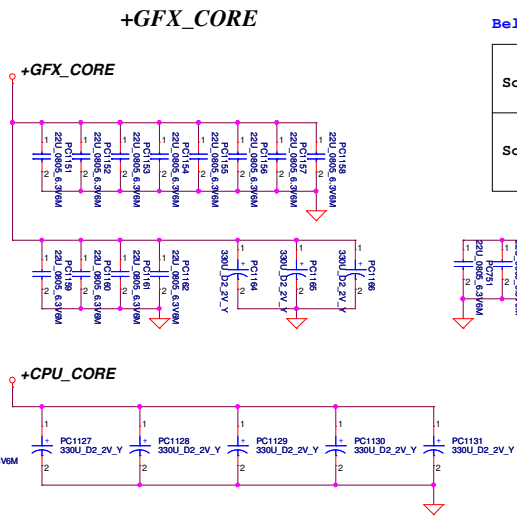
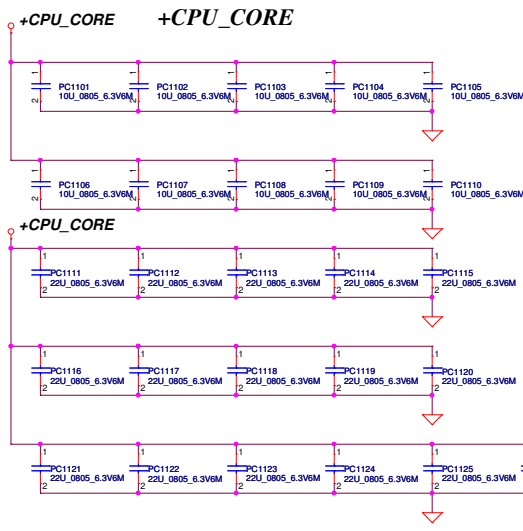
+VCC\_SAP  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

Security Classification	Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	<b>PWR-VCC_SAP</b>
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				Rev 0.2
				Date Thursday, February 16, 2012
				Sheet 41 of 48



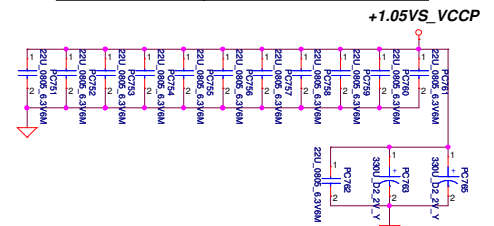
Security Classification	2009/12/01	Compal Secret Data	2010/12/31	Title	<b>PWR-CPU CORE</b>
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Docu	Custom
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Date	Thursday, February 16, 2012	Sheet	42	of	48





Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites



	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

Security Classification	Compal Secret Data		Title		<b>Compal Electronics, Inc.</b>	
Issued Date	2008/09/15	Deciphered Date	2012/12/31	PWR - PROCESSOR DECOUPLING		
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				Date	Thursday, February 16, 2012	Sheet 44 of 48

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2011/09/29		P51-FWR_+3VALWP/+5VALWP	Change PU330 to RT8205L
2.	2011/09/29		P53-FWR_+1.05VS_VCCP/+16VSP	Change PU400 to RT8237C
3.	2011/09/29		P54-FWR_+VCCSAP/1.8VSP	Change PU450 to SY8037B
4.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change HMOS to MDV1525
5.	2011/09/29		P53-FWR_+1.05VS_VCCP/+16VSP	Change HMOS to MDV1525
6.	2011/09/29		P49-FWR_BATTERY CONN / OTP	Change PD5,PD6 to SCA00001G00
7.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PR589 from 348 to 8.06k
8.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PR590 from 3.65k to 806
10.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PC574 from 680P to 0.033u
11.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PC577 from 4700P to 0.033u
12.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PR548 from 1.21k to 8.06k
13.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PR550 from 10.7k to 806
14.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PC547 from 680P to 0.033u
15.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Change PC551 from 4700P to 0.033u
16.	2011/09/29		P57-FWR +CPU_CORE DECOUPLING	Add snubber and boost resistor
17.	2011/09/29		P49-FWR_BATTERY CONN / OTP	Add PR22 30k, PR27 100k, PR32 0 Ohm
18.	2011/09/29		P51-FWR_+3VALWP/+5VALWP	Change PC360 to SE000006R80
19.	2011/09/29		P49-FWR_BATTERY CONN / OTP	Add PR17 14k, PR33 0 Ohm
20.	2011/09/29		P51-FWR_+3VALWP/+5VALWP	Add PR373 0 Ohm

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/11	Deciphered Date	2011/11/11	Title	<b>Power PIR</b>
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				Date	Thursday, February 16, 2012
				Sheet	45 of 48

# HW PIR (Product Improve Record)

QCLA4.5 LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.0 TO 0.1

GERBER-OUT DATE: 2011/12/30

NO DATE PAGE MODIFICATION LIST PURPOSE

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	11/24	33	Change P33 ALC280 schematic to ALC259 schematic.	For audio function
2	11/24	34	Change JEXMIC.4 JACK_SENSE to MIC_SENSE.	For audio function
3	11/24	35	Delete UB3, RB26, CB18, RH296	For delete CIR function
4	11/24	6,13,21	Delete QC1, RC4, C261, U17, R147, R103, R360, R392, R390, R1441~1442, R361, R106, RH304	For LVDS only
5	11/24	6,13,17	Delete Q23, C293, R62, R389, R120, R79, R97, L60, R262~265, R299~300, RH275, R1440	For LVDS only
6	11/24	6,13	Delete CPU_EDP_HPD, +LCD_VDD_R, +PANEL_VDD, LVDS_ENVDD, +3VS_LVDSDDC	For LVDS only
7	11/24	13	Delete D15 BOM structure and JLVDS.10 connect to +3VS	For LVDS function
8	11/24	13	Add J17 connector and change JLVDS from 40 to 30 pin connector.	For LVDS function
9	11/24	20	Delete USB20_N13, USB20_P13	For no Glasses free 3D Panel
10	11/24	13	Change RC82 BOM structure from IEDP@ to @.	For LVDS function
11	11/24	5,17	Change RC157, RC158, RH119, RH203 BOM structure from LVDS@ to mount.	For LVDS function
12	11/24	17	Delete CLK_CPU_EDP#, CLK_CPU_EDP	For LVDS only
13	11/24	15	Delete CEC schematic and JHDMI.13 HDMI_CEC net	For no CEC support
14	11/24	15	Delete R570, D55 and change U9.4 HDMI_HPD_R to HDMI_HPD	For HDMI HPD
15	11/25	15	Change L8-11 to SM070001U00	For HDMI signal
16	11/25	15	Delete U9.5 from +5V1 to +5VS	For HDMI HPD
17	11/25	33	Change Audio codec schematic	For ALC259-VC2
18	11/25	17,29	Delete CH16, CH18, card reader schematic	For RTS5129
19	11/25	26	Delete FP & B-CAS schematic	For no support FP & B-CAS function
20	11/25	35,37	Delete JFUN, R8, R1466~1467, D90	For no support JFUN
21	11/25	20,27	Delete USB20_N10, USB20_P10, USB20_N12, USB20_P12	For no support TV tuner & 3G
22	11/25	27	Delete RH181 & 3G, B-CAS, JET schematic	For no support TV tuner & 3G
23	11/25	16,27	Delete mSATA schematic	For no support mSATA function
24	11/25	27	Delete RCL3, 271@ component and net OSC_IN_R_R, OSC_IN_R	For no support S&M function
25	11/25	6	Change RC3 from 1Kohm to 10Kohm (SD028100280)	For no support eDP function
26	11/25	35	Delete UB1.89 HDPACT, UB1.86 HDPLLOCK, UB1.68 HDPINT	For no support G-SENSOR function
27	11/28	35	Change PCH_PWR_EN from UB1.70 to UB1.68 and add UB1.70 EN_DFAN1	For support RPM FAN
28	11/28	5,35	Delete C1-4, R1~2, D1 and UB1.26 FANPWM	For no support PWM FAN
29	11/29	25	Delete S&C schematic	For no support S&C
30	11/29	31,32	Delete USB3.0 Host schematic	For no support external USB3.0 host IC
31	11/30	38	change R409 from 120K_1% to 120K_5%	For change tolerance
32	11/30	33	change RA17 from 0.1% to 0.5%	For change tolerance
33	11/30	13	Delete R260 and short directly	For reduce circuit
34	12/01	16	change DH1 from @ to NOGCLK@	For BOM control
35	12/01	37	Add SW4	For Debug
36	12/01	36	Delete U21, C453, C452	For LID on small board
37	12/02	35	Delete CPSETIN	For delete EC930 schematic
38	12/02	16	Add JRTC, CH9, DH8, DH9, R227	For non-rechargeable RTC schematic
39	12/02	36	Delete JBLG schematic	For non-keyboard led schematic
40	12/05	36	Modify JKB pin define	For meet SS KB Matrix
41	12/05	13	Change location from J17 to JLVDS1	For location naming
42	12/06	35	Delete UB1.85 SM_SENSE#	For no support S&M
43	12/06	25	Modify JUSIO pin define	For small board connect
44	12/06	38	Delete R425 and 0.75V_R_EN#	For Power circuit connect
45	12/07	25	Add JODDB	For 15" ODD connector
46	12/07	15	Change U9.5 connect from +5VS to +HDMI_5V_OUT	For prevent leakage issue
47	12/08	29	Change JCRI0 pin define	For small board connect
48	12/12	21	Change UH1.K1 and RH180.2 from BT_ON# to PCH_GPIO34	For common GPIO pins on EC side
49	12/12	35	UB1.18 and RB11 connect to BT_ON#	For common GPIO pins on EC side
50	12/12	25,35,37	Delete PWR_ON_LED# net	For common GPIO pins on EC side
51	12/12	25	Change JUSIO pin define	For LED behavior
52	12/12	16	Delete CH9, DH8, DH9, R277, JRTC	For RTC change to rechargeable
53	12/13	21	Delete Q51 and change PCH_WL_BT_LED to PCH_GPIO69	For change WL_BT_LED# to EC GPIO
54	12/13	35	UB1.21 connect WL_BT_LED#	For change WL_BT_LED# to EC GPIO
55	12/13	37	Change Q156B.3 from WL_BT_LED# to WIMAX_LED# and connect to R802	For WLAN LED behavior
56	12/13	35	Delete UB1.127 (USB_OC#0) and UB1.17 (USB_OC#1)	For no support USB S&C
57	12/13	20,29	Add TPM schematic	For TPM function
58	12/13	27	Delete Q36	For change BT_ON# to EC GPIO
59	12/13	14,30,37	Change JCRT, JUSBA, JUSBB, JTP symbol	For connector list update
60	12/13	25,29	Change JUSIO, JCRI0 symbol	For connector list update
61	12/14	27	Change UCL1 to SLG3NB244VTR	For green clock
62	12/14	29	Change UT1.5 and RT7.1 net from +3VALW to +3VALW_PCH	For ErP Lot6 function
63	12/14	21	Add RH181 and connect ISDBT_DET, delete RH297	For no support TV tuner
64	12/14	21	Change RH194 from 100K 5% to 10K 5%	For update resistor value
65	12/14	21	Change RH315.2 connect +3VS and BOM structure to mount	For update resistor value
66	12/14	37	Change ZZZ P/N to DA60000T600	For update PCB P/N
67	12/14	37	Move D89 to TP small board	For Move to TP small board
68	12/15	16~24	Change UH1 P/N to SA00005FH30	For update UH1 P/N
69	12/15	30	Change CR40 P/N to SF000002Y00	For layout limitation
70	12/15	33	Delete RA53	For common design
71	12/15	25	Delete C381~4	For placement update
72	12/15	30	Delete RR23~24, CR26, RR36~37, CR29	For connect GND directly
73	12/15	9	Delete CC67	For not reserve
74	12/19	16	Delete T67~T69	For not reserve
75	12/19	29	Change YT1 form SJ132P7KW10 to SJ100004Z00 (small package)	For change to small size
76	12/19	29	Change CT2, CT3, CT4, CT5 from SE095104K80 to SE102104K00	For BOM reduce
77	12/19	29	Change JCRI0 to SP010015H00	For follow connector list
78	12/20	13	Delete JLVDS.28 (+LCD_INV)	For prevent issue
79	12/20	37	Modify H1~H17	For Update screw hole

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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title
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# HW PIR (Product Improve Record)

QCLA4.5 LA-8862P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.0 TO 0.1

GERBER-OUT DATE: 2011/12/30

NO DATE PAGE MODIFICATION LIST

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
80	12/20	35	Change UB1.68 (PCH_PWR_EN) to UB1.107	For EC common
81	12/20	35	Change UB1.73 (UMA_ENBKL) to UB1.76	For Update screw hole
82	12/20	21	Change RH198 from 100k to 10k	For follow Intel checklist
83	12/20	05	Change UC1.5 from +3VALW to +3VALW_PCH	For design change
84	12/20	16	Modify SATA_LED# to10k (RH29) +5VS pull high & 20k (RH35) pull low	For design change
85	12/20	17	Change CLKREQ_CR#,CLKREQ_USBA30#,CLKREQ_USB30# to PCH_GPIO25, 26, 44	For design change
86	12/20	20,23	Change CH104 to 100p and CH71 to 0402	For design change
87	12/20	27,35	Change BT_ON# netname to BT_ON and UA4 to UM4	For design change
88	12/20	27	Modify LED_WIMAX# to 100k +5VS pull high & 200k pull low	For design change
89	12/20	35	Delete CB13	For design change
90	12/20	33	Change CA3,CA46,CA36 to 0805_6.3V6M	For cost down
91	12/20	38	Delete R5534 and short directly	For design change
92	12/20	37	Changr R819 from +5VS to +3VS	For design change
93	12/20	5,25	Changr C13,C17,C356,C355,C354 to 0805_6.3V6M and unmount C354	For cost down
94	12/20	35	Delete UB2,CB17,RB25 and connect UB1.127 to PM_SLP_S4#, UB1.14 to PM_SLP_S5#	For cost down
95	12/20	35	Delete RB24,RE28,RA4,RE5,RE7,R37 and change UB1.119,117,75,64,27,16 to NC	For cost down
96	12/21	28	Change symbol from SP021105131	For apply symbol
97	12/21	35	Change TP_CLK,TP_DATA pull high to +5VS	For TP spec
98	12/21	13	Unmount D84	For reserve
99	12/22	15,25,30	Swap L9,L11,LR1,LR2,L53,L54 signal	For swap signal
100	12/22	30	Swap U3TXDP1_R_L and U3TXDN1_R_L swap U3RXDP1_R_L and U3RXDN1_R_L	For swap signal
101	12/23	14,15	Change F1,F2 to SP040003A00	For component common
102	12/24	29	Change RR66~67 to mount, LR9 to unmount	For choke reserved
103	12/24	37	Cancel H6, H17 (FAN stand-off) and change H4 to H_3P3 (VGA)	For ME drawing update
104	12/24	28	Change PJ29 from JUMP_43X118 to JUMP_43X39	For layout concern
105	12/24	38	Delete R105, add PJ30 to contact +3VS & +3V_WLAN	For no support AOAC function
106	12/26	36	Update JDB symbol and modify pin define	For connector list update and pin define for customer's request
107	12/26	13,17	Delete RH282, change RH116 to mount, JLVDS1.2 contact LVDS_SEL	For update pin define and BOM reduce
108	12/26	13	JLVDS1.1&11&12 contact GND	For LVDS cable smooth route and BOM reduce
109	12/26	33	Move RA32 & RA33 to Audio/B	For AMIC function
110	12/26	29	JCRIO.11 contact SENSE_A, JCRIO.12 contact INT_MIC	For AMIC function
111	12/26	36	Swap JKB connector pin define	For latest keyboard spec
112	12/26	29	Swap LR9 pin define	For layout concern
113	12/27	29	Swap JCRIO pin define	For layout concern
114	12/27	37	Update JTP pin define	For PIN define rule
115	12/27	29	Update TPM schematic	For co-lay SLB9635 and SLB9655
116	12/27	28	Add CL35 and un-mount	For EMI request
117	12/27	21	Change CIR_EN# to PCH_GPIO39 and ISDBT_DET to PCH_GPIO48	For schematic update
118	12/27	21	Change HDD2_DET# to PCH_GPIO57 and LNB_EN to PCH_GPIO70	For schematic update
119	12/27	21	Change 3D_DET# to PCH_GPIO71	For schematic update
120	12/27	20,30,35	Add S&C schematic	For reserve S&C schematic
121	12/27	33	Add Analog MIC schematic	For Analog MIC
122	12/27	28	Change RL8.2 from LAN_X1 to LAN_X2	For vendor recommendation
123	12/27	11,21	Add D54,RH210,RH100,QC9 and delete RC117,RC118	For Ivy/Sandy bridge M1/M3 co-lay solution
124	12/27	11	Change QC7,QC8 to always mount	For Ivy/Sandy bridge M1/M3 co-lay solution
125	12/27	38	Change R158 from 100Kohm to 220Kohm	For intel S3 power reduce sequence between +1.5VS_CPU and +0.75VS
126	12/27	33	Add CA64 0402 cap @ on SENSE_A	For audio sense A pin
127	12/28	30	Change R569 to PJ31	For S&C function
128	12/28	30	Add RH4,CH80	For prevent abnormal turn on
129	12/28	30	Add CH99,CH102 and delete CH97	For prevent abnormal turn on and do soft start
130	12/29	38	Change R5545 from 100k to 10k	For prevent abnormal turn on and do soft start
131	01/03	28	Change UL3,UL4 from SP050006N00 to SP050005Z00	For update transformer P/N
132	01/03	29	change UT1 P/N from SA00000GG40 to SA00000GG60.	For TPM firmware update
133	01/03	27	change R1456,R1457,C907,C908,Q210 to @	For TPM firmware update

QCLA4.5 LA-8862P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2012/01/10

NO DATE PAGE MODIFICATION LIST

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	02/01	28	Add PJ32 and connect +3VALW_PCH & +3V_LAN	For power saving
2	02/02	29	Change JCRIO.2 to connect MIC_SENSE and JCRIO.1 to connect NBA_PLUG	For change pin define
3	02/02	33	Delete sense_A off page,CA64 and add RA32,RA33	For sense A circuit
4	02/02	37	Change JTP from SP010015H00 to SP01001BF10	For connector list
5	02/02	33	Add JMIC connector SP02000R000	For connector list
6	02/02	27	Change JWLAN from SP07000FP00 to SP07000TB00	For connector list
7	02/02	38	Change Q44A to Q6B and delete Q44	For component reduce
8	02/02	16	Delete T67-69	For common design
9	02/03	35	UB1.38 connect AOAC_WLAN_PWR_EN# and UB1.91 connect WLAN_RST#	For WLAN Power on/off and WLAN reset
10	02/03	27	Change R1456,R1457,C907,C908,Q210 to mount	For WLAN Power on/off and WLAN reset
11	02/03	27	change R1457.1 to connect AOAC_WLAN_PWR_EN#	For WLAN Power on/off and WLAN reset
12	02/03	27	Change JWLAN.22 to connect WLAN_RST#_R	For WLAN Power on/off and WLAN reset
13	02/03	27	Change C260,CM7,CM8,CM9,C254 to connect +1.5VS_WLAN	For WLAN Power on/off and WLAN reset
14	02/03	27	ADD PJ33 (PJ33 don't short),UM5,RM19,RM21 and +1.5VS_WLAN (power)	For WLAN Power on/off and WLAN reset
15	02/03	27	Change UM4.1 to connect AOAC_WLAN_PWR_EN#	For WLAN Power on/off and WLAN reset
16	02/06	28	Change CL63 from SE120102K80 to SE120102K90	For sourcer suggestion
17	02/06	37	Change H18,H19 to H_3P0N	For ME drawing update
18	02/08	21	Change UH1.T7 from HDMI_HPD to CHP3_SERDBG	For Eureka Serial POST GPIO
19	02/08	21	Change RH292 from 10Kohm to 1Kohm and delete T66	For Eureka Serial POST GPIO
20	02/08	21	Change UH1.T7 from HDMI_HPD to CHP3_SERDBG and connect to JCRT.4	For Eureka Serial POST GPIO

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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title
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				QCLA4.5 LA-8862P M/B
				Date: Thursday, February 16, 2012
				Sheet 47 of 48

QCLA4,5 LA-8862P SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1 TO 0.2  
 GERBER-OUT DATE: 2012/01/10

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
21	02/08	27	Add TL1 test point	For LAN FAE suggestion
22	02/09	15	Add D94-D96 on HDMI signal	For ESD request
23	02/09	27	Add D99,D100 on LAN signal	For ESD request
24	02/09	14	DEL D3-D5 and add D97,D98 on CRT signal	For ESD request
25	02/09	7,31	Add RC74 and net DRAMRST_CNTRL_EC connect RC74.1 & UB1.89	For DS3 function reserve
26	02/09	25	Add R79~82	For reduce SATA signals reflection
27	02/14	11	Change CD7 from SF000002000 (H=5.9) to SF000002Z00 (H=4.4)	For thermal issue

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title
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Date	Thursday, February 16, 2012		Sheet	48 of 48