

Model : X72IA6

Intel Yonah CPU + 945PM / ICH7-M Chipset

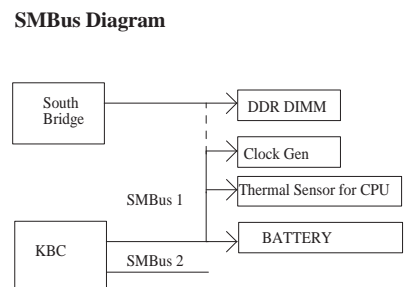
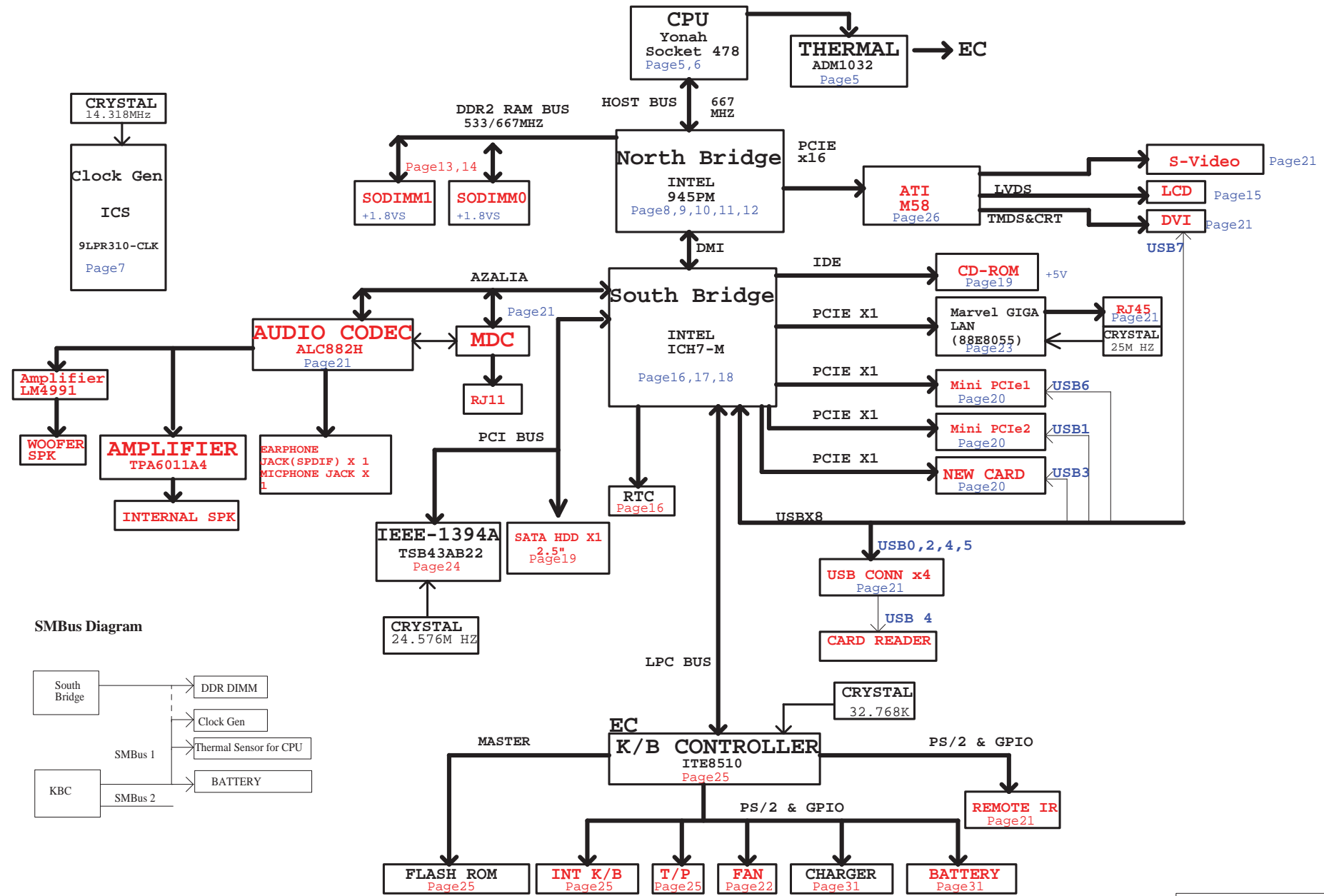
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PG06 CPU YONAH-2/2
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PG22 Audio PWR/FAN CTL
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PG25 EC IT8510E/BIOS/TP CON
PG26 VGA MXM CON
PG27 CPU CORE
PG28 1.05V/1.5V/1.8V/2.5V/0.9V
PG29 +3.3VA/+5VA/+12VA
PG30 VCC SW/+1.05VS/+1.5VS
PG31 BATT IN/Charger
PG32 Appendix A.Ver.History

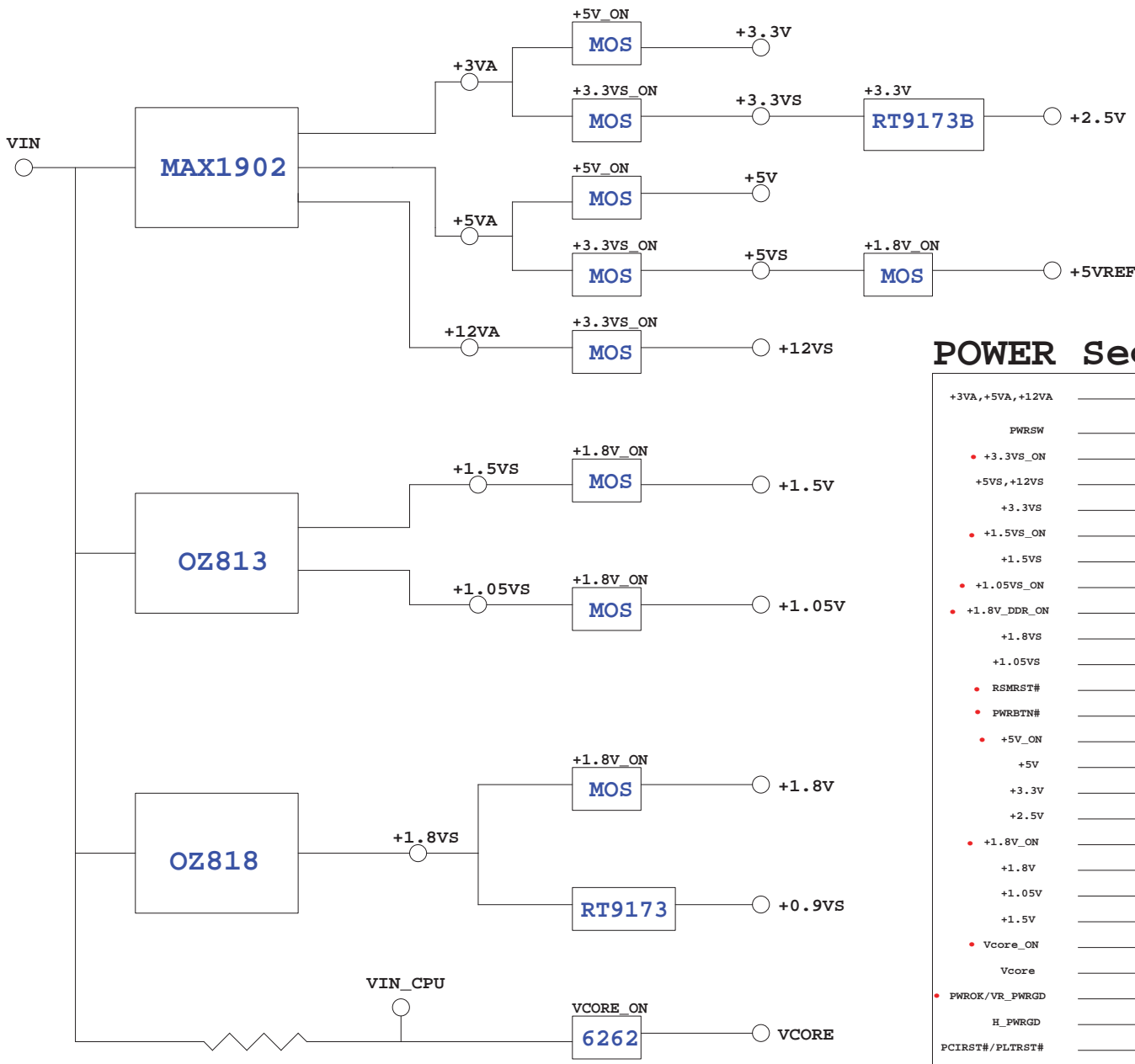
Revision History	
A	ORIGINAL RELEASE
B	

UNIWILL COMPUTER (SIP) Co.,LTD			
Title			
X72IA6			
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	SCHMATIC1	B	
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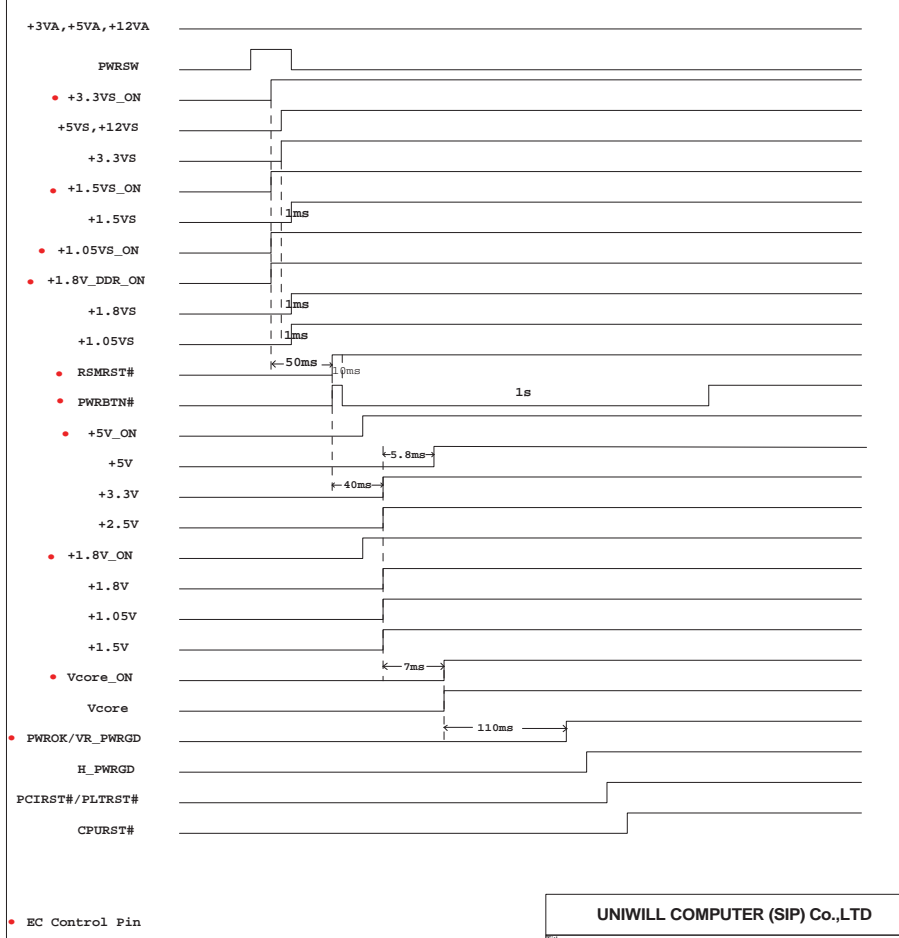
X72IA6 SYSTEM BLOCK DIAGRAM



POWER BLOCK DIAGRAM



POWER Sequence



ICH7-M GPIO	
GPIO0	BM_BUSY#
GPIO9	EC_EXTSMI#
GPIO11	SMB_ALERT#
GPIO12	PNLSW0
GPIO13	PNLSW1
GPIO14	PNLSW2
GPIO16	PM DPRSLPVR
GPIO18	PM_STPPCI#
GPIO20	PM_STPCPU#
GPIO49	H_PWRGD

ITE8510E GPIO	
GPCF0	RF_SW#
GPCF1	SILENT#
GPCF2	IR_PS2CLK1
GPCF3	IR_PS2DAT1
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	KEY_16
GPCF7	KEY_17
GPI0	SCROLL_LED#
GPI1	CAPS_LED#
GPI2	NUM_LED#
GPI3	CHG_R_LED#
GPI4	CHG_G_LED#
GPI5	SUSLED_LED#
GPI6	IR_MAXVOLUME
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GPG4	TP_DISABLE
GPG5	LCDSW
GPG6	MUTE#
GPG7	EXTTS#0
GPB0	ROM_WE_DIS
GPB1	NA
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	NA
GPE1	EC_CPU_BSEL1
GPE2	NA
GPE3	NA
GPE4	PWRSW
GPE5	LID#
GPE6	PCM#
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	REMOTE_ON#
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	PM_SLP_S4#
GPD5	PM_THROTTLING#
GPD6	FAN_SPD#
GPD7	NA
GPA0	BTL_BEEP
GPA1	NA
GPA2	NA
GPA3	NA
GPA4	NA
GPA5	SMP1_EN#
GPA6	MALL#
GPA7	PWRBTN#

ITE8510E GPIO	
GPC0	PWROK
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	SB_ALERT#1/EC_171
GPC4	SB_ALERT#2/BROWSER#
GPC5	TP_LED#
GPC6	CHG_ON
GPC7	SILENT_LED#
ADC0	BAT_TEMP
ADC1	ADAPTOR_I
ADC2	DDR2_TEMP
ADC3	VGA_TEMP
DAC0	BRIGHTADJ
DAC1	CHG_I
DAC2	FAN_CTRL0
DAC3	NA

CPU				
CPU CORE (V)	ICC (mA)	W	TEMP (°C)	
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

MCHE			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
-VCC_SWITCH_D08E	266	0.452	

ICH6-M			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

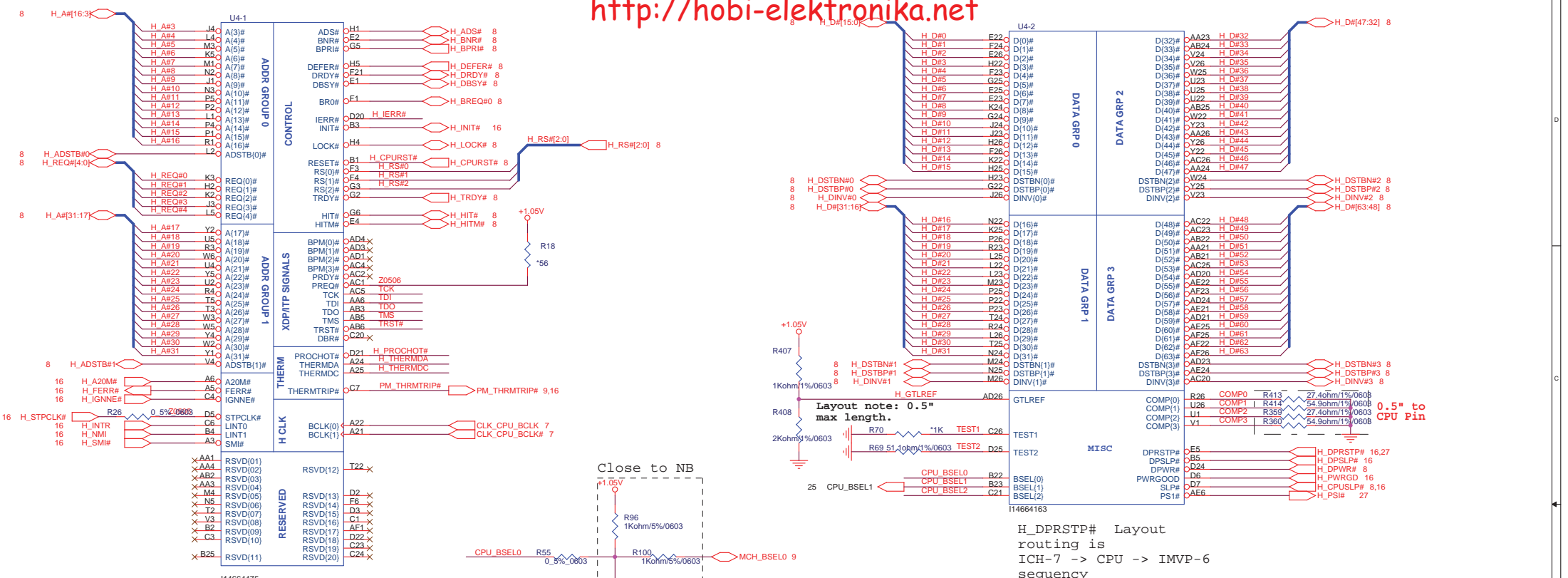
ITE8510E			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	300	1	70

CLOCK GENERATOR			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	180	0.594	70

ALC880			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V(DVDD)	71	0.234	70

TPA6011A4			
VCC	ICC (mA)	W	TEMP (°C)
3.3V	30	0.099W	85

ADM1032			
VCC	ICC	W	TEMP (°C)
+3.3V	170uA	0.56mW	150



I14664475

H_DPRSTP# Layout routing is ICH-7 -> CPU -> IMVP-6 sequency

	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	133
PSB667	0	1	1	166

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Title: **X721A6**

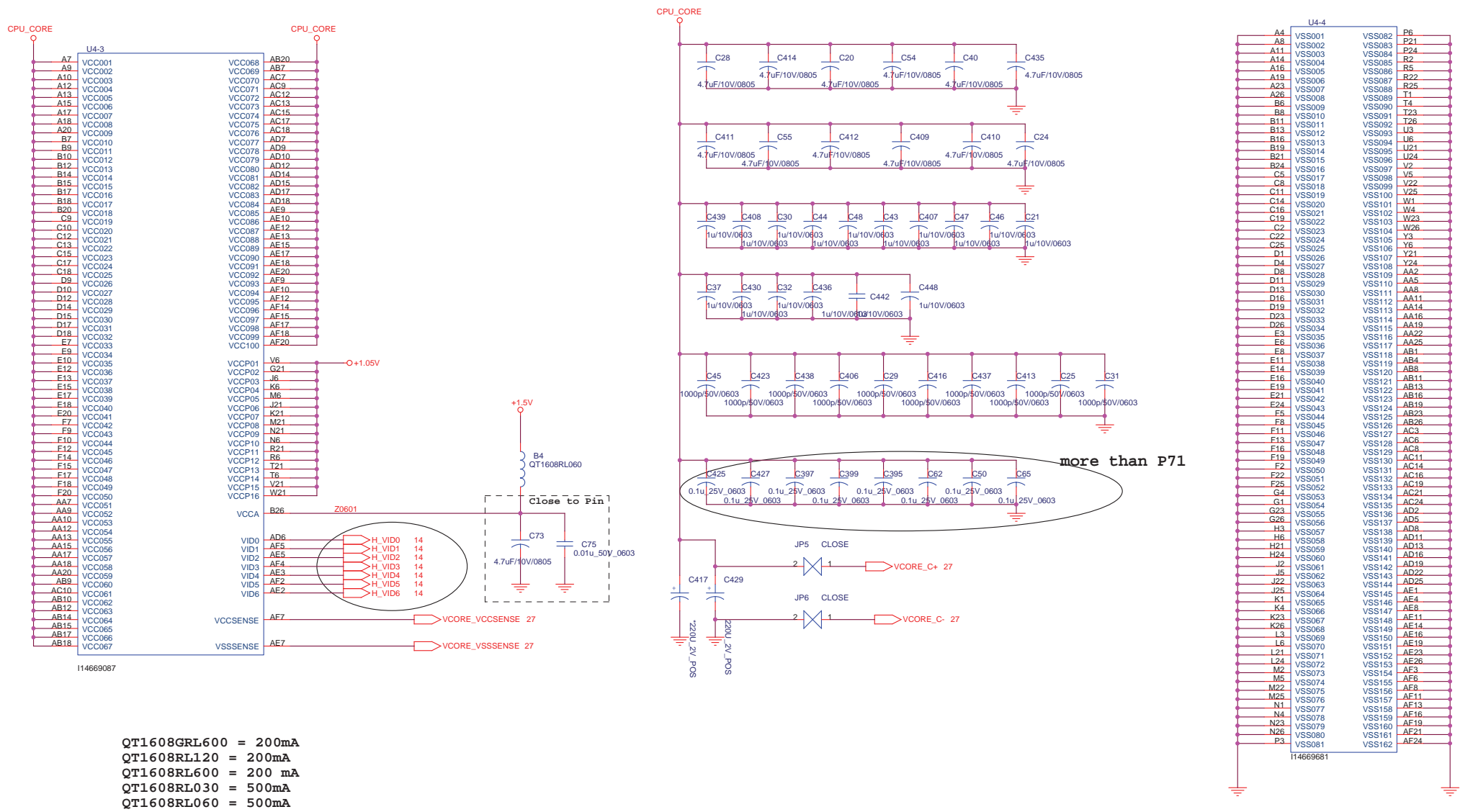
Document Number: **CPU YONAH-1/2**

Schematic: **CPU YONAH-1/2**

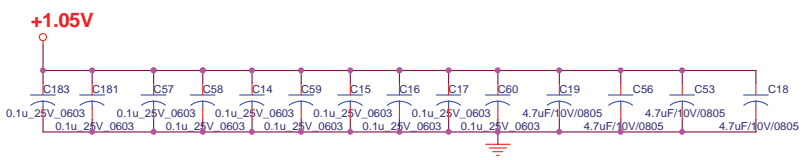
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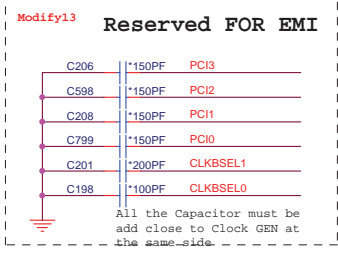
Rev B



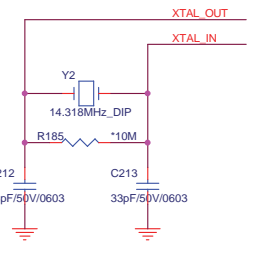
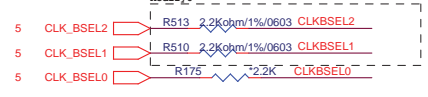
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Title	X721A6	
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more than P71

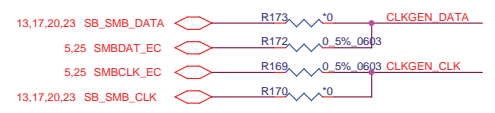


Bsel [0,2]
 Vil = 0.3
 Vih = 0.7



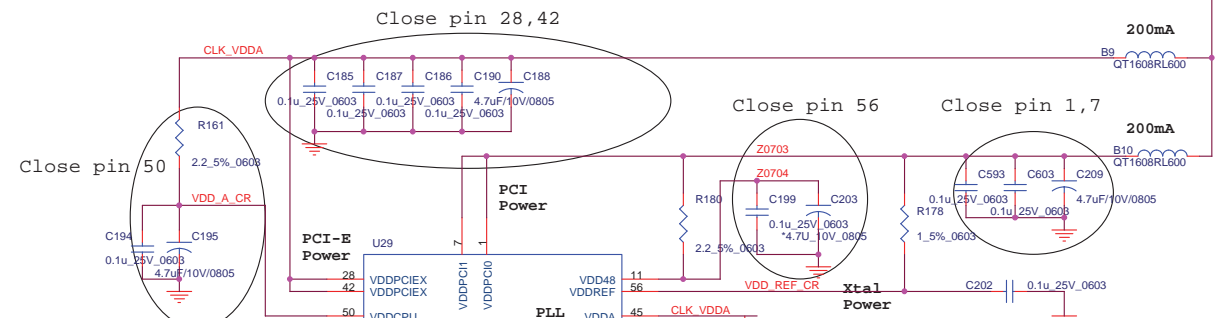
$$C_e = 2 * C_L - (C_s + C_i)$$

CL = Crystal Load Cap = 20P
 Ci = IC internal Cap = 5P
 Cs = 2P
 Ce = Crystal external Cap = 33P

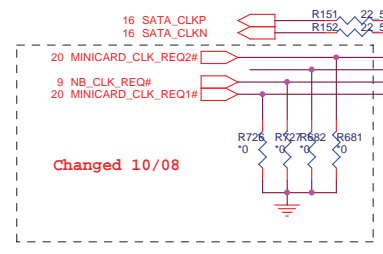


	FS4	FS3	BSEL2 FSLC	BSEL1 FSL1	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ	SPREAD %
PSB533	0	0	0	0	1	133			
PSB667	0	0	0	1	1	166	33	100	0.5% DOWN
PSB533	0	1	0	0	1	133			+/- 0.25%
PSB667	0	1	0	1	1	166	33	100	CENTER

FS3 , FS 4 SEETING BY I2C BUS



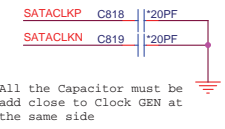
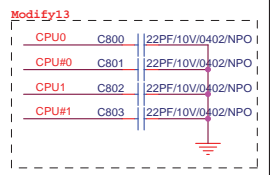
SELDOT , 1= Pin 14/15 DOT 96MHZ , Pin 17/18 LCDCLK
 0= Pin 14/15 27MHZ Fix/SS Pin 17/18 PCIEIX



PCI-Express

	Reserve	MCH	N_Card	ICH7-M	VGA	LAN	Mini_C1	Mini_C2	Reserve
	0	1	2	3	4	5	6	7	8
PEREQ1#	V						V		
PEREQ2#		V							V
PEREQ3#			V		V				
PEREQ4#				V		V		V	

GCLK => PCI-E & DMI (100MHZ)
 DREFCLK => Display PLLA (nun- ss 96MHZ)
 DRESSFCLK => Display LVDS PLLB (ss 100MHZ)



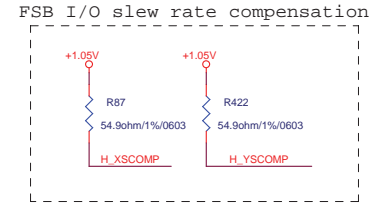
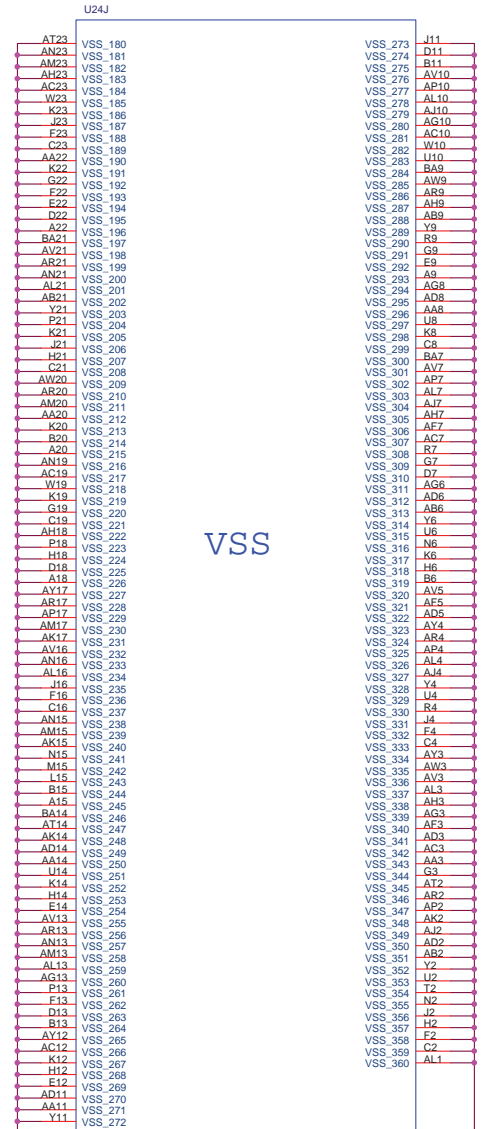
All the Capacitor must be add close to Clock GEN at the same side

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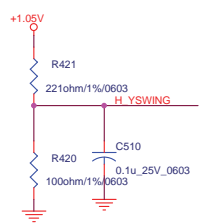
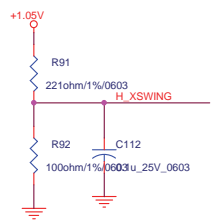
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Size: Document Number: **CLOCK GEN ICS9LPR310**

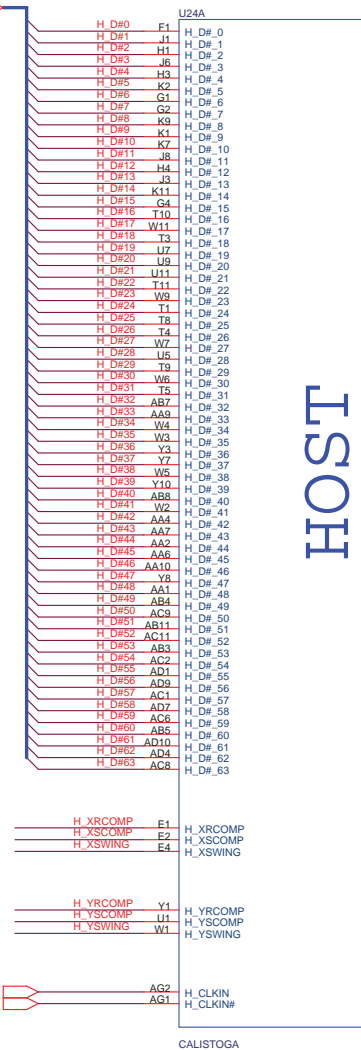
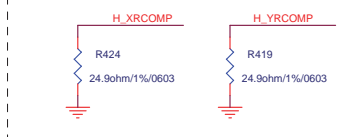
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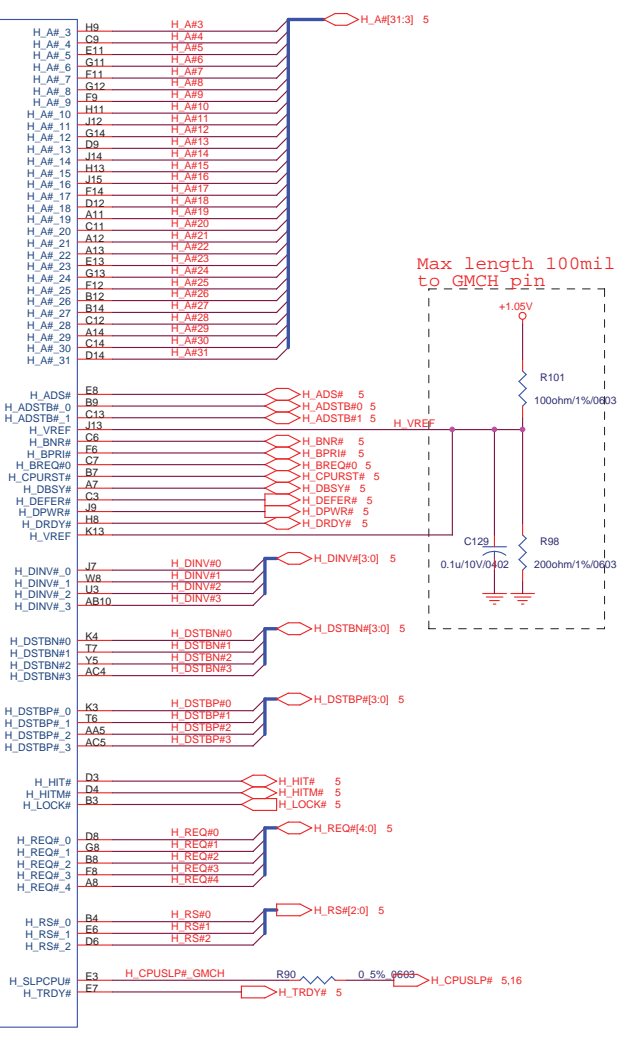
Reference Voltage for RCOMP
10mil trace 20mil spacing



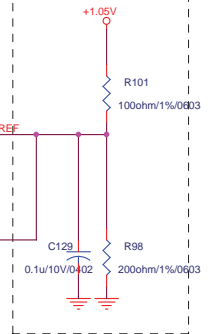
Calibration FSB I/O Buffer
10mil trace 20mil spacing



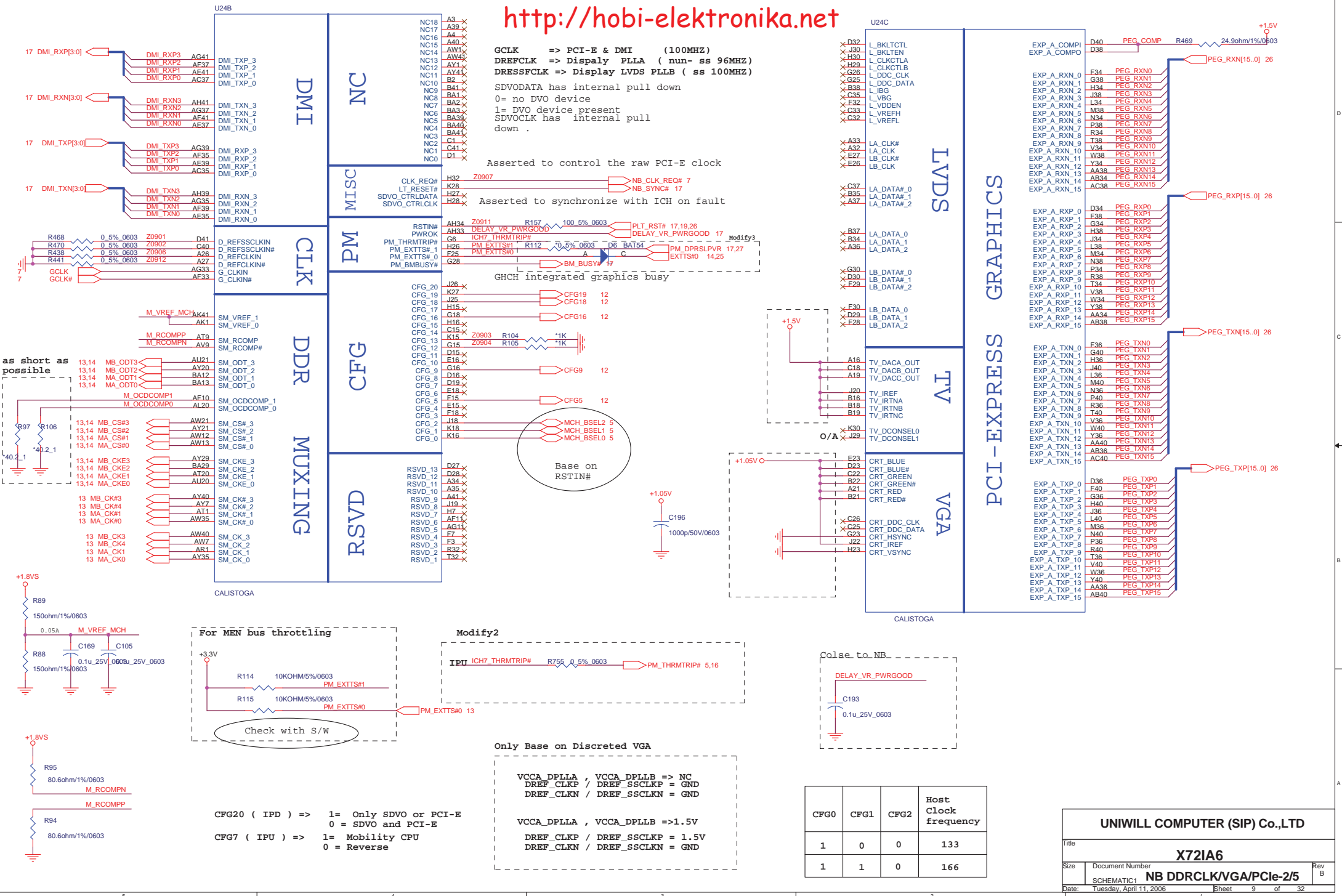
HOST



Max length 100mil
to GMCH pin



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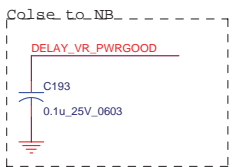
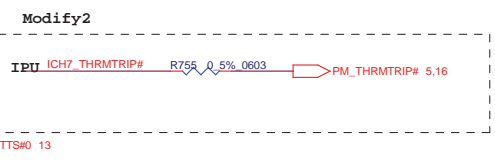
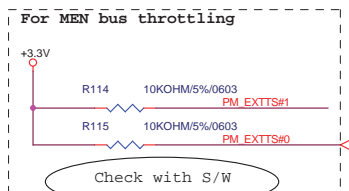
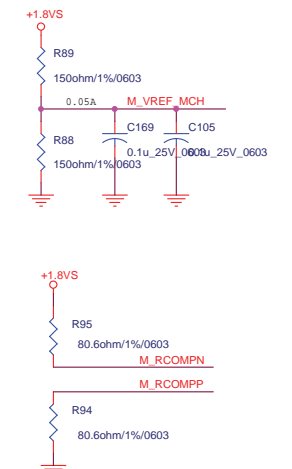
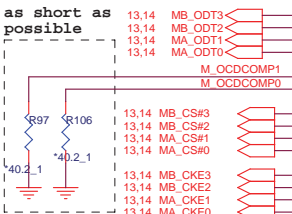
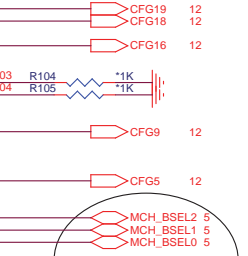
GCLK => PCI-E & DMI (100MHZ)
 DREFCLK => Display PLLA (nun-ss 96MHZ)
 DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

SDVODATA has internal pull down
 0= no DVO device
 1= DVO device present
 SDVOCLK has internal pull down

Asserted to control the raw PCI-E clock

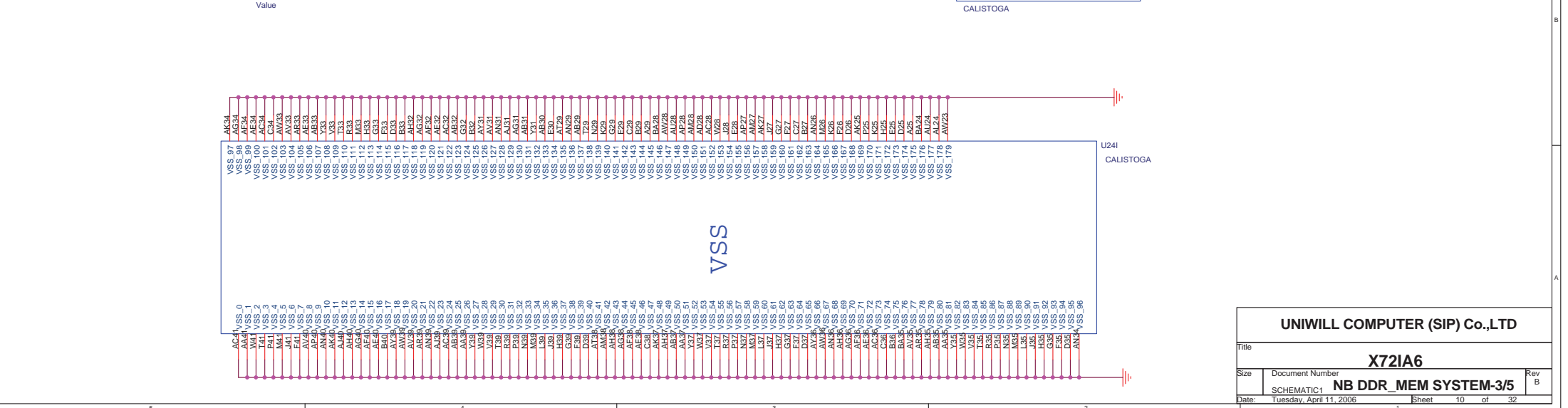
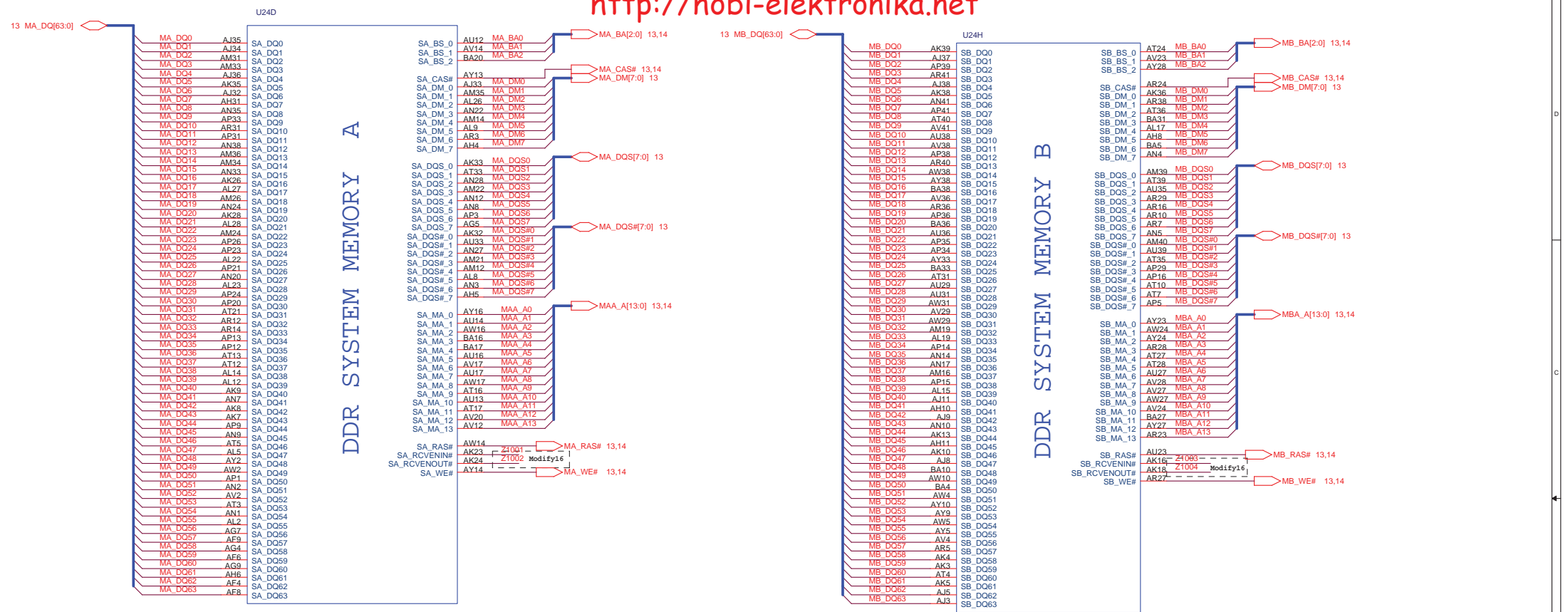
Asserted to synchronize with ICH on fault

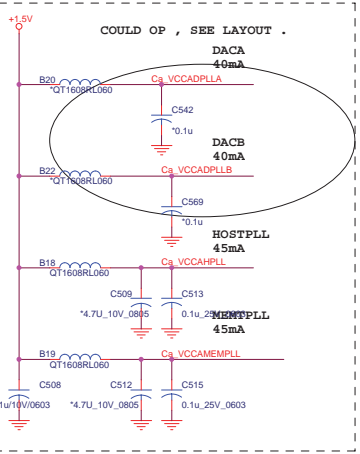
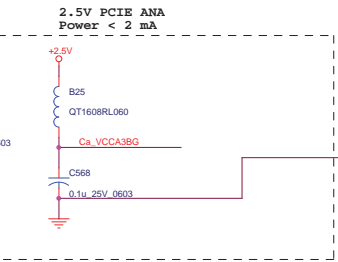
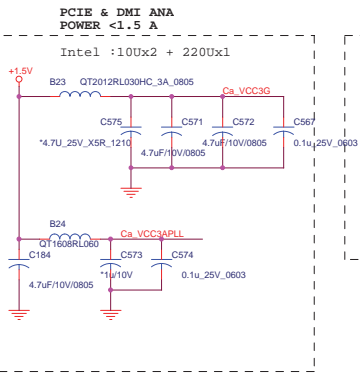
GHCH integrated graphics busy



Only Base on Discreted VGA

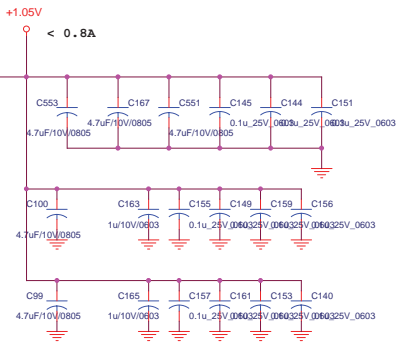
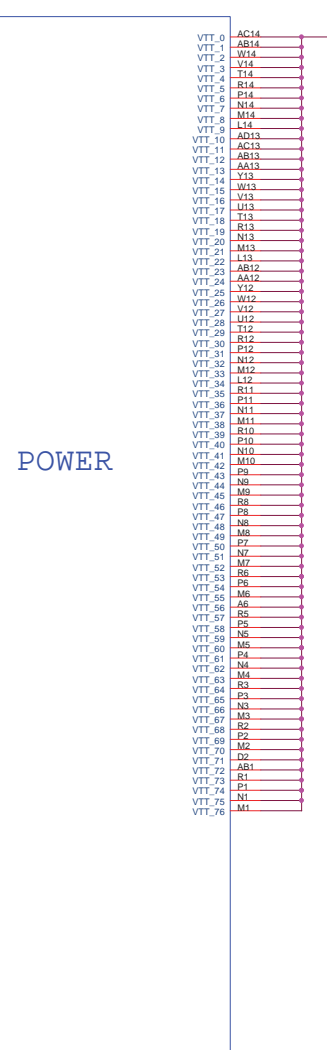
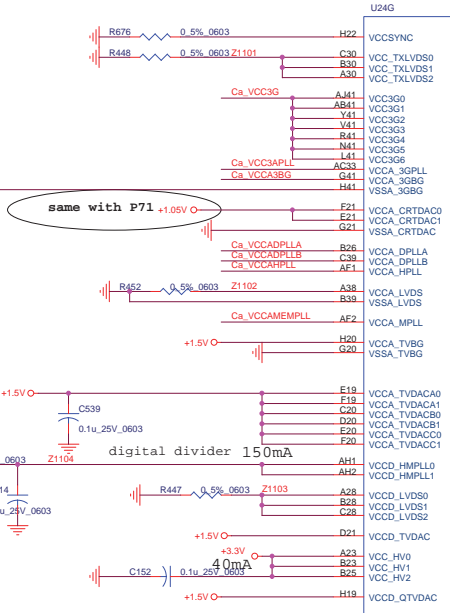
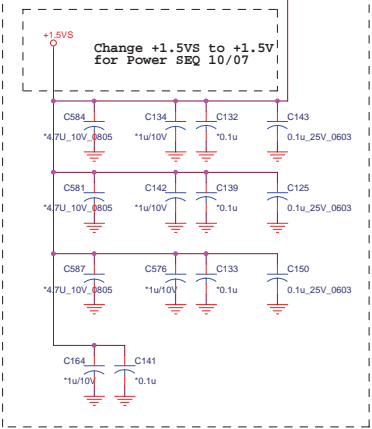
CFG0	CFG1	CFG2	Host Clock frequency
1	0	0	133
1	1	0	166



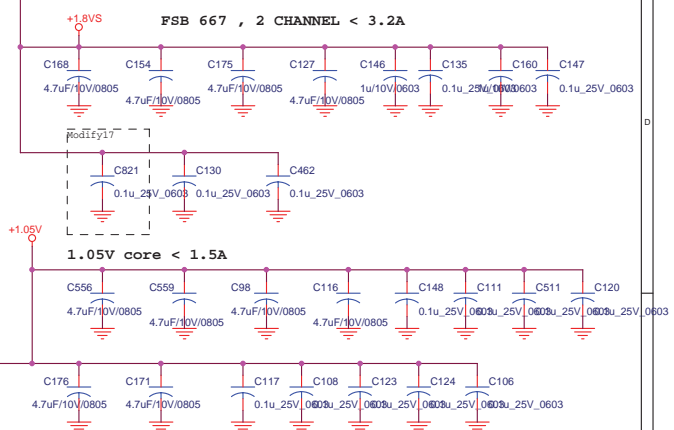
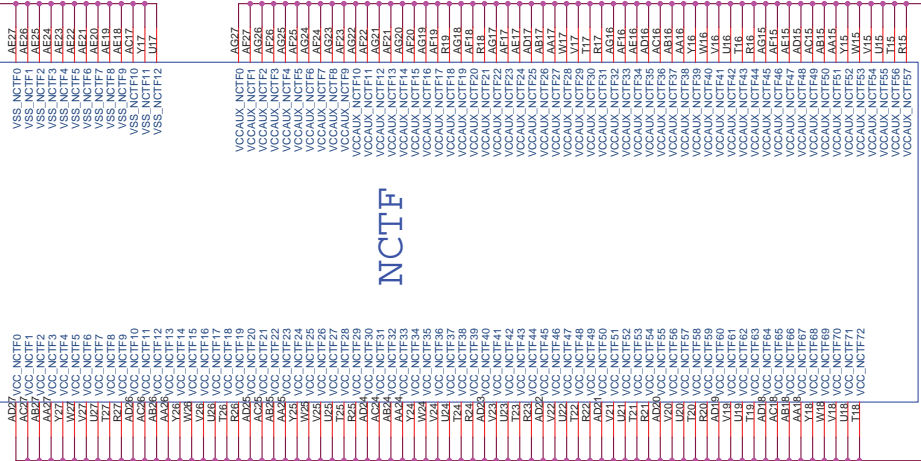
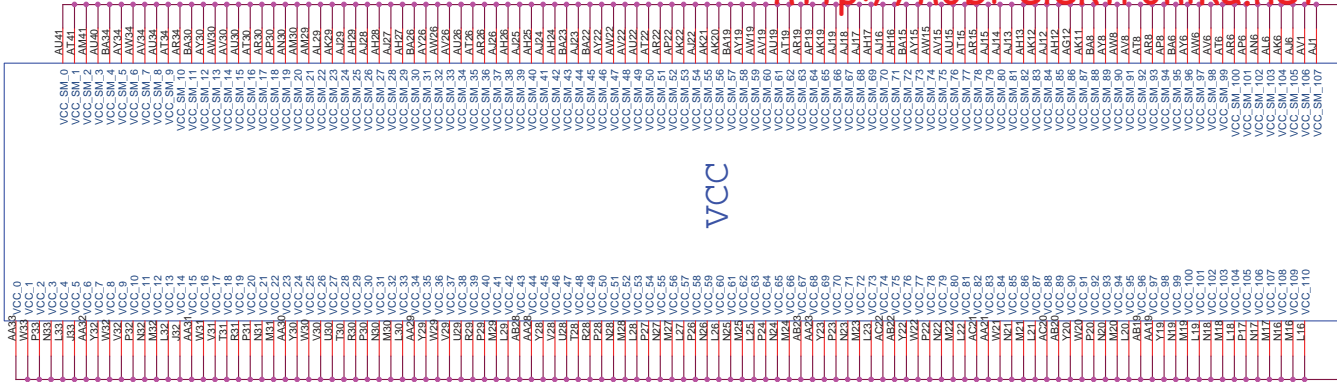


For DDR DLL , DDR IO ,
FSB IO < 1.9A

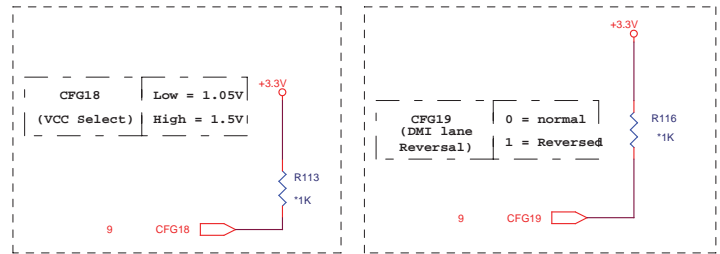
Filter component only need when
GMCH core is 1.5V for extended
graphics performance .



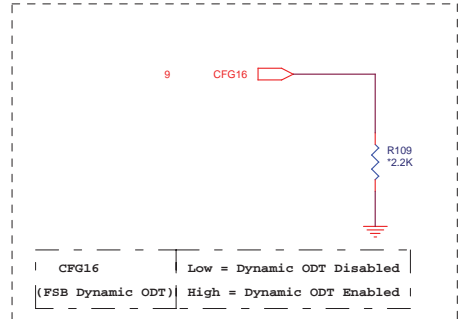
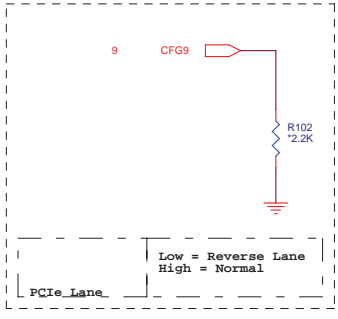
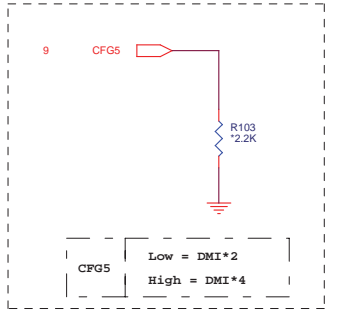
- NB 1.05V layout < 2.5A
- NB 1.5VS layout < 1.9A
- NB 1.5V layout < 1.8A
- NB 2.5V layout < 0.1A
- NB 3.3V layout < 0.1A
- NB 1.8VS layout < 3.2A



Change +1.5VS to +1.5V for Power SEQ 10/07

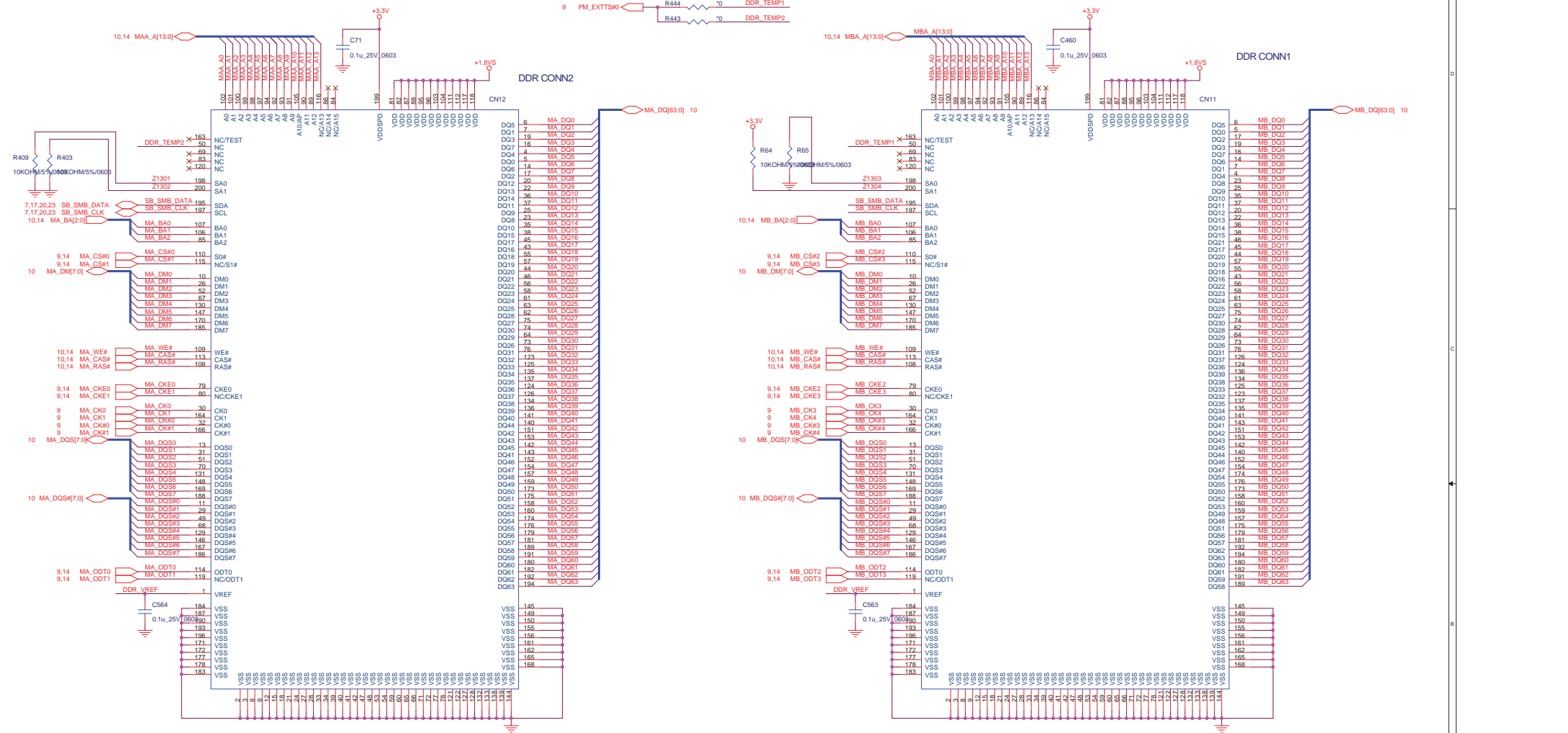


CFG[20:18] have internal pulldown resistors.

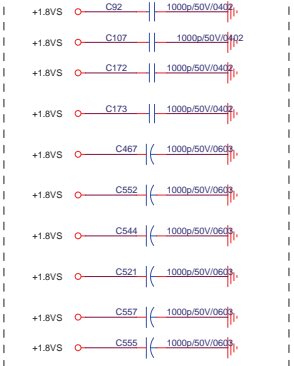


CFG[17:3] have internal pullup resistors.

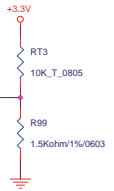
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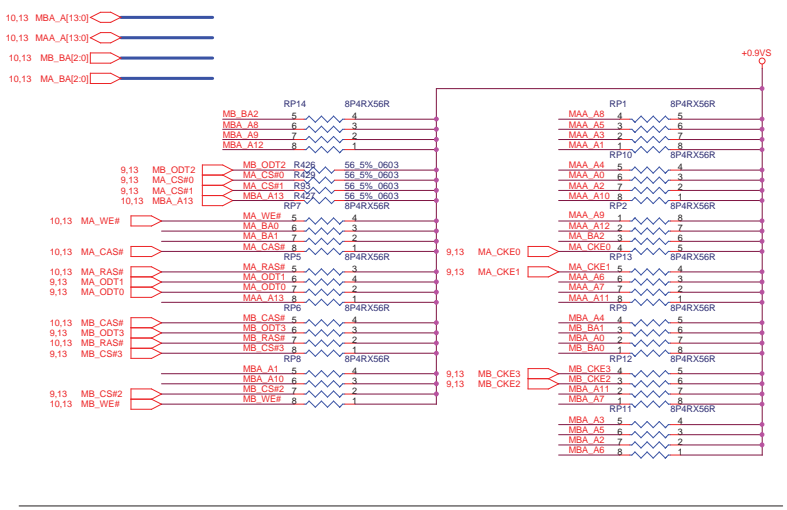
For current return path



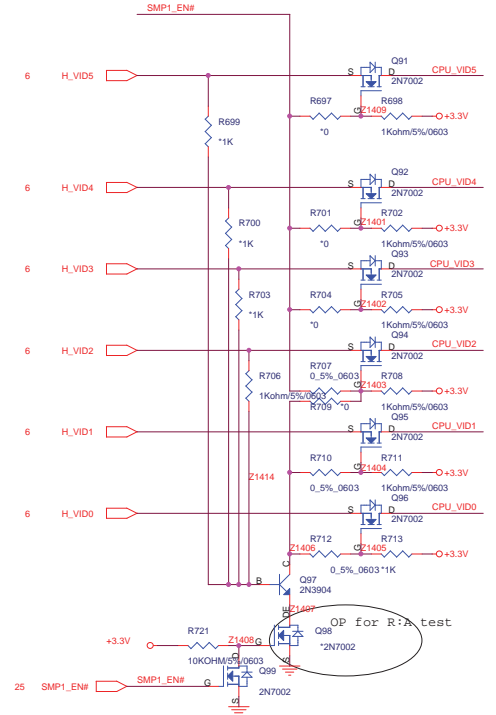
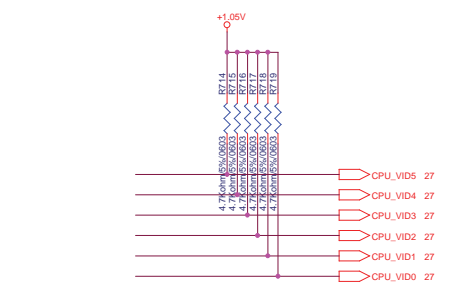
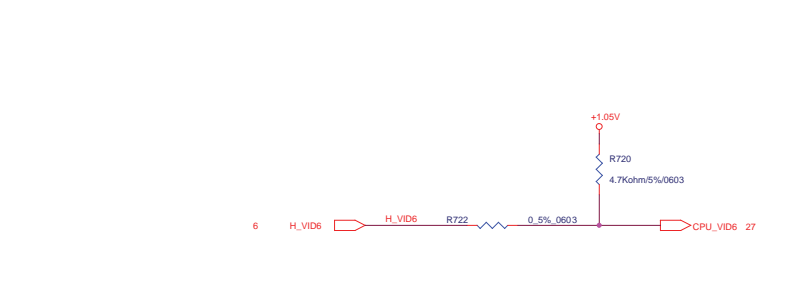
Thermistor



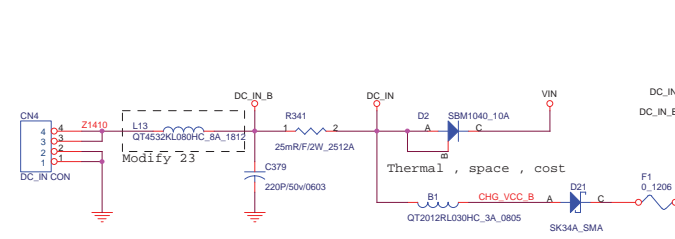
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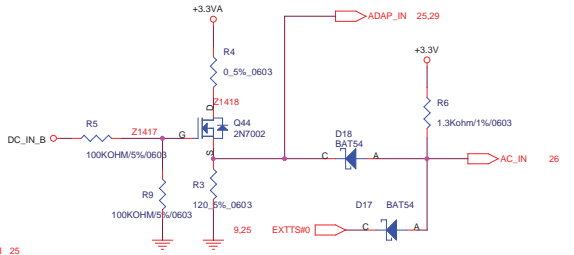
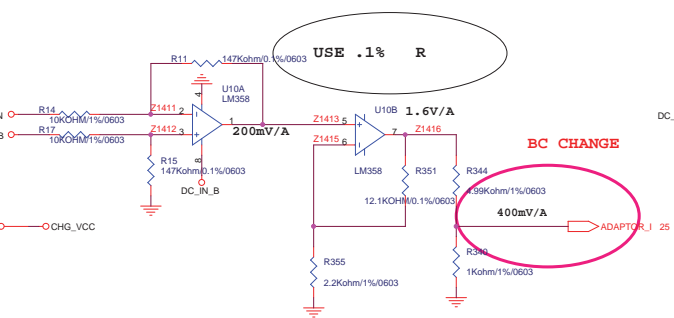
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0	0	0	0	0	1	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	1	0		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	1	0		
0	0	1	1	0	1	0		

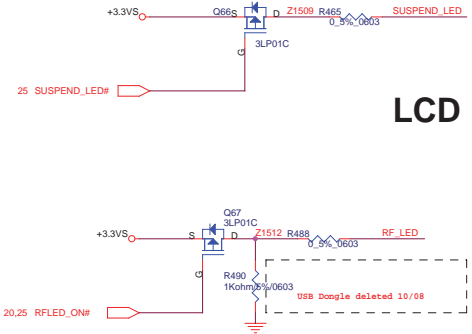
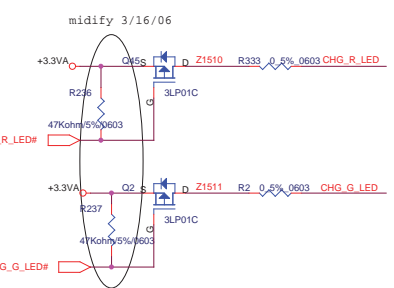
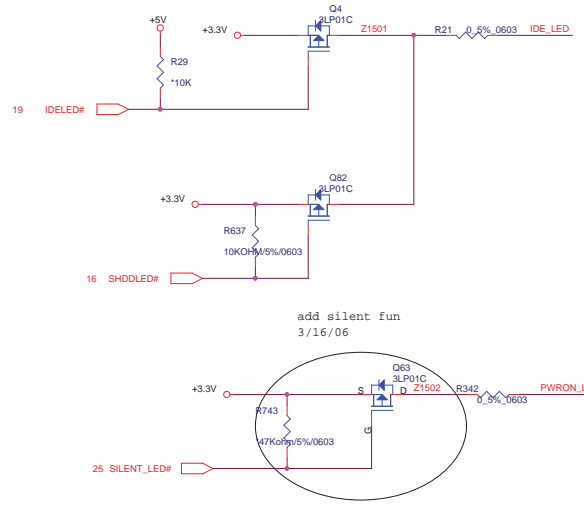
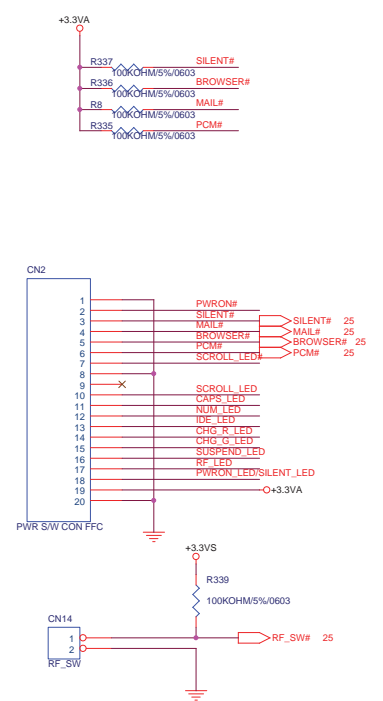


DC IN



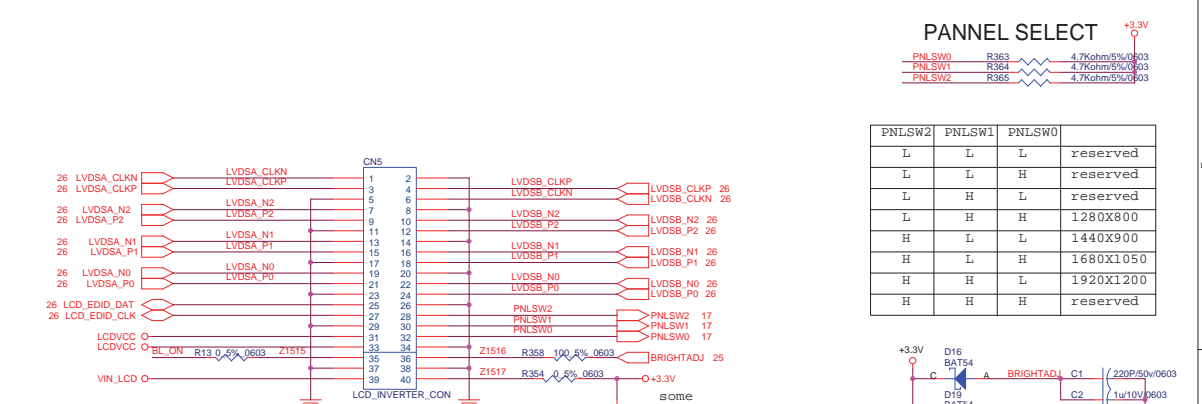
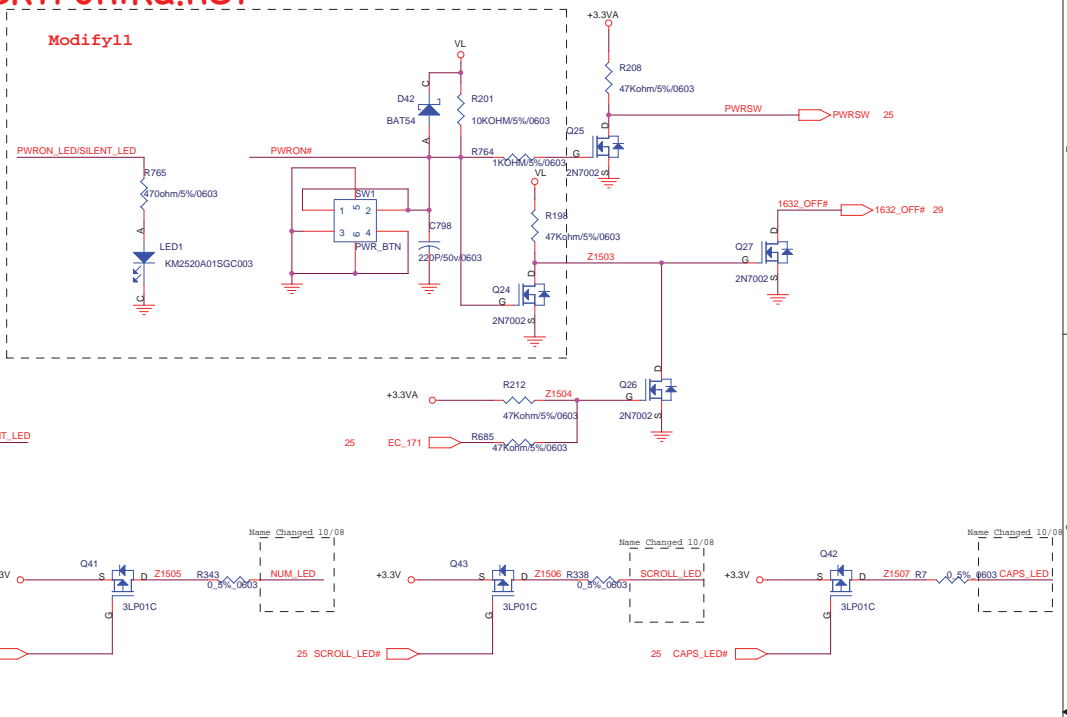
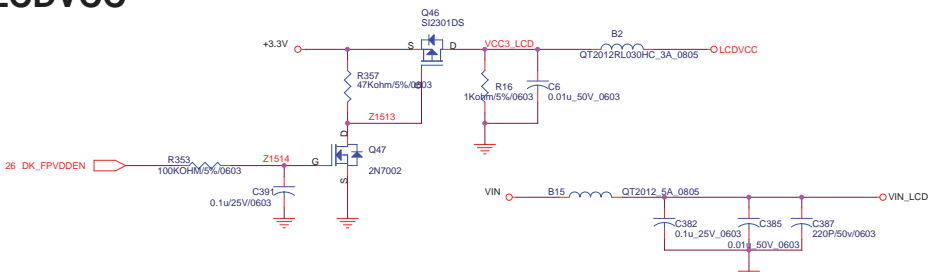
TOTAL POWER



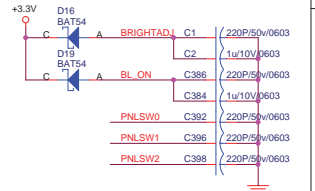
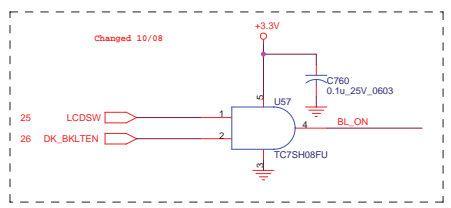


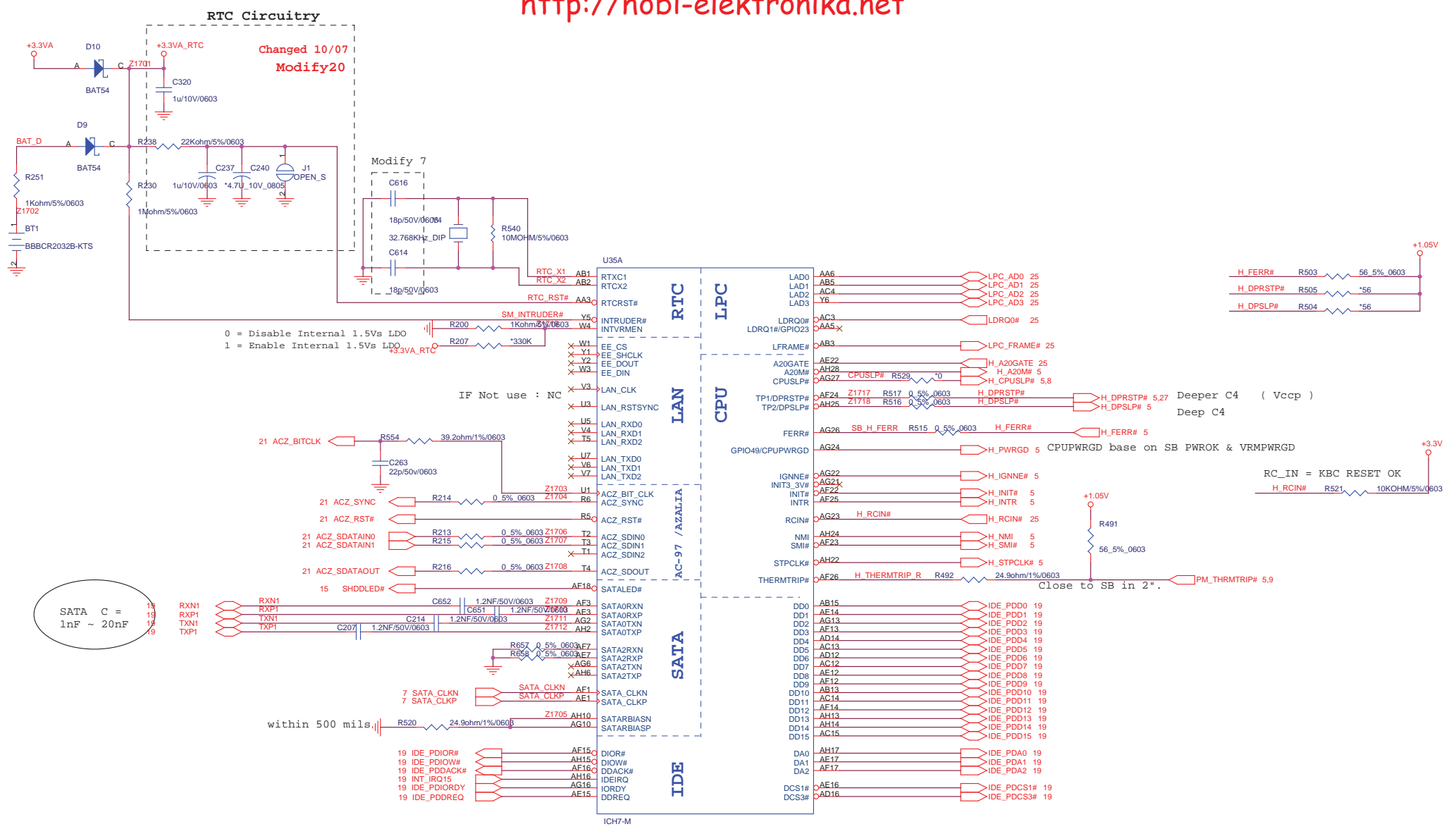
LCD

LCDVCC

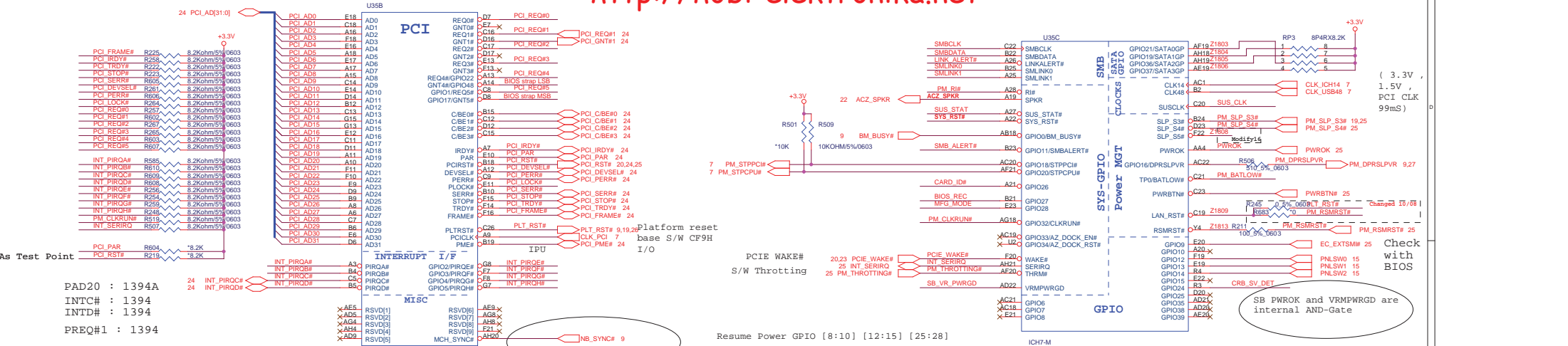


INVERTER



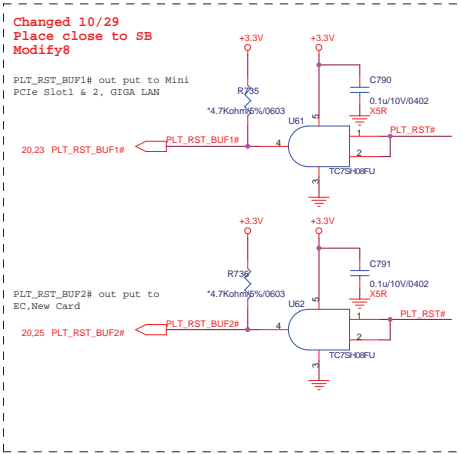
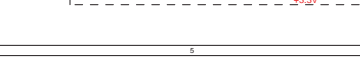
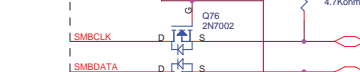
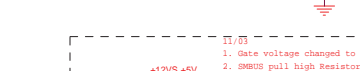
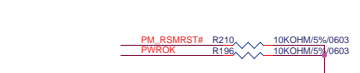
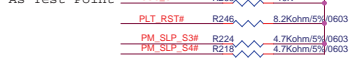


UNIWILL COMPUTER (SIP) Co.,LTD		
Title		
X721A6		
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SCHEMATIC: SB ICH7-M CPU/SATA/IDE-1/3		
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As Test Point
 PAD20 : 1394A
 INTCH# : 1394
 INTD# : 1394
 PREQ#1 : 1394

Sample on PWROK rise edge
 01 = SPI
 10 = PCI
 11 = LPC
 (Internal PU)
 Strap SPKR 1:Normal
 0:No Reboot Mode



U280	U281	U282	U283	U284	U285	U286	U287
CardReader	TV Tuner	CON(USB BD)	NEW_CARD	CON(USB BD)	CON(USB BD)	mini PCIe	DVI DOCKING

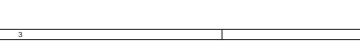
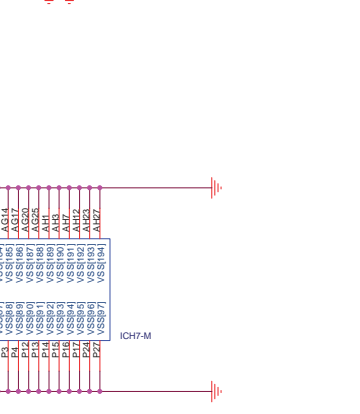
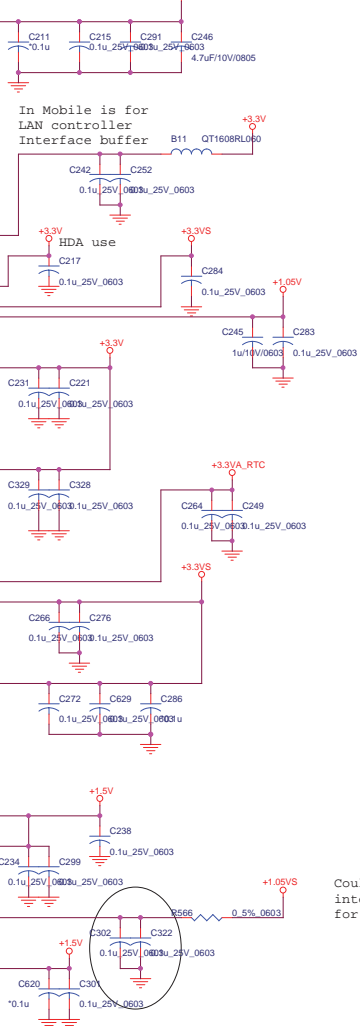
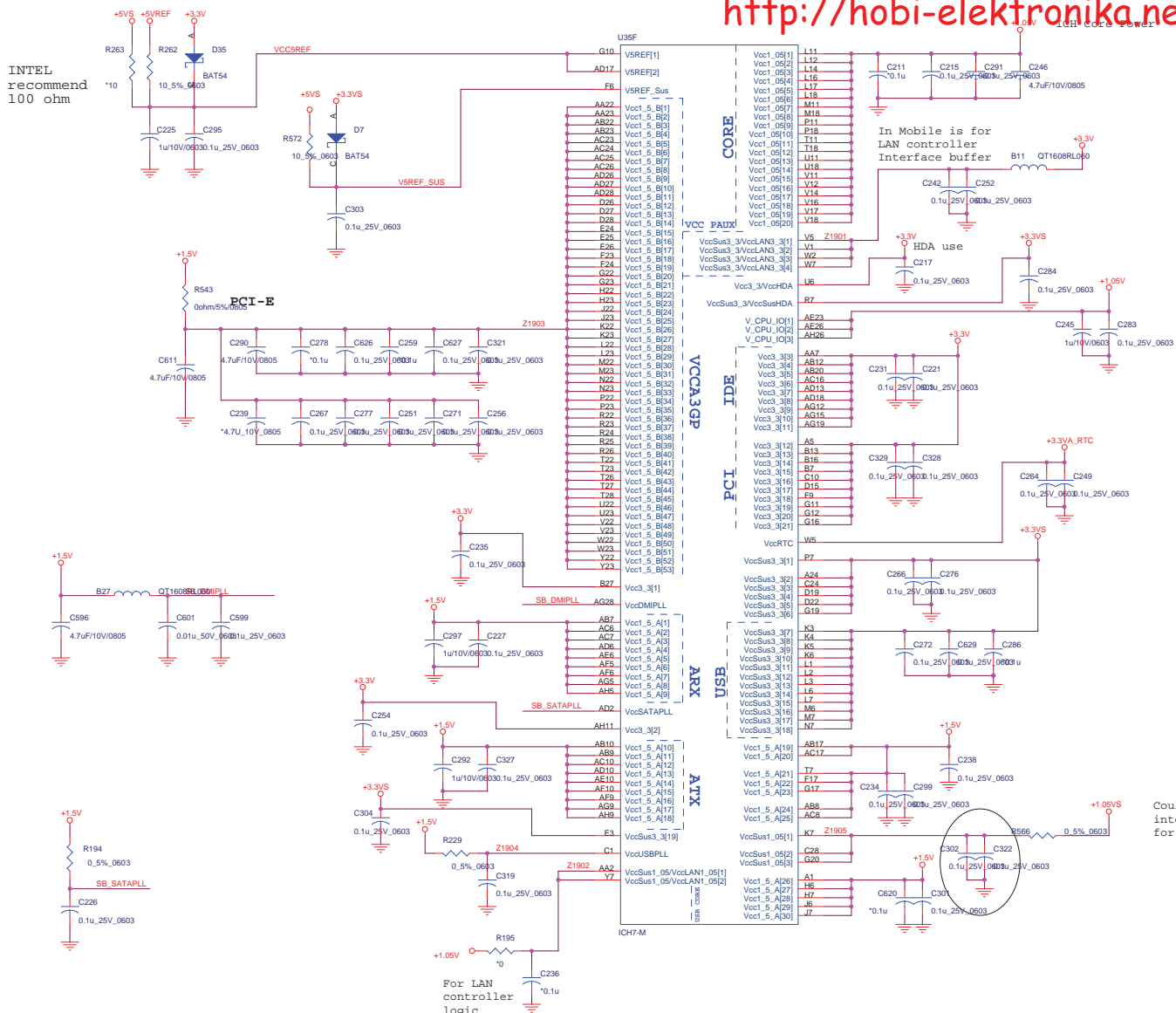
UNIWILL COMPUTER (SIP) Co.,LTD

X72IA6

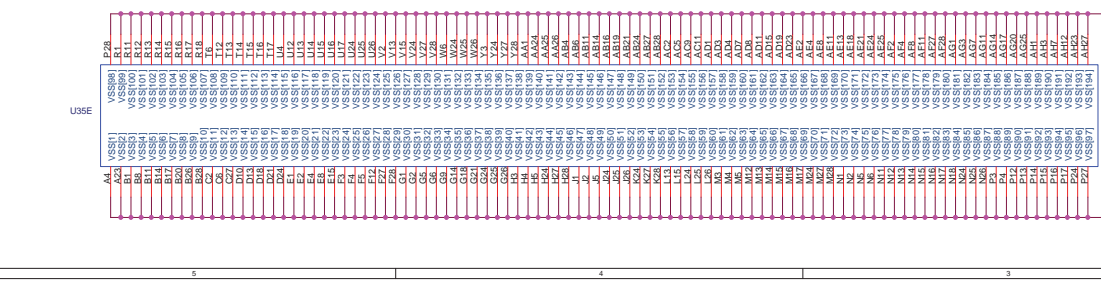
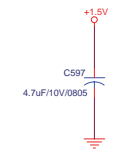
SB ICH7-M VO/GPIO/SYS-2/3

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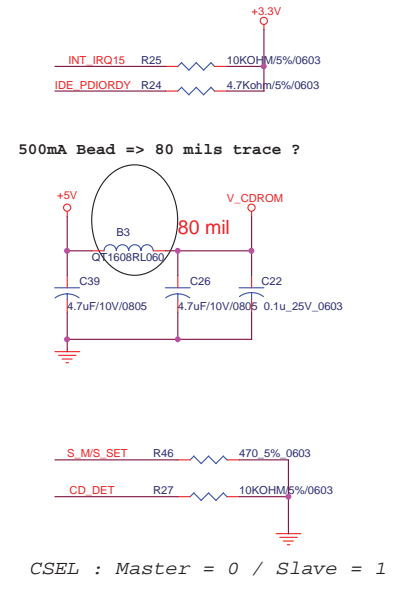
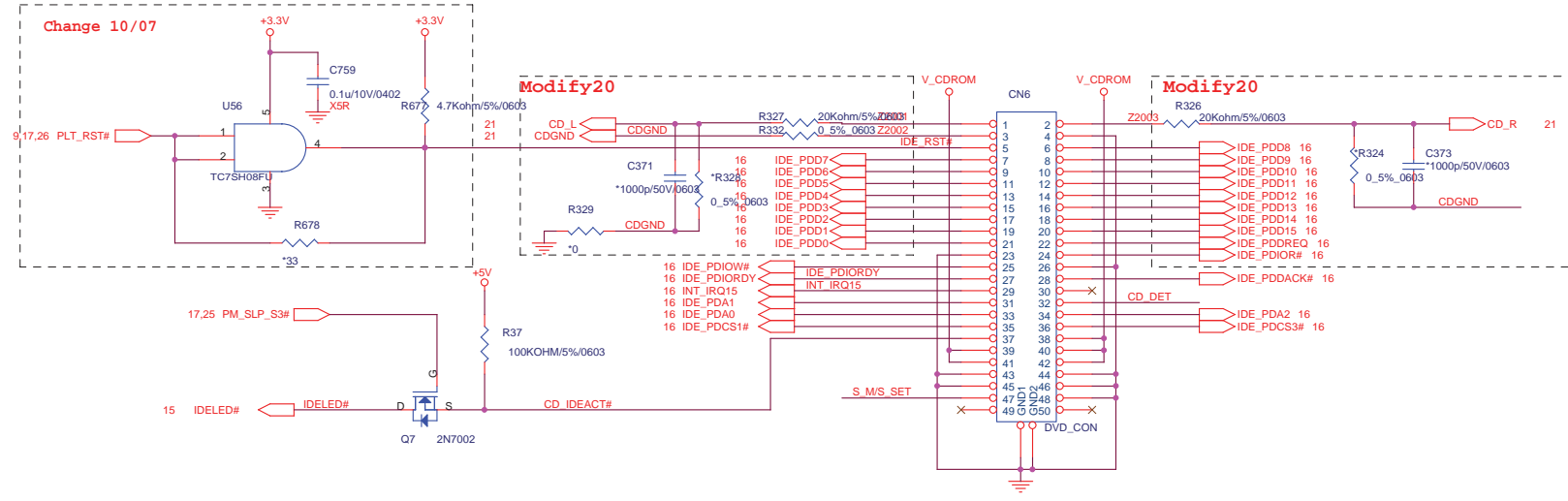
INTEL recommend 100 ohm



Could be generated internal by strap for LAN logic

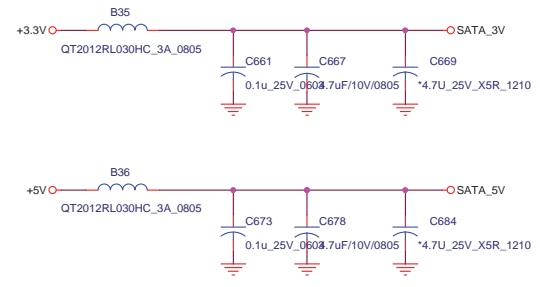
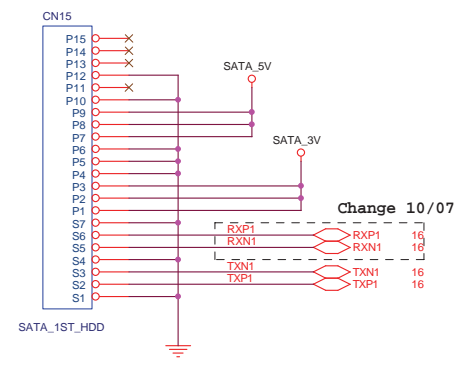


CR-ROM

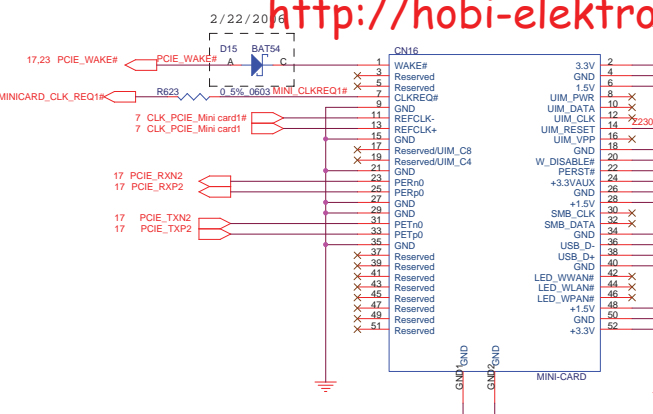
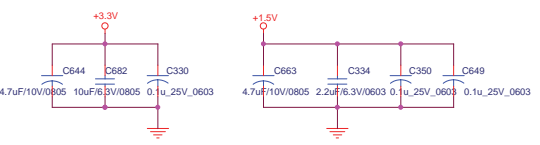


CSEL : Master = 0 / Slave = 1

SATA HDD

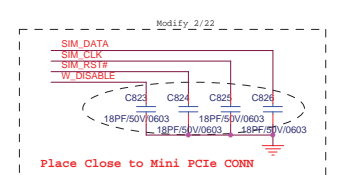
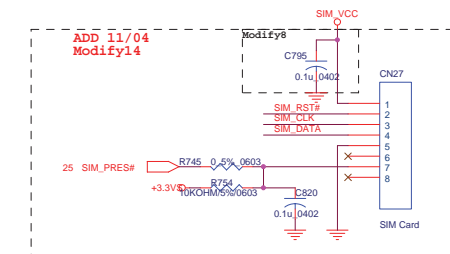
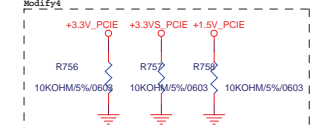
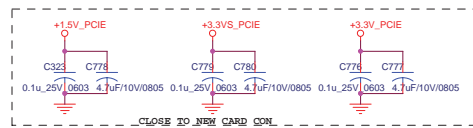
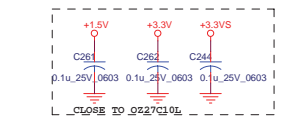
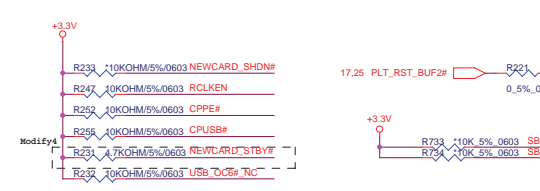
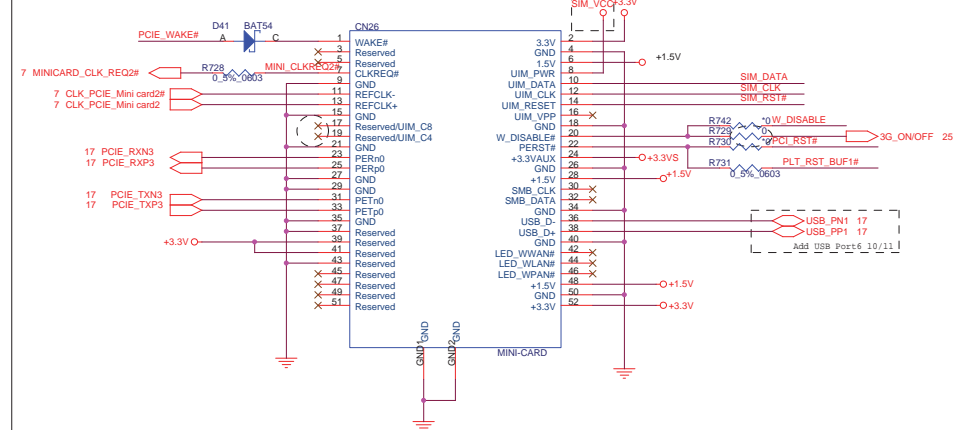
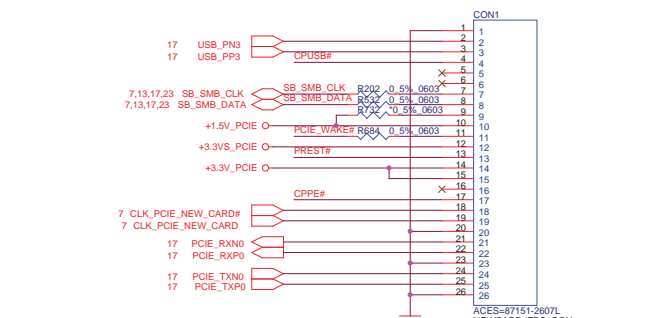
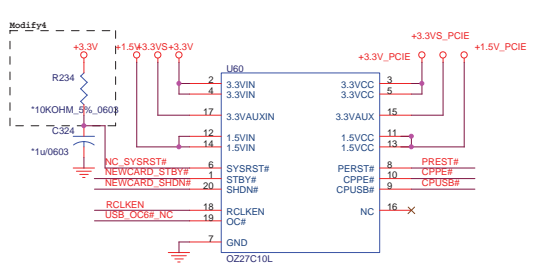
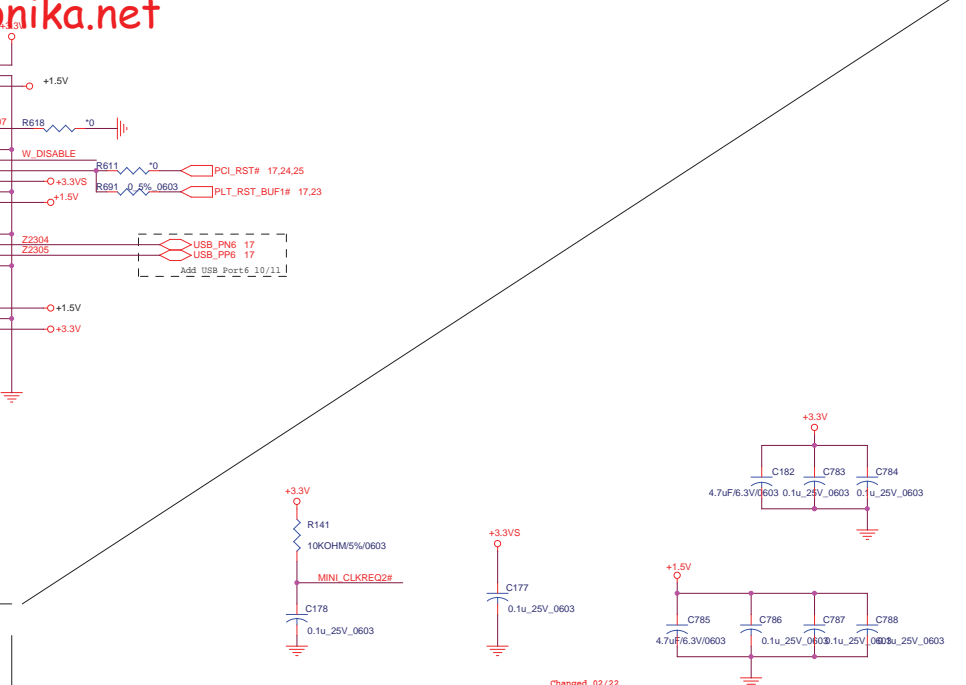
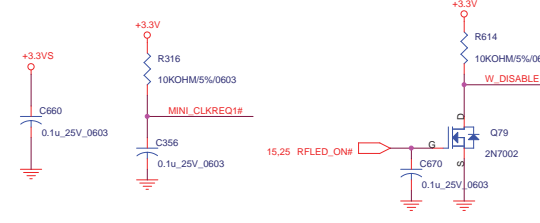


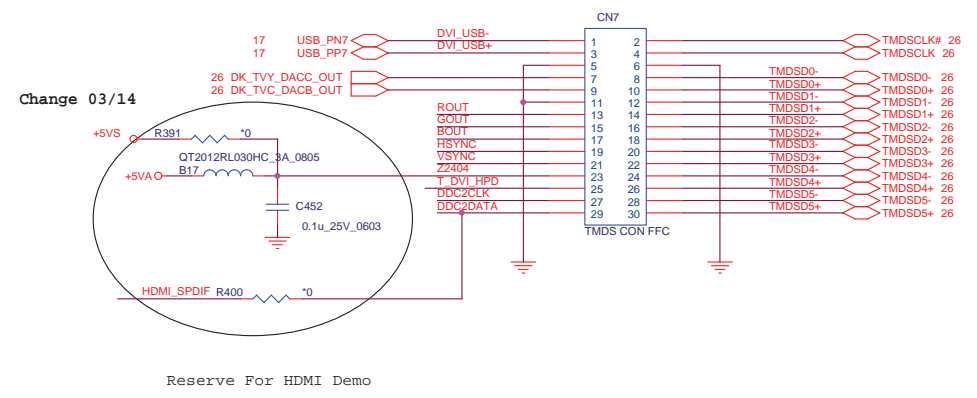
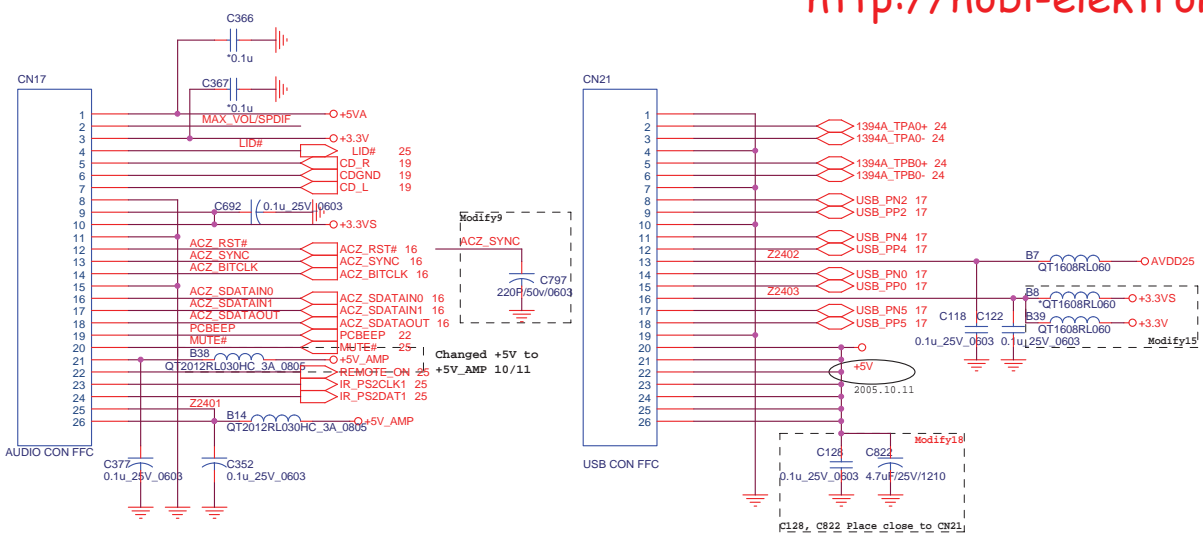
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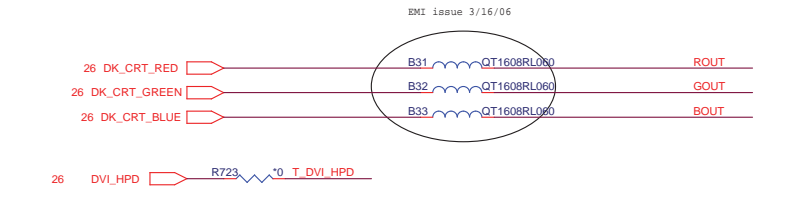
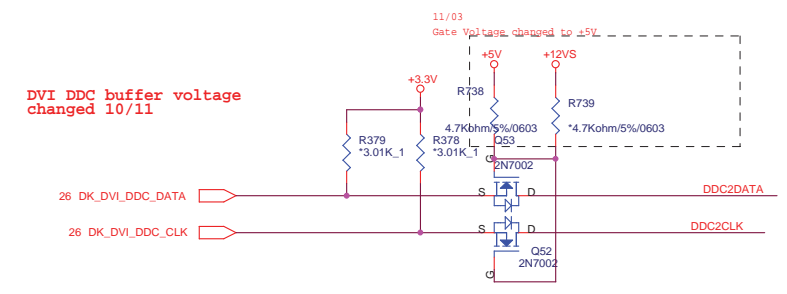
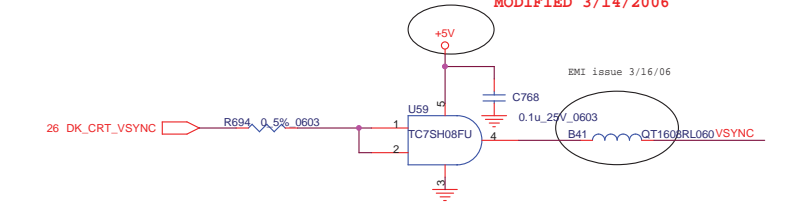
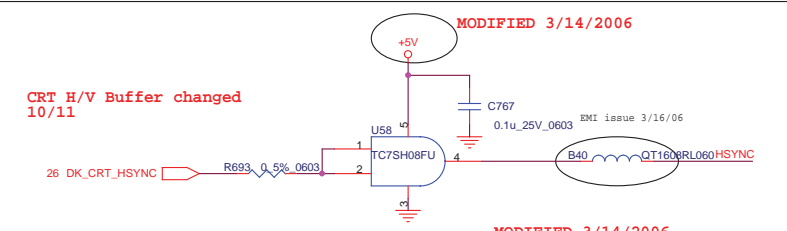
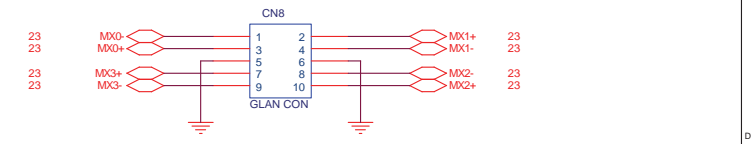
MINI CARD CONN
Intel PRO/Wireless 2100 LAN

Pin	Signal	Level	Function
Pin11	LD_MLAN_LINK	Hi (3.3V)	Solid ON Not Associated with an AP
Pin12	LD_MLAN_ACT	Hi (3.3V)	Rapid Blinking Passing data traffic to AP
Pin13	HM_RadioXMIT_OFF#	Hi (3.3V)	Enable Radio transmitter is ON
		Low (0V)	Disable Radio transmitter turn off



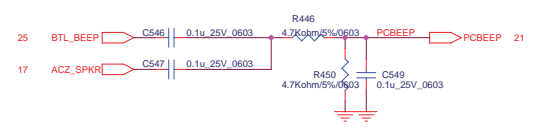
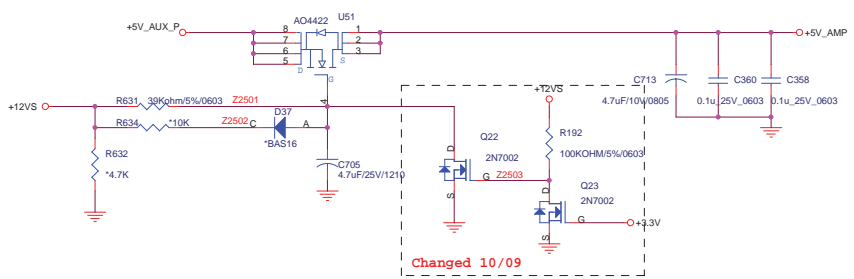


Reserve For HDMI Demo

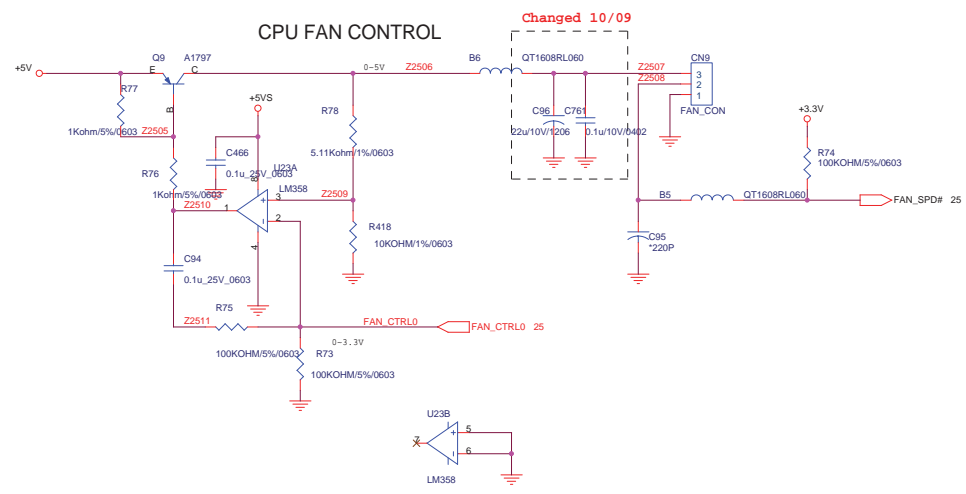


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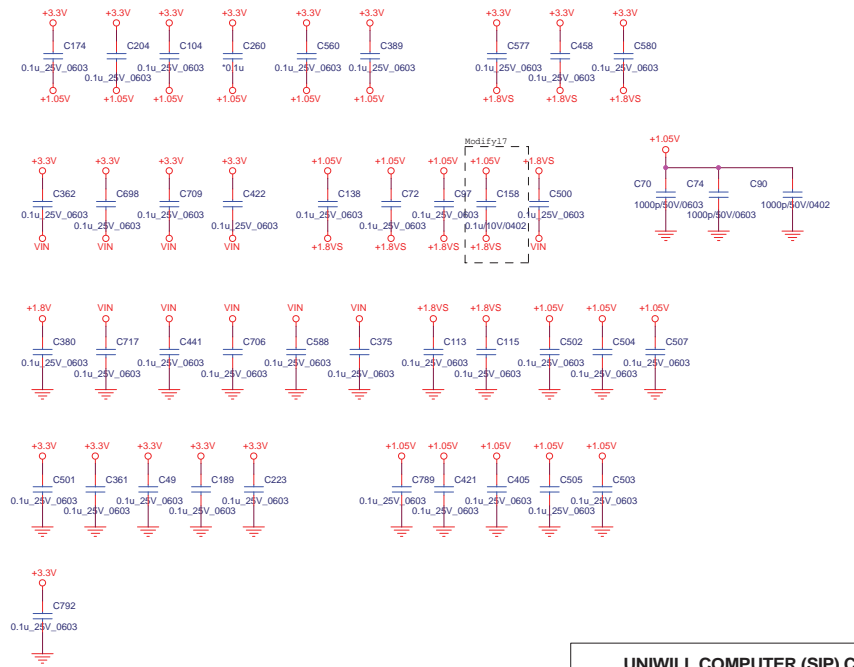
AMP VDD

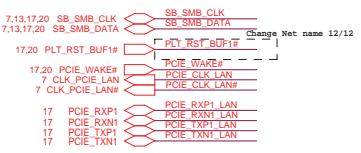


CPU FAN CONTROL

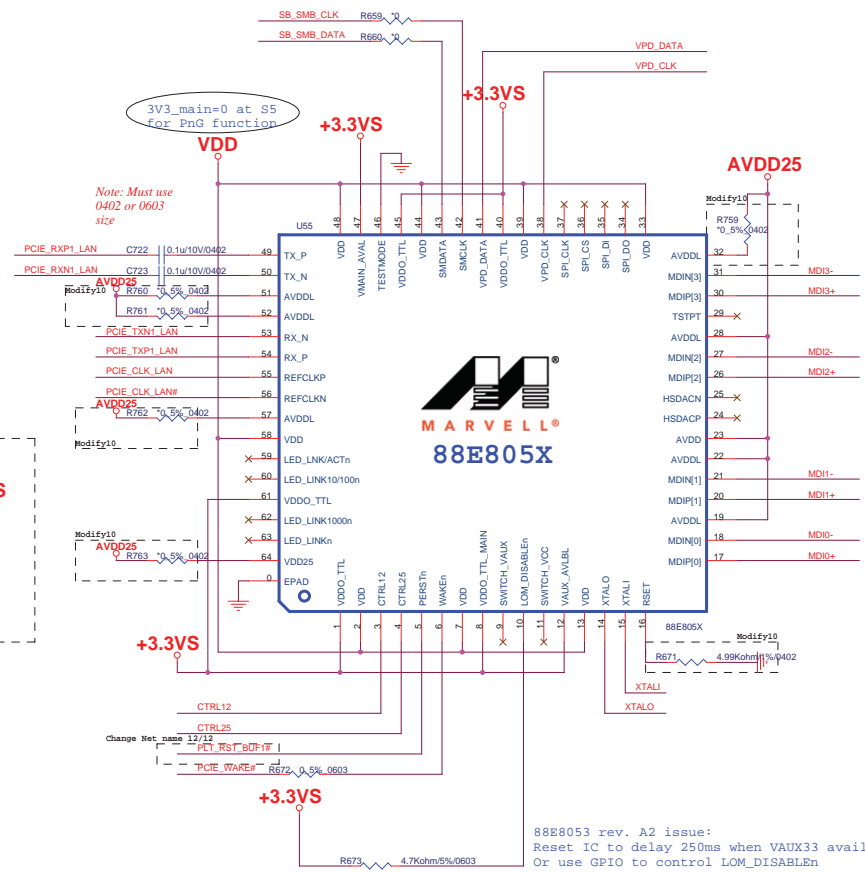
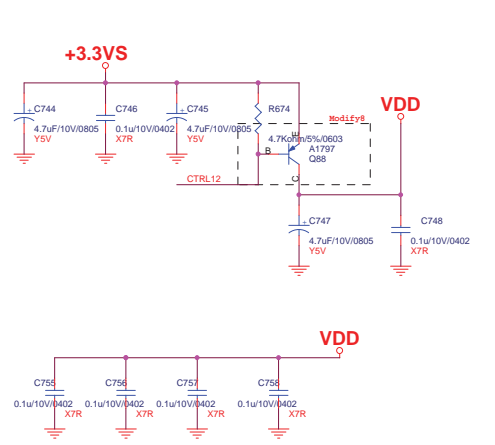
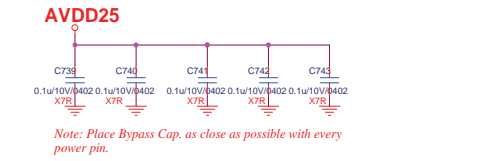
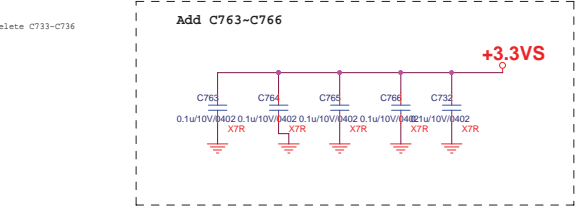
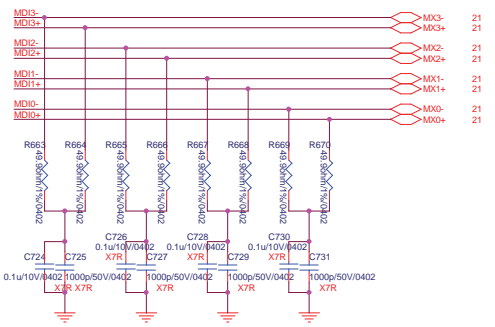


FOR EMI



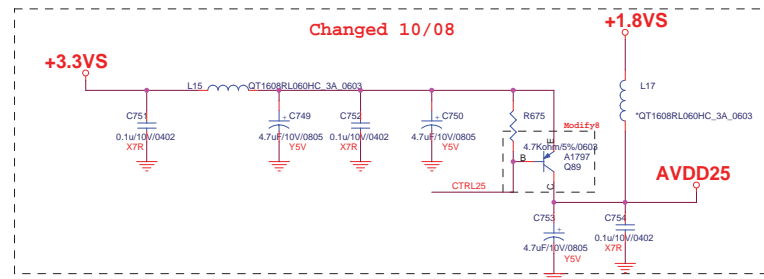


If use 88E8053, Pin42,Pin43 must be pulled up to 3.3V with 4.7KOHM



Note: Must use 0402 or 0603 size

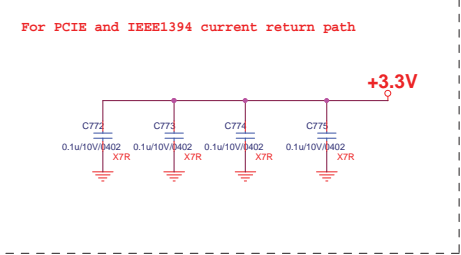
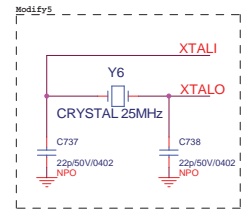
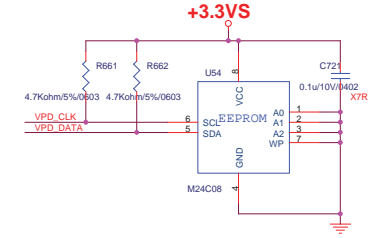
88E8053 rev. A2 issue: Reset IC to delay 250ms when VAUX33 available. Or use GPIO to control LOM_DISABLEn

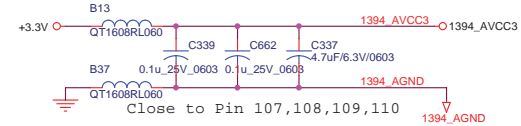
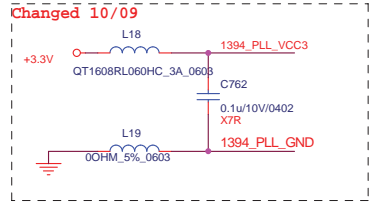


PLACE PNP TO CHIP ACAP CTRL25 PIN TRACE IS 25MIL

R671 as close as possible to ASIC
 88E8053: R671=4.87Kohm/1%/0603
 R759,R760,R761,R762,R763 Stuff
 88E8055: R671=4.99Kohm/1%/0603
 (Default)R759,R760,R761,R762,R763 not Stuff

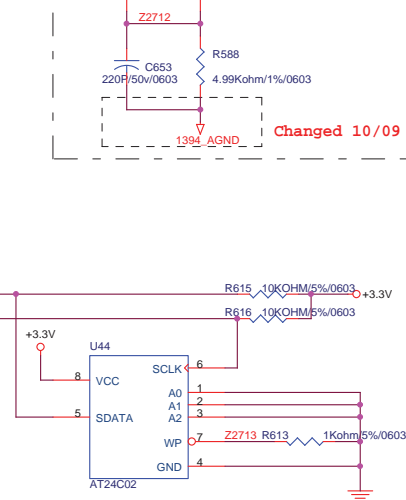
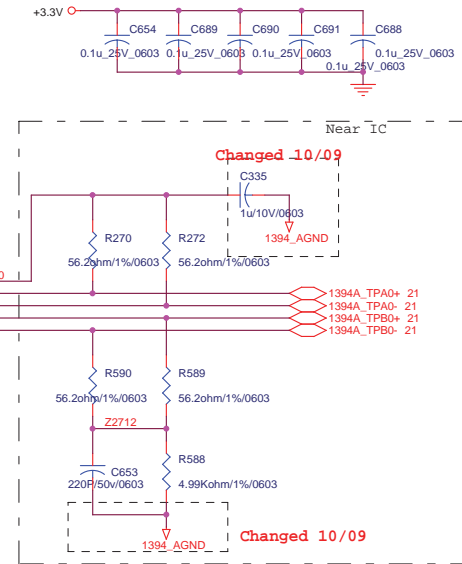
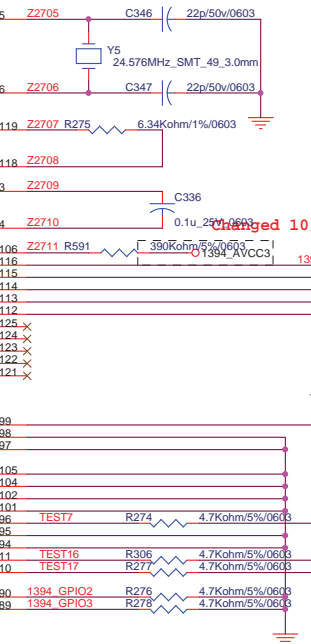
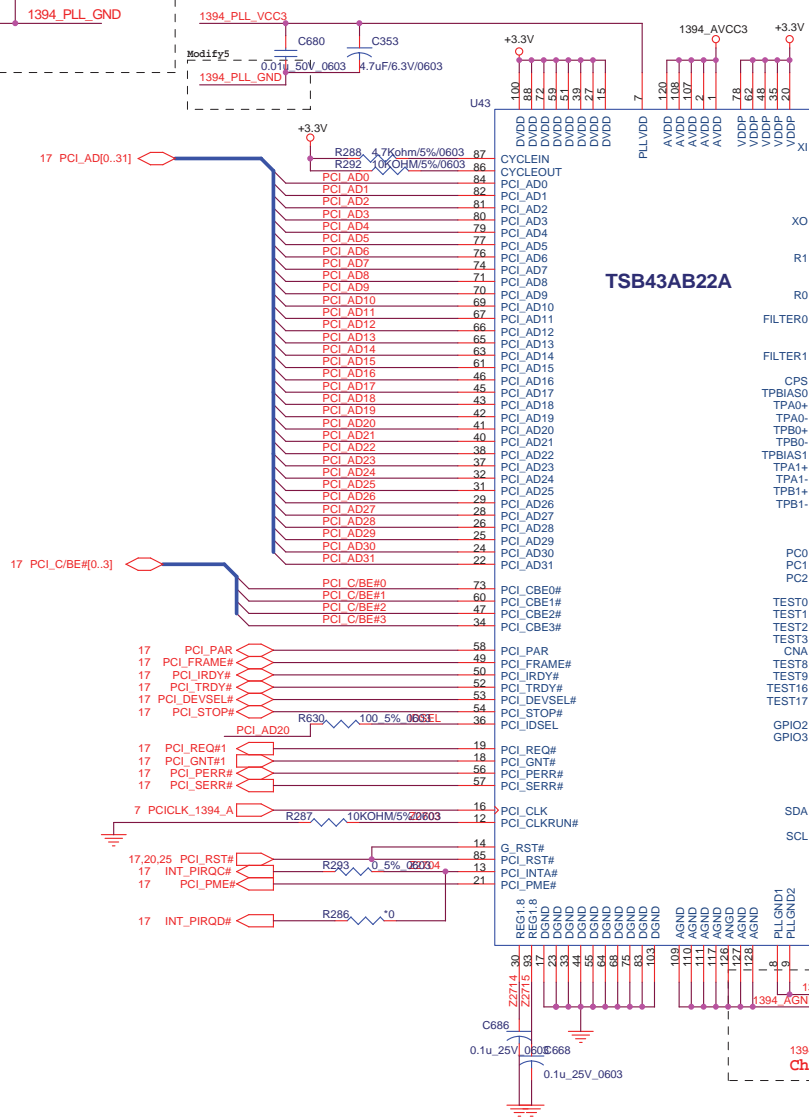
	88E8053	88E8055
AVDD25	2.5V	1.8V





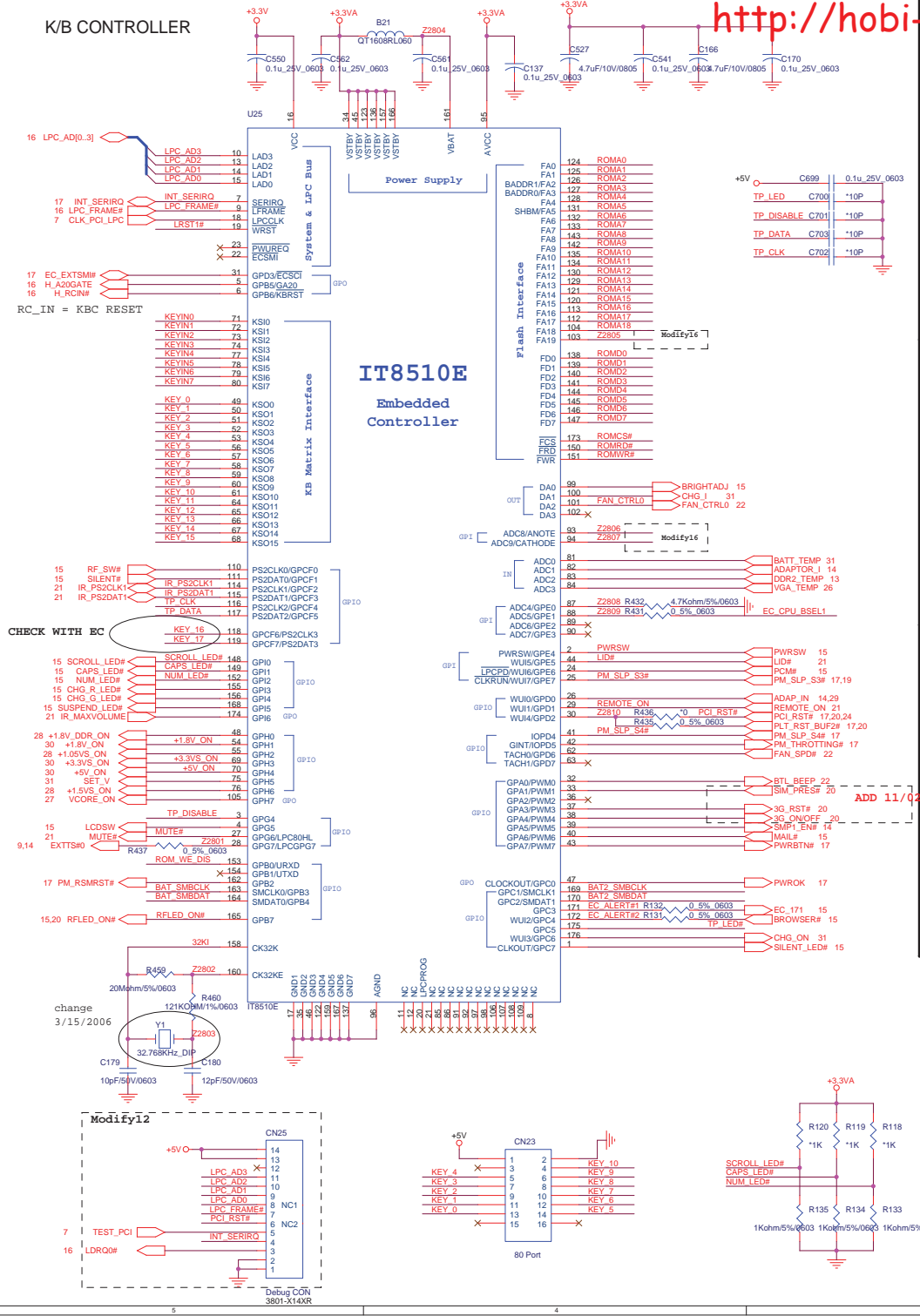
Crystal Placement

Crystal must be placed as close as possible to the TSB43AB22. Keep traces all on one PCB layer.

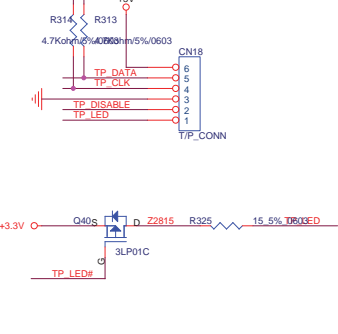


UNIWILL COMPUTER (SIP) Co.,LTD		
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SCHMATIC1	IEEE1394A TSB43AB22A	B
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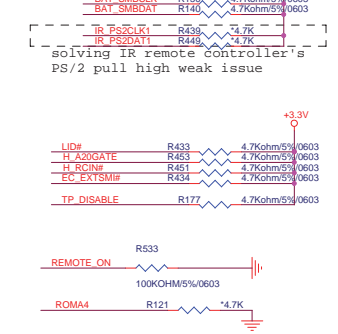
K/B CONTROLLER



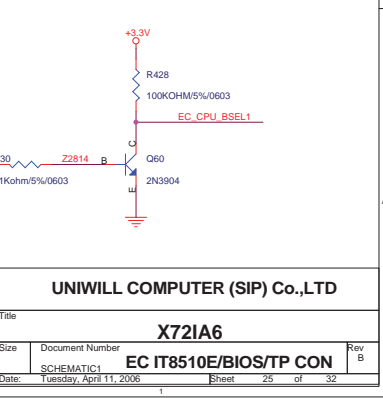
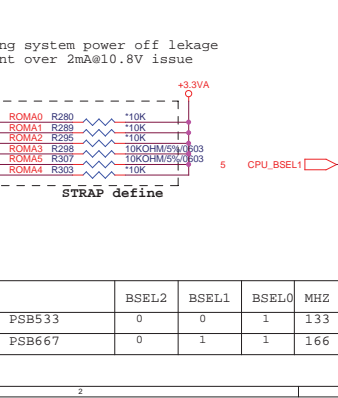
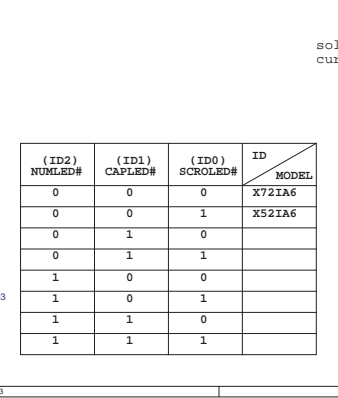
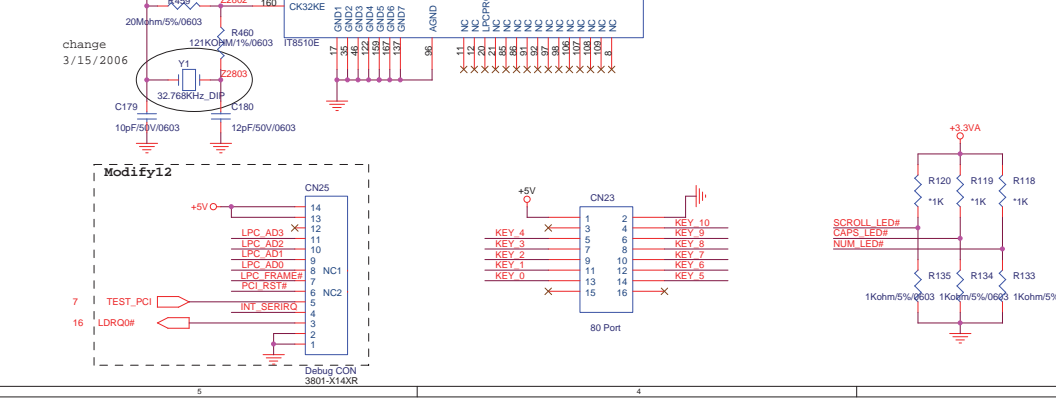
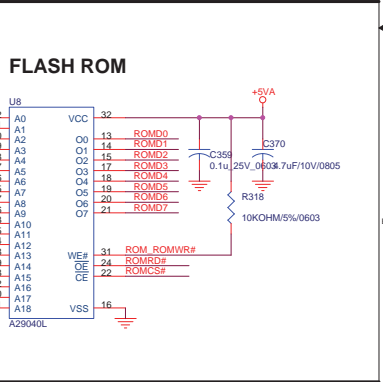
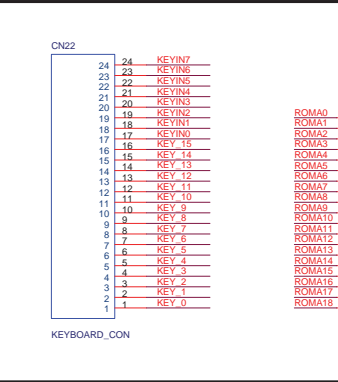
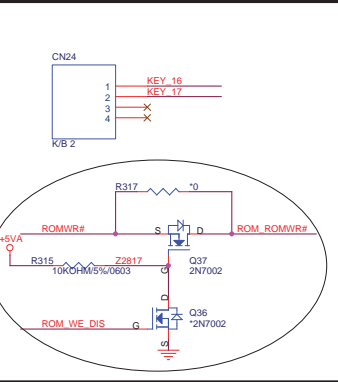
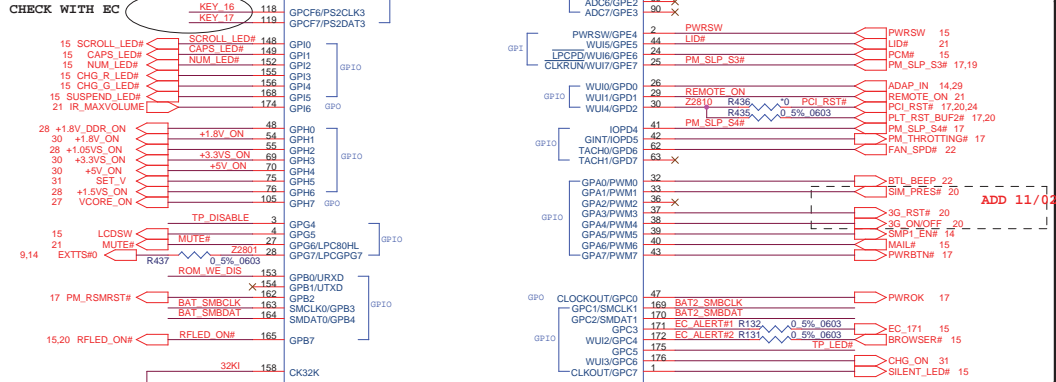
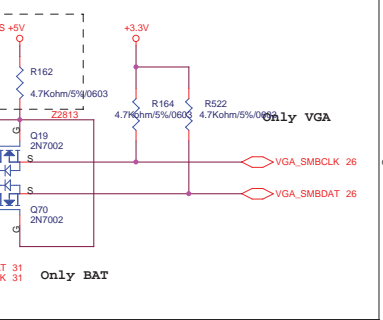
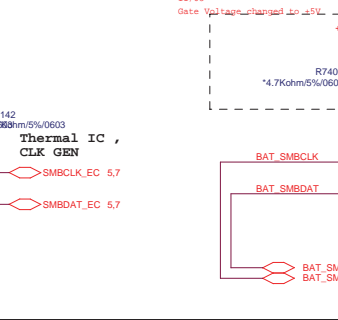
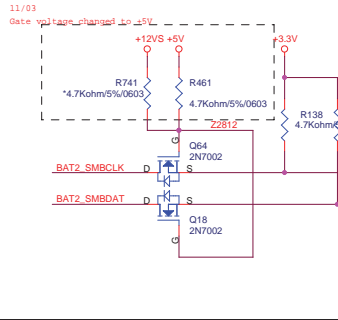
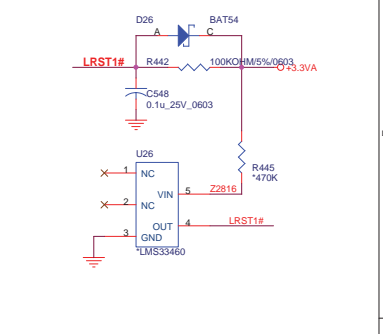
TOUCHPAD CONNECTOR



PS/2 pull high weak issue



Only VGA



(ID2) NUMLED#	(ID1) CAPLED#	(ID0) SCROLED#	ID	MODEL
0	0	0	0	X72IA6
0	0	1	0	X52IA6
0	1	0	1	
0	1	1	1	
1	0	0	0	
1	0	1	0	
1	1	0	0	
1	1	1	1	

	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	1.33
PSB667	0	1	1	1.66

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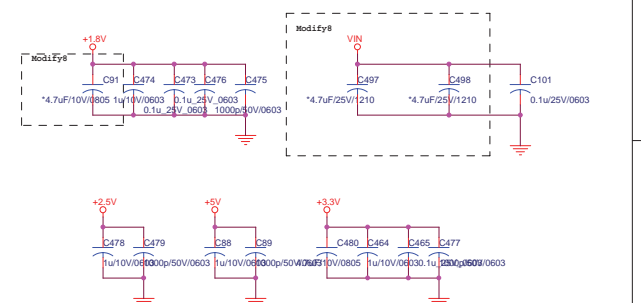
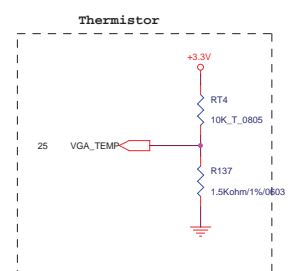
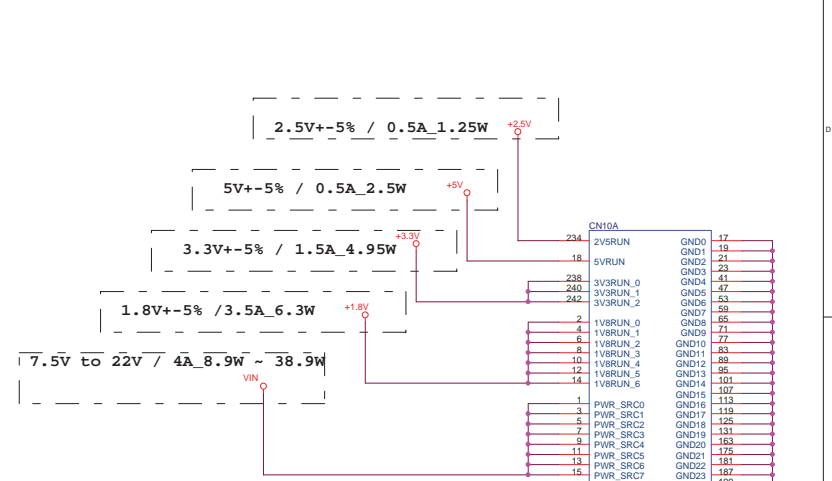
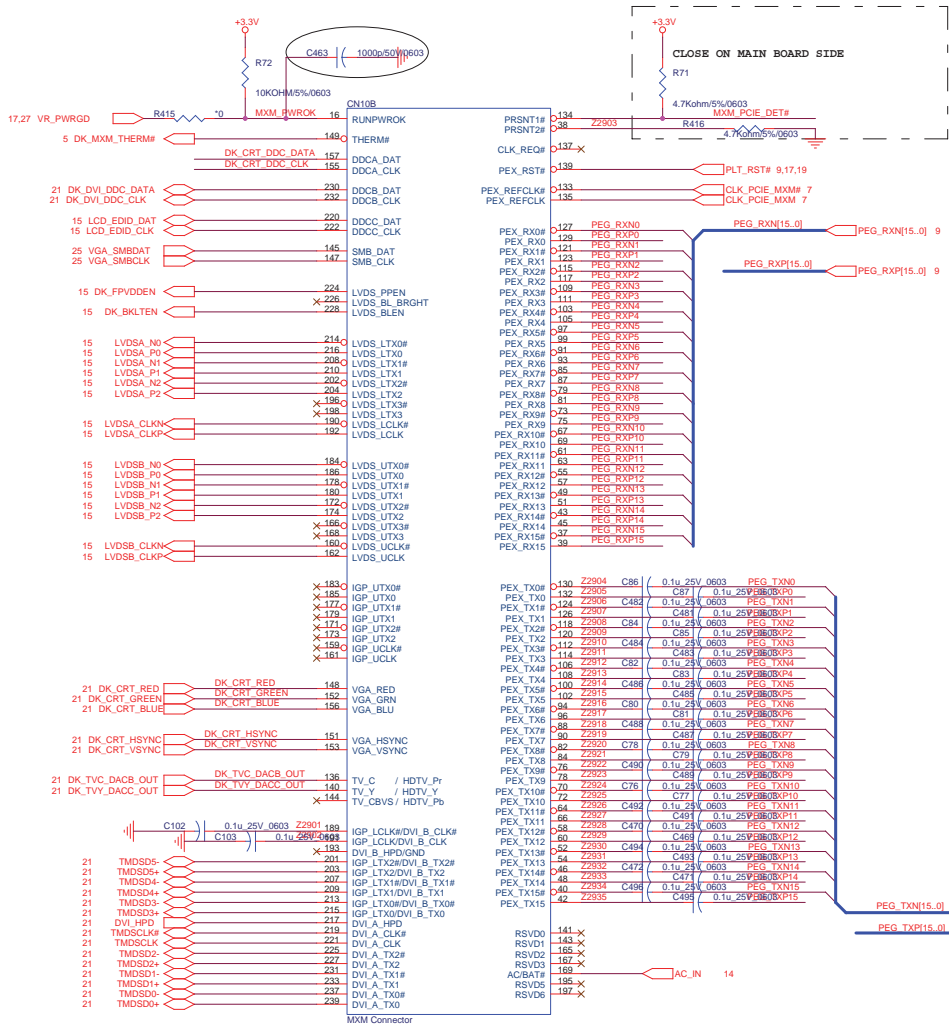
Title: X72IA6

EC IT8510E/BIOS/TP CON

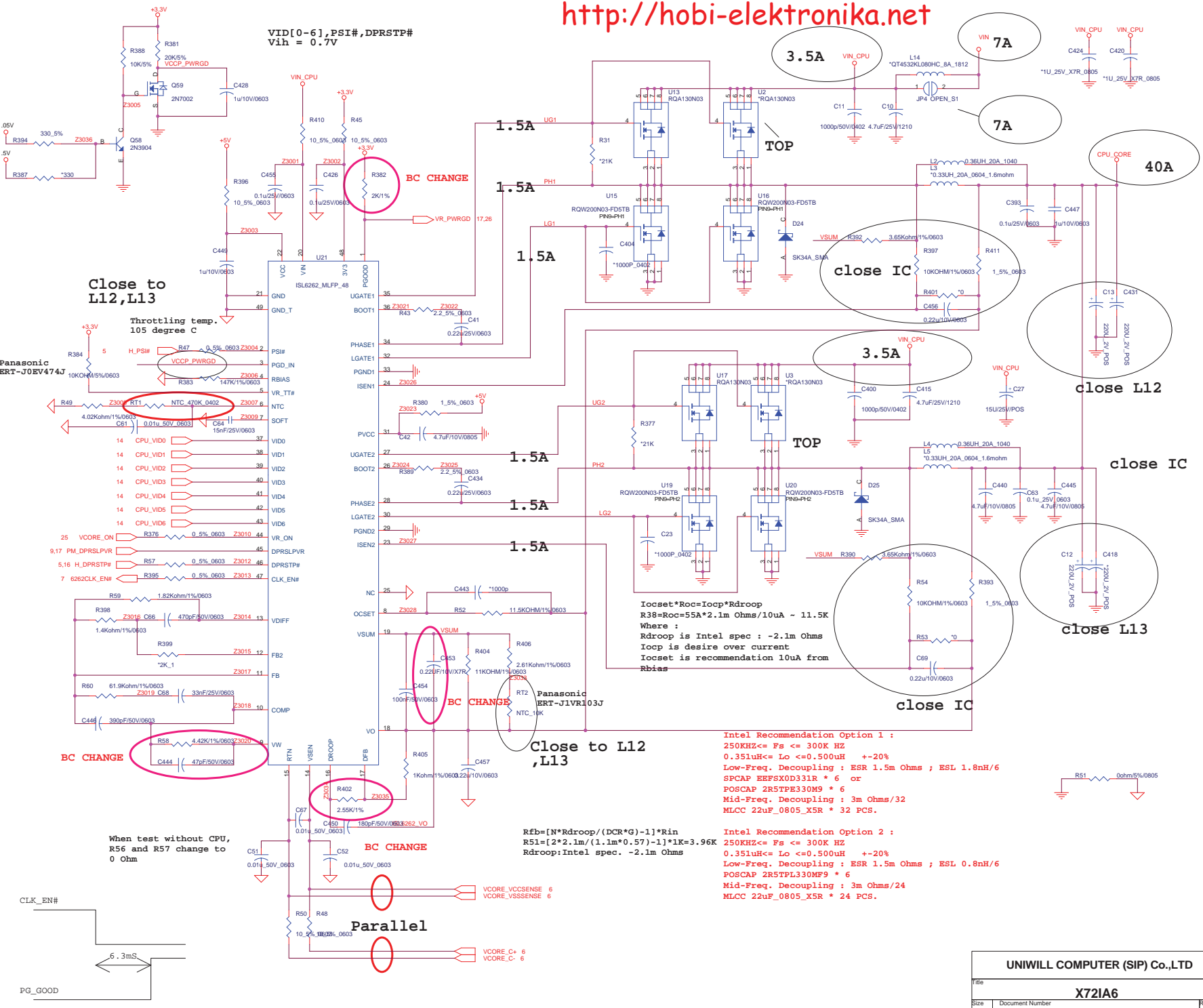
Document Number: Schematic1

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VID[0-6],PSI#,DPRSTP#
Vih = 0.7V



Intel Recommendation Option 1 :
 250KHZ <= Fs <= 300K HZ
 0.35uH <= Lc <= 0.500uH +-20%
 Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 1.8nH/6
 SPCAP EEF5XD331R * 6 or
 POSCAP 2R5TPE330M9 * 6
 Mid-Freq. Decoupling : 3m Ohms/32
 MLCC 22uF_0805_X5R * 32 PCS.

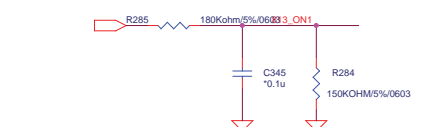
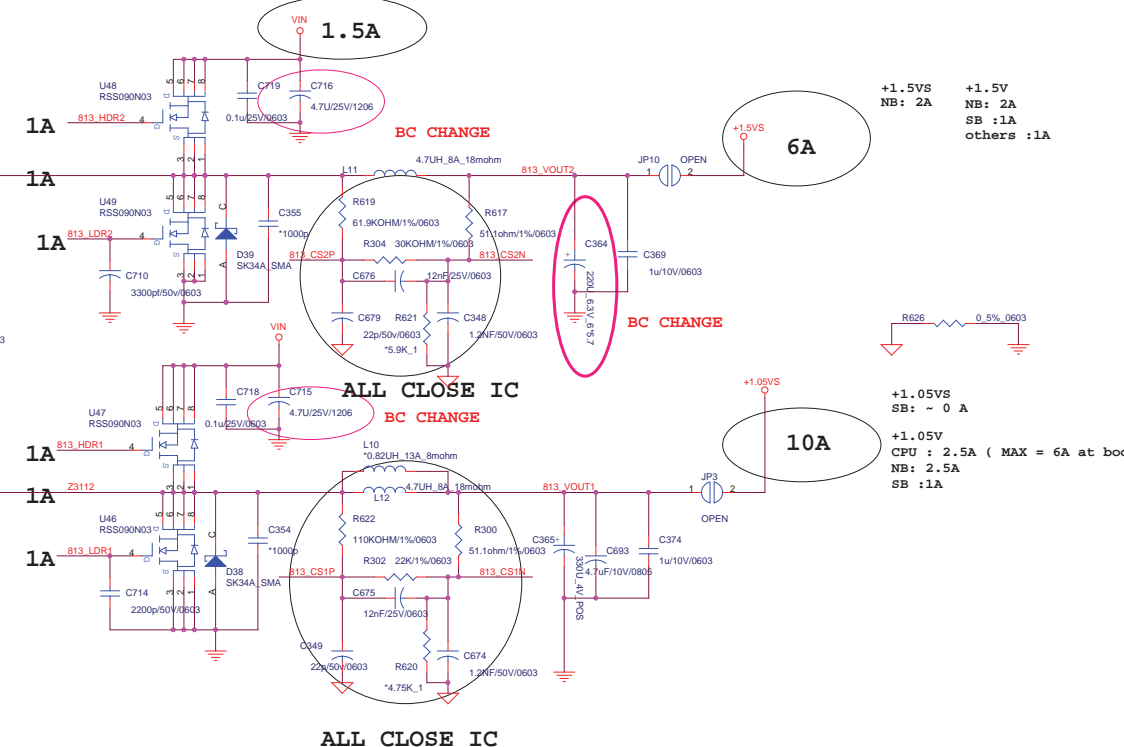
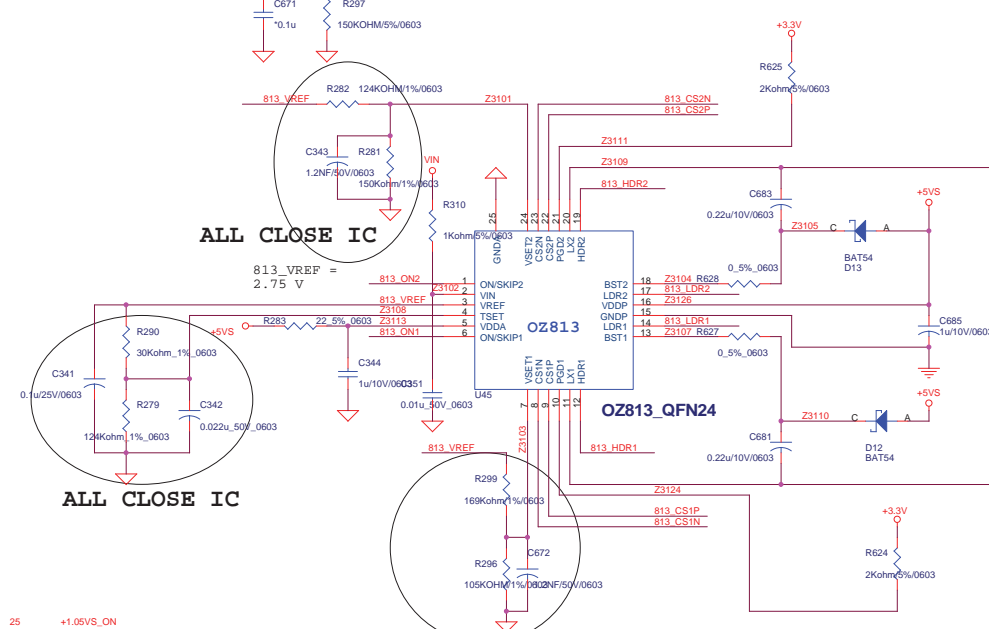
Intel Recommendation Option 2 :
 250KHZ <= Fs <= 300K HZ
 0.35uH <= Lc <= 0.500uH +-20%
 Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 0.8nH/6
 POSCAP 2R5TPL330MP9 * 6
 Mid-Freq. Decoupling : 3m Ohms/24
 MLCC 22uF_0805_X5R * 24 PCS.

$R_{fb} = [N * R_{droop} / (DCR * G) - 1] * R_{in}$
 $R_{51} = [2 * 2.1m / (1.1m * 0.57) - 1] * 1K = 3.96K$
 $R_{droop} : \text{Intel spec. } -2.1m \text{ Ohms}$

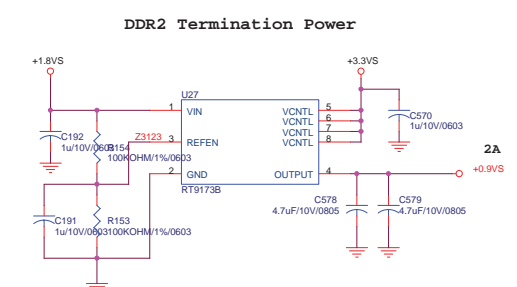
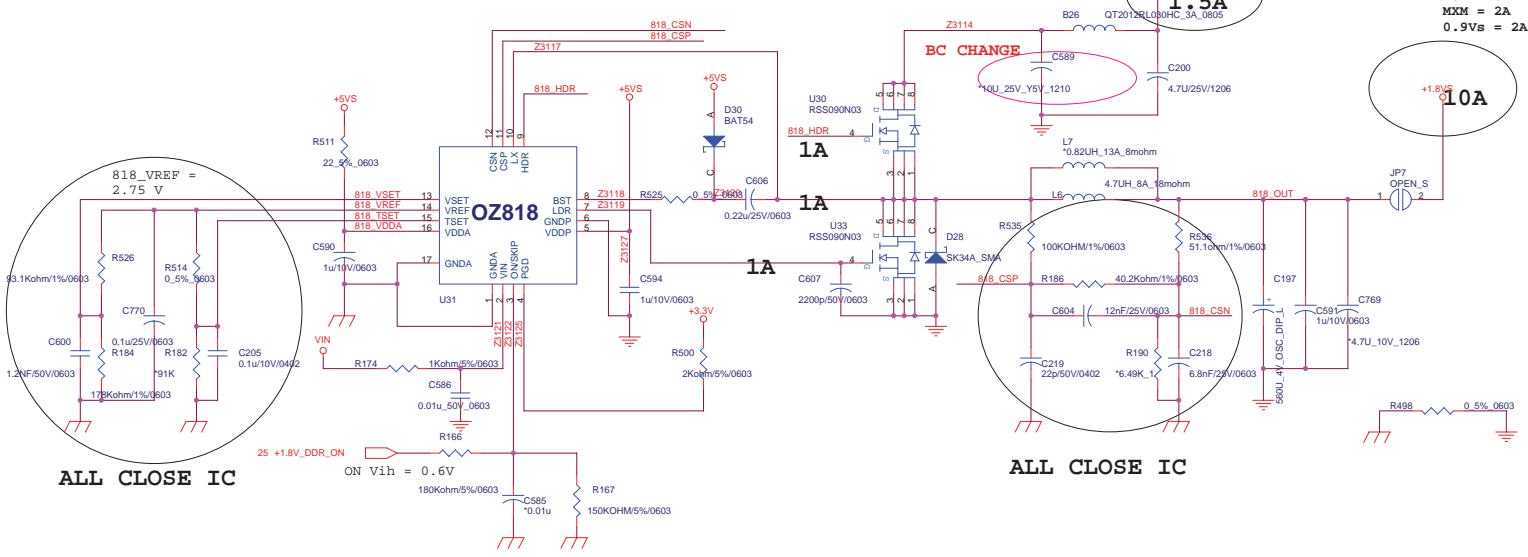
$I_{ocset} * R_{oc} = I_{ocp} * R_{droop}$
 $R_{38} = R_{oc} = 55A * 2.1m \text{ Ohms} / 10uA \sim 11.5K$
 Where :
 R_{droop} is Intel spec : -2.1m Ohms
 I_{ocp} is desire over current
 I_{ocset} is recommendation 10uA from Rbias

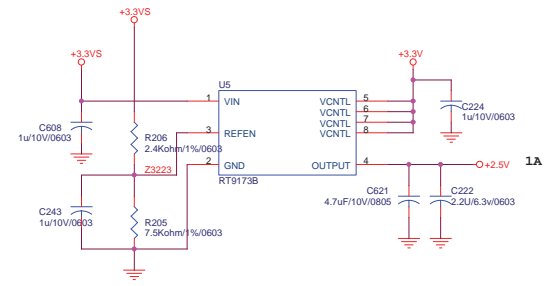
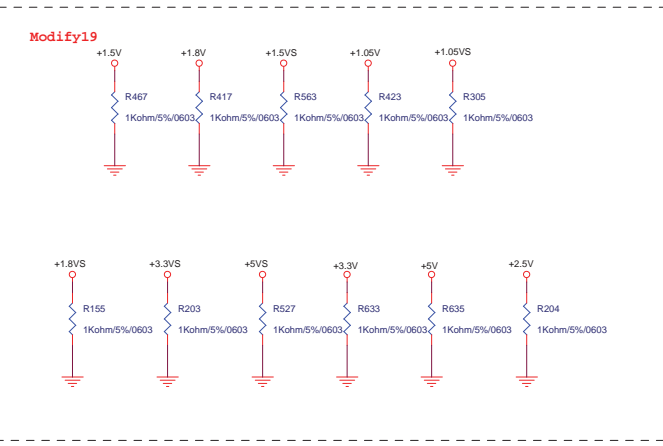
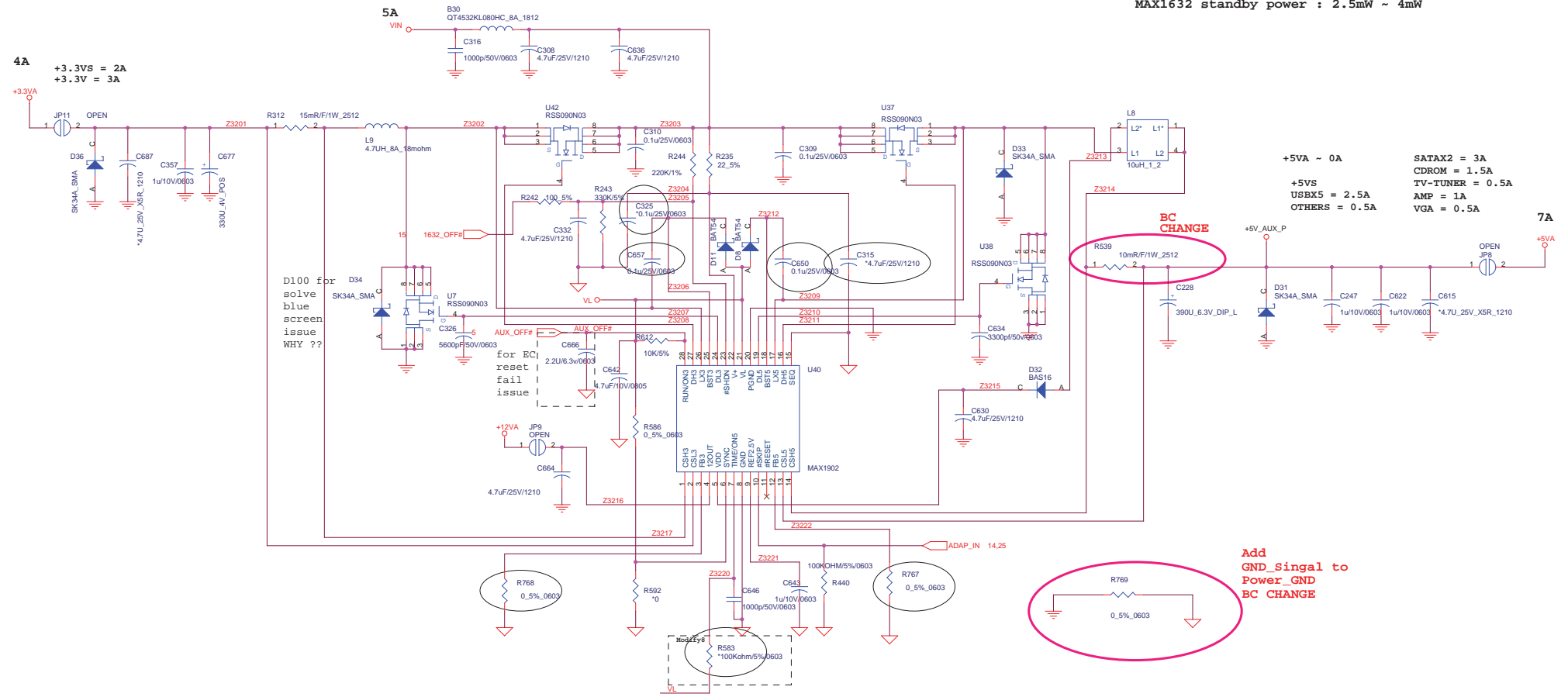
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25 +1.5V_ON ON Vih = 0.6V
0.6V ~ 2.1V = PWM ON
> 2.1V PWM + SKIP

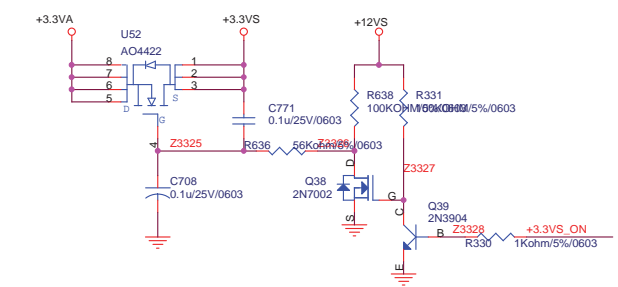
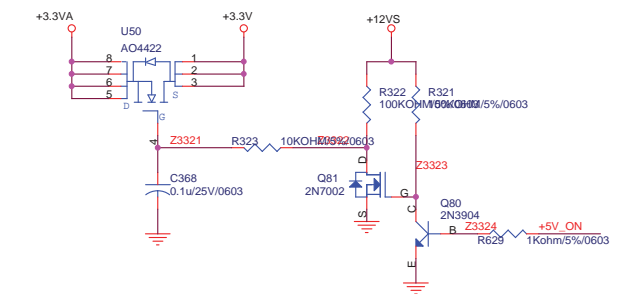
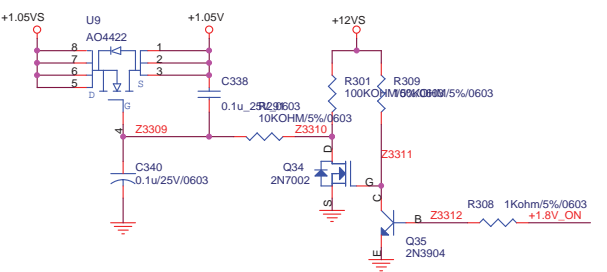
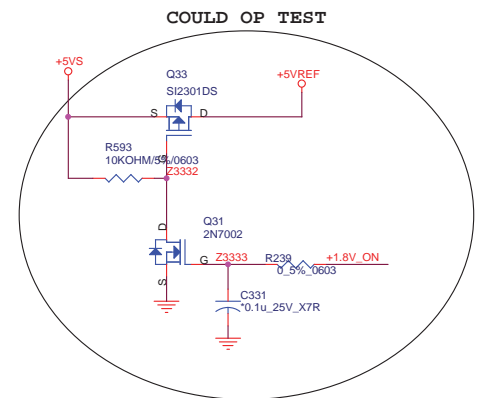
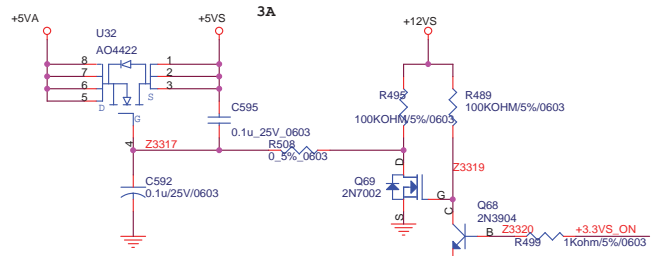
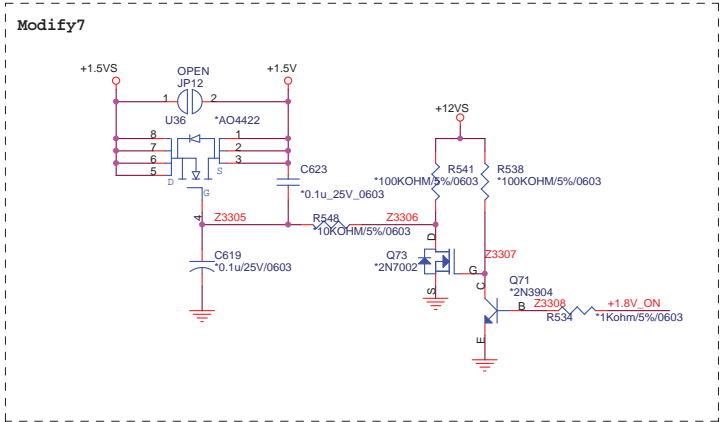
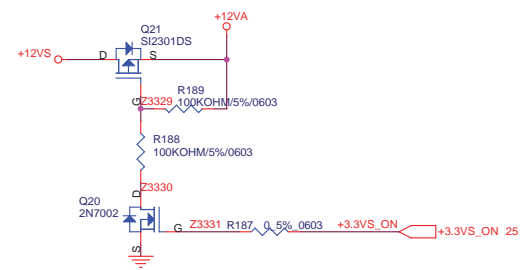
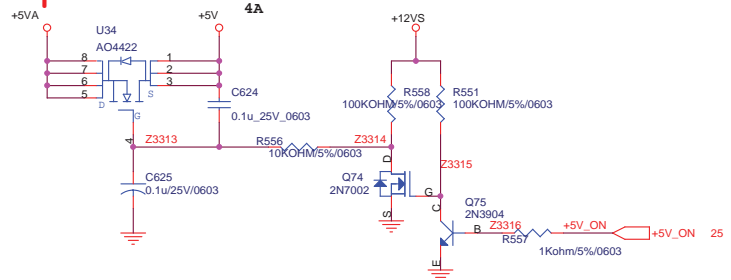
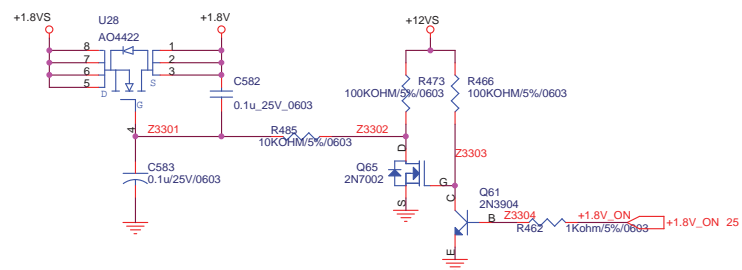


mem = 6A
MXM = 2A
0.9Vs = 2A



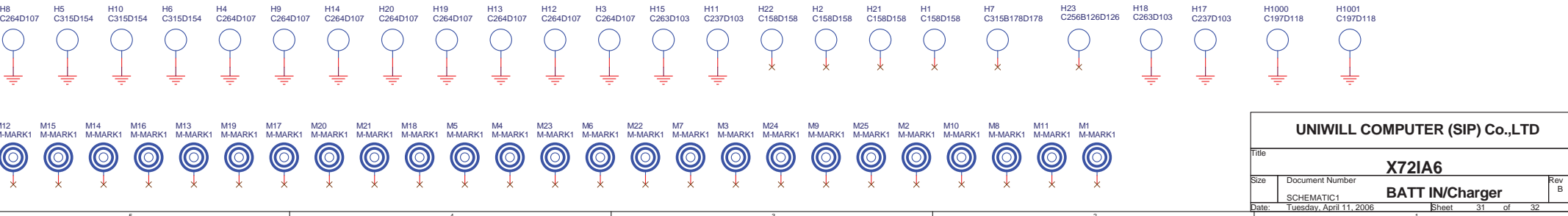
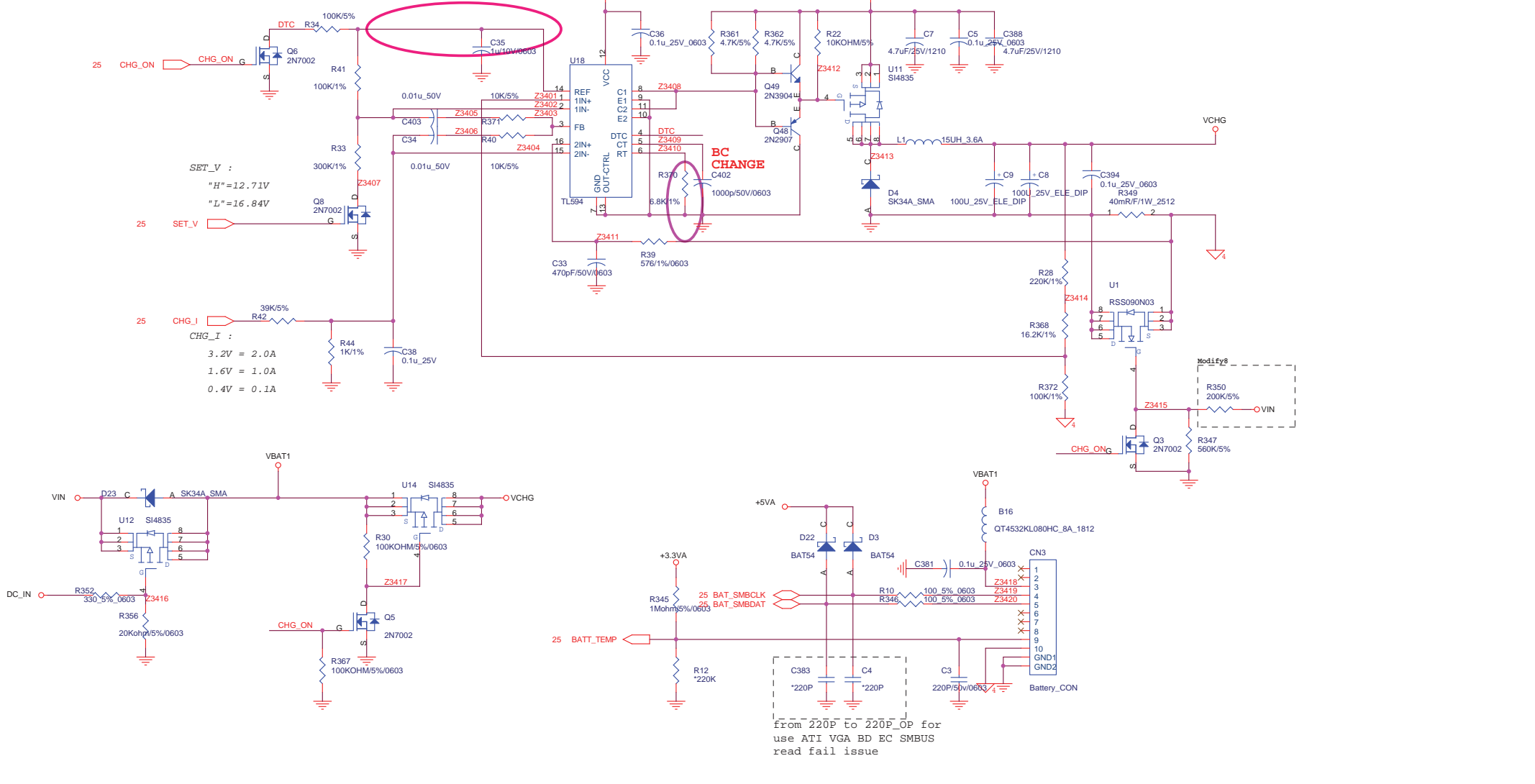


	MAX1632	MAX1902	SC1404
R767	0	100pF	
R768	0	100pF	
R583	100K_OP	100K	
R312, R539	15mR, 15mR	8mR, 8mR	
C315	OP	4.7U_25V	
C325	OP	0.1U_25V	
C650, C657	0.1U_16V	0.22U_25V	



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BC CHANGE Del Vcc5V



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Document Number: **BATT IN/Charger**

Rev: **B**

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Rev: B

- Modify2: I945PM Add Thermal Strap, Add R755, Delete D5 at Page09
- Modify3: Reserved R112 at Page09
- Modify4: Revise NewCard Power supply, Reserved R234, Stuff R231 & change to 4.7KOHM , Add R756,R757,R758,R766 at Page20
- Modify5: Revise 1393 PLL Ground, Change C680,C353 GND net to 1394_PLL_GND at Page24
- Modify6: For cost down, Change Y6 P/N at Page23
- Modify7: Change +1.5V Power Supply method, Reserve U36,Q73,Q71,C619,C623,R534,R538,R541,R548 at Page30
- Modify8: Change U4 P/N at Page4,5
Change R350 P/N at Page31,
Change R510,R513 P/N at Page07
Change Q88,Q89 P/N at Page23
Change CN27 C794,C795,C796 P/N at Page20
Reserve R583 at Page29
Reserve C91,C497,C498 at Page26
Reserve R735, R736 at Page17
- Modify9: For solve ACZ_BITCLK crosstalk on ACZ_SYNC, Add C797 at Page21
- Modify10: For 88E8053,88E8055 Pin-To-Pin compatible, Add & Reserved R759,R760,R761,R762,R763 at Page23
R671 changed to 4.99Kohm for 88E8055
- Modify11: Add R764,R765,SW1,LED1,C798,D42 at Page15
- Modify12: Debug Connector signal define changed at Page25
- Modify13: Add Low pass circuit for clock at Page07
- Modify14: According to the SIM_Card's Requirement, CN27 Pin8 connect to +3.3V & Add C820 at Page20
- Modify15: Add B39 and Reserved B8, for CardReader Power Supply Changed to +3.3V. at Page21
- Modify16: Delete TP1,TP2,TP3,TP4,TP6,TP7,TP8,TP9,TP12,TP13,TP14,TP15
- Modify17: Revise C158's Net at Page22;
Add C821 at Page12;
Stuff C800,C801,C802,C803 at Page07
For solve CPU_CLK duty cycle under Spec issue.
- Modify18: Add C822 for USB Drop test fail issue at Page21
- Modify19: To Decrease static current under S3, Change R155, R203, R204, R305, R417, R423, R467, R527, R563, R633 P/N at Page29.
- Modify20: Delete Analog CD In Circuit at Page19
Reserve R326, R327,R332, C371, C373;
Change R324, R328 P/N
- Modify21: Del D27,D14,C315,C325,L3,L5, C637, C659
Change C218,R535,R402,C453,C454,R312,R539,C657,C650,U40,L1,C677,C365 P/N
Add L2,L4, R767, R768

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	SCHMATIC1	Rev	B
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