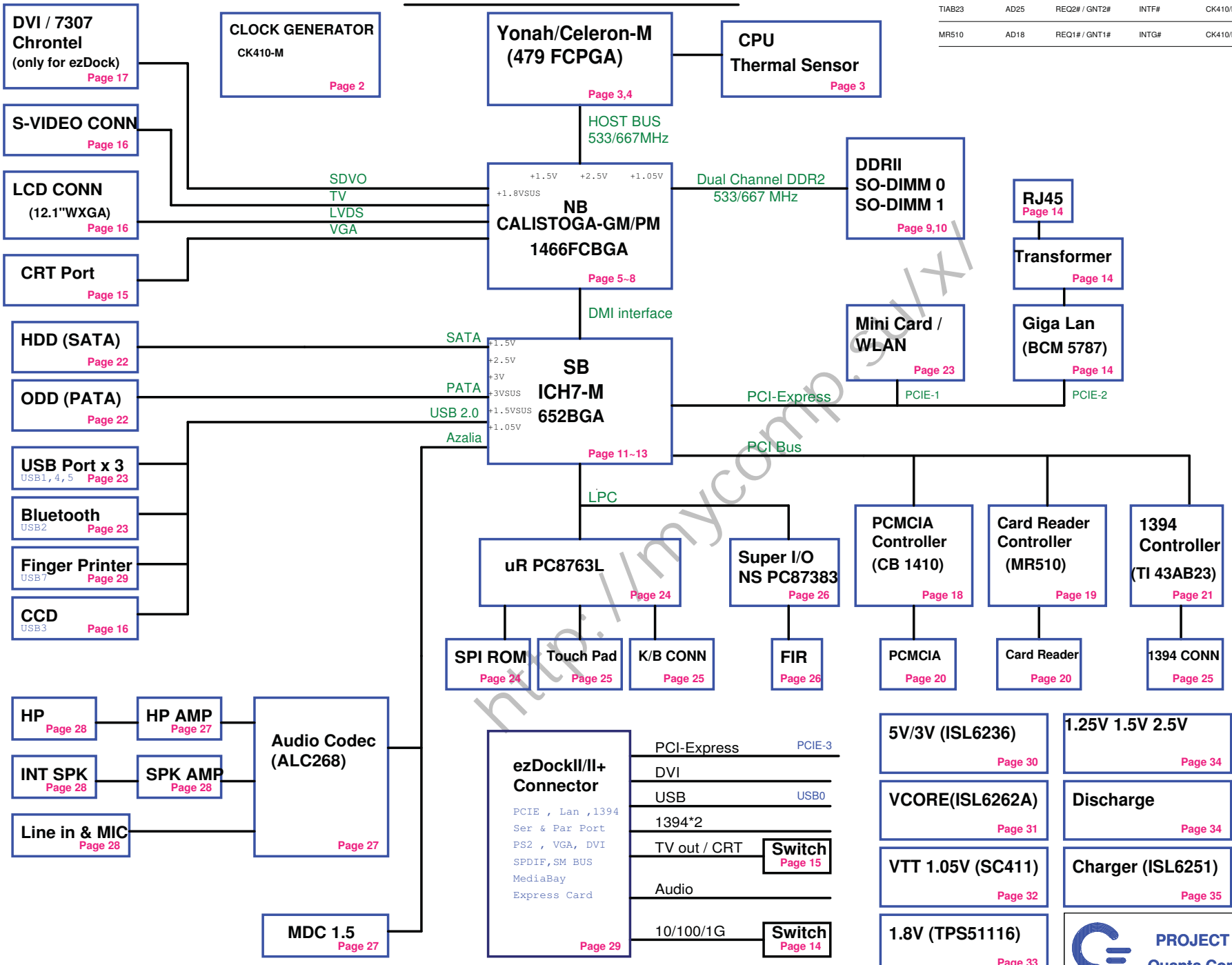


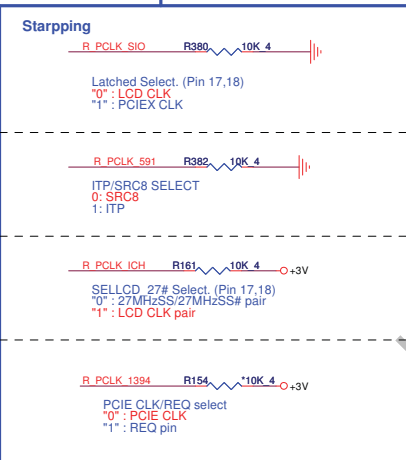
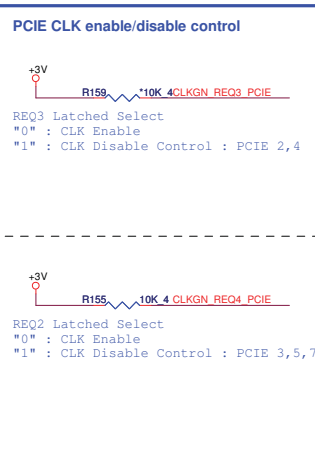
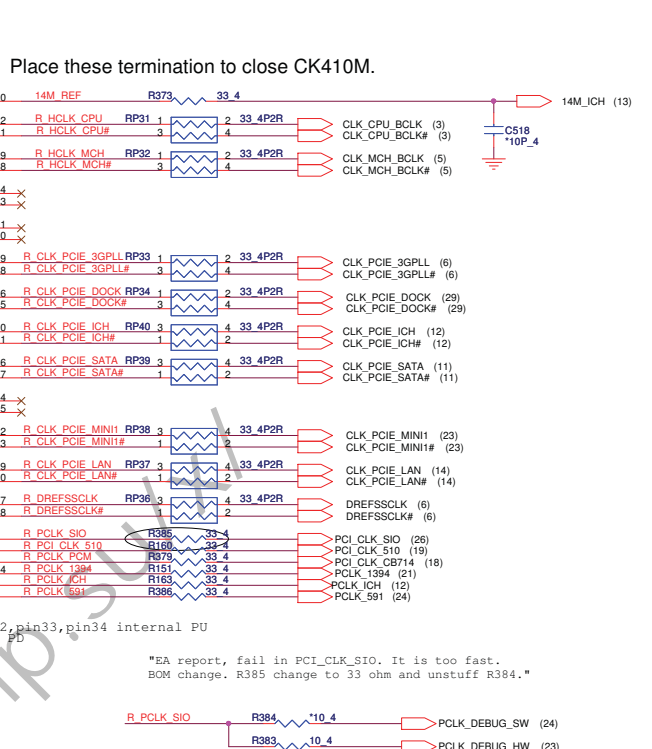
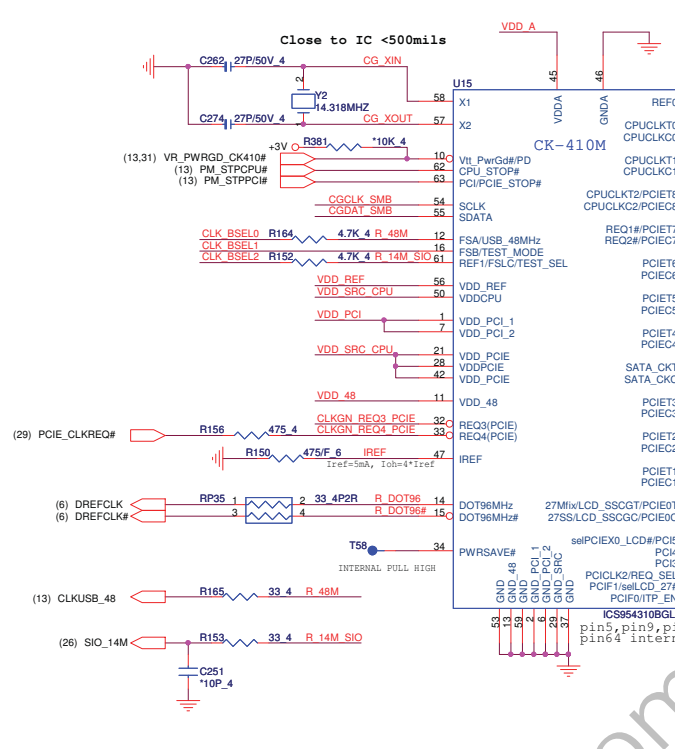
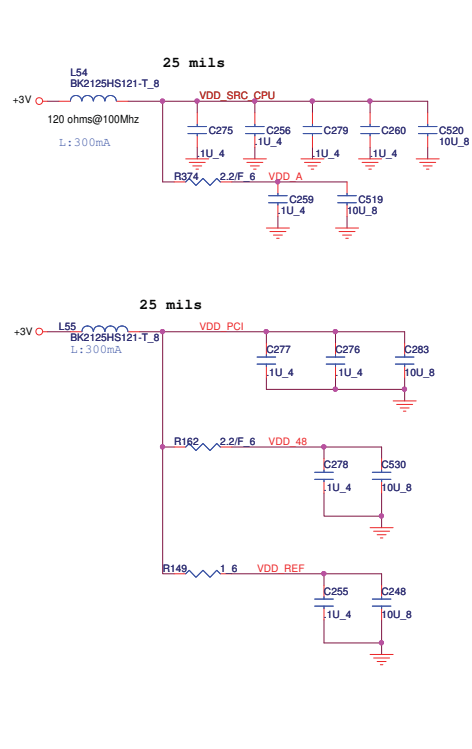
ZU2 SYSTEM BLOCK DIAGRAM

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTE#	CK410/PC13
TIAB23	AD25	REQ2# / GNT2#	INTF#	CK410/PC18
MR510	AD18	REQ1# / GNT1#	INTG#	CK410/PC14



PROJECT : ZU2
Quanta Computer Inc.

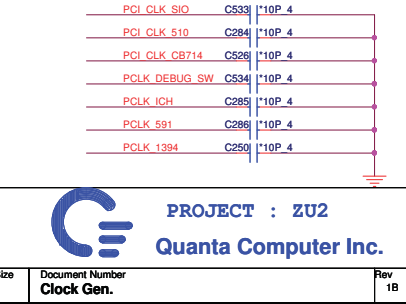
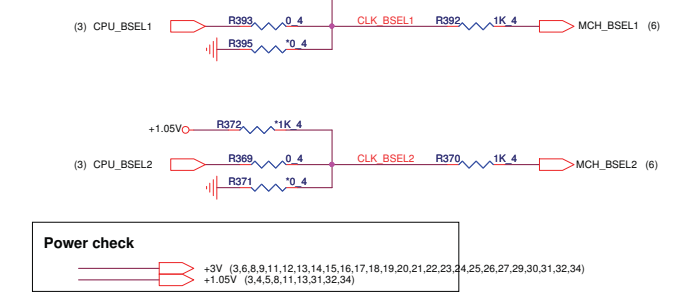
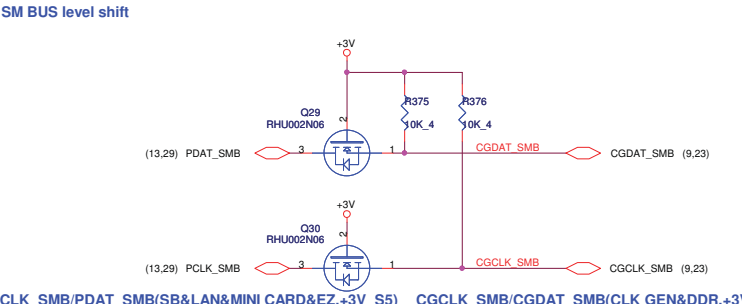
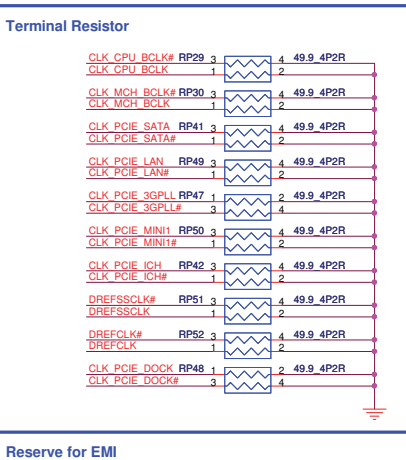
Size	Document Number	Rev
	Block Diagram	1A
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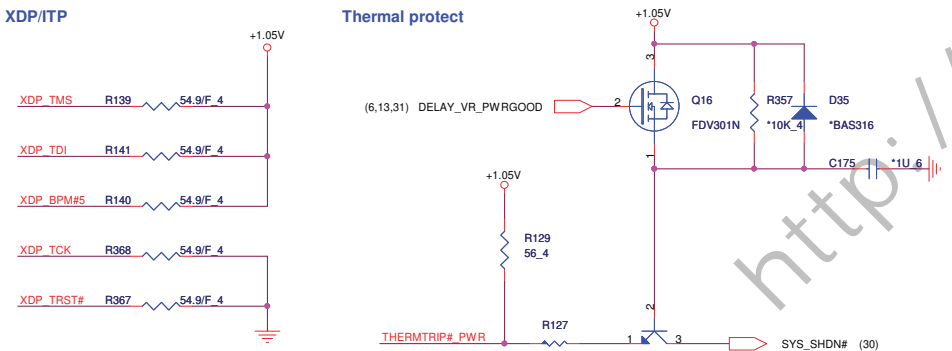
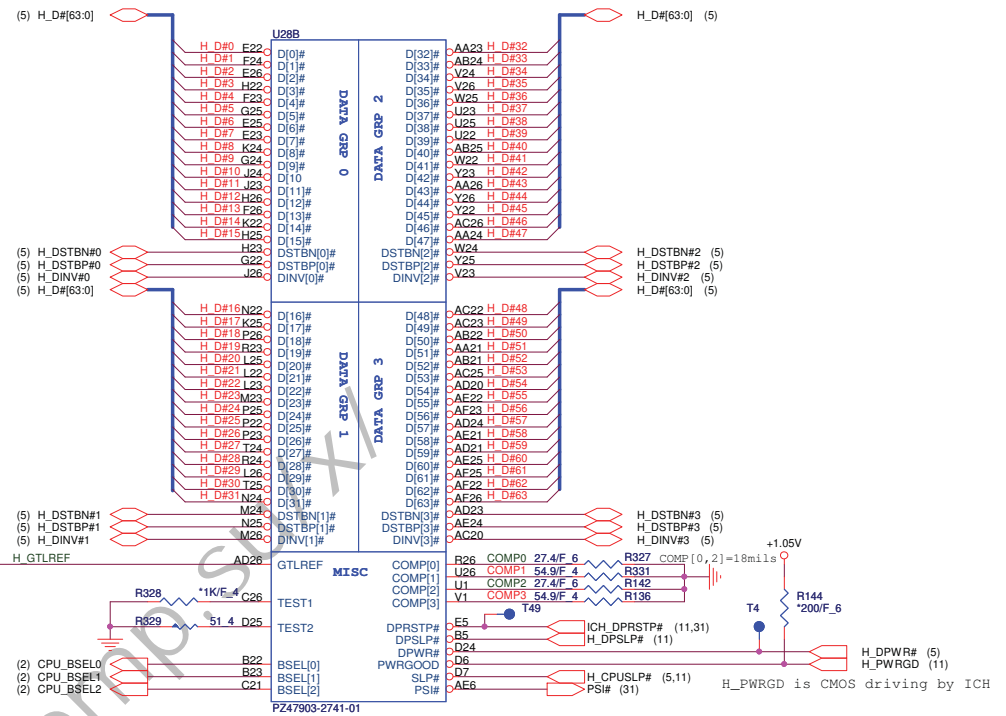
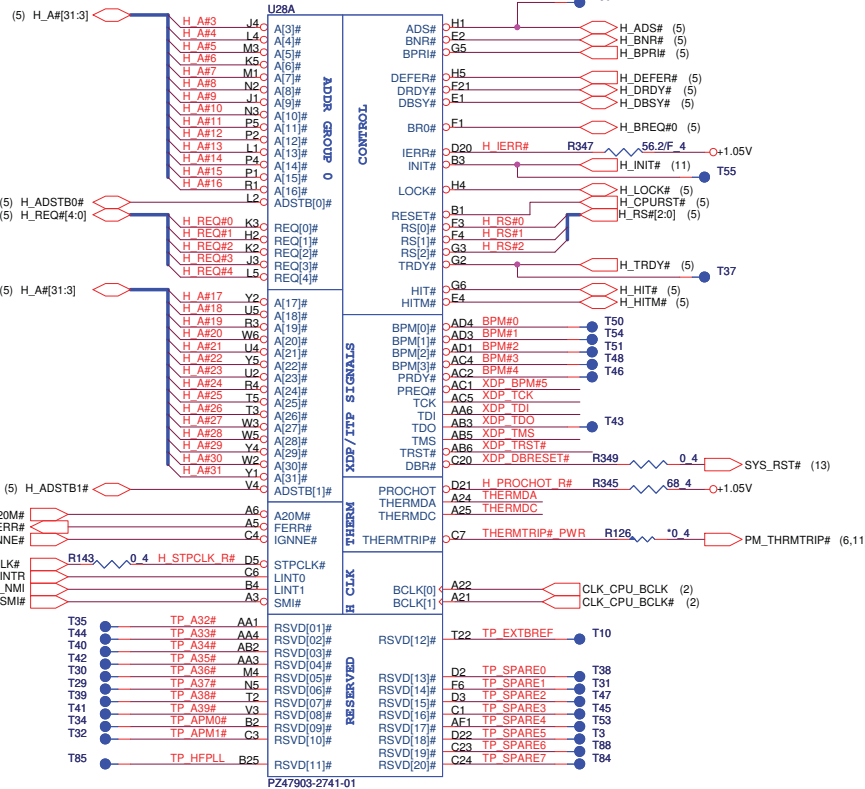


Frequency select

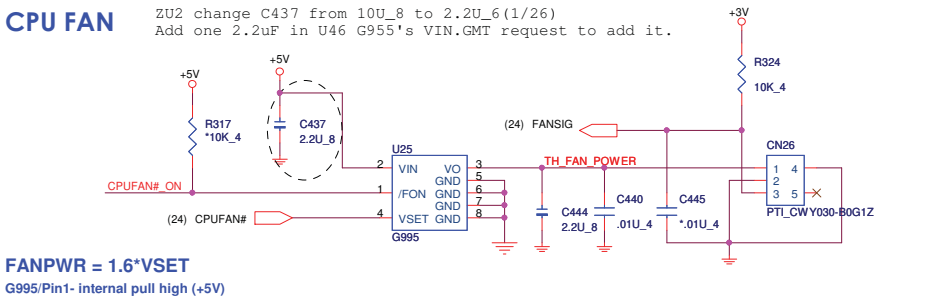
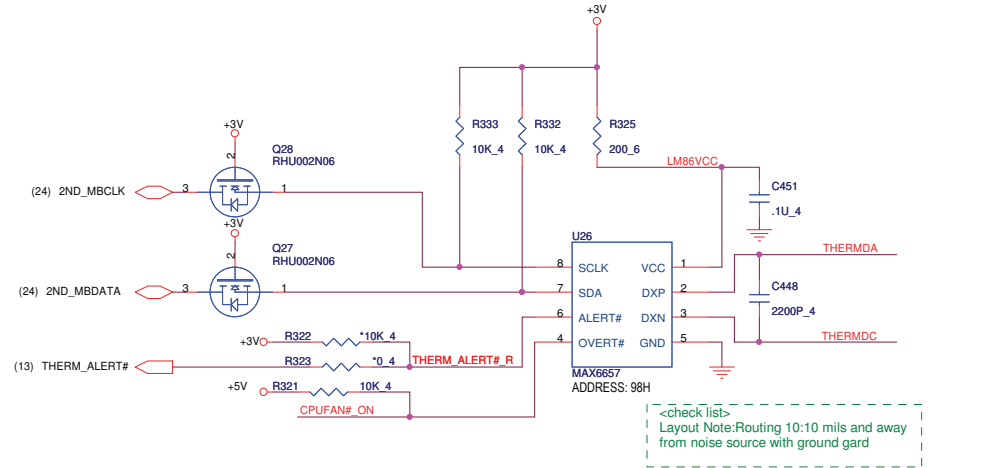
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	Default
0	0	1	133	100	33	
0	1	1	166	100	33	Default
0	1	0	200	100	33	
0	0	0	266	100	33	Default
1	0	0	333	100	33	
1	1	0	400	100	33	Default
1	1	1	200	100	33	

BSEL strappings need to be set for 533MHz Moby Dick (Intel i99150M - Callistoga Interposer) (if Callistoga is designed for 667MHz board).





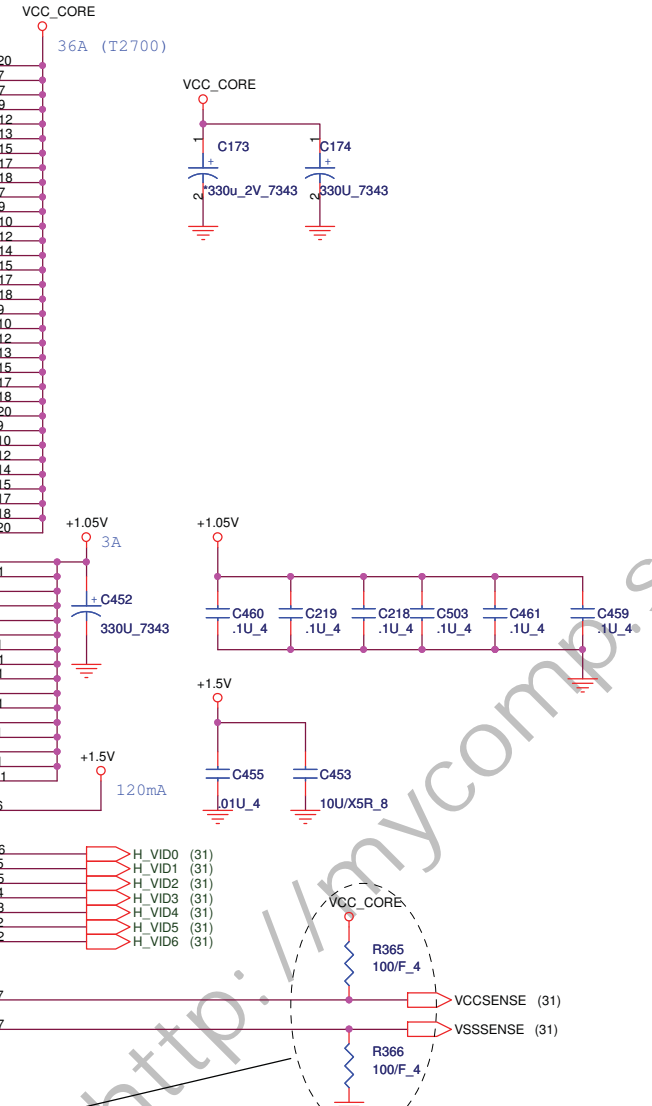
CPU Thermal monitor



PROJECT : ZU2
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U28D		VSS		P6	
A4	VSS[001]	VSS[082]	P6		
A8	VSS[002]	VSS[083]	P21		
A11	VSS[003]	VSS[084]	P24		
A14	VSS[004]	VSS[085]	R2		
A16	VSS[005]	VSS[086]	R22		
A19	VSS[006]	VSS[087]	R25		
A23	VSS[007]	VSS[088]	T1		
A26	VSS[008]	VSS[089]	T4		
B6	VSS[009]	VSS[090]	T23		
B8	VSS[010]	VSS[091]	T26		
B11	VSS[011]	VSS[092]	U3		
B13	VSS[012]	VSS[093]	U6		
B16	VSS[013]	VSS[094]	U21		
B19	VSS[014]	VSS[095]	U24		
B21	VSS[015]	VSS[096]	V2		
B24	VSS[016]	VSS[097]	V5		
C5	VSS[017]	VSS[098]	V22		
C8	VSS[018]	VSS[099]	V25		
C11	VSS[019]	VSS[100]	W1		
C14	VSS[020]	VSS[101]	W4		
C16	VSS[021]	VSS[102]	W23		
C19	VSS[022]	VSS[103]	W26		
C2	VSS[023]	VSS[104]	Y3		
C22	VSS[024]	VSS[105]	Y6		
C25	VSS[025]	VSS[106]	Y21		
D1	VSS[026]	VSS[107]	Y24		
D4	VSS[027]	VSS[108]	AA2		
D8	VSS[028]	VSS[109]	AA5		
D11	VSS[029]	VSS[110]	AA8		
D13	VSS[030]	VSS[111]	AA11		
D16	VSS[031]	VSS[112]	AA14		
D19	VSS[032]	VSS[113]	AA17		
D23	VSS[033]	VSS[114]	AA19		
D26	VSS[034]	VSS[115]	AA22		
E3	VSS[035]	VSS[116]	AA25		
E6	VSS[036]	VSS[117]	AB1		
E8	VSS[037]	VSS[118]	AB4		
E11	VSS[038]	VSS[119]	AB8		
E14	VSS[039]	VSS[120]	AB11		
E16	VSS[040]	VSS[121]	AB13		
E19	VSS[041]	VSS[122]	AB16		
E21	VSS[042]	VSS[123]	AB19		
E24	VSS[043]	VSS[124]	AB23		
F5	VSS[044]	VSS[125]	AB26		
F8	VSS[045]	VSS[126]	AC3		
F11	VSS[046]	VSS[127]	AC6		
F13	VSS[047]	VSS[128]	AC8		
F16	VSS[048]	VSS[129]	AC11		
F19	VSS[049]	VSS[130]	AC14		
F2	VSS[050]	VSS[131]	AC16		
F22	VSS[051]	VSS[132]	AC19		
F25	VSS[052]	VSS[133]	AC21		
G4	VSS[053]	VSS[134]	AC24		
G1	VSS[054]	VSS[135]	AD2		
G23	VSS[055]	VSS[136]	AD5		
G26	VSS[056]	VSS[137]	AD8		
H3	VSS[057]	VSS[138]	AD11		
H6	VSS[058]	VSS[139]	AD13		
H21	VSS[059]	VSS[140]	AD16		
H24	VSS[060]	VSS[141]	AD19		
J2	VSS[061]	VSS[142]	AD22		
J5	VSS[062]	VSS[143]	AD25		
J22	VSS[063]	VSS[144]	AD25		
J25	VSS[064]	VSS[145]	AE1		
K1	VSS[065]	VSS[146]	AE4		
K4	VSS[066]	VSS[147]	AE8		
K23	VSS[067]	VSS[148]	AE11		
K26	VSS[068]	VSS[149]	AE14		
L3	VSS[069]	VSS[150]	AE16		
L6	VSS[070]	VSS[151]	AE19		
L21	VSS[071]	VSS[152]	AE23		
L24	VSS[072]	VSS[153]	AE26		
M2	VSS[073]	VSS[154]	AF3		
M5	VSS[074]	VSS[155]	AF6		
M22	VSS[075]	VSS[156]	AF8		
M25	VSS[076]	VSS[157]	AF11		
N1	VSS[077]	VSS[158]	AF13		
N4	VSS[078]	VSS[159]	AF16		
N23	VSS[079]	VSS[160]	AF19		
N26	VSS[080]	VSS[161]	AF21		
P3	VSS[081]	VSS[162]	AF24		

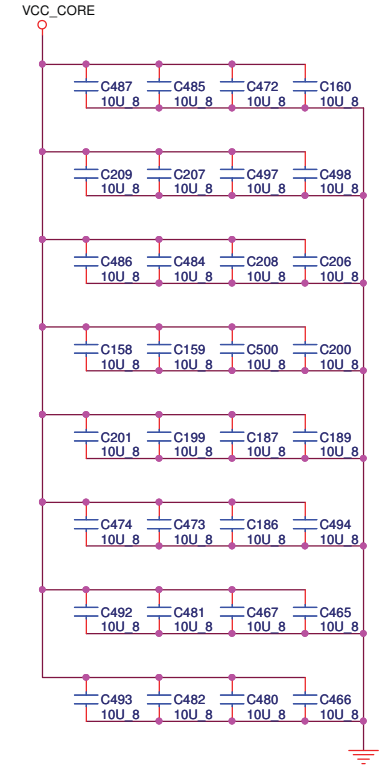
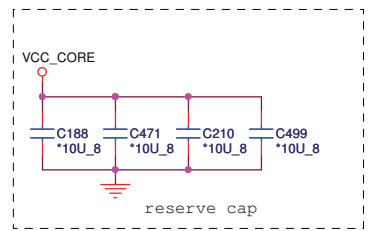
VCC_CORE		U28C		VCC_CORE	
A7	VCC[001]	VCC[68]	AB20	36A (T2700)	
A9	VCC[002]	VCC[69]	AB7		
A10	VCC[003]	VCC[70]	AC7		
A12	VCC[004]	VCC[71]	AC9		
A13	VCC[005]	VCC[72]	AC12		
A15	VCC[006]	VCC[73]	AC13		
A17	VCC[007]	VCC[74]	AC15		
A18	VCC[008]	VCC[75]	AC17		
A20	VCC[009]	VCC[76]	AC18		
B7	VCC[010]	VCC[77]	AD7		
B9	VCC[011]	VCC[78]	AD9		
B10	VCC[012]	VCC[79]	AD10		
B12	VCC[013]	VCC[80]	AD12		
B14	VCC[014]	VCC[81]	AD14		
B15	VCC[015]	VCC[82]	AD15		
B17	VCC[016]	VCC[83]	AD17		
B18	VCC[017]	VCC[84]	AD18		
B20	VCC[018]	VCC[85]	AE9		
C9	VCC[019]	VCC[86]	AE10		
C10	VCC[020]	VCC[87]	AE12		
C12	VCC[021]	VCC[88]	AE13		
C13	VCC[022]	VCC[89]	AE15		
C15	VCC[023]	VCC[90]	AE17		
C17	VCC[024]	VCC[91]	AE18		
C18	VCC[025]	VCC[92]	AE20		
D9	VCC[026]	VCC[93]	AE9		
D10	VCC[027]	VCC[94]	AE10		
D12	VCC[028]	VCC[95]	AE12		
D14	VCC[029]	VCC[96]	AE14		
D15	VCC[030]	VCC[97]	AE15		
D17	VCC[031]	VCC[98]	AE17		
D18	VCC[032]	VCC[99]	AE18		
E7	VCC[033]	VCC[100]	AE20		
E9	VCC[034]				
E10	VCC[035]	VCCP[01]	V6		
E12	VCC[036]	VCCP[02]	G21		
E13	VCC[037]	VCCP[03]	J6		
E15	VCC[038]	VCCP[04]	K6		
E17	VCC[039]	VCCP[05]	M6		
E18	VCC[040]	VCCP[06]	J21		
E19	VCC[041]	VCCP[07]	K21		
F7	VCC[042]	VCCP[08]	M21		
F9	VCC[043]	VCCP[09]	N21		
F10	VCC[044]	VCCP[10]	N6		
F12	VCC[045]	VCCP[11]	R21		
F14	VCC[046]	VCCP[12]	R6		
F15	VCC[047]	VCCP[13]	T21		
F17	VCC[048]	VCCP[14]	T6		
F18	VCC[049]	VCCP[15]	V21		
F20	VCC[050]	VCCP[16]	W21		
AA7	VCC[051]				
AA9	VCC[052]				
AA10	VCC[053]				
AA12	VCC[054]				
AA13	VCC[055]				
AA15	VCC[056]				
AA17	VCC[057]				
AA18	VCC[058]				
AA20	VCC[059]				
AB9	VCC[060]				
AC10	VCC[061]				
AB10	VCC[062]				
AB12	VCC[063]				
AB14	VCC[064]				
AB15	VCC[065]	VCCSENSE	AE7		
AB17	VCC[066]	VSSSENSE	AE7		
AB18	VCC[067]				



Add 100_F PU on VCCSENSE.
 Add 100_F PD on VSSSENSE.
 Check intel circuit by Alan(1/26)

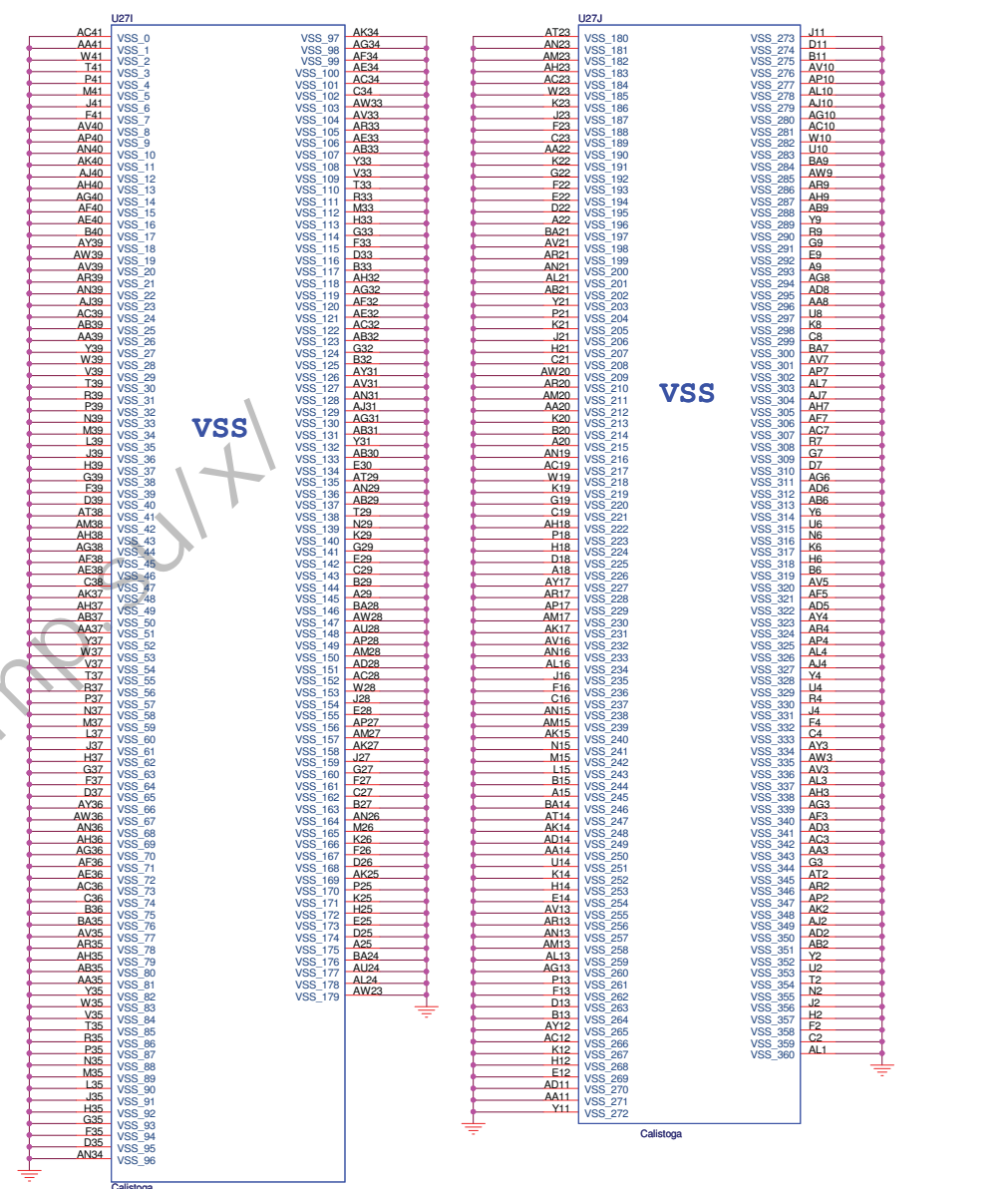
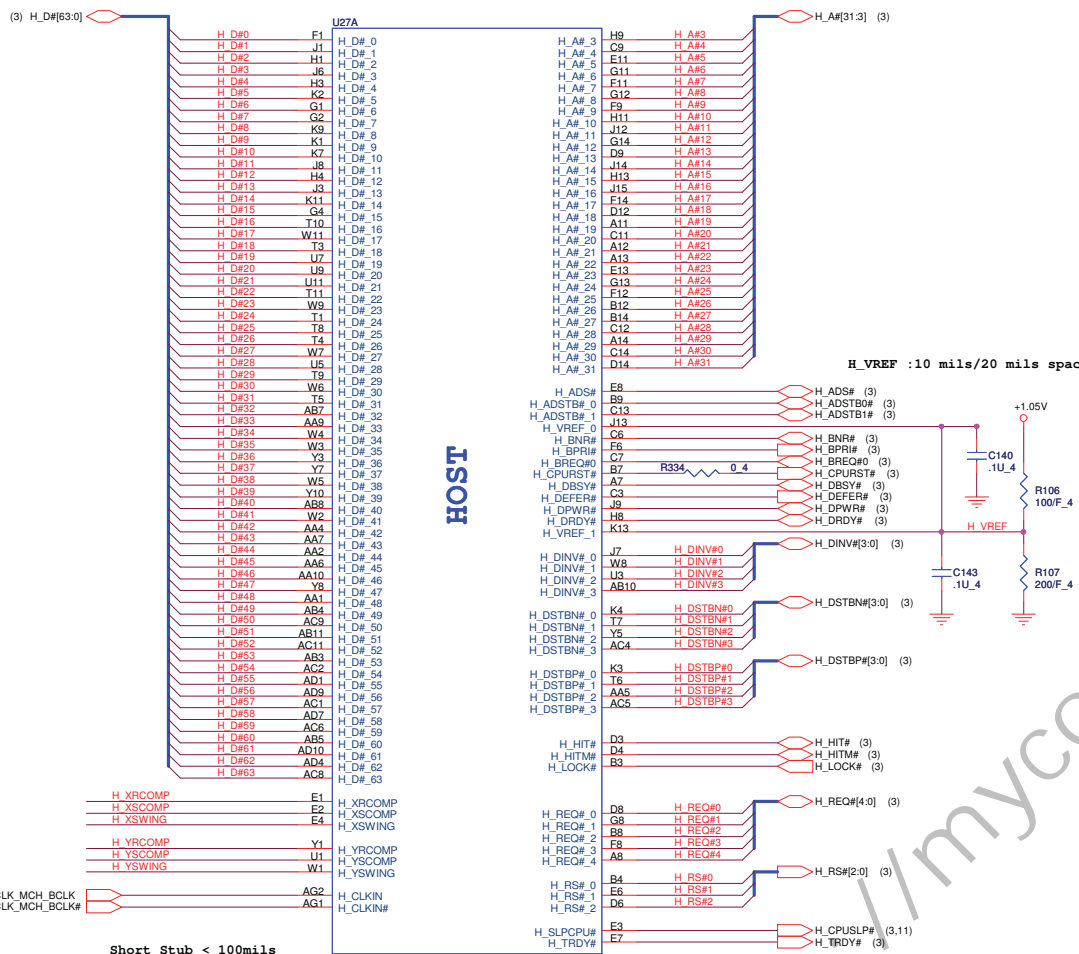
+1.05V → +1.05V (2,3,5,8,11,13,31,32,34)
 VCC_CORE → VCC_CORE (31)
 +1.5V → +1.5V (8,12,13,23,27,34)

VCC_CORE CAP.

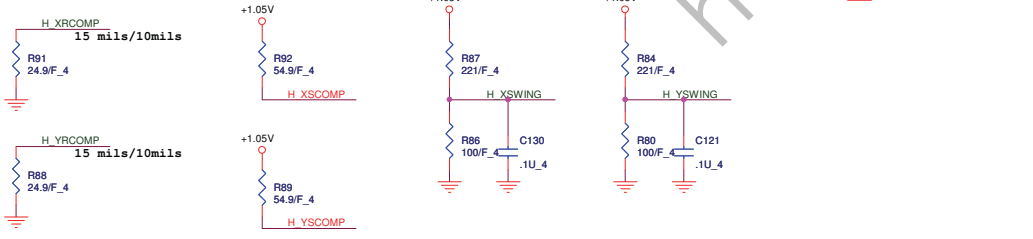


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Quanta Computer Inc.

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	Yonah/Merom CPU(Power/GND)-2	1A
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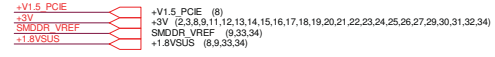
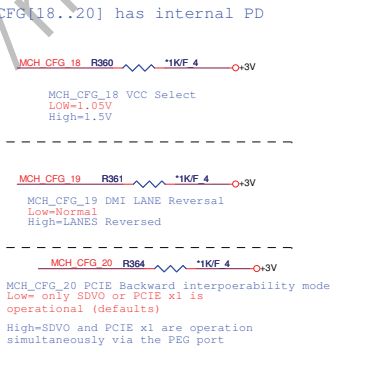
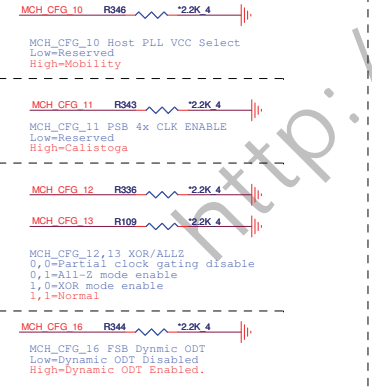
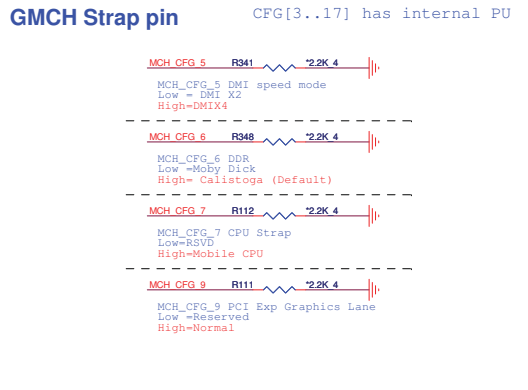
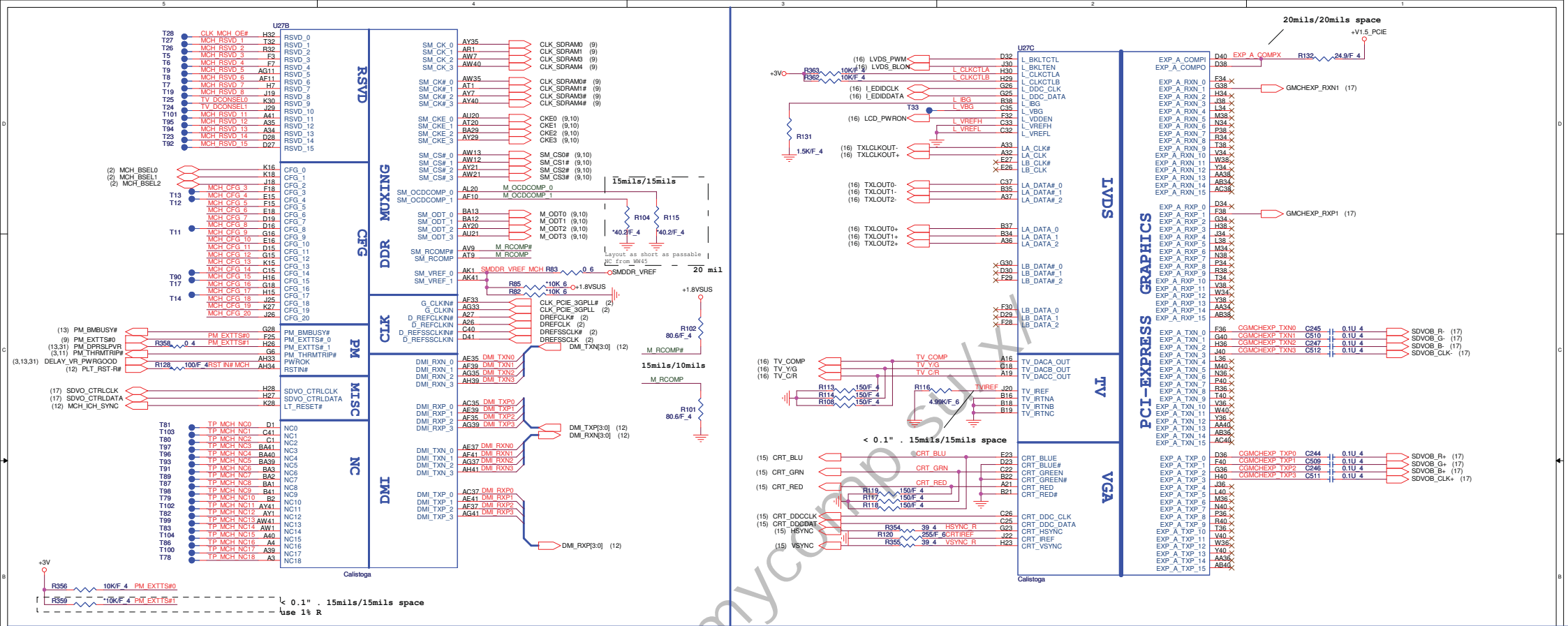
Slew/IO Buffer COMP.



COMPONENTS	P/N
945GM	AJSL8Z20T25
ICH7-M	AJSL8YB0T21

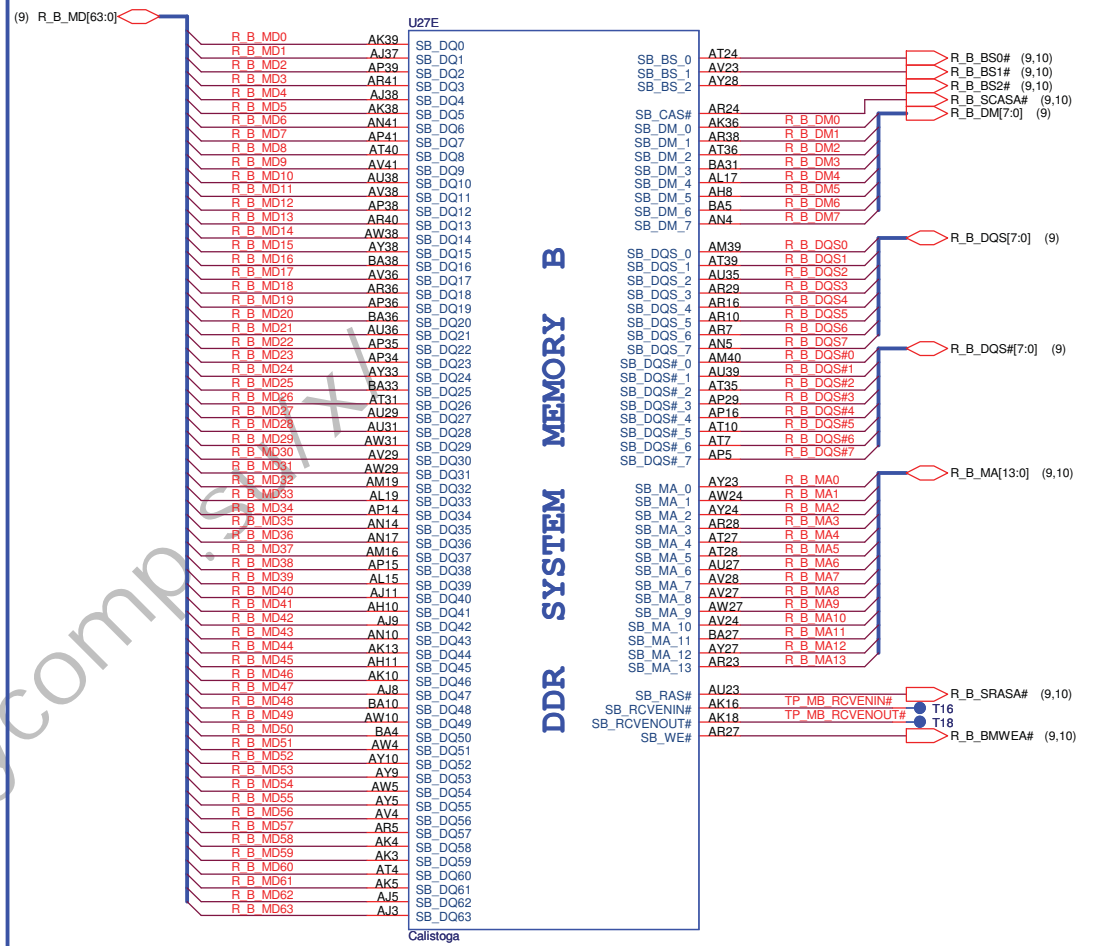
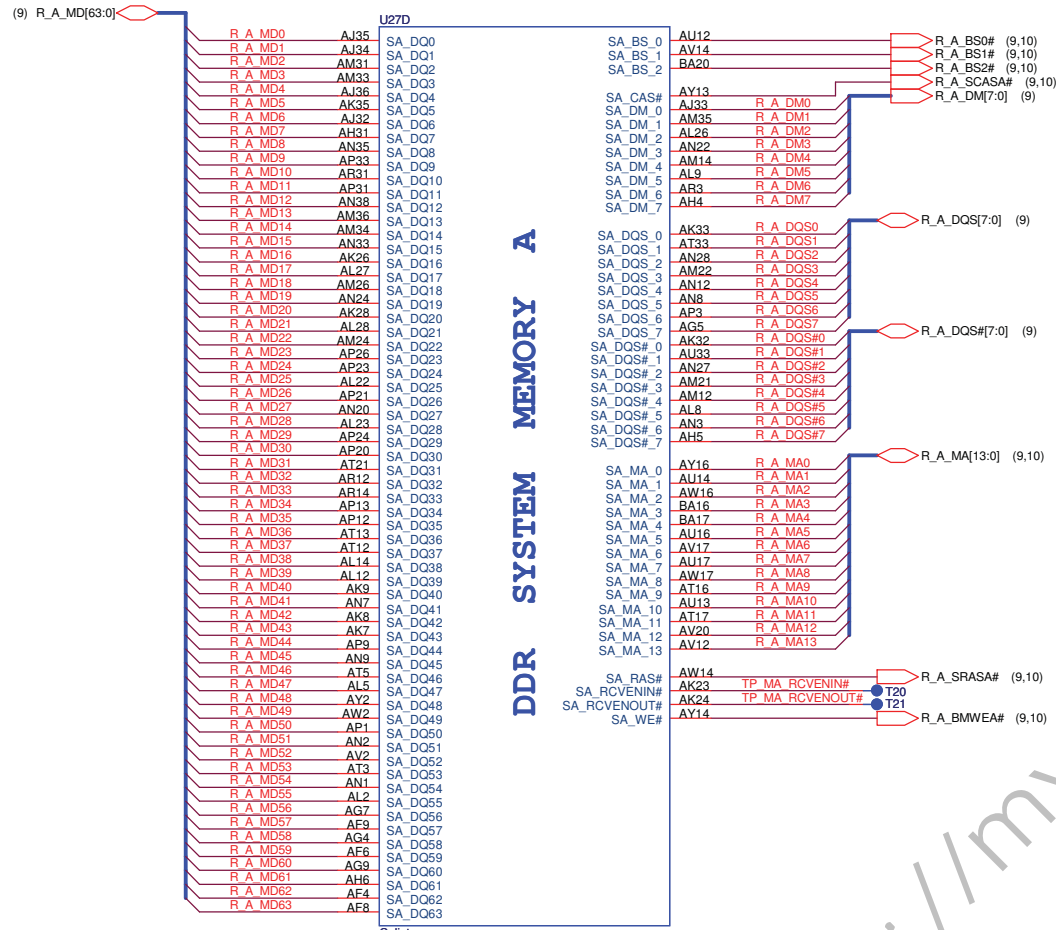
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Quanta Computer Inc.

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Quanta Computer Inc.

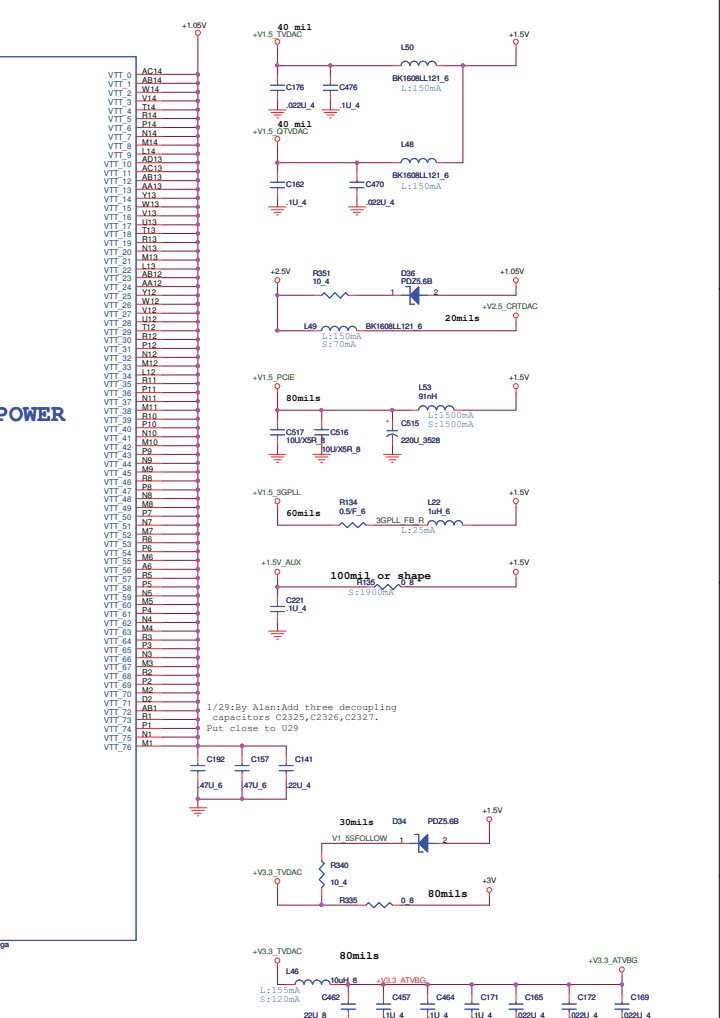
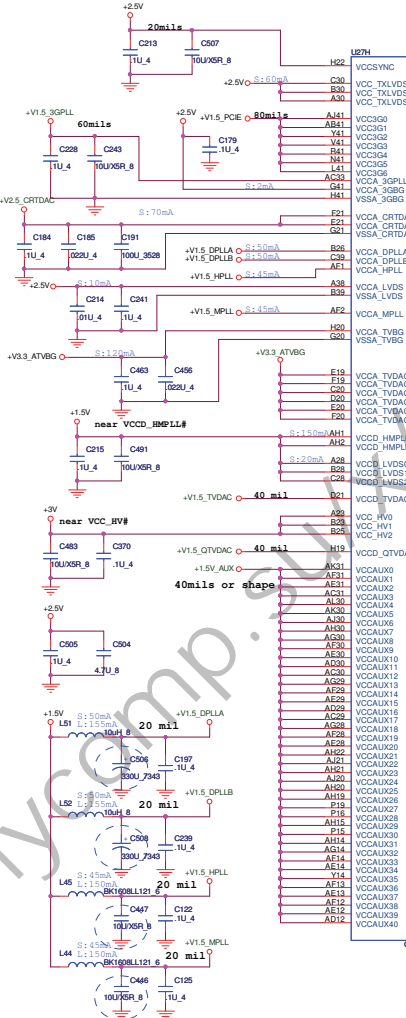
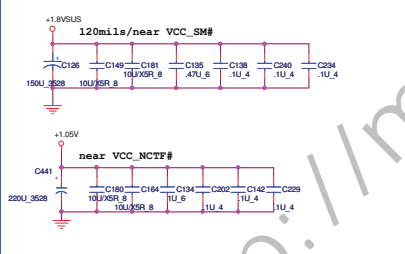
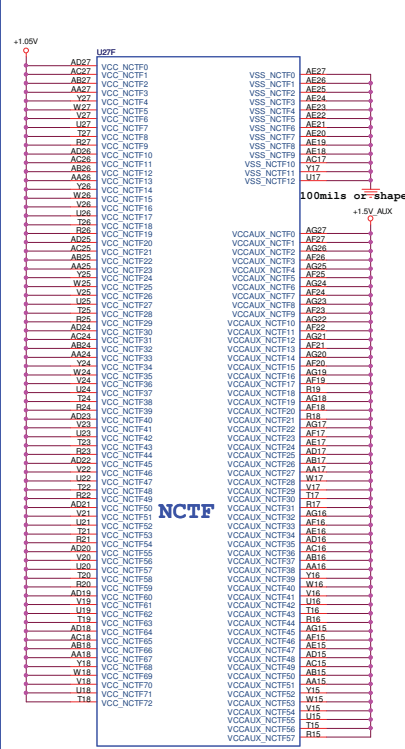
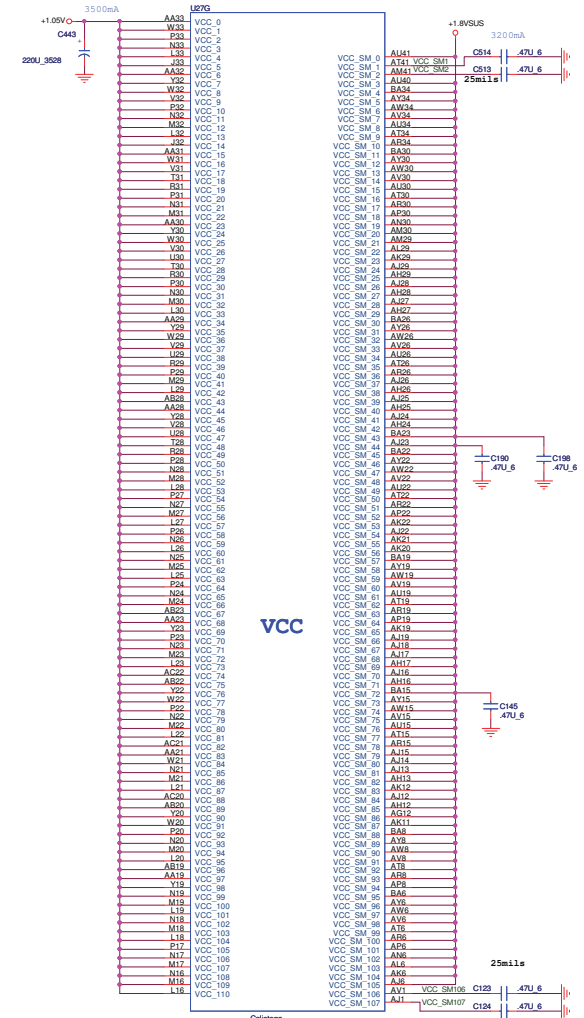
Size	Document Number	Rev
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http://mycomp.com

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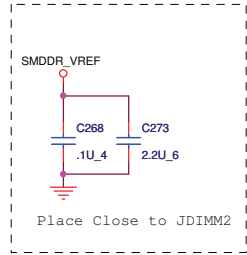
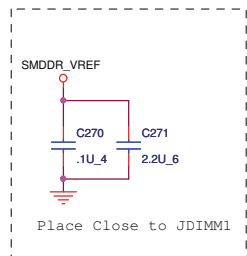
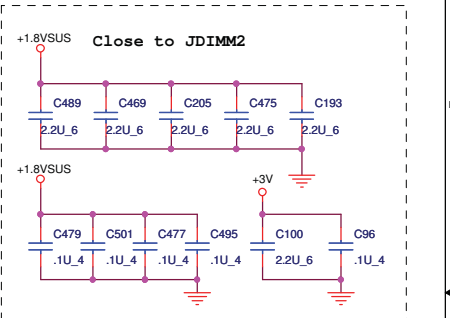
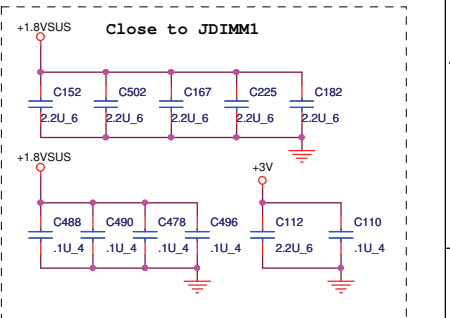
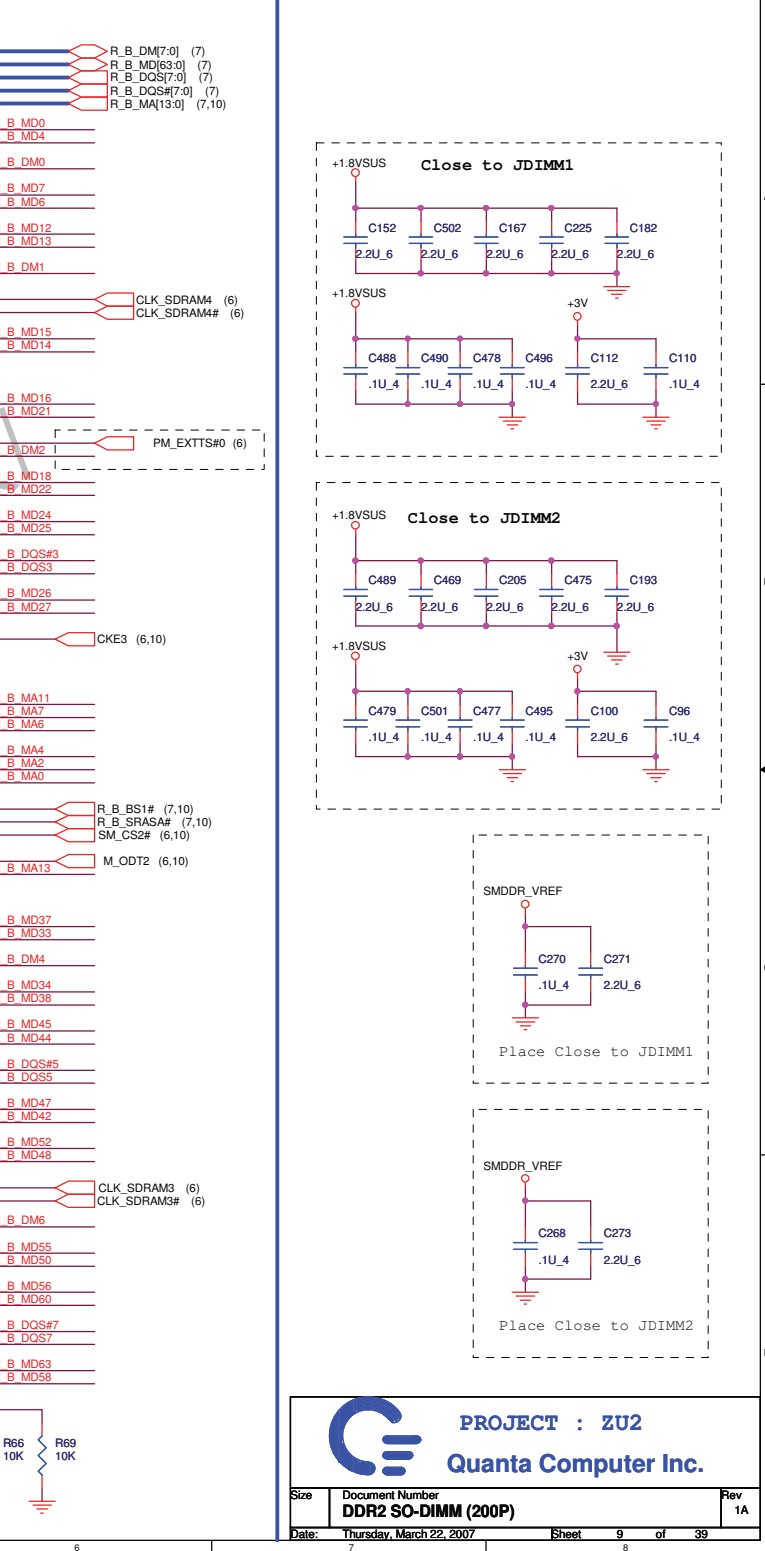
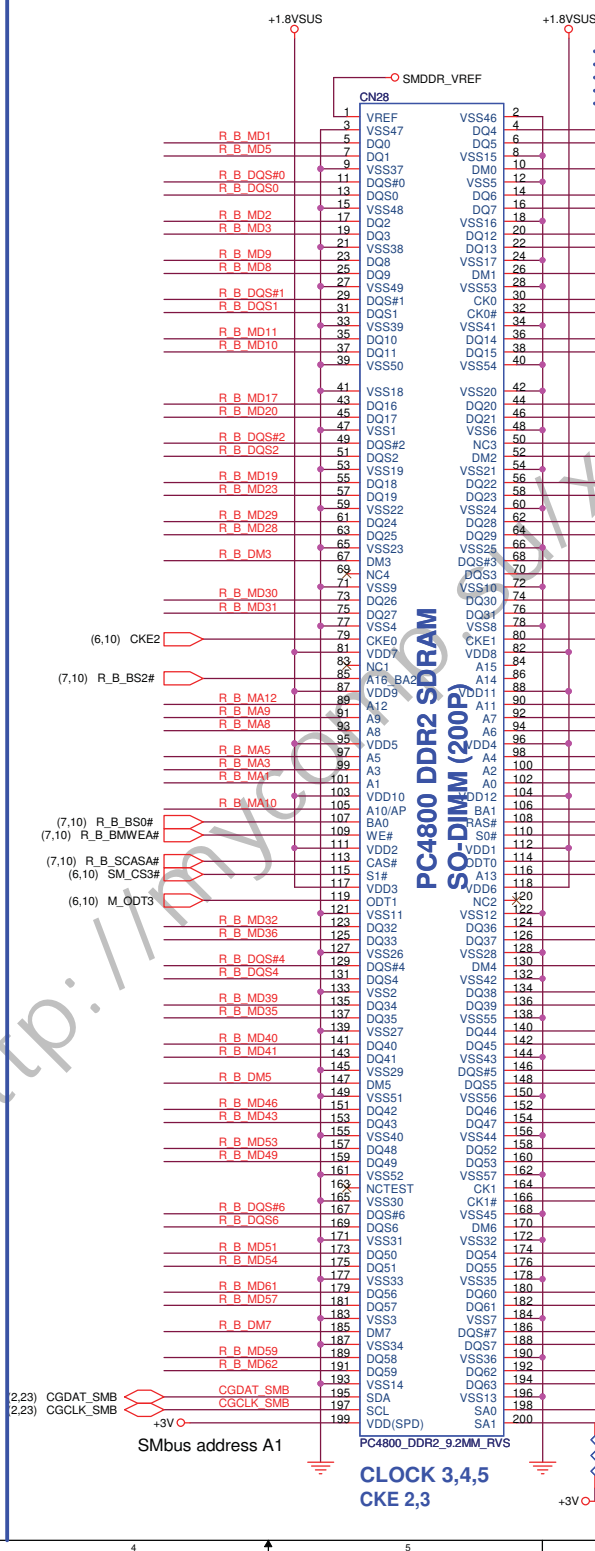
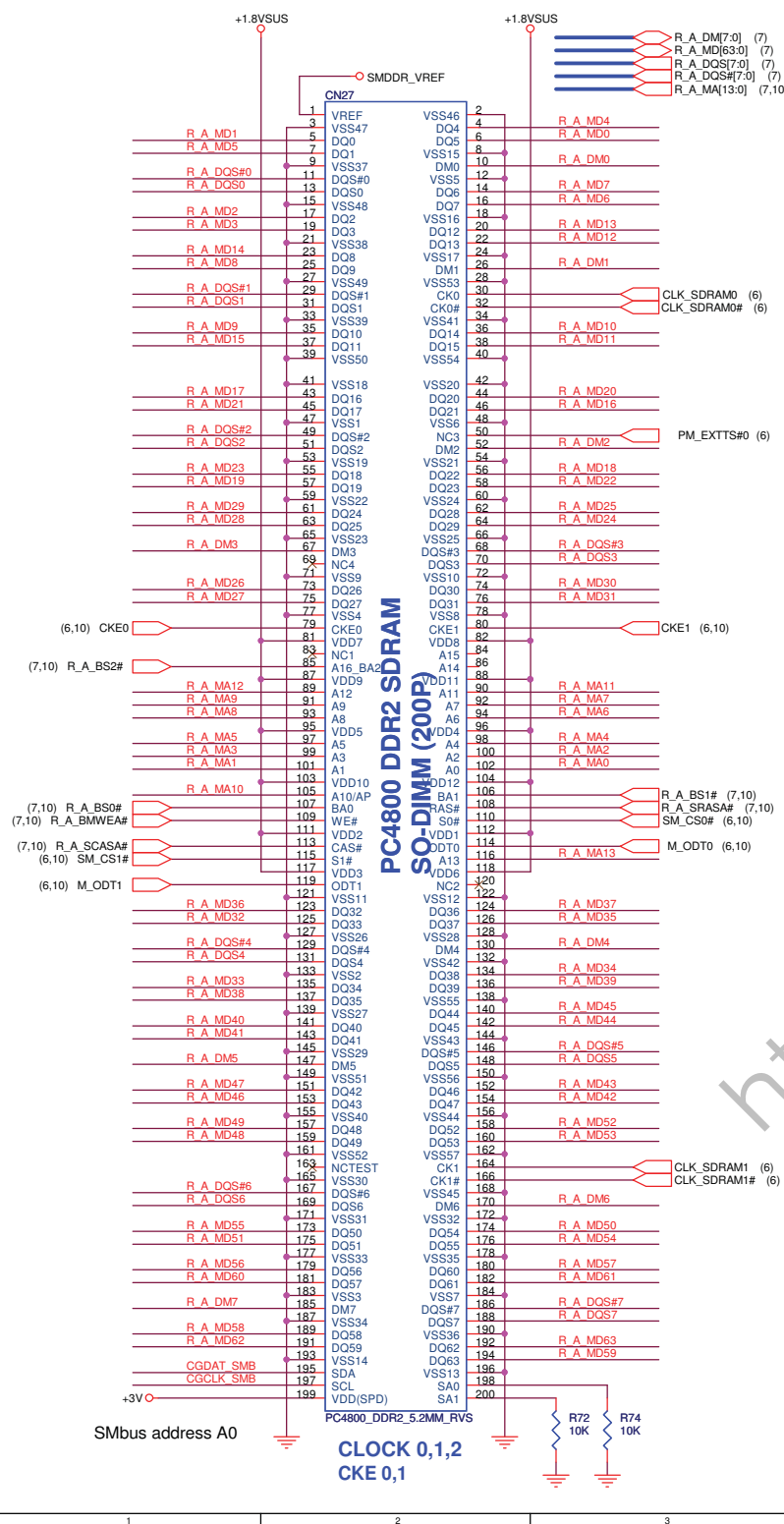


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Quanta Computer Inc.

Rev 1A

Document Number: **GMCH (POWER)**

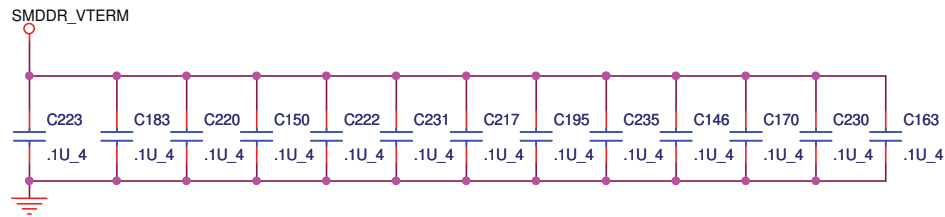
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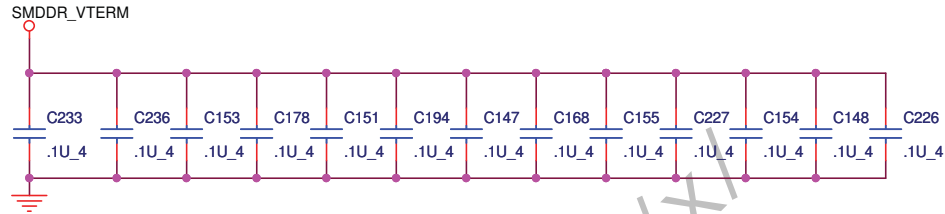
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Quanta Computer Inc.

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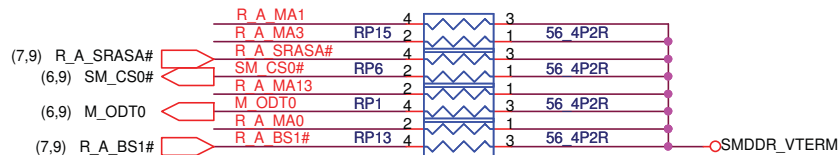
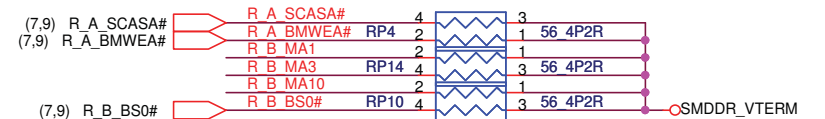
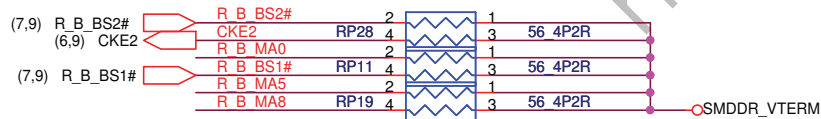
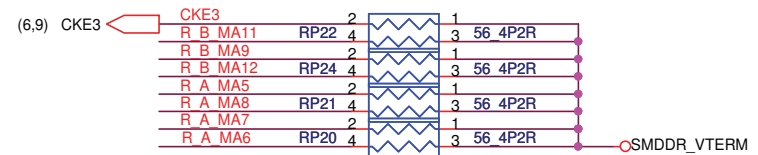
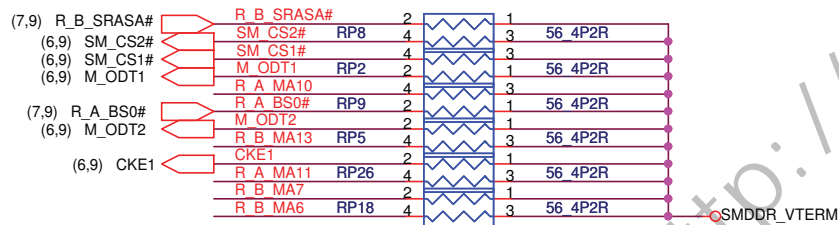
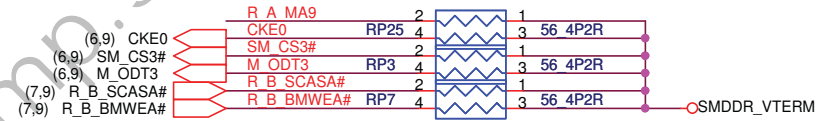
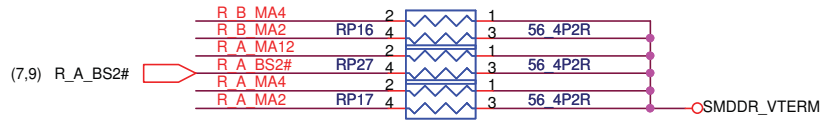
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM

R_A_MA[0..13] (7,9)

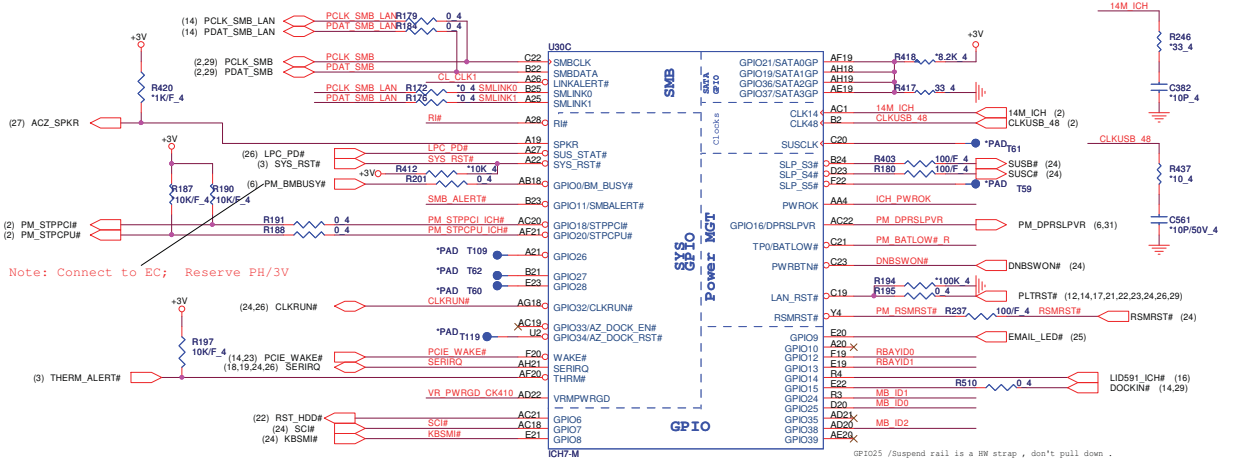
R_B_MA[0..13] (7,9)



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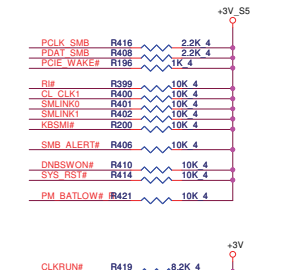
1/31: ASF issue, to support slave mode



Note: Connect to EC; Reserve PH/3V

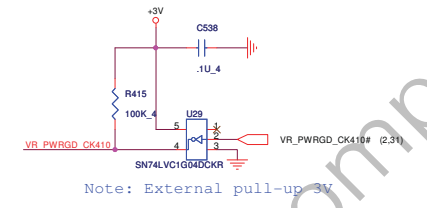
GPIO25 / suspend rail is a MW strap, don't pull down.

ICH PWROK

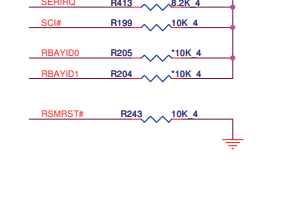


(3,6,31) DELAY_VR_PWRGOOD (24) PWROK_EC

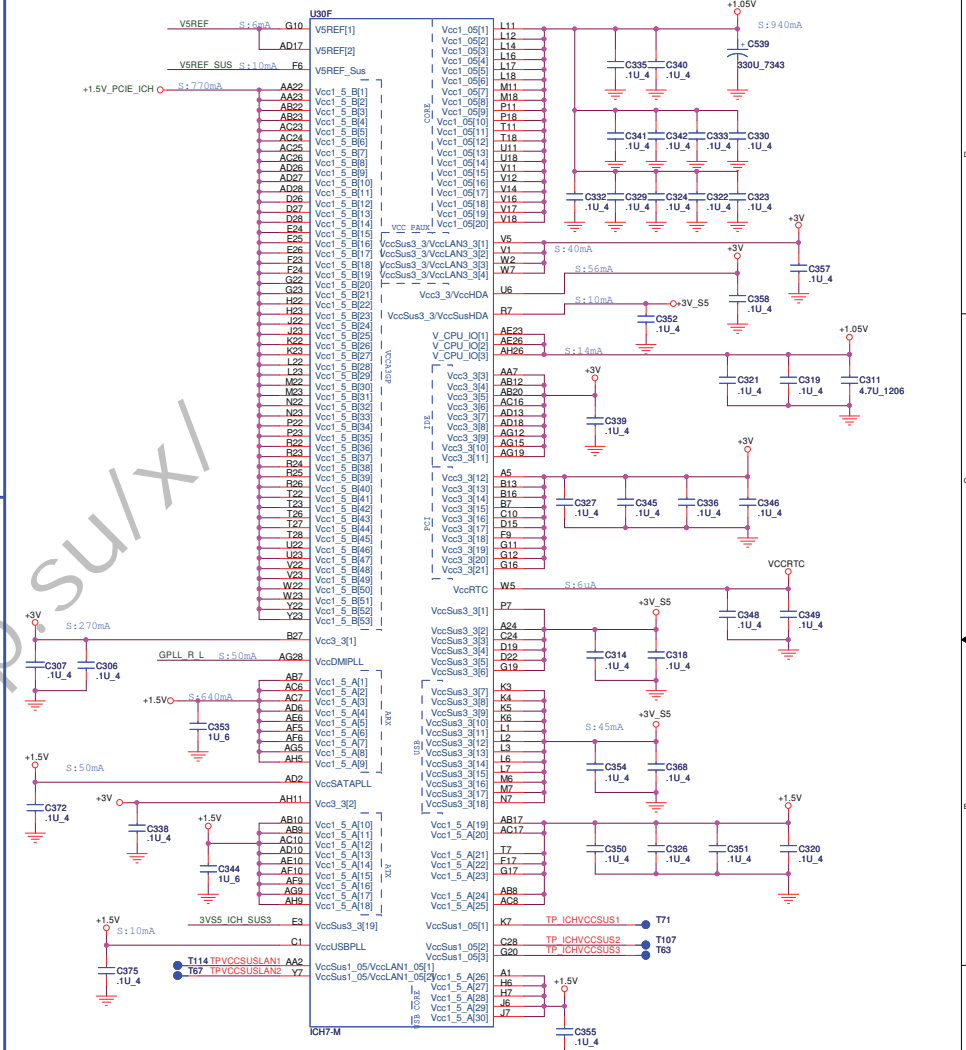
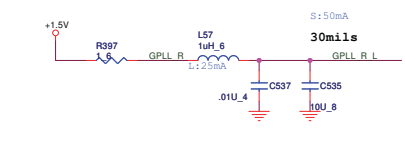
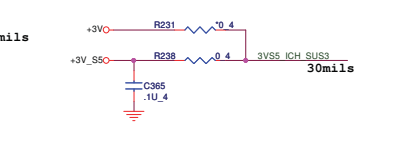
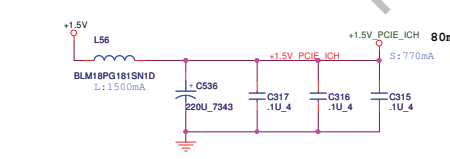
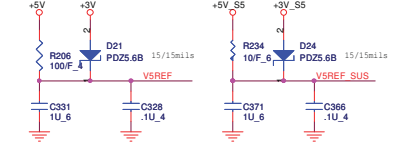
VR PWROK



M/B ID Select



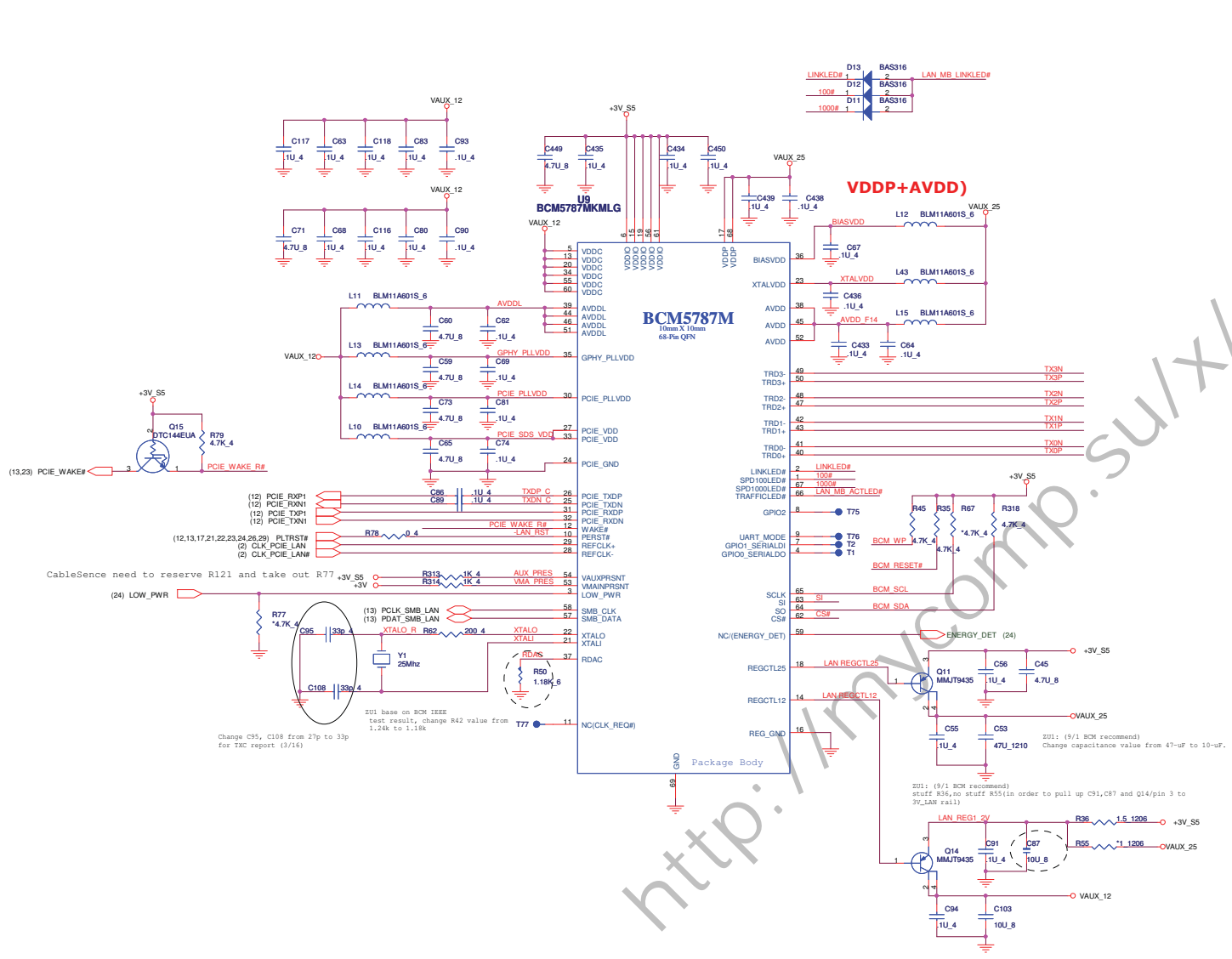
MB_ID2 MB_ID1 MB_ID0 MB_TYPE



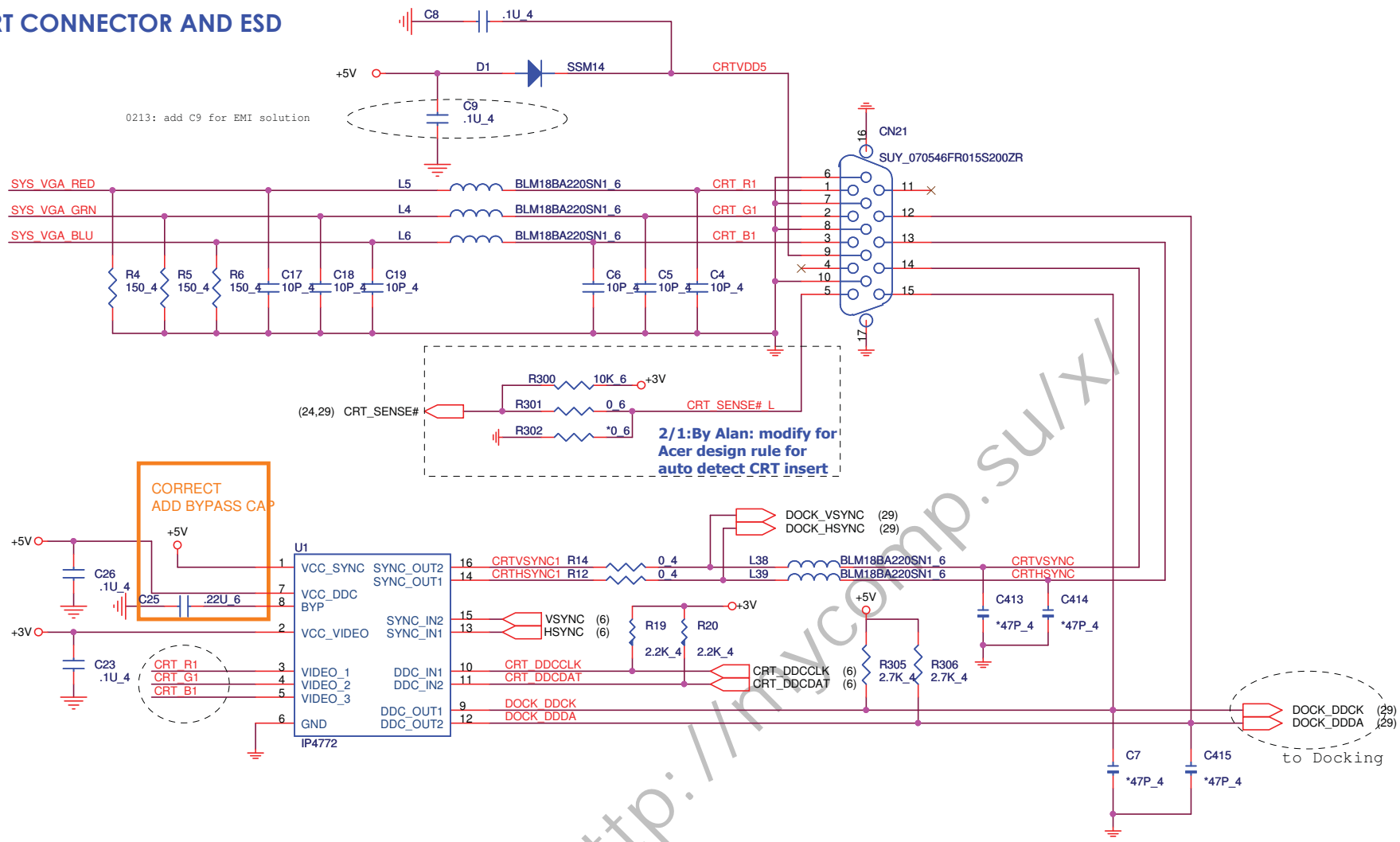
PROJECT : ZU2
Quanta Computer Inc.

Size: Document Number: ICH7-M (POWER & GND) Rev: 1B
 Date: Thursday, March 22, 2007 Sheet: 13 of 39

Giga LAN BCM5787M



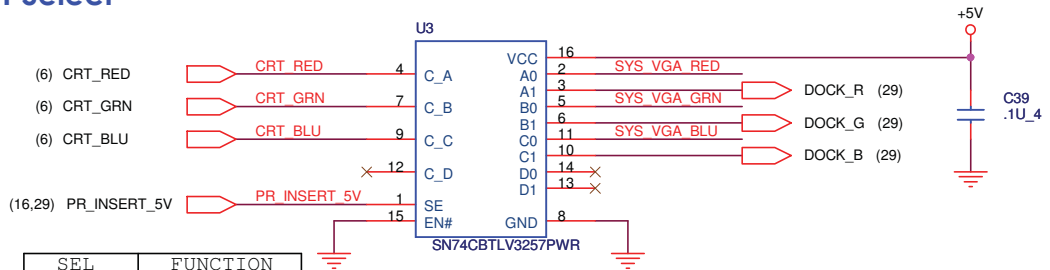
CRT CONNECTOR AND ESD




**CORRECT
ADD BYPASS CAP**

2/1:By Alan: modify for
Acer design rule for
auto detect CRT insert

CRT Select



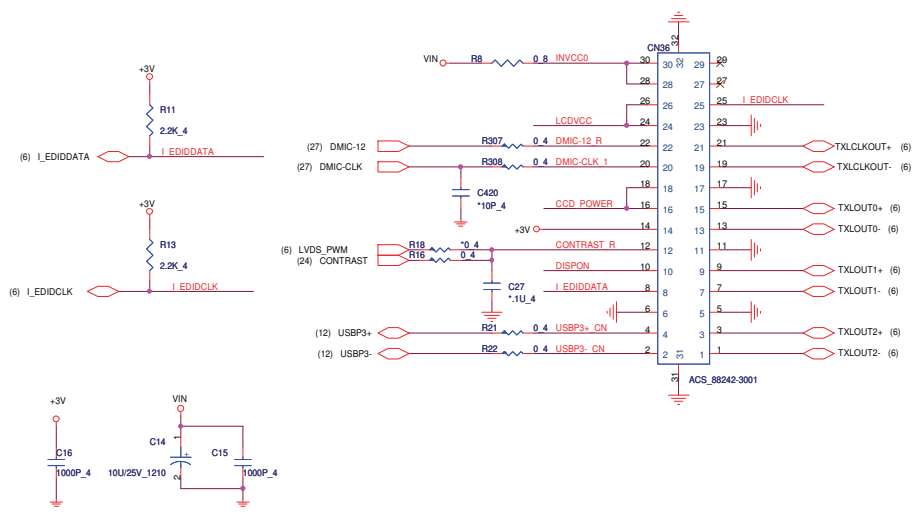
SEL	FUNCTION
LOW	IN_0
HIGH	IN_1



PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	CRT	1A
Date:	Thursday, March 22, 2007	Sheet 15 of 39

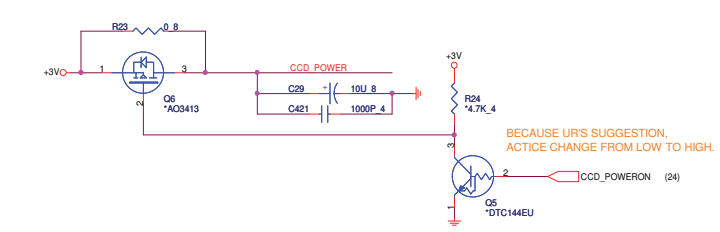
LVDS



ZU1:(12/28) EMI request: reserve L-C footprint for debug use (R52,C650)

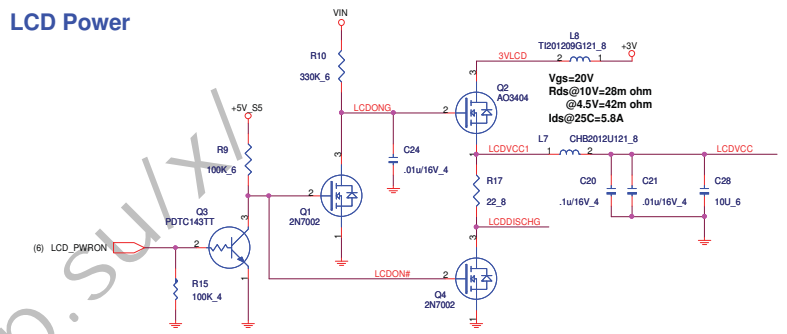
(3/19)Change MB LCD connector pin define(CN3) and LCD cable pin define to cover production line issue (Inverter short with signal to burn system)->ZR1 issue
 (1)pin 27,29->NC
 (2)pin 8->INT_LVDS_EDIDDATA

CAMERA MODULE



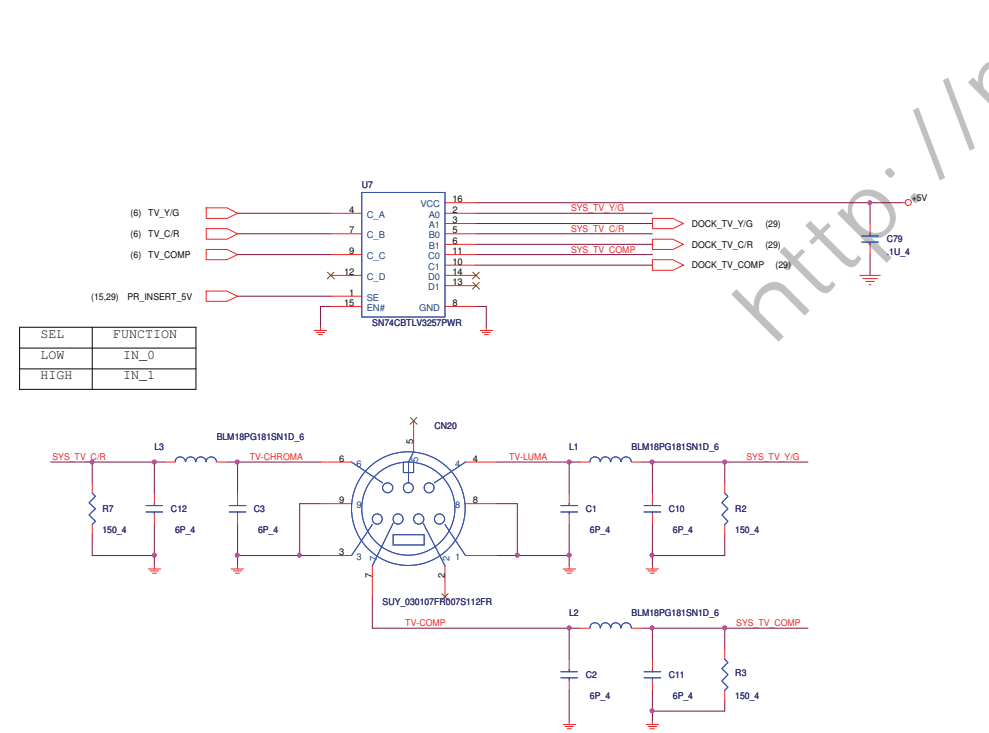
BECAUSE UR'S SUGGESTION, ACTICE CHANGE FROM LOW TO HIGH.

LCD Power



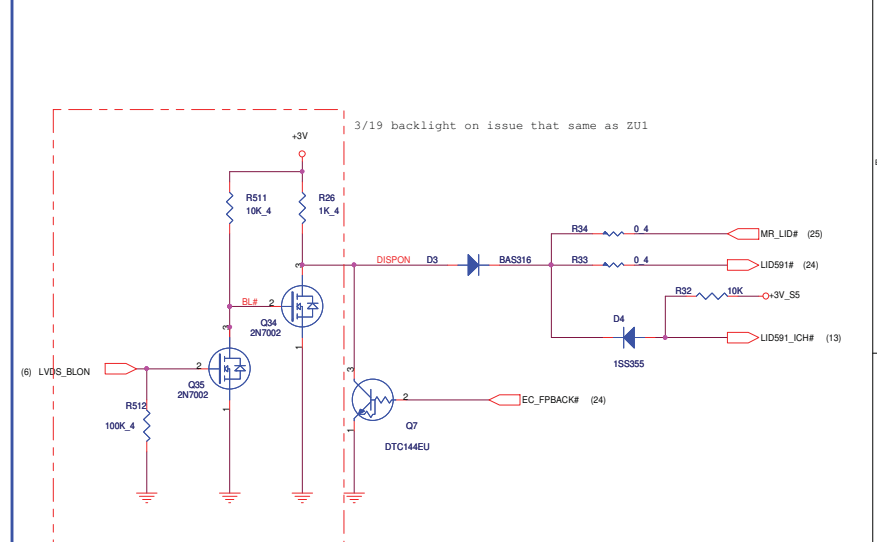
1/29:By Alan: AAT4280 fail on power ON rising time and falling time. EA.Additionally, some LCD panels will have garbage. follow ZR1 circuit.

TV Out (SVHS) MiniDIN 7-pin

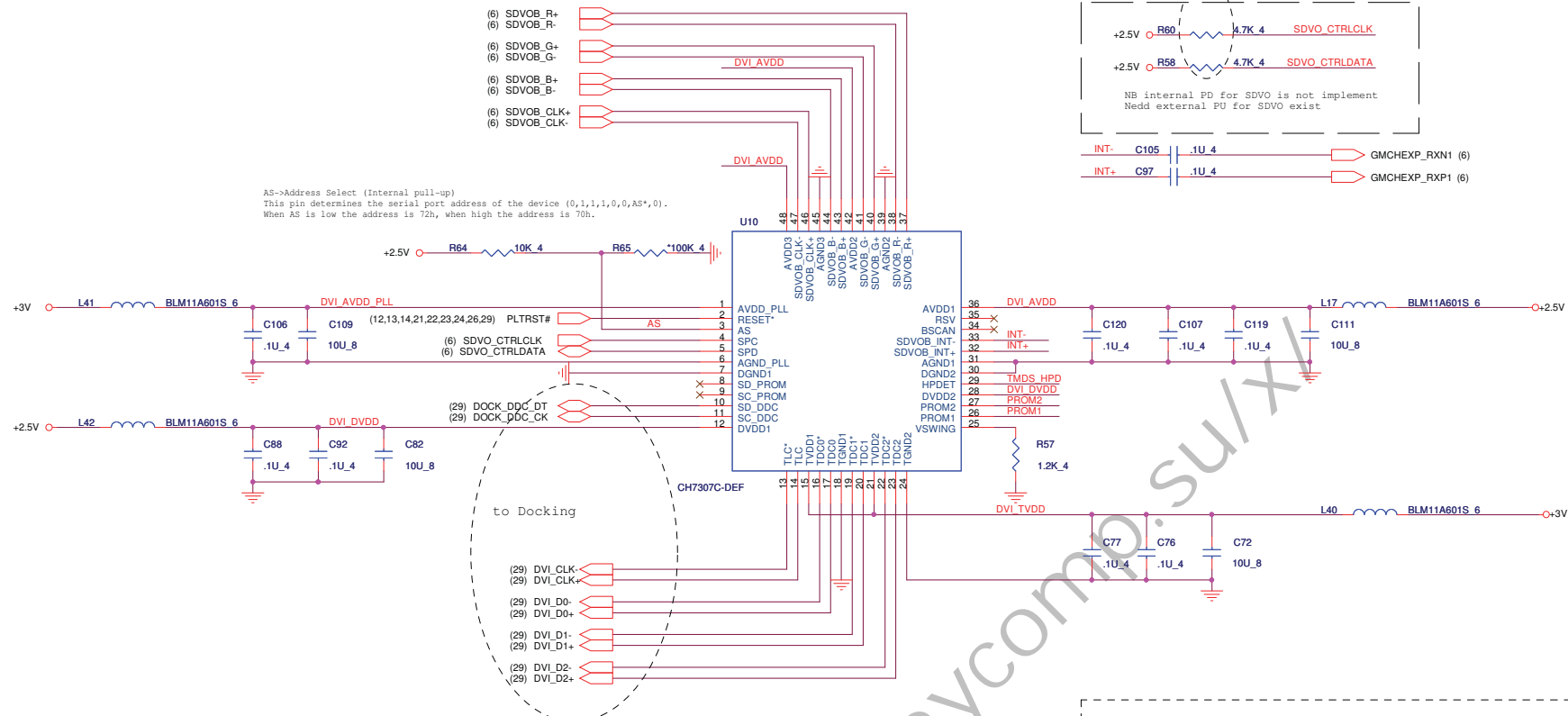


SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

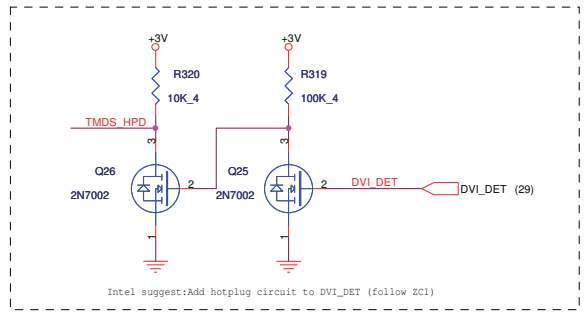
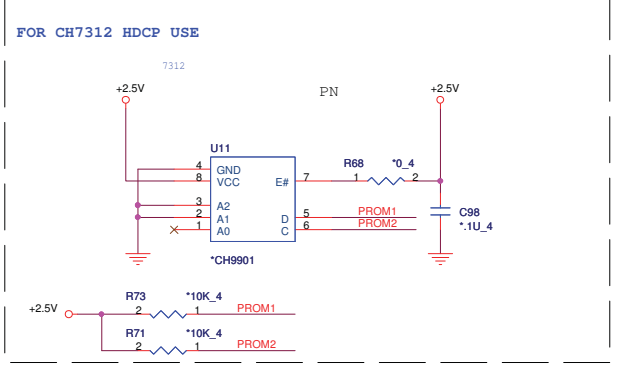
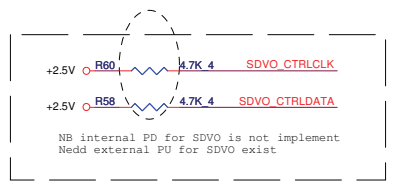
MR Sensor

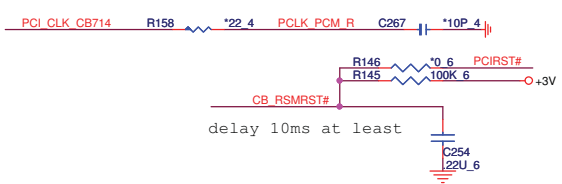
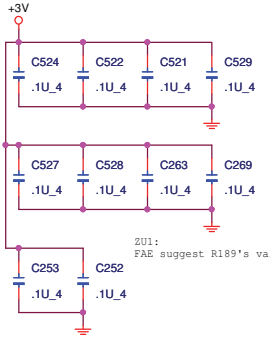


3/19 backlight on issue that same as ZU1



AS->Address Select (Internal pull-up)
 This pin determines the serial port address of the device (0,1,1,1,0,0,AS*,0).
 When AS is low the address is 72h, when high the address is 70h.



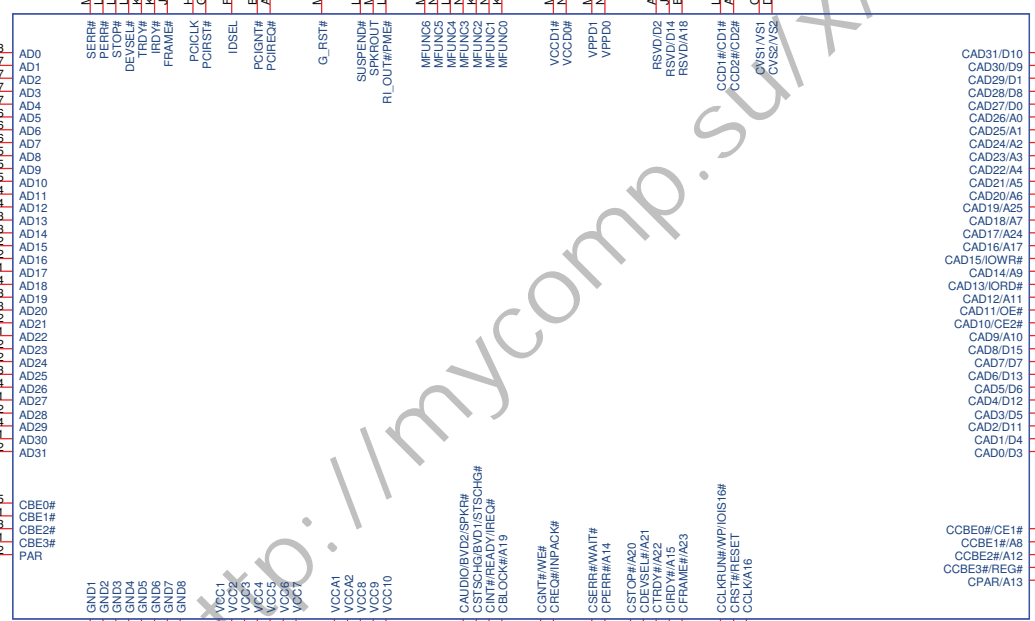
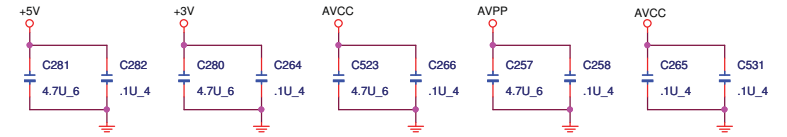
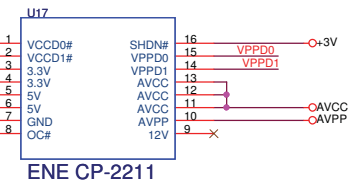


- (12,19,24,26) SERIRQ
- (12,19,21) PCI_PME#
- (27) PCMSPK
- (12) REQ0#
- (12) GNT0#
- (12,19,23) PCIRST#
- (2) PCI_CLK_CB714
- (12,19,21) FRAME#
- (12,19,21) IRDY#
- (12,19,21) TRDY#
- (12,19,21) DEVSEL#
- (12,19,21) STOP#
- (12,19,21) PERR#
- (12,19,21) SERR#

ENE1410 AJ014100T41

ID Select : AD17
 Interrupt Pin : INTE#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#

- (12,19,21) CBE0#
- (12,19,21) CBE1#
- (12,19,21) CBE2#
- (12,19,21) CBE3#
- (12,19,21) PAR



- VCCD1#
- VCCD0#
- VPPD1
- VPPD0
- A_CRSVD/D2
- A_CRSVD/D14
- A_CRSVD/A18
- A_CCD1#
- A_CCD2#
- A_CV1#
- A_CV2#

- A_CAD31
- A_CAD30
- A_CAD29
- A_CAD28
- A_CAD27
- A_CAD26
- A_CAD25
- A_CAD24
- A_CAD23
- A_CAD22
- A_CAD21
- A_CAD20
- A_CAD19
- A_CAD18
- A_CAD17
- A_CAD16
- A_CAD15
- A_CAD14
- A_CAD13
- A_CAD12
- A_CAD11
- A_CAD10
- A_CAD9
- A_CAD8
- A_CAD7
- A_CAD6
- A_CAD5
- A_CAD4
- A_CAD3
- A_CAD2
- A_CAD1
- A_CAD0
- A_CC/BE0#
- A_CC/BE1#
- A_CC/BE2#
- A_CC/BE3#
- A_CPAR

- A_CCLK
- A_CCRST#
- A_CCLKRUN#
- A_CFRAME#
- A_CIRDY#
- A_CTRDY#
- A_CDEVSEL#
- A_CSTOP#
- A_CPERR#
- A_CSERR#
- A_CREQ#
- A_CGNT#
- A_CBLOCK#
- A_CINT#
- A_CSTSCHG
- A_AUDIO

PROJECT : ZU2
Quanta Computer Inc.

Size: Document Number
PCMCIA (ENE CB1410)

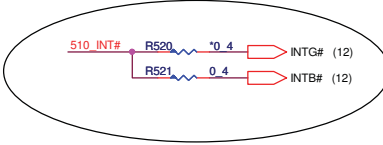
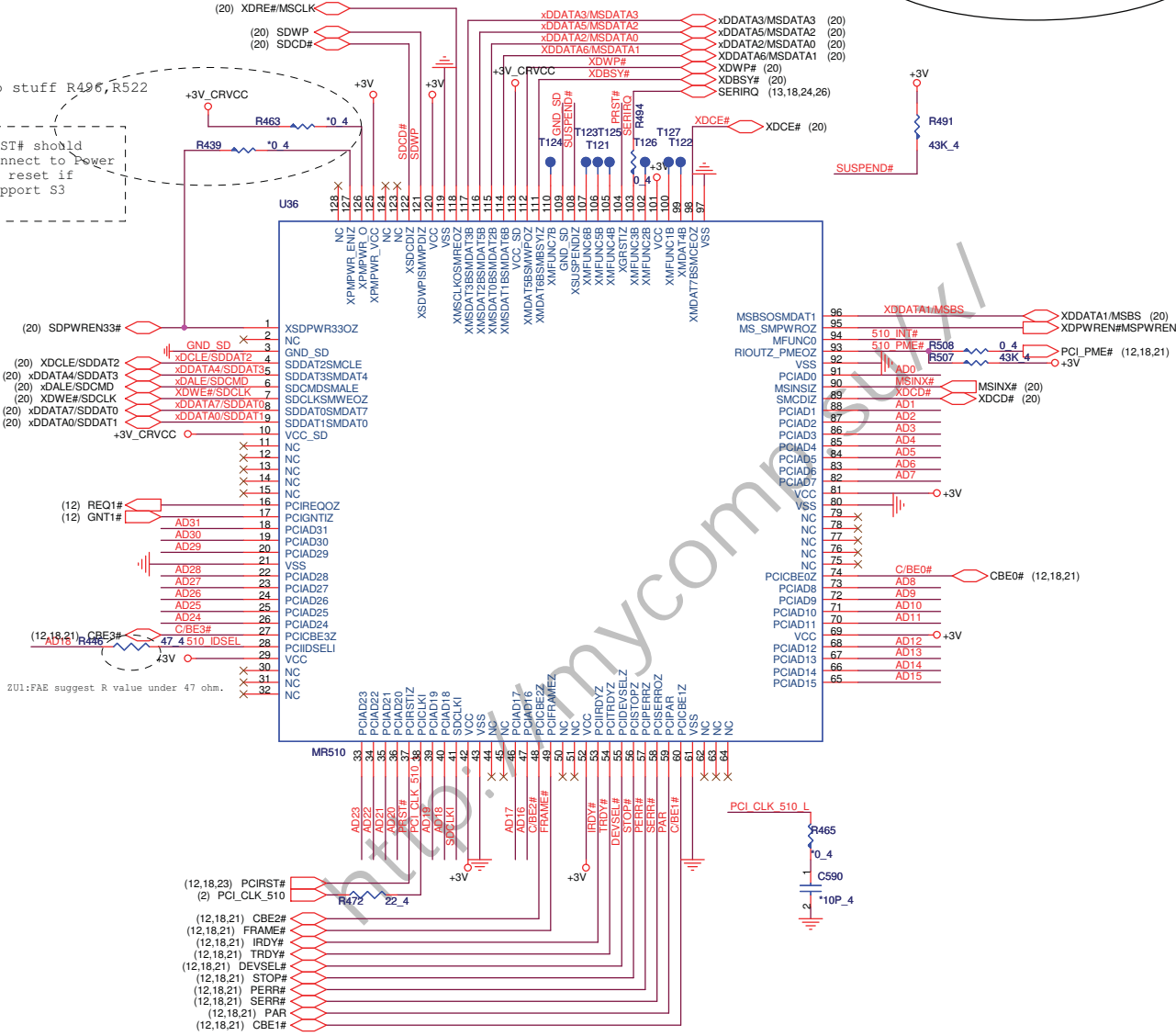
Date: Thursday, March 22, 2007 Sheet 18 of 39 Rev 1A

ID Select : AD18
 Interrupt Pin : INTG#
 Request Indicate : REQ1#
 Grant Indicate : GNT1#

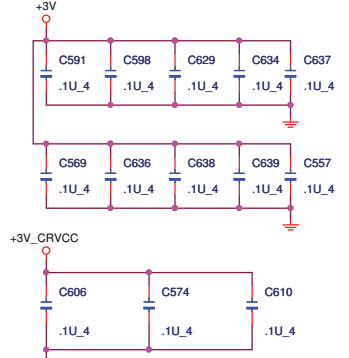
ZU1:no stuff R496,R522

GRST# should connect to Power On reset if support S3

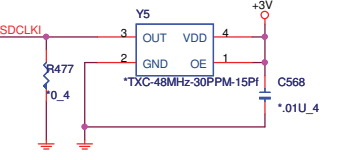
(12,18,21) AD[31..0]



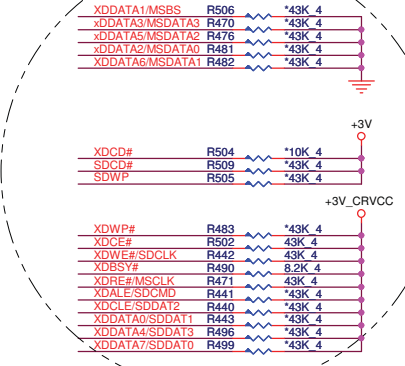
Decoupling CAP.



48MHz CLK



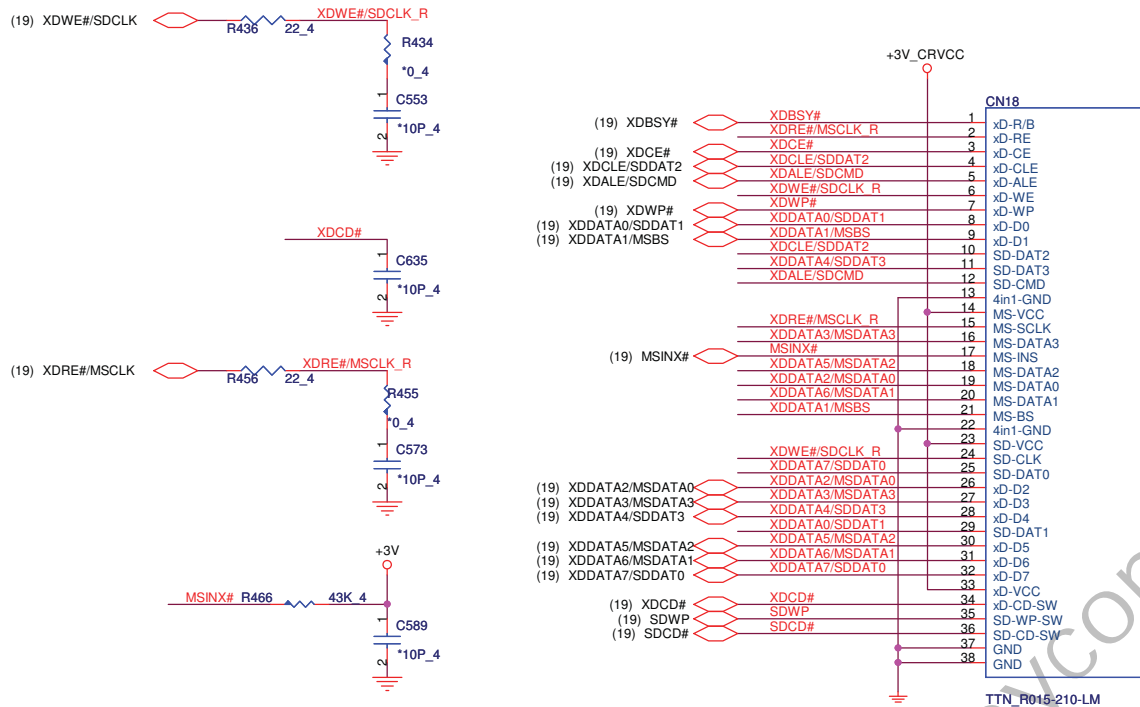
PU/PD



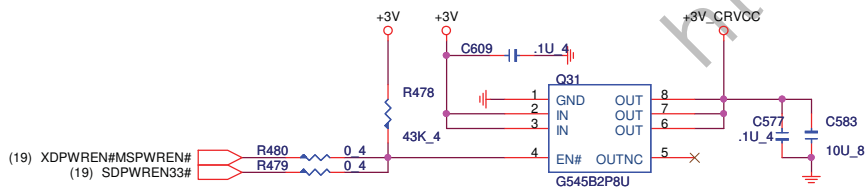
0213: follow ZU1 for cost down issue with FAE

PROJECT : ZU2
Quanta Computer Inc.

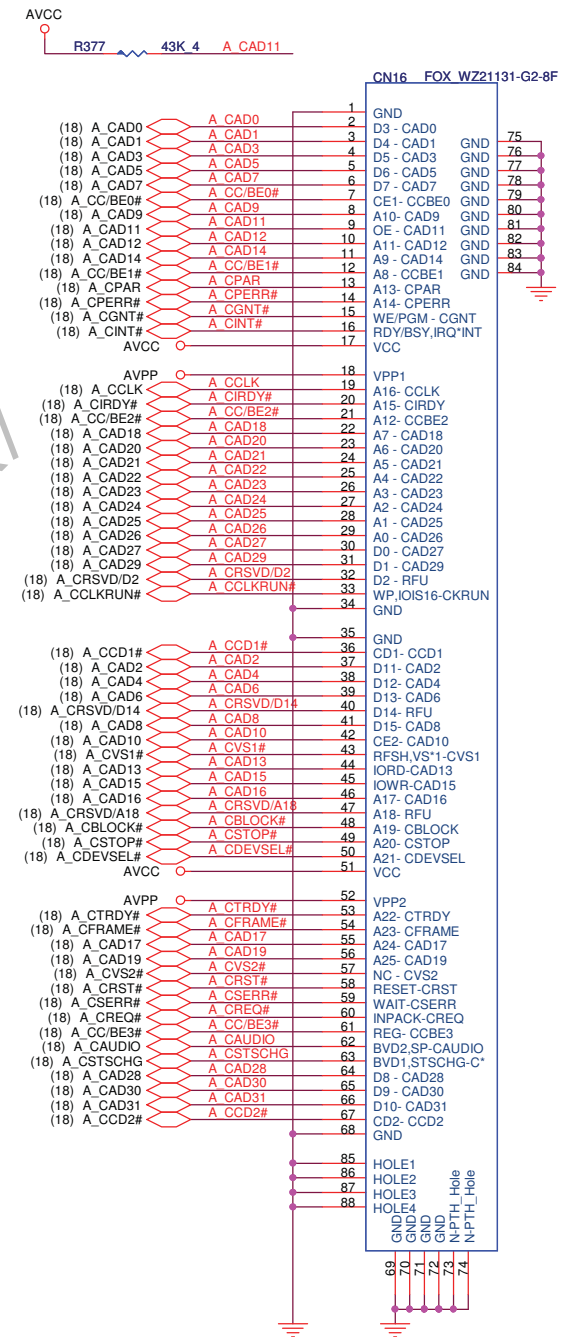
CardReader




CardReader Power switch



PCMCIA

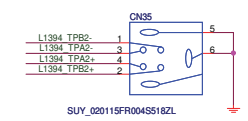
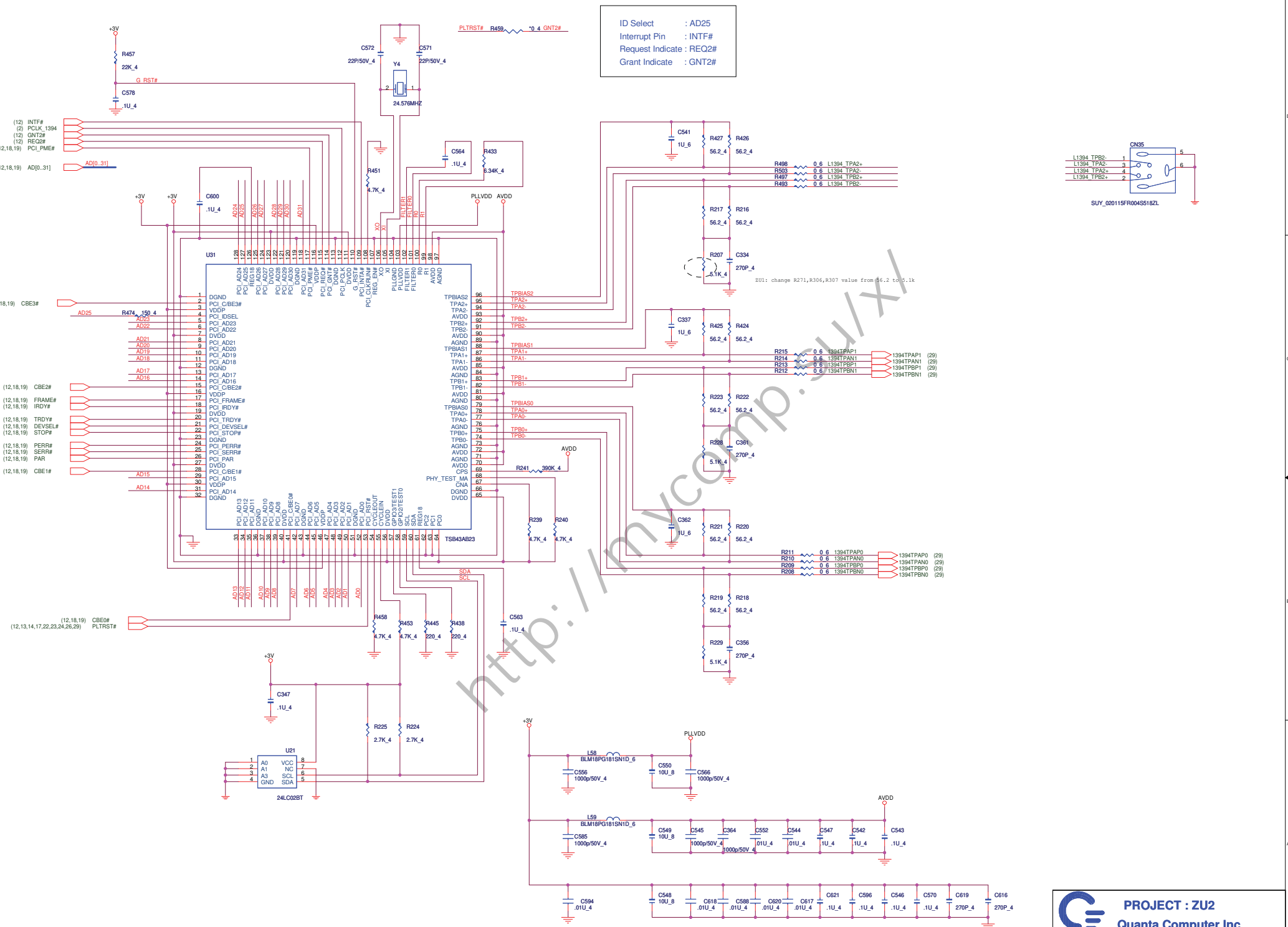




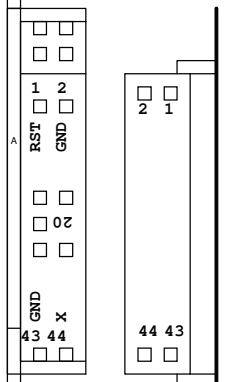
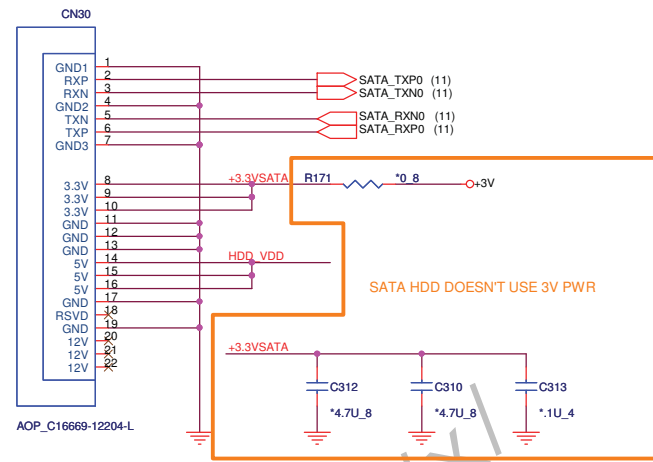
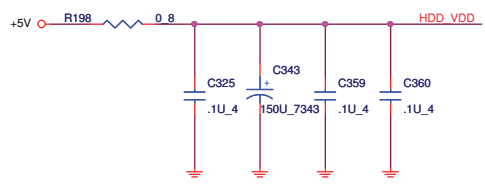
PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	CARD Reader & PCMCIA SLOT	1A
Date:	Thursday, March 22, 2007	Sheet 20 of 39

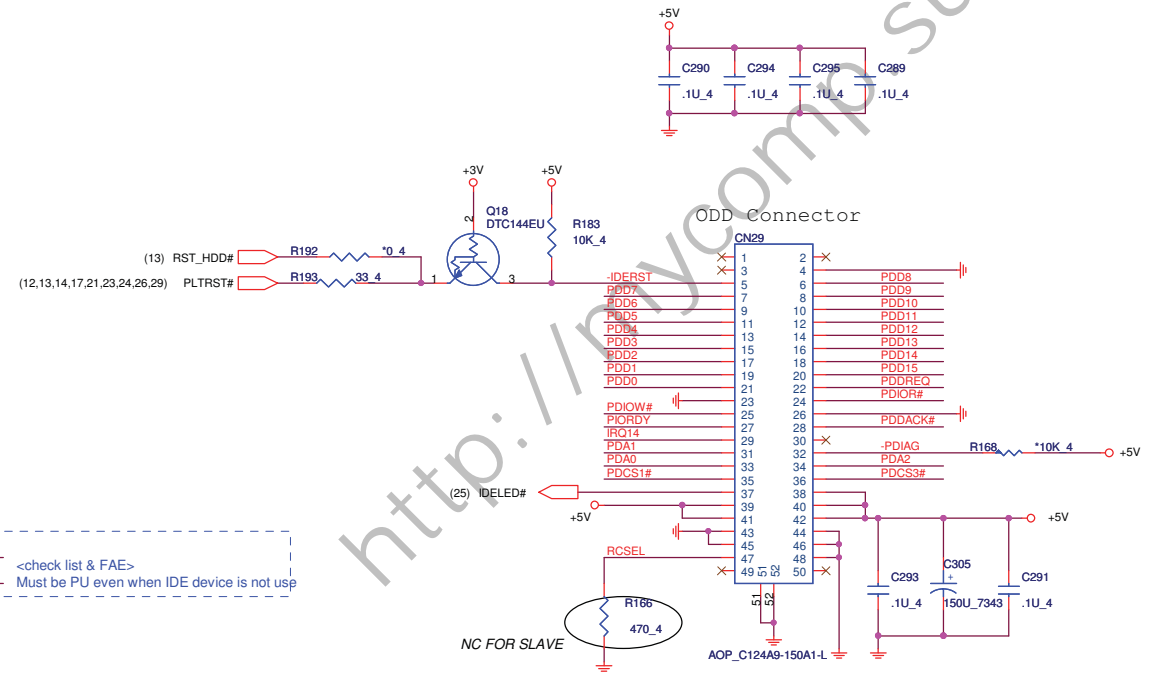
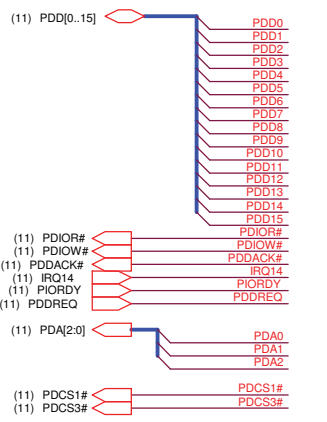
ID Select : AD25
 Interrupt Pin : INTF#
 Request Indicate : REQ2#
 Grant Indicate : GNT2#



SATA HDD



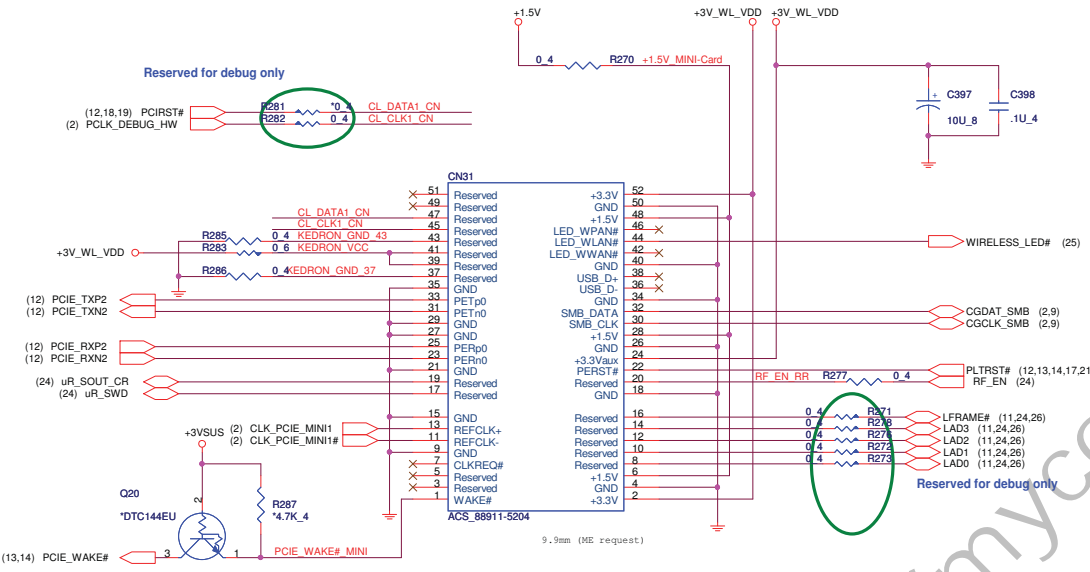
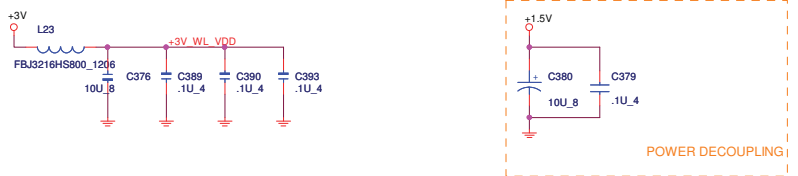
PATA ODD



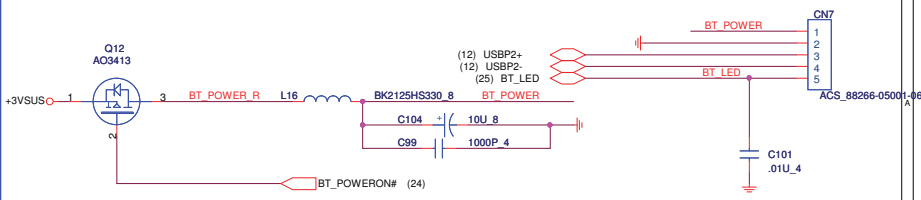
PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD & PATA-ODD	1A
Date:	Thursday, March 22, 2007	Sheet 22 of 39

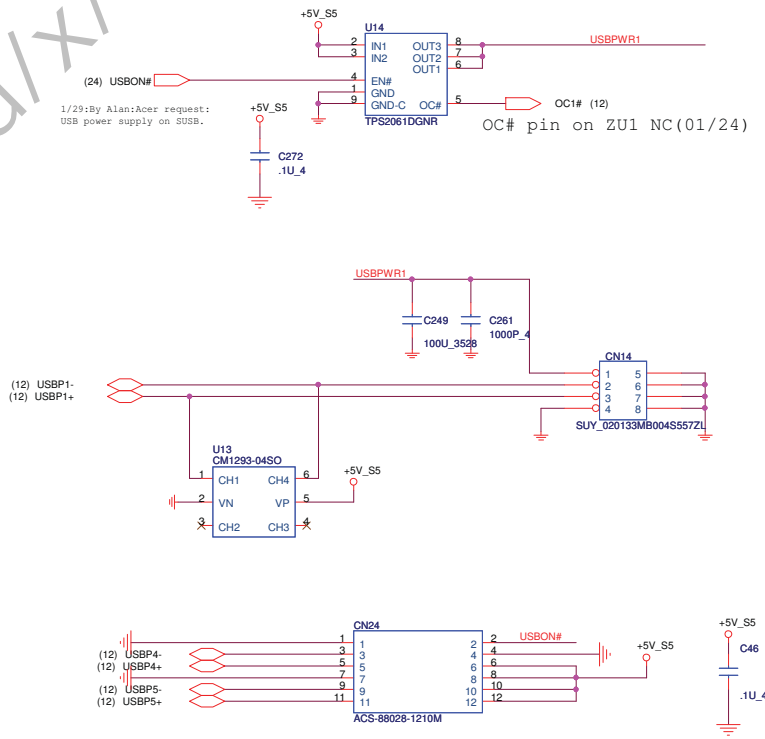
MINI-Card



BLUETOOTH MODULE CONNECTOR



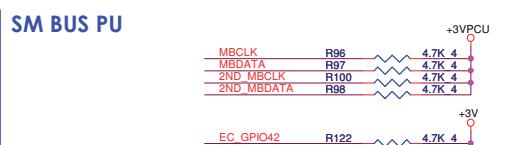
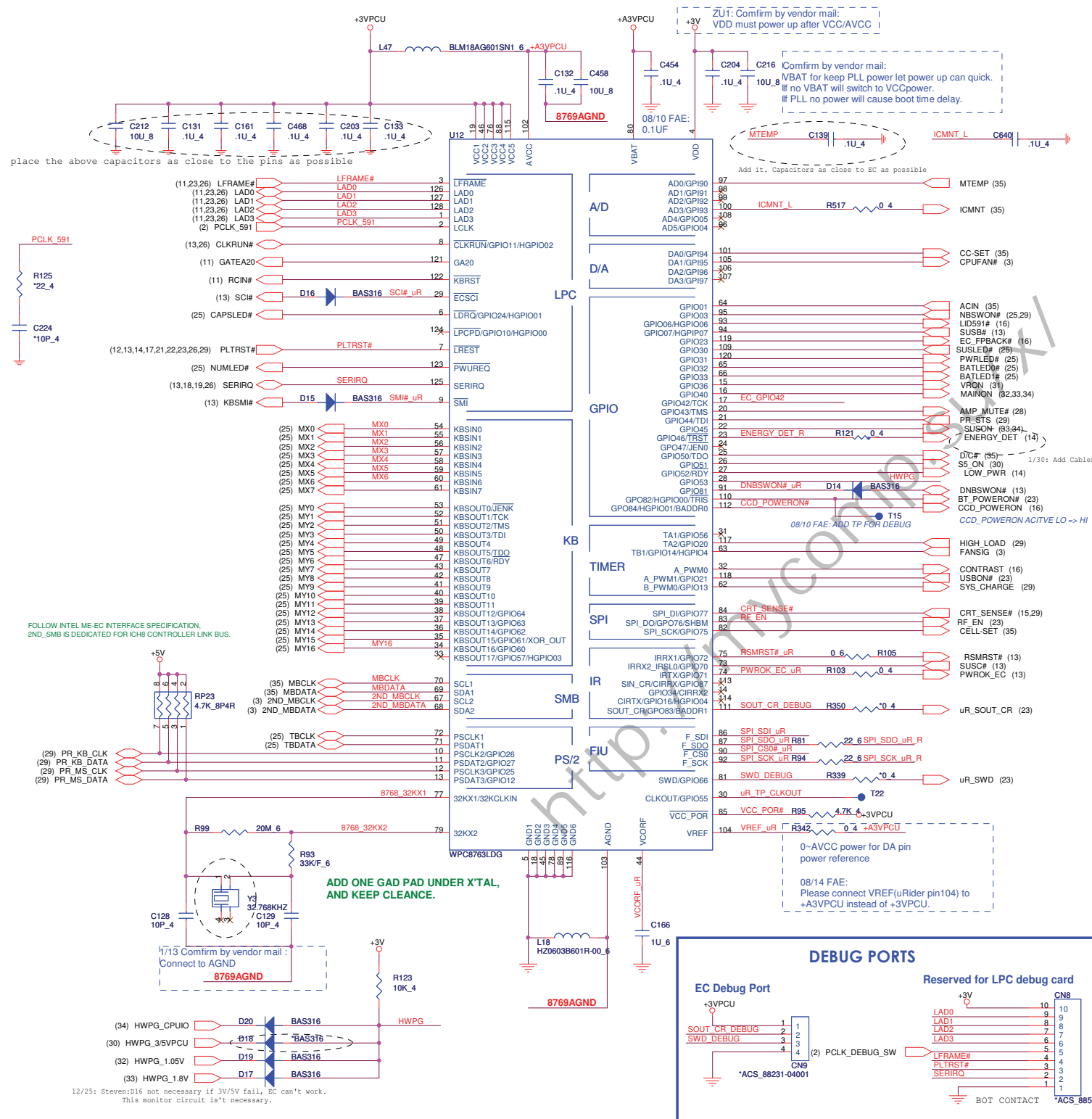
System USB



<http://mycomp.su/xl>

PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	Mini card/USB/Bluetooth	1B
Date:	Wednesday, March 28, 2007	Sheet 23 of 39

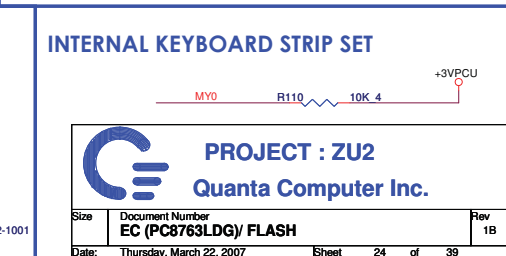
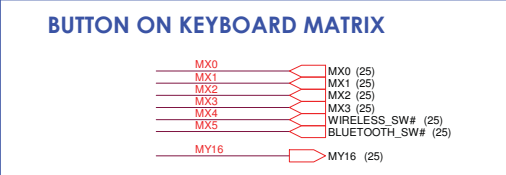
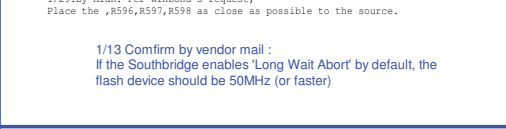
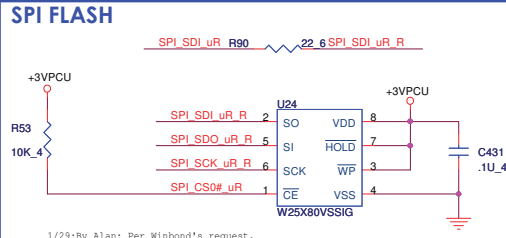
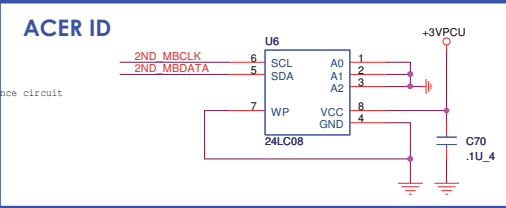


I/O ADDRESS SETTING

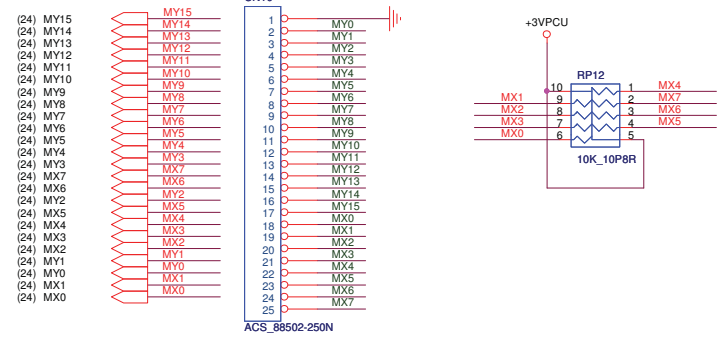
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 CCD_POWERON# R353 10K 4
 BADDR1 SOUT_CR_DEBUG R352 *10K 4
 SHBM RF_EN R338 10K 4

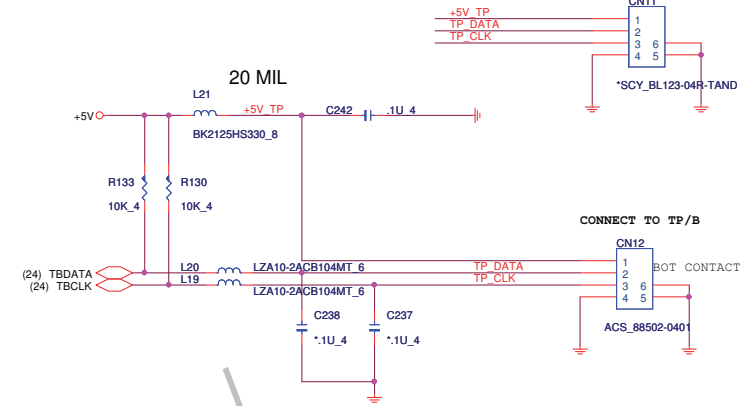


INT K/B

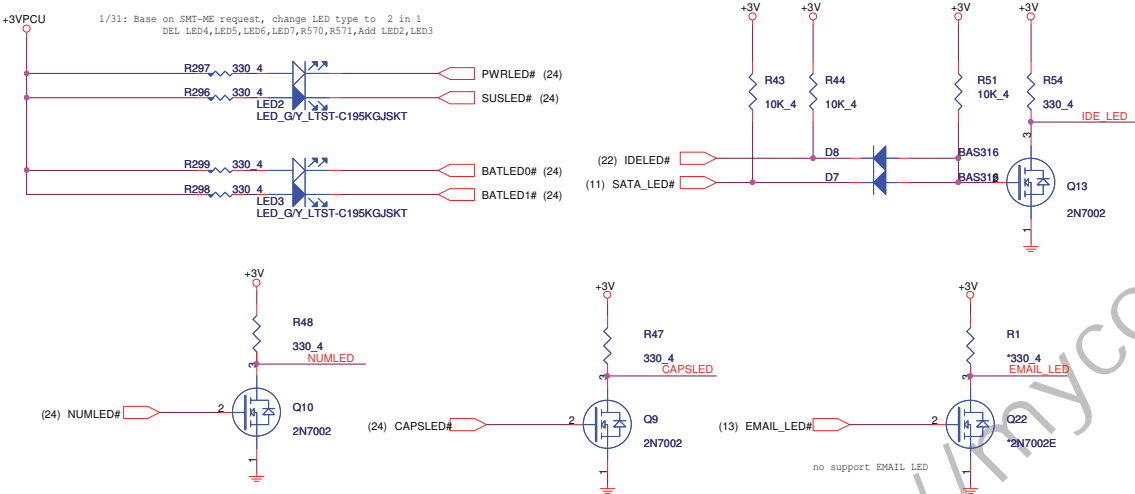


uR REQUEST
MY DOES NOT NEED PU.
MY CAN NOT USE EMI BYPASS CAP, DUE TO FLASH.

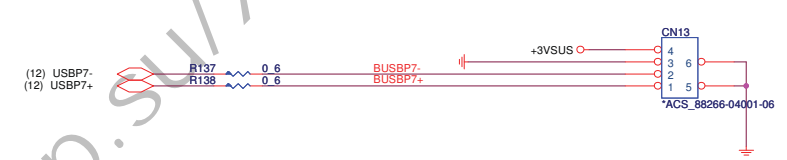
TOUCH PAD



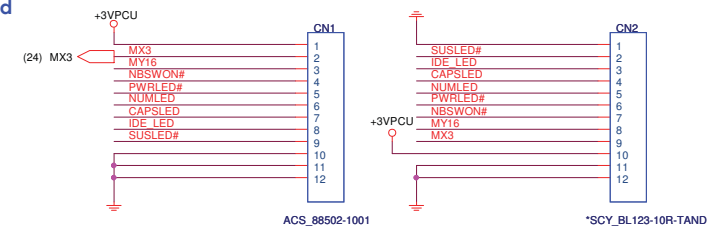
LED



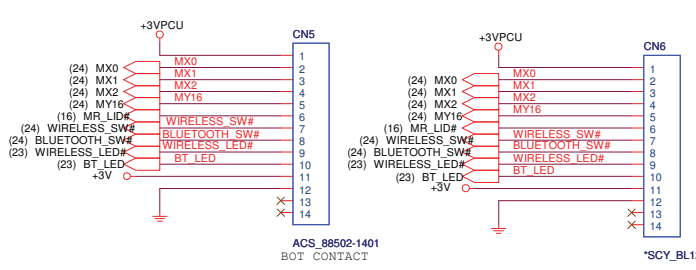
Finger Printer



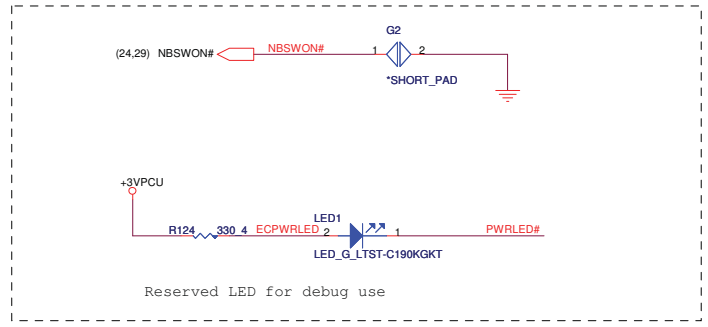
LED Board



Function Board

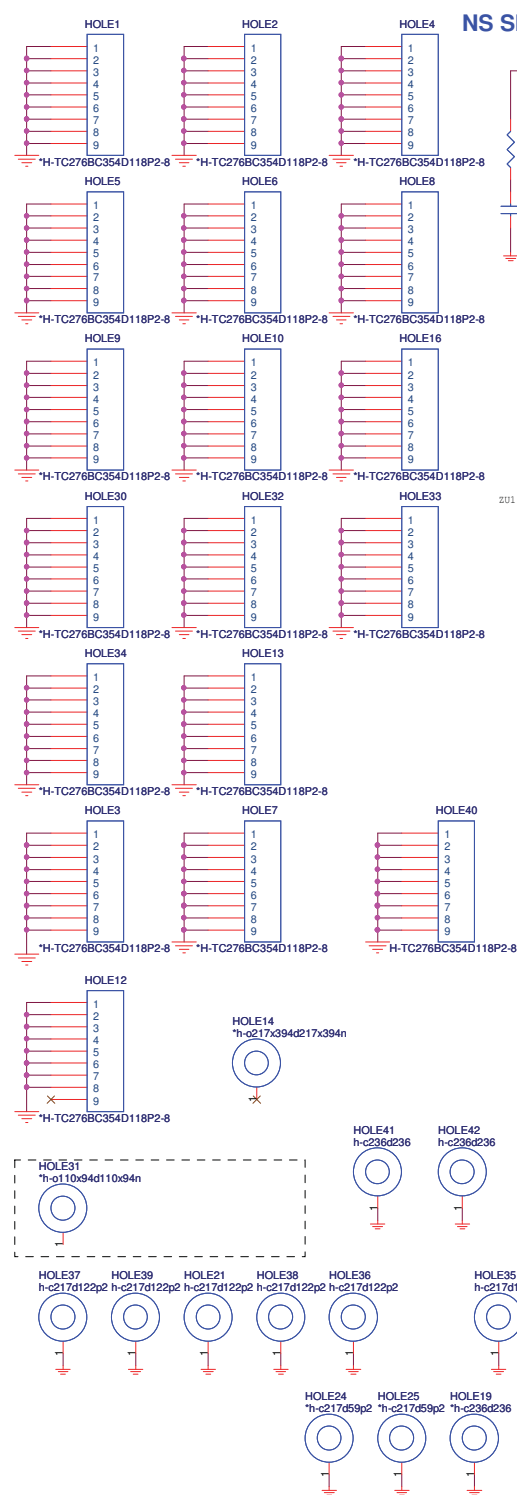


Keyboard Matrix	Button
MX0/MY16	acer EAP Button
MX1/MY16	acer EMAIL Button
MX2/MY16	acer WW Button
MX3/MY16	acer EPM Button
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button

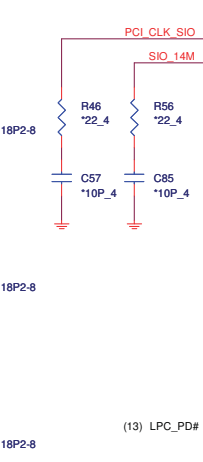


PROJECT : ZU2
Quanta Computer Inc.

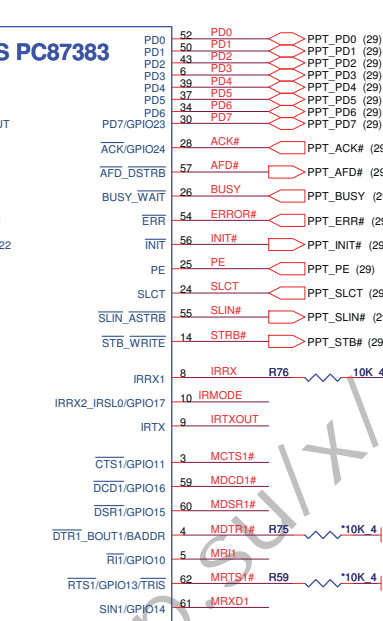
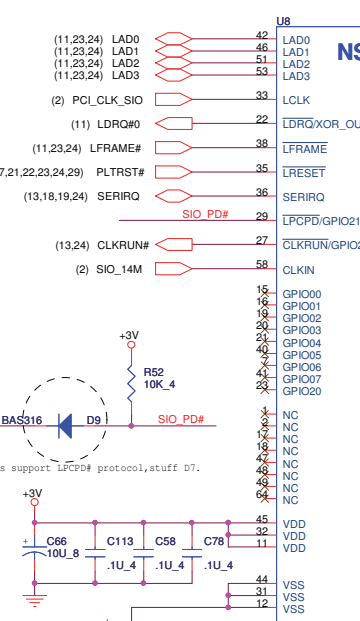
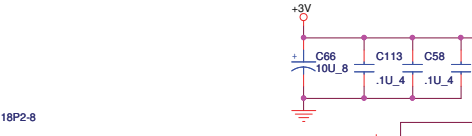
Size	Document Number	Rev
	SWITCH,LED,KB,Finger,TP	1B
Date:	Tuesday, March 27, 2007	Sheet 25 of 39



NS SIO PC87383



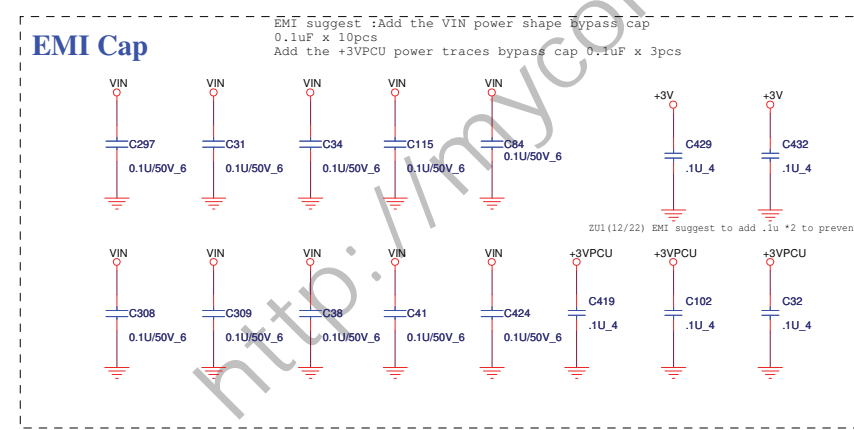
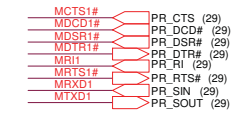
ZUI(12/12) Intel suggest: All LPC devices support LPCPD# protocol, stuff D7.



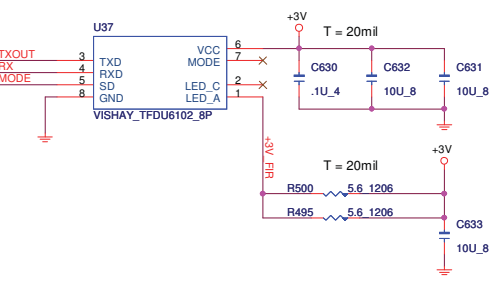
OPEN : 164Eh~164Fh
LOW : 2Eh~2Fh

OPEN : normal pin operation
LOW : float device pin

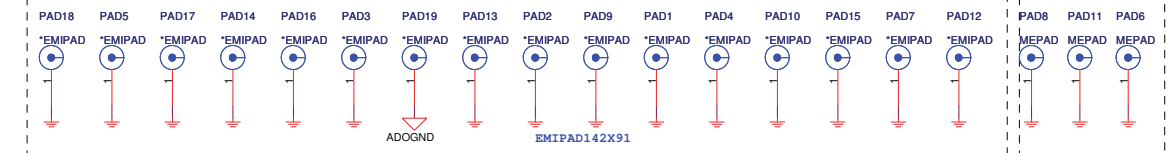
OPEN : normal Device operation
LOW : XOR pin tree



FIR



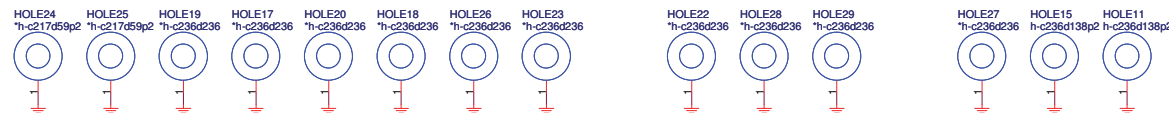
ESDPad



C2A: (12/22) EMI suggest add three clip to contact with CPU cooler's fins (PAD23, 24, 25)

C2A: (12/22) Add three PAD per ME request (fix wire)

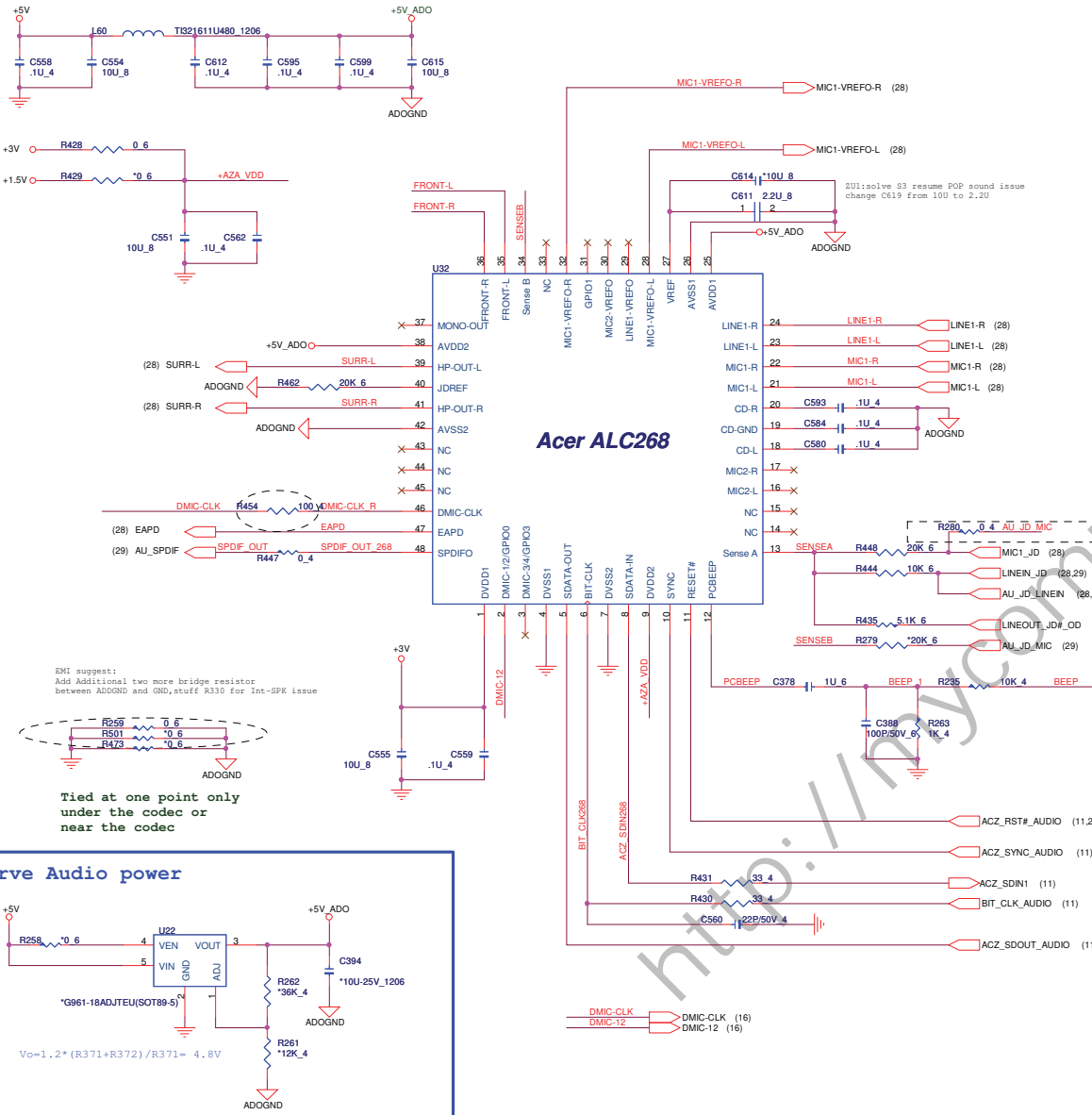
HOLE



PROJECT : ZU2
Quanta Computer Inc.

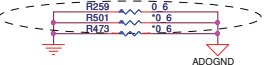
Size	Document Number	Rev
	SUPER-IO/FIR/HOLE	1A
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CODEC (ALC268)



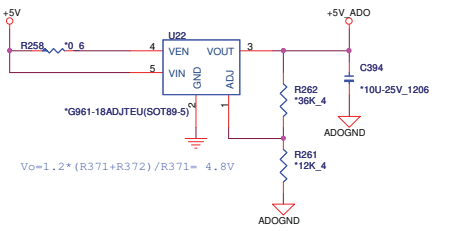
Acer ALC268

EMI suggest:
Add Additional two more bridge resistor
between ADOGND and GND,stuff R330 For Int-SPK issue



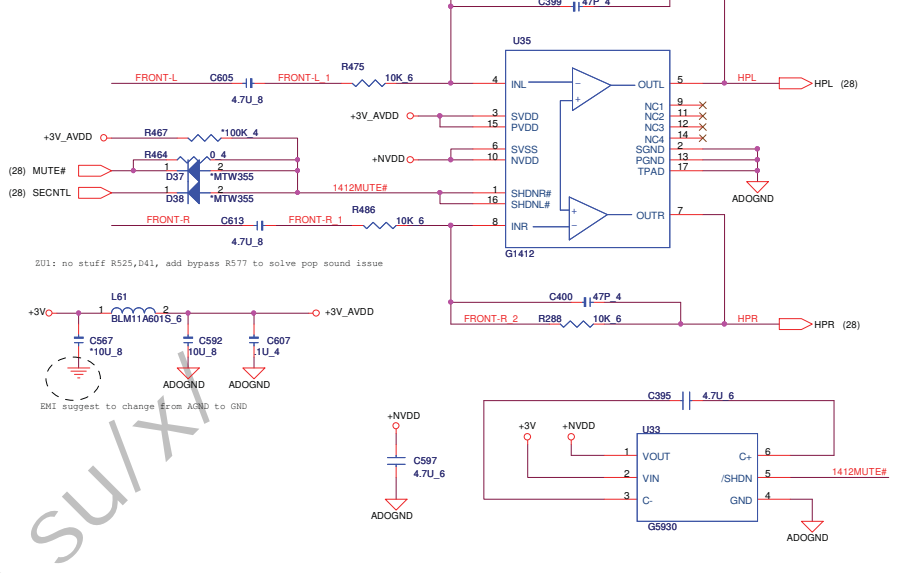
Tied at one point only
under the codec or
near the codec

Reserve Audio power



$$V_o = 1.2 * (R371 + R372) / R371 = 4.8V$$

LINE OUT Amplifier

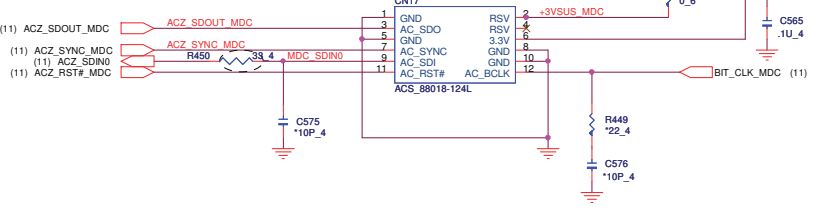


ZUI: no stuff R525,D41, add bypass R577 to solve pop sound issue

ZUI suggest to change from AAZ to GND

- SYS / EZ MIC
- SYS Line-in
- EZ Line-in
- SYS/EZ Line-out
- EZ MIC (reserve)

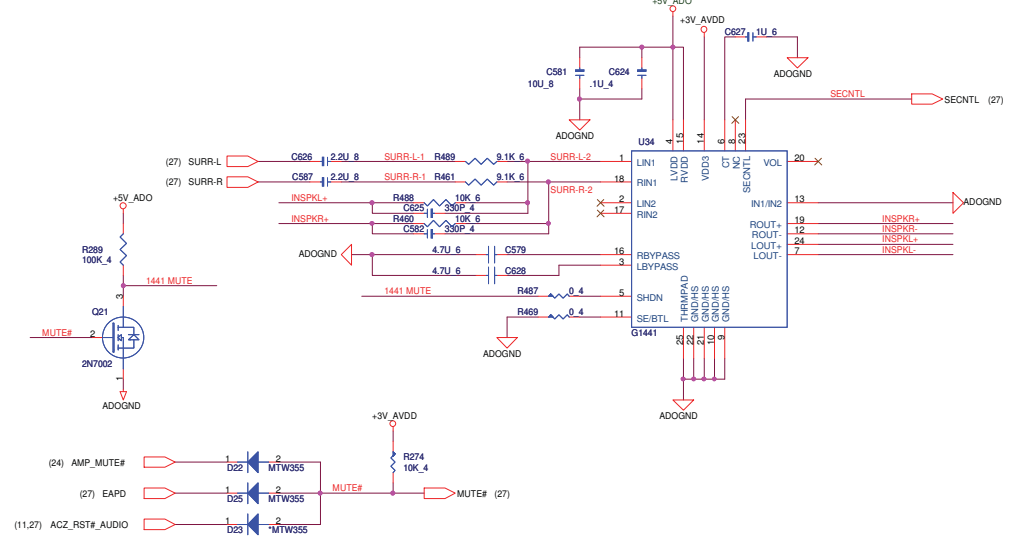
MDC



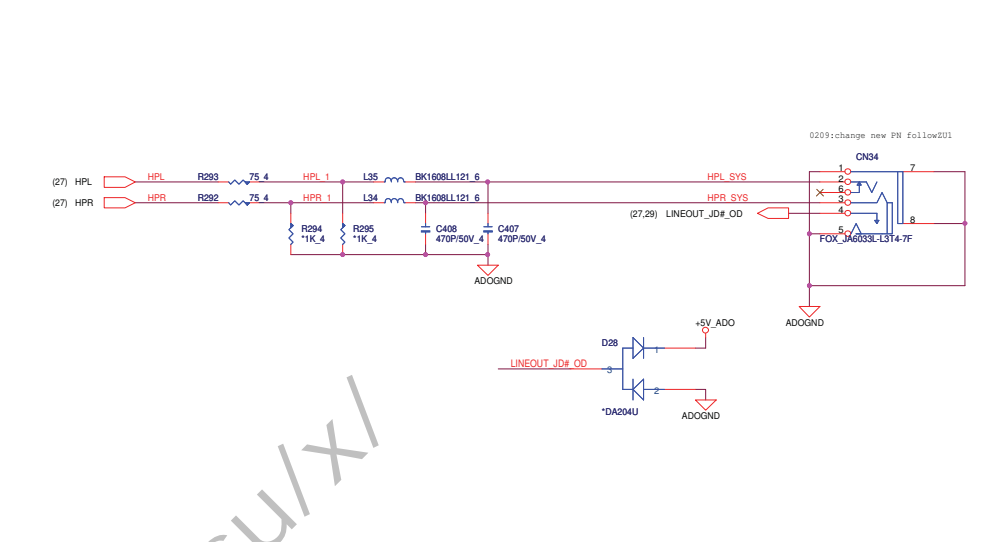
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Quanta Computer Inc.

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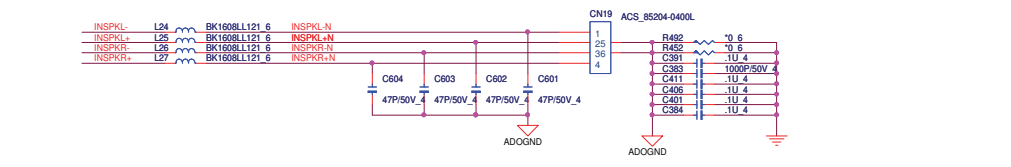
Speaker Amplifier



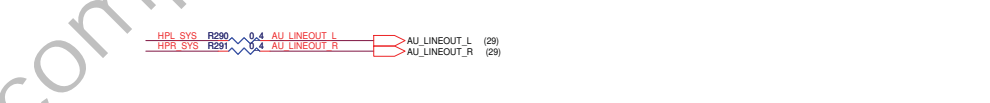
SYSTEM LINE OUT



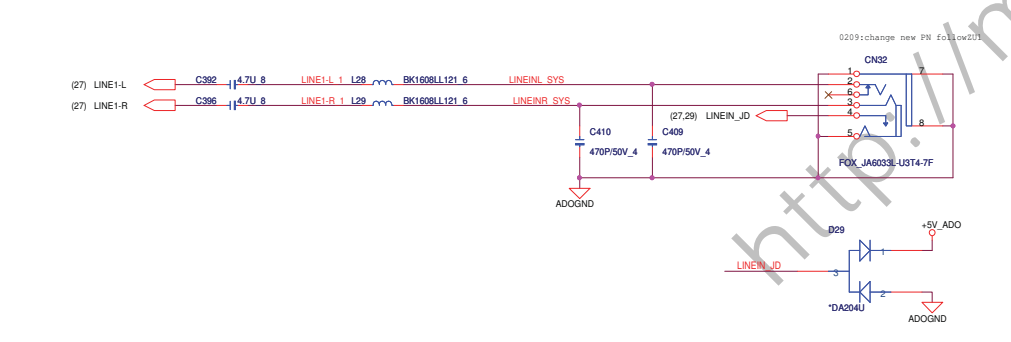
SPEAKER



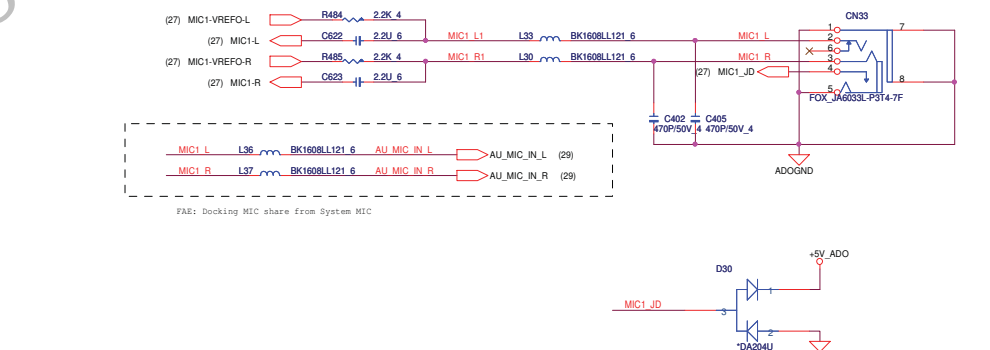
Docking LINE OUT/SPDIF



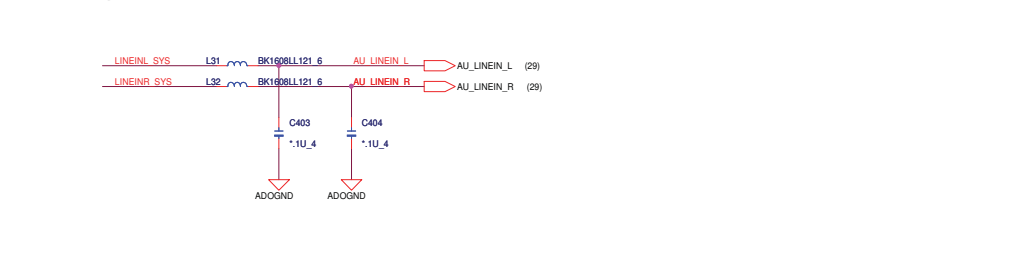
SYSTEM LINE IN



SYSTEM MIC

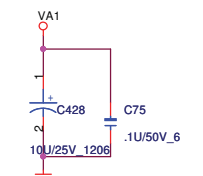
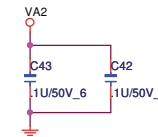
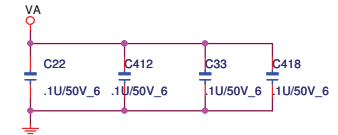


Docking LINE IN

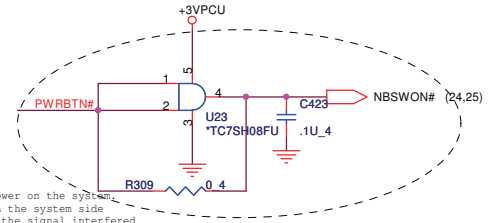


3/16 Modify D5 Footprint from SBM1040-3P to SBM1040-3P-ZU1

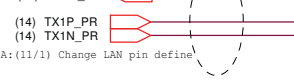
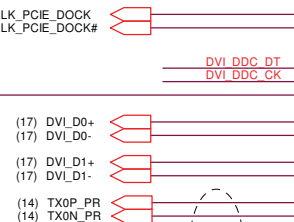
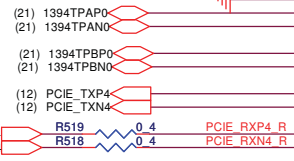
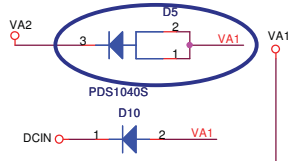
1/31: Acer DVR1012 Design Requirement Checklist:
The system side should have a diode to block the AC adaptor power coming from ezDock.



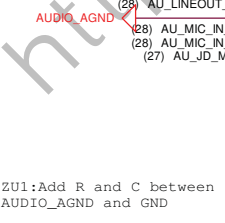
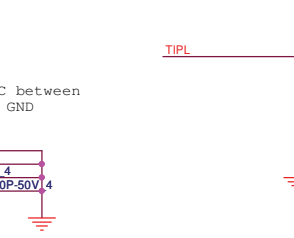
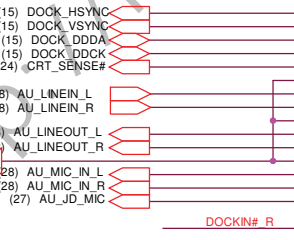
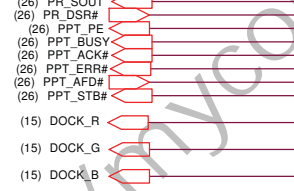
POWER DECOUPLING



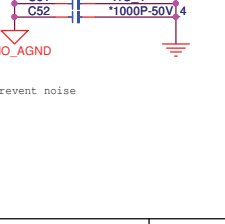
refer to Acer Design Guide:
this signal is asserted to power on the system.
A buffer used for PWRBTN# on the system side
may be necessary to prevent the signal interfered
by the contact noise.



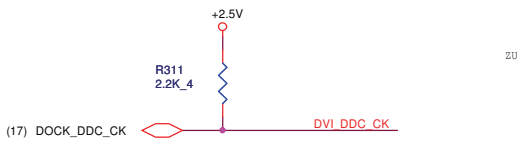
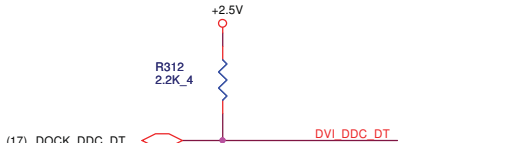
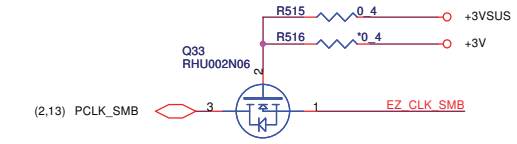
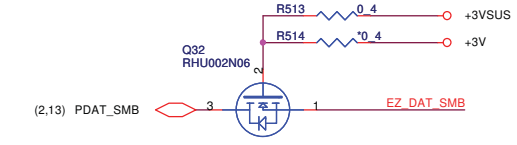
ZU1: Add PL 100K for DVI_DET



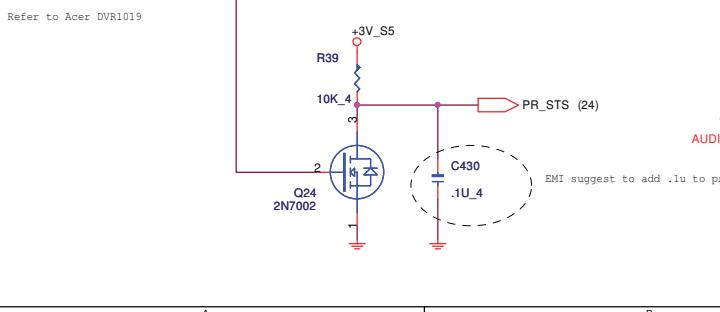
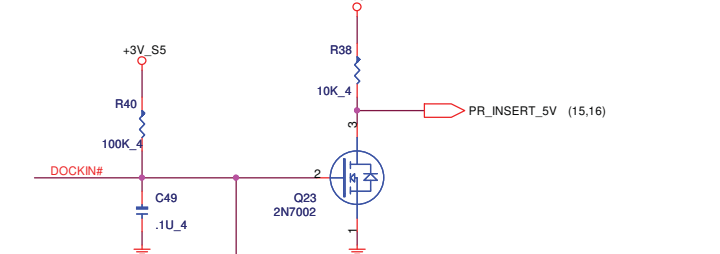
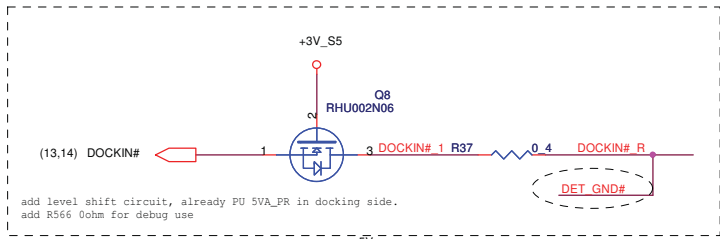
ZU1: Add R and C between AUDIO_AGND and GND



EMI suggest to add .1u to prevent noise

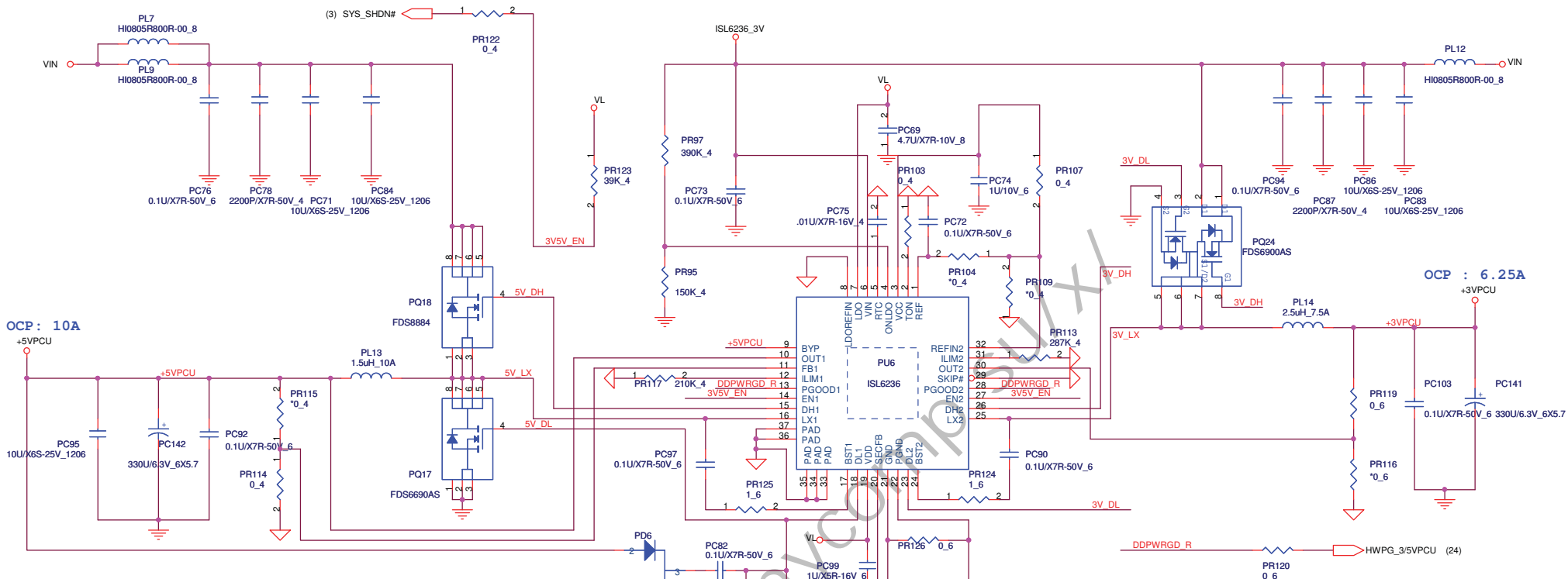


(1) Remove Level-shift circuit (already in docking side)
(2) change Power from +3V to +2.5V
(3) stuff 2.2k (R374, R375)



Refer to Acer DVR1019

MAIND → MAIND (34)
 SUS → SUS (34)

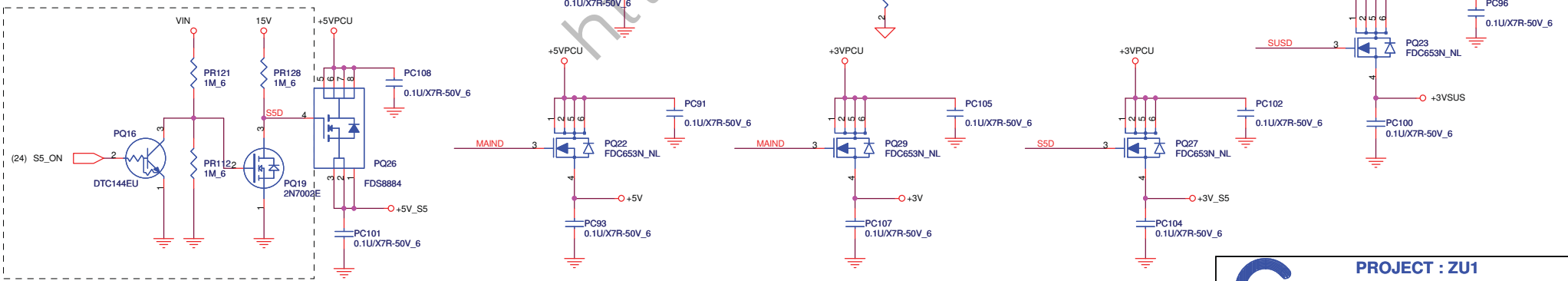


OCP : 10A

OCP : 6.25A

OCP : 10A
 $L(\text{ripple current}) = (19-5) * 5 / (1.5 * 0.4 * 19) \sim 6A$
 $I_{ocp} = 10 - (6/2) = 7A$
 $V_{th} = 9A * 15m\Omega = 105mV$
 $R(I_{lim}) = (105mV * 10) / 5\mu A \sim 210K$

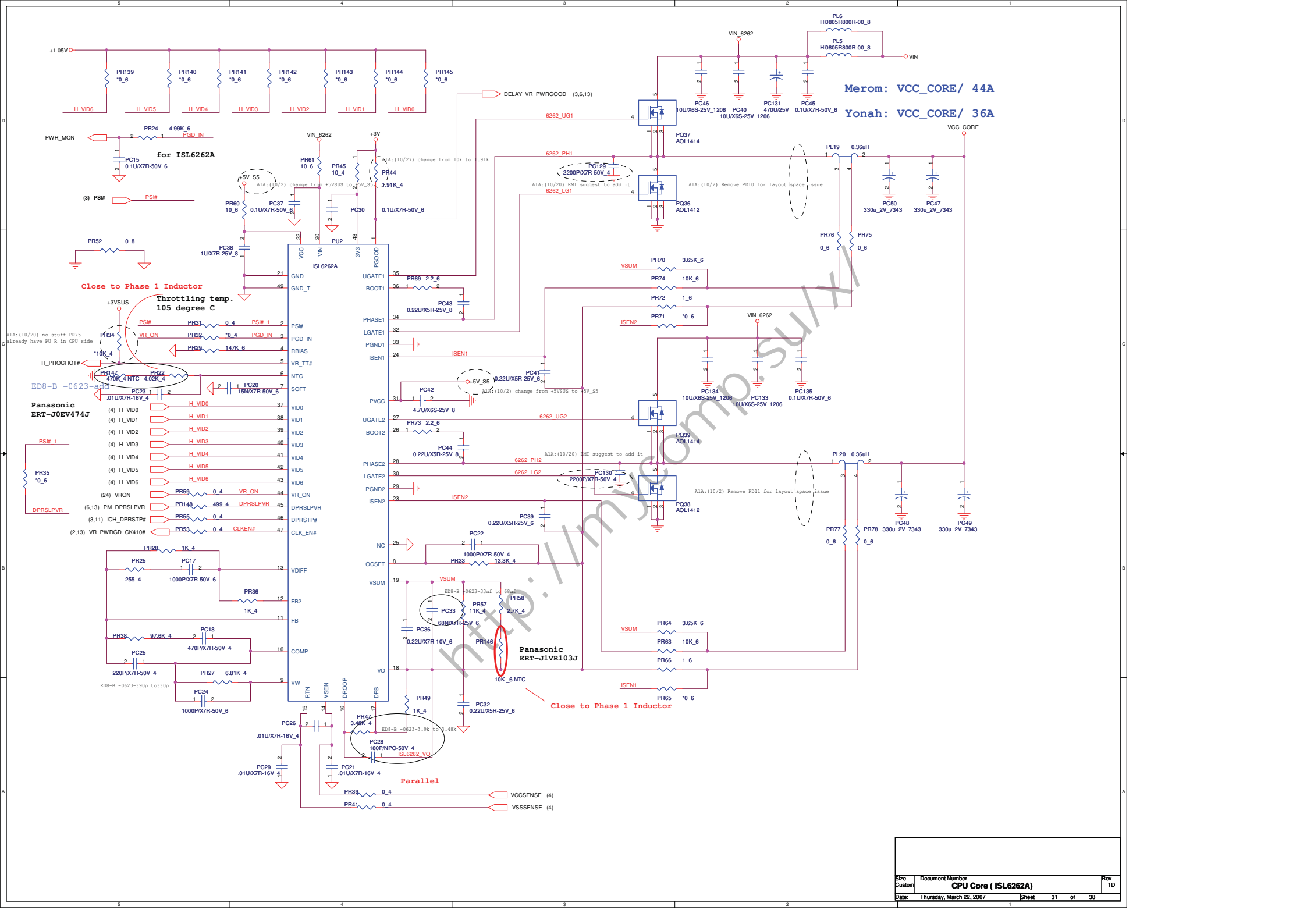
OCP : 6.25A
 $L(\text{ripple current}) = (19-3.3) * 3.3 / (2.5 * 0.5 * 19) \sim 2.18A$
 $I_{ocp} = 6.25 - (2.18/2) = 5.16A$
 $V_{th} = 5.16A * 28m\Omega = 145mV$
 $R(I_{lim}) = (145mV * 10) / 5\mu A \sim 294K$



C2A: (12/10) change S5_ON control circuit
 B1C: (11/29) change PQ26 from FDS6690AS (BAM66900022) to FDS8884 (BAM88840006)

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Quanta Computer Inc.

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Merom: VCC_CORE/ 44A

Yonah: VCC_CORE/ 36A

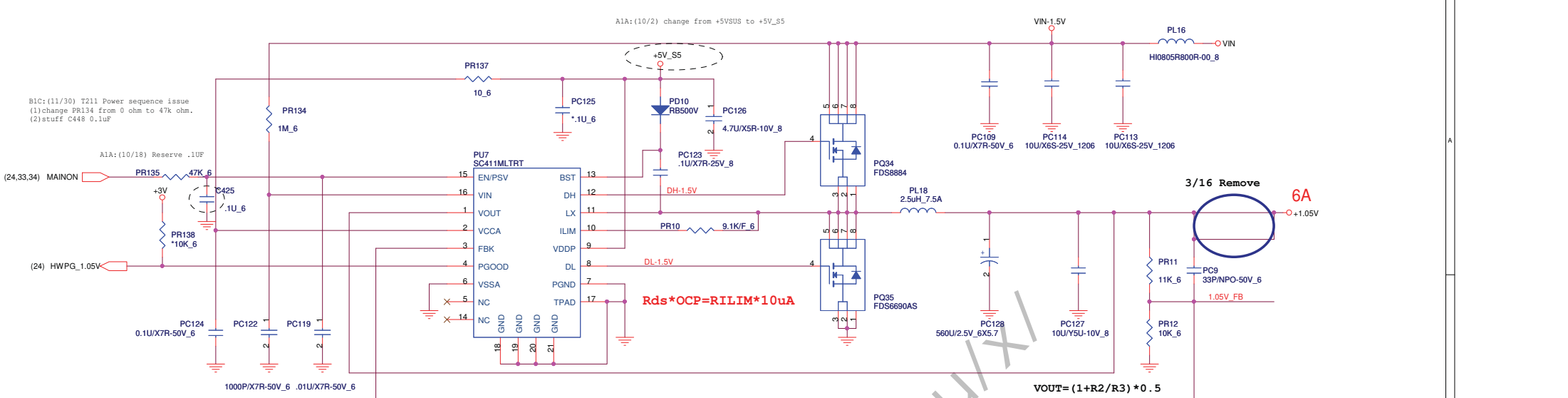
Close to Phase 1 Inductor

Throttling temp.
105 degree C

Close to Phase 1 Inductor

- Panasonic ERT-J0EV474J**
- (4) H_VID0
 - (4) H_VID1
 - (4) H_VID2
 - (4) H_VID3
 - (4) H_VID4
 - (4) H_VID5
 - (4) H_VID6
 - (24) VRON
 - (6.13) PM_DPRSLPVR
 - (3.11) ICH_DPRSTP#
 - (2.13) VR_PWRGDD_CK410#
- Panasonic ERT-J1VR103J**
- 10K_6 NTC

Size	Document Number	Rev
Custom	CPU Core (ISL6262A)	1D
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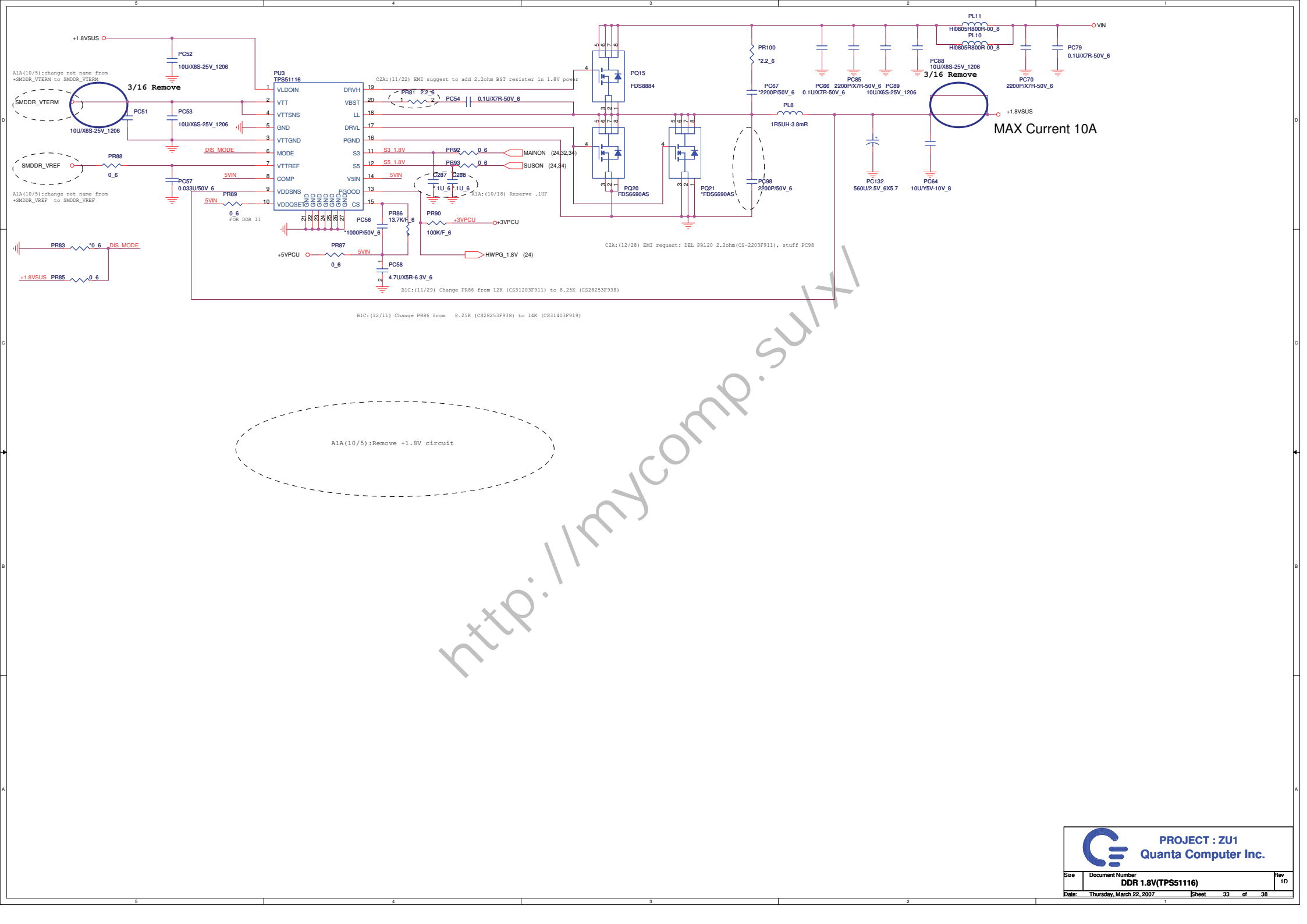
B1C:(11/30) T211 Power sequence issue
 (1)change PR134 from 0 ohm to 47k ohm.
 (2)stuff C428 0.1uF

A1A:(10/18) Reserve .1uF

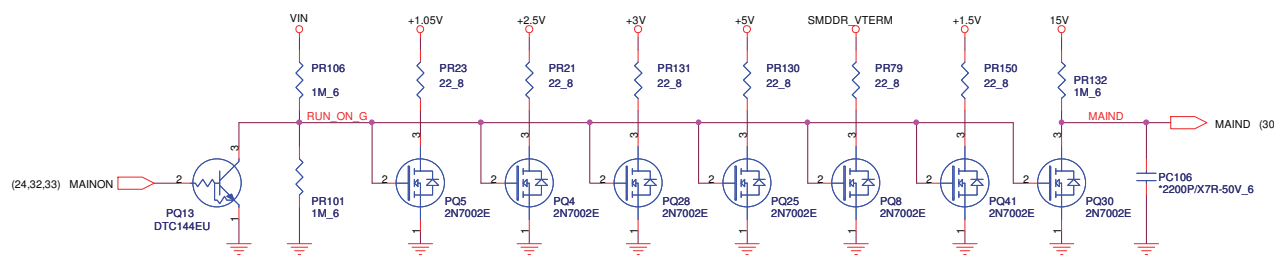
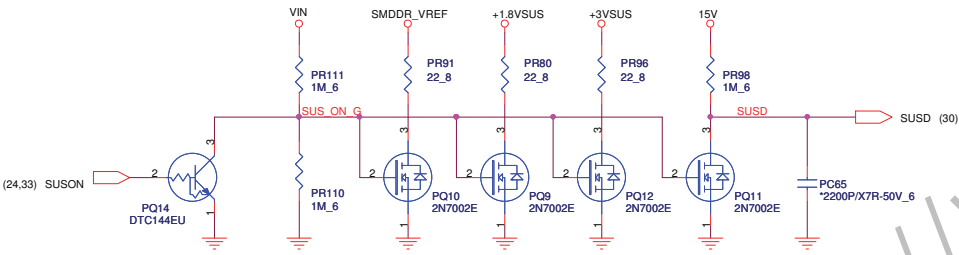
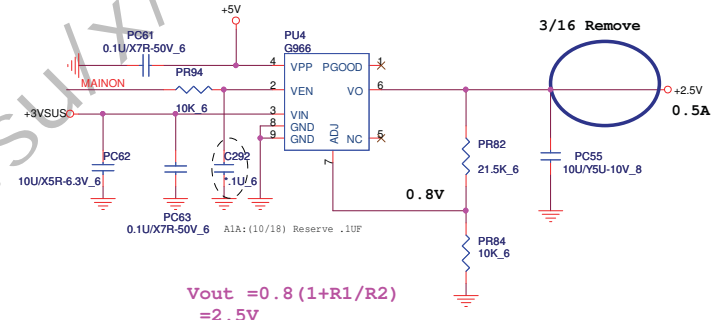
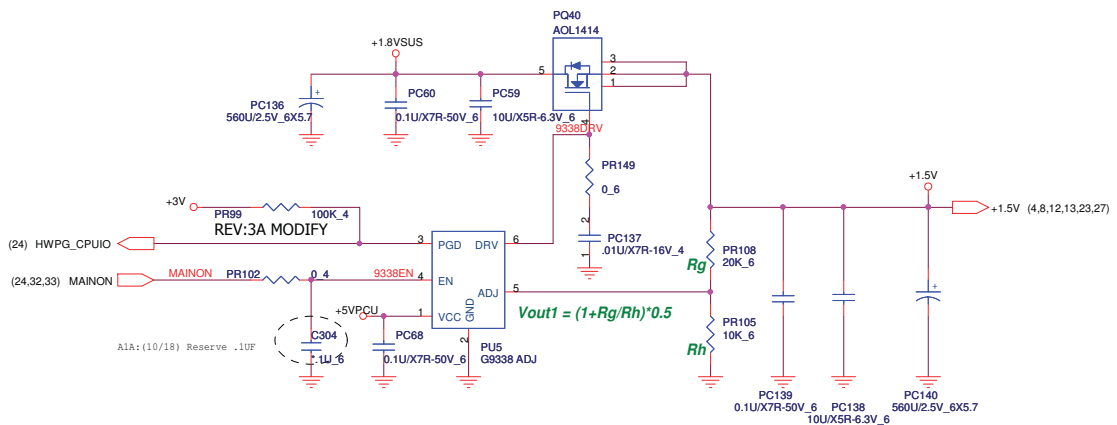
A1A:(10/2) change from +5V5US to +5V_S5

B1C:(11/29) Change PR8 from 20K(CS32003P933) to 6.65K ohm (CS26653P911)

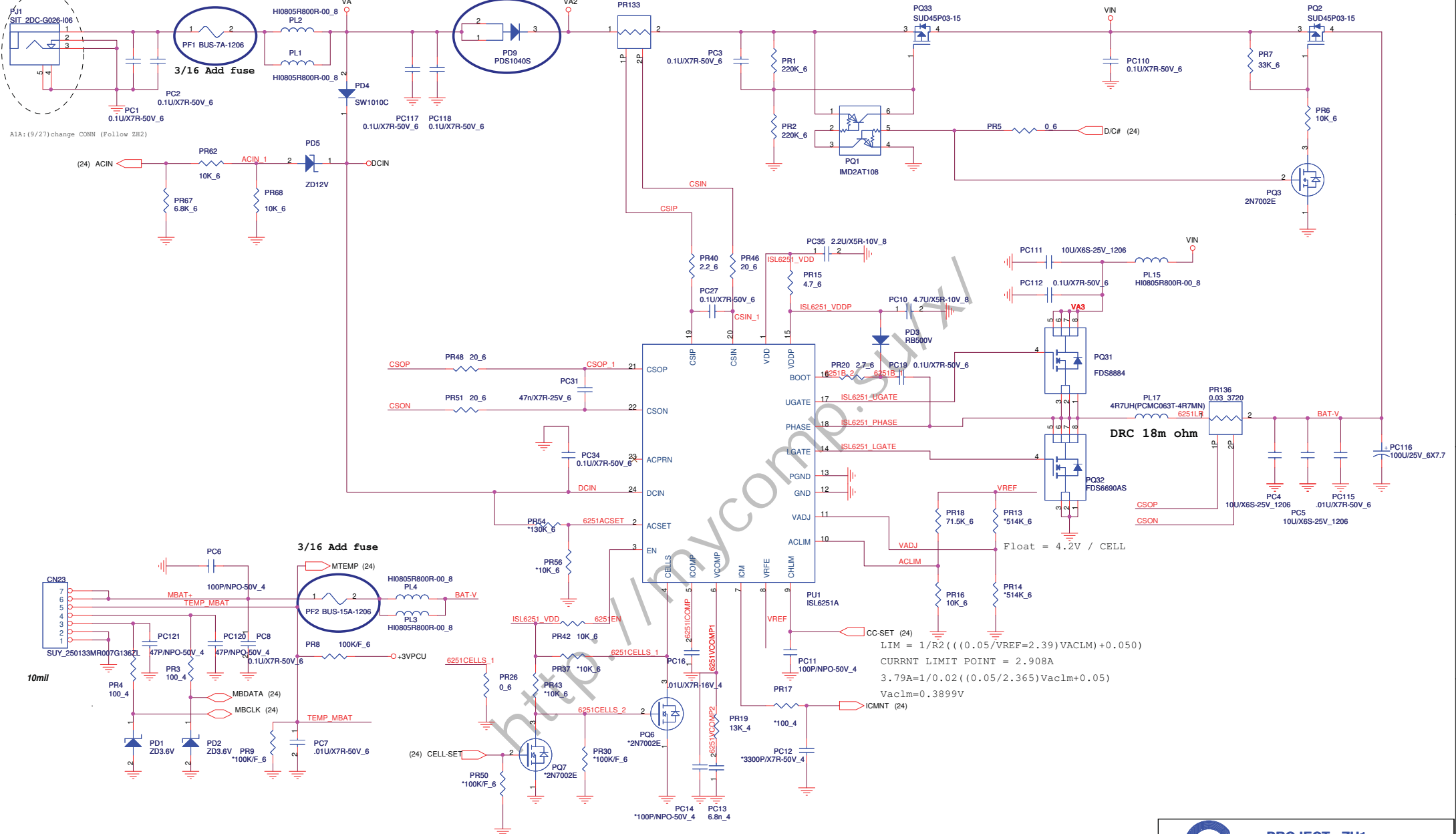
<http://mycomp.su/x/>



<http://mycomp.su/xl/>



3/16 Modify PD9 Footprint from SBM1040-3P to SBM1040-3P-ZU1



A1A: (9/27) change CONN (Follow ZH2)

10mil

CELL-SET = Hi ----> Cells = VDD ---->4S
 CELL-SET = Low ----> Cells = GND ---->3S

CC-SET (24)
 LIM = 1/R2 ((0.05/VREF=2.39) VACLIM) + 0.050
 CURRNT LIMIT POINT = 2.908A
 3.79A = 1/0.02 ((0.05/2.365) VACLIM + 0.05)
 VACLIM = 0.3899V

PROJECT : ZU1
Quanta Computer Inc.

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	Charger (ISL6251)	1D
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