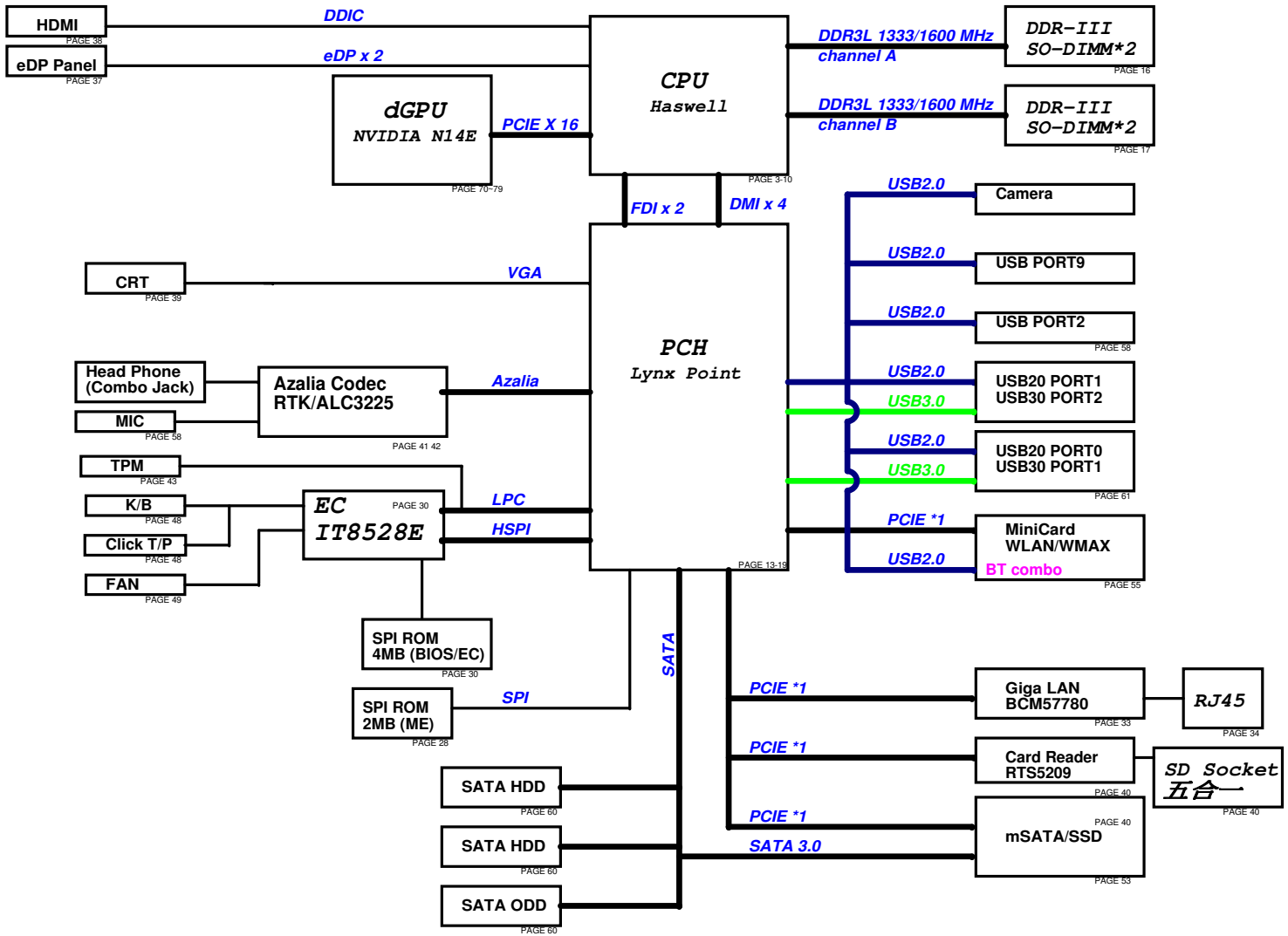
VA70HW BLOCK DIAGRAM



POWER

CPU VCORE PAGE 80
SYSTEM, +3V, +5V PAGE 81
+VCCP & +VCCP_VT PAGE 82
DDR & VTT PAGE 83
2.5V & 1.5VS &1.1VS PAGE 84
SMART CHARGER PAGE 88
POWER DETECT PAGE 90
LOAD SWITCH PAGE 91
POWER PROTECT PAGE 92

VGA POWER

GPU VCORE PAGE 80
+1.05VS_VGA
+3VS_VGA
+12VS_VGA
LOAD SWITCH PAGE 91
POWER PROTECT PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	VS
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4	ON	ON	ON	OFF
S5/ AC	ON	ON	ON	OFF
S5/ DC	ON	ON	OFF	OFF

PCIe Port

PCIE_P1	CARDREADER
PCIE_P2	mSATA
PCIE_P3	Mini CARD (WLAN)
PCIE_P4	LAN
PCIE_P5	
PCIE_P6	

USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	External DB
USB P03	
USB P04	
USB P05	WiFi
USB P08	Camera
USB P09	External DB
USB P10	BT
USB P11	PCIE/mSATA
USB P12	
USB P13	

SATA PORT

SATA P0	HDD 1
SATA P1	
SATA P2	ODD
SATA P3	
SATA P4	mSATA
SATA P5	HDD 2

IO BOARD

USB PORT3	HP_OUT
USB PORT9	MIC IN

PWR BOARD

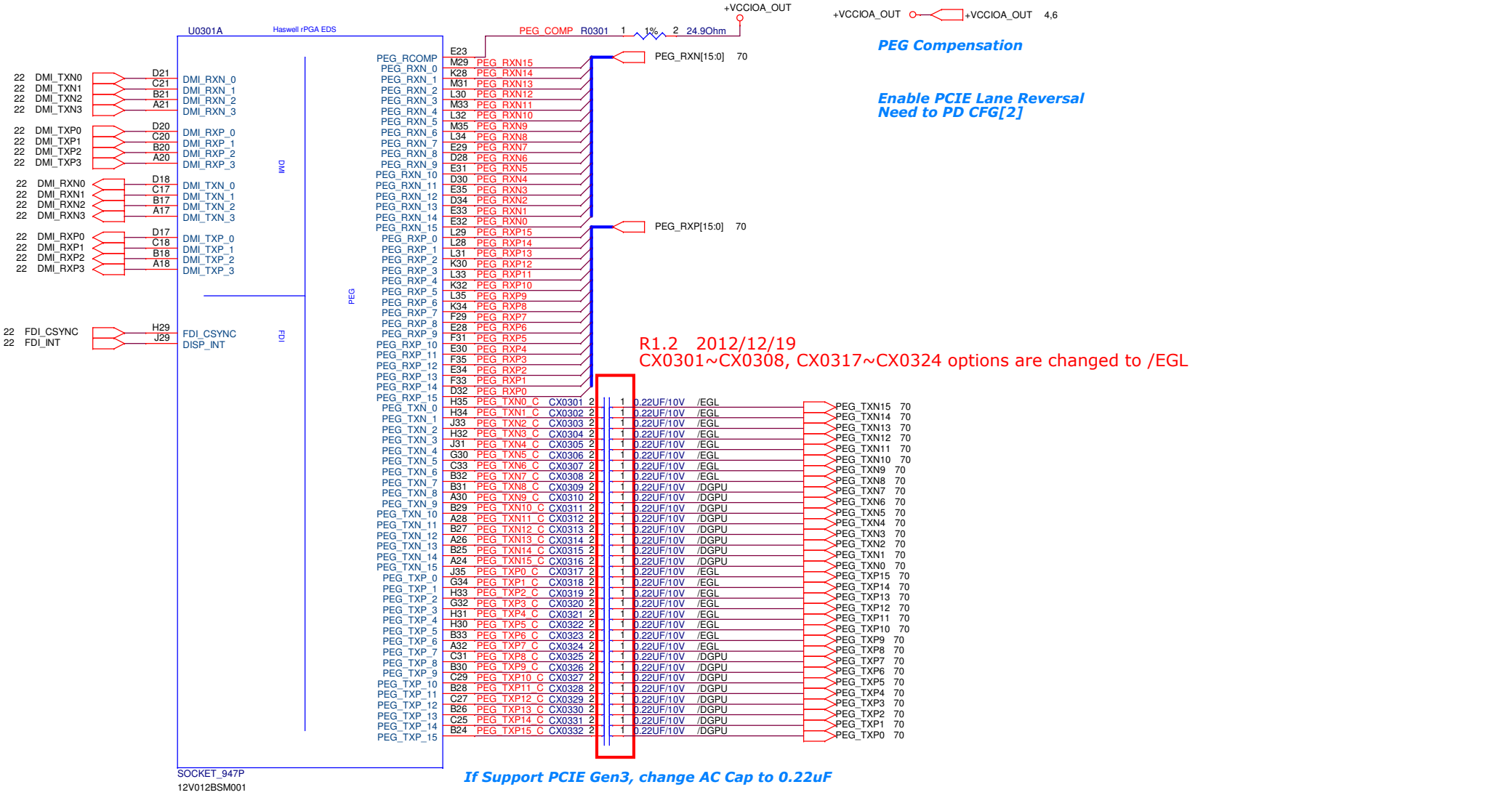
- POWER Button
- POWER LED
- LID SW

PEGATRON Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Monday, February 04, 2013 Sheet 1 of 96



PEGATRON

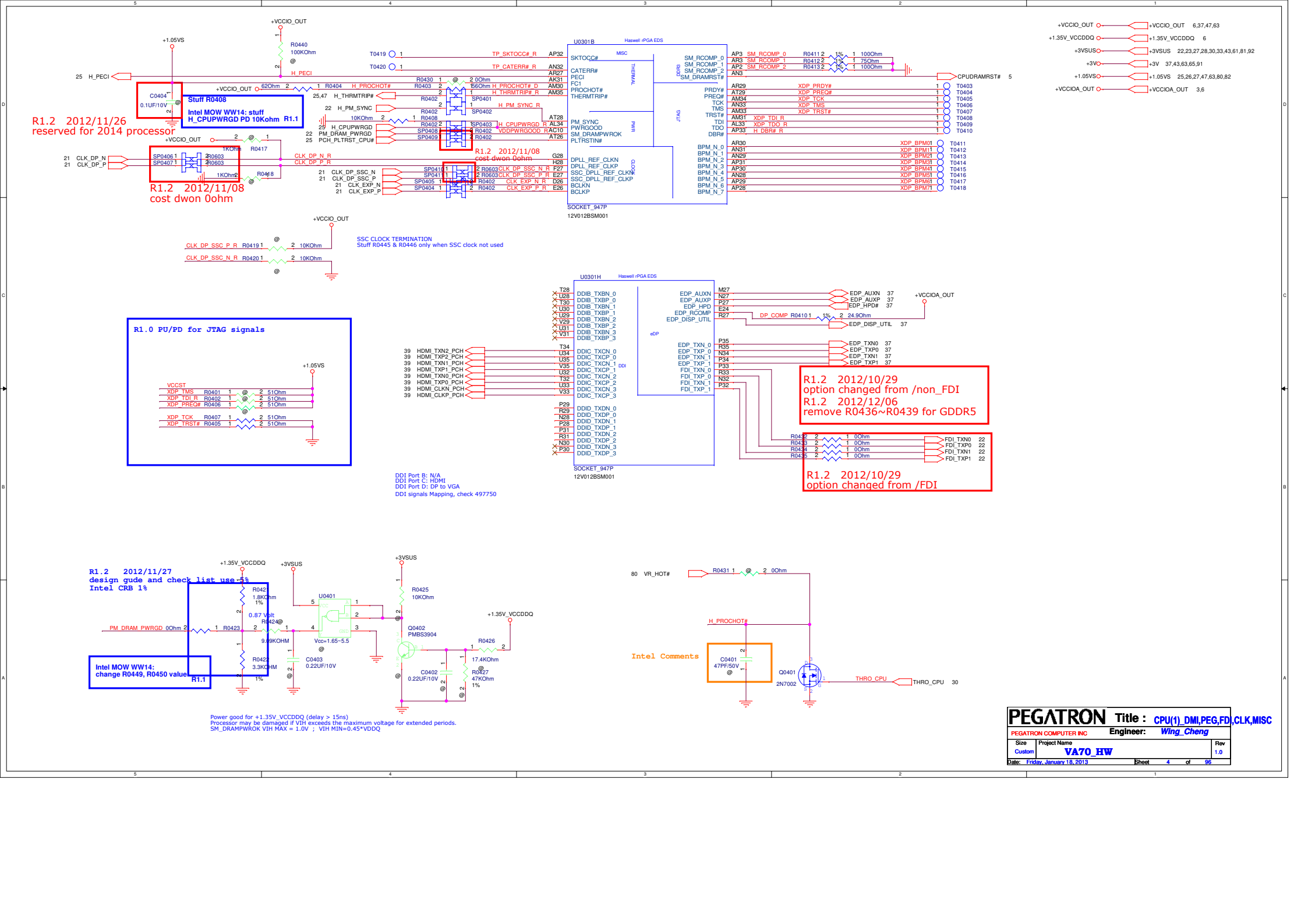
Title : CPU(1)_DMI,PEG,FDI,CLK,MISC

PEGATRON COMPUTER INC

Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 3 of 96


+VCCIO_OUT
+1.05VS
R0440
100KOhm
H_PECI
C0404
0.1UF/10V
Stuff R0408
Intel MOW WW14: stuff
H_CPUPWRGD PD 10Kohm R1.1
R1.2 2012/11/26
reserved for 2014 processor
R0404 62Ohm H_PROCHOT#
H_THRMTRIP#
H_PM_SYNC
H_CPUPWRGD
PM_DRAM_PWRGD
PCH_PLTRST_CPU#
R0417 1KOhm
R0418 1KOhm
CLK_DP_N
CLK_DP_P
R1.2 2012/11/08
cost dwon 0ohm
CLK_DP_SSC_N
CLK_DP_SSC_P
CLK_EXP_N
CLK_EXP_P
R1.2 2012/11/08
cost dwon 0ohm
U0301B
Haswell rPGA EDS
SOCKET_947P
12V012BSM001
SSC CLOCK TERMINATION
Stuff R0445 & R0446 only when SSC clock not used
CLK_DP_SSC_P_R R0419 10KOhm
CLK_DP_SSC_N_R R0420 10KOhm
R1.0 PU/PD for JTAG signals
VCCST
XDP_TMS R0401 51Ohm
XDP_TDI_R R0402 51Ohm
XDP_PREQ# R0406 51Ohm
XDP_TCK R0407 51Ohm
XDP_TRST# R0405 51Ohm
U0301H
Haswell rPGA EDS
SOCKET_947P
12V012BSM001
HDMI_TXN2_PCH
HDMI_TXP2_PCH
HDMI_TXN1_PCH
HDMI_TXP1_PCH
HDMI_TXN0_PCH
HDMI_TXP0_PCH
HDMI_CLKN_PCH
HDMI_CLKP_PCH
DDI Port B: N/A
DDI Port C: HDMI
DDI Port D: DP to VGA
DDI signals Mapping, check 497750
DP_COMP R0410 24.9Ohm
EDP_AUXN
EDP_AUXP
EDP_HPD#
EDP_DISP_UTIL
EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove R0436~R0439 for GDDR5
R0432 0Ohm
R0433 0Ohm
R0434 0Ohm
R0435 0Ohm
FDI_TXN0
FDI_TXP0
FDI_TXN1
FDI_TXP1
R1.2 2012/10/29
option changed from /FDI
R1.2 2012/11/27
design gude and check list use 5%
Intel CRB 1%
+1.35V_VCCDDQ
+3VSUS
R0423 9.09KOHM
R0424 0.87 Volt
R0422 3.3KOHM
U0401
Vcc=1.65~5.5
C0403 0.22UF/10V
R0425 10KOhm
Q0402 PMBS3904
R0426 17.4KOhm
C0402 0.22UF/10V
R0427 47KOhm
Intel MOW WW14:
change R0449, R0450 value
R1.1
Power good for +1.35V_VCCDDQ (delay > 15ns)
Processor may be damaged if VIH exceeds the maximum voltage for extended periods.
SM_DRAMPWROK VIH MAX = 1.0V ; VIH MIN=0.45*VDDQ
VR_HOT#
R0431 0Ohm
H_PROCHOT#
Intel Comments
C0401 47PF/50V
Q0401 2N7002
THRO_CPU
+VCCIO_OUT 6,37,47,63
+1.35V_VCCDDQ 6
+3VSUS 22,23,27,28,30,33,43,61,81,92
+3V 37,43,63,65,91
+1.05VS 25,26,27,47,63,80,82
+VCCIOA_OUT 3,6
PEGATRON
Title : CPU(1)_DMI,PEG,FDI,CLK,MISC
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 4 of 96

+1.35V +1.35V 6,16,18,63,83

R0520,R0521 must be grounded.
CRB 0.7

16 M_A_DQ[63:0]

Haswell rPGA EDS U0301C

M_A_DQ0	AR15	SA_DQ_0	RSVD_AC7	AC7	
M_A_DQ1	AT14	SA_DQ_1	SA_CK_N_0	U4	M_A_DIM0_CLK_DDR#0 16
M_A_DQ2	AM14	SA_DQ_2	SA_CK_P_0	V4	M_A_DIM0_CLK_DDR0 16
M_A_DQ3	AN14	SA_DQ_3	SA_CKE_0	AD9	M_A_DIM0_CKE0 16
M_A_DQ4	AT15	SA_DQ_4	SA_CK_N_1	U3	M_A_DIM0_CLK_DDR#1 16
M_A_DQ5	AR14	SA_DQ_5	SA_CK_P_1	V3	M_A_DIM0_CLK_DDR1 16
M_A_DQ6	AN15	SA_DQ_6	SA_CKE_1	AC9	M_A_DIM0_CKE1 16
M_A_DQ7	AM15	SA_DQ_7	SA_CK_N_2	U2	M_A_DIM0_CLK_DDR#2 16
M_A_DQ8	AM9	SA_DQ_8	SA_CK_P_2	V2	M_A_DIM0_CLK_DDR2 16
M_A_DQ9	AN9	SA_DQ_9	SA_CKE_2	AD8	M_A_DIM0_CKE2 16
M_A_DQ10	AM8	SA_DQ_10	SA_CK_N_3	U1	M_A_DIM0_CLK_DDR#3 16
M_A_DQ11	AN8	SA_DQ_11	SA_CK_P_3	V1	M_A_DIM0_CLK_DDR3 16
M_A_DQ12	AR9	SA_DQ_12	SA_CKE_3	AC8	M_A_DIM0_CKE3 16
M_A_DQ13	AT9	SA_DQ_13			
M_A_DQ14	AR8	SA_DQ_14	SA_CS_N_0	M7	M_A_DIM0_CS#0 16
M_A_DQ15	AT8	SA_DQ_15	SA_CS_N_1	L9	M_A_DIM0_CS#1 16
M_A_DQ16	AJ9	SA_DQ_16	SA_CS_N_2	M9	M_A_DIM0_CS#2 16
M_A_DQ17	AK9	SA_DQ_17	SA_CS_N_3	M10	M_A_DIM0_CS#3 16
M_A_DQ18	AJ6	SA_DQ_18	SA_ODT_0	M8	M_A_DIM0_ODT0 16
M_A_DQ19	AK6	SA_DQ_19	SA_ODT_1	L7	M_A_DIM0_ODT1 16
M_A_DQ20	AJ10	SA_DQ_20	SA_ODT_2	L8	M_A_DIM0_ODT2 16
M_A_DQ21	AK10	SA_DQ_21	SA_ODT_3	L10	M_A_DIM0_ODT3 16
M_A_DQ22	AJ7	SA_DQ_22	SA_BS_0	V5	M_A_BS0 16
M_A_DQ23	AK7	SA_DQ_23	SA_BS_1	U5	M_A_BS1 16
M_A_DQ24	AF4	SA_DQ_24	SA_BS_2	AD1	M_A_BS2 16
M_A_DQ25	AF5	SA_DQ_25			
M_A_DQ26	AF1	SA_DQ_26	VSS1	V10	
M_A_DQ27	AF2	SA_DQ_27	SA_RAS#	U6	M_A_RAS# 16
M_A_DQ28	AG4	SA_DQ_28	SA_WE#	U7	M_A_WE# 16
M_A_DQ29	AG5	SA_DQ_29	SA_CAS#	U8	M_A_CAS# 16
M_A_DQ30	AG1	SA_DQ_30			M_A_A[15:0] 16
M_A_DQ31	AG2	SA_DQ_31	SA_MA_0	V8	M_A_A0
M_A_DQ32	J1	SA_DQ_32	SA_MA_1	AC6	M_A_A1
M_A_DQ33	J2	SA_DQ_33	SA_MA_2	V9	M_A_A2
M_A_DQ34	J5	SA_DQ_34	SA_MA_3	U9	M_A_A3
M_A_DQ35	H5	SA_DQ_35	SA_MA_4	AC5	M_A_A4
M_A_DQ36	H2	SA_DQ_36	SA_MA_5	AC4	M_A_A5
M_A_DQ37	H1	SA_DQ_37	SA_MA_6	AD6	M_A_A6
M_A_DQ38	J4	SA_DQ_38	SA_MA_7	AC3	M_A_A7
M_A_DQ39	H4	SA_DQ_39	SA_MA_8	AD5	M_A_A8
M_A_DQ40	F2	SA_DQ_40	SA_MA_9	AC2	M_A_A9
M_A_DQ41	F1	SA_DQ_41	SA_MA_10	V6	M_A_A10
M_A_DQ42	D2	SA_DQ_42	SA_MA_11	AC1	M_A_A11
M_A_DQ43	D3	SA_DQ_43	SA_MA_12	AD4	M_A_A12
M_A_DQ44	D1	SA_DQ_44	SA_MA_13	V7	M_A_A13
M_A_DQ45	F3	SA_DQ_45	SA_MA_14	AD3	M_A_A14
M_A_DQ46	C3	SA_DQ_46	SA_MA_15	AD2	M_A_A15
M_A_DQ47	B3	SA_DQ_47			
M_A_DQ48	B5	SA_DQ_48			
M_A_DQ49	E6	SA_DQ_49	SA_DQS_N_0	AP15	M_A_DQS#0
M_A_DQ50	A5	SA_DQ_50	SA_DQS_N_1	AP6	M_A_DQS#1
M_A_DQ51	D6	SA_DQ_51	SA_DQS_N_2	AJ8	M_A_DQS#2
M_A_DQ52	D5	SA_DQ_52	SA_DQS_N_3	AF3	M_A_DQS#3
M_A_DQ53	E5	SA_DQ_53	SA_DQS_N_4	J3	M_A_DQS#4
M_A_DQ54	B6	SA_DQ_54	SA_DQS_N_5	E2	M_A_DQS#5
M_A_DQ55	A6	SA_DQ_55	SA_DQS_N_6	C5	M_A_DQS#6
M_A_DQ56	E12	SA_DQ_56	SA_DQS_N_7	C11	M_A_DQS#7
M_A_DQ57	D12	SA_DQ_57	SA_DQS_P_0	AP14	M_A_DQS0
M_A_DQ58	B11	SA_DQ_58	SA_DQS_P_1	AP9	M_A_DQS1
M_A_DQ59	A11	SA_DQ_59	SA_DQS_P_2	AK8	M_A_DQS2
M_A_DQ60	E11	SA_DQ_60	SA_DQS_P_3	AG3	M_A_DQS3
M_A_DQ61	D11	SA_DQ_61	SA_DQS_P_4	H3	M_A_DQS4
M_A_DQ62	B12	SA_DQ_62	SA_DQS_P_5	E3	M_A_DQS5
M_A_DQ63	A12	SA_DQ_63	SA_DQS_P_6	C6	M_A_DQS6
	AM3	SM_VREF	SA_DQS_P_7	C12	M_A_DQS7
	F16	SA_DIMM_VREFDQ			
	F13	SB_DIMM_VREFDQ			

SOCKET_947P
12V012BSM001

M_A_DQS#[7:0] 16
M_A_DQS[7:0] 16

17 M_B_DQ[63:0]

Haswell rPGA EDS U0301D

M_B_DQ0	AR18	SB_DQ_0	RSVD1	AG8	
M_B_DQ1	AT18	SB_DQ_1	SB_CKN0	Y4	M_B_DIM0_CLK_DDR#0 17
M_B_DQ2	AM17	SB_DQ_2	SB_CK0	AA4	M_B_DIM0_CLK_DDR0 17
M_B_DQ3	AM18	SB_DQ_3	SB_CKE_0	AF10	M_B_DIM0_CKE0 17
M_B_DQ4	AR17	SB_DQ_4	SB_CKN1	Y3	M_B_DIM0_CLK_DDR#1 17
M_B_DQ5	AT17	SB_DQ_5	SB_CK1	AA3	M_B_DIM0_CLK_DDR1 17
M_B_DQ6	AN17	SB_DQ_6	SB_CKE_1	AG10	M_B_DIM0_CKE1 17
M_B_DQ7	AN18	SB_DQ_7	SB_CKN2	Y2	M_B_DIM0_CLK_DDR#2 17
M_B_DQ8	AT12	SB_DQ_8	SB_CK2	AA2	M_B_DIM0_CLK_DDR2 17
M_B_DQ9	AR12	SB_DQ_9	SB_CKE_2	AG9	M_B_DIM0_CKE2 17
M_B_DQ10	AN12	SB_DQ_10	SB_CKN3	Y1	M_B_DIM0_CLK_DDR#3 17
M_B_DQ11	AM11	SB_DQ_11	SB_CK3	AA1	M_B_DIM0_CLK_DDR3 17
M_B_DQ12	AT11	SB_DQ_12	SB_CKE_3	AF9	M_B_DIM0_CKE3 17
M_B_DQ13	AR11	SB_DQ_13			
M_B_DQ14	AM12	SB_DQ_14	SB_CS_N_0	P4	M_B_DIM0_CS#0 17
M_B_DQ15	AN11	SB_DQ_15	SB_CS_N_1	R2	M_B_DIM0_CS#1 17
M_B_DQ16	AR5	SB_DQ_16	SB_CS_N_2	P3	M_B_DIM0_CS#2 17
M_B_DQ17	AR6	SB_DQ_17	SB_CS_N_3	P1	M_B_DIM0_CS#3 17
M_B_DQ18	AM5	SB_DQ_18			
M_B_DQ19	AM6	SB_DQ_19	SB_ODT_0	R4	M_B_DIM0_ODT0 17
M_B_DQ20	AT5	SB_DQ_20	SB_ODT_1	R3	M_B_DIM0_ODT1 17
M_B_DQ21	AT6	SB_DQ_21	SB_ODT_2	R1	M_B_DIM0_ODT2 17
M_B_DQ22	AN5	SB_DQ_22	SB_ODT_3	P2	M_B_DIM0_ODT3 17
M_B_DQ23	AN6	SB_DQ_23	SB_BS_0	R7	M_B_BS0 17
M_B_DQ24	AL4	SB_DQ_24	SB_BS_1	P8	M_B_BS1 17
M_B_DQ25	AK4	SB_DQ_25	SB_BS_2	AA9	M_B_BS2 17
M_B_DQ26	AJ1	SB_DQ_26			
M_B_DQ27	AJ2	SB_DQ_27	VSS2	R10	
M_B_DQ28	AM1	SB_DQ_28	SB_RAS#	R6	M_B_RAS# 17
M_B_DQ29	AN1	SB_DQ_29	SB_WE#	P6	M_B_WE# 17
M_B_DQ30	AK2	SB_DQ_30	SB_CAS#	P7	M_B_CAS# 17
M_B_DQ31	AK1	SB_DQ_31			M_B_A[15:0] 17
M_B_DQ32	L2	SB_DQ_32	SB_MA_0	R8	M_B_A0
M_B_DQ33	M2	SB_DQ_33	SB_MA_1	Y5	M_B_A1
M_B_DQ34	L4	SB_DQ_34	SB_MA_2	Y10	M_B_A2
M_B_DQ35	M4	SB_DQ_35	SB_MA_3	AA5	M_B_A3
M_B_DQ36	L1	SB_DQ_36	SB_MA_4	Y7	M_B_A4
M_B_DQ37	M1	SB_DQ_37	SB_MA_5	AA6	M_B_A5
M_B_DQ38	L5	SB_DQ_38	SB_MA_6	Y6	M_B_A6
M_B_DQ39	M5	SB_DQ_39	SB_MA_7	AA7	M_B_A7
M_B_DQ40	G7	SB_DQ_40	SB_MA_8	Y8	M_B_A8
M_B_DQ41	J8	SB_DQ_41	SB_MA_9	AA10	M_B_A9
M_B_DQ42	G8	SB_DQ_42	SB_MA_10	R9	M_B_A10
M_B_DQ43	G9	SB_DQ_43	SB_MA_11	Y9	M_B_A11
M_B_DQ44	J7	SB_DQ_44	SB_MA_12	AF7	M_B_A12
M_B_DQ45	J9	SB_DQ_45	SB_MA_13	P9	M_B_A13
M_B_DQ46	G10	SB_DQ_46	SB_MA_14	AA8	M_B_A14
M_B_DQ47	J10	SB_DQ_47	SB_MA_15	AG7	M_B_A15
M_B_DQ48	A8	SB_DQ_48			
M_B_DQ49	B8	SB_DQ_49			
M_B_DQ50	A9	SB_DQ_50	SB_DQS_N_0	AP18	M_B_DQS#0
M_B_DQ51	B9	SB_DQ_51	SB_DQS_N_1	AP11	M_B_DQS#1
M_B_DQ52	D8	SB_DQ_52	SB_DQS_N_2	AP5	M_B_DQS#2
M_B_DQ53	E8	SB_DQ_53	SB_DQS_N_3	AJ3	M_B_DQS#3
M_B_DQ54	D9	SB_DQ_54	SB_DQS_N_4	L3	M_B_DQS#4
M_B_DQ55	E9	SB_DQ_55	SB_DQS_N_5	H9	M_B_DQS#5
M_B_DQ56	E15	SB_DQ_56	SB_DQS_N_6	C8	M_B_DQS#6
M_B_DQ57	D15	SB_DQ_57	SB_DQS_N_7	C14	M_B_DQS#7
M_B_DQ58	A15	SB_DQ_58	SB_DQS_P_0	AP17	M_B_DQS0
M_B_DQ59	B15	SB_DQ_59	SB_DQS_P_1	AP12	M_B_DQS1
M_B_DQ60	E14	SB_DQ_60	SB_DQS_P_2	AP6	M_B_DQS2
M_B_DQ61	D14	SB_DQ_61	SB_DQS_P_3	AK3	M_B_DQS3
M_B_DQ62	A14	SB_DQ_62	SB_DQS_P_4	M3	M_B_DQS4
M_B_DQ63	B14	SB_DQ_63	SB_DQS_P_5	H8	M_B_DQS5
			SB_DQS_P_6	C9	M_B_DQS6
			SB_DQS_P_7	C15	M_B_DQS7

SOCKET_947P
12V012BSM001

M_B_DQS#[7:0] 17
M_B_DQS[7:0] 17

R1.2 2012/11/08
cost dwon 0ohm

18 DIMM_VREF_CA

DRAMRST_CNTRL_PCH

SP0501 R0603 Q0501 2N7002

16,18 DIMM0_VREF_DQ

R1.2 2012/11/28
cost dwon 0ohm

SP0502 R0603 Q0502 UM6K1N/31DTN

DRAMRST_CNTRL_PCH

DDR_CA_VREF
DDR_WR_VREF01
DDR_WR_VREF02

R0515 1KOhm 1% @
R0509 1KOhm 1% @
R0510 1KOhm 1% @

SP0503 R0603 Q0502 UM6K1N/31DTN

DRAMRST_CNTRL_PCH

R1.2 2012/11/28
cost dwon 0ohm

17,18 DIMM1_VREF_DQ

CPU driven VREF path is stuffed by default
CRB 0.7

R1.0 S3 circuit:- DRAM_RST# to memory should be high during S3

+1.35V
R0507 1KOhm @

0614-change Q0501 from UM6K1N to 2N7002

R0501 0Ohm

R1.0 0209
Change R0508 to 1K ohm
R0508 close to DIMM

16,17 DDR3_DRAMRST# R0508 1KOhm CPUDRAMRST# R

@ Q0501 2N7002

CPUDRAMRST# 4

@ R0506 1% 4.99KOhm

21 DRAMRST_CNTRL_PCH

@ C0501 0.047UF/16V

Reserve S3 power reduction schematic

If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

5. Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

7. Unmount R2232, R2231, Q2203

PEGATRON	Title : CPU(2)_DDR3		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 5	of 96	

Decoupling guide from Intel (SPEC)
VDDQ 22uF * 11 pcs (stuff)
10uF * 10 pcs (stuff)
330uF * 2 pcs (stuff)

Decoupling guide from Intel (EE)
VDDQ 22uF * 2pcs (stuff)
10uF * 2pcs (stuff)
330uF * 1pcs (stuff)

Decoupling guide from Intel (SPEC)
+VCORE 10uF * 11pcs (stuff)
22uF * 19pcs (stuff)
470uF * 4pcs (stuff)

Decoupling guide from Intel (EE)
+VCORE 10uF * 11 pcs (stuff)
22uF * 19 pcs (stuff)
470uF * 5 pcs (stuff)

+1.35V_VCCDDQ — +1.35V_VCCDDQ 4
+1.35V — +1.35V 5,16,18,63,83
+VCORE — +VCORE 9,63,80
+VCCIO_OUT — +VCCIO_OUT 4,37,47,63
+VCCIO2PCH — +VCCIO2PCH 27
+VCCIOA_OUT — +VCCIOA_OUT 3,4

Default: no support
S3 power reduction

+VCCIO_OUT(1---1.05V) output from CPU

Unstuff R0622
Intel MOW WW09: renamed
VCCIO2PCH to RSVD R1.1

Placement note:
1. R0602 close to CPU
2. R0603 close to CPU
3. R0605 close to VR
4. R0608 close to CPU
5. R0607 close to VR
6. R0611 close to CPU

R1.2 2012/11/16
follow Intel CRB
Place as close to CPU as possible
R1.2 2012/11/26
follow design guide

R1.2 2012/11/08
cost dwon 0ohm

Power team suggestion

If XDP not implemented, then Route Processor PWR_DEBUG as a test point.
This Test point must be clearly labeled(shark bay schematic check list 497750)

Cap of 470UF or more place at power schematic

U0301E — Haswell rPGA EDS — SOCKET_947P — 12V012BSM001

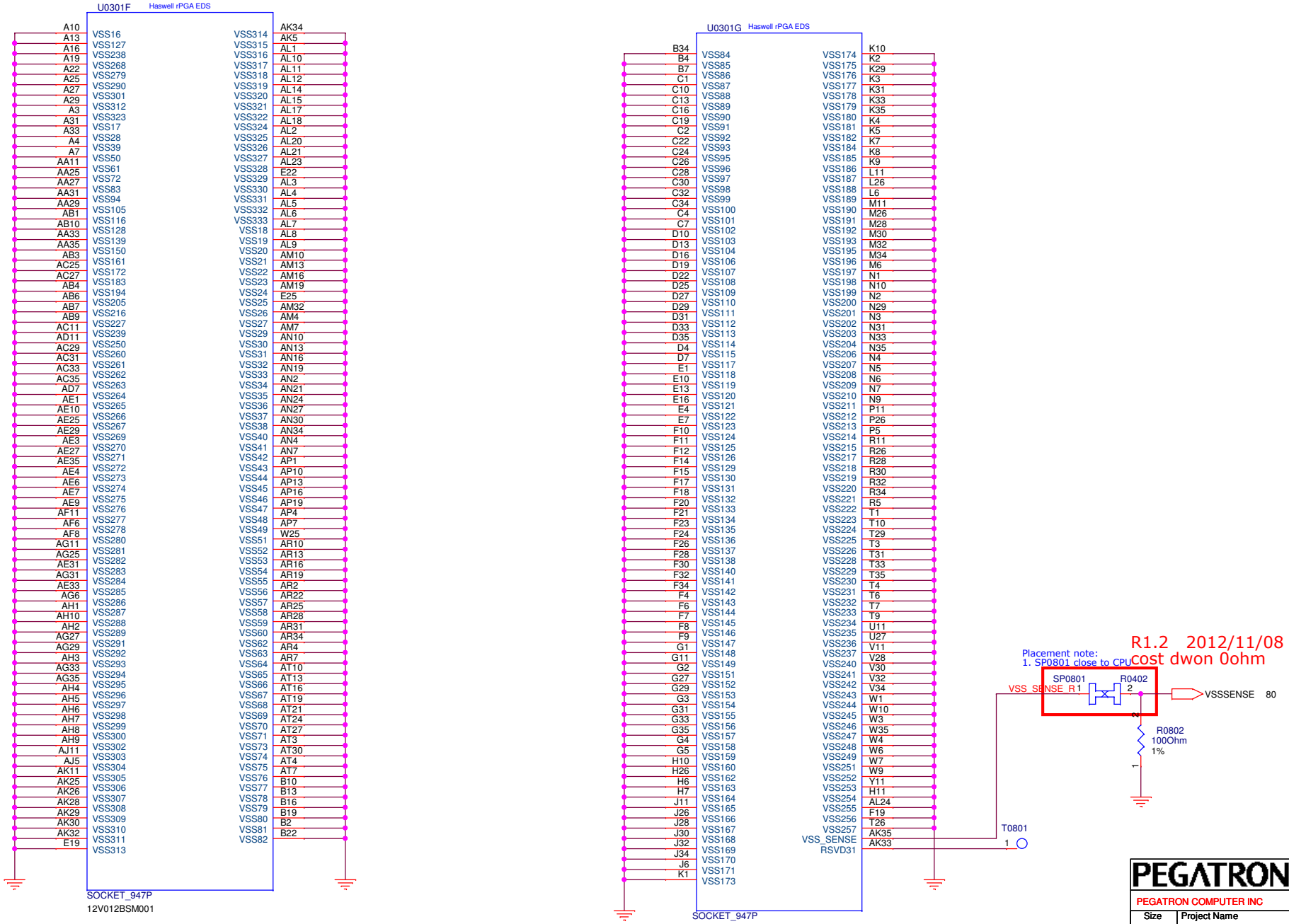
PEGATRON	Title :	CPU(4)_PWR	
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng	
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 6	of 98	

PEGATRON Title : CPU(4)_PWR

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 7 of 96



PEGATRON	Title : CPU(3)_CFG,RSVD,GND
PEGATRON COMPUTER INC	Engineer: Wing_Cheng
Size: B	Project Name: VA70_HW
Rev: 1.0	
Date: Friday, January 18, 2013	Sheet 8 of 96

CFG strapping information: The CFG signals have a default value of '1'

CFG[1:0]: Reserved configuration lane.

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

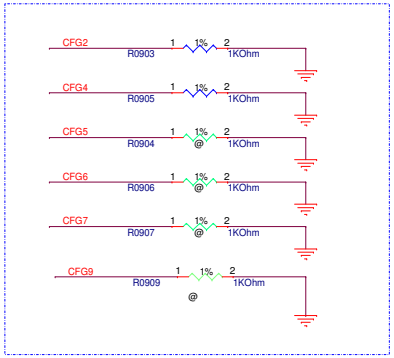
CFG[4]: eDP enable

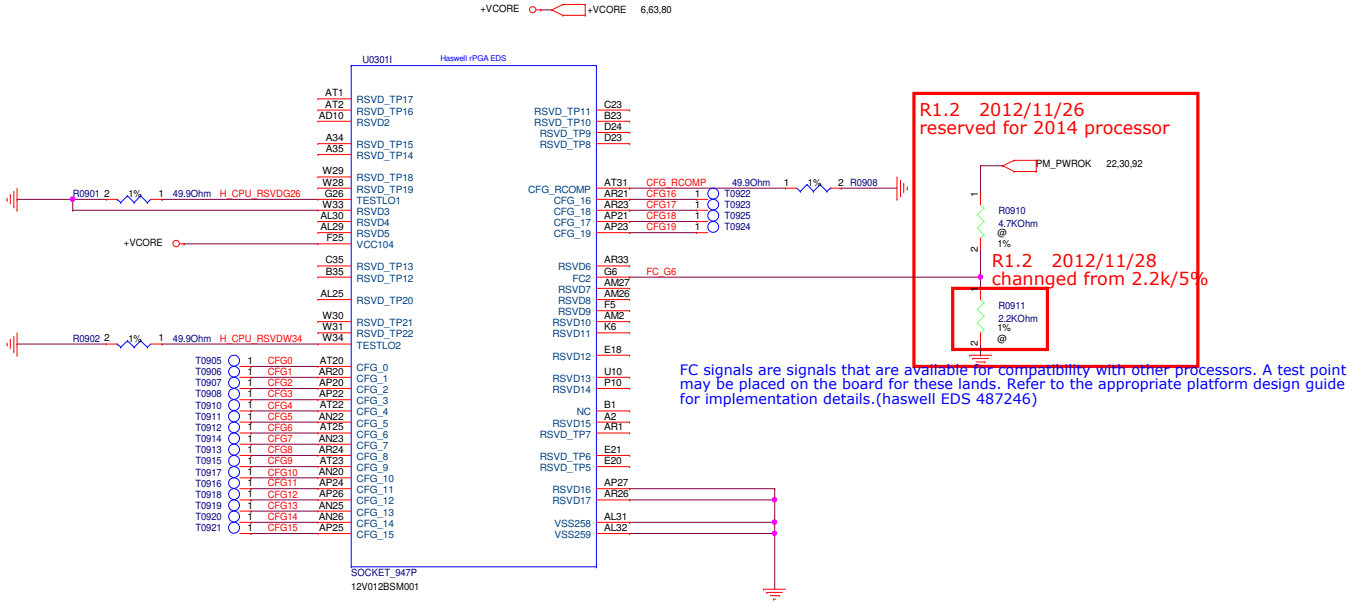
-1 = Disabled
-0 = Enabled

CFG[6:5]: PCI Express Port Bifurcation Straps

-00 = 1 x8, 2 x4 PCI Express*
-01 = reserved
-10 = 2 x8 PCI Express*
-11 = 1 x16 PCI Express*

CFG[19:7]: Reserved configuration lane.





FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.(haswell EDS 487246)

PEGATRON COMPUTER INC

Title : CPU(3)_CFG,RSVD,GND

Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 9 of 96

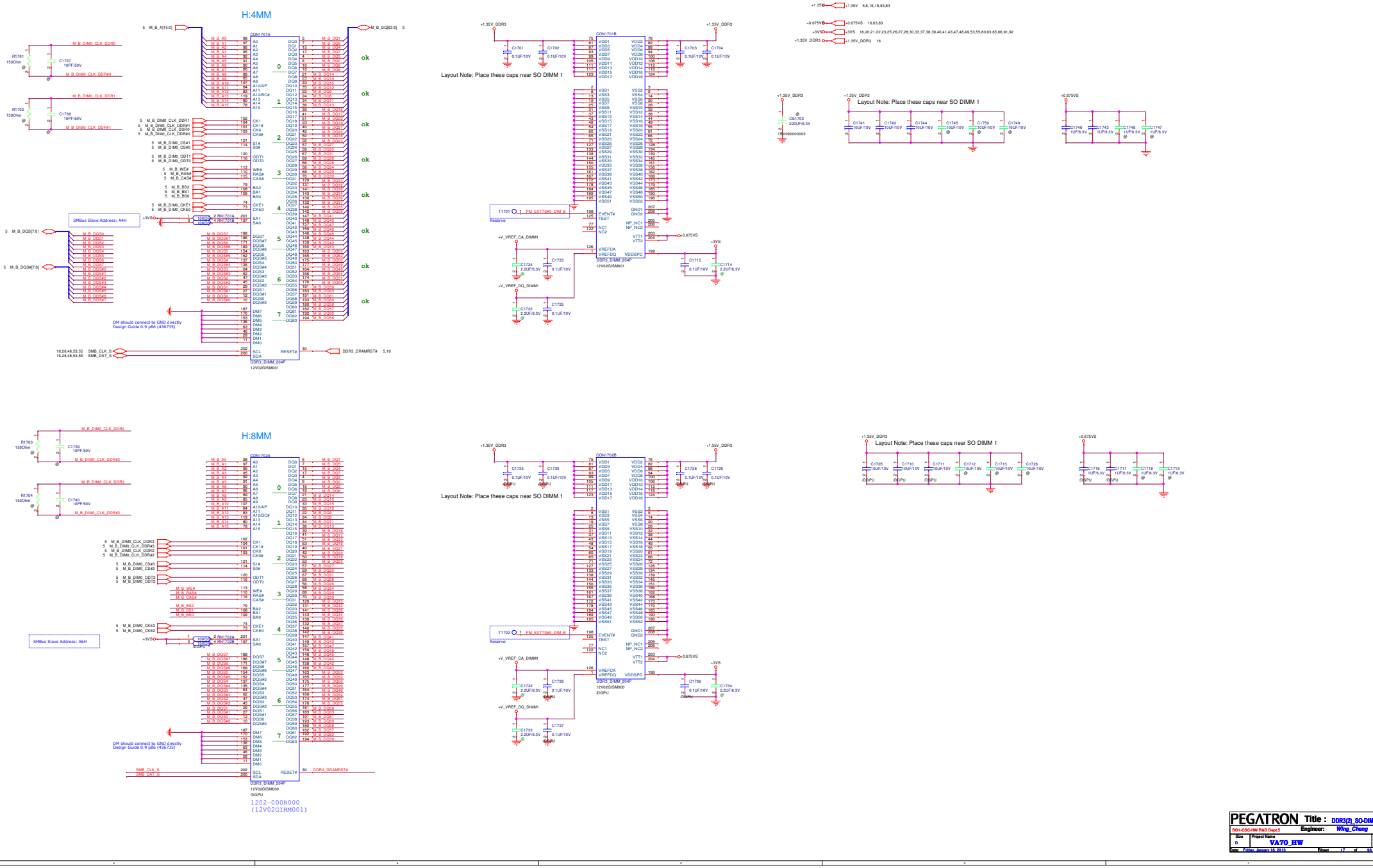
PEGATRON Title : NB(3)_****

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 10 of 96

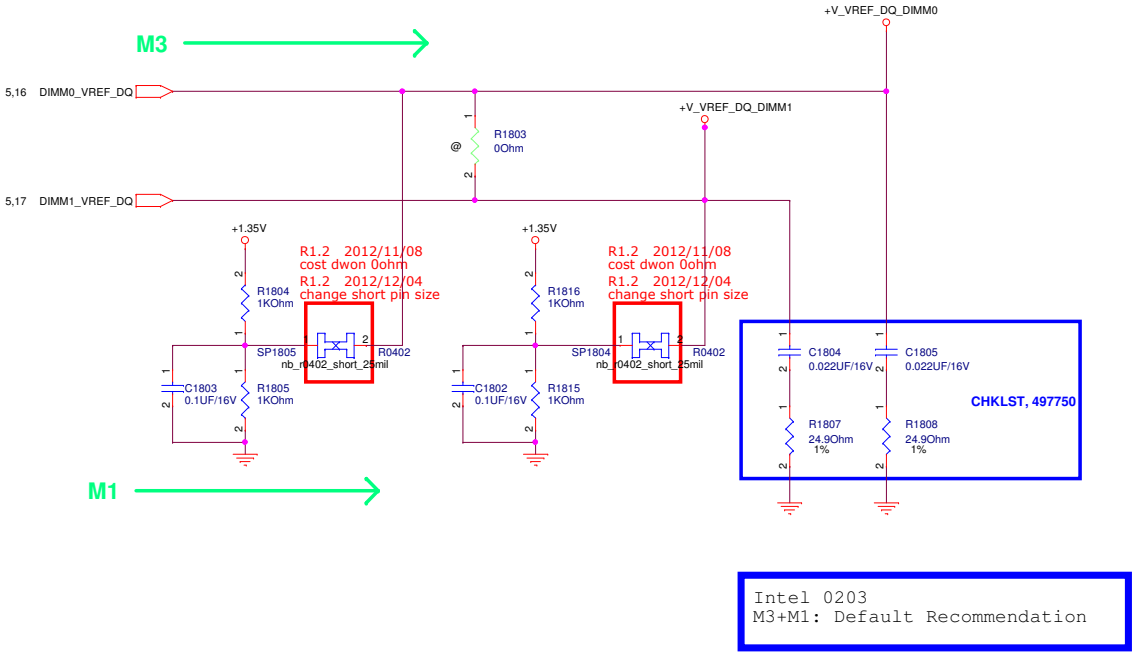

R1.2 2012/11/20
Part ref. changed
H:4mm
R1.2 2012/11/20
Part ref. changed
H:8mm
Layout Note: Place these caps near SO DIMM 0
SMBus Slave Address: A0H
SMBus Slave Address: A2H
DM should connect to GND directly
Design Guide 0.9 p86 (436735)
DDR3_DRAMRST#
SMB_CLK_S
SMB_DAT_S
/DGPU
ok


H:4MM
H:8MM
Layout Note: Place these caps near SO DIMM 1
SMBus Slave Address: A4H
SMBus Slave Address: A6H
DM should connect to GND directly
Design Guide 0.9 p86 (436735)
1202-000R000
(12V02GIRM001)
PEGATRON
Title : DDR3(2)_SO-DIMM1
Engineer: Wing_Cheng
Project Name VA70_HW
Rev 1.0
Sheet 17 of 96

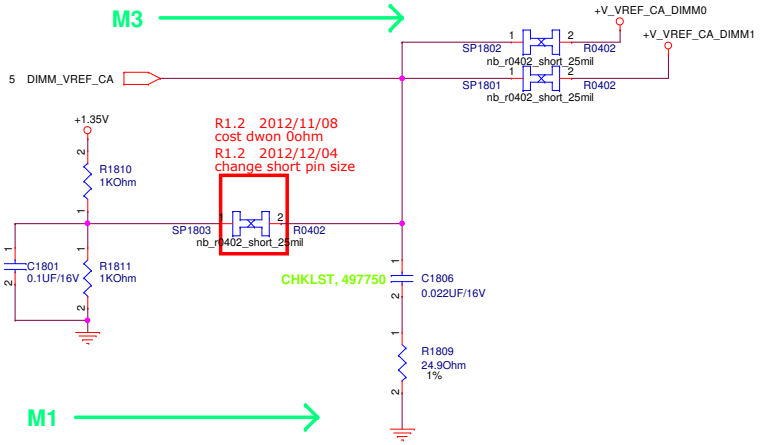
DDR3L Vref

+1.35V_DDR3 → +1.35V_DDR3 16,17
+V_VREF_CA_DIMM0 → +V_VREF_CA_DIMM0 16
+V_VREF_DQ_DIMM0 → +V_VREF_DQ_DIMM0 5,16
+V_VREF_CA_DIMM1 → +V_VREF_CA_DIMM1 17
+V_VREF_DQ_DIMM1 → +V_VREF_DQ_DIMM1 5,17

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



Intel 0203
M3+M1: Default Recommendation



PEGATRON Title : DDR3(3)_CA/DQ Voltage
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size: Custom | Project Name: VA70_HW | Rev: 1.0
Date: Friday, January 18, 2013 Sheet 18 of 96

R1.4--2

PEGATRON Title : VID Controller

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 19 of 96

RTC battery

R1.2 2012/11/06
工廠要求增加

+RTCBAT, T2011, T2010, +3VA, D2001, +VCC_RTC, T2012, +RTC_BAT, R2001 1KOhm, 1V/0.2A, C2003 1UF/6.3V, U2001 BATT_HOLDER_2P, GND

R1.0 0110
增加點膠點

12V20GBSM000

Connector Type 1217-001L000

+VCC_RTC → +VCC_RTC 22,27
+3VA → +3VA 27,30,63,65,81,88,93
+3VS → +3VS 16,17,21,22,23,25,26,27,28,30,33,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
+3VSUS_ORG → +3VSUS_ORG 21,22,24,25,26,27
+12VS → +12VS 28,39,41,63,91
+1.5VS → +1.5VS 21,22,24,26,27,41,53,55,63,84
+VTT_PCH_VCCIO → +VTT_PCH_VCCIO 26,27

+VCC_RTC
RTCRST# RC delay should be 18ms~25ms
R2018 5% 20KOhm, C2005 1UF/6.3V, JRST2001 SGL_JUMP @, GND
R2023 1MOhm, R2021 5% 20KOhm, C2004 1UF/6.3V, JRST2002 SGL_JUMP @, GND

TPM Settings	JRST2001
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Request by CSC for CMOS clear function

CMOS Settings	JRST2002
Clear CMOS	Shunt
Keep CMOS	Open (Default)

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs
PCH_INTVRMEN 330KOhm 1% @ R2028 GND

C2001 15PF/50V, 1RTC_X1_C, SP2002 R0402, X2001 32.768KHZ, R2002 10MOhm, C2002 15PF/50V, 07V000000003, GND

T2005, T2007, T2006, +VCC_RTC, R2020 330KOhm 1%

U2001A LPT_PCH_M_EDS

RTC_X1	B5	RTCX1	RTC
RTC_X2	B4	RTCX2	
SRTC_RST#	B9	SRTCRST#	
SM_INTRUDER#	A8	INTRUDER#	
PCH_INTVRMEN	G10	INTVRMEN	
RTC_RST#	D9	RTCRST#	
ACZ_BCLK	B25	HDA_BCLK	AZALIA
ACZ_SYNC	A22	HDA_SYNC	
	AL10	SPKR	
ACZ_RST#	C24	HDA_RST#	
	L22	HDA_SDI0	
	K22	HDA_SDI1	
	G22	HDA_SDI2	
	F22	HDA_SDI3	
ACZ_SDOUT	A24	HDA_SDO	
HDA_DOCK_EN#	B17	DOCKEN#/GPIO33	
	C22	HDA_DOCK_RST#/GPIO13	

41 ACZ_BCLK_AUD R2011 33Ohm
41 ACZ_SYNC_AUD R2012 33Ohm
41 SB_SPKR
41,42 ACZ_RST#_AUD R2015 33Ohm
41 ACZ_SDIN0_AUD

R1.2 2012/12/03
Add R2031
30 PCH_FLASH_DESCRIPTOR R2031 10KOhm
41 ACZ_SDOUT_AUD R2013 33Ohm
Remove TP

30 EXT_SCI# R2017 10KOhm +3VSUS_ORG
R1.1

T2001 PCH_JTAG_TCK_BUF AB3 JTAG_TCK
T2002 PCH_JTAG_TMS AD1 JTAG_TMS
T2003 PCH_JTAG_TDI AE2 JTAG_TDI
T2004 PCH_JTAG_TDO AD3 JTAG_TDO
R2027 0Ohm F8 TP25
C26 TP22
T2008 PM_TEST_RST_N AB6 TP20

R1.2 2012/11/28
follow Intel design guide

DH82LPMS
02V000000012

SATA_RXN0 / SATA_RXP0	BC8 / BE8	SATA_RXN0 60 / SATA_RXP0 60	HDD1
SATA_TXN0 / SATA_TXP0	AW8 / AY8	SATA_TXN0 60 / SATA_TXP0 60	
SATA_RXN1 / SATA_RXP1	BC10 / BE10		
SATA_TXN1 / SATA_TXP1	AV10 / AW10		
SATA_RXN2 / SATA_RXP2	BB9 / BD9	SATA_RXN2 60 / SATA_RXP2 60	ODD
SATA_TXN2 / SATA_TXP2	AY13 / AW13	SATA_TXN2 60 / SATA_TXP2 60	
SATA_RXN3 / SATA_RXP3	BC12 / BE12		
SATA_TXN3 / SATA_TXP3	AR13 / AT13		
SATA_RXN4 / SATA_RXP4	BD13 / BB13	SATA_RXN4 53 / SATA_RXP4 53	mSATA
SATA_TXN4 / SATA_TXP4	AV15 / AW15	SATA_TXN4 53 / SATA_TXP4 53	
SATA_RXN5 / SATA_RXP5	BC14 / BE14	SATA_RXN5 60 / SATA_RXP5 60	HDD2
SATA_TXN5 / SATA_TXP5	AP15 / AR15	SATA_TXN5 60 / SATA_TXP5 60	

R1.3 2013/1/11
mSATA move to port 4

SATA_RCOMP AY5 SATA_COMP R2026 7.5KOhm +1.5VS
SATALED# AP3 R2024 10KOhm +3VS SATA_LED# 66
SATA0GP/GPIO21 AT1 SATA_DET0_R_N T2009
SATA1GP/GPIO19 AU2 Int_PU BBS_BIT0_R SP2001 R0402 BBS_BIT0 23
SATA_IREF BD4
TP9 BA2 R2016 0Ohm +1.5VS
TP8 BB2

SATA0GP的pull up電阻：參考線路(43K ohm)和check list(10K ohm))寫的不同??先照參考線路

HDA_DKEN : Flash Descriptor Security Overide
H = Disabled (Default)
L = Enabled
Note : Rising edge of PWROK
JRST2003 1MM_OPEN_M1M2, HDA_DOCK_EN# R2030 1KOhm @

Strap information:

HDA_SPKR: No reboot strap
Low: Disable (Default)
High:Enable
SB_SPKR R2019 1KOhm @ +3VS

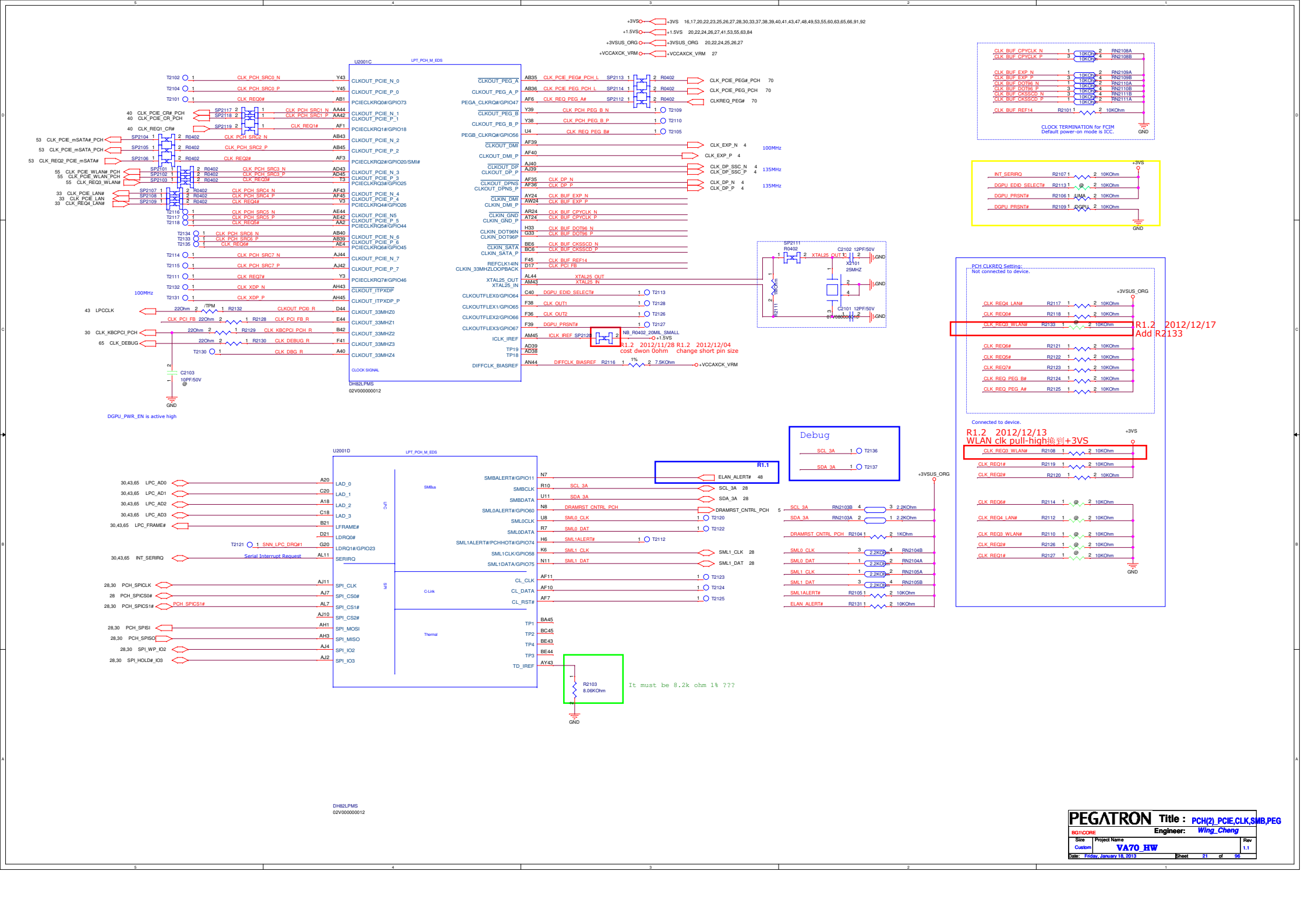
HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.HDA_SDO which sample high on the rising edge of PWROK
Will also disable Intel ME.
ACZ_SDOUT R2022 1KOhm @ +3VSUS_ORG

HDA_DOCK_EN#:
Reserved

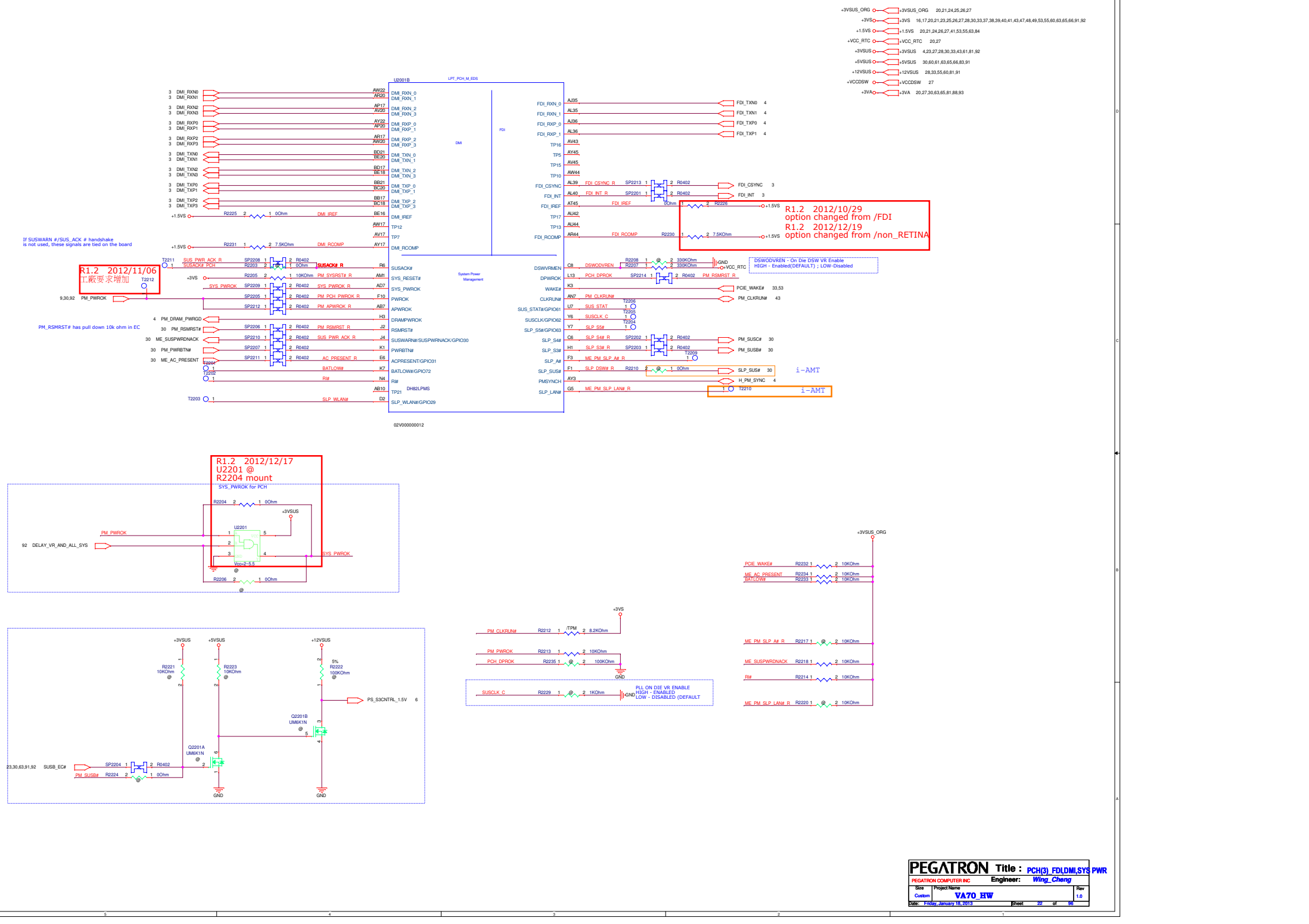
[0216] : ACZ_SYNC strap is no longer supported on LPT, by Intel FAE Stu.

+3VS
SATA_DET0_R_N R2025 10KOhm @

PEGATRON Title : PCH(1)_SATA,IHDA,RTC,LPC
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name VA70_HW | Rev 1.0
Date: Friday, January 18, 2013 | Sheet 20 of 96



PEGATRON	Title :	PCH(2)_PCIE,CLK,SMB,PEG	
BG1CORE	Engineer:	Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.1	
Date: Friday, January 18, 2013	Sheet 21 of 96		



PEGATRON	Title :	PCH(3)_FDI,DMI,SYS PWR	
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0	
Date: Friday, January 18, 2013	Sheet 22 of 86		

R1.2 2012/10/29
option changed from /non_FDI_@
R1.2 2012/12/06
remove R2335~R2337, R2339~R2341, JP2304~JP2306 for GDDR5

R1.2 2012/10/29
option changed from /FDI
R1.2 2012/12/19
option changed from /non_RETINA
R1.3 2013/1/8
R2332~R2334 are removed

R1.2 2012/10/29
option changed from /FDI
R1.2 2012/12/19
option changed from /non_RETINA

R1.2 2012/12/19
option changed from /non_RETINA

R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove R2338, R2329~R2331, R2349 for GDDR5

R1.2 2012/11/27
follow intel design guide

是否會浪費電?

R1.1

CRT Disable: (For discrete graphic)

1. NC:
   CRT_R,CRT_G,CRT_B
   CRT_HSYCN,CRT_VSYNC
2. 1KΩ+-5% pull-down to GND:
3. Connected to GND:
   CRT_ITRN
   DAC_IREF
4. Connect to +V3.3:
   VCCADAC

BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI **(PCH) DEFAULT**

Sampled on rising edge of PWROK.

R1.1

STP_A16OVR:
A16 swap override Strap/ Top-Block swap override jumper

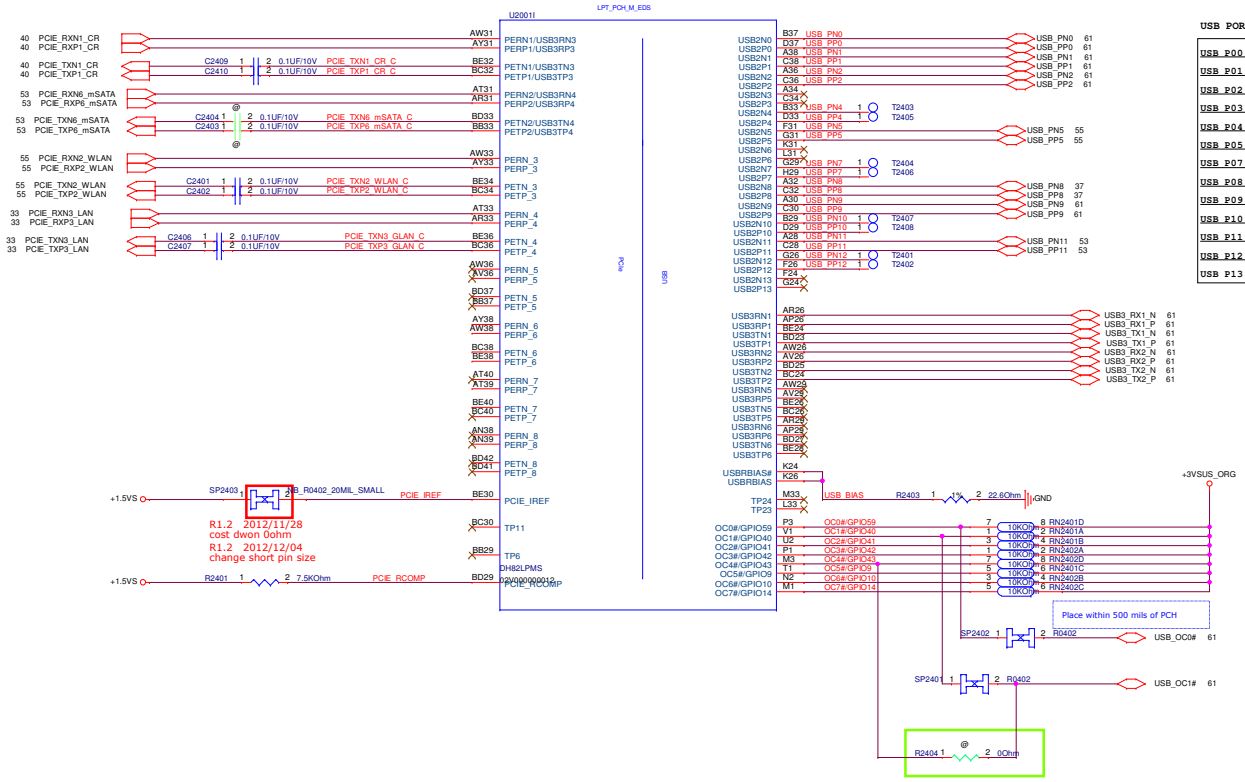
Low=Enabled A16 swap override/ Top-Block swap override
High=Default

Strap information:

There signals have a weak internal pull down

DDPB_CTRLDATA: "0" = Port is not detected; "1"= Port is detected
DDPC_CTRLDATA: "0" = Port is not detected; "1"= Port is detected
DDPD_CTRLDATA: "0" = Port is not detected; "1"= Port is detected

PEGATRON	Title :	PCH(4)_DP,LVDS,CRT	
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng	
Size: C	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 23 of 96		



R1.2 2012/11/28
cost dwon 0ohm
R1.2 2012/12/04
change short pin size

USB PORT

USB_P00	External 2.0/3.0
USB_P01	External 2.0/3.0
USB_P02	External 2.0
USB_P03	
USB_P04	
USB_P05	WiFi
USB_P07	
USB_P08	Camera
USB_P09	External 2.0
USB_P10	BT
USB_P11	PCIE/mSATA
USB_P12	
USB_P13	

+3VSUS 4,22,23,27,28,30,33,43,61,81,92
+3VS 16,17,20,21,22,23,25,26,27,28,30,33,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
+3V 37,43,63,65,91
+3VSUS_ORG 20,21,22,25,26,27
+12VS 28,39,41,63,91
+1.5VS 20,21,22,26,27,41,53,55,63,84

Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

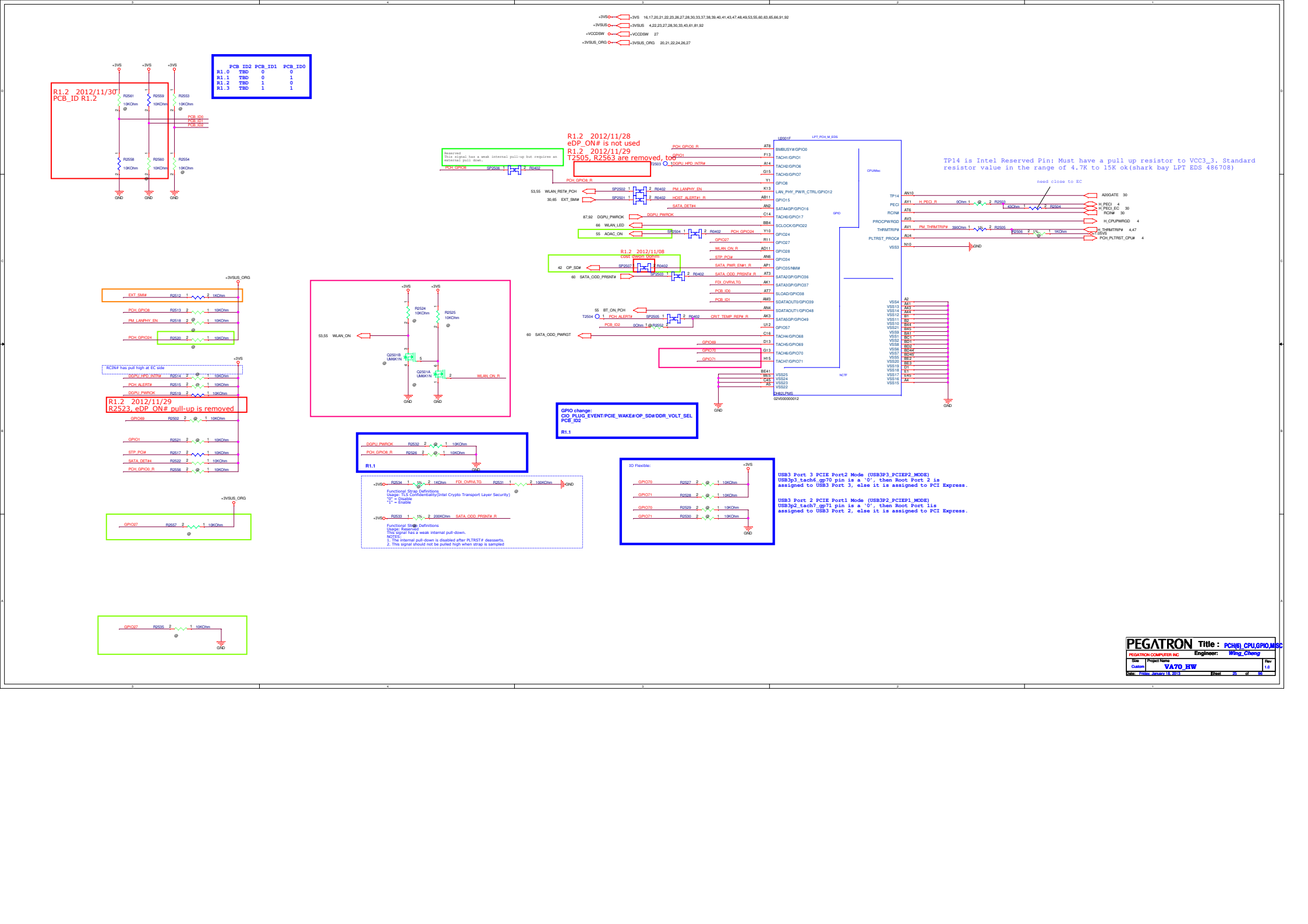
Table 1-5. Mobile Lynx Point SKUs Flexible I/O Map

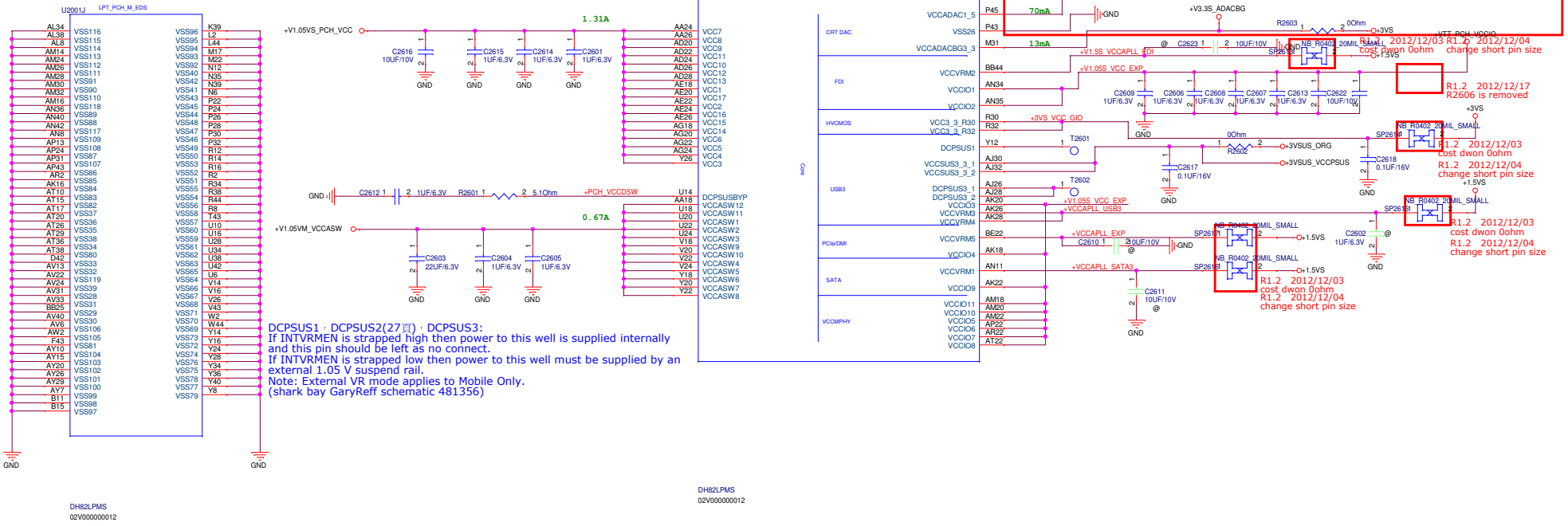
SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
QM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4	SATA 6Gb/s Port 5	SATA 3Gb/s Port 0	NA	SATA 3Gb/s Port 2	NA

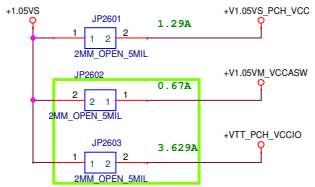
NOTES:

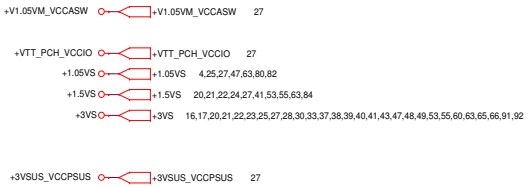
1. Ports listed with NA are not available and are disabled.

PEGATRON COMPUTER INC
Title : PCH(5)_PCI,NVRAM,USB
Engineer: Wing_Cheng
Size: Custom | Project Name: VA70_HW | Rev: 1.0
Date: Friday, January 18, 2013 | Sheet 24 of 96


+3VSO +3VS 16,17,20,21,22,23,26,27,28,30,33,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
+3VSUS +3VSUS 4,22,23,27,28,30,33,43,61,81,92
+VCCDSW +VCCDSW 27
+3VSUS_ORG +3VSUS_ORG 20,21,22,24,26,27
PCB_ID2 PCB_ID1 PCB_ID0
R1.0 TBD 0 0
R1.1 TBD 0 1
R1.2 TBD 1 0
R1.3 TBD 1 1
R1.2 2012/11/30
PCB_ID R1.2
R2561 10KOhm
R2559 10KOhm
R2553 10KOhm
R2558 10KOhm
R2560 10KOhm
R2554 10KOhm
PCB_ID0
PCB_ID1
PCB_ID2
GND
R1.2 2012/11/28
eDP_ON# is not used
R1.2 2012/11/29
T2505, R2563 are removed, too
Reserved
This signal has a weak internal pull-up but requires an external pull down.
PCH_GPIO6
SP2506
R2402
PCH_GPIO6_R
GPIO1
T2505
DGPU_HPD_INTR#
53,55 WLAN_RST#_PCH
30,65 EXT_SMI#
SP2502
SP2501
PM_LANPHY_EN
HOST_ALERT#1_R
SATA_DET#4
87,92 DGPU_PWROK
66 WLAN_LED
55 AOAC_ON
SP2504
PCH_GPIO24
GPIO27
WLAN_ON_R
STP_PCI#
SATA_PWR_EN#1_R
42 OP_SD#
60 SATA_ODD_PRSNT#
SP2507
SP2503
SATA_ODD_PRSNT#_R
FDI_OVRVLTG
PCB_ID0
PCB_ID1
R1.2 2012/11/08
cost down: 0ohm
55 BT_ON_PCH
T2504
PCH_ALERT#
SP2505
CRIT_TEMP_REP#_R
PCB_ID2
0Ohm
R2552
60 SATA_ODD_PWRGT
GPIO69
GPIO70
GPIO71
LPT_PCH_M_EDS
U2001F
BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
GPIO34
GPIO35/NMI#
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57
TACH4/GPIO68
TACH5/GPIO69
TACH6/GPIO70
TACH7/GPIO71
VSS25
VSS24
VSS23
VSS22
CHIPLEVEL
02V000000012
CPUMisc
GPIO
NCTF
TP14 is Intel Reserved Pin: Must have a pull up resistor to VCC3_3. Standard resistor value in the range of 4.7K to 15K ok(shark bay LPT EDS 486708)
need close to EC
AN10
AY1
AT6
AV3
AY1
AU4
N10
TP14
PECI
RCIN#
PROCPWRGD
THRMTRIP#
PLTRST_PROC#
VSS3
H_PECI_R
0Ohm
R2503
43Ohm
R2504
PM_THRMTRIP#
390Ohm
R2505
R2508
1KOhm
A20GATE 30
H_PECI 4
H_PECI_EC 30
RCIN# 30
H_CPUPWRGD 4
H_THRMTRIP# 4,47
PCH_PLTRST_CPU# 4
+1.05VS
GND
VSS4
VSS13
VSS14
VSS12
VSS11
VSS10
VSS21
VSS9
VSS1
VSS2
VSS8
VSS6
VSS7
VSS5
VSS20
VSS19
VSS18
VSS17
VSS16
VSS15
+3VSUS_ORG
EXT_SMI# R2512 1K0hm
PCH_GPIO8 R2513 10KOhm
PM_LANPHY_EN R2518 10KOhm
PCH_GPIO24 R2520 10KOhm
RCIN# has pull high at EC side
DGPU_HPD_INTR# R2514 10KOhm
PCH_ALERT# R2515 10KOhm
DGPU_PWROK R2519 10KOhm
R1.2 2012/11/29
R2523, eDP_ON# pull-up is removed
GPIO69 R2502 10KOhm
GPIO1 R2521 10KOhm
STP_PCI# R2517 10KOhm
SATA_DET#4 R2522 10KOhm
PCH_GPIO0_R R2556 10KOhm
GPIO27 R2557 10KOhm
+3VS
R2524 10KOhm
R2525 10KOhm
53,55 WLAN_ON
Q2501B UM6K1N
Q2501A UM6K1N
WLAN_ON_R
GND
DGPU_PWROK R2532 10KOhm
PCH_GPIO8_R R2526 10KOhm
R1.1
+3VSO R2534 1% 1KOhm FDI_OVRVLTG R2531 100KOhm GND
Functional Strap Definitions
Usage: TLS Confidentiality(Intel Crypto Transport Layer Security)
"0" = Disable
"1" = Enable
+3VSO R2533 1% 200KOhm SATA_ODD_PRSNT#_R
Functional Strap Definitions
Usage: Reserved
This signal has a weak internal pull-down.
NOTES:
1. The internal pull-down is disabled after PLTRST# deasserts.
2. This signal should not be pulled high when strap is sampled
GPIO change:
CIO_PLUG_EVENT/PCIE_WAKE#/OP_SD#/DDR_VOLT_SEL
PCB_ID2
R1.1
IO Flexible:
GPIO70 R2527 10KOhm
GPIO71 R2528 10KOhm
GPIO70 R2529 10KOhm
GPIO71 R2530 10KOhm
USB3 Port 3 PCIE Port2 Mode (USB3P3_PCIEP2_MODE)
USB3p3_tach6_gp70 pin is a '0', then Root Port 2 is assigned to USB3 Port 3, else it is assigned to PCI Express.
USB3 Port 2 PCIE Port1 Mode (USB3P2_PCIEP1_MODE)
USB3p2_tach7_gp71 pin is a '0', then Root Port 1is assigned to USB3 Port 2, else it is assigned to PCI Express.
GPIO27 R2535 10KOhm
PEGATRON
Title : PCH(6)_CPU,GPIO,MISC
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 16, 2015
Sheet 25 of 86





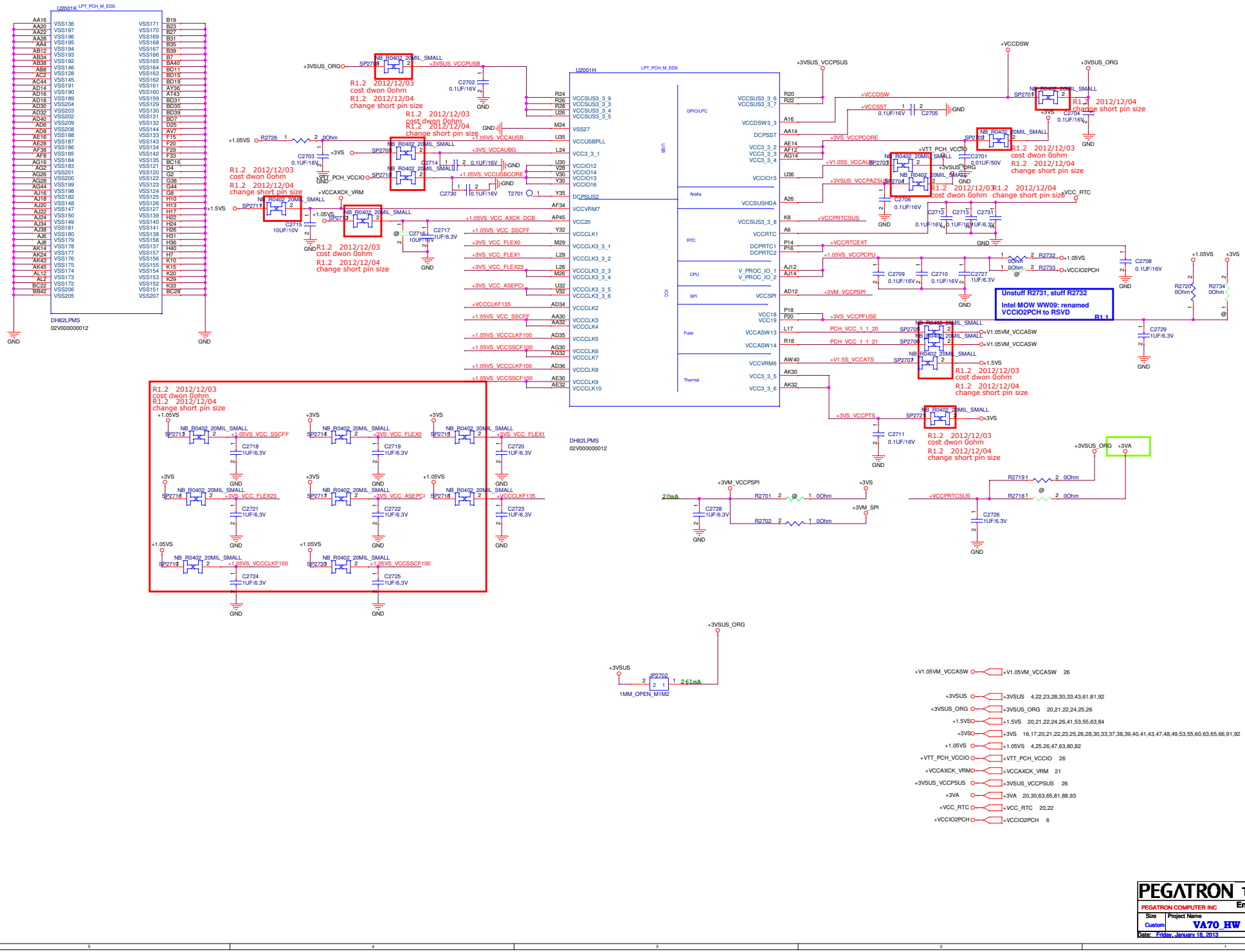


PEGATRON Title : PCH(7)_POWER,GND

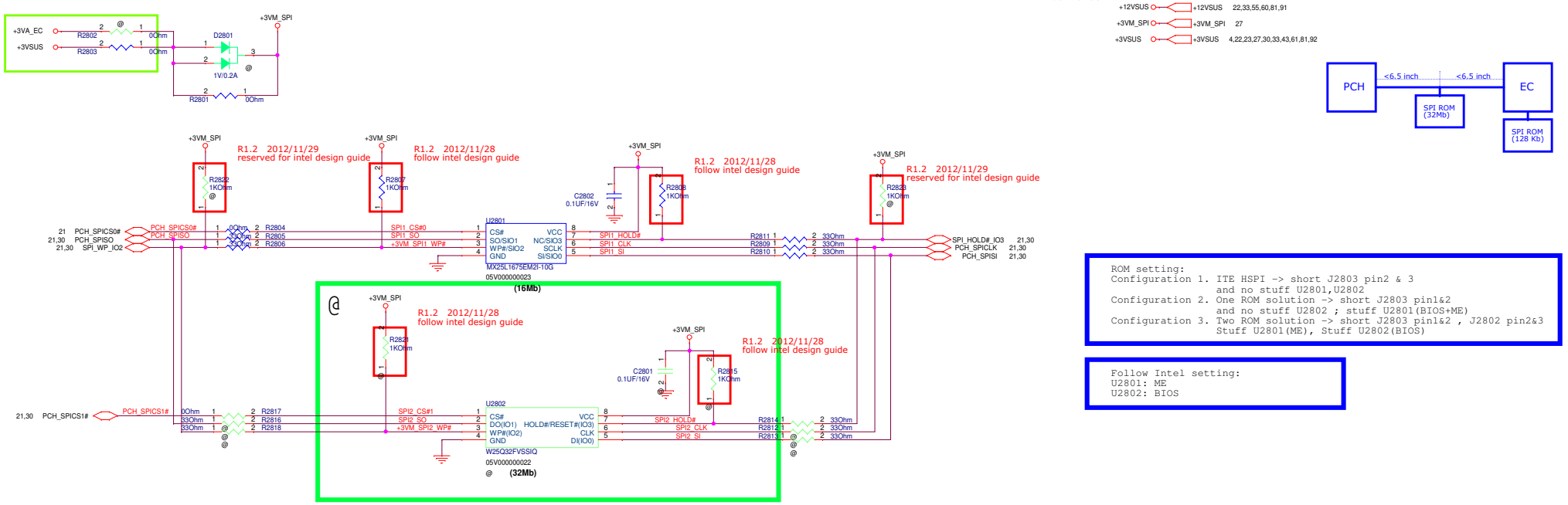
BG1\CORE Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.1

Date: Friday, January 18, 2013 Sheet 26 of 96


U2001K
LPT_PCH_M_EDS
DH82LPMS
02V000000012
U2001H
R1.2 2012/12/03
cost dwon 0ohm
R1.2 2012/12/04
change short pin size
Unstuff R2731, stuff R2732
Intel MOW WW09: renamed
VCCIO2PCH to RSVD
R1.1
PEGATRON
Title : PCH(8)_POWER,GND
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 27 of 96

PCH SPI ROM



R1.0 0106

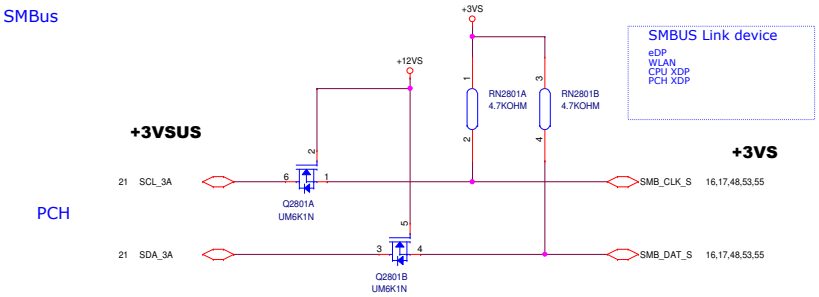
+3VS 16,17,20,21,22,23,25,26,27,30,33,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
+12VS 39,41,63,91
+12VSUS 22,33,55,60,81,91
+3VM_SPI 27
+3VSUS 4,22,23,27,30,33,43,61,81,92

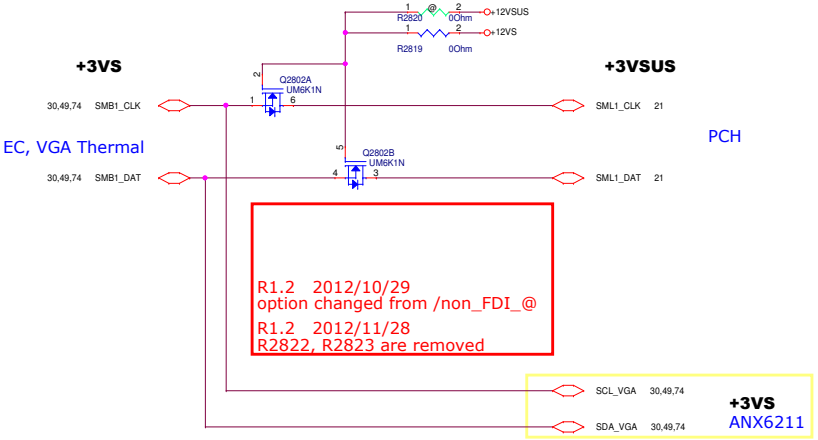
ROM setting:
Configuration 1. ITE HSPI -> short J2803 pin2 & 3
and no stuff U2801,U2802
Configuration 2. One ROM solution -> short J2803 pin1&2
and no stuff U2802 ; stuff U2801(BIOS+ME)
Configuration 3. Two ROM solution -> short J2803 pin1&2 , J2802 pin2&3
Stuff U2801(ME), Stuff U2802(BIOS)

Follow Intel setting:
U2801: ME
U2802: BIOS

SPI Debug Connector

PCH SMBus





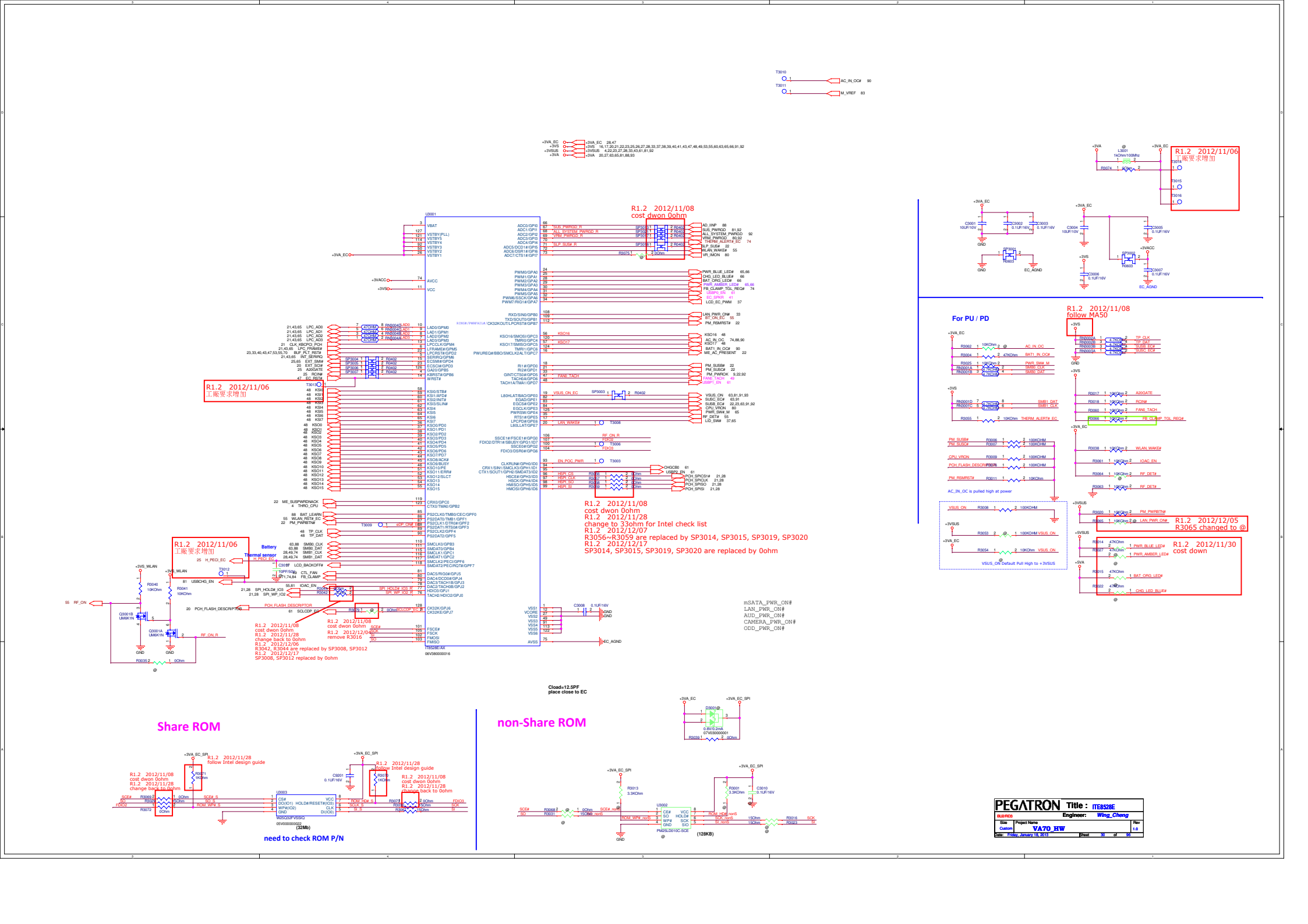
PEGATRON Title : PCH(9)_SPI,SMB
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name VA70_HW | Rev 1.0
Date: Friday, January 18, 2013 | Sheet 28 of 96

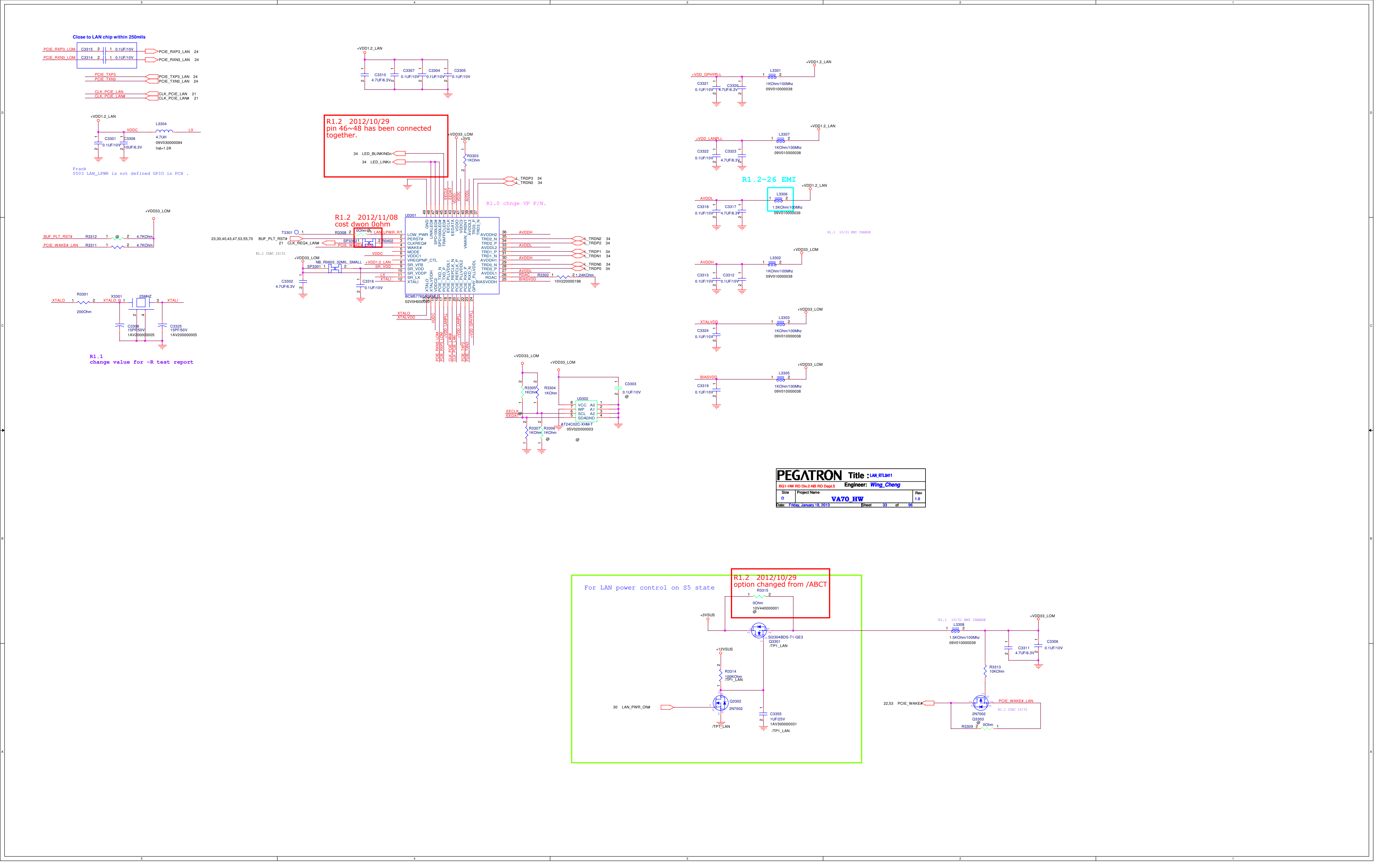
PEGATRON Title : CLK_ICS9LRS3197

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 29 of 96

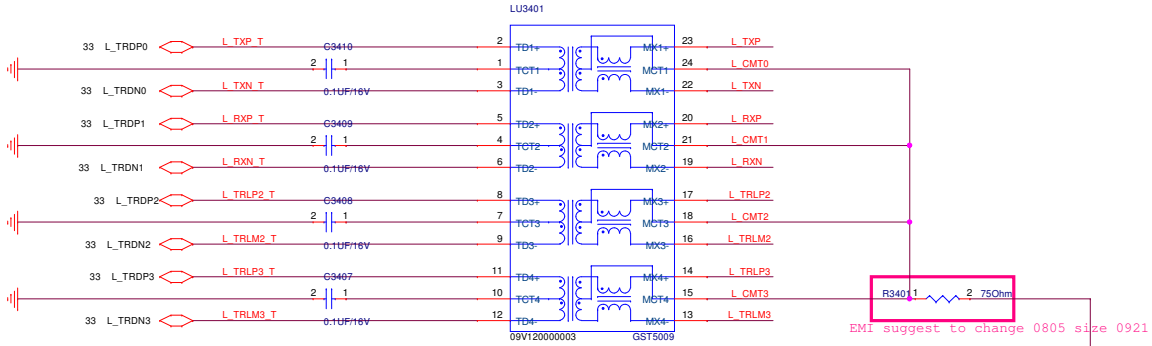

R1.2 2012/11/06
工廠要求增加
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/28
change to 33ohm for Intel check list
R1.2 2012/12/07
R3056~R3059 are replaced by SP3014, SP3015, SP3019, SP3020
R1.2 2012/12/17
SP3014, SP3015, SP3019, SP3020 are replaced by 0ohm
For PU / PD
R1.2 2012/11/08
follow MA50
R1.2 2012/12/05
R3065 changed to @
R1.2 2012/11/30
cost down
Battery
Thermal sensor
Share ROM
non-Share ROM
need to check ROM P/N
Cload=12.5PF
place close to EC
mSATA_PWR_ON#
LAN_PWR_ON#
AUD_PWR_ON#
CAMERA_PWR_ON#
ODD_PWR_ON#
PEGATRON
Title : ITE8528E
Engineer: Wing_Cheng
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 30 of 98



Close to LAN chip within 250mils
R1.2 2012/10/29
pin 46~48 has been connected together.
R1.2 2012/11/08
cost dwon 0ohm
R1.0 chnge VP P/N.
Frank
0503 LAN_LPWR is not defined GPIO in PCH .
R1.1
change value for -R test report
R1.2-26 EMI
R1.1 10/31 EMI CHANGE
R1.1 IOAC 10/31
U3301
BCM57786
U3302
AT24C02C-XHM-T
05V020000003
For LAN power control on S5 state
R1.2 2012/10/29
option changed from /ABCT
SI2304BDS-T1-GE3
Q3301
Q3302
2N7002
Q3303
30 LAN_PWR_ON#
22,53 PCIE_WAKE#
PCIE_WAKE#_LAN
PEGATRON
Title : LAN_RTL8411
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Wing_Cheng
Size D
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 33 of 96

FAE suggestion 1003

Co-Layout



R3401 1 2 75Ohm

EMI suggest to change 0805 size 0921

C3403 1500PF/2KV

LAN_GND

EMI Req

D3401 @ AZ2025-01H.R7G

R3402 1 2 0Ohm

10PF/50V C3404

10PF/50V C3405

10PF/50V C3406

LAN_GND

R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/12/04
change short pin size

+VDD33_LOM

SP3402 NB_R0402_20MIL_SMALL

510Ohm R3405 LED_LINKn LED_LINKn 33

C3402 470PF/50V @

LAN_GND

LAN_GND

LAN_JACK_8P

R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/12/04
change short pin size

+VDD33_LOM

SP3402 NB_R0402_20MIL_SMALL

L_TXP
L_TXN
L_RXP
L_TRLP2
L_TRLM2
L_RXN
L_TRLP3
L_TRLM3

P_GND1
P_GND2

CON3401 T2V23GBSD009

R3404 1 2 510Ohm LED_BLINKINGn 33

@ C3401 470PF/50V Close Connector

LAN_GND

LAN_GND

<Variant Name>

PEGATRON Title : RJ45/ RJ11

BG1-CSC-HW R&D Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 34 of 96

R1.2 2012/10/29
All components options changed from /non_FDI

R1.2 2012/12/06
remove U3501 for GDDR5

<Variant Name>

PEGATRON Title : DP to VGA

BG1-CSC-HW R&D Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 35 of 56

Initial Code EEPROM

PEGATRON Title : LVDS CONN

BU1-PD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 36 of 98

LVDS

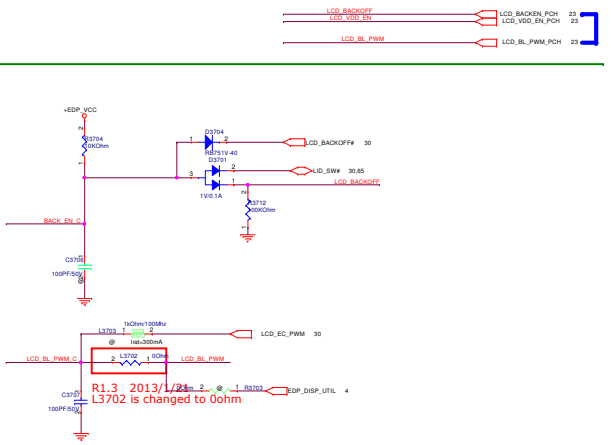
CH A

CH B

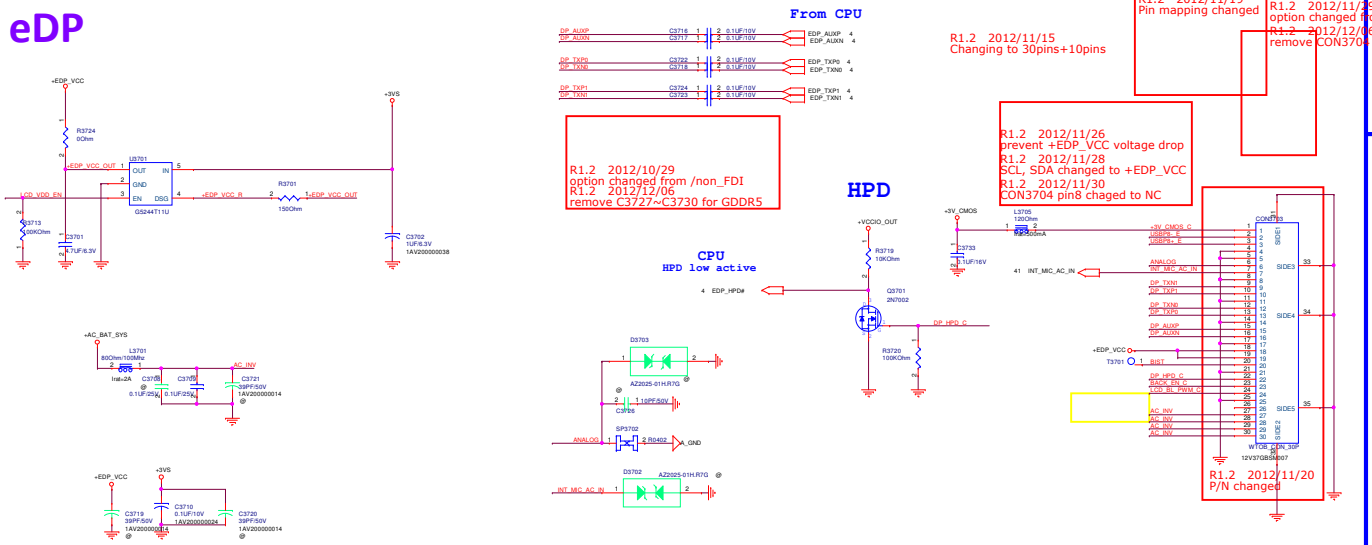
LVDS/eDP control signal

LVDS/EDP共用pin

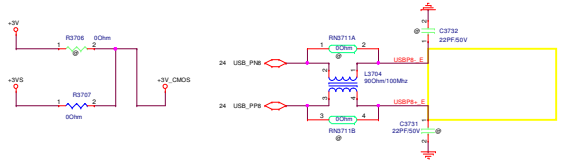
LVDS/EDP共用pin



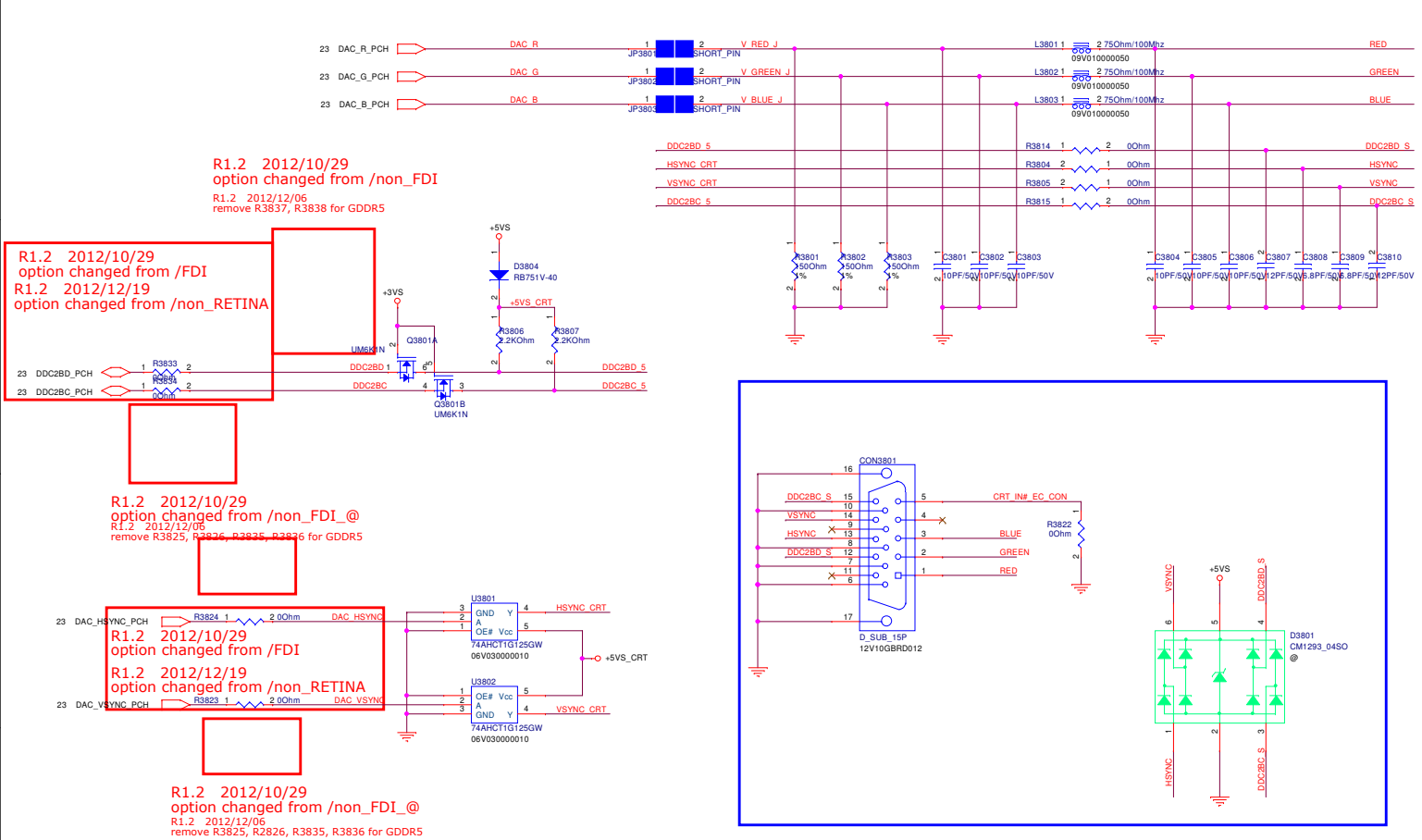
eDP

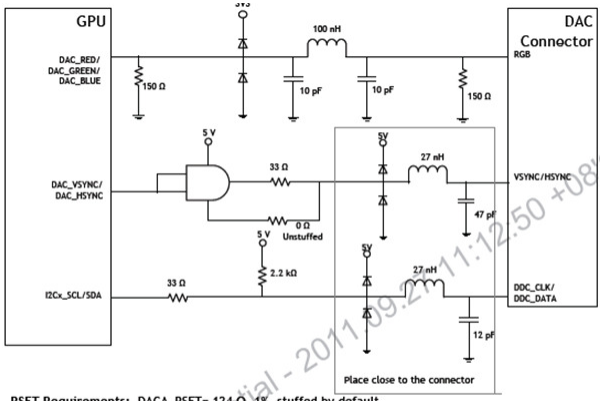


USB Camera



PEGATRON	Title : LVDS CONN		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Monday, January 21, 2013	Sheet: 37 of 56		



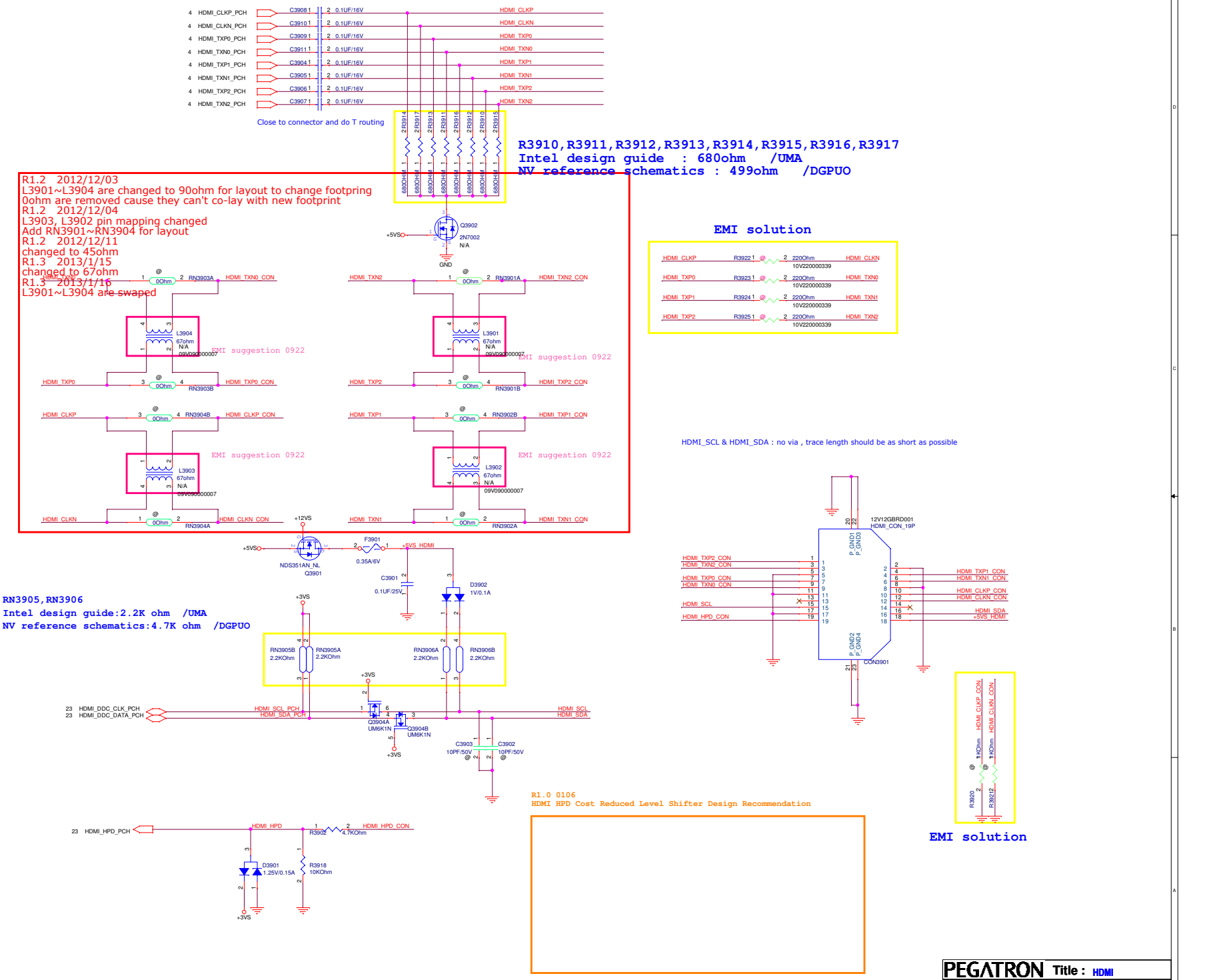


RSET Requirements: DACA_RSET= 124 Ω, 1%, stuffed by default.

Figure 71. GPU-DAC Connections

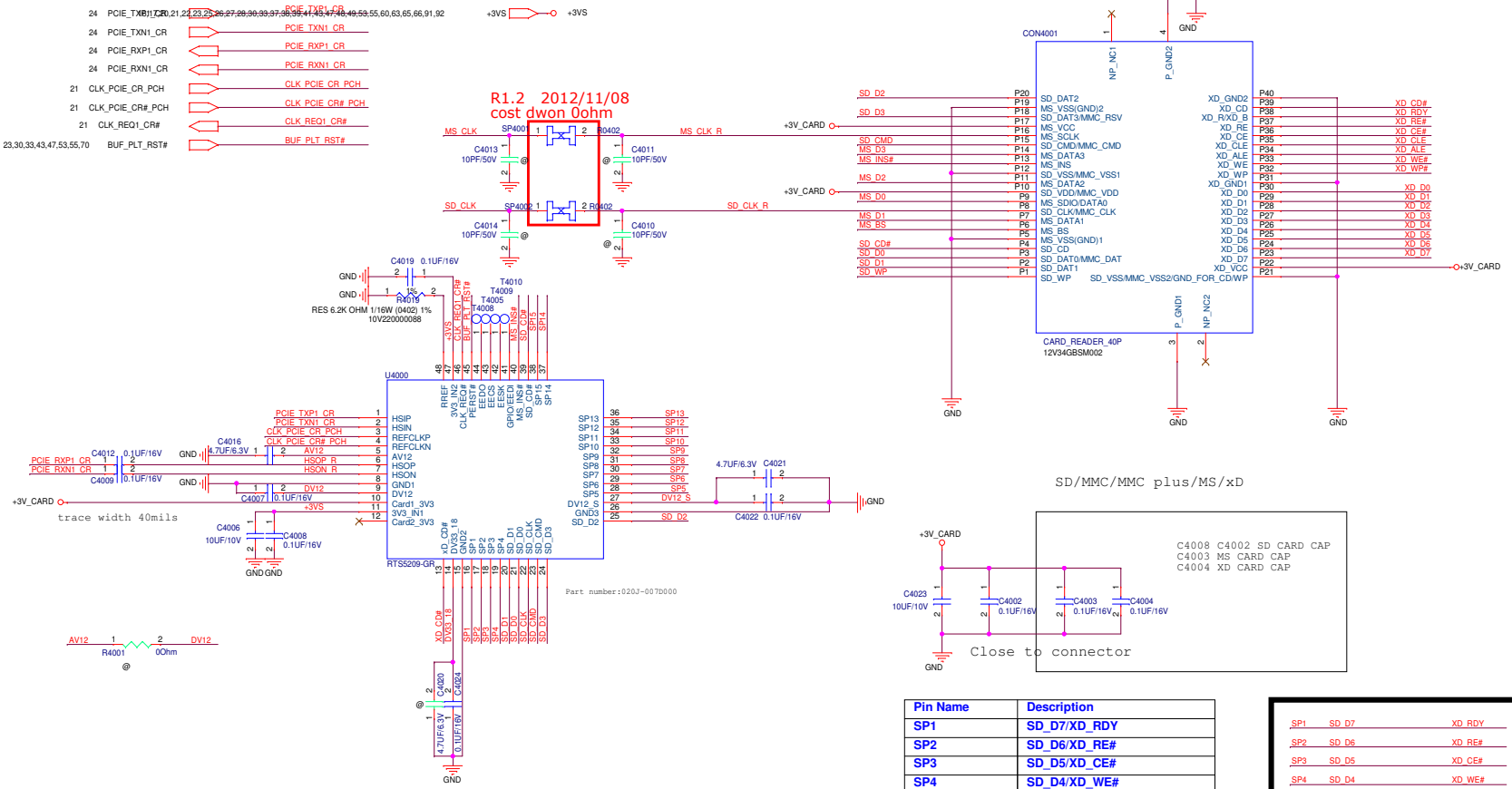
The LC filter circuit(NV DSC only)
DDC:L=27nH,C=12PF
HSYNC/VSYNC:L=27nH,C=47PF
RGB:L=100nH,C=10PF

PEGATRON	Title : CRT	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 38 of 96	



PEGATRON	Title : HDMI		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 39 of 96		

From System's PCIE interface



Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

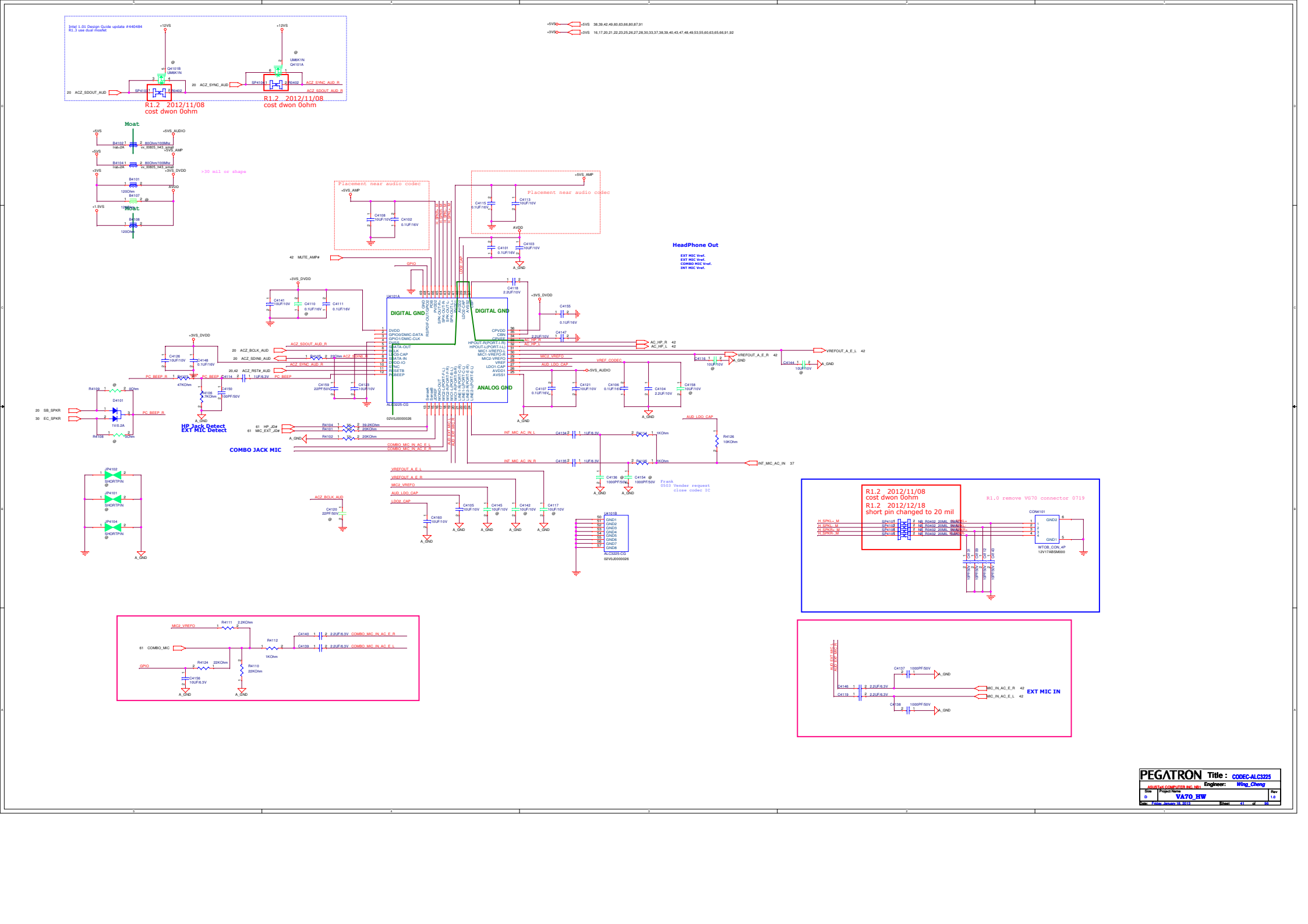
Share Pin

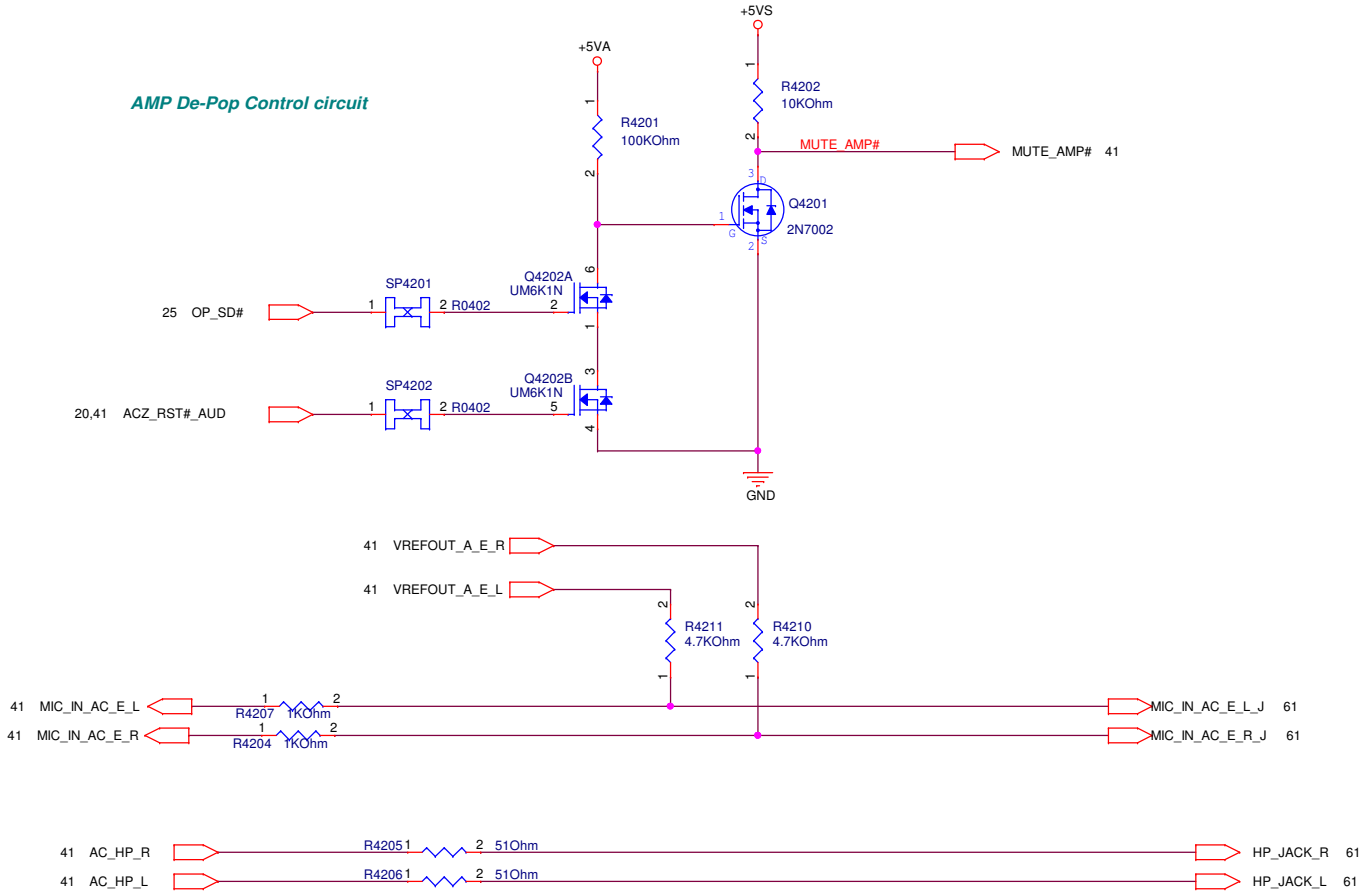
PEGATRON Title : RTS5209

BG1/CSC/HW5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 40 of 96


Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/08
cost dwon 0ohm
Moat
Moat
>30 mil ox shape
Placement near audio codec
Placement near audio codec
HeadPhone Out
EXT MIC Vref.
EXT MIC Vref.
COMBO MIC Vref.
INT MIC Vref.
DIGITAL GND
DIGITAL GND
ANALOG GND
HP Jack Detect
EXT MIC Detect
COMBO JACK MIC
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/12/18
short pin changed to 20 mil
R1.0 remove VG70 connector 0719
Frank
0503 Vender request
close codec IC
EXT MIC IN
PEGATRON
Title : CODEC-ALC3225
ASUSTeK COMPUTER INC. NB1
Engineer: Wing_Cheng
Size: D
Project Name: VA70_HW
Rev: 1.0
Date: Friday, January 18, 2013
Sheet 41 of 86



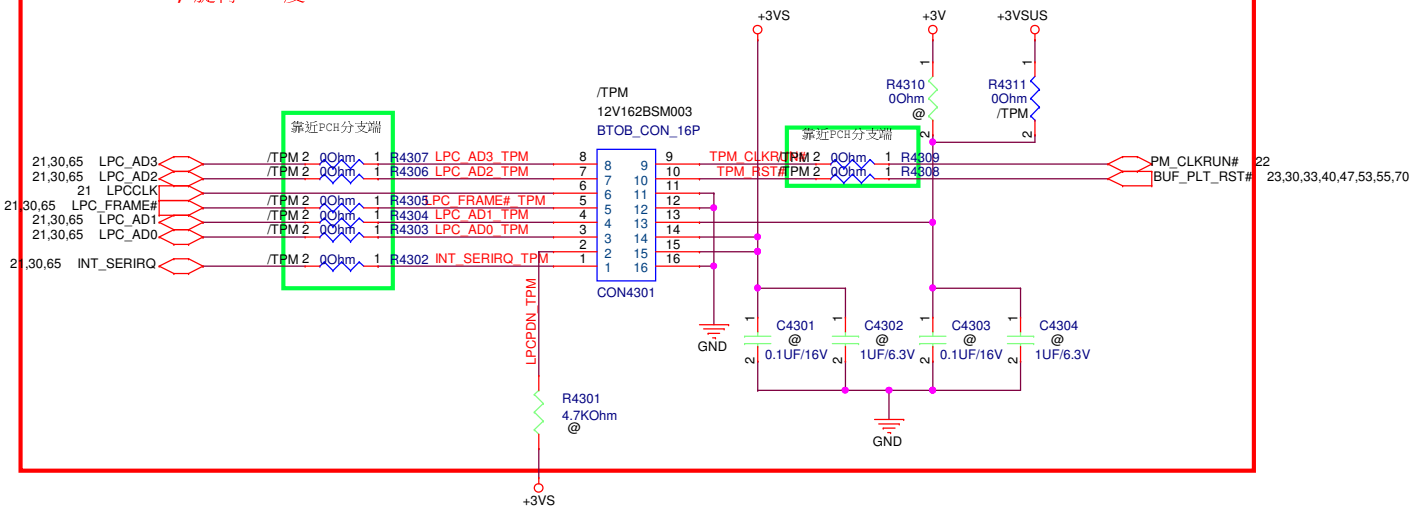
PEGATRON Title : AUDIO ALC269

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 42 of 96

R1.2 2012/11/30
follow MA50, 旋轉180度



PEGATRON Title : TPM CONN

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 43 of 96

Del Entry audio circuit

SR-8
0121-11

PEGATRON Title : CODEC-ALC269

ASUSTeK COMPUTER INC. NB1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 44 of 96

Del Entry audio circuit

SR-8
0121-11

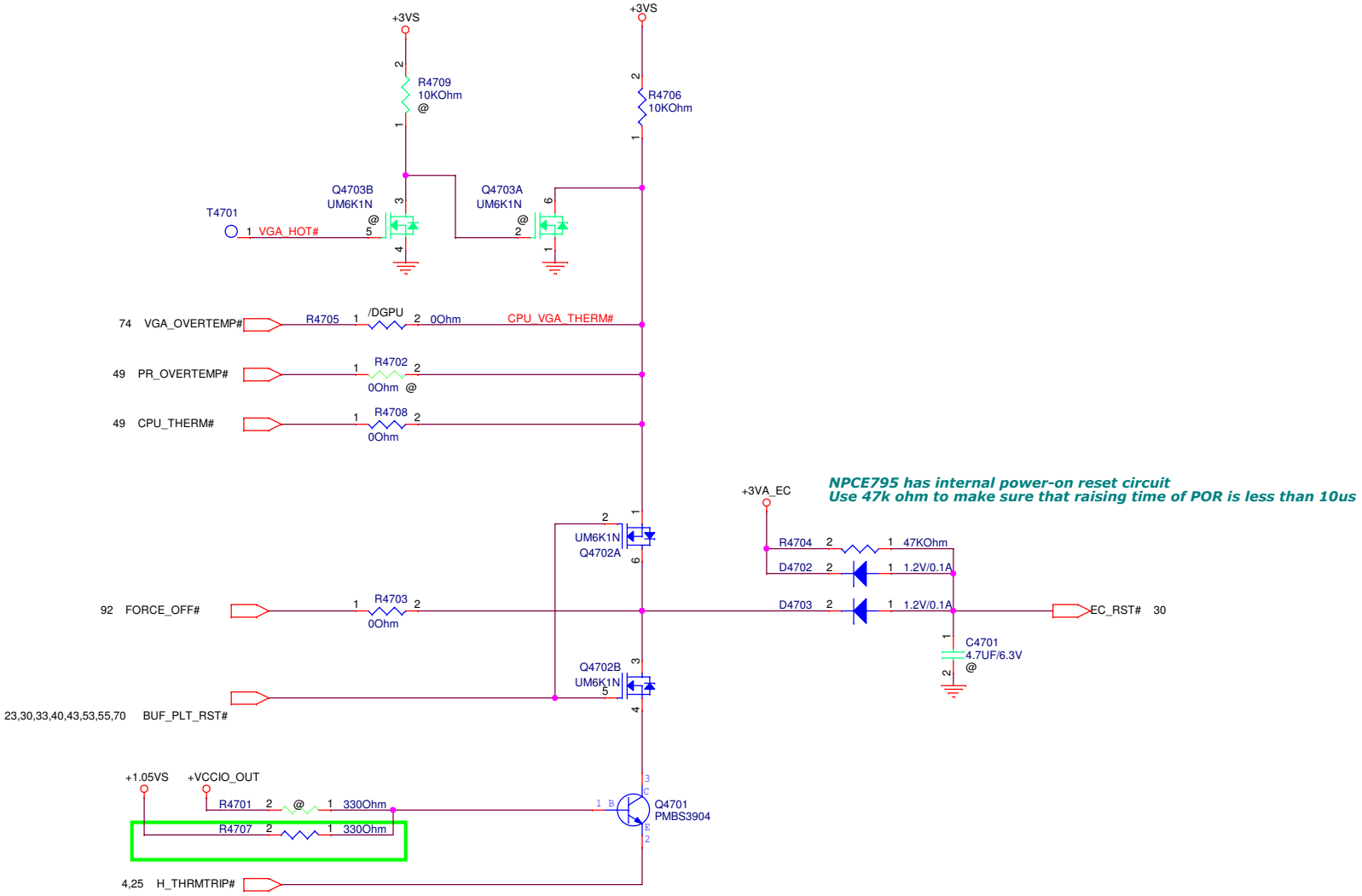
PEGATRON Title : AUDIO ALC269

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 45 of 96

Thermal Policy



+3VA_EC +3VA_EC 28,30

+3VS +3VS 16,17,20,21,22,23,25,26,27,28,30,33,37,38,39,40,41,43,48,49,53,55,60,63,65,66,91,92

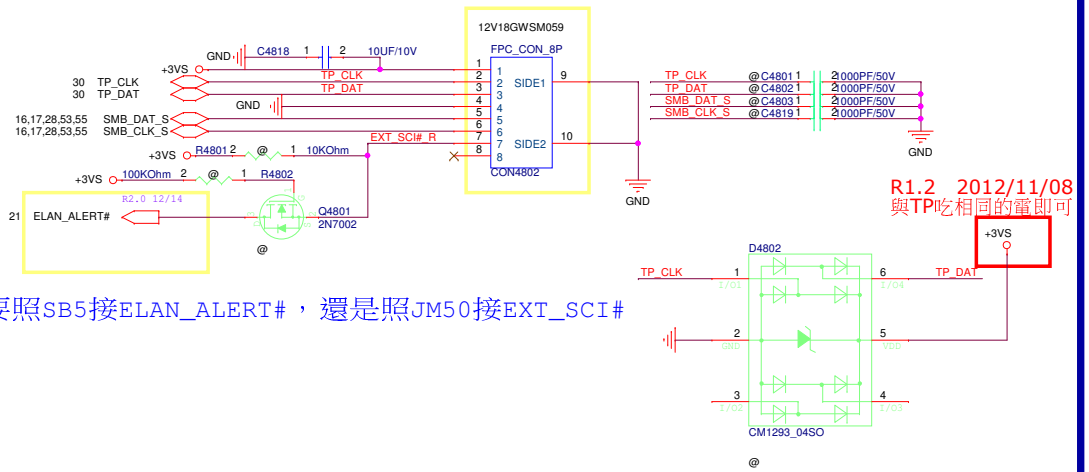
PEGATRON Title : RST_Reset Circuit

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

Date: Friday, January 25, 2013 Sheet 47 of 96

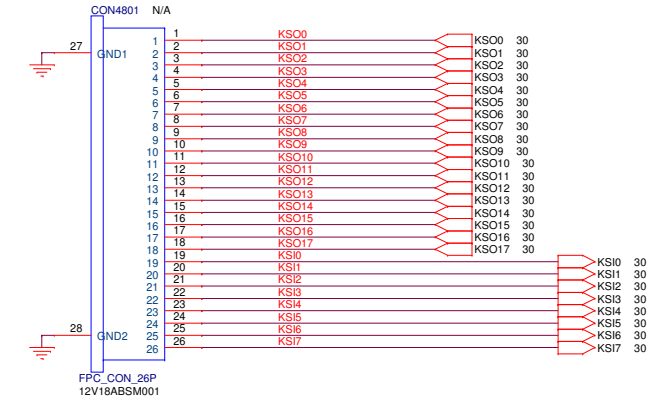
Touch Pad Button



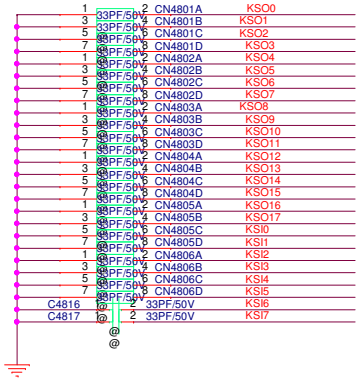
R1.2 2012/11/08
與TP吃相同的電即可

要照SB5接ELAN_ALERT#，還是照JM50接EXT_SCI#

Keyboard

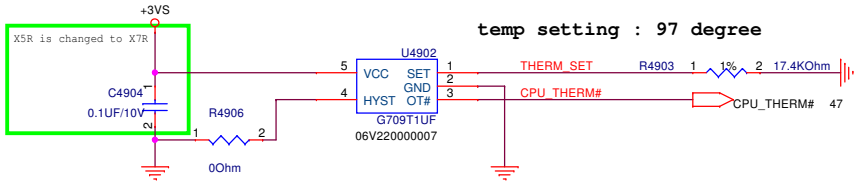


1218-00MW000

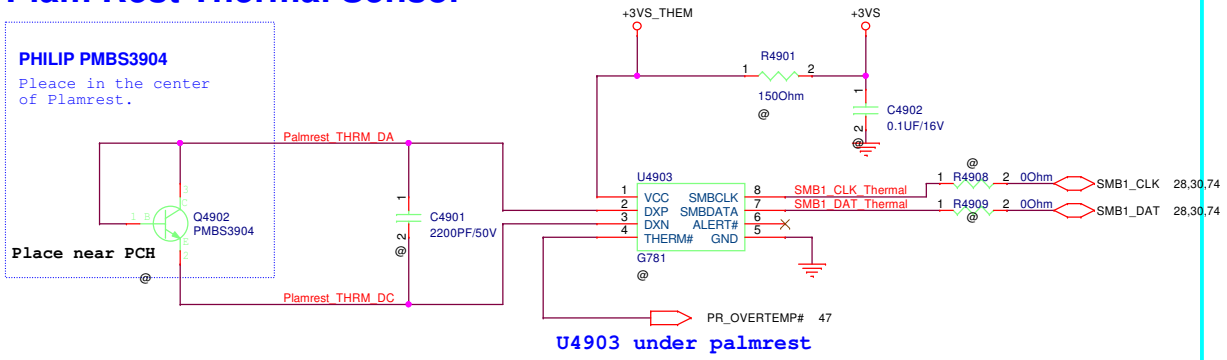


PEGATRON	Title : KB/ TP/ FLASH		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 48 of 96		

U5001 Close to CPU

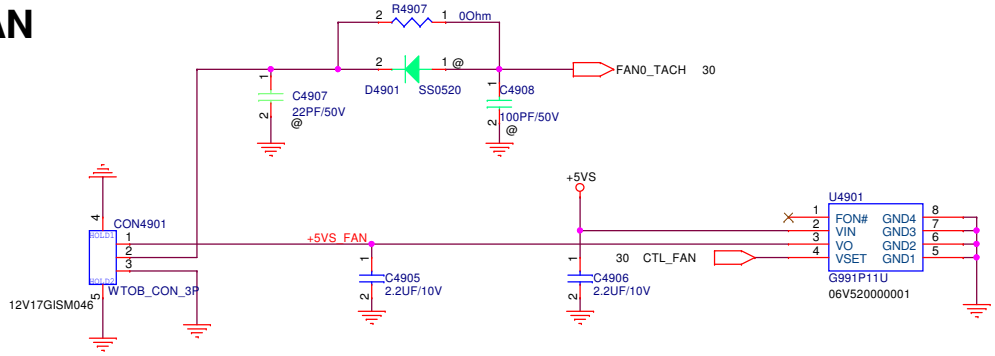


Plam Rest Thermal Sensor



R1.2-10

FAN



PEGATRON	Title : THERMAL/ FAN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 49 of 96	

PEGATRON Title : Realtek_RTS5138

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 50 of 96

PEGATRON

Title : USB3.0 uPD720200

BG1\HW1

Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 51 of 96

PEGATRON

Title : PCIE NEW CARD

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 52 of 96

PCIE/mSATA

Select PCIE or mSATA IF select mSATA(only +3VAUX)

24 PCIE_RXN6_mSATA — R5320 1 @ 2 0Ohm — PCIE_mSATA_C23 — C5314 1 2 0.01UF/50V — SATA_RXP4 20
24 PCIE_RXP6_mSATA — R5321 1 @ 2 0Ohm — PCIE_mSATA_C25 — C5315 1 2 0.01UF/50V — SATA_RXN4 20

24 PCIE_TXN6_mSATA — R5318 1 @ 2 0Ohm — PCIE_mSATA_C31 — C5316 1 2 0.01UF/50V — SATA_TXN4 20
24 PCIE_TXP6_mSATA — R5319 1 @ 2 0Ohm — PCIE_mSATA_C33 — C5317 1 2 0.01UF/50V — SATA_TXP4 20

+3.3VS_mSATA

Q5310
2N7002
@

R5315
10KOhm
@

22,33 PCIE_WAKE#

PCIE_WAKE#_mSATA

+3.3VS_mSATA

+1.5VS_mSATA

H5301 HT-G4041M20TFE

H5302 HT-G4041M20TFE

CON5301

PCIE_WAKE#_mSATA 1	WAKE#	3.3V_1	2
3	Reserved1	GND7	4
5	Reserved2	1.5V_1	6
7	CLKREQ#	UIM_PWR	8
9	GND1	UIM_DATA	10
11	REFCLK-	UIM_CLK	12
13	REFCLK+	UIM_RESET	14
15	GND2	UIM_VPP	16
17	Reserved/UIM_C8	GND8	18
19	Reserved/UIM_C4W_DISABLE#		20
21	GND3	PERST#	22
23	PERn0	+3.3Vaux	24
25	PERp0	GND9	26
27	GND4	1.5V_2	28
29	GND5	SMB_CLK	30
31	PETn0	SMB_DATA	32
33	PETp0	GND10	34
35	GND6	USB_D-	36
37	Reserved3	USB_D+	38
39	Reserved4	GND11	40
41	Reserved5	LED_WWAN#	42
43	Reserved6	LED_WLAN#	44
45	Reserved7	LED_WPAN#	46
47	Reserved8	1.5V_3	48
49	Reserved9	GND12	50
51	Reserved10	3.3V_2	52
53	GND13	NP_NC2	56
54	GND14	NP_NC1	55

MINI_PCI_LATCH_52P
12V44GISM005

21 CLK_REQ2_PCIE_mSATA#
21 CLK_PCIE_mSATA#_PCH
21 CLK_PCIE_mSATA_PCH

Follow SanDisk SSD U100 spec.
23 TXP
25 TXN
31 RXN
33 RXP

PCIE_mSATA_C23
PCIE_mSATA_C25
PCIE_mSATA_C31
PCIE_mSATA_C33

+3.3VS_mSATA

MINICARD_RST#_mSATA — R5305 2 1 0Ohm — WLAN_ON 25,55
R5306 2 1 0Ohm — BUF_PLT_RST# 23,30,33,40,43,47,55,70
WLAN_RST#_PCH 25,55

SMBC_mSATA — R5316 1 @ 2 0Ohm — SMB_CLK_S 16,17,28,48,55
SMBD_mSATA — R5317 1 @ 2 0Ohm — SMB_DAT_S 16,17,28,48,55

USBP11-
USBP11+

USBP11- — 3 RN5301B 4 0Ohm — @
3 4 — L5301 90Ohm/100MHz 09V090000002 — USB_PN11 24, USB_PP11 24
2 1 — @
USBP11+ — 1 RN5301A 2 0Ohm — @

+3.3VS_mSATA

C5302 10UF/10V 1AV500000008
C5303 0.1UF/16V
C5304 0.1UF/16V
C5305 0.01UF/50V @
C5301 0.01UF/50V @

+1.5VS_mSATA

C5307 10UF/10V 1AV500000008 @
C5308 0.1UF/16V @
C5309 0.1UF/16V @
C5310 0.01UF/50V @

R5308 0Ohm 10V440000001
+3VS — +3.3VS_mSATA

R5313 0Ohm 10V440000001
+1.5VS — +1.5VS_mSATA

PEGATRON	Title : WiFi/WiMAX	
BU1-RD Div.1-HW RD Dept.1	Engineer:	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 53 of 96	

PEGATRON

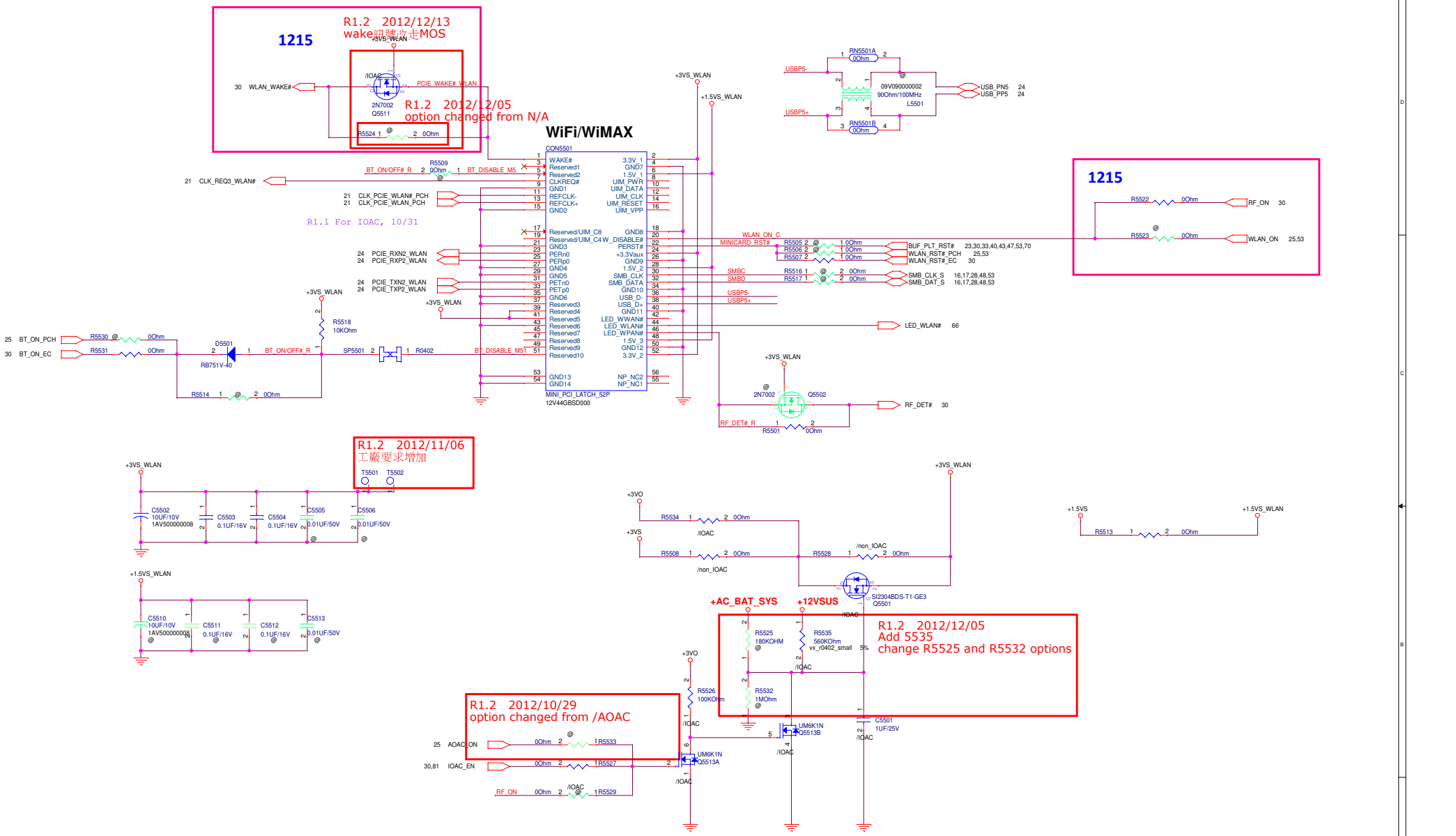
Title : MINICARD (WUSB /UPCONVERT)

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 54 of 96



PEGATRON Title : WIFIWIMAX

BU1-RD Div.1-HW RD Dept.1 Engineer:

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 55 of 96

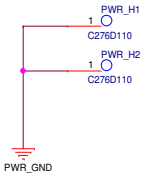
PEGATRON Title :TP_M

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

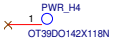
Date: Friday, January 18, 2013 Sheet 56 of 96

Screw G x 2

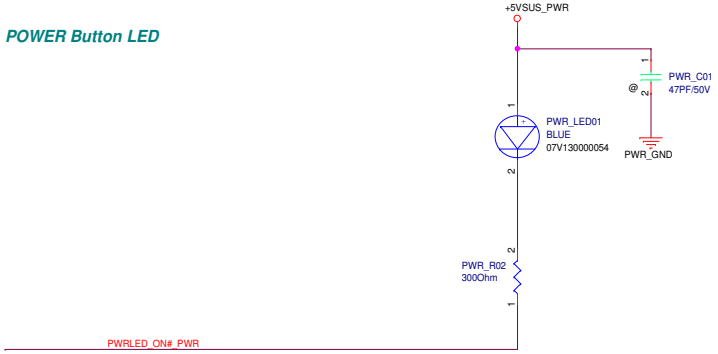


Fix Hole H x 1

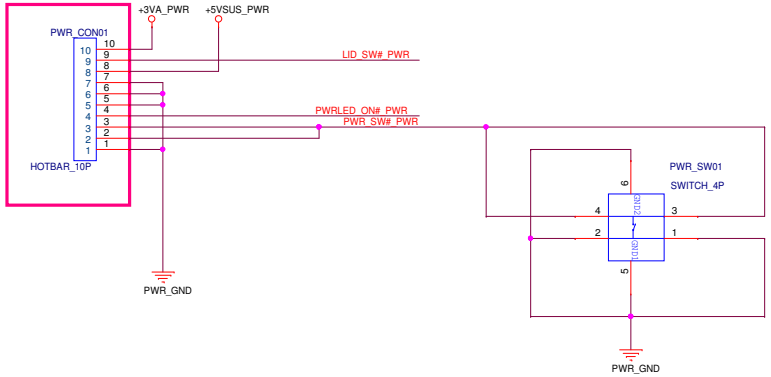
Fix Hole I x 1

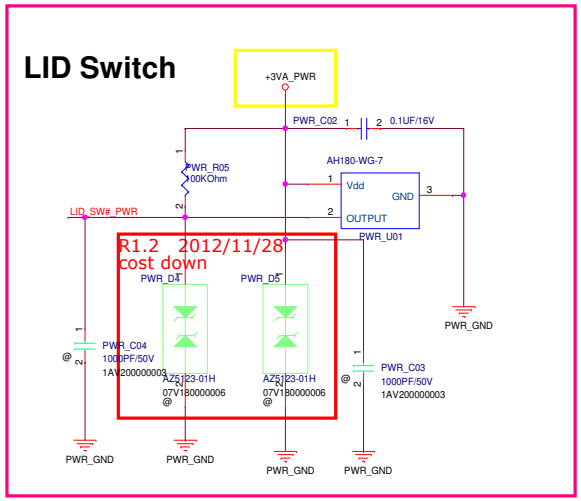


POWER Button LED

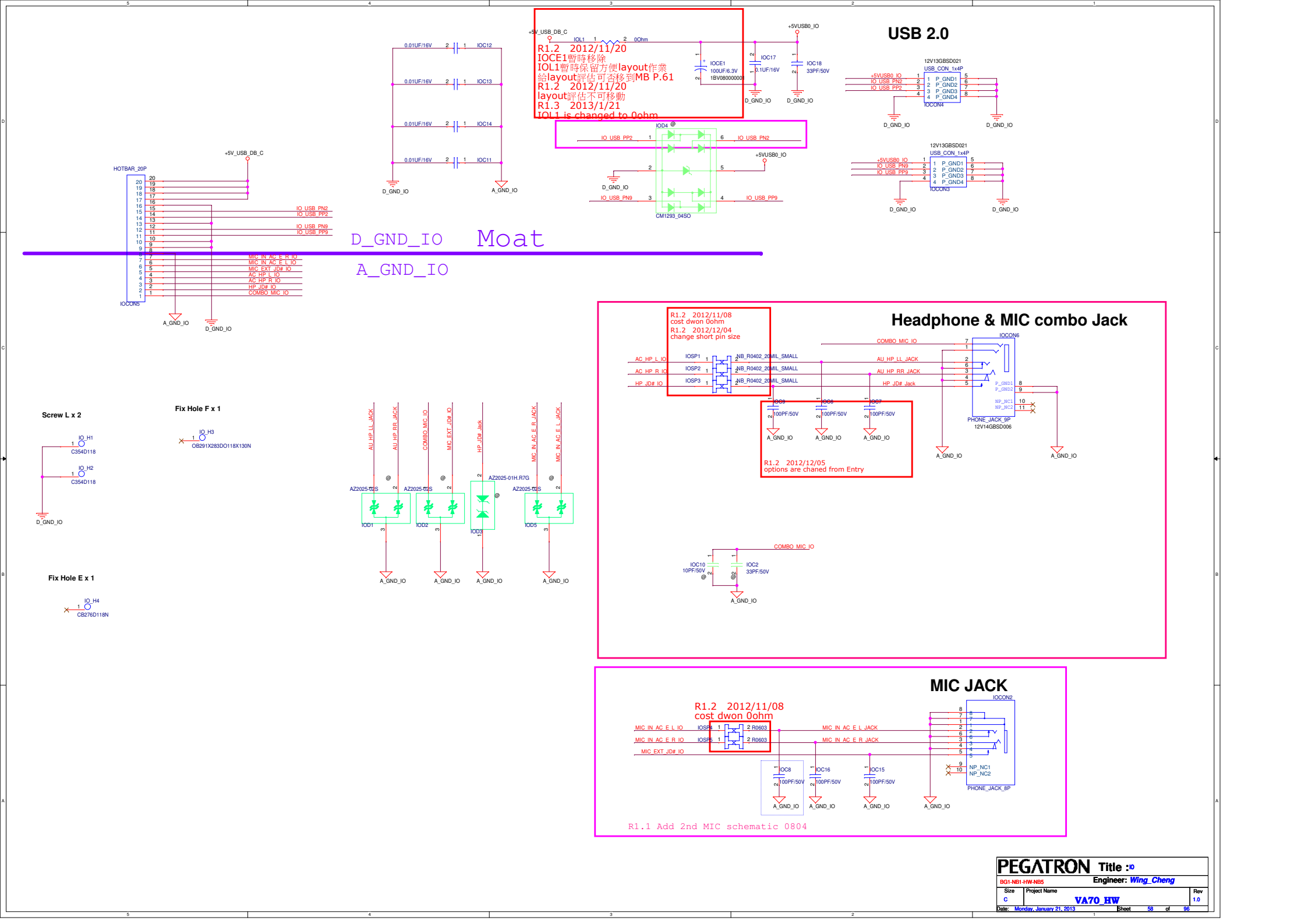


R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024



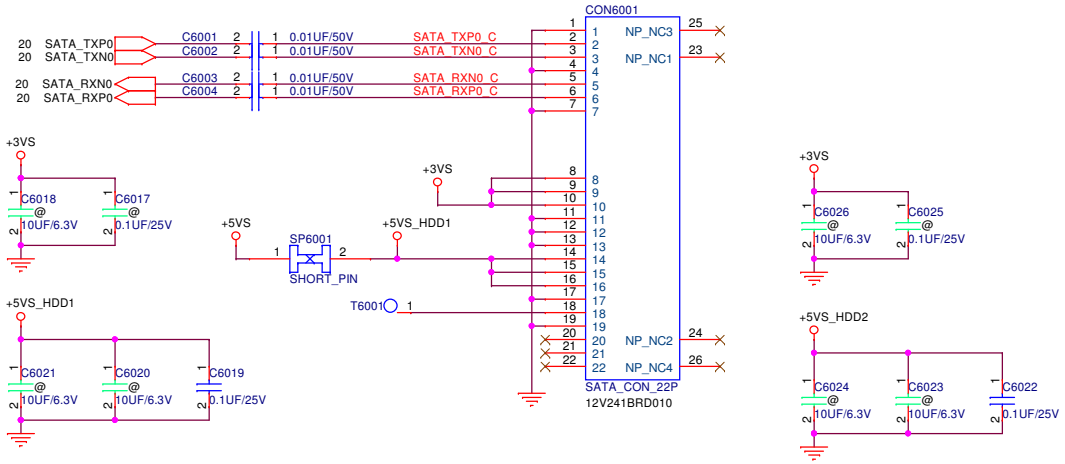


PEGATRON	Title : PWR BTN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 57 of 96	


USB 2.0
R1.2 2012/11/20
IOCE1暫時移除
IOL1暫時保留方便layout作業
給layout評估可否移到MB P.61
R1.2 2012/11/20
layout評估不可移動
R1.3 2013/1/21
IOL1 is changed to 0ohm
D_GND_IO Moat
A_GND_IO
Headphone & MIC combo Jack
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/12/04
change short pin size
R1.2 2012/12/05
options are chaned from Entry
MIC JACK
R1.2 2012/11/08
cost dwon 0ohm
R1.1 Add 2nd MIC schematic 0804
Screw L x 2
Fix Hole F x 1
Fix Hole E x 1
PEGATRON
Title :IO
Engineer: Wing_Cheng
VA70_HW
Monday, January 21, 2013
Sheet 58 of 96

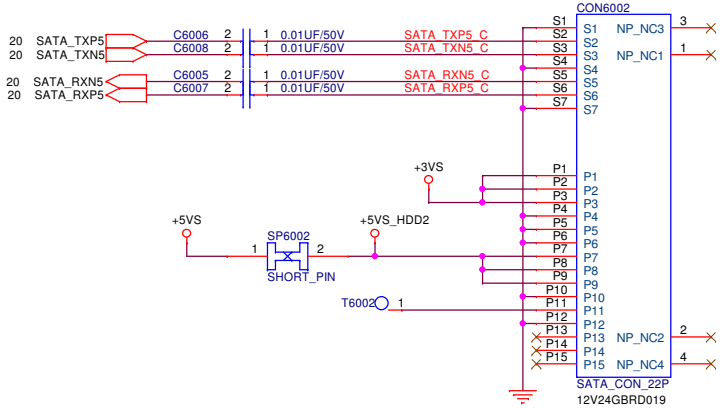
HDD 1

9.5mm

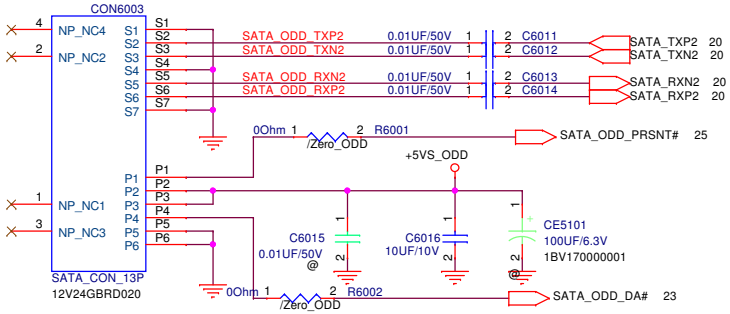


HDD 2

12.5mm

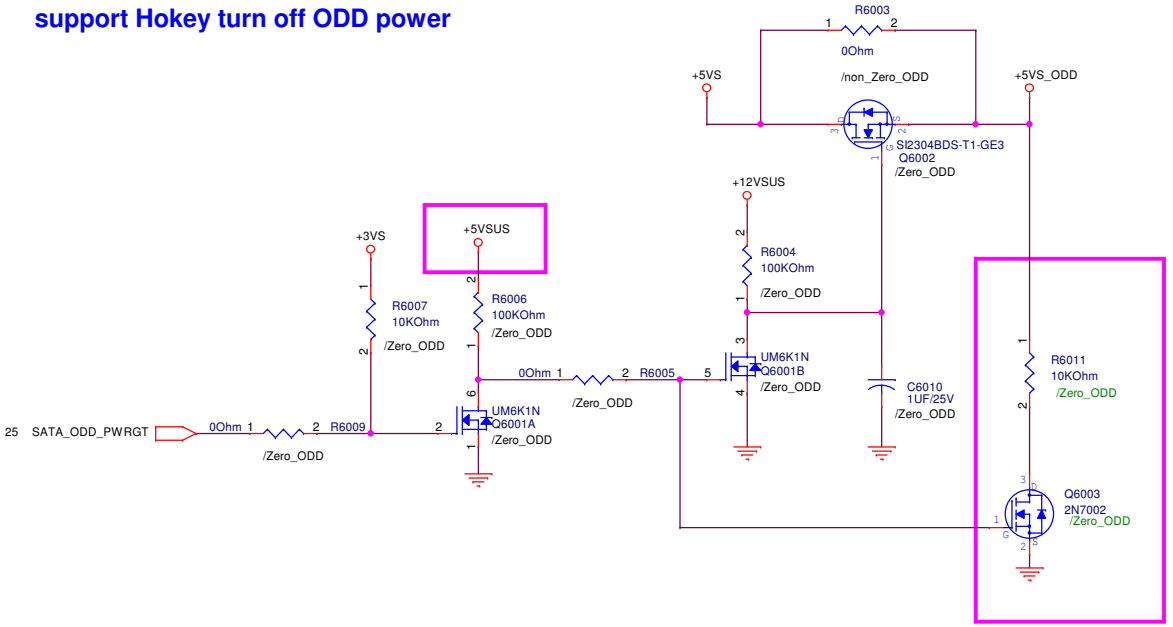


ODD



ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



PEGATRON	Title : SATA HDD/ ODD	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 60 of 96	

MB USB

R1.3 2013/1/21
L6110 is changed to 0ohm

R1.2 2012/11/20
Changed from 560UF/2.5V

USB 3.0

Sleep & Charge

R1.3 2013/1/21
L6111 is changed to 0ohm

PLACE ESD Diodes 0700-0014000 near Connector

no sleep & charge

USB 3.0

R1.2 2012/11/20
Changed from 100UF/6.3V
R1.2 2012/11/23
changed from 220UF/6.3V

IO Board

USB Power Switch for USB DB Main

BIOS debug port

AUDIO BOARD/w USB2.0 x2

R1.2 2012/11/20
Add 560UF/2.5V for layout to estimate
R1.2 2012/11/23
changed from 560/2.5V
R1.2 2012/11/27
L6115, CE6105 are removed

A_GND

PEGATRON Title : USB PORTS eSATA
Engineer: Wing_Chang
Size: Custom | Project Name: VA70_HW | Rev: 1.0
Date: Monday, January 21, 2013 | Sheet 41 of 56

PEGATRON Title : Camera/ BT/ FL CONN

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

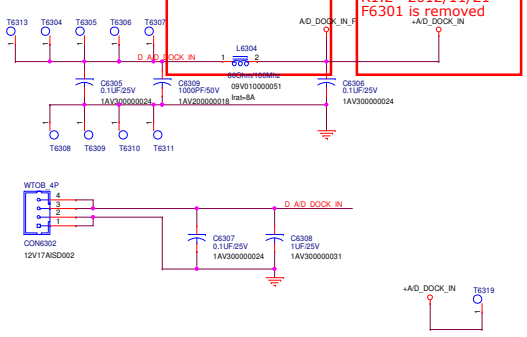
Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 62 of 96

DC IN

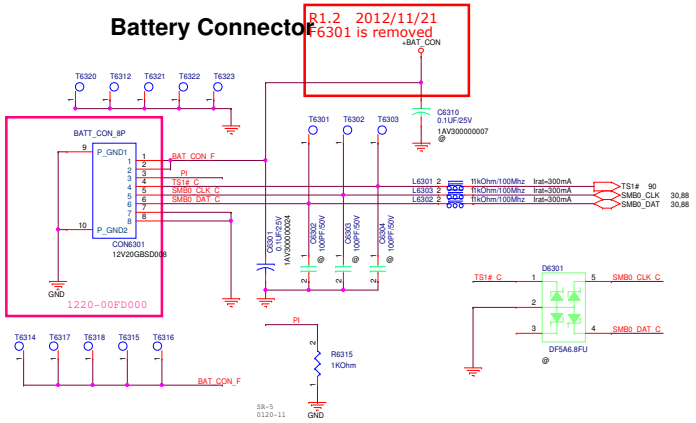
R1.3 2013/1/4
L6304 is changed to Irat=8A

R1.2 2012/11/21
F6301 is removed



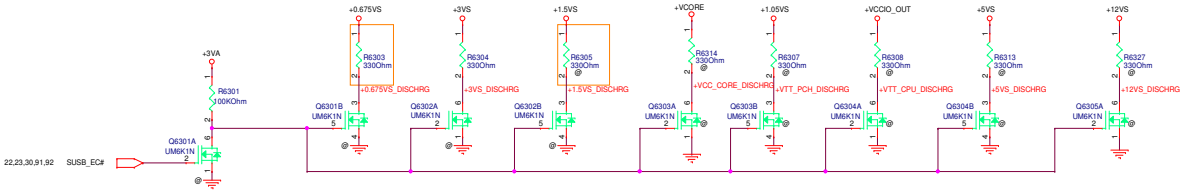
Battery Connector

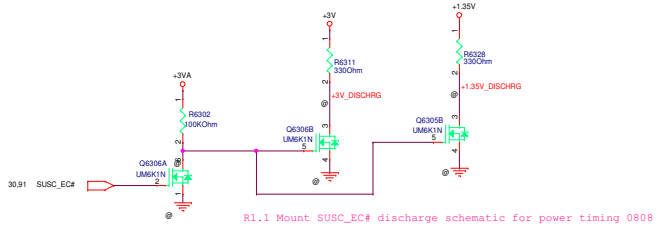
R1.2 2012/11/21
F6301 is removed

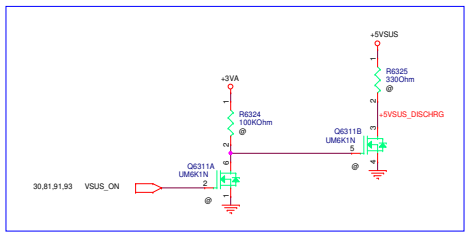


Discharge Circuit

Frank
0505 Follow EVEREST







R1.1 Mount SUSC_EC# discharge schematic for power timing 0808

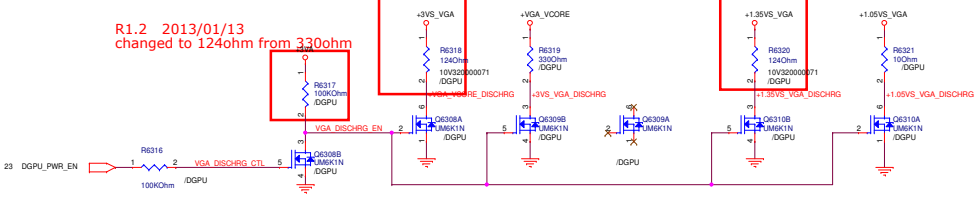
VGA Discharge Circuit

R1.2 2013/01/13
changed to 124ohm from 330ohm

R1.2 2013/01/02
changed to 124ohm from 330ohm

R1.2 2012/12/10
changed to +1.35VS_VGA

R1.2 2013/01/02
changed to 124ohm from 330ohm



Unmount +VGA_Vcore discharg

PEGATRON	Title : DC-IN/ DISCHARGE	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 63 of 96	

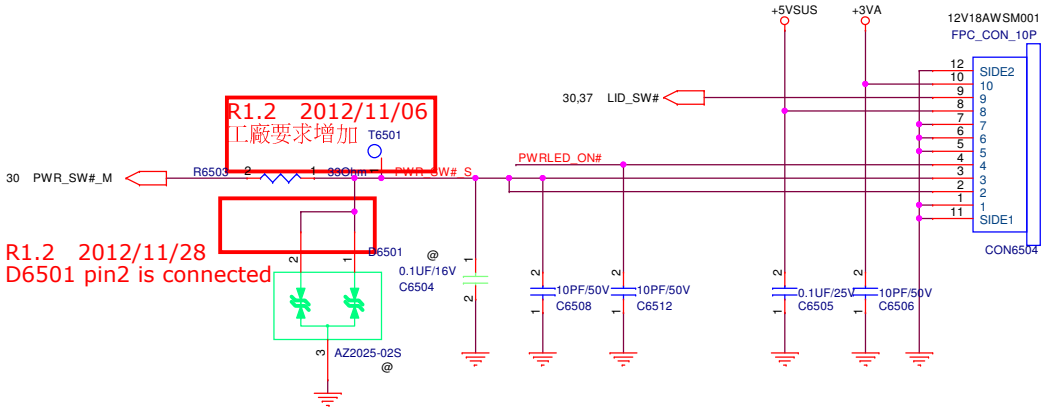
PEGATRON Title: SCHEMATIC

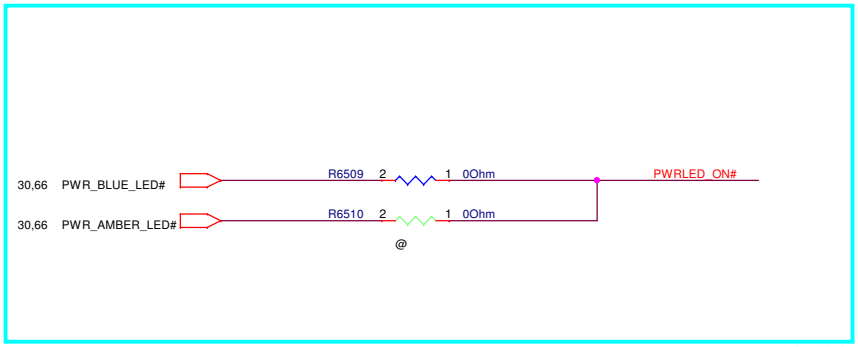
Engineer: Wing_Chang

Size: A | Project Name: VA70_EV | Rev: 1A

Date: Friday, January 18, 2013 | Sheet 1 of 1

PWR BRD/ AMBIENT/ HALL CONN.



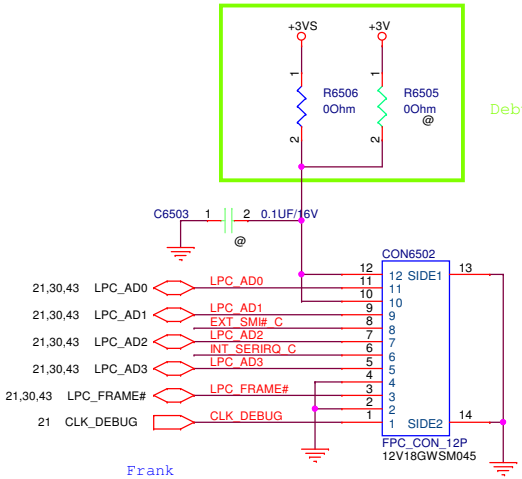


R1.2-28

change Power LED CON6503 circuit

R1.0 remove VG70 POWER connector CON6503 0719

DEBUG CARD CONN.

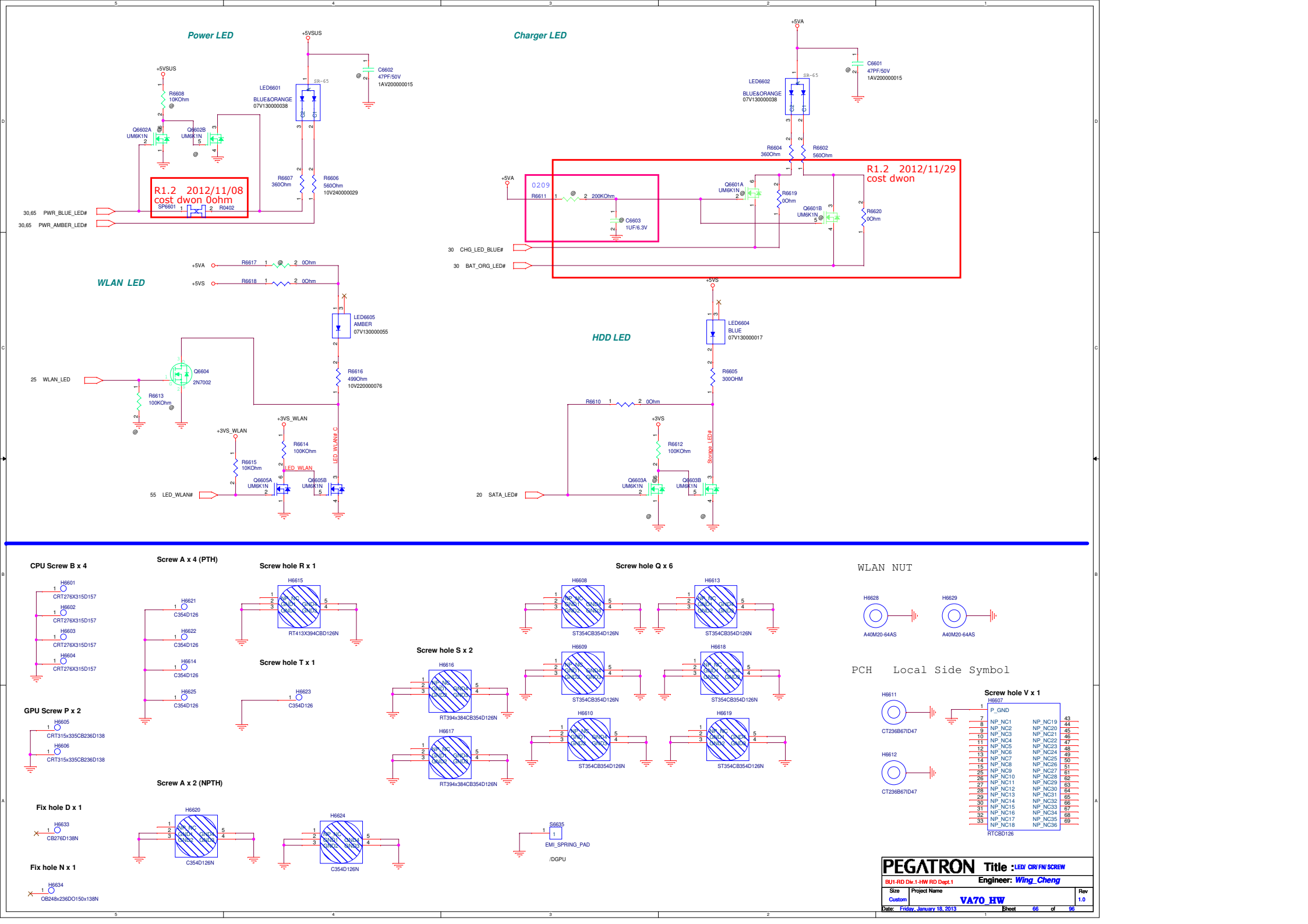


Debug port power is changed to +3VS

Frank
0425_modify Debug port
(add EXT_SMI#_C and INT_SERIRQ_C)

CR R1.0 change part for EOL. Joyoung0803
PS. Pin define is reverse.

PEGATRON Title : MDC/ PWR SW/ Debug
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng
Size: Custom | Project Name: VA70_HW | Rev: 1.0
Date: Friday, January 18, 2013 | Sheet 65 of 96


Power LED
+5VSUS
R6608 10KOhm
Q6602A UM6K1N
Q6602B UM6K1N
LED6601 BLUE&ORANGE 07V130000038
C6602 47PF/50V 1AV200000015
R6607 360Ohm
R6606 560Ohm 10V240000029
R1.2 2012/11/08 cost dwon 0ohm
SP6601
R0402
30,65 PWR_BLUE_LED#
30,65 PWR_AMBER_LED#
Charger LED
+5VA
LED6602 BLUE&ORANGE 07V130000038
C6601 47PF/50V 1AV200000015
R6604 360Ohm
R6602 560Ohm
0209
R6611 200KOhm
C6603 1UF/6.3V
Q6601A UM6K1N
Q6601B UM6K1N
R6619 0Ohm
R6620 0Ohm
R1.2 2012/11/29 cost dwon
30 CHG_LED_BLUE#
30 BAT_ORG_LED#
WLAN LED
+5VA
+5VS
R6617 0Ohm
R6618 0Ohm
LED6605 AMBER 07V130000055
R6616 499Ohm 10V220000076
25 WLAN_LED
Q6604 2N7002
R6613 100KOhm
+3VS_WLAN
R6615 10KOhm
R6614 100KOhm
LED_WLAN
Q6605A UM6K1N
Q6605B UM6K1N
55 LED_WLAN#
HDD LED
+5VS
LED6604 BLUE 07V130000017
R6605 300OHM
R6610 0Ohm
+3VS
R6612 100KOhm
Storage_LED#
Q6603A UM6K1N
Q6603B UM6K1N
20 SATA_LED#
CPU Screw B x 4
H6601 CRT276X315D157
H6602 CRT276X315D157
H6603 CRT276X315D157
H6604 CRT276X315D157
GPU Screw P x 2
H6605 CRT315x335CB236D138
H6606 CRT315x335CB236D138
Fix hole D x 1
H6633 CB276D138N
Fix hole N x 1
H6634 OB248x236DO150x138N
Screw A x 4 (PTH)
H6621 C354D126
H6622 C354D126
H6614 C354D126
H6625 C354D126
Screw A x 2 (NPTH)
H6620 C354D126N
H6624 C354D126N
Screw hole R x 1
H6615 RT413X394CBD126N
Screw hole T x 1
H6623 C354D126
Screw hole S x 2
H6616 RT394x384CB354D126N
H6617 RT394x384CB354D126N
Screw hole Q x 6
H6608 ST354CB354D126N
H6613 ST354CB354D126N
H6609 ST354CB354D126N
H6618 ST354CB354D126N
H6610 ST354CB354D126N
H6619 ST354CB354D126N
S6635 EMI_SPRING_PAD /DGPU
WLAN NUT
H6628 A40M20-64AS
H6629 A40M20-64AS
PCH Local Side Symbol
H6611 CT236B67ID47
H6612 CT236B67ID47
Screw hole V x 1
H6607 RTCBD126
P_GND
NP_NC1 NP_NC2 NP_NC3 NP_NC4 NP_NC5 NP_NC6 NP_NC7 NP_NC8 NP_NC9 NP_NC10 NP_NC11 NP_NC12 NP_NC13 NP_NC14 NP_NC15 NP_NC16 NP_NC17 NP_NC18
NP_NC19 NP_NC20 NP_NC21 NP_NC22 NP_NC23 NP_NC24 NP_NC25 NP_NC26 NP_NC27 NP_NC28 NP_NC29 NP_NC30 NP_NC31 NP_NC32 NP_NC33 NP_NC34 NP_NC35 NP_NC36
PEGATRON
Title : LED/ CIR/ FN/ SCREW
BU1-RD Div.1-HW RD Dept.1
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 66 of 96

PEGATRON Title : TPM

Pegatron Corp. Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 67 of 96

PEGATRON

Title : Finger Printer

Pegatron Corp.

Engineer: Wing_Cheng

Size	Project Name	Rev
A	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 68 of 96

PEGATRON

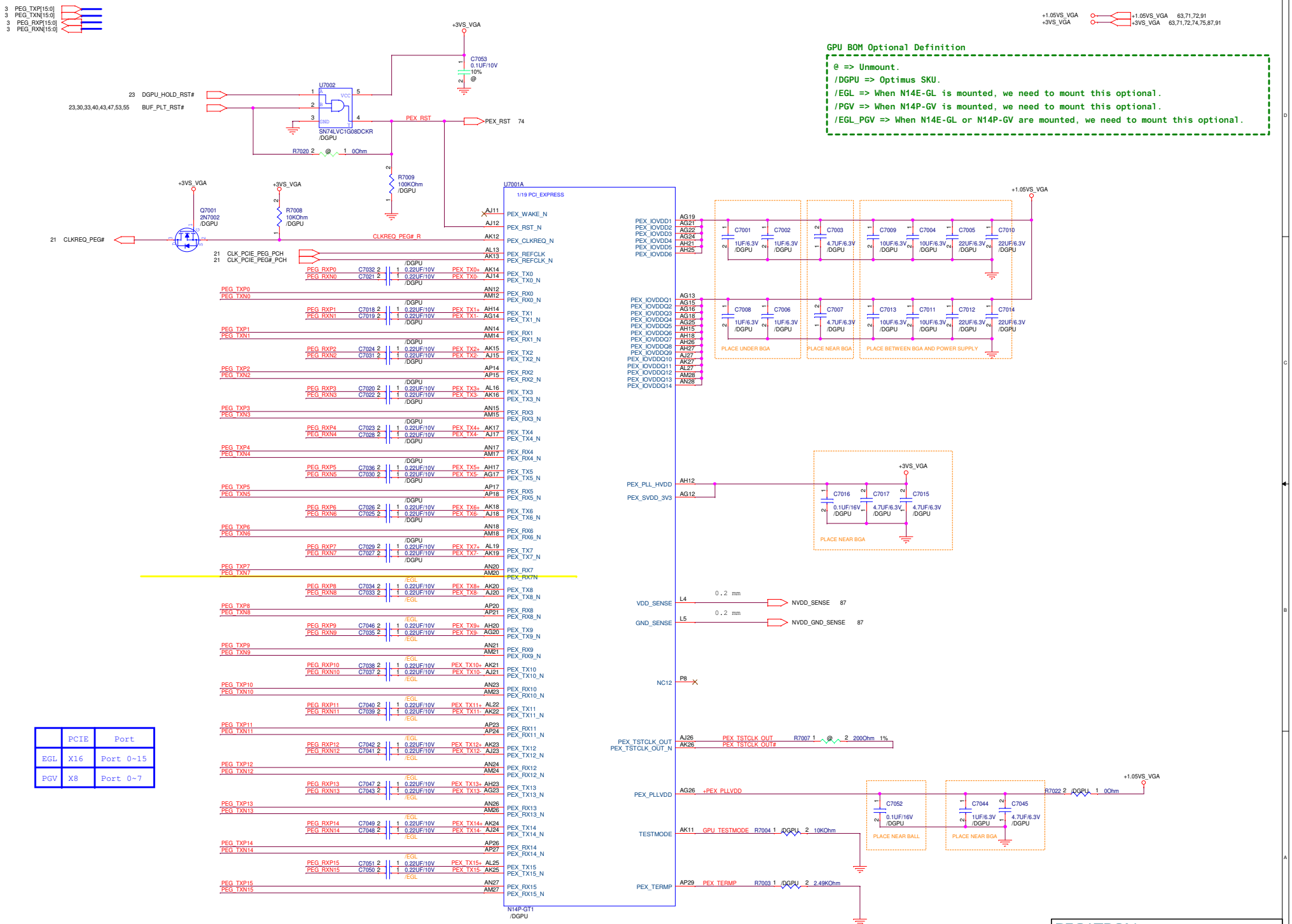
Title : G-Sensor TSH35TR

BU1-RD Div.1-HW RD Dept.1

Engineer: *Wing_Cheng*

Size	Project Name	Rev
A		1.0

Date: Friday, January 18, 2013 Sheet 69 of 96



	PCIE	Port
EGL	X16	Port 0~15
PGV	X8	Port 0~7

PEGATRON

Title : N14xxx-PCIE

PEGATRON COMPUTER INC

Engineer: Panda_Wang

Size	Project Name	Rev
C	VA70_HW	1.3
	P/N	

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76,77 FBAD[0..63]
76,77 FBA_DBI[0..7]
76,77 FBA_EDC[0..7]
76,77 FBA_CMD[0..31]

78,79 FBBD[0..63]
78,79 FBB_DBI[0..7]
78,79 FBB_EDC[0..7]
78,79 FBB_CMD[0..31]

+1.05VS_VGA +1.05VS_VGA 63,70,72,91
+1.35VS_VGA +1.35VS_VGA 63,75,76,77,78,79,84
+3VS_VGA +3VS_VGA 63,70,72,74,75,87,91

U7001B
2/19 FBA

BOT SIDE

FBAD0	L28	FBA_D0
FBAD1	M29	FBA_D1
FBAD2	L29	FBA_D2
FBAD3	M28	FBA_D3
FBAD4	N31	FBA_D4
FBAD5	P29	FBA_D5
FBAD6	R29	FBA_D6
FBAD7	P28	FBA_D7
FBAD8	J28	FBA_D8
FBAD9	H29	FBA_D9
FBAD10	J29	FBA_D10
FBAD11	H28	FBA_D11
FBAD12	G29	FBA_D12
FBAD13	E31	FBA_D13
FBAD14	E32	FBA_D14
FBAD15	F30	FBA_D15
FBAD16	C34	FBA_D16
FBAD17	D32	FBA_D17
FBAD18	B33	FBA_D18
FBAD19	C33	FBA_D19
FBAD20	F33	FBA_D20
FBAD21	F32	FBA_D21
FBAD22	H33	FBA_D22
FBAD23	H32	FBA_D23
FBAD24	P34	FBA_D24
FBAD25	P32	FBA_D25
FBAD26	P31	FBA_D26
FBAD27	P33	FBA_D27
FBAD28	L31	FBA_D28
FBAD29	L34	FBA_D29
FBAD30	L32	FBA_D30
FBAD31	L33	FBA_D31
FBAD32	AG28	FBA_D32
FBAD33	AF29	FBA_D33
FBAD34	AG29	FBA_D34
FBAD35	AF28	FBA_D35
FBAD36	AD30	FBA_D36
FBAD37	AD29	FBA_D37
FBAD38	AC29	FBA_D38
FBAD39	AD28	FBA_D39
FBAD40	AJ29	FBA_D40
FBAD41	AK29	FBA_D41
FBAD42	AJ30	FBA_D42
FBAD43	AK28	FBA_D43
FBAD44	AM29	FBA_D44
FBAD45	AM31	FBA_D45
FBAD46	AN29	FBA_D46
FBAD47	AM30	FBA_D47
FBAD48	AN31	FBA_D48
FBAD49	AN32	FBA_D49
FBAD50	AP30	FBA_D50
FBAD51	AP32	FBA_D51
FBAD52	AM33	FBA_D52
FBAD53	AL31	FBA_D53
FBAD54	AK33	FBA_D54
FBAD55	AK32	FBA_D55
FBAD56	AD34	FBA_D56
FBAD57	AD32	FBA_D57
FBAD58	AC30	FBA_D58
FBAD59	AD33	FBA_D59
FBAD60	AF31	FBA_D60
FBAD61	AG34	FBA_D61
FBAD62	AG32	FBA_D62
FBAD63	AG33	FBA_D63

FBA_DBI0	P30	FBA_DQM0
FBA_DBI1	F31	FBA_DQM1
FBA_DBI2	F34	FBA_DQM2
FBA_DBI3	M32	FBA_DQM3
FBA_DBI4	AD31	FBA_DQM4
FBA_DBI5	AL29	FBA_DQM5
FBA_DBI6	AM32	FBA_DQM6
FBA_DBI7	AF34	FBA_DQM7

FBA_EDC0	M31	FBA_DQS_WP0
FBA_EDC1	G31	FBA_DQS_WP1
FBA_EDC2	E33	FBA_DQS_WP2
FBA_EDC3	M33	FBA_DQS_WP3
FBA_EDC4	AE31	FBA_DQS_WP4
FBA_EDC5	AK30	FBA_DQS_WP5
FBA_EDC6	AN33	FBA_DQS_WP6
FBA_EDC7	AF33	FBA_DQS_WP7

M30		FBA_DQS_RN0
H30		FBA_DQS_RN1
E34		FBA_DQS_RN2
M34		FBA_DQS_RN3
AF30		FBA_DQS_RN4
AK31		FBA_DQS_RN5
AM34		FBA_DQS_RN6
AF32		FBA_DQS_RN7

T7101 1 H26 FB_VREF

N14P-GT1
/DGPU

FB_CLAMP E1 FB_CLAMP_R R7121 2 /DGPU 1 0Ohm FB_CLAMP → FB_CLAMP 30,74,84
R7130 2 /DGPU 1 10KOhm → GND
+1.05VS_VGA
FB_DLL_AVDD K27 +FB_DLL_AVDD_R L7102 1 /DGPU 2 30Ohm/100Mhz
50mA C7115 0.1UF/10V 10% /DGPU
C7121 22UF/6.3V /DGPU

FB_DLL_AVDD		
EGL	1.05V	50mA
PGV		35mA

20121212(Eli)
FB_DLL_AVDD table follow NV SPEC DG_06246_001_V04 Page121

GDDR5 CMD Mapping Table

<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE*
13	29	RESET*

FBA_CMD0	T31	FBA_CMD0
FBA_CMD1	U29	FBA_CMD1
FBA_CMD2	R34	FBA_CMD2
FBA_CMD3	R33	FBA_CMD3
FBA_CMD4	U32	FBA_CMD4
FBA_CMD5	U33	FBA_CMD5
FBA_CMD6	U28	FBA_CMD6
FBA_CMD7	V28	FBA_CMD7
FBA_CMD8	V29	FBA_CMD8
FBA_CMD9	V30	FBA_CMD9
FBA_CMD10	U34	FBA_CMD10
FBA_CMD11	U31	FBA_CMD11
FBA_CMD12	V34	FBA_CMD12
FBA_CMD13	V33	FBA_CMD13
FBA_CMD14	V32	FBA_CMD14
FBA_CMD15	AA31	FBA_CMD15
FBA_CMD16	AA29	FBA_CMD16
FBA_CMD17	AA28	FBA_CMD17
FBA_CMD18	AC34	FBA_CMD18
FBA_CMD19	AC33	FBA_CMD19
FBA_CMD20	AA32	FBA_CMD20
FBA_CMD21	AA33	FBA_CMD21
FBA_CMD22	Y28	FBA_CMD22
FBA_CMD23	Y29	FBA_CMD23
FBA_CMD24	W31	FBA_CMD24
FBA_CMD25	Y30	FBA_CMD25
FBA_CMD26	AA34	FBA_CMD26
FBA_CMD27	Y31	FBA_CMD27
FBA_CMD28	Y34	FBA_CMD28
FBA_CMD29	Y33	FBA_CMD29
FBA_CMD30	V31	FBA_CMD30
FBA_CMD31		FBA_CMD31

FBA_CMD14 R7124 2 /DGPU 1 10KOhm +1.35VS_VGA
FBA_CMD30 R7123 2 /DGPU 1 10KOhm
FBA_CMD29 R7125 2 /DGPU 1 10KOhm
FBA_CMD13 R7126 2 /DGPU 1 10KOhm GND

FBA_CMD_RFU0 R32
FBA_CMD_RFU1 AC35

+1.35VS_VGA
FBA_DEBUG0 R28 FBA_DEBUG0 R7101 1 2 60.4Ohm 1%
FBA_DEBUG1 AC28 FBA_DEBUG1 R7102 1 2 60.4Ohm 1%

FBA_CLK0	R30	FBA_CLK0 76
FBA_CLK0_N	R31	FBA_CLK0# 76
FBA_CLK1	AB31	FBA_CLK1 77
FBA_CLK1_N	AC31	FBA_CLK1# 77

FBA_WCK01	K31	FBA_WCK01 76
FBA_WCK01_N	L30	FBA_WCK01# 76
FBA_WCK23	H34	FBA_WCK23 76
FBA_WCK23_N	J34	FBA_WCK23# 76
FBA_WCK45	AG30	FBA_WCK45 77
FBA_WCK45_N	AG31	FBA_WCK45# 77
FBA_WCK67	AJ34	FBA_WCK67 77
FBA_WCK67_N	AK34	FBA_WCK67# 77

FBA_WCKB01	J30	
FBA_WCKB01_N	J31	
FBA_WCKB23	J32	
FBA_WCKB23_N	J33	
FBA_WCKB45	AH31	
FBA_WCKB45_N	AJ31	
FBA_WCKB67	AJ32	
FBA_WCKB67_N	AJ33	

+FB_PLL_AVDD
FBA_PLL_AVDD U27 120mA
C7109 0.1UF/10V /DGPU
C7119 22UF/6.3V /DGPU
Place Close to BALL
Place Close to BGA

+FB_PLL_AVDD → C7112 1UF/6.3V 10% /DGPU
L7101 30Ohm/100Mhz /PGV
+1.05VS_VGA → C7113 1UF/6.3V 10% /PGV
L7103 30Ohm/100Mhz /EGL
+3VS_VGA → C7122 1UF/6.3V 10% /EGL

FBx_PLL_AVDD		
EGL	3.3V	120mA
PGV	1.05V	62mA

Place Close to BGA

20121214(Eli)
R7129 change to bead type 30ohm(ESR=0.01ohm) follow NV FAE recommend

U7001C
3/19 FBB

FBBD0	G9	FBB_D0
FBBD1	E9	FBB_D1
FBBD2	G8	FBB_D2
FBBD3	F9	FBB_D3
FBBD4	F11	FBB_D4
FBBD5	G11	FBB_D5
FBBD6	F12	FBB_D6
FBBD7	G12	FBB_D7
FBBD8	G6	FBB_D8
FBBD9	F5	FBB_D9
FBBD10	E6	FBB_D10
FBBD11	F6	FBB_D11
FBBD12	F4	FBB_D12
FBBD13	G4	FBB_D13
FBBD14	E2	FBB_D14
FBBD15	F3	FBB_D15
FBBD16	C2	FBB_D16
FBBD17	D4	FBB_D17
FBBD18	D3	FBB_D18
FBBD19	C1	FBB_D19
FBBD20	B3	FBB_D20
FBBD21	C4	FBB_D21
FBBD22	B5	FBB_D22
FBBD23	C5	FBB_D23
FBBD24	A11	FBB_D24
FBBD25	C11	FBB_D25
FBBD26	D11	FBB_D26
FBBD27	B11	FBB_D27
FBBD28	D8	FBB_D28
FBBD29	A8	FBB_D29
FBBD30	C8	FBB_D30
FBBD31	B8	FBB_D31
FBBD32	F24	FBB_D32
FBBD33	G23	FBB_D33
FBBD34	E24	FBB_D34
FBBD35	G24	FBB_D35
FBBD36	D21	FBB_D36
FBBD37	E21	FBB_D37
FBBD38	G21	FBB_D38
FBBD39	F21	FBB_D39
FBBD40	G27	FBB_D40
FBBD41	D27	FBB_D41
FBBD42	G26	FBB_D42
FBBD43	E27	FBB_D43
FBBD44	E29	FBB_D44
FBBD45	F29	FBB_D45
FBBD46	E30	FBB_D46
FBBD47	D30	FBB_D47
FBBD48	A32	FBB_D48
FBBD49	C31	FBB_D49
FBBD50	C32	FBB_D50
FBBD51	B32	FBB_D51
FBBD52	D29	FBB_D52
FBBD53	A29	FBB_D53
FBBD54	C29	FBB_D54
FBBD55	B29	FBB_D55
FBBD56	B31	FBB_D56
FBBD57	C23	FBB_D57
FBBD58	A21	FBB_D58
FBBD59	C21	FBB_D59
FBBD60	B24	FBB_D60
FBBD61	C24	FBB_D61
FBBD62	B26	FBB_D62
FBBD63	C26	FBB_D63

FBB_DBI0	E11	FBB_DQM0
FBB_DBI1	E3	FBB_DQM1
FBB_DBI2	A3	FBB_DQM2
FBB_DBI3	C9	FBB_DQM3
FBB_DBI4	F23	FBB_DQM4
FBB_DBI5	F27	FBB_DQM5
FBB_DBI6	C30	FBB_DQM6
FBB_DBI7	A24	FBB_DQM7

FBB_EDC0	D10	FBB_DQS_WP0
FBB_EDC1	D5	FBB_DQS_WP1
FBB_EDC2	C3	FBB_DQS_WP2
FBB_EDC3	B9	FBB_DQS_WP3
FBB_EDC4	E23	FBB_DQS_WP4
FBB_EDC5	E28	FBB_DQS_WP5
FBB_EDC6	B30	FBB_DQS_WP6
FBB_EDC7	A23	FBB_DQS_WP7

D9		FBB_DQS_RN0
E4		FBB_DQS_RN1
B2		FBB_DQS_RN2
A9		FBB_DQS_RN3
D22		FBB_DQS_RN4
D28		FBB_DQS_RN5
A30		FBB_DQS_RN6
B23		FBB_DQS_RN7

N14P-GT1
/DGPU

FBB_CMD0	D13	FBB_CMD0
FBB_CMD1	E14	FBB_CMD1
FBB_CMD2	F14	FBB_CMD2
FBB_CMD3	A12	FBB_CMD3
FBB_CMD4	B12	FBB_CMD4
FBB_CMD5	C14	FBB_CMD5
FBB_CMD6	B14	FBB_CMD6
FBB_CMD7	G15	FBB_CMD7
FBB_CMD8	F15	FBB_CMD8
FBB_CMD9	E15	FBB_CMD9
FBB_CMD10	D15	FBB_CMD10
FBB_CMD11	A14	FBB_CMD11
FBB_CMD12	D14	FBB_CMD12
FBB_CMD13	A15	FBB_CMD13
FBB_CMD14	B15	FBB_CMD14
FBB_CMD15	C17	FBB_CMD15
FBB_CMD16	D18	FBB_CMD16
FBB_CMD17	E18	FBB_CMD17
FBB_CMD18	F18	FBB_CMD18
FBB_CMD19	A20	FBB_CMD19
FBB_CMD20	B20	FBB_CMD20
FBB_CMD21	C18	FBB_CMD21
FBB_CMD22	B18	FBB_CMD22
FBB_CMD23	G18	FBB_CMD23
FBB_CMD24	G17	FBB_CMD24
FBB_CMD25	F17	FBB_CMD25
FBB_CMD26	D16	FBB_CMD26
FBB_CMD27	A18	FBB_CMD27
FBB_CMD28	D17	FBB_CMD28
FBB_CMD29	A17	FBB_CMD29
FBB_CMD30	B17	FBB_CMD30
FBB_CMD31	E17	FBB_CMD31

+1.35VS_VGA
FBB_CMD30 R7119 2 /DGPU 1 10KOhm
FBB_CMD14 R7122 2 /DGPU 1 10KOhm
FBB_CMD29 R7120 2 /DGPU 1 10KOhm
FBB_CMD13 R7127 2 /DGPU 1 10KOhm GND

FBB_CMD_RFU0 C12
FBB_CMD_RFU1 C20

+1.35VS_VGA
FBB_DEBUG0 G14 FBC_DEBUG0 R7103 1 2 60.4Ohm 1%
FBB_DEBUG1 G20 FBC_DEBUG1 R7104 1 2 60.4Ohm 1%

FBB_CLK0	D12	FBB_CLK0 78
FBB_CLK0_N	E12	FBB_CLK0# 78
FBB_CLK1	E20	FBB_CLK1 79
FBB_CLK1_N	F20	FBB_CLK1# 79

FBB_WCK01	F8	FBB_WCK01 78
FBB_WCK01_N	E8	FBB_WCK01# 78
FBB_WCK23	A5	FBB_WCK23 78
FBB_WCK23_N	A6	FBB_WCK23# 78
FBB_WCK45	D24	FBB_WCK45 79
FBB_WCK45_N	D25	FBB_WCK45# 79
FBB_WCK67	B27	FBB_WCK67 79
FBB_WCK67_N	C27	FBB_WCK67# 79

FBB_WCKB01	D6	
FBB_WCKB01_N	D7	
FBB_WCKB23	C6	
FBB_WCKB23_N	B6	
FBB_WCKB45	F26	
FBB_WCKB45_N	E26	
FBB_WCKB67	A26	
FBB_WCKB67_N	A27	

FBB_PLL_AVDD H17 120mA
+FB_PLL_AVDD
C7120 0.1UF/10V 10% /DGPU
Place Close to BALL

PEGATRON
PEGATRON COMPUTER INC
Title : N14xxx BUFFER
Engineer: Panda_Wang
Size C | Project Name VA70_HW | Rev 1.3
P/N
Date: Friday, January 18, 2013 | Sheet 71 of 99

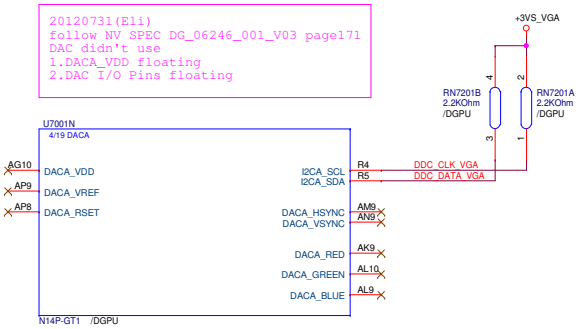
VGA

+1.05VS_VGA
+3VS_VGA

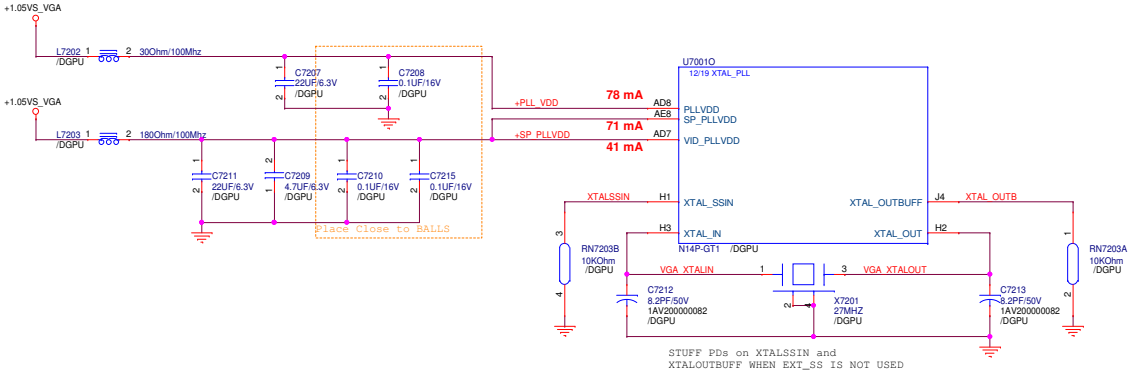
+1.05VS_VGA 63,70,71,91
+3VS_VGA 63,70,71,74,75,87,91

20120731(Eli)
follow NV SPEC DG_06246_001_V03 page171
DAC didn't use
1.DACA_VDD floating
2.DAC I/O Pins floating

20121214(Eli)
Modify RN7201 optional from @ to /DGPU and remove R7201
follow NV FAE recommend



X'TAL



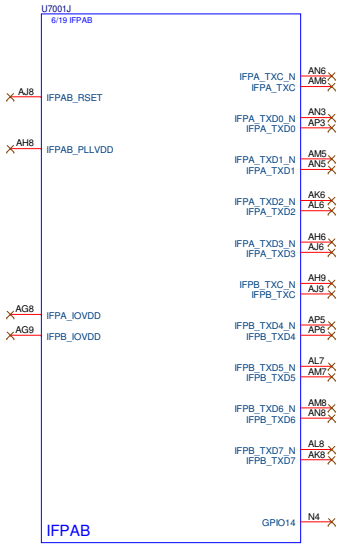
PEGATRON
PEGATRON COMPUTER INC

Title : N14xxx_RGB,XTAL
Engineer: Panda_Wang

Size	Project Name	Rev
C	VA70_HW	1.3
	P/N	

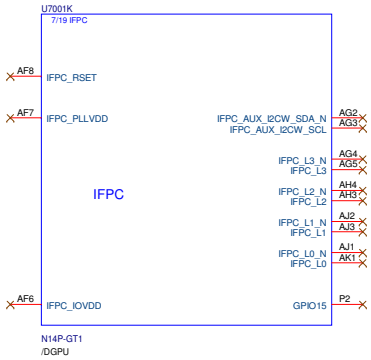
Date: Friday, January 18, 2013 Sheet 72 of 99

LVDS

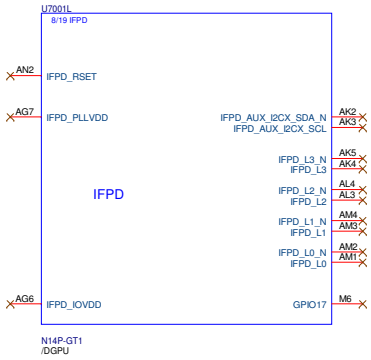


20121214(Eli)
Remove R7303, R7304, R7305, R7306, R7308, R7309, R7310, R7312, RN7301, RN7302 follow NV FAE recommend

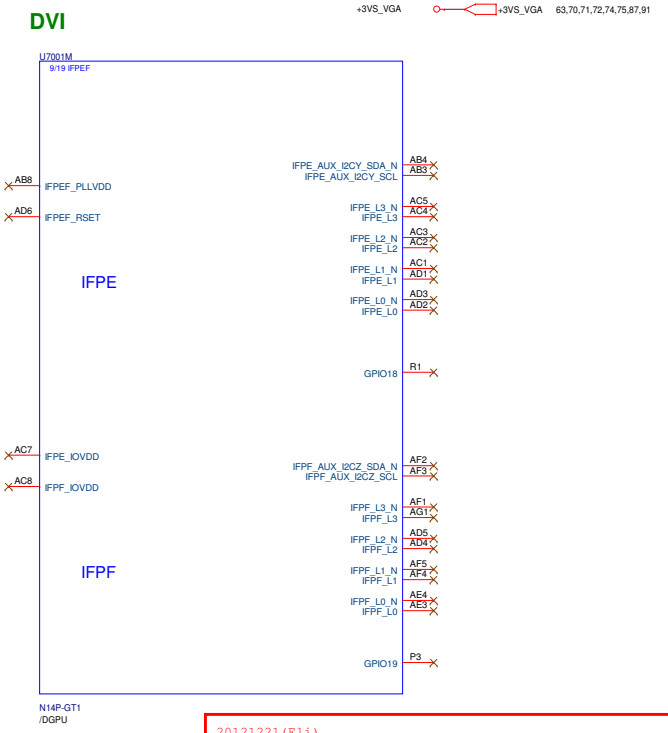
HDMI



eDP



DVI



20121221(Eli)
Remove T7301, T7302, T7303, T7304 follow NV FAE recommend

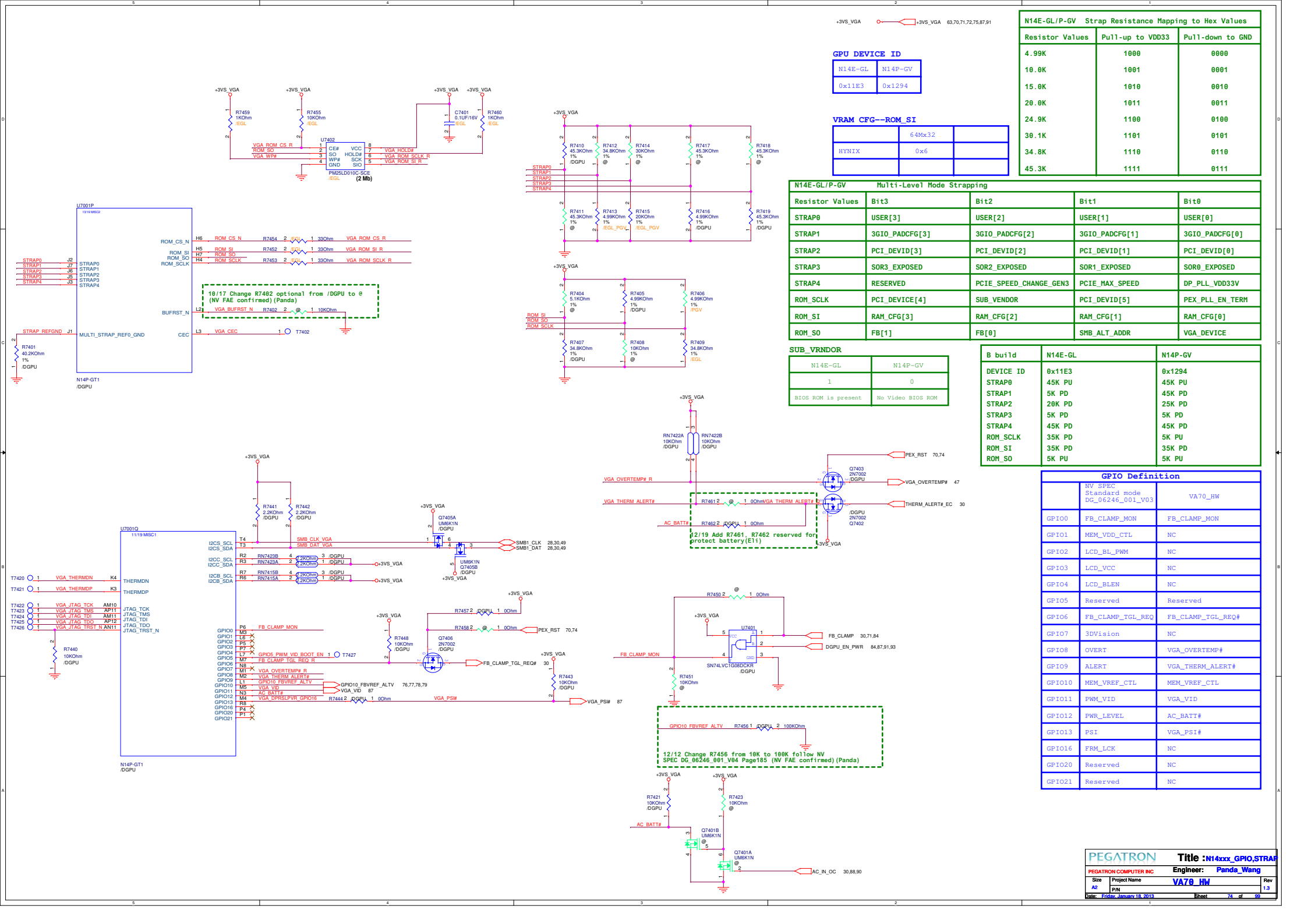
IFPX channel

	N14E-GL Standard Mode	N14P-GV Combined Mode
IFPA	LVDS	LVDS(DP/DVI)
IFPB	LVDS	LVDS(DP/DVI)
IFPC	DP/HDMI	DP/HDMI
IFPD	DP/eDP	DP/eDP
IFPE	DP/DVI	X
IFPF	DP/DVI	X

GPIO Definition

	NV SPEC Standard mode DG_06246_001_V03	VA70_HW
GPIO14	IFPAB_HPD(LVDS)	NC
GPIO15	IFPC_HPD(HDMI)	NC
GPIO17	IFPD_HPD(eDP)	NC
GPIO18	IFPE_HPD(DVI)	NC
GPIO19	IFPF_HPD(DVI)	NC

PEGATRON
PEGATRON COMPUTER INC
Title : N14xxx_LVDS_HDMI
Engineer: Panda_Wang
Size: C | Project Name: VA70_HW | Rev: 1.3
P/N:
Date: Friday, January 18, 2013 | Sheet 73 of 99


+3VS_VGA
+3VS_VGA 63,70,71,72,75,87,91
GPU DEVICE ID
N14E-GL | N14P-GV
0x11E3 | 0x1294
VRAM CFG--ROM_SI
64Mx32
HYNIX | 0x6
N14E-GL/P-GV Strap Resistance Mapping to Hex Values
Resistor Values | Pull-up to VDD33 | Pull-down to GND
4.99K | 1000 | 0000
10.0K | 1001 | 0001
15.0K | 1010 | 0010
20.0K | 1011 | 0011
24.9K | 1100 | 0100
30.1K | 1101 | 0101
34.8K | 1110 | 0110
45.3K | 1111 | 0111
N14E-GL/P-GV Multi-Level Mode Strapping
Resistor Values | Bit3 | Bit2 | Bit1 | Bit0
STRAP0 | USER[3] | USER[2] | USER[1] | USER[0]
STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0]
STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0]
STRAP3 | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED
STRAP4 | RESERVED | PCIE_SPEED_CHANGE_GEN3 | PCIE_MAX_SPEED | DP_PLL_VDD33V
ROM_SCLK | PCI_DEVICE[4] | SUB_VENDOR | PCI_DEVID[5] | PEX_PLL_EN_TERM
ROM_SI | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0]
ROM_SO | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE
SUB_VRNDOR
N14E-GL | N14P-GV
1 | 0
BIOS ROM is present | No Video BIOS ROM
B build | N14E-GL | N14P-GV
DEVICE ID | 0x11E3 | 0x1294
STRAP0 | 45K PU | 45K PU
STRAP1 | 5K PD | 45K PD
STRAP2 | 20K PD | 25K PD
STRAP3 | 5K PD | 5K PD
STRAP4 | 45K PD | 45K PD
ROM_SCLK | 35K PD | 5K PU
ROM_SI | 35K PD | 35K PD
ROM_SO | 5K PU | 5K PU
GPIO Definition
 | NV SPEC Standard mode DG_06246_001_V03 | VA70_HW
GPIO0 | FB_CLAMP_MON | FB_CLAMP_MON
GPIO1 | MEM_VDD_CTL | NC
GPIO2 | LCD_BL_PWM | NC
GPIO3 | LCD_VCC | NC
GPIO4 | LCD_BLEN | NC
GPIO5 | Reserved | Reserved
GPIO6 | FB_CLAMP_TGL_REQ | FB_CLAMP_TGL_REQ#
GPIO7 | 3DVision | NC
GPIO8 | OVERT | VGA_OVERTEMP#
GPIO9 | ALERT | VGA_THERM_ALERT#
GPIO10 | MEM_VREF_CTL | MEM_VREF_CTL
GPIO11 | PWM_VID | VGA_VID
GPIO12 | PWR_LEVEL | AC_BATT#
GPIO13 | PSI | VGA_PSI#
GPIO16 | FRM_LCK | NC
GPIO20 | Reserved | NC
GPIO21 | Reserved | NC
U7001P
N14P-GT1
/DGPU
ROM_CS_N
ROM_SI
ROM_SO
ROM_SCLK
BUFRST_N
CEC
MULTI_STRAP_REF0_GND
STRAP_REFGND
10/17 Change R7402 optional from /DGPU to @ (NV FAE confirmed)(Panda)
U7402
PM25LD010C-SCE
/EGL
(2 Mb)
VGA_ROM_CS_R
ROM_SO
VGA_WP#
VGA_HOLD#
VGA_ROM_SCLK_R
VGA_ROM_SI_R
U7001Q
11/19 MISC1
N14P-GT1
/DGPU
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST_N
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
SMB_CLK_VGA
SMB_DAT_VGA
SMB1_CLK
SMB1_DAT
GPIO0 FB_CLAMP_MON
GPIO5_PWM_VID_BOOT_EN
FB_CLAMP_TGL_REQ_R
FB_CLAMP_TGL_REQ#
VGA_OVERTEMP#_R
VGA_THERM_ALERT#
VGA_VID
AC_BATT#
VGA_DPRSLPVR_GPIO16
GPIO10_FBVREF_ALTV
VGA_PSI#
PEX_RST
VGA_OVERTEMP#
THERM_ALERT#_EC
FB_CLAMP
DGPU_EN_PWR
12/19 Add R7461, R7462 reserved for protect battery(Eli)
12/12 Change R7456 from 10K to 100K follow NV SPEC DG_06246_001_V04 Page185 (NV FAE confirmed)(Panda)
AC_IN_OC
PEGATRON
Title : N14xxx_GPIO,STRAP
PEGATRON COMPUTER INC
Engineer: Panda_Wang
Size A2
Project Name VA70_HW
Rev 1.3
P/N
Date: Friday, January 18, 2013
Sheet 74 of 89

+3VS_VGA
+1.35VS_VGA
+VGA_VCORE

+3VS_VGA 63,70,71,72,74,87,91
+1.35VS_VGA 63,71,76,77,78,79,84
+VGA_VCORE 63,87

+VGA_VCORE

U7001E
14/19 NVVDD

PLACE UNDER GPU

C7511 C7510 C7513 C7512 C7515 C7514 C7517 C7516 0.1UF/16V /DGPU
C7518 C7519 C7520 C7521 C7522 C7523 C7524 C7530 4.7UF/6.3V /DGPU
C7525 C7526 C7527 C7528 C7529 C7536 C7537 4.7UF/6.3V /DGPU
C7531 C7532 C7533 C7535 C7534 C7552 C7553 4.7UF/6.3V /DGPU
22UF/6.3V /DGPU
47UF/4V @
CE7501 330UF/2V /DGPU
C7547 4.7UF/6.3V @
C7566 C7567 C7568 C7569 C7570 C7571 22UF/6.3V @
GND

PLACE NEAR GPU

VDD1 AA12
VDD2 AA14
VDD3 AA16
VDD4 AA19
VDD5 AA21
VDD6 AA23
VDD7 AB13
VDD8 AB15
VDD9 AB17
VDD10 AB18
VDD11 AB20
VDD12 AB22
VDD13 AC12
VDD14 AC14
VDD15 AC16
VDD16 AC19
VDD17 AC21
VDD18 AC23
VDD19 M12
VDD20 M14
VDD21 M16
VDD22 M19
VDD23 M21
VDD24 M23
VDD25 N13
VDD26 N15
VDD27 N17
VDD28 N18
VDD29 N20
VDD30 N22
VDD31 P12
VDD32 P14
VDD33 P16
VDD34 P19
VDD35 P21
VDD36 P23
VDD37 R13
VDD38 R15
VDD39 R17
VDD40 R18
VDD41 R20
VDD42 R22
VDD43 T12
VDD44 T14
VDD45 T16
VDD46 T19
VDD47 T21
VDD48 T23
VDD49 U13
VDD50 U15
VDD51 U17
VDD52 U18
VDD53 U20
VDD54 U22
VDD55 V13
VDD56 V15
VDD57 V17
VDD58 V18
VDD59 V20
VDD60 V22
VDD61 W12
VDD62 W14
VDD63 W16
VDD64 W19
VDD65 W21
VDD66 W23
VDD67 Y13
VDD68 Y15
VDD69 Y17
VDD70 Y18
VDD71 Y20
VDD72 Y22

N14P-GT1
/DGPU

U7001F
18/19 NC/VDD33

85mA
+VDD33_GPU
C7507 C7501 C7504 0.1UF/16V /DGPU
C7502 1UF/6.3V /DGPU
C7503 4.7UF/6.3V /DGPU
Place near BALLs
Place near BGA
GND
R7501 2 /DGPU 1 0Ohm
+3VS_VGA

AC6 NC1
AJ28 NC2
AJ4 NC3
AJ5 NC4
AL11 NC5
C15 NC6
D19 NC7
D20 NC8
D23 NC9
D26 NC10
H31 NC11
T8 NC13
V32 NC14
3V3MISC_1
3V3MISC_2
VDD33_1
VDD33_2
J8
K8
L8
M8

N14P-GT1
/DGPU

XVDD

EGL	floating
PGV	NC

U7001H
10/19 XVDD

CONFIGURABLE POWER CHANNELS

XVDD_1 U1
XVDD_2 U2
XVDD_3 U3
XVDD_4 U4
XVDD_5 U5
XVDD_6 U6
XVDD_7 U7
XVDD_8 U8
XVDD_9 V1
XVDD_10 V2
XVDD_11 V3
XVDD_12 V4
XVDD_13 V5
XVDD_14 V6
XVDD_15 V7
XVDD_16 V8
XVDD_17 W2
XVDD_18 W3
XVDD_19 W4
XVDD_20 W5
XVDD_21 W7
XVDD_22 W8
XVDD_23 Y1
XVDD_24 Y2
XVDD_25 Y3
XVDD_26 Y4
XVDD_27 Y5
XVDD_28 Y6
XVDD_29 Y7
XVDD_30 Y8
XVDD_31 AA1
XVDD_32 AA2
XVDD_33 AA3
XVDD_34 AA4
XVDD_35 AA5
XVDD_36 AA6
XVDD_37 AA7
XVDD_38 AA8

N14P-GT1
/DGPU

U7001G
16/19 GND_1/2

A2 GND1
AA17 GND5
AA18 GND6
AA20 GND7
AA22 GND8
AB12 GND9
AB14 GND10
AB16 GND11
AB19 GND12
AB2 GND13
AB21 GND14
A33 GND2
AB23 GND15
AB28 GND16
AB30 GND17
AB32 GND18
AB5 GND19
AB7 GND20
AC13 GND21
AC15 GND22
AC17 GND23
AC18 GND24
AA13 GND3
AC20 GND25
AC22 GND26
AE2 GND27
AE28 GND28
AE30 GND29
AE32 GND30
AE33 GND31
AE5 GND32
AE7 GND33
AH10 GND34
AA15 GND35
AH13 GND4
AH16 GND37
AH19 GND38
AH2 GND39
AH22 GND40
AH24 GND41
AH28 GND42
AH29 GND43
AH30 GND44
AH32 GND45
AH33 GND46
AH5 GND47
AH7 GND48
AJ7 GND49
AK10 GND50
AK7 GND51
AL12 GND52
AL13 GND53
AL14 GND54
AL15 GND55
AL17 GND56
AL18 GND57
AL2 GND58
AL20 GND59
AL21 GND60
AL23 GND61
AL24 GND62
AL26 GND63
AL28 GND64
AL30 GND65
AL32 GND66
AL33 GND67
AL5 GND68
AM13 GND69
AM16 GND70
AM19 GND71
AM22 GND72
GND73 AM25
GND74 AN1
GND75 AN10
GND76 AN13
GND77 AN16
GND78 AN19
GND79 AN22
GND80 AN25
GND81 AN30
GND82 AN34
GND83 AN4
GND84 AN7
GND85 AP2
GND86 AP33
GND87 B1
GND88 B10
GND89 B22
GND90 B25
GND91 B28
GND92 B31
GND93 B34
GND94 B4
GND95 B7
GND96 C10
GND97 C13
GND98 C22
GND99 C25
GND100 C28
GND101 C7
GND102 D2
GND103 D31
GND104 D33
GND105 E10
GND106 E22
GND107 E25
GND108 E5
GND109 E7
GND110 F28
GND111 F7
GND112 G10
GND113 G13
GND114 G16
GND115 G19
GND116 G2
GND117 G22
GND118 G25
GND119 G28
GND120 G3
GND121 G30
GND122 G32
GND123 G33
GND124 G5
GND125 G7
GND126 K2
GND127 K28
GND128 K30
GND129 K32
GND130 K33
GND131 K5
GND132 K7
GND133 M13
GND134 M15
GND135 M17
GND136 M18
GND137 M20
GND138 M22
GND139 N12
GND140 N14
GND141 N16
GND142

N14P-GT1
/DGPU

U7001I
17/19 GND_2/2

N19 GND143
N2 GND144
N21 GND145
N23 GND146
N28 GND147
N30 GND148
N32 GND149
N33 GND150
N5 GND151
N7 GND152
P13 GND153
P15 GND154
P17 GND155
P18 GND156
P20 GND157
P22 GND158
R12 GND159
R14 GND160
R16 GND161
R19 GND162
R21 GND163
R23 GND164
T13 GND165
T15 GND166
T17 GND167
T18 GND168
T2 GND169
T20 GND170
T22 GND171
GND172 T28
GND173 T32
GND174 T5
GND175 T7
GND176 U12
GND177 U14
GND178 U16
GND179 U19
GND180 U21
GND181 U23
GND182 V12
GND183 V14
GND184 V16
GND185 V19
GND186 V21
GND187 V23
GND188 W13
GND189 W15
GND190 W17
GND191 W18
GND192 W20
GND193 W22
GND194 W28
GND195 Y12
GND196 Y14
GND197 Y16
GND198 Y19
GND199 Y21
GND200 Y23
AG11 GND34
GND36 AH11
GND_OPT1 GND_OPT2 C16 W32
Optional CMD GNDs (2)
NC for 4-Lyr cards

N14P-GT1
/DGPU

+1.35VS_VGA

U7001D
15/19 FBVDDQ

AA27 FBVDDQ1
AA30 FBVDDQ2
AB27 FBVDDQ3
AB33 FBVDDQ4
AC27 FBVDDQ5
AD27 FBVDDQ6
AE27 FBVDDQ7
AF27 FBVDDQ8
AG27 FBVDDQ9
B13 FBVDDQ10
B16 FBVDDQ11
B19 FBVDDQ12
E13 FBVDDQ13
E16 FBVDDQ14
E19 FBVDDQ15
H10 FBVDDQ16
H11 FBVDDQ17
H12 FBVDDQ18
H13 FBVDDQ19
H14 FBVDDQ20
H15 FBVDDQ21
H16 FBVDDQ22
H18 FBVDDQ23
H19 FBVDDQ24
H20 FBVDDQ25
H21 FBVDDQ26
H22 FBVDDQ27
H23 FBVDDQ28
H24 FBVDDQ29
H8 FBVDDQ30
H9 FBVDDQ31
L27 FBVDDQ32
M27 FBVDDQ33
N27 FBVDDQ34
P27 FBVDDQ35
R27 FBVDDQ36
T27 FBVDDQ37
T30 FBVDDQ38
T33 FBVDDQ39
V27 FBVDDQ40
W27 FBVDDQ41
W30 FBVDDQ42
W33 FBVDDQ43
Y27 FBVDDQ44

+1.35VS_VGA

C7539 C7559 C7544 C7538 C7574 C7555 C7554 C7541 0.1UF/16V /DGPU
1UF/6.3V /DGPU
4.7UF/6.3V /DGPU
10UF/6.3V /DGPU
22UF/6.3V /DGPU
C7551 C7556 C7545 C7560 C7575 C7562 C7550 C7557 0.1UF/16V /DGPU
1UF/6.3V /DGPU
4.7UF/6.3V /DGPU
10UF/6.3V /DGPU
22UF/6.3V /DGPU
GND
Place Close to BALLs
Place Under to BGA
Place Close to BGA

C7563 C7564 C7565 @ 0.1UF/16V
GND

Add C7563,C7564,C7565 (0.1uF) at +1.35VS_VGA (EMI Recommend)

Check with NV

T7508
T7509

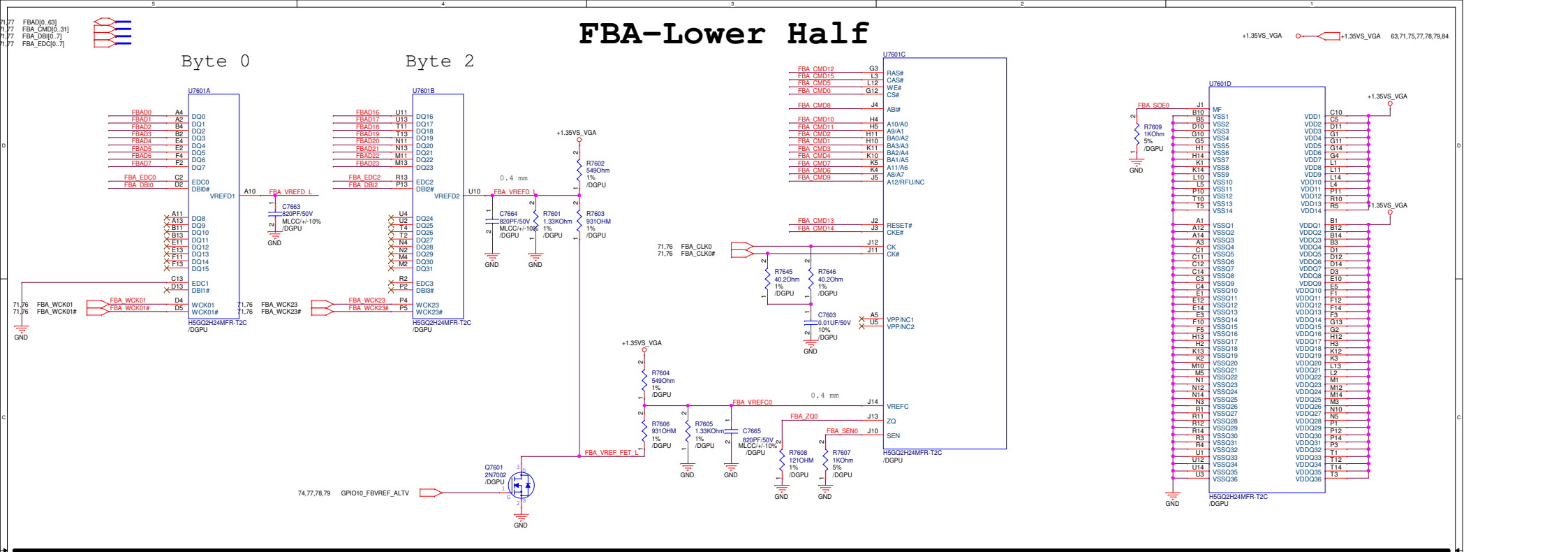
FB_VDDQ_SENSE F1 FBVDDQ_SENSE 1
FB_GND_SENSE F2 FBVDDQ_GND_SENSE 1
FB_CAL_PD_VDDQ J27 +FB_CAL_PD_VDDQ
FB_CAL_PU_GND H27 +FB_CAL_PU_GND
FB_CAL_TERM_GND H25 +FB_CAL_TERM_GND

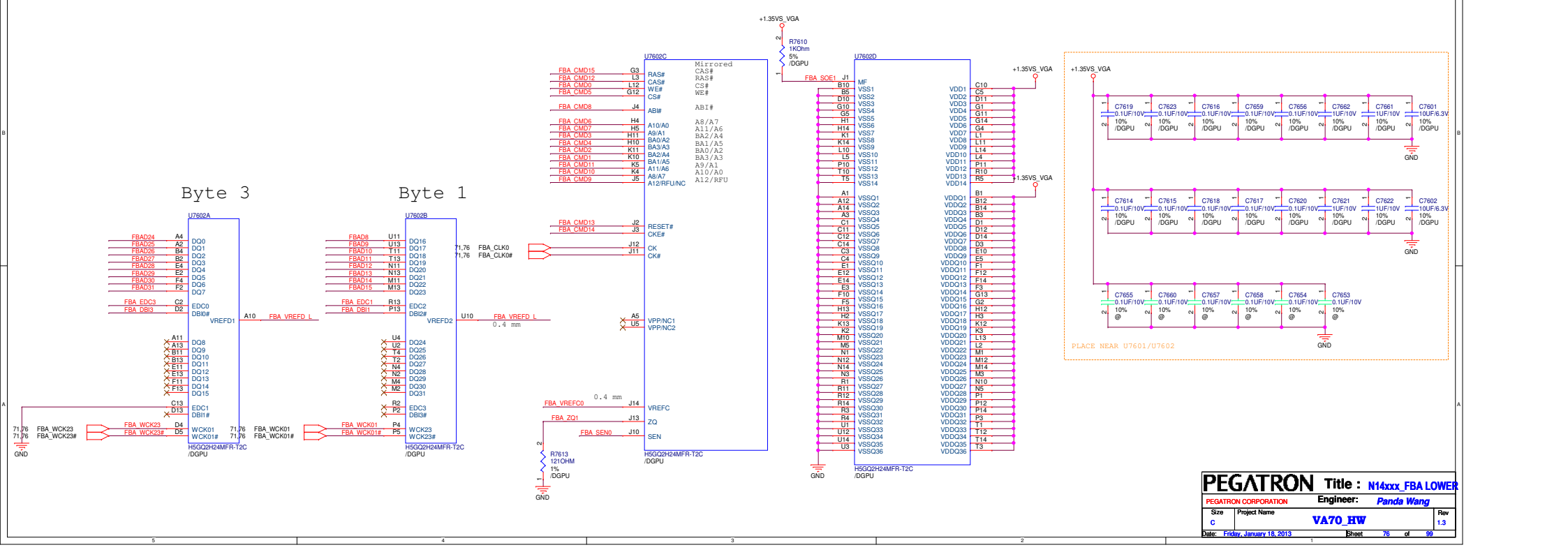
+1.35VS_VGA
R7507 1 /DGPU 2 40.2Ohm 1%
R7509 1 /DGPU 2 40.2Ohm 1%
R7510 /DGPU 60.4Ohm
GND
Place Close to BALLs

CALIBRATION PIN	DDR3	GDDR5
FB_CALx_PD_VDDQ	40	40.2
FB_CALx_PU_GND	42.2	40.2
FB_CALx_TERM_GND	51.1	60.4

PEGATRON
Title :N14xxx_Power,GND
PEGATRON COMPUTER INC
Engineer: Panda_Wang
Size C
Project Name VA70_HW
Rev 1.3
P/N
Date: Friday, January 18, 2013
Sheet 75 of 99

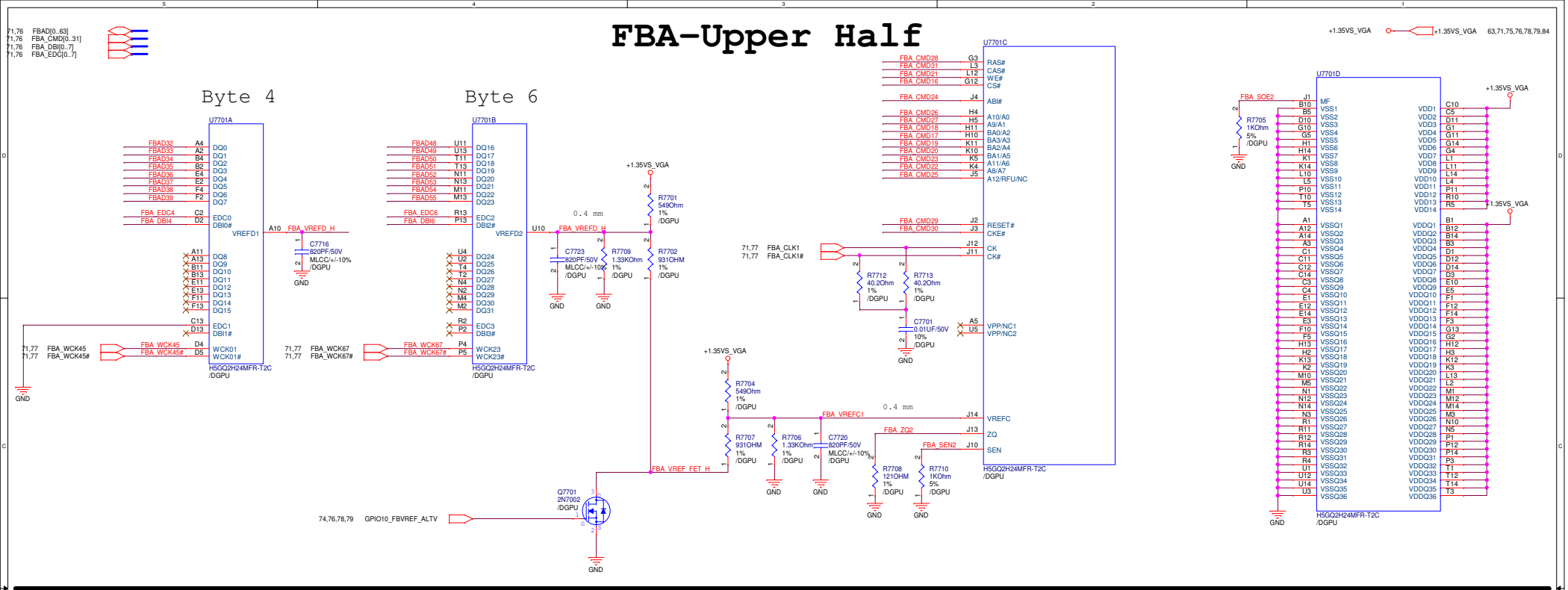
FBA-Lower Half

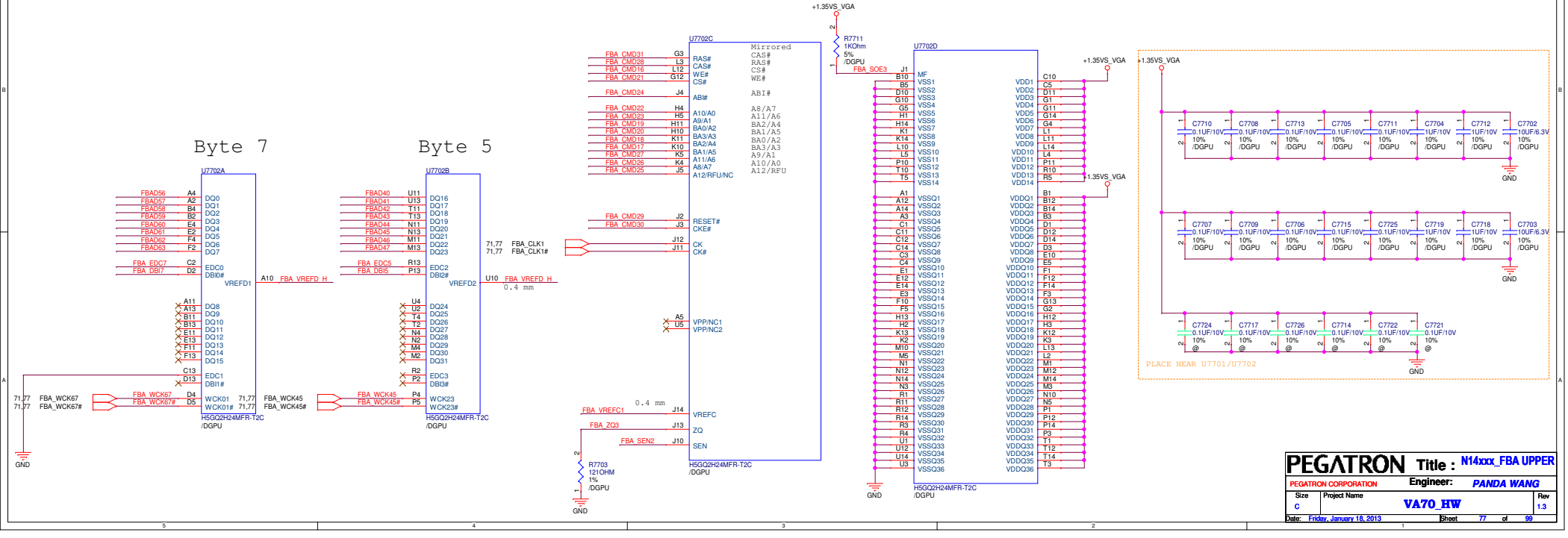




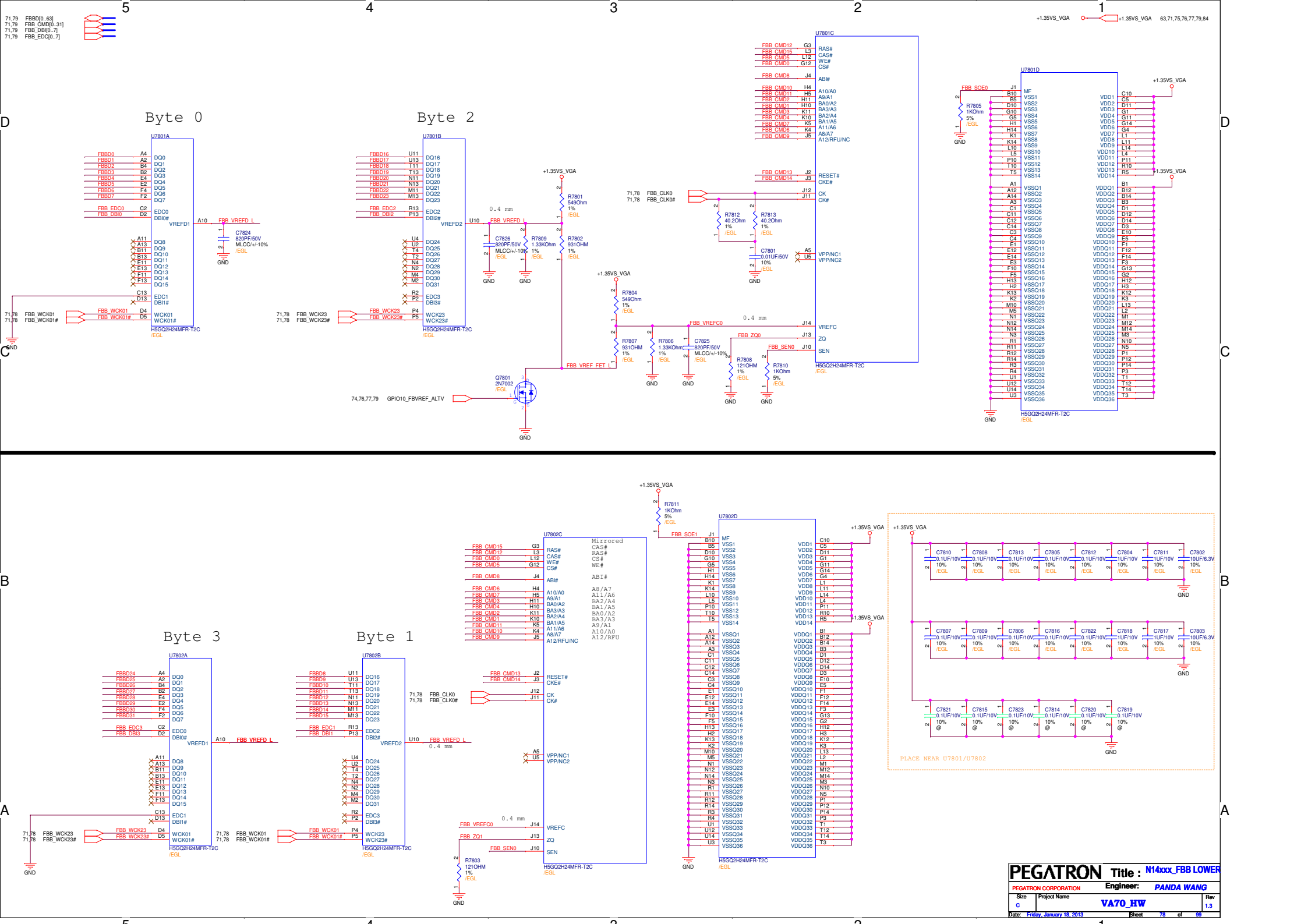
PEGATRON	Title : N14xxx_FBA LOWER		
PEGATRON CORPORATION	Engineer: Panda Wang		
Size: C	Project Name: VA70_HW		Rev: 1.3
Date: Friday, January 18, 2013	Sheet 76 of 99		

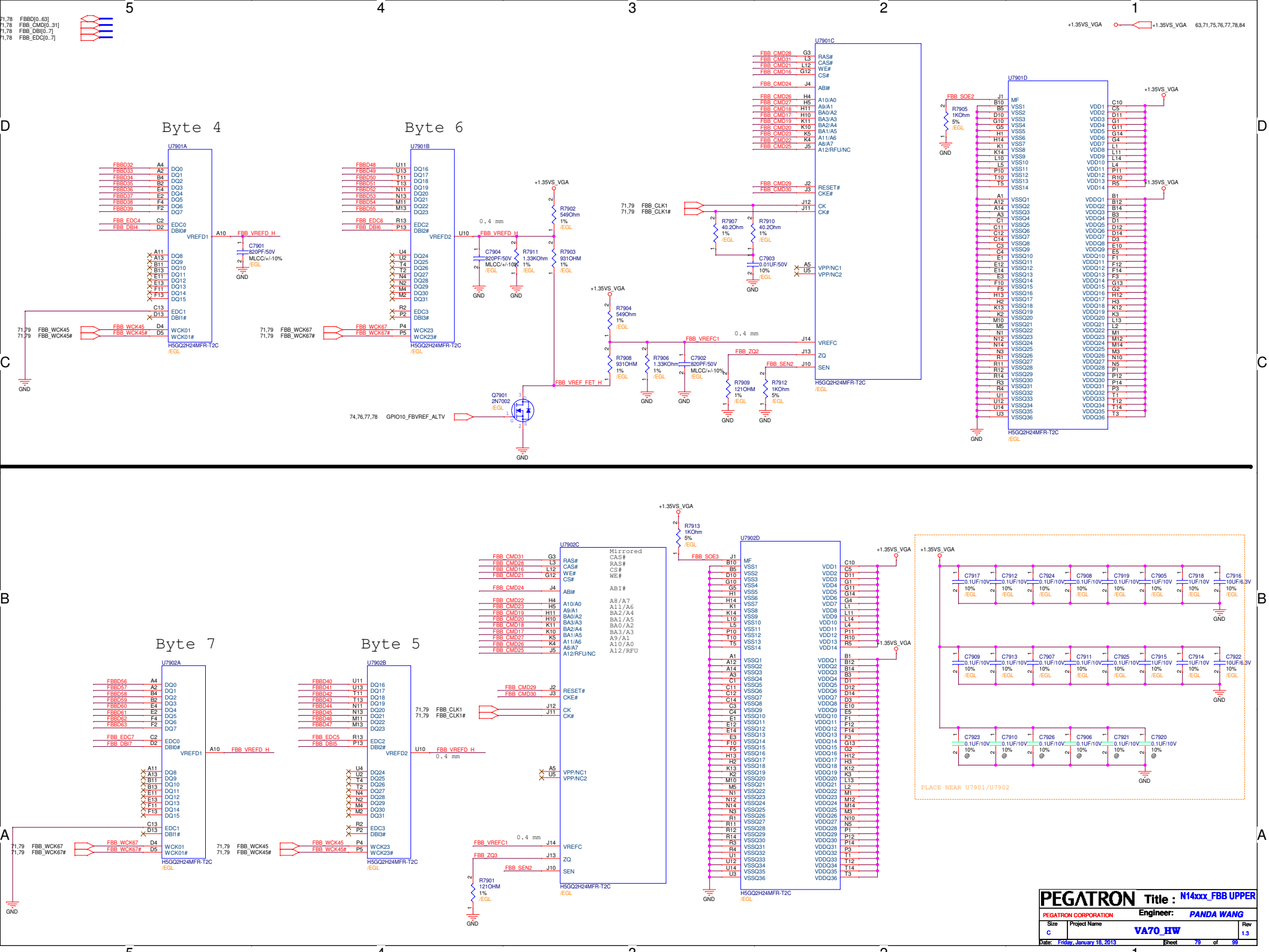
FBA-Upper Half





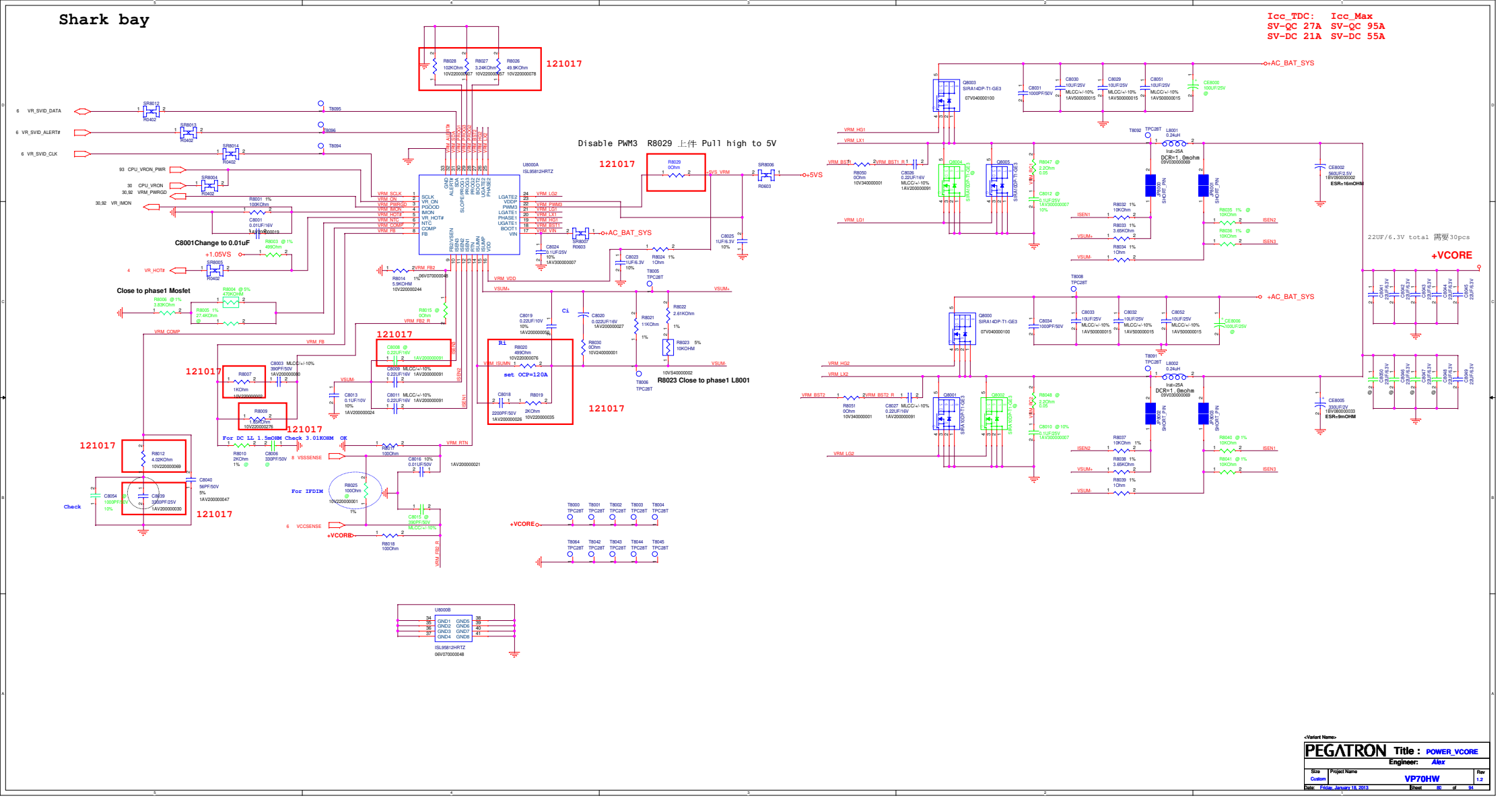
PEGATRON	Title :	N14xxx_FBA UPPER	
PEGATRON CORPORATION	Engineer:	PANDA WANG	
Size: C	Project Name: VA70_HW		Rev: 1.3
Date: Friday, January 18, 2013	Sheet 77 of 99		


Byte 0
Byte 2
Byte 3
Byte 1
U7801A
U7801B
U7801C
U7801D
U7802A
U7802B
U7802C
U7802D
H5GQ2H24MFR-T2C
+1.35VS_VGA
GND
FBB_VREFD_L
FBB_VREFC0
FBB_VREF_FET_L
FBB_ZQ0
FBB_SEN0
FBB_WCK01
FBB_WCK23
FBB_CLK0
GPIO10_FBVREF_ALTV
PLACE NEAR U7801/U7802
PEGATRON
Title : N14xxx_FBB LOWER
PEGATRON CORPORATION
Engineer: PANDA WANG
Project Name
VA70_HW
Date: Friday, January 18, 2013
Sheet 78 of 99


Byte 4
Byte 6
Byte 7
Byte 5
U7901A
U7901B
U7901C
U7901D
U7902A
U7902B
U7902C
U7902D
H5GQ2H24MFR-T2C
/EGL
GND
+1.35VS_VGA
FBB_VREFD_H
FBB_VREF_FET_H
FBB_VREFC1
FBB_ZQ2
FBB_SEN2
FBB_SOE2
FBB_SOE3
FBB_CLK1
FBB_CLK1#
FBB_WCK45
FBB_WCK45#
FBB_WCK67
FBB_WCK67#
GPIO10_FBVREF_ALTV
Q7901
2N7002
0.4 mm
PLACE NEAR U7901/U7902
PEGATRON
Title : N14xxx_FBB UPPER
PEGATRON CORPORATION
Engineer: PANDA WANG
Size C
Project Name VA70_HW
Rev 1.3
Date: Friday, January 18, 2013
Sheet 79 of 99

Shark bay

Icc_TDC: Icc_Max
SV-QC 27A SV-QC 95A
SV-DC 21A SV-DC 55A



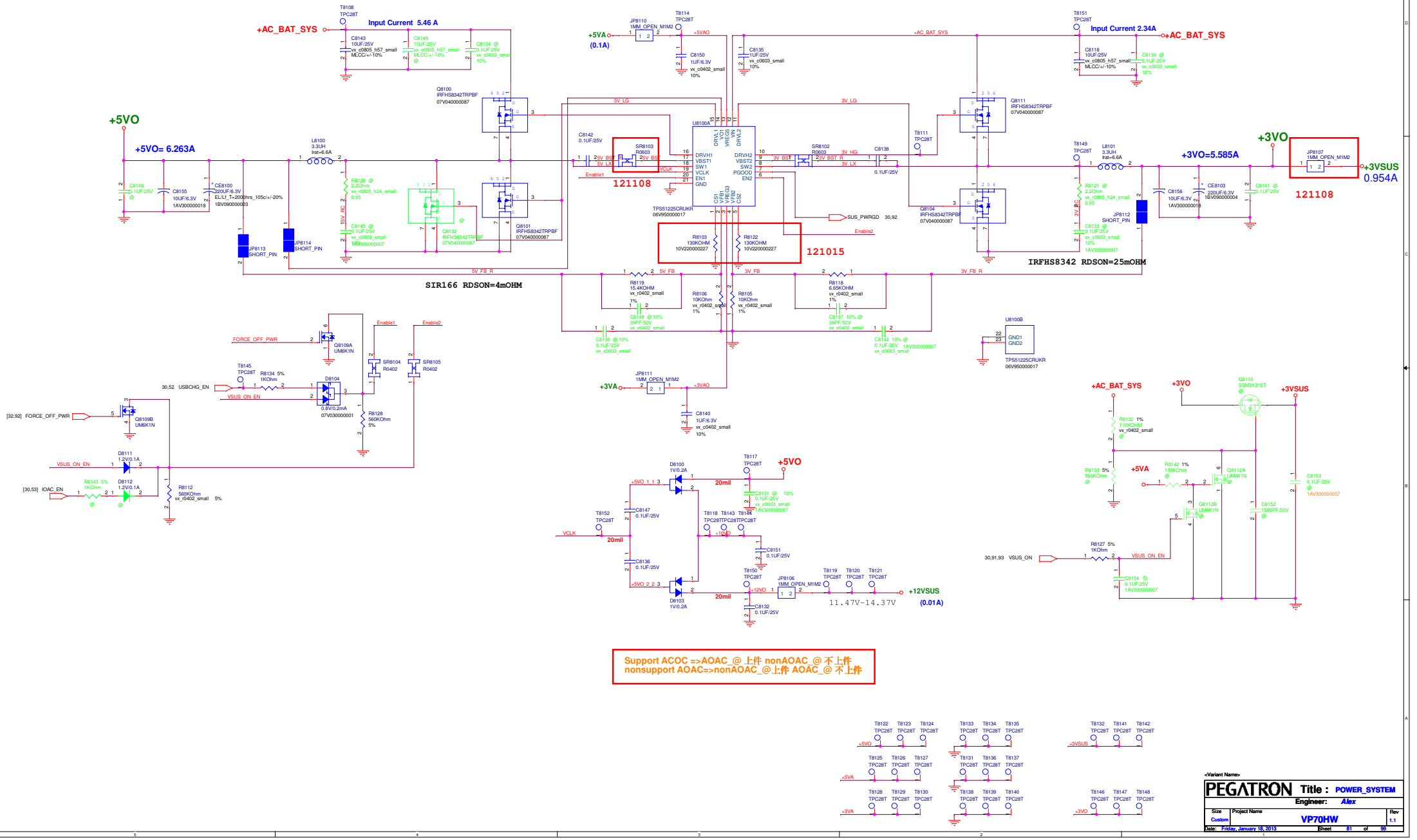
<Variant Name>

PEGATRON Title : POWER_VCORE
Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.2

Date: Friday, January 18, 2013 Sheet 80 of 94

+5VO & +3VO POWER SUPPLY



<variant_name>

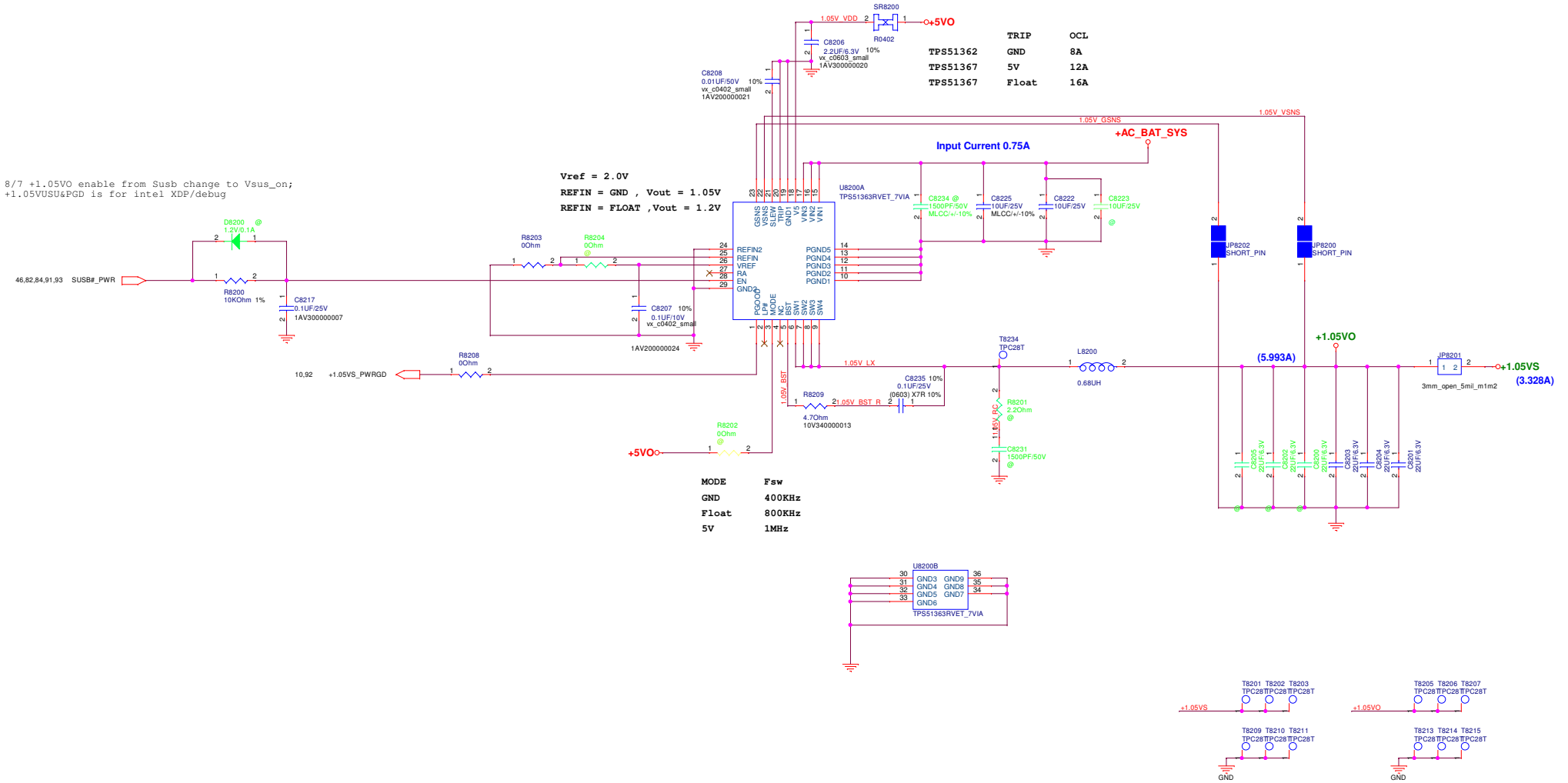
PEGATRON Title : POWER_SYSTEM

Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 81 of 99

+1.05VS POWER SUPPLY



<Variant Name>

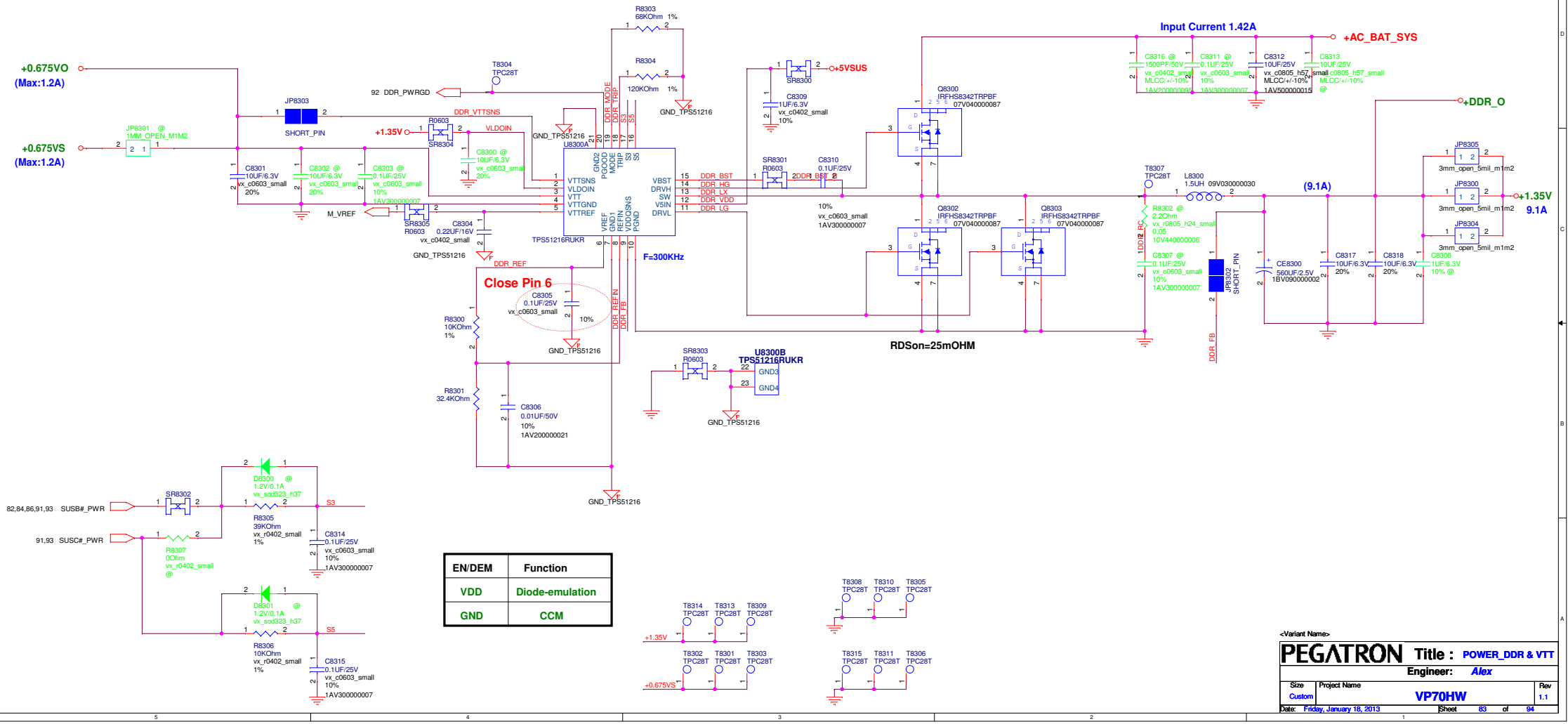
PEGATRON Title : POWER_+1.05VS

Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 82 of 94

DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

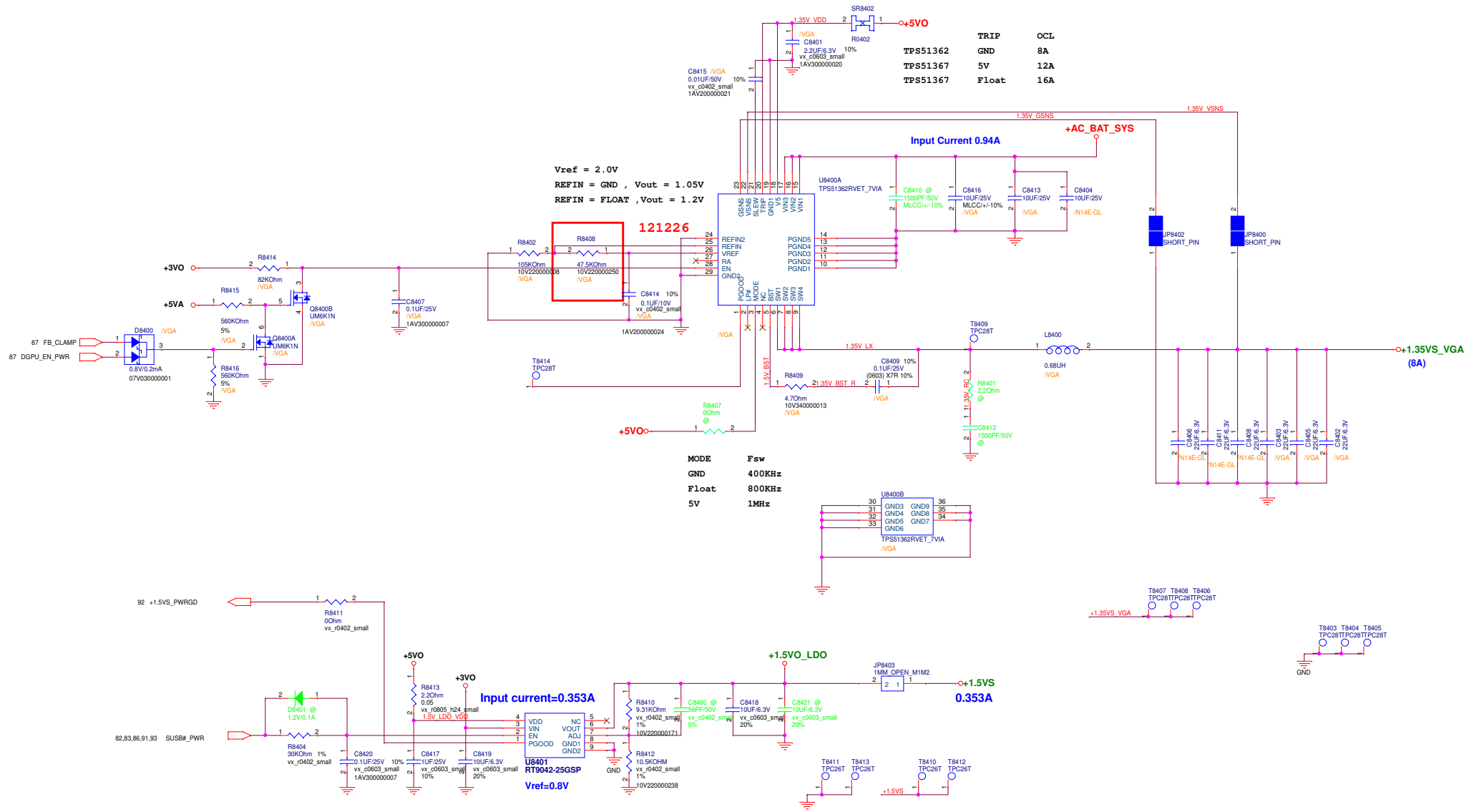
PEGATRON Title : POWER_DDR & VTT

Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 83 of 94

+1.35VS POWER SUPPLY



<Variant Name>

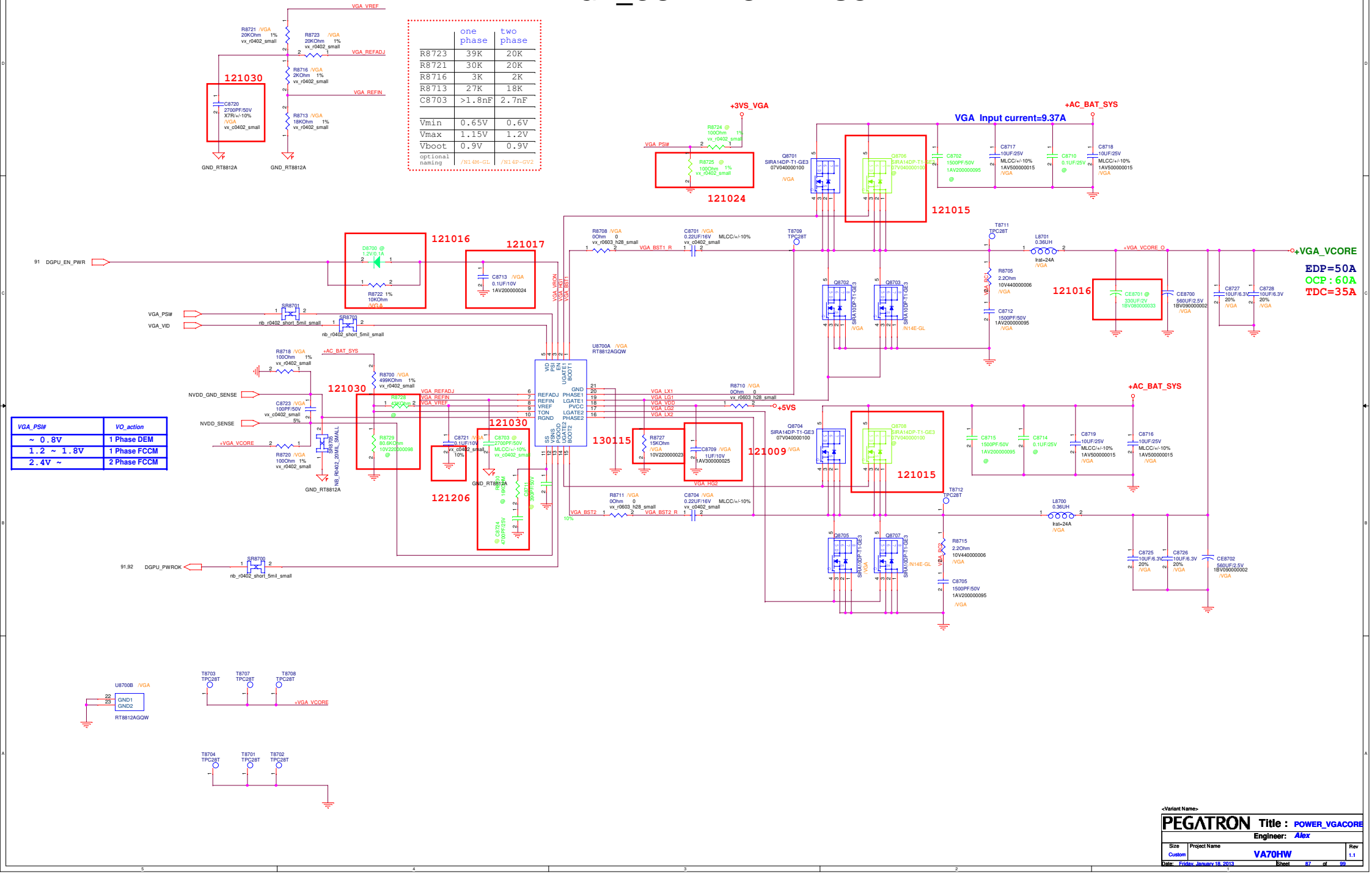
PEGATRON Title : POWER_1.5VS

Engineer: Alex

Size	Project Name	Rev
C	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 84 of 94

VGA_CORE POWER SUPPLY



VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

<variant_name>

PEGATRON Title : POWER_VGACORE

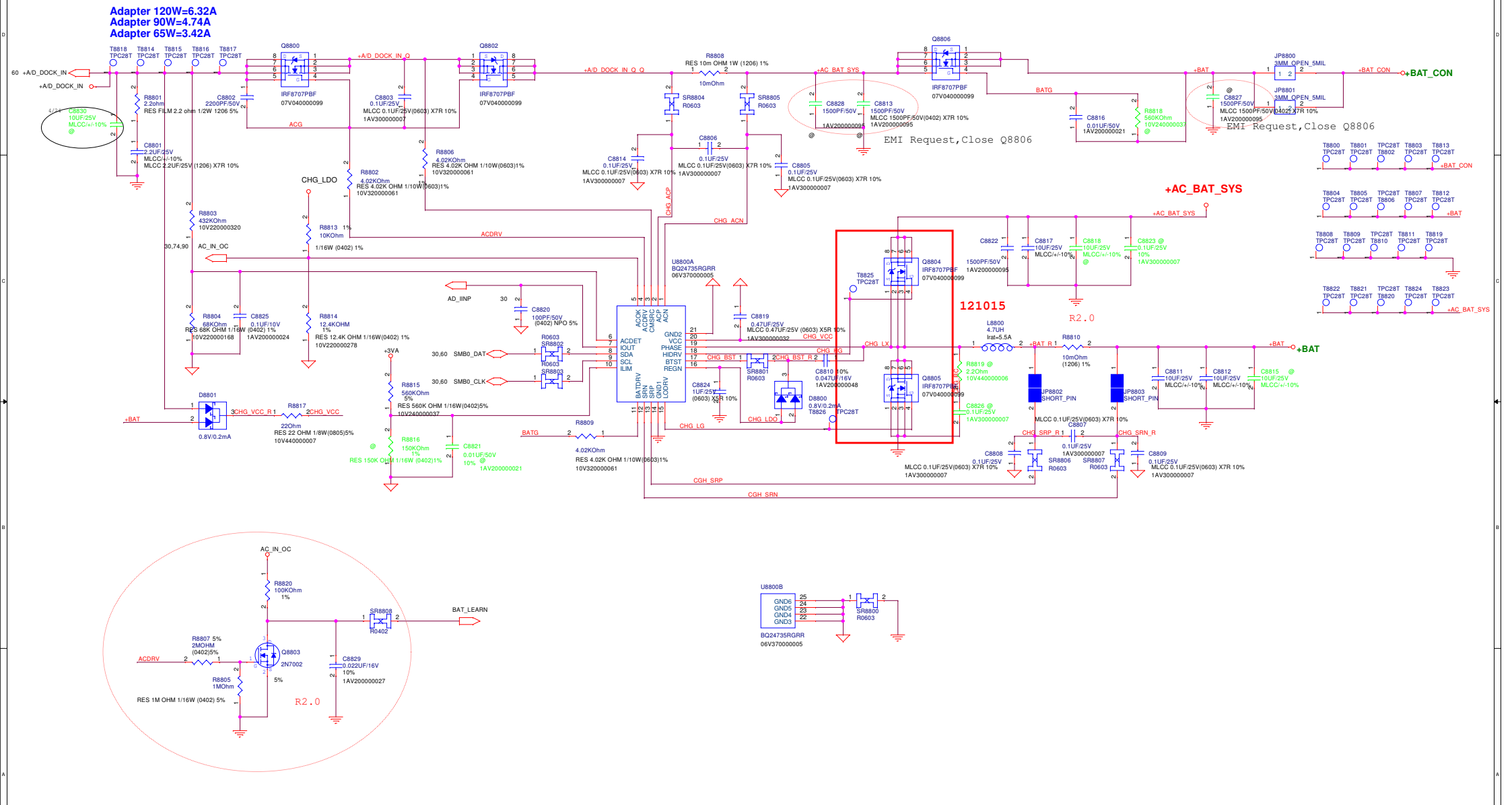
Engineer: Alex

Size	Project Name	Rev
Custom	VA70HW	1.1

Date: Friday, January 18, 2013 Sheet 87 of 99

BATTERY CHARGER

Adapter 120W=6.32A
Adapter 90W=4.74A
Adapter 65W=3.42A



<Variant Name>

PEGATRON Title : POWER_CHARGER

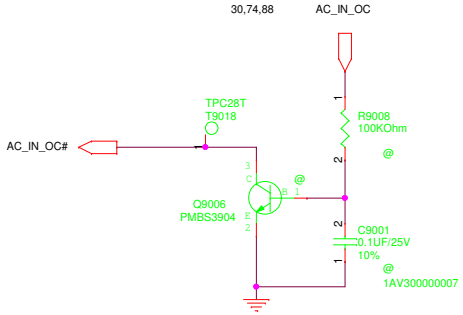
Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 88 of 15

BATTERY IN DETECT

ADAPTER IN DETECT



<Variant Name>

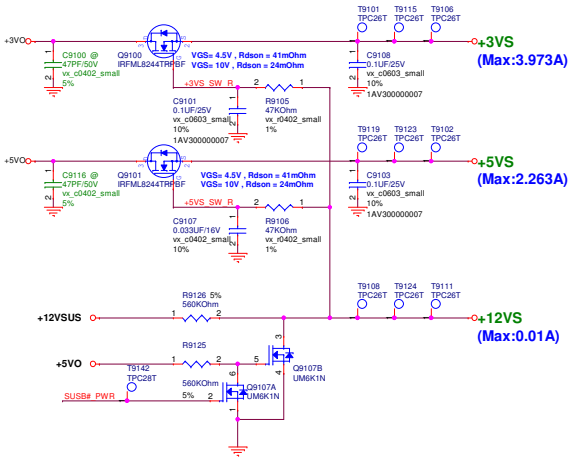
PEGATRON Title : POWER_DETECT

Engineer: Alex

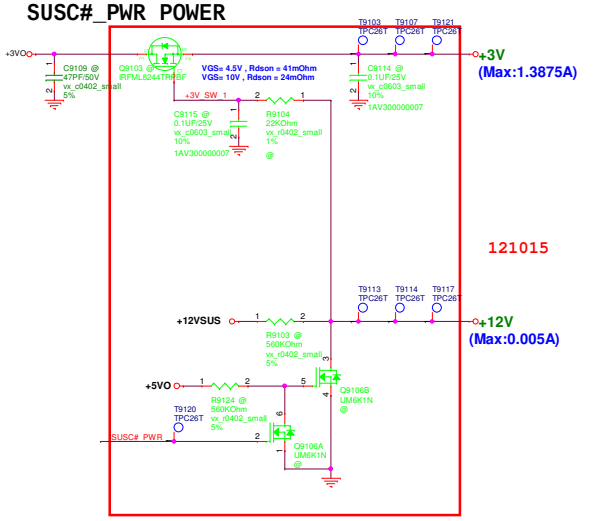
Size	Project Name	Rev
Custom	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 90 of 99

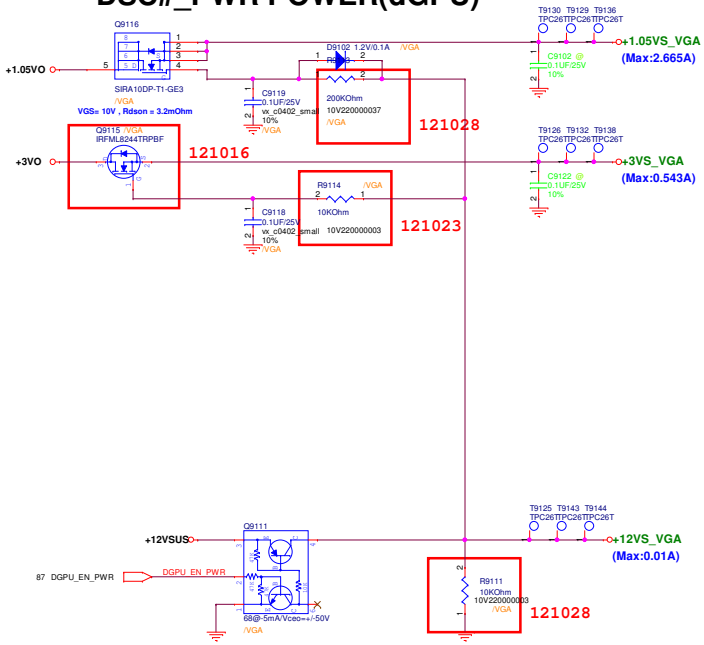
SUSB#_PWR POWER



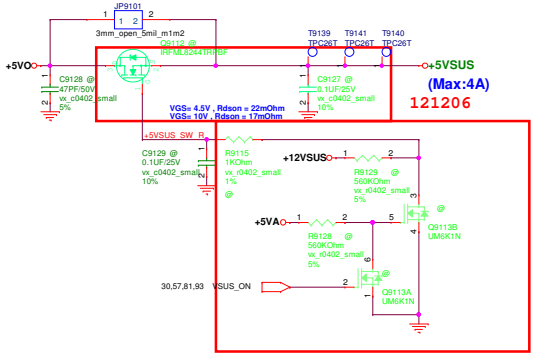
SUSC#_PWR POWER

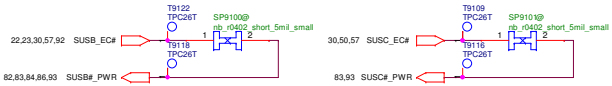


DSC#_PWR POWER(dGPU)

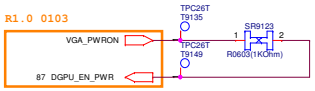


VSUS_ON POWER





DSC_VGA_PWR POWER Control



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

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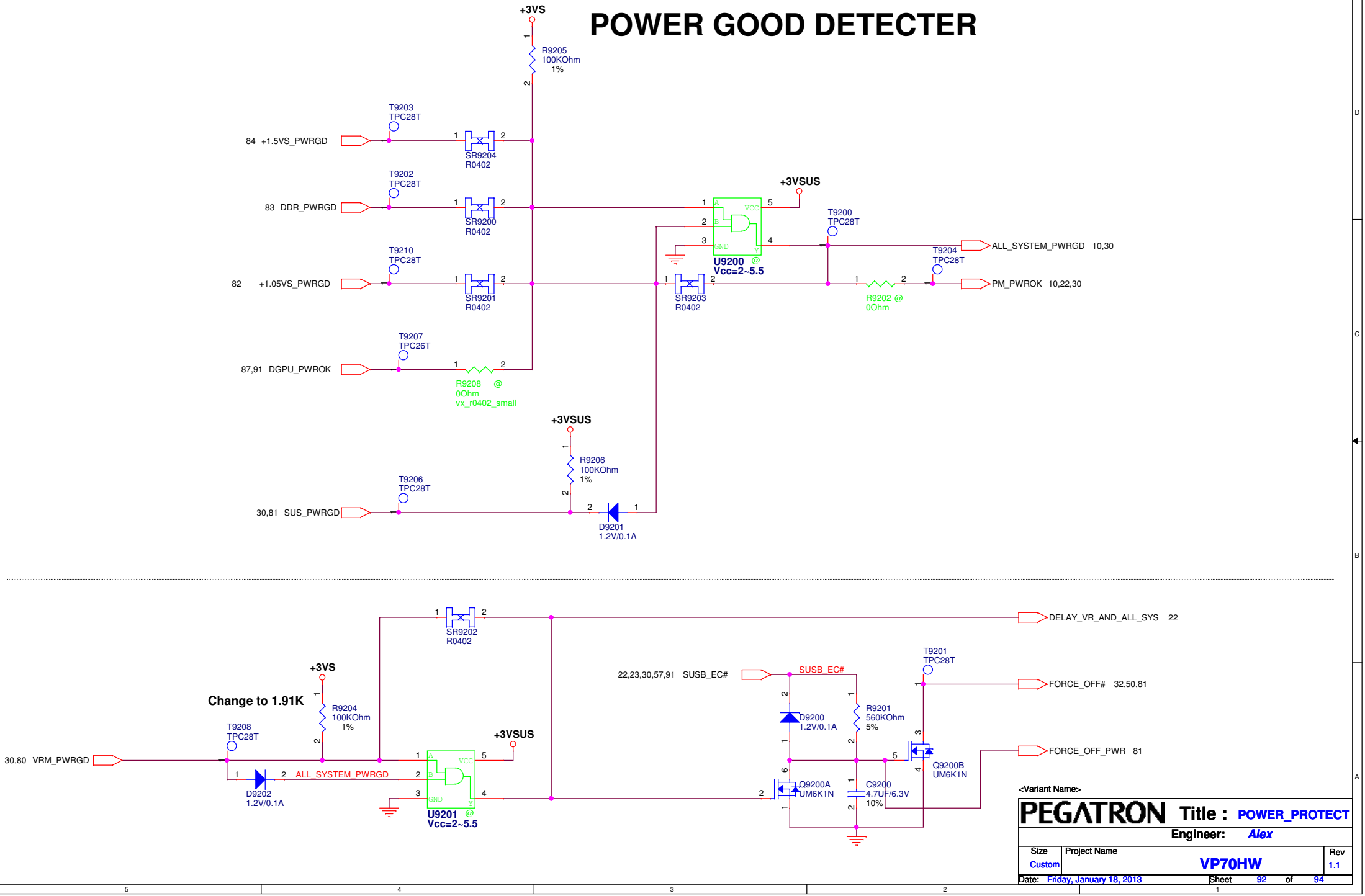
POWER GOOD DETECTER



<Variant Name>

PEGATRON Title : POWER_PROTECT

Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

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+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,86,87,88

+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 50,52,81,91

+3VA → +3VA 20,27,30,52,56,57,65,81,88

+5VO → +5VO 81,84,91

+3VO → +3VO 37,81,84,91

+1.05VS → +1.05VS 86,91

+1.05VO → +1.05VO 82,91

+12VSUS → +12VSUS 22,28,53,81,91

+5VSUS → +5VSUS 22,25,52,53,81,82,83,86,91

+3VSUS → +3VSUS 4,10,22,23,27,28,30,33,53,81,92

+12V → +12V 91

+3V → +3V 4,23,31,40,55,57,91

+12VS → +12VS 20,28,48,91

+5VS → +5VS 25,30,31,36,37,46,48,50,51,56,57,58,80,87,91

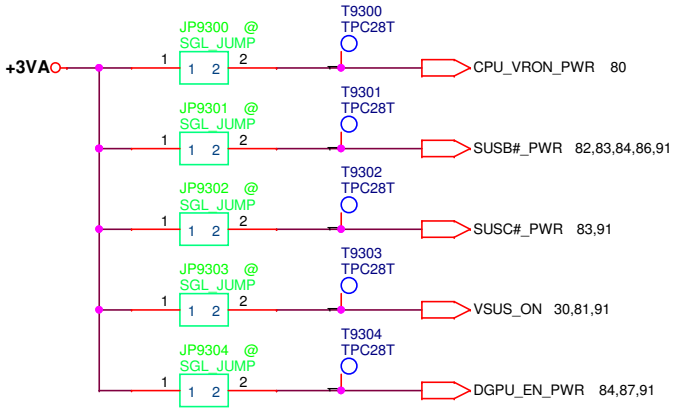
+3VS → +3VS 16,17,20,21,22,23,25,26,27,28,30,32,33,36,37,44,45,46,48,50,51,53,57,58,91,92

+1.5VS → +1.5VS 20,21,22,24,26,27,53,57,84,86,91

+1.05VS → +1.05VS 4,10,26,27,57,82,87

+VCORE → +VCORE 6,9,57,80

FOR POWER TEST



<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

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