

Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-02-16

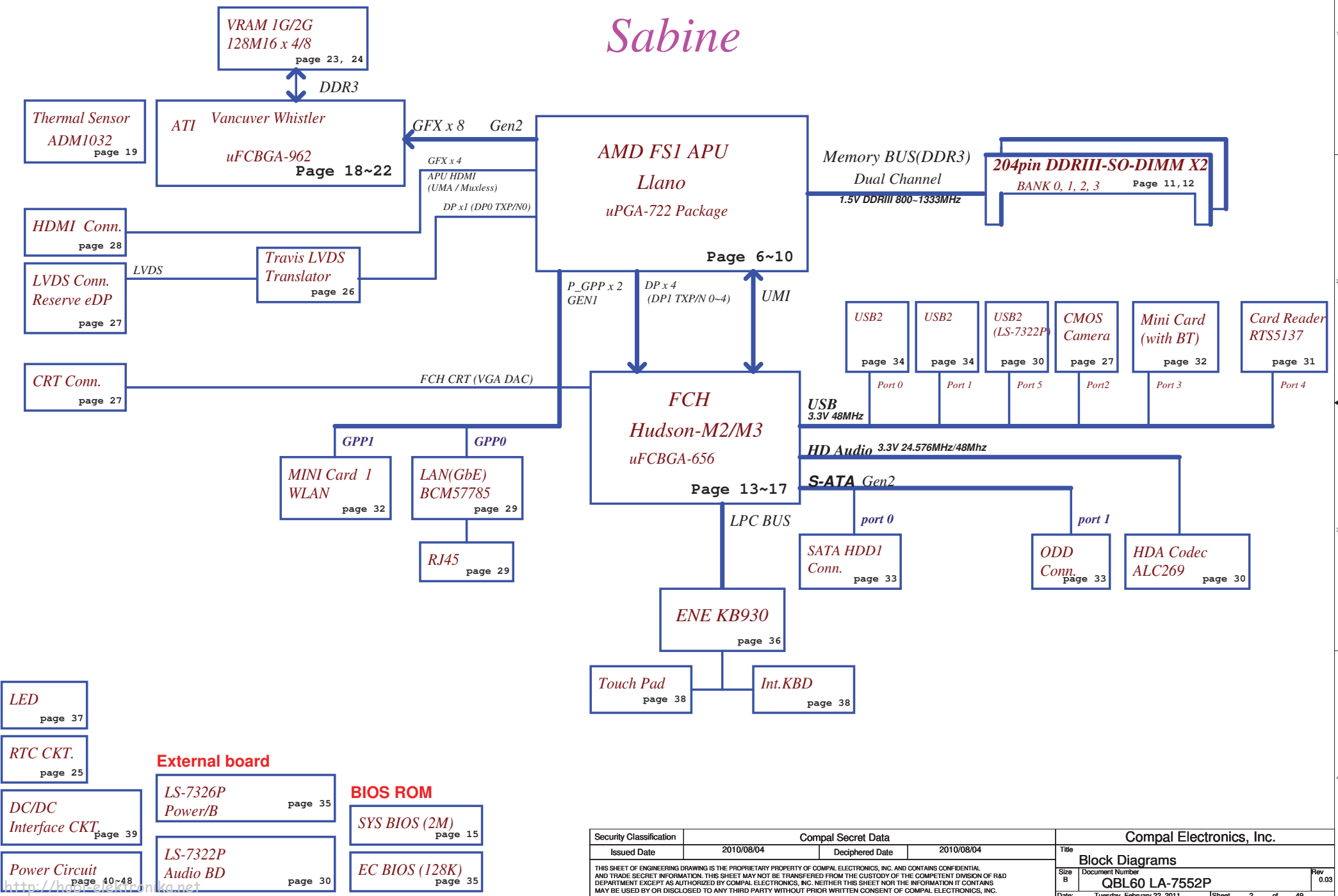
LA-7552P REV: 0.03

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Model Name : QBL60

Sabine



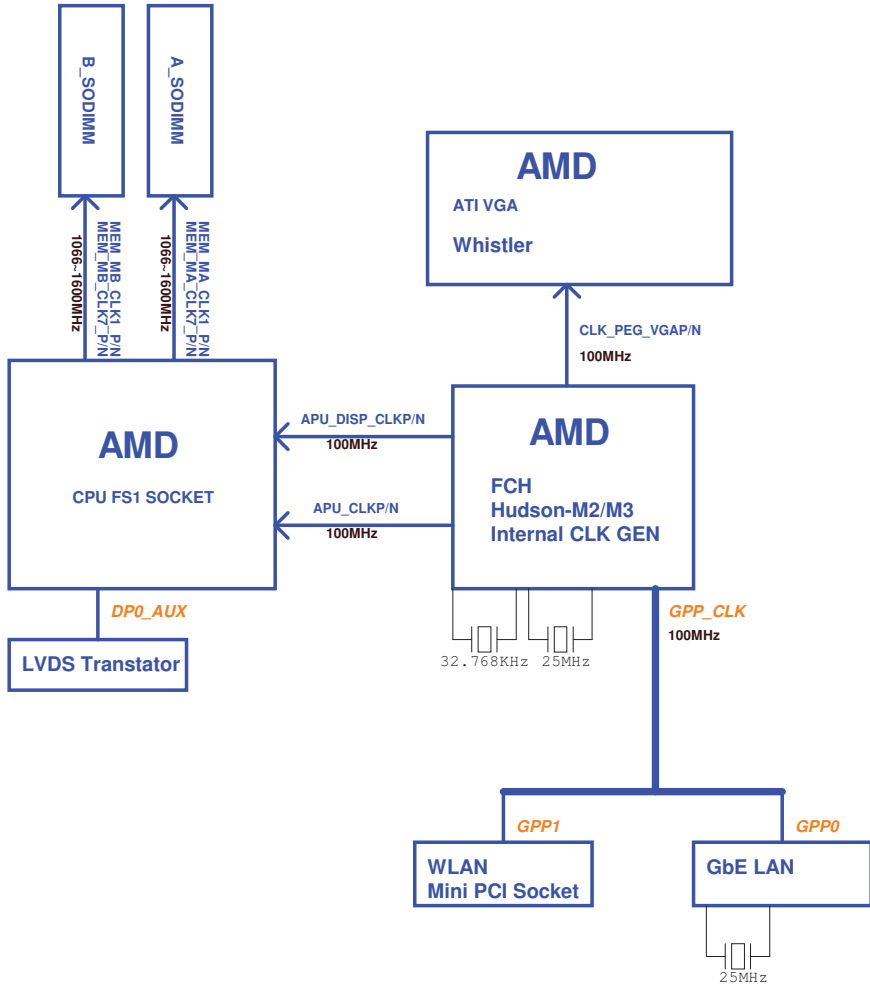
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- RTC CKT. page 25
- DC/DC Interface CKT. page 39
- Power Circuit page 40~48

- External board**
- LS-7326P Power/B page 35
 - LS-7322P Audio BD page 30

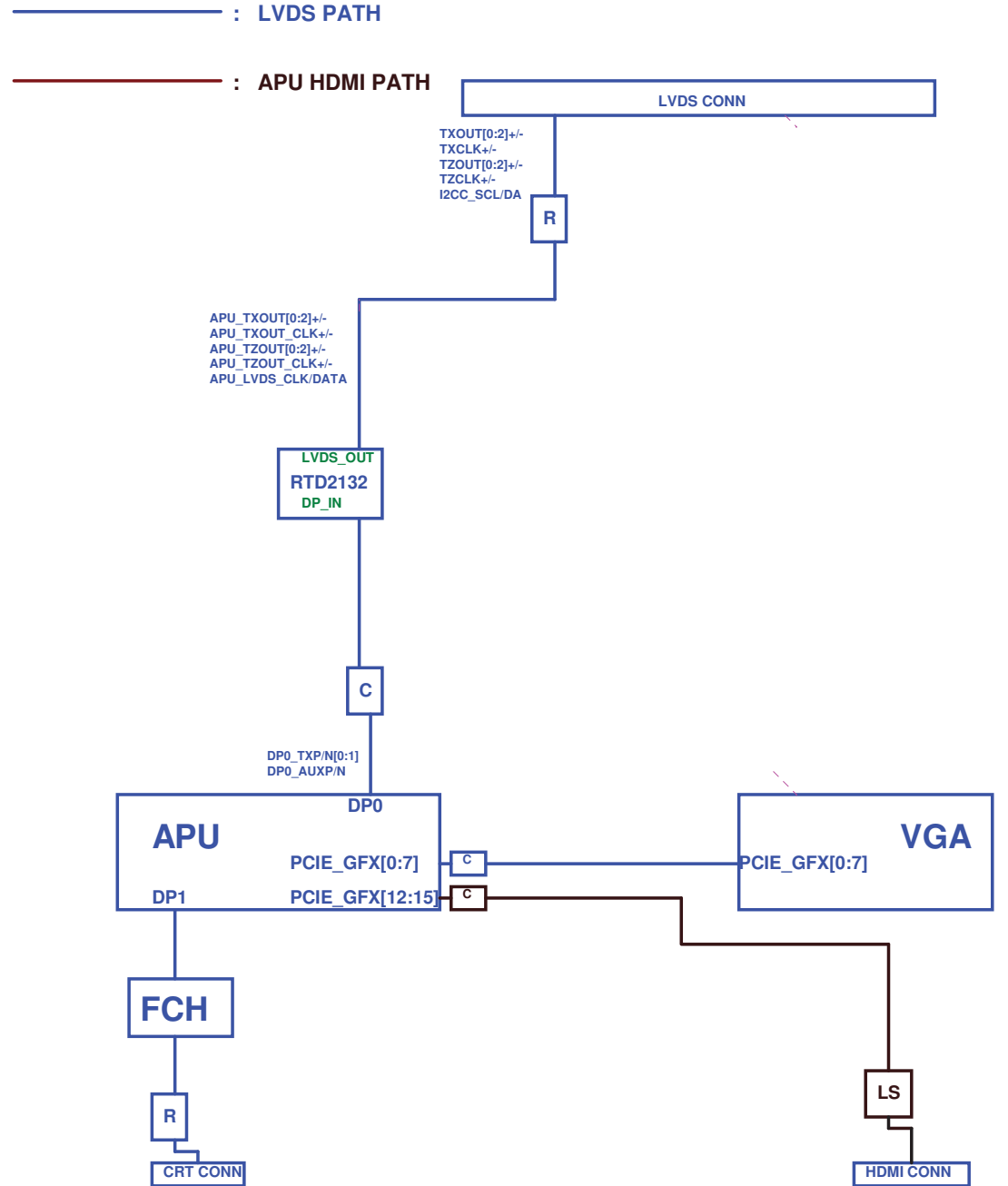
- BIOS ROM**
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 - EC BIOS (128K) page 35

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CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25



FCH M3
Part Number = SA000043190

BOM Config

x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

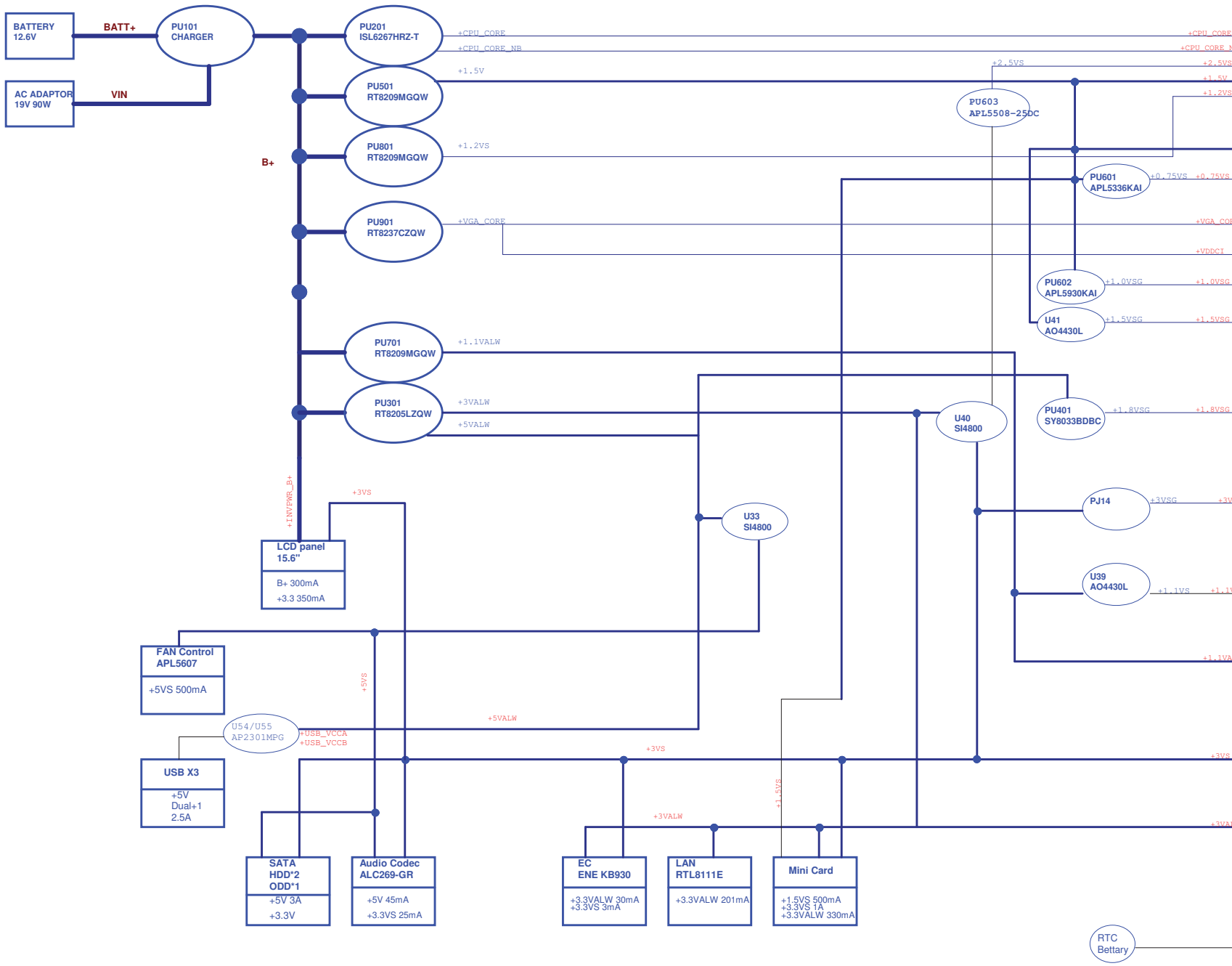
FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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AMD APU FS1	
0.7~1.475V	VDD CORE 54A
0.7~1.475V	VDDNB 27.5A
+2.5VS	VDDA 500mA
+1.5V	VDDIO 4.6A
+1.2VS	VDDR 6.7A





RAM DDRIII SODIMMx2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A





VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCI_VDDC: 2000 mA DP[A,E]_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1D1: 100 mA VDD2D1: 50 mA AZVDDC: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCI_VDDC: 40 mA MPV18: 150 mA SPV18: 75 mA PCI_VDDR: 400 mA DP[A,F]_VDD18: 920 mA DP[A,F]_PVDD: 120 mA
+3VSG	A2VDD: 130 mA VDDR3: 60 mA

VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A



FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIE: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

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18 PCIE_GTX_C_FRX_P0[0..7]  
 18 PCIE_GTX_C_FRX_N0[0..7]  

PCIE_FTX_C_GRX_P0[0..7] 18  
 PCIE_FTX_C_GRX_N0[0..7] 18  

APU To HDMI

 PCIE_FTX_GRX_P[12..15] 28
 PCIE_FTX_GRX_N[12..15] 28

JCPU1A		CONN@	
PCI EXPRESS			
PCIE_GTX_C_FRX_P0 AA8	P_GFX_RXP0	P_GFX_TXP0	AA2 PCIE_FTX_GRX_P0 C917VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0 AA9	P_GFX_RXN0	P_GFX_TXN0	AA3 PCIE_FTX_GRX_N0 C918VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1 Y7	P_GFX_RXP1	P_GFX_TXP1	Y2 PCIE_FTX_GRX_P1 C919VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1 Y8	P_GFX_RXN1	P_GFX_TXN1	Y1 PCIE_FTX_GRX_N1 C920VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2 W5	P_GFX_RXP2	P_GFX_TXP2	Y4 PCIE_FTX_GRX_P2 C921VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2 W6	P_GFX_RXN2	P_GFX_TXN2	Y5 PCIE_FTX_GRX_N2 C922VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3 W8	P_GFX_RXP3	P_GFX_TXP3	W2 PCIE_FTX_GRX_P3 C923VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3 W9	P_GFX_RXN3	P_GFX_TXN3	W3 PCIE_FTX_GRX_N3 C924VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4 V7	P_GFX_RXP4	P_GFX_TXP4	V2 PCIE_FTX_GRX_P4 C925VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4 V8	P_GFX_RXN4	P_GFX_TXN4	V1 PCIE_FTX_GRX_N4 C926VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5 U5	P_GFX_RXP5	P_GFX_TXP5	V4 PCIE_FTX_GRX_P5 C927VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5 U6	P_GFX_RXN5	P_GFX_TXN5	V5 PCIE_FTX_GRX_N5 C928VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6 U8	P_GFX_RXP6	P_GFX_TXP6	U2 PCIE_FTX_GRX_P6 C929VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P6
PCIE_GTX_C_FRX_N6 U9	P_GFX_RXN6	P_GFX_TXN6	U3 PCIE_FTX_GRX_N6 C930VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7 T7	P_GFX_RXP7	P_GFX_TXP7	T2 PCIE_FTX_GRX_P7 C931VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7 T8	P_GFX_RXN7	P_GFX_TXN7	T1 PCIE_FTX_GRX_N7 C932VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N7
X B5	P_GFX_RXP8	P_GFX_TXP8	T4 X
X B6	P_GFX_RXN8	P_GFX_TXN8	T5 X
X B8	P_GFX_RXP9	P_GFX_TXP9	B2 X
X B9	P_GFX_RXN9	P_GFX_TXN9	R3 X
X P7	P_GFX_RXP10	P_GFX_TXP10	P2 X
X P8	P_GFX_RXN10	P_GFX_TXN10	P1 X
X N5	P_GFX_RXP11	P_GFX_TXP11	P4 X
X N6	P_GFX_RXN11	P_GFX_TXN11	P5 X
N8	P_GFX_RXP12	P_GFX_TXP12	N2 PCIE_FTX_GRX_P12
N9	P_GFX_RXN12	P_GFX_TXN12	N3 PCIE_FTX_GRX_N12
M7	P_GFX_RXP13	P_GFX_TXP13	M2 PCIE_FTX_GRX_P13
M8	P_GFX_RXN13	P_GFX_TXN13	M1 PCIE_FTX_GRX_N13
L5	P_GFX_RXP14	P_GFX_TXP14	M4 PCIE_FTX_GRX_P14
L6	P_GFX_RXN14	P_GFX_TXN14	M5 PCIE_FTX_GRX_N14
L8	P_GFX_RXP15	P_GFX_TXP15	L2 PCIE_FTX_GRX_P15
L9	P_GFX_RXN15	P_GFX_TXN15	L3 PCIE_FTX_GRX_N15

For UMA Mux.

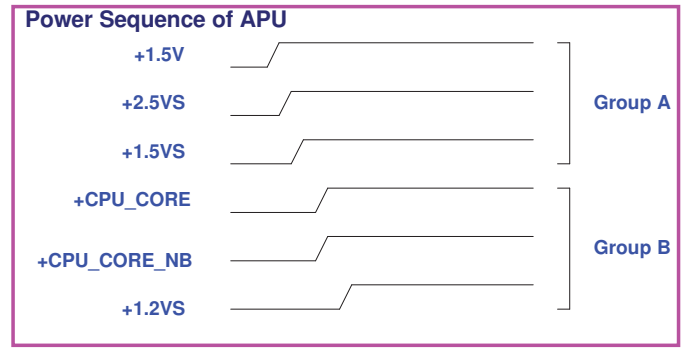
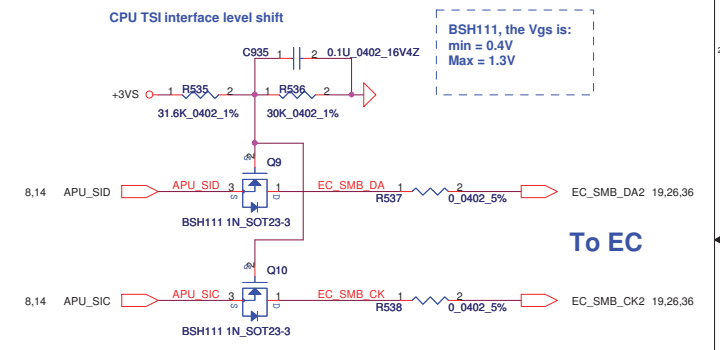
2
1
0
To HDMI
CK

29 PCIE_DTX_C_FRX_P0 AC5
 29 PCIE_DTX_C_FRX_N0 AC6
 32 PCIE_DTX_C_FRX_P1 AC8
 32 PCIE_DTX_C_FRX_N1 AC9

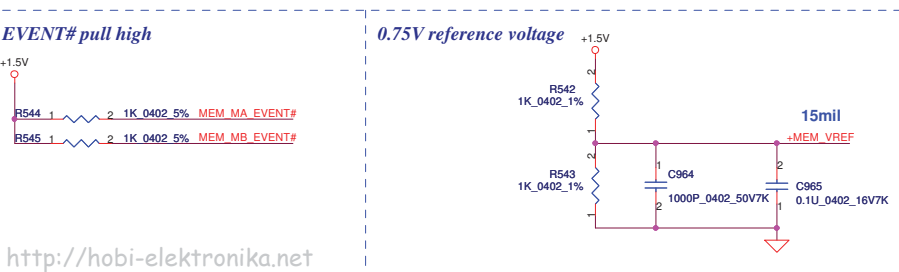
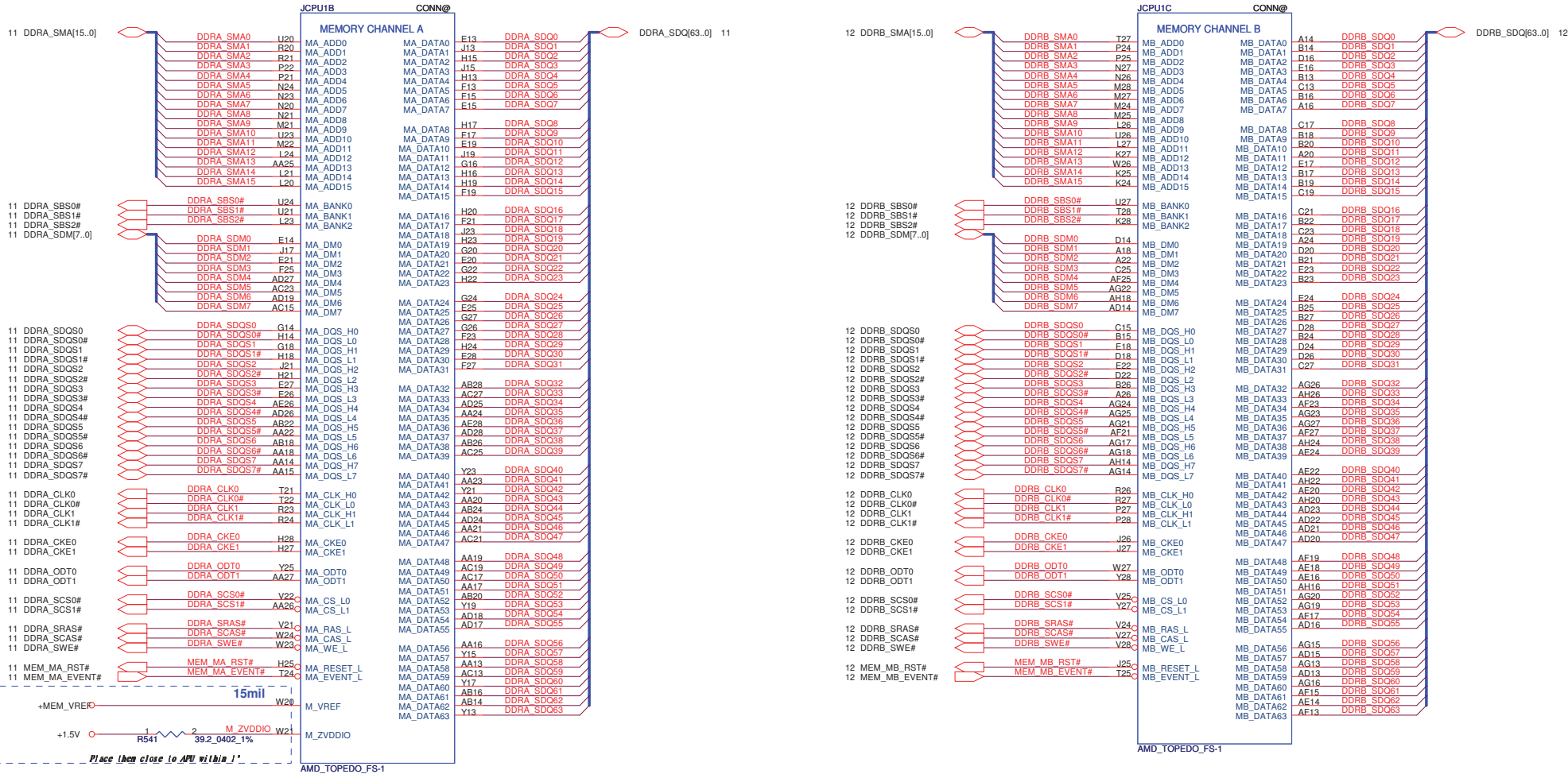
GPP		GLAN		WLAN	
P_GPP_RXP0	P_GPP_TXP0	AD4 PCIE_FTX_DRX_P0 C950 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_P0 29		
P_GPP_RXN0	P_GPP_TXN0	AD5 PCIE_FTX_DRX_N0 C951 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_N0 29		
P_GPP_RXP1	P_GPP_TXP1	AC2 PCIE_FTX_DRX_P1 C952 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_P1 32		
P_GPP_RXN1	P_GPP_TXN1	AC3 PCIE_FTX_DRX_N1 C953 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_N1 32		
X AB7	P_GPP_RXP2	AB2 X			
X AB8	P_GPP_RXN2	AB1 X			
X AA5	P_GPP_RXP3	AB4 X			
X AA6	P_GPP_RXN3	AB5 X			

13 UMI_MTX_C_FRX_P0 AF8
 13 UMI_MTX_C_FRX_N0 AF7
 13 UMI_MTX_C_FRX_P1 AE6
 13 UMI_MTX_C_FRX_N1 AE5
 13 UMI_MTX_C_FRX_P2 AE9
 13 UMI_MTX_C_FRX_N2 AE8
 13 UMI_MTX_C_FRX_P3 AD8
 13 UMI_MTX_C_FRX_N3 AD7

UMI - I-URK		UMI	
P_UMI_RXP0	P_UMI_TXP0	AF1 UMI_FTX_MRX_P0 C956 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 13
P_UMI_RXN0	P_UMI_TXN0	AF2 UMI_FTX_MRX_N0 C957 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N0 13
P_UMI_RXP1	P_UMI_TXP1	AF5 UMI_FTX_MRX_P1 C958 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P1 13
P_UMI_RXN1	P_UMI_TXN1	AF4 UMI_FTX_MRX_N1 C959 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N1 13
P_UMI_RXP2	P_UMI_TXP2	AE3 UMI_FTX_MRX_P2 C960 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P2 13
P_UMI_RXN2	P_UMI_TXN2	AE2 UMI_FTX_MRX_N2 C961 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N2 13
P_UMI_RXP3	P_UMI_TXP3	AD1 UMI_FTX_MRX_P3 C962 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P3 13
P_UMI_RXN3	P_UMI_TXN3	AD2 UMI_FTX_MRX_N3 C963 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N3 13



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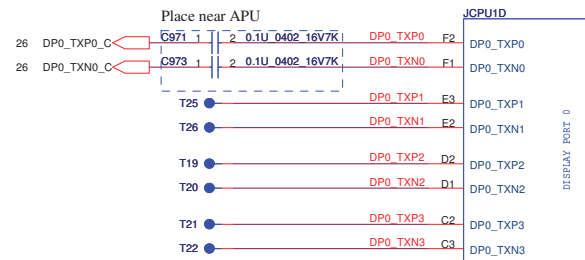


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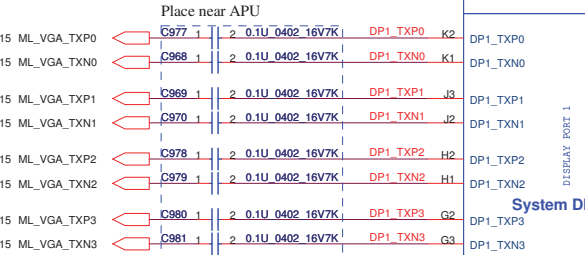
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AMD FS1 DDRIII I/F		
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To LVDS Translator



To FCH VGA ML



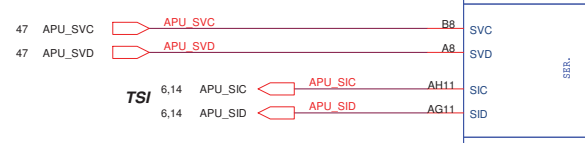
100MHz



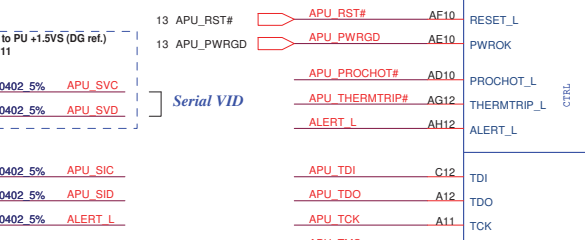
100MHz_NSS



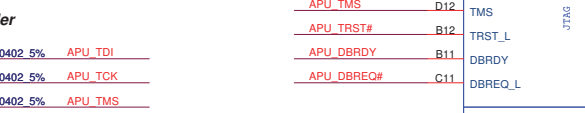
Serial VID



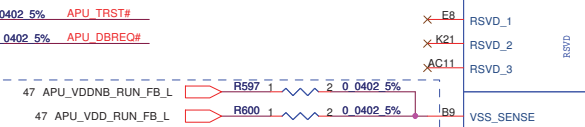
Close to Header



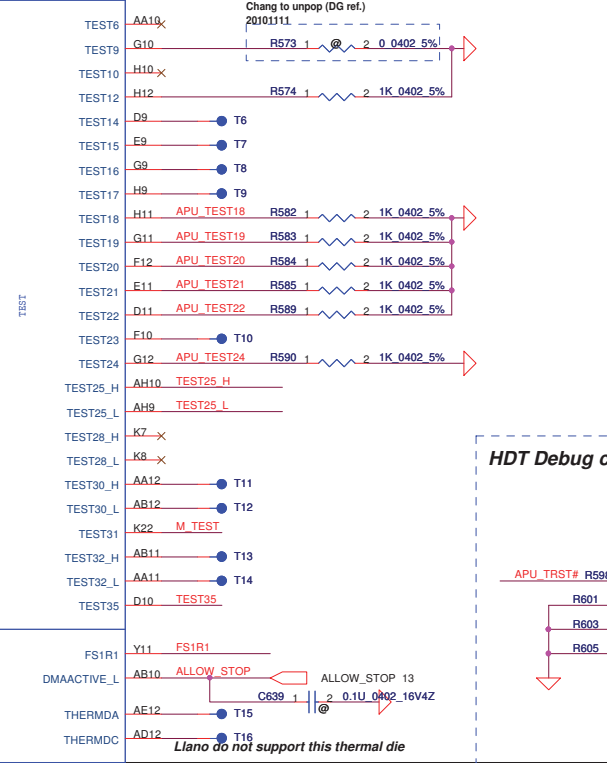
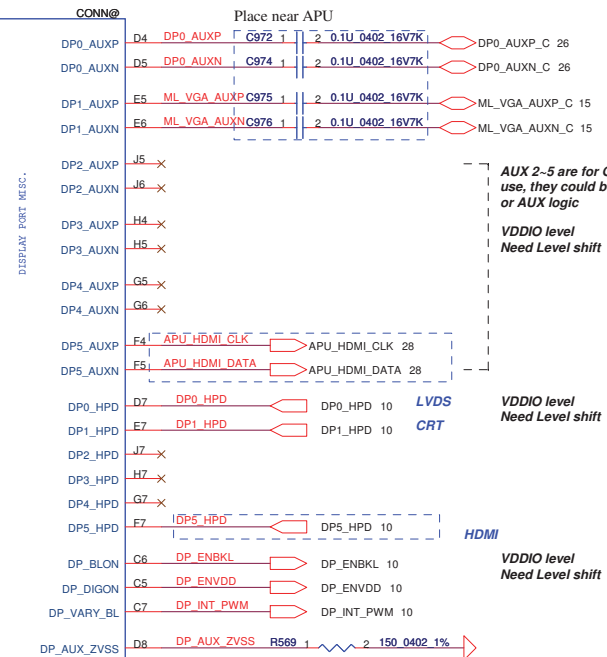
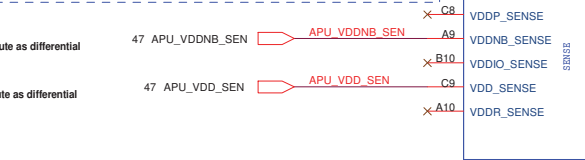
Route as differential with VSS_SENSE



Route as differential



AMD_TOPEDO_FS-1



To LVDS Translator

To FCH

AUX 2-5 are for GFX interface use, they could be selected to I2C or AUX logic

VDDIO level Need Level shift

VDDIO level Need Level shift

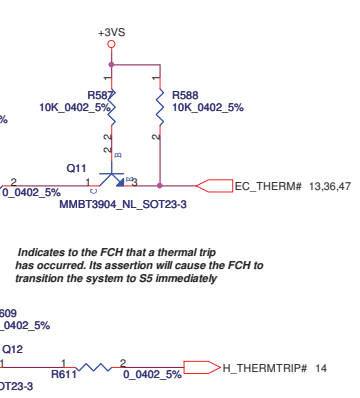
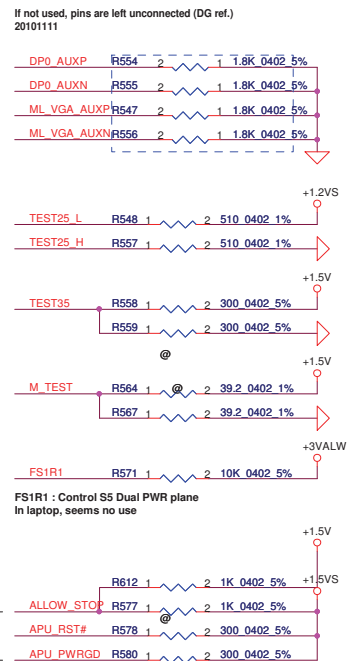
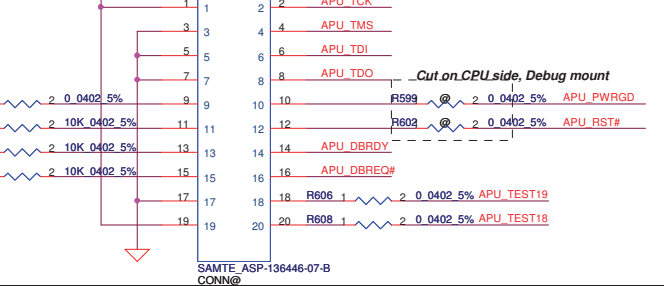
HDMI

VDDIO level Need Level shift

Asserted as an input to force the processor into the HTC-active state

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

HDT Debug conn

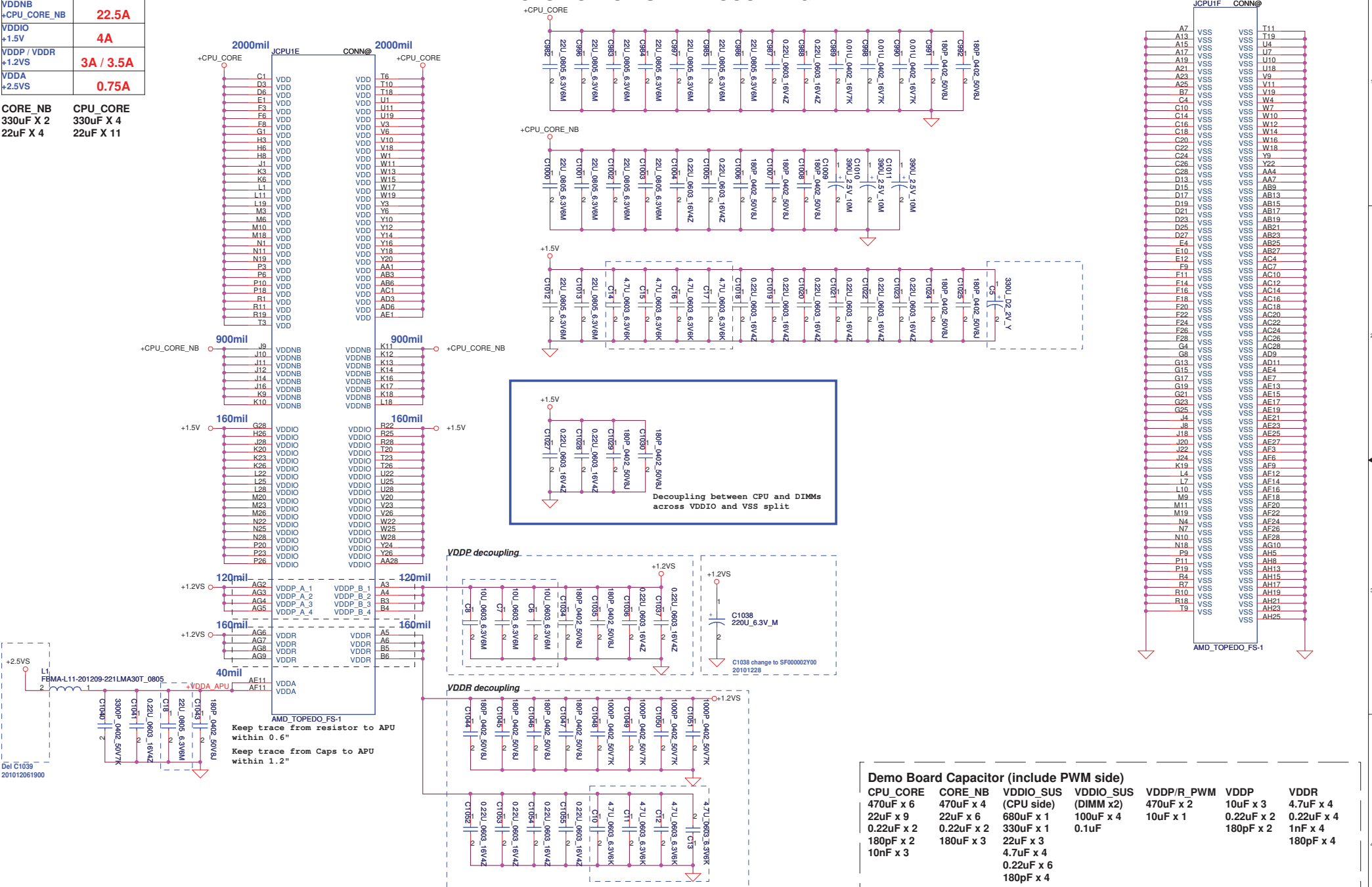


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Issued Date	2010/08/04	Deciphered Date	2010/08/04	AMD FS1 Display / MISC / HDT	
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Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB CPU_CORE
330uF X 2 330uF X 4
22uF X 4 22uF X 11

CPU BOTTOM SIDE DECOUPLING



Demo Board Capacitor (include PWM side)						
CPU_CORE	CORE_NB	VDDIO_SUS	VDDIO_SUS	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	(CPU side)	(DIMM x2)	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	680uF x 1	100uF x 4	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	330uF x 1	0.1uF		180pF x 2	1nF x 4
180pF x 2	180uF x 3	22uF x 3				180pF x 4
10nF x 3		4.7uF x 4				
		0.22uF x 6				
		180pF x 4				

Security Classification	Compal Secret Data		Title	
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Date			Sheet	of
			9	49

HPD

Translator HPD

From Translator



CRT HPD

From FCH

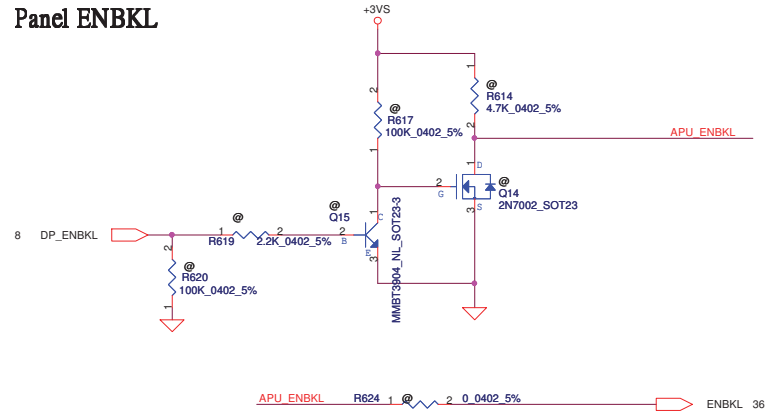


HDMI HPD

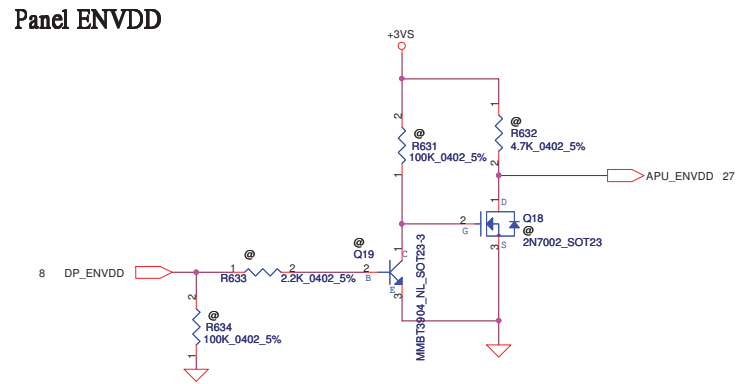
From HDMI Conn



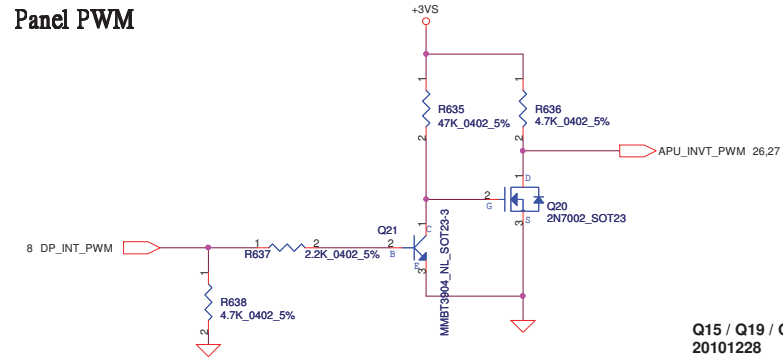
Panel ENBKL



Panel ENVDD

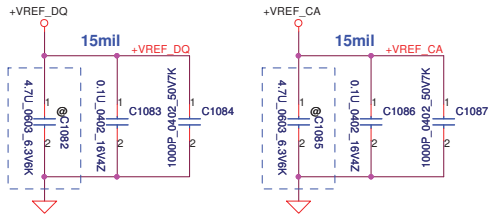
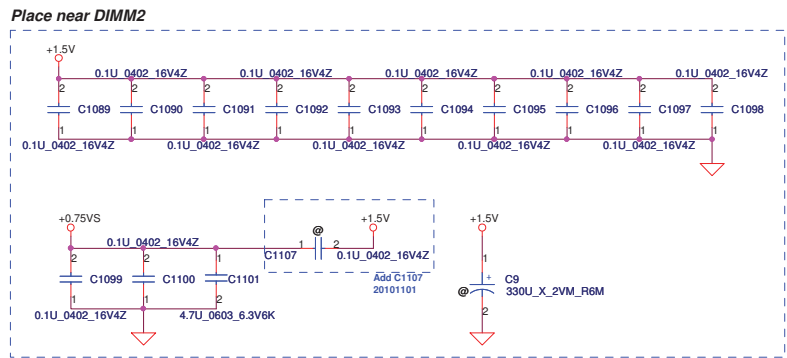
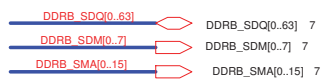
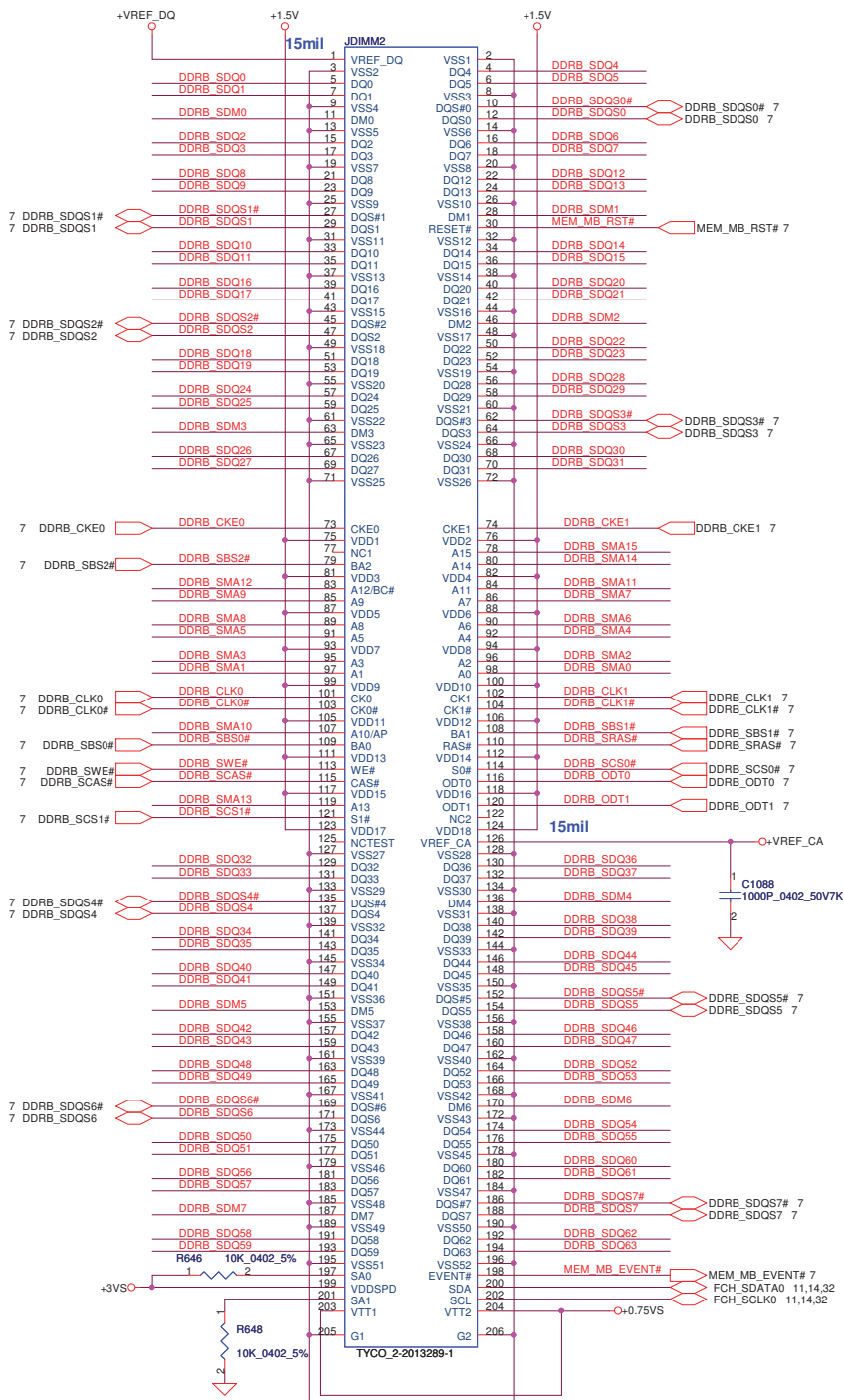


Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

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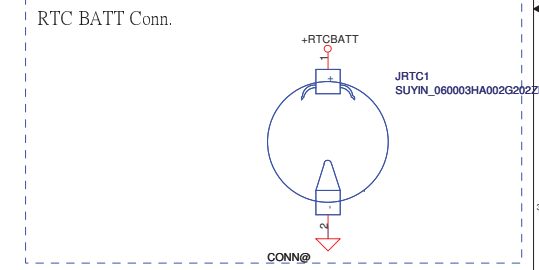
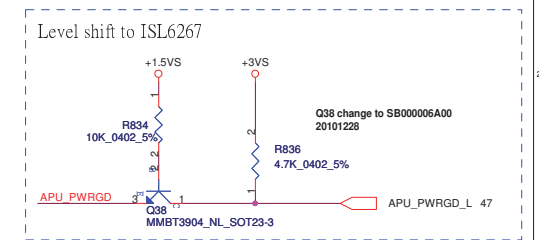
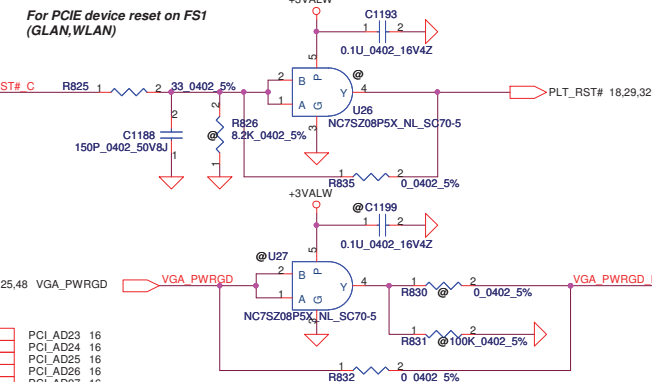
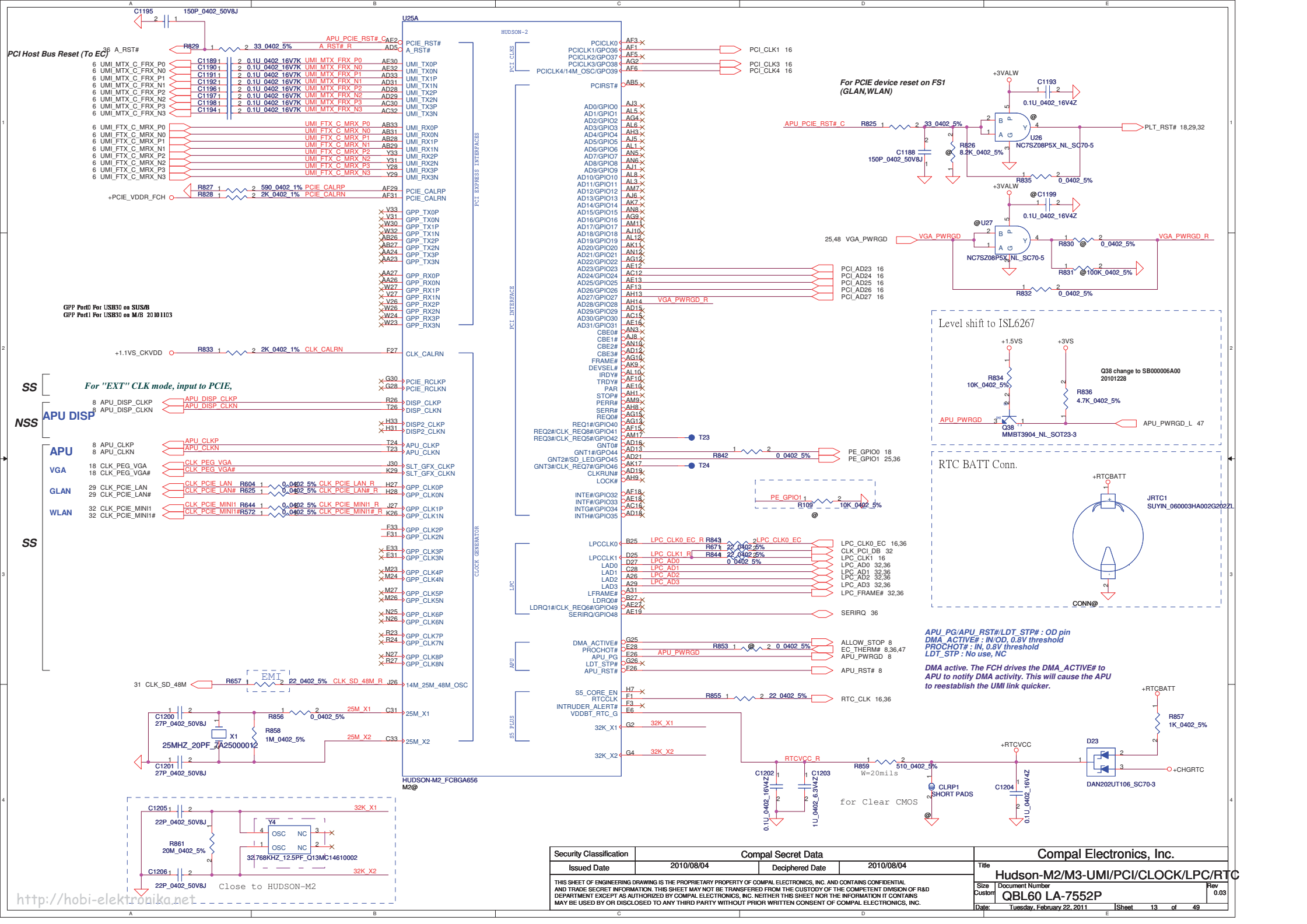
DIMM_B STD H:5.2mm
 <Address: 01>

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Title			
DDRIII SO-DIMM 2			
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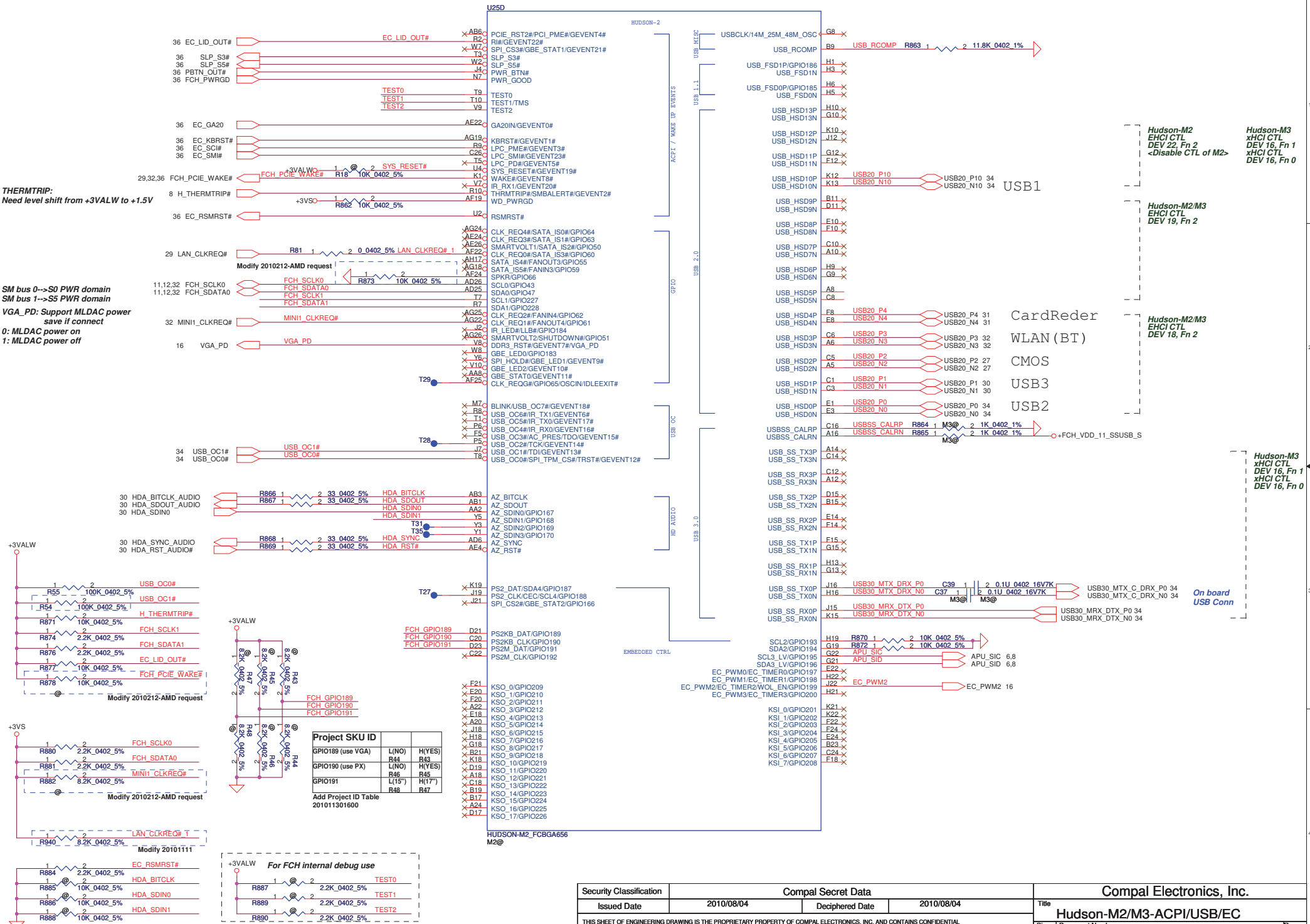


APU_PG/APU_RST#/LDT_STP# : OD pin
 DMA_ACTIVE# : IN/OD, 0.8V threshold
 PROCHOT# : IN, 0.8V threshold
 LDT_STP# : No use, NC

DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

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				Date	Tuesday, February 22, 2011	Sheet	13 of 49

PCIE_RST2 : Reset PCIE device on Hudson2



THERMTRIP:
Need level shift from +3VALW to +1.5V

SM bus 0->S0 PWR domain
SM bus 1->S5 PWR domain

VGA_PD: Support MLDAC power
save if connect

0: MLDAC power on
1: MLDAC power off

+3VALW

+3VS

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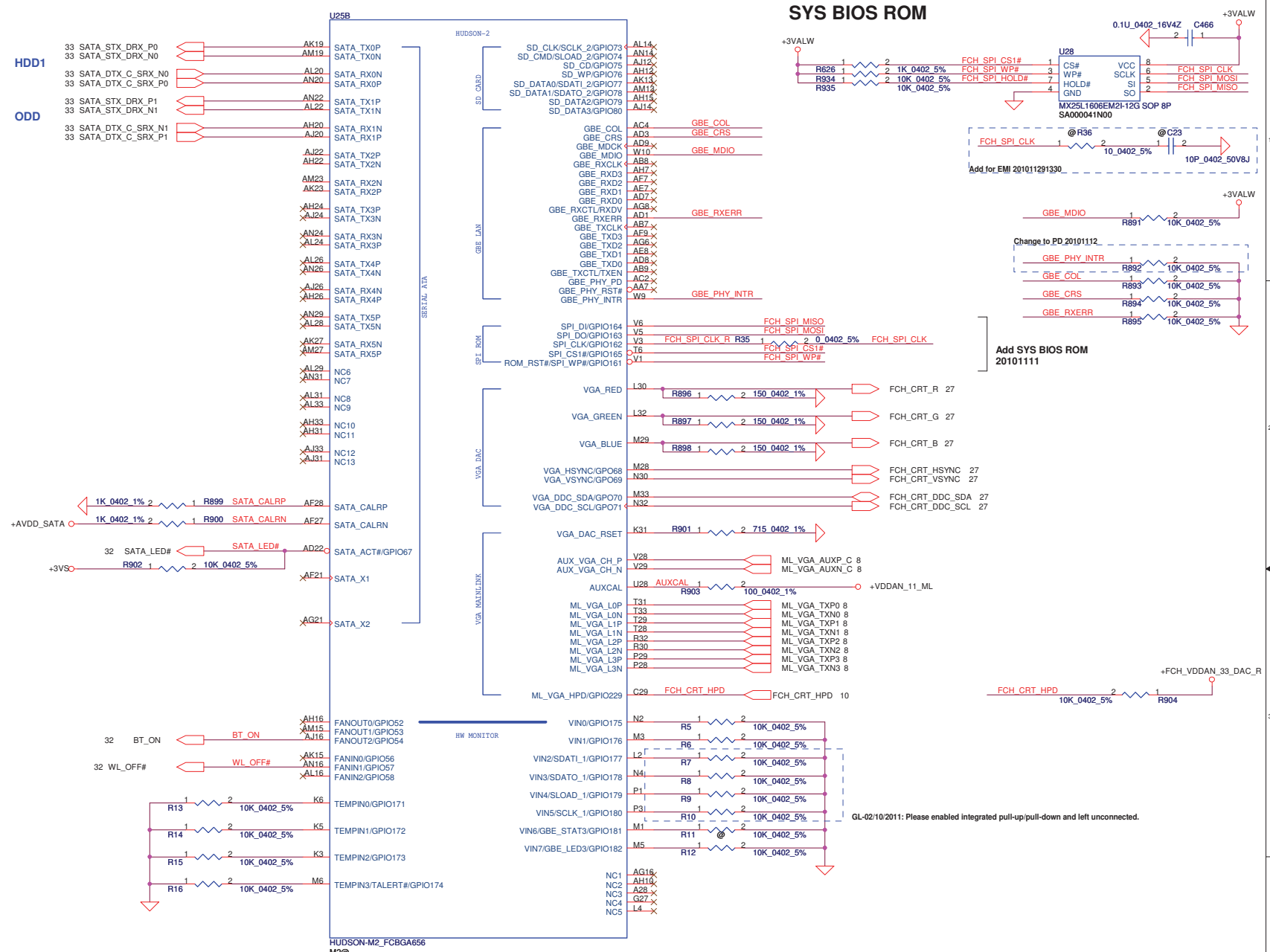
Project SKU ID	LNO	R4	H(Y)ES
GPIO189 (use VGA)	R44	R45	(YES)
GPIO190 (use PX)	R46	R45	(YES)
GPIO191	R48	R47	(YES)

Add Project ID Table
201011301600

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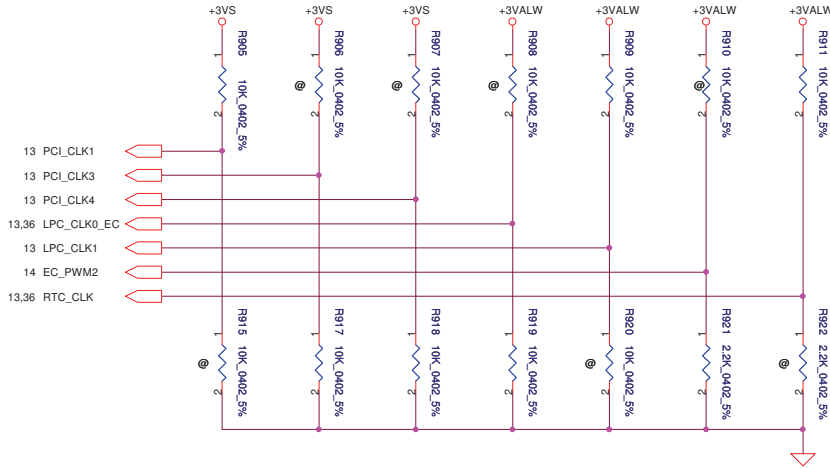
Compal Electronics, Inc.		
Title Hudson-M2/M3-ACPI/USB/EC		
Size Custom	Document Number QBL60 LA-7552P	Rev 0.03
Date: Tuesday, February 22, 2011	Sheet 14	of 49



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Size	Document Number	Rev	QBL60 LA-7552P Date: Tuesday, February 22, 2011 Sheet 15 of 49		

STRAP PINS

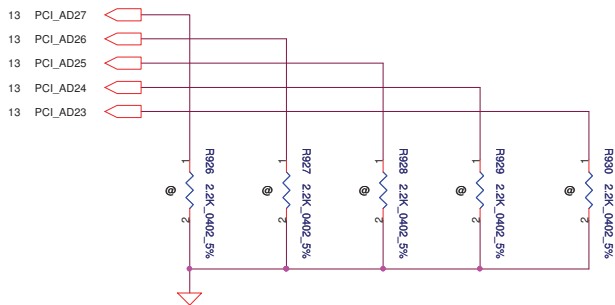
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



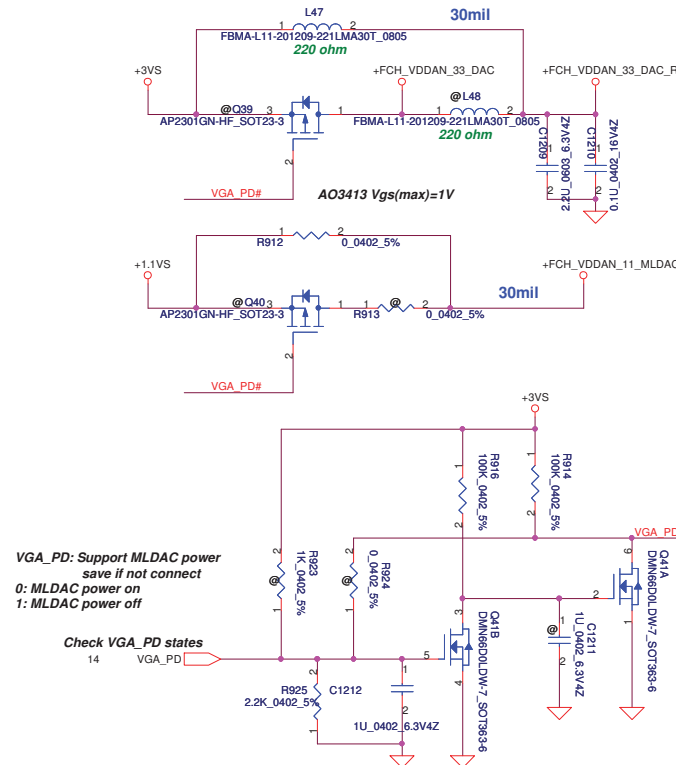
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23	
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

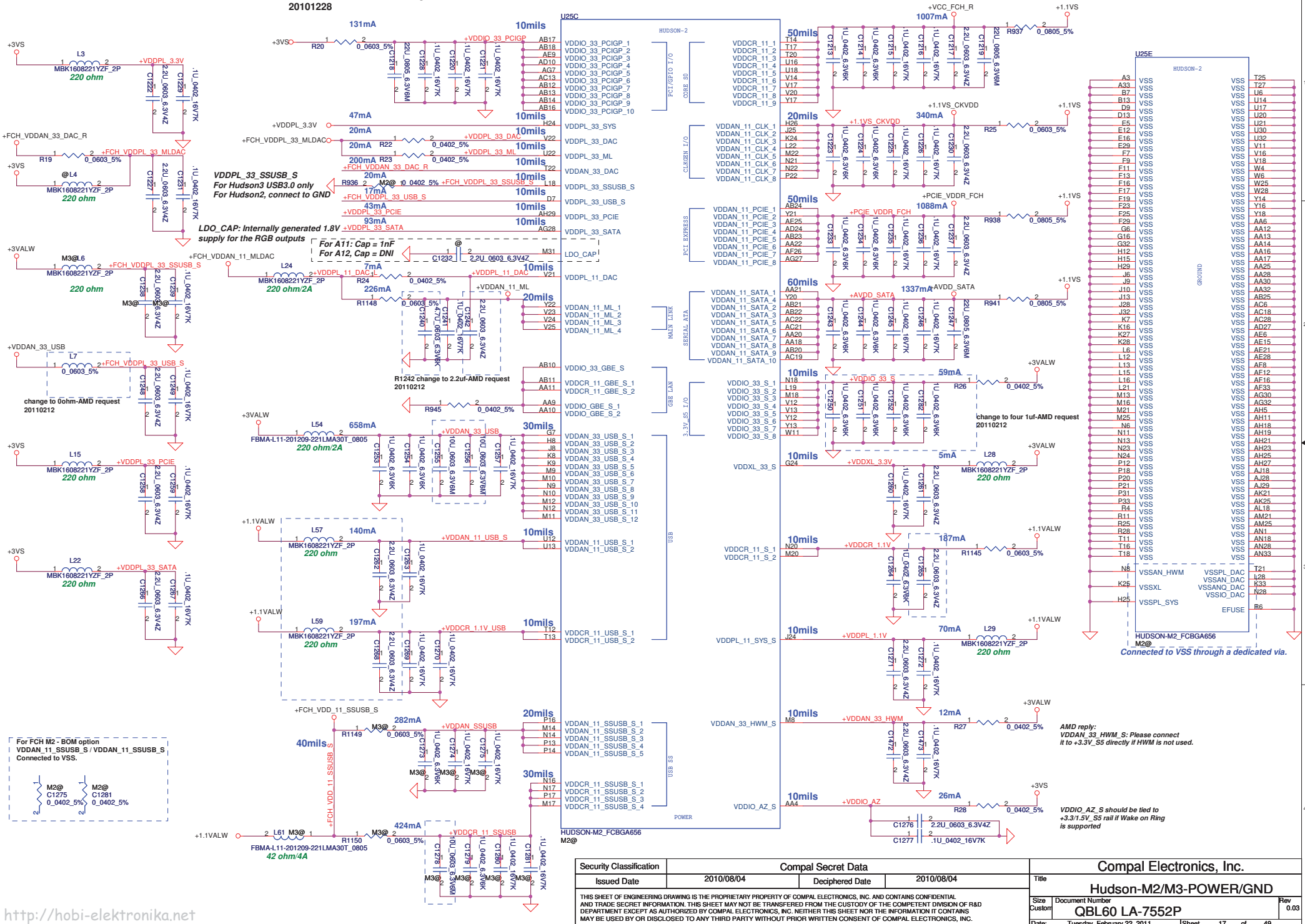


If support ML DAC power down when no VGA plug



C1218 / C1219 / C1247 Change to SE00000110

20101228

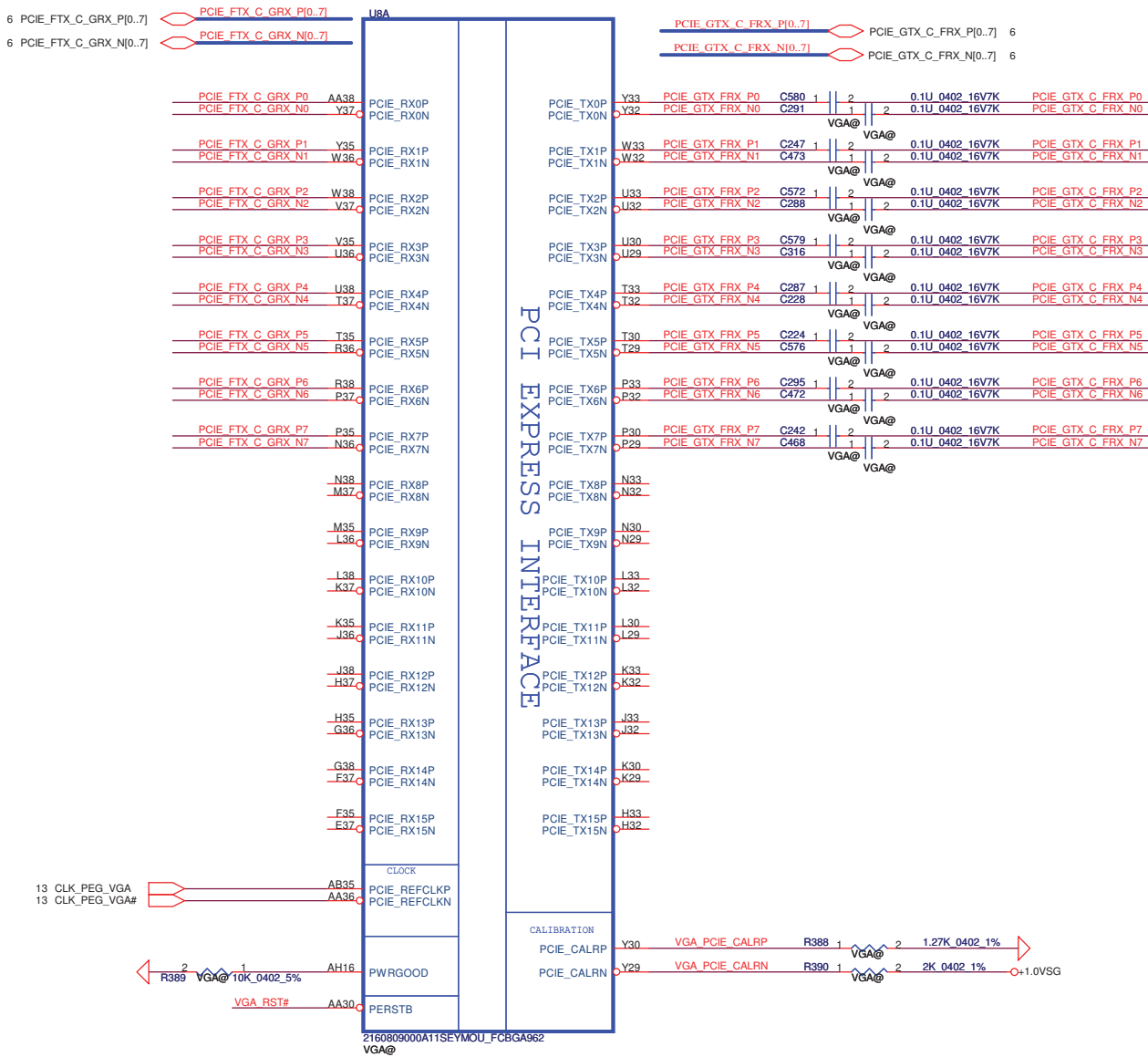


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Compal Electronics, Inc.		
Hudson-M2/M3-POWER/GND		
Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03
Date:	Tuesday, February 22, 2011	Sheet 17 of 49

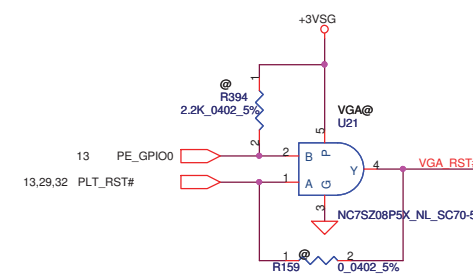
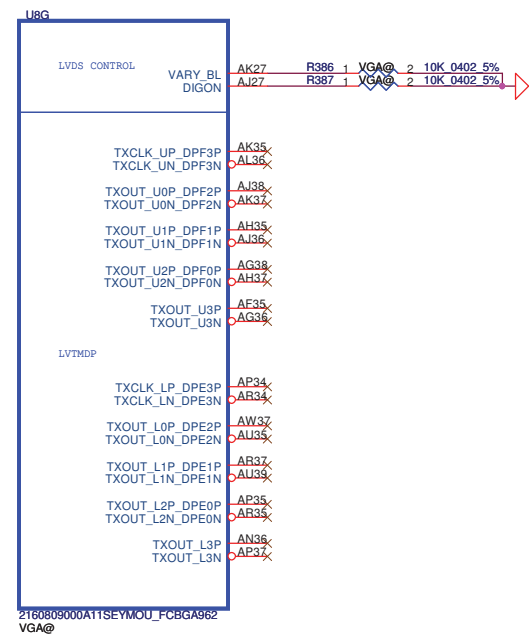
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GFX PCIE LANE REVERSAL



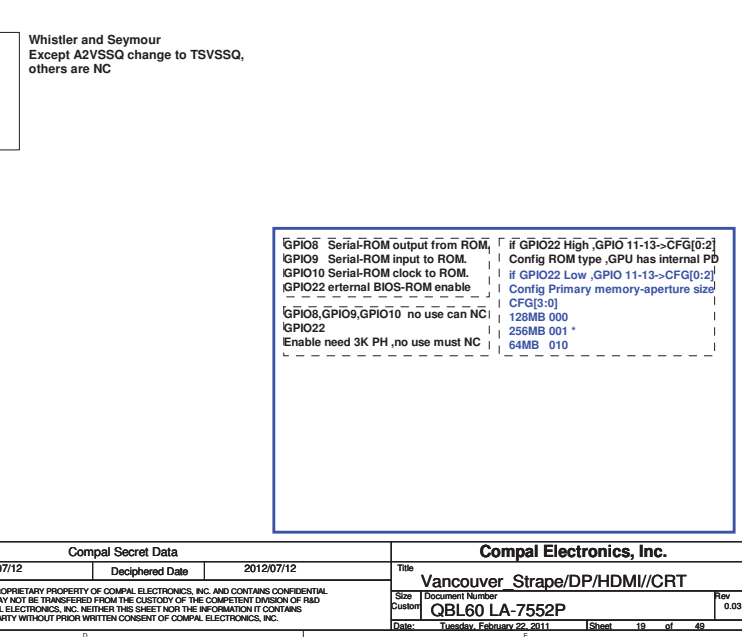
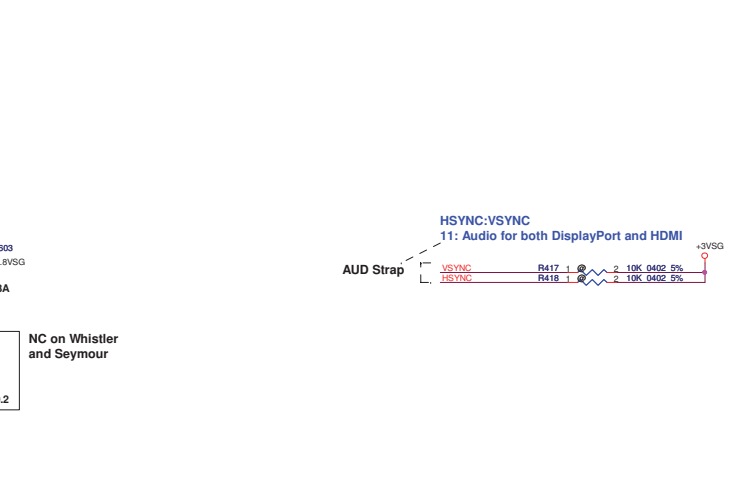
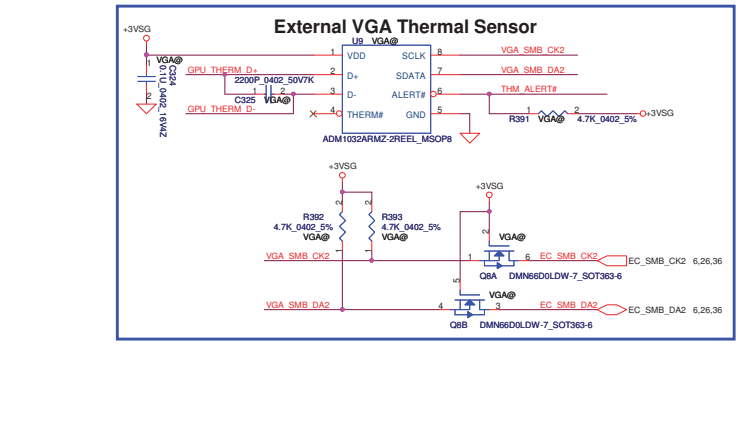
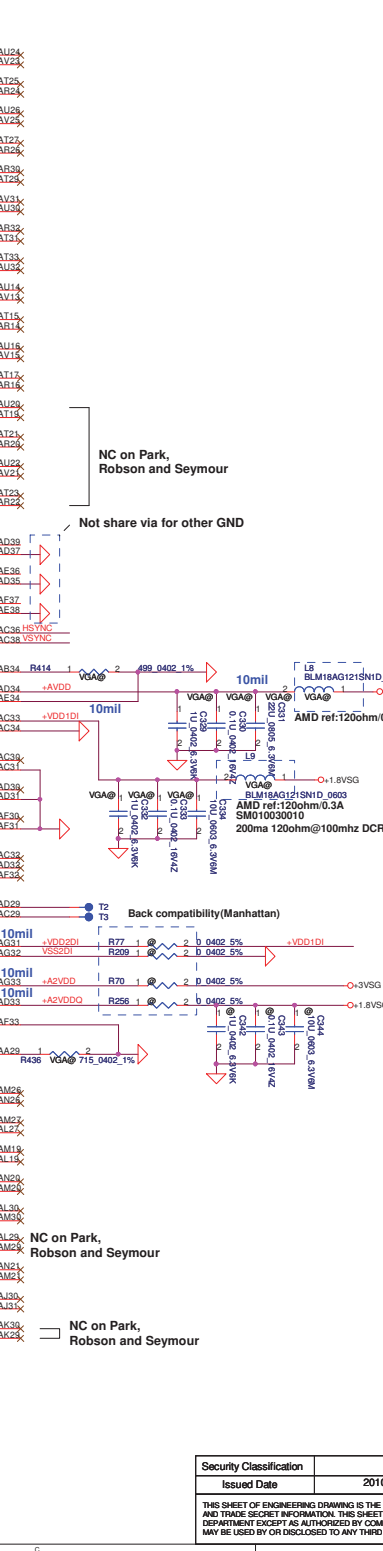
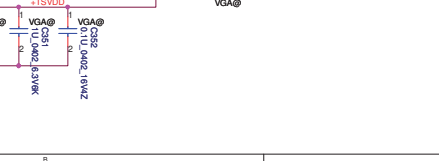
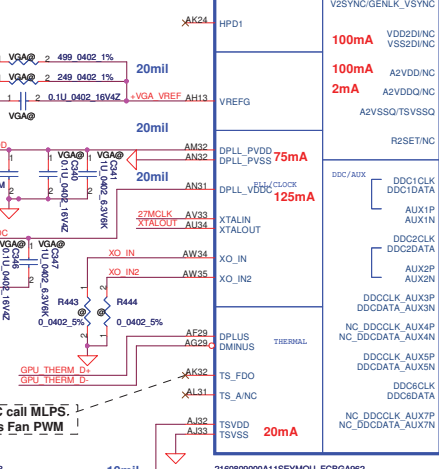
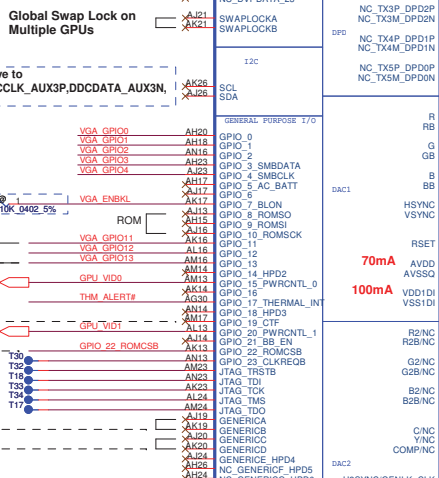
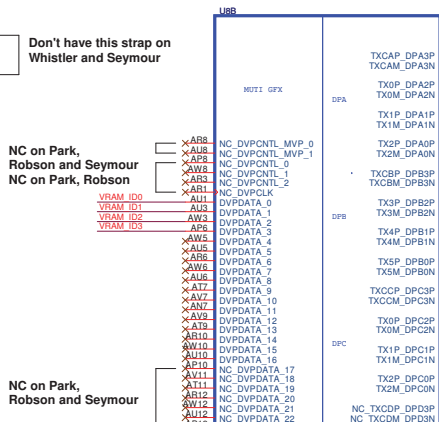
<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need

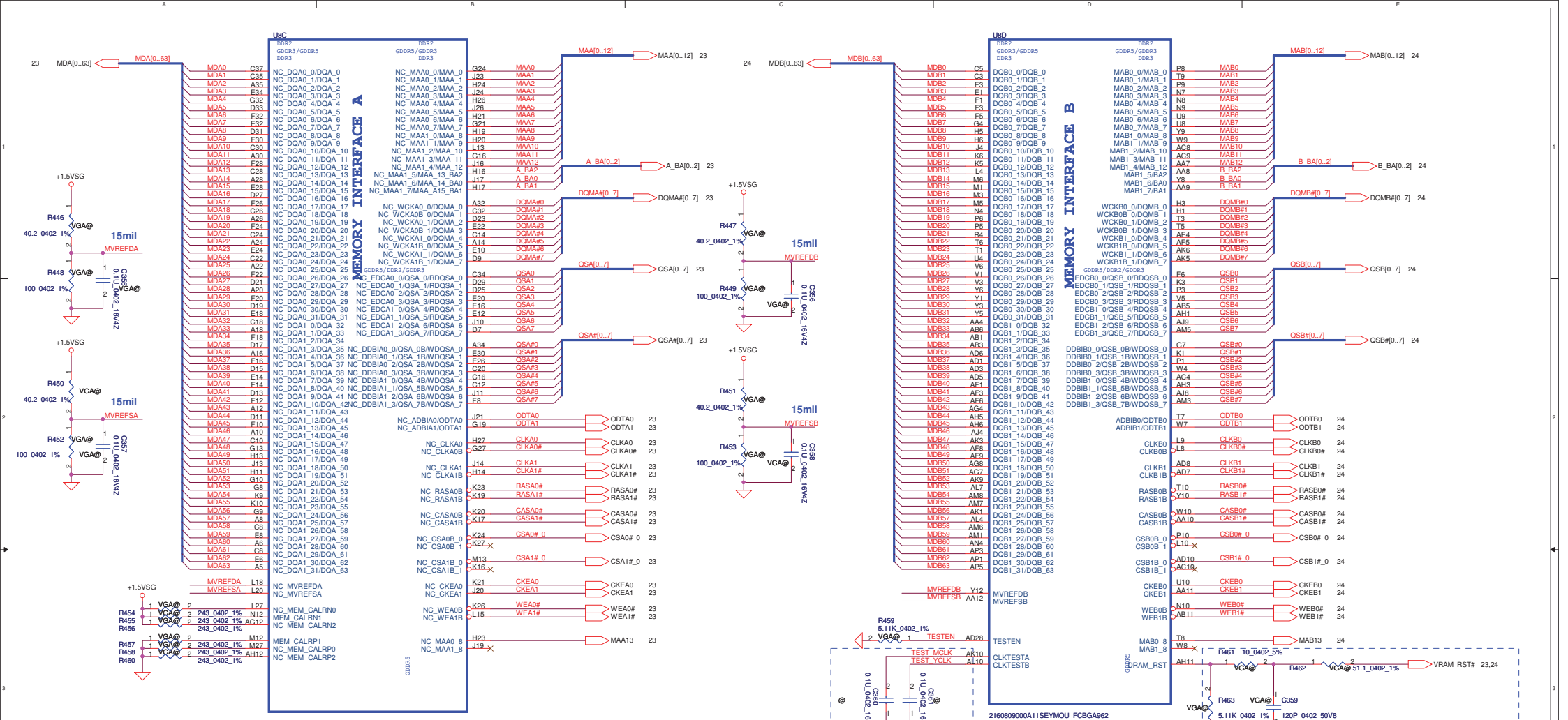


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Size Custom	Document Number			Rev	
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Strap Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 010	001
CONFIG[1]		
CONFIG[0]		
BIOS_ROM_EN	Enable external BIOS ROM device (Internal PD) 0: Disable, 1: Enable	0
AUD[1]	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
AUD[0]		
BIF_GEN2_EN	0: Advertises the PCIe device as 2.5 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

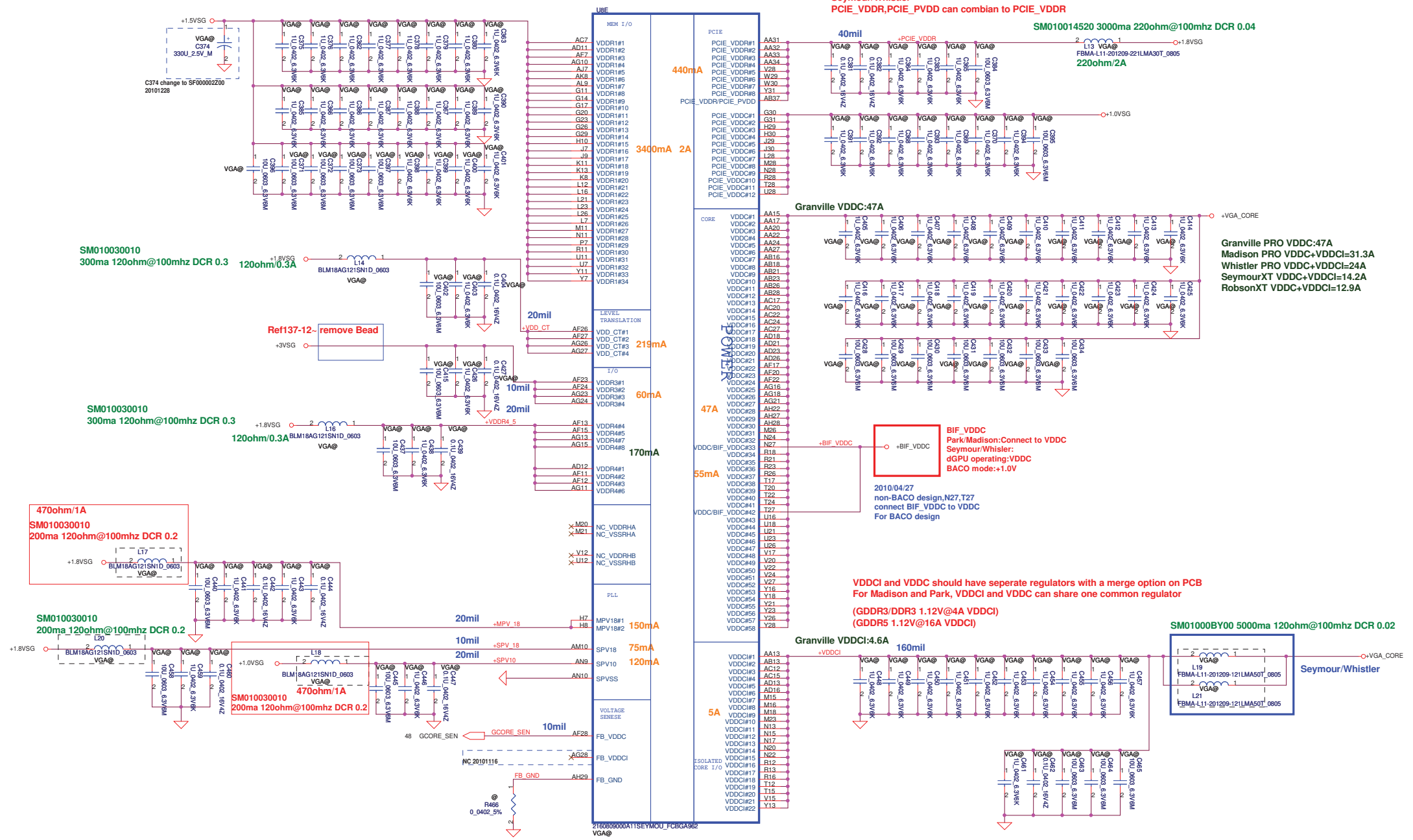


GPIO8 Serial-ROM output from ROM. If GPIO22 High, GPIO 11-13 -> CFG[0:2] Config ROM type, GPU has internal PD
 GPIO10 Serial-ROM input to ROM. If GPIO22 Low, GPIO 11-13 -> CFG[0:2] Config Primary memory-aperture size
 GPIO19 Serial-ROM clock to ROM.
 GPIO22 external BIOS-ROM enable. Config CFG[3:0] 128MB 000 256MB 001 * 64MB 010
 GPIO8, GPIO9, GPIO10 no use can NC
 GPIO22 Enable need 3K PH, no use must NC

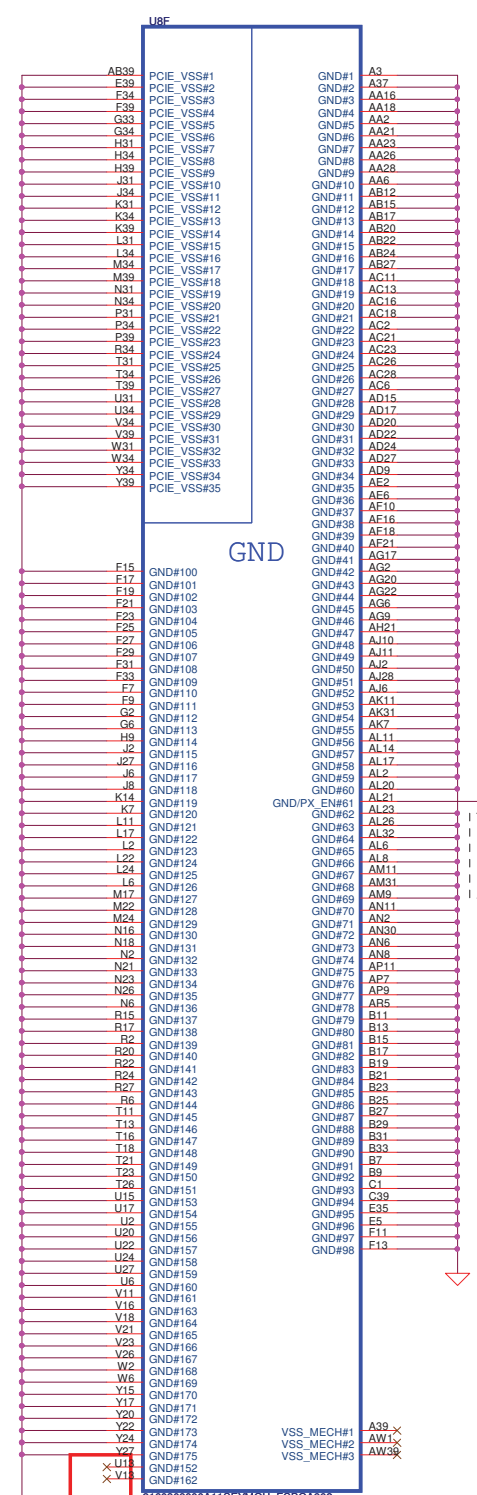


Note:
route 50ohms single-ended
and 100ohms diff
and keep short
REF137-03 suggest

Park&Seymour is single channel for memory (channel B only)



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Date:	Tuesday, February 22, 2011	Sheet	21	of	49		

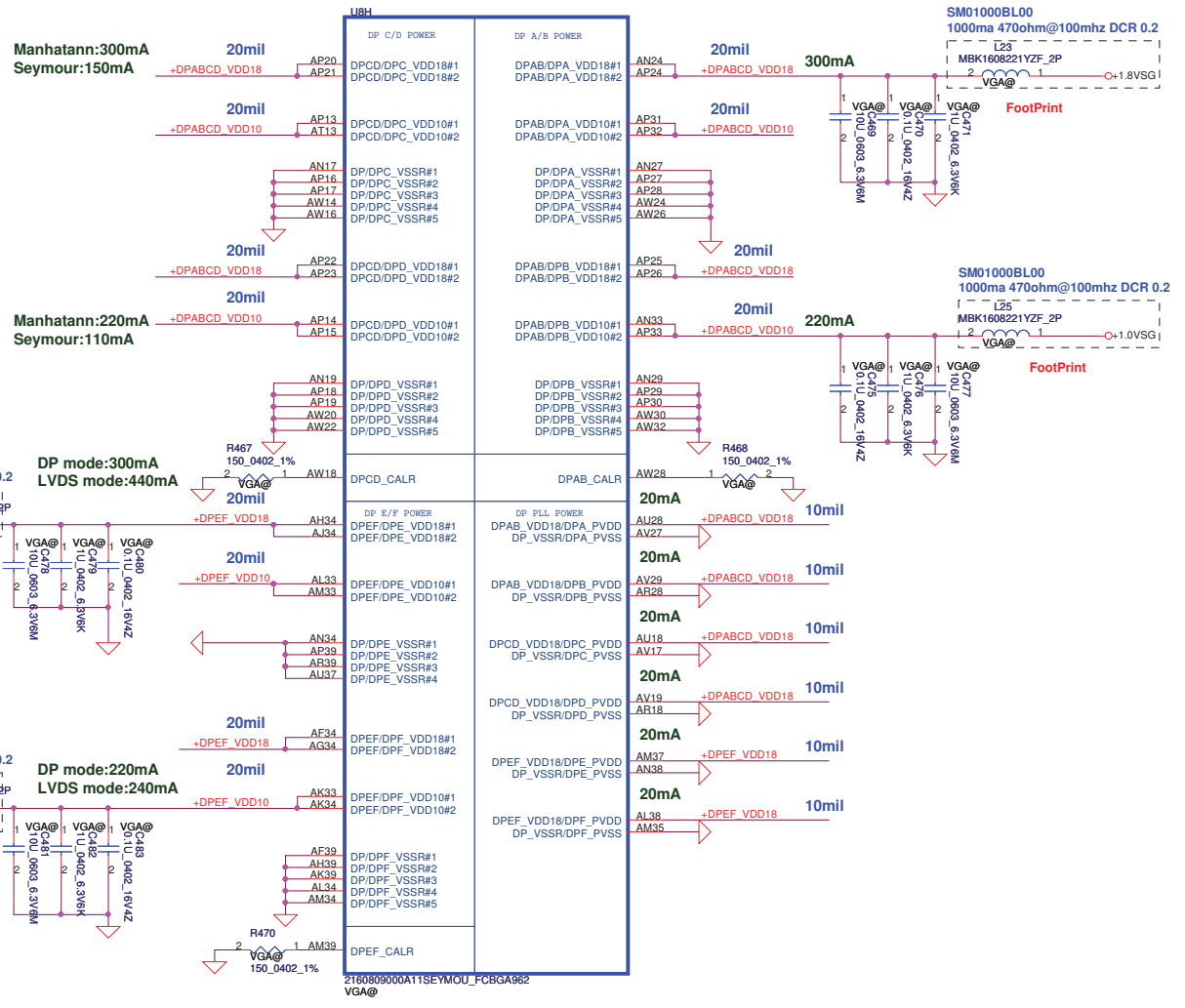


DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD can combian to DPAB_VDD18
 DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD can combian to DPCD_VDD18
 (DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
 DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD can combian to DPEF_VDD18

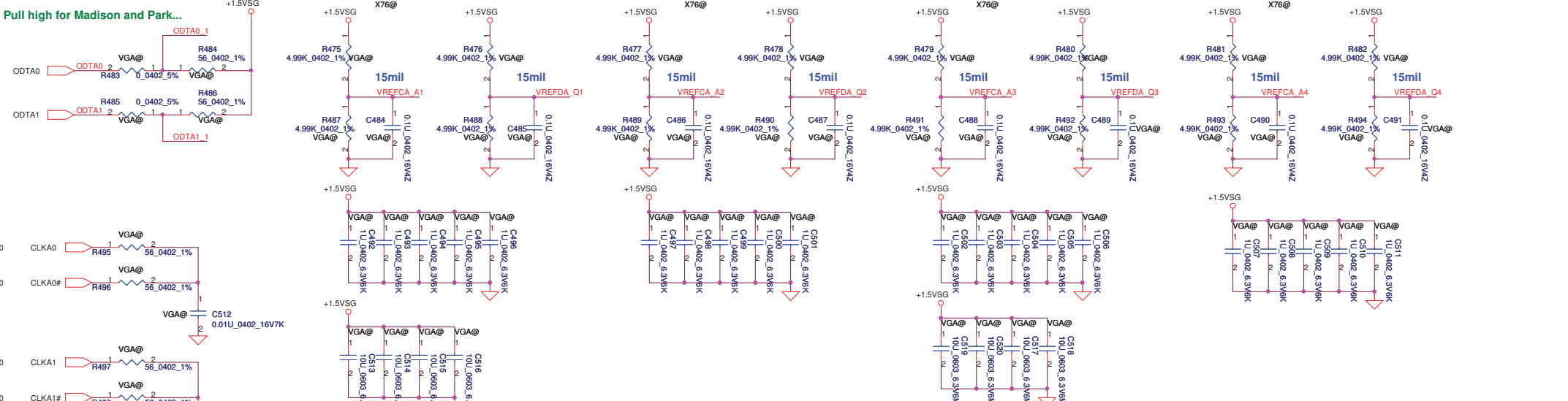
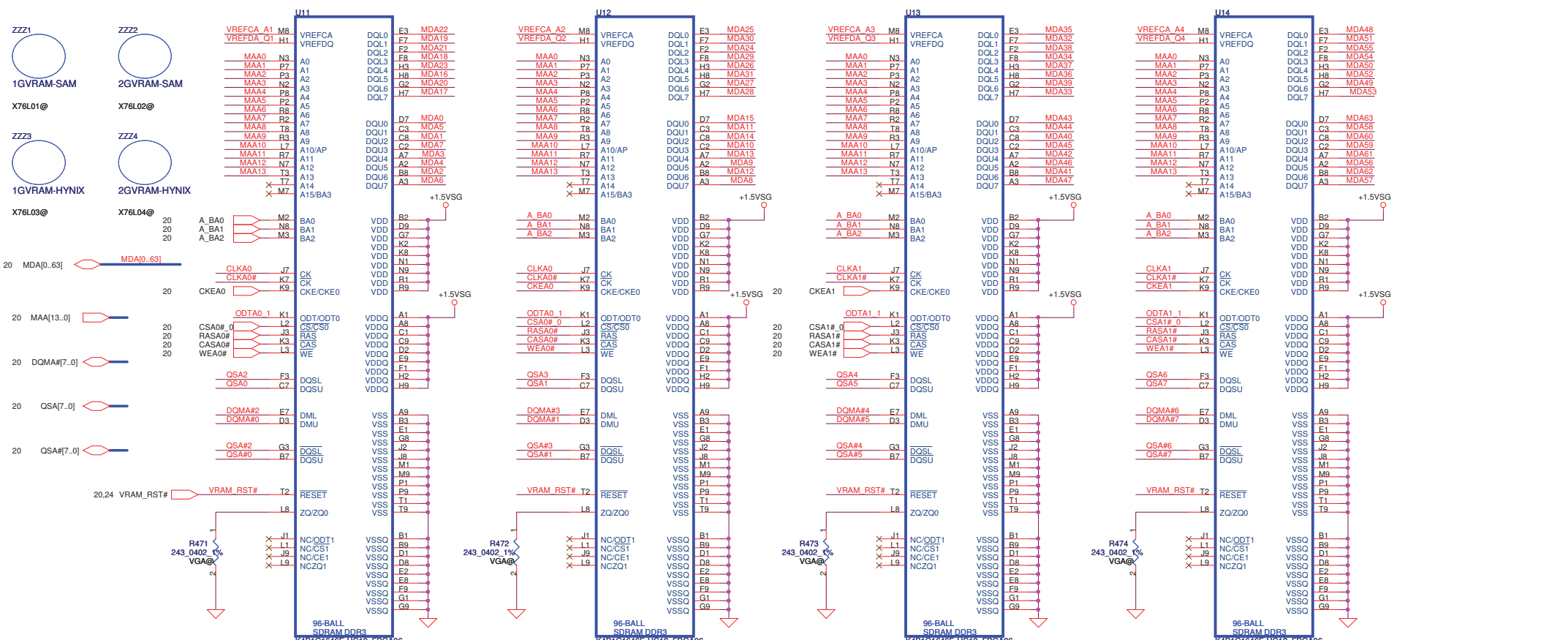
Seymour/Whistler :
 DPA_VDD10,DPB_VDD10 can combian to DPAB_VDD10
 DPC_VDD10,DPD_VDD10 can combian to DPCD_VDD10
 DPE_VDD10,DPD_VDD10 can combian to DPEF_VDD10

DPx-VSSR,DPx_PVSS can combian to DP_VSSR (Manhattan should have individual GND) where x is A,B,C,D,E,F

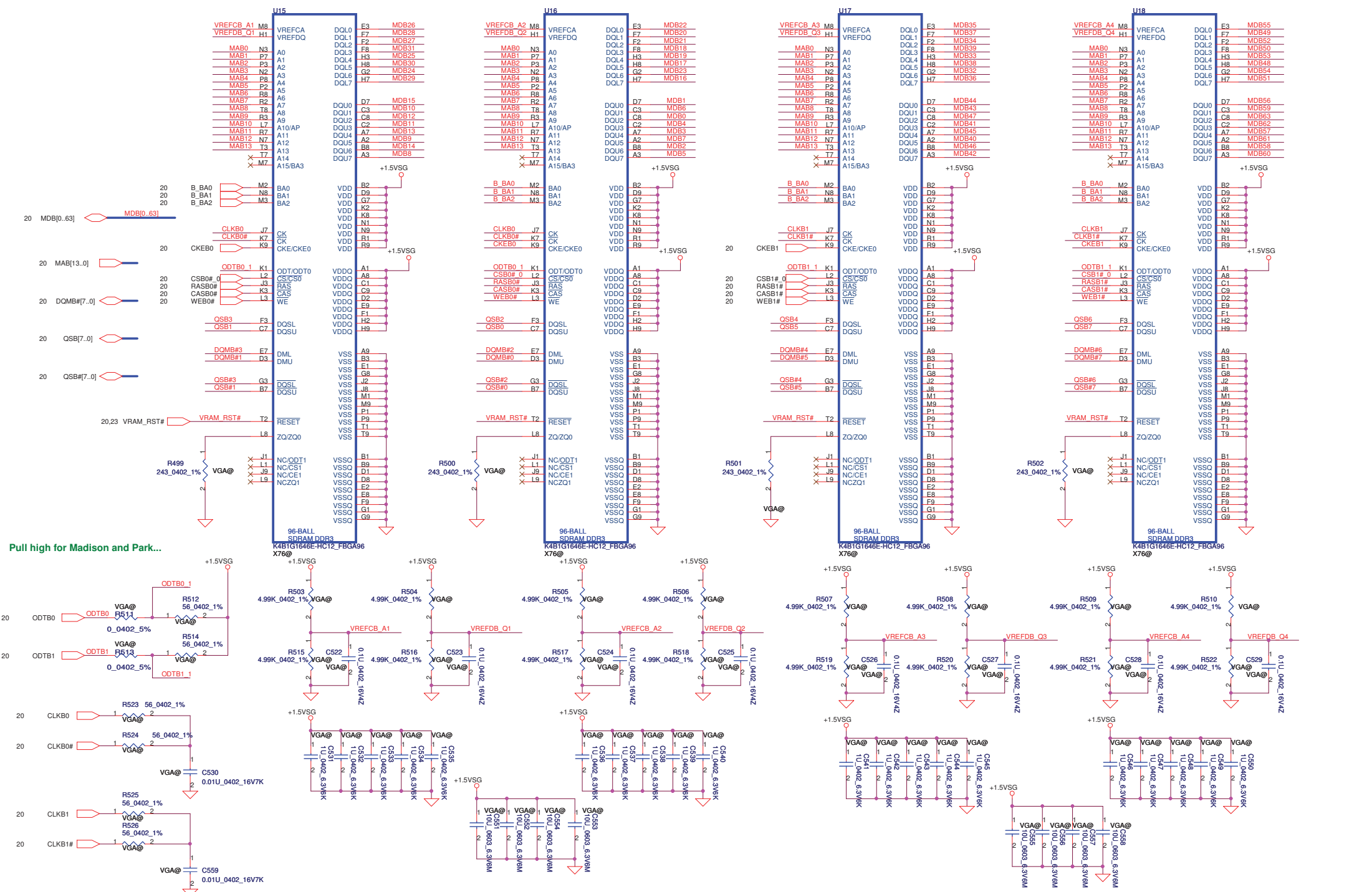
Park/Madison :AL21left NC
 Seymour/Whistler:
 AL21:PX_EN
 use to control discreate GPU regulators for power express BACO mode
 Support BACO:
 output High3.3V:turn off regulators (BACO mode on)
 output Low0V:turn on regulators (BACO mode off) need PD resistor
 No support BACO:
 left NC



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Date: Tuesday, February 22, 2011				Sheet 22	of 49



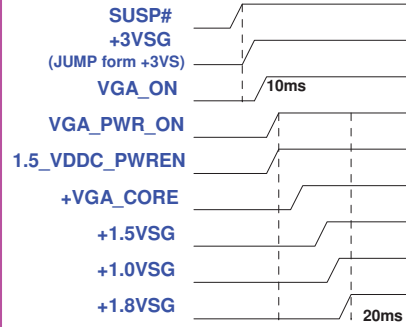
Security Classification		Compal Secret Data		Title		
Issued Date	2010/07/12	Deciphered Date	2012/07/12	VRAM DDR3 / Channel A		
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				Date:	Tuesday, February 22, 2011	Sheet 23 of 49



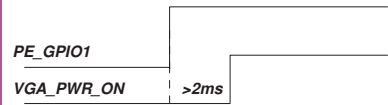
Pull high for Madison and Park...

Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/12	VRAM DDR3 / Channel B	
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				Date: Tuesday, February 22, 2011	Sheet 24 of 49

Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

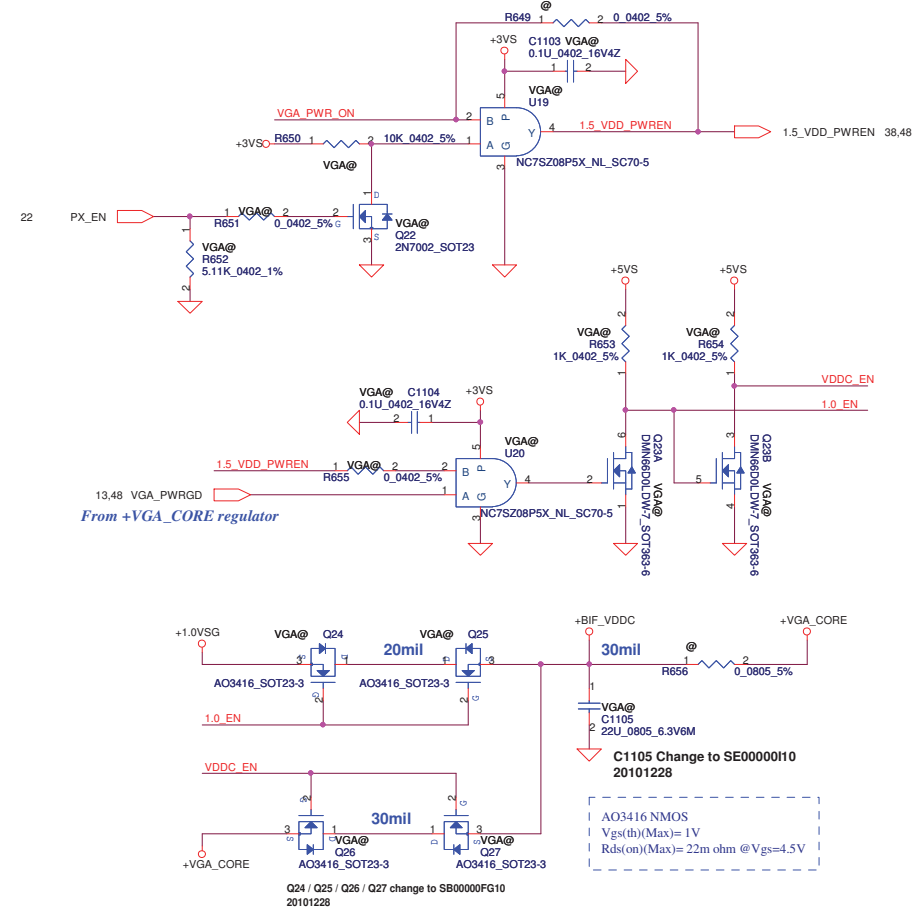
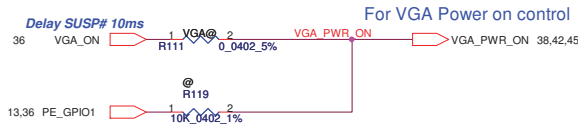


VGA Muxless with BACO Status Mapping table

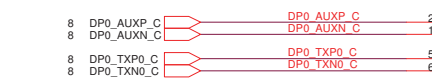
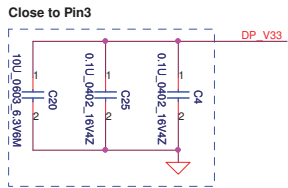
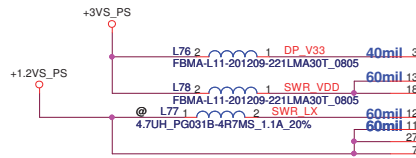
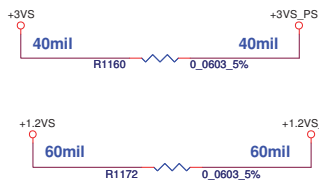
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

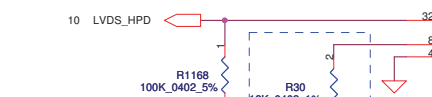
VGA_PWR_ON source signal	Whistler
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



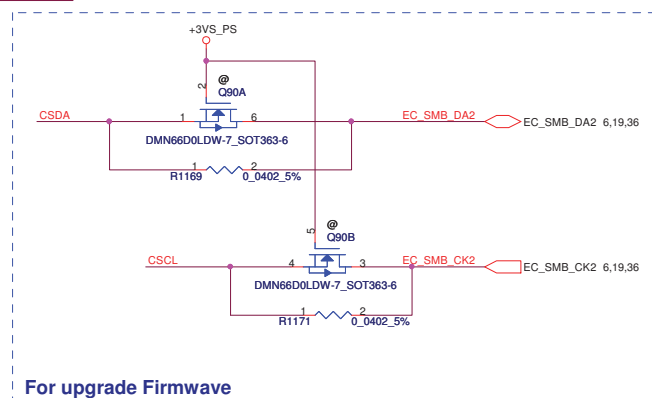
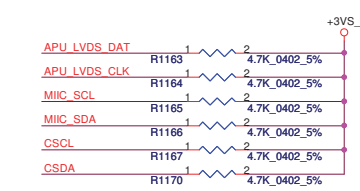
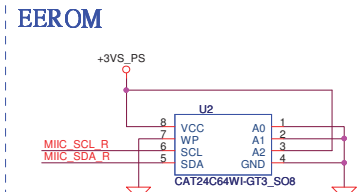
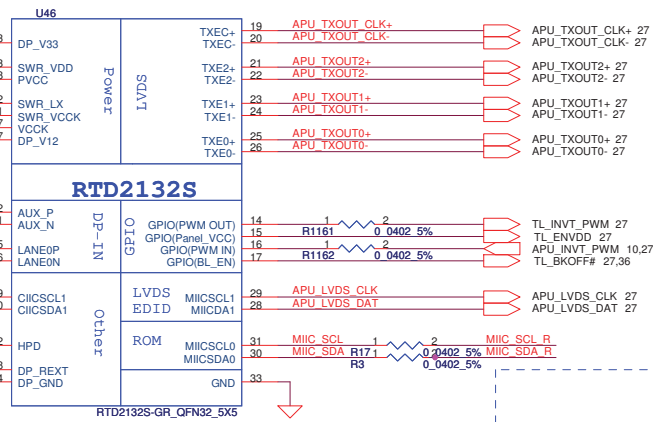
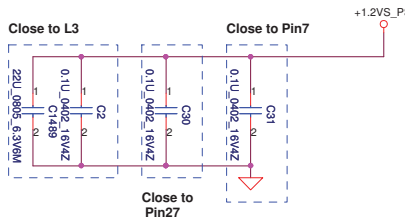
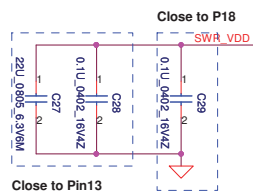
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Issued Date	2010/08/04	Deciphered Date	2010/08/04	VGA power sequence and BACO	
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Reserved for EC programming ROM
Need EC confirm



Change to 12Kohm 1% (DG ref.)
20101114

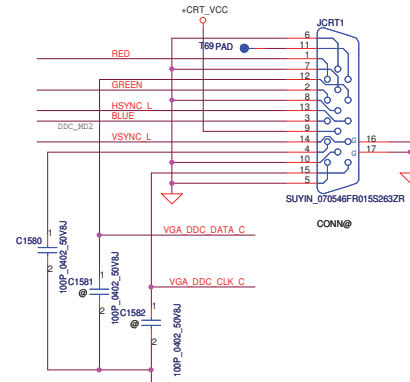
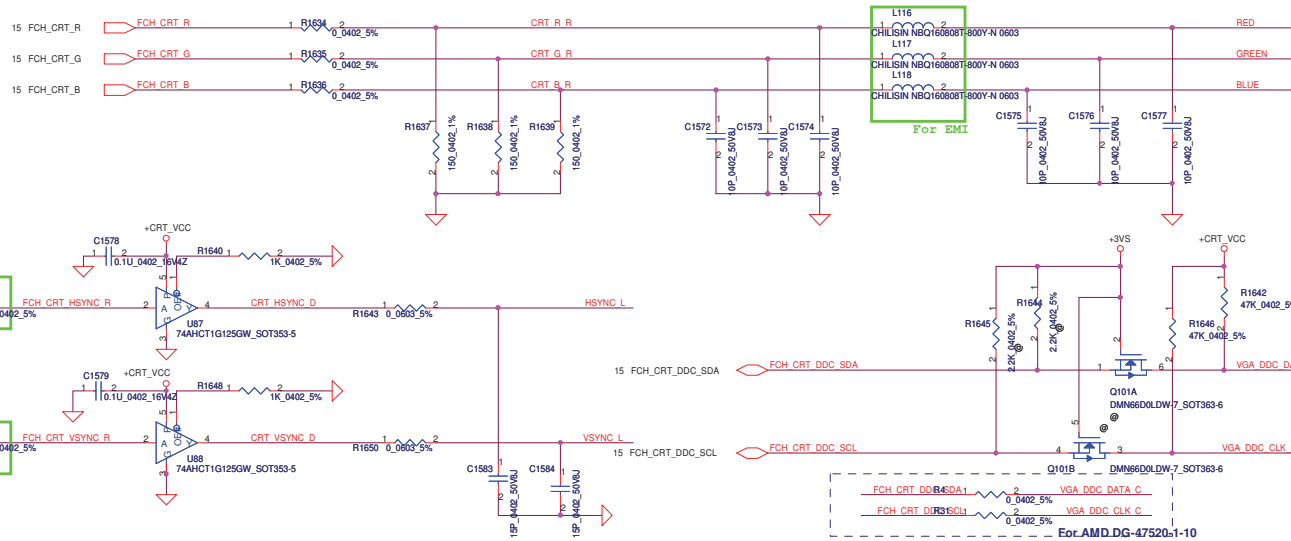
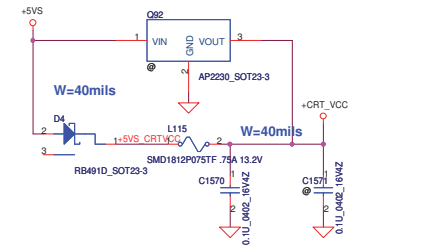
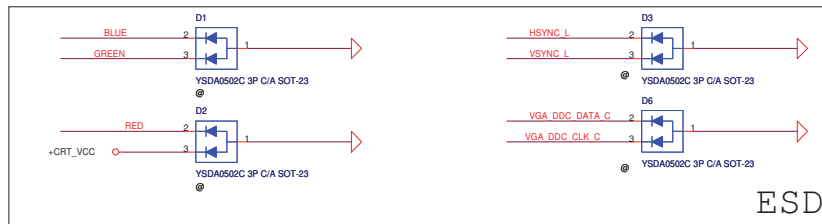


For upgrade Firmwave

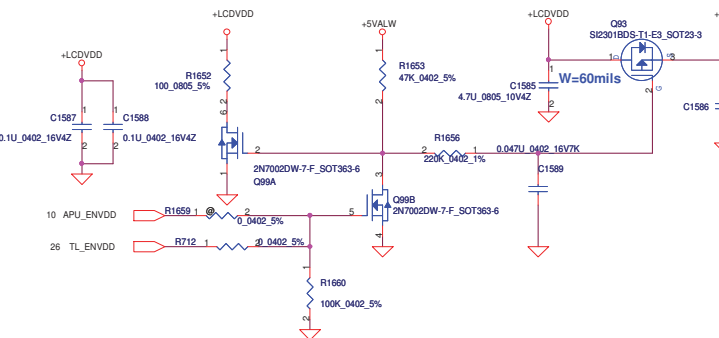


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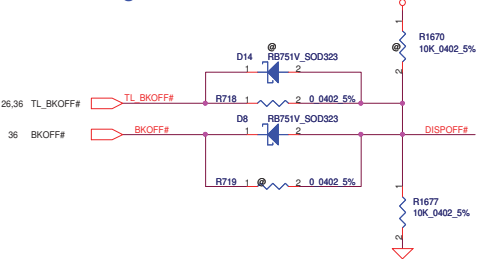
CRT



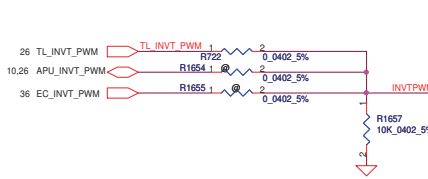
Panel LCDVDD Control



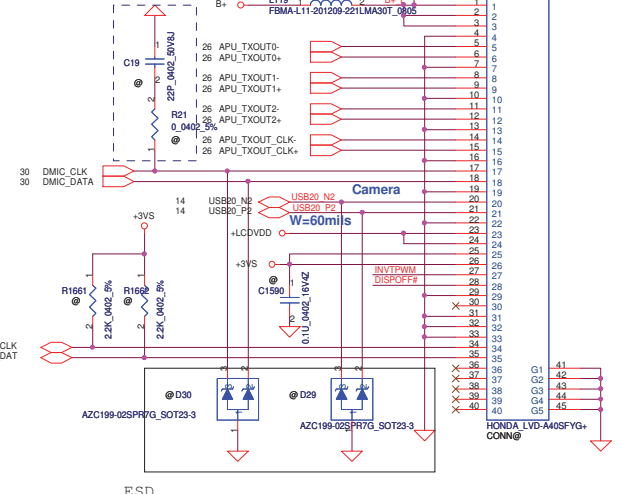
Panel Backlight Control



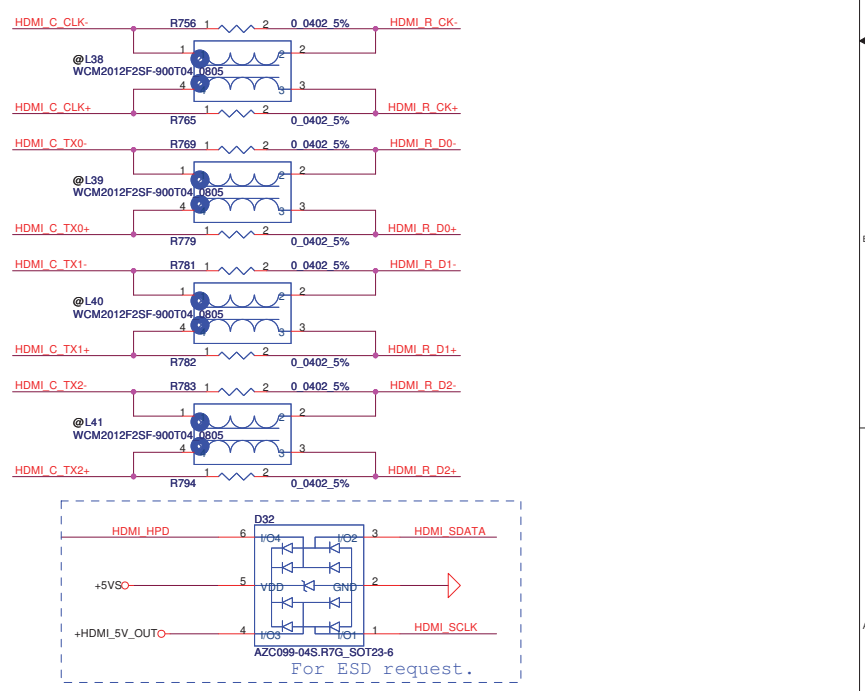
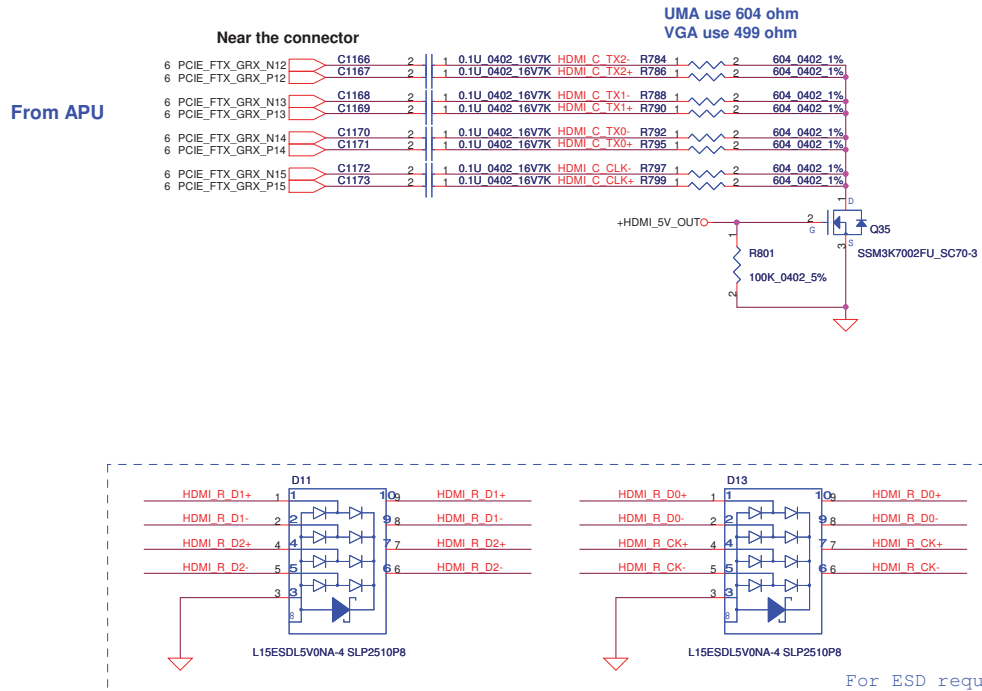
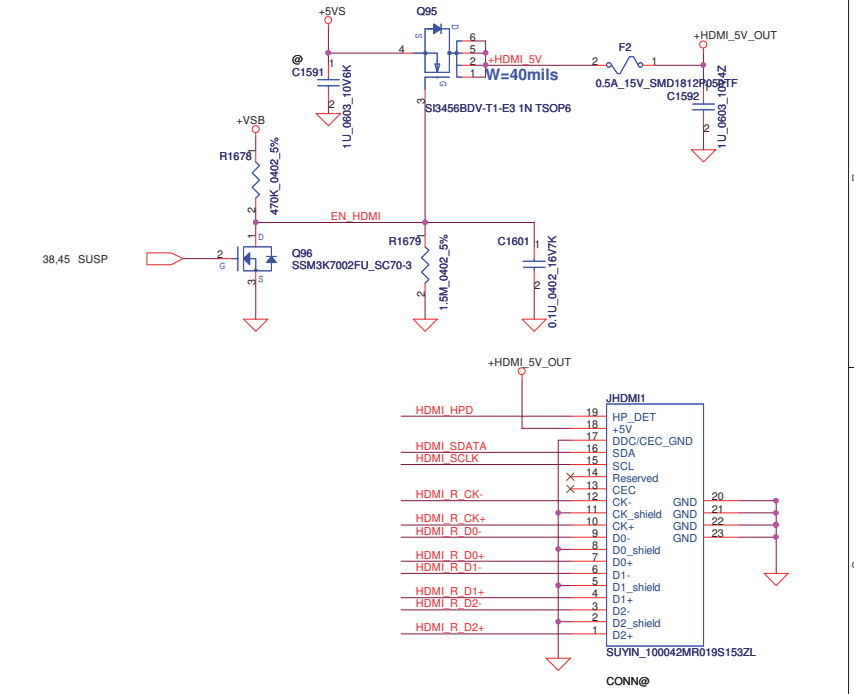
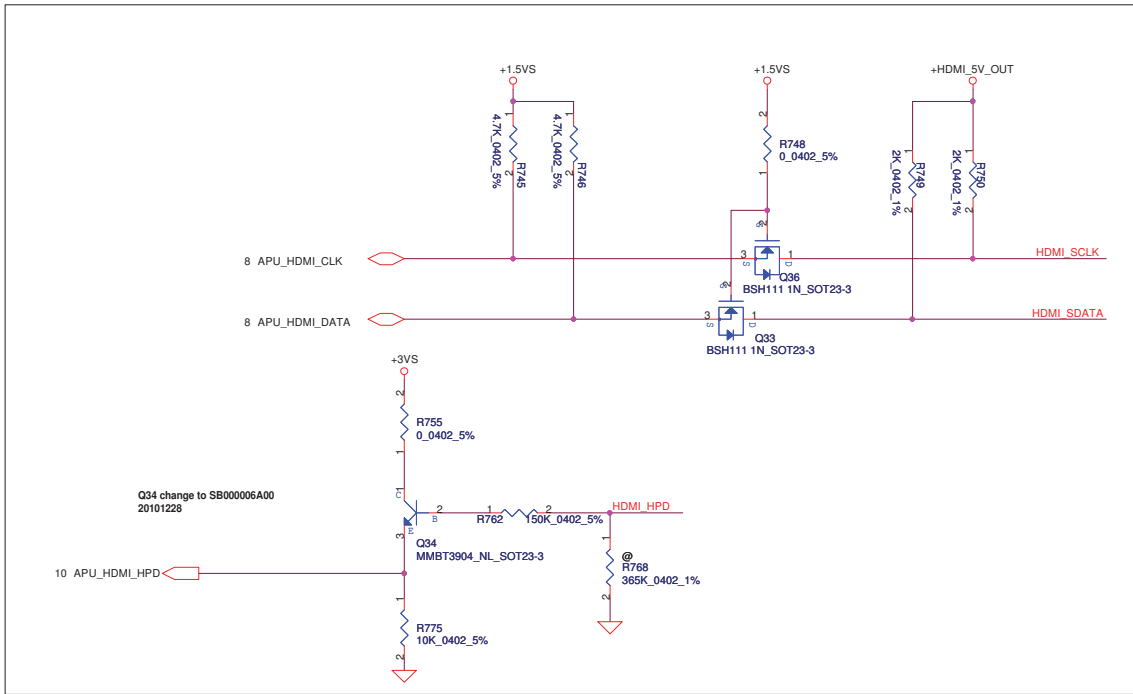
Panel PWM Control



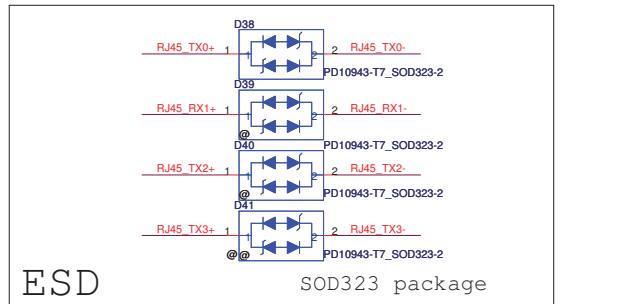
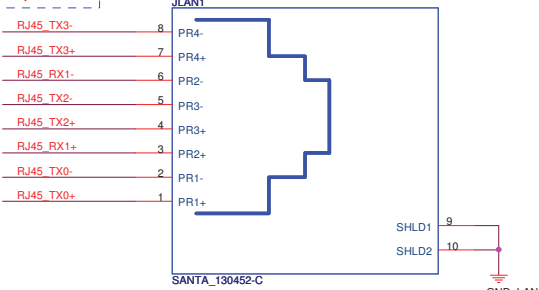
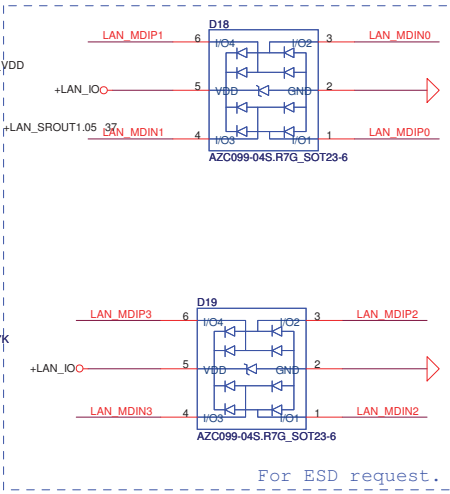
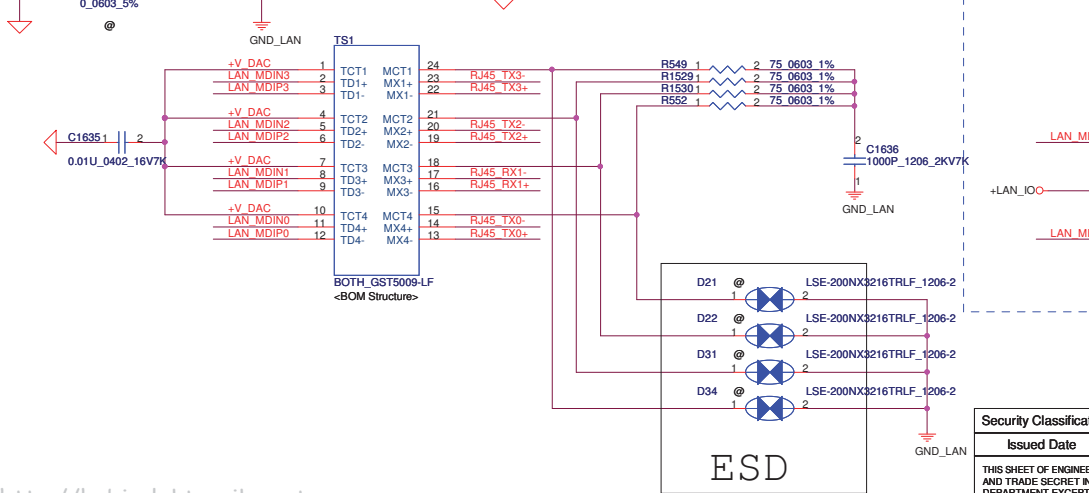
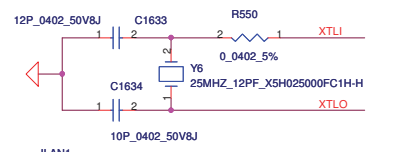
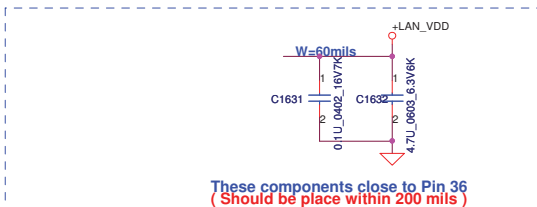
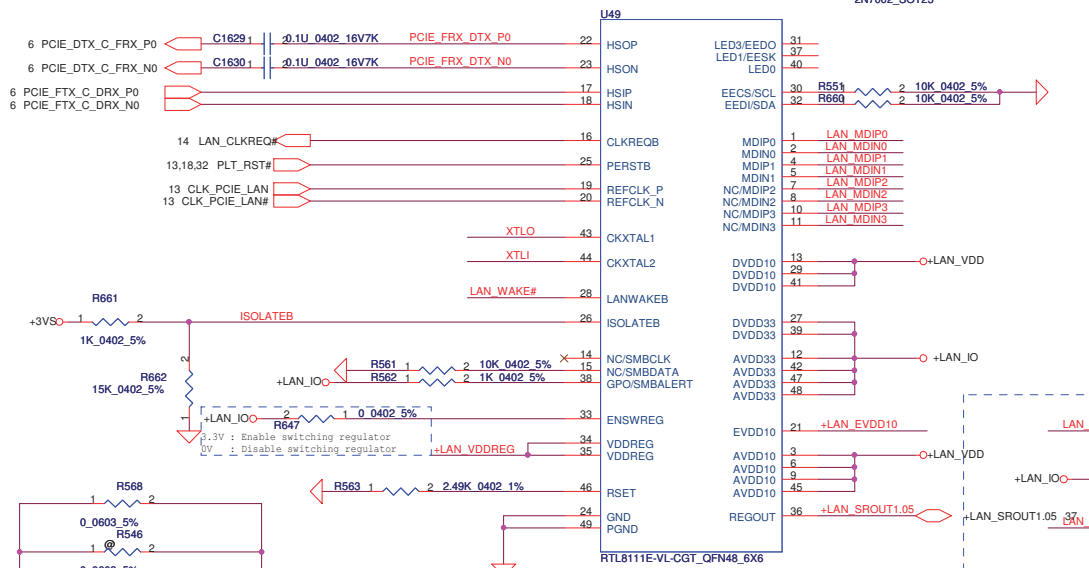
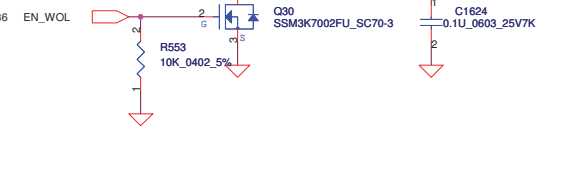
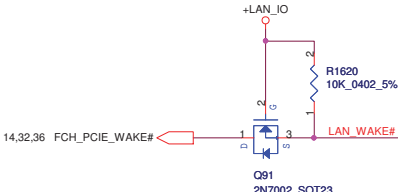
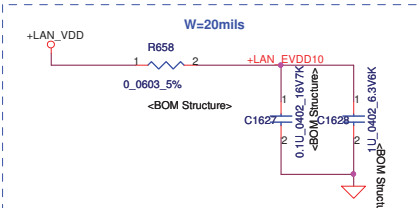
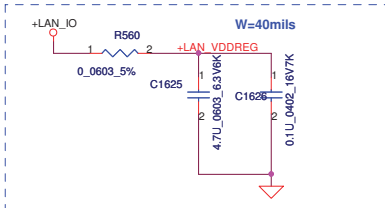
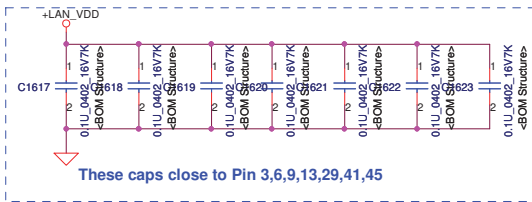
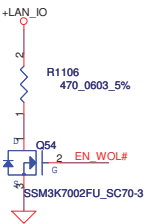
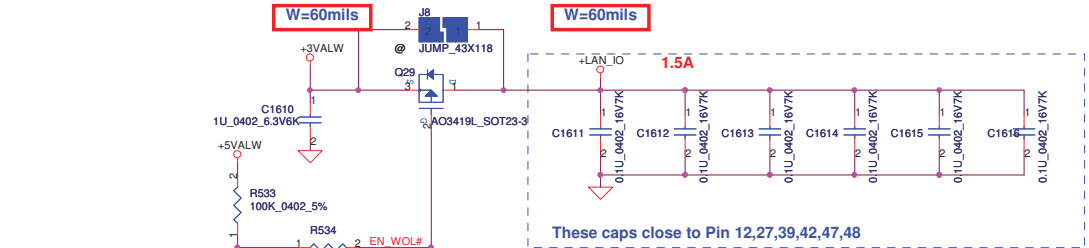
For EMI, close to JLVDS1.

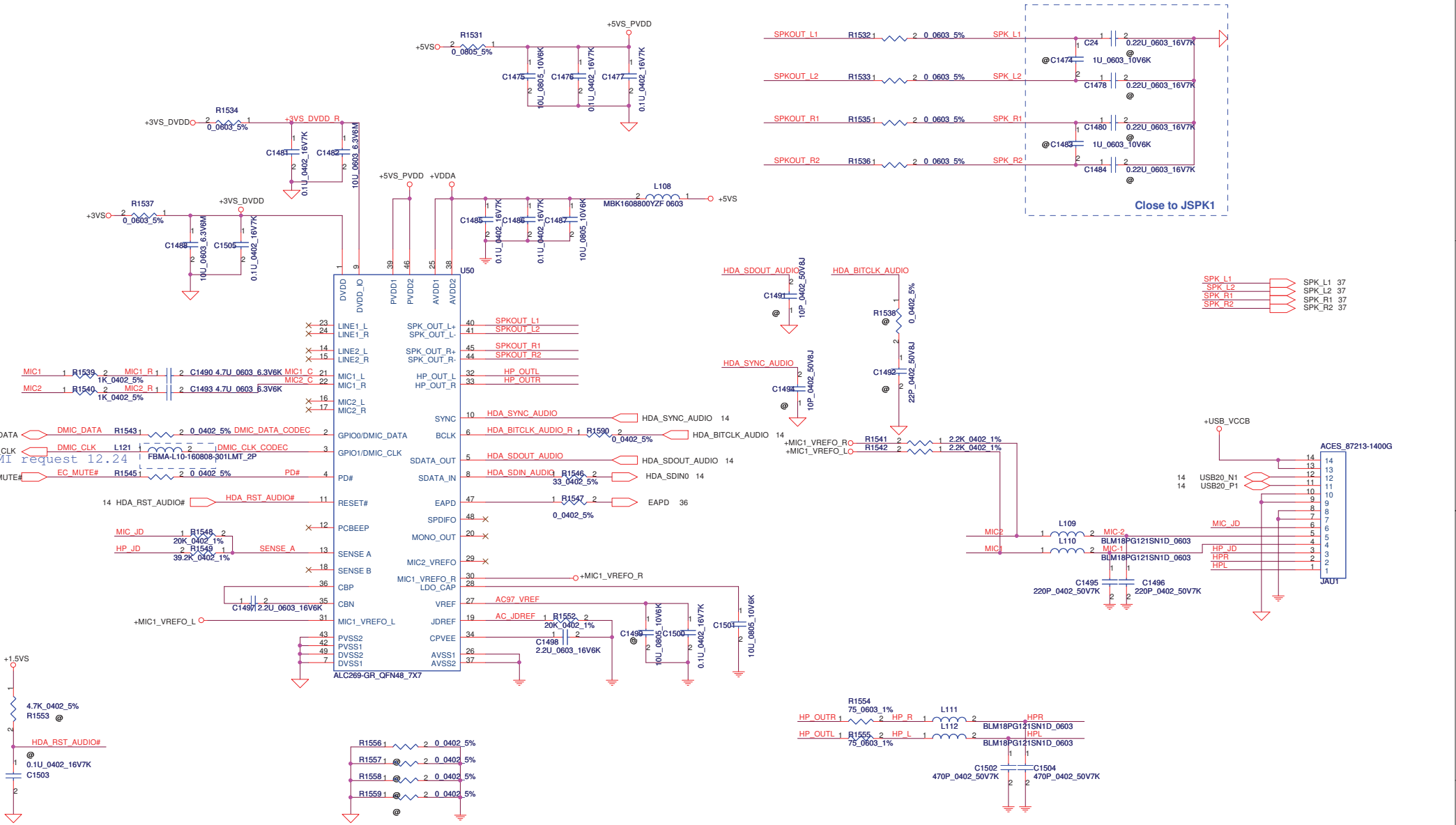


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Size	Document Number	Rev	QBL60 LA-7552P	
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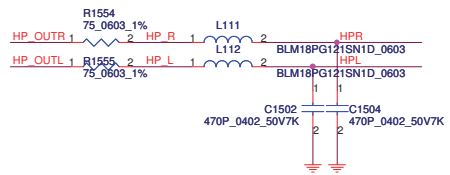
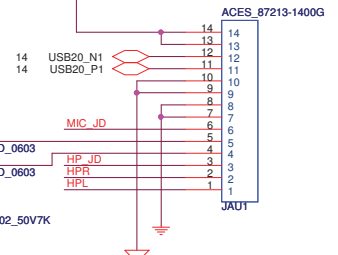


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				HDMI Connector	
				Size	Document Number
				Custom	QBL60 LA-7552P
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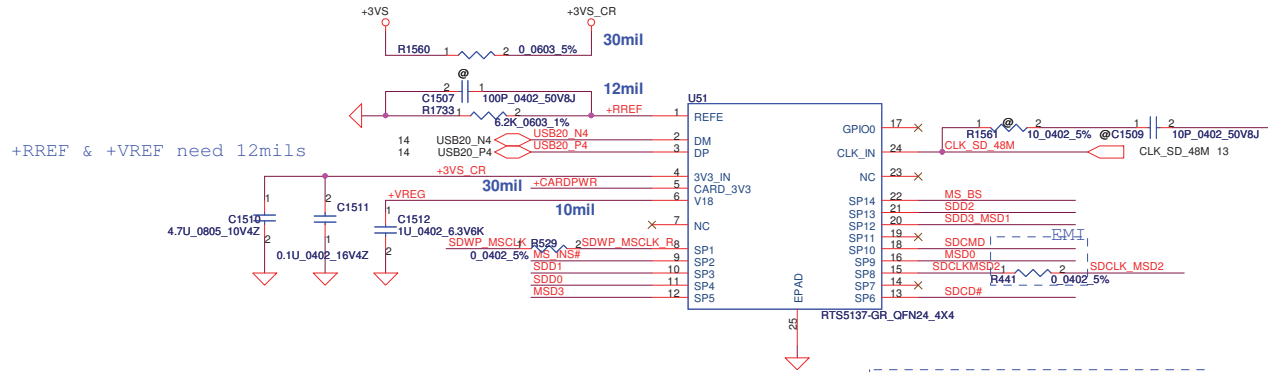


- SPK L1 → SPK_L1 37
- SPK L2 → SPK_L2 37
- SPK R1 → SPK_R1 37
- SPK R2 → SPK_R2 37

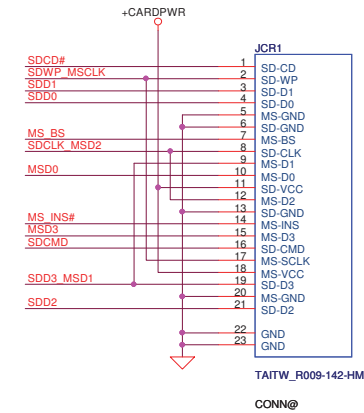
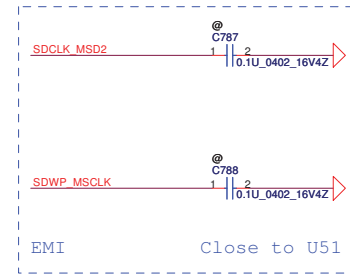
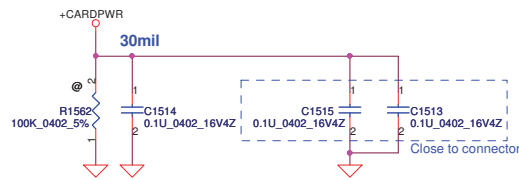


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Card Reader RTS5137 (only SD/MMC/MS function)



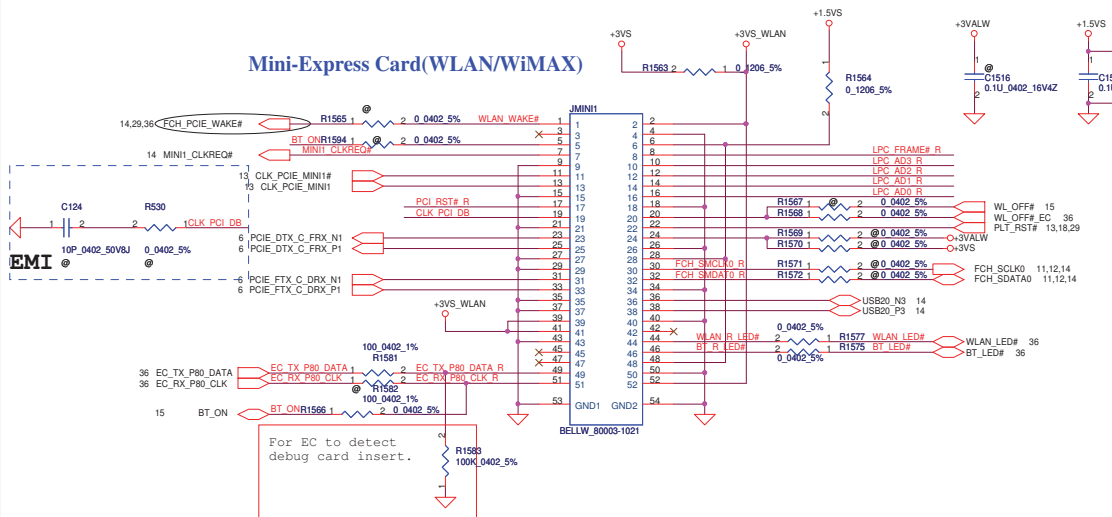
Card Reader Connector



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Size	Document Number	Rev		0.03	
Custom	QBL60 LA-7552P				
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Mini-Express Card for WLAN/WiMAX(Half)

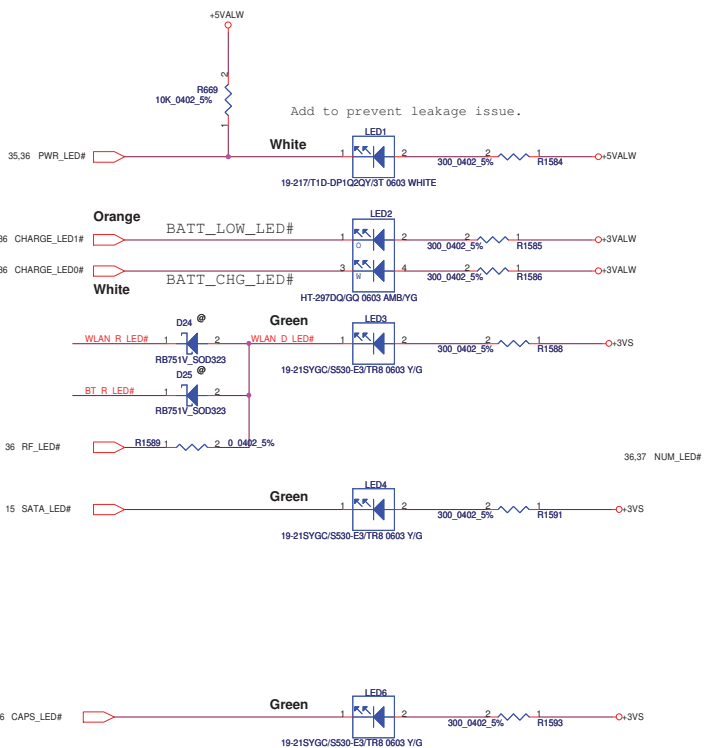
Mini-Express Card(WLAN/WiMAX)



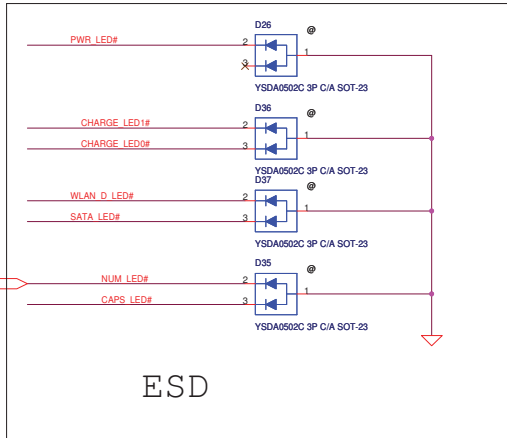
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R1573	1	2	0.0402_5%	LPC_FRAME#	LPC_FRAME#	13,36
LPC_AD3 R	R1574	1	2	0.0402_5%	LPC_AD3	LPC_AD3	13,36
LPC_AD2 R	R1576	1	2	0.0402_5%	LPC_AD2	LPC_AD2	13,36
LPC_AD1 R	R1578	1	2	0.0402_5%	LPC_AD1	LPC_AD1	13,36
LPC_AD0 R	R1579	1	2	0.0402_5%	LPC_AD0	LPC_AD0	13,36
PCI_RST# R	R1580	1	2	0.0402_5%	PLT_RST#	LPC_AD0	13,36
CLK_PCIE_DB						CLK_PCIE_DB	13

LED

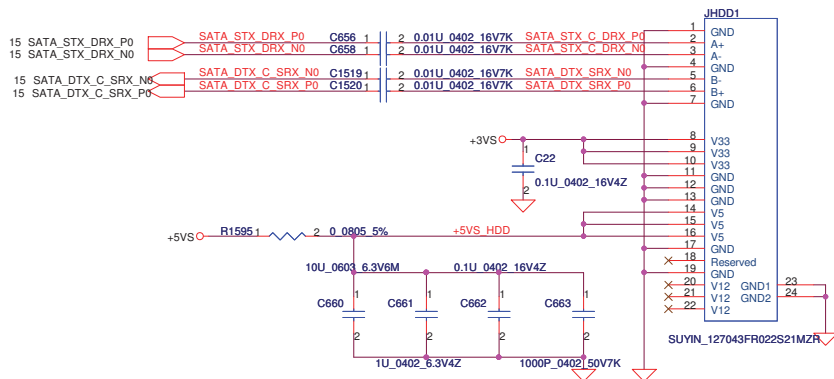


ESD

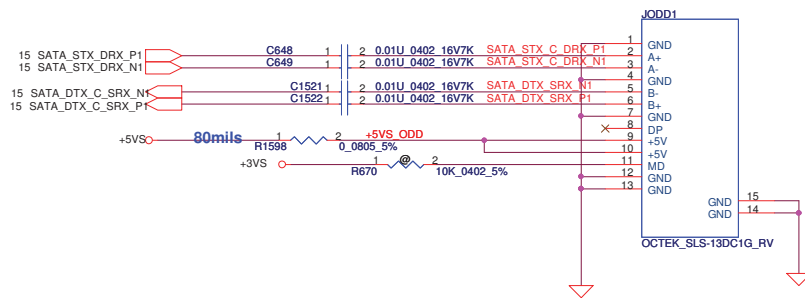


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				P28-Mini PCIE/LED	
				QBL60 LA-7552P	
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SATA HDD Conn.

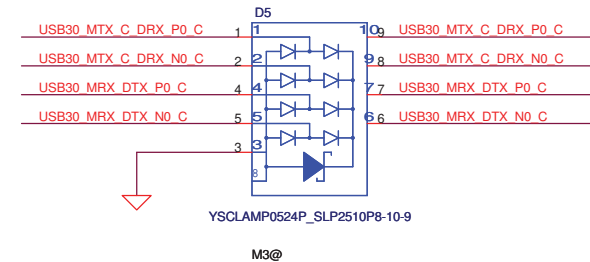
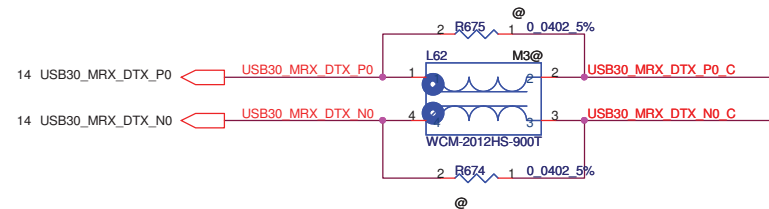
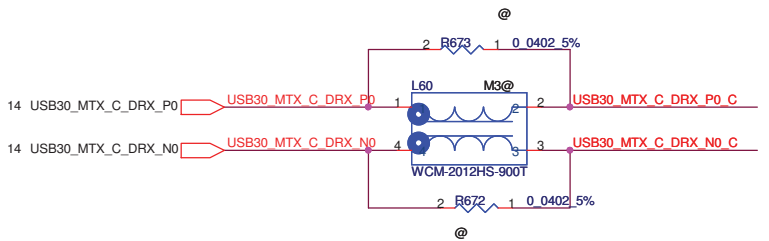
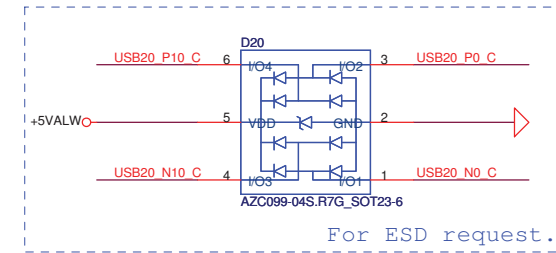
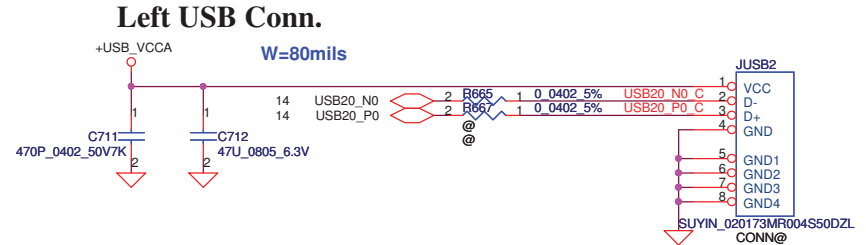
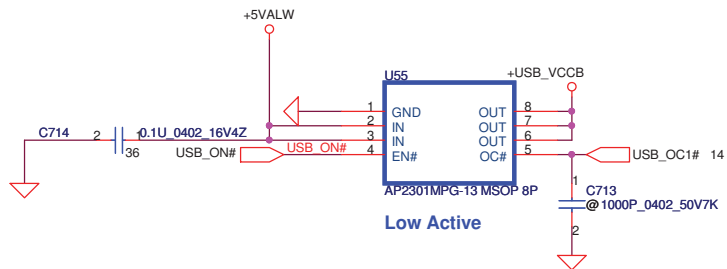
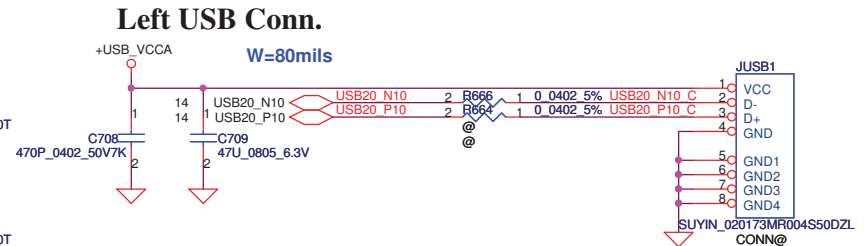
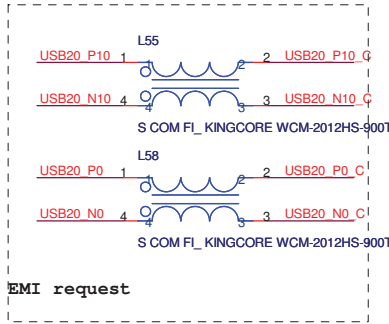
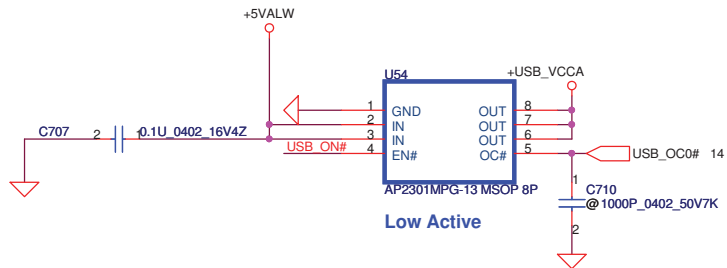


SATA ODD FFC Conn.



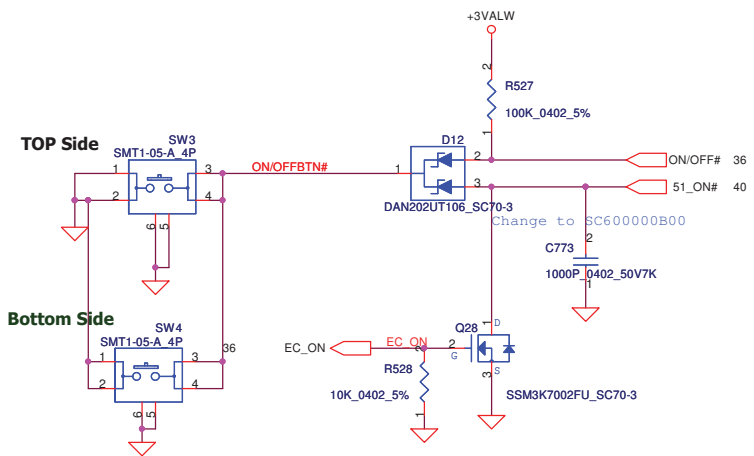
Security Classification	Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date
		2012/06/30
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>		

Compal Electronics, Inc. P29-HDD & ODD CONN		
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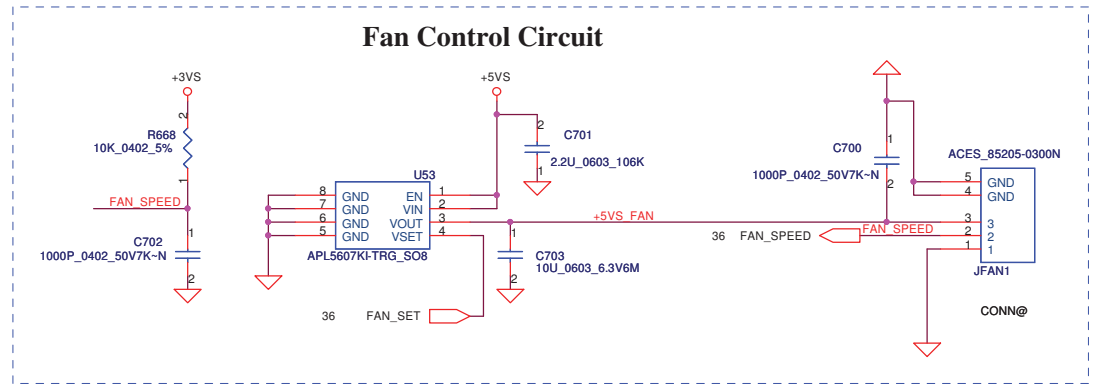


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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	
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				Custom	0.03
				Document Number	QBL60 LA-7552P
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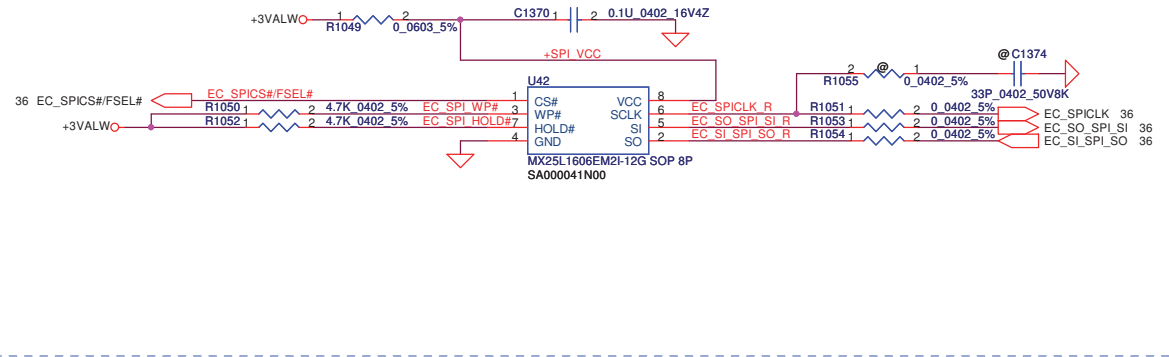
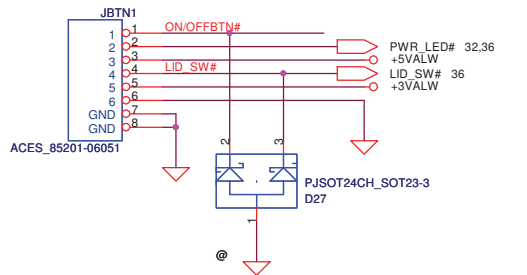
ON/OFF switch Power Button



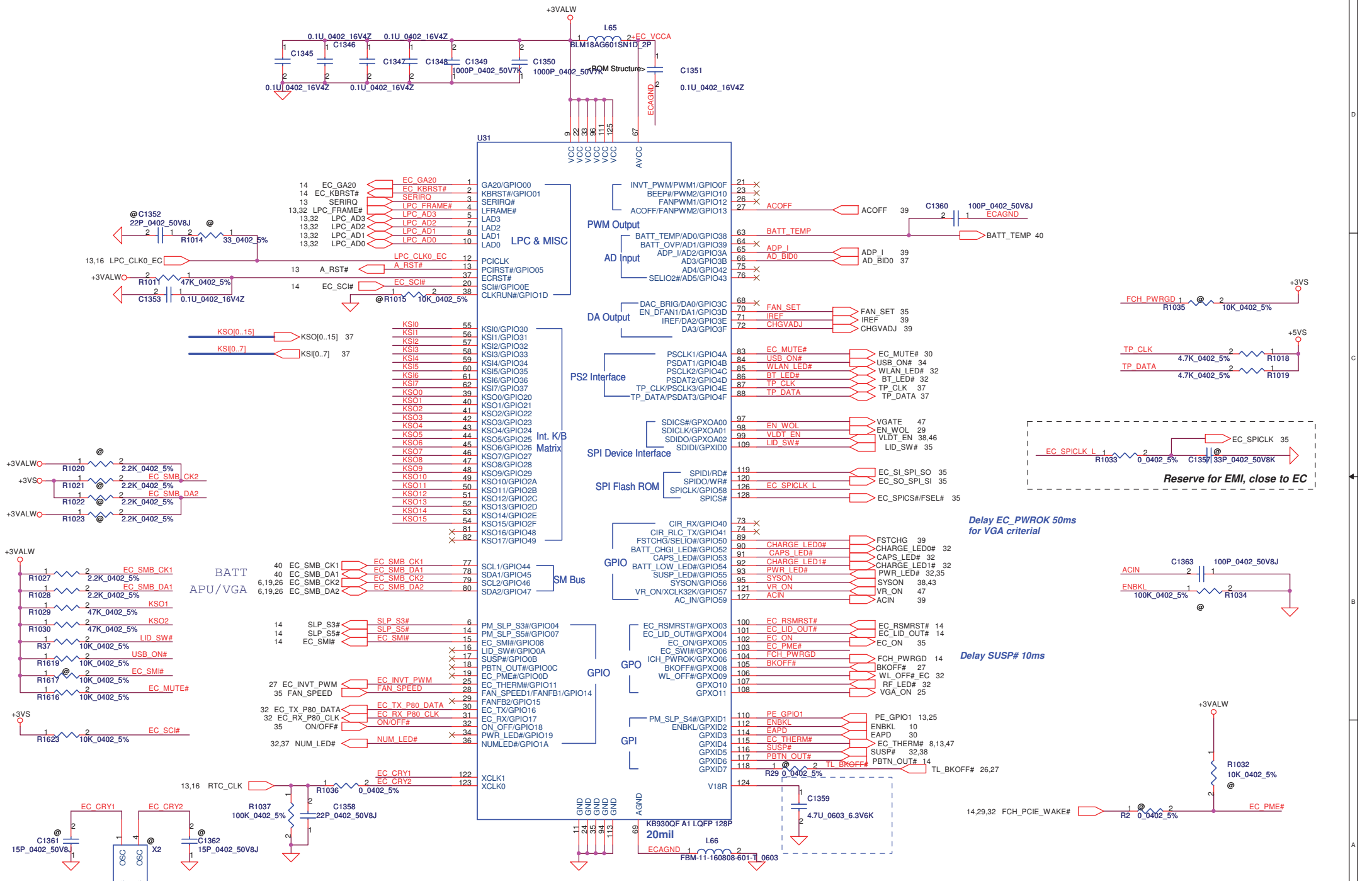
Fan Control Circuit



EC BIOS ROM



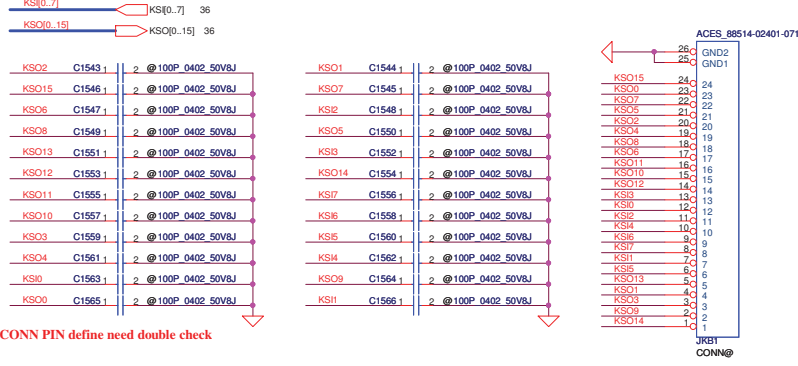
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	
				P31-KB /SW/TP/Lid	
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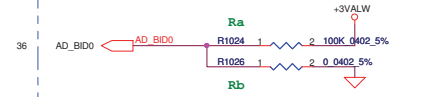
Compal Electronics, Inc.			
Title EC ENE KB930			
Size B	Document Number QBL60 LA-7552P	Rev 0.03	
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INT_KBD Conn.

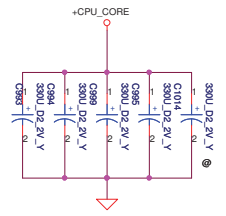


CONN PIN define need double check

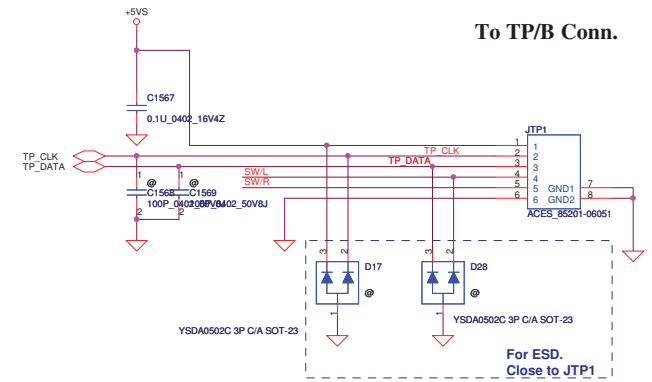
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V



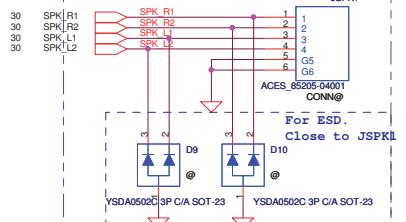
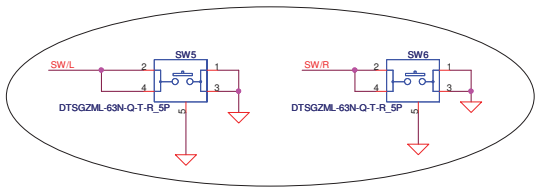
P9 FS1 PWR/GND



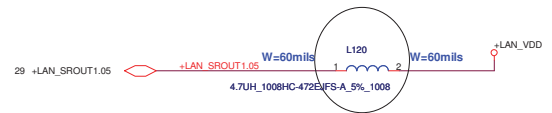
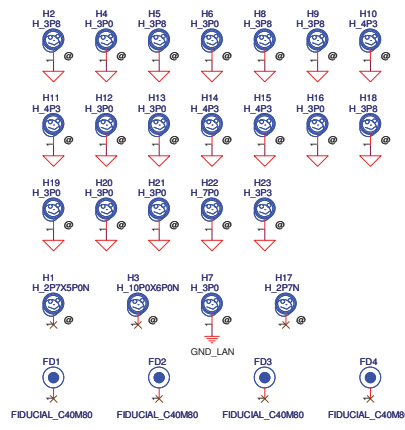
To TP/B Conn.



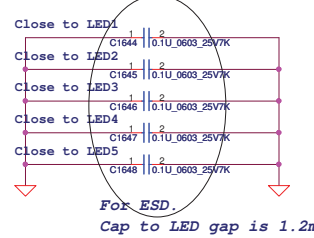
For ESD. Close to JTP1



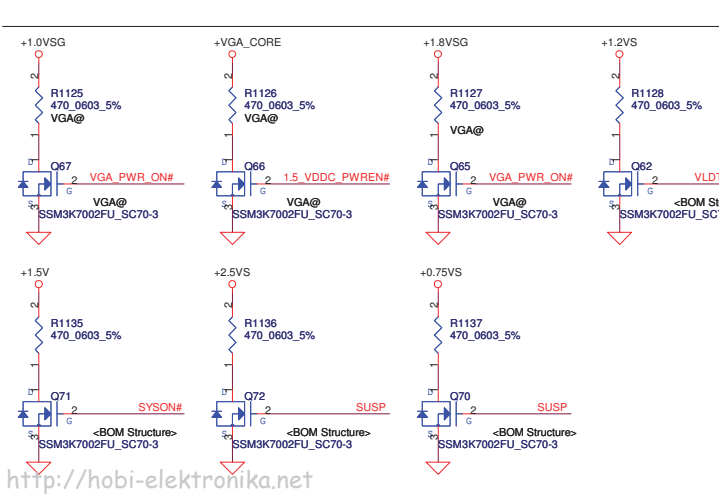
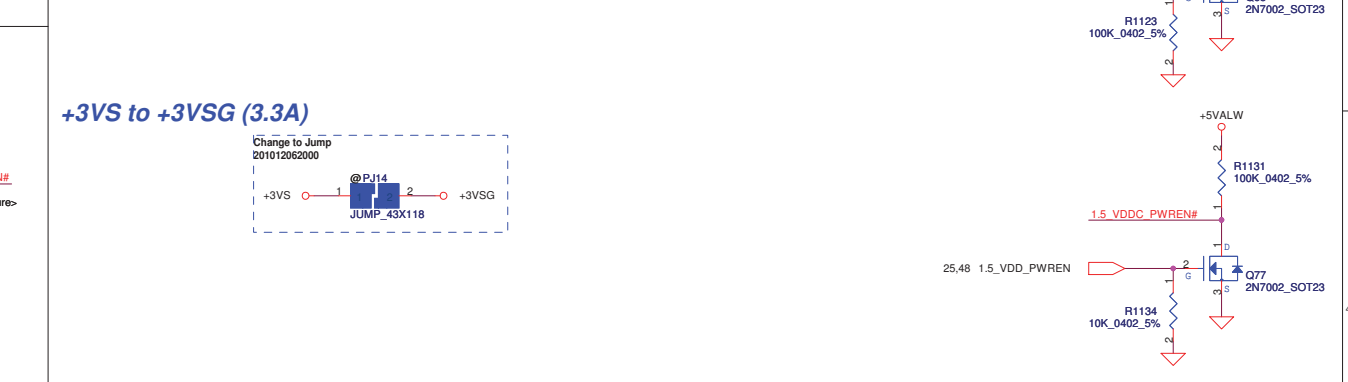
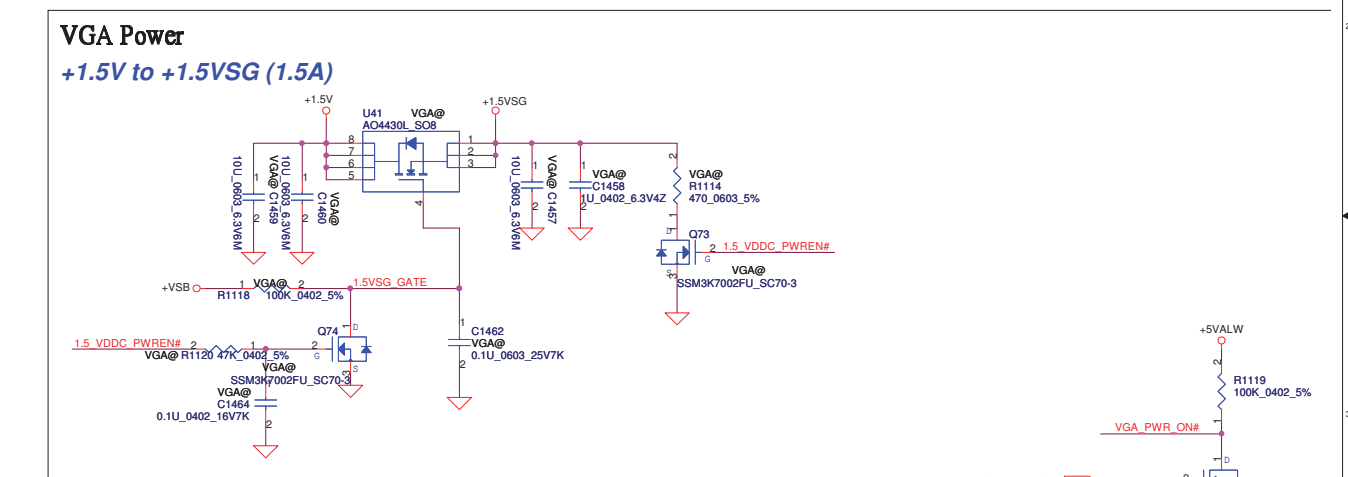
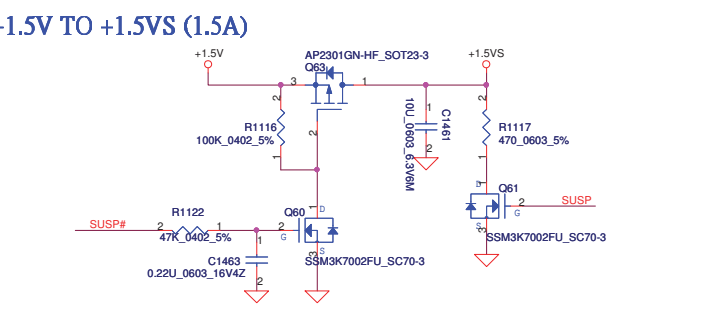
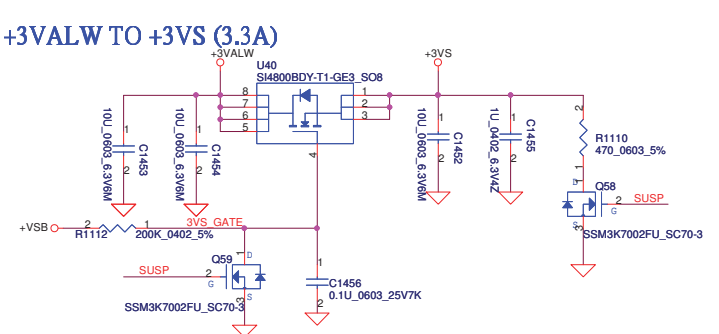
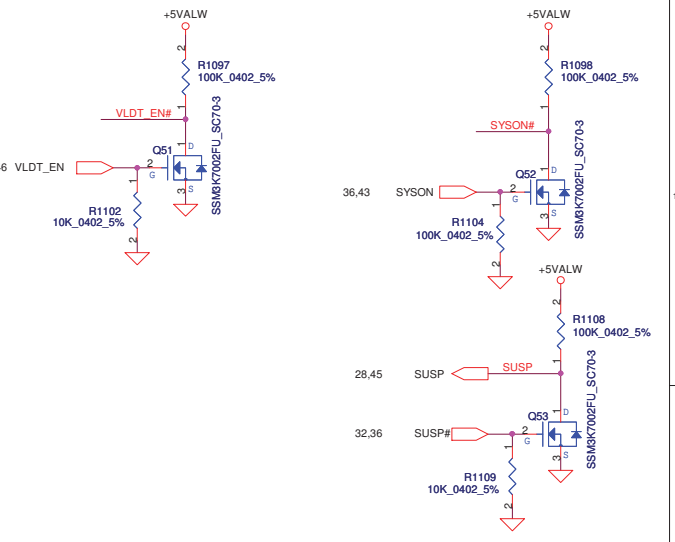
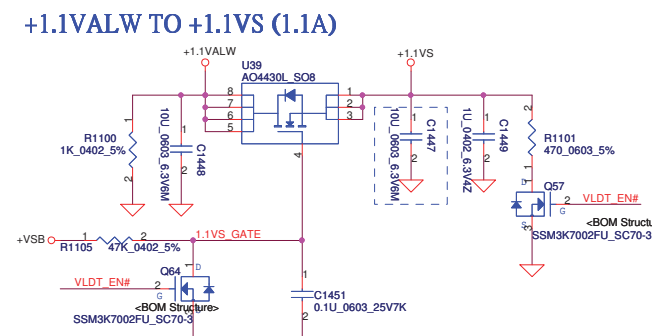
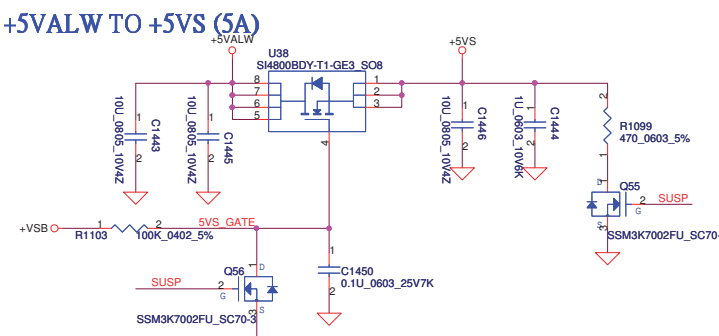
For ESD. Close to JSPK1



These components close to Pin 36 (Should be place within 200 mils)

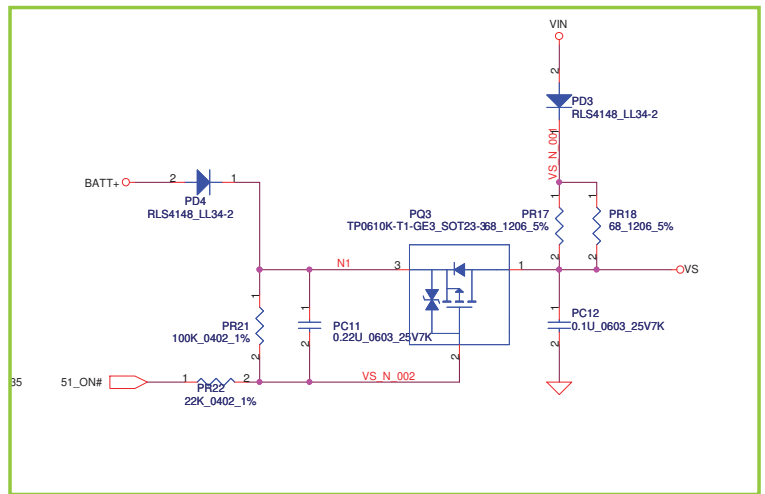
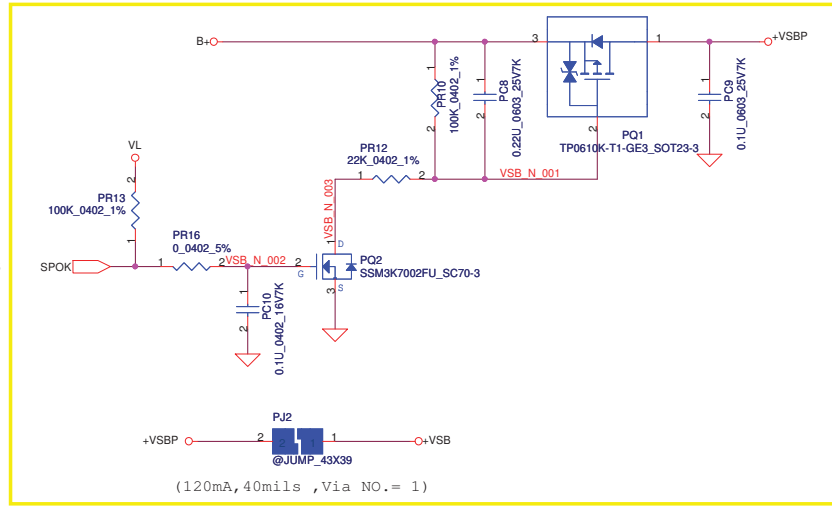
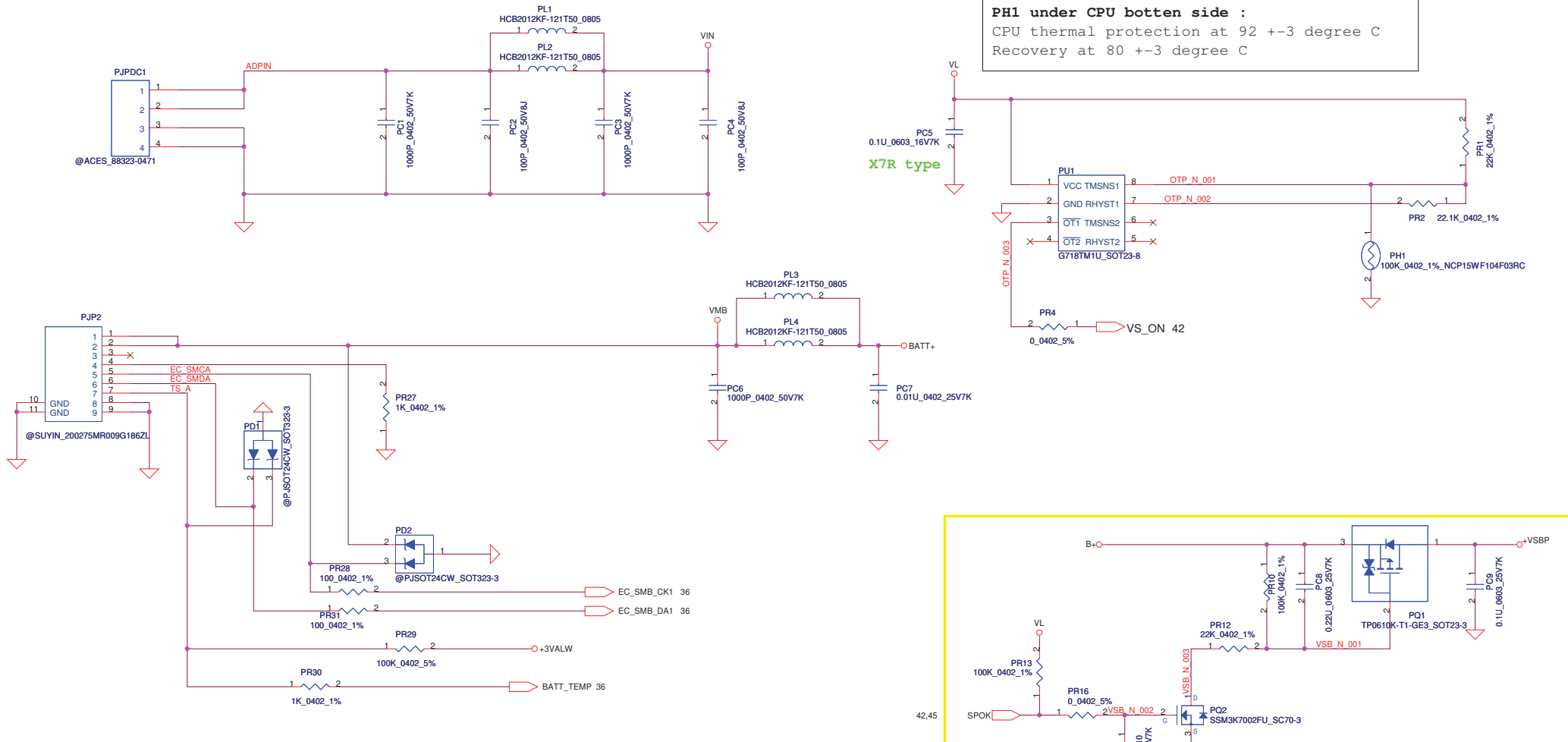


For ESD. Cap to LED gap is 1.2mm.



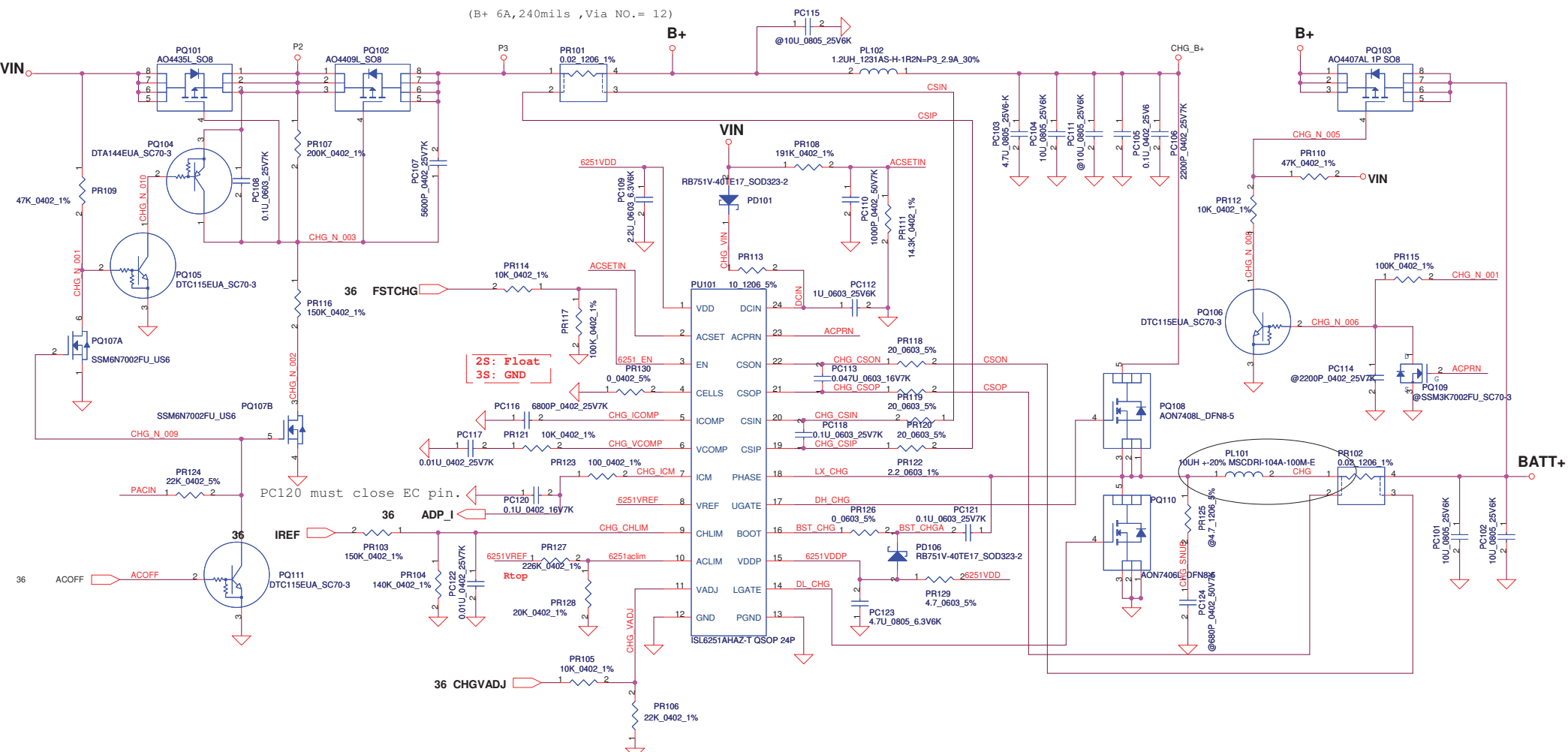
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Issued Date	2010/08/04	Deciphered Date	2010/08/04	DC Interface	
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PH1 under CPU botten side :
 CPU thermal protection at 92 +/-3 degree C
 Recovery at 80 +/-3 degree C



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(B+ 6A,240mils ,Via NO.= 12)



2S: Float
3S: GND

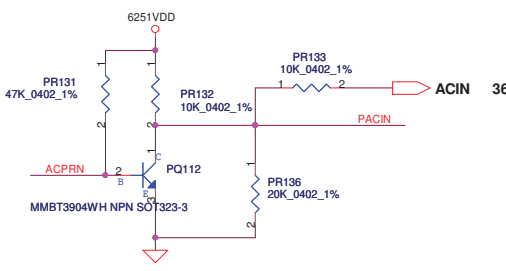
36 CHGVADJ

CP= 85%*Iada;
Iada=0~4.737A (90W); CP=4.03A; where Racdet=0.020ohm, where Rtop=12.4K
90W for Dis: Rtop: SD00000AJ80
Iada=0~3.421A (65W); CP=2.91A; where Racdet=0.020ohm, where Rtop=226K
65W for UMA: Rtop: SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*(0.05*Vaclim/VREF+0.05)
when 90W, Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W, Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

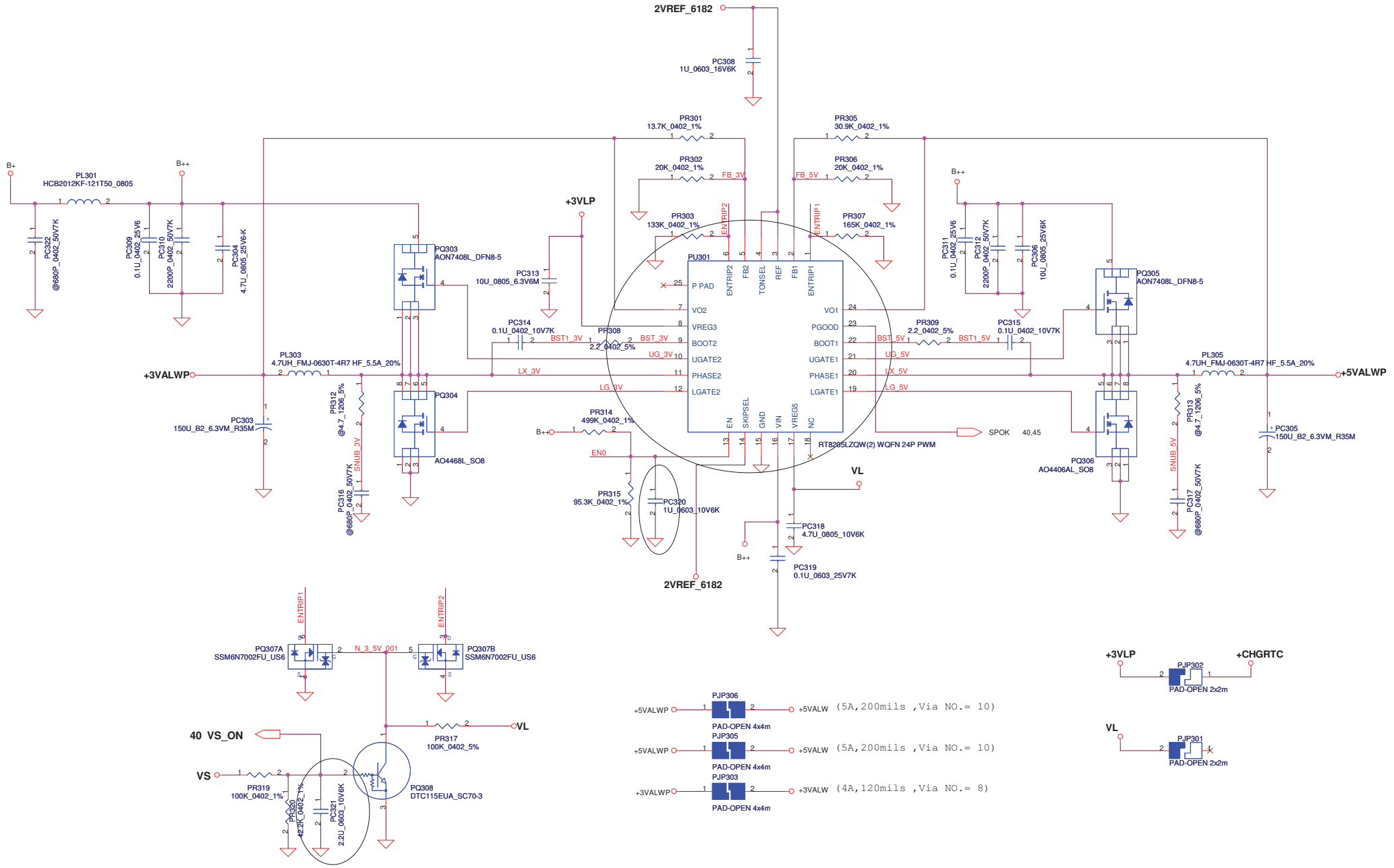
CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V-3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V



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Compal Electronics, Inc.			
CHARGER			
Title	Document Number	Rev	
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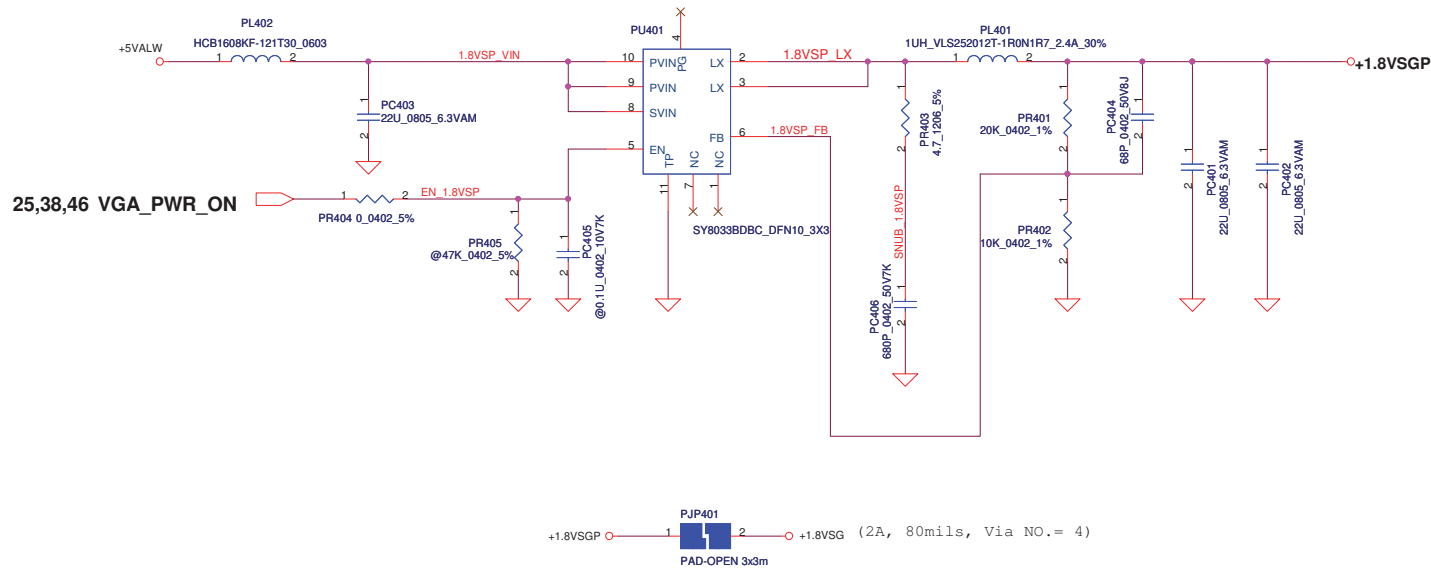


EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

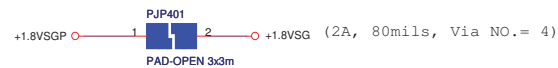
Security Classification	Compal Secret Data	
Issued Date	2007/08/02	Deciphered Date
		2008/08/02

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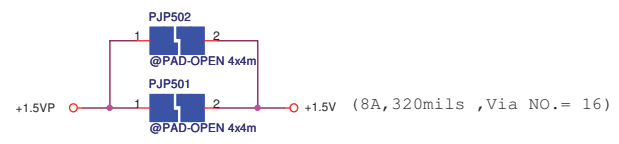
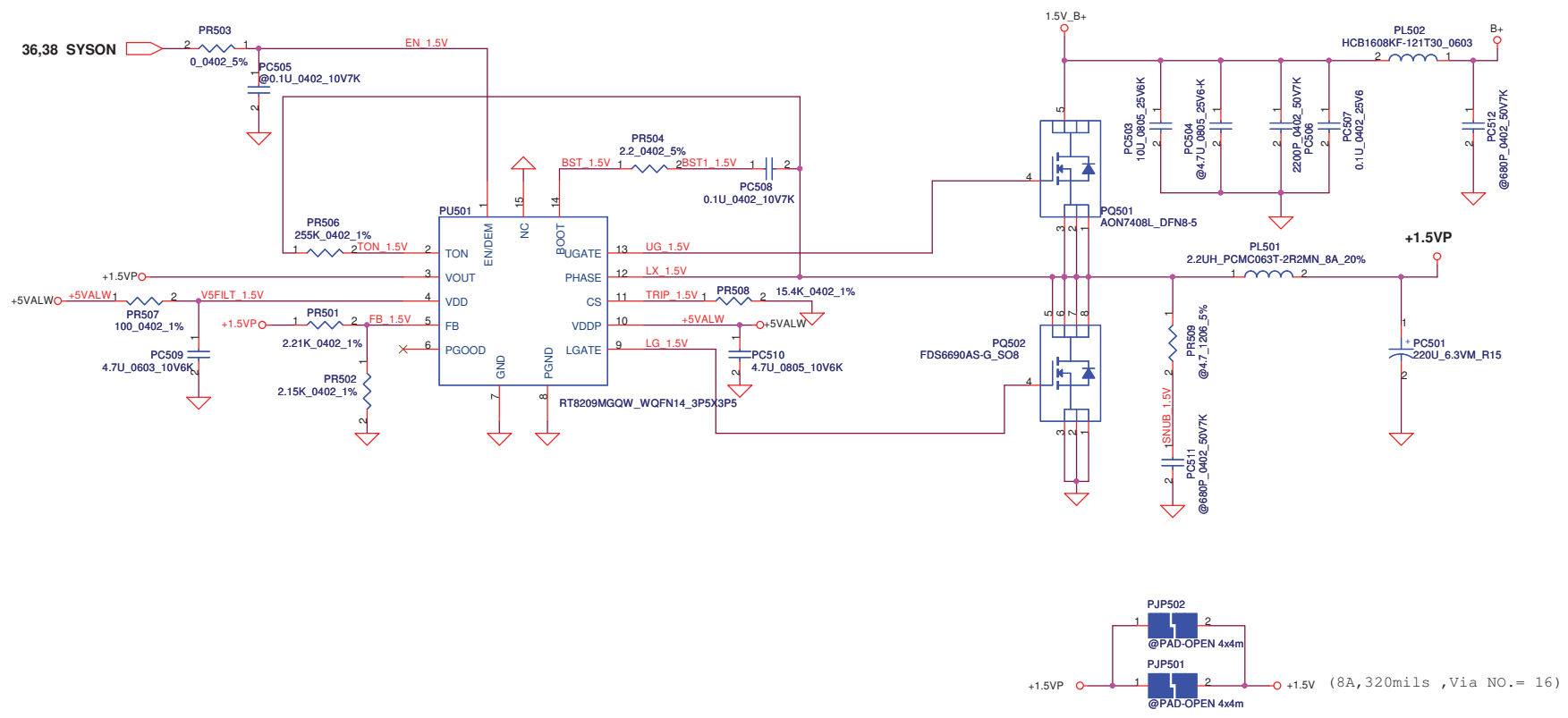
Title		
3.3VALWP/5VALWP		
Size	Document Number	Rev
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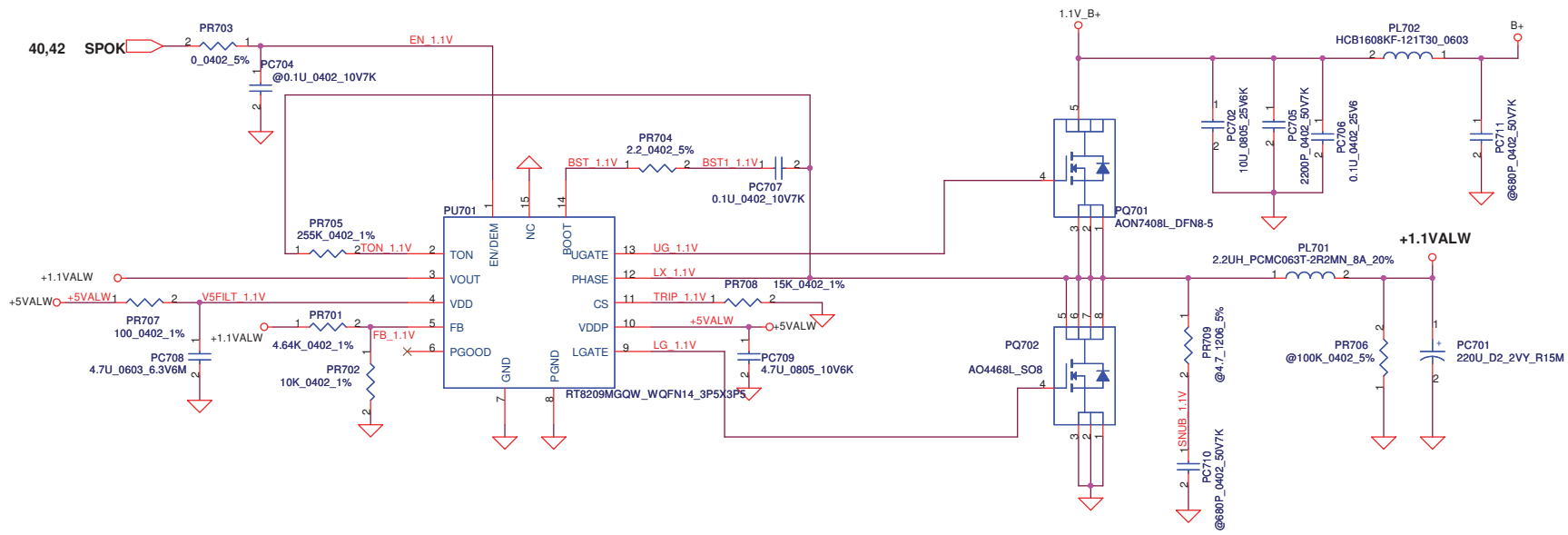
<Vo=1.8V> VFB=0.6V
 $V_o = V_{FB} * (1 + PR401/PR402) = 0.6 * (1 + 20K/10K) = 1.8V$



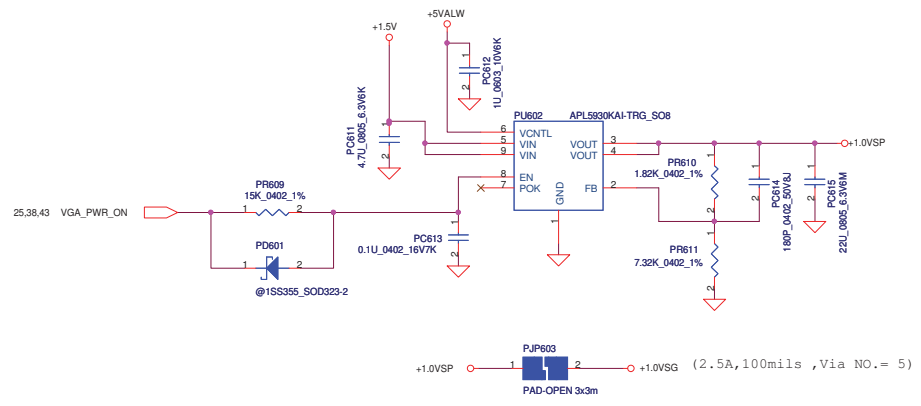
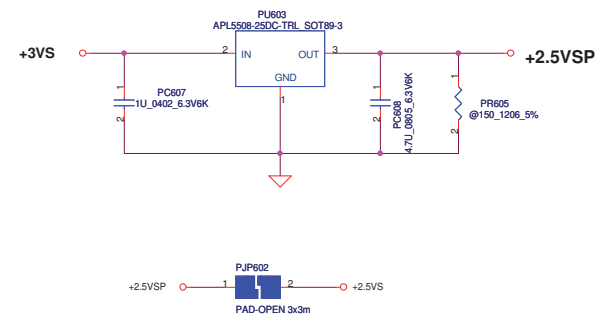
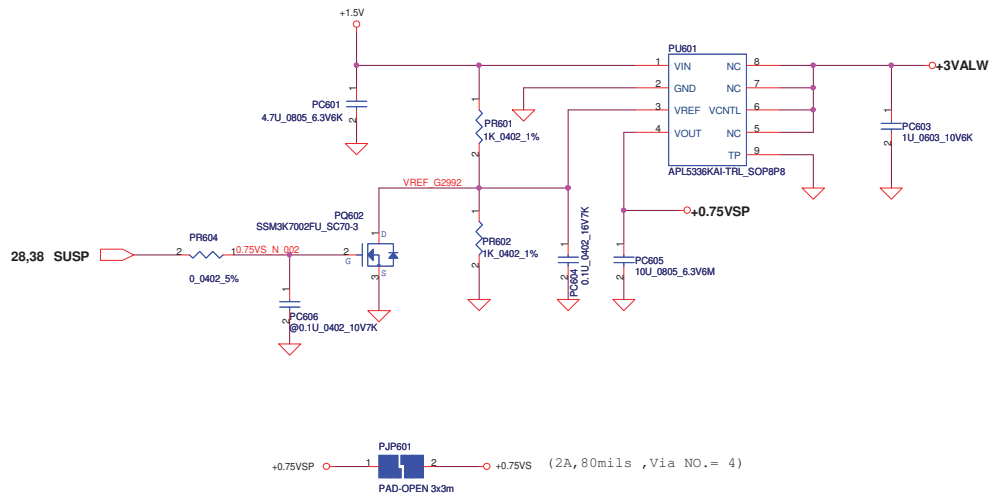
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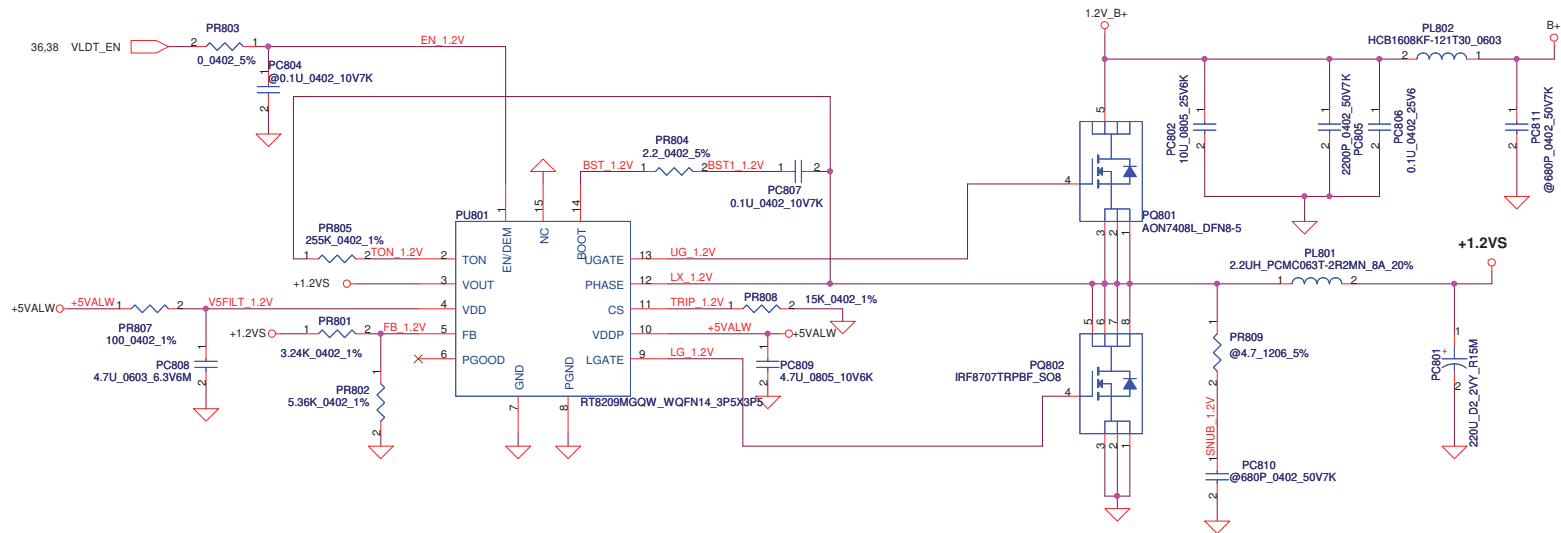
Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	+1.5VP	
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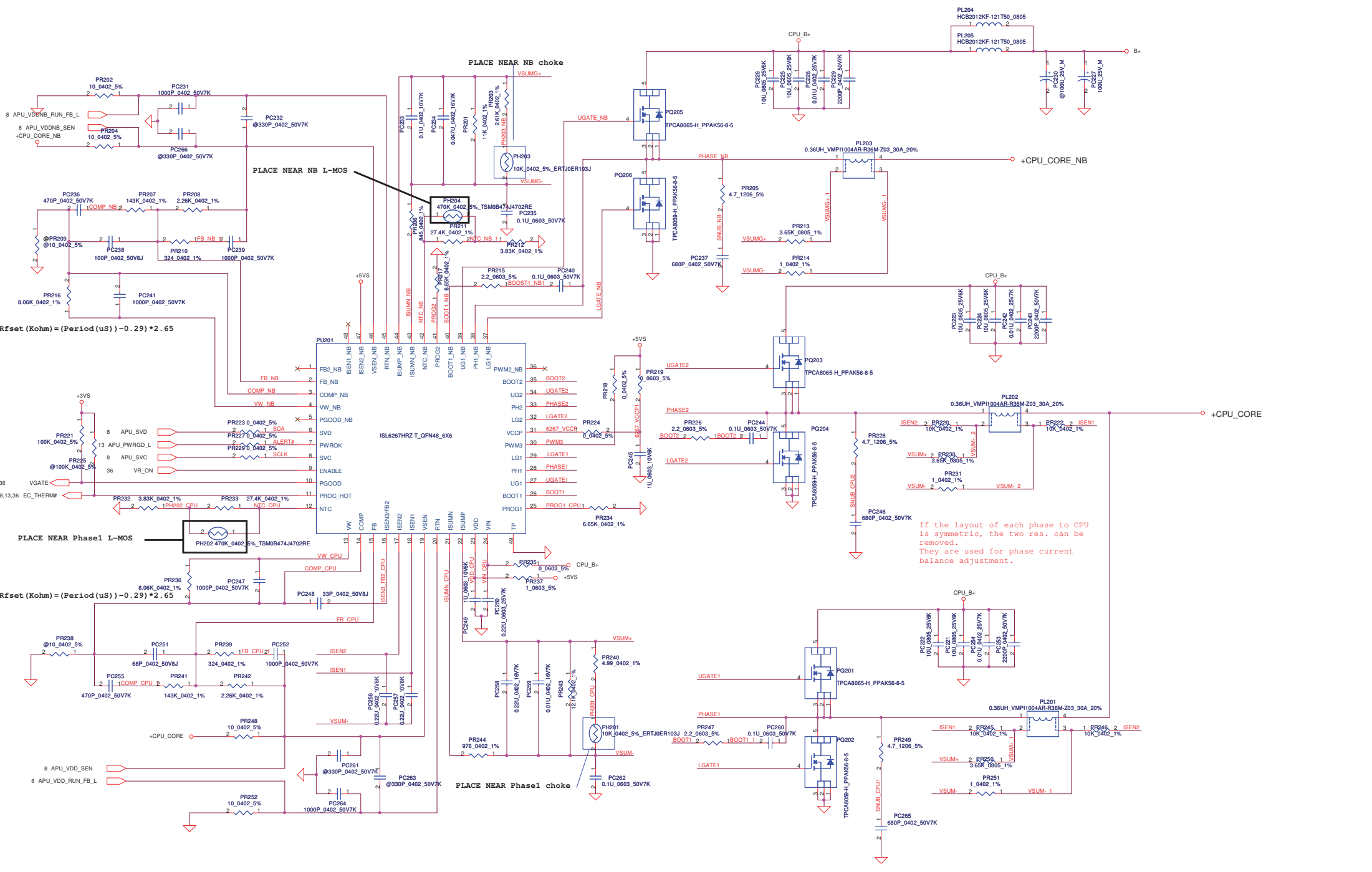
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR+1.1VALWP
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				Date:	Tuesday, February 22, 2011
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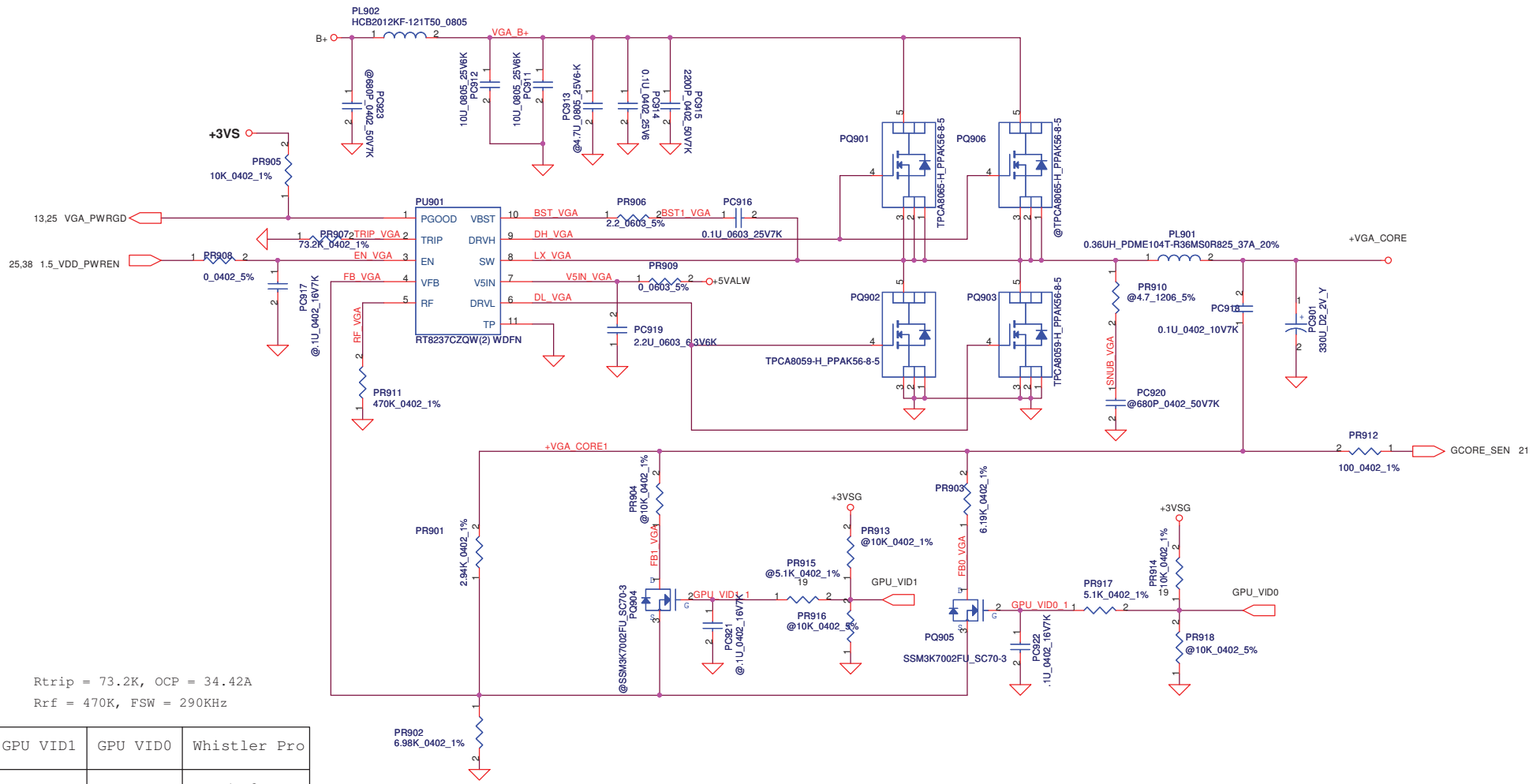


$$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$$

$$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$$

If the layout of each phase to CPU is symmetric, the two res. can be removed. They are used for phase current balance adjustment.

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Rtrip = 73.2K, OCP = 34.42A
 Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

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