

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

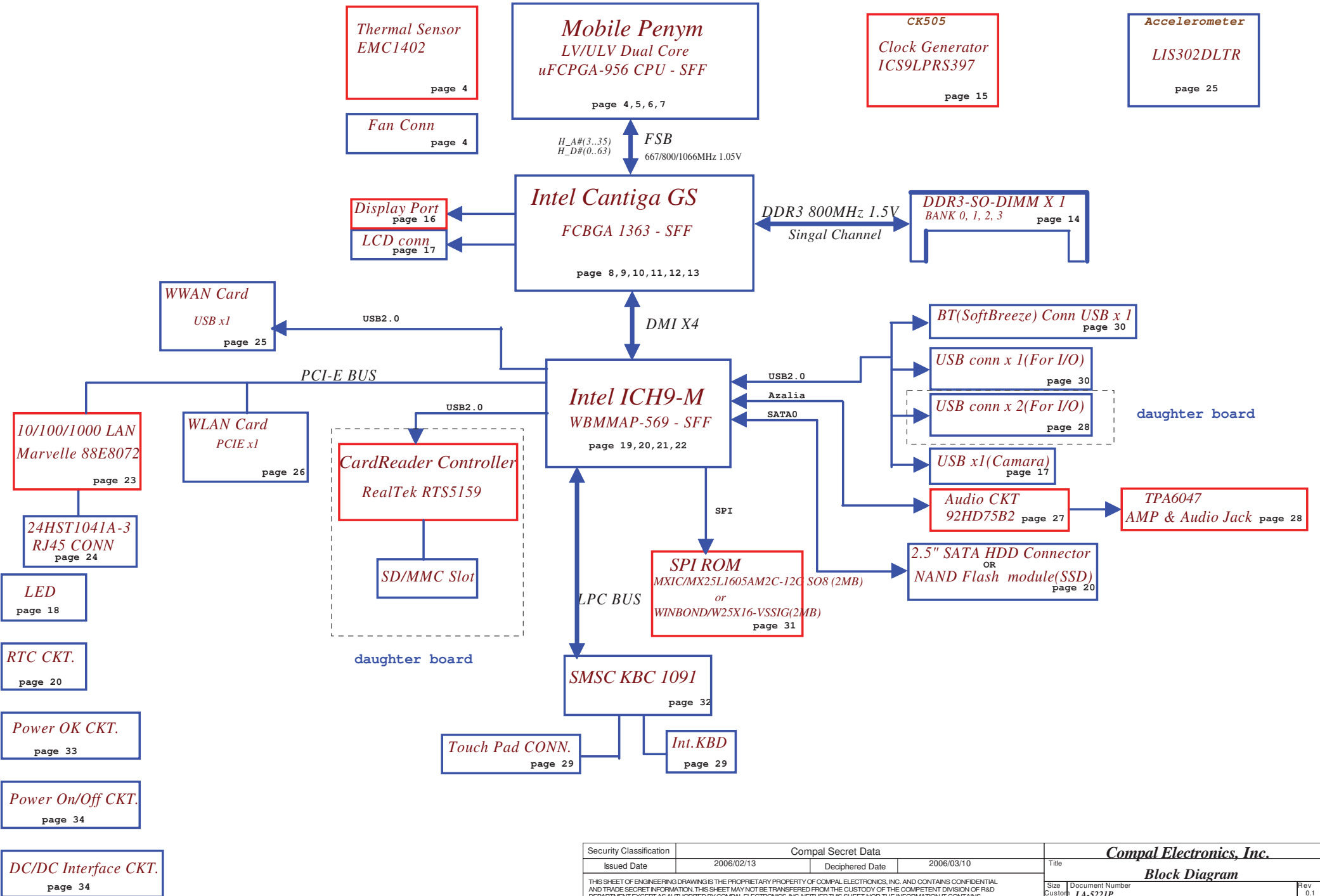
Fossil

2009-02-03

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	產出人員	
	產出日期	
	解密日期	

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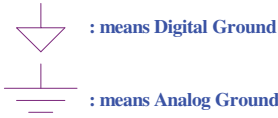
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Title			Block Diagram	
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+B +3VL	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
 CONN@ : means ME part.
 45@ : means install after SMT.

ULV723@ mean CPU ULV723 (U1) for L01
 SU9300@ mean CPU SU9300 (U1) for L02



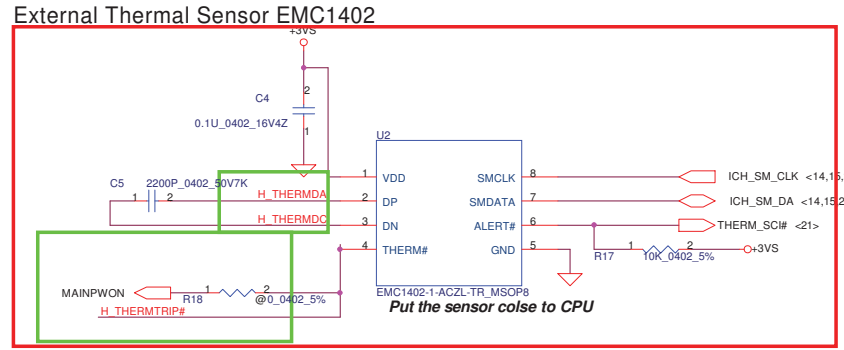
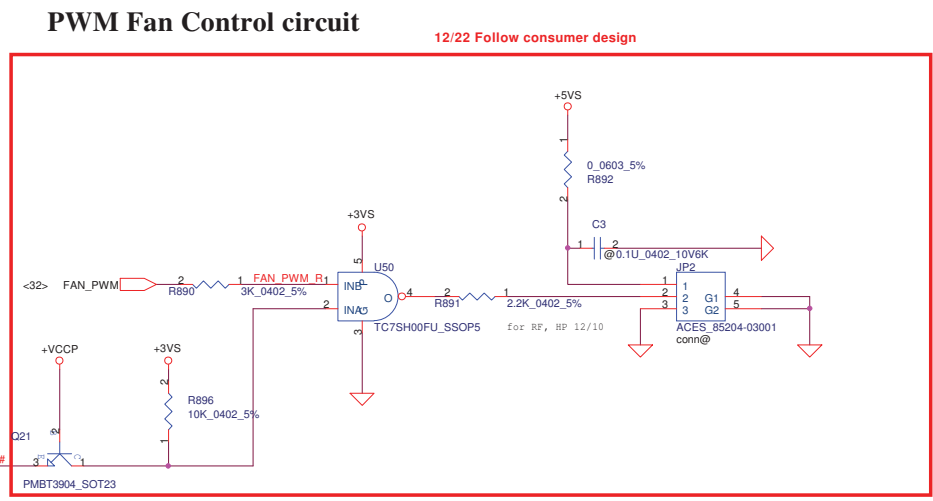
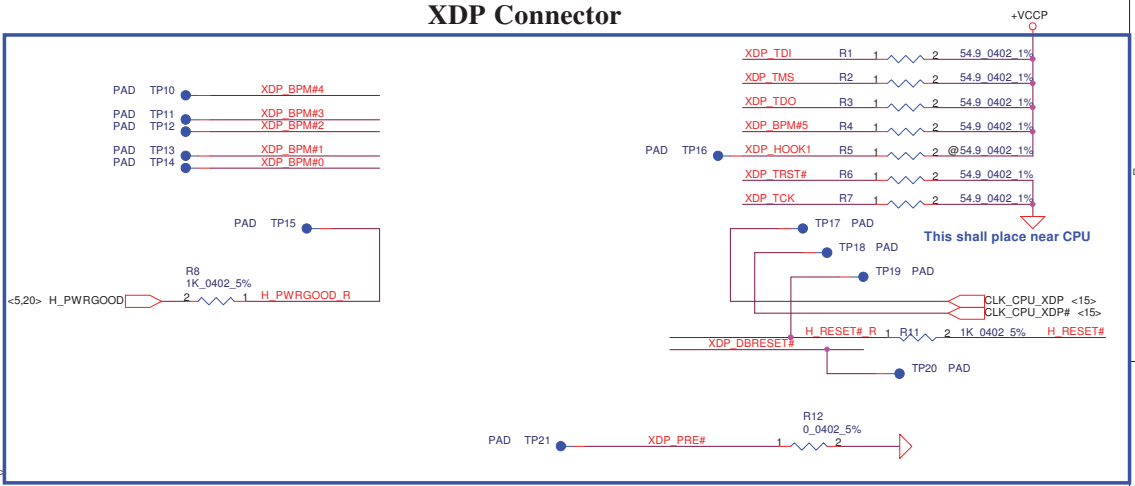
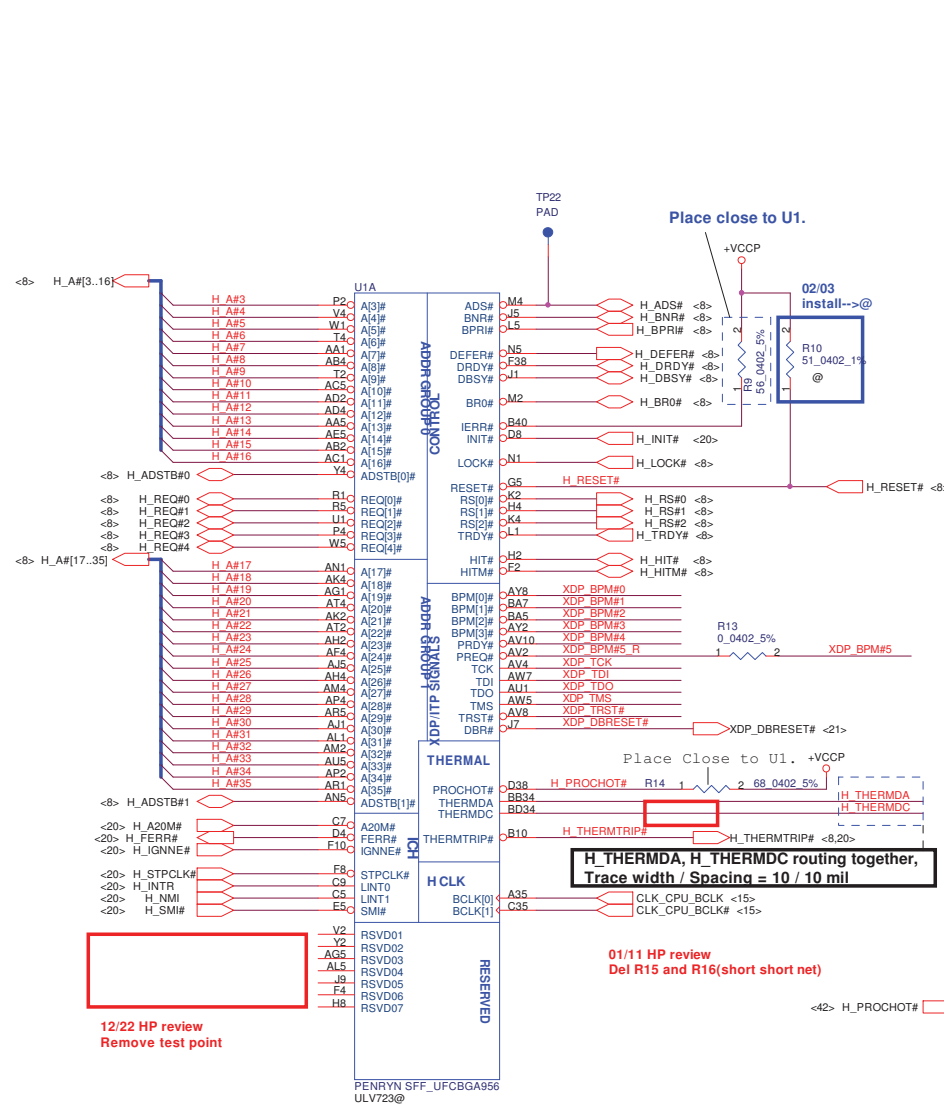
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

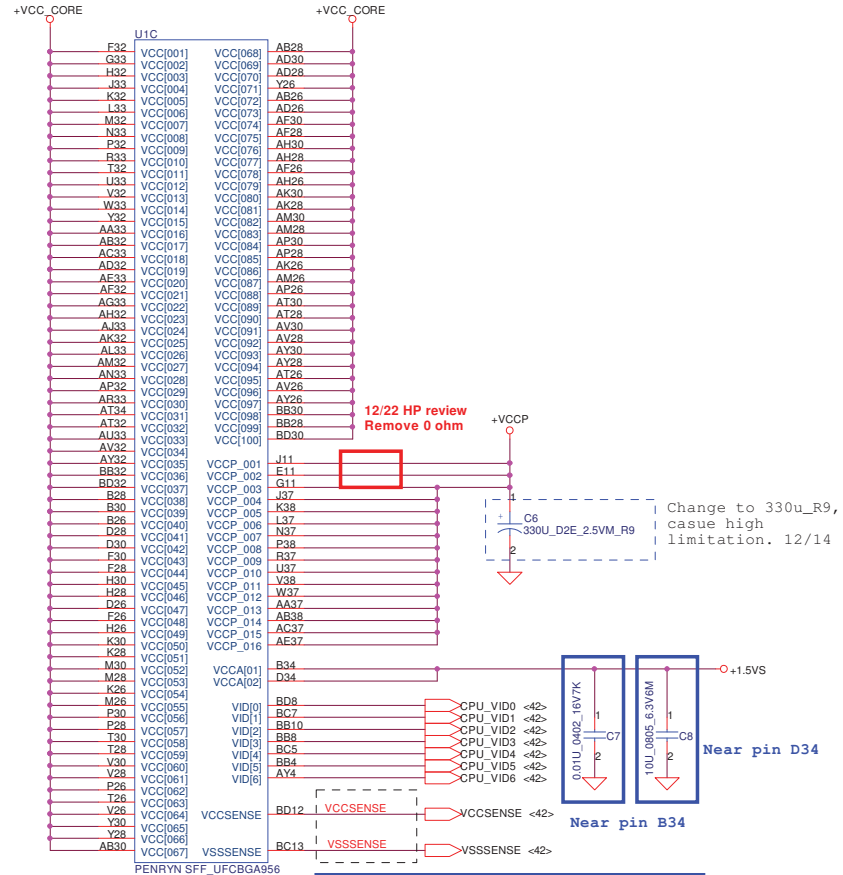
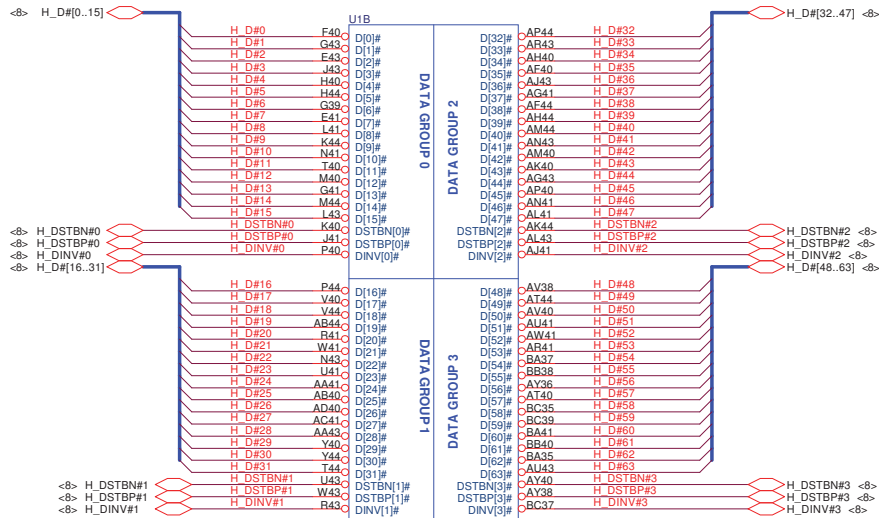
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

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12/17 HP review
Remove test point

12/22 HP review
Remove test point

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

12/22 HP review
Remove 0 ohm

Change to 330u_R9, casue high limitation. 12/14

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

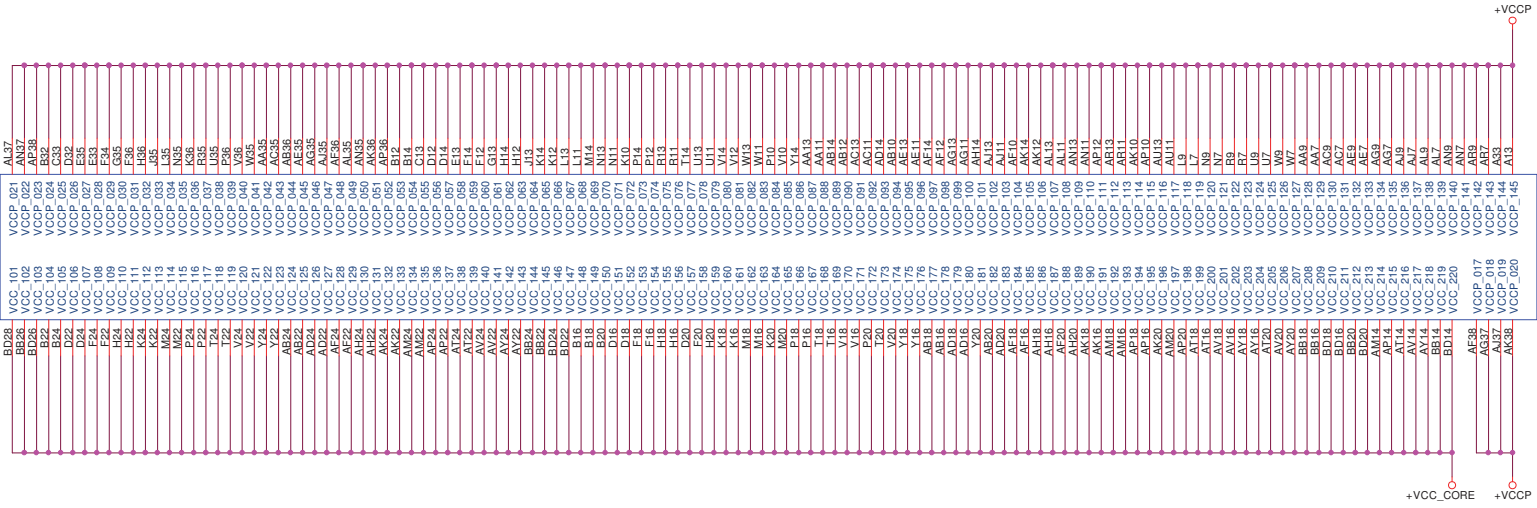
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Close to CPU pin AW43 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

Close to CPU pin within 500mils.

ULV723@



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U1D	U1E	U1E
B42	VSS001	AM36
F44	VSS002	AR35
D44	VSS003	AJ05
D42	VSS004	AV34
F42	VSS005	AW35
H42	VSS006	AW33
K42	VSS007	AT36
M42	VSS008	AT36
P42	VSS009	AV36
T42	VSS010	BA33
Y42	VSS011	BB33
Y42	VSS012	BB36
AB42	VSS013	BD36
AD42	VSS014	C27
AF42	VSS015	C29
AH42	VSS016	C31
AK42	VSS017	E29
AM42	VSS018	E27
AP42	VSS019	W25
AY42	VSS020	G27
AV44	VSS021	E31
AT42	VSS022	G31
AV42	VSS023	J29
BA42	VSS024	L29
BB42	VSS025	L27
C42	VSS026	N29
G42	VSS027	AE25
H38	VSS028	J31
I38	VSS029	L31
J38	VSS030	N31
L38	VSS031	AG23
M38	VSS032	R27
N38	VSS033	AG21
R38	VSS034	U29
T38	VSS035	U27
U38	VSS036	AJ21
W39	VSS037	U31
Y38	VSS038	W29
Y42	VSS039	W27
AC39	VSS040	AA29
AD38	VSS041	AA27
AE39	VSS042	AA25
AG39	VSS043	AC29
AH38	VSS044	AC27
AJ39	VSS045	AC25
AL39	VSS046	AC23
AM38	VSS047	AC21
AN39	VSS048	AE27
AR39	VSS049	AE25
AR37	VSS050	AG27
AT38	VSS051	AJ29
AU39	VSS052	AJ27
AU37	VSS053	AE31
AW39	VSS054	AG31
AW37	VSS055	AJ31
BA39	VSS056	AL29
BC41	VSS057	AL27
BD40	VSS058	AN29
BD38	VSS059	AN27
B36	VSS060	AL31
D36	VSS061	AN31
H34	VSS062	AR27
M34	VSS063	AR25
M36	VSS064	AR23
P34	VSS065	AR21
T34	VSS066	AW27
Y34	VSS067	AW25
Y36	VSS068	AW23
AB34	VSS069	AU31
AD34	VSS070	AW31
AF34	VSS071	BA29
AH34	VSS072	BA27
AJ34	VSS073	BA25
AK34	VSS074	BA23
AM34	VSS075	BA21
AP34	VSS076	BA19
	VSS077	BA17
	VSS078	BA15
	VSS079	BA13
	VSS080	BA11
	VSS081	BA09
	VSS162	E21
	VSS163	E21

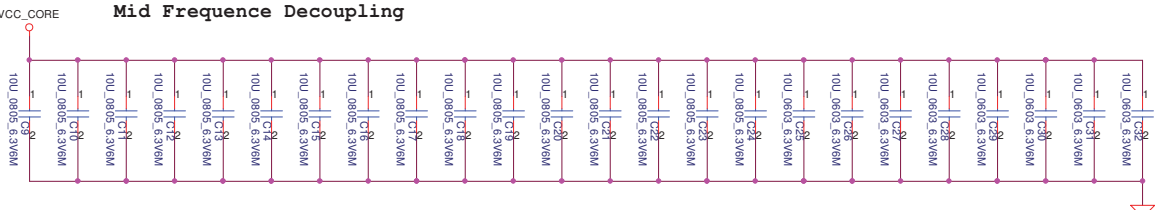
PENRYN SFF_UFCBGA956

ULV723@

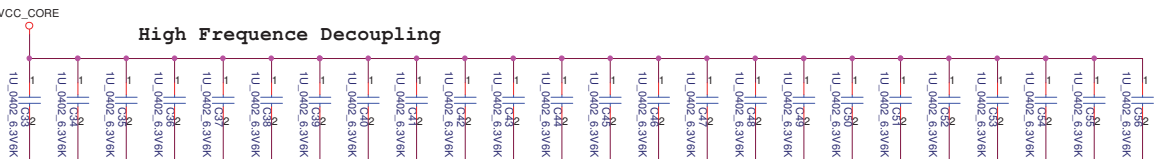
PENRYN SFF_UFCBGA956

ULV723@

Mid Frequency Decoupling



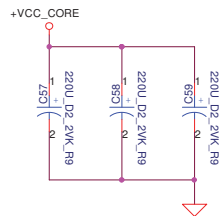
High Frequency Decoupling



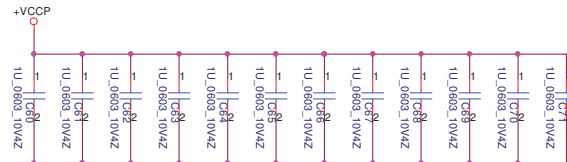
6/14 :Replace 12pcs 10uF_0805 to 24 pcs 1uF_0402 for CPU transient fail issue.

ESR <= 1.5m ohm

Near CPU CORE regulator

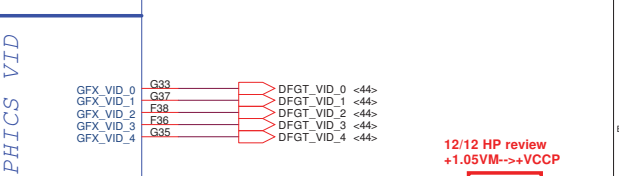
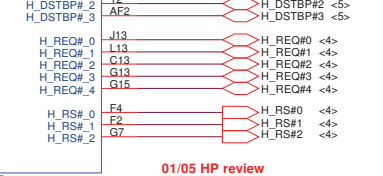
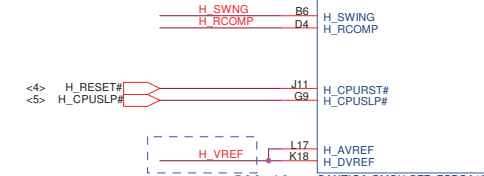
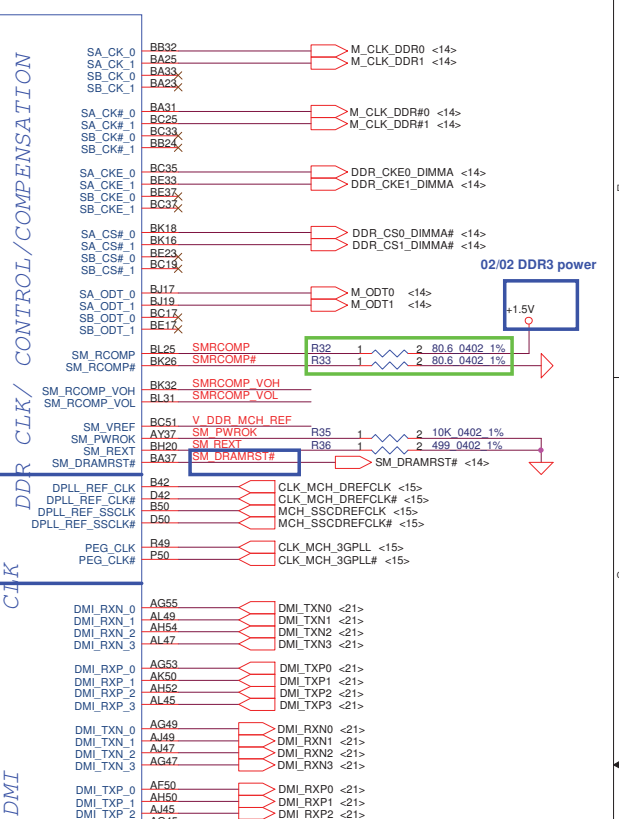
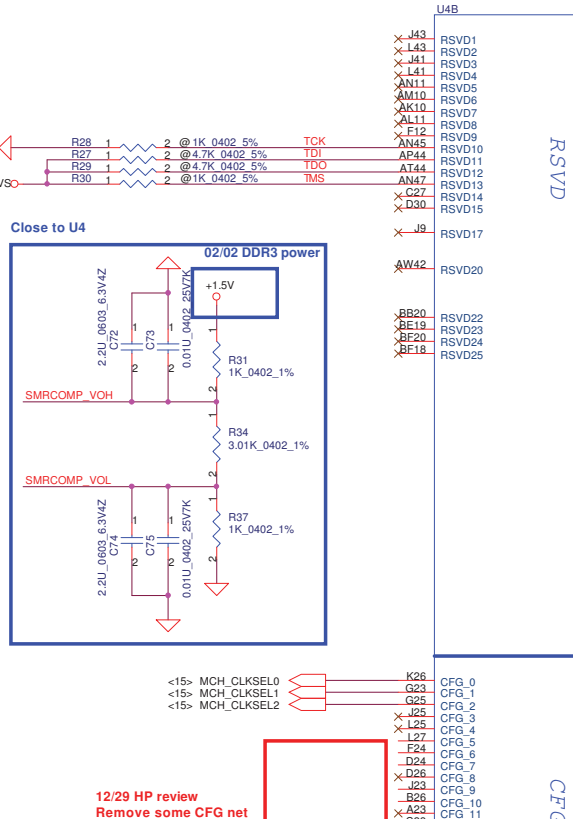
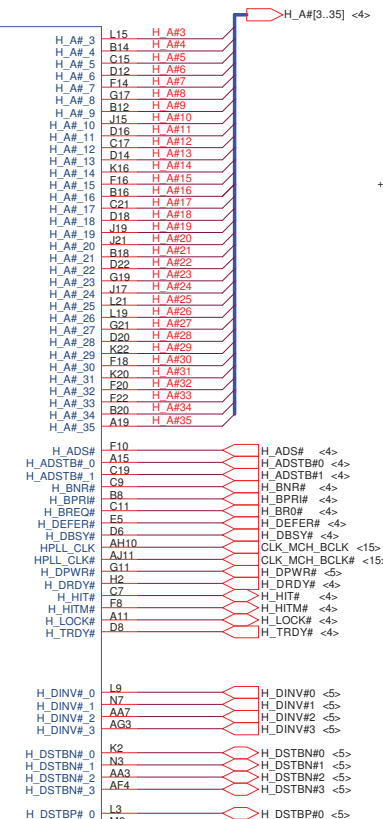
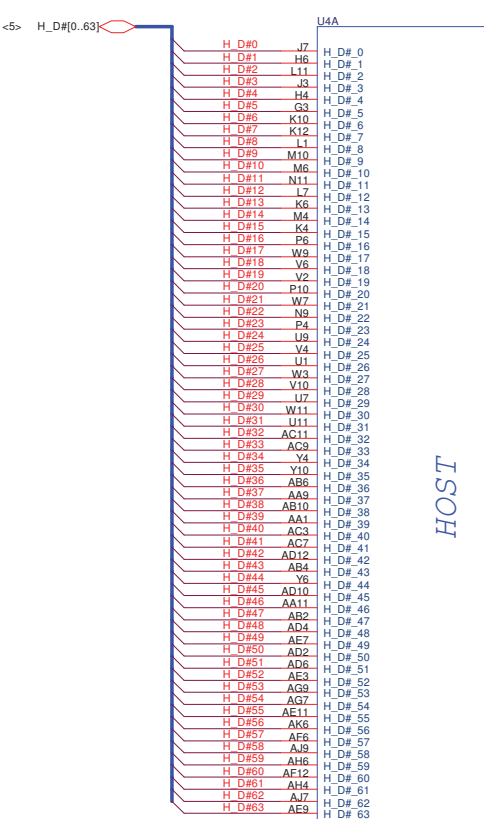


Del C37 to improve power plan. 6/14



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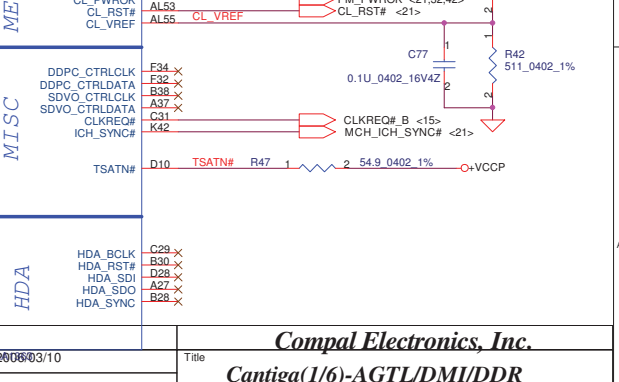
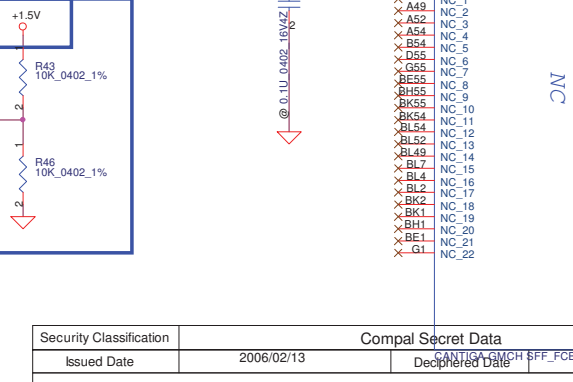
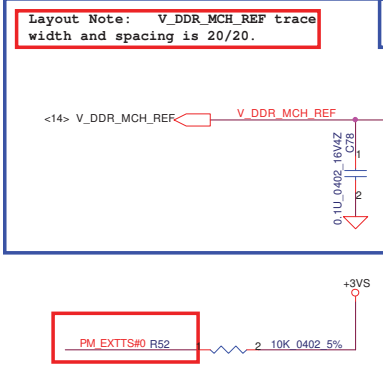
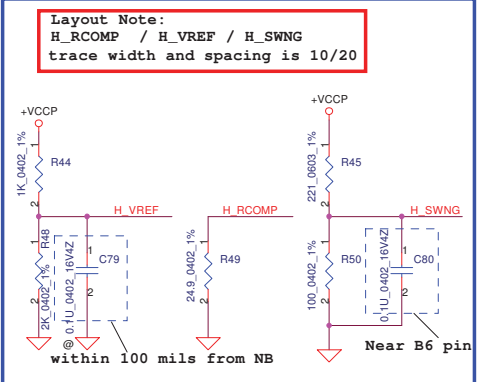


layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

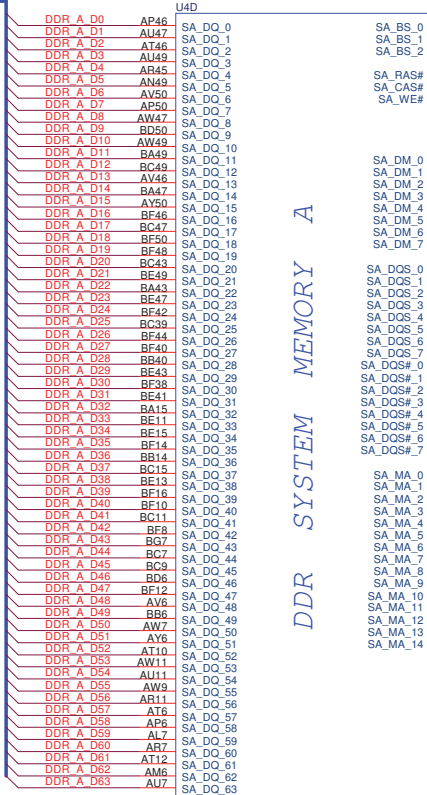
layout note:
Place them close to U4 pin BC51.

layout note:
Add R428 in 9/26

layout note:
12/12 HP review +1.05V-->+VCCP

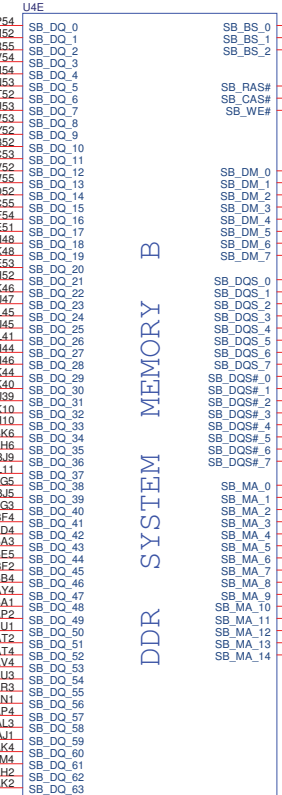
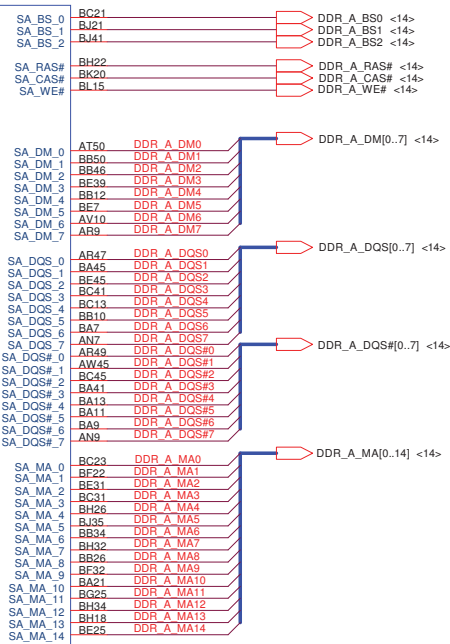


<14> DDR_A_D[0..63]



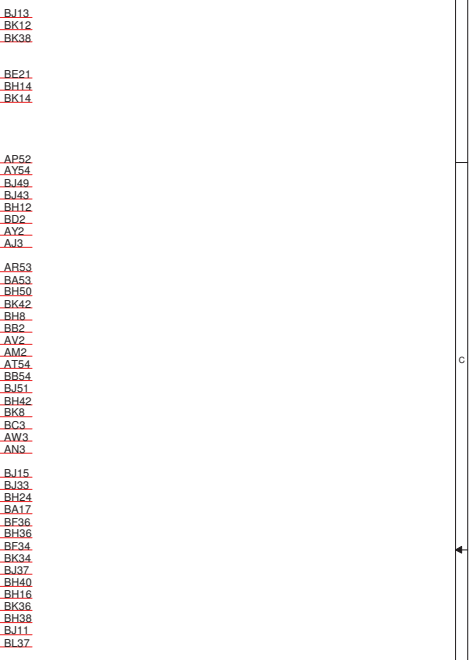
DDR SYSTEM MEMORY A

CANTIGA GMCH SFF_FCBGA1363



DDR SYSTEM MEMORY B

CANTIGA GMCH SFF_FCBGA1363

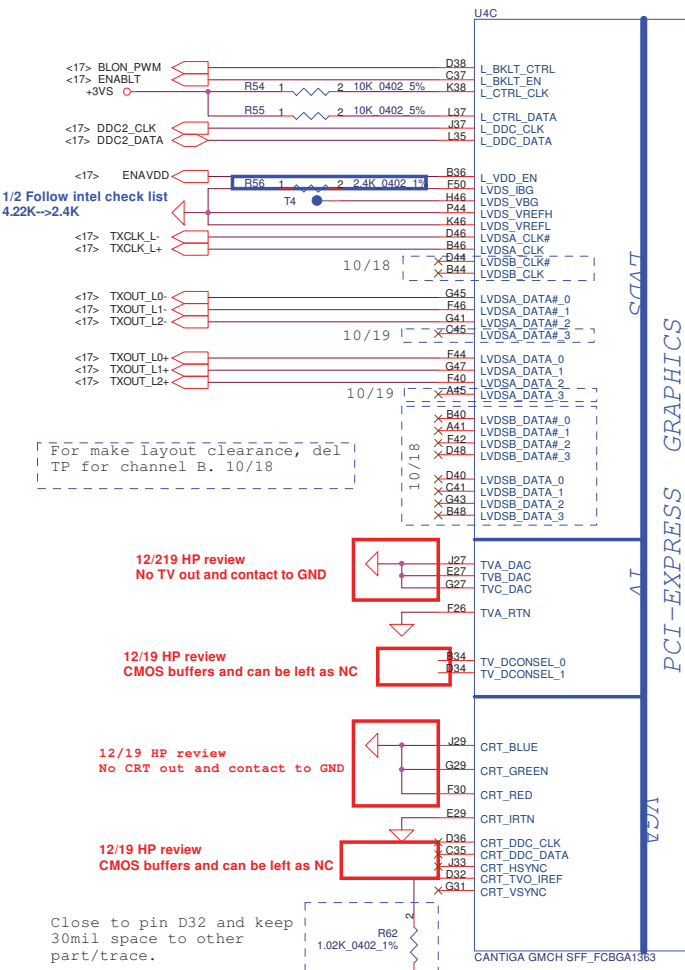


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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

Place R53 <500mils to U4 pin U45&T44.



1/2 Follow intel check list 4.22K->2.4K

For make layout clearance, del TP for channel B. 10/18

12/19 HP review
No TV out and contact to GND

12/19 HP review
CMOS buffers and can be left as NC

12/19 HP review
No CRT out and contact to GND

12/19 HP review
CMOS buffers and can be left as NC

Close to pin D32 and keep 30mil space to other part/trace.

12/29 HP review
Remove some reserved R for CFG net



12/22 HP review
Pin J31 L31 contact to GND

12/24 HP review
Pin J31 L31 contact to GND

12/22 HP review
DPLLA contact with DPLLA PWR

12/22 HP review
Remove 0 ohm

12/17 HP review
+1.05VM-->+VCCP

12/17 HP review
Remove 0 ohm

12/17 HP review
Remove 0 ohm

POWER

852mA

Near AXF PIN

01/10 HP review
3VS_HV-->+3VS

12/22 HP review
+1.05VM-->+VCCP

9/27

12/12

12/22 HP review
+1.05VM-->+VCCP

12/22 HP review
+1.05VM-->+VCCP
Remove 0ohm

12/22 HP review
+1.05VM-->+VCCP
Remove 0ohm

12/22 HP review
+1.05VM-->+VCCP
Remove 0ohm

12/22 HP review
Remove 0 ohm

12/22 HP review
+1.05VM-->+VCCP

12/22 HP review
+1.5VS-->GND

12/22 HP review
Remove 0 ohm

12/22 HP review
+1.05VM-->+VCCP
Remove 0ohm

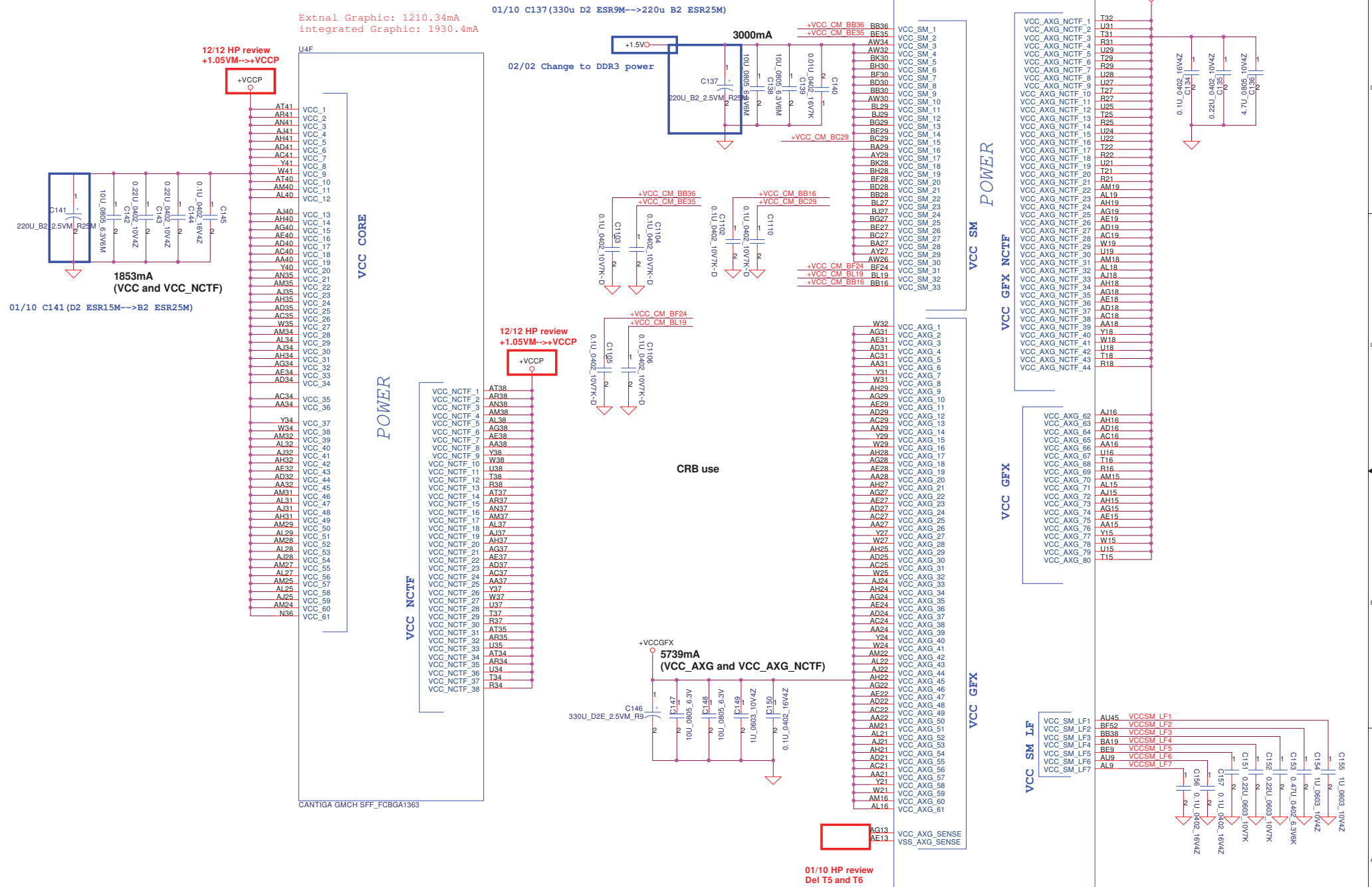
12/22 HP review
+1.05VM-->+VCCP

12/22 HP review
+1.05VM-->+VCCP
Remove 0ohm

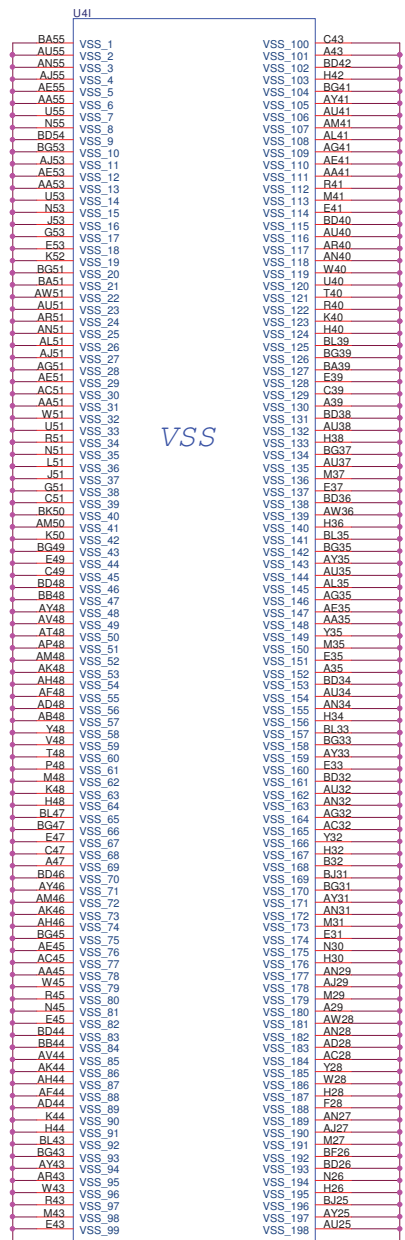
+VCCP_D

01/10 HP review
Del R75 0ohm and +3VS_HV-->+3VS

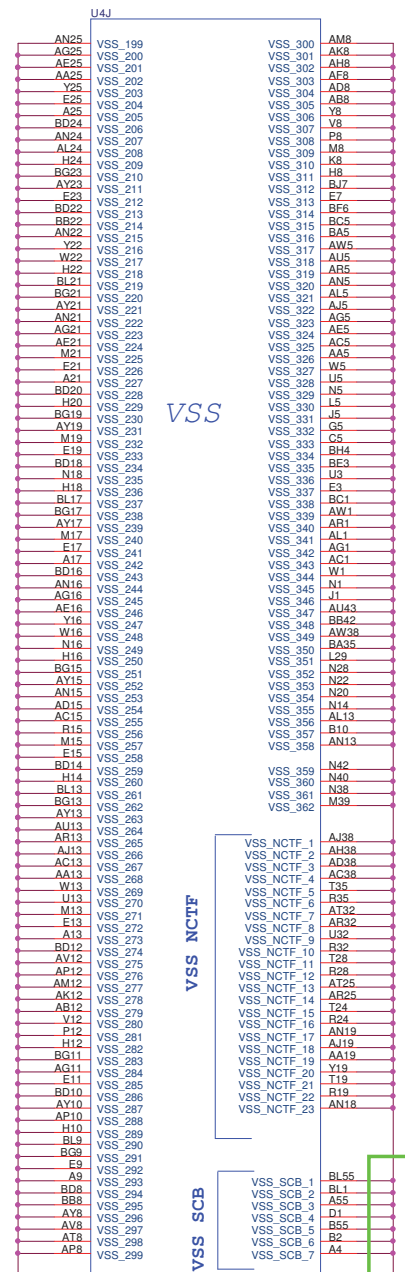
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				Cantiga(5/6)-PWR/GND
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VSS



VSS

VSS NCTF

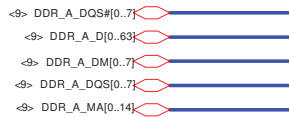
VSS SCB

2/12 FOR NO CRACK DETECT FUNCTION

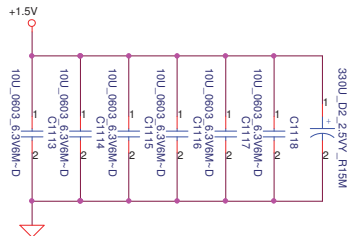
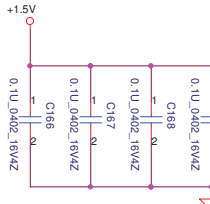


12/12 FOR NO CRACK DETECT FUNCTION

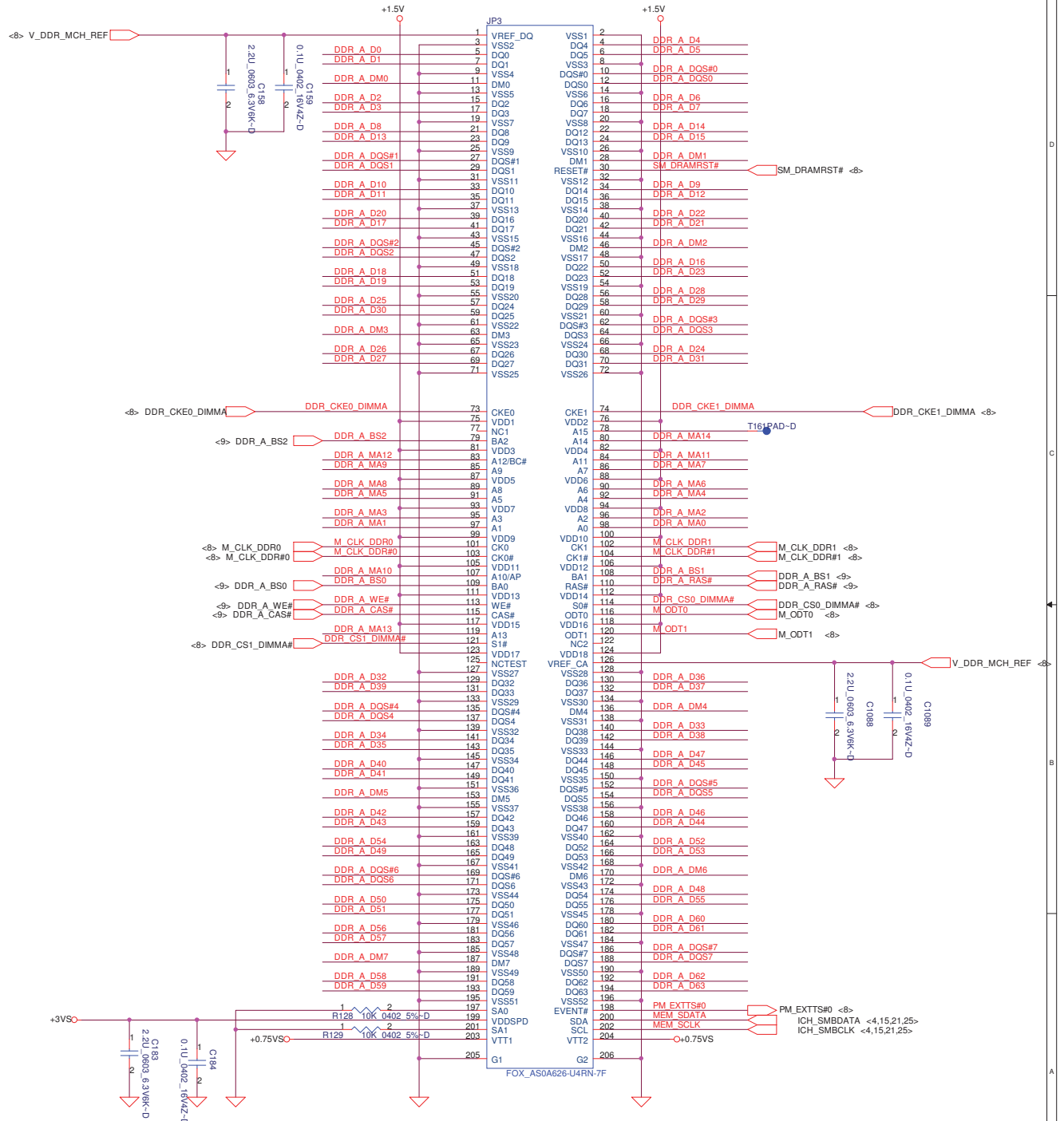
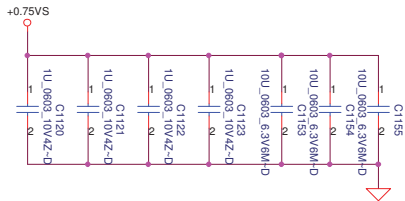
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Layout Note:
Place near JP3



Layout Note:
Place near JP3 203,204

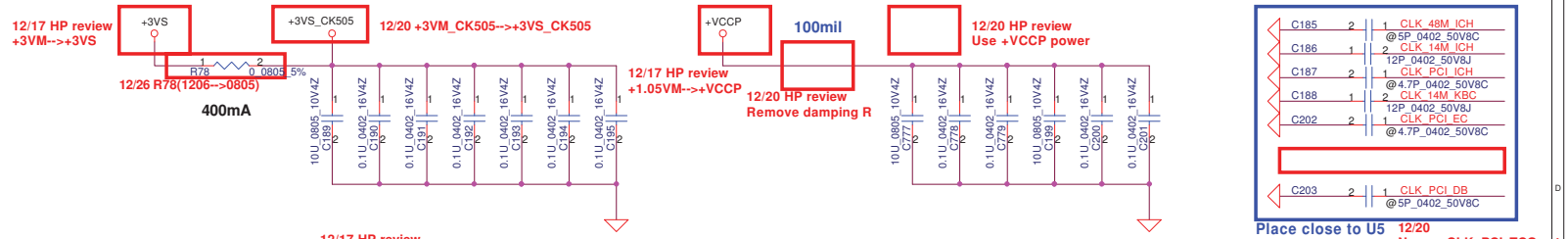


Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/03/10

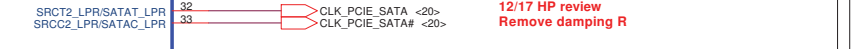
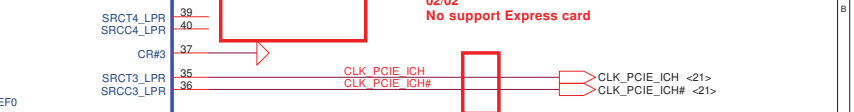
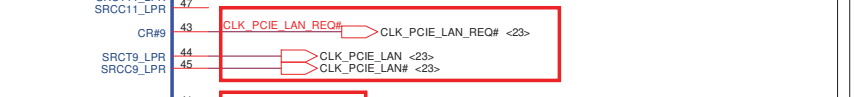
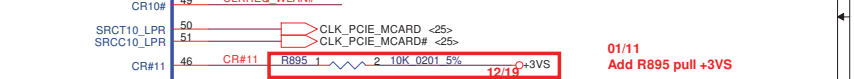
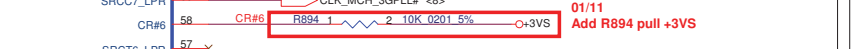
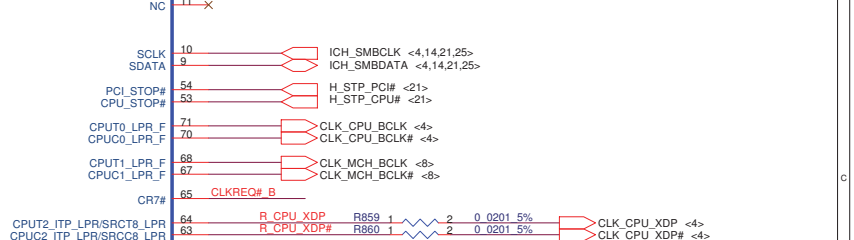
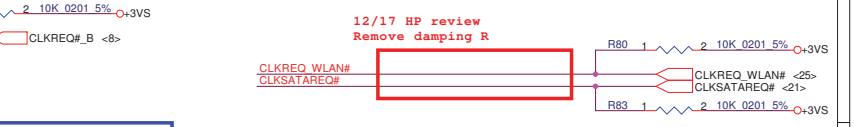
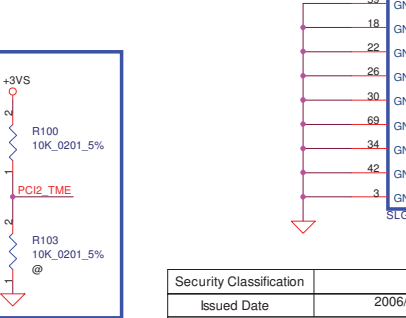
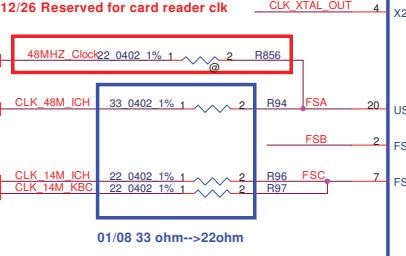
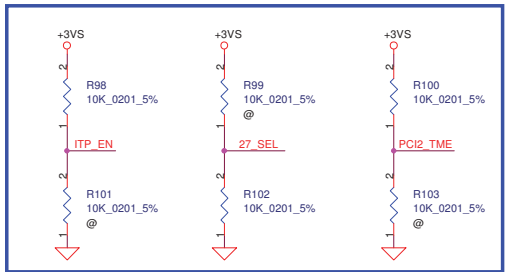
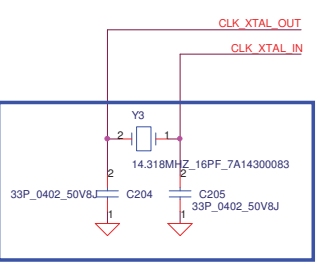
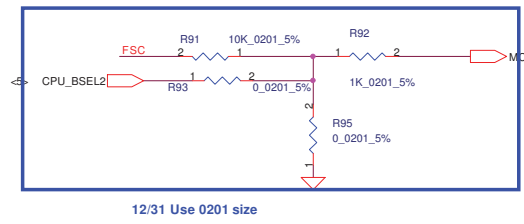
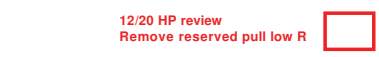
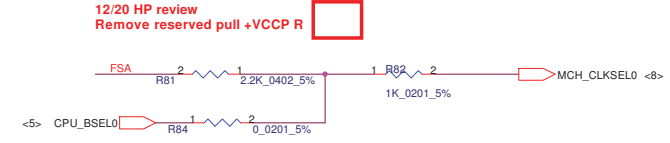
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Title			Compal Electronics, Inc.	
			DDRII-SODIMM SLOT	
Size	Document Number	Rev		
	LA-522IP	0.1		
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FSLC	FSLB	FSLA	CPU	FSB	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3

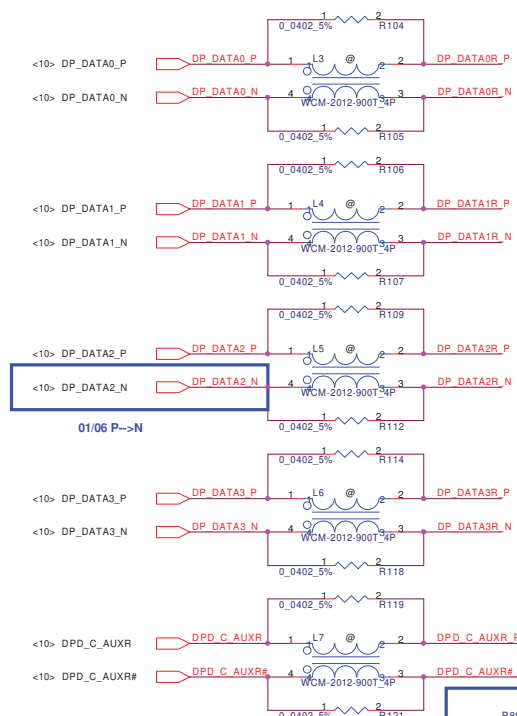


C185	2	1	CLK_48M_ICH	@5P_0402_50V8C
C186	1	2	CLK_14M_ICH	12P_0402_50V8J
C187	2	1	CLK_PCI_ICH	@4.7P_0402_50V8C
C188	1	2	CLK_14M_KBC	12P_0402_50V8J
C202	2	1	CLK_PCI_EC	@4.7P_0402_50V8C
C203	2	1	CLK_PCI_DB	@5P_0402_50V8C

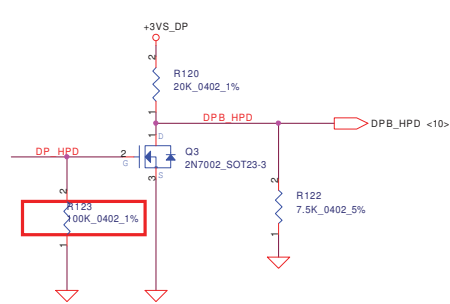
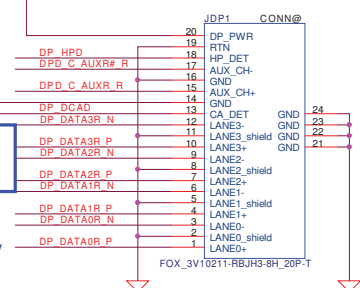
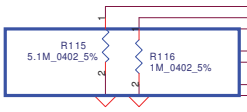
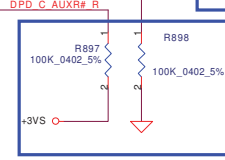
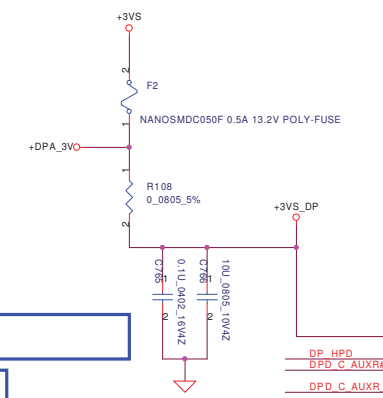
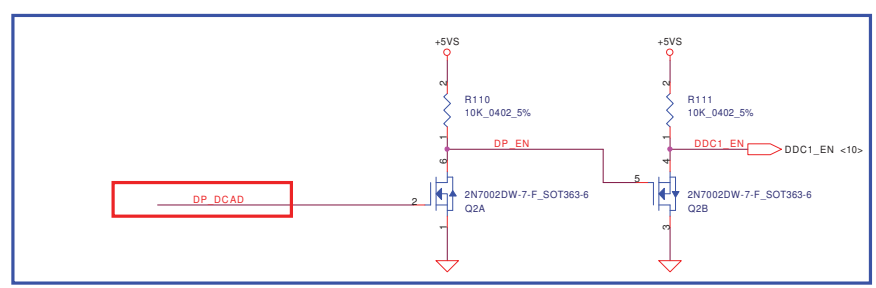


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				CLOCK GENERATOR
Size		Document Number	Rev	
		LA-5221P	0.1	
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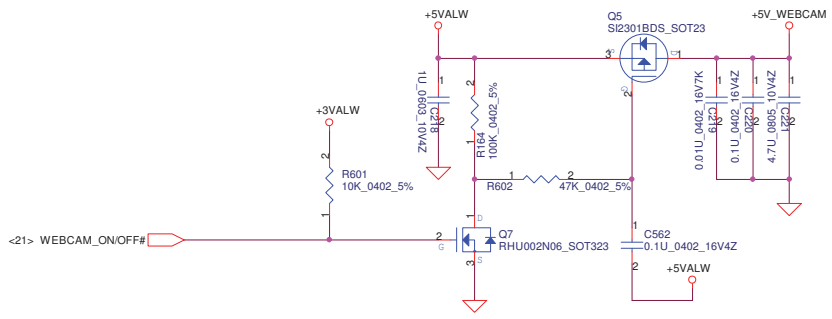
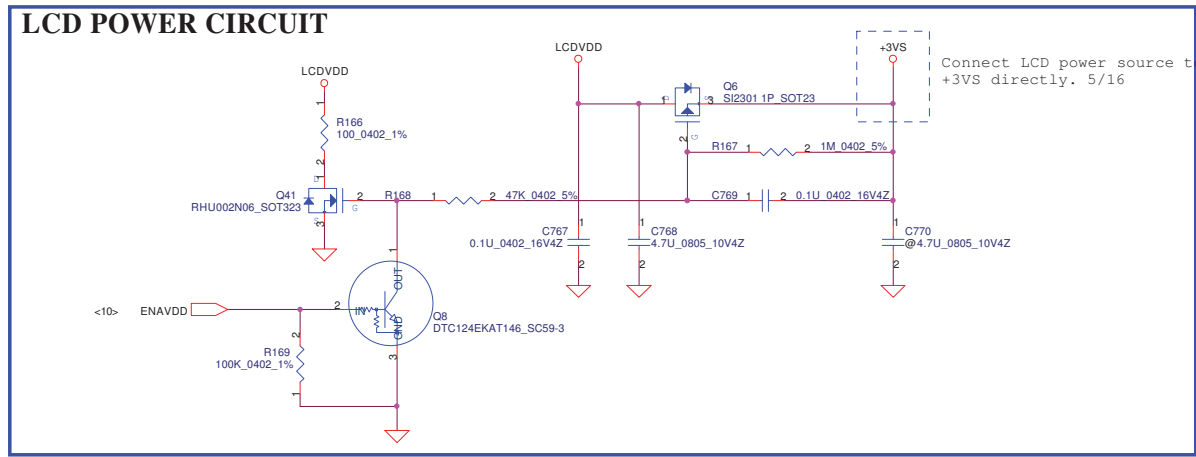
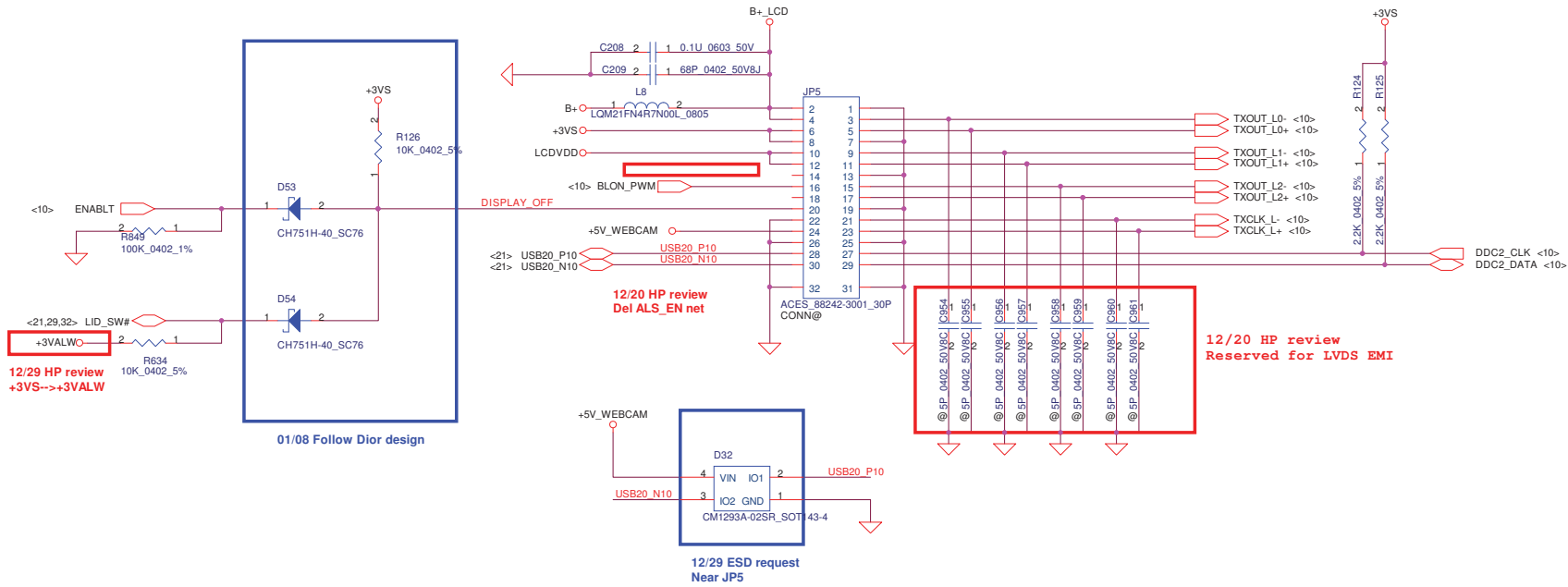


01/12
Del reserved ESD part, because M/B no more space

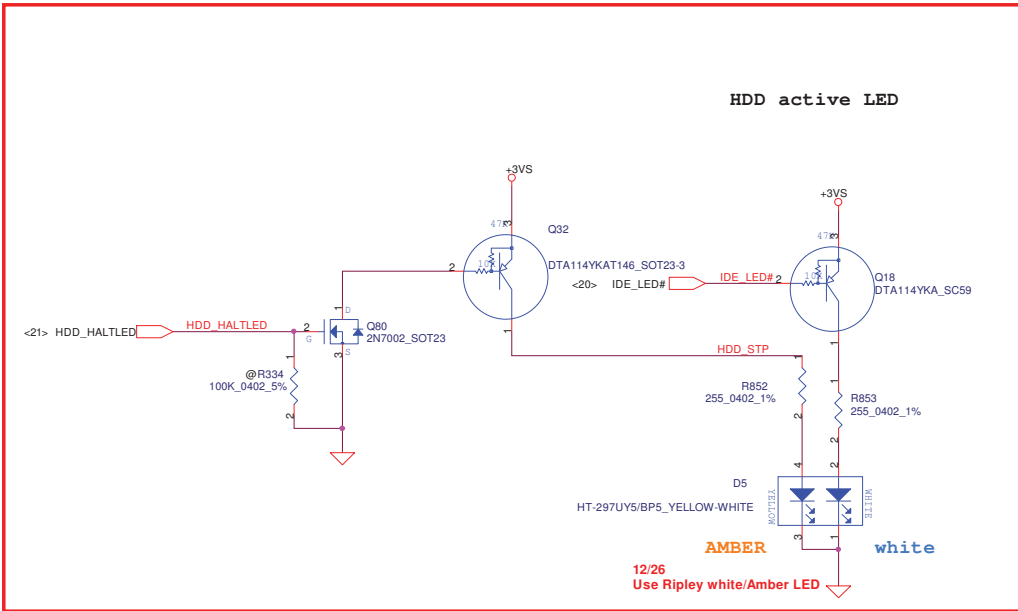


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Size	Document Number	Date		Rev
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LED/PANEL BD. CONN.

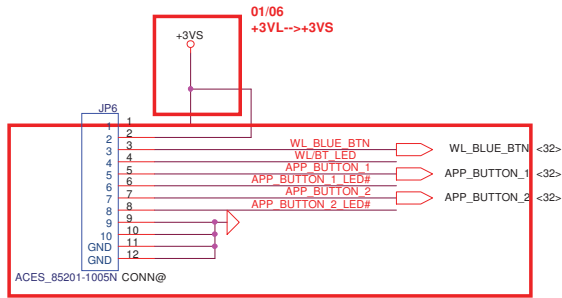


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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc.
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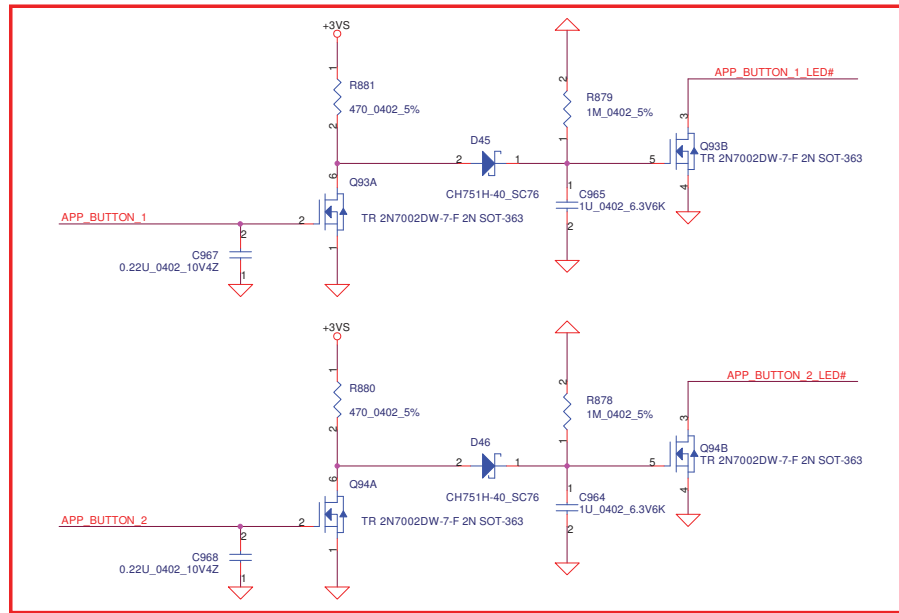
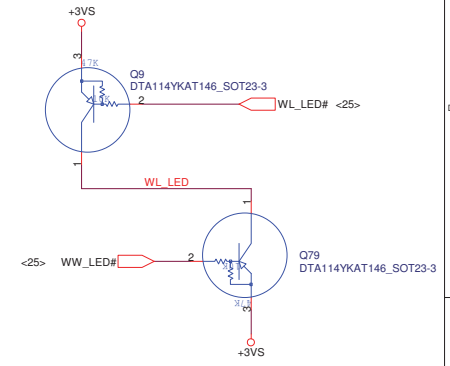
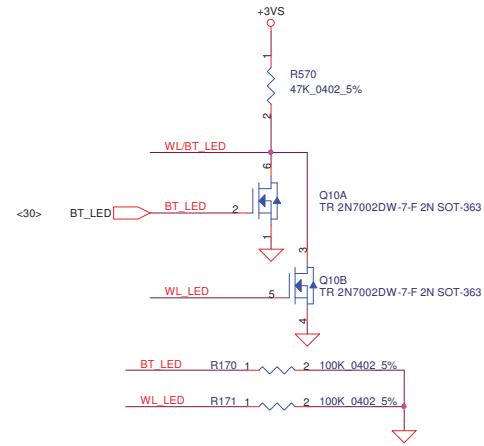


12/26
Modify HD LED control(follow sky)

To LED small board



12/26
Power LED on small board

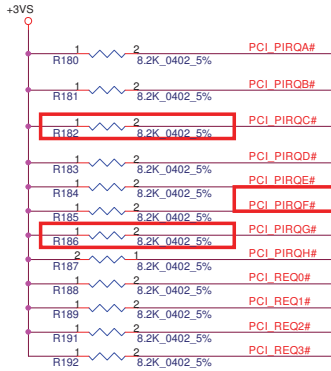
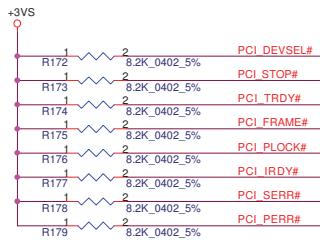


12/26
LID switch on small board



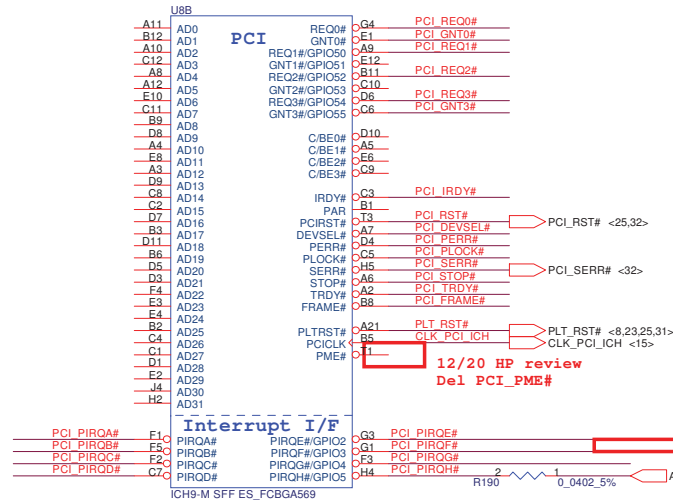
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Issued Date	2006/02/13	Deciphered Date	2006/03/10
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LEDS & LID		
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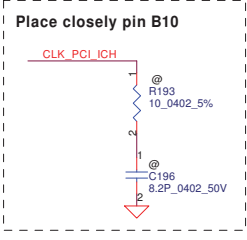


01/13 HP review
Add R182 and R186

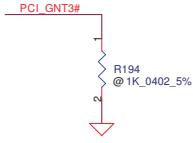
12/20 HP review
Update net (No ODD_DET#)



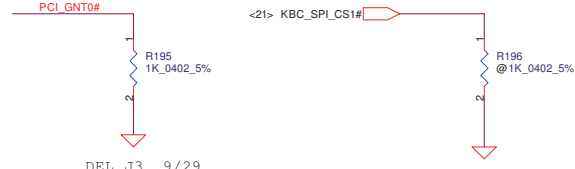
12/20 HP review
Update net (No ODD_DET#)



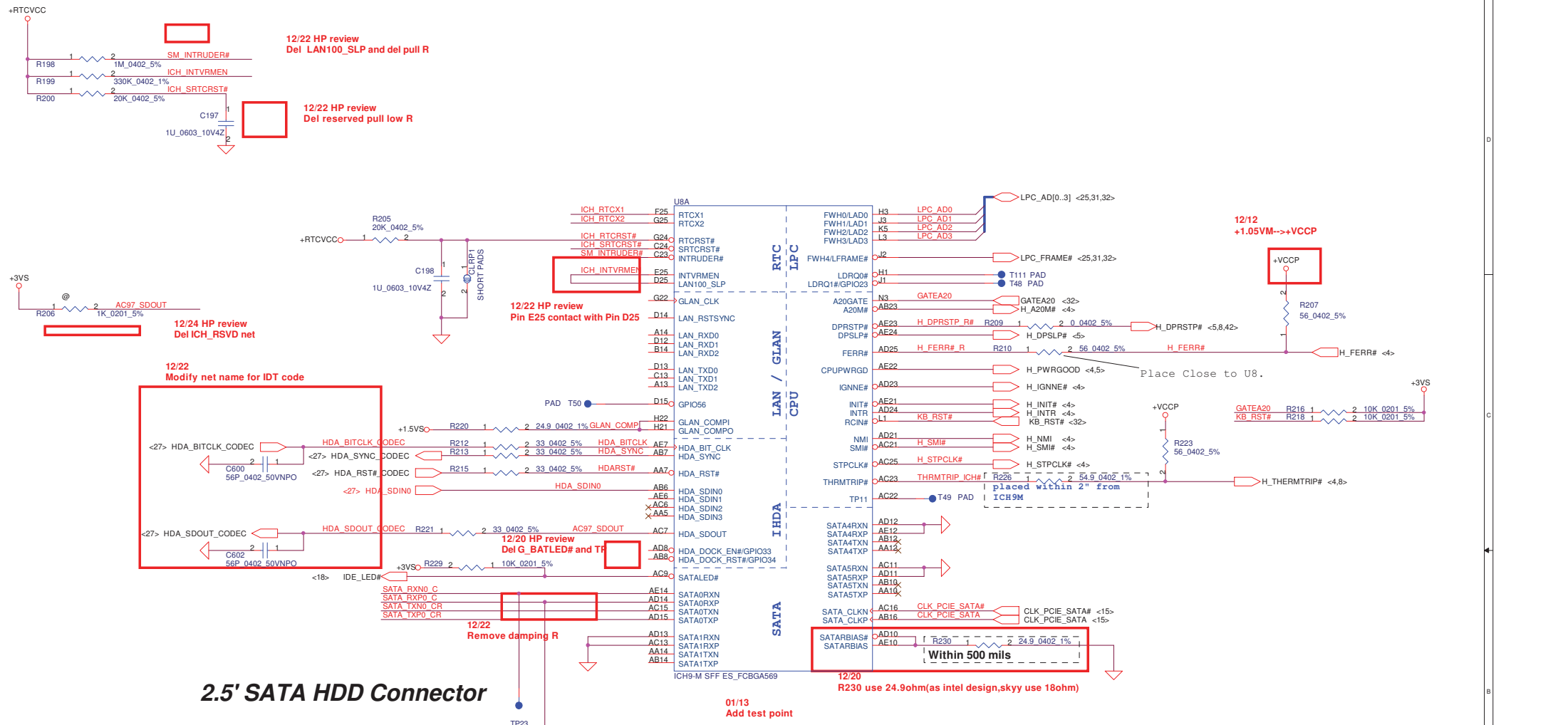
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



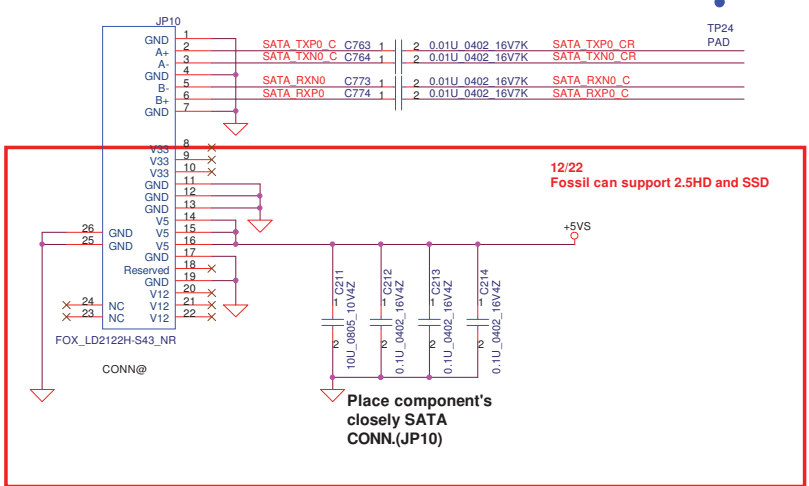
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



DEL J3. 9/29

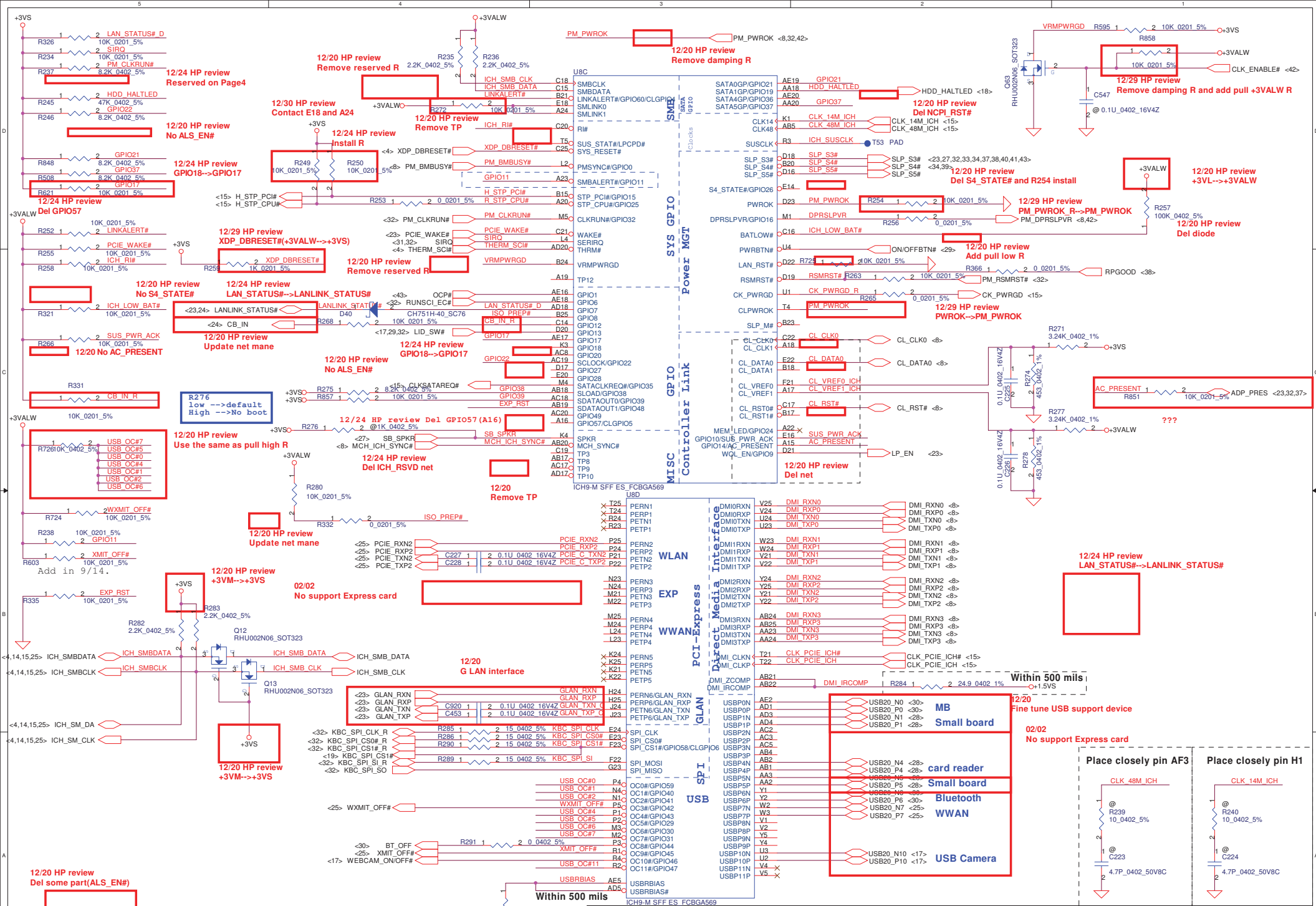


2.5' SATA HDD Connector



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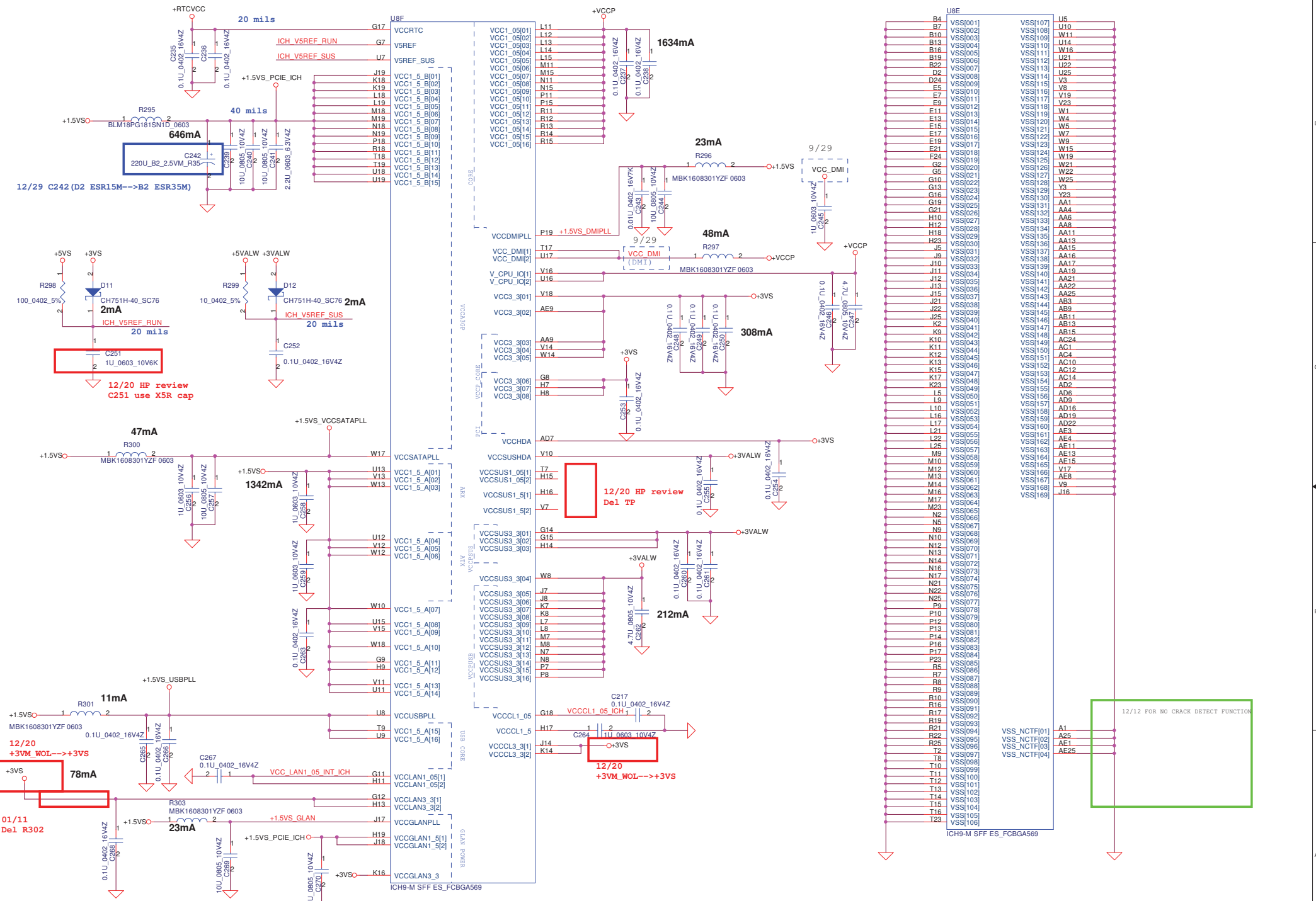
Compal Electronics, Inc.			
Title ICH9(2/4) LAN,HD,IDE,LPC			
Size	Document Number	Rev	
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Title: ICH9(3/4) DMI,USB,GPIO,PCIE	
Size: Custom	Document Number: LA-5221P
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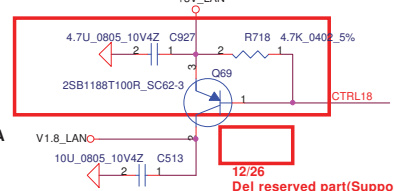
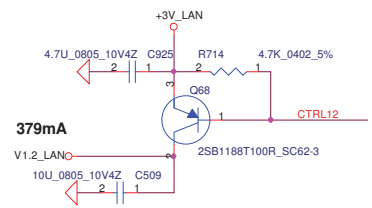
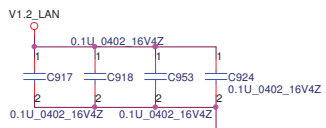
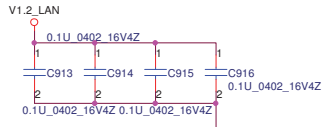
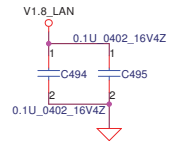
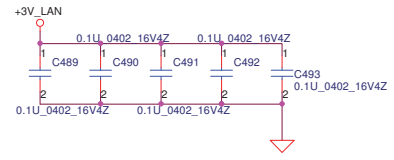
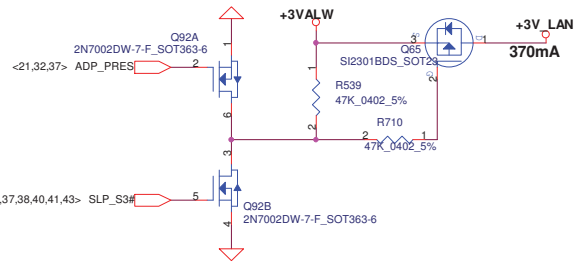
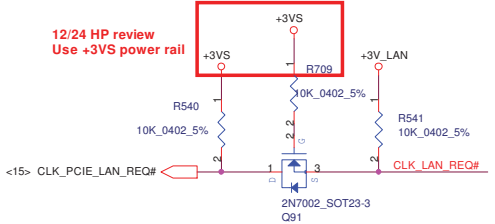


U8E	U5		
B4	VSS1001	VSS107	U5
B7	VSS1002	VSS108	U10
B10	VSS1003	VSS109	U11
B13	VSS1004	VSS110	U14
B16	VSS1005	VSS111	U16
B19	VSS1006	VSS112	U21
B22	VSS1007	VSS113	U22
B25	VSS1008	VSS114	U25
D24	VSS1009	VSS115	U3
E5	VSS1010	VSS116	V8
E7	VSS1011	VSS117	V19
E9	VSS1012	VSS118	V23
E11	VSS1013	VSS119	W1
E13	VSS1014	VSS120	W4
E15	VSS1015	VSS121	W5
E17	VSS1016	VSS122	W7
E19	VSS1017	VSS123	W9
E21	VSS1018	VSS124	W15
F24	VSS1019	VSS125	W19
G2	VSS1020	VSS126	W21
G5	VSS1021	VSS127	W22
G10	VSS1022	VSS128	W25
G13	VSS1023	VSS129	Y3
G16	VSS1024	VSS130	Y23
G19	VSS1025	VSS131	AA1
G24	VSS1026	VSS132	AA4
H10	VSS1027	VSS133	AA6
H12	VSS1028	VSS134	AA8
H18	VSS1029	VSS135	AA11
H23	VSS1030	VSS136	AA13
J5	VSS1031	VSS137	AA15
J9	VSS1032	VSS138	AA16
J10	VSS1033	VSS139	AA17
J11	VSS1034	VSS140	AA19
J12	VSS1035	VSS141	AA22
J13	VSS1036	VSS142	AA25
J15	VSS1037	VSS143	AA28
J21	VSS1038	VSS144	AB9
J22	VSS1039	VSS145	AB11
J25	VSS1040	VSS146	AB13
K2	VSS1041	VSS147	AB24
K6	VSS1042	VSS148	AC1
K10	VSS1043	VSS149	AC4
K11	VSS1044	VSS150	AC10
K12	VSS1045	VSS151	AC12
K13	VSS1046	VSS152	AC14
K15	VSS1047	VSS153	AD2
K17	VSS1048	VSS154	AD6
K23	VSS1049	VSS155	AD9
L5	VSS1050	VSS156	AD16
L10	VSS1051	VSS157	AD19
L16	VSS1052	VSS158	AD22
L17	VSS1053	VSS159	AE3
L22	VSS1054	VSS160	AE4
L25	VSS1055	VSS161	AE11
M9	VSS1056	VSS162	AE13
M10	VSS1057	VSS163	AE15
M12	VSS1058	VSS164	V17
M13	VSS1059	VSS165	AE8
M14	VSS1060	VSS166	V9
M16	VSS1061	VSS167	J16
M17	VSS1062	VSS168	
M23	VSS1063	VSS169	
N2	VSS1064		
N5	VSS1065		
N6	VSS1066		
N7	VSS1067		
N8	VSS1068		
N10	VSS1069		
N12	VSS1070		
N13	VSS1071		
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N22	VSS1076		
N25	VSS1077		
P9	VSS1078		
P10	VSS1079		
P12	VSS1080		
P13	VSS1081		
P14	VSS1082		
P16	VSS1083		
P17	VSS1084		
P23	VSS1085		
R5	VSS1086		
R7	VSS1087		
R8	VSS1088		
R9	VSS1089		
R10	VSS1090		
R16	VSS1091		
R17	VSS1092		
R19	VSS1093		
R21	VSS1094		
R22	VSS1095		
R25	VSS1096		
T2	VSS1097		
T8	VSS1098		
T10	VSS1099		
T11	VSS1100		
T12	VSS1101		
T13	VSS1102		
T14	VSS1103		
T15	VSS1104		
T16	VSS1105		
T23	VSS1106		
IC9-M SFF ES_FCBGA569		VSS_NCTF[01]	A1
		VSS_NCTF[02]	A25
		VSS_NCTF[03]	AE1
		VSS_NCTF[04]	AE25

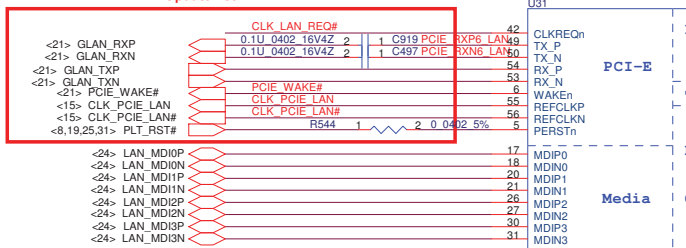
Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/03/10
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Compal Electronics, Inc.		
ICH9(4/4) POWER&GND		
Title	Document Number	Rev
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12/24 HP review
Use +3VS power rail



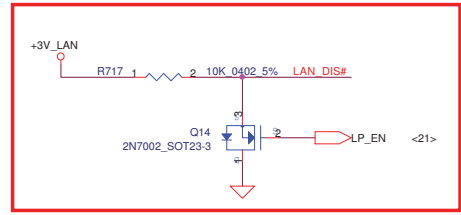
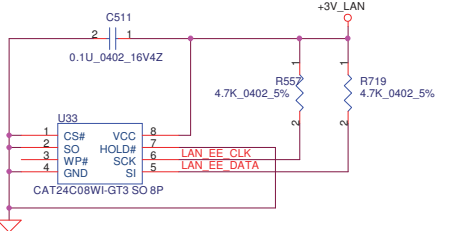
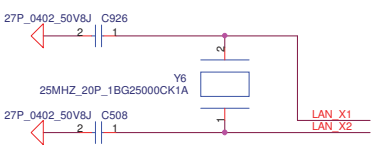
12/20
Update net



12/20
Del reserved SPI net



12/26
8072@-->install
01/23
No support 8075



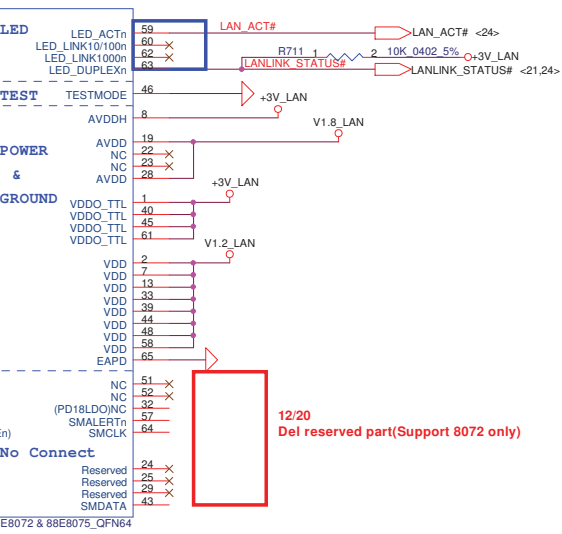
12/22 HP review
Add LP_EN

Insert	88E8072	88E8075
	R653	R654
	C533	R655
	R440	U36
	Q28	C694
		R659
		R658
	R656	
	R652	
	R660	



12/20
Del reserved SPI part

0115 Marvell
Open Pin62 Pin63



12/20
Del reserved part(Support 8072 only)

12/26
8072@-->install

151mA

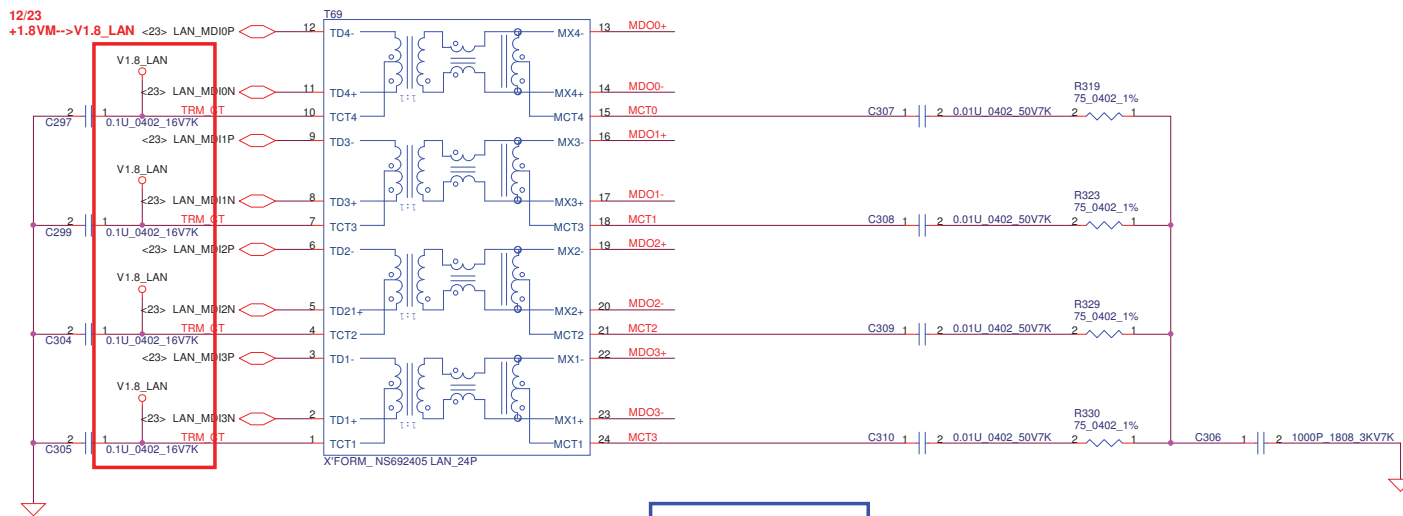
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Issued Date	2008/10/03	Deciphered Date	2009/10/03
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Date	Tuesday, February 03, 2009	Sheet	23	of	45

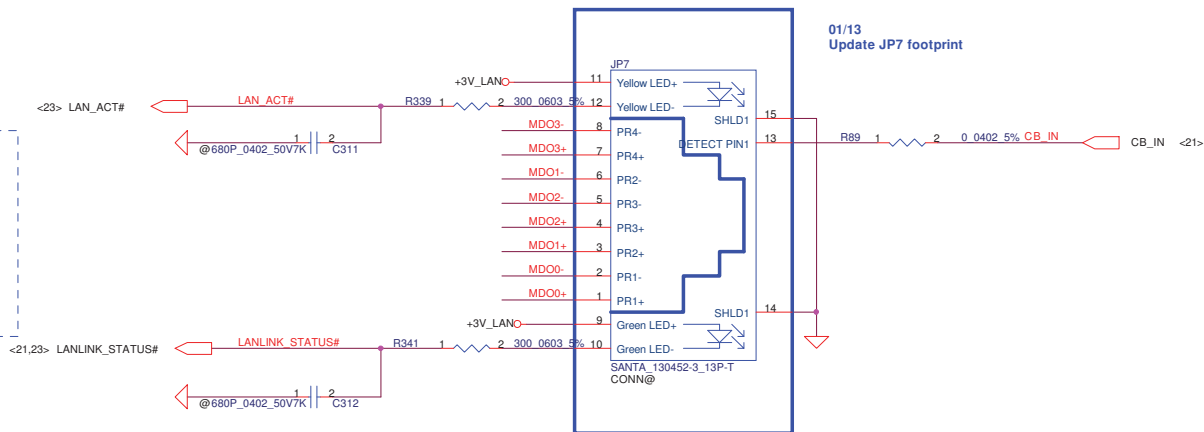
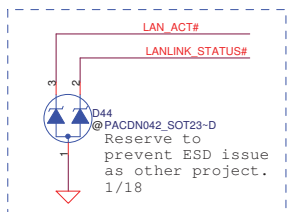


12/15 No support Docking

Delete all termination cause they are already inside BOAZMAN. 9/28

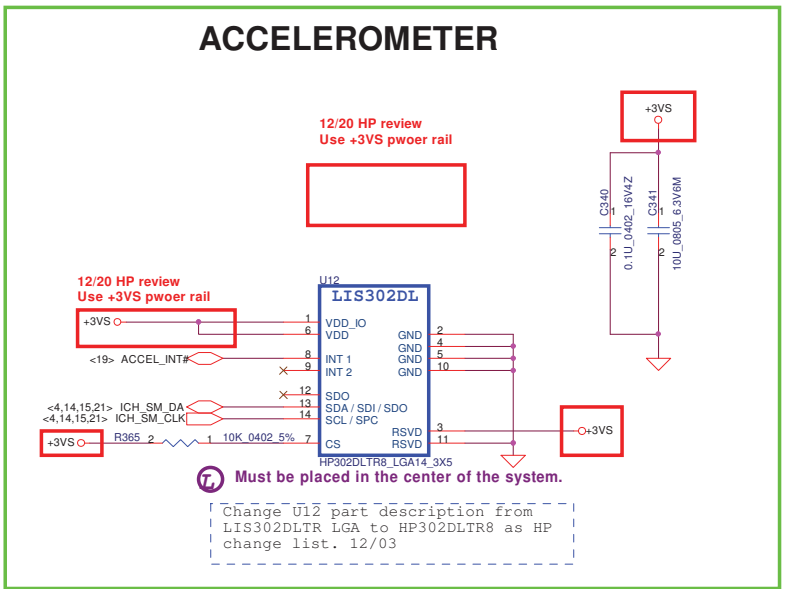
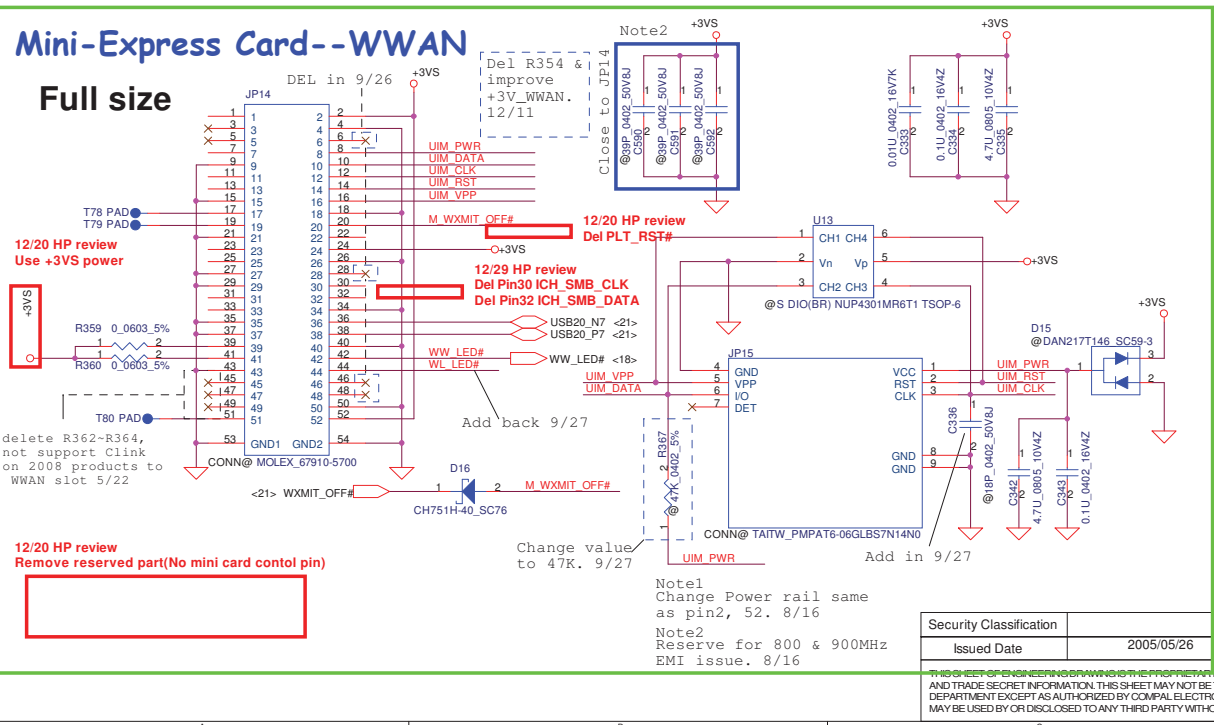
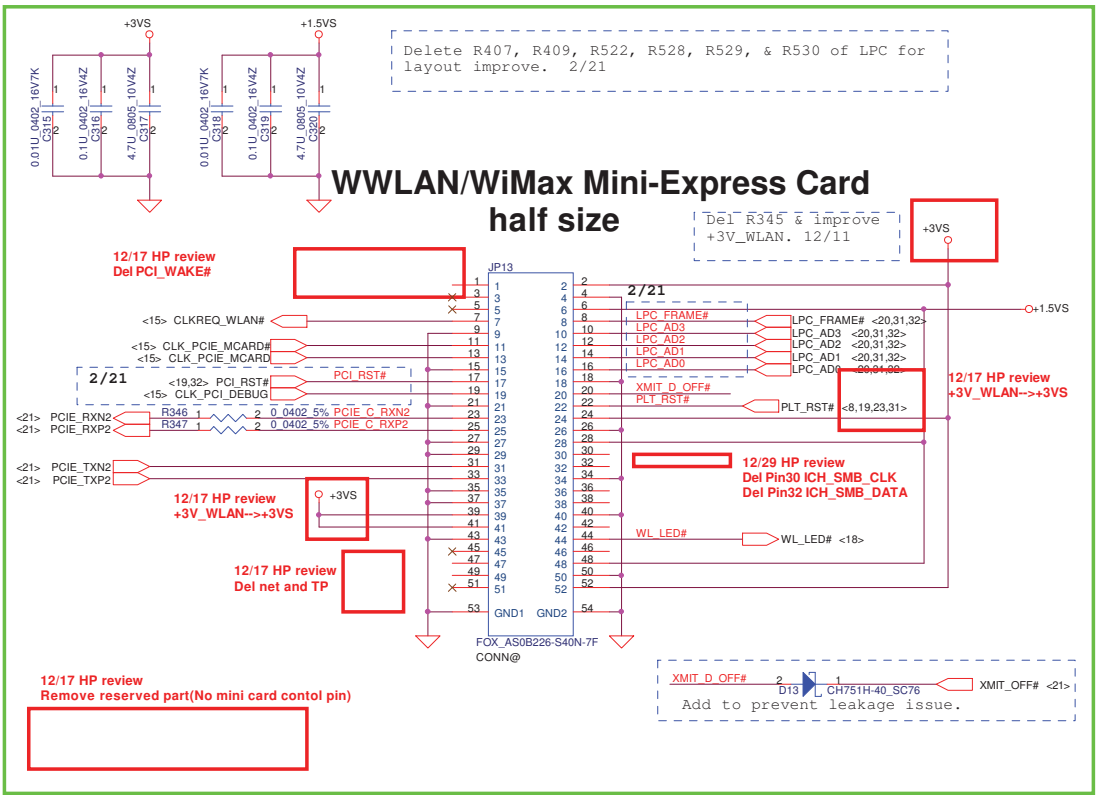


12/29 HP review
Del Q23 Q24



Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/07/26
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Title		
Compal Electronics, Inc.		
Magnetic & RJ45		
Size	Document Number	Rev
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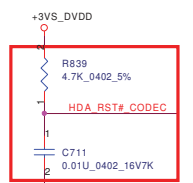
Security Classification	Compal Secret Data	Title	Compal Electronics, Inc.	
Issued Date	2005/05/26	Deciphered Date	2006/07/26	Rev
		Size	Document Number	0.1
		LA-5221P		
		Date	Tuesday, February 03, 2009	Sheet 25 of 45

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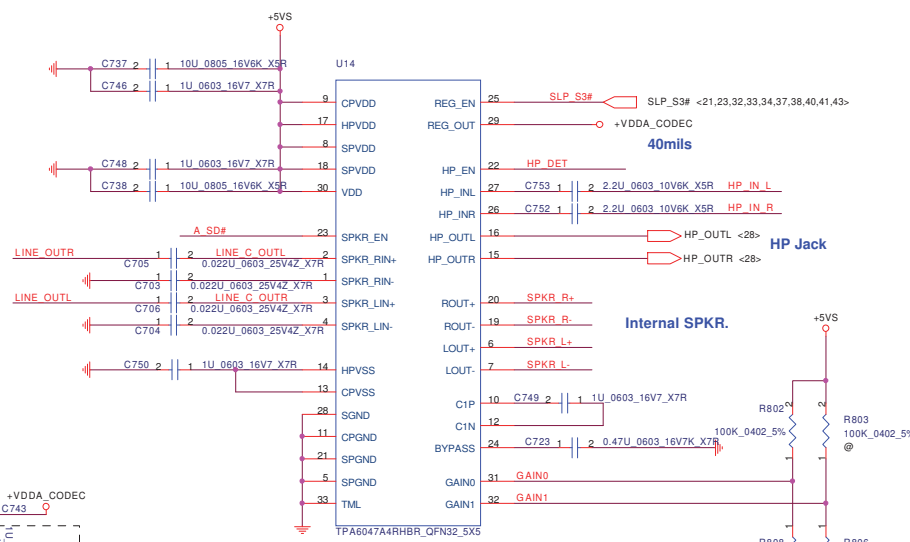
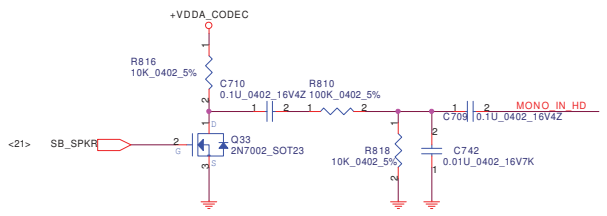
12/17 Remove to small board

Title		
Card reader board		
Size	Document Number	Rev
	LA-5221P	0.1
Date:	Tuesday, February 03, 2009	Sheet 26 of 45

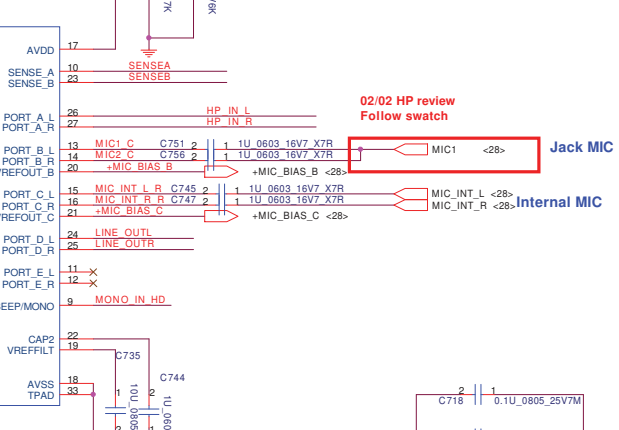
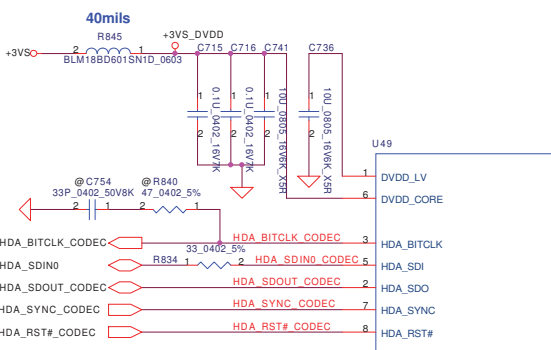
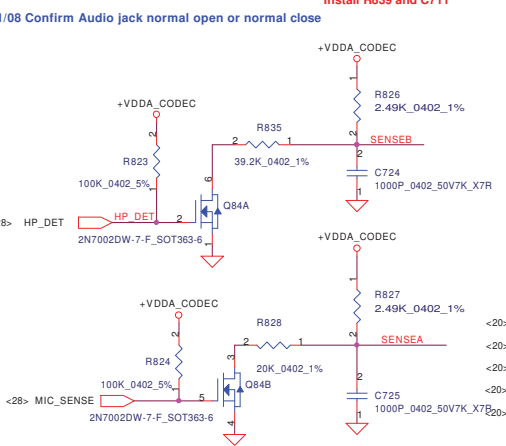
TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5



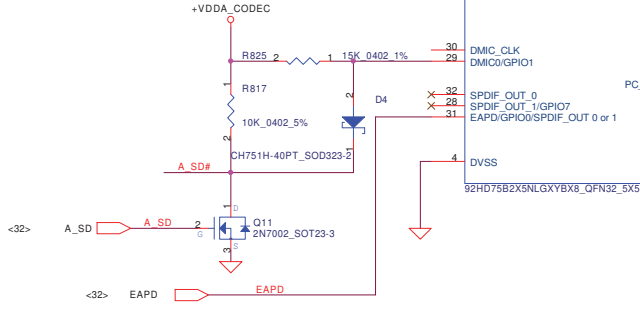
01/08 HP review
Install R839 and C711



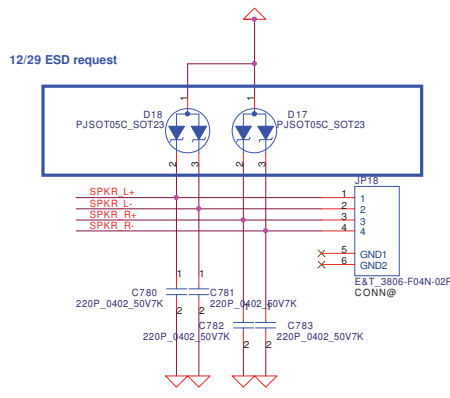
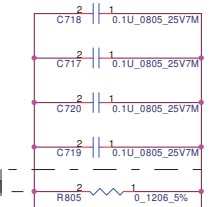
GAIN0	GAIN1	Av (inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



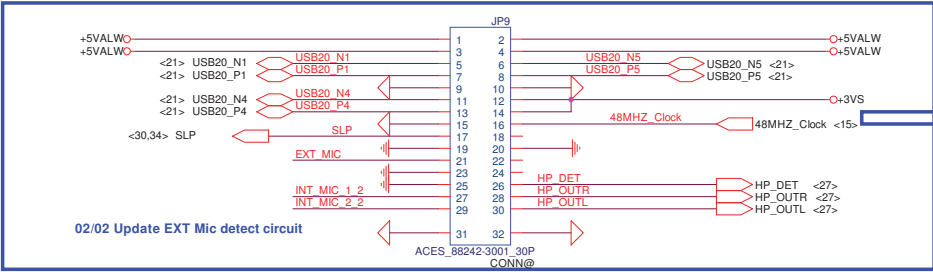
02/02 HP review
Follow swatch



audio ground must be connect to digital ground with an 80m1 copper bridge located directly under codec to prevent ESD latch up.



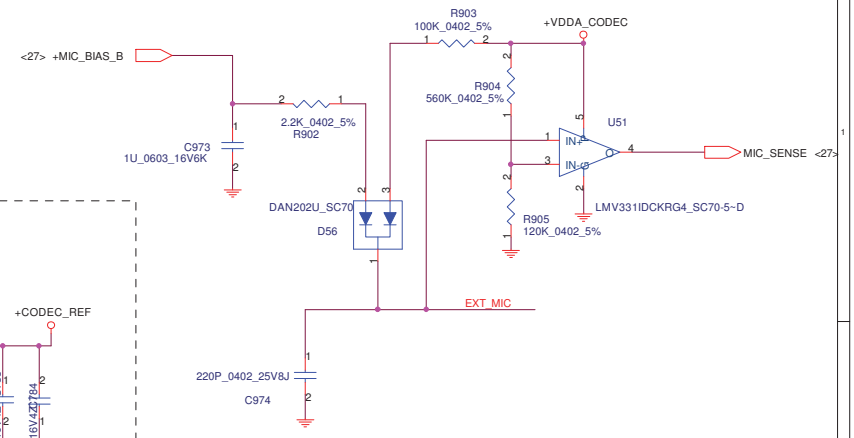
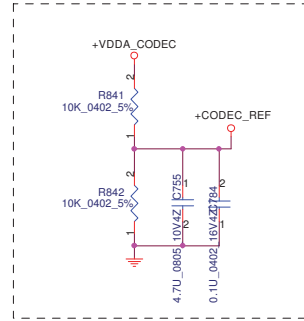
01/10 Fine tune pin define Use the same conn JP9



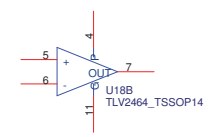
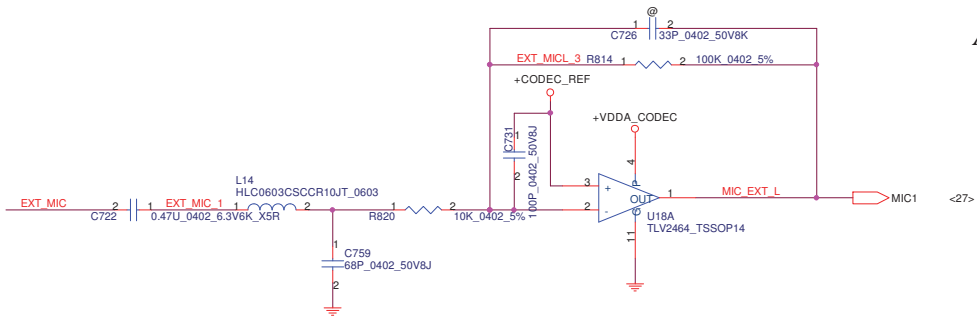
USB I/O connx2 , Audio JACK
Card reader transfer conn

12/26 Reserved for card reader

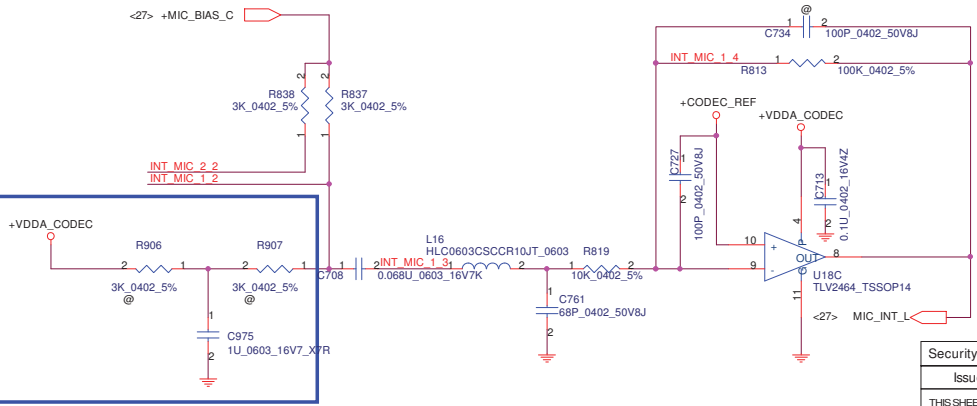
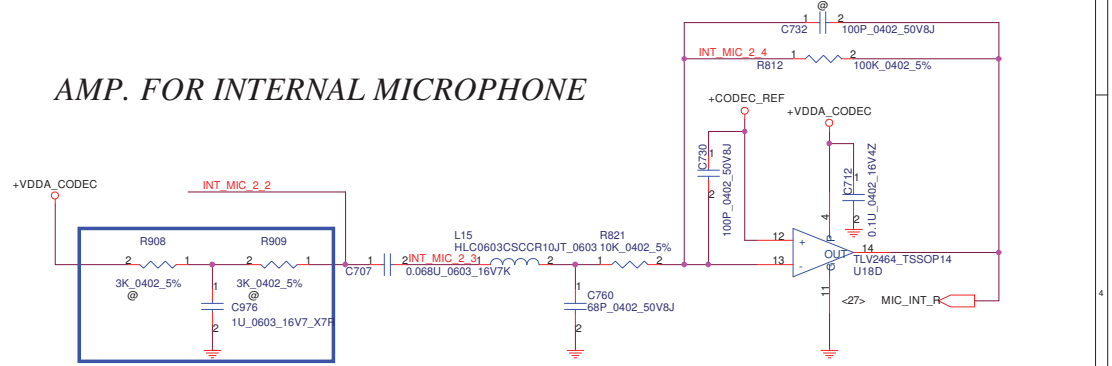
Place close to U18



AMP. FOR EXTERNAL MICROPHONE



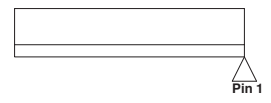
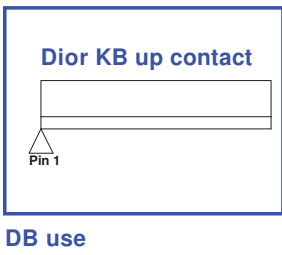
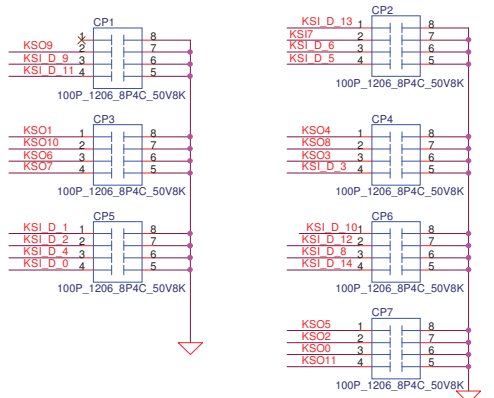
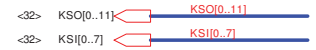
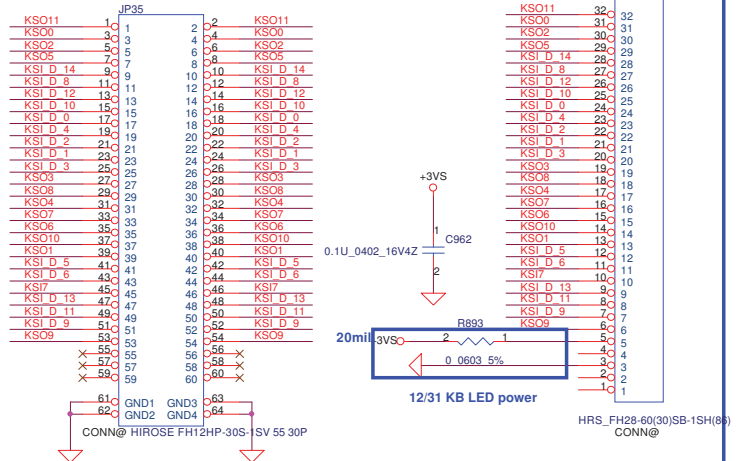
AMP. FOR INTERNAL MICROPHONE



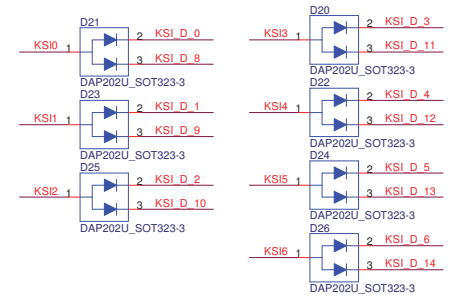
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	AMP & Audio Jack	
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INT_KBD_CONN.

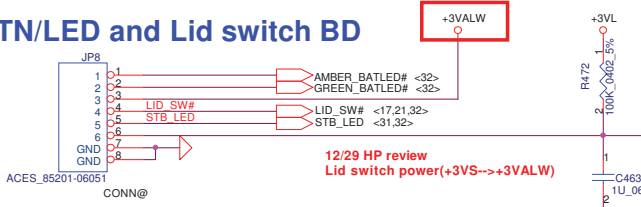
01/09 Co layout for DB phase



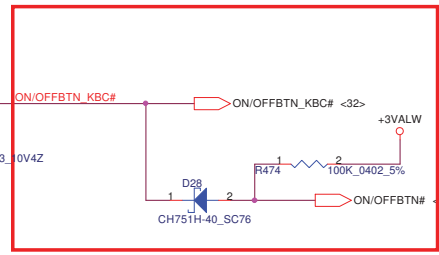
Pin1 reserve , so net name is reserve for Fossil down contact



Power BTN/LED and Lid switch BD

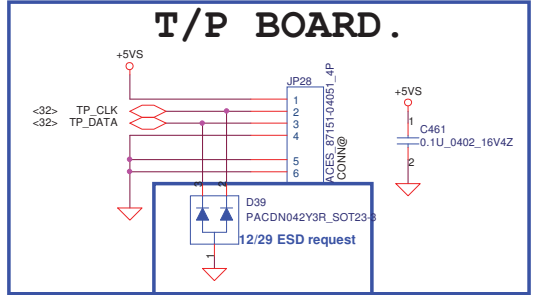


PS:GND use DC in jack GND

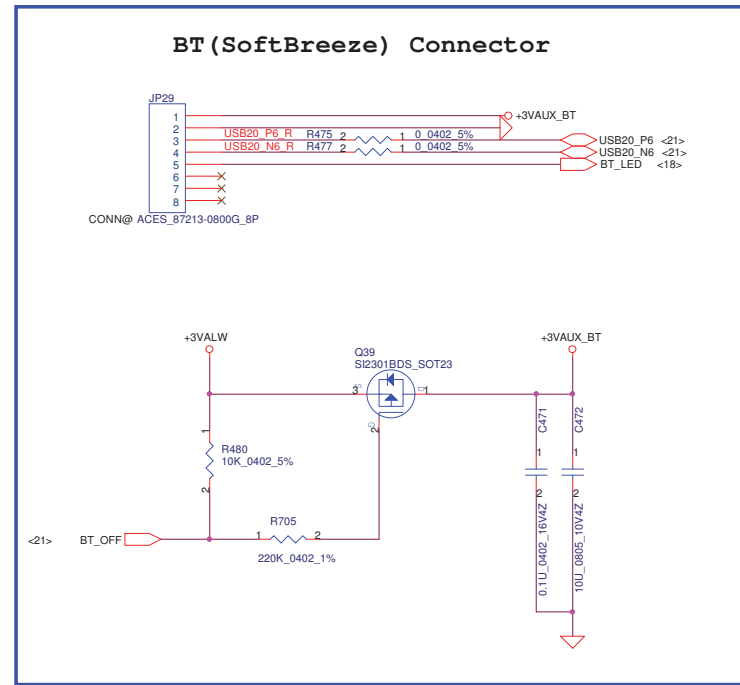
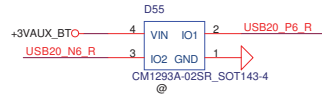


12/20 HP review
Modify ON/OFFBTN# circuit

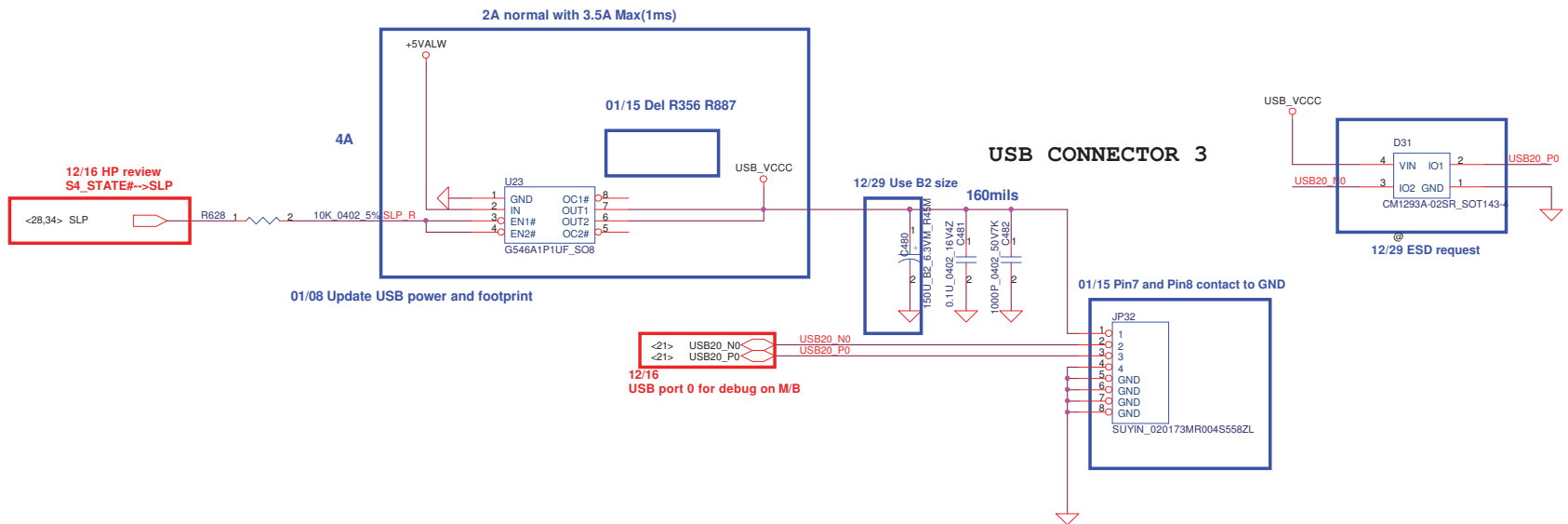
T/P BOARD.



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Issued Date	2005/03/10	Deciphered Date		
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Size	Document Number	Date		Rev
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		Sheet	29	of 45

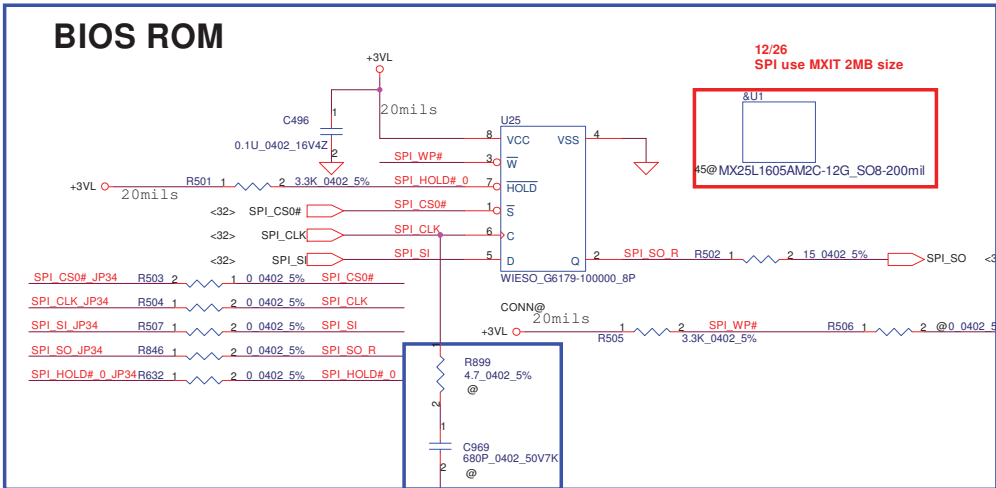


12/16 change to small board

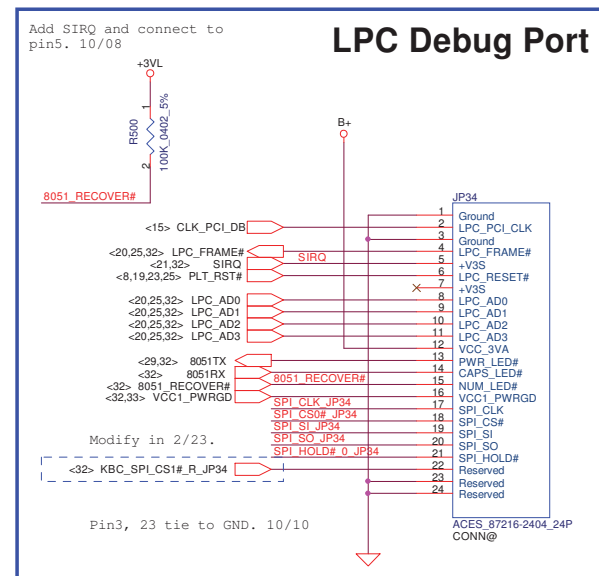


Security Classification	Compal Secret Data			Title		
Issued Date	2006/02/13	Deciphered Date	2006/07/26	Compal Electronics, Inc.		
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01/23
 U25 is conn
 &U1 is SPI ROM



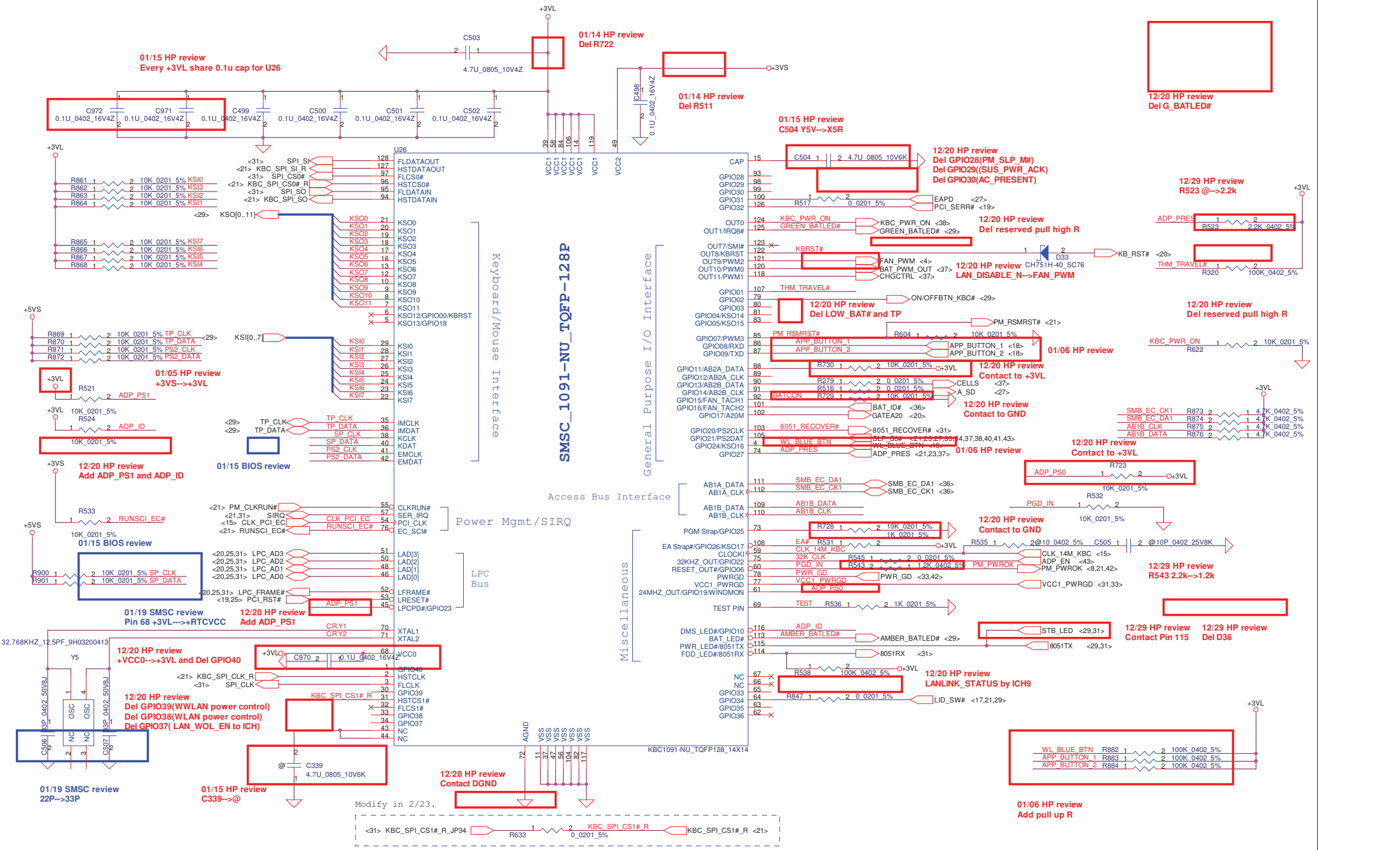
01/13
 Reserved for ESD



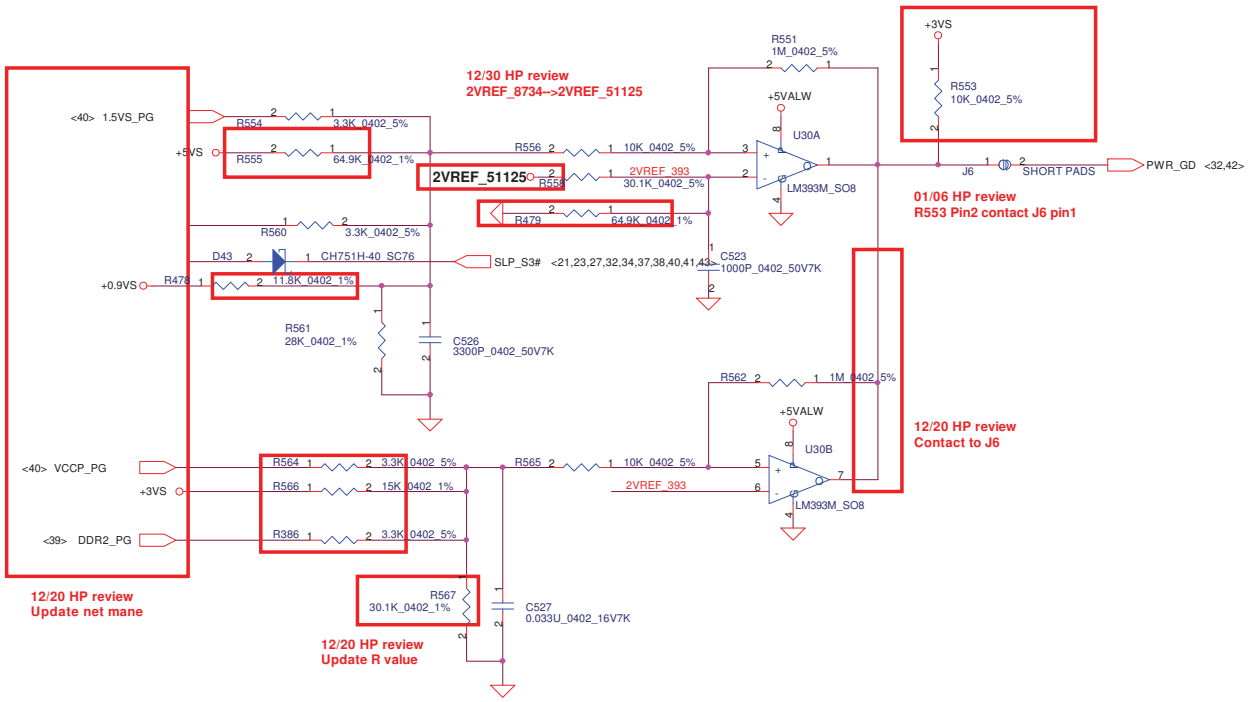
Security Classification	Compal Secret Data			Title TCG/BIOS ROM/PS2/SW LPC DEBUG	
Issued Date	2005/03/10	Deciphered Date	2006/03/10		
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Compal Electronics, Inc.

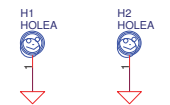
Rev 0.1



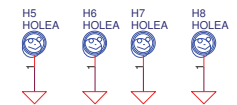
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Issued Date	2006/02/13	Deciphered Date	2006/07/26		
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			32	45	



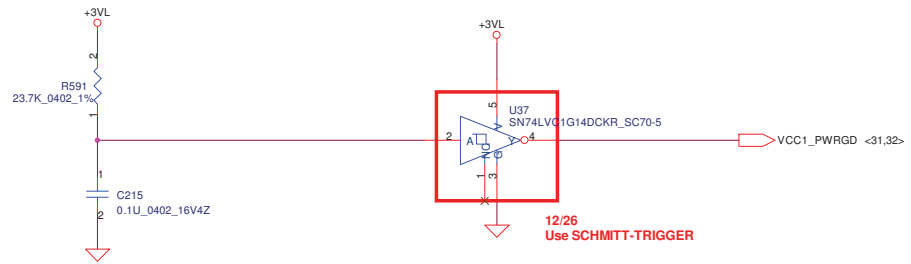
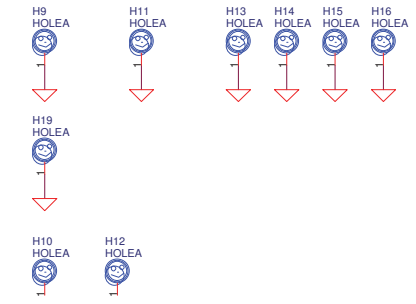
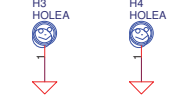
WWAN Card STANDOFF



CPU support



WWLAN Card STANDOFF



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Issued Date	2005/05/26	Deciphered Date		
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Title			POK CKT	
Size	Document Number	Rev		
	LA-522IP	0.1		
Date:	Tuesday, February 03, 2009	Sheet	33	of 45

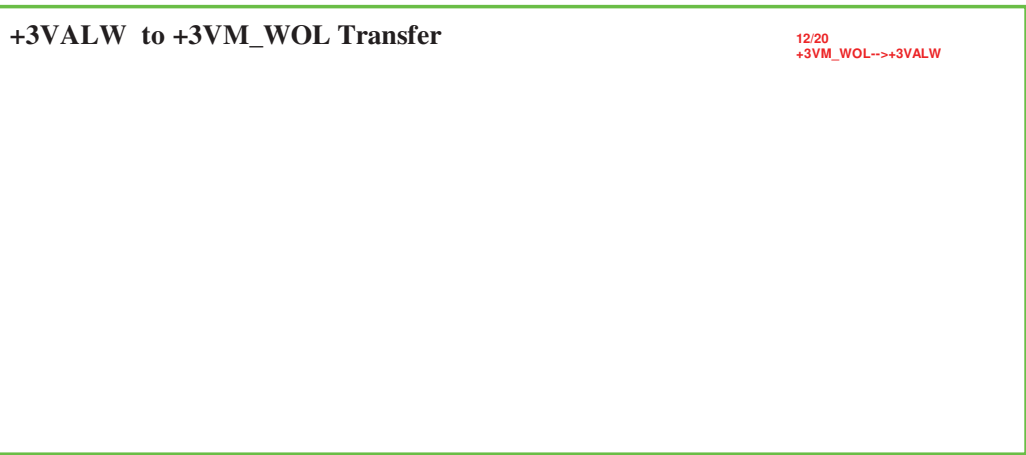
+1.05VM to +VCCP Transfer

12/12
+1.05VN-->+VCCP



+3VALW to +3VM_WOL Transfer

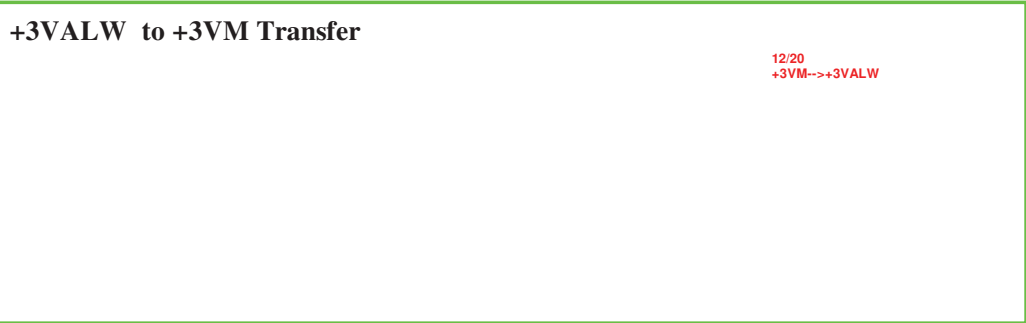
12/20
+3VM_WOL-->+3VALW



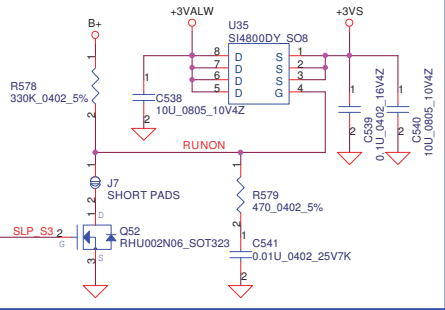
12/12 REMOVE

+3VALW to +3VM Transfer

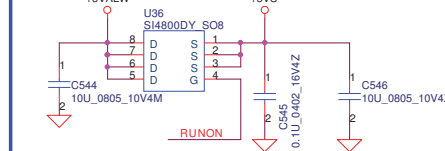
12/20
+3VM-->+3VALW



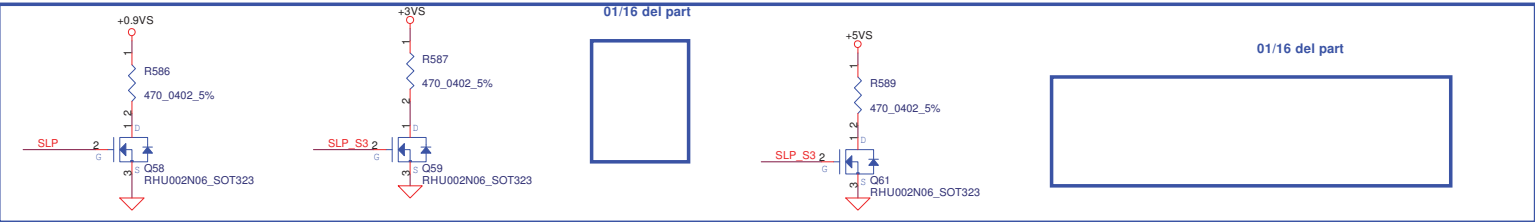
+3VALW to +3VS Transfer



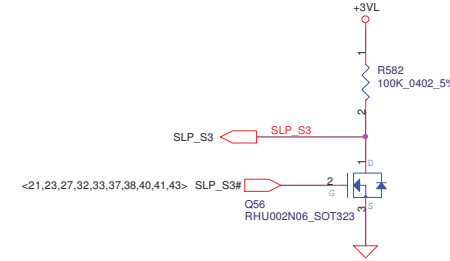
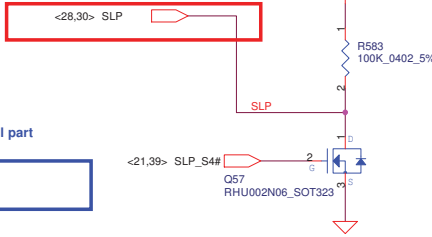
+5VALW to +5VS Transfer



Discharge circuit-1

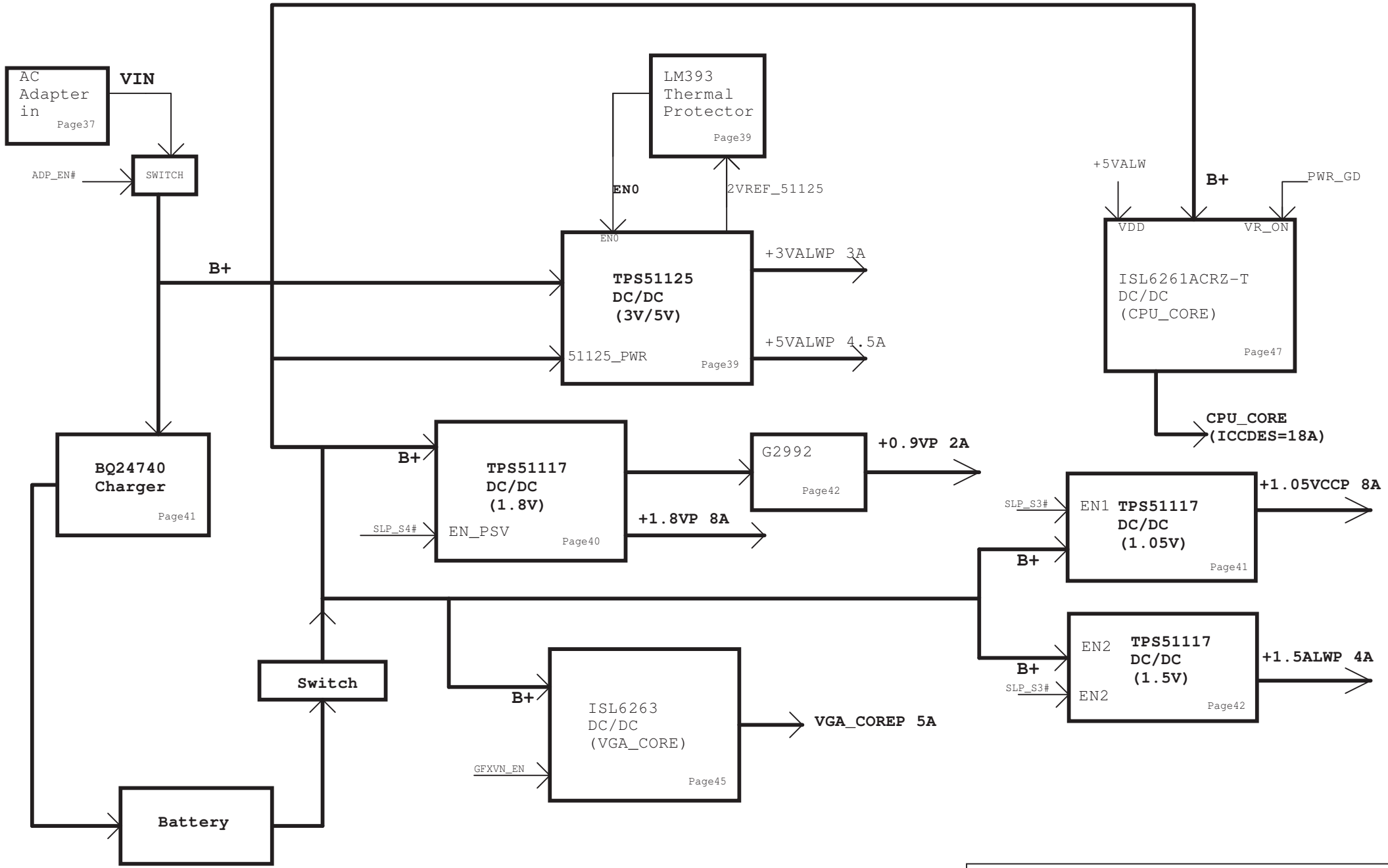


12/20 HP review
SLP control

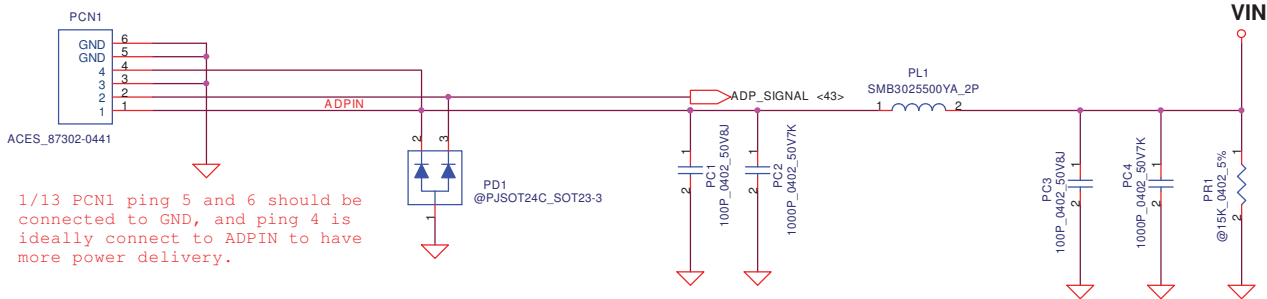


Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26
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Compal Electronics, Inc.		
Title DC/DC Circuits		
Size	Document Number LA-5221P	Rev 0.1
Date	Tuesday, February 03, 2009	Sheet 34 of 45

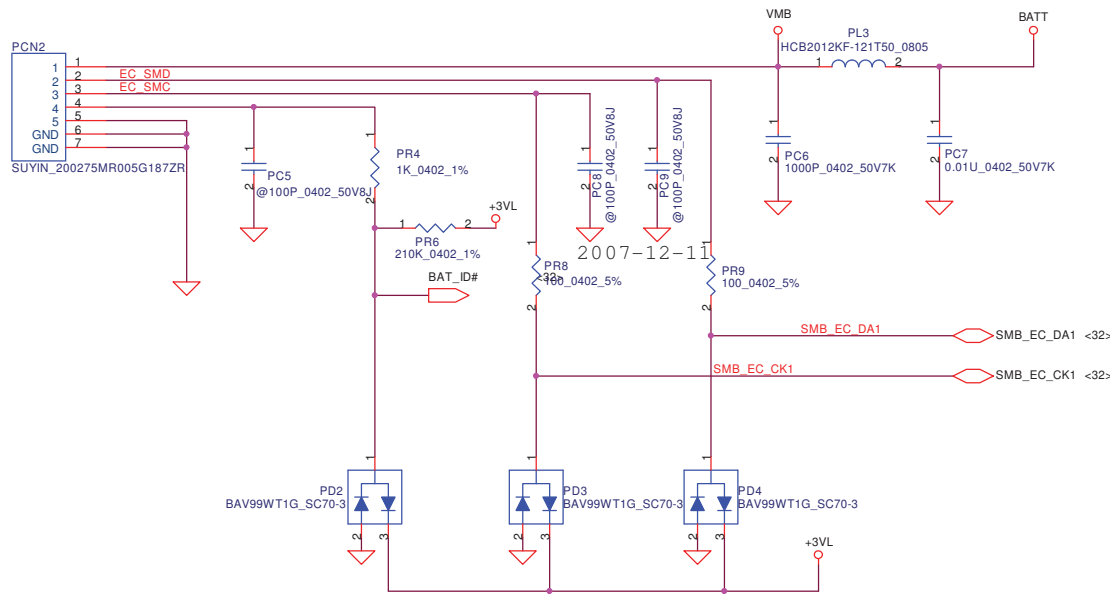


Title		
POWER BLOCK DIAGRAM		
Size	Document Number	Rev
Date:	Tuesday, February 03, 2009	Sheet 35 of 45



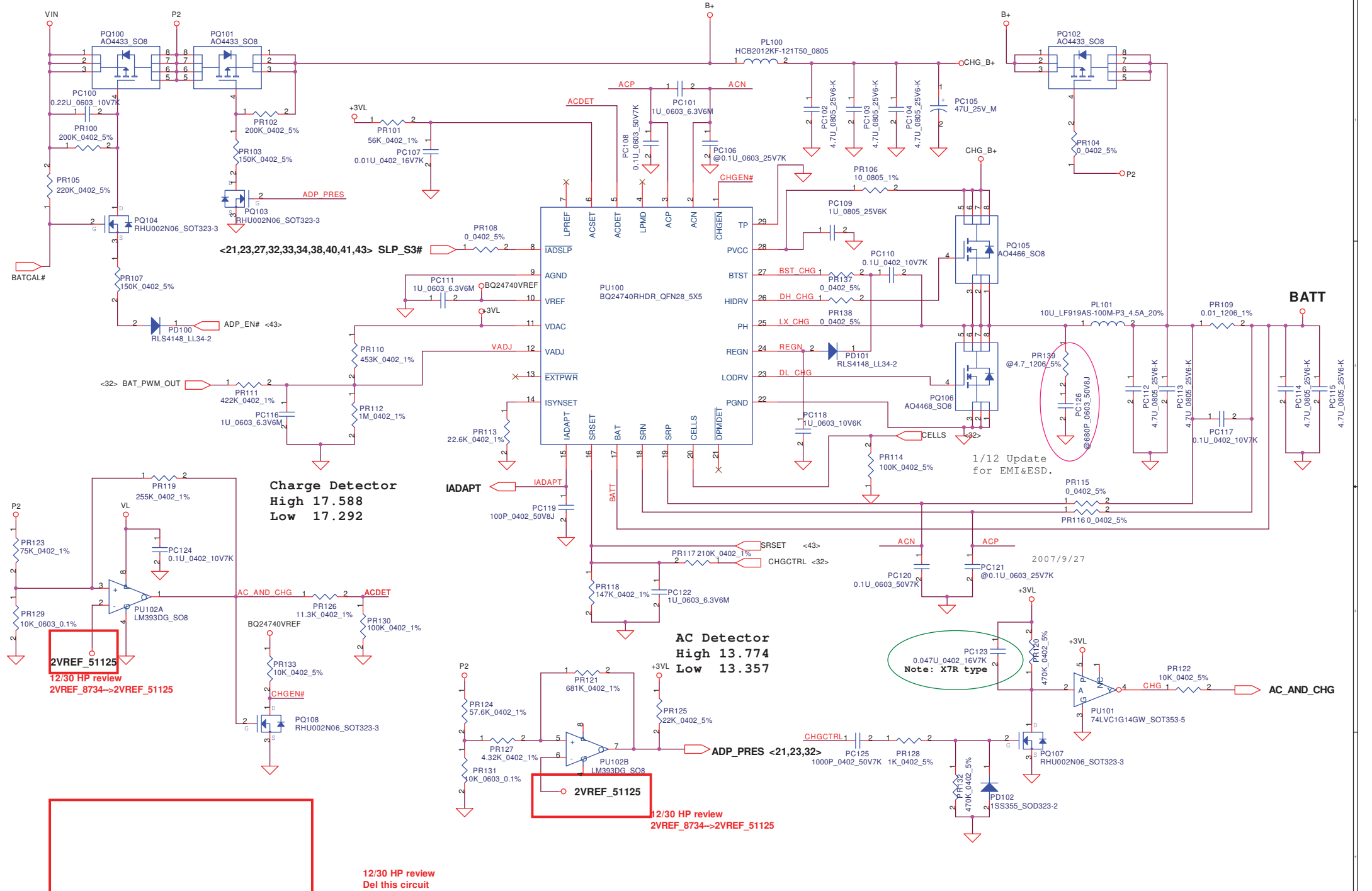
1/13 PCN1 ping 5 and 6 should be connected to GND, and ping 4 is ideally connect to ADPIN to have more power delivery.

PH1 under CPU botten side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 47 +-3 degree C



12/26 HP review
 Remove reserved PH1 circuit

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Date:	Tuesday, February 03, 2009	Sheet	36	of	45

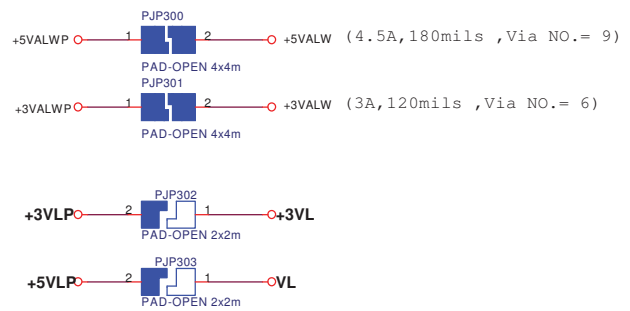
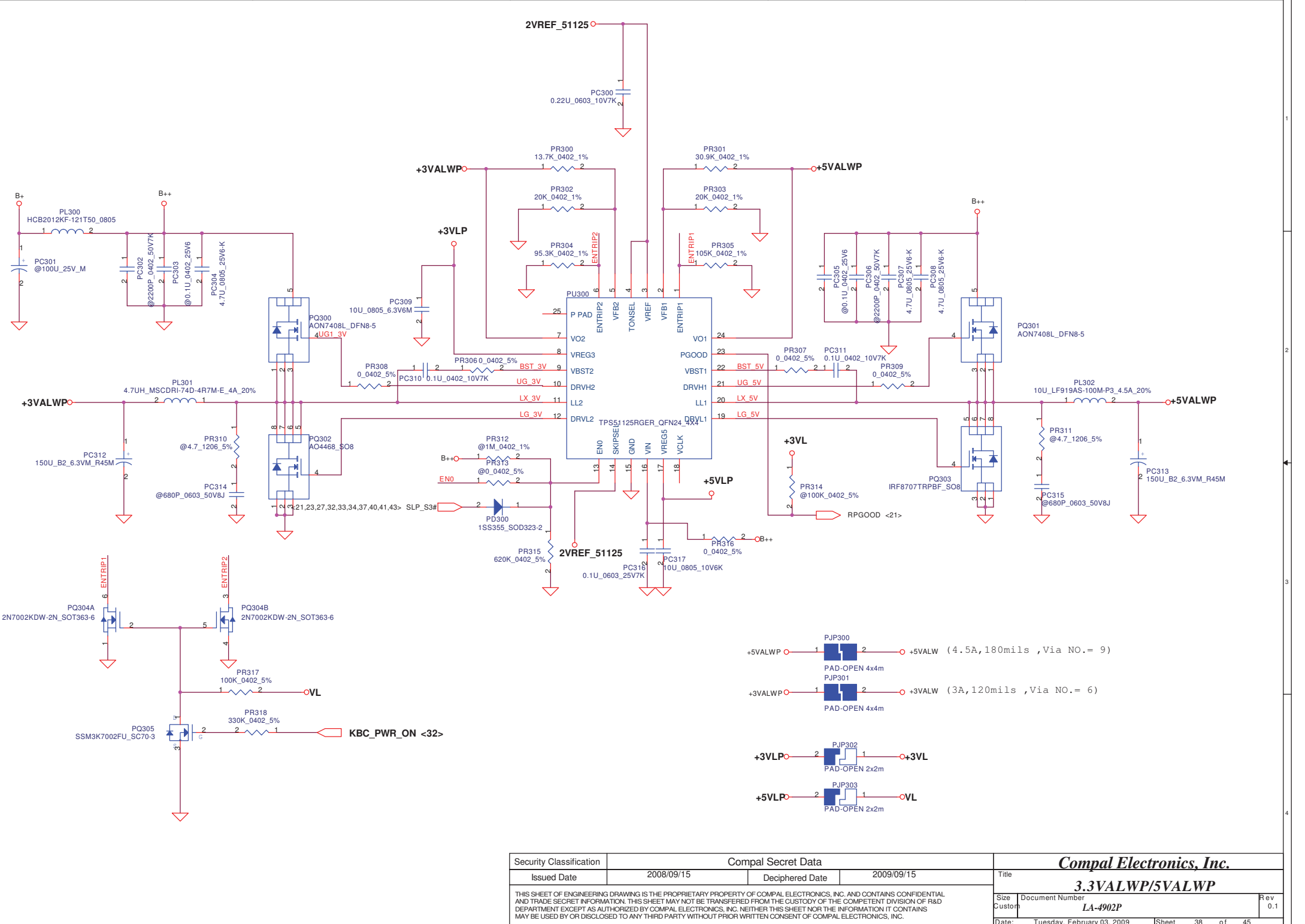


Charge Detector
 High 17.588
 Low 17.292

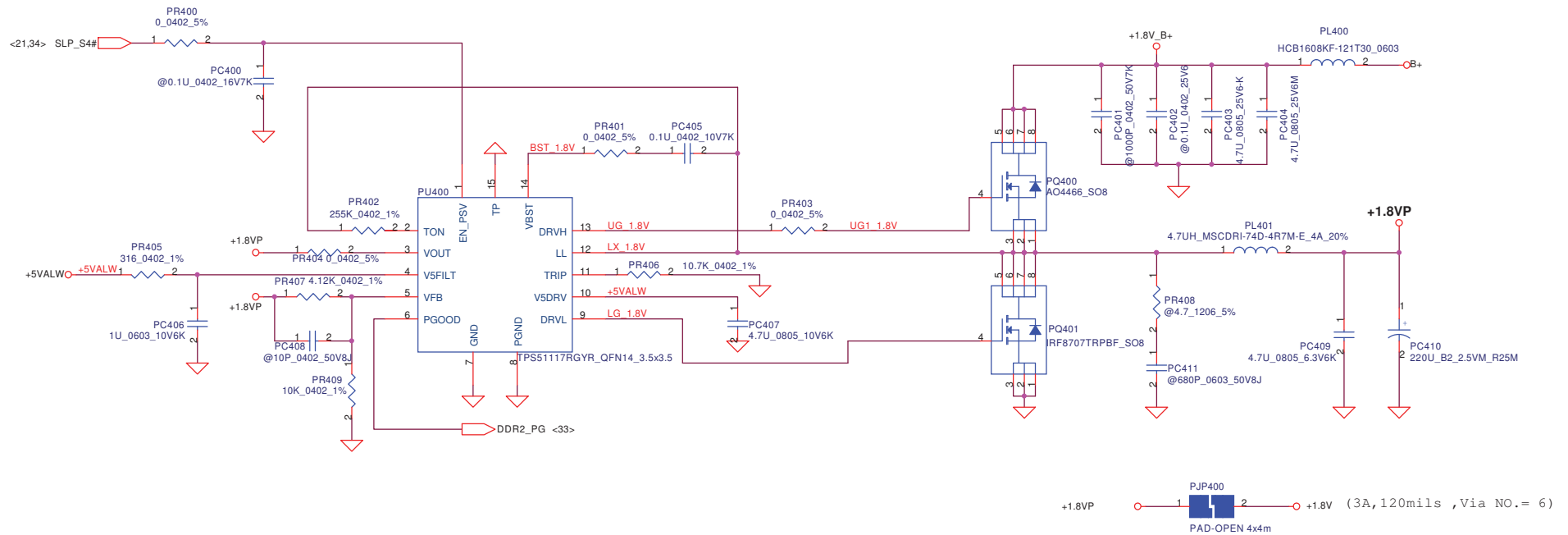
AC Detector
 High 13.774
 Low 13.357

12/30 HP review
 Del this circuit

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Size	Document Number	Date		Sheet	Rev
	LA-3941P	Tuesday, February 03, 2009		37	0.1
				of	45

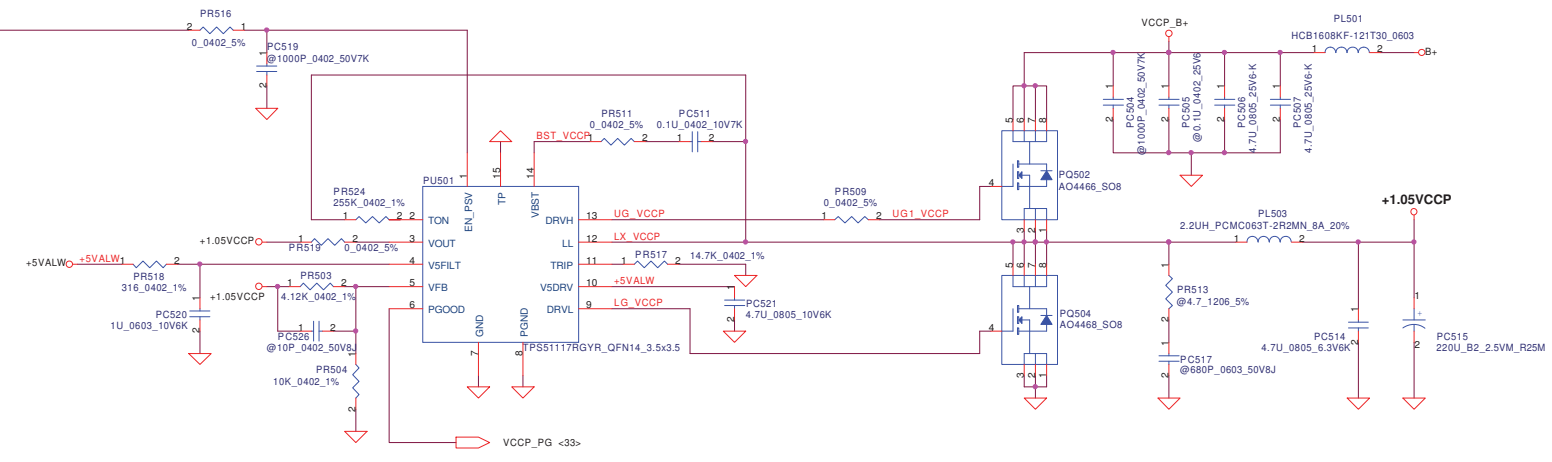


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				Document Number LA-4902P	Rev 0.1
				Date Tuesday, February 03, 2009	Sheet 38 of 45

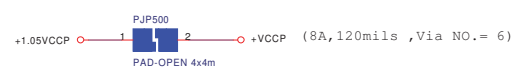
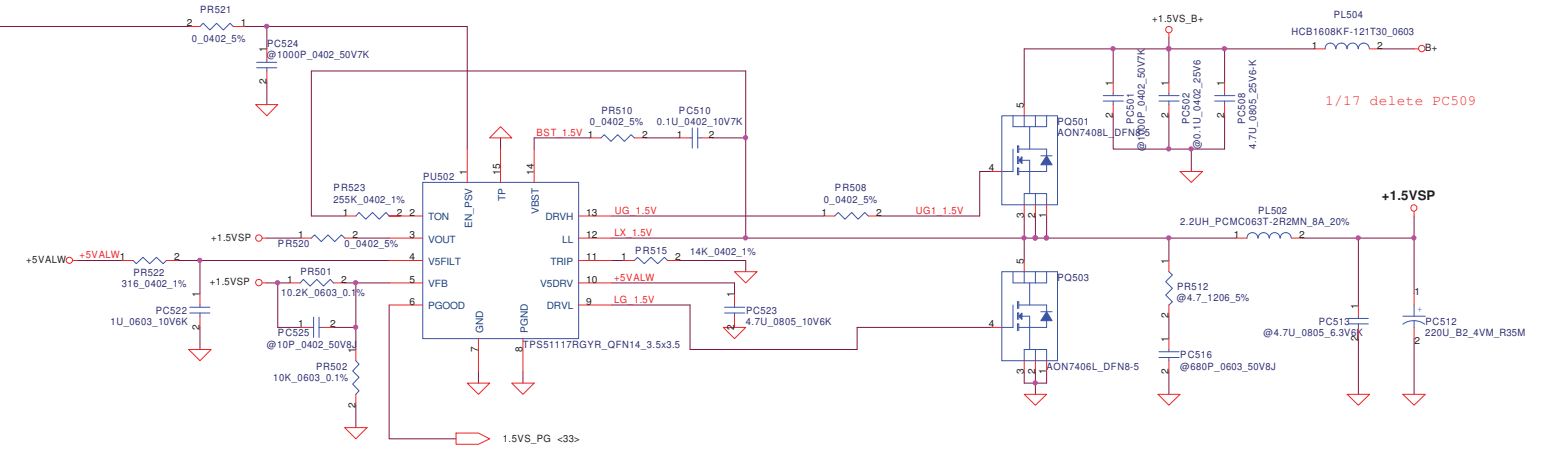


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Size	Document Number	Rev		
	LA-3942P	0.1		
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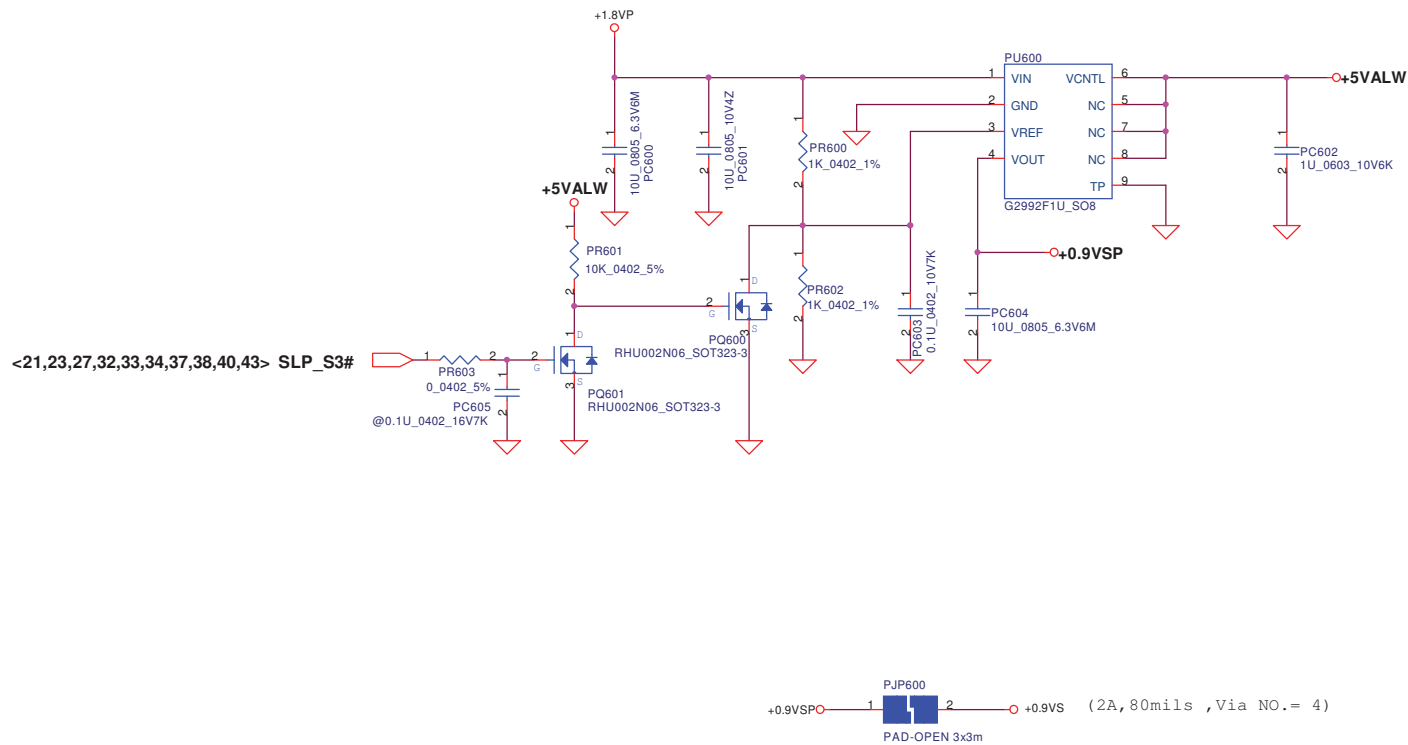
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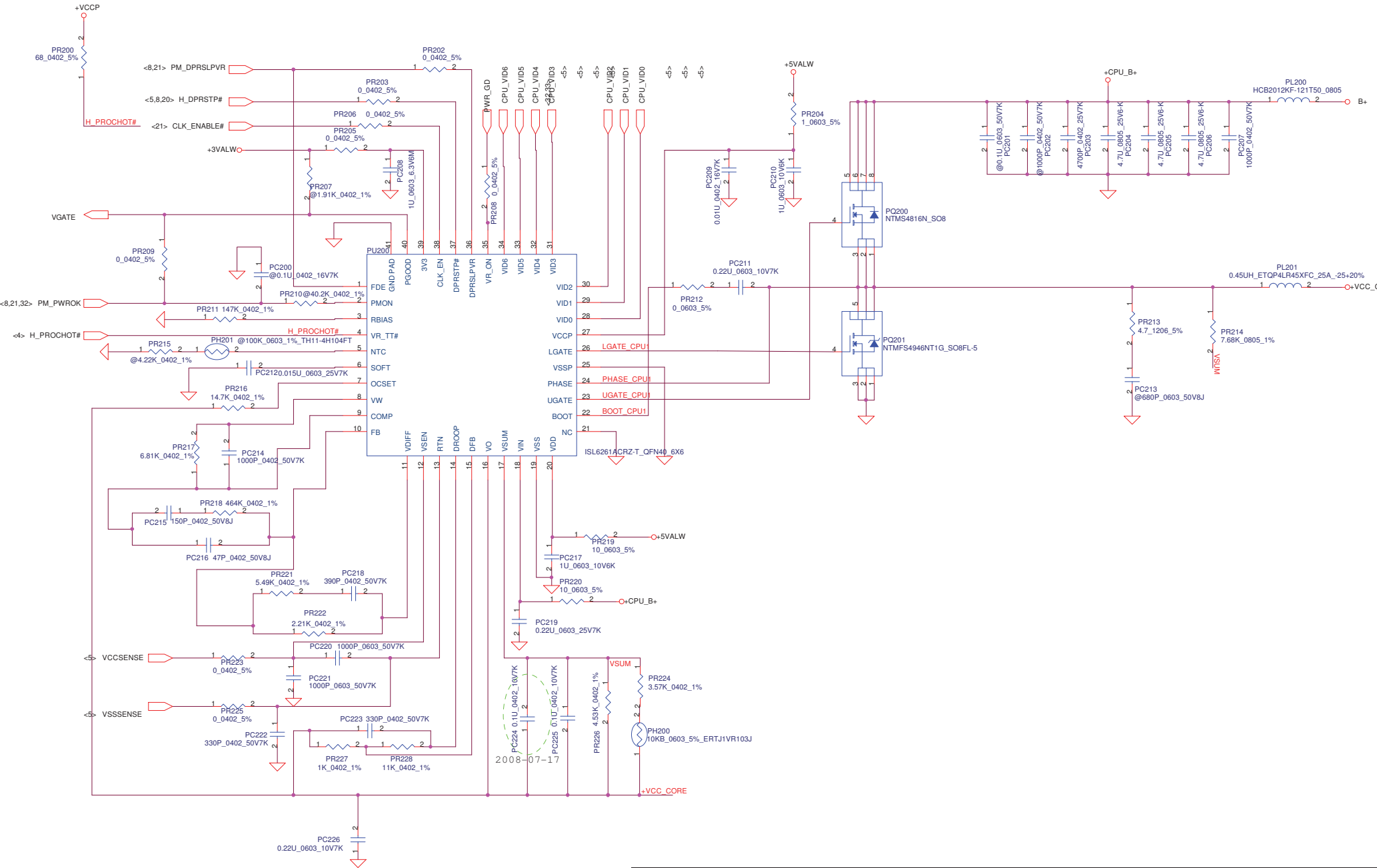
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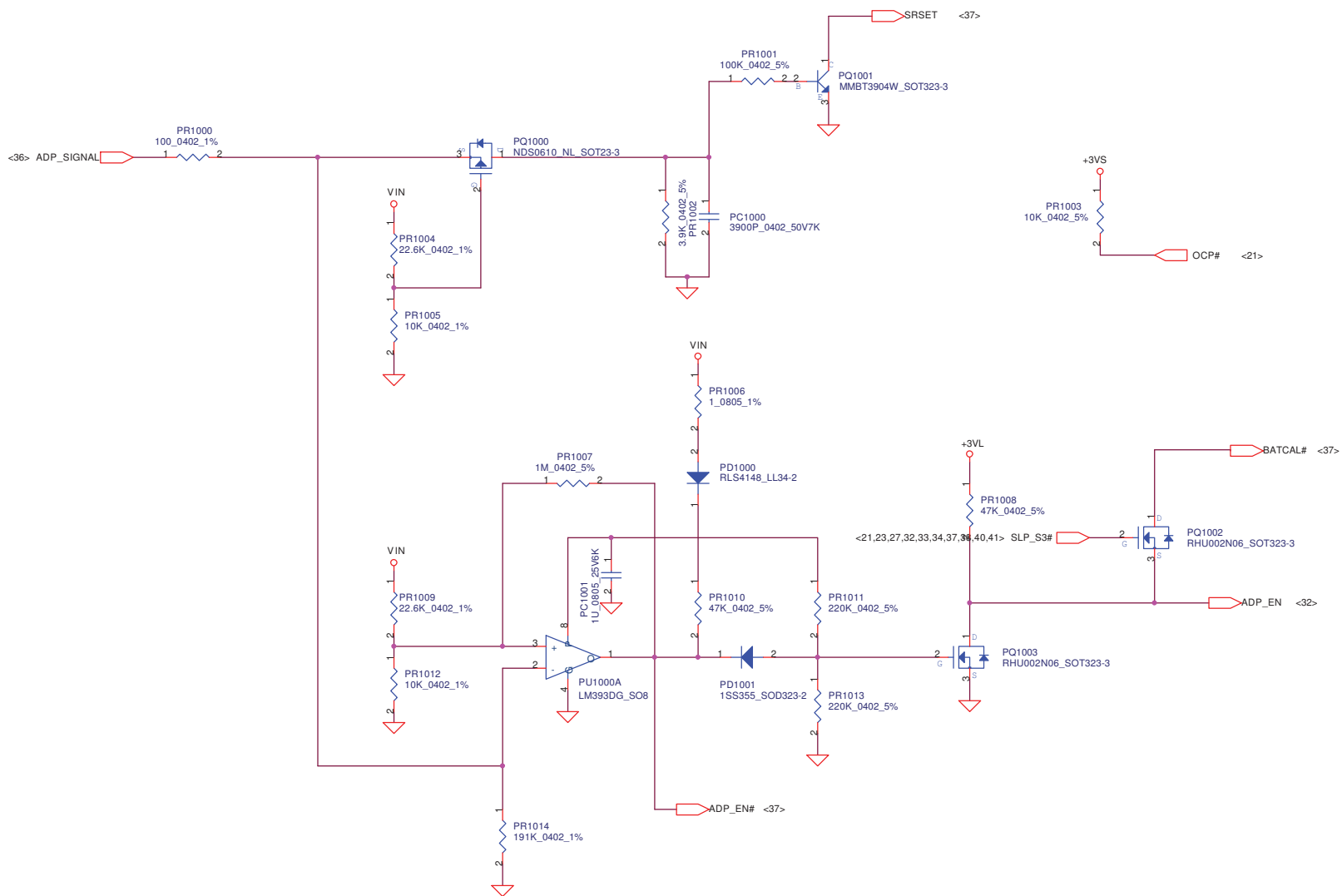


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				Size	Document Number
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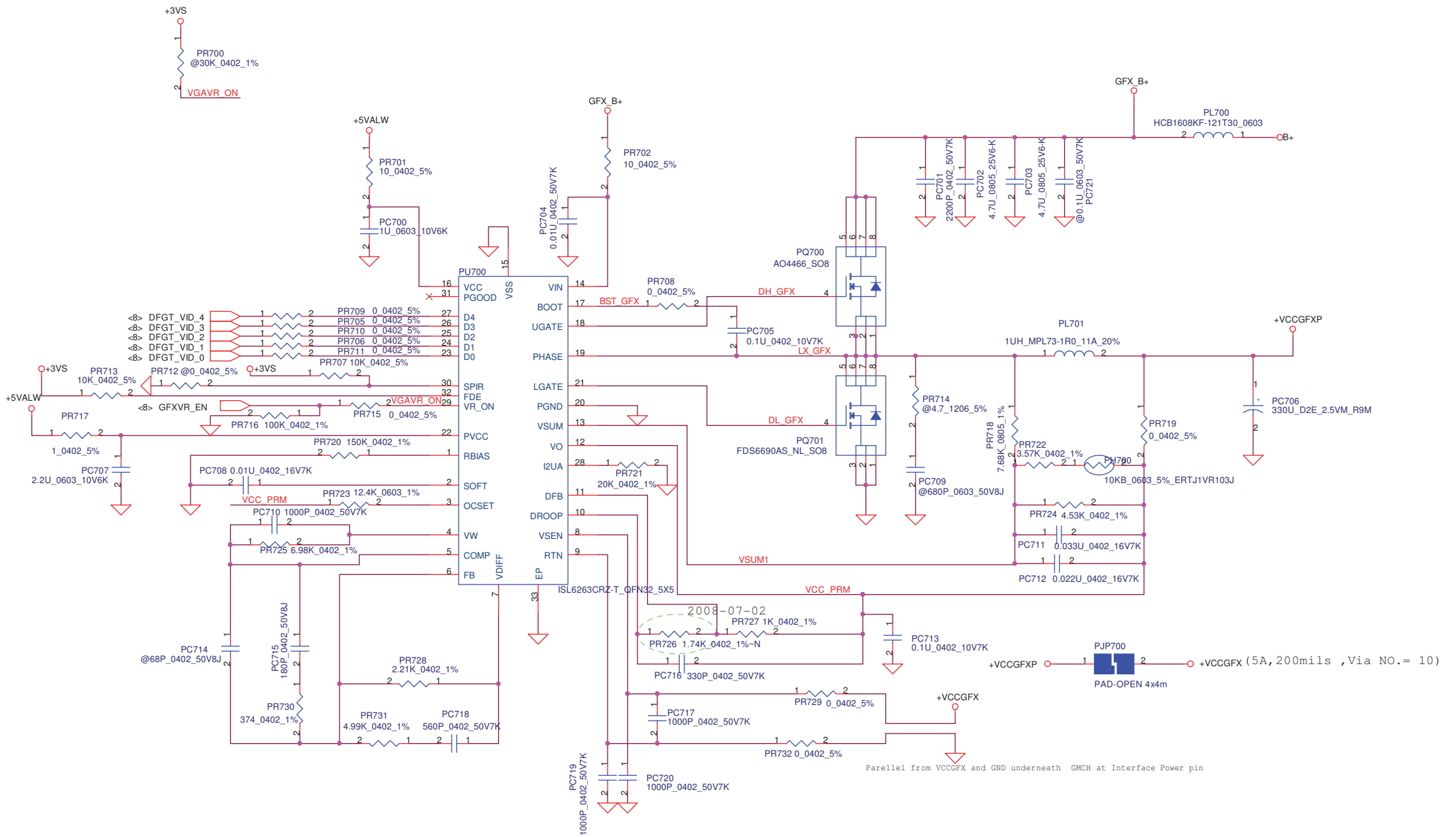


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Compal Electronics, Inc.		
CPU_CORE		
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Custom	IAX00	0.1
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Custom	LA-4902P			
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				Size	Document Number
				LA-326IP UMA	
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Item	Reason for change	PG#	Modify List	Date	Phase
1		40			
2		42			
3		44			
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7		39 41 43			
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Security Classification		Control - Secret Data		Control - Secret Data	
Issued Date	2006/02/28	Dispersed Date	2007/02/28	Cumtel Electronics Inc. Control - Secret Data Changed List History - Core	
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