

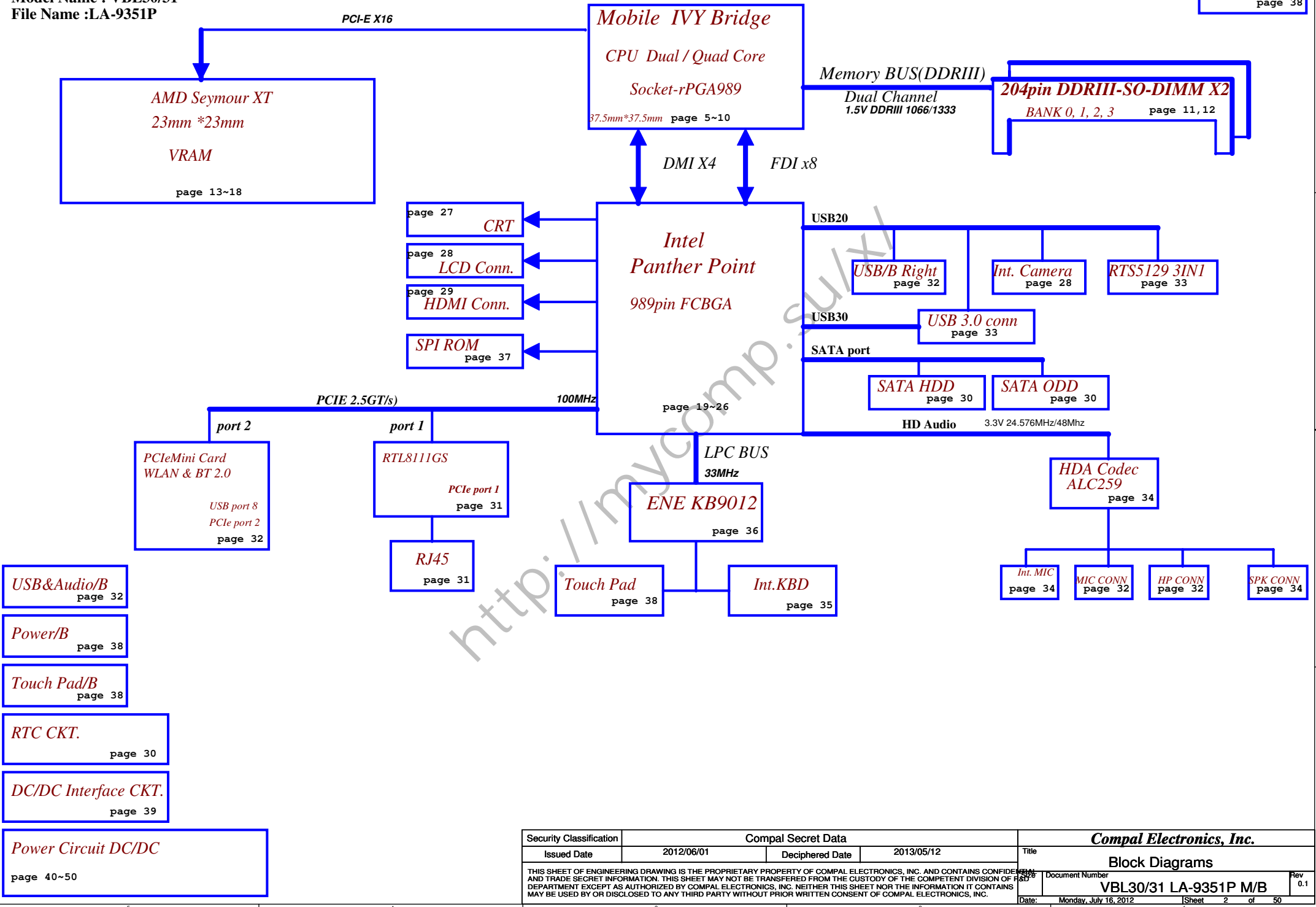
Compal Confidential

VBL30/31

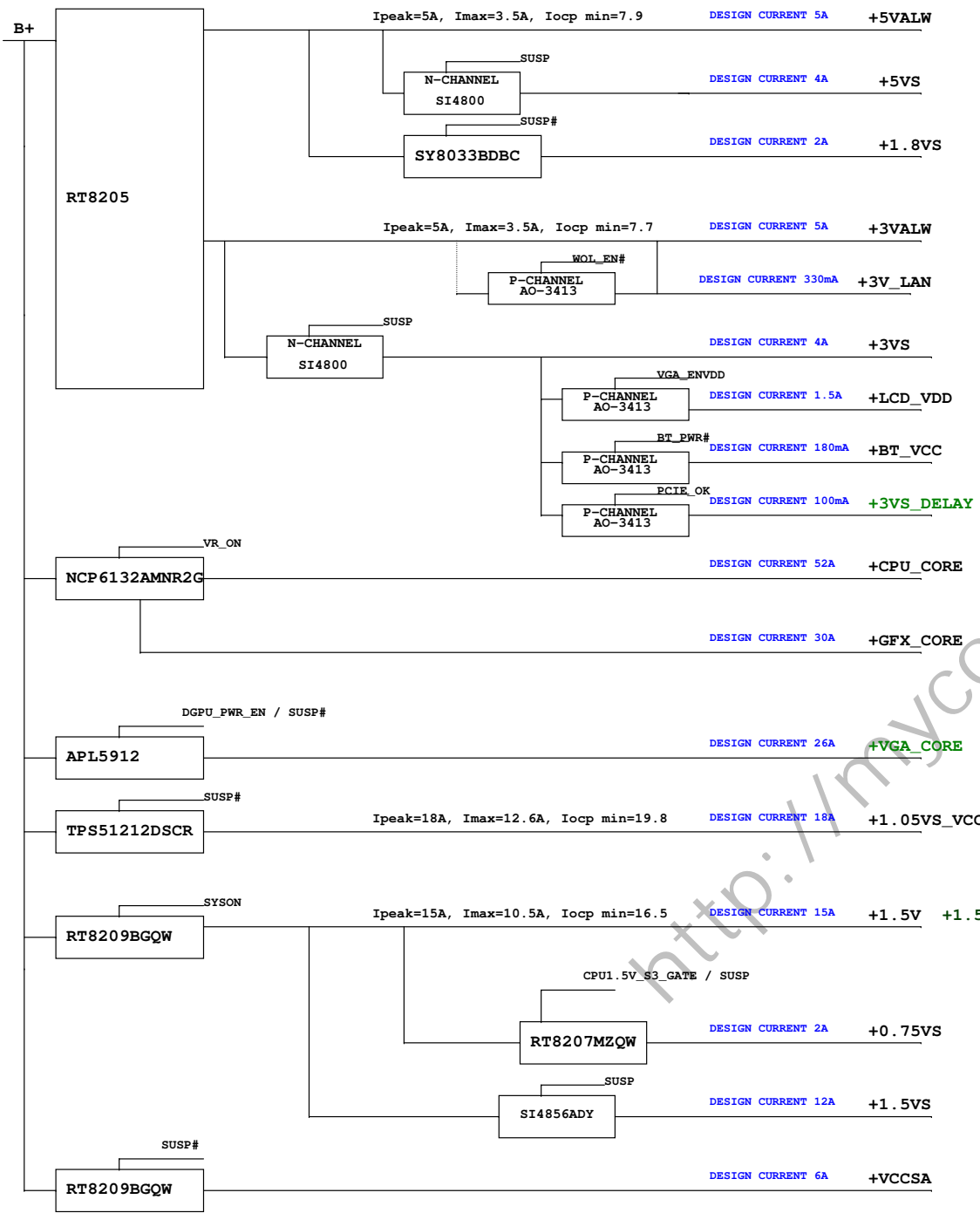
LA-9351P REV0.1 Schematic

Intel Ivy Bridge/Panther Point
AMD Seymour XT
2012-05-08 Rev 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	Cover Page
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Block Diagrams
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Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG
State		+3VALW	+1.5V_IO	+1.8VS +0.75VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

@	Reserve
CONN@	ME CONNECTOR
KB9012@	ENE EC
Nuvton@	Nuvton EC
NOW8@	not Support Win8
WIN8@	Support Win8
UMA@	UMA Sku
PX@	PX Sku

EC SM Bus1 address

Power	Device	Address
+3VALW	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	VGA Internal thermal sensor	1001 111Xb (0x9E)

PCH SM Bus address

Power	Device	Address
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b

SMBUS Control Table

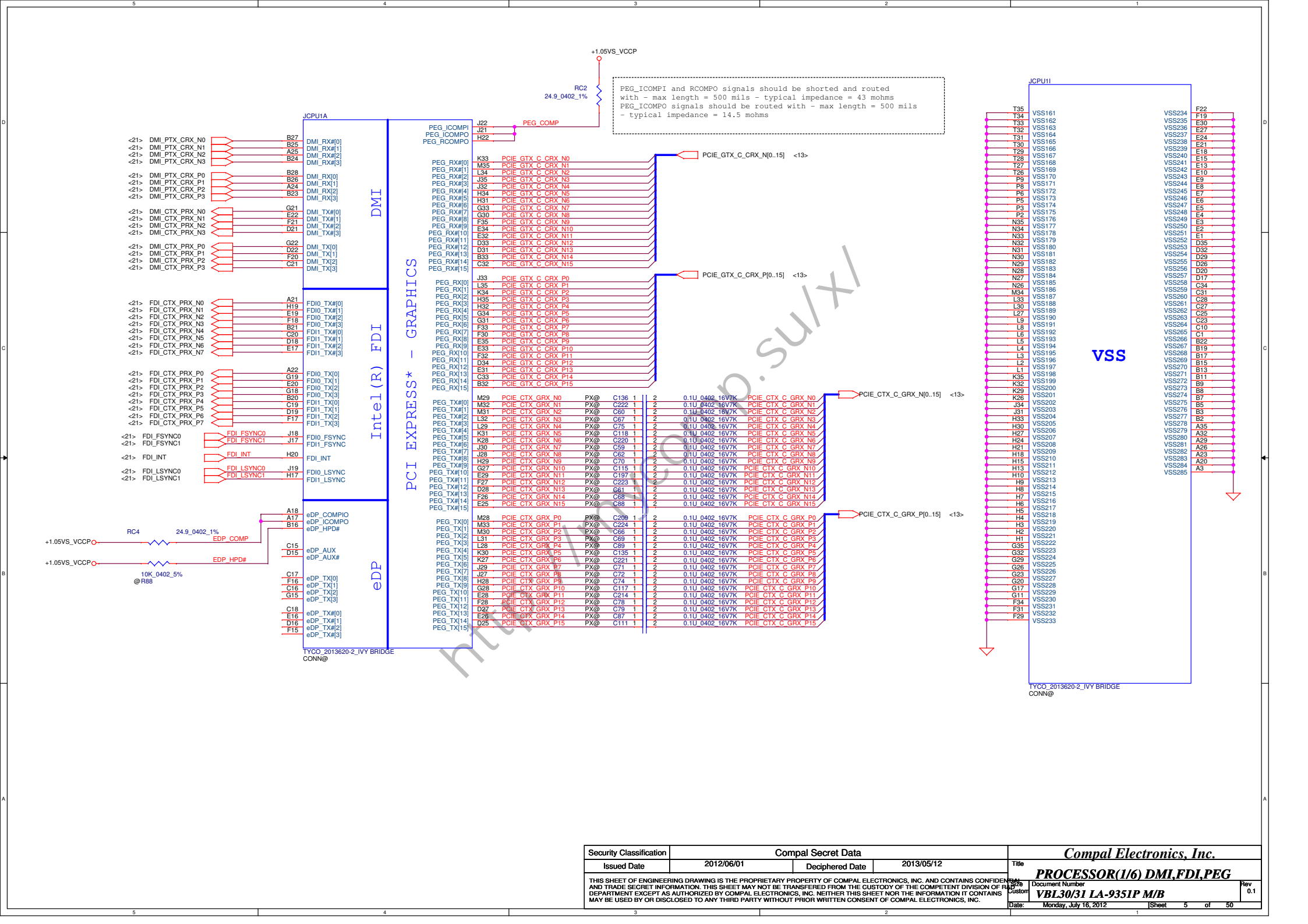
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW	X	+3VALW	X	X	X	X	X
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW	X	X	X	X	X	X	+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW	X	X	X	+3VS	+3VS	X	X
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW	X	X	X	X	X	X	X
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS	X	+3VS	X	X	+3VS	X

PCH X76 and PCBA table

		config
X76	ZZZ X76@ HYN 1G	ZZZ @ HYN 1G
	ZZZ X76@ SAM 1G	R359 @ 10K_0402_5%
PCH	UH1 BD82HM70 QPXH C1 BGA 989P PCH@	R61 @ 10K_0402_5%
		R462 @ 10K_0402_5%
PCB	ZZZ DAZ@	R360 @ 10K_0402_5%
	ZZZ DA8@	R61 @ 10K_0402_5%
	ZZZ DA4@	R461 @ 10K_0402_5%
	ZZZ DA2@	R461 @ 10K_0402_5%

(@/CONN@/DA2@/DA4@/DA8@/DAZ@/KB9012@/NOW8@/Nuvton@/PCH@/PX@/Rev01@/Rev02@/Rev03@/Rev04@/Rev10@/UMA@/WIN8@/X76@)

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				Notes List
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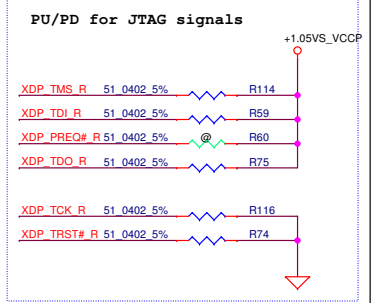
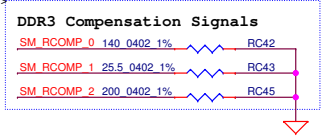
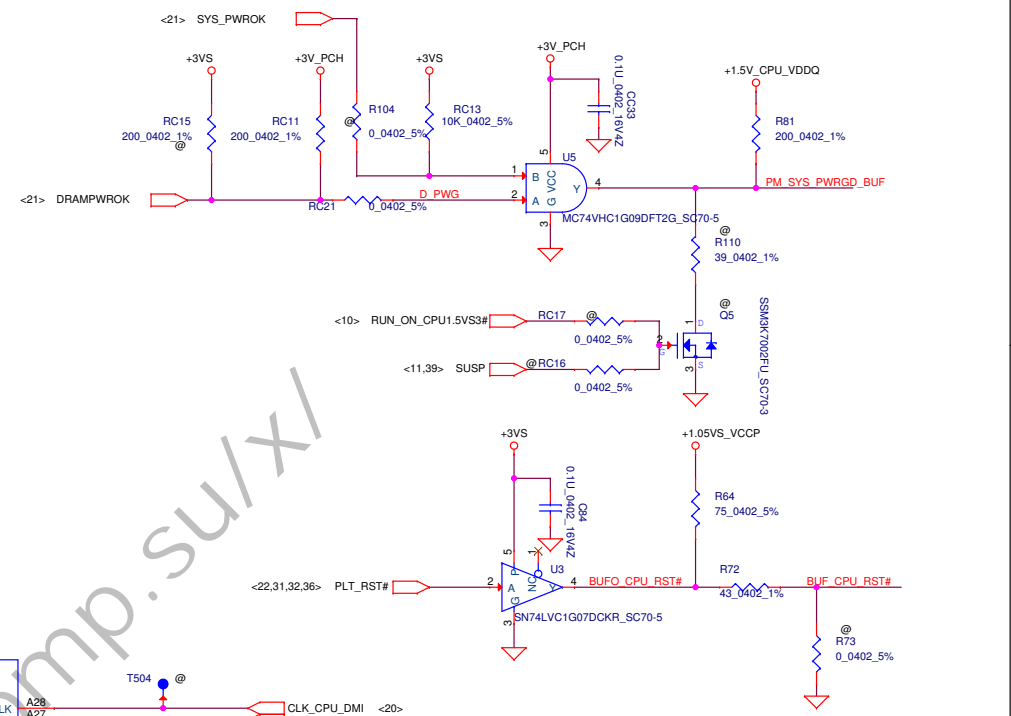
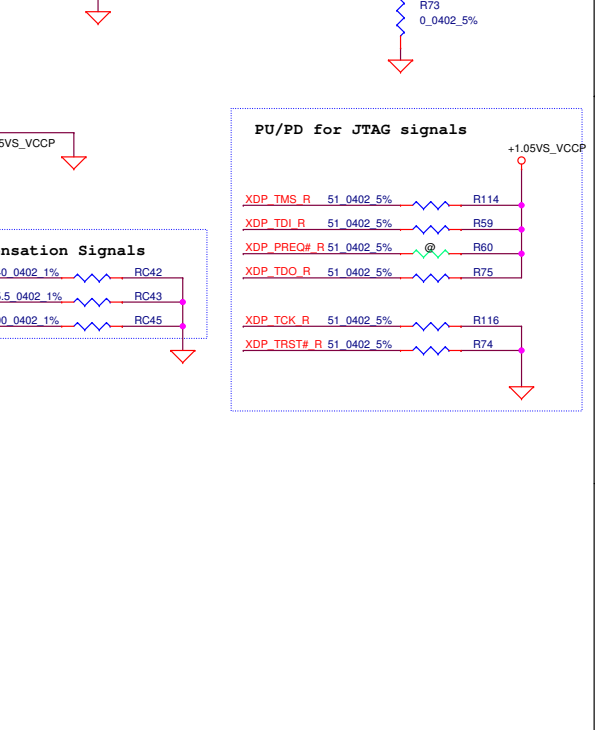
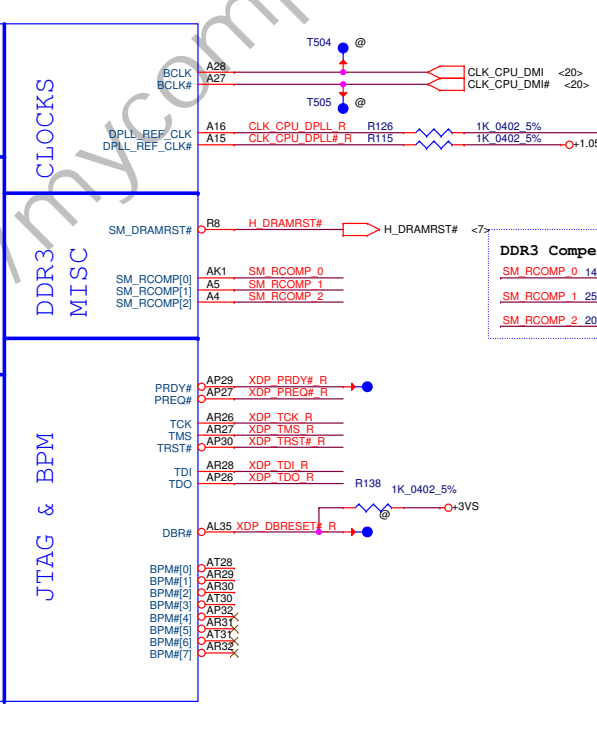
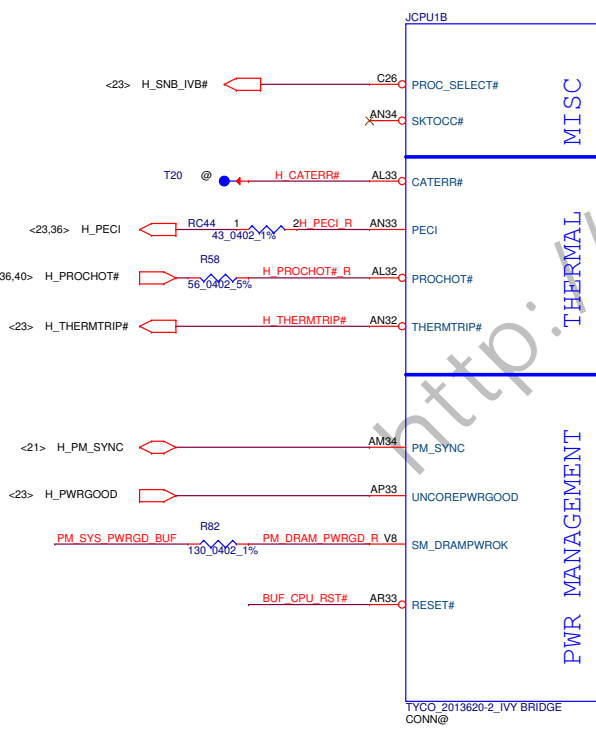
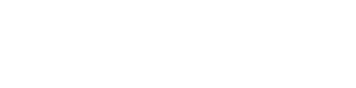
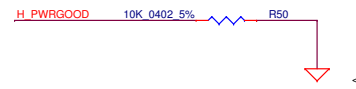
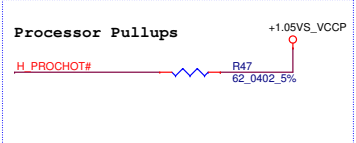


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

Intel(R) FDI
 PCI EXPRESS* - GRAPHICS

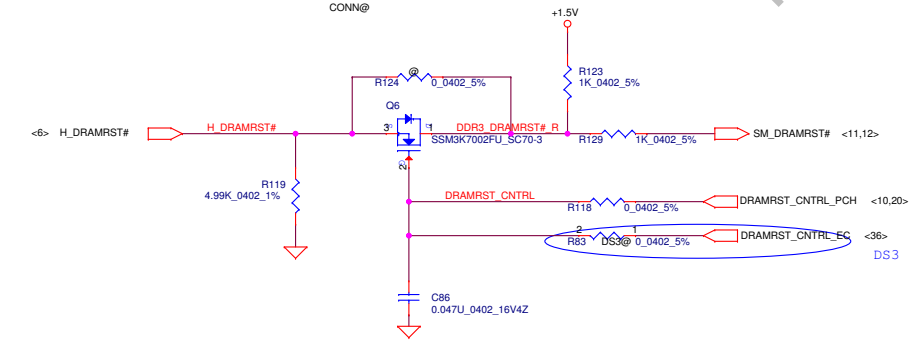
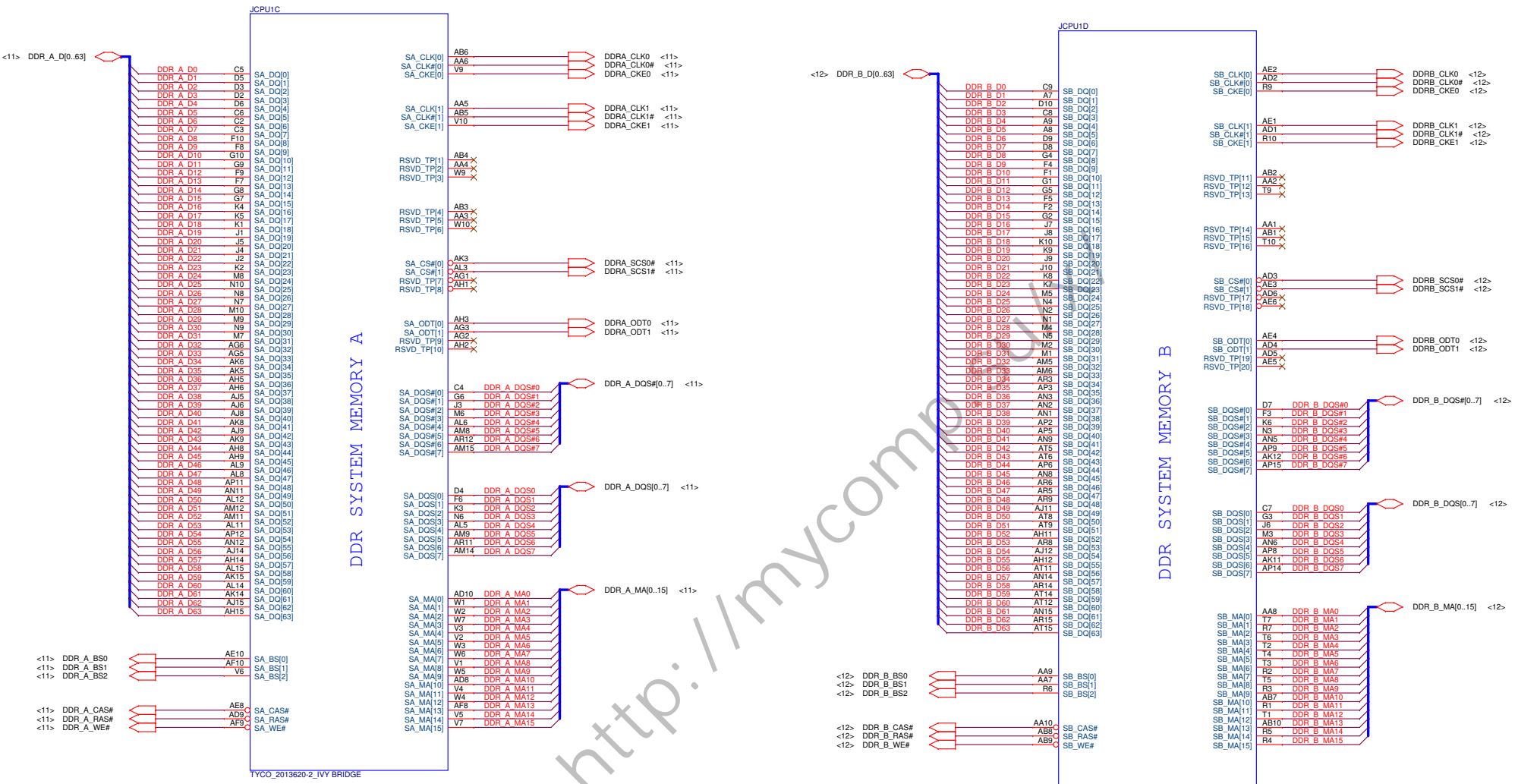
Signal	Component	Value	Notes
PEG_RX#0	K33	PCIE GTX C CRX N0	
PEG_RX#1	M35	PCIE GTX C CRX N1	
PEG_RX#2	L34	PCIE GTX C CRX N2	
PEG_RX#3	J35	PCIE GTX C CRX N3	
PEG_RX#4	J32	PCIE GTX C CRX N4	
PEG_RX#5	H34	PCIE GTX C CRX N5	
PEG_RX#6	H31	PCIE GTX C CRX N6	
PEG_RX#7	G33	PCIE GTX C CRX N7	
PEG_RX#8	G30	PCIE GTX C CRX N8	
PEG_RX#9	F35	PCIE GTX C CRX N9	
PEG_RX#10	E34	PCIE GTX C CRX N10	
PEG_RX#11	E32	PCIE GTX C CRX N11	
PEG_RX#12	D33	PCIE GTX C CRX N12	
PEG_RX#13	D31	PCIE GTX C CRX N13	
PEG_RX#14	B33	PCIE GTX C CRX N14	
PEG_RX#15	C32	PCIE GTX C CRX N15	
PEG_TX#0	J33	PCIE GTX C CRX P0	
PEG_TX#1	L35	PCIE GTX C CRX P1	
PEG_TX#2	K34	PCIE GTX C CRX P2	
PEG_TX#3	H35	PCIE GTX C CRX P3	
PEG_TX#4	H32	PCIE GTX C CRX P4	
PEG_TX#5	G34	PCIE GTX C CRX P5	
PEG_TX#6	G31	PCIE GTX C CRX P6	
PEG_TX#7	F33	PCIE GTX C CRX P7	
PEG_TX#8	F30	PCIE GTX C CRX P8	
PEG_TX#9	E35	PCIE GTX C CRX P9	
PEG_TX#10	E33	PCIE GTX C CRX P10	
PEG_TX#11	F32	PCIE GTX C CRX P11	
PEG_TX#12	D34	PCIE GTX C CRX P12	
PEG_TX#13	E31	PCIE GTX C CRX P13	
PEG_TX#14	C33	PCIE GTX C CRX P14	
PEG_TX#15	B32	PCIE GTX C CRX P15	
PEG_TX#0	M29	PCIE CTX GRX N0	PX@ C136 1 2
PEG_TX#1	M32	PCIE CTX GRX N1	PX@ C222 1 2
PEG_TX#2	M31	PCIE CTX GRX N2	PX@ C60 1 2
PEG_TX#3	L32	PCIE CTX GRX N3	PX@ C67 1 2
PEG_TX#4	L29	PCIE CTX GRX N4	PX@ C75 2 2
PEG_TX#5	K31	PCIE CTX GRX N5	PX@ C113 1 2
PEG_TX#6	K28	PCIE CTX GRX N6	PX@ C220 1 2
PEG_TX#7	J30	PCIE CTX GRX N7	PX@ C59 1 2
PEG_TX#8	J28	PCIE CTX GRX N8	PX@ C62 1 2
PEG_TX#9	H29	PCIE CTX GRX N9	PX@ C70 1 2
PEG_TX#10	G27	PCIE CTX GRX N10	PX@ C115 1 2
PEG_TX#11	E29	PCIE CTX GRX N11	PX@ C197 1 2
PEG_TX#12	P27	PCIE CTX GRX N12	PX@ C223 2 2
PEG_TX#13	D28	PCIE CTX GRX N13	PX@ C61 1 2
PEG_TX#14	F26	PCIE CTX GRX N14	PX@ C88 1 2
PEG_TX#15	E25	PCIE CTX GRX N15	PX@ C88 1 2
PEG_TX#0	M28	PCIE CTX GRX P0	PX@ C209 1 2
PEG_TX#1	M33	PCIE CTX GRX P1	PX@ C224 1 2
PEG_TX#2	M30	PCIE CTX GRX P2	PX@ C66 1 2
PEG_TX#3	L31	PCIE CTX GRX P3	PX@ C69 1 2
PEG_TX#4	K30	PCIE CTX GRX P4	PX@ C135 1 2
PEG_TX#5	K27	PCIE CTX GRX P5	PX@ C221 1 2
PEG_TX#6	J29	PCIE CTX GRX P6	PX@ C71 1 2
PEG_TX#7	J27	PCIE CTX GRX P7	PX@ C72 1 2
PEG_TX#8	H28	PCIE CTX GRX P8	PX@ C74 1 2
PEG_TX#9	G28	PCIE CTX GRX P9	PX@ C117 1 2
PEG_TX#10	E28	PCIE CTX GRX P10	PX@ C214 1 2
PEG_TX#11	F28	PCIE CTX GRX P11	PX@ C78 1 2
PEG_TX#12	D27	PCIE CTX GRX P12	PX@ C79 1 2
PEG_TX#13	E26	PCIE CTX GRX P13	PX@ C87 1 2
PEG_TX#14	D25	PCIE CTX GRX P14	PX@ C111 1 2
PEG_TX#15			

Signal	Component	Value
T35	VSS161	
T34	VSS162	
T33	VSS163	
T32	VSS164	
T31	VSS165	
T30	VSS166	
T29	VSS167	
T28	VSS168	
T27	VSS169	
T26	VSS170	
T25	VSS171	
T24	VSS172	
T23	VSS173	
T22	VSS174	
T21	VSS175	
T20	VSS176	
T19	VSS177	
T18	VSS178	
T17	VSS179	
T16	VSS180	
T15	VSS181	
T14	VSS182	
T13	VSS183	
T12	VSS184	
T11	VSS185	
T10	VSS186	
T09	VSS187	
T08	VSS188	
T07	VSS189	
T06	VSS190	
T05	VSS191	
T04	VSS192	
T03	VSS193	
T02	VSS194	
T01	VSS195	
L3	VSS196	
L2	VSS197	
L1	VSS198	
K35	VSS199	
K32	VSS200	
K29	VSS201	
K26	VSS202	
J34	VSS203	
J31	VSS204	
H33	VSS205	
H30	VSS206	
H27	VSS207	
H24	VSS208	
H18	VSS209	
H15	VSS210	
H13	VSS211	
H10	VSS212	
H9	VSS213	
H7	VSS214	
H6	VSS215	
H5	VSS216	
H4	VSS217	
H3	VSS218	
H2	VSS219	
H1	VSS220	
G35	VSS221	
G32	VSS222	
G29	VSS223	
G26	VSS224	
G23	VSS225	
G20	VSS226	
G17	VSS227	
G13	VSS228	
G11	VSS229	
F34	VSS230	
F31	VSS231	
F29	VSS232	
F28	VSS233	
F22	VSS234	
F19	VSS235	
F18	VSS236	
F17	VSS237	
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E5	VSS248	
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E3	VSS250	
E2	VSS251	
E1	VSS252	
D35	VSS253	
D32	VSS254	
D29	VSS255	
D26	VSS256	
D25	VSS257	
D24	VSS258	
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D16	VSS266	
D15	VSS267	
D14	VSS268	
D13	VSS269	
D12	VSS270	
D11	VSS271	
D10	VSS272	
D9	VSS273	
D8	VSS274	
D7	VSS275	
D6	VSS276	
D5	VSS277	
D4	VSS278	
D3	VSS279	
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A26	VSS282	
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A3	VSS285	



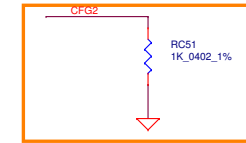
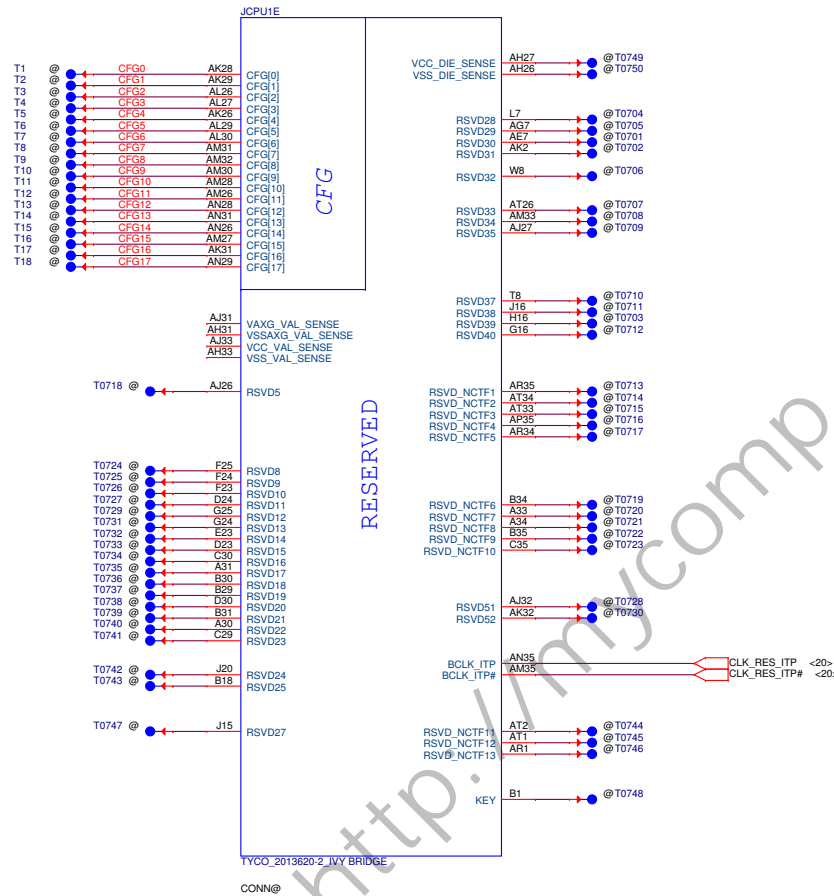
TYCO_2013620-2_IVY BRIDGE
CONN@

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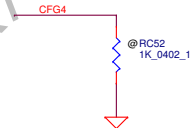


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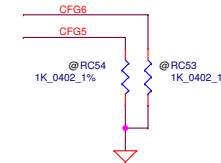
CFG Straps for Processor



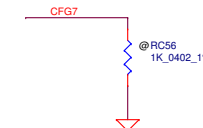
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



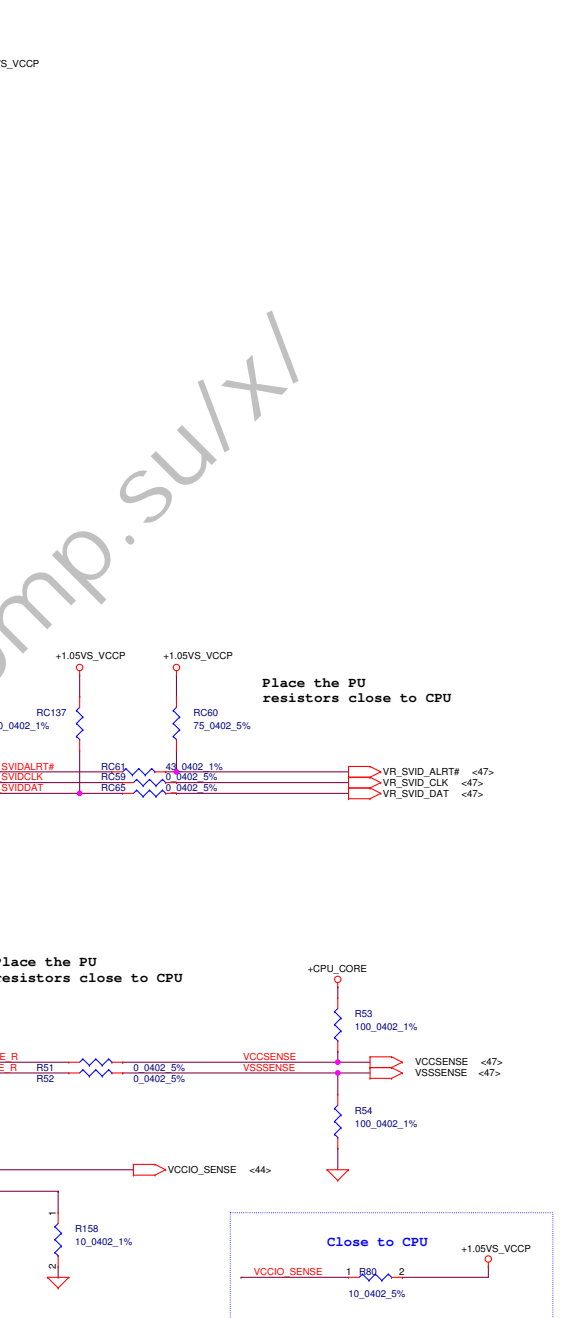
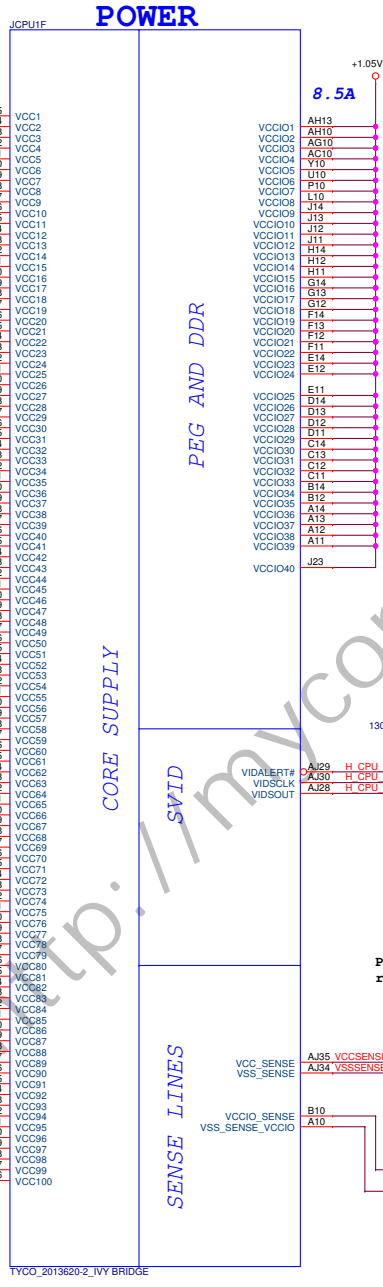
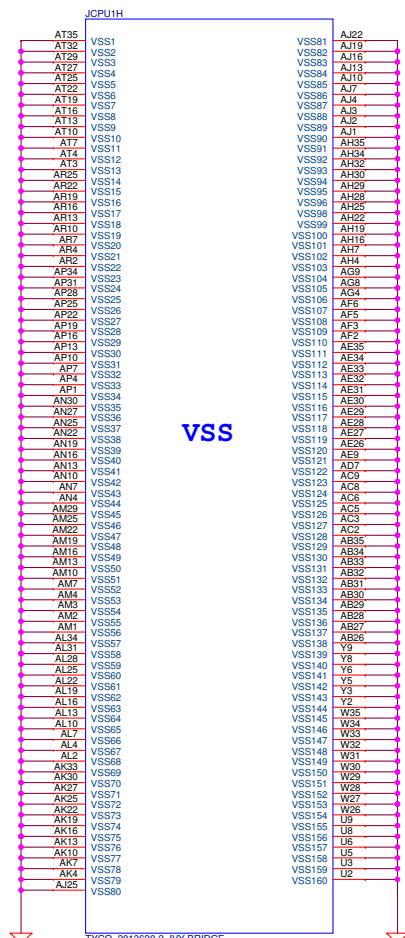
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



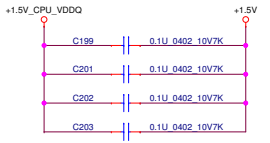
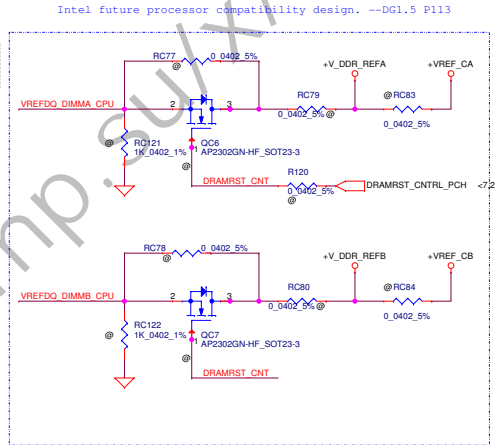
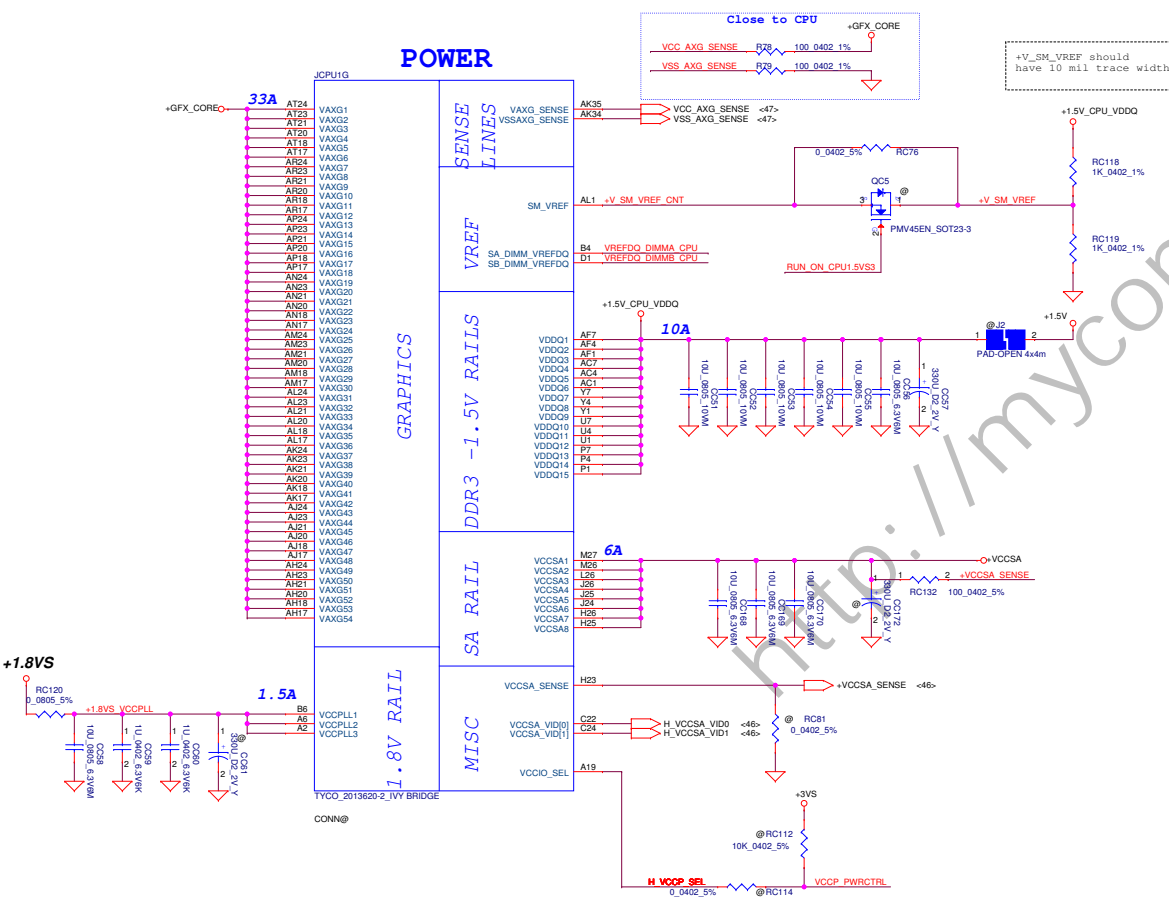
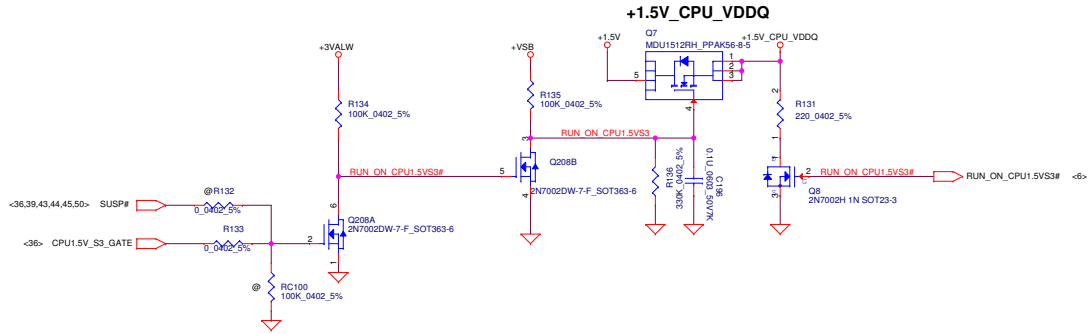
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training



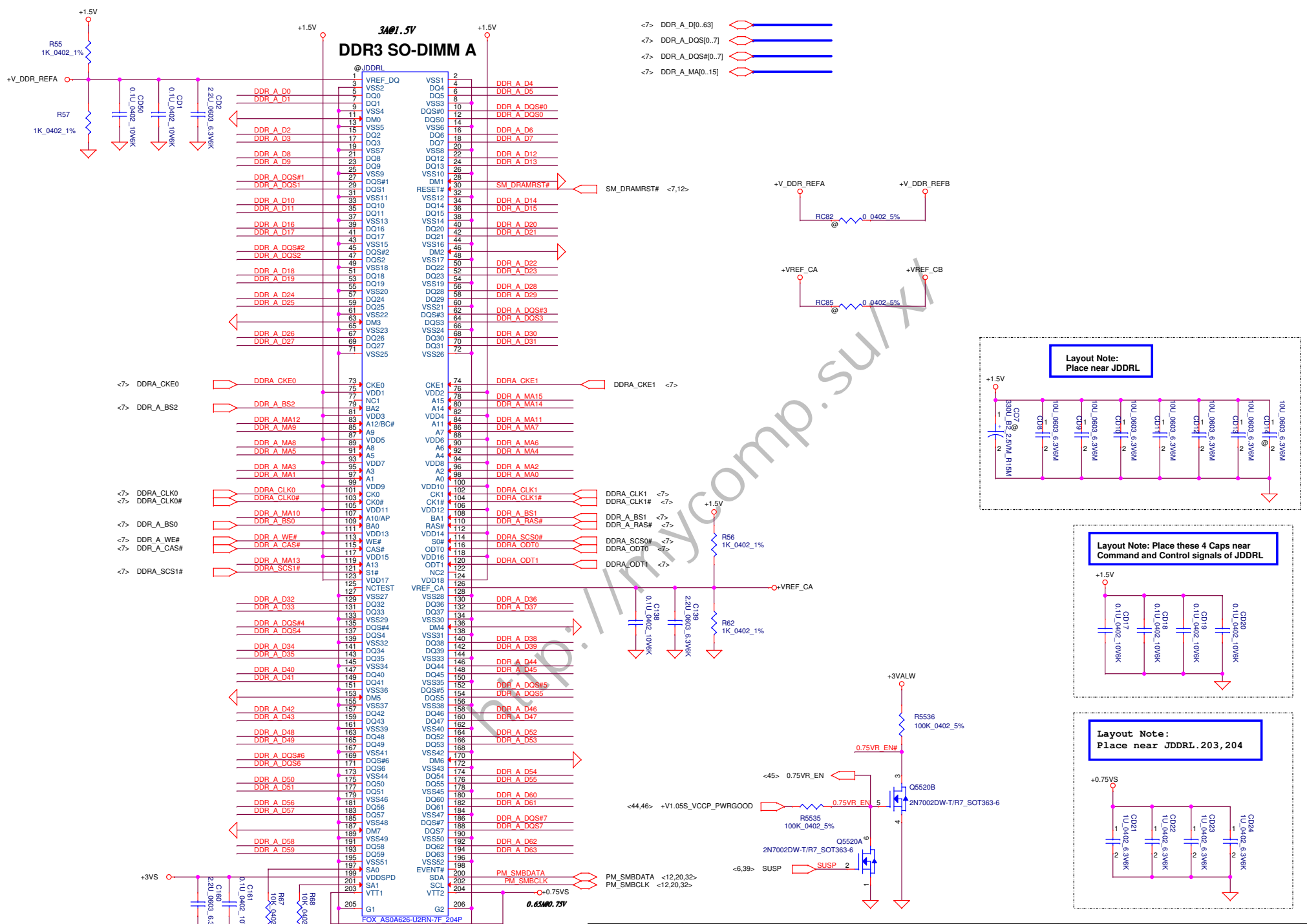
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				PROCESSOR(5/6) PWR,BYPASS
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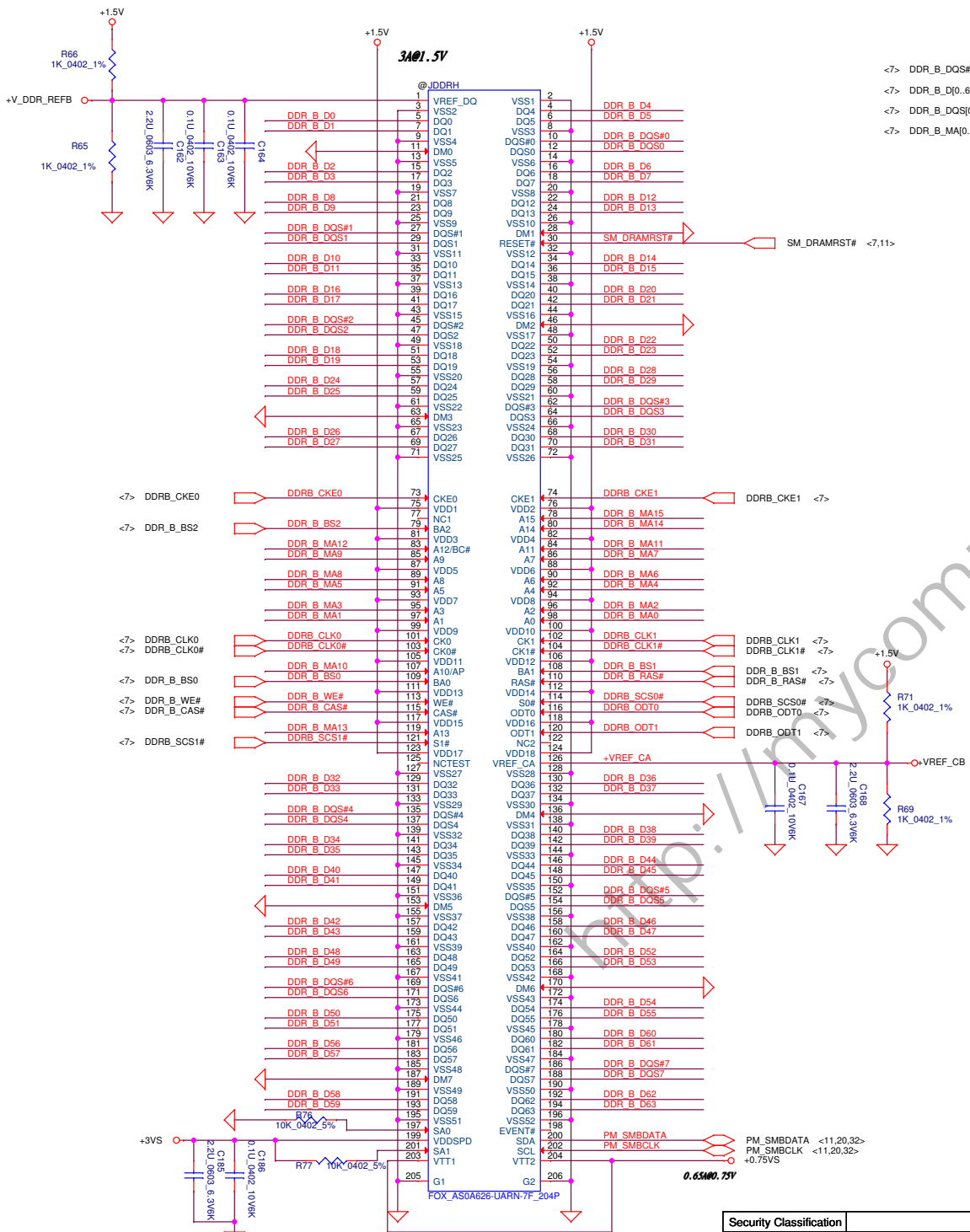
IVY Bridge drives VCCIO_SEL low
 VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
 VCCP_PWRCTRL:1

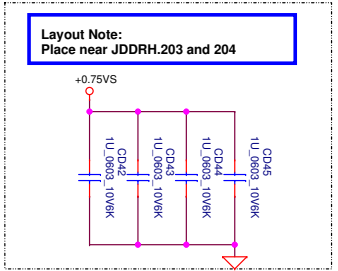
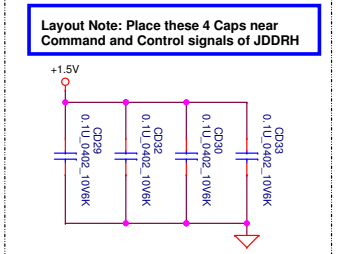
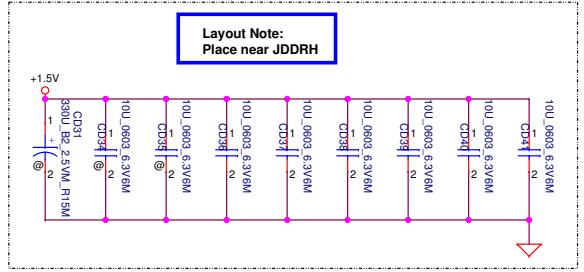
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	PROCESSOR(6/6) PWR,VSS	
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<small>Document Number</small> VPL30/31 LA-9351P M/B				<small>Rev</small> 0.1	
<small>Date</small> Monday, July 16, 2012				<small>Sheet</small> 10 of 50	



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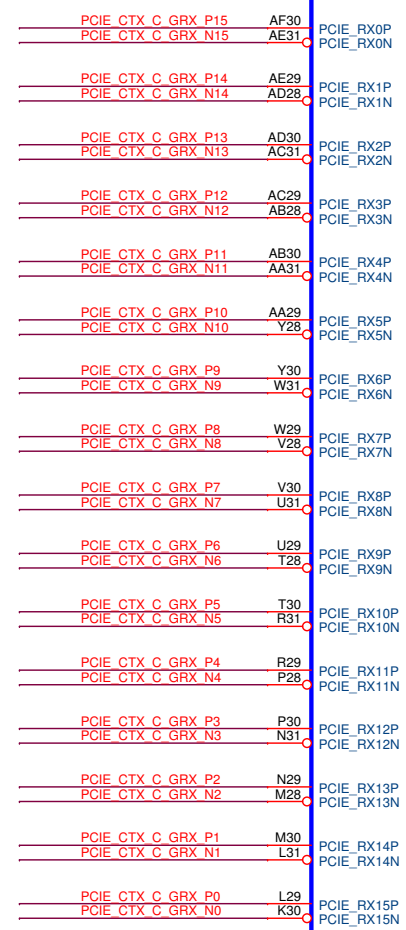
- <7> DDR_B_DQS#[0..7]
- <7> DDR_B_D[0..63]
- <7> DDR_B_DQS#[0..7]
- <7> DDR_B_MA#[0..15]



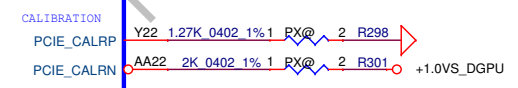
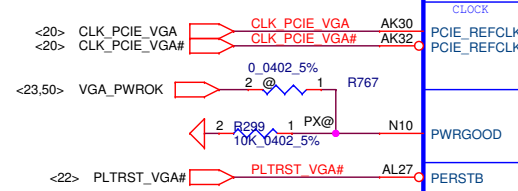
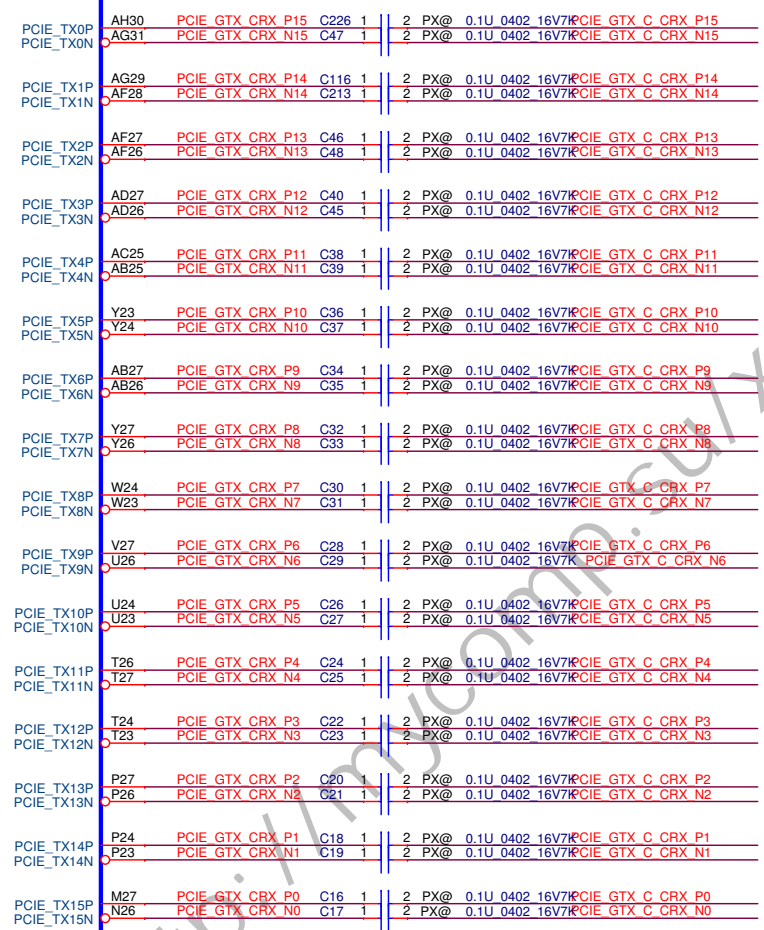
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				VBL30/31 LA-9351P/M/B	
				Sheet 12 of 50	

<5> PCIE_CTX_C_GRX_P[15..0] → PCIE_CTX_C_GRX_P[15..0]
 <5> PCIE_CTX_C_GRX_N[15..0] → PCIE_CTX_C_GRX_N[15..0]

PCIE GTX C CRX P[0..15] → PCIE GTX_C_CRX_P[0..15] <5>
 PCIE GTX C CRX N[0..15] → PCIE GTX_C_CRX_N[0..15] <5>

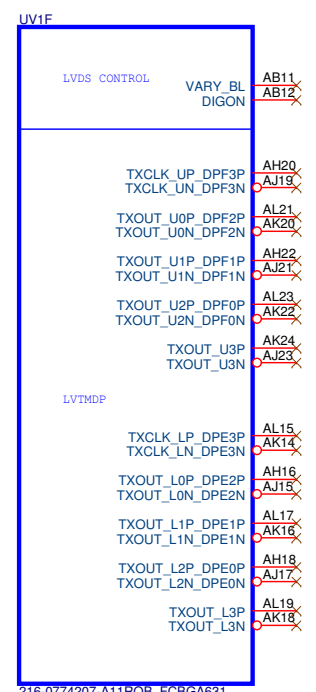


PCI EXPRESS INTERFACE



216-0774207-A111ROB_FCBGA631
 PX@

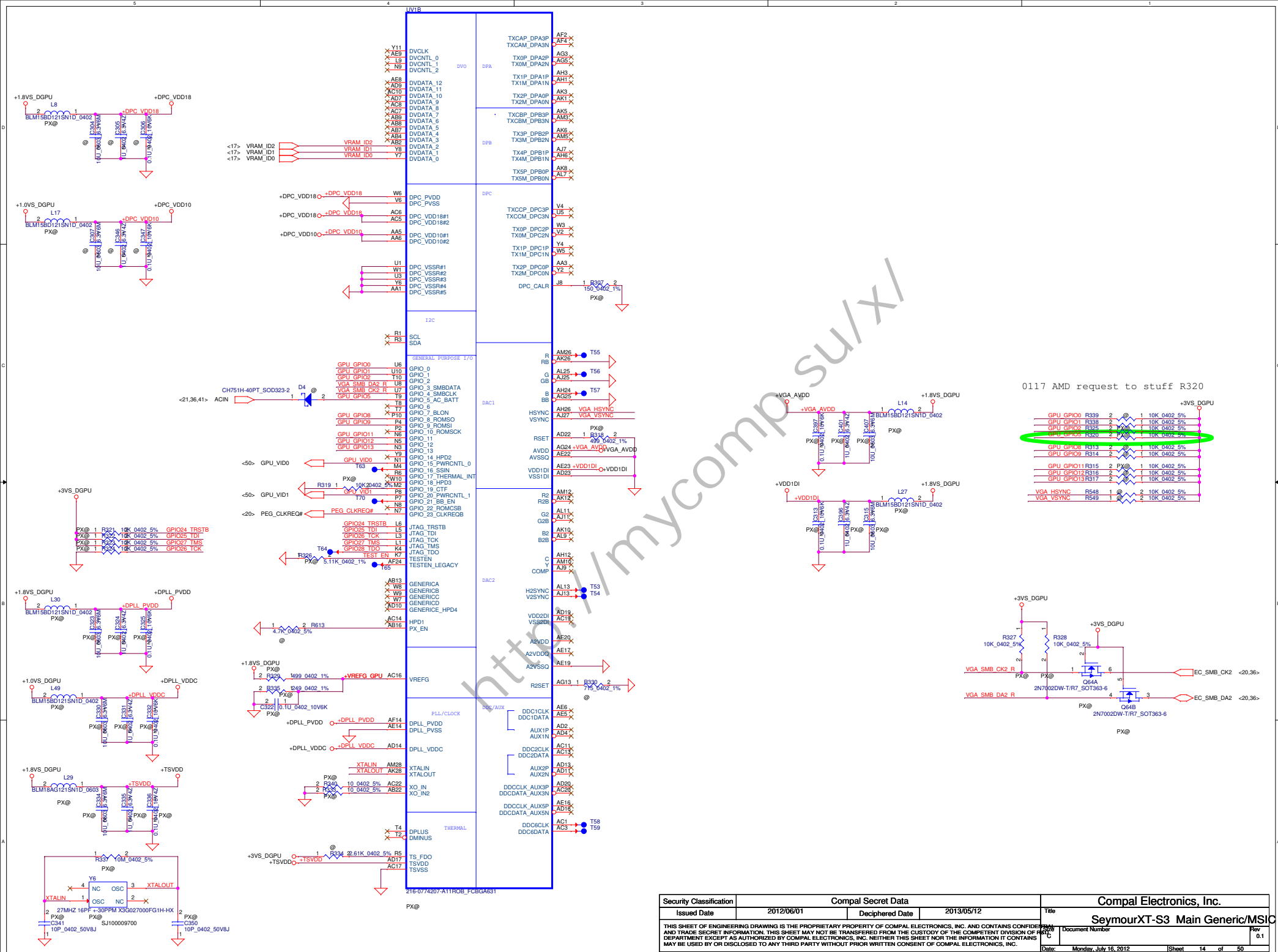
PCIE LANE



216-0774207-A111ROB_FCBGA631

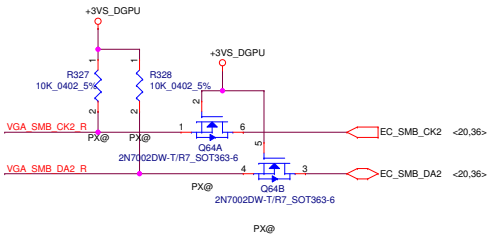
PX@ **LVDS**

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				Document Number	Rev 0.1
				Date: Monday, July 16, 2012	Sheet 13 of 50

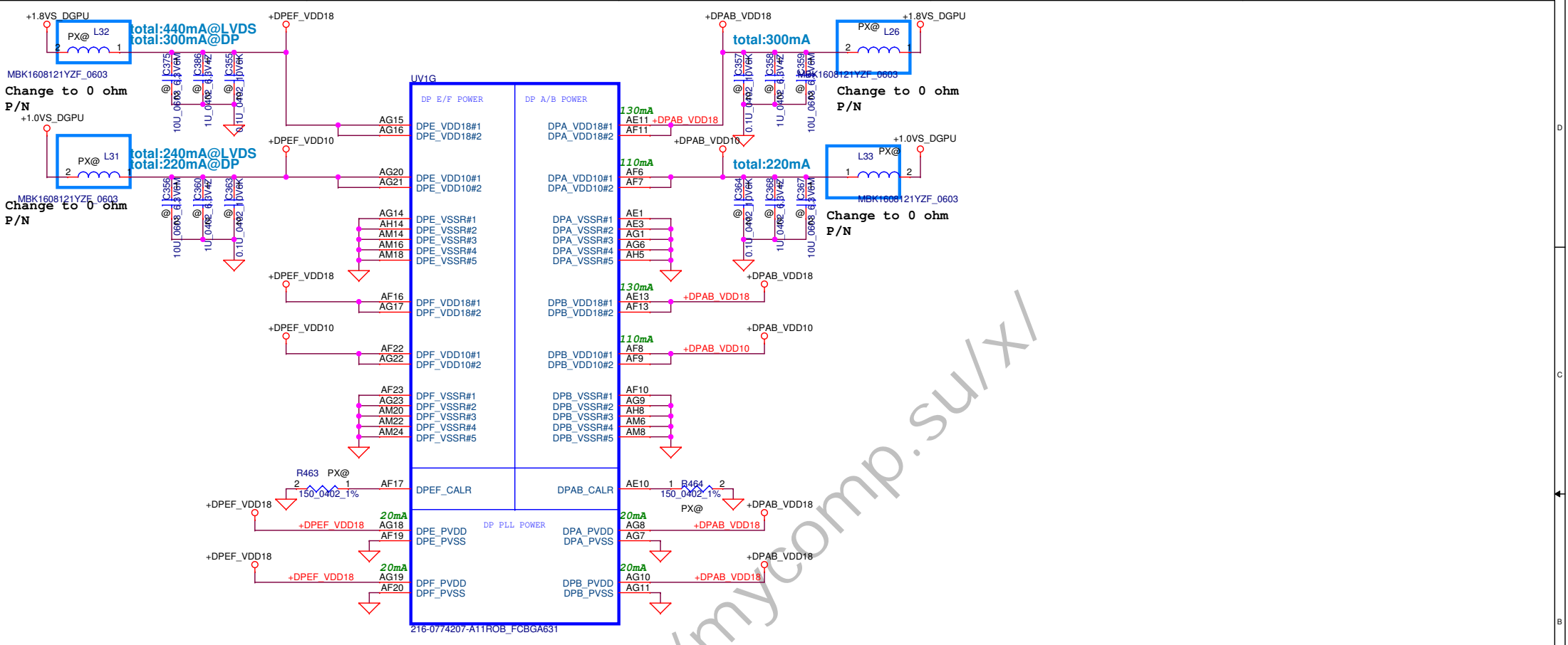


0117 AMD request to stuff R320

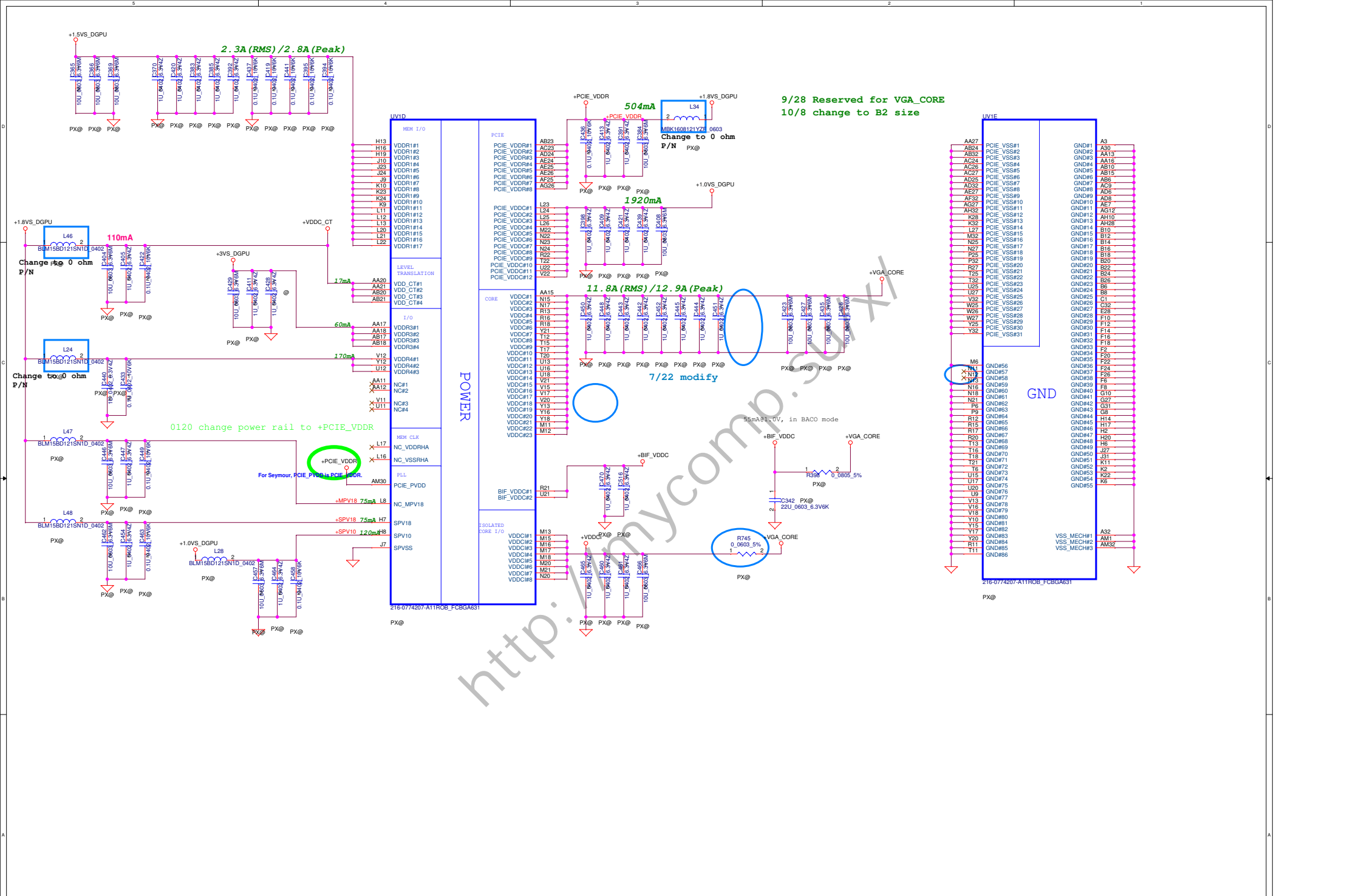
Component	Value	Quantity	Footprint	Part	Notes
GPU GPIO0	R339	2	0603	10K 0402 5%	
GPU GPIO1	R338	2	0603	10K 0402 5%	
GPU GPIO2	R325	2	0603	10K 0402 5%	
GPU GPIO3	R320	2	0603	10K 0402 5%	
GPU GPIO4	R313	2	0603	10K 0402 5%	
GPU GPIO5	R314	2	0603	10K 0402 5%	
GPU GPIO11	R315	2	0603	10K 0402 5%	
GPU GPIO12	R316	2	0603	10K 0402 5%	
GPU GPIO13	R317	2	0603	10K 0402 5%	
VGA HSYNC	R548	1	0603	2 10K 0402 5%	
VGA VSYNC	R549	1	0603	2 10K 0402 5%	



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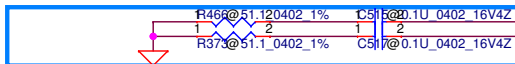
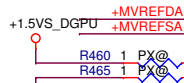
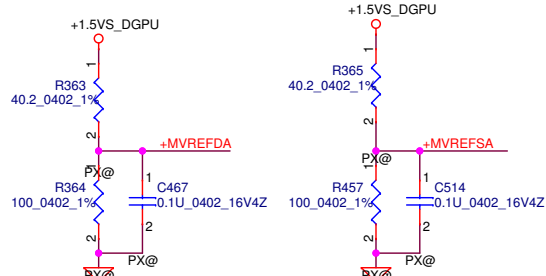
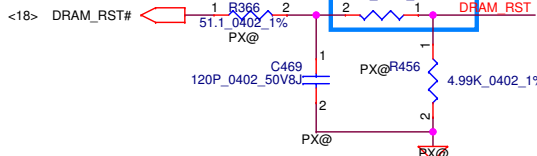
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	SeymourXT-S3 DP PWR
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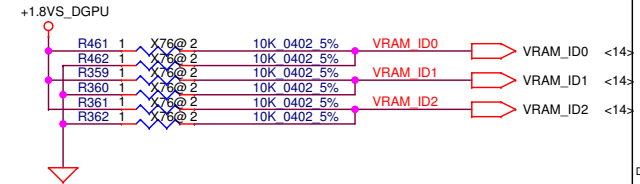
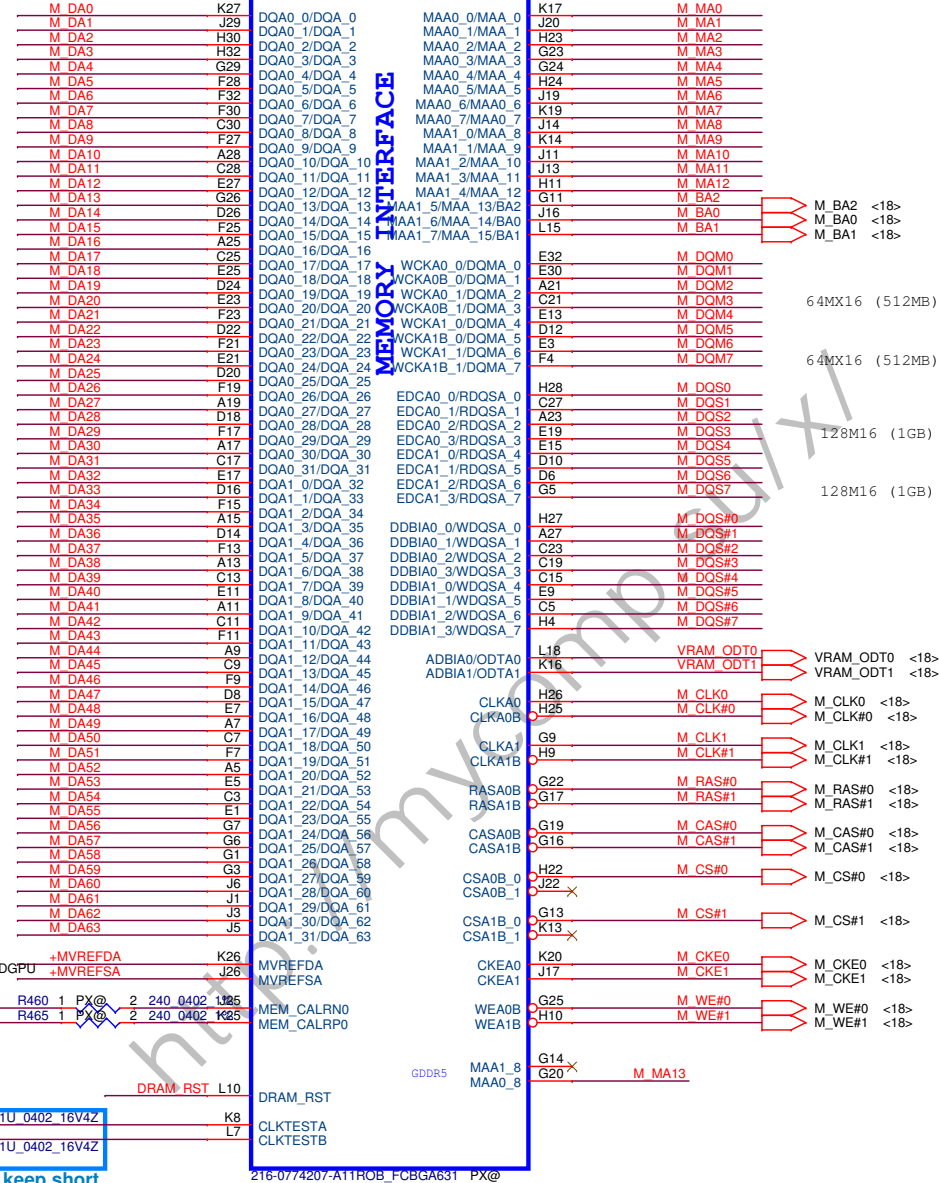
Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	SeymourXT-S3 PWR/GND	
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<18> M_DA[63..0] M_DA[63..0]
 <18> M_MA[13..0] M_MA[13..0]
 <18> M_DQM[7..0] M_DQM[7..0]
 <18> M_DQS[7..0] M_DQS[7..0]
 <18> M_DQS# [7..0] M_DQS# [7..0]

PARK SCL has different recommend
 9/28 change P/N to SD034100A00 R455



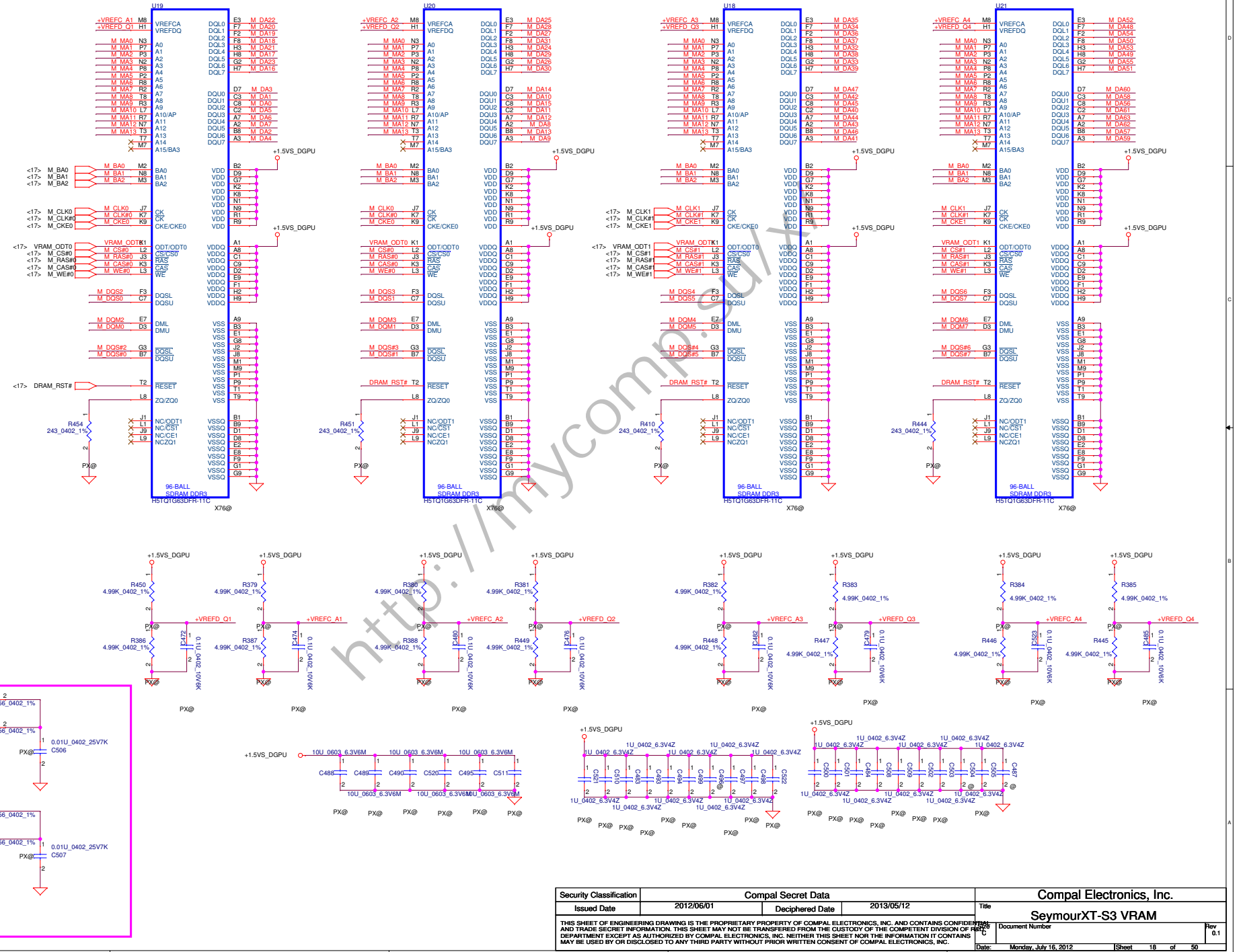
Route 50ohms single-ended/100ohm diff and keep short debug only, for clock observation, if not need, DNI.



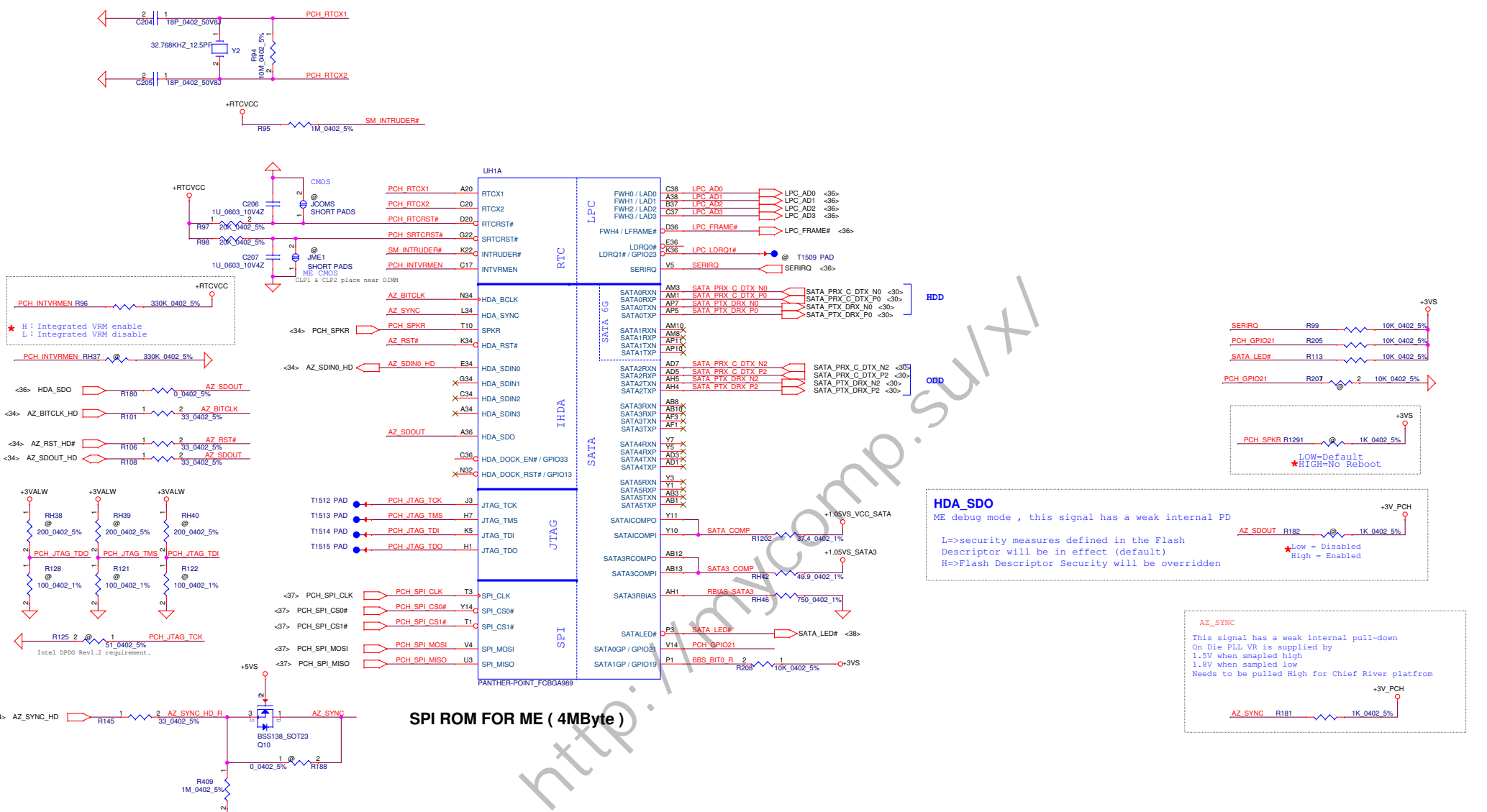
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 Samsung 128MB PN:SA00004GS00	R461	R360	R362
H5TQ1G63DFR-11C Hynix 128MB PN:SA000041S20	R462	R359	R362
K4W2G1646C-BC11 Samsung 256MB PN:SA000047Q00	R461	R360	R361
H5TQ2G63BFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003Y0A0	R462	R359	R361

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- <17> M_DA[63..0] <M_DA[63..0]>
- <17> M_MA[19..0] <M_MA[19..0]>
- <17> M_DQM[7..0] <M_DQM[7..0]>
- <17> M_DQS[7..0] <M_DQS[7..0]>
- <17> M_DQS[7..0] <M_DQS[7..0]>



ref 139-02 recommend
 add off page
 Park SCL recommend pu 60.4
 ohm to 1.5VGS 0619 update



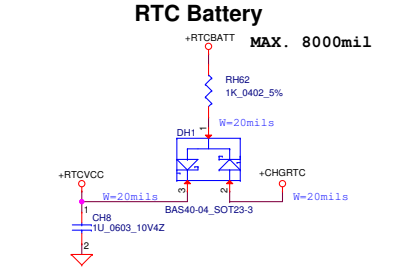
* H : Integrated VRM enable
 * L : Integrated VRM disable

+3VALW
 RH38 @ 200_0402_5%
 RH39 @ 200_0402_5%
 RH40 @ 200_0402_5%
 PCH_JTAG_TDO R128 @ 100_0402_1%
 PCH_JTAG_TMS R121 @ 100_0402_1%
 PCH_JTAG_TDI R122 @ 100_0402_1%
 R125 2 @ 51_0402_2%
 Intel DDPG Rev1.2 requirement.

SPI ROM FOR ME (4MByte)

HDA_SDO
 ME debug mode , this signal has a weak internal PD
 L=>security measures defined in the Flash Descriptor will be in effect (default)
 H=>Flash Descriptor Security will be overridden

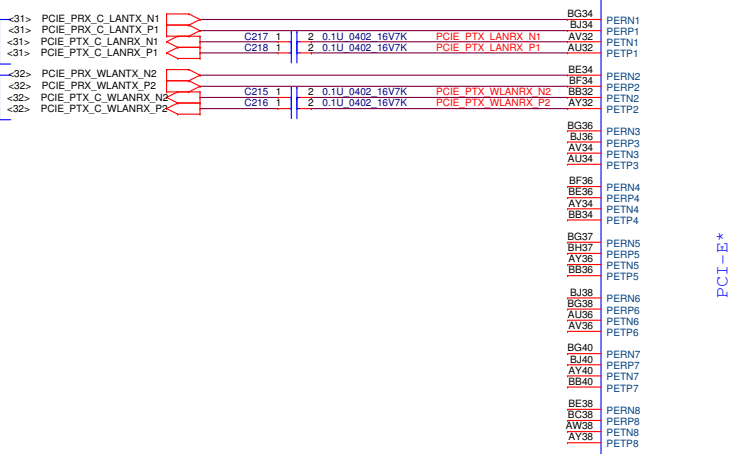
AZ_SYNC
 This signal has a weak internal pull-down
 On Die PLL VR is supplied by 1.5V when sampled high 1.8V when sampled low
 Needs to be pulled High for Chief River platform



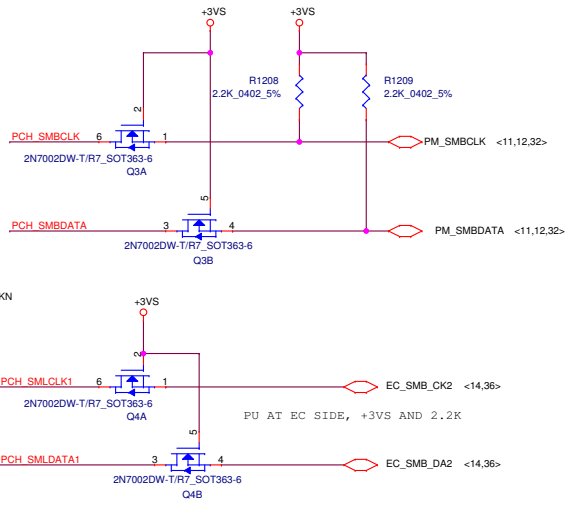
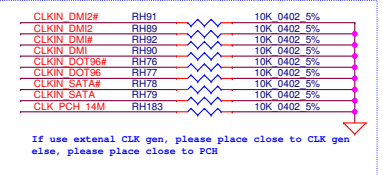
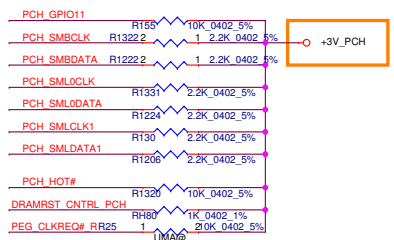
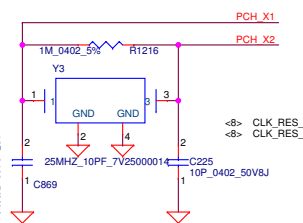
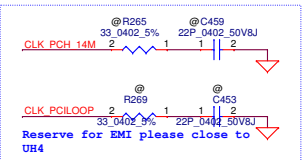
Security Classification	Compal Secret Data		Title	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	PCH (I/8) SATA,HDA,SPI, LPC
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Document Number	VBL30/31 LA-9351P M/B			Rev 0.1
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10/100/1G LAN ---->

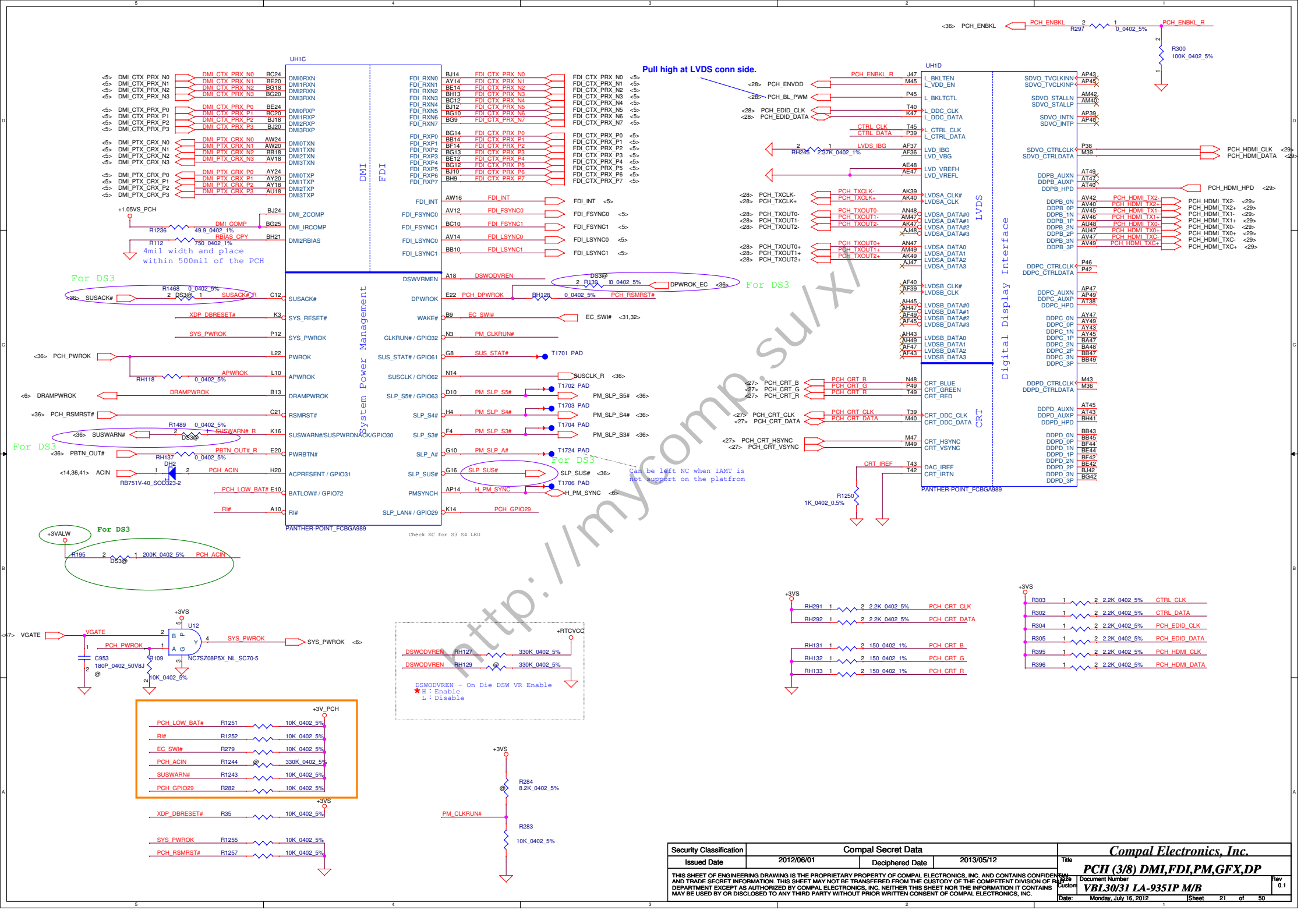
MiniWLAN (Mini Card 1)---->



10/100/1G LAN ---->



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Document Number				Rev	
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Date				Sheet	
Monday, July 16, 2012				20 of 50	



UH1C
 UH1D
 System Power Management
 Digital Display Interface

Pull high at LVDS conn side.

For DS3

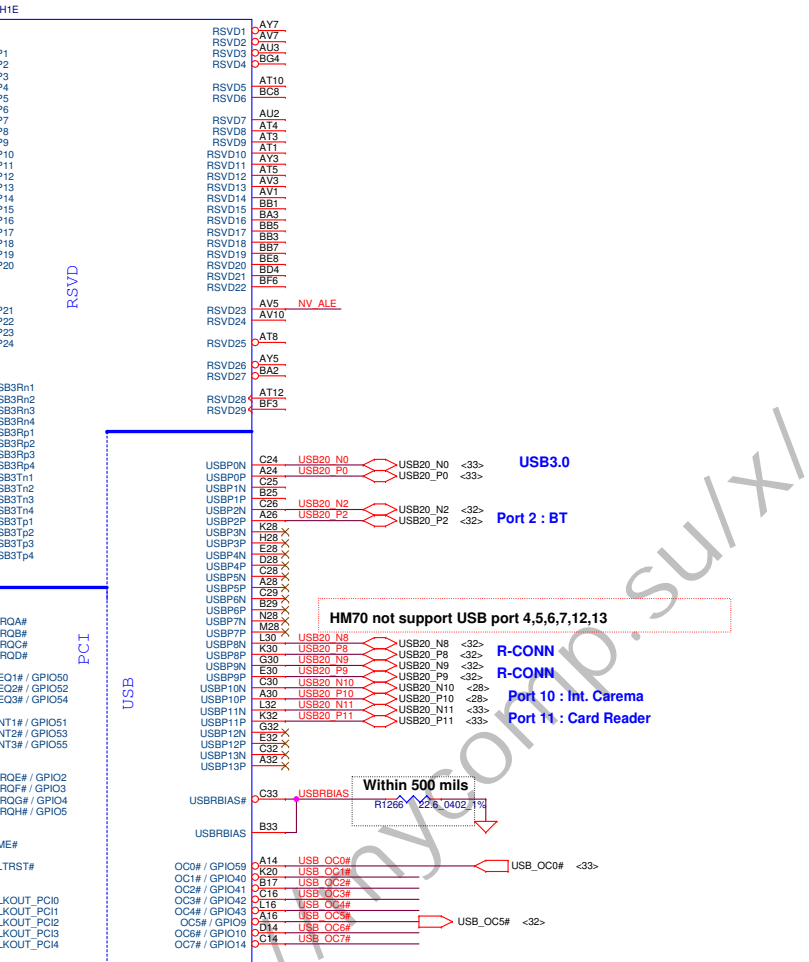
For DS3

For DS3

For DS3

Can be left NC when IAMT is not supported on the platform

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				VBL30/31 LA-9351P M/B	0.1
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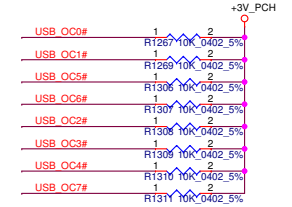
GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI *

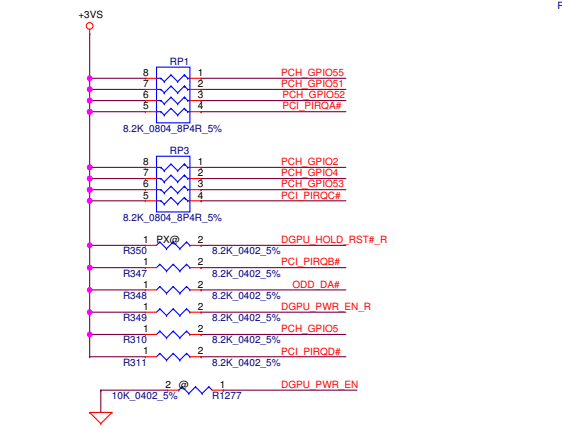
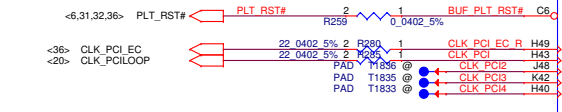
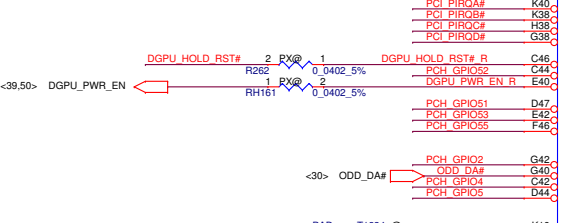
Intel Anti-Theft Techonlogy

NV_ALE	High-Enabled
Low=Disable(floating) *	

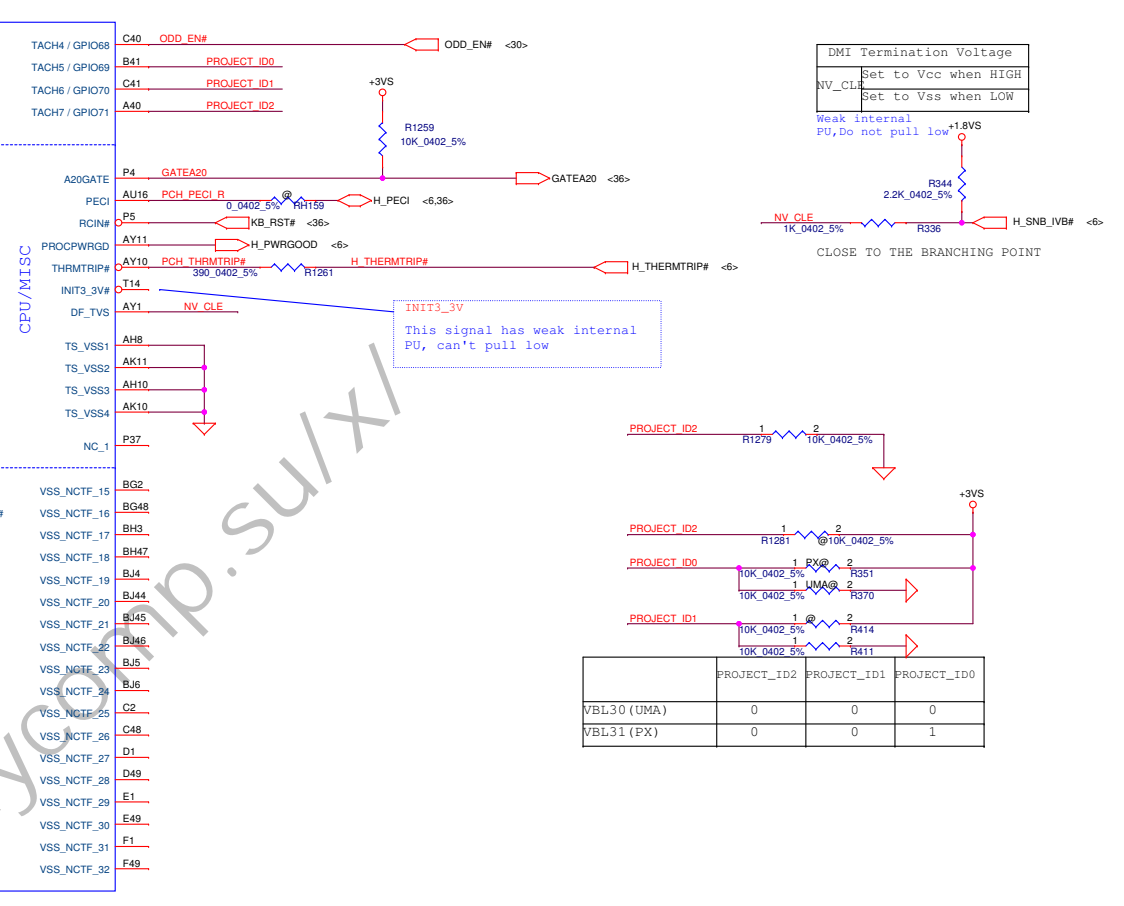
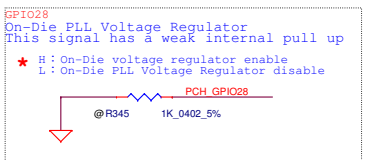
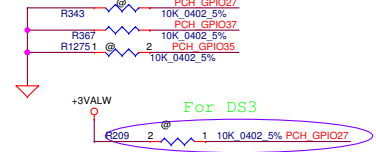
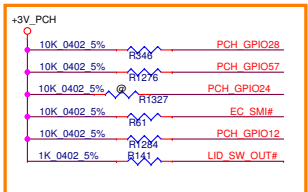
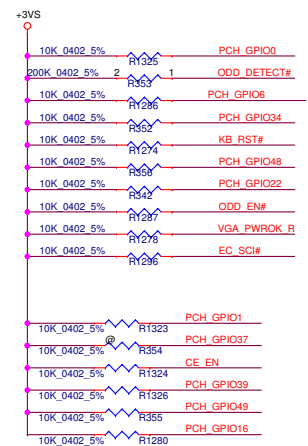
NV_ALE @R341 1K 0402 5% +1.8VS



- UH1E
- BG26 TP1
- B126 TP2
- BH25 TP3
- B116 TP3
- BG16 TP4
- AH38 TP5
- AH37 TP6
- AK43 TP7
- AK45 TP8
- TP9
- C18 TP10
- N30 TP10
- H3 TP11
- TP12
- AH12 TP13
- AM4 TP14
- TP15
- Y13 TP16
- K24 TP17
- L54 TP17
- AB46 TP18
- TP19
- AB45 TP20
- B21 TP21
- ME0 TP22
- AY16 TP23
- BG46 TP24

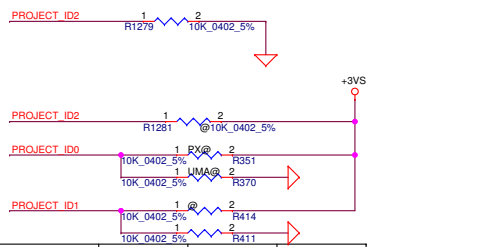


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				PCH (4/8) PCI, USB, NVRAM	
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DMI Termination Voltage
 NV_CL# Set to Vcc when HIGH
 Set to Vss when LOW
 Weak internal PU, Do not pull low

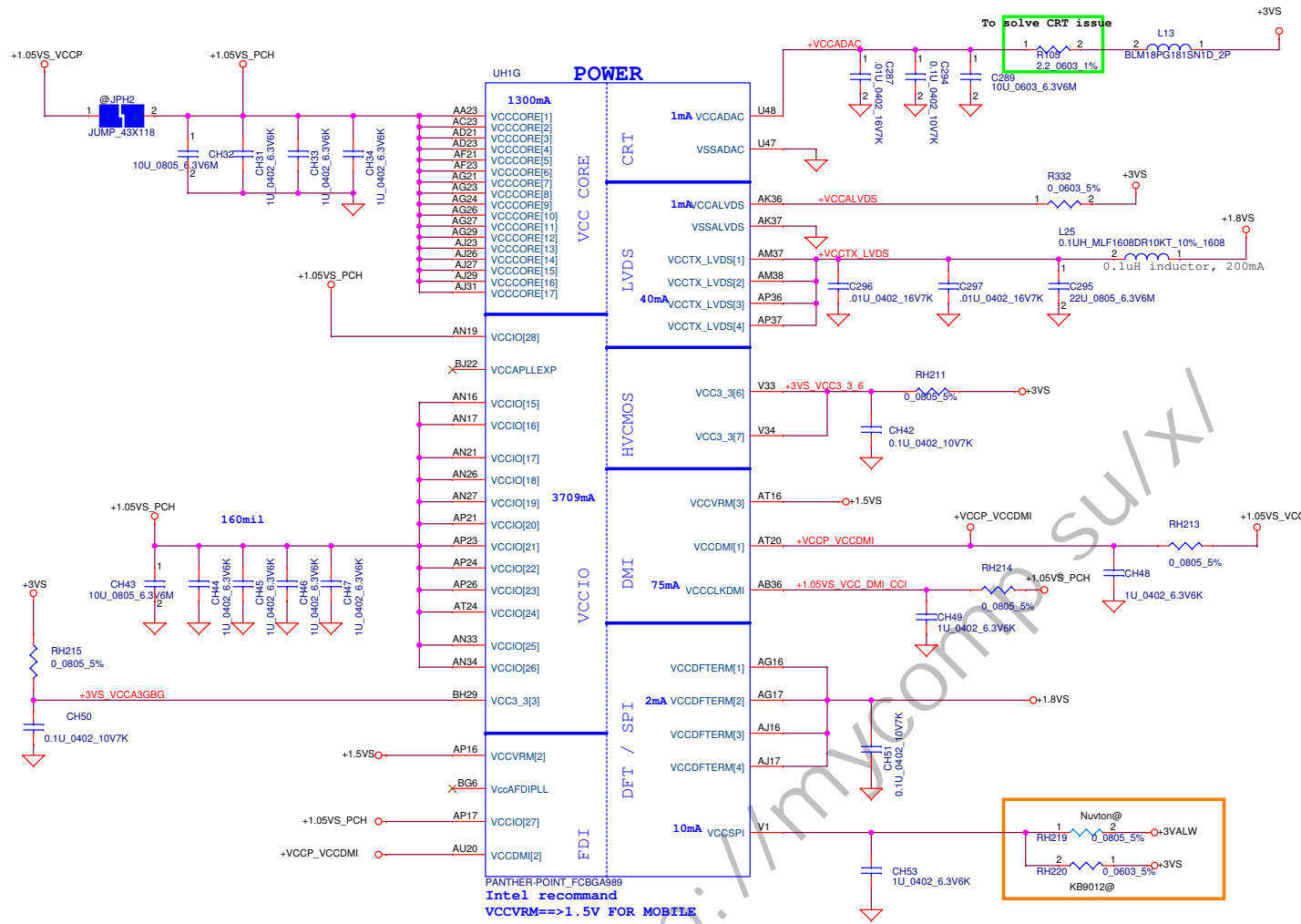
INIT3_3V
 This signal has weak internal PU, can't pull low



	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
VBL30 (UMA)	0	0	0
VBL31 (PX)	0	0	1

PCH_GPIO28 needs to be connected to XDP_FN8
 PCH_GPIO35 needs to be connected to XDP_FN9
 PCH_GPIO15 needs to be connected to XDP_FN16
 Please refer to Huron River Debug Board DG 1.2

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				Sheet 23 of 50



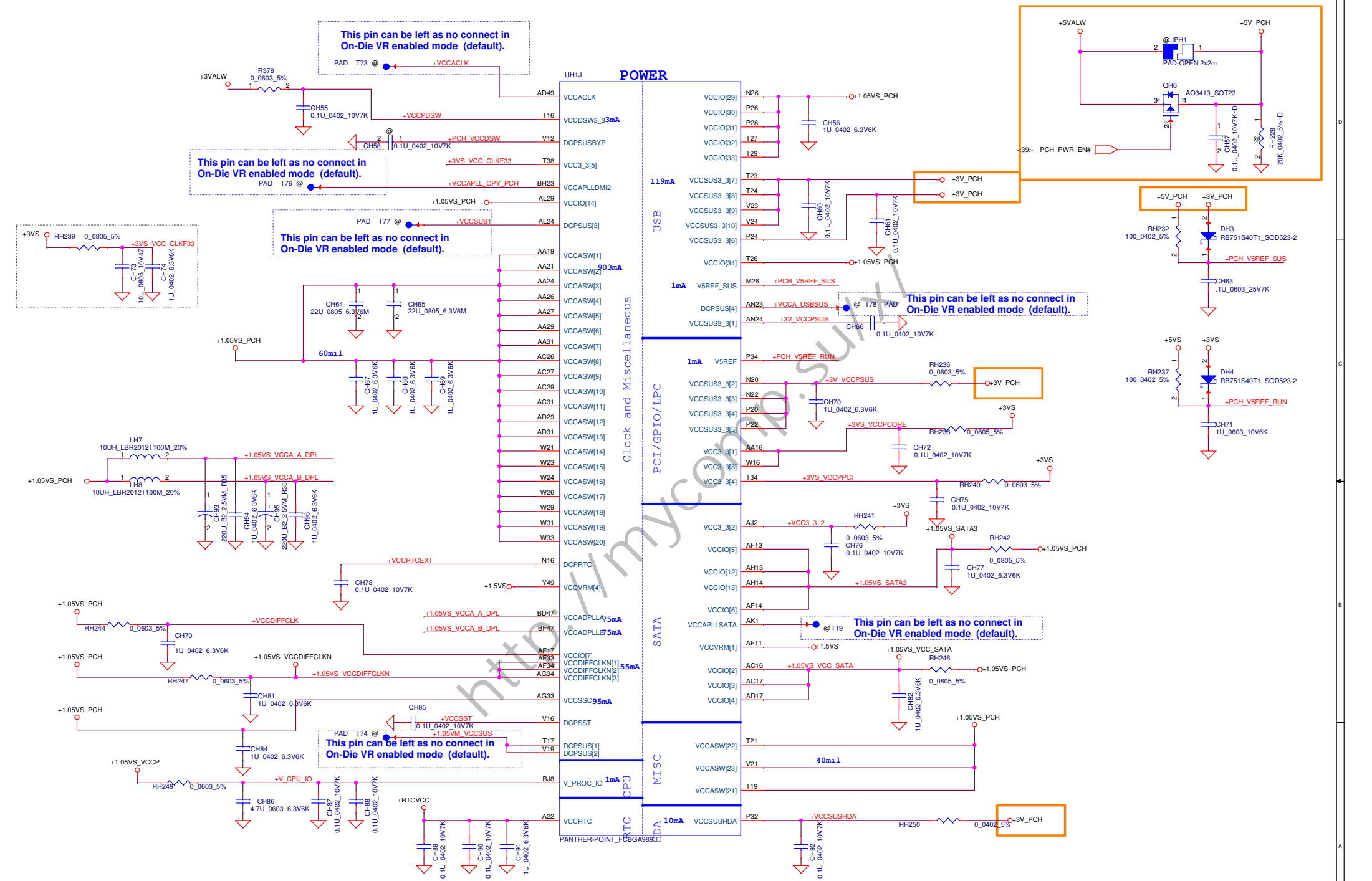
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

PANTHER-POINT_FCBGA989
Intel recommend
VCCVRM==>1.5V FOR MOBILE

http://m/y.com/p/su/xi

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Title	PCH (7/8) PWR	
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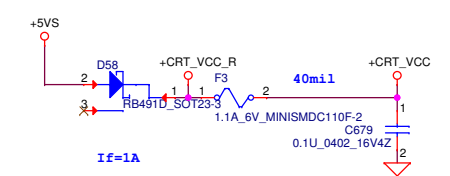
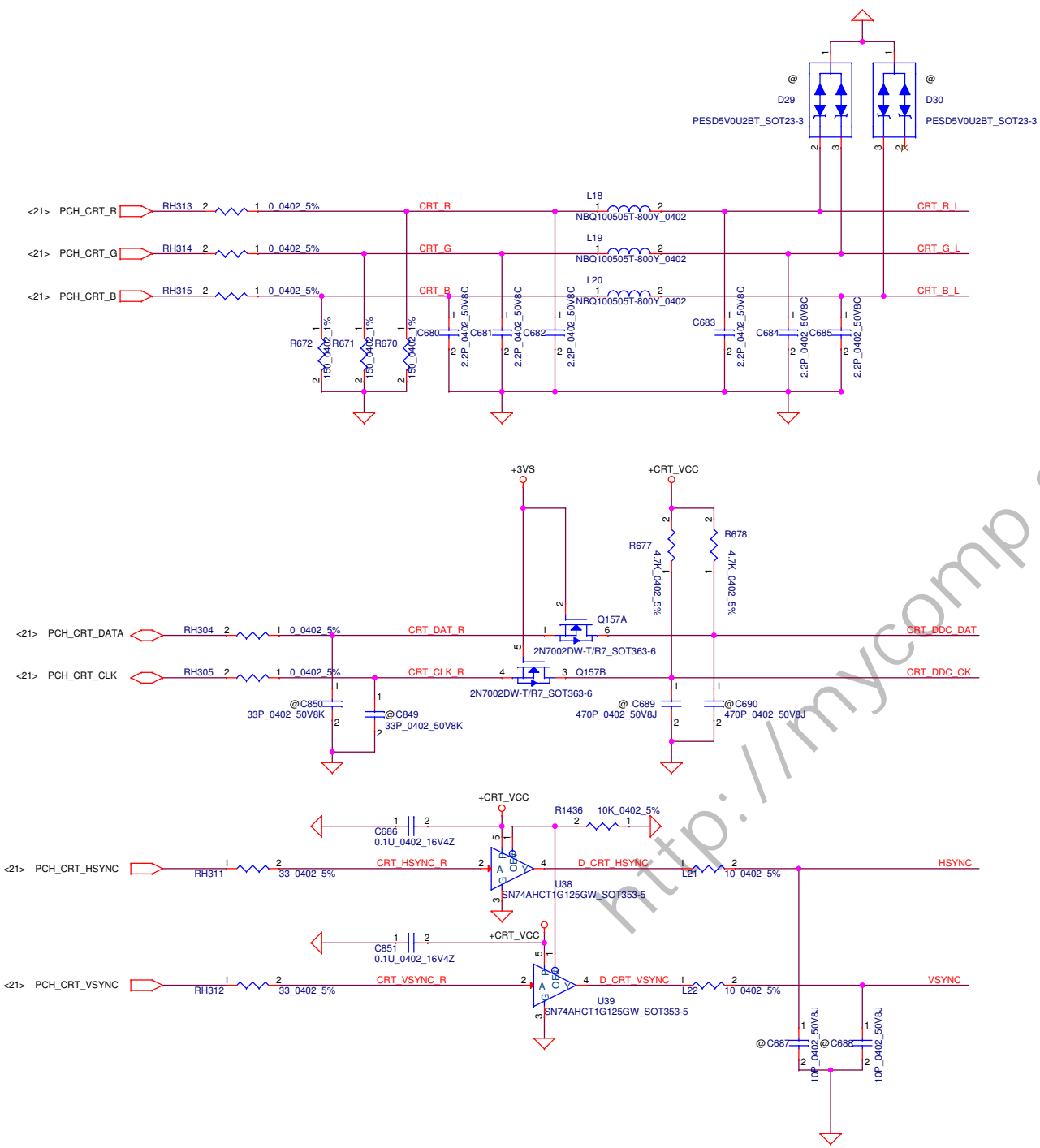
UH1H		UH1	
H5	VSS[0]		
AA17	VSS[1]	VSS[80]	AK38
AA2	VSS[2]	VSS[81]	AK4
AA3	VSS[3]	VSS[82]	AK42
AA33	VSS[4]	VSS[83]	AK46
AA34	VSS[5]	VSS[84]	AK9
AB11	VSS[6]	VSS[85]	AL16
AB14	VSS[7]	VSS[86]	AL17
AB39	VSS[8]	VSS[87]	AL19
AB4	VSS[9]	VSS[88]	AL2
AB43	VSS[10]	VSS[89]	AL21
AB5	VSS[11]	VSS[90]	AL23
AB7	VSS[12]	VSS[91]	AL26
AC19	VSS[13]	VSS[92]	AL27
AC2	VSS[14]	VSS[93]	AL31
AC21	VSS[15]	VSS[94]	AL33
AC24	VSS[16]	VSS[95]	AL34
AC33	VSS[17]	VSS[96]	AL48
AC34	VSS[18]	VSS[97]	AM11
AC48	VSS[19]	VSS[98]	AM14
AD10	VSS[20]	VSS[99]	AM36
AD11	VSS[21]	VSS[100]	AM39
AD12	VSS[22]	VSS[101]	AM43
AD13	VSS[23]	VSS[102]	AM45
AD19	VSS[24]	VSS[103]	AM46
AD24	VSS[25]	VSS[104]	AM7
AD26	VSS[26]	VSS[105]	AN29
AD27	VSS[27]	VSS[106]	AN3
AD33	VSS[28]	VSS[107]	AN31
AD34	VSS[29]	VSS[108]	AN2
AD36	VSS[30]	VSS[109]	AN29
AD37	VSS[31]	VSS[110]	AN3
AD38	VSS[32]	VSS[111]	AP12
AD39	VSS[33]	VSS[112]	AP19
AD4	VSS[34]	VSS[113]	AP28
AD40	VSS[35]	VSS[114]	AP30
AD42	VSS[36]	VSS[115]	AP32
AD43	VSS[37]	VSS[116]	AP38
AD45	VSS[38]	VSS[117]	AP4
AD46	VSS[39]	VSS[118]	AP42
AD8	VSS[40]	VSS[119]	AP46
AE2	VSS[41]	VSS[120]	AP8
AE3	VSS[42]	VSS[121]	AR2
AF10	VSS[43]	VSS[122]	AR48
AF12	VSS[44]	VSS[123]	AT11
AD14	VSS[45]	VSS[124]	AT13
AD16	VSS[46]	VSS[125]	AT18
AF16	VSS[47]	VSS[126]	AT22
AF19	VSS[48]	VSS[127]	AT26
AF24	VSS[49]	VSS[128]	AT28
AF26	VSS[50]	VSS[129]	AT30
AF27	VSS[51]	VSS[130]	AT32
AF29	VSS[52]	VSS[131]	AT34
AF31	VSS[53]	VSS[132]	AT39
AF38	VSS[54]	VSS[133]	AT42
AF4	VSS[55]	VSS[134]	AT46
AF42	VSS[56]	VSS[135]	AT7
AF46	VSS[57]	VSS[136]	AU24
AF5	VSS[58]	VSS[137]	AU30
AF7	VSS[59]	VSS[138]	AV16
AF8	VSS[60]	VSS[139]	AV20
AG19	VSS[61]	VSS[140]	AV30
AG2	VSS[62]	VSS[141]	AV38
AG31	VSS[63]	VSS[142]	AV4
AG48	VSS[64]	VSS[143]	AV9
AH11	VSS[65]	VSS[144]	AW14
AH3	VSS[66]	VSS[145]	AW18
AH36	VSS[67]	VSS[146]	AW2
AH39	VSS[68]	VSS[147]	AW22
AH40	VSS[69]	VSS[148]	AW26
AH42	VSS[70]	VSS[149]	AW32
AH46	VSS[71]	VSS[150]	AW34
AH7	VSS[72]	VSS[151]	AW36
AJ19	VSS[73]	VSS[152]	AW40
AJ21	VSS[74]	VSS[153]	AW48
AJ24	VSS[75]	VSS[154]	AV11
AJ33	VSS[76]	VSS[155]	AY12
AJ34	VSS[77]	VSS[156]	AY22
AK12	VSS[78]	VSS[157]	AY28
AK3	VSS[79]	VSS[158]	

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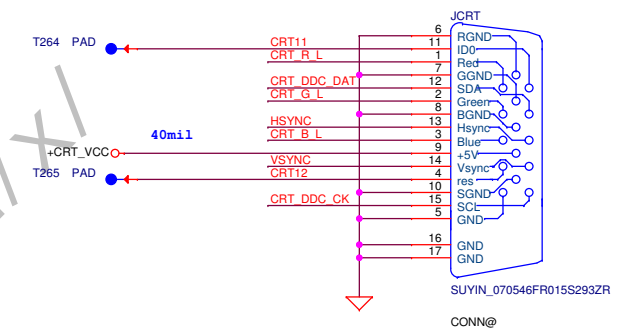
UH1		UH1	
AY4	VSS[159]	VSS[259]	H46
AY42	VSS[160]	VSS[260]	K18
AY46	VSS[161]	VSS[261]	K26
AY8	VSS[162]	VSS[262]	K39
B11	VSS[163]	VSS[263]	K46
B15	VSS[164]	VSS[264]	K7
B19	VSS[165]	VSS[265]	L18
B23	VSS[166]	VSS[266]	L2
B27	VSS[167]	VSS[267]	L20
B31	VSS[168]	VSS[268]	L26
B35	VSS[169]	VSS[269]	L28
B39	VSS[170]	VSS[270]	L36
B7	VSS[171]	VSS[271]	L48
F45	VSS[172]	VSS[272]	M12
BB12	VSS[173]	VSS[273]	P16
BB16	VSS[174]	VSS[274]	M18
BB20	VSS[175]	VSS[275]	M22
BB22	VSS[176]	VSS[276]	M24
BB24	VSS[177]	VSS[277]	M30
BB28	VSS[178]	VSS[278]	M32
BB30	VSS[179]	VSS[279]	M34
BB38	VSS[180]	VSS[280]	M38
BB4	VSS[181]	VSS[281]	M4
BB46	VSS[182]	VSS[282]	M42
BC14	VSS[183]	VSS[283]	M46
BC18	VSS[184]	VSS[284]	M8
BC2	VSS[185]	VSS[285]	N18
BC22	VSS[186]	VSS[286]	P30
BC26	VSS[187]	VSS[287]	N47
BC32	VSS[188]	VSS[288]	P11
BC34	VSS[189]	VSS[289]	P18
BC38	VSS[190]	VSS[290]	T33
BC40	VSS[191]	VSS[291]	P40
BC42	VSS[192]	VSS[292]	P43
BC48	VSS[193]	VSS[293]	P47
BD46	VSS[194]	VSS[294]	P7
BD5	VSS[195]	VSS[295]	R2
BE22	VSS[196]	VSS[296]	R48
BE26	VSS[197]	VSS[297]	T12
BE40	VSS[198]	VSS[298]	T31
BF10	VSS[199]	VSS[299]	T37
BF12	VSS[200]	VSS[300]	T4
BF16	VSS[201]	VSS[301]	W34
BF20	VSS[202]	VSS[302]	T46
BF22	VSS[203]	VSS[303]	T47
BF24	VSS[204]	VSS[304]	T8
BF26	VSS[205]	VSS[305]	V11
BF28	VSS[206]	VSS[306]	V17
BF3	VSS[207]	VSS[307]	V25
BF30	VSS[208]	VSS[308]	V27
BF38	VSS[209]	VSS[309]	V29
BF40	VSS[210]	VSS[310]	V31
BF8	VSS[211]	VSS[311]	V36
BG17	VSS[212]	VSS[312]	V39
BG21	VSS[213]	VSS[313]	V43
BG33	VSS[214]	VSS[314]	V7
BG44	VSS[215]	VSS[315]	W17
BG8	VSS[216]	VSS[316]	W19
BH11	VSS[217]	VSS[317]	W2
BH15	VSS[218]	VSS[318]	W48
BH17	VSS[219]	VSS[319]	W27
BH19	VSS[220]	VSS[320]	Y12
H10	VSS[221]	VSS[321]	Y38
BH27	VSS[222]	VSS[322]	Y42
BH31	VSS[223]	VSS[323]	Y46
BH33	VSS[224]	VSS[324]	Y8
BH35	VSS[225]	VSS[325]	YG29
BH39	VSS[226]	VSS[326]	N24
BH43	VSS[227]	VSS[327]	AJ3
BH7	VSS[228]	VSS[328]	AD47
D3	VSS[229]	VSS[329]	BE10
D12	VSS[230]	VSS[330]	BG41
D16	VSS[231]	VSS[331]	G14
D18	VSS[232]	VSS[332]	H16
D22	VSS[233]	VSS[333]	T36
D24	VSS[234]	VSS[334]	BC22
D26	VSS[235]	VSS[335]	BC24
D30	VSS[236]	VSS[336]	C22
D32	VSS[237]	VSS[337]	AP13
D34	VSS[238]	VSS[338]	M14
D38	VSS[239]	VSS[339]	AP3
D42	VSS[240]	VSS[340]	AP1
D8	VSS[241]	VSS[341]	BE16
E18	VSS[242]	VSS[342]	BC16
E26	VSS[243]	VSS[343]	BC28
G18	VSS[244]	VSS[344]	BJ28
G20	VSS[245]	VSS[345]	
G26	VSS[246]	VSS[346]	
G28	VSS[247]	VSS[347]	
G36	VSS[248]	VSS[348]	
G48	VSS[249]	VSS[349]	
H12	VSS[250]	VSS[350]	
H18	VSS[251]	VSS[351]	
H22	VSS[252]	VSS[352]	
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

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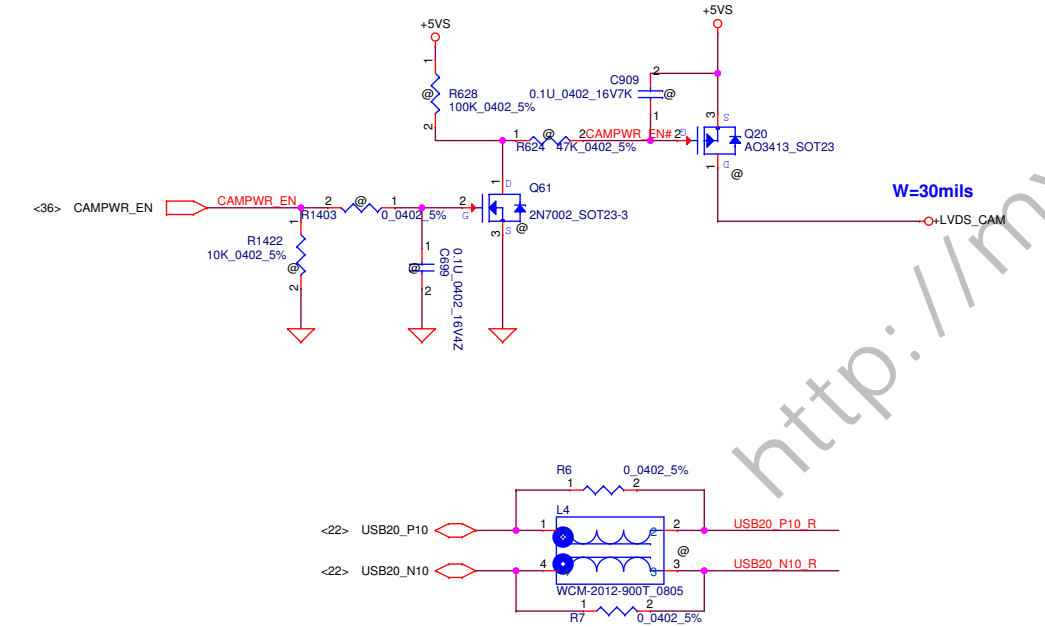
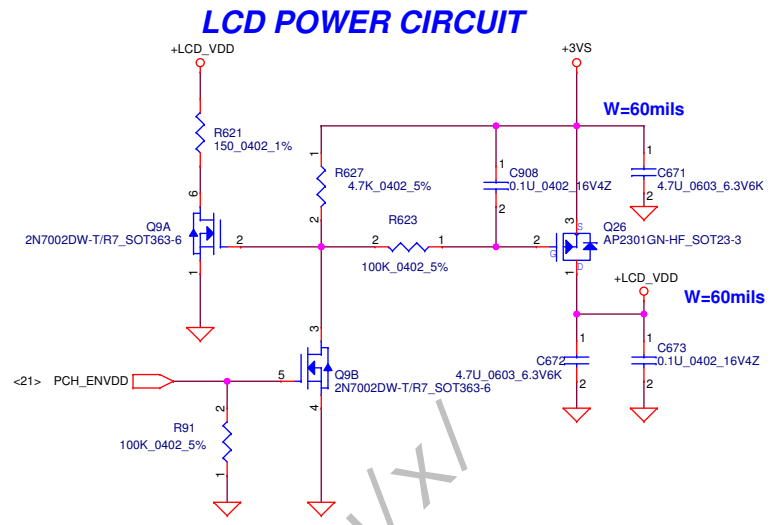
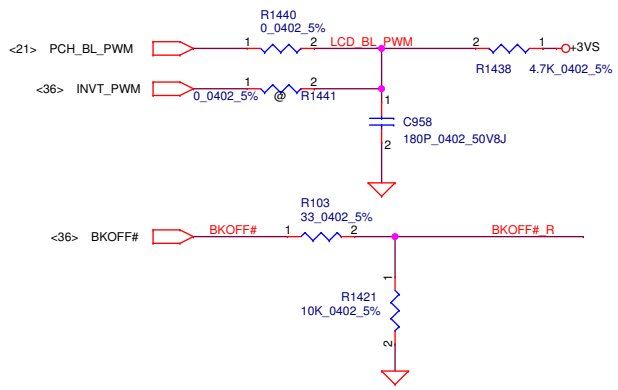
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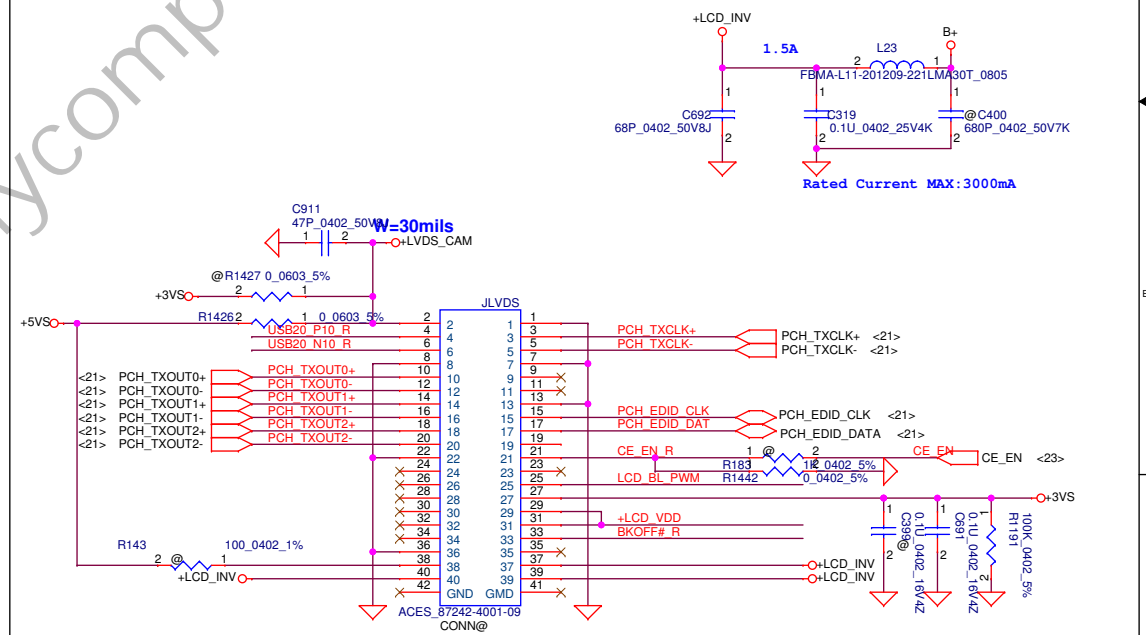
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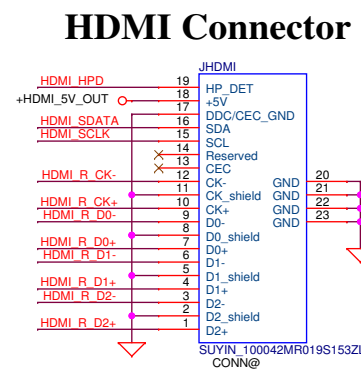
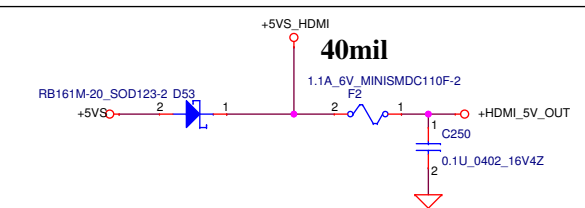
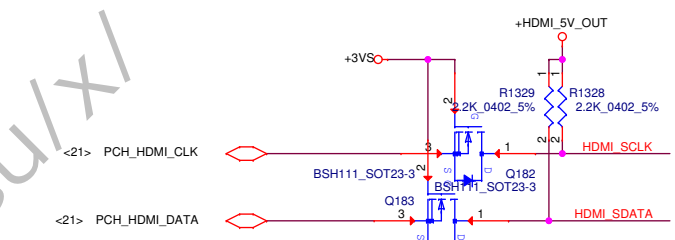
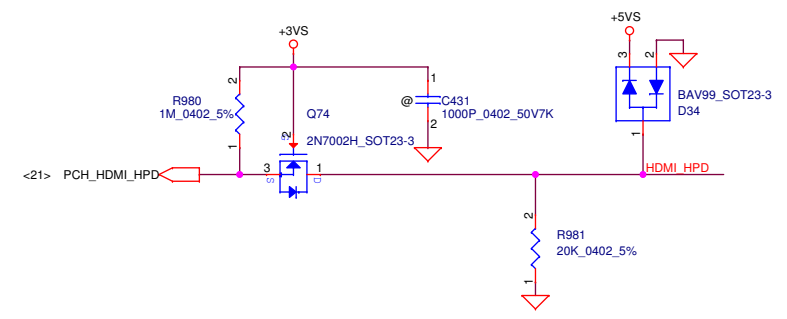
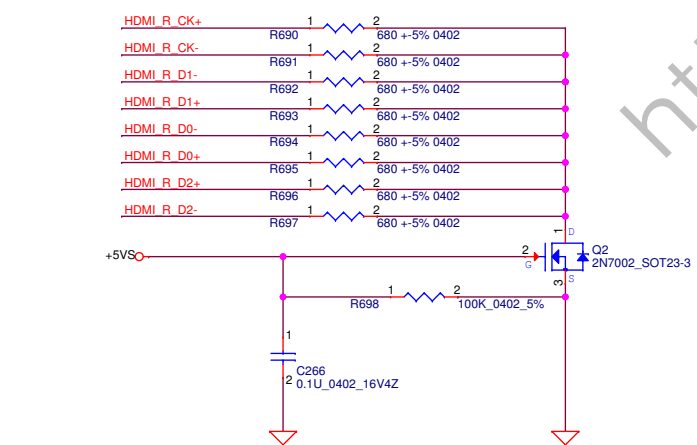
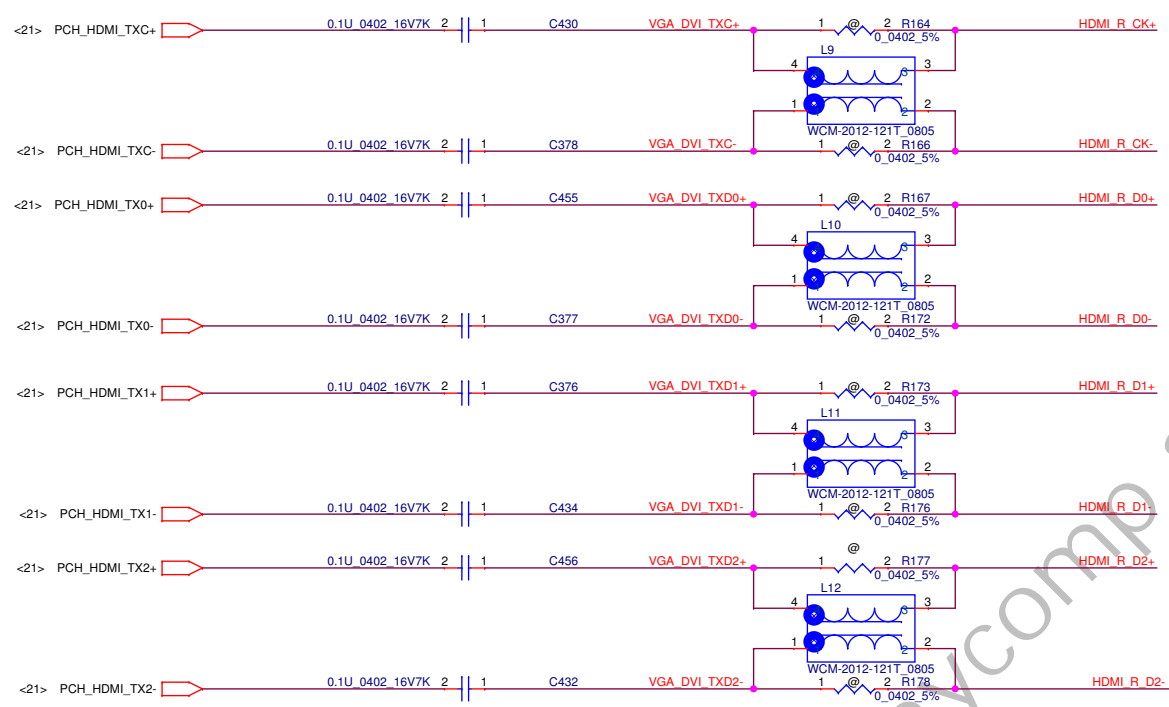
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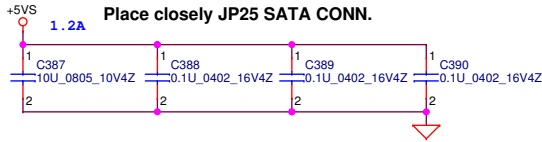


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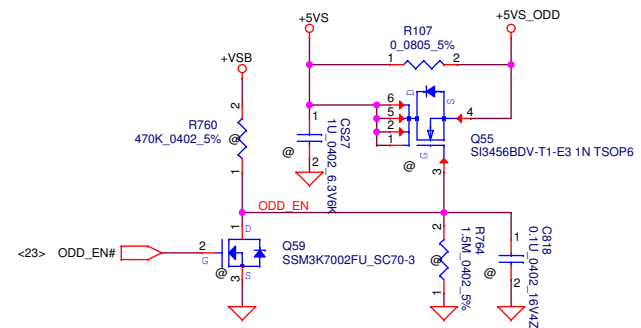
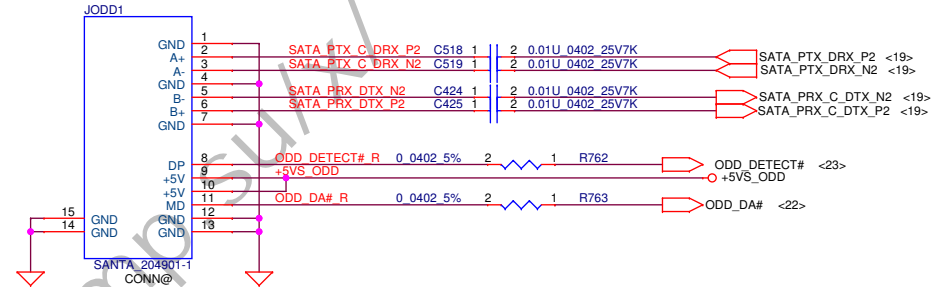
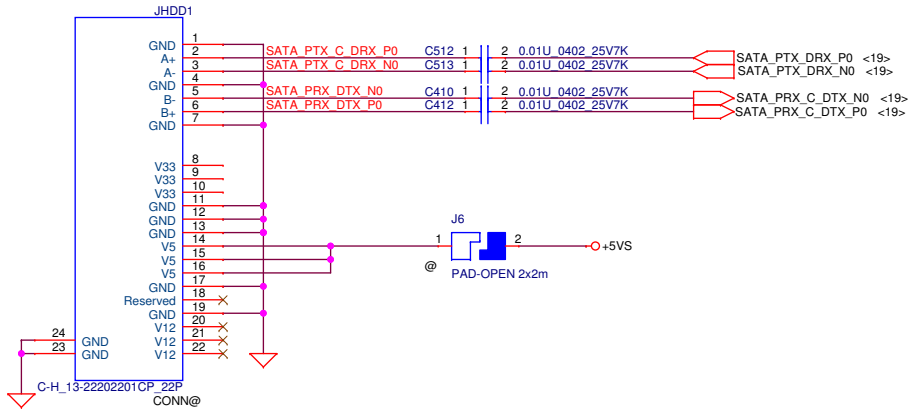
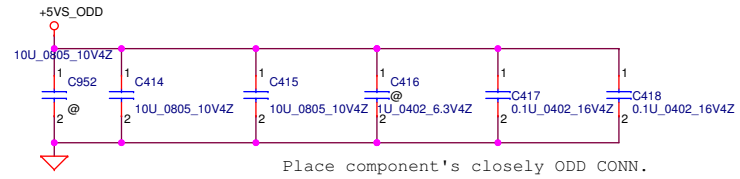


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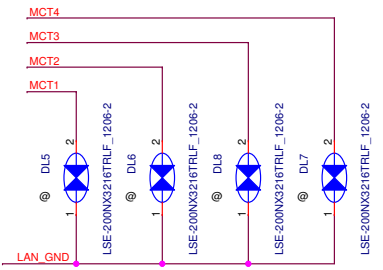
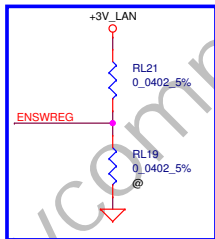
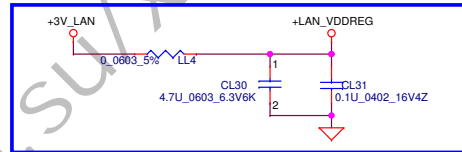
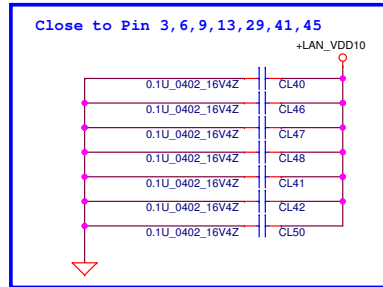
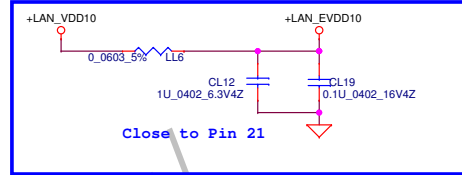
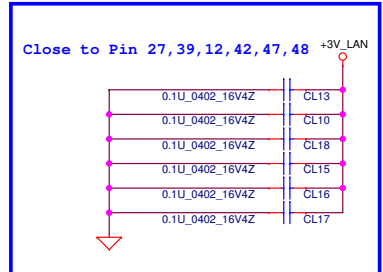
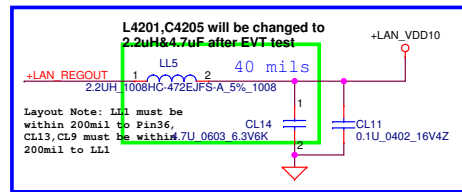
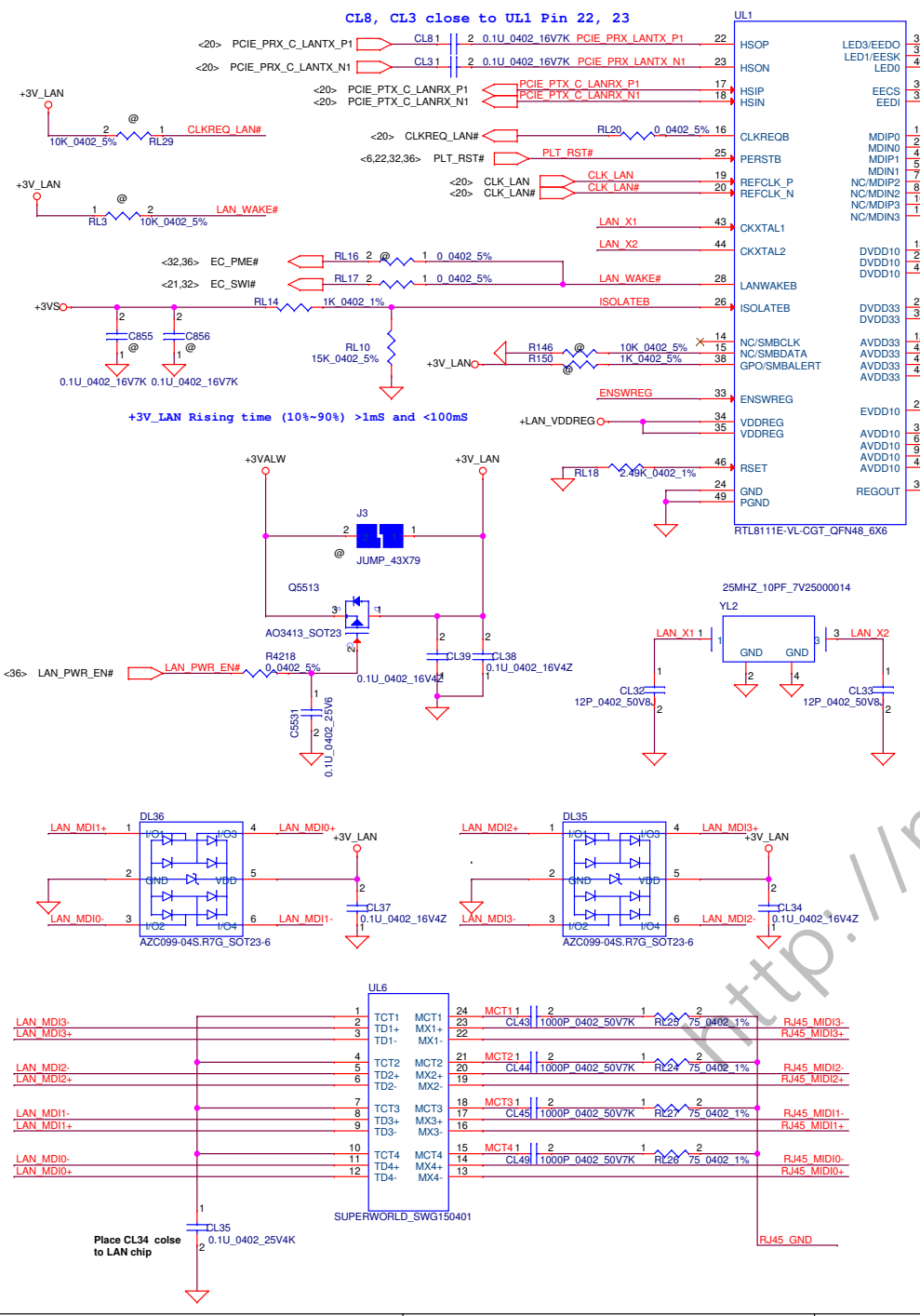
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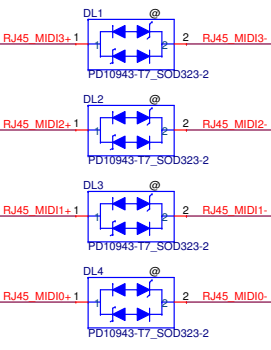
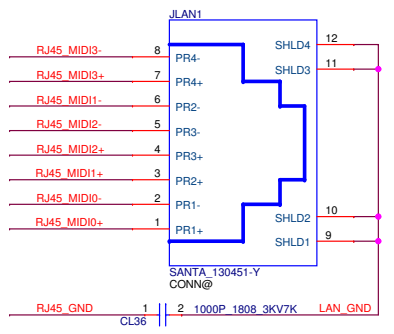
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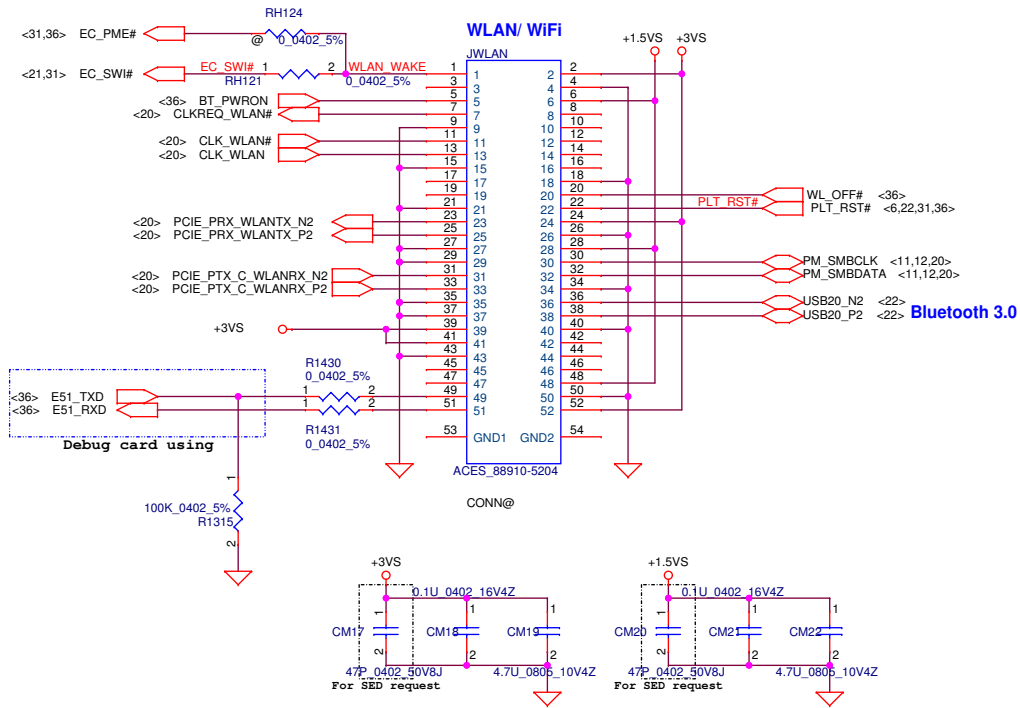
LAN Conn.



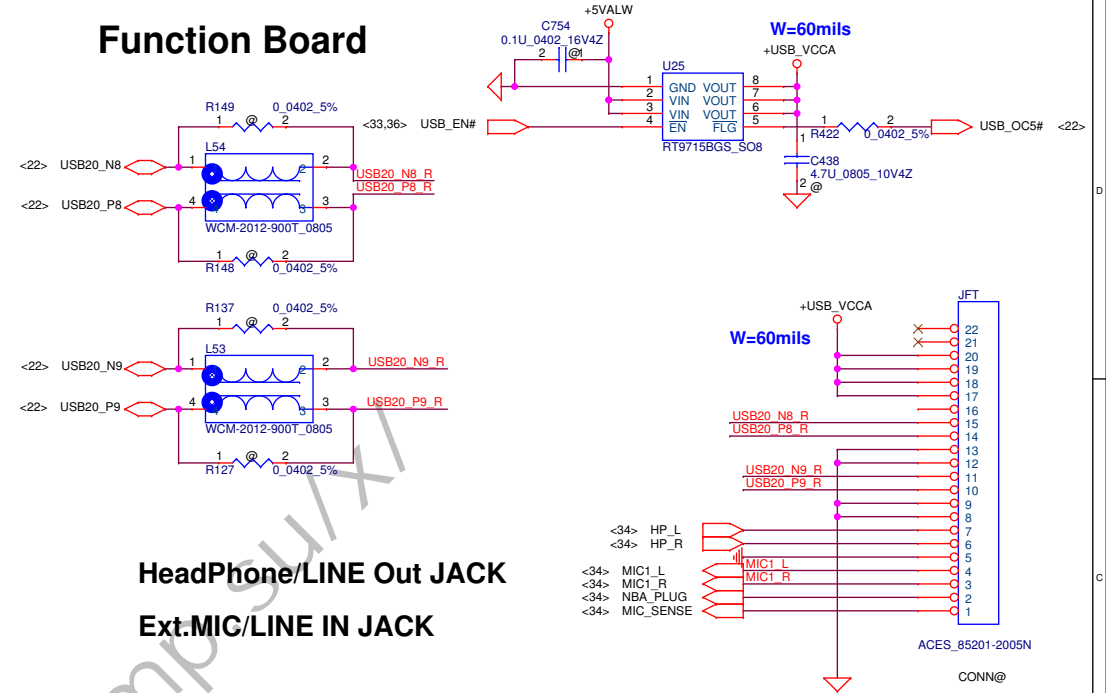
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Issued Date	2012/06/01	Deciphered Date	2011/05/17
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Compal Electronics, Inc.	
Title	RTL8111F
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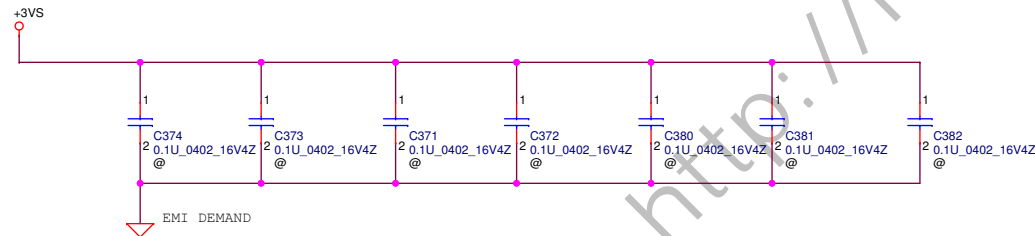
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Function Board

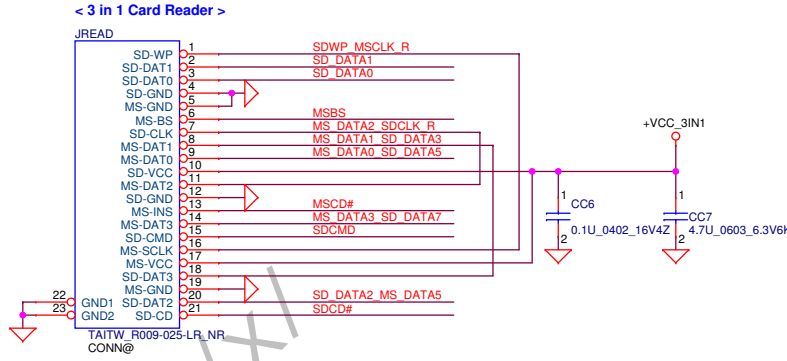
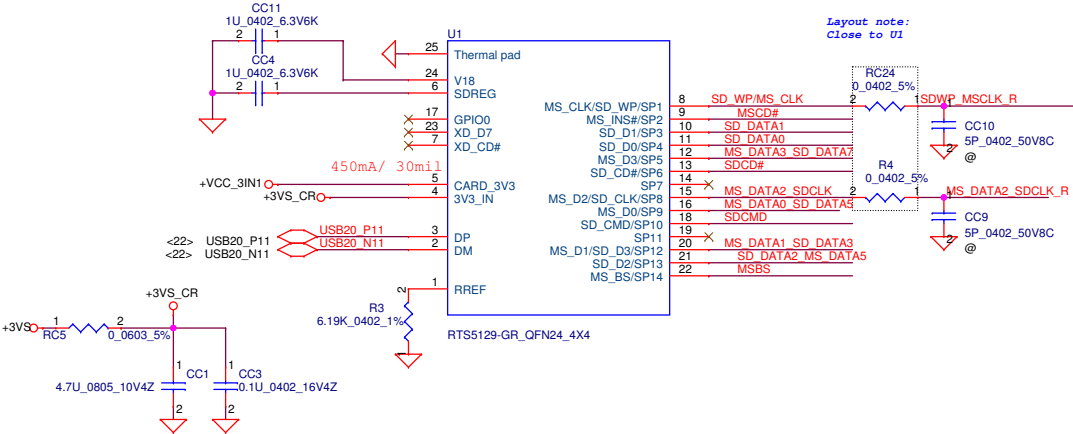


HeadPhone/LINE Out JACK Ext.MIC/LINE IN JACK

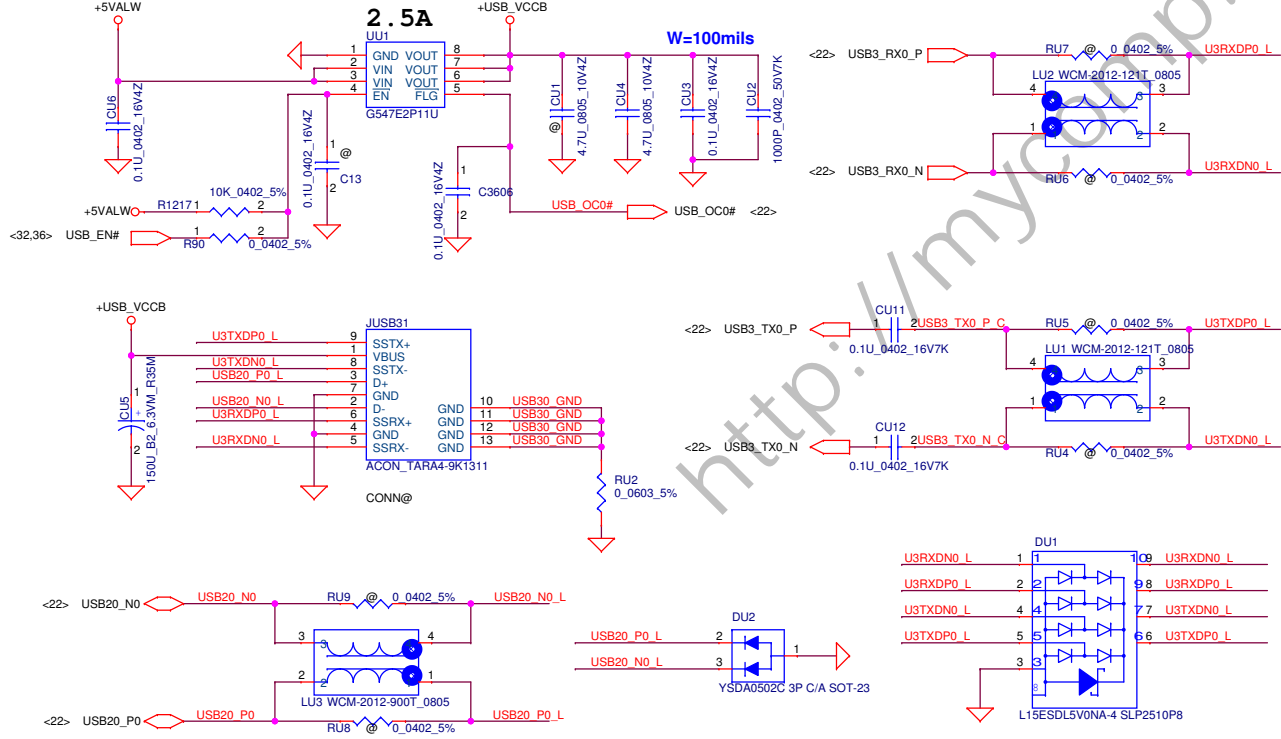


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Issued Date		Deciphered Date		WLAN/USB	
2012/06/01		2013/05/12		Document Number	
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Card Reader



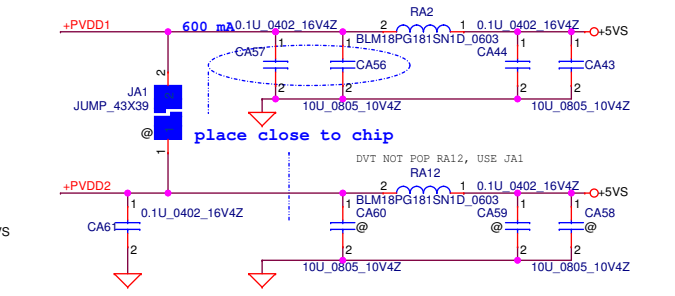
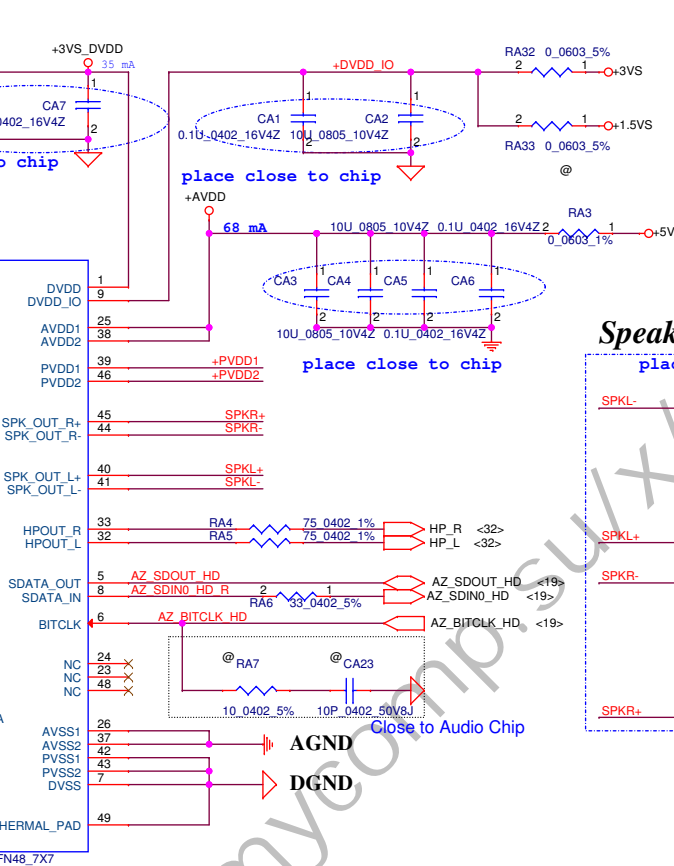
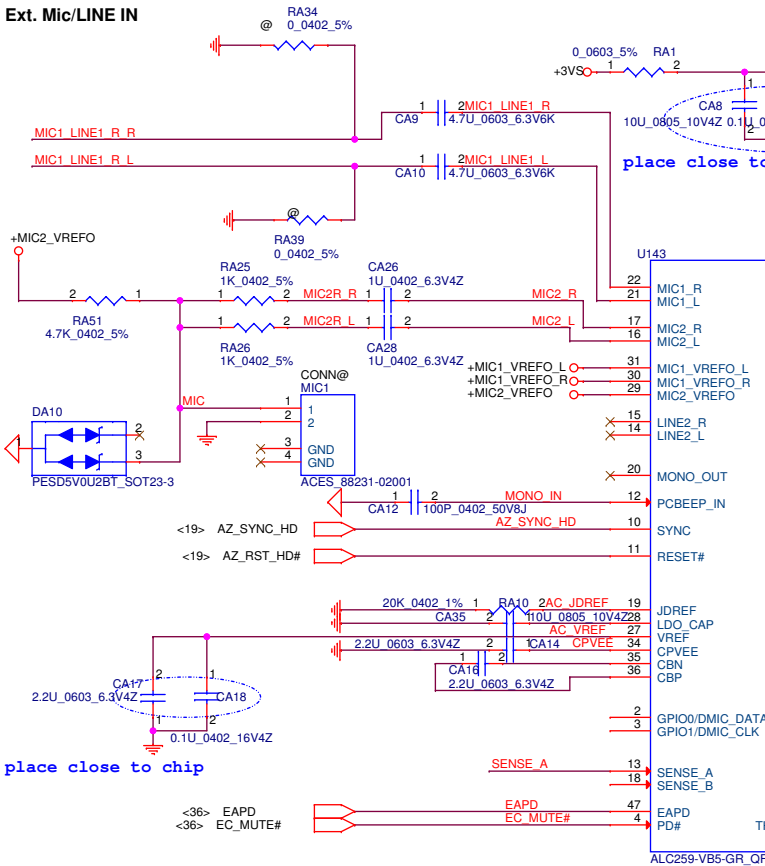
USB3.0 Port



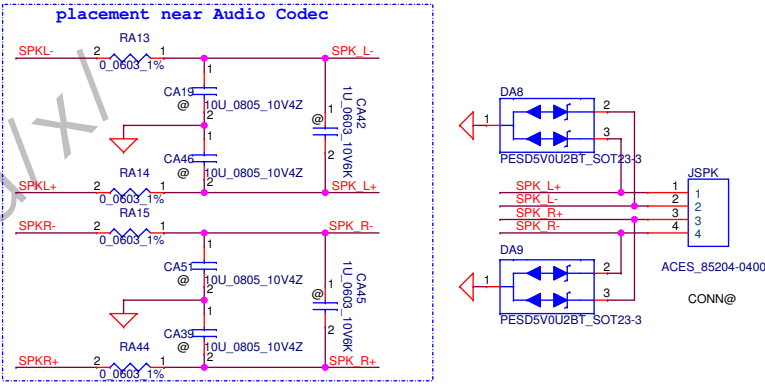
Security Classification		Compal Secret Data	
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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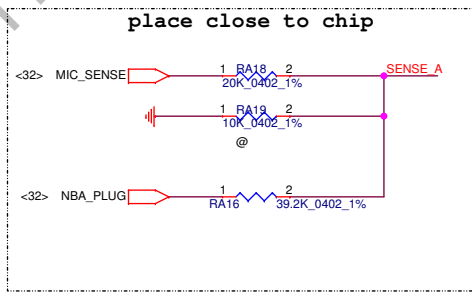
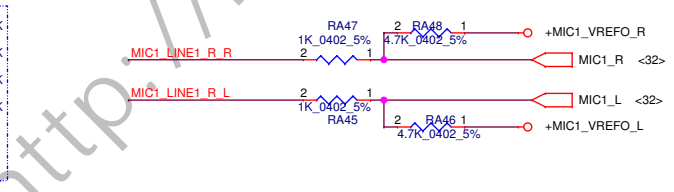
Title		Compal Electronics, Inc.	
USB-Card Reader-RTS5129		Document Number	
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Speaker Connector

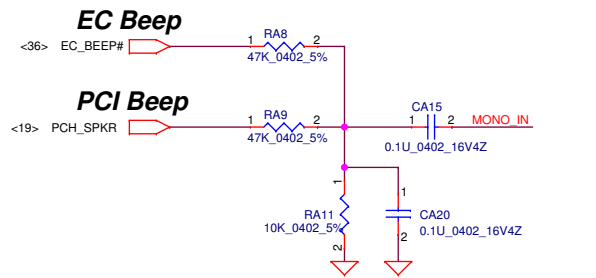


Ext. MIC/LINE IN JACK



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

Beep sound

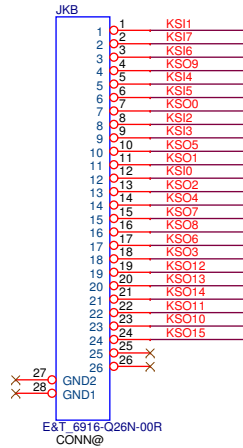


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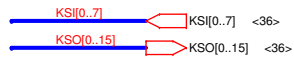
KEYBOARD CONN.

For EMC

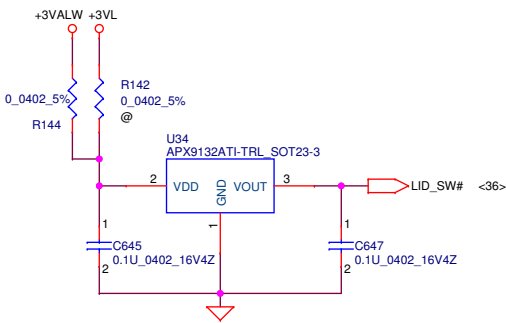
KSO10	1	2
C803	1	100P_0402_50V8J
KSO11	1	2
C804	1	100P_0402_50V8J
KSO12	1	2
C805	1	100P_0402_50V8J
KSO15	1	2
C807	1	100P_0402_50V8J
KSI7	1	2
C808	1	100P_0402_50V8J
KSI2	1	2
C810	1	100P_0402_50V8J
KSI3	1	2
C811	1	100P_0402_50V8J
KSI4	1	2
C812	1	100P_0402_50V8J
KSI0	1	2
C813	1	100P_0402_50V8J
KSI5	1	2
C814	1	100P_0402_50V8J
KSI6	1	2
C815	1	100P_0402_50V8J
KSI1	1	2
C816	1	100P_0402_50V8J
KSO2	1	2
C793	1	100P_0402_50V8J
KSO1	1	2
C790	1	100P_0402_50V8J
KSO0	1	2
C791	1	100P_0402_50V8J
KSO4	1	2
C792	1	100P_0402_50V8J
KSO3	1	2
C795	1	100P_0402_50V8J
KSO5	1	2
C796	1	100P_0402_50V8J
KSO14	1	2
C797	1	100P_0402_50V8J
KSO6	1	2
C798	1	100P_0402_50V8J
KSO7	1	2
C799	1	100P_0402_50V8J
KSO13	1	2
C800	1	100P_0402_50V8J
KSO8	1	2
C801	1	100P_0402_50V8J
KSO9	1	2
C802	1	100P_0402_50V8J



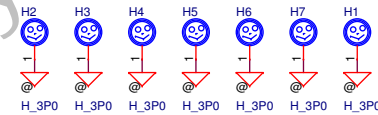
13.3" and 14"



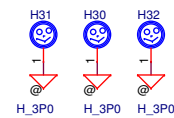
Lid SW



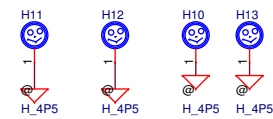
Screw Hole



Break hole



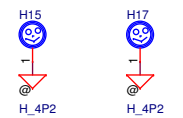
CPU



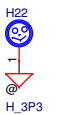
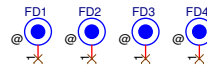
JWLAN



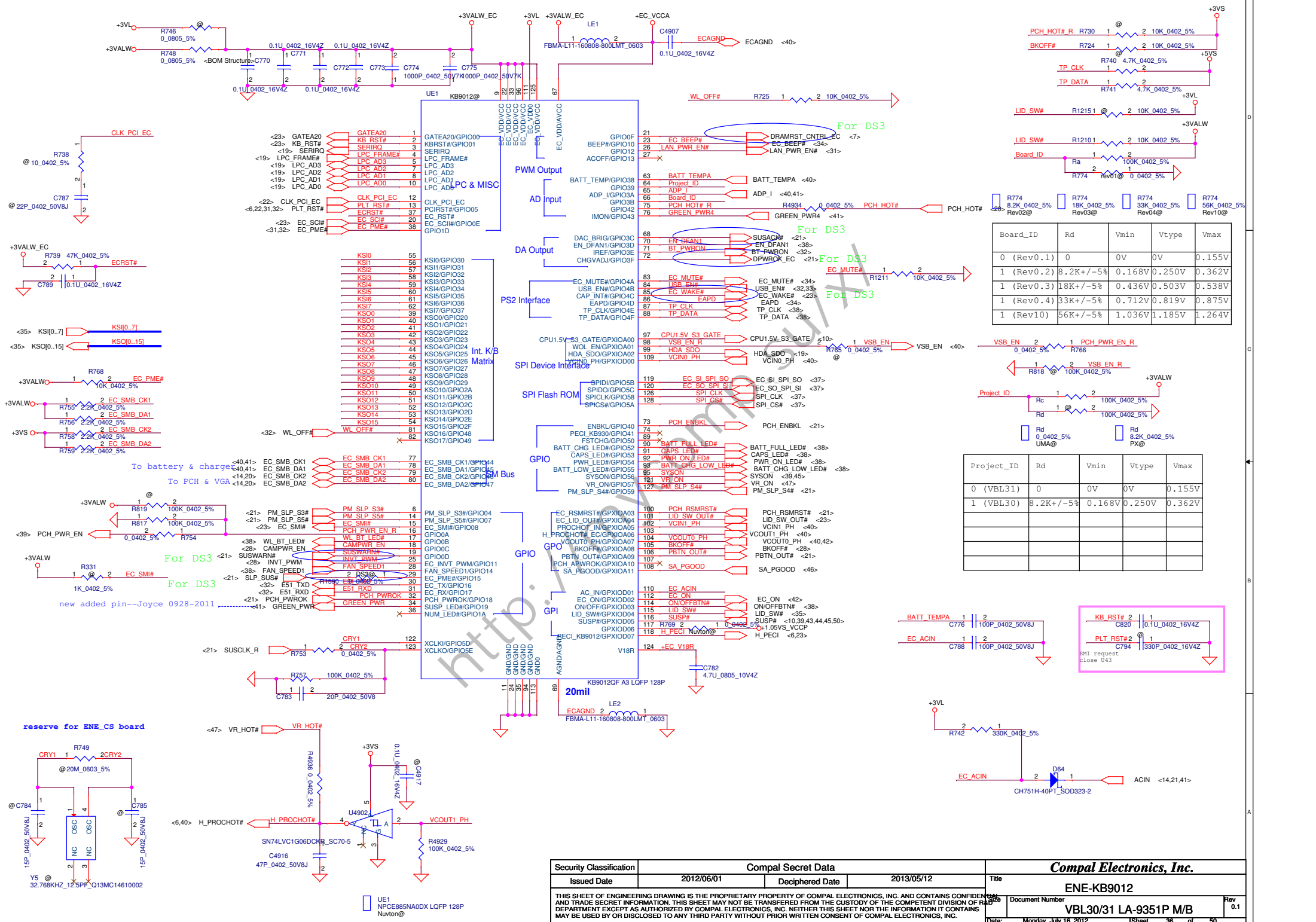
VGA



PCB Federal Mark PAD



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<23>	GATEA20	1	GATEA20/GPIO00
<23>	KB_RST#	2	KB_RST#/GPIO01
<19>	SERRIQ	3	SERRIQ
<19>	LPC_FRAME#	4	LPC_FRAME#
<19>	LPC_AD3	5	LPC_AD3
<19>	LPC_AD2	6	LPC_AD2
<19>	LPC_AD1	7	LPC_AD1
<19>	LPC_AD0	8	LPC_AD0
<22>	CLK_PCI_EC	12	CLK_PCI_EC
<22,31,32>	PLT_RST#	13	PLT_RST#/GPIO05
<23>	EC_RST#	37	EC_RST#
<23>	EC_SCH#	20	EC_SCH#/GPIO0E
<23>	EC_PME#	38	EC_PME#/GPIO0E

55	KS10	GPIO30	KS10/GPIO30
56	KS11	GPIO31	KS11/GPIO31
57	KS12	GPIO32	KS12/GPIO32
58	KS13	GPIO33	KS13/GPIO33
59	KS14	GPIO34	KS14/GPIO34
60	KS15	GPIO35	KS15/GPIO35
61	KS16	GPIO36	KS16/GPIO36
62	KS00	GPIO37	KS00/GPIO37
40	KS01	GPIO20	KS01/GPIO20
41	KS02	GPIO21	KS02/GPIO21
42	KS03	GPIO22	KS03/GPIO22
43	KS04	GPIO23	KS04/GPIO23
44	KS05	GPIO24	KS05/GPIO24
45	KS06	GPIO25	KS06/GPIO25
46	KS07	GPIO26	KS07/GPIO26
47	KS08	GPIO27	KS08/GPIO27
48	KS09	GPIO28	KS09/GPIO28
49	KS10	GPIO29	KS10/GPIO29
50	KS11	GPIO2A	KS11/GPIO2A
51	KS12	GPIO2B	KS12/GPIO2B
52	KS13	GPIO2C	KS13/GPIO2C
53	KS14	GPIO2D	KS14/GPIO2D
54	KS15	GPIO2E	KS15/GPIO2E
81	KS16	GPIO48	KS16/GPIO48
82	KS17	GPIO49	KS17/GPIO49

21	GPIODF	DRAMRST_CNTRL_EC	<7>
23	EC_BEEP#	EC_BEEP#	<34>
26	LAN_PWR_EN#	LAN_PWR_EN#	<31>
27	X		
63	BATT_TEMP#	BATT_TEMP#	<40>
64	Project ID	Project ID	<40,41>
65	ADP	ADP	<40,41>
66	Board ID	Board ID	<40,41>
75	PCH_HOT#_R	R4934	0.402 5% PCH_HOT#
76	GREEN_PWR4	GREEN_PWR4	<41>
68	EN_SFANI	SUSACK#	<21>
70	EN_SFANI	EN_SFANI	<38>
71	BT_PWROK	BT_PWROK	<32>
72	DPWROK_EC	DPWROK_EC	<21>
83	EC_MUTE#	EC_MUTE#	<34>
84	USB_EN#	USB_EN#	<32,33>
85	EC_WAKE#	EC_WAKE#	<23>
86	EAPD	EAPD	<34>
87	TP_CLK	TP_CLK	<38>
88	TP_DATA	TP_DATA	<38>
97	CPH_V5_S3_GATE	CPH_V5_S3_GATE	<10>
98	VSB_EN_R	VSB_EN	<40>
99	HDA_SDO	HDA_SDO	<19>
109	VCINO_PH	VCINO_PH	<40>
119	EC_SI_SPL_SO	EC_SI_SPL_SO	<37>
120	EC_SO_SPL_SI	EC_SO_SPL_SI	<37>
126	SPI_CLK	SPI_CLK	<37>
128	SPI_CS#	SPI_CS#	<37>
73	PCH_ENBKL	PCH_ENBKL	<21>
74	X		
89	BATT_FULL_LED#	BATT_FULL_LED#	<38>
90	CAPS_LED#	CAPS_LED#	<38>
91	PWR_ON_LED#	PWR_ON_LED#	<38>
92	BATT_CHG_LOW_LED#	BATT_CHG_LOW_LED#	<38>
93	SVSON	SVSON	<39,45>
95	VR_ON	VR_ON	<47>
121	PM_SLP_S4#	PM_SLP_S4#	<21>
127	X		
100	PCH_RSMRST#	PCH_RSMRST#	<21>
101	LID_SW_OUT#	LID_SW_OUT#	<23>
102	VCINI_PH	VCINI_PH	<40>
103	VCOUTI_PH	VCOUTI_PH	<40,42>
104	BKOFF#	BKOFF#	<28>
105	PBTN_OUT#	PBTN_OUT#	<21>
106	SA_PG00D	SA_PG00D	<46>
108	X		
110	EC_ACIN	EC_ON	<42>
112	ONOFFBTB#	ONOFFBTB#	<38>
114	LID_SW#	LID_SW#	<35>
115	SUSP#	SUSP#	<10,39,43,44,45,50>
116	H_PECI_Nuvon@	H_PECI	<6,23>
117	X		
118	X		
124	EC_V18R	EC_V18R	

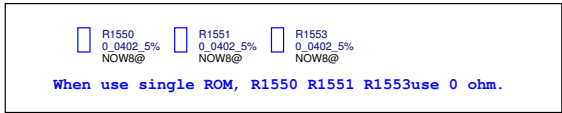
Board_ID	Rd	Vmin	Vtype	Vmax
0 (Rev0.1)	0	0V	0V	0.155V
1 (Rev0.2)	8.2K+/-5%	0.168V	0.250V	0.362V
1 (Rev0.3)	18K+/-5%	0.436V	0.503V	0.538V
1 (Rev0.4)	33K+/-5%	0.712V	0.819V	0.875V
1 (Rev1.0)	56K+/-5%	1.036V	1.185V	1.264V

Project_ID	Rd	Vmin	Vtype	Vmax
0 (VBL31)	0	0V	0V	0.155V
1 (VBL30)	8.2K+/-5%	0.168V	0.250V	0.362V

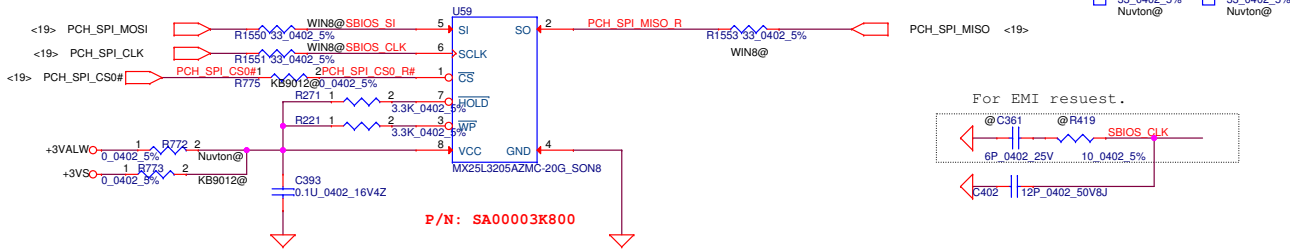
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Title		ENE-KB9012	
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BIOS Bus switch

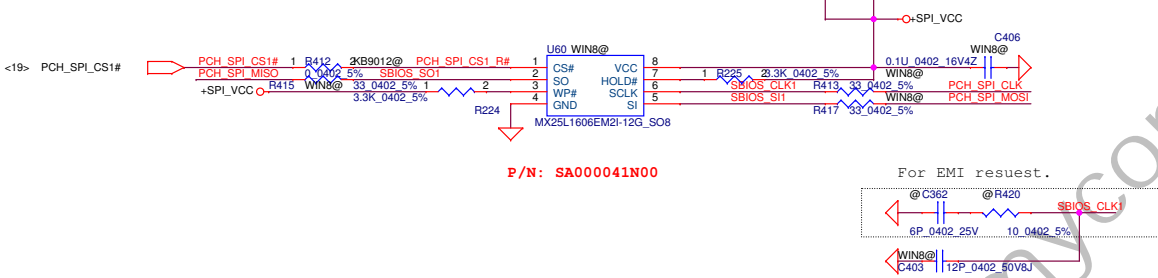
<36> EC_SI SPI_SO R266 1 Nuvton@233_0402_5%PCH_SPI_MISO_R
 <36> EC_SO SPI_SI R267 1 Nuvton@233_0402_5%SBIOS_SI
 <36> SPI_CLK R268 1 Nuvton@233_0402_5%SBIOS_CLK
 <36> SPI_CS# R270 1 Nuvton@233_0402_5%PCH_SPI_CS0_R#



BIOS SPI Flash (4MByte*1)



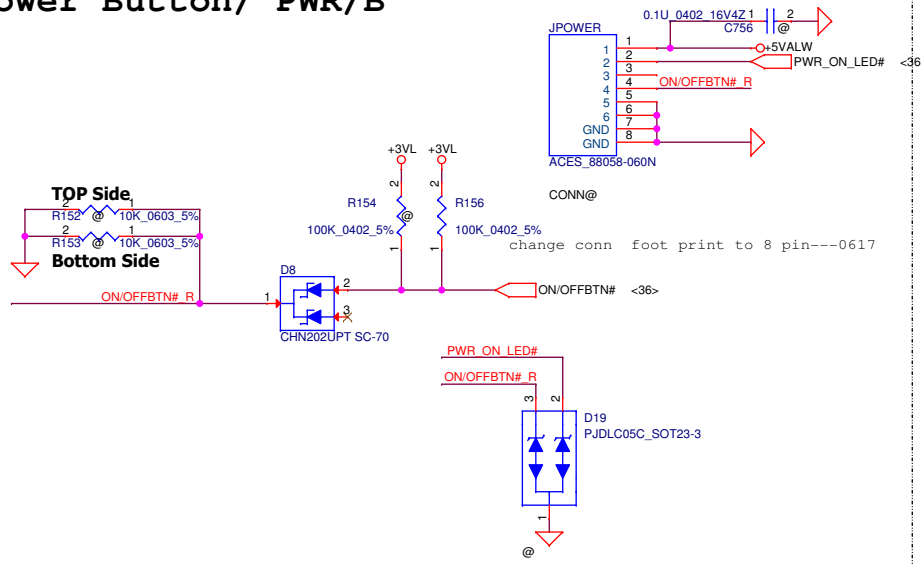
BIOS SPI Flash (2MByte*1) For Win8



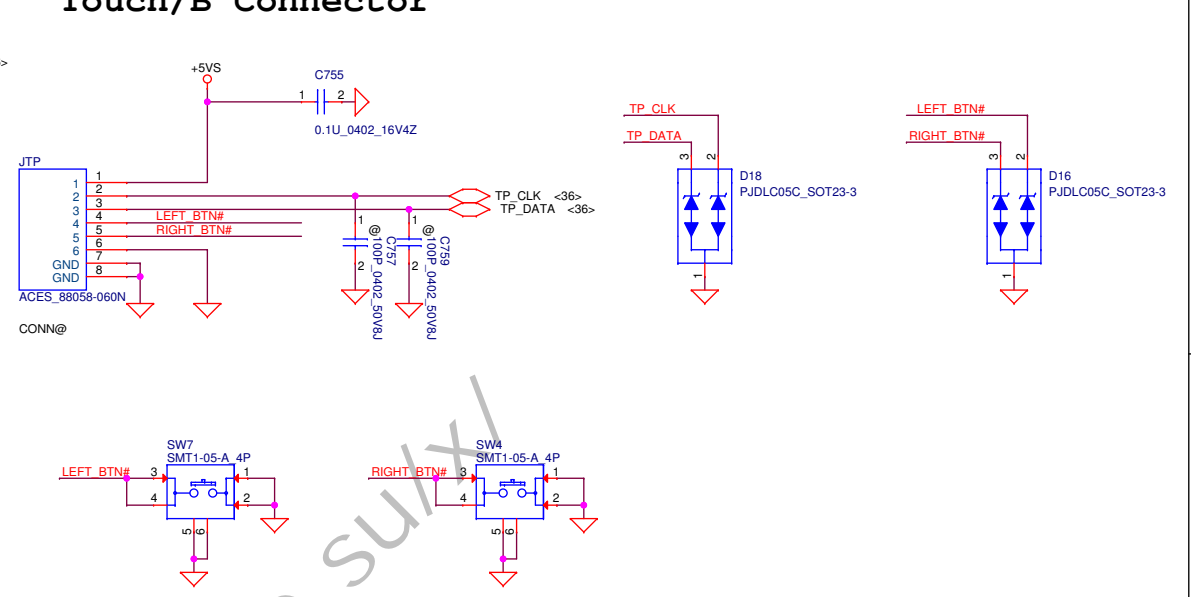
http://imgcomp.su/xl

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				SBIOS & EC ROM	
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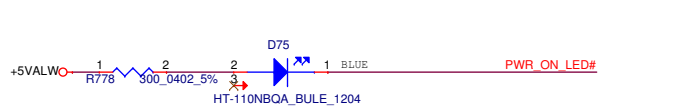
Power Button/ PWR/B



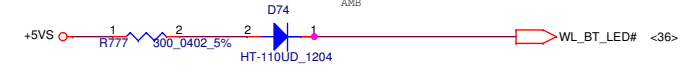
Touch/B Connector



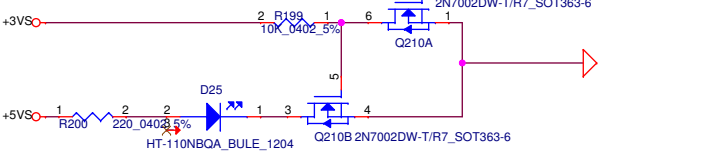
DC-IN LED



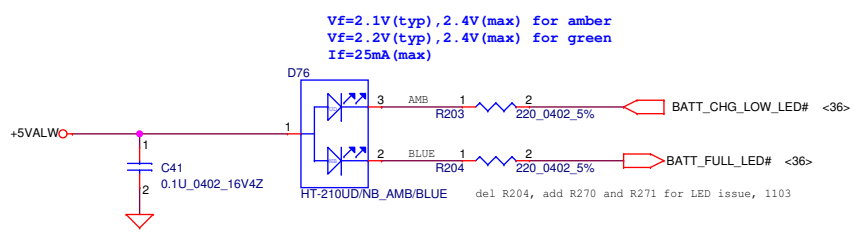
WL&BT LED



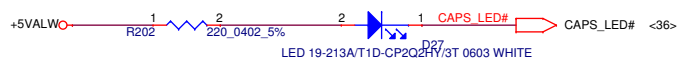
HDD LED



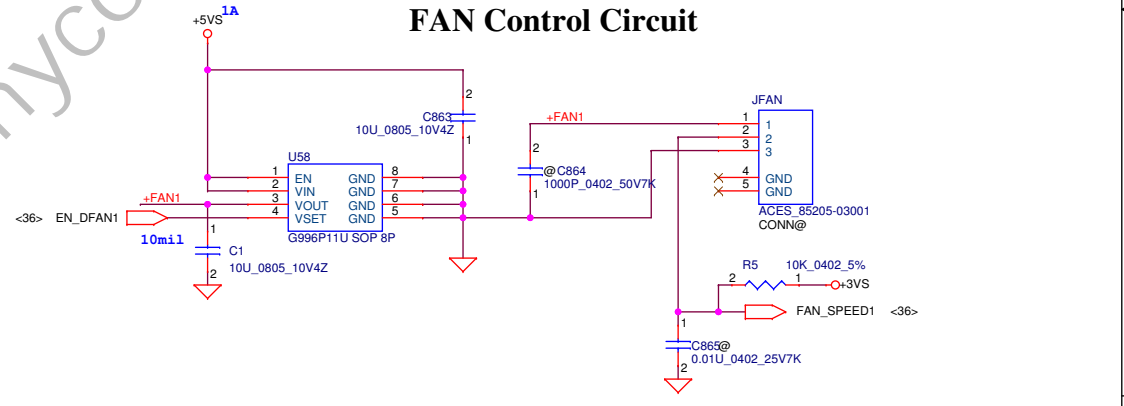
BATT CHARGE/FULL LED



CAP LOCK LED

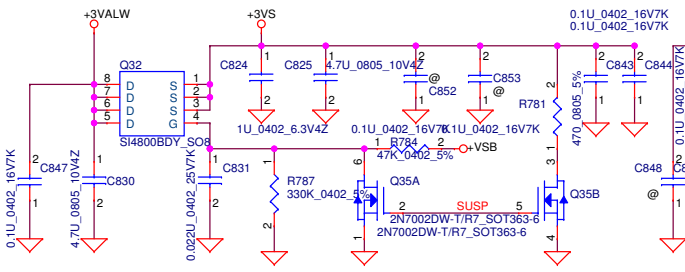


FAN Control Circuit

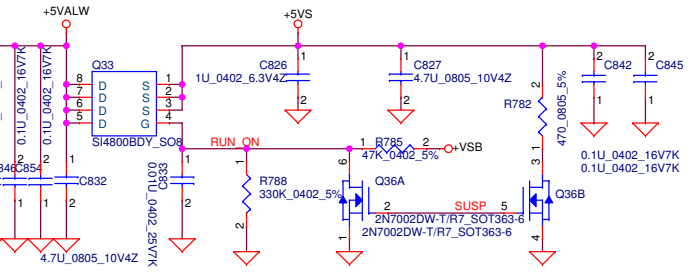


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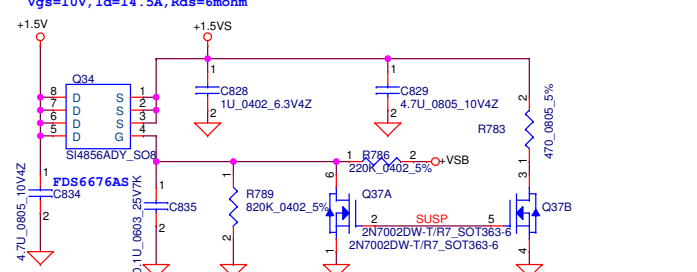
+3VALW TO +3VS
Vgs=-0V, Id=9A, Rds=18.5mohm



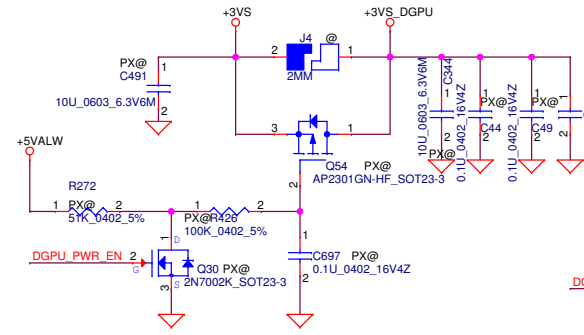
+5VALW TO +5VS



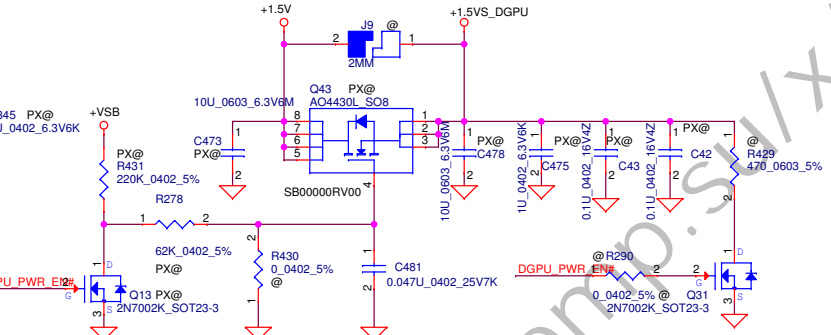
+1.5V to +1.5VS
Vgs=10V, Id=14.5A, Rds=6mohm



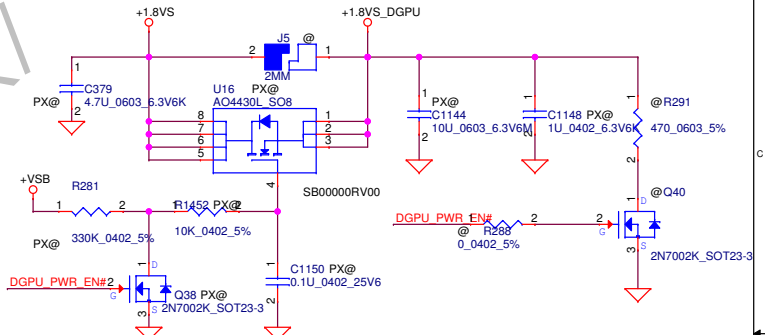
+3VS TO +3VS_DGPU



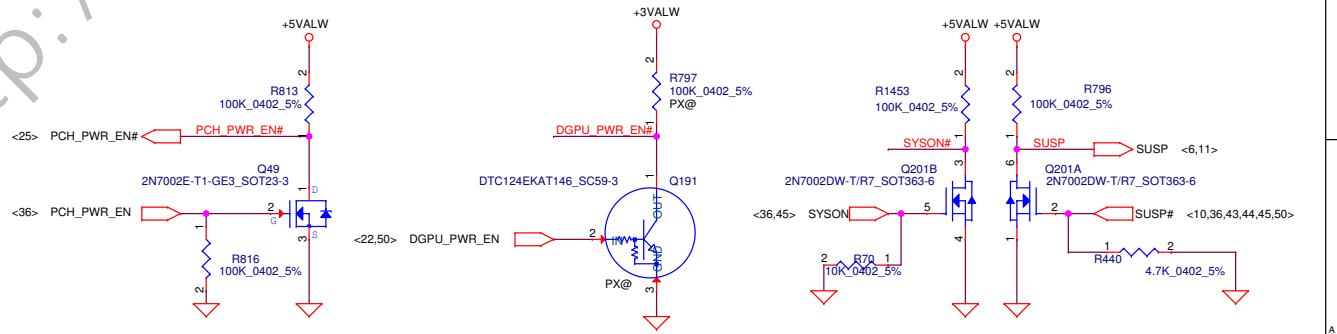
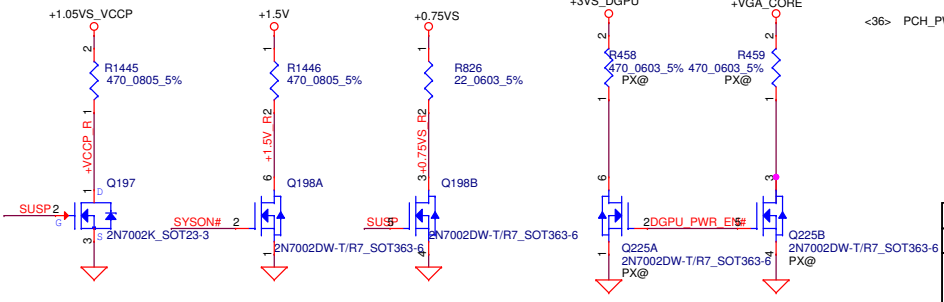
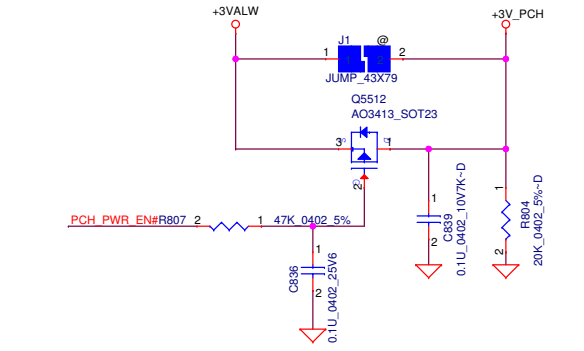
+1.5V TO +1.5VS_DGPU



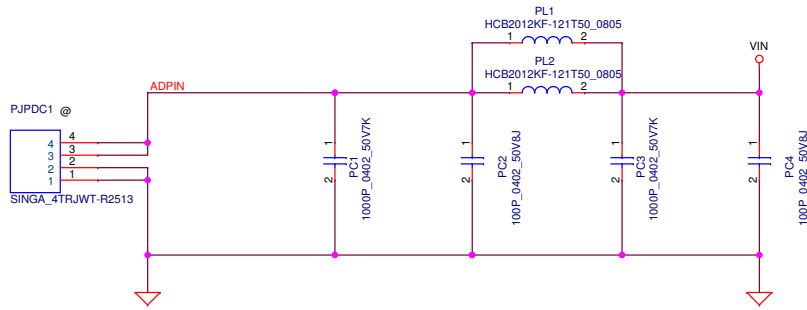
+1.8VS TO +1.8VS_DGPU



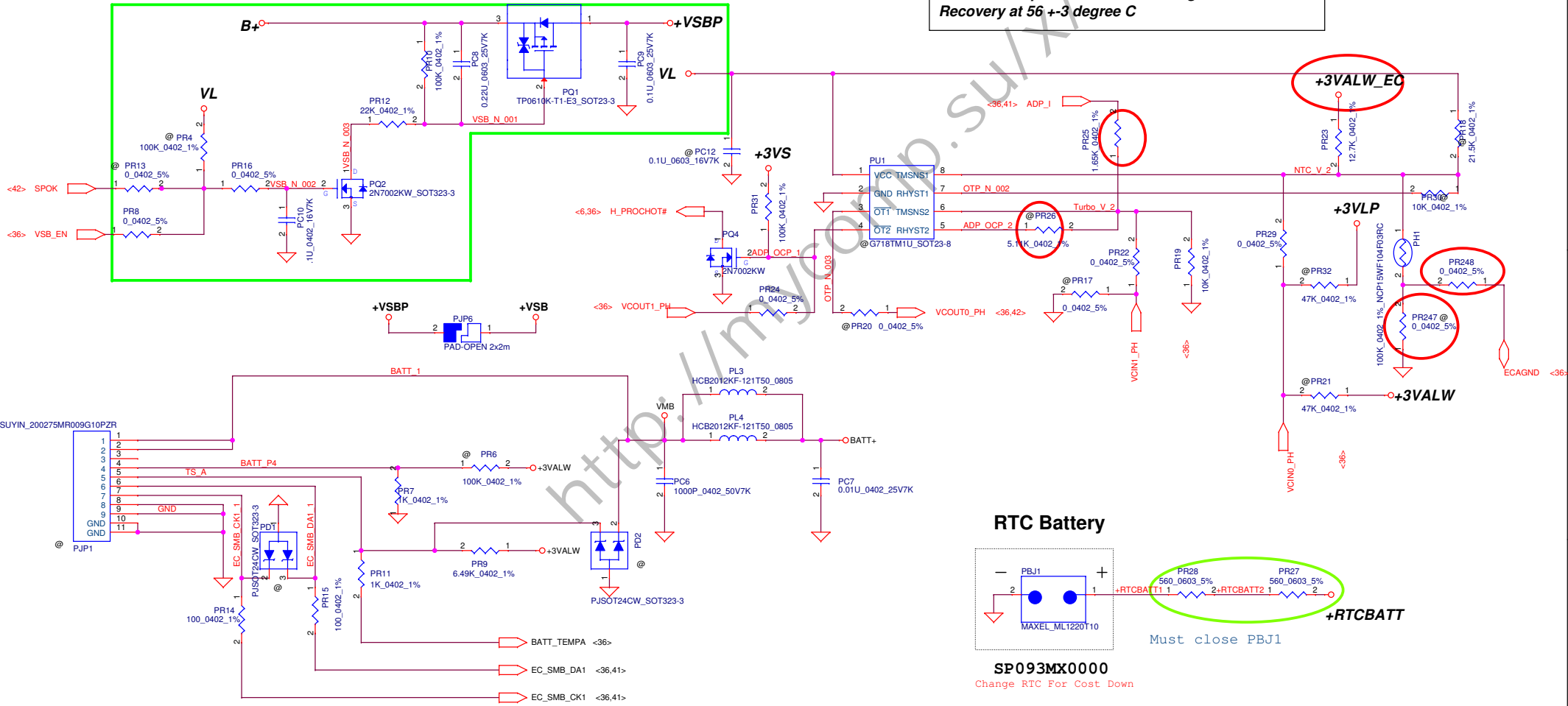
+3VALW to +3V_PCH



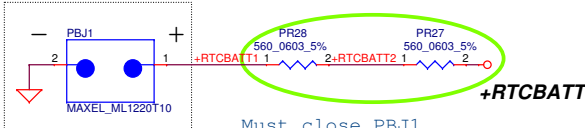
Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	DC-DC INTERFACE	
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Date: Monday, July 16, 2012				Sheet	39 of 50



PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

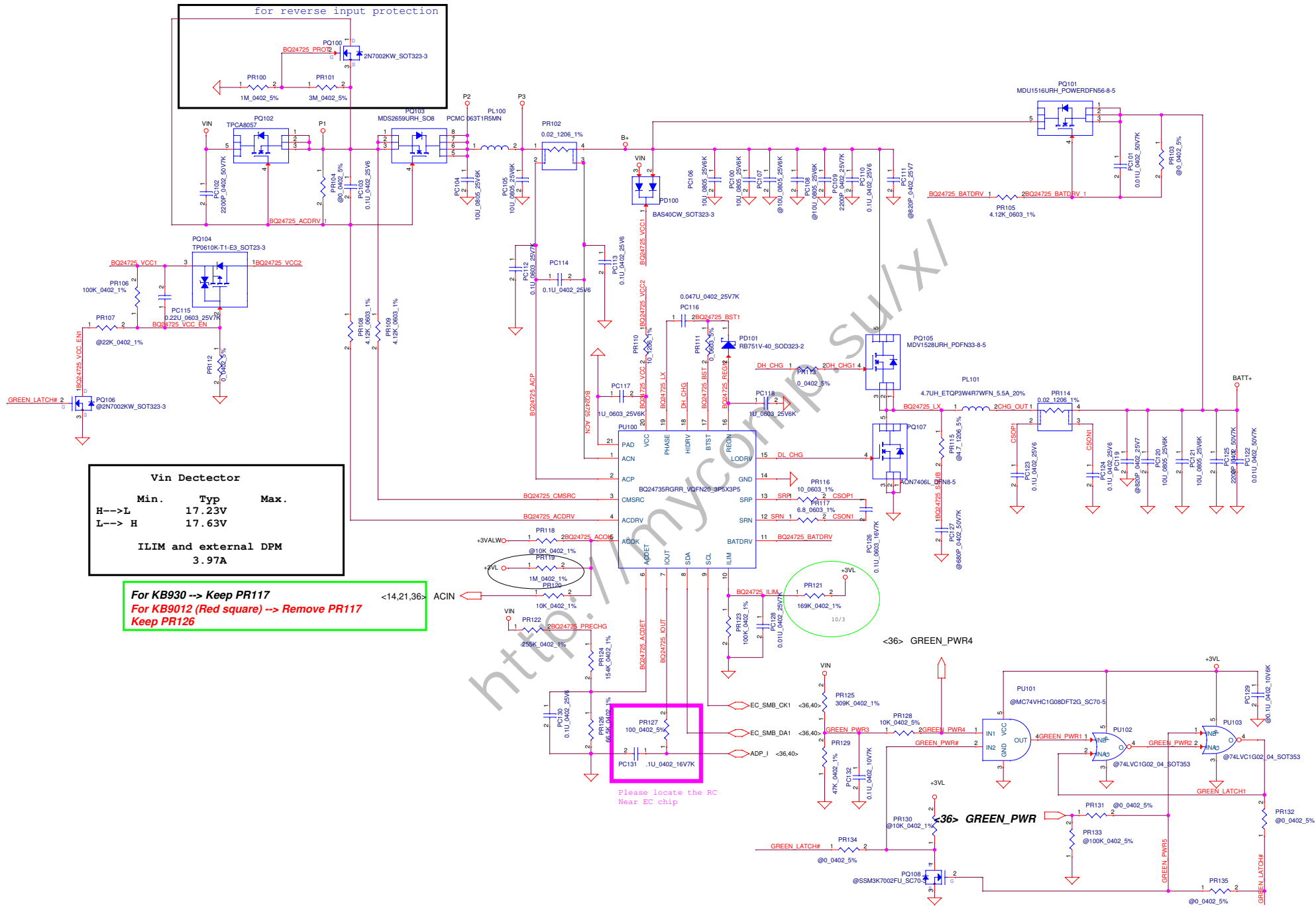


RTC Battery



SP093MX0000
 Change RIC For Cost Down

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/23	Deciphered Date	2012/12/31	PWR-DCIN / BATT CONN / OTP	
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for reverse input protection

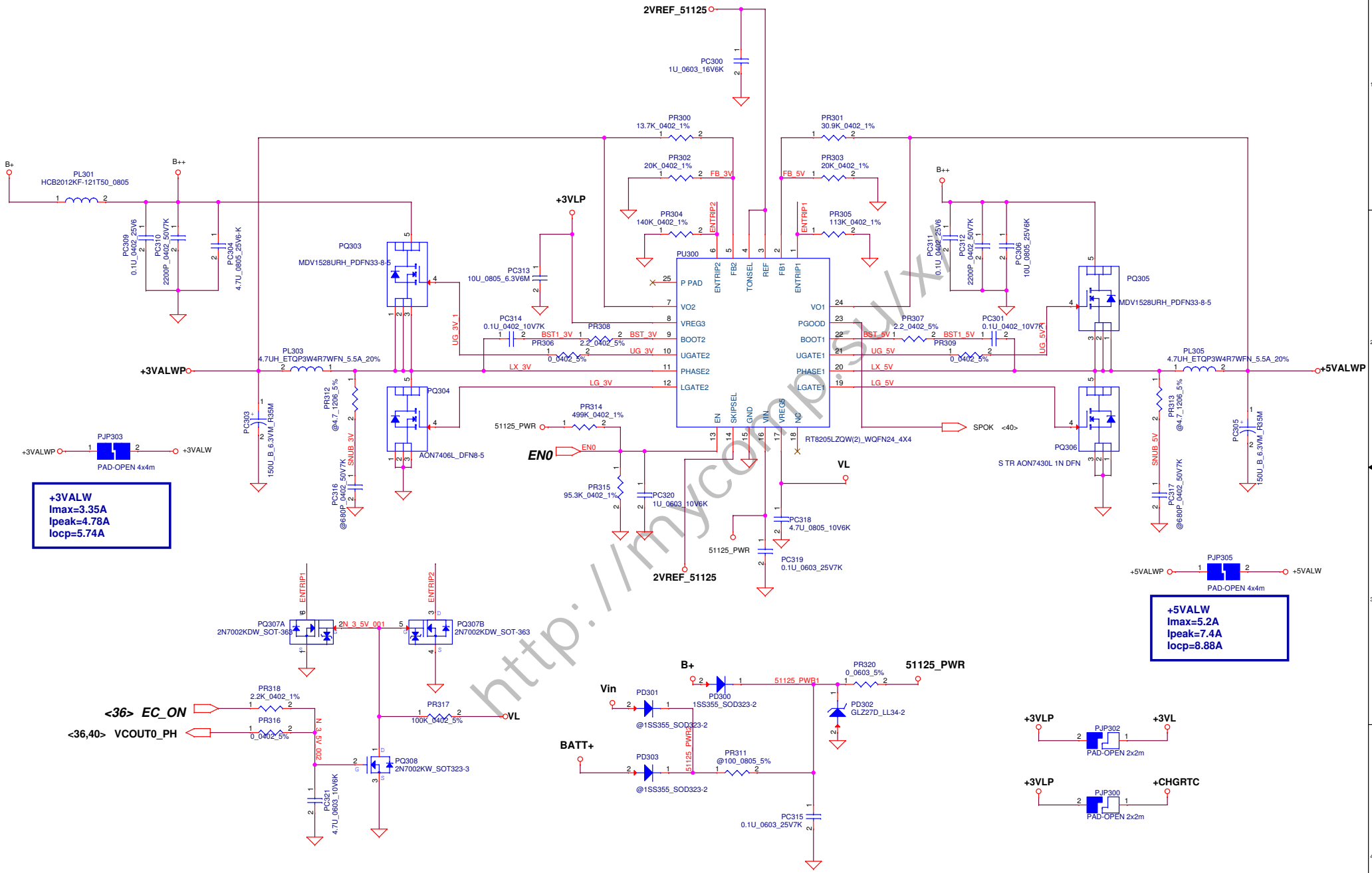
Vin Detector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
3.97A

For KB930 --> Keep PR117
For KB9012 (Red square) --> Remove PR117
Keep PR126

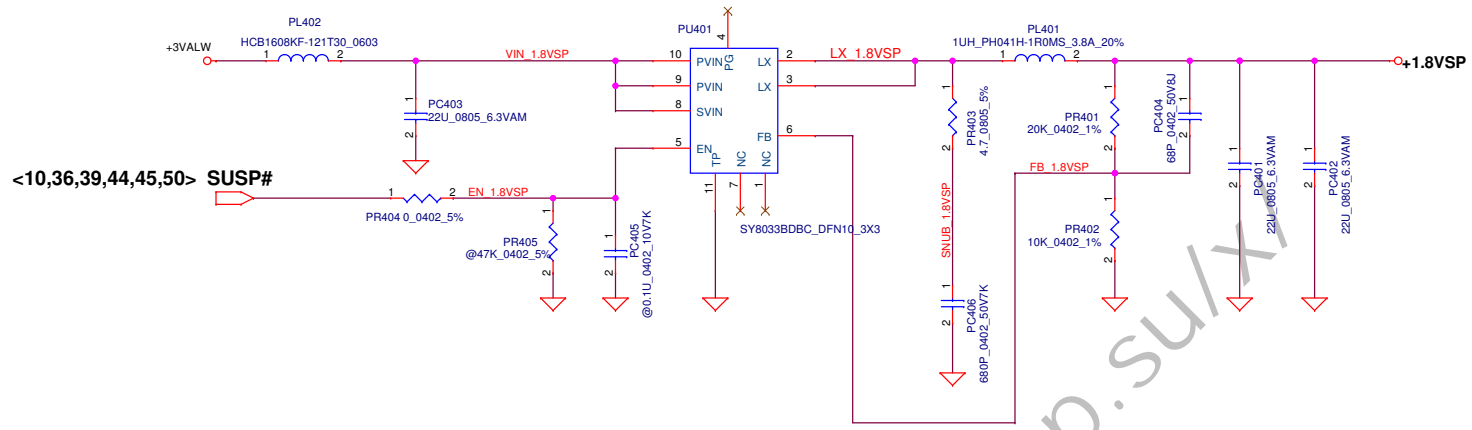
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2009/01/23	Deciphered Date	2012/12/31	PWR-CHARGER
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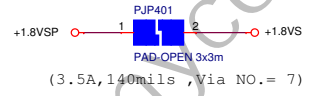
+3VALW
 $I_{max}=3.35A$
 $I_{peak}=4.78A$
 $I_{ocp}=5.74A$

+5VALW
 $I_{max}=5.2A$
 $I_{peak}=7.4A$
 $I_{ocp}=8.88A$

Security Classification	Compal Secret Data		Title
Issued Date	2007/08/02	Deciphered Date	2012/12/31
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			Rev 0.1
			Sheet 42 of 50



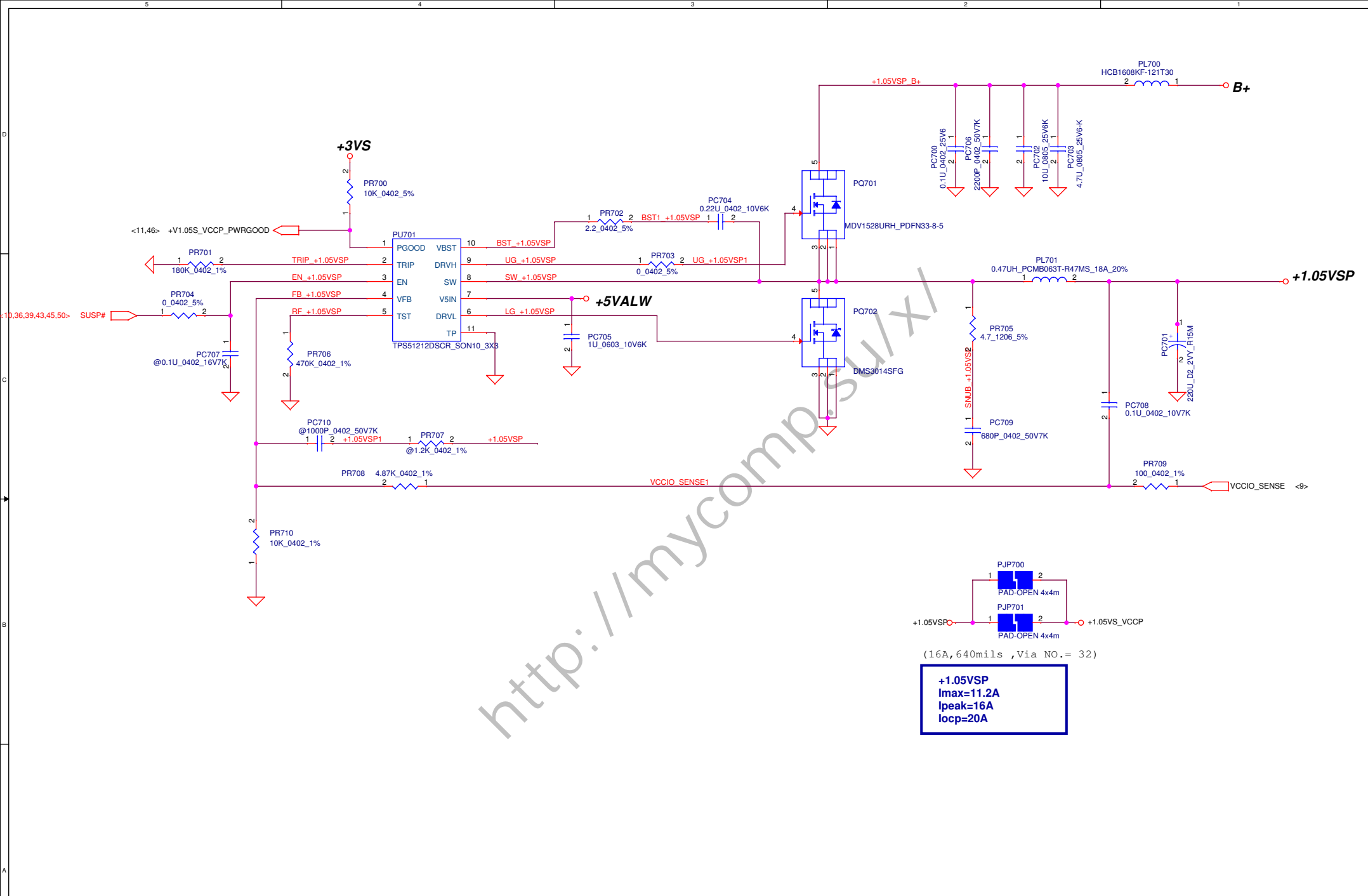
<10,36,39,44,45,50> SUSP#



+1.8V
 $I_{max}=2.25A$
 $I_{peak}=3.22A$

http://www.Comp.sul/x

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Date: Monday, July 16, 2012				Sheet	43 of 50



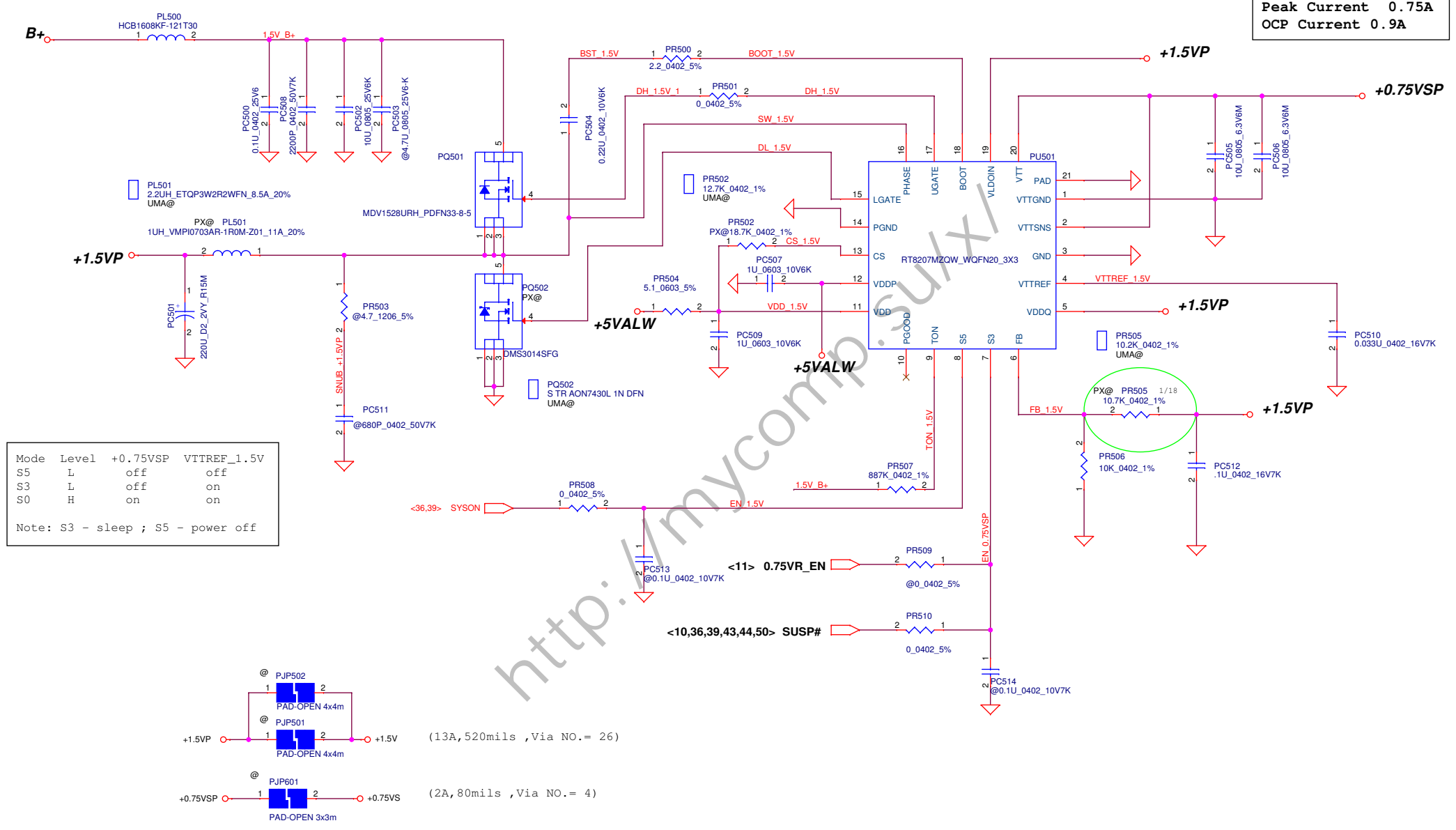
http://mycomp.com/SU/1

(16A, 640mils, Via NO. = 32)

+1.05VSP
I_{max}=11.2A
I_{peak}=16A
I_{ocp}=20A

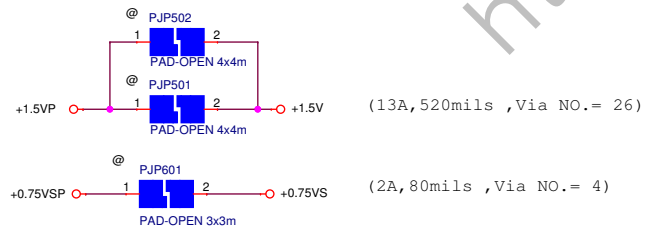
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	PWR-+V1.05S_VCCP	
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0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A

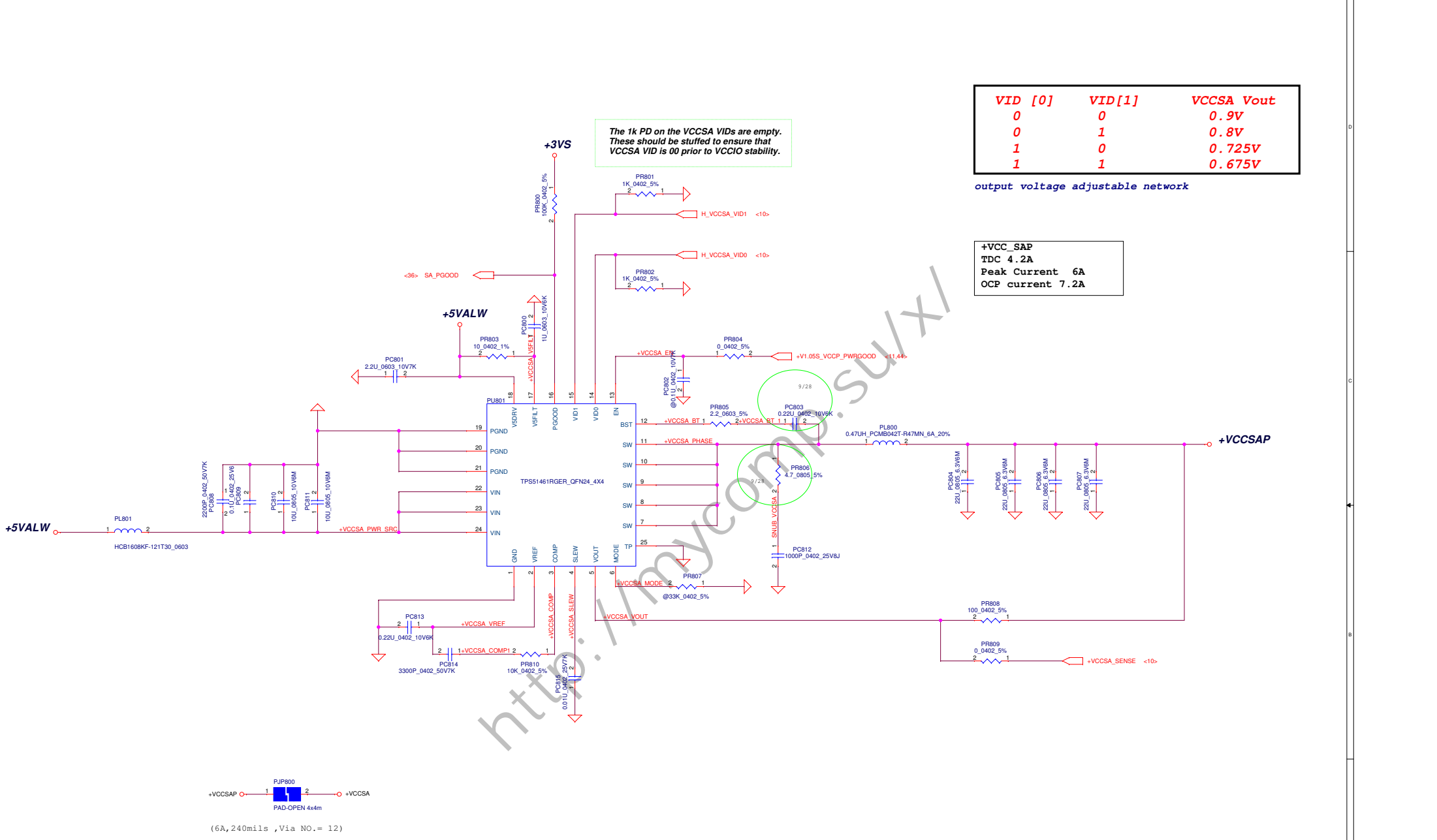


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	PWR-1.5VP / +0.75VSP	
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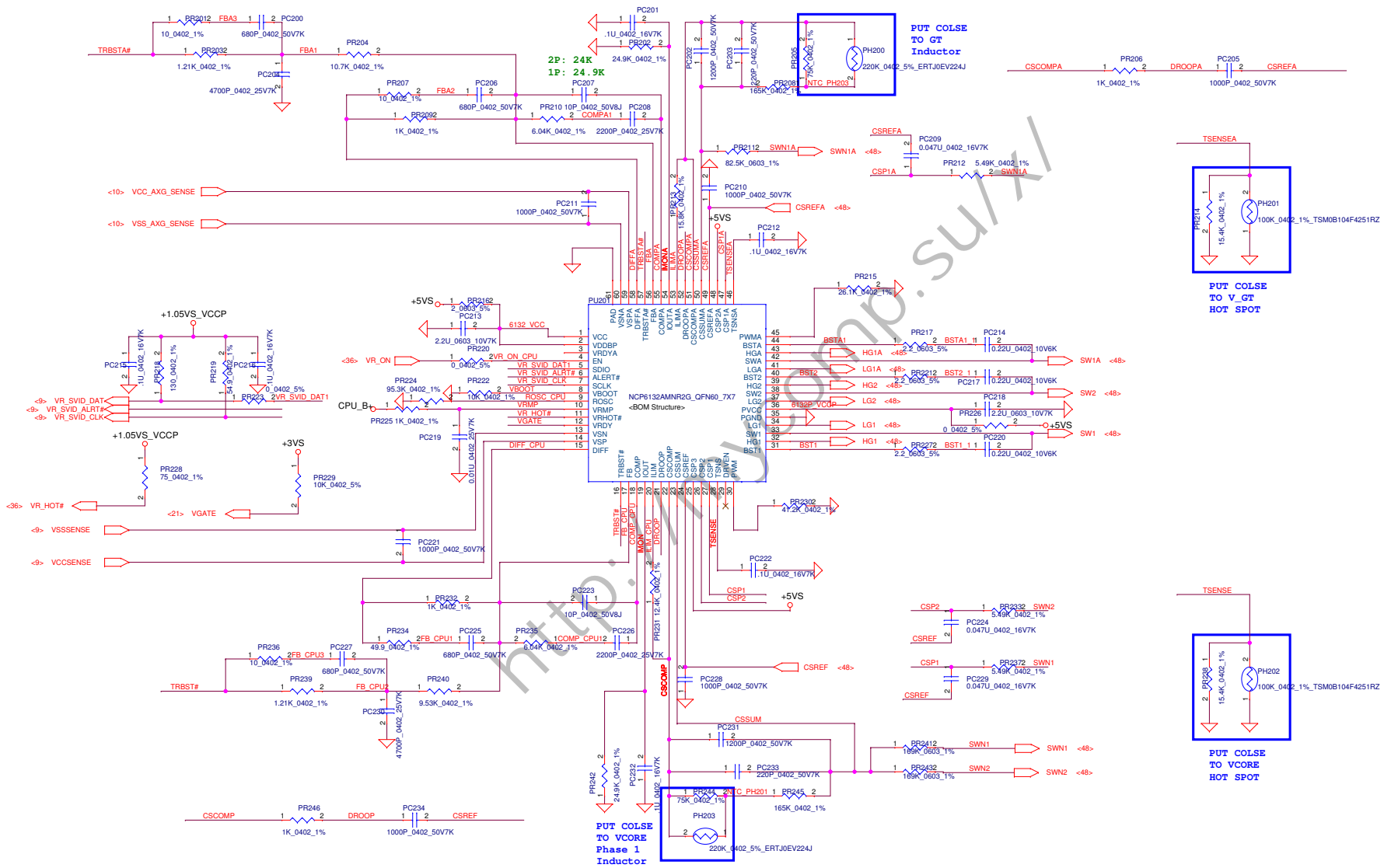
The 1k PD on the VCCSA VID's are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

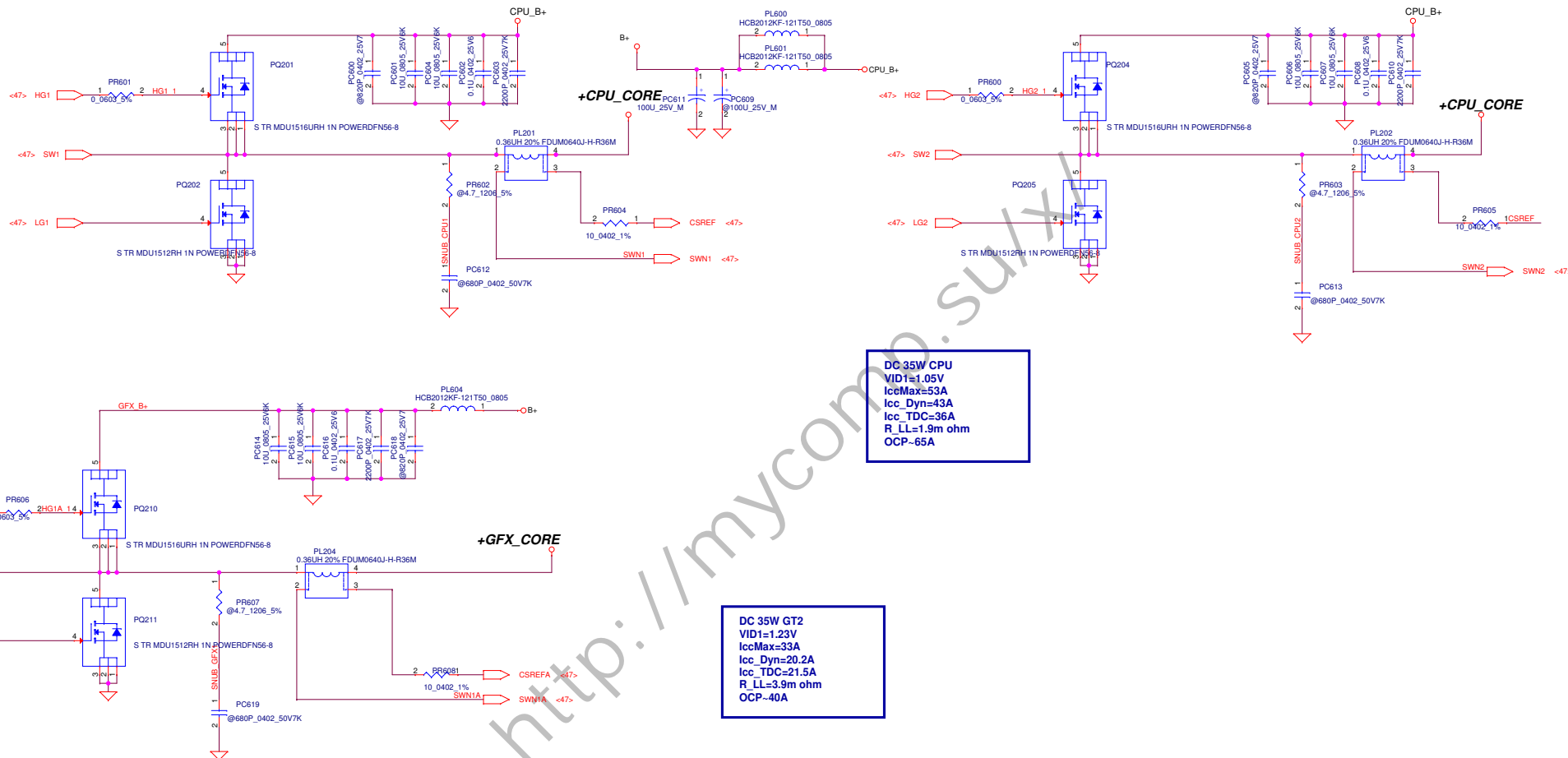
output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A


 +VCCSAP 1 2 +VCCSA
 PAD-OPEN 4x4mm
 (6A, 240mils, Via NO.= 12)
+VCCSA
 I_{max}=4.2A
 I_{peak}=6A
 I_{ocp}=7.2



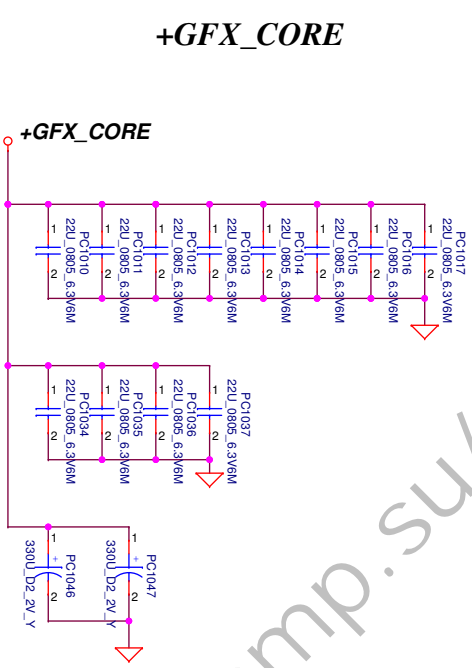
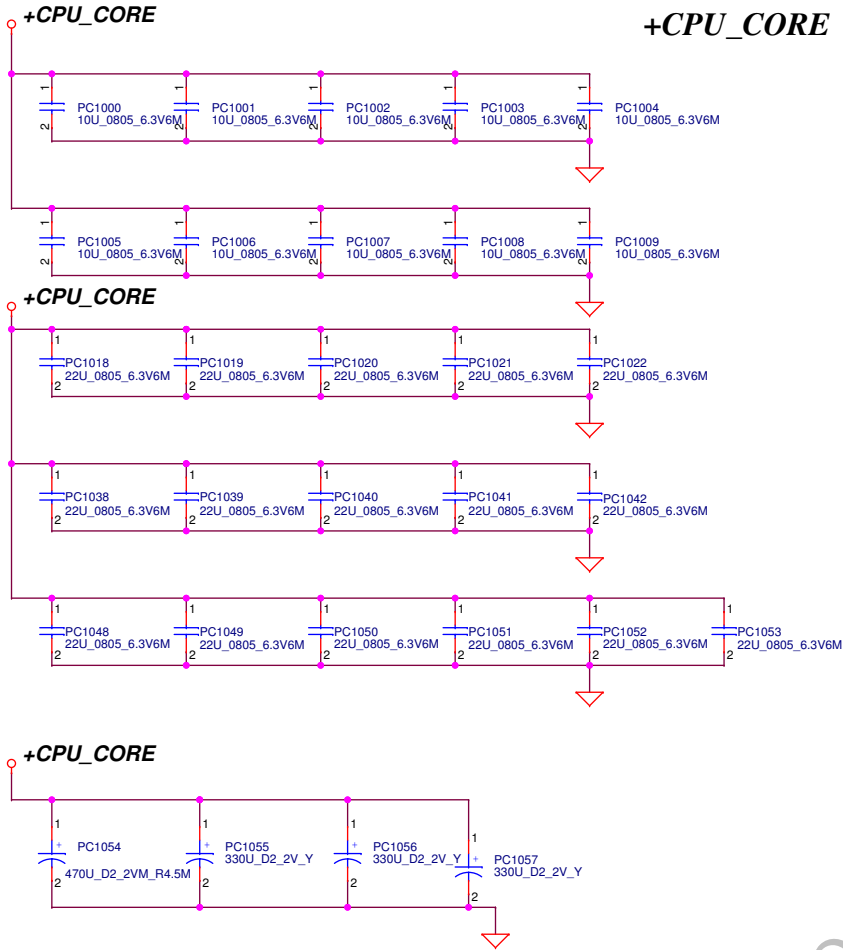
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/10/31	Deciphered Date	2012/12/31	Title	PWR-CPU CORE	
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DC 35W CPU
 VID1=1.05V
 IccMax=53A
 Icc_Dyn=43A
 Icc_TDC=36A
 R_LL=1.9m ohm
 OCP=65A

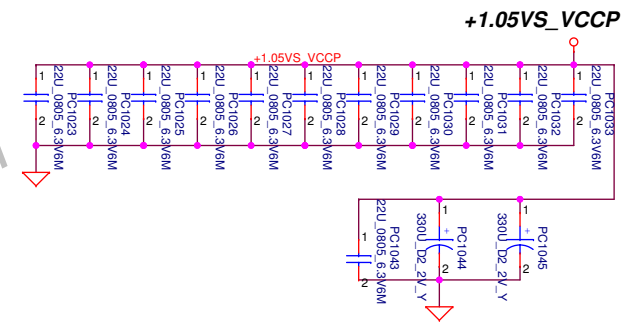
DC 35W GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm
 OCP=40A

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Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

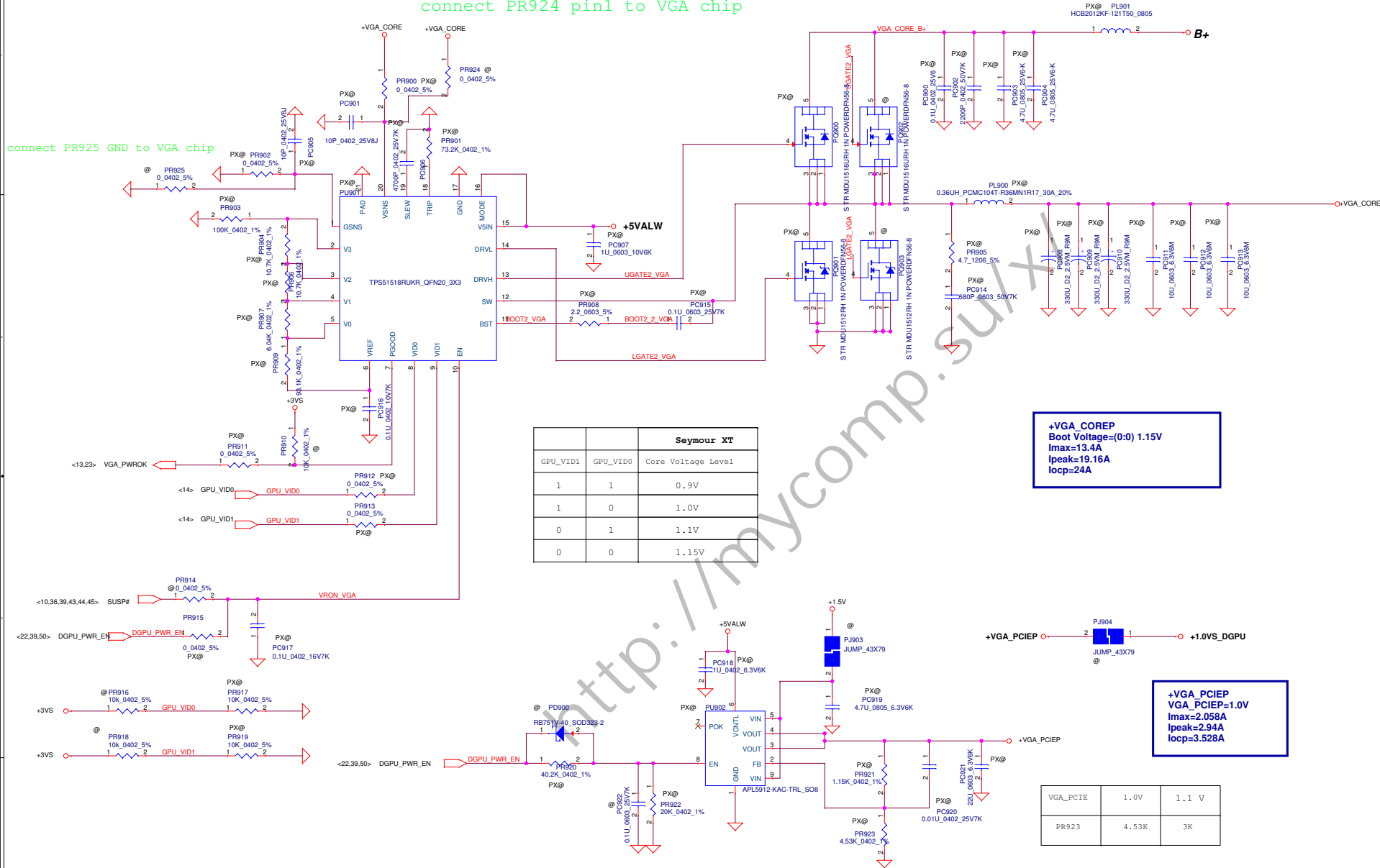


<http://mycomp.su/xl>

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connect PR924 pin1 to VGA chip

connect PR925 GND to VGA chip



Seymour XT		
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.1V
0	0	1.15V

+VGA_CORE
 Boot Voltage=(0:0) 1.15V
 I_{max}=13.4A
 I_{peak}=19.16A
 I_{ocp}=24A

+VGA_PCIE
 VGA_PCIE=1.0V
 I_{max}=2.058A
 I_{peak}=2.94A
 I_{ocp}=3.528A

VGA_PCIE	1.0V	1.1V
PR923	4.53K	3K