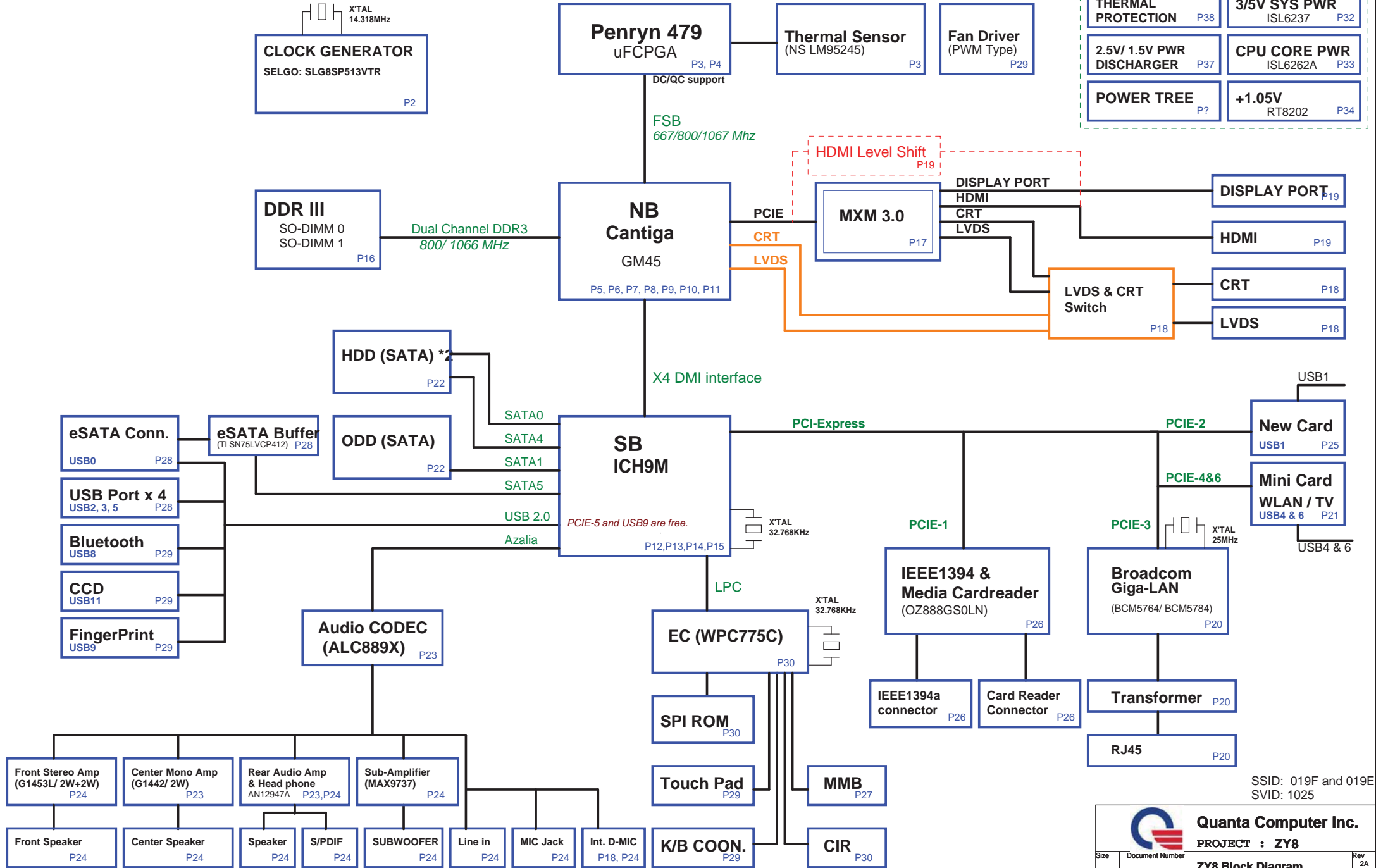


31ZY8MB0000
 ZY8 MB ASSY(DC/GM/MXM)ASSY W/O CPU
 31ZY8MB0010
 ZY8 MB ASSY(QC/GM/MXM)ASSY W/O CPU

ZY8 SYSTEM BLOCK DIAGRAM

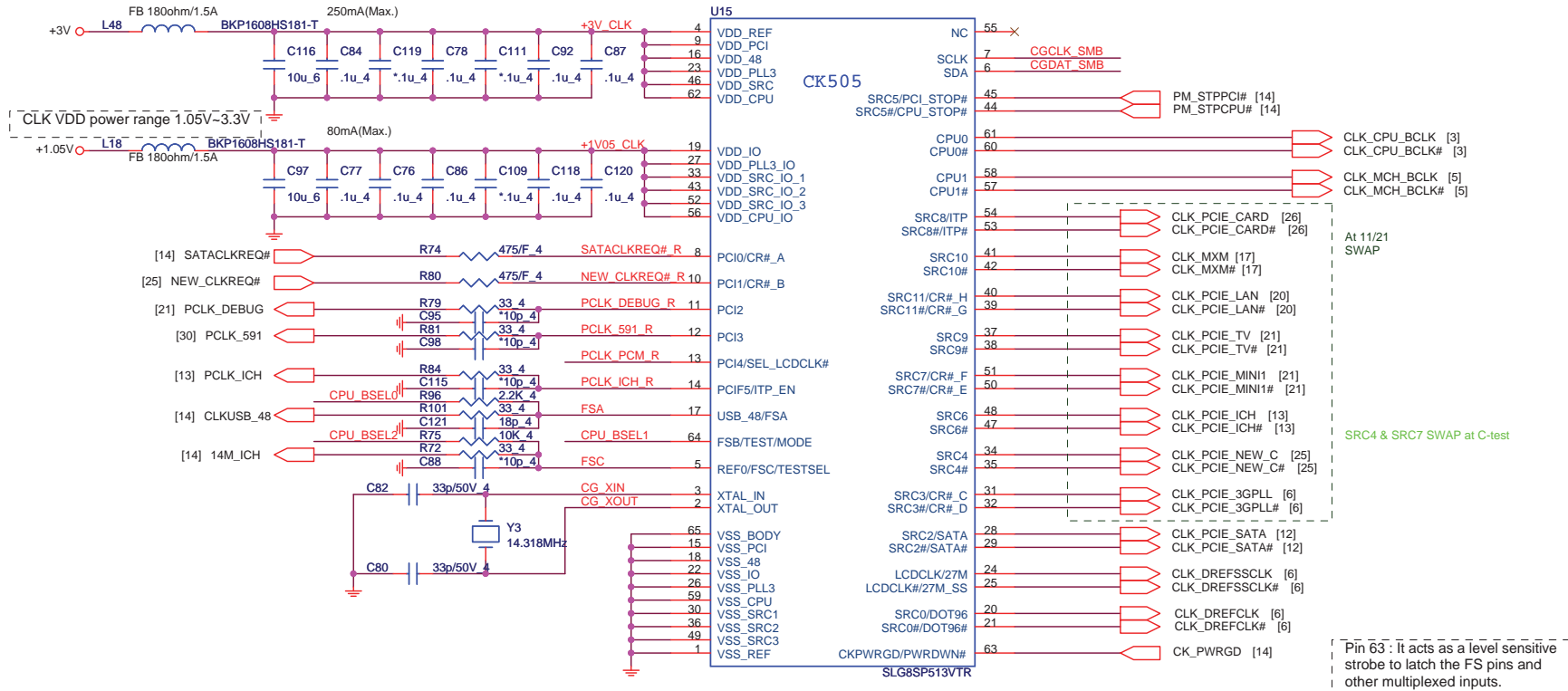


SSID: 019F and 019E
 SVID: 1025

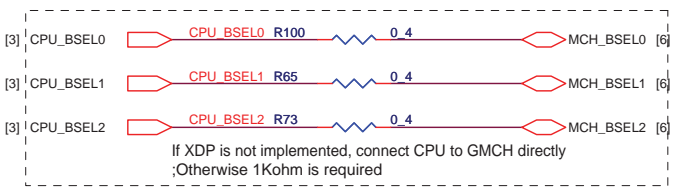
Quanta Computer Inc.
 PROJECT : ZY8
 ZY8 Block Diagram
 Date: Tuesday, December 30, 2008 Sheet 1 of 39

<http://laptop-motherboard-schematic.blogspot.com/>

Clock Generator



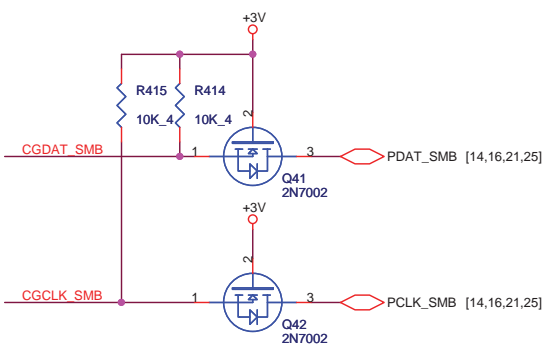
CPU Clock select



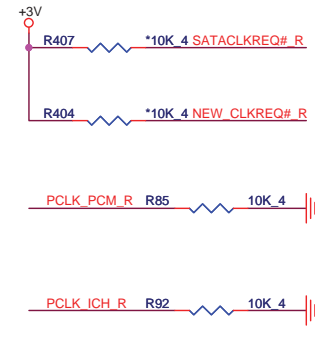
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

SMBus



Strap table



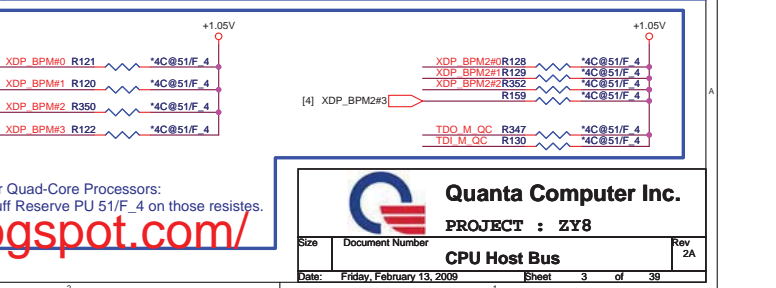
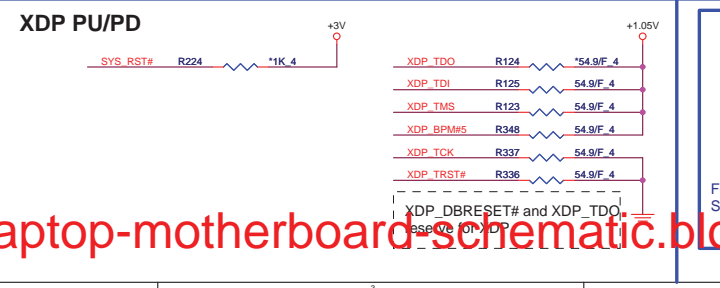
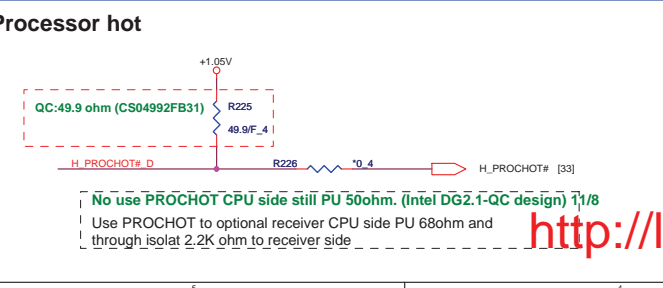
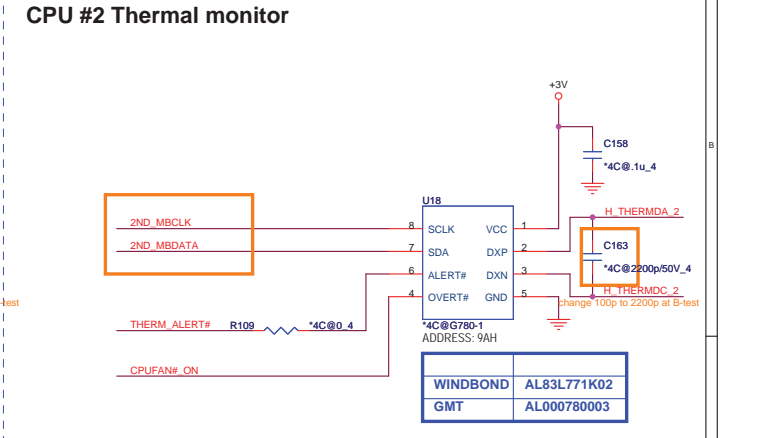
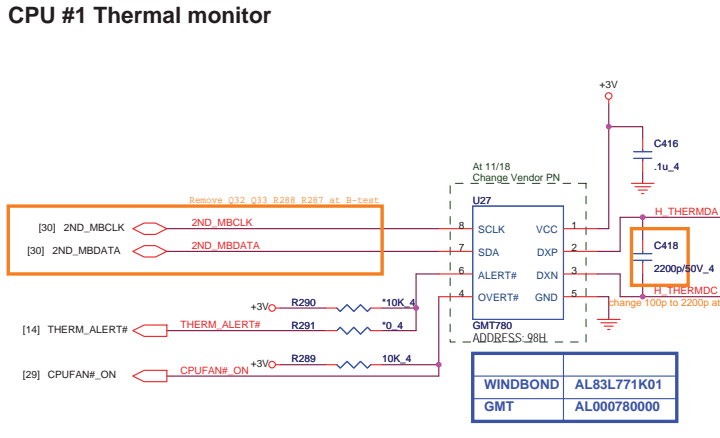
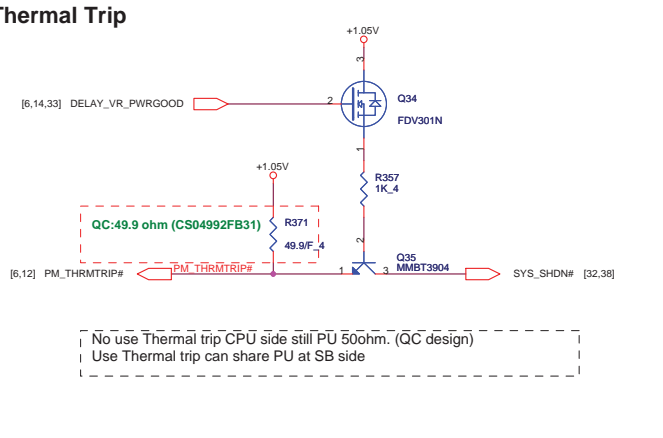
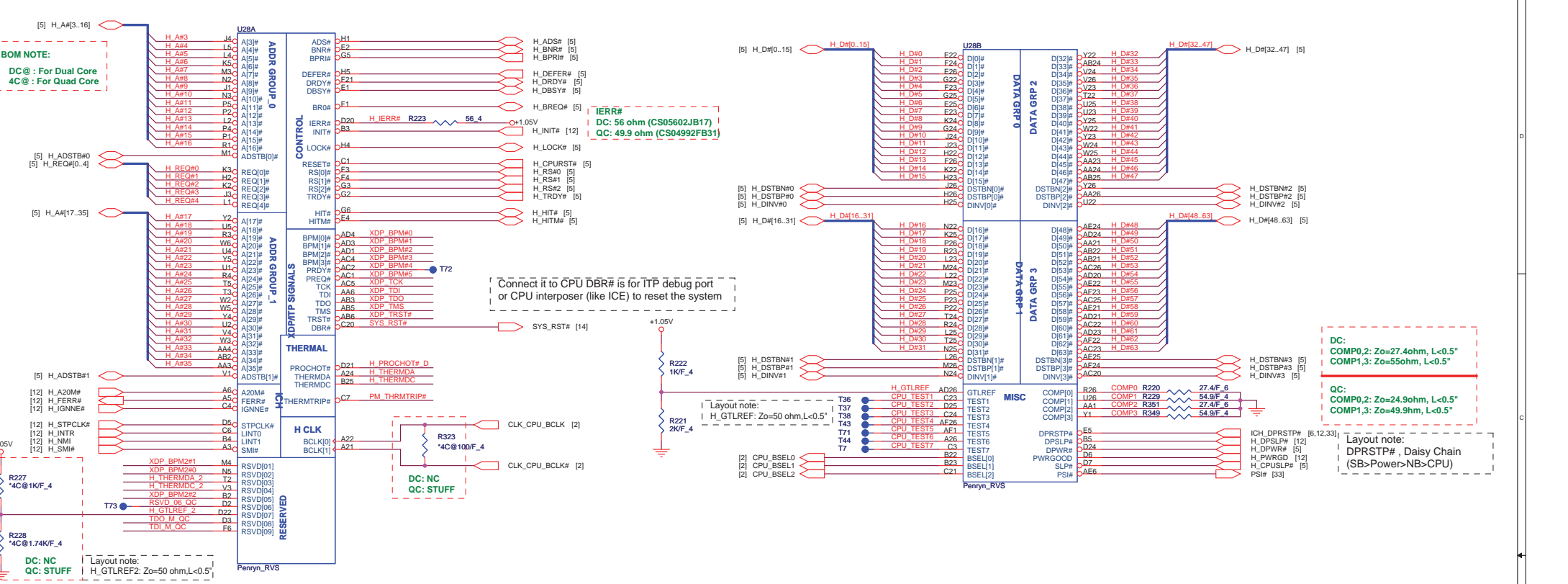
- Pin 8 : PCI_0 or CKREQ#_A selection
0 = PCI_0 output
1 = CKREQ#_A (Control SRC_0 & SRC_2)
- Pin 10 : PCI_1 or CKREQ#_B selection
0 = PCI_1 output
1 = CKREQ#_B (Control LCDCLK & SRC_4)
- Pin 13 : For Pin 20/21 and 24/25 selection
0 = LCDCLK & DOT96 for internal graphic (Setting)
1 = 27M & 27M_SS & SRC_0 for external graphic
- Pin 14 : For Pin 53/54 (CPU_ITP or SRC_8) selection
0 = SRC_8 (Setting)
1 = CPU_ITP

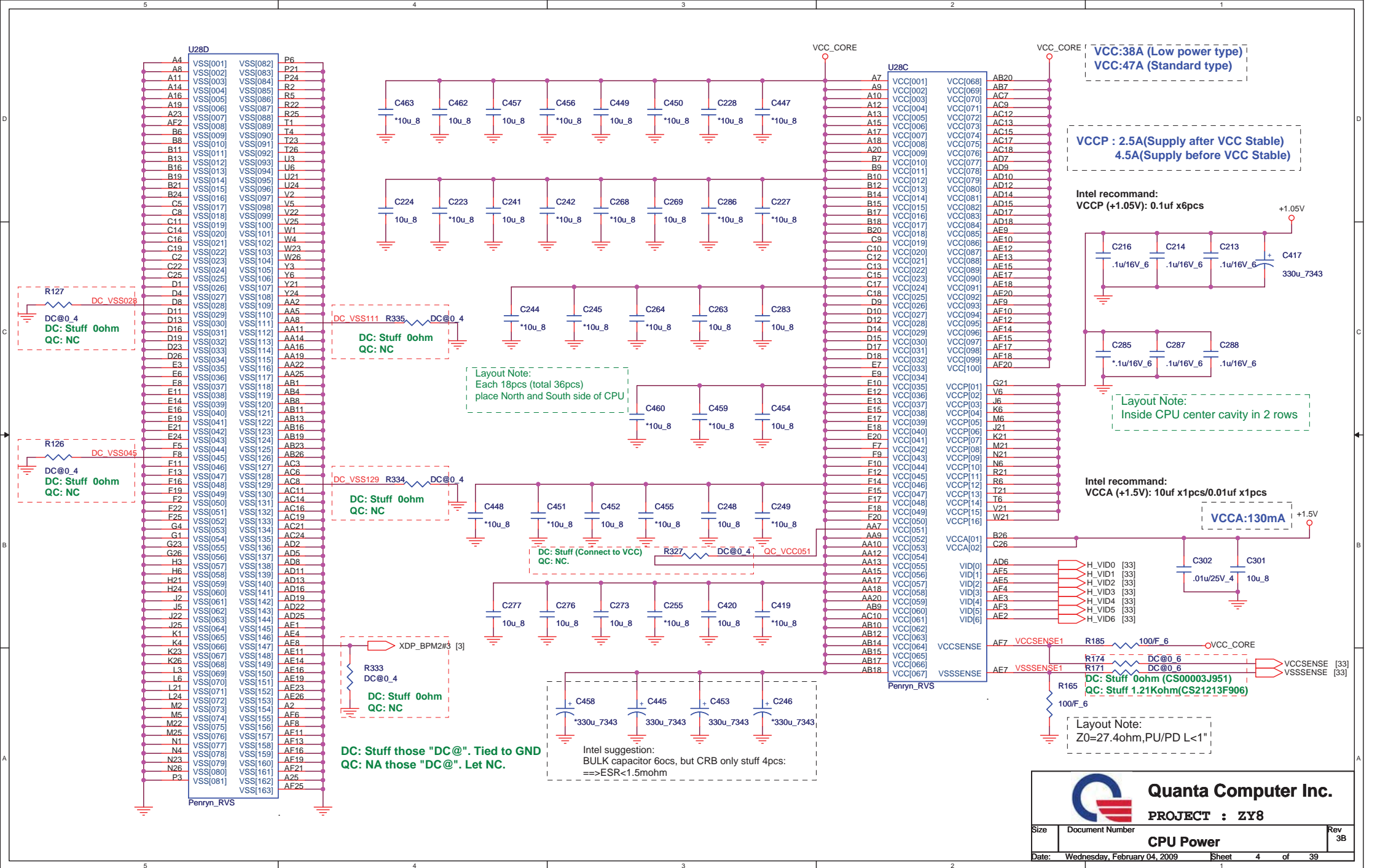


Size	Document Number	Rev
	CLOCK GENERATOR	2A

Date: Tuesday, February 17, 2009 Sheet 2 of 39

BOM NOTE:
 DC@ : For Dual Core
 4C@ : For Quad Core

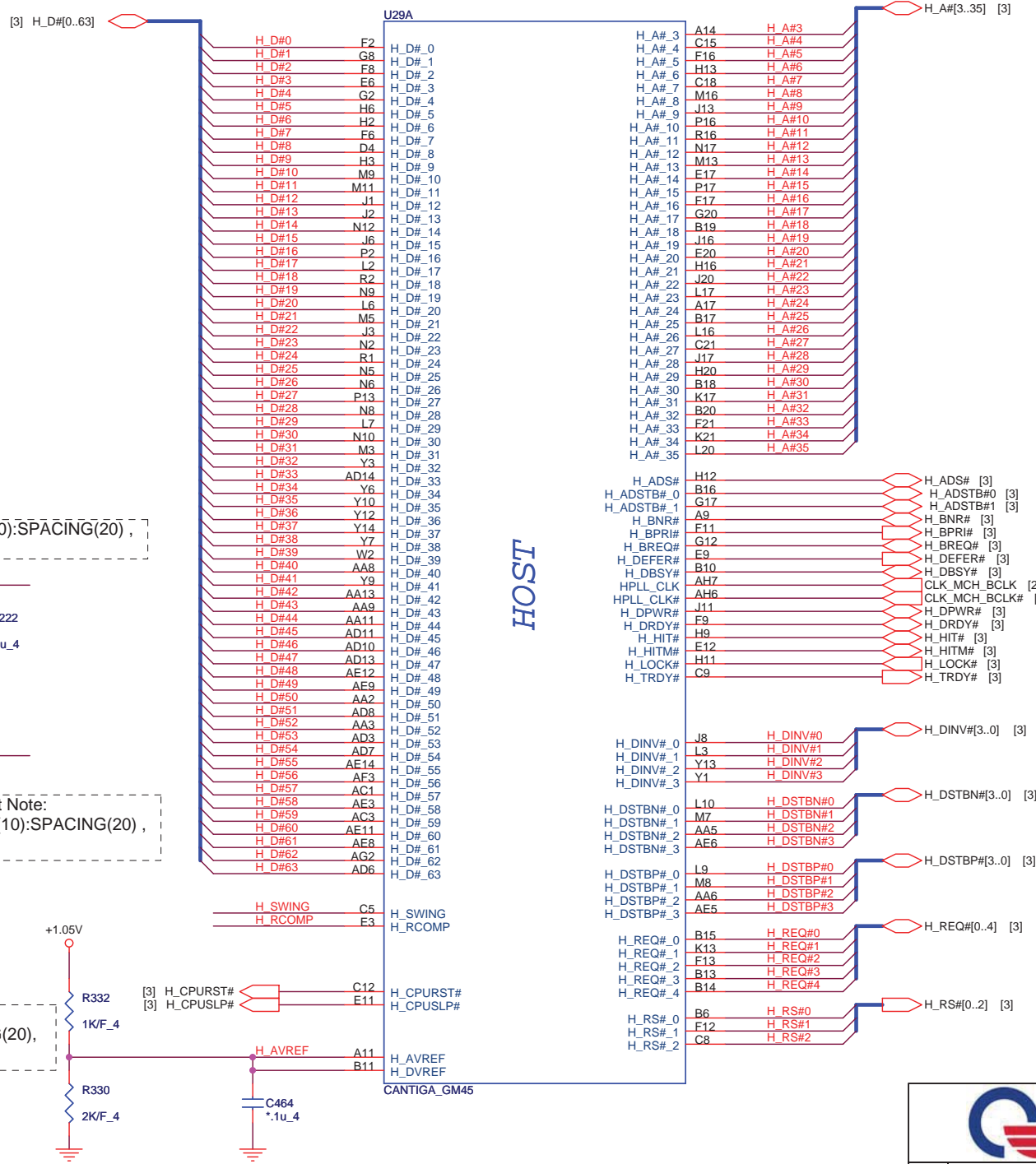




Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
		3B
CPU Power		
Date:	Wednesday, February 04, 2009	Sheet 4 of 39

	QCI P/N
Intel Cantiga (G)M	AJ0QV080T06



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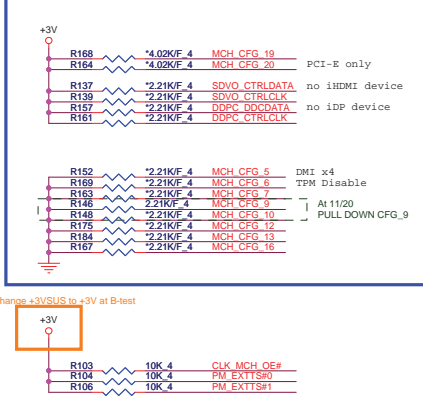
Size	Document Number	Rev
		3B
Date	Wednesday, February 11, 2009	Sheet 5 of 39

GMCH HOST

Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/iHDMI Device Present(Default) 1 = SDVO/iHDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin



NB Thermal trip pin
No use Thermal trip NB side can NC, (NB has ODT)

PM DPRST#
The Daisy chain topology should be routed from ICH9M to IMVP, then to (G)MCH and CPU, in that order.

U298

M36 RSV01
M36 RSV02
M36 RSV03
M36 RSV04
M36 RSV05
M36 RSV06
M36 RSV07
M36 RSV08
M36 RSV09

T24 RSV014
B31 RSV015
M1 RSV017
Y21 RSV020

B2 RSV021
B3 RSV022
B4 RSV023
B5 RSV024
B6 RSV025

T20 MCH_BSELO
T20 MCH_BSEL1
T20 MCH_CFG_3
T19 MCH_CFG_4
T19 MCH_CFG_5
T19 MCH_CFG_6
T19 MCH_CFG_7
T14 MCH_CFG_9
T17 MCH_CFG_10
T22 MCH_CFG_11
T13 MCH_CFG_12
T13 MCH_CFG_13
T13 MCH_CFG_14
T13 MCH_CFG_15
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T11 MCH_CFG_17
T11 MCH_CFG_18
T11 MCH_CFG_19
T11 MCH_CFG_20

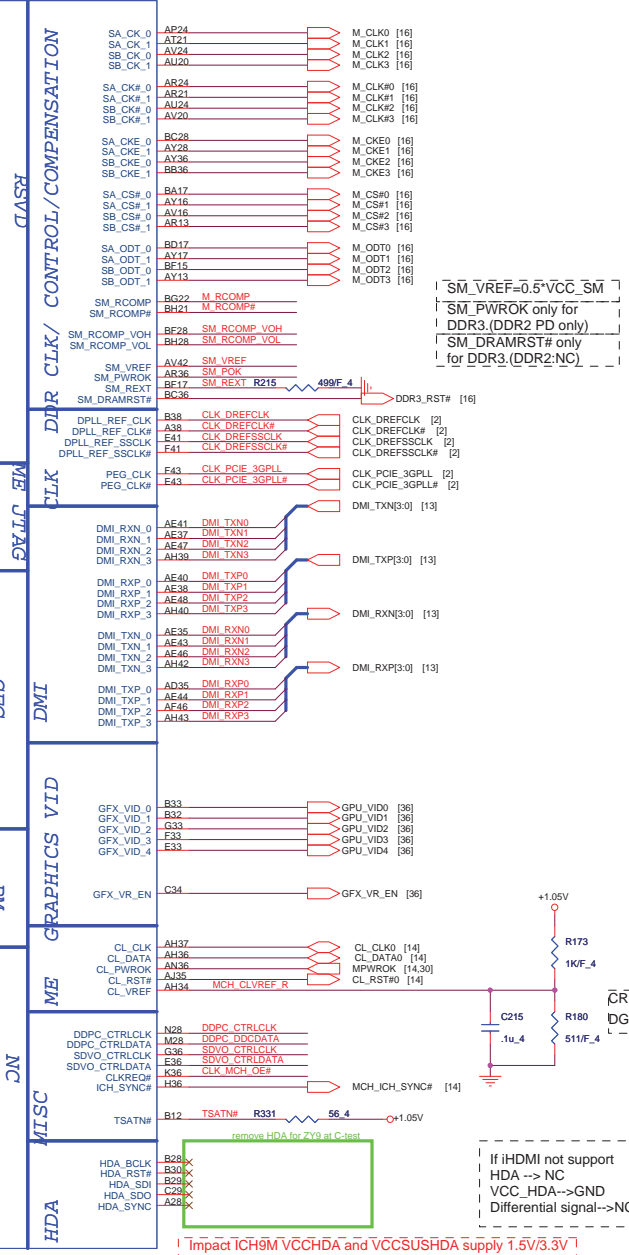
T25 JTAG_TCK
T18 JTAG_TDI
T25 JTAG_TDO
T21 JTAG_TMS

T25 MCH_BSELO
T25 MCH_BSEL1
T25 MCH_CFG_3
T19 MCH_CFG_4
T19 MCH_CFG_5
T19 MCH_CFG_6
T19 MCH_CFG_7
T14 MCH_CFG_9
T17 MCH_CFG_10
T22 MCH_CFG_11
T13 MCH_CFG_12
T13 MCH_CFG_13
T13 MCH_CFG_14
T13 MCH_CFG_15
T11 MCH_CFG_16
T11 MCH_CFG_17
T11 MCH_CFG_18
T11 MCH_CFG_19
T11 MCH_CFG_20

R29 PM_SYNC#
R29 ICH_DPRSTP#
R29 PM_DPRSTP#
R29 PM_EXT_TSP_#
R29 PM_EXT_TSP_#_0
R29 PM_EXT_TSP_#_1
R29 PWROK
R29 RSTIN#
R29 RSTIN#
R29 THERMTRIP#
R29 DPRSLV#

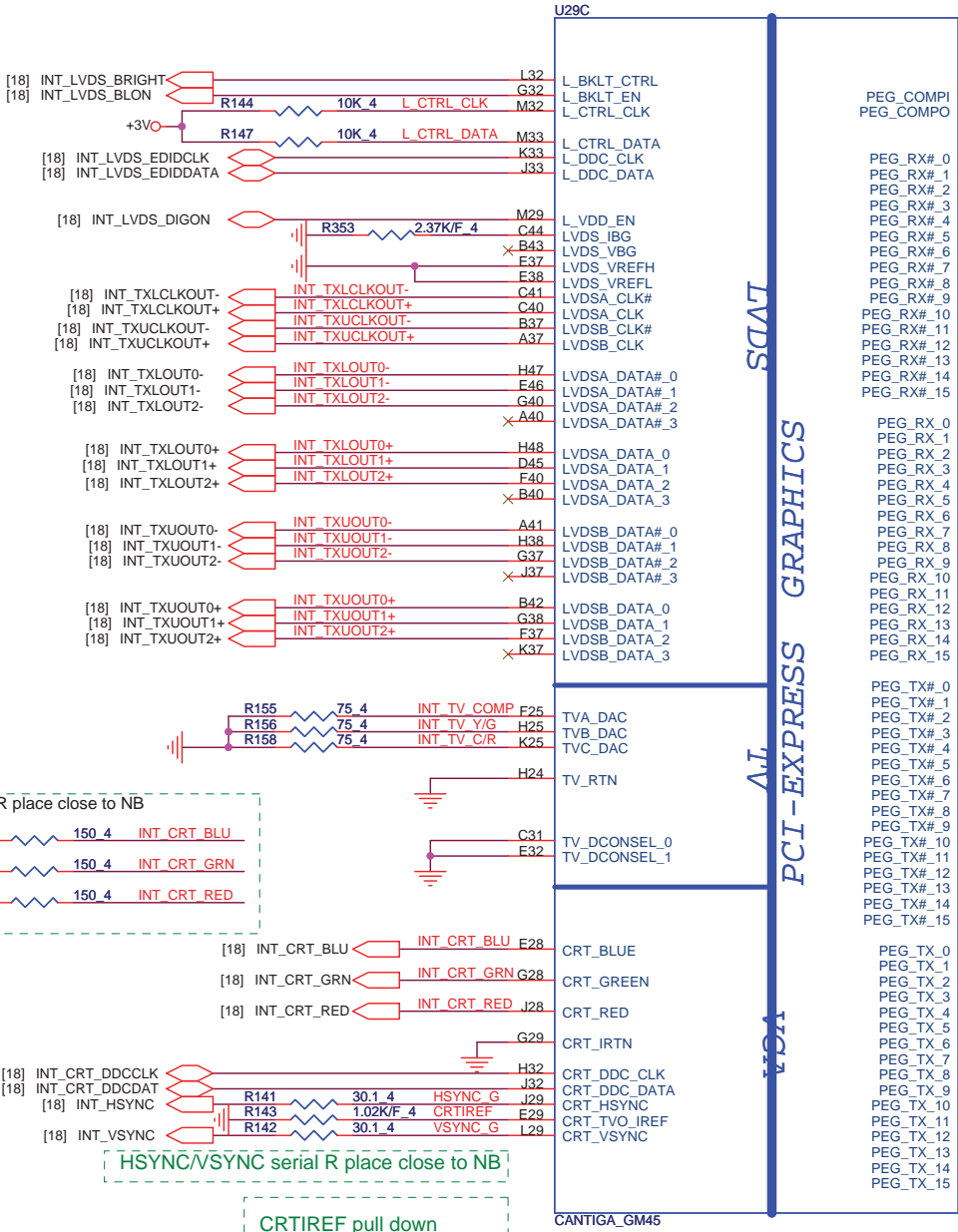
BG48 NC_1
BG48 NC_2
BG48 NC_3
BG48 NC_4
BG48 NC_5
BG48 NC_6
BG48 NC_7
BG48 NC_8
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BG48 NC_10
BG48 NC_11
BG48 NC_12
BG48 NC_13
BG48 NC_14
BG48 NC_15
BG48 NC_16
BG48 NC_17
BG48 NC_18
BG48 NC_19
BG48 NC_20
BG48 NC_21
BG48 NC_22
BG48 NC_23
BG48 NC_24
BG48 NC_25

B28 HDA_BCLK
B30 HDA_RST#
B30 HDA_SDI
C23 HDA_SDO
A28 HDA_SYNC

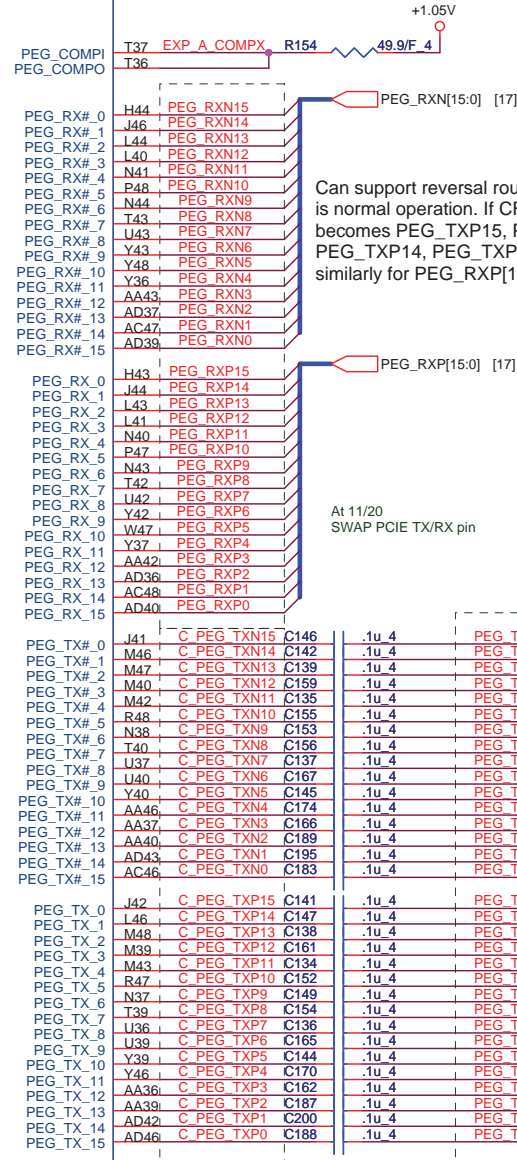


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PROJECT : ZY8
GMCH DMI

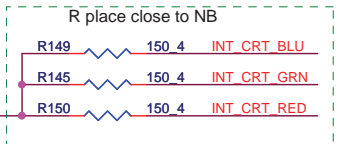
Document Number
Date: Wednesday, February 11, 2009 Sheet 6 of 39



L<0.5", If PCIe not support still connect to +VCC_PEG



Can support reversal routing. If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]



HSYNC/VSYNC serial R place close to NB

CRTIREF pull down for IV cantiga 1.02k ohm/F

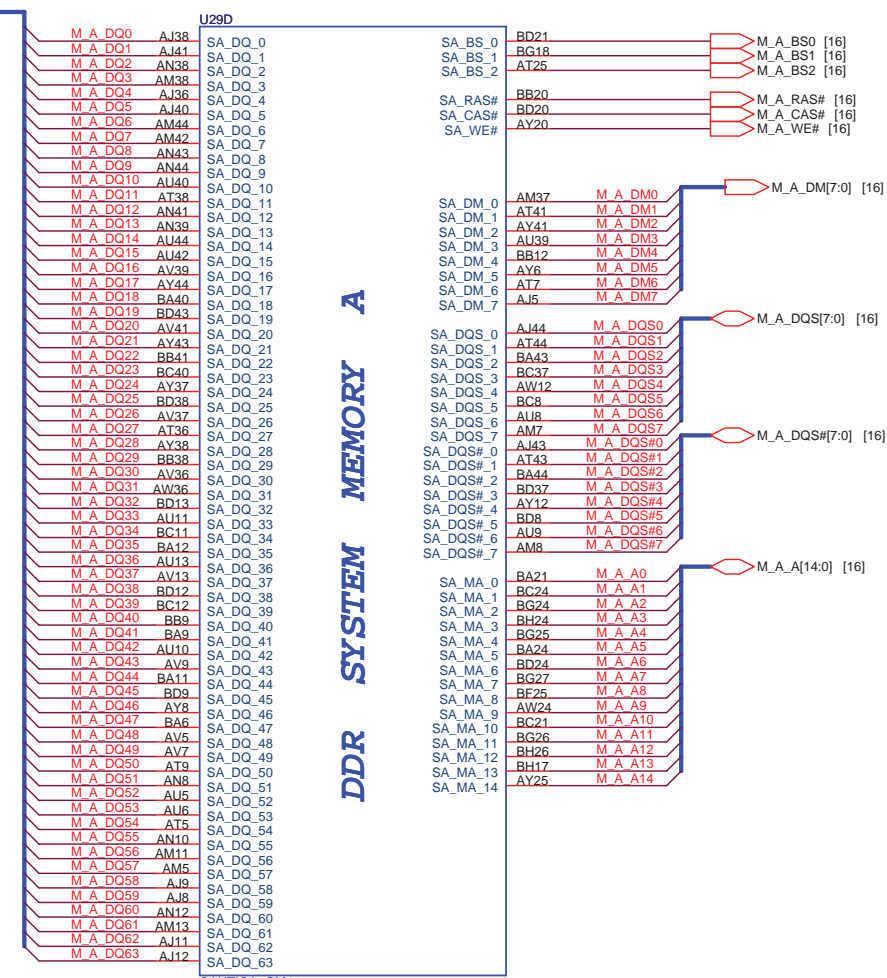
Quanta Computer Inc.
PROJECT : ZY8

Size Document Number Rev 3B

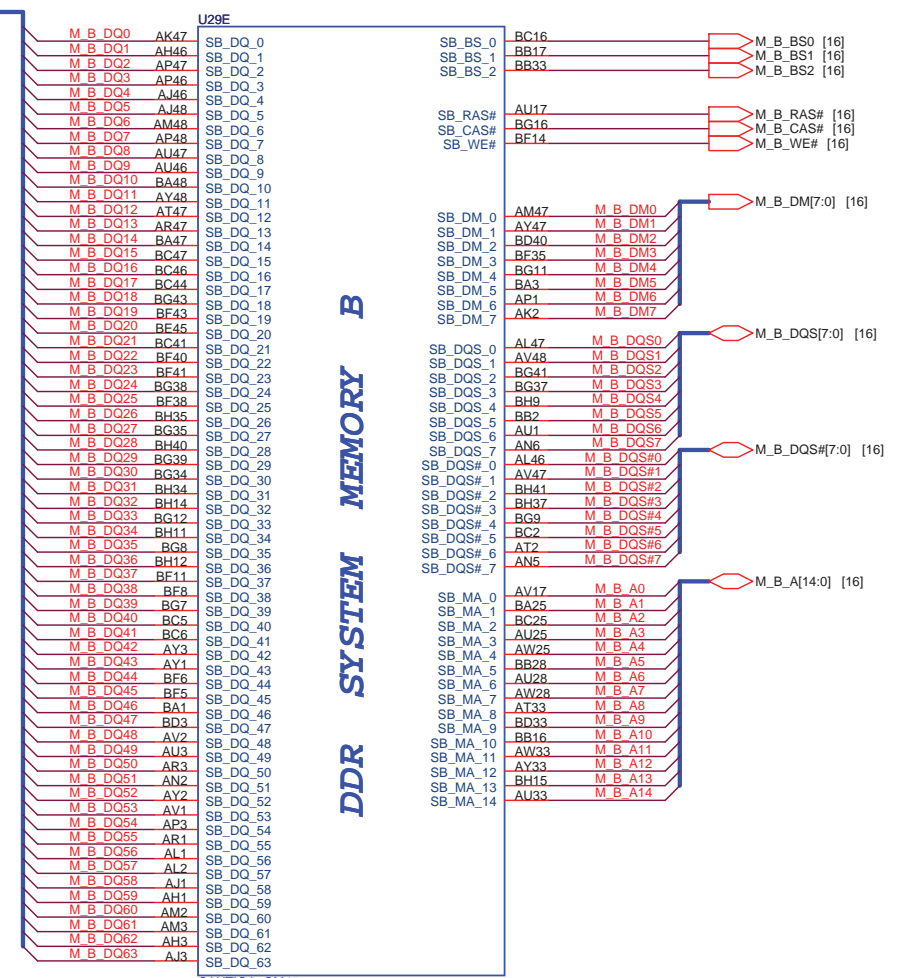
GMCH VGA/PEG

Date: Wednesday, February 11, 2009 Sheet 7 of 39


[16] M_A_DQ[63:0]



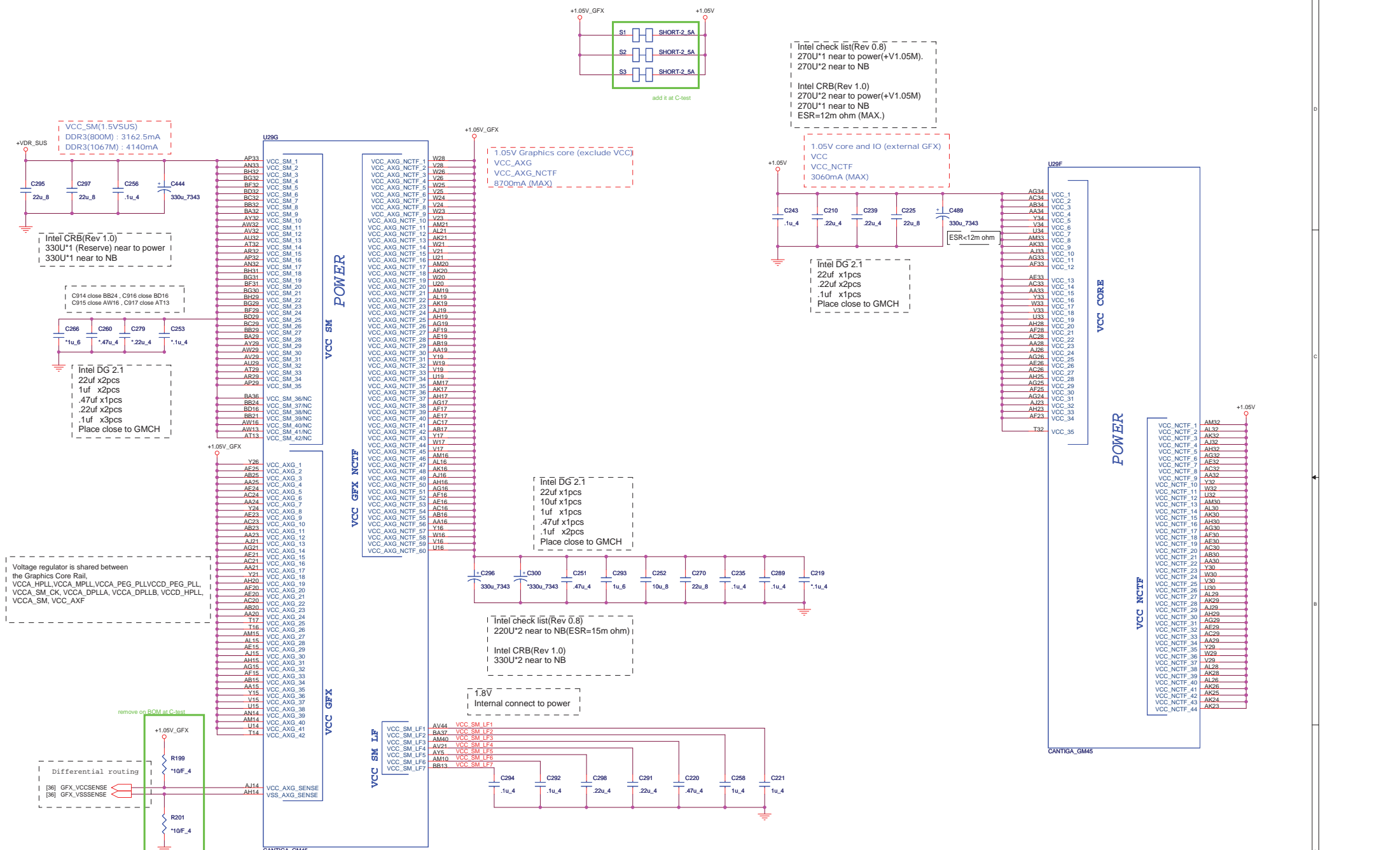
[16] M_B_DQ[63:0]



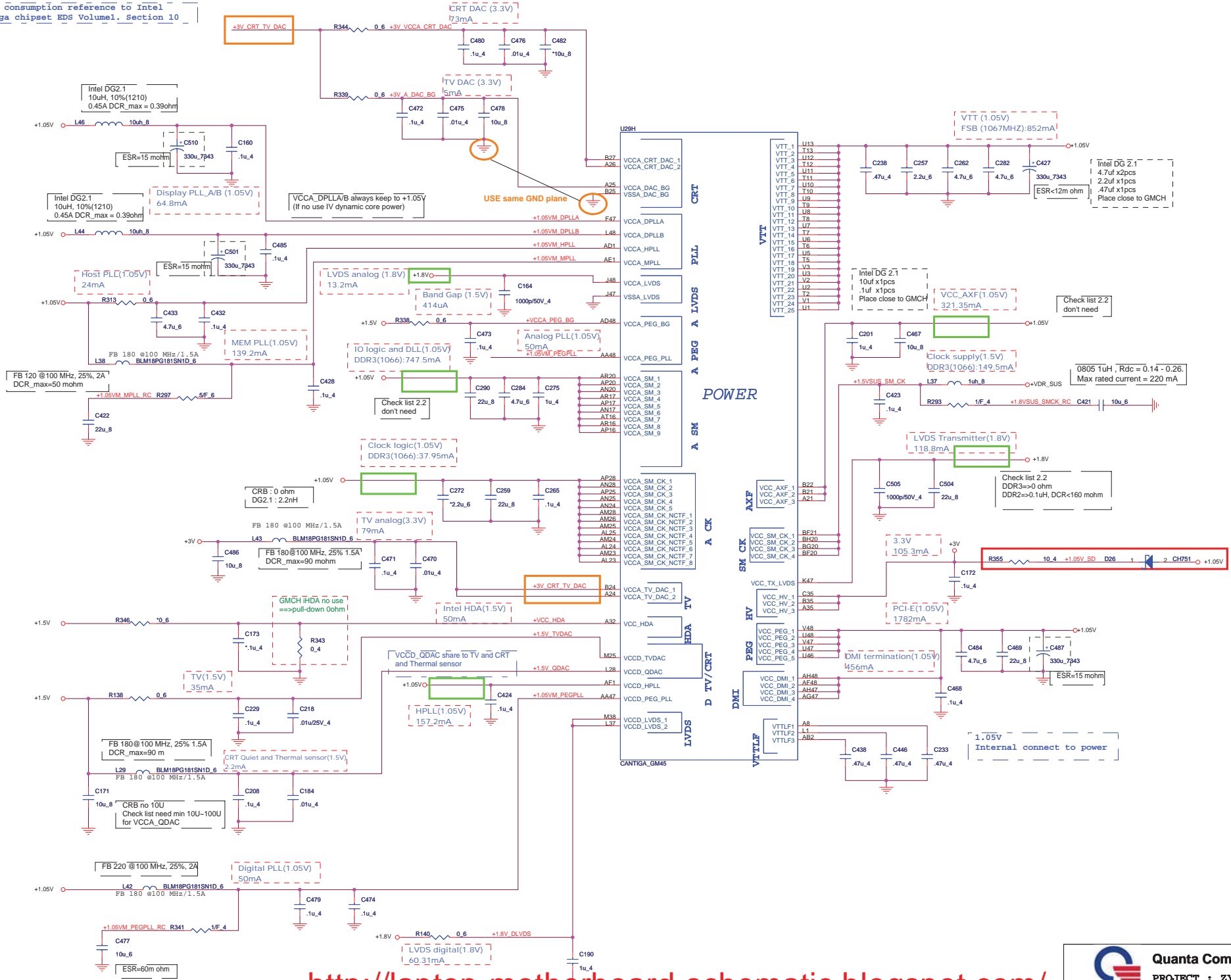
GMCH (CANTIGA)

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 PROJECT : ZY8

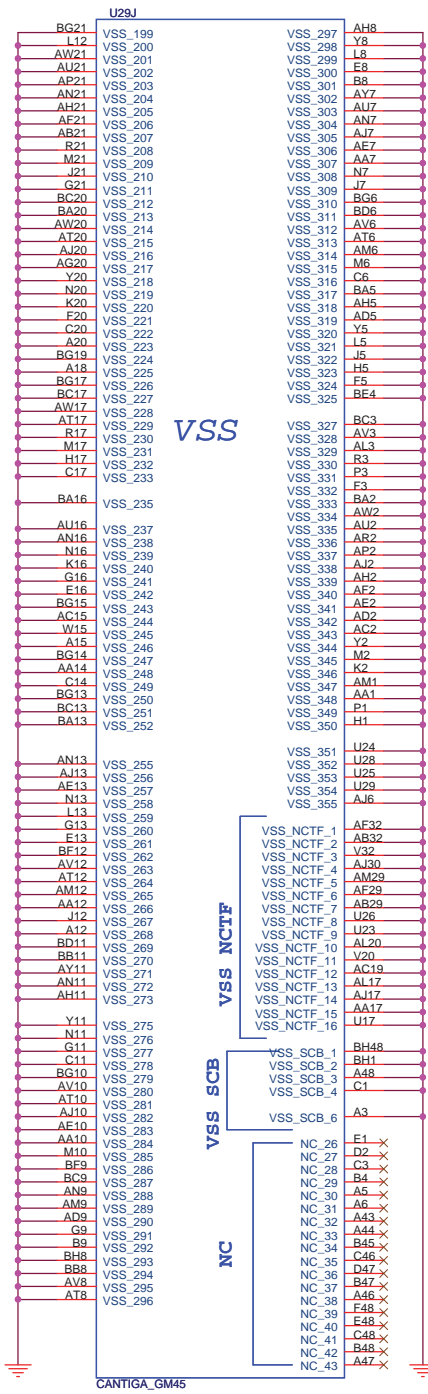
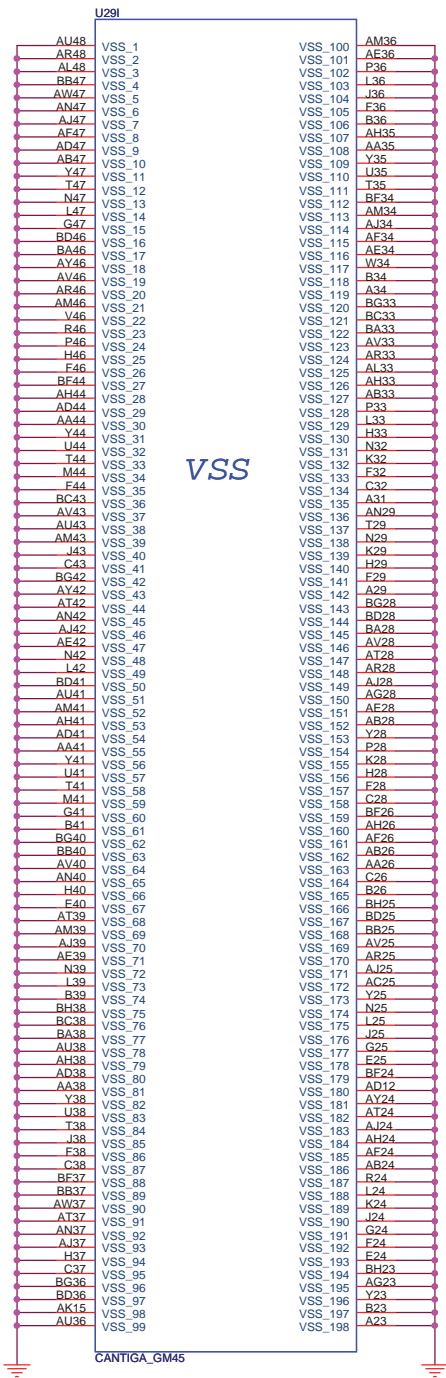
Size	Document Number	Rev
	GMCH DDR I/F	3B
Date:	Wednesday, February 11, 2009	Sheet 8 of 39




1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +V GFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest



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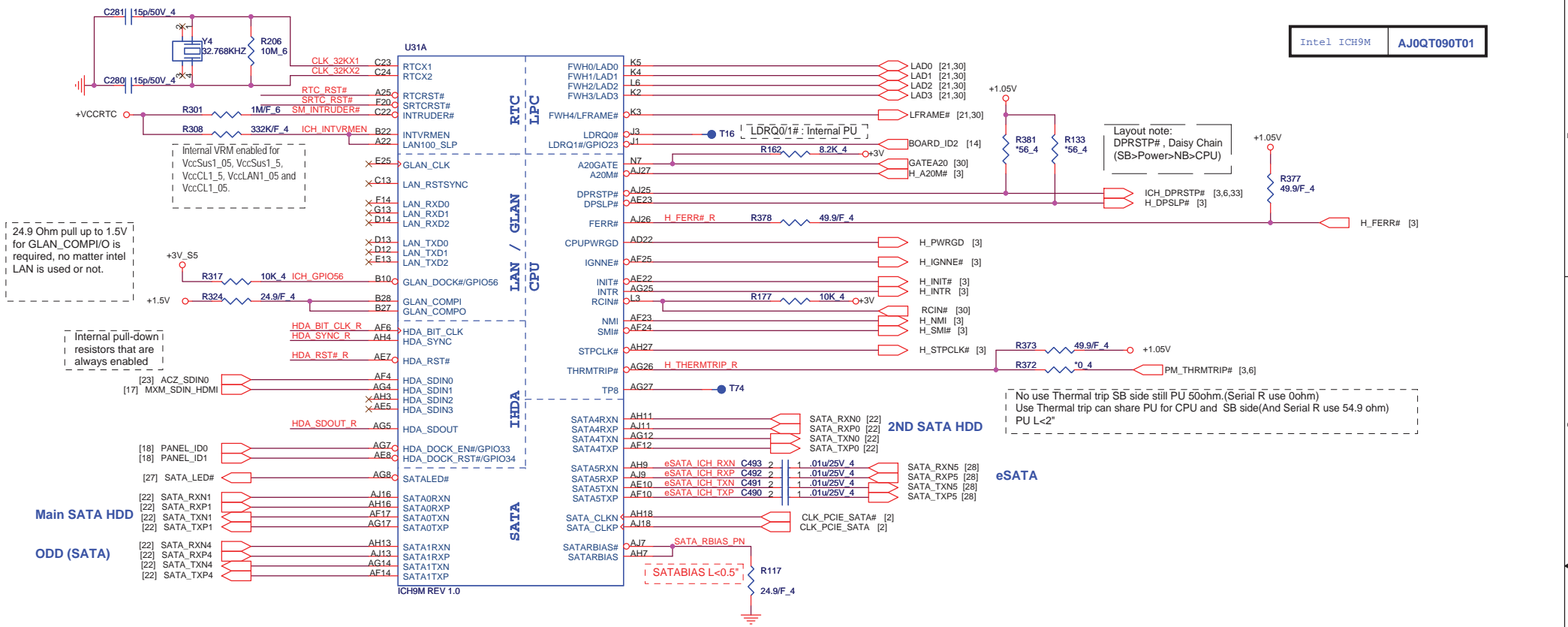


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PROJECT : ZY8

Size	Document Number	Rev
	GMCH VSS	3B

Date: Wednesday, February 11, 2009 Sheet 11 of 39



24.9 Ohm pull up to 1.5V for GLAN_COMP# is required, no matter intel LAN is used or not.

Internal pull-down resistors that are always enabled

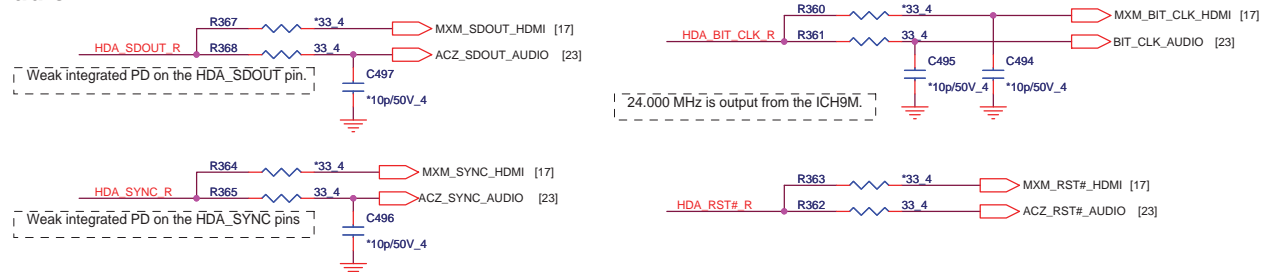
Main SATA HDD

ODD (SATA)

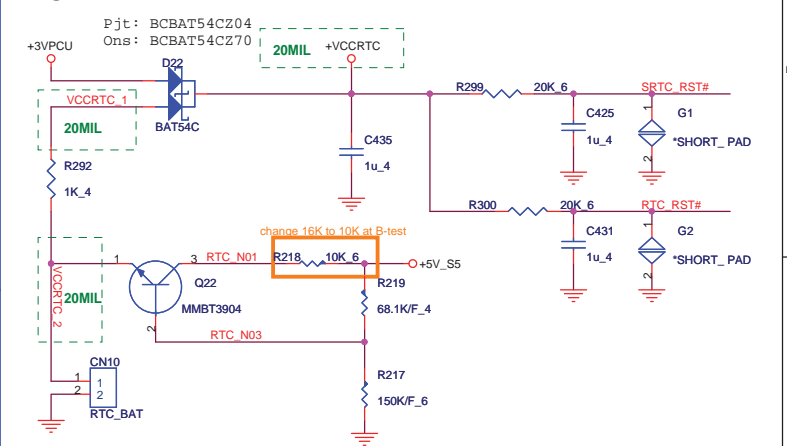
Layout note:
DPRSTP#, Daisy Chain (SB>Power>NB>CPU)

No use Thermal trip SB side still PU 50ohm (Serial R use 0ohm)
Use Thermal trip can share PU for CPU and SB side (And Serial R use 54.9 ohm)
PU L<2"

HD Audio



RTC



South Bridge Strap Pin (1/3)

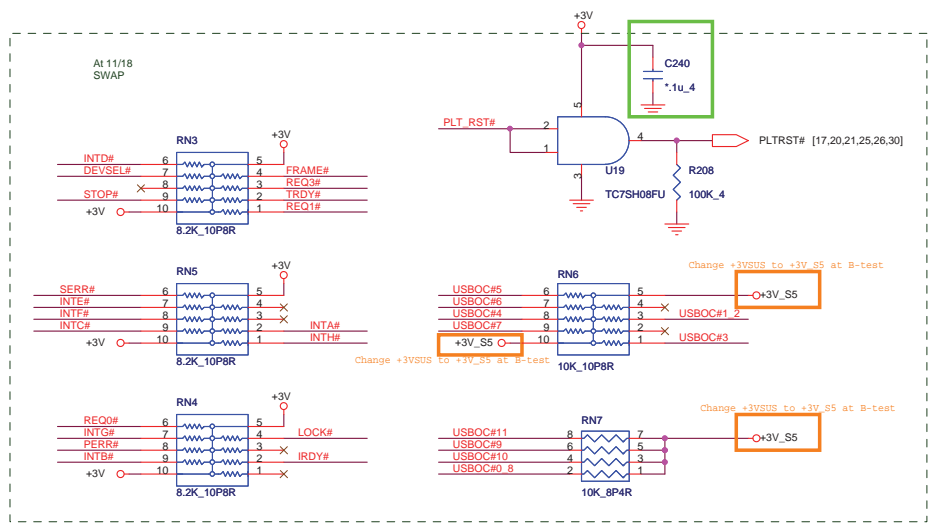
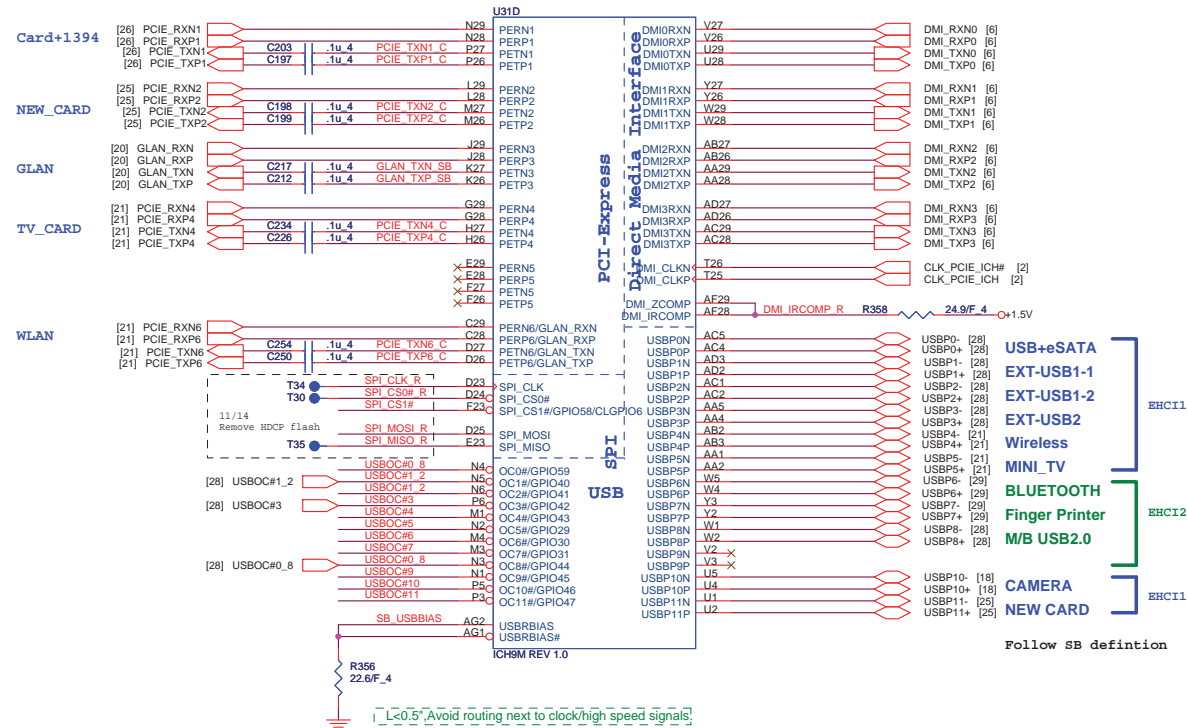
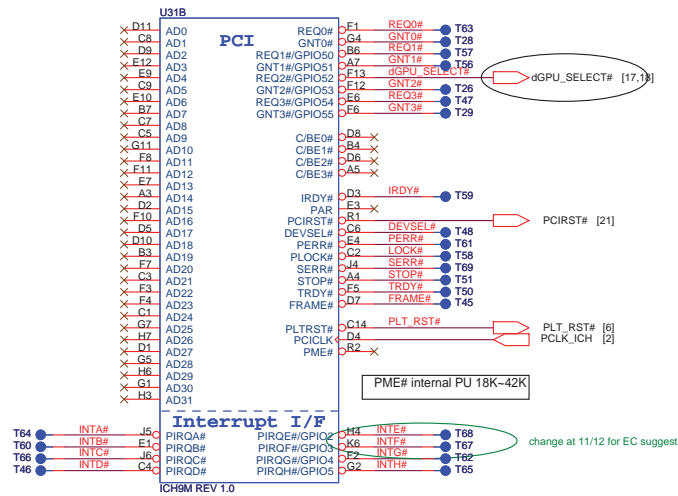
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 HDA_SDOUT Description	[14] ICH_TP3 → ICH_TP3 R316 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1 (Port 1-4)	PWROK	0 1 Normal operation (Default) 1 0 Set PCIe port config 1 bit 1	HDA_SDOUT_R R366 *1K_4

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PROJECT : ZY8

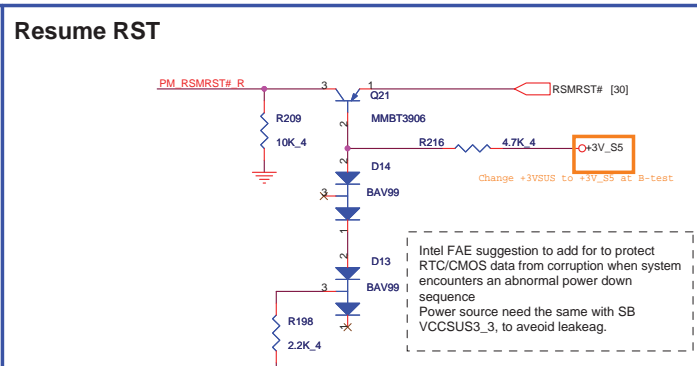
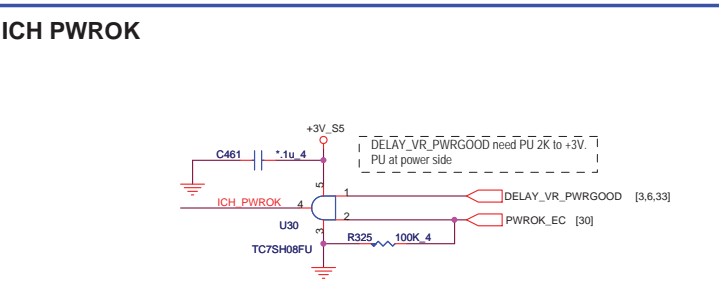
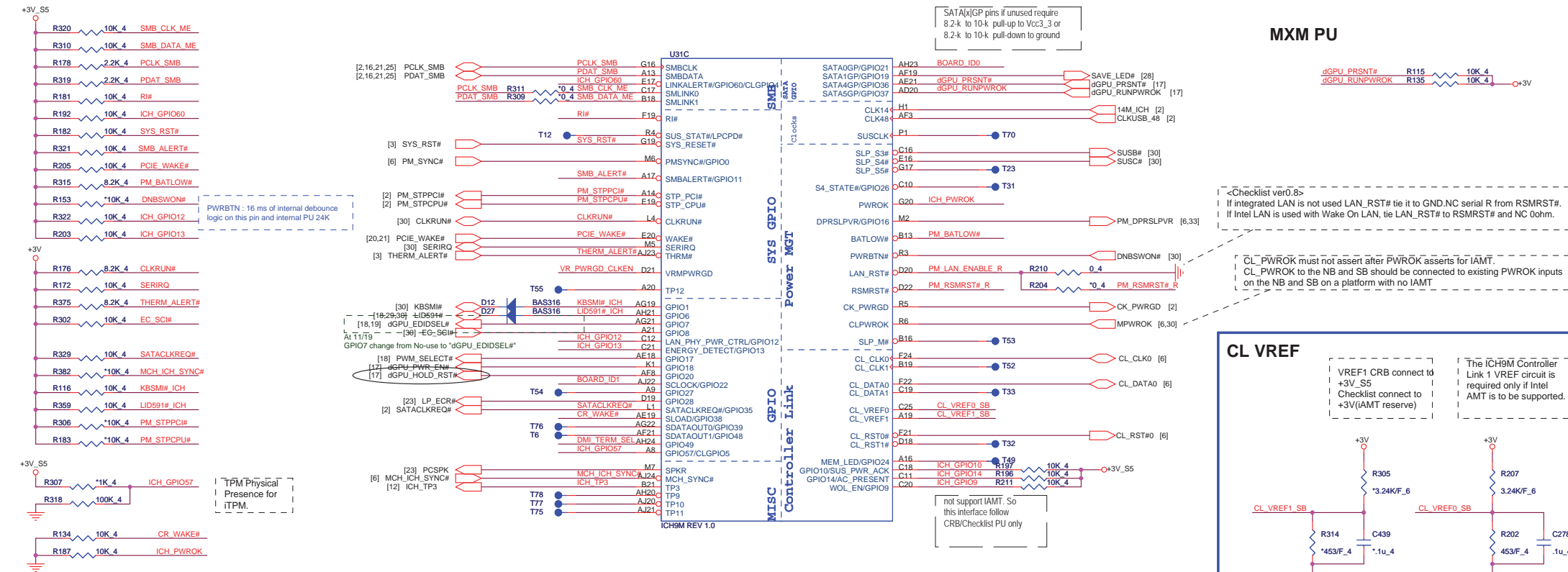
Size	Document Number	Rev
	ICH9M HOST	3B

Date: Tuesday, February 10, 2009 Sheet 12 of 39



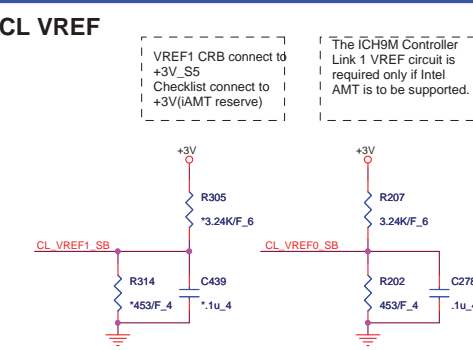
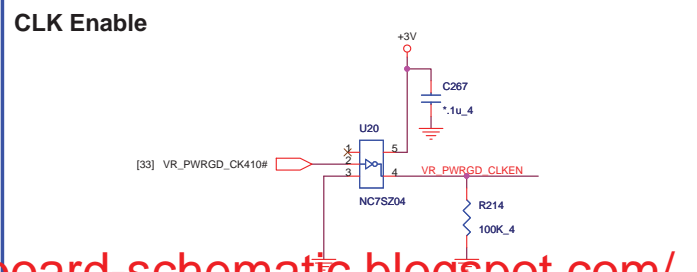
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD									
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0										
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default										
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R193 *1K_4									
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R200 *20K_4 +3V_S5									
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>0</td> <td>1</td> <td>SPI</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI	GNT0# R186 *1K_4			
PCI_GNT#0	SPI_CS#1	Boot Location											
0	1	SPI											
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>LPC(Default)</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	1	0	PCI	1	1	LPC(Default)	SPI_CS1# R191 *1K_4
PCI_GNT#0	SPI_CS#1	Boot Location											
1	0	PCI											
1	1	LPC(Default)											



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R166 *1K 4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R383 *1K 4



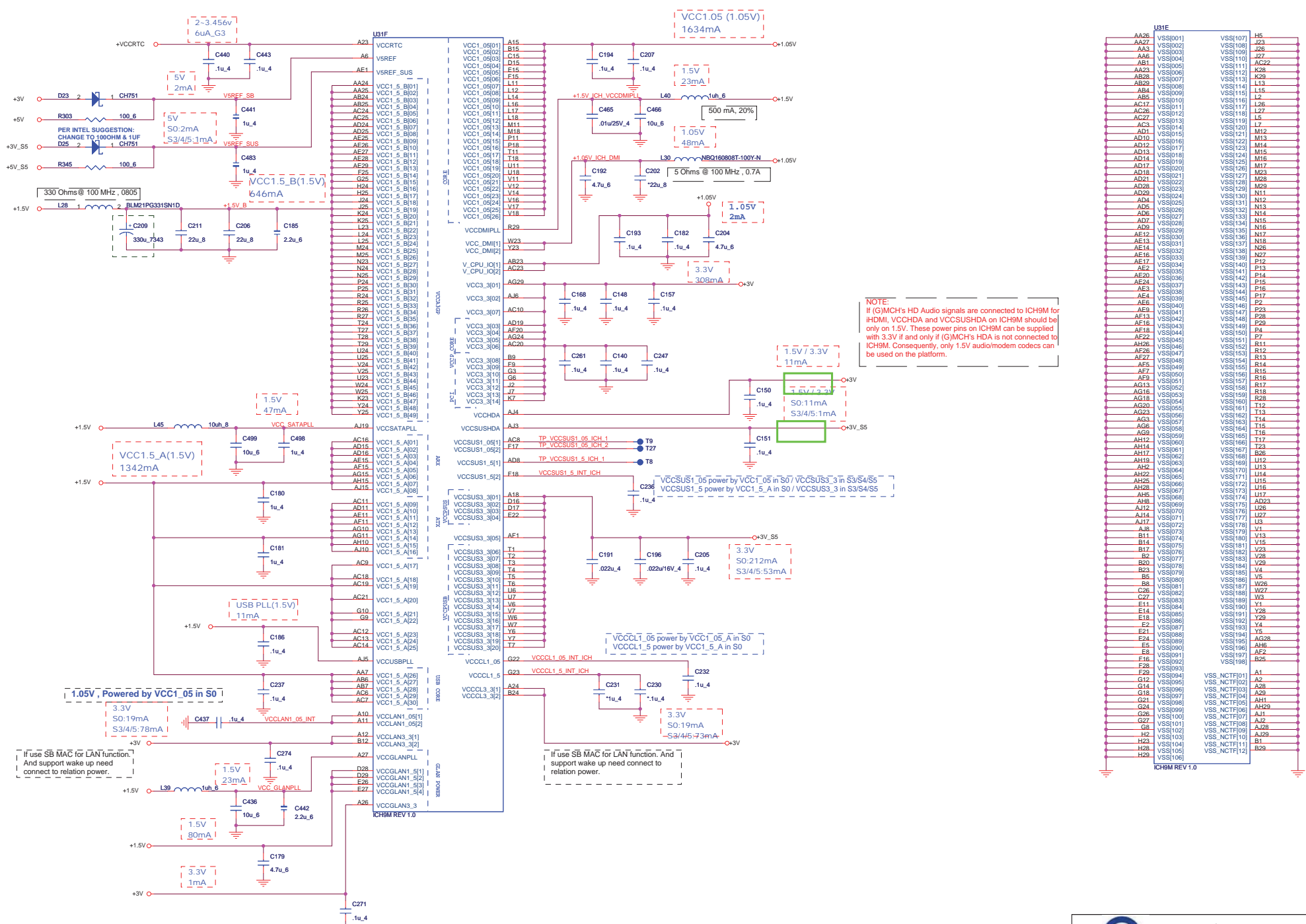
Board ID	ID2	ID1	ID0
default	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0

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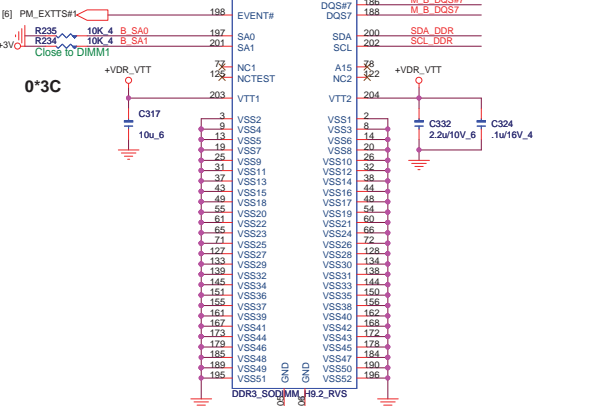
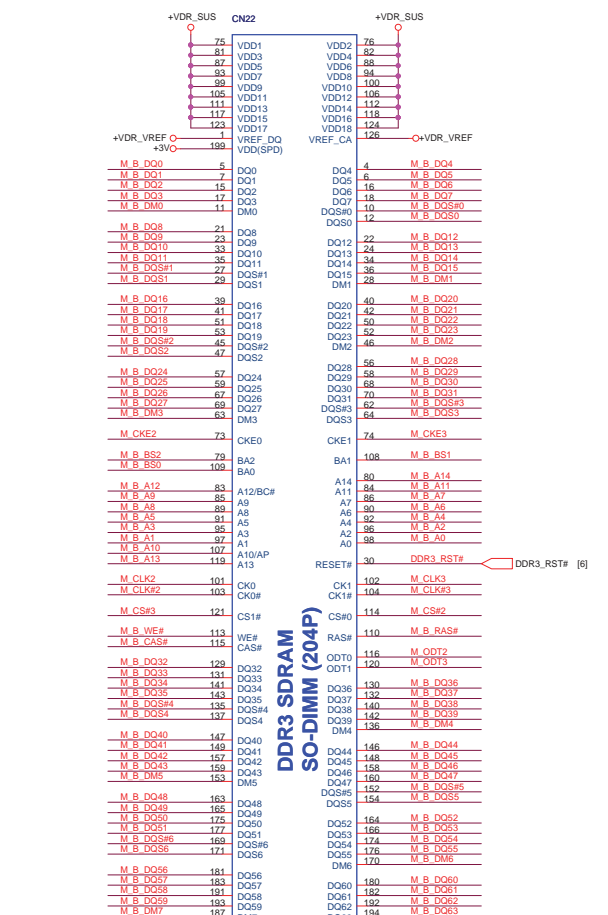
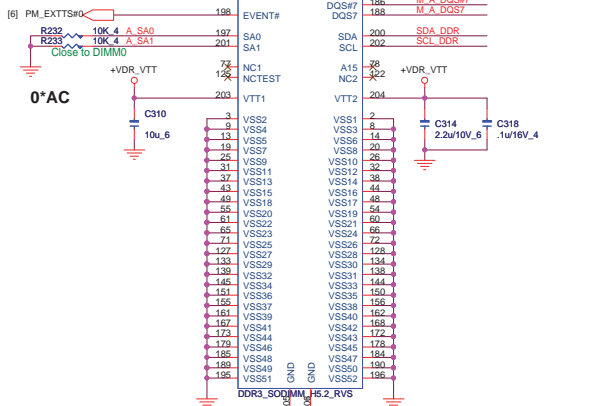
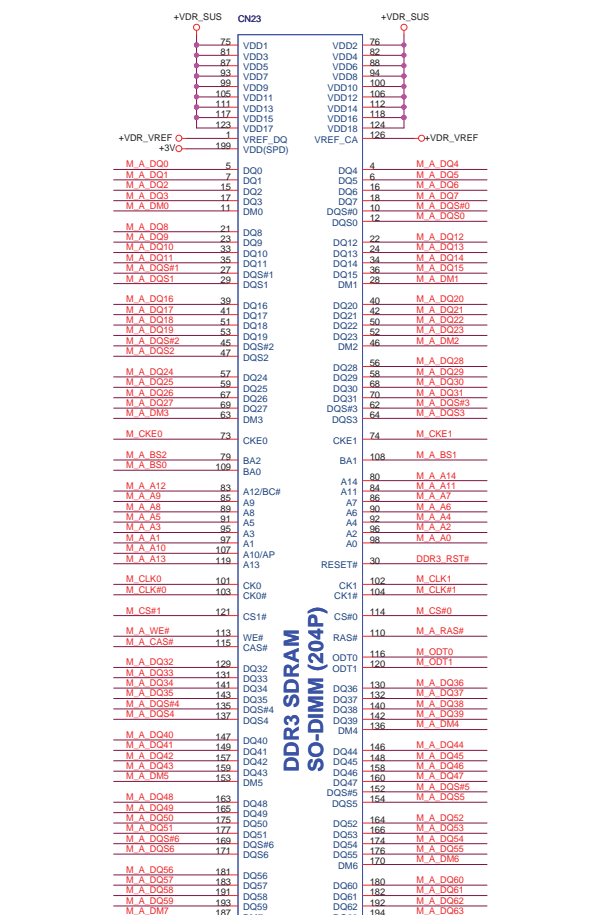
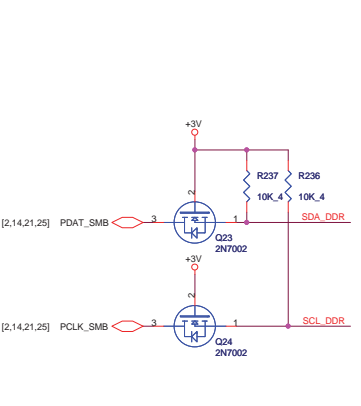
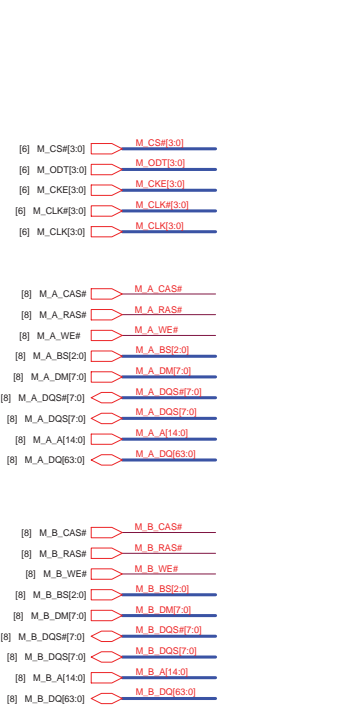
PROJECT : ZY8

Size: Document Number: ICH9M GPIO Rev: 3B

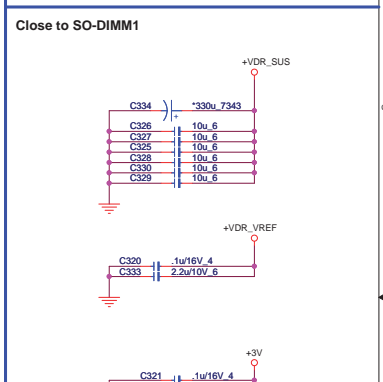
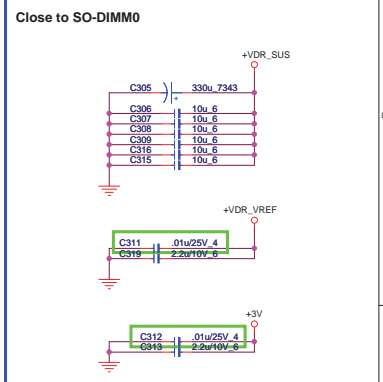
Date: Monday, January 05, 2009 Sheet: 14 of 39



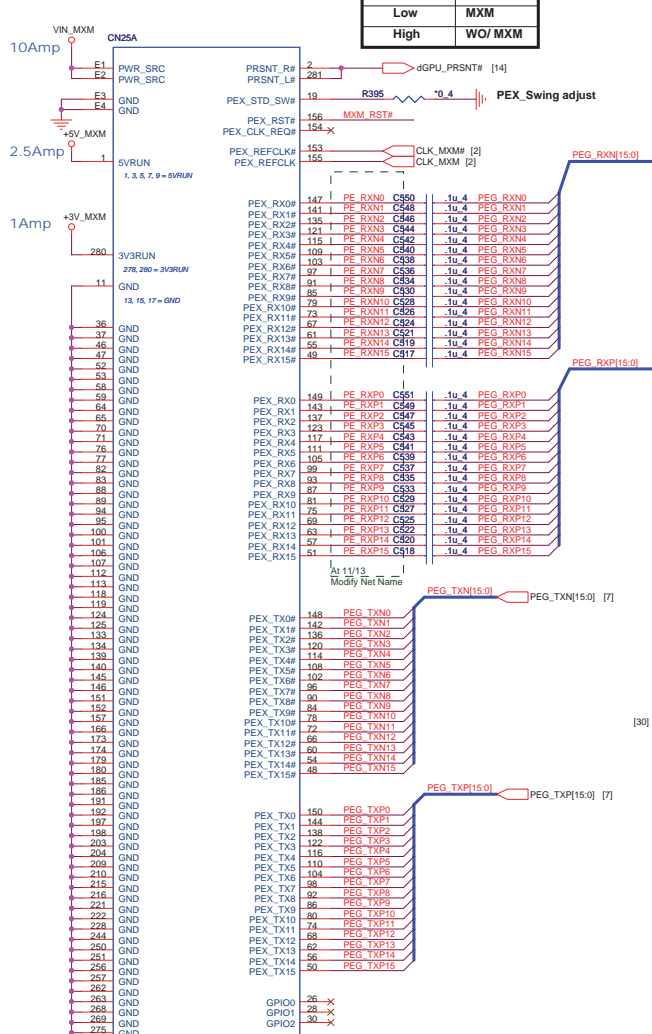
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Decoupling capacitor

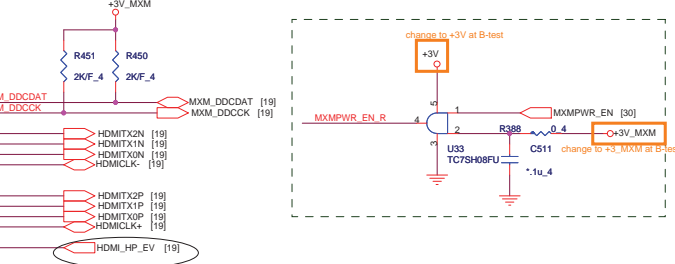
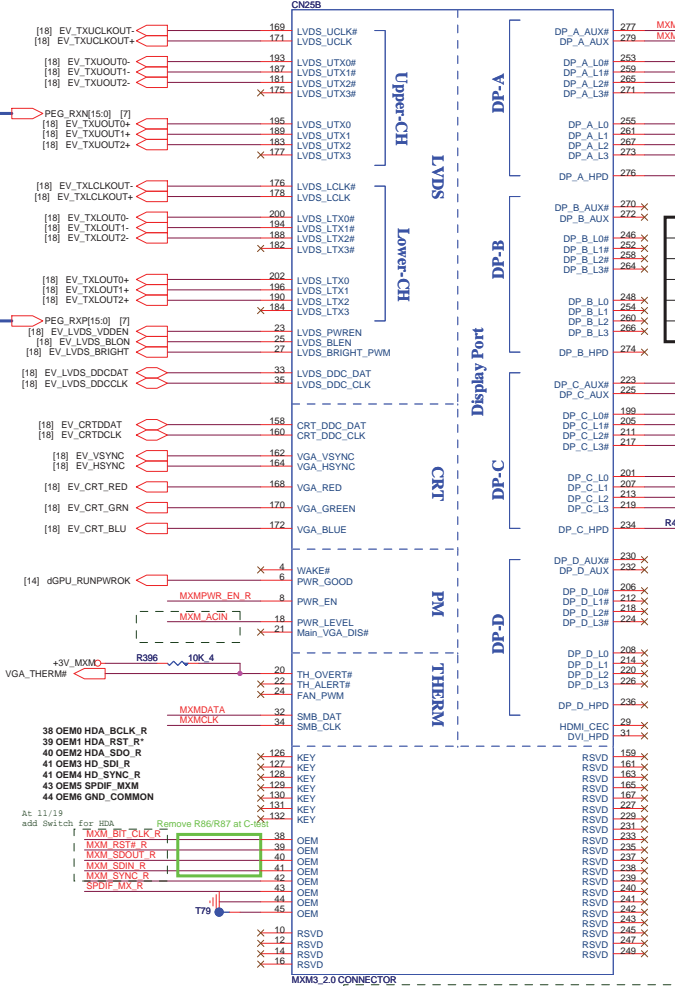


MXM Module

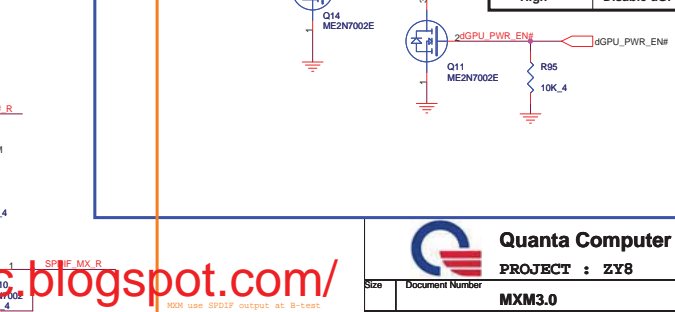
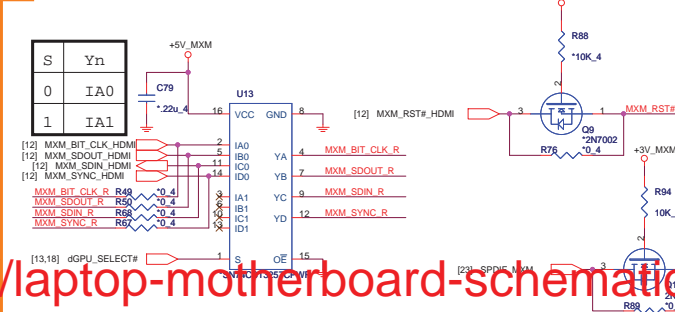
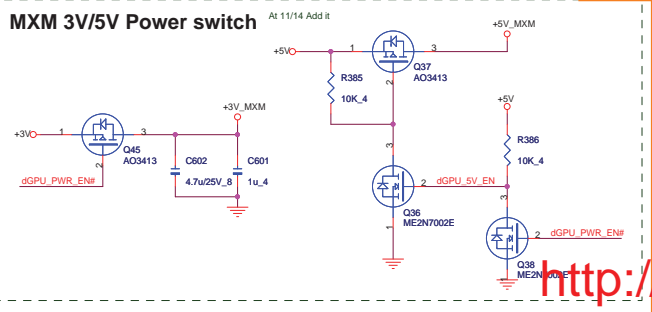
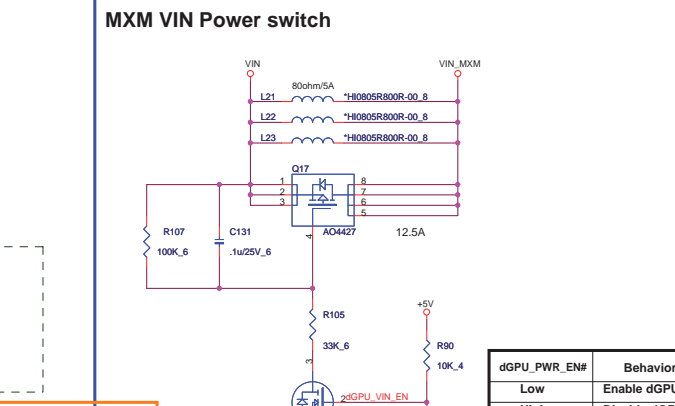
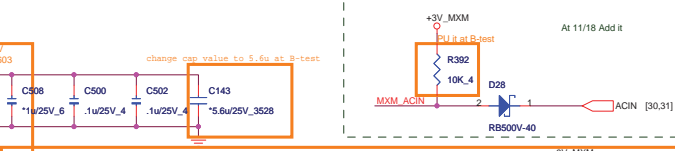
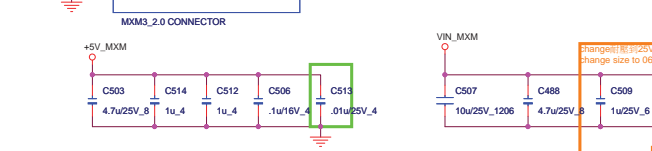
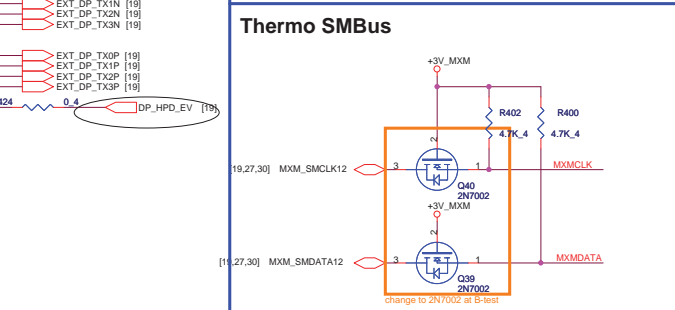
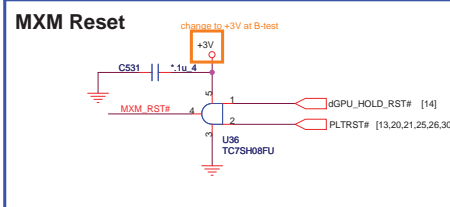


dGPU_PSRNT#	Sku
Low	MXM
High	WO/MXM

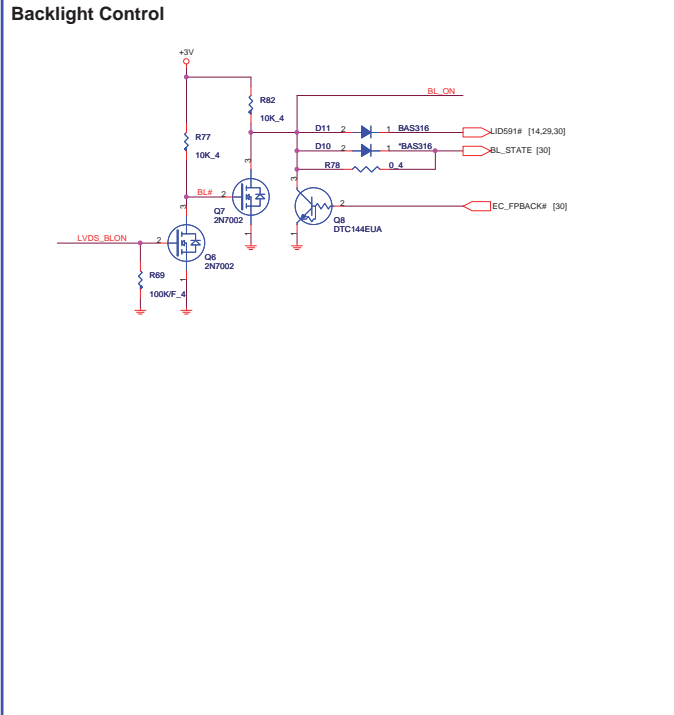
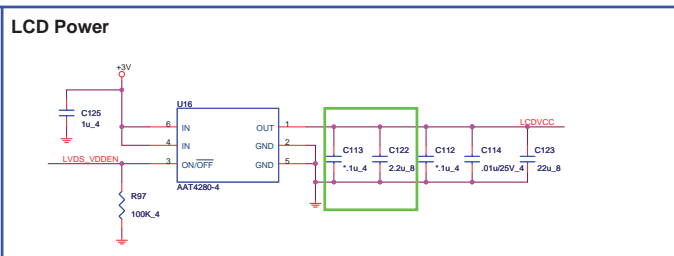
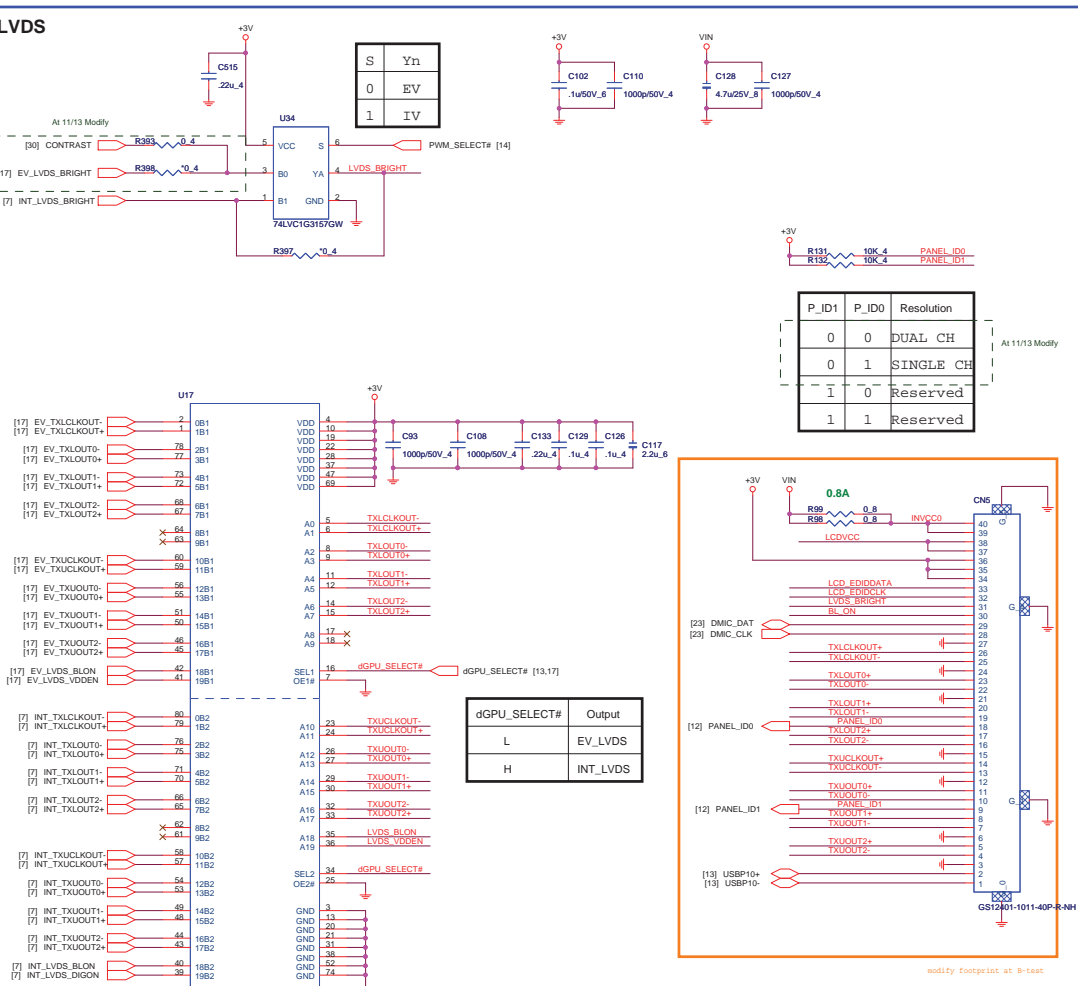
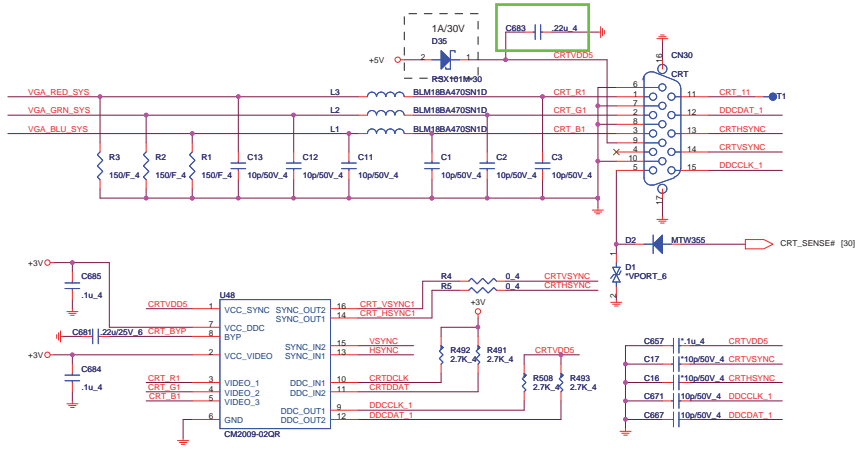
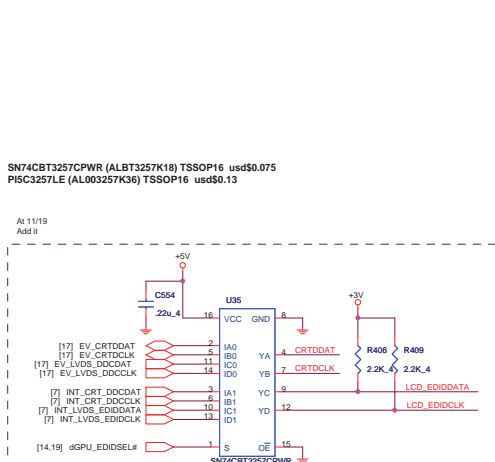
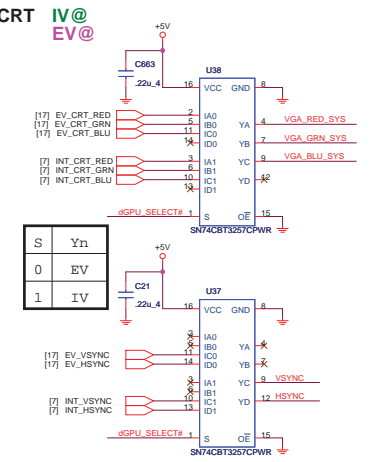
At 11/21
update MXM footprint to mm-mxm70-314-310b1-270p



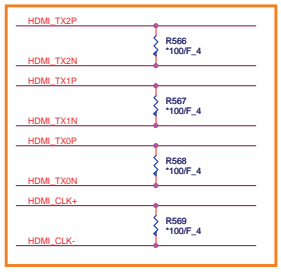
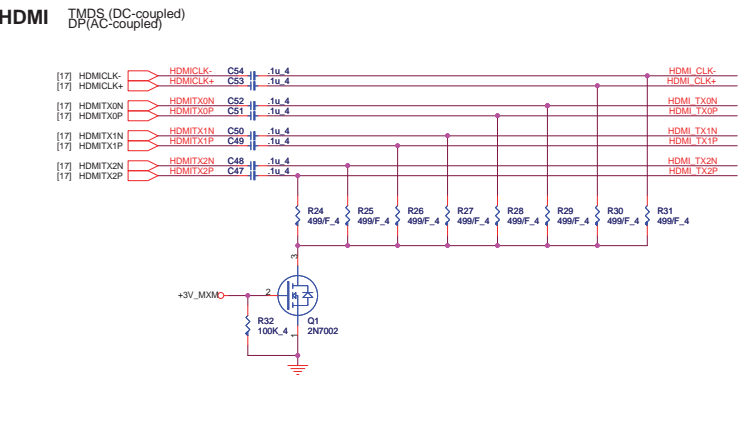
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A



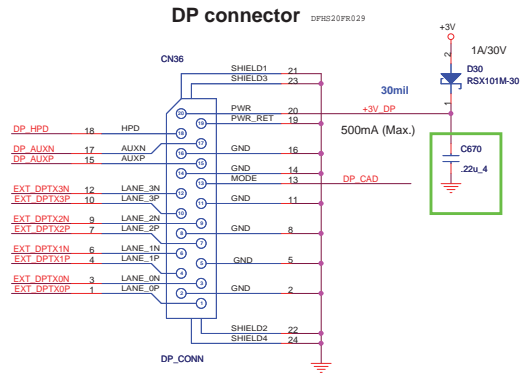
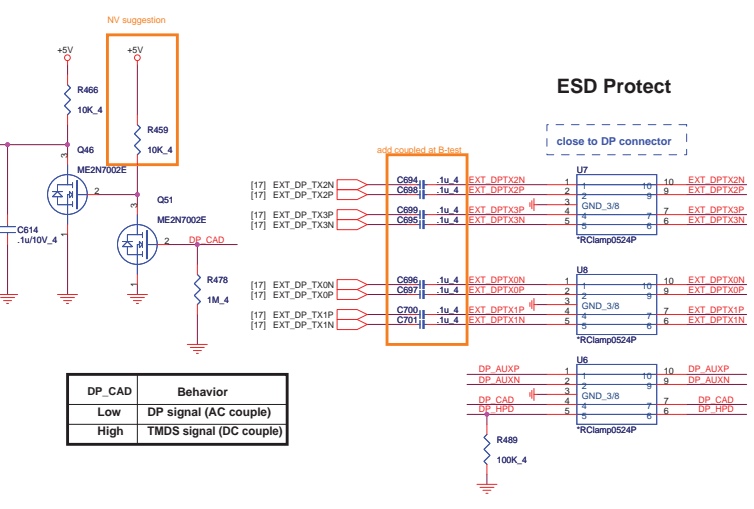
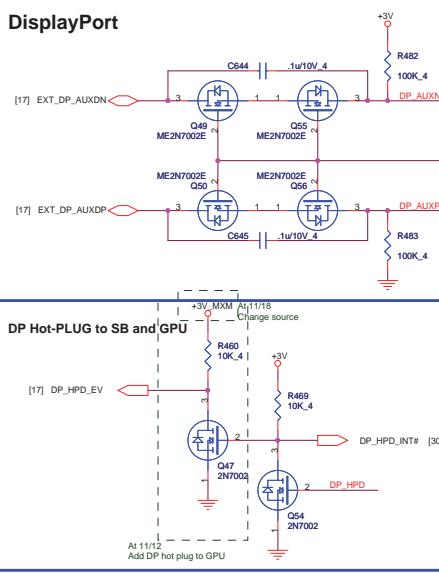
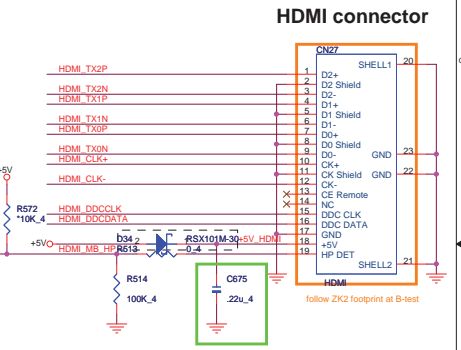
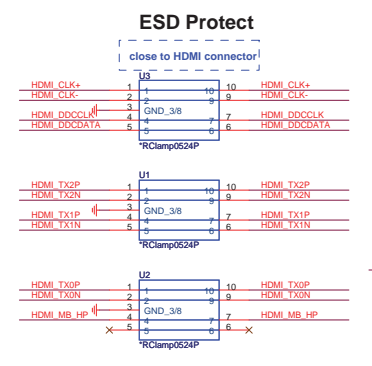
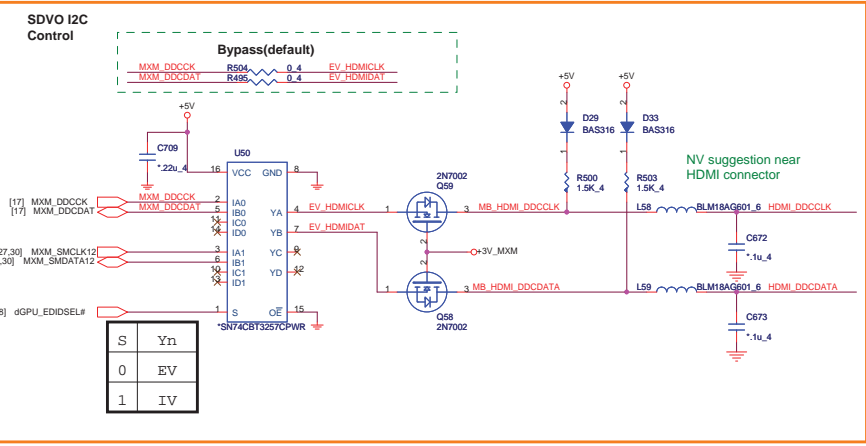
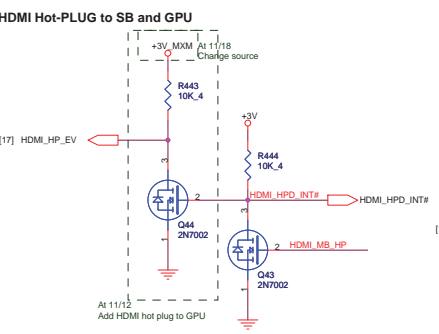
<http://laptop-motherboard-schematic.blogspot.com/>



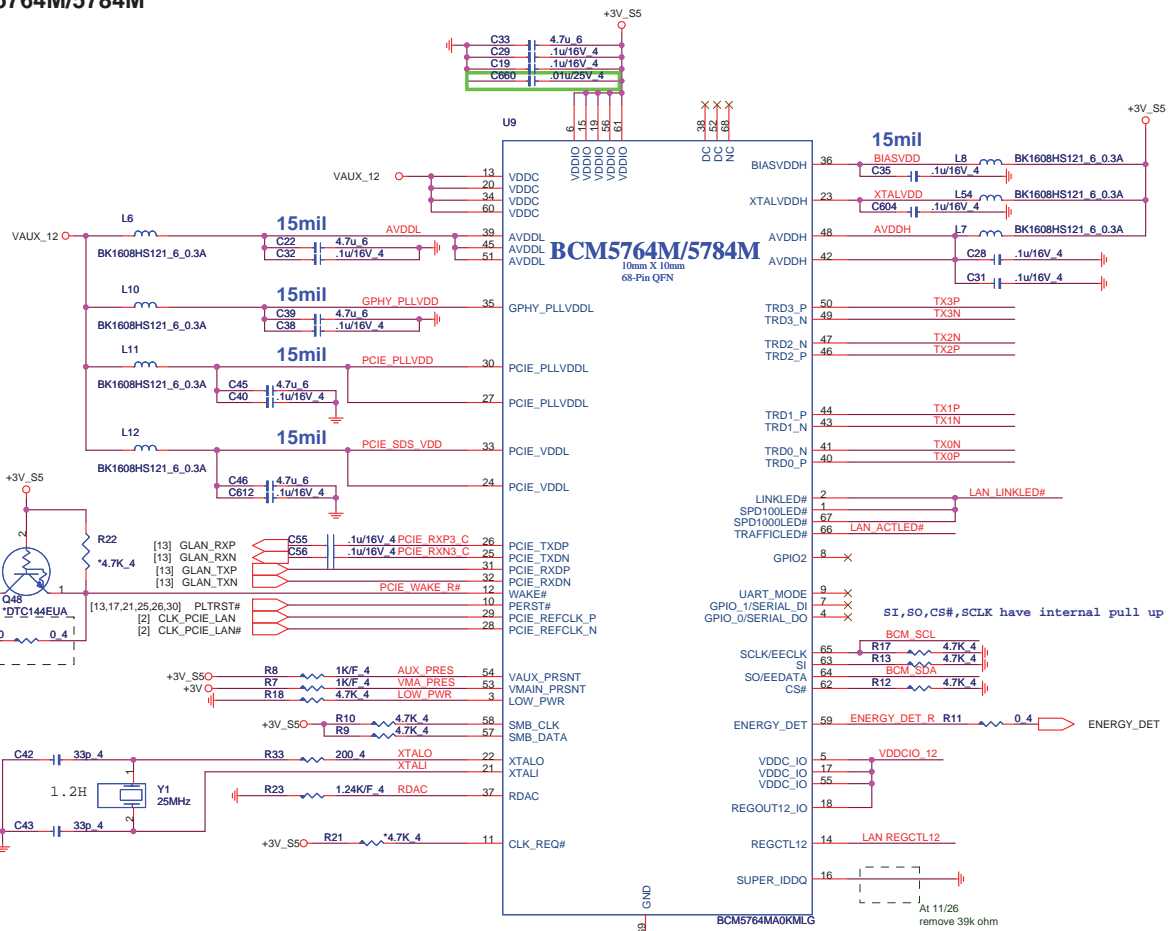
<http://laptop-motherboard-schematic.blogspot.com/>



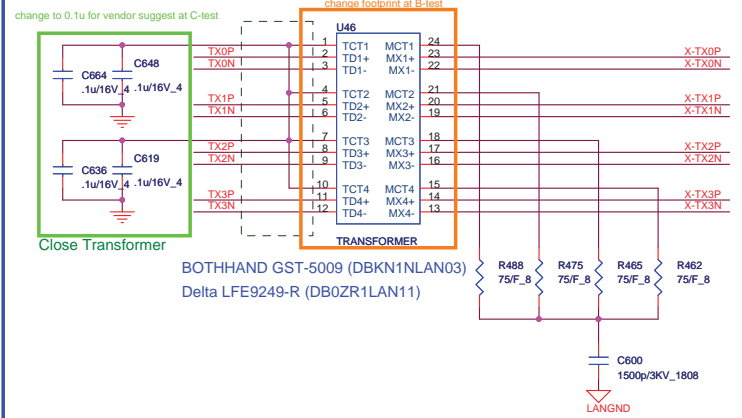
Close CN27



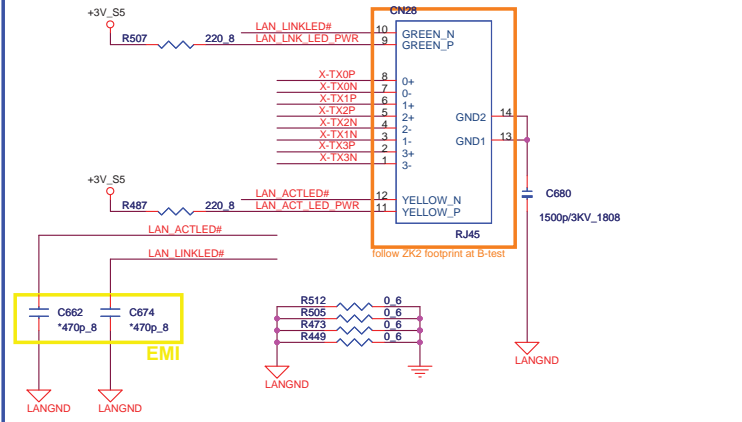
Giga-LAN BCM5764M/5784M



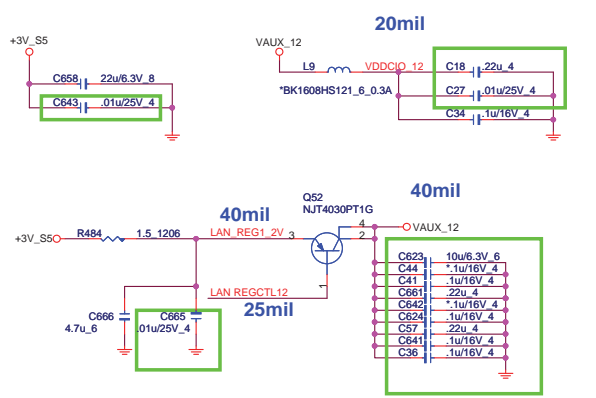
TRANSFORMER



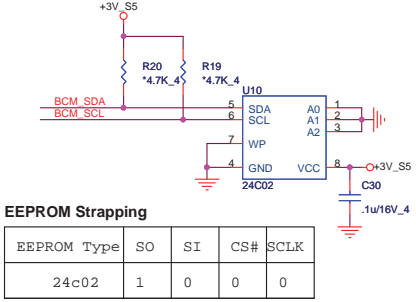
RJ45



LAN POWER




EEPROM



EEPROM Strapping

EEPROM Type	SO	SI	CS#	SCLK
24c02	1	0	0	0

<http://laptop-motherboard-schematic.blogspot.com/>



Quanta Computer Inc.
PROJECT : ZY8

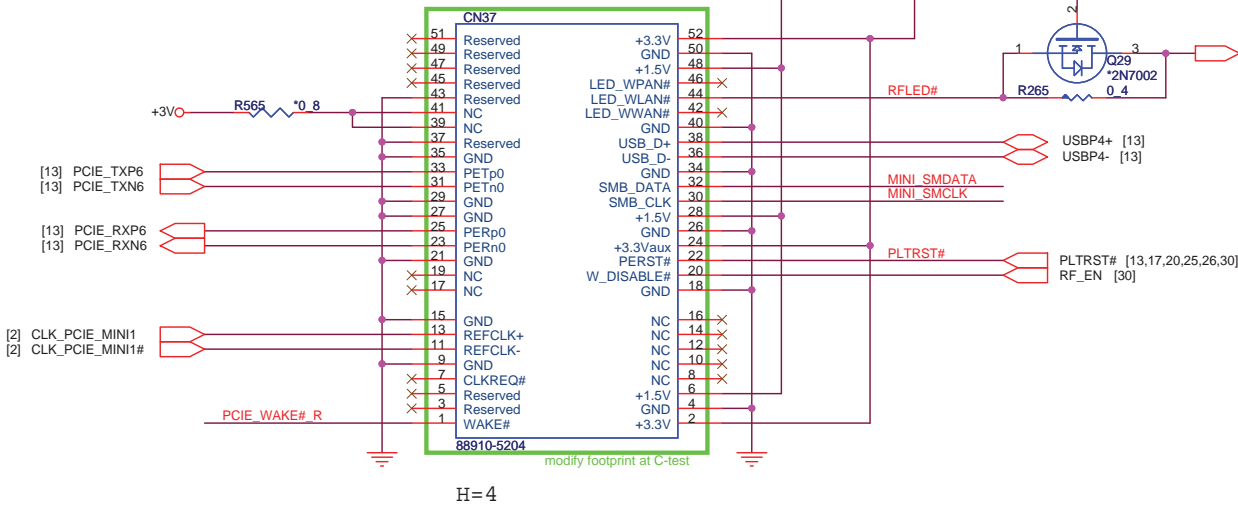
Size	Document Number				Rev 3B
LAN (BCM5764M/5784M)					
Date:	Friday, February 13, 2009	Sheet	20	of	39

Wireless

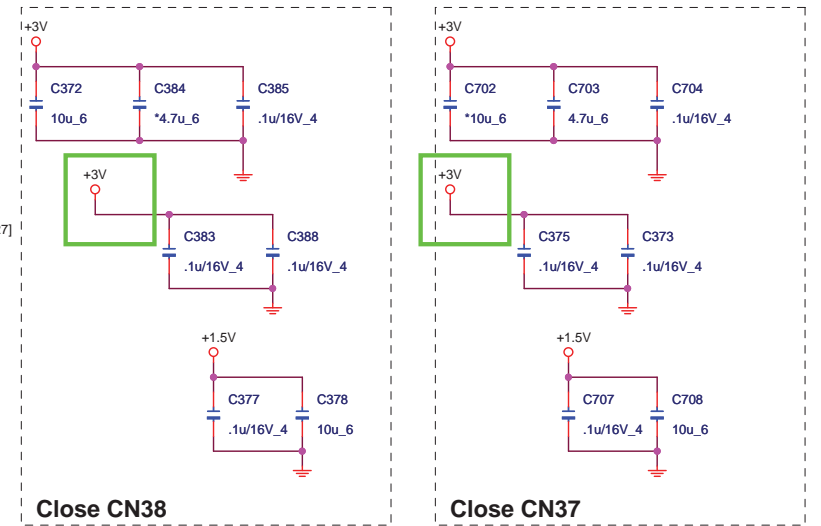
+3.3V: 1000mA
 +3.3Vaux: 330mA
 +1.5V: 500mA

Modify to 2Conn. at B-test

Fotprint : MINIPCI-AAA-PCL-099-P01-52P-LDV



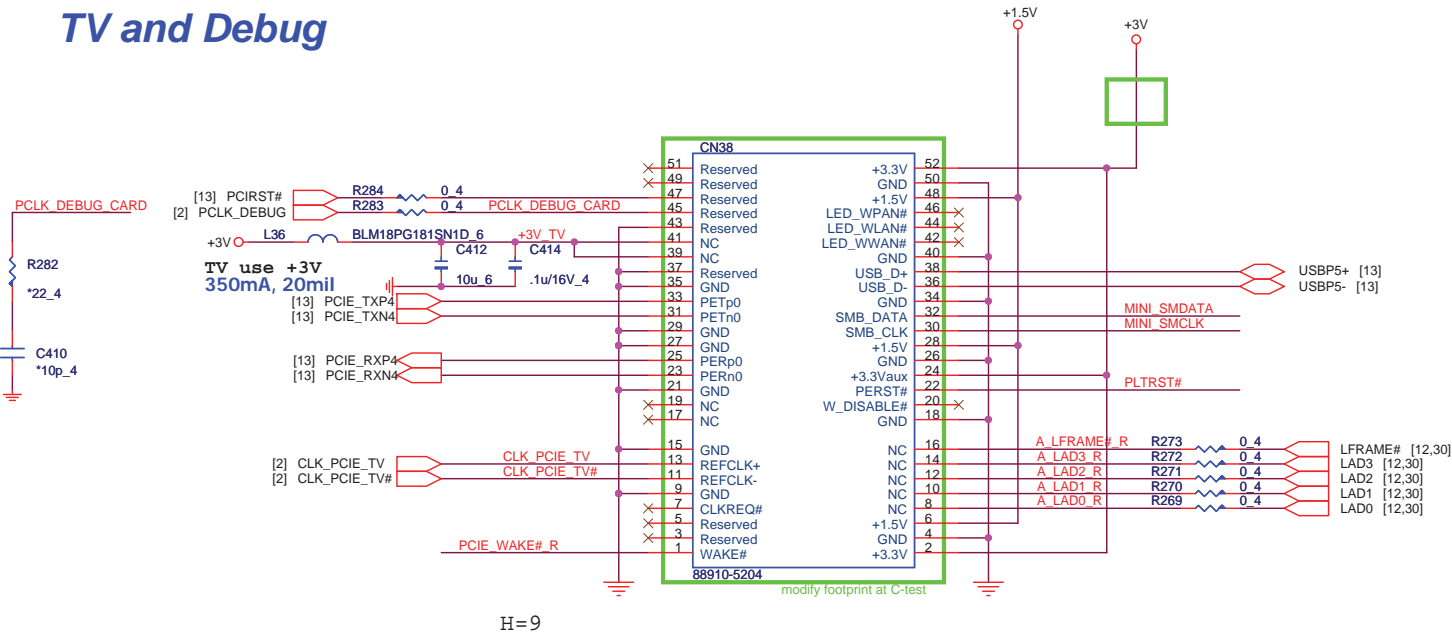
H=4



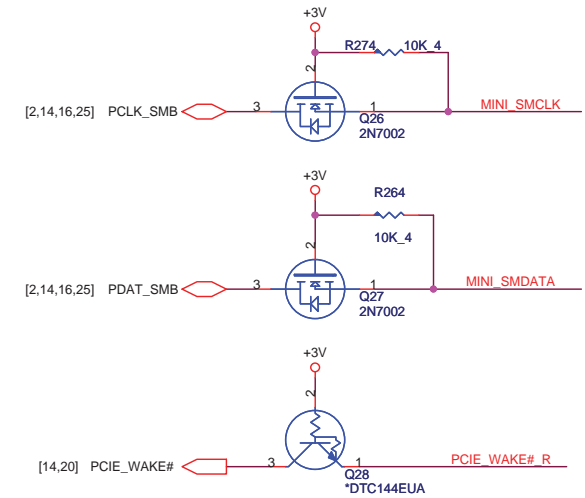
Close CN38

Close CN37

TV and Debug



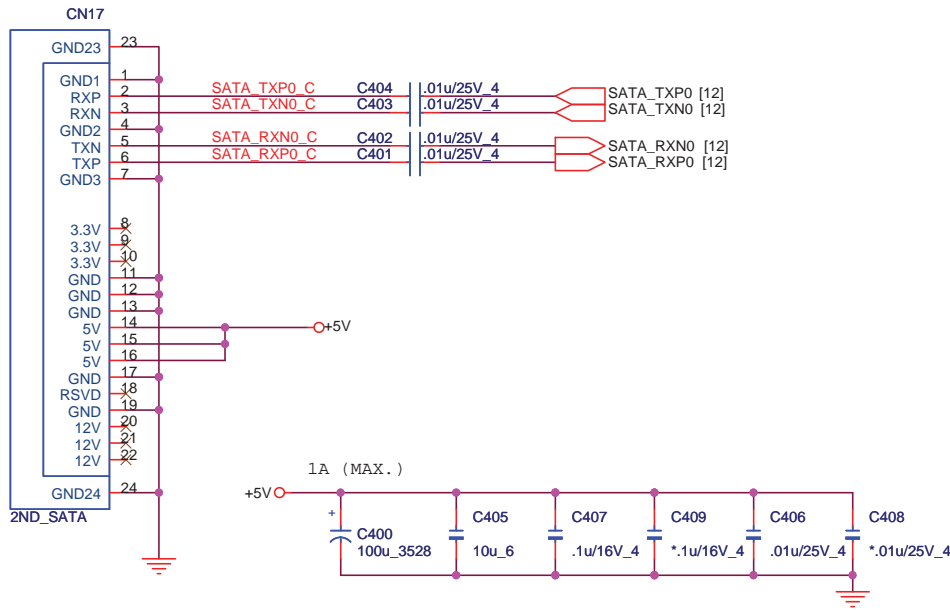
H=9



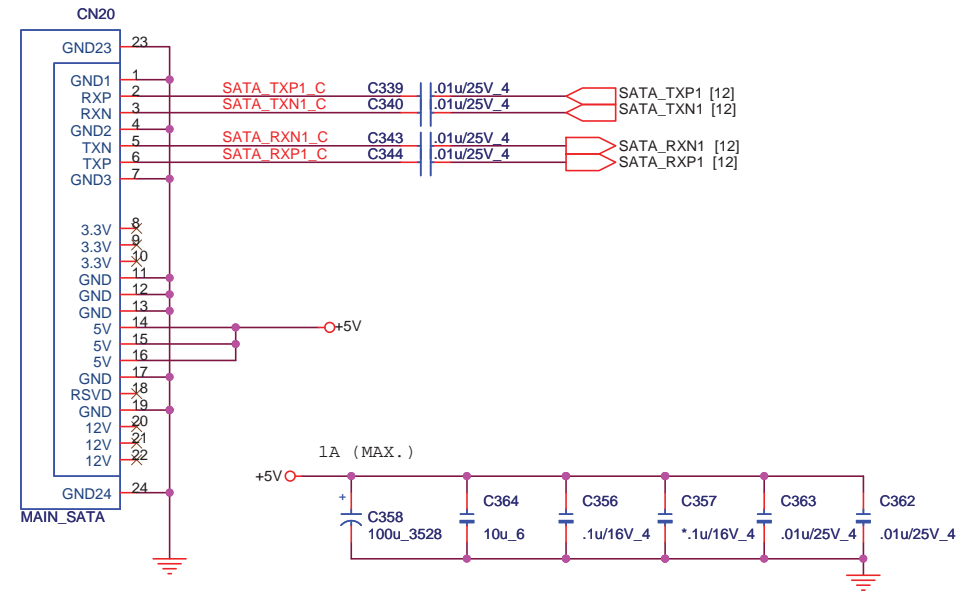
Quanta Computer Inc.
 PROJECT : ZY8

Size	Document Number	Rev
	MINI PCI-E card/TV	3B
Date:	Friday, February 13, 2009	Sheet 21 of 39

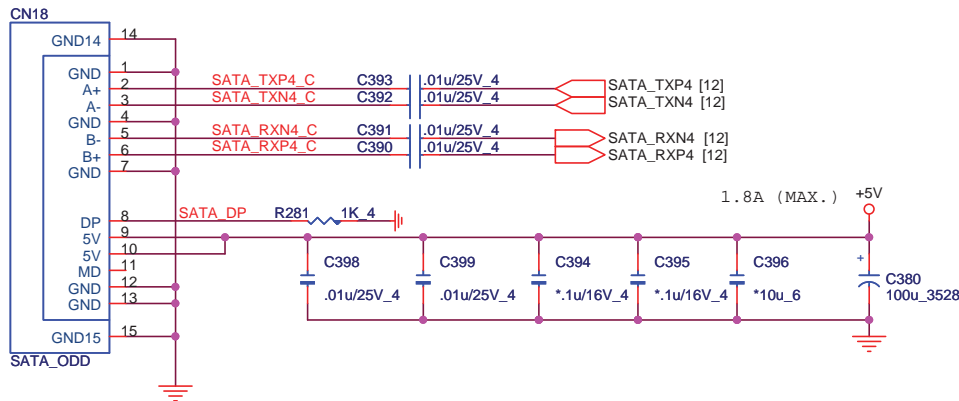
2nd SATA HDD (edge of board)



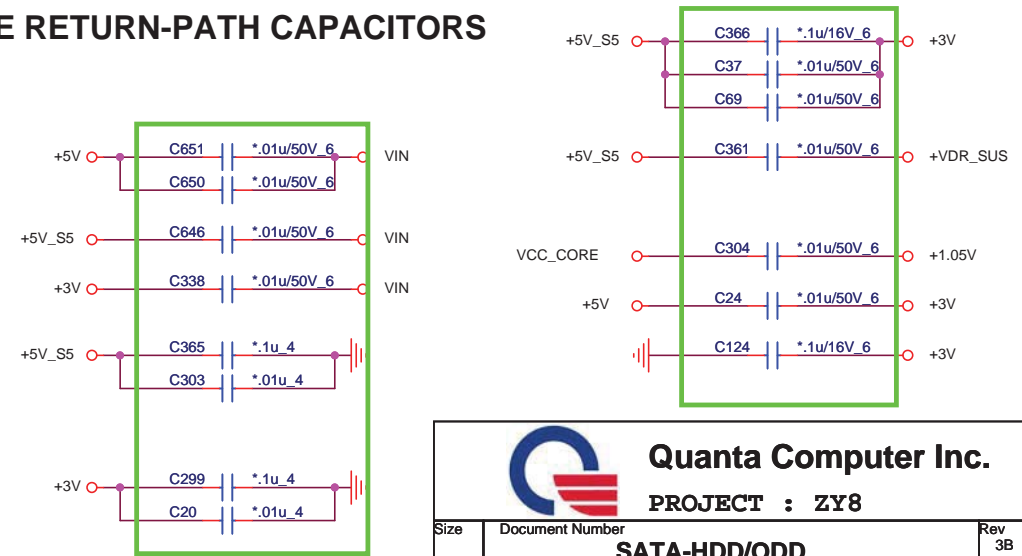
MAIN SATA HDD



ODD (SATA)



EE RETURN-PATH CAPACITORS

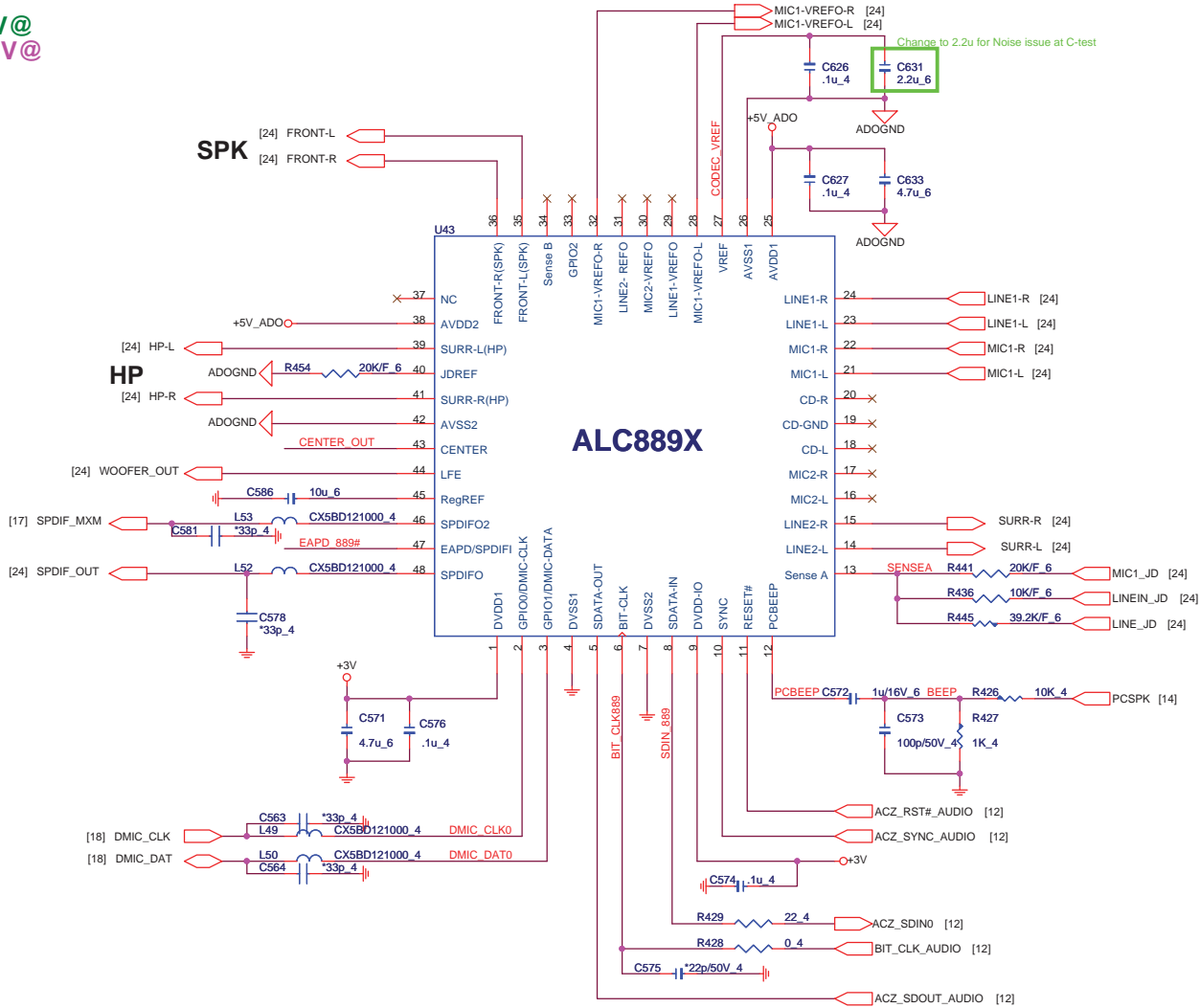


Quanta Computer Inc.
PROJECT : ZY8

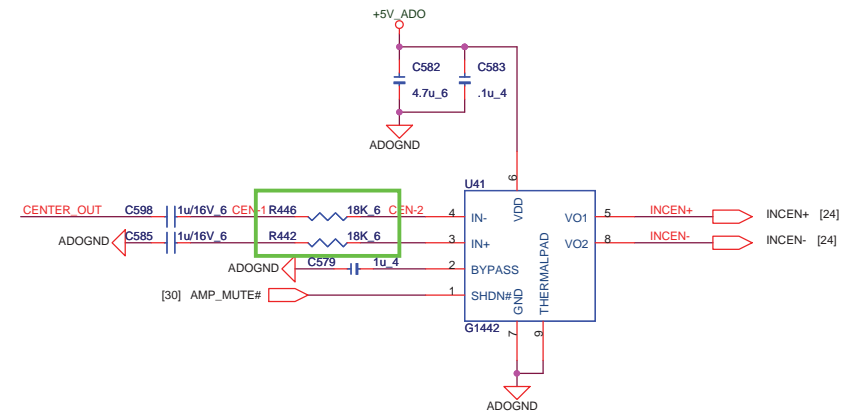
Size	Document Number	Rev
	SATA-HDD/ODD	3B
Date:	Friday, February 13, 2009	Sheet 22 of 39

CODEC(ALC889X)

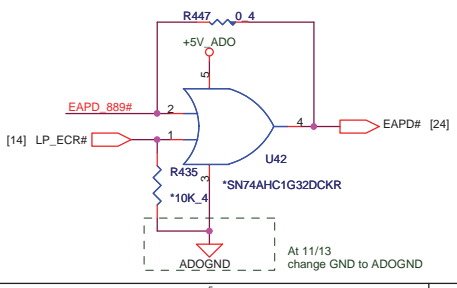
IV@
EV@



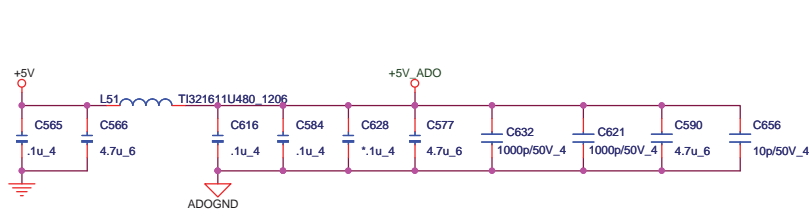
CENTER MONO




EAPD pin



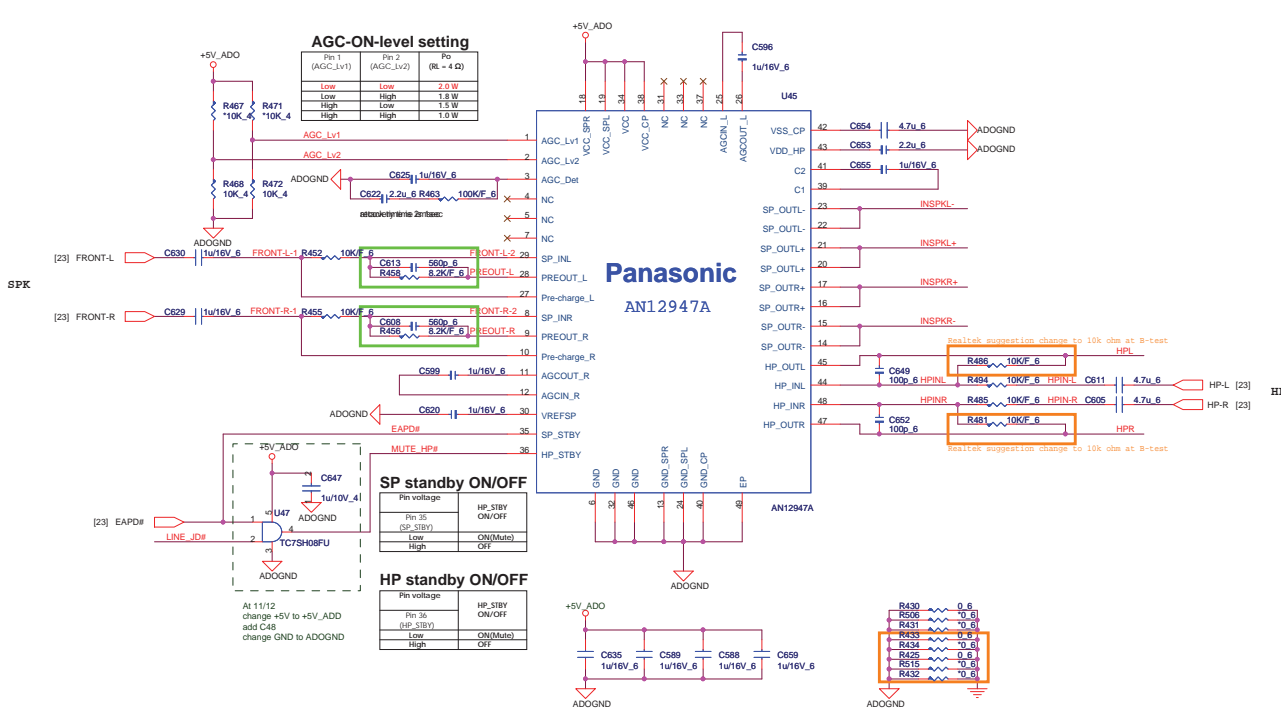
CODEC/AMP Power



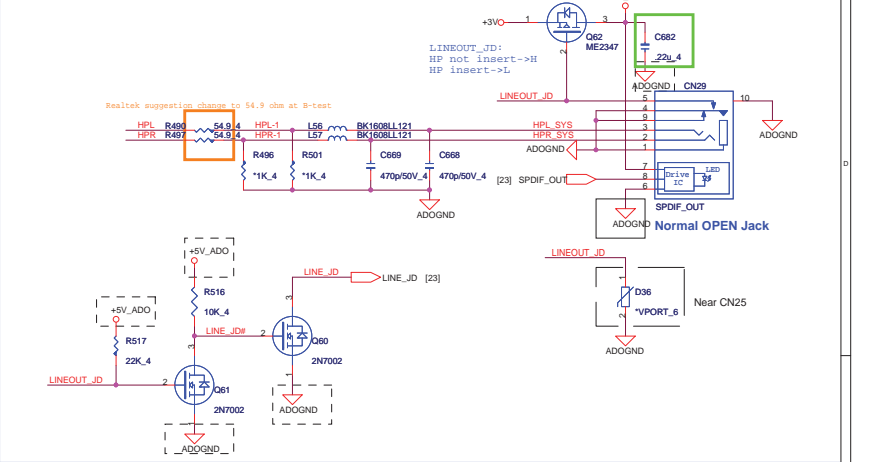
<http://laptop-motherboard-schematic.blogspot.com/>

 Quanta Computer Inc. PROJECT : ZY8		
Size	Document Number	Rev
		3B
REALTEK ALC889X/MONO-AMP		
Date:	Tuesday, February 17, 2009	Sheet 23 of 39

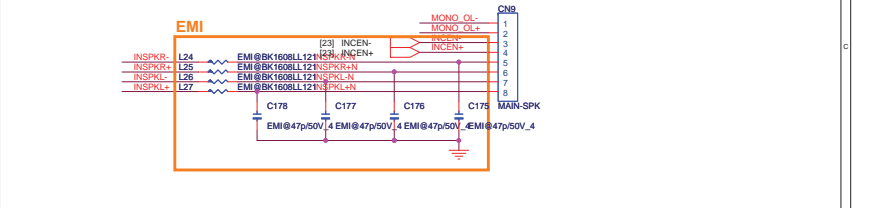
SPEAKER/HP AMP.



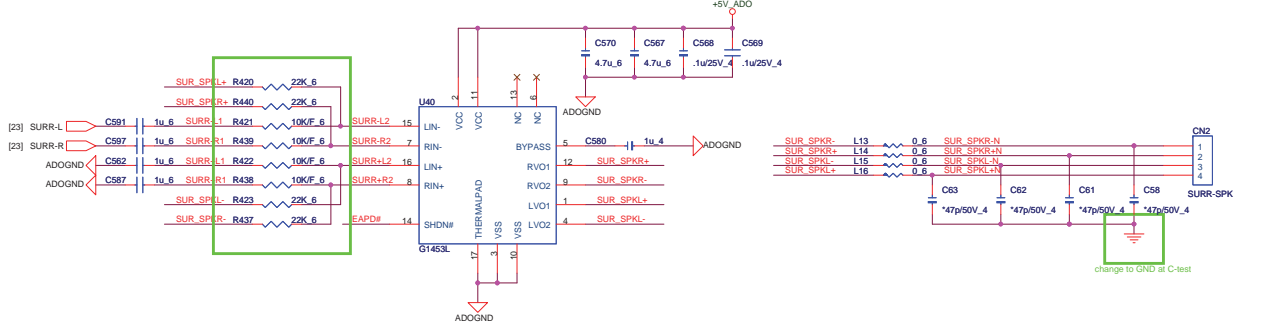
LINE-OUT/SPDIFO



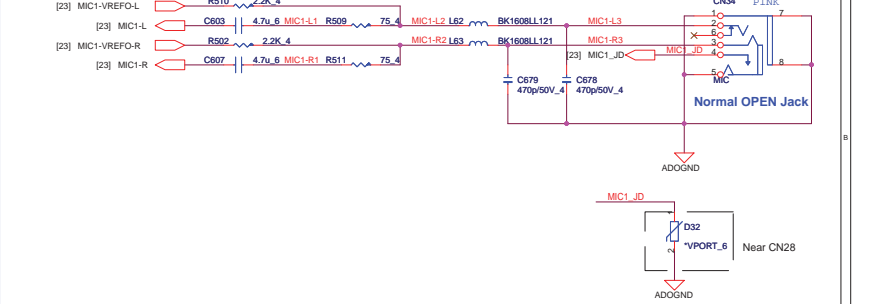
Main SPK/Center/Subwoofer



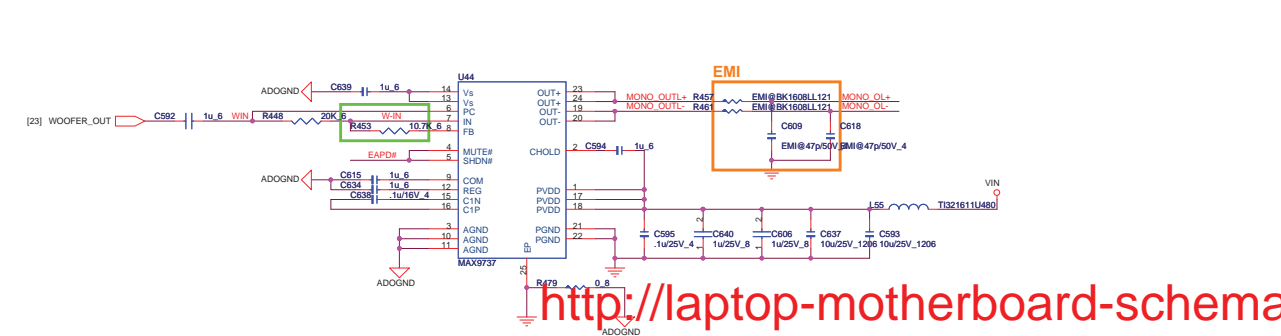
SURR-SPK



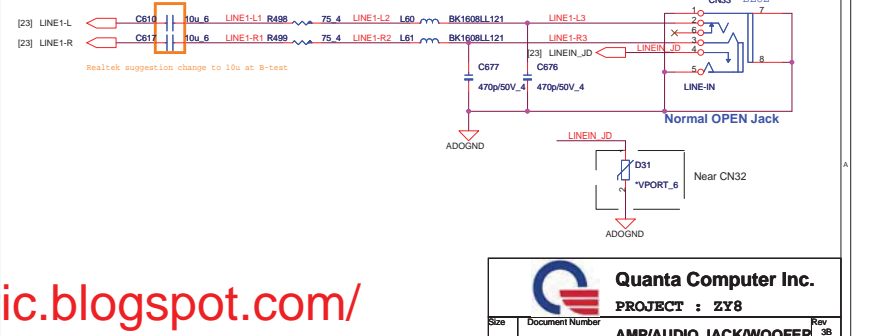
MIC



SUBWOOFER

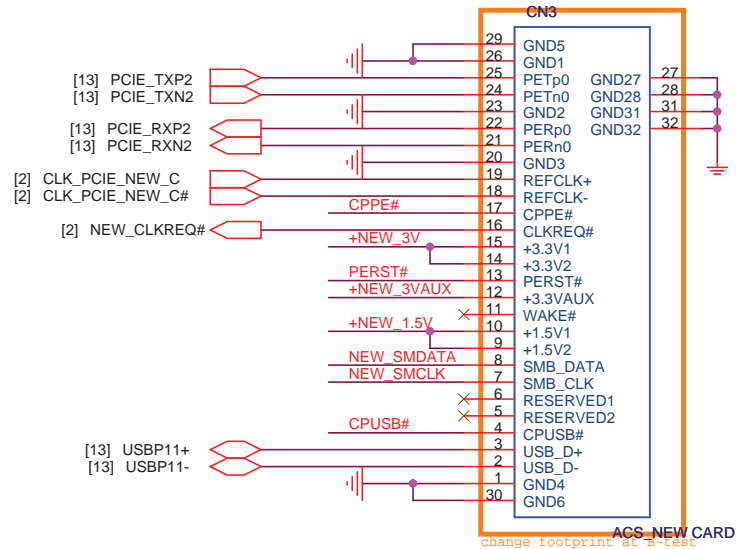


LINE IN



<http://laptop-motherboard-schematic.blogspot.com/>

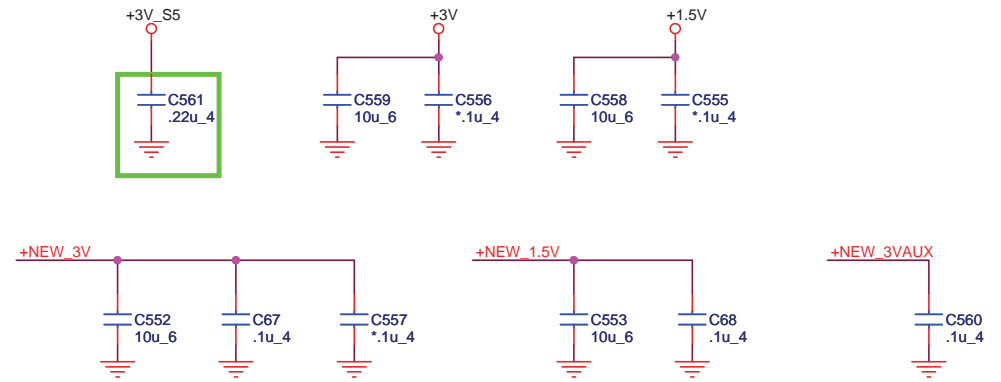
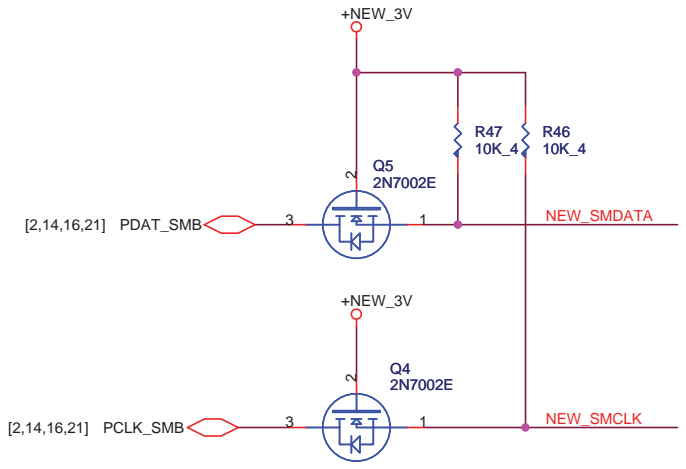
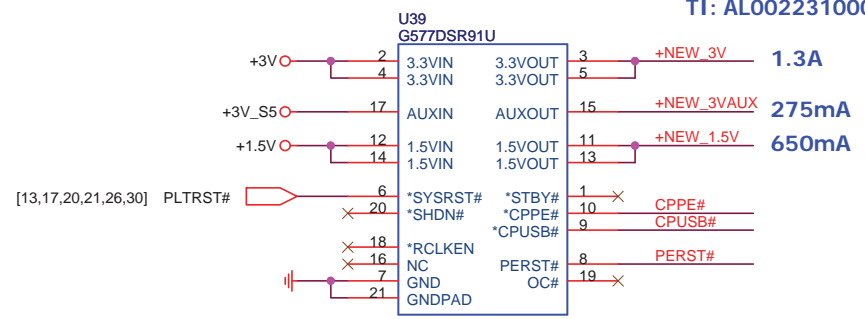
NEW CARD



At 11/18
Change GMT cost down version.

NEW CARD'S POWER SWITCH

GMT: AL000577002
TI: AL002231000

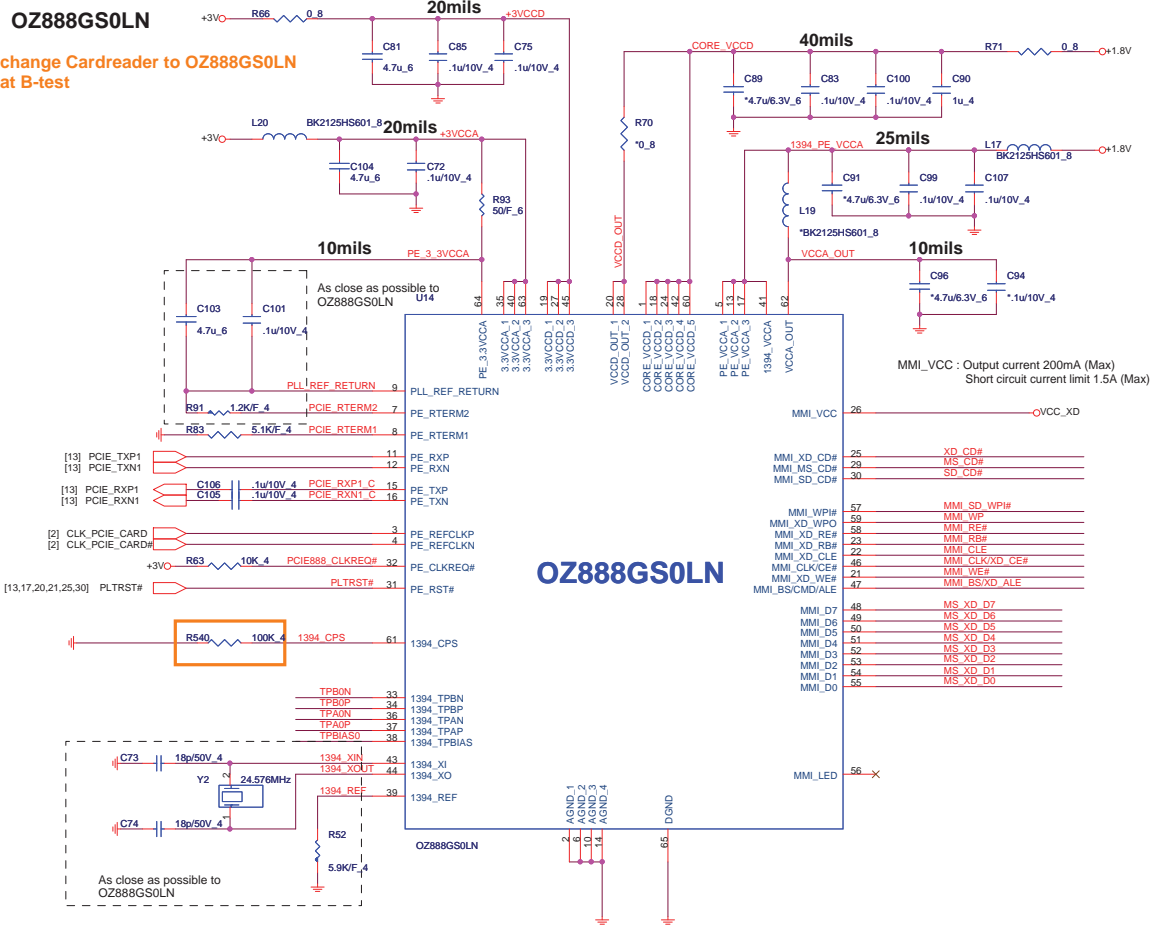


Quanta Computer Inc.
PROJECT : ZY8

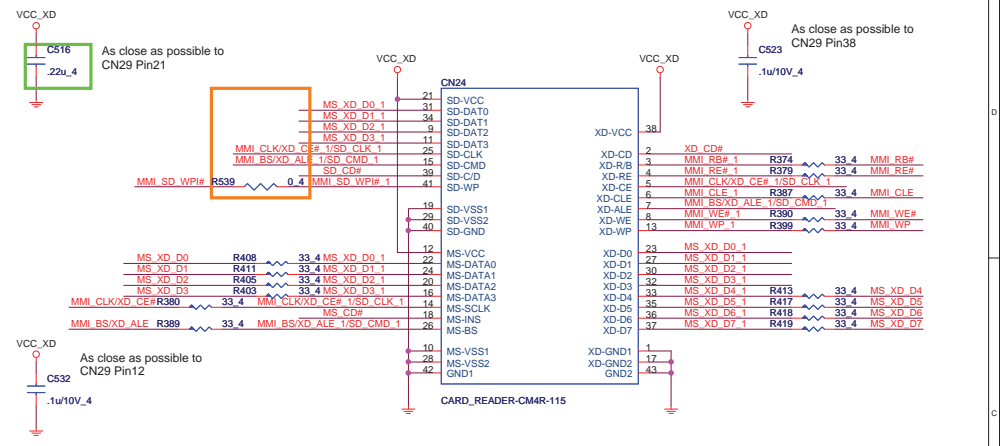
Size	Document Number	Rev
	NEW CARD	3B
Date:	Friday, February 13, 2009	Sheet 25 of 39

OZ888GS0LN

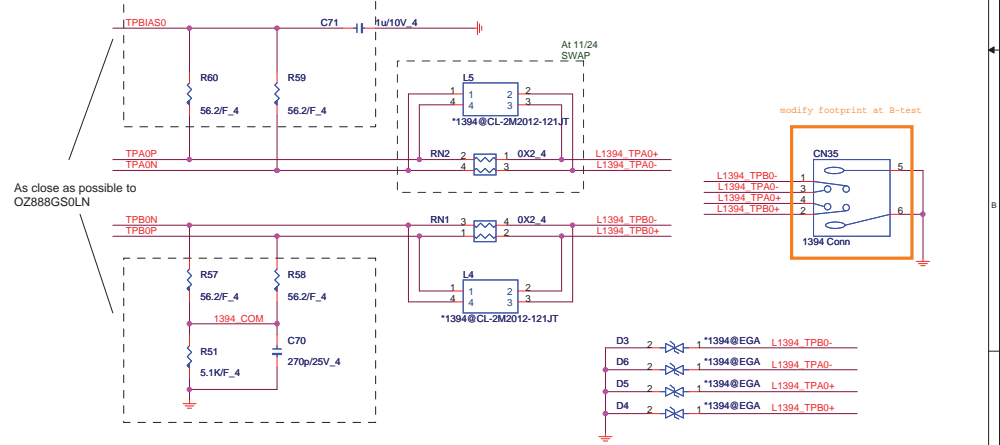
change Cardreader to OZ888GS0LN at B-test



5 IN 1 CARD READER



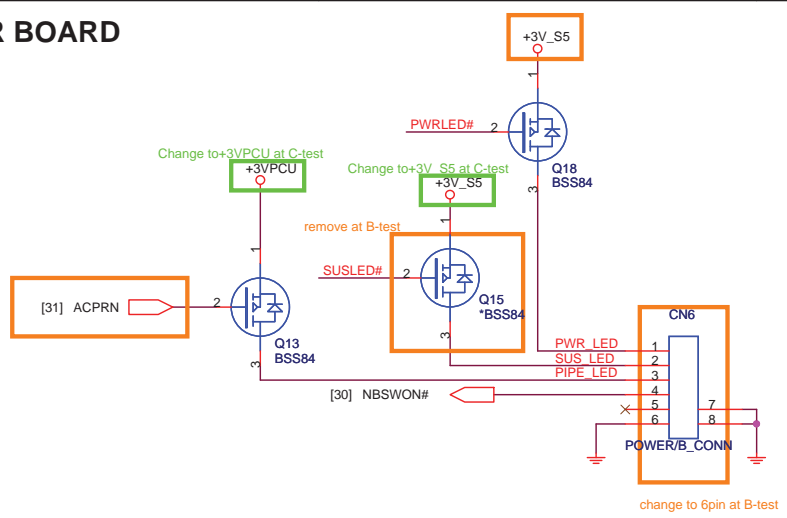
1394



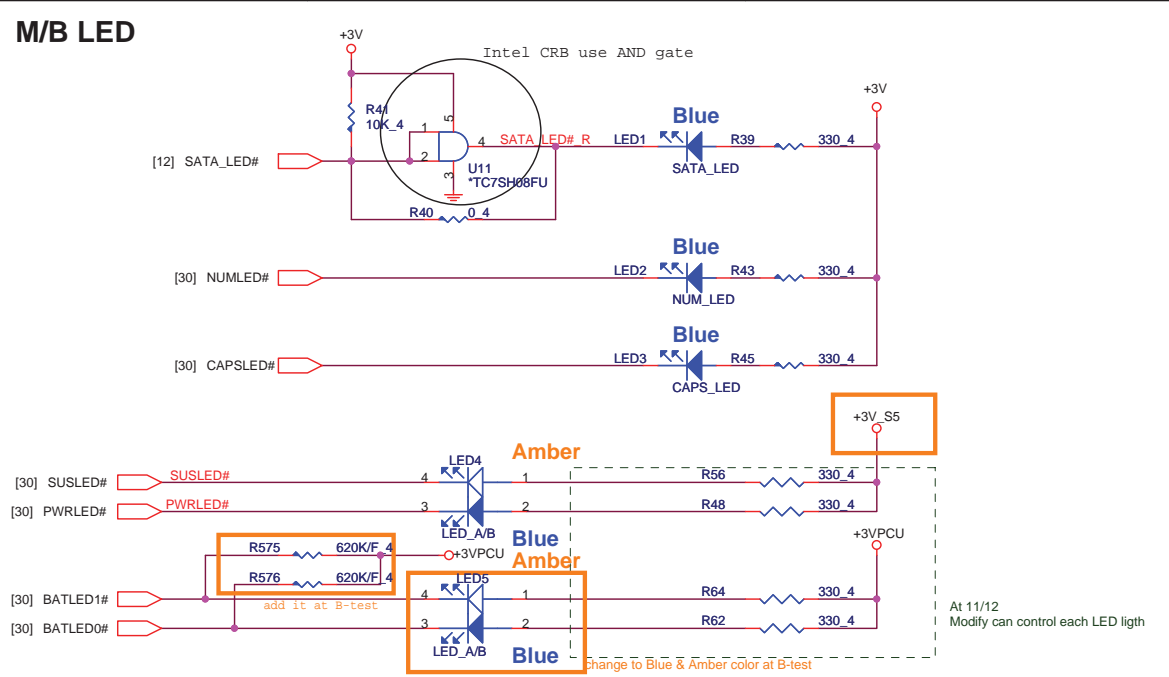
Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	OZ888GS0L1N	Rev	3B
Date:	Friday, February 13, 2009	Sheet	28	of 39

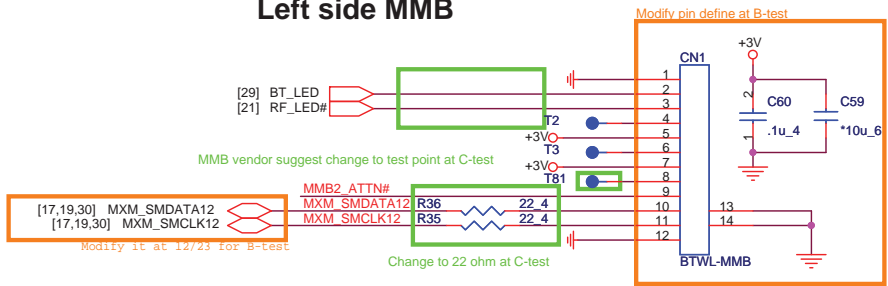
POWER BOARD



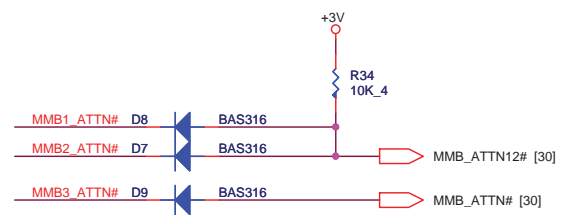
M/B LED



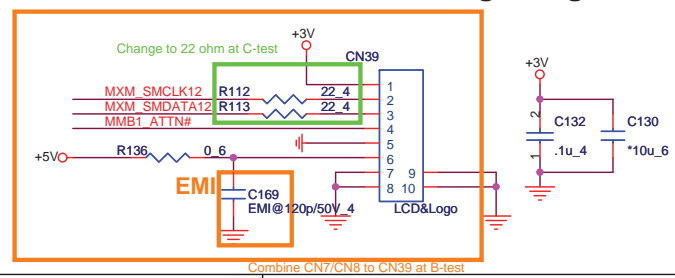
Left side MMB



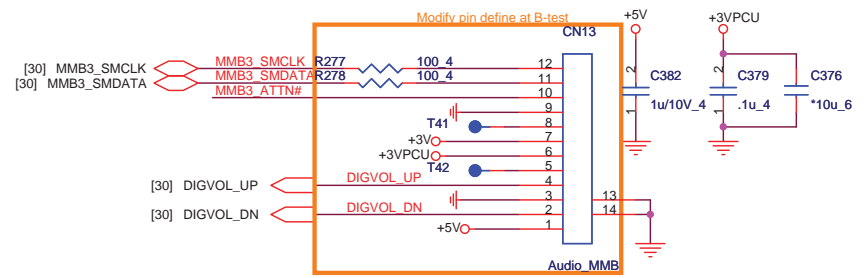
MMB Status



LCD BL_ON/OFF MMB & Backlight Logo LED



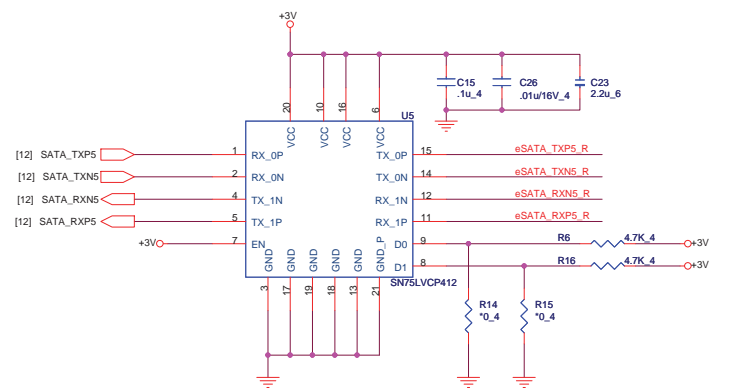
Right Side MMB



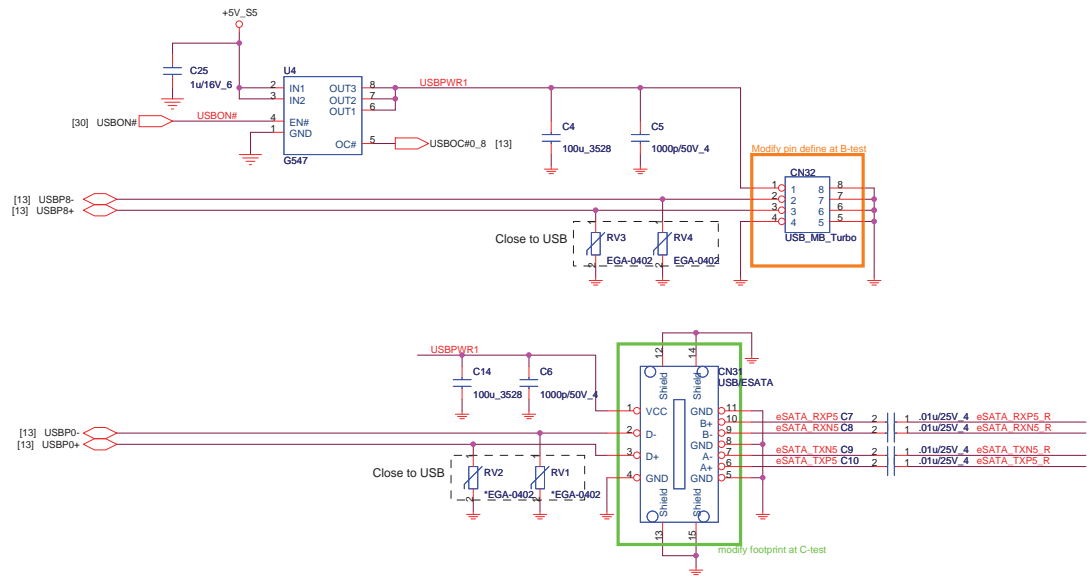
Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
		3B
POWER/MMB/LAUNCH/LED		
Date:	Friday, February 13, 2009	Sheet 27 of 39

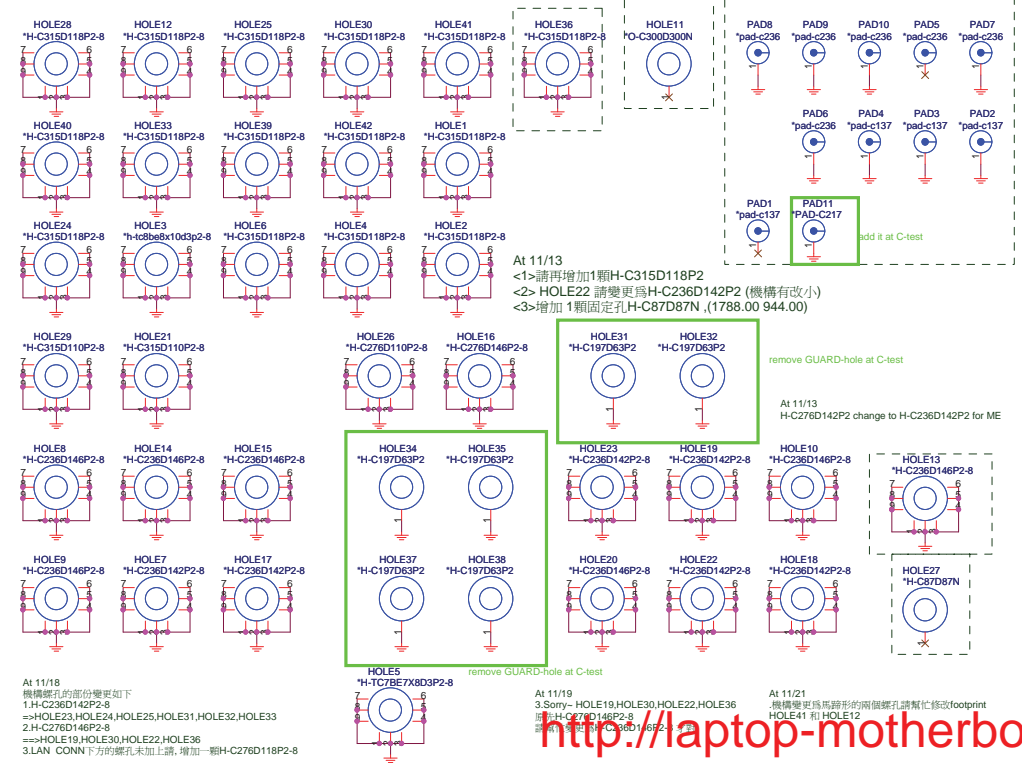
USB & eSATA



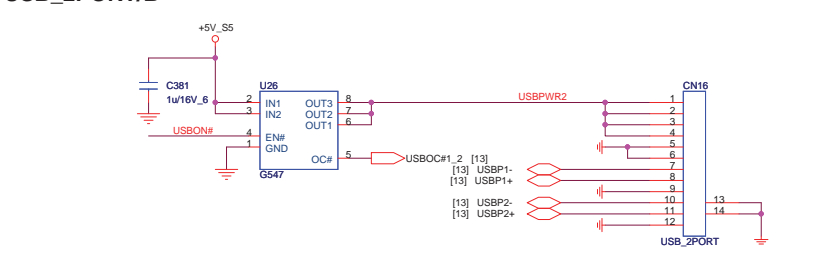
EN	DO	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)



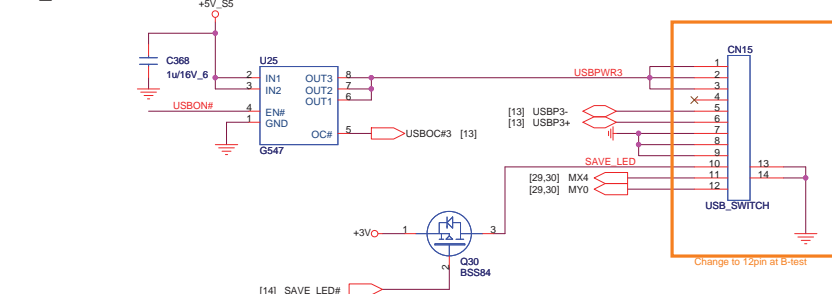
HOLES



USB_2PORT/B



USB_SWITCH/B



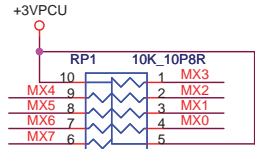
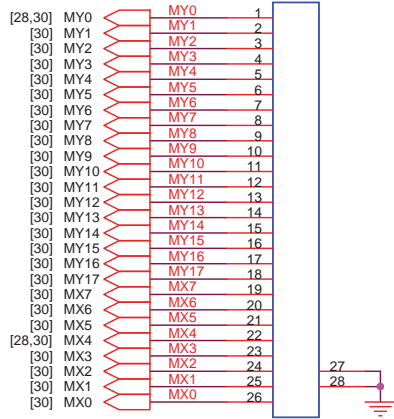
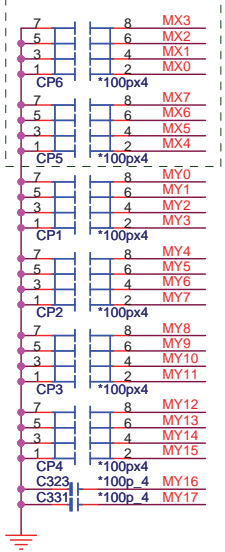
Quanta Computer Inc.
PROJECT : ZY8
USB/eSATA

Document Number: []
Rev: 38

Date: Friday, February 13, 2009
Sheet: 26 of 38

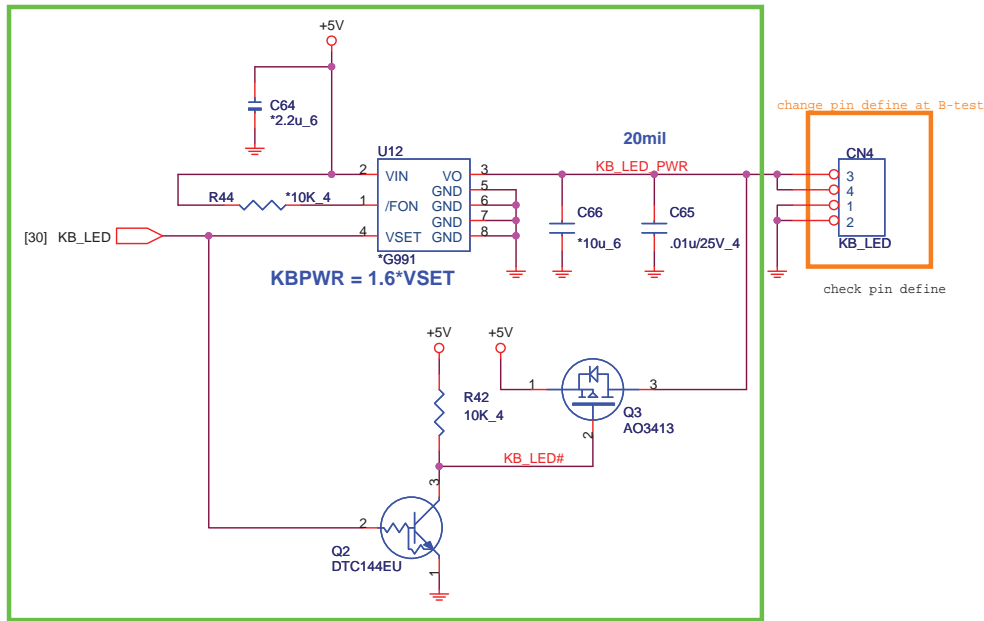
INT K/B

At 11/18 SWAP

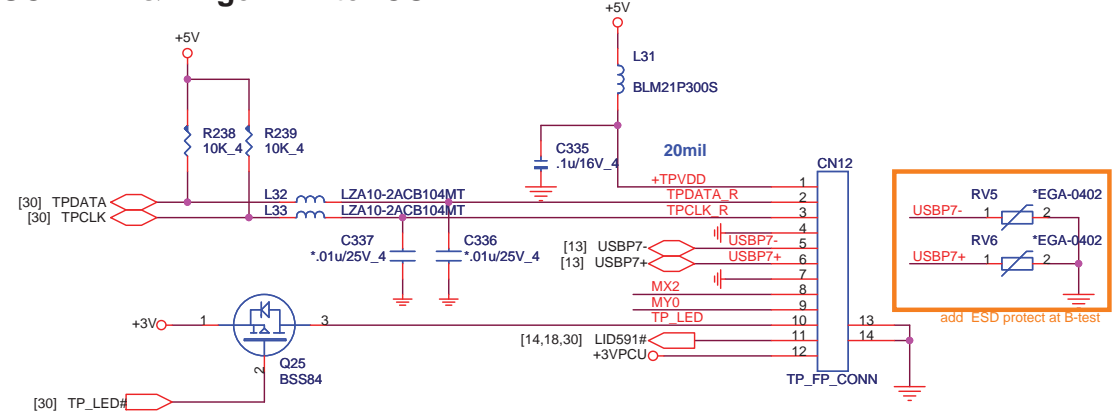


Keyboard LED control

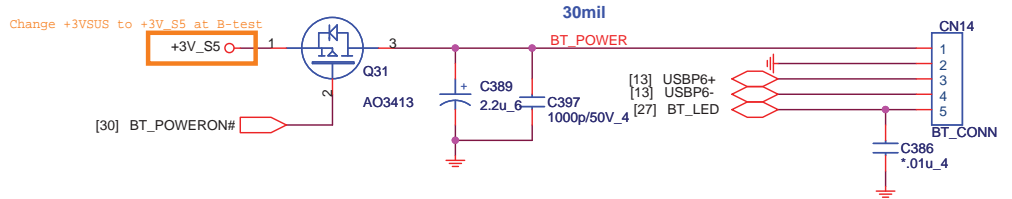
Remove: U12, C64, R44, C66.
Stuff: Q3, R42, Q2 at C-test



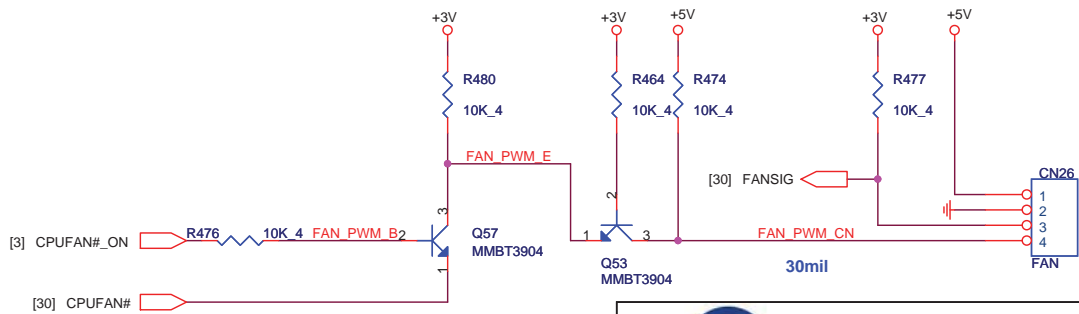
TOUCHPAD & Finger-Printer CONN.



BLUETOOTH CONNECTOR



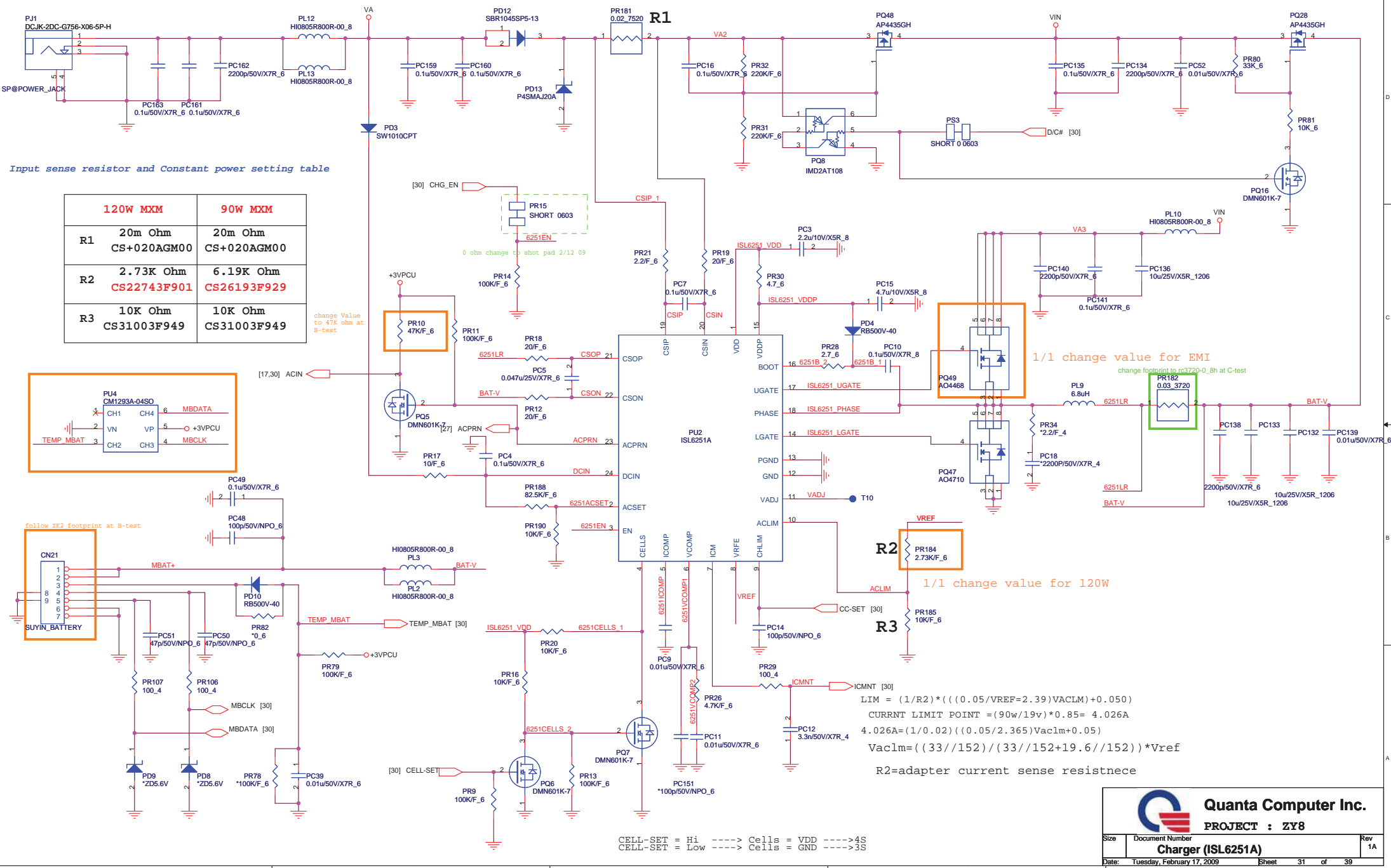
CPU FAN



Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
		3B

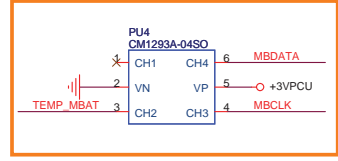
Date: Monday, February 16, 2009 Sheet 29 of 39



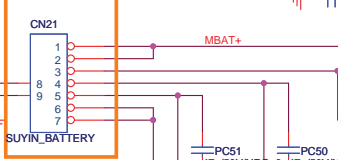
Input sense resistor and Constant power setting table

	120W MXM	90W MXM
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	2.73K Ohm CS22743F901	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949

change Value to 47k ohm at B-test



follow 2K2 footprint at B-test



$$LIM = (1/R2) * (((0.05/VREF=2.39) VACLm) + 0.050)$$

$$CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$$

$$4.026A = (1/0.02) * (((0.05/2.365) VACLm) + 0.05)$$

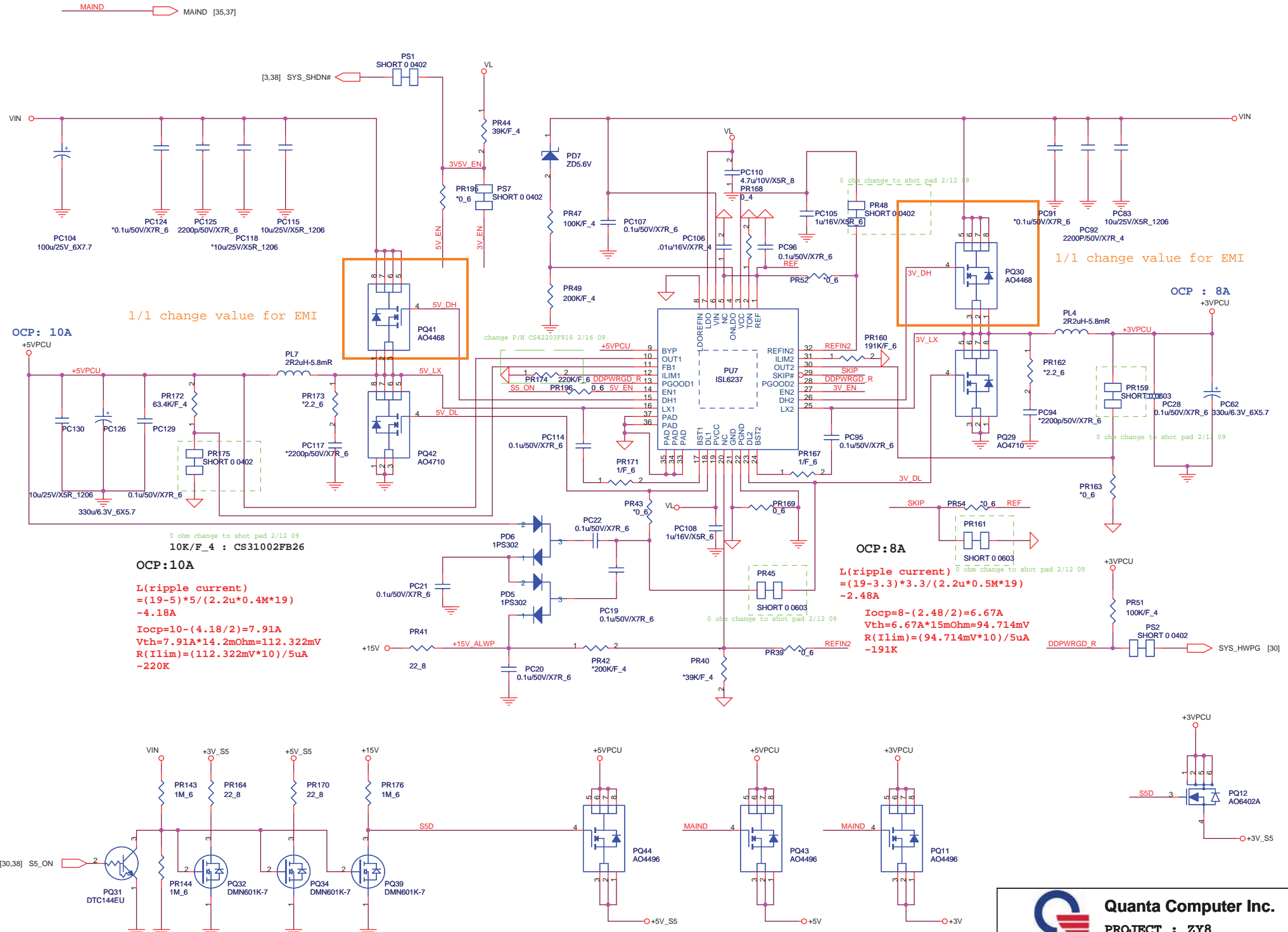
$$VACLm = ((33//152) / ((33//152) + 19.6//152)) * Vref$$

R2=adapter current sense resistnece

CELL-SET = Hi ----> Cells = VDD ----> 4S
 CELL-SET = Low ----> Cells = GND ----> 3S

Quanta Computer Inc.
 PROJECT : ZY8

Size	Document Number	Rev
	Charger (ISL6251A)	1A
Date:	Tuesday, February 17, 2009	Sheet 31 of 39



1/1 change value for EMI

1/1 change value for EMI

OCP: 10A

L(ripple current)
 = (19-5) * 5 / (2.2u * 0.4M * 19)
 ~ 4.18A
 Iocp = 10 - (4.18 / 2) = 7.91A
 Vth = 7.91A * 14.2mOhm = 112.322mV
 R(Ilim) = (112.322mV * 10) / 5uA
 ~ 220K

OCP: 8A

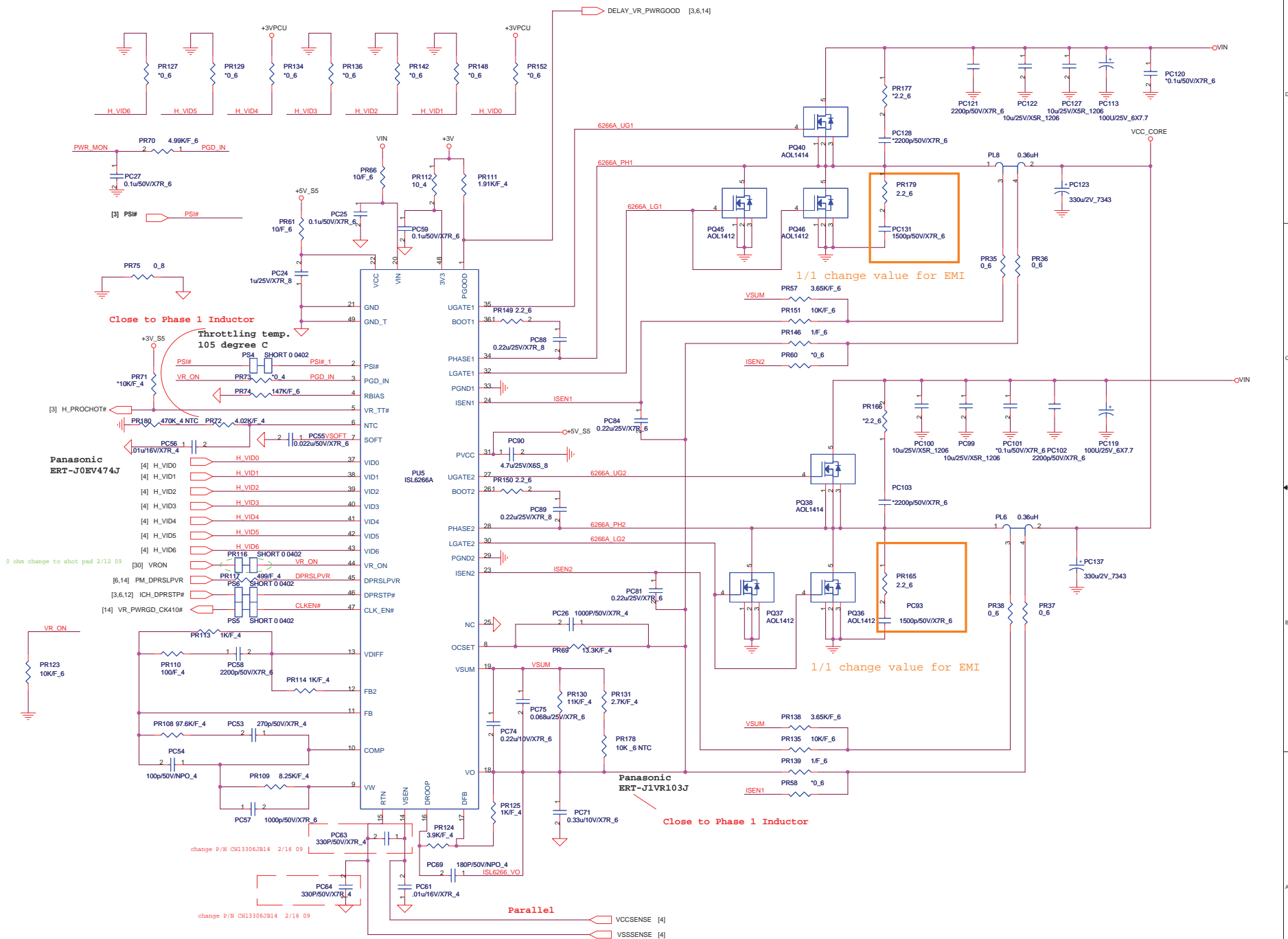
L(ripple current)
 = (19-3.3) * 3.3 / (2.2u * 0.5M * 19)
 ~ 2.48A

Iocp = 8 - (2.48 / 2) = 6.67A
 Vth = 6.67A * 15mOhm = 94.714mV
 R(Ilim) = (94.714mV * 10) / 5uA
 ~ 191K


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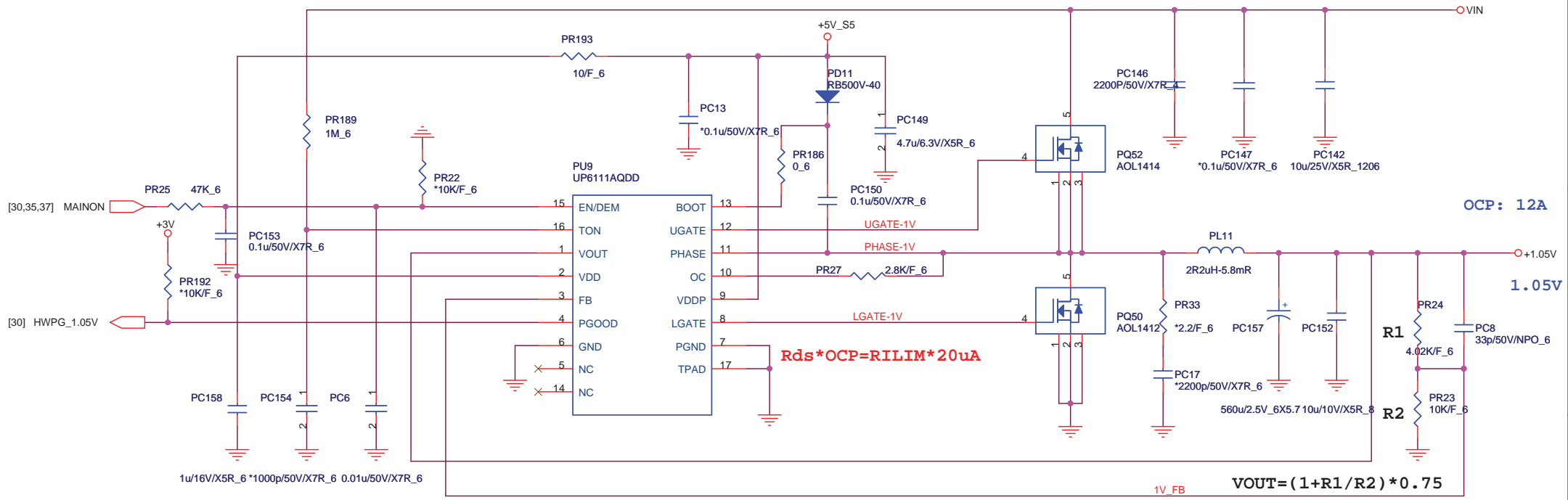
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PROJECT : ZY8

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	1A
Date:	Tuesday, February 17, 2009	Sheet 32 of 39



<http://laptop-motherboard-schematic.blogspot.com/>


Quanta Computer Inc.
 PROJECT : ZY8
 Document Number: QCP-RE(ISL6266A)
 Date: Tuesday, February 17, 2009 Sheet 33 of 39
 Rev 1A



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AOL1412 $R_{dson} = 4.6m\Omega$

OCP = 16 - 0.8A

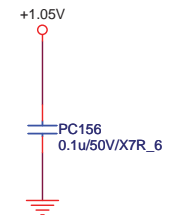
$$L(\text{ripple current}) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.646A$$


$$4.6m * 12 = RILIM * 20uA$$

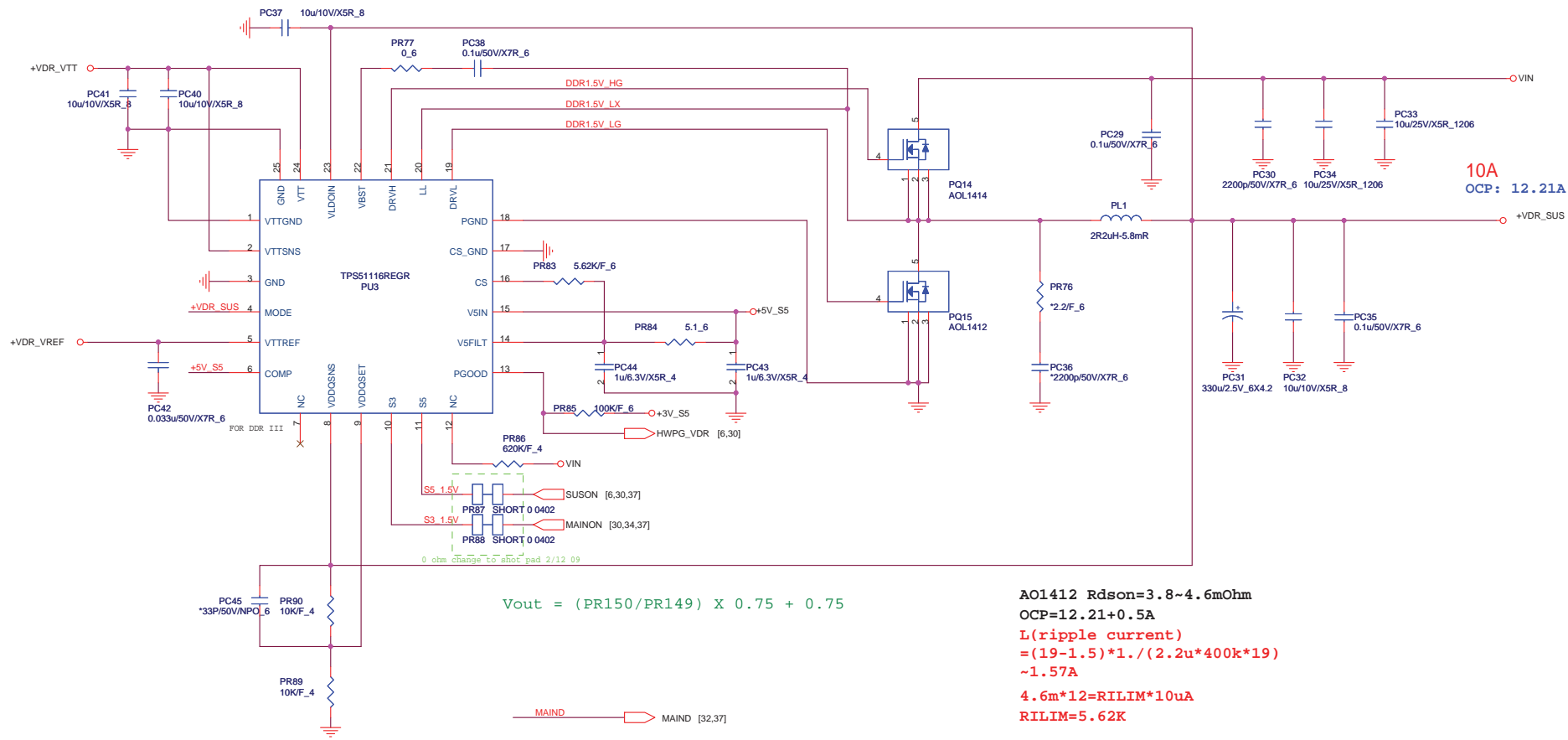
$$RILIM = 2.76K \text{ --- } 2.8K$$

$$VOUT = (1 + R1/R2) * 0.75$$

1V_FB

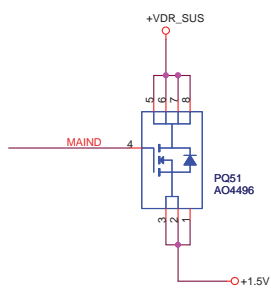


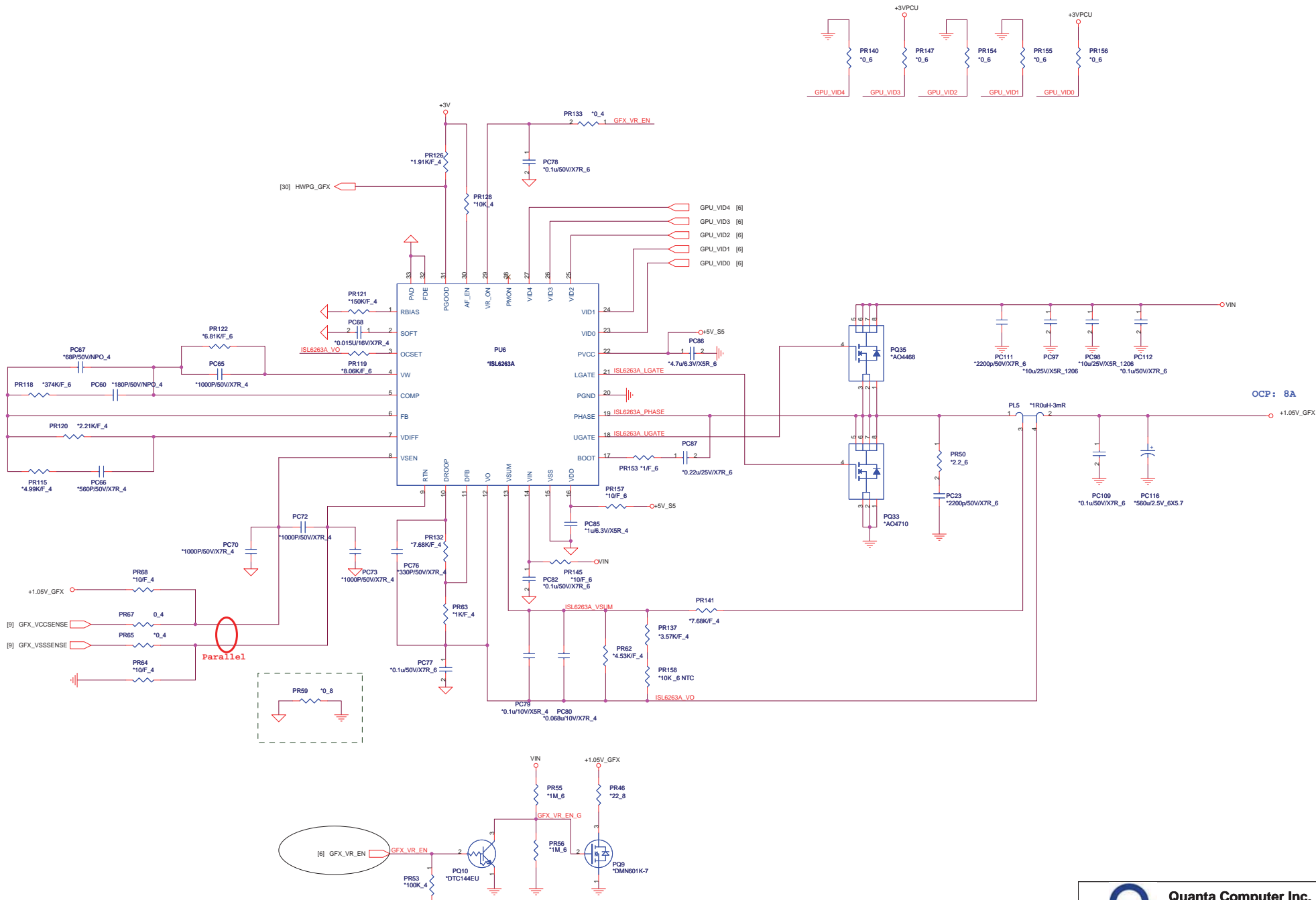
 Quanta Computer Inc. PROJECT : ZY8		Size	Document Number	Rev
		VCCP 1.05V(UP6111A)		1A
Date:	Tuesday, February 17, 2009	Sheet	34	of 39



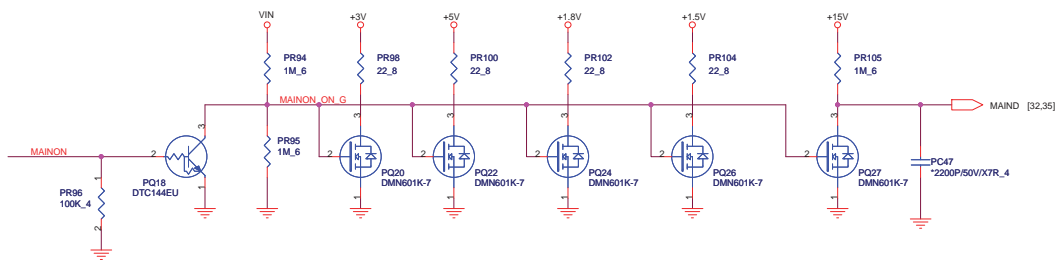
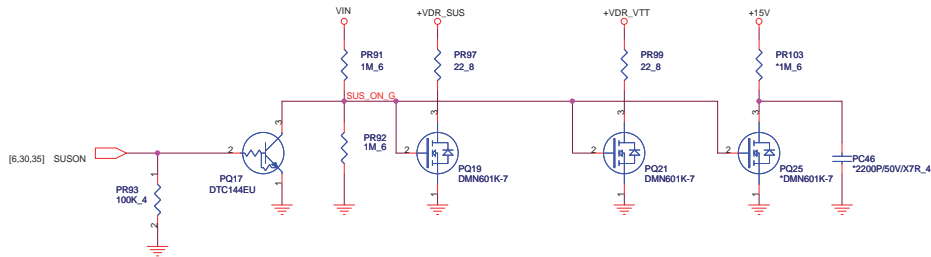
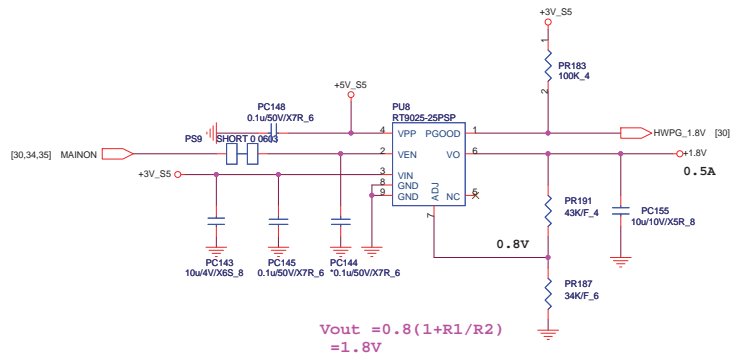
$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO1412 $R_{dson} = 3.8 \sim 4.6m\Omega$
 OCP = 12.21 + 0.5A
 L(ripple current)
 $= (19 - 1.5) \times 1. / (2.2u \times 400k \times 19)$
 $\sim 1.57A$
 $4.6m \times 12 = RILIM \times 10uA$
 RILIM = 5.62K
 $(10u \times PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$

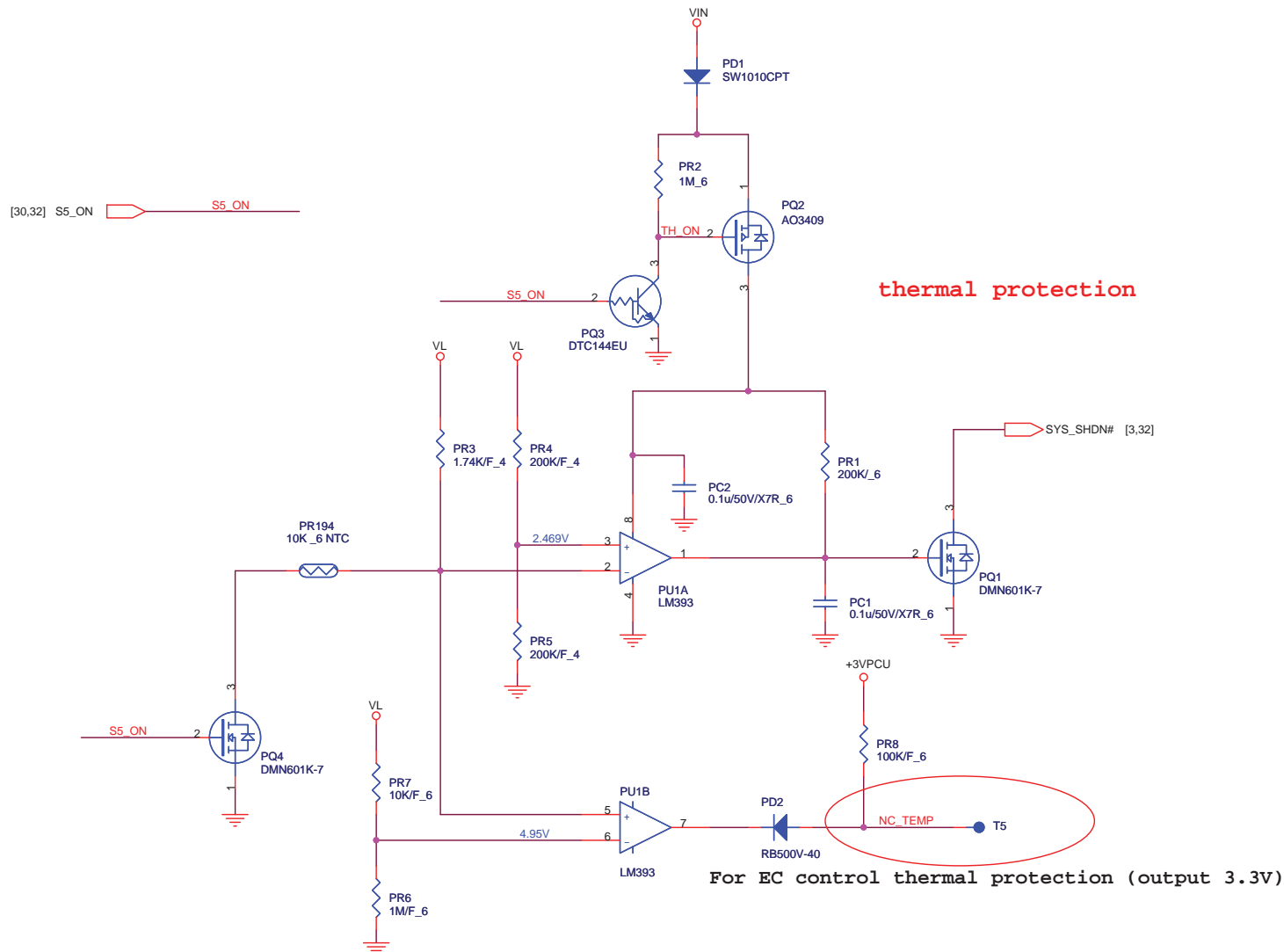





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 Quanta Computer Inc. PROJECT : ZY8		Rev 1A
Date: Tuesday, February 17, 2009		Sheet 38 of 39

