

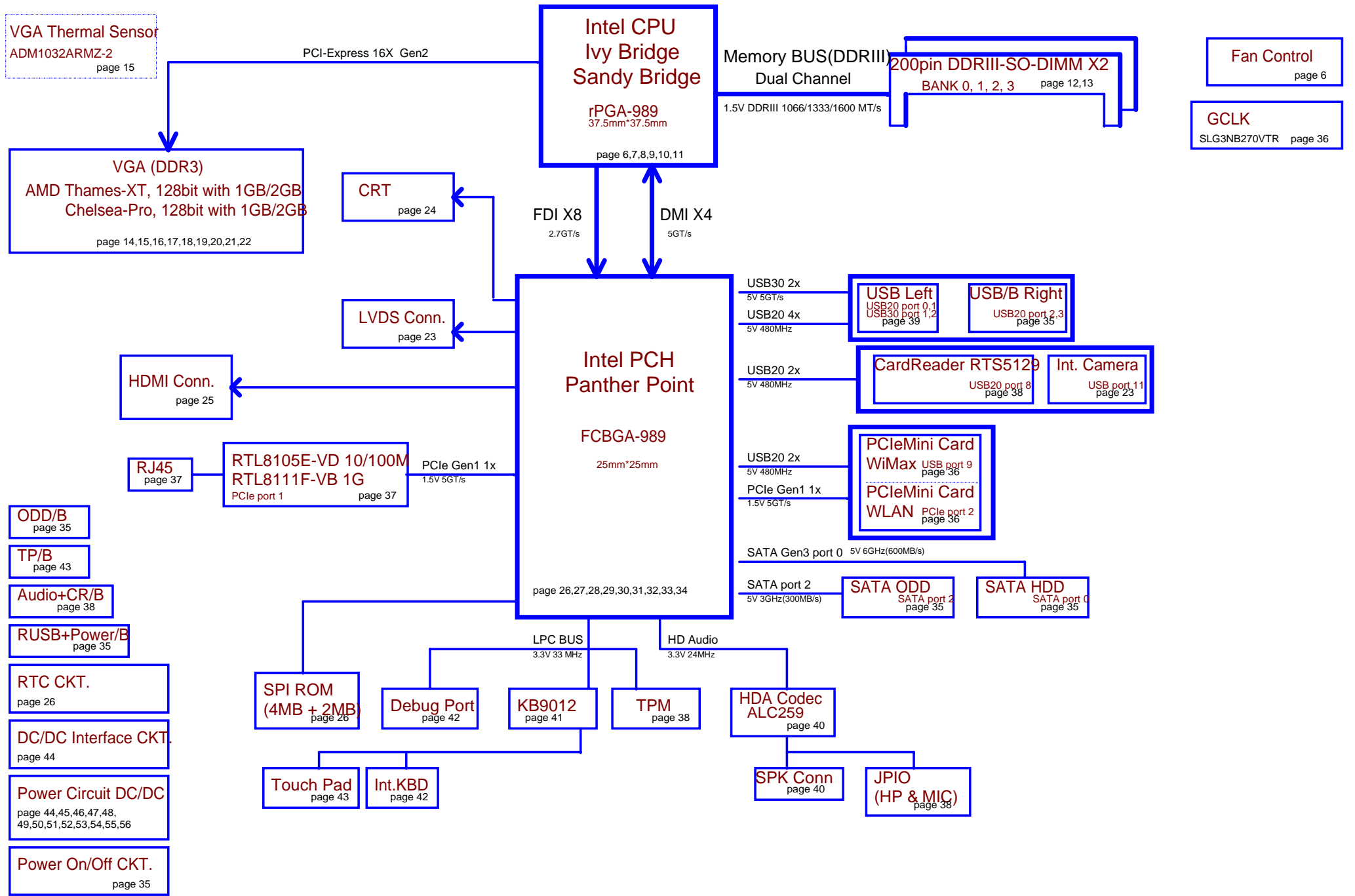
QCLA4 / QCLA5

Eureka 10FG

LA-8861P REV 0.2 Schematic

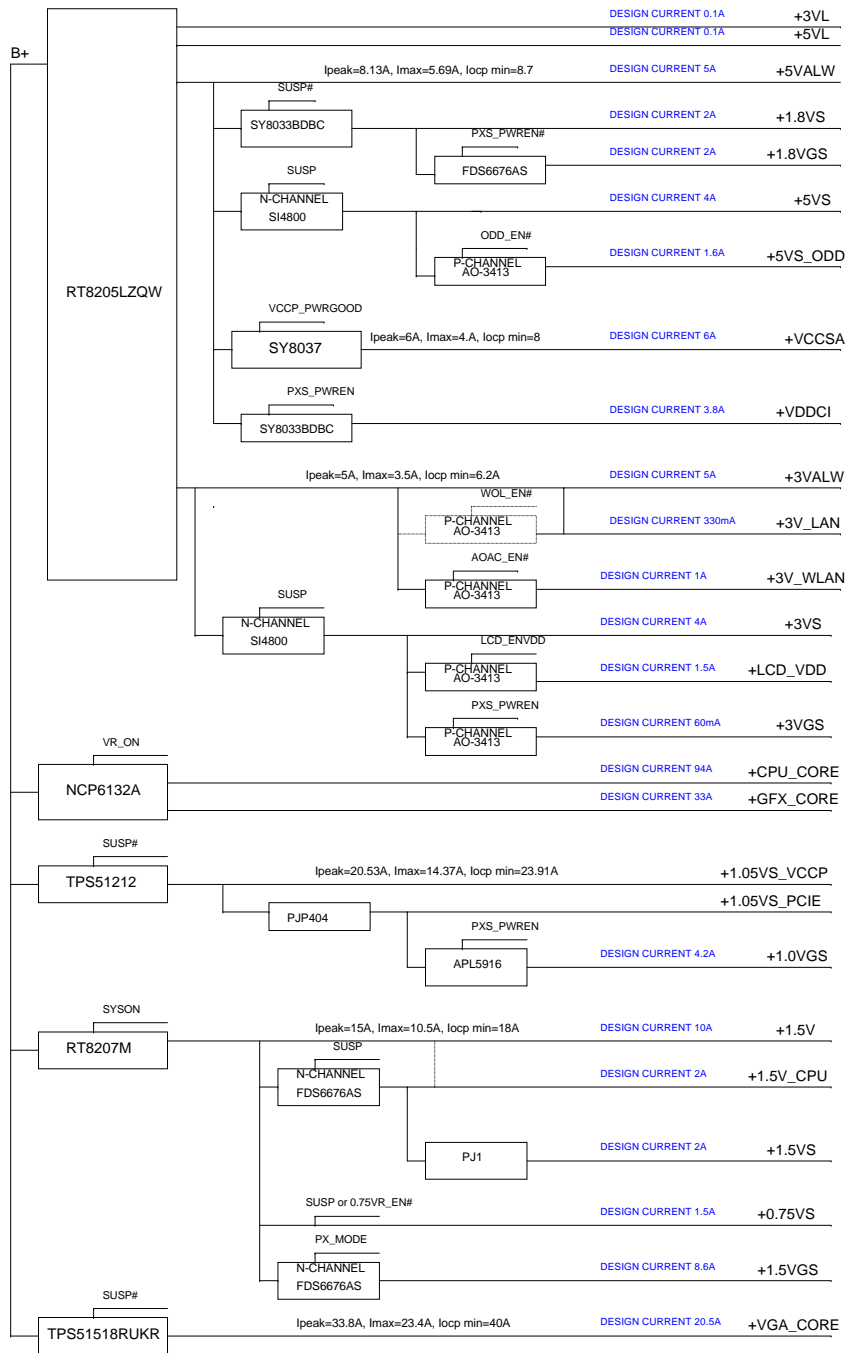
Intel Processor (Ivy Bridge) / PCH(Panther Point)
2012-02-09 Rev 0.2

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU	
	S0	O	O	O	O	O	
	S1	O	O	O	O	O	O
	S3	O	O	O	O	O	X
	S5 S4/AC	O	O	O	O	X	X
	S5 S4/ Battery only	O	O	O	X	X	X
	S5 S4/AC & Battery don't exist	O	X	X	X	X	X

Platform	SKU	CPU	PCH	VGA
Chief River		Clarksfield	HM76ES2/HM70C0 (PCHB0@/HM70C0@)	Themes/Chlsea (TH@/CH@)

BTO Option Table

Function	SKU	MIC	LAN	TPM
description	SKU	MIC	LAN	TPM
explain	PX4(reserve)	Dig Mic	Analog Mic	10/100M Giga 9635 9655
BTO	PX4@	CAM@	AMIC@	8105ELDO@ 8111FVB@ TPM9635@ TPM9655@

Function							
description							
explain							
BTO							

Function							
description							
explain							
BTO							

Function			
description			
explain			
BTO			

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH	HIGH
S3(Suspend to RAM)		LOW	HIGH	HIGH
S4(Suspend to Disk)		LOW	LOW	HIGH
S5(Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address

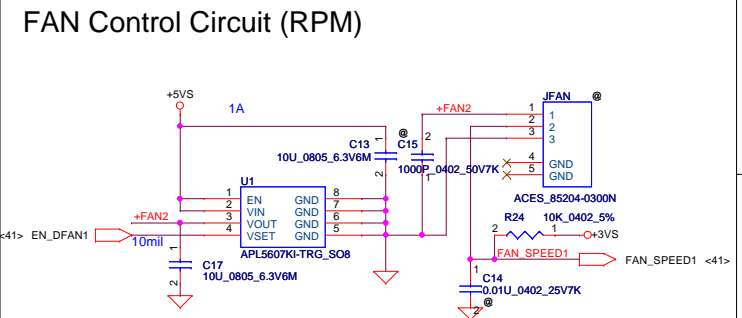
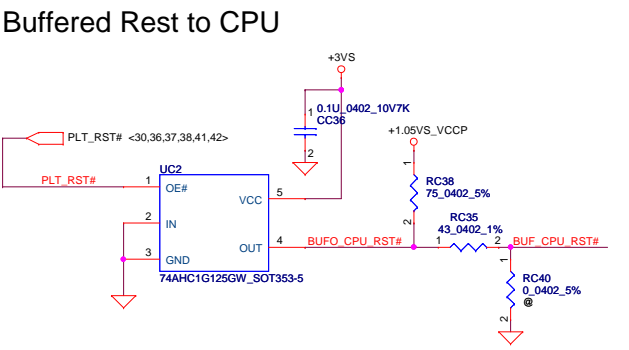
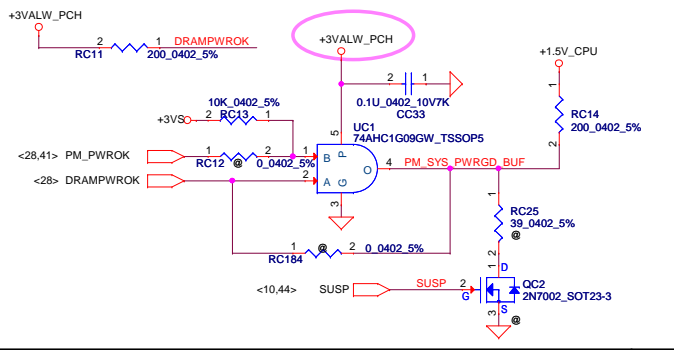
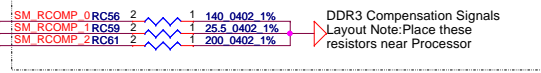
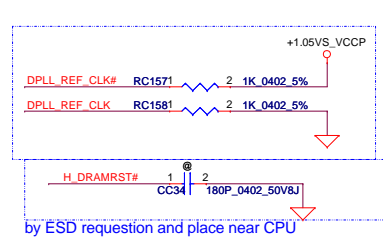
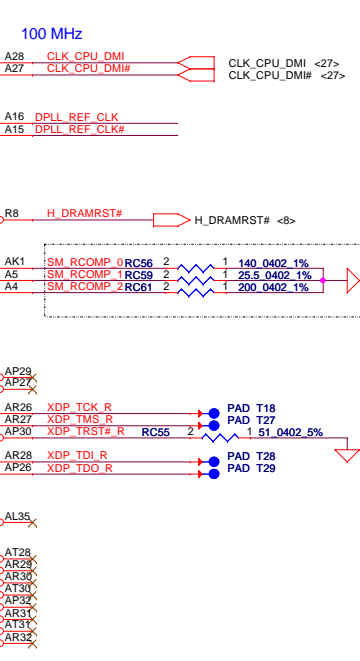
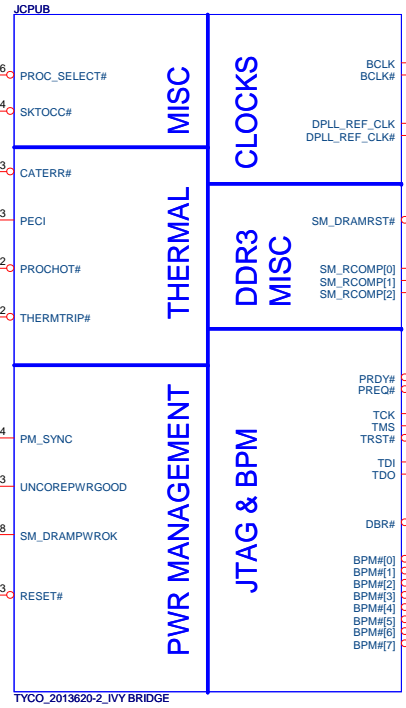
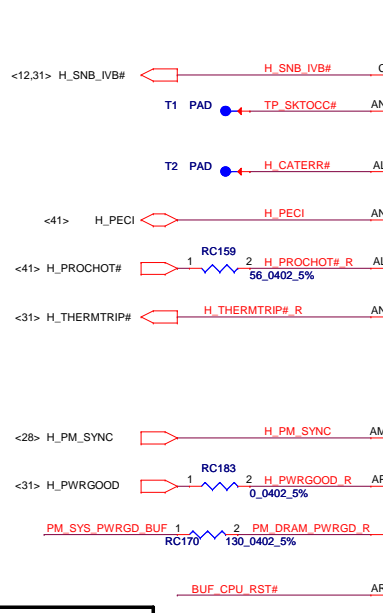
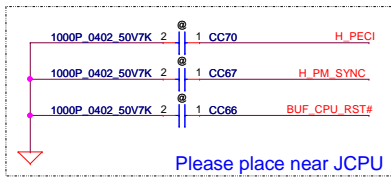
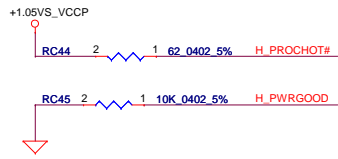
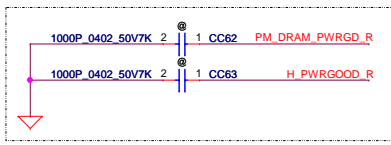
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	ATI GPU	82 H	1000 0010 b
Power	Device	HEX	Address

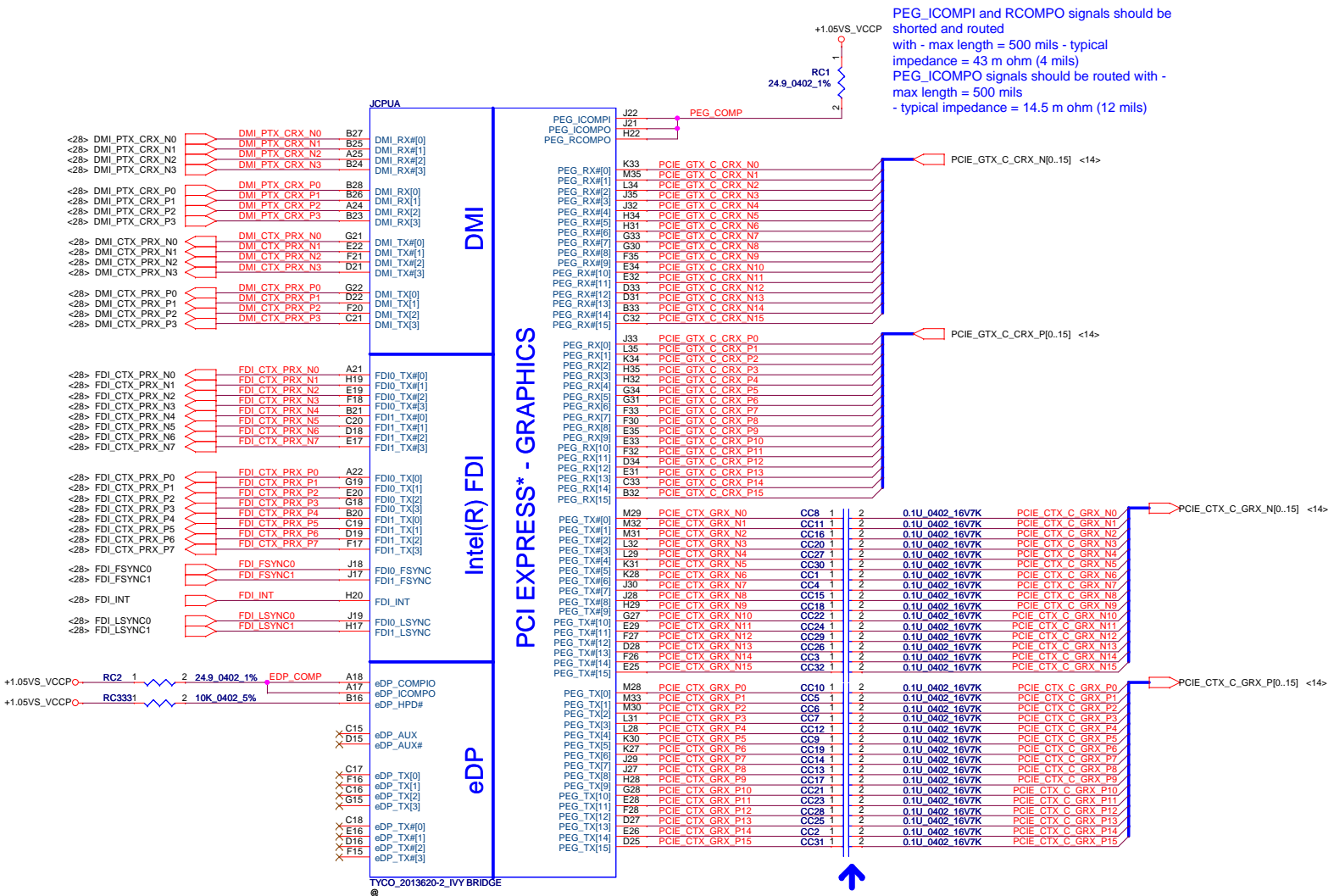
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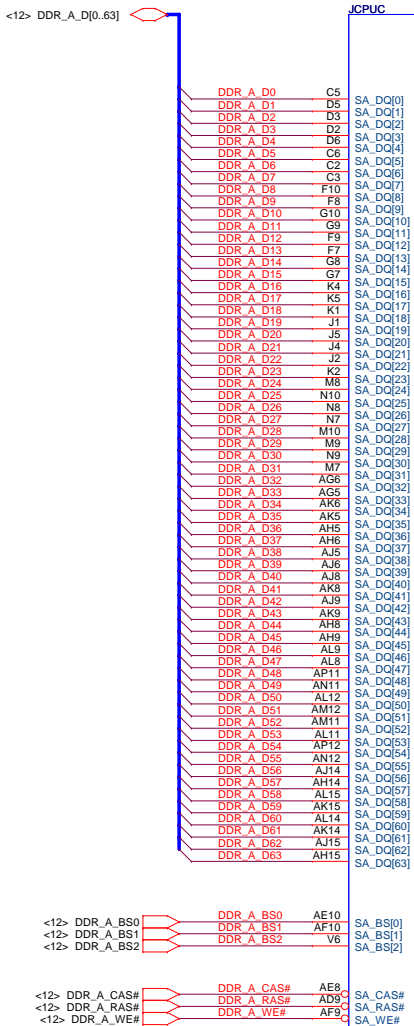
www.pdzpwx.com



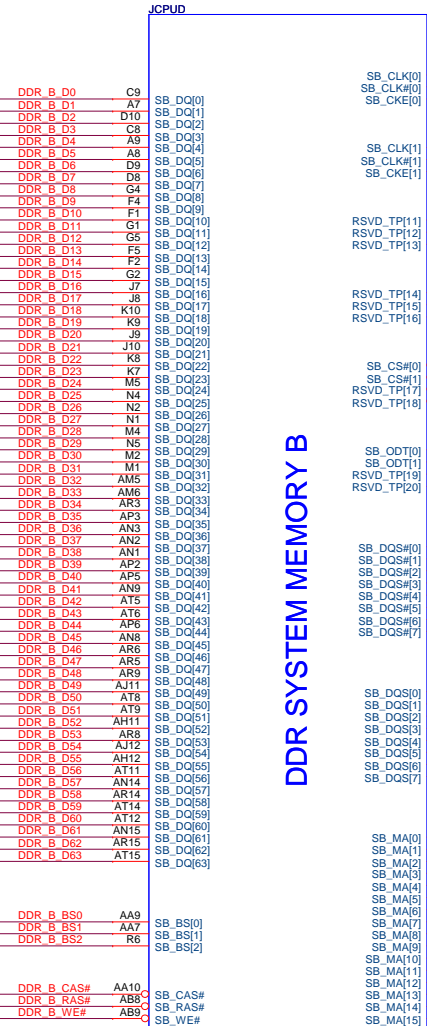
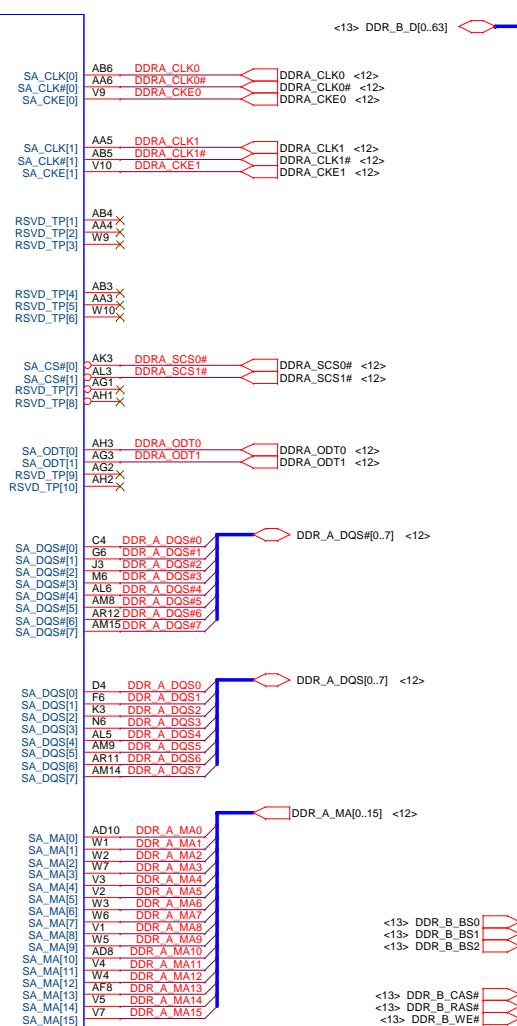
	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF-265 nF
	Gen3	180 nF-265 nF
SANDY Bridge	Gen1/Gen2	100 nF-220 nF

AMD GPU (Themes & Chlsea) only support up to Gen2

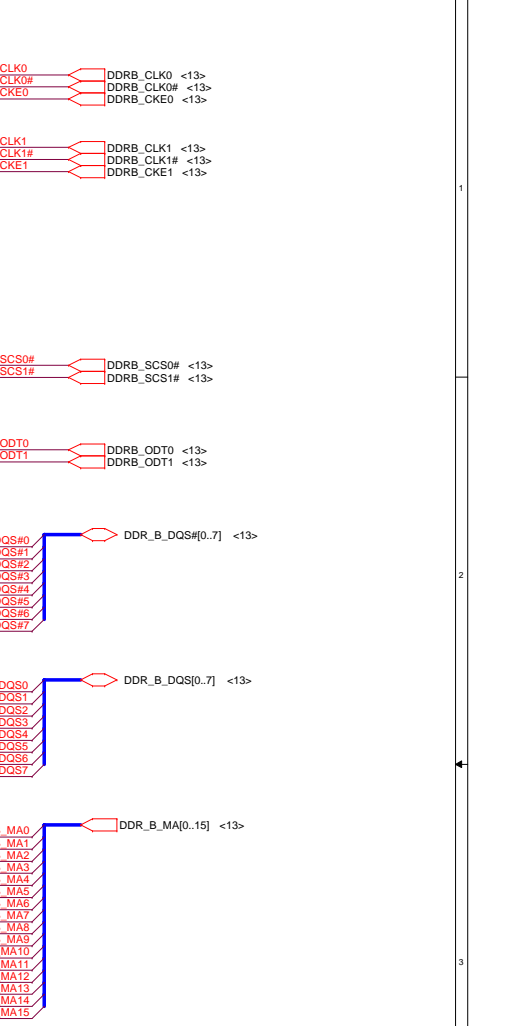
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DDR SYSTEM MEMORY A

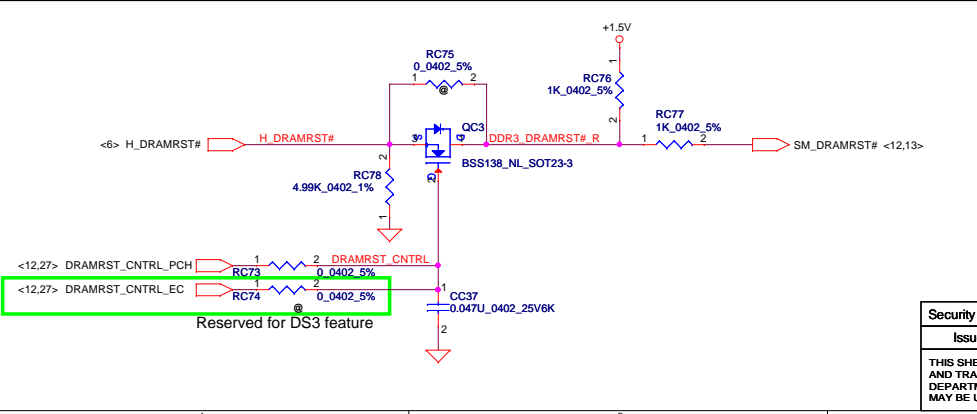


DDR SYSTEM MEMORY B

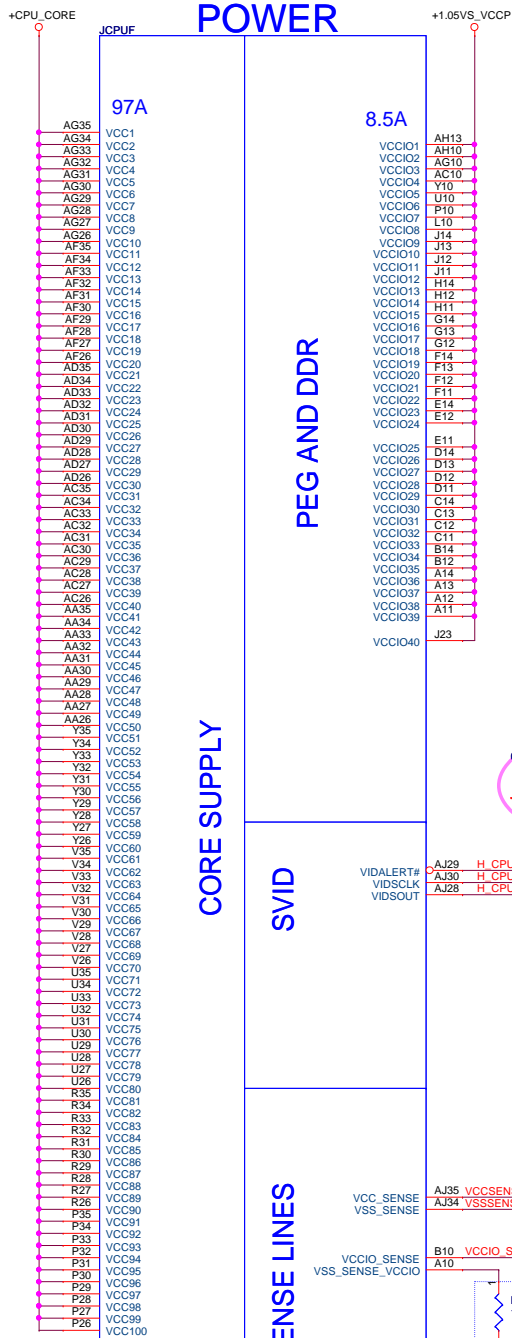


TYCO_2013620-2_IVY BRIDGE

TYCO_2013620-2_IVY BRIDGE



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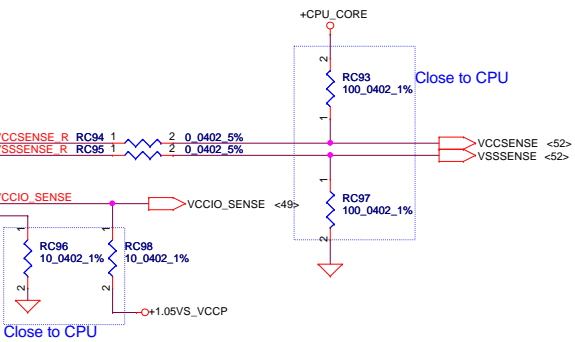
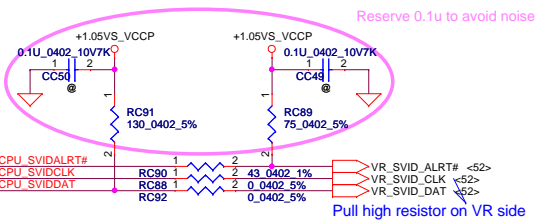
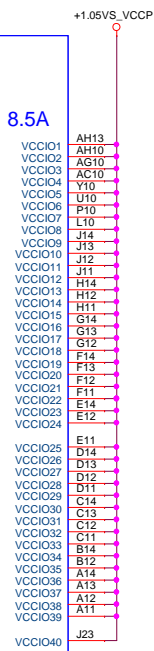
POWER

CORE SUPPLY

SENSE LINES

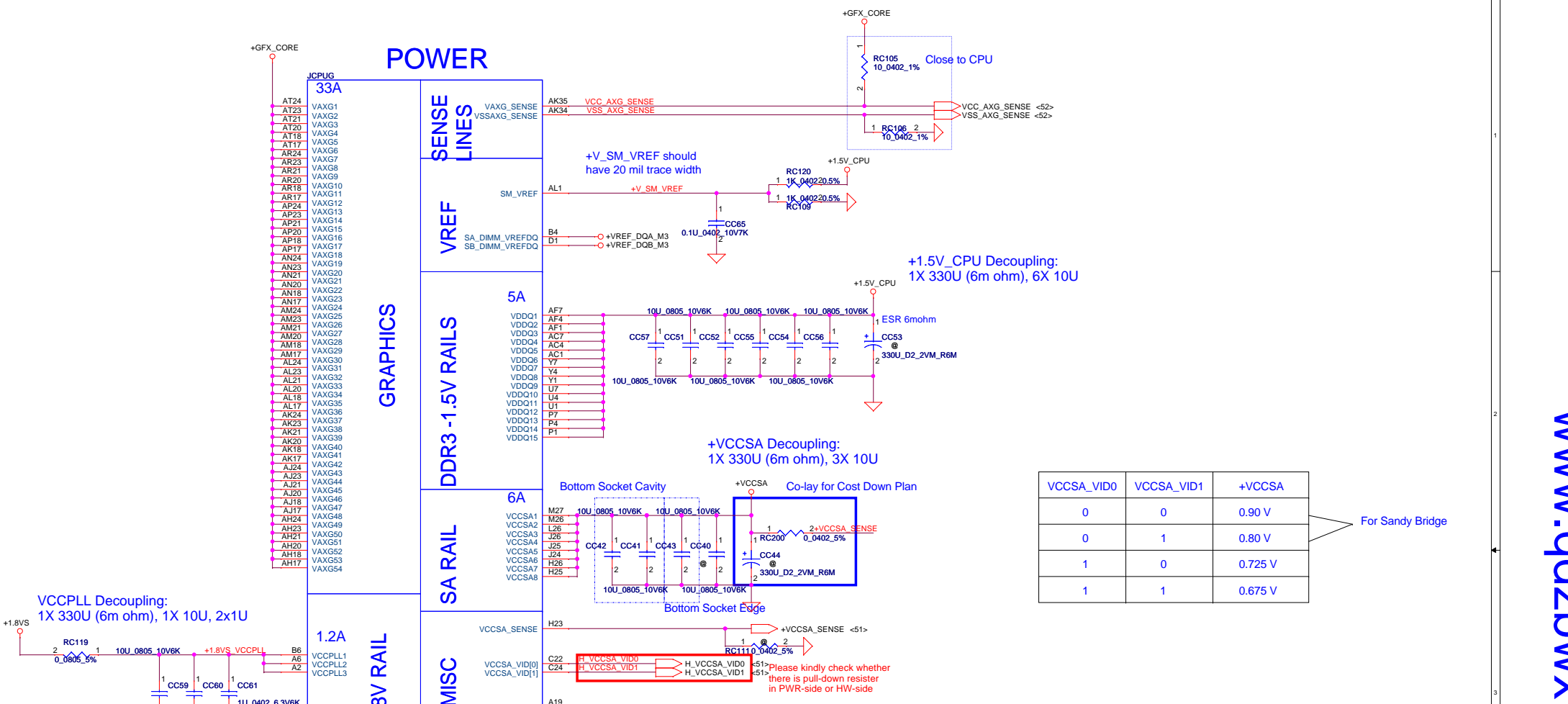
PEG AND DDR

SVID



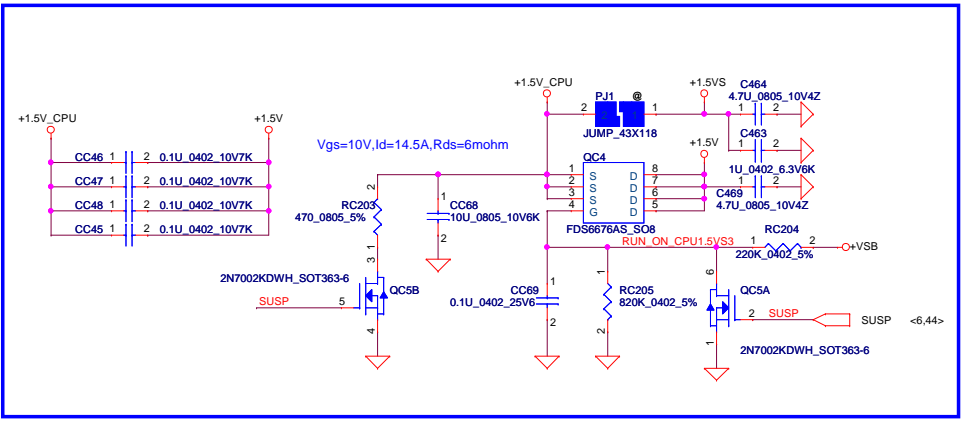
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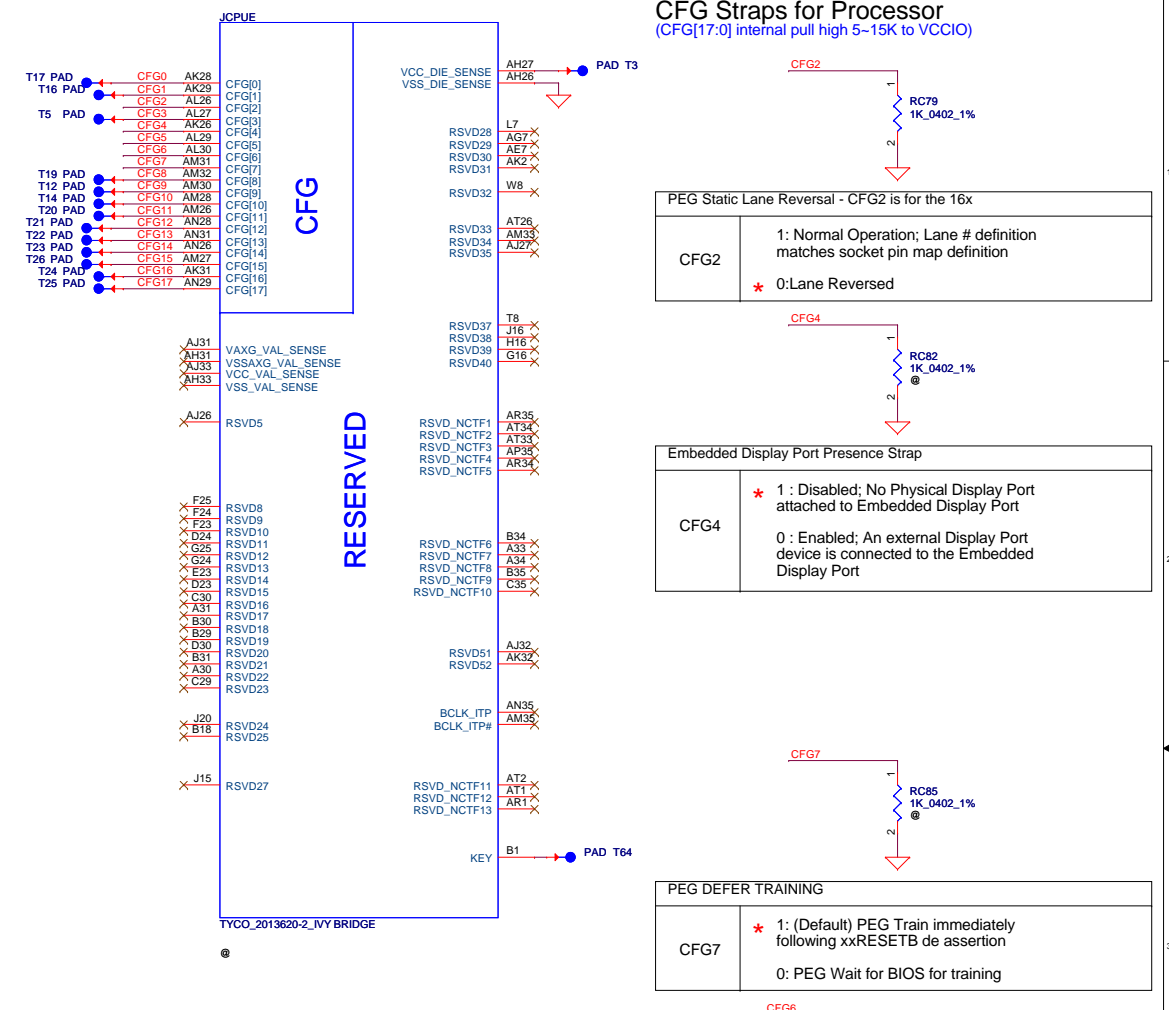
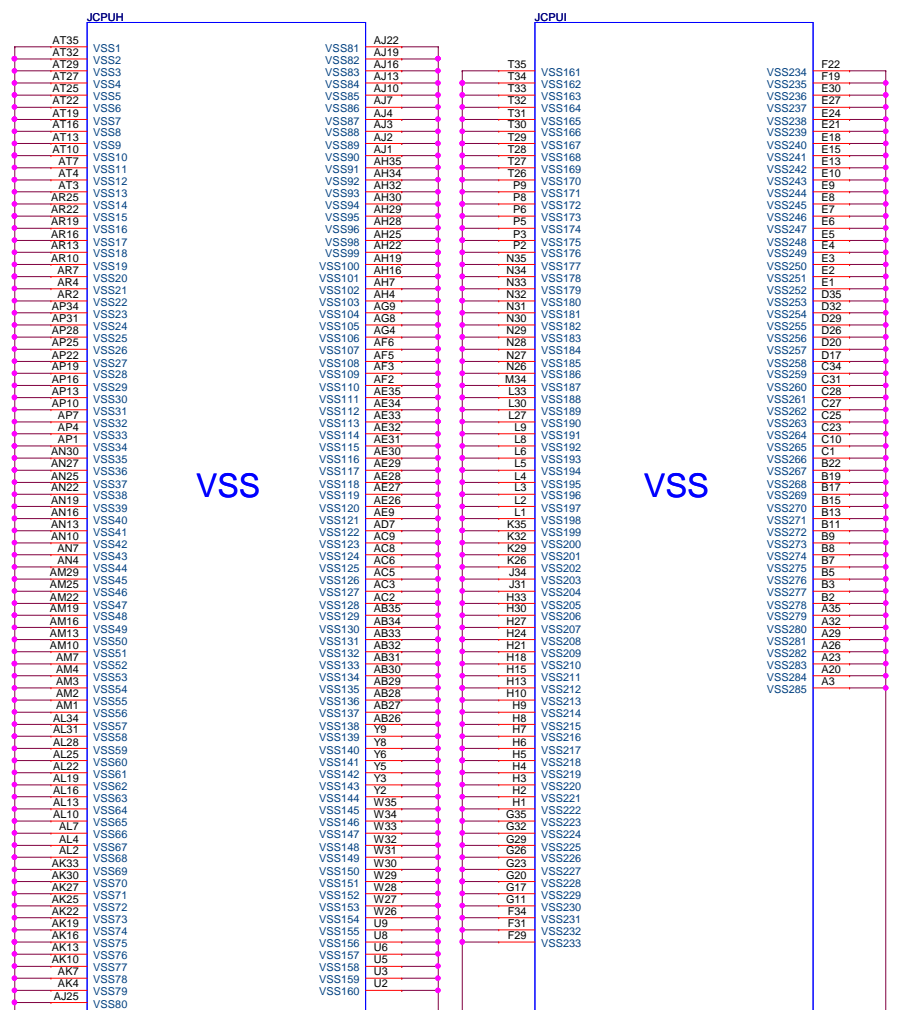
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge



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CFG Straps for Processor
(CFG[17:0] internal pull high 5~15K to VCCIO)

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed

Embedded Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING

CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

PCIe Port Bifurcation Straps

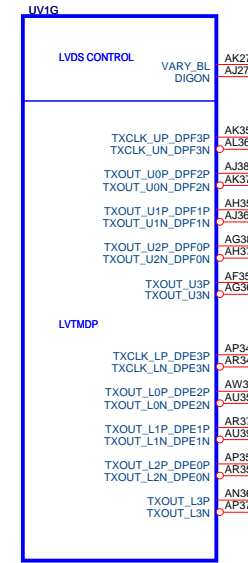
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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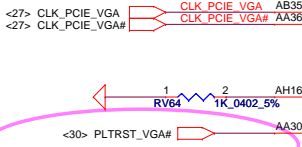
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GFX PCIE LANE REVERSAL

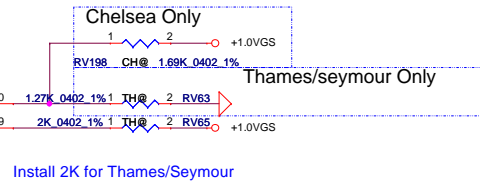
LVDS Interface



THAMES XT M2 TH0



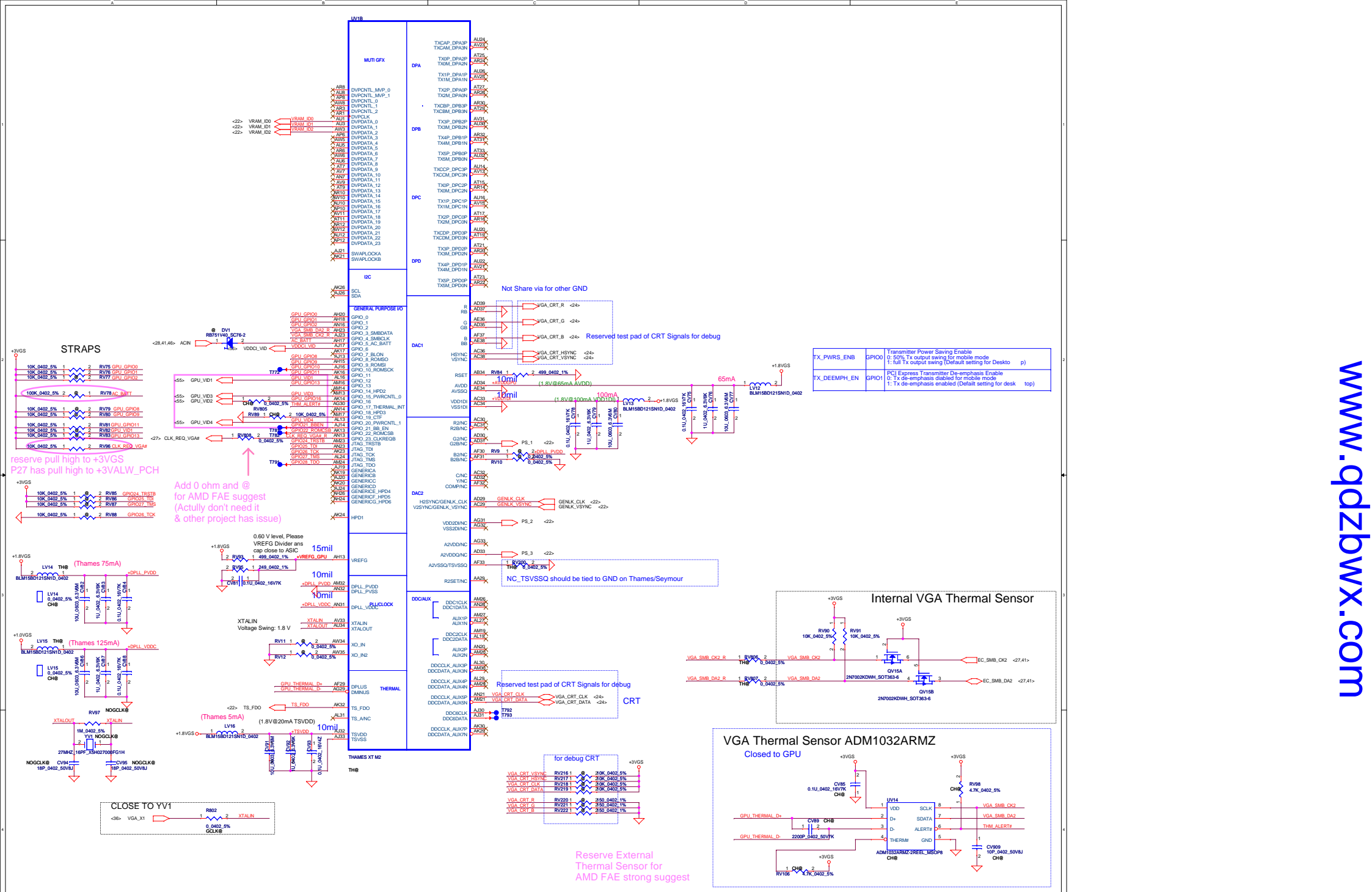
Pull down 100k in P30



RV65
1K 0.402 1%
CH0

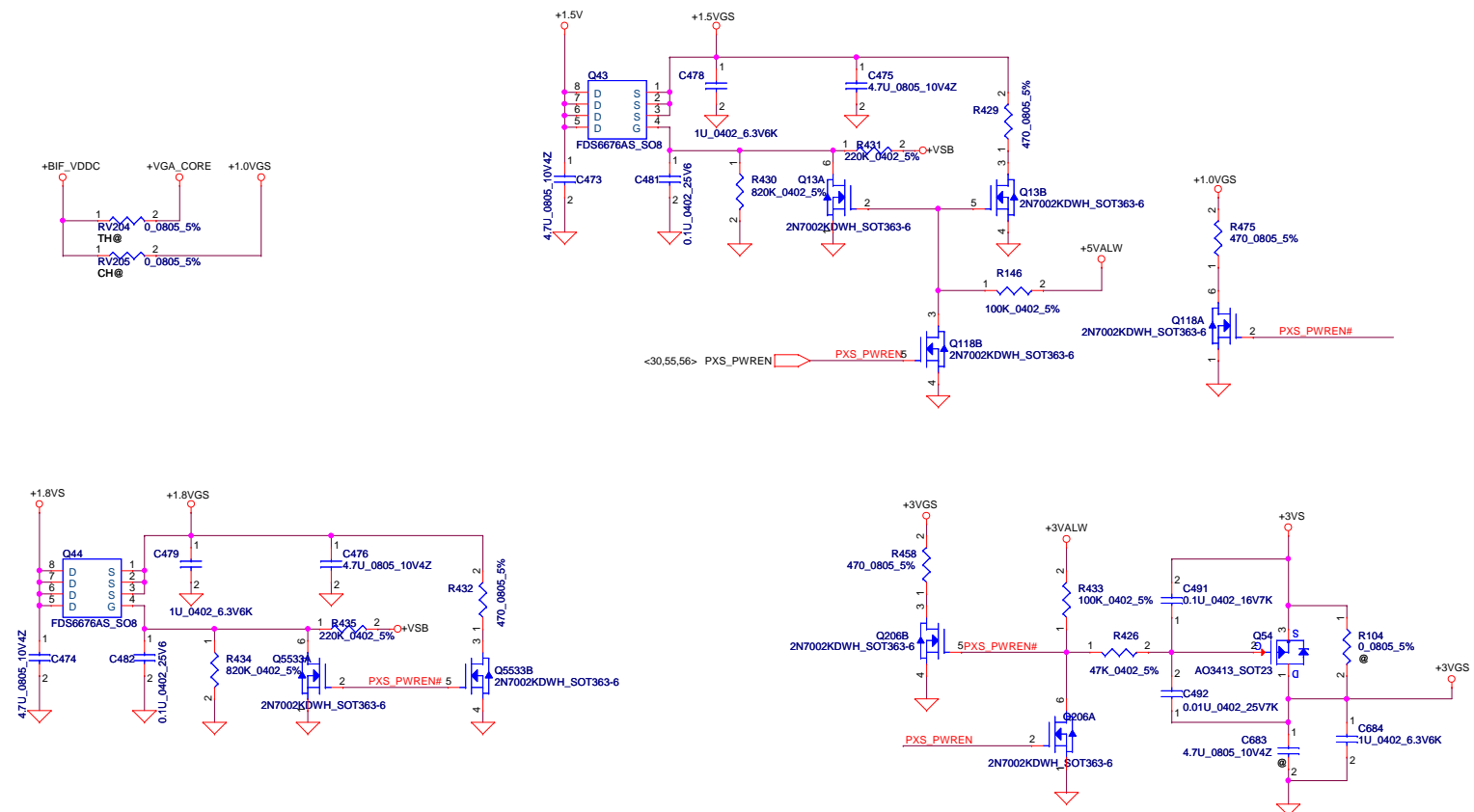
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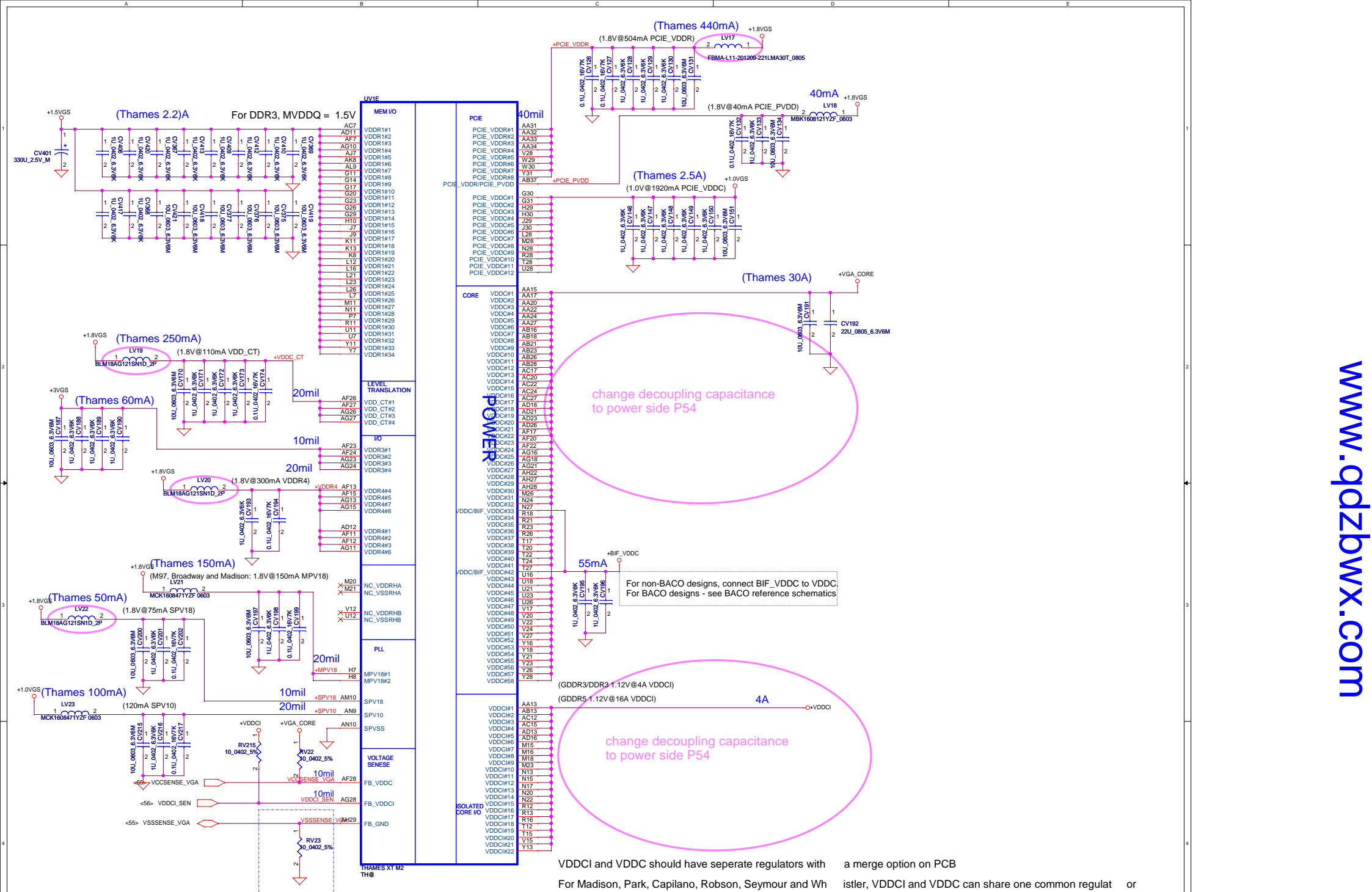


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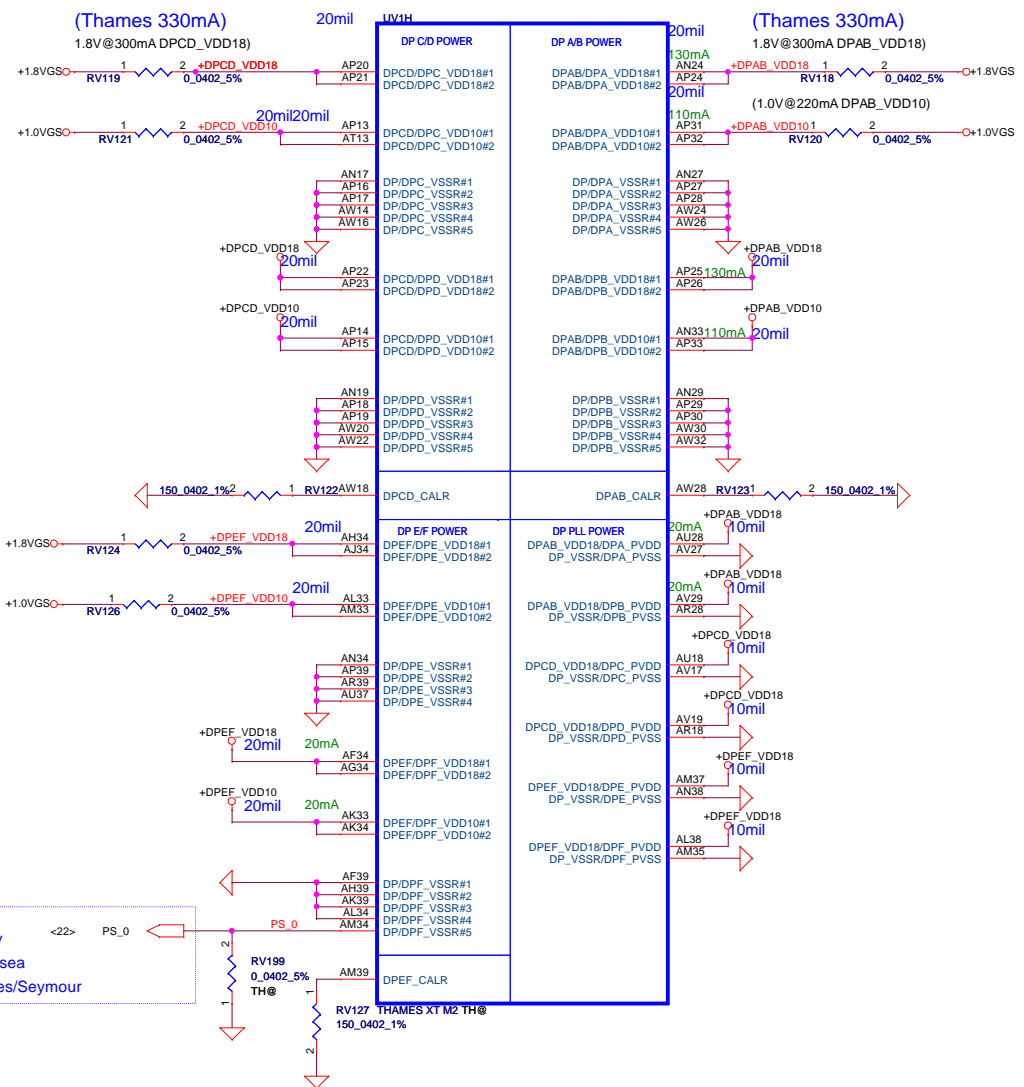
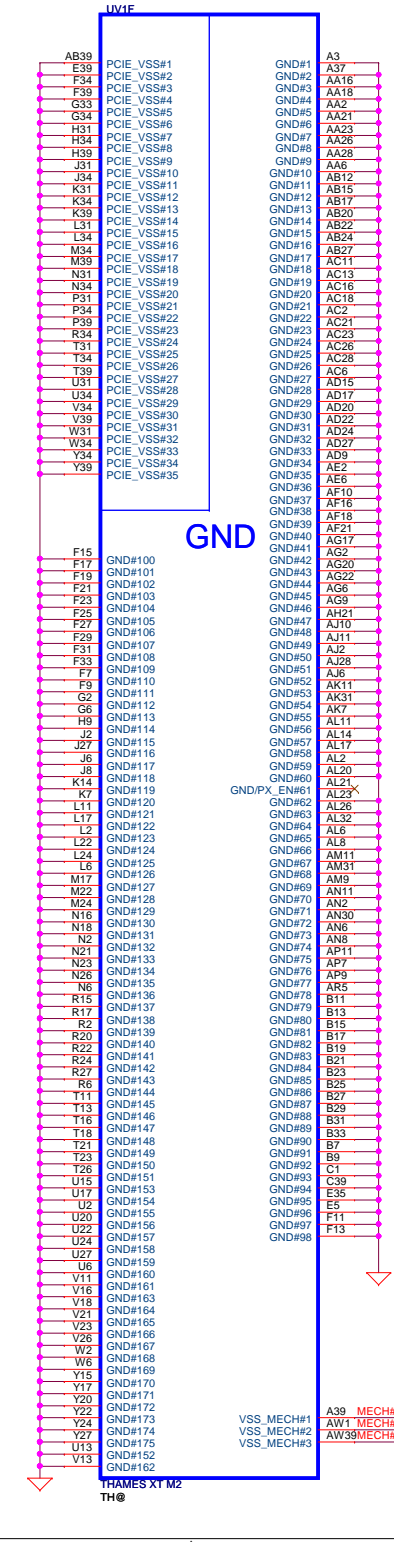
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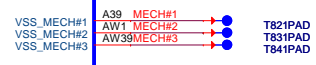
Compal Electronics, Inc.	
Title	ATI_SeymourXT_M2_Power

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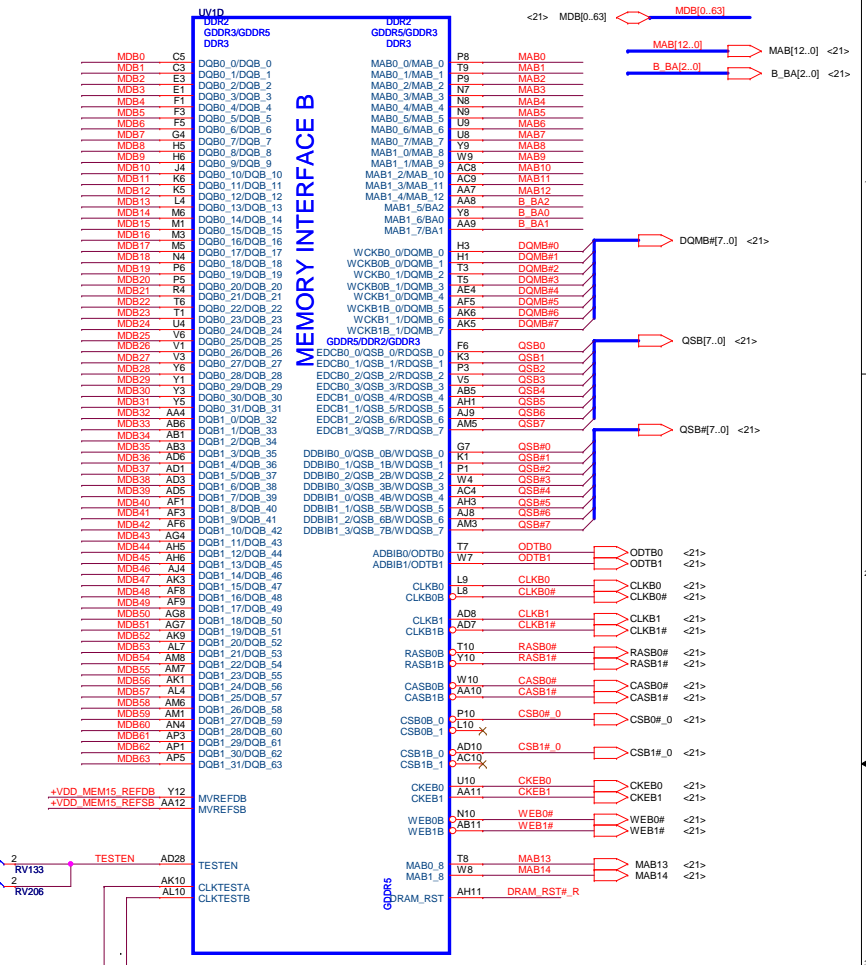
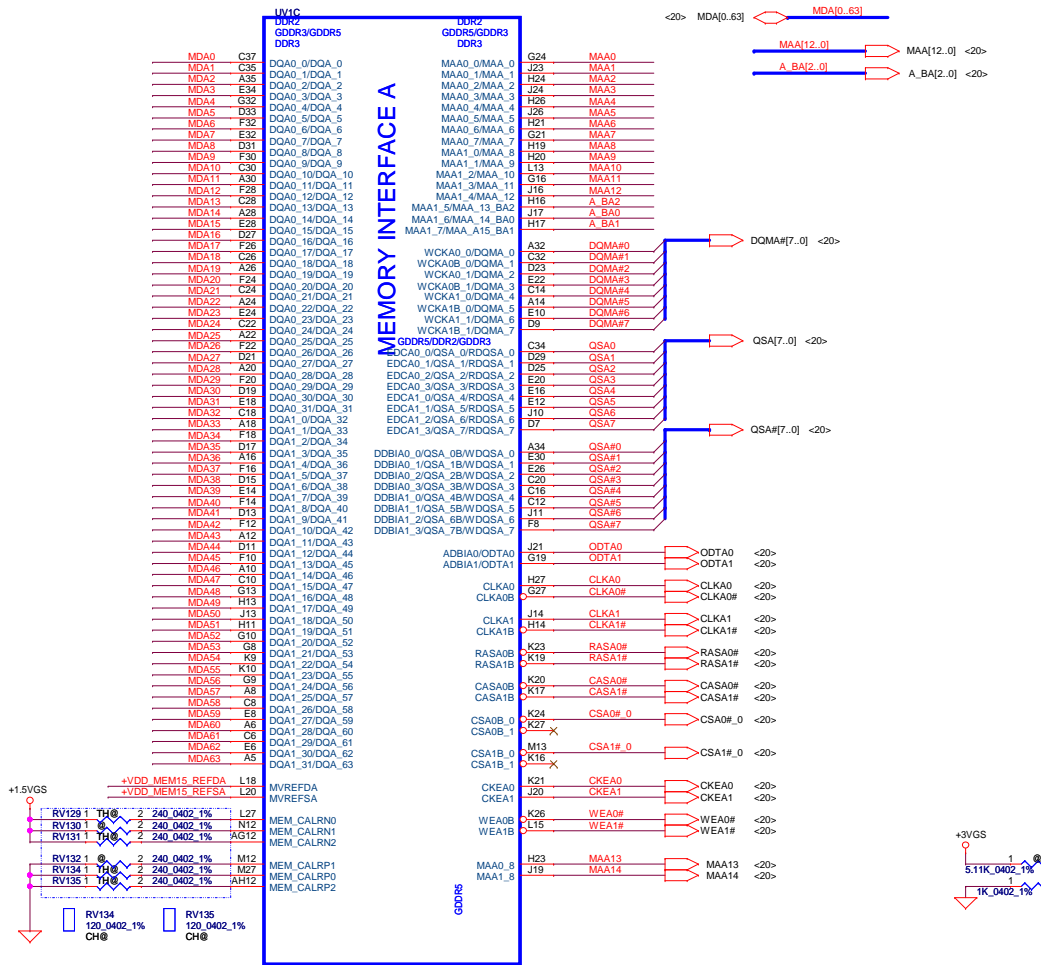


Thames/Seymour Only <2> PS_0
 Do not install for Heathrow/Chelsea
 PS_0 Should be tied to GND on Thames/Seymour

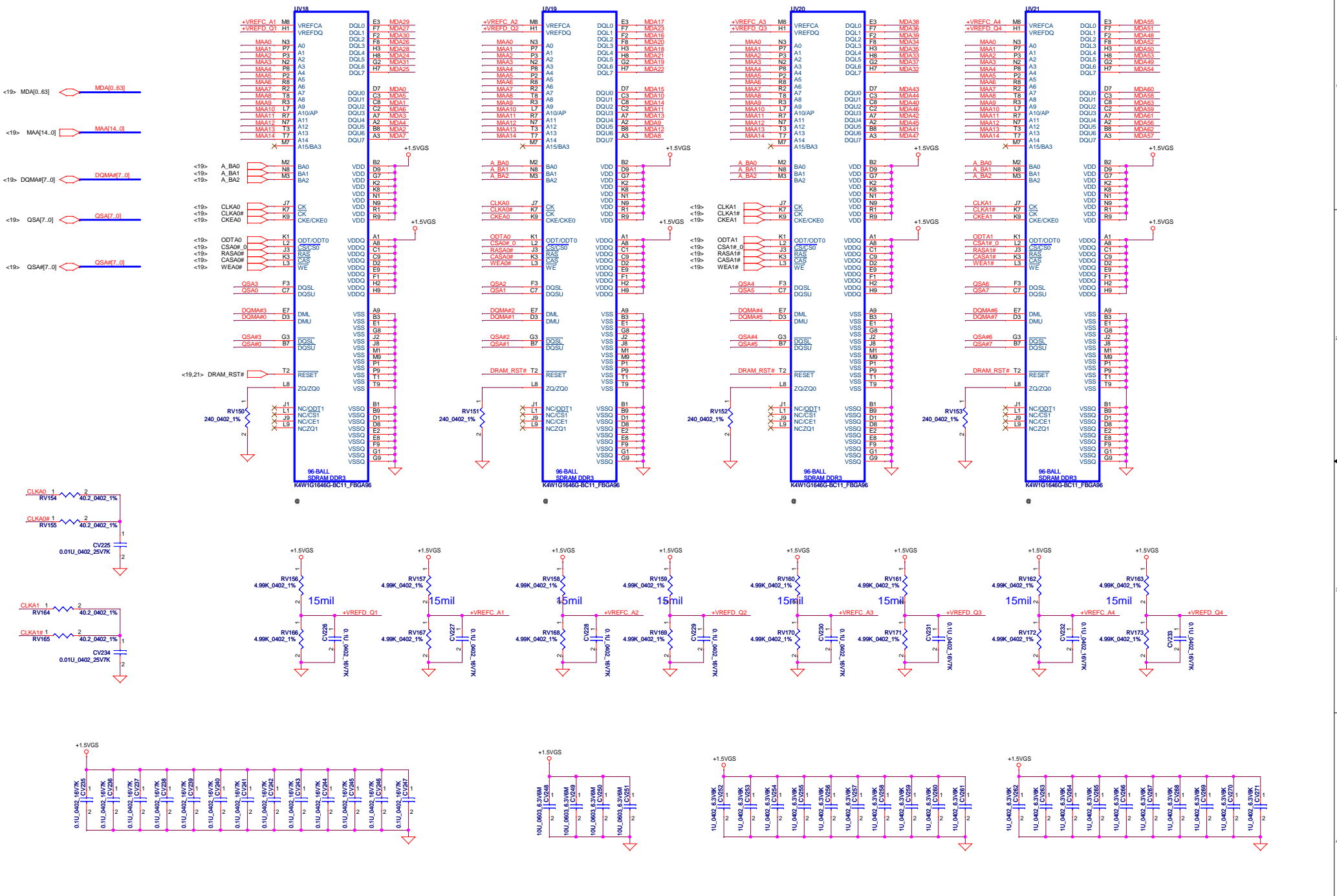


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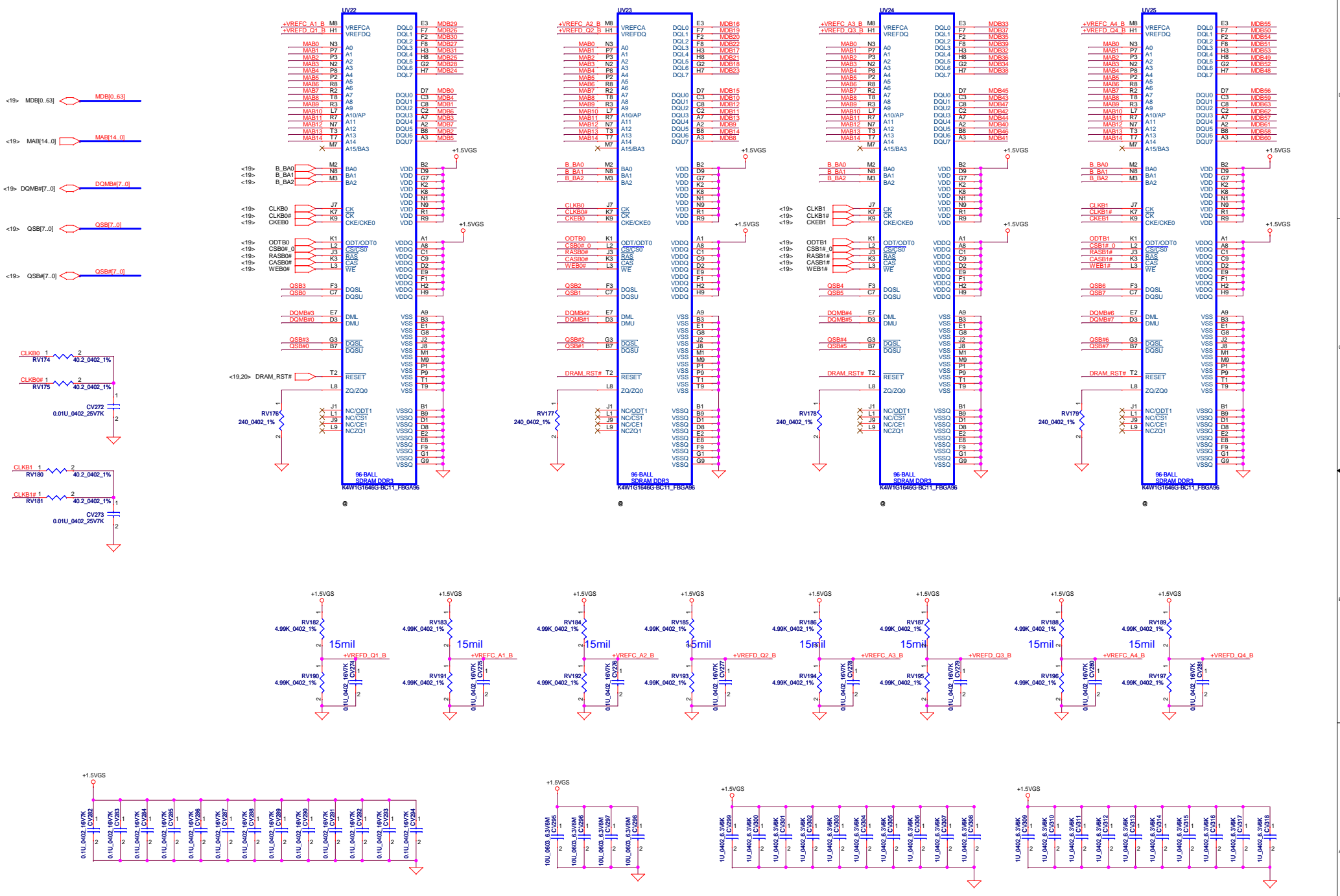
CHANNEL A: 256MB/512MB DDR3



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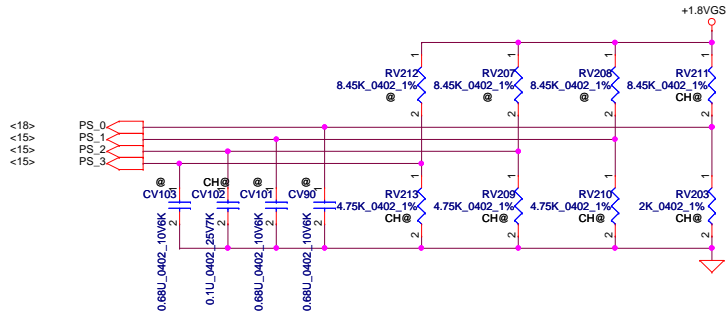
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Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title
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Size	C	Document Number	QCLA4 LA-8861P M/B	Rev 02
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CHANNEL B: 256MB/512MB DDR3

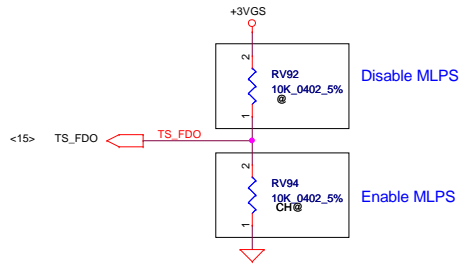


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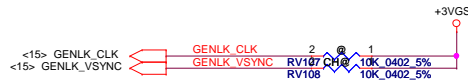
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Size	C	Document Number	QCLA4 LA-8861P M/B	Rev
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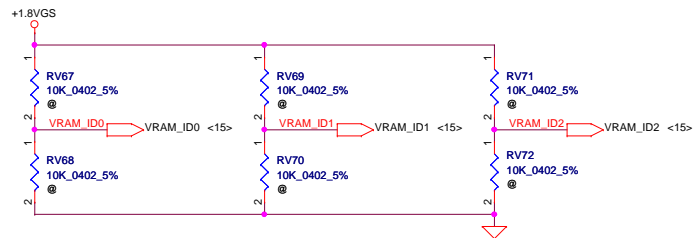
	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45k	2k
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75k
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75k
PS_3[5:1]	1 1	0 0 0	NC	NC	4.75k



VRAM Straps		! "#\$% "	"#\$% "	"#\$% "	
64MX16 (1G)	H5TG63DFR-11C				
64MX16 (1G)	K4W1G1648G-BC11		0	0	1
* 128M16 (2G)	H5TQ2G63BFR-11C		1	0	1
* 128M16 (2G)	K4W2G1648C-HC11		0	1	1
			1	1	1



Modify VRAM Straps different from AMD platform (Because BIOS team want to Common VBIOS, Separate VRAM Straps could be easily control VRAM if AMD & Intel have different VRAM turning setting)



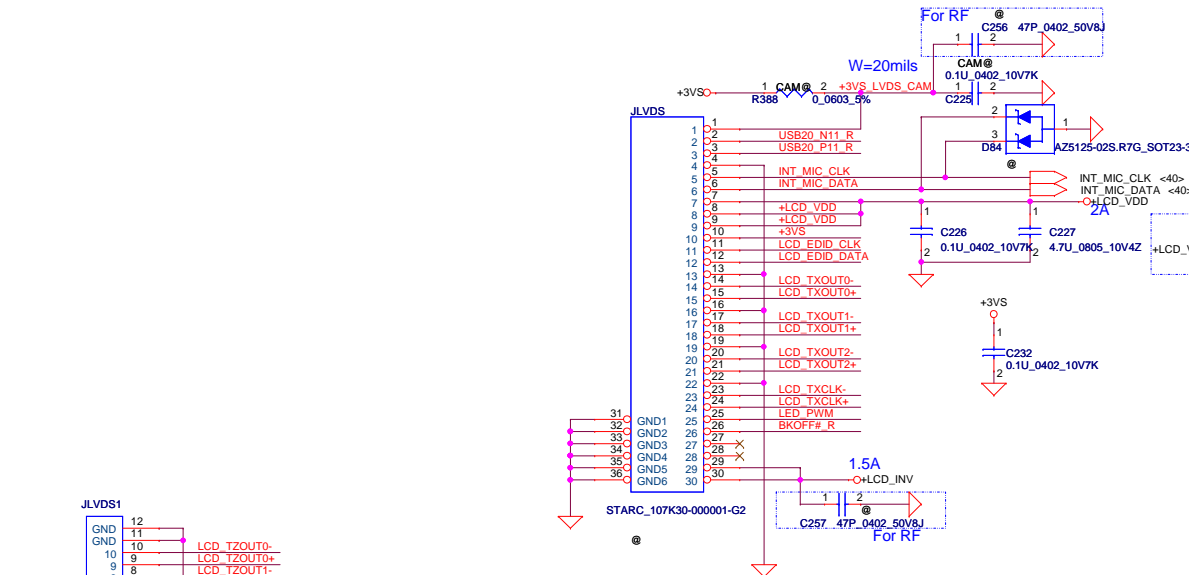
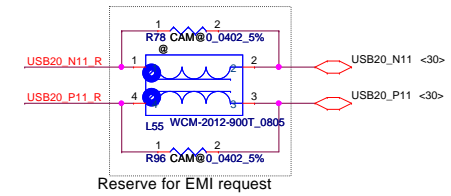
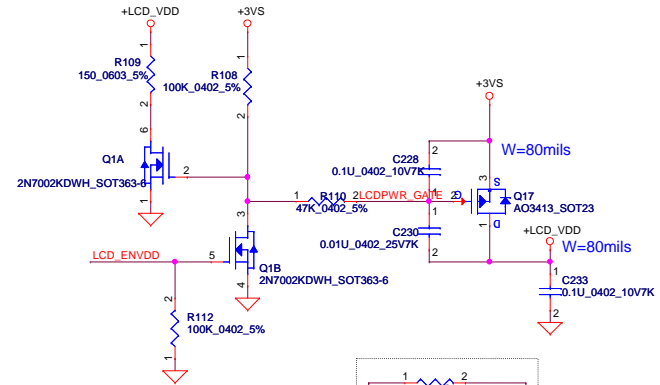
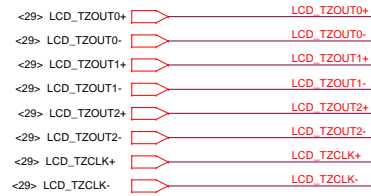
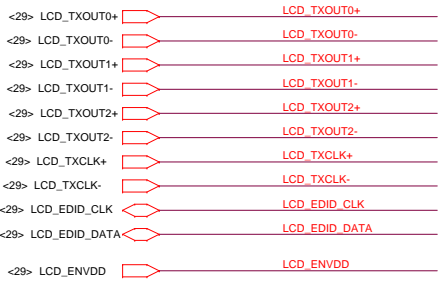
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

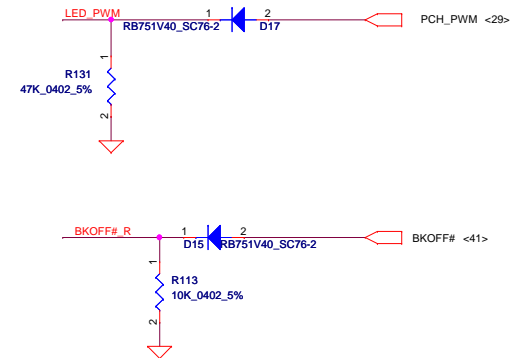
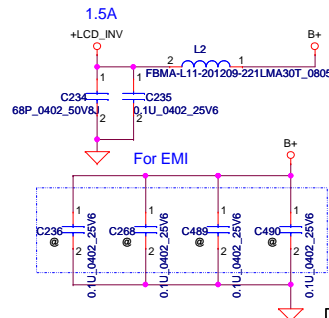
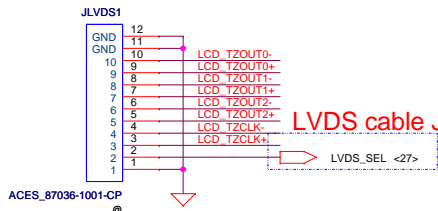
RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 10K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

MLPS Bit	STRAPS	Conventional Pin Strap Equivalent	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
PS_0[3:1]	ROMIDCFG(2:0)	GPIO[13:11]	Memory aperture size select 256MB: 0 0 1	0 0 1
PS_0[4]	N/A	GENLK_VSYNC	Must be 1 at rest. (Chelsea PRO)	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO2	PCIe Gen3 capability 0: 2.5GT/s 1: 5GT/s	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO8	PCIe clock power management capability.	0
PS_1[3]	N/A	GENLK_CLK	Must be 0 at rest. (Chelsea PRO)	0
PS_1[4]	TX_PWRS_ENB	GPIO0	PCIe full TX output swing 0: Half swing 1: Full swing	1
PS_1[5]	TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enable 0: Disable 1: Enable	1
PS_2[1] PS_2[2]	N/A	N/A	Reserved	N/A
PS_2[3]	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM 0: Disable 1: Enable	0
PS_2[4]	VGA DIS	GPIO9	VGA disable 0: Enable 1: Disable	0
PS_2[5] PS_3[3:1]	N/A	N/A	Reserved	N/A
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	N/A	Audio-capable display outputs 0 0 0 All endpoints are usable 1 1 1 No usable endpoints.	1 1 1
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]			
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]			
AUD[1]	HSYNC		AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0
AUD[0]	VSYNC			
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET				
GPIO21 H2SYNC GENERICC GPIO2 GPIO8				

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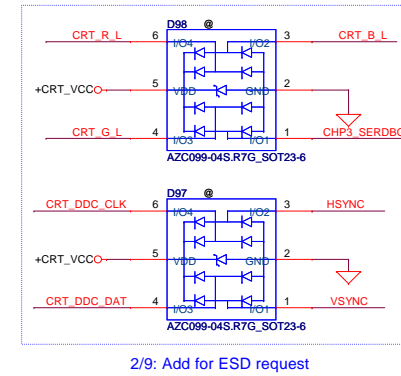
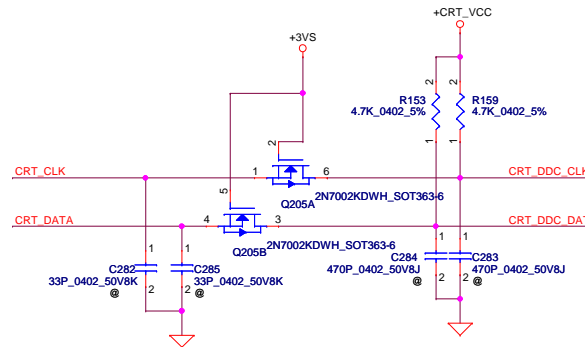
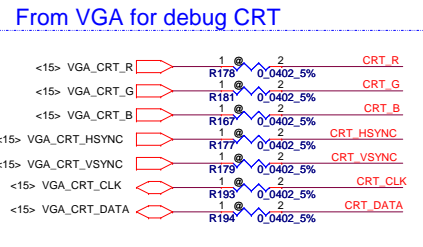
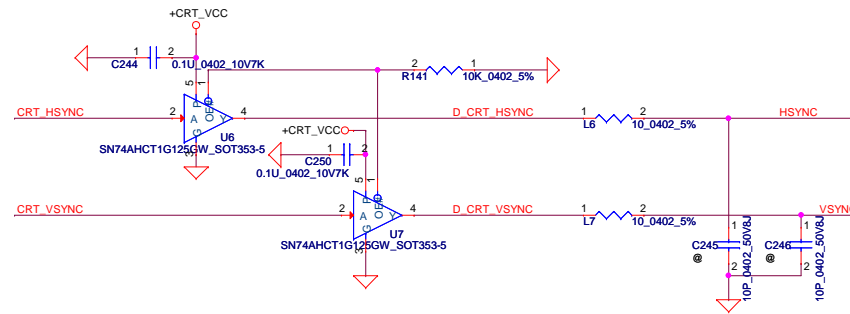
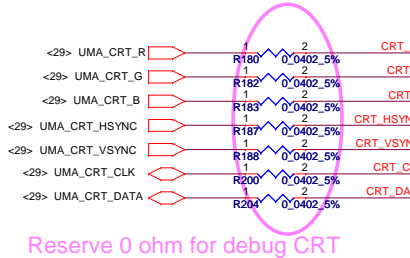
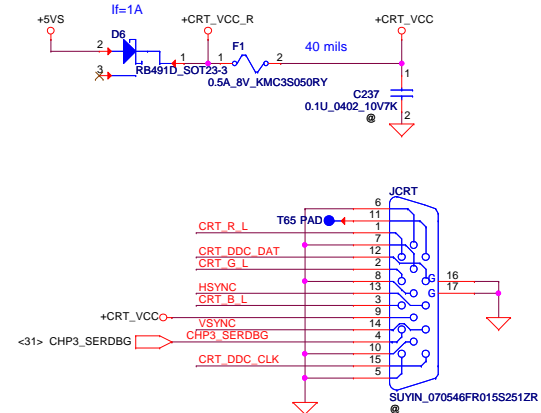
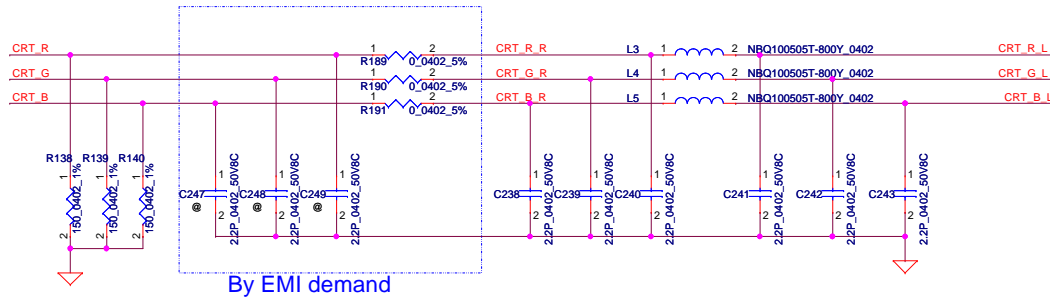


LVDS cable JLVDS1.2 need to contact GND



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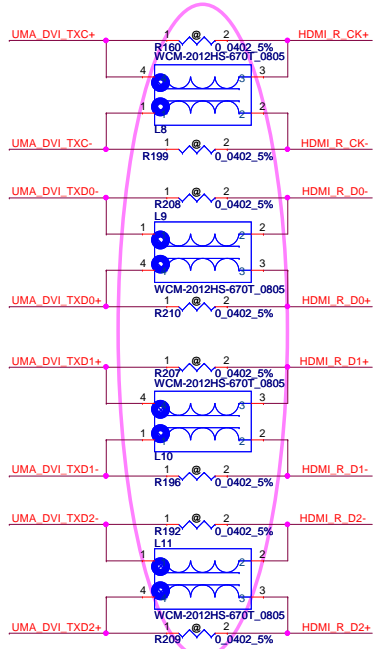
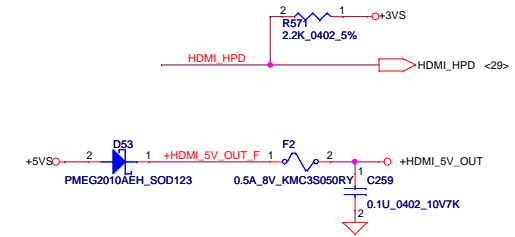
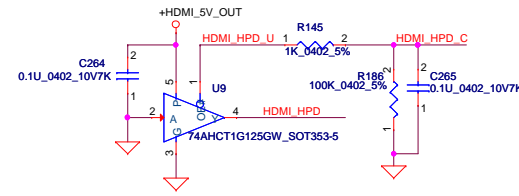
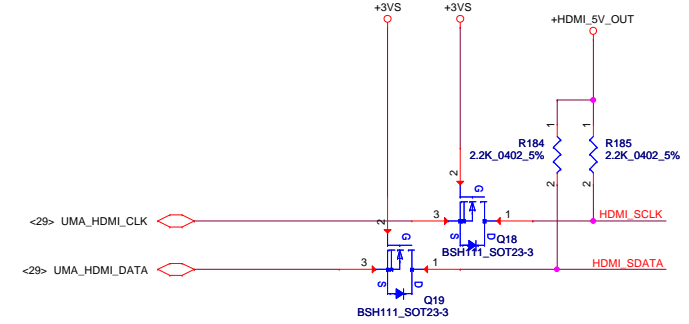
CRT CONNECTOR



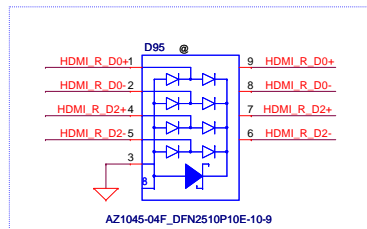
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Issued Date	2011/11/11	Deciphered Date	2012/12/31	CRT	
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				QCLA4 LA-8861P M/B	0.2
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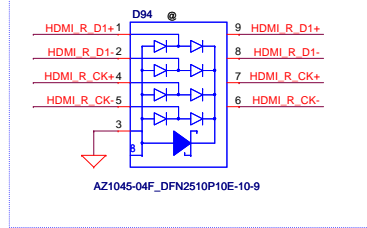
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<29>	UMA_HDMI_TXC-	CV337	1	2	0.1U_0402_10V7K	UMA_DVI_TXC-
<29>	UMA_HDMI_TX0+	CV338	1	2	0.1U_0402_10V7K	UMA_DVI_TXD0+
<29>	UMA_HDMI_TX0-	CV339	1	2	0.1U_0402_10V7K	UMA_DVI_TXD0-
<29>	UMA_HDMI_TX1+	CV340	1	2	0.1U_0402_10V7K	UMA_DVI_TXD1+
<29>	UMA_HDMI_TX1-	CV341	1	2	0.1U_0402_10V7K	UMA_DVI_TXD1-
<29>	UMA_HDMI_TX2+	CV342	1	2	0.1U_0402_10V7K	UMA_DVI_TXD2+
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change to 67ohm

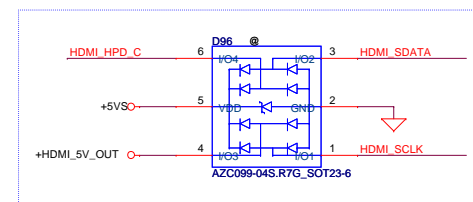


AZ1045-04F_DFN2510P10E-10-9



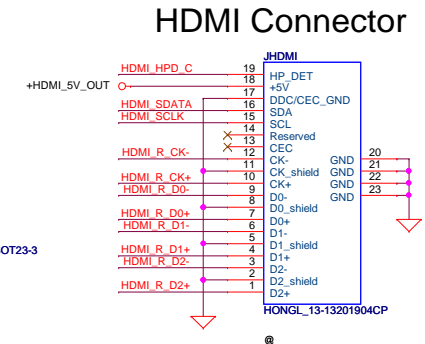
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2/9: Add for ESD request



AZC099-04S.R7G_SOT23-6

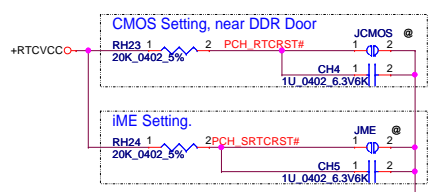
2/9: Add for ESD request



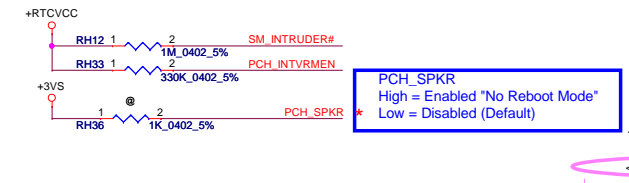
HDMI Connector

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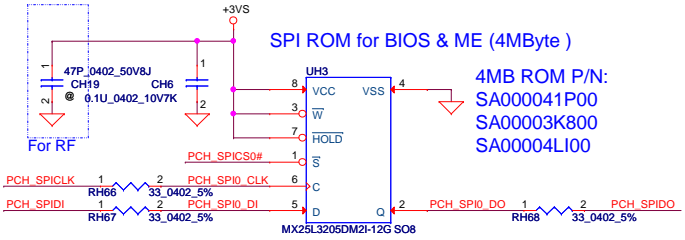
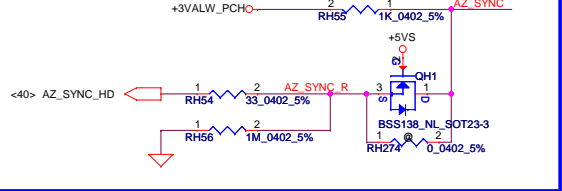


Integrated SUS 1.05V VRM Enable
 PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

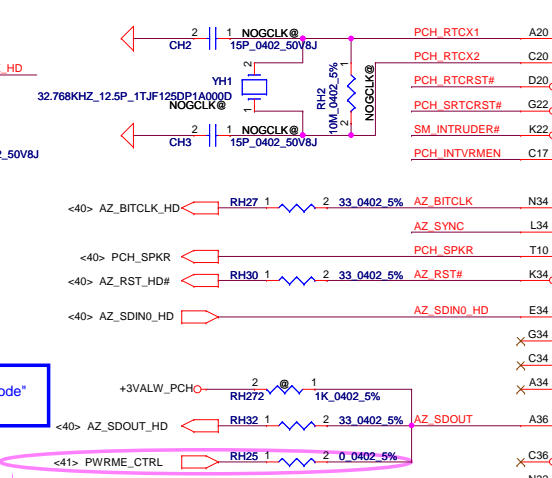


ME debug mode, this signal has a weak internal pull down
 * Low = Disable (default)
 High = Enable (flash descriptor security override)

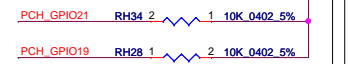
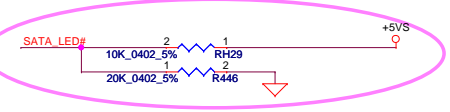
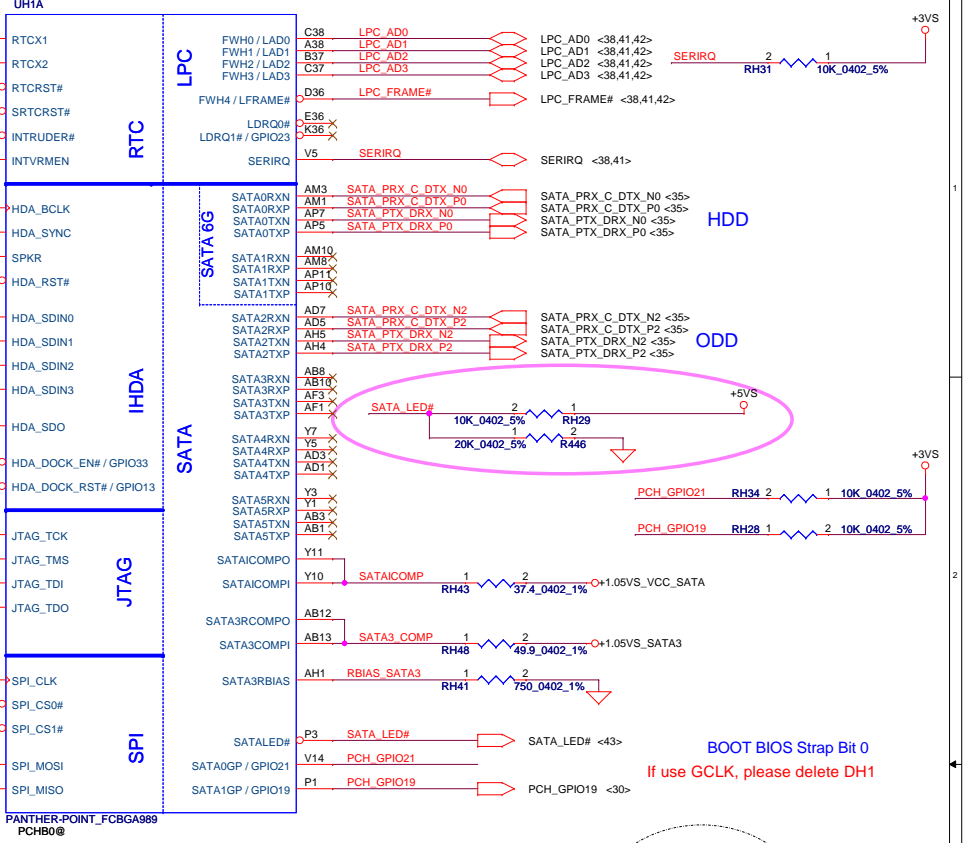
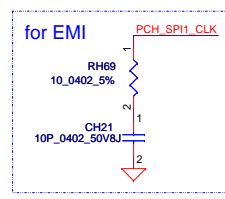
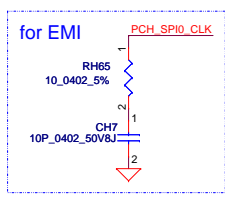
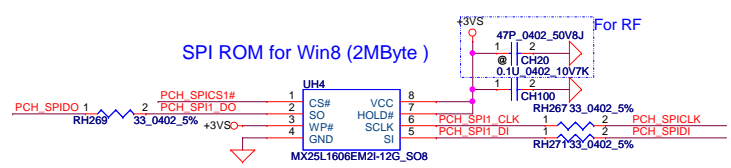
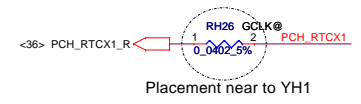
* This signal has a weak internal pull down
 H=>On Die PLL is supplied by 1.5V
 L=>On Die PLL is supplied by 1.8V
 Need to pull high for Chief River Mobile platform



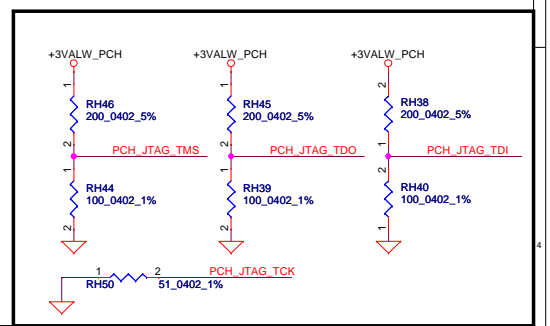
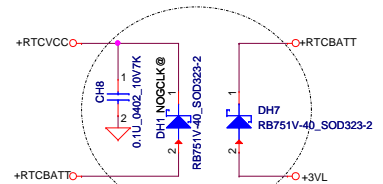
Socket: SP07000F500/SP07000H900
 Please place U13 & U4 close to U2 PCH, please place RH66, RH67, RH68 near UH3
 Please place RH267 near RH66, Please place RH271 near RH67, Please place RH269 near RH68.



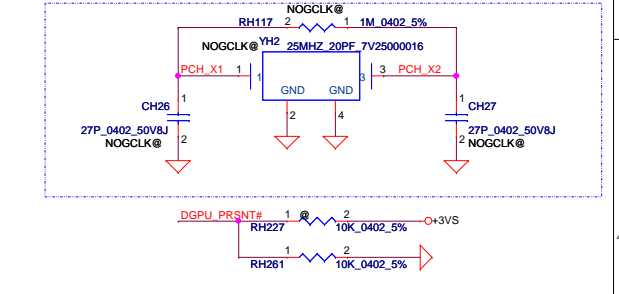
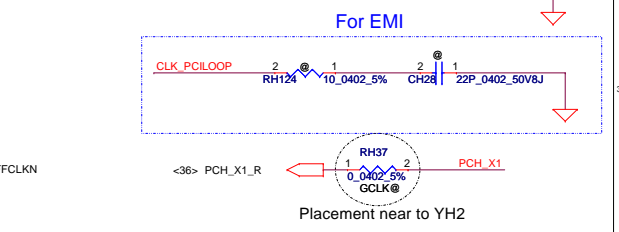
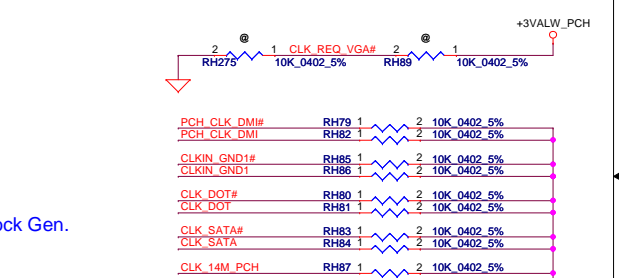
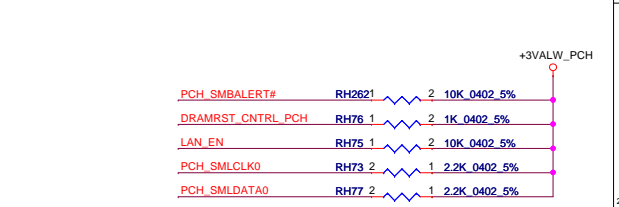
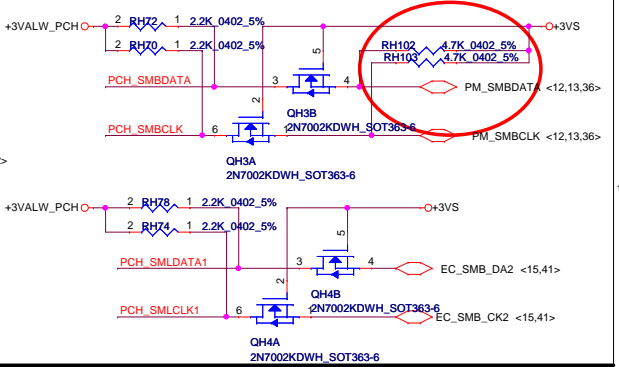
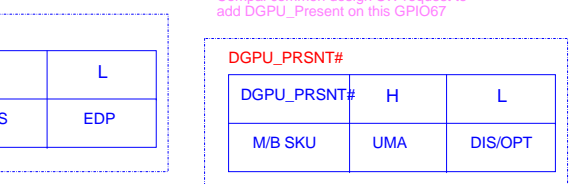
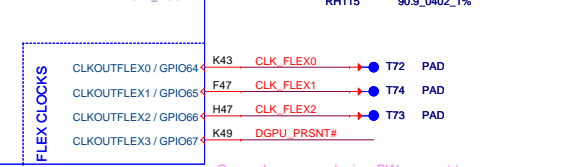
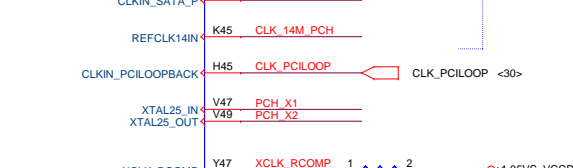
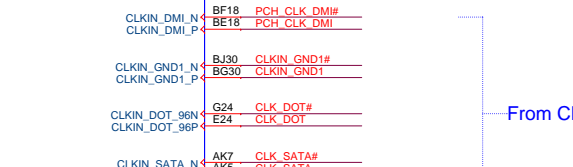
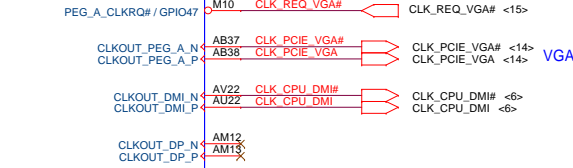
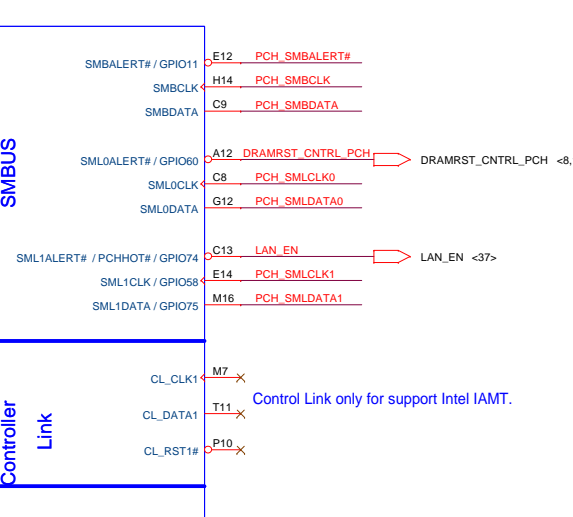
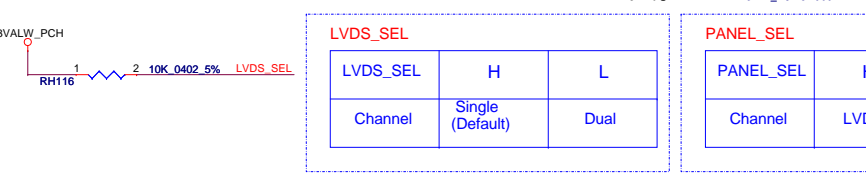
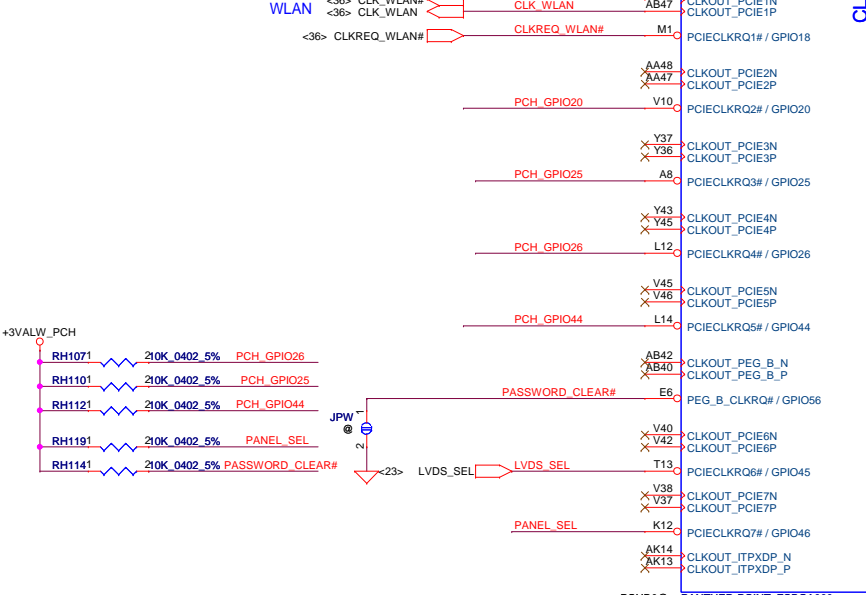
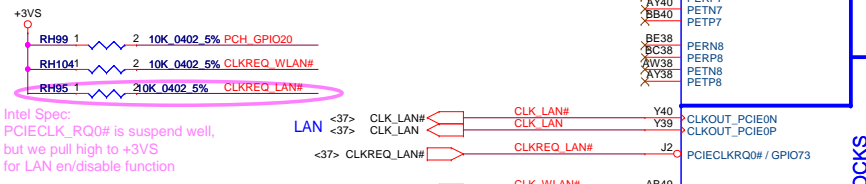
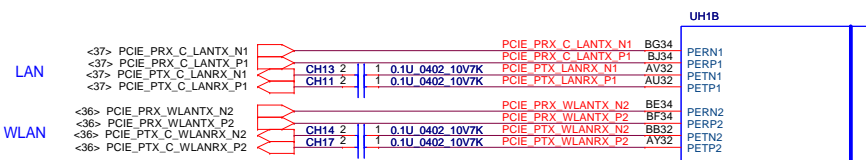
Change Net name due to this function is high active



BOOT BIOS Strap Bit 0
 If use GCLK, please delete DH1

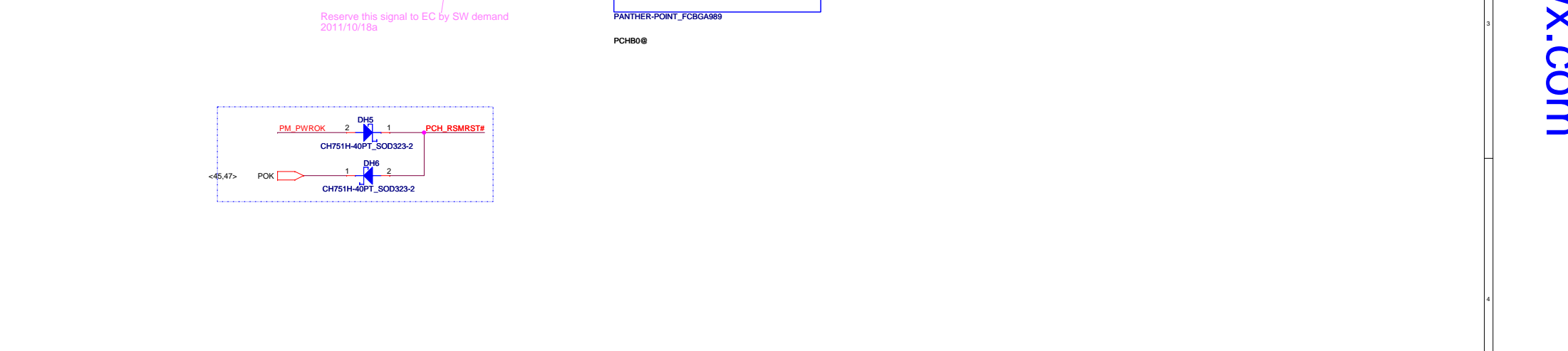
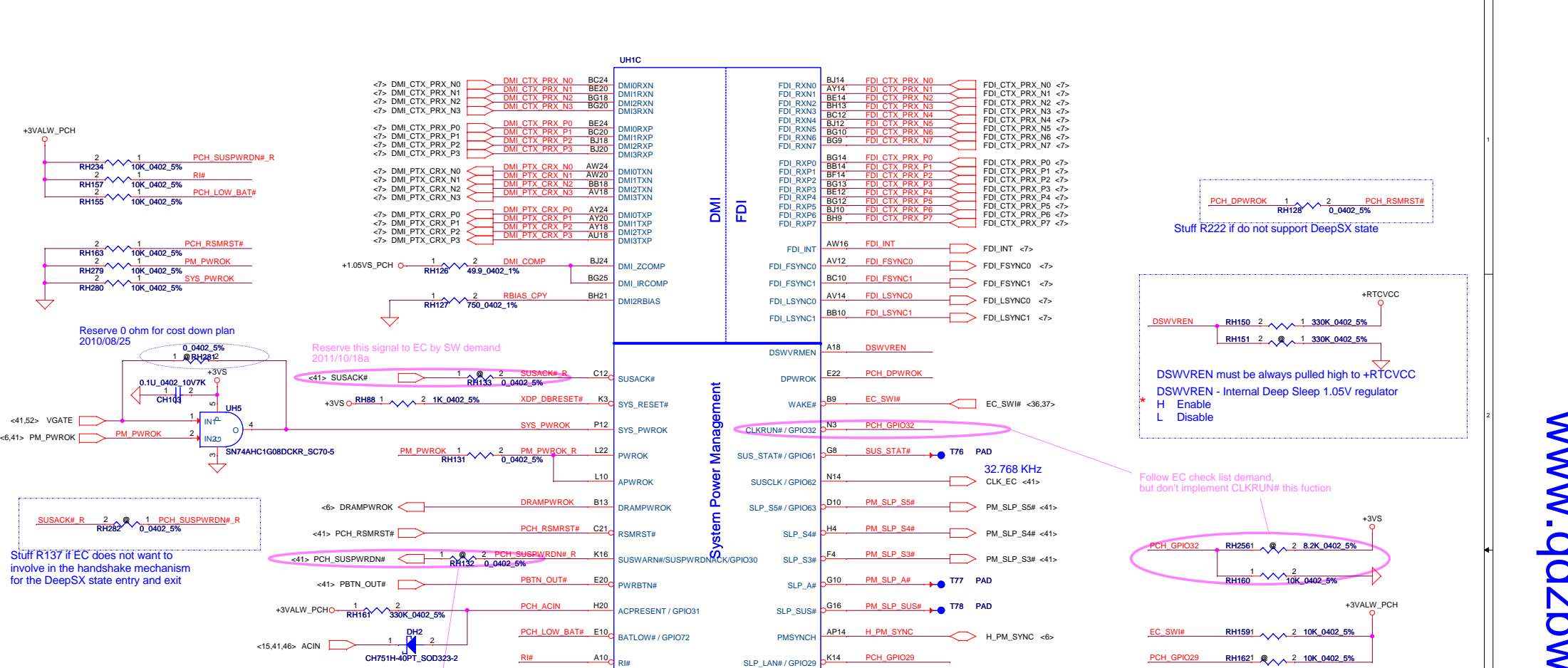


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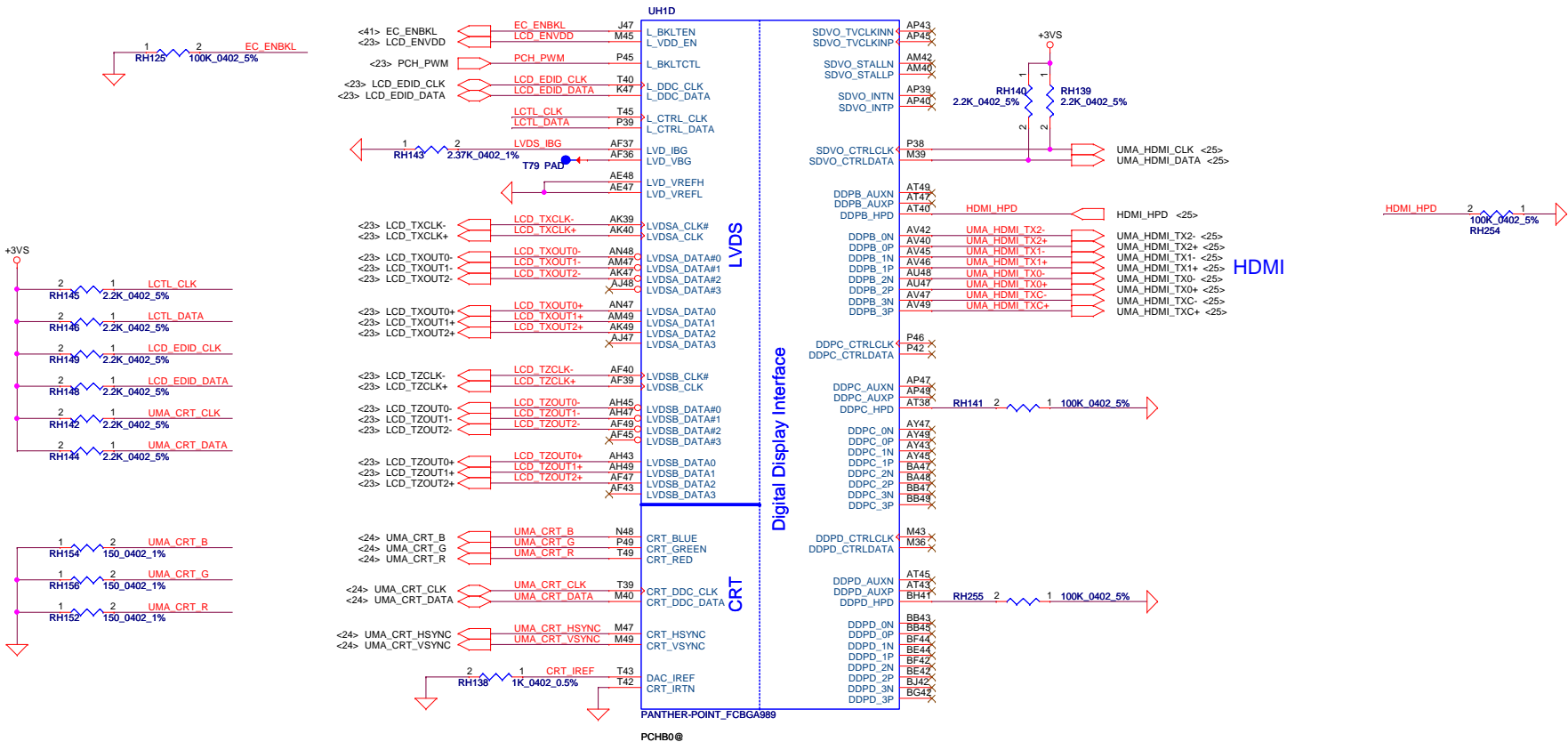
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Issued Date	2011/11/11	Deciphered Date	2012/12/31	PCH_PCI-E/SMBUS/CLK	
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				QCLA4 LA-8861P M/B	0.2
				Date: Tuesday, February 14, 2012	Sheet 27 of 58



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				PCH_DMI/FDI/PM
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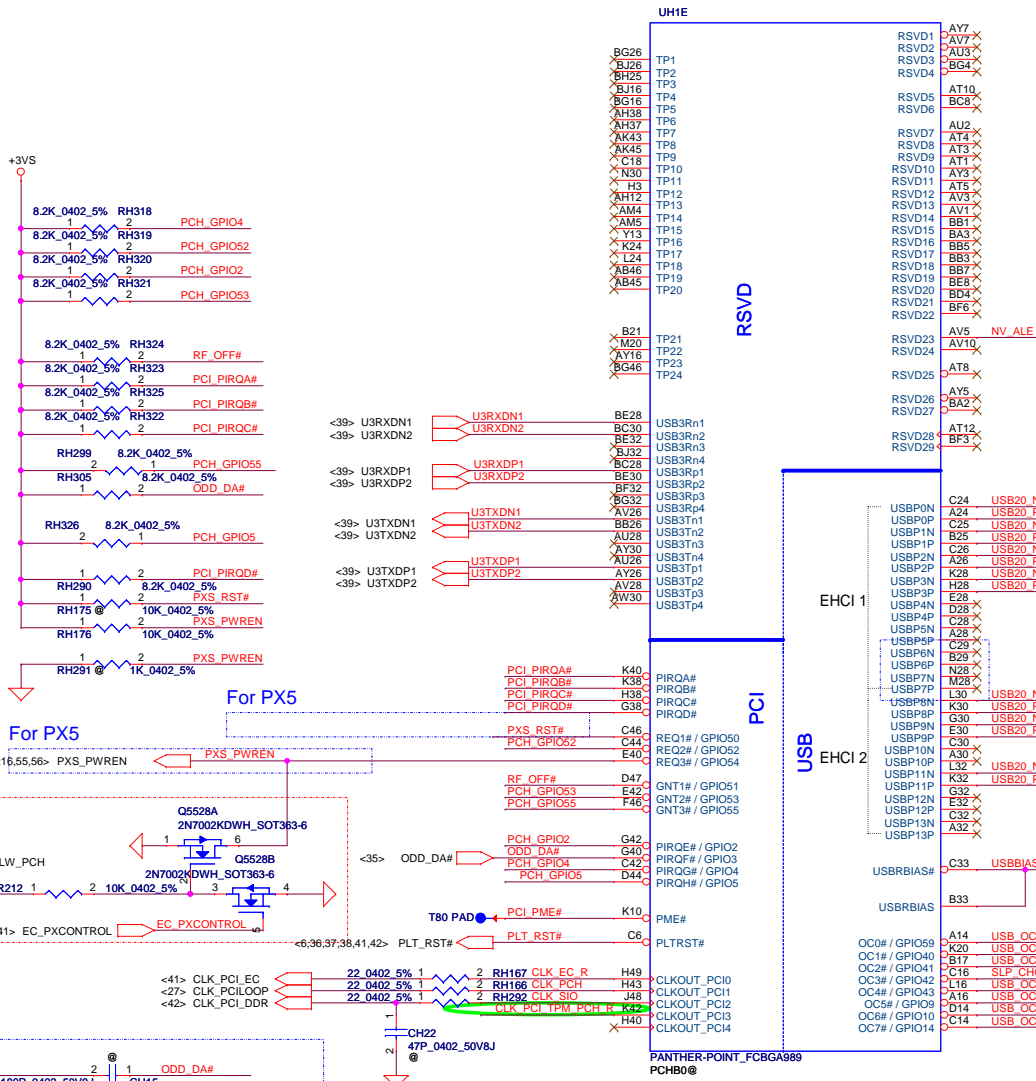
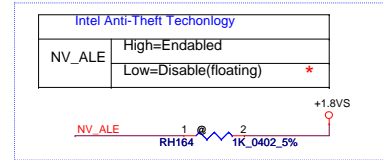
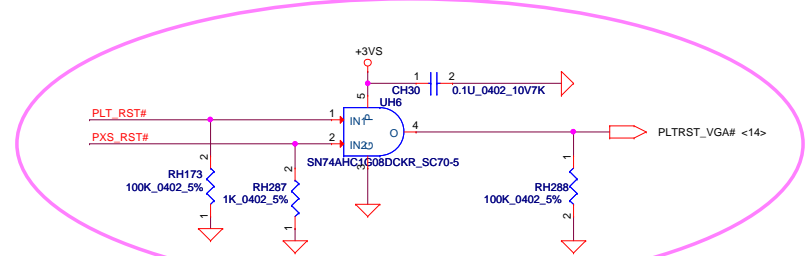
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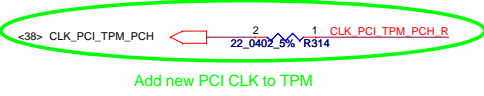
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/11	Deciphered Date	2012/12/31	Title
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				Rev
				0.2
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For PX5



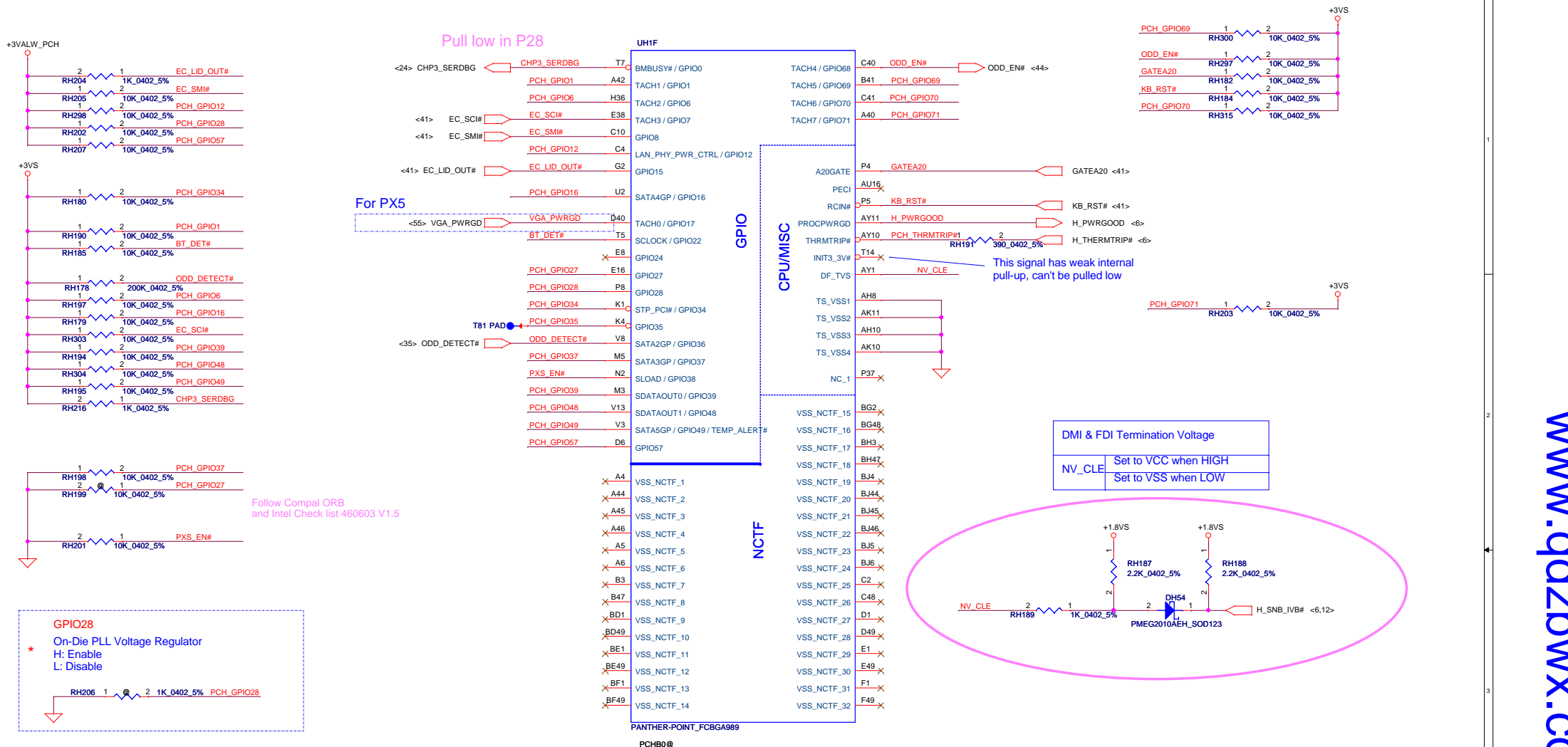
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

WL_OFF#	Low=A16 swap override Enable	High=A16 swap override Disable
*		



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Pull low in P28

For PX5

This signal has weak internal pull-up, can't be pulled low

DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW

Follow Compal ORB and Intel Check list 460603 V1.5

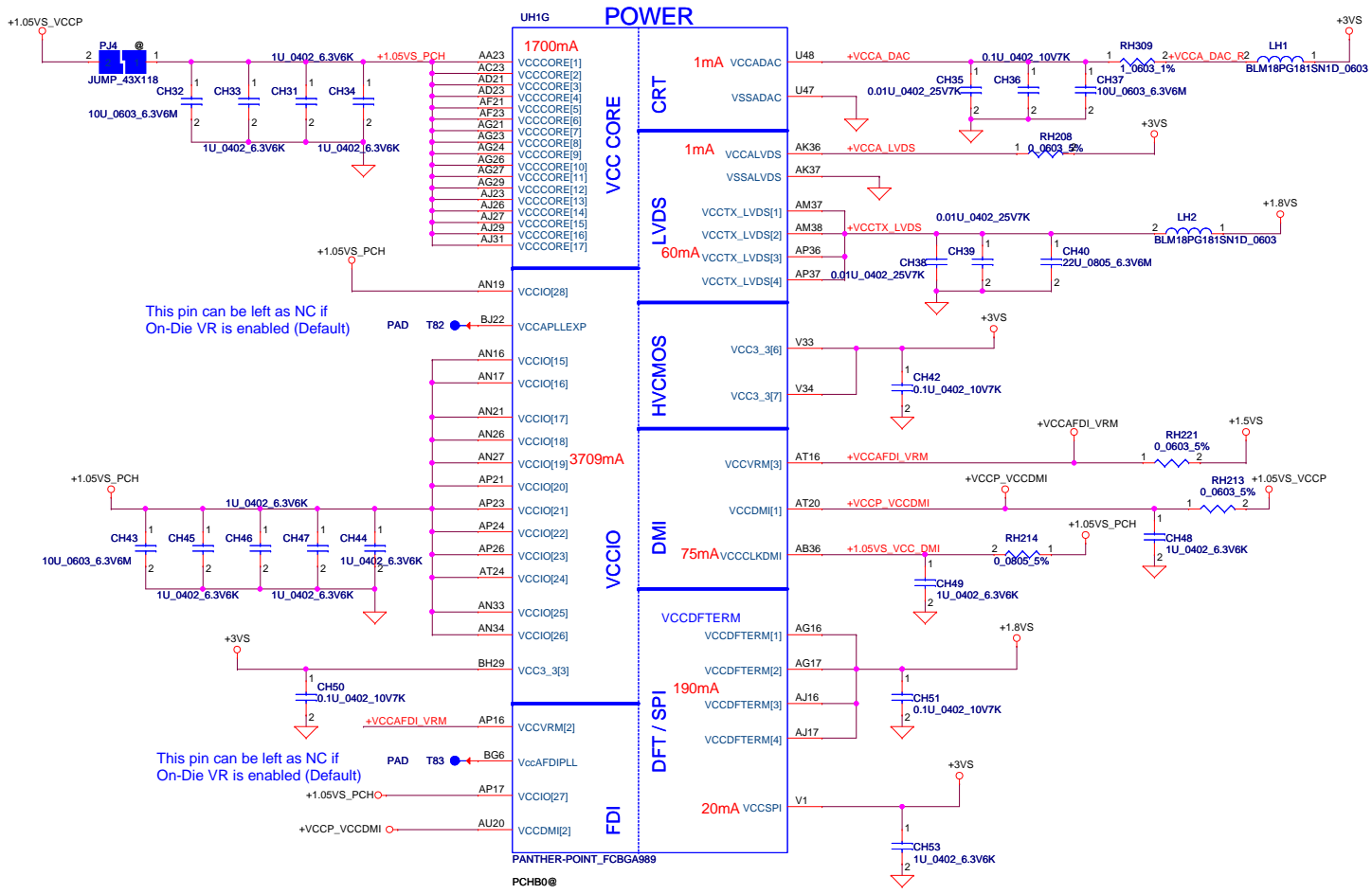
GPIO28
On-Die PLL Voltage Regulator
H: Enable
L: Disable

GPIO8
Integrated Clock Chip Enable (Removed)
H: Disable
L: Enable

Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

PXS_EN#

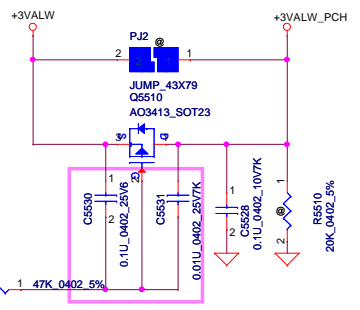
PXS_EN#	H	L
SKU	NonPXS	PXS



This pin can be left as NC if On-Die VR is enabled (Default)

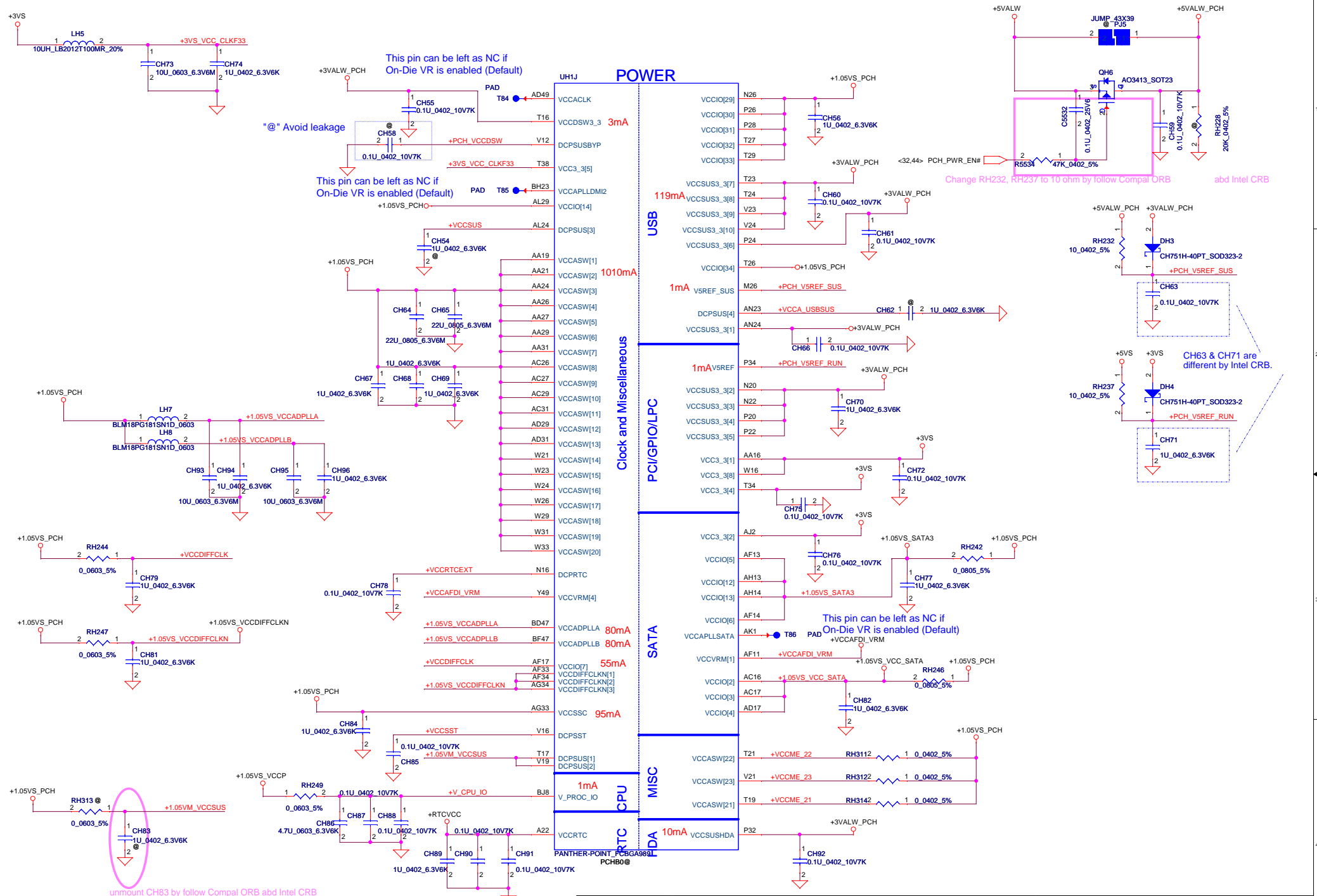
This pin can be left as NC if On-Die VR is enabled (Default)

+3VALW to +3V_PCH



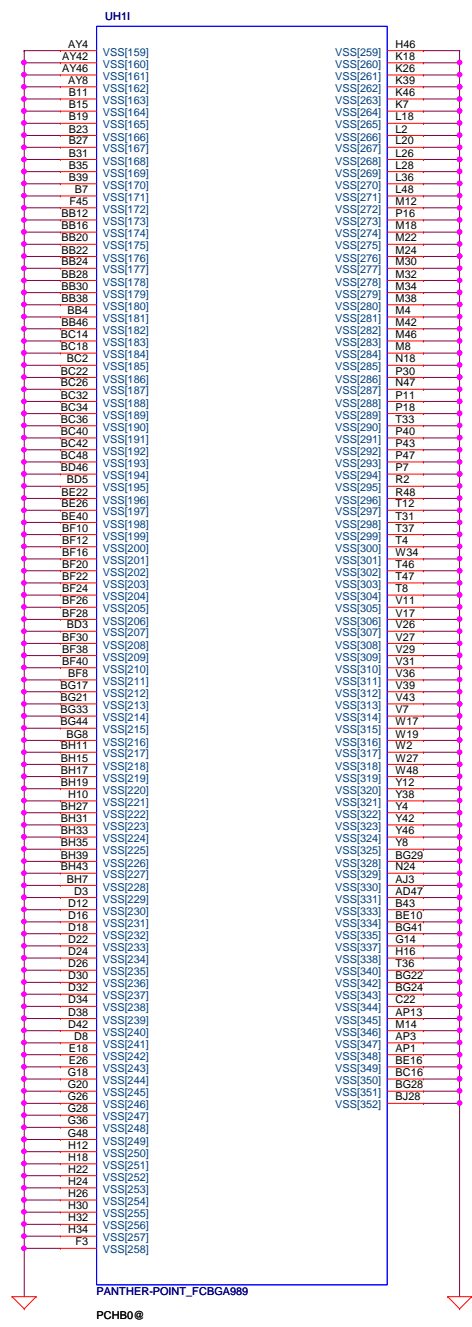
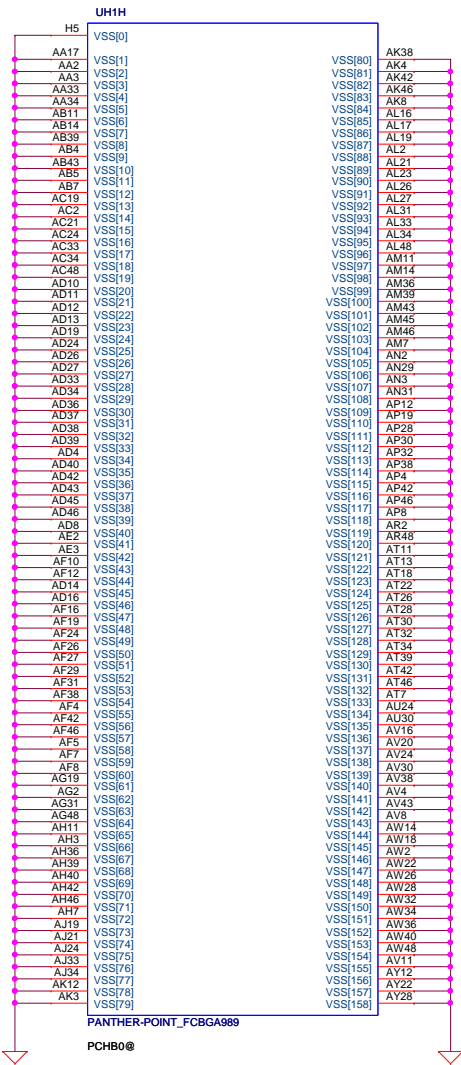
PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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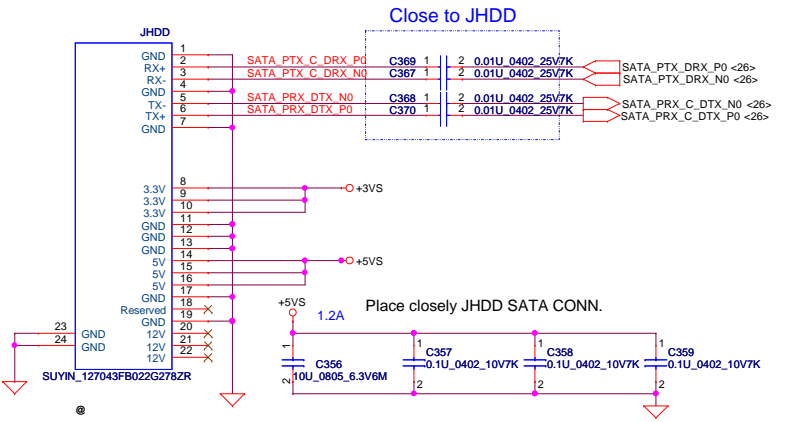
www.pdzpwx.com



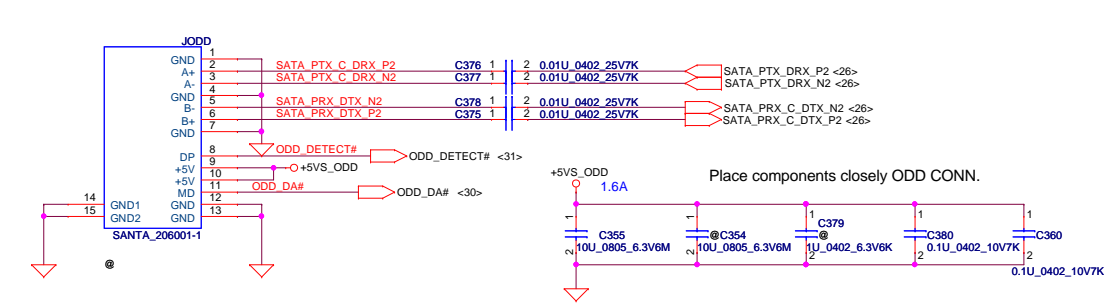
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Issued Date	2011/11/11	Deciphered Date	2012/12/31	PCH_GND	
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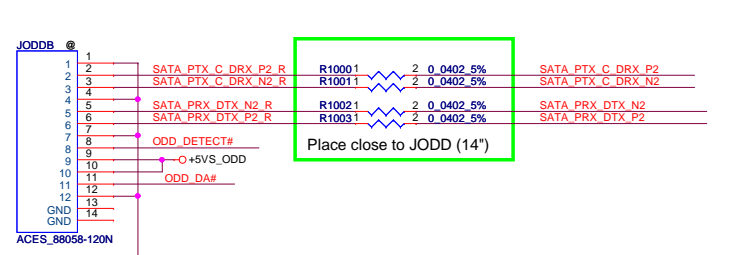
SATA HDD Conn.



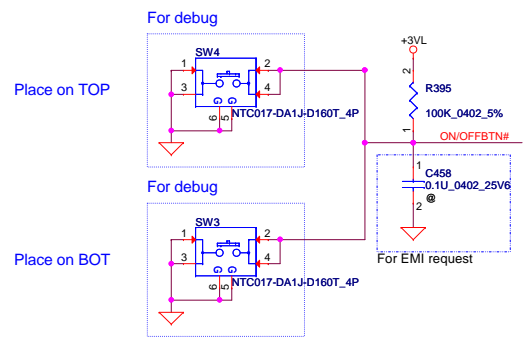
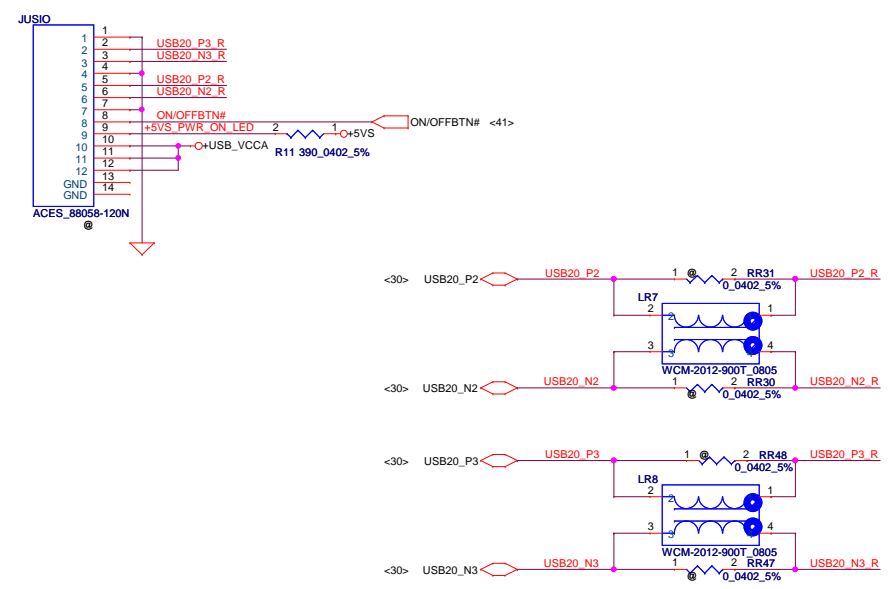
SATA ODD Conn



SATA ODD Conn (for 15')



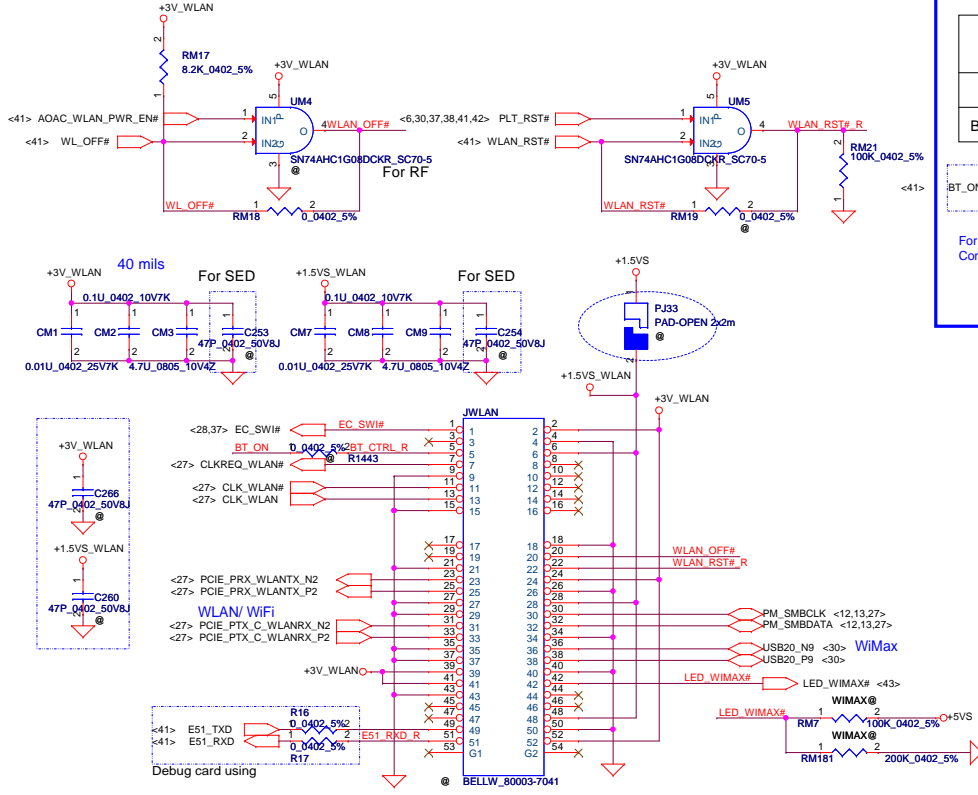
Power Button & RUSB connector



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				SATA-HDD/ODD/USB
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Slot 1 Half PCIe Mini Card-WLAN/ WiMax

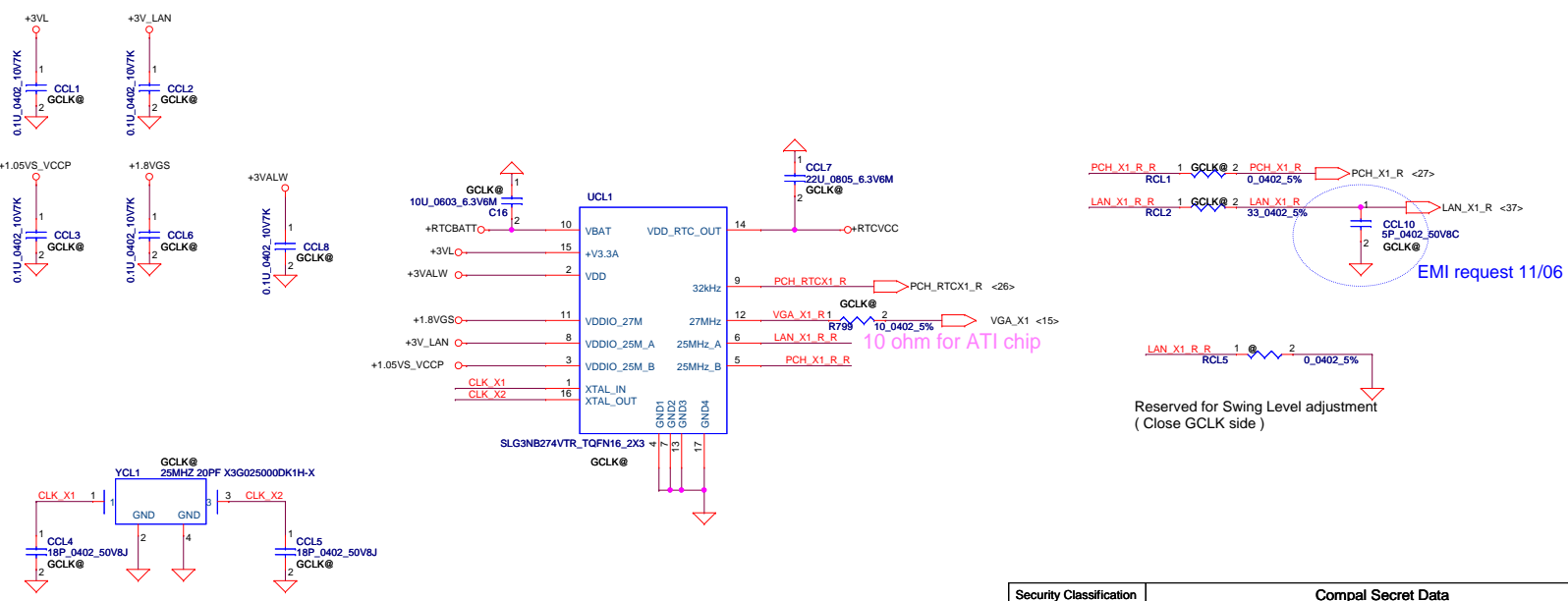
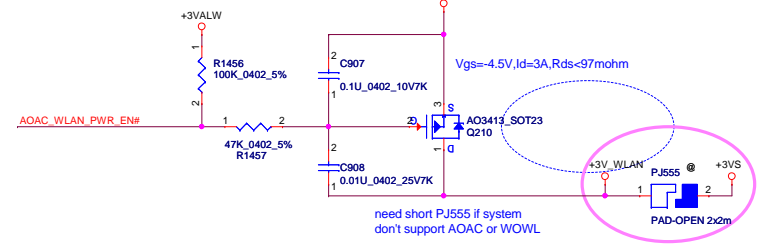


WLAN&BT Combo module circuits

	BT on module	BT on module
	Enable	Disable
BT_ON#	H	L

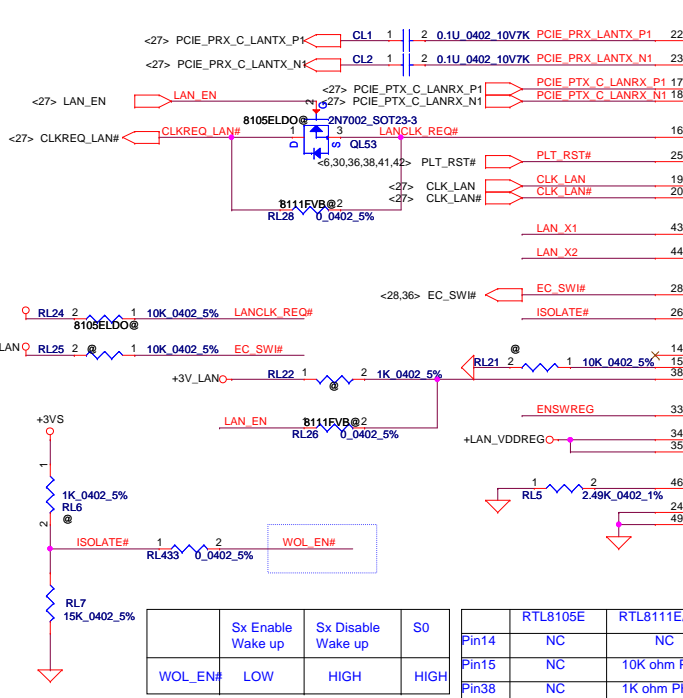
For isolate Intel Rainbow Peak and Compal Debug Card.

+3VALW TO +3V_WLAN for AOAC and WOWL

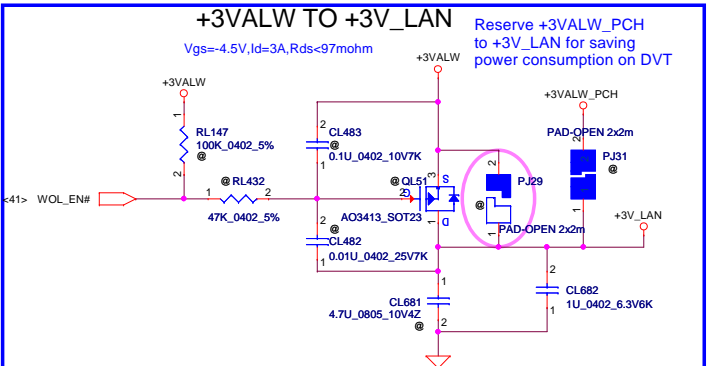
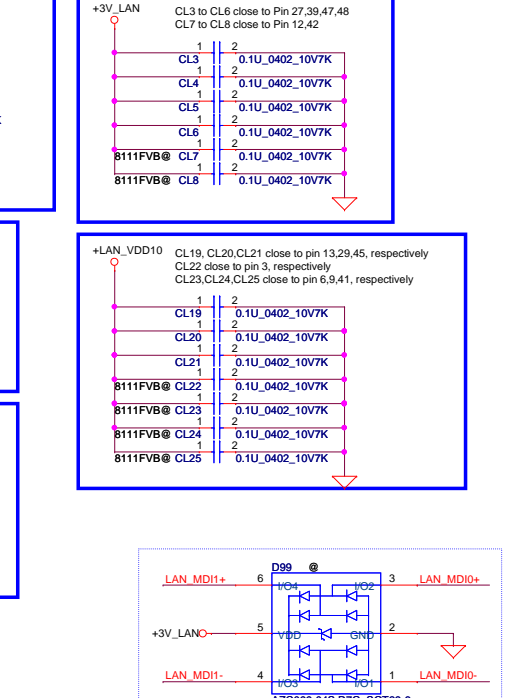
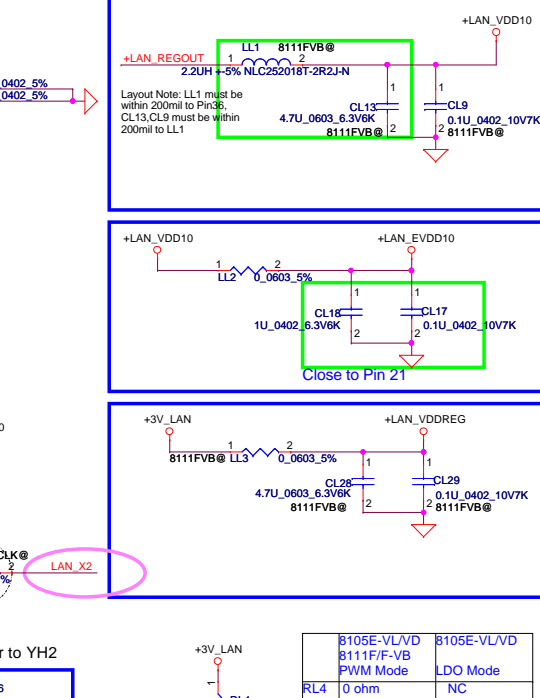
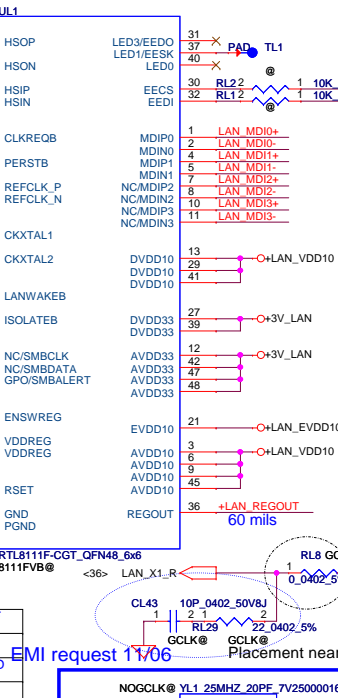


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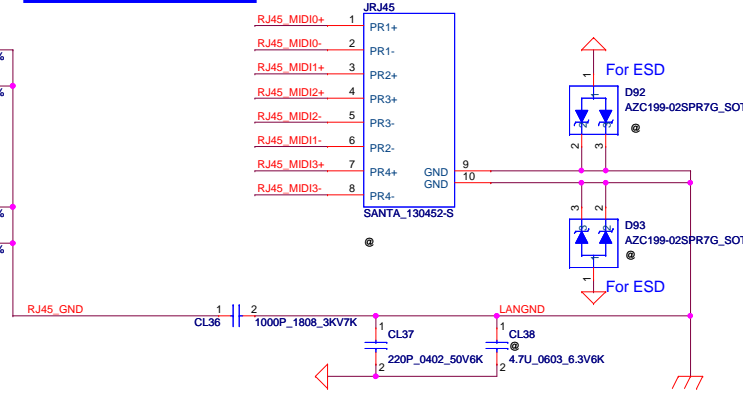
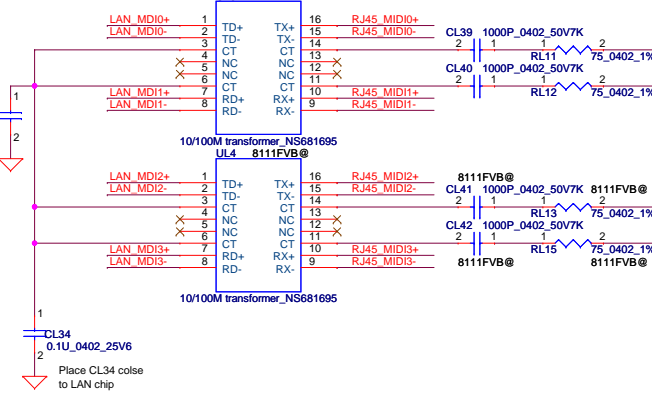
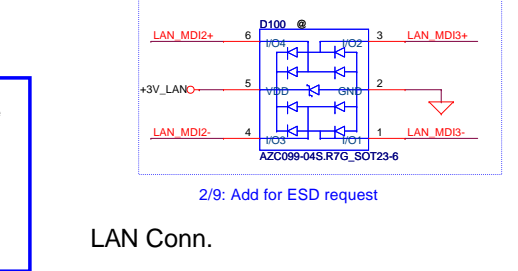
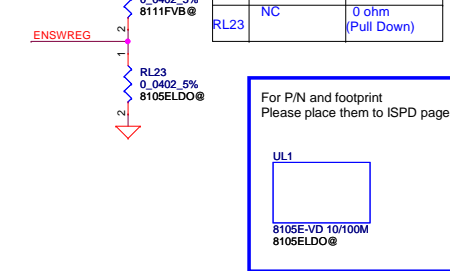
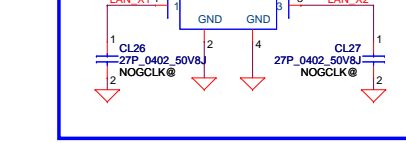
Sx Enable	Sx Disable	S0	RTL8105E	RTL8111E/F
WOL_EN#	LOW	HIGH	NC	NC
			Pin14	Pin15
			NC	10K ohm PD
			Pin38	1K ohm PH



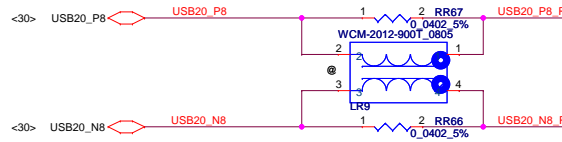
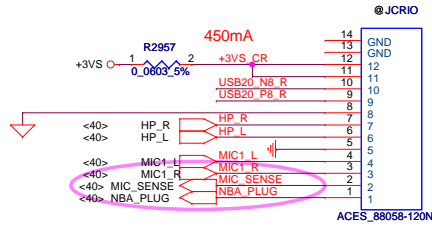
+3V_LAN rising time (10%-90%) need > 1ms and < 100μs.

LAN	WOL	LAN_EN	ISOLATEB
S0	Sx	S0	Sx
0	0	0	1
0	1	0	0
1	0	1	1
1	1	1	1
1	1	1	0*

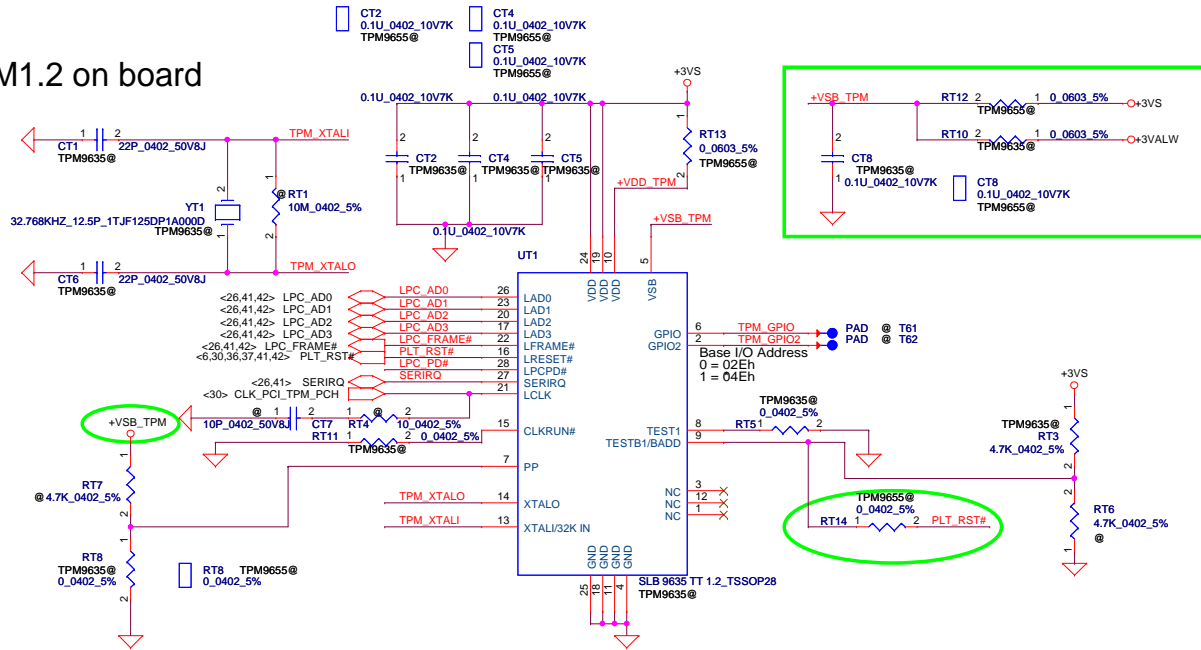
* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



CardReader Conn.

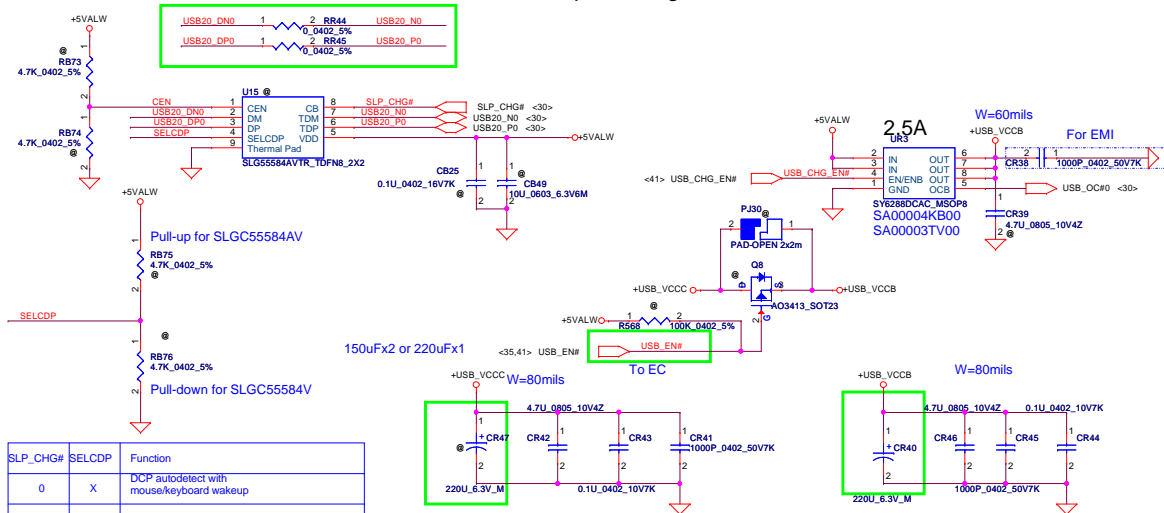


TPM1.2 on board

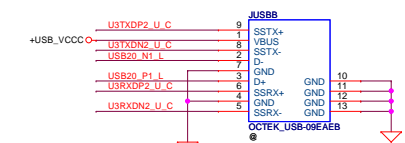
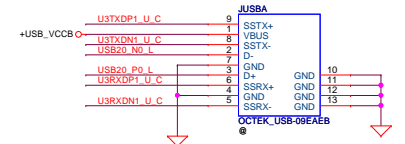
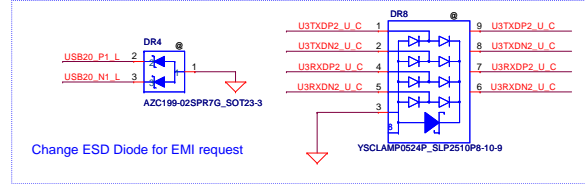
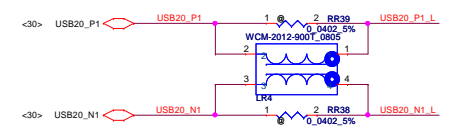
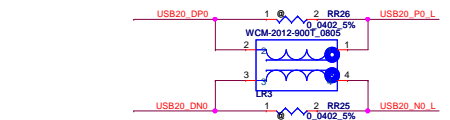
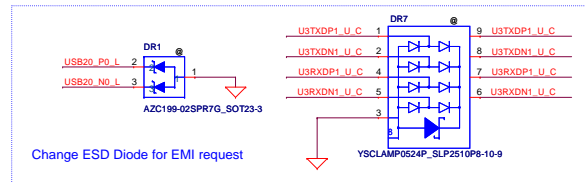


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				USB-CardReader RTS5129/TPM
				QCLA4 LA-8861P M/B
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Sleep & Charge Function

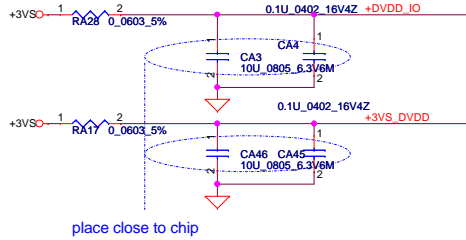


150uFx2 or 220uFx1

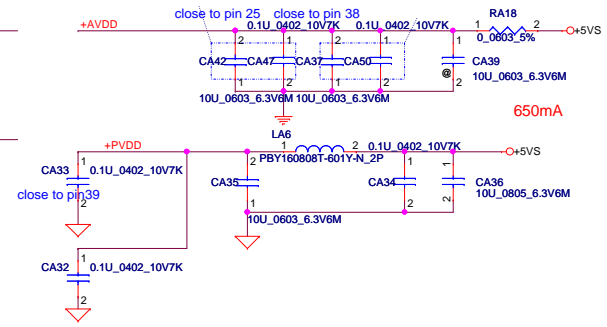


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		PCIE-USB3.0 connector		
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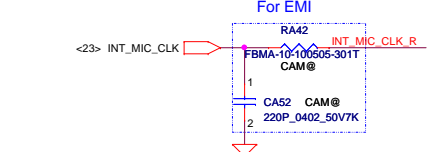
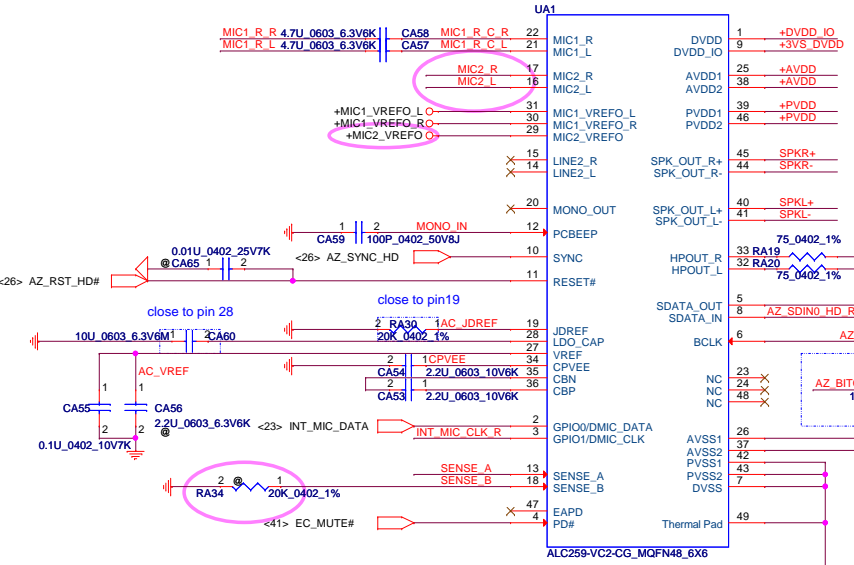
35mA for 3.3V level



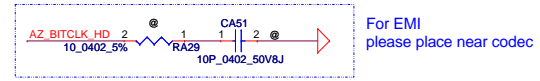
place close to chip



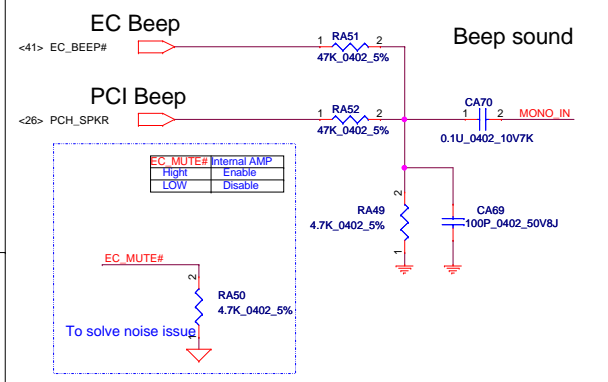
650mA



For EMI



For EMI please place near codec



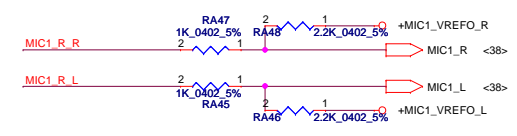
EC Beep

Beep sound

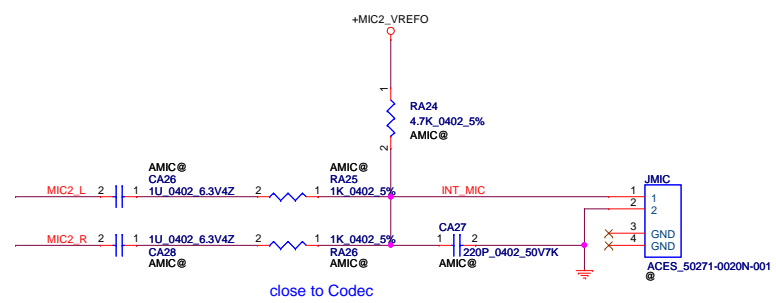
PCI Beep

EC MUTE#	Internal AMP
High	Enable
LOW	Disable

Ext.MIC/LINE IN JACK

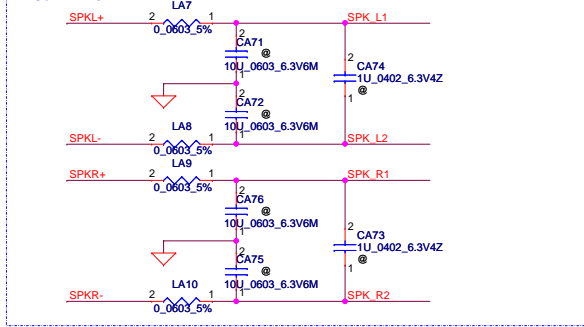


Analog MIC

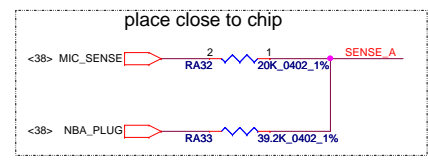


close to Codec

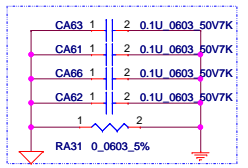
placement near Audio Codec



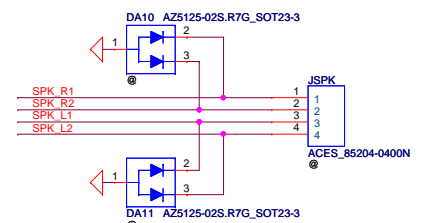
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

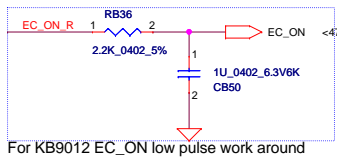
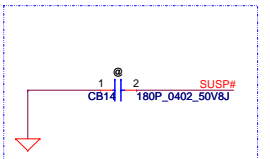
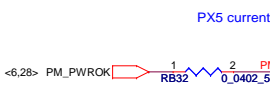
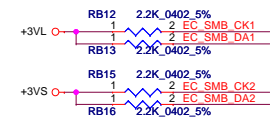
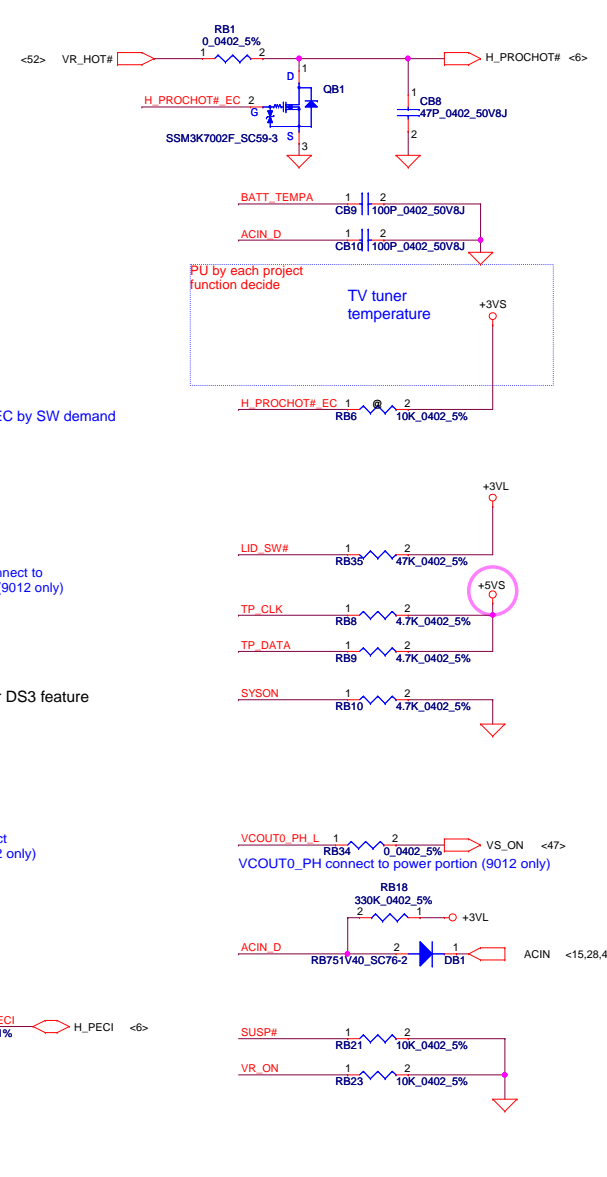
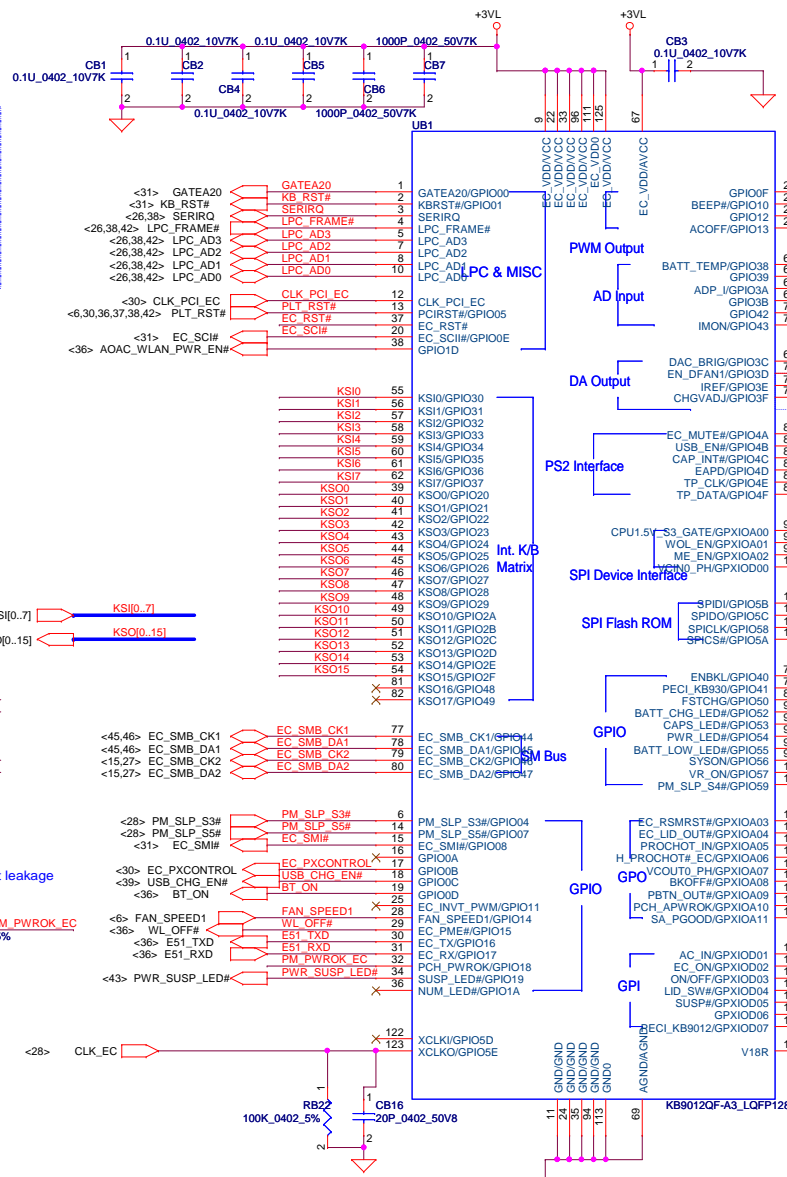
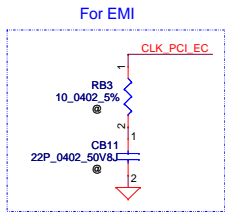


place close to chip



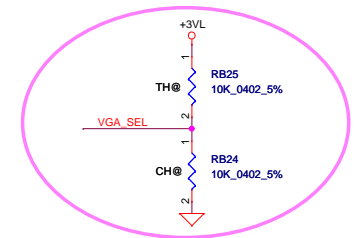
SPK Conn.





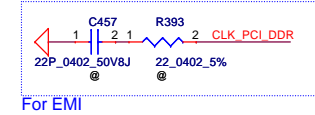
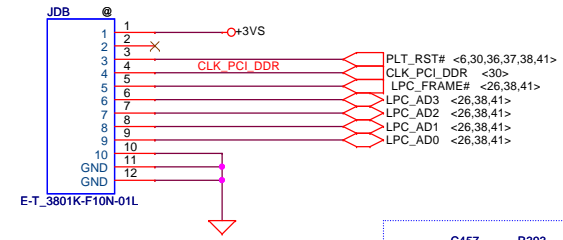
Voltage Comparator Pins FOR 9012 A3

VGIN0 pin109	>1.2V	<1.2V
VGIN1 pin102		
VCOU0 pin104	HIGH	LOW
VCOU1 pin103	LOW	HIGH

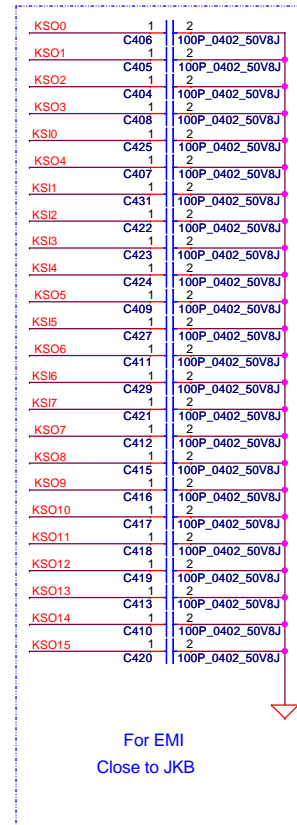
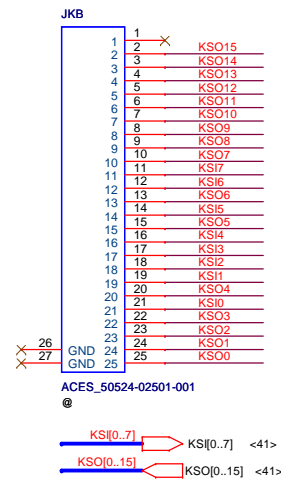


VGA_SEL (for thermal sensor)	High	Low
Pin117	Thames	Chelsea
Address	82h	9Ah

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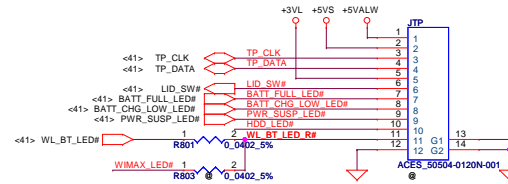


KEYBOARD CONN.

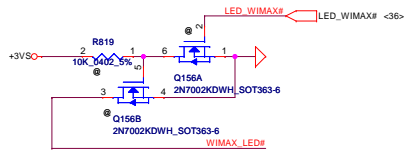


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Size	Document Number	QCLA4 LA-8861P M/B		Rev
Date:	Tuesday, February 14, 2012	Sheet	42 of 58	0.2

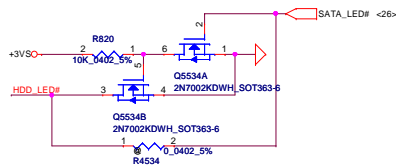
Touchpad Connector



WiMAX LED



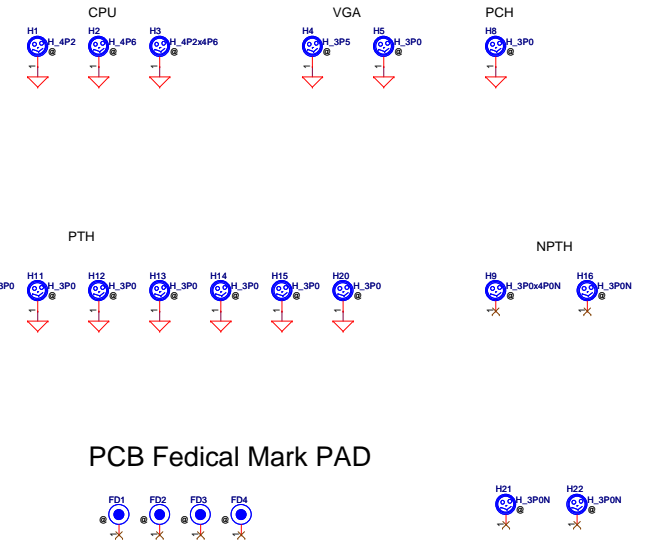
SATA LED



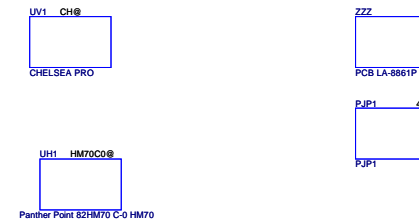
ESD solution

EMI solution

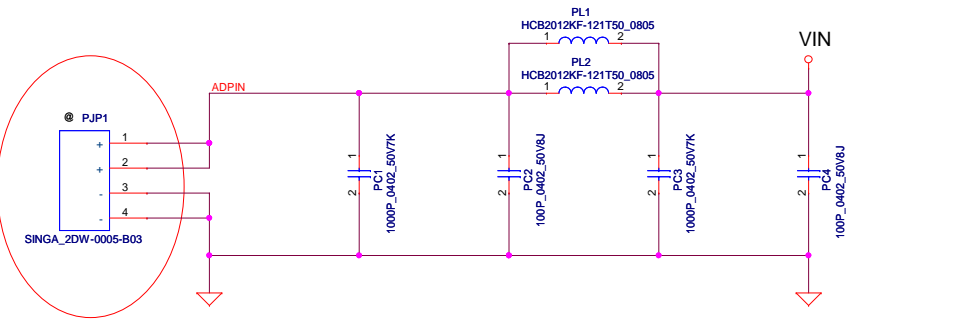
Screw Hole



ISPD

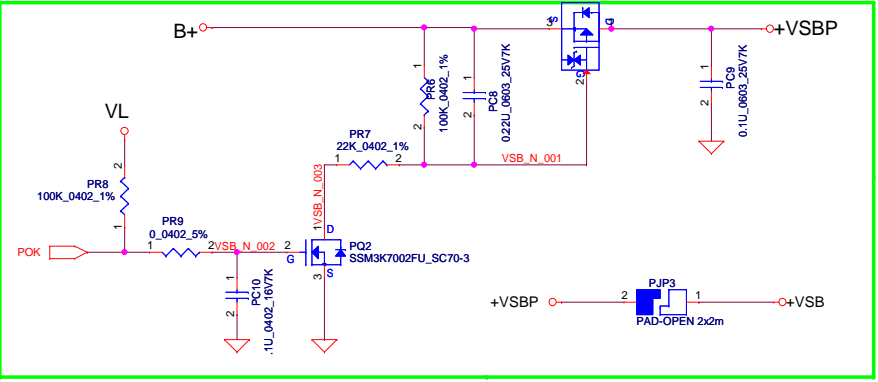
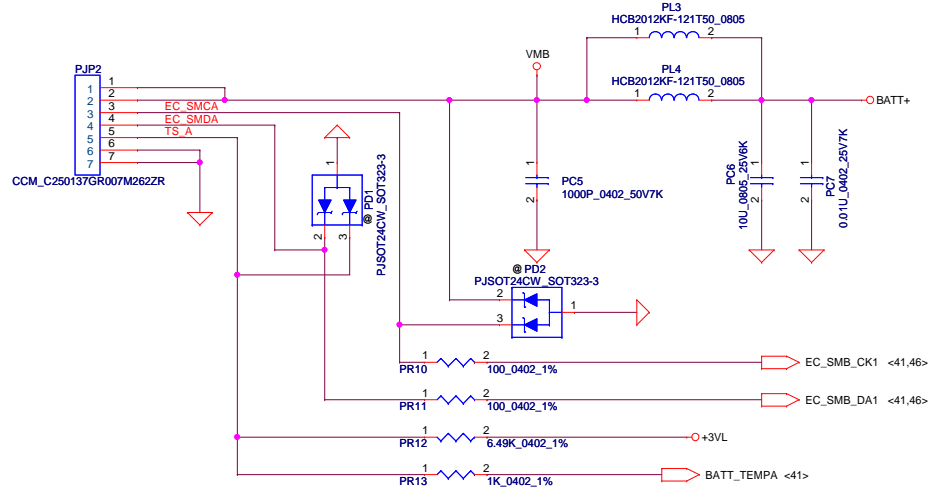
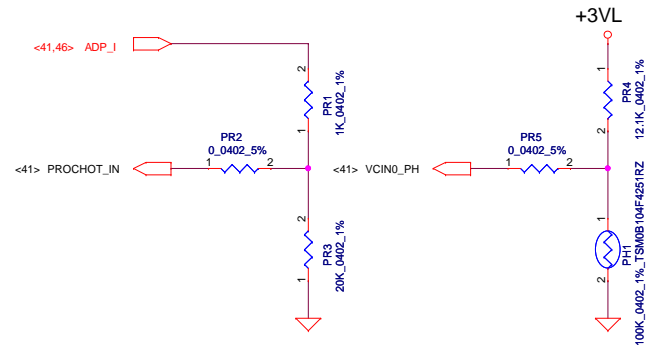


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Size	Document Number	Rev	Date
	QCLA4 LA-8861P M/B	0.2	Tuesday, February 14, 2012
			Sheet 43 of 58

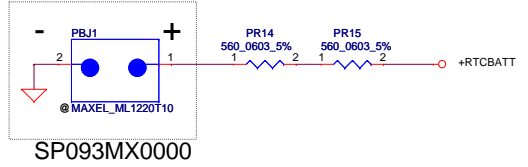


PH1 on CPU bottom side :
 CPU thermal protection at 93 +3 degree C
 Recovery at 56 +3 degree C

Please locate these parts
 Near EC chip



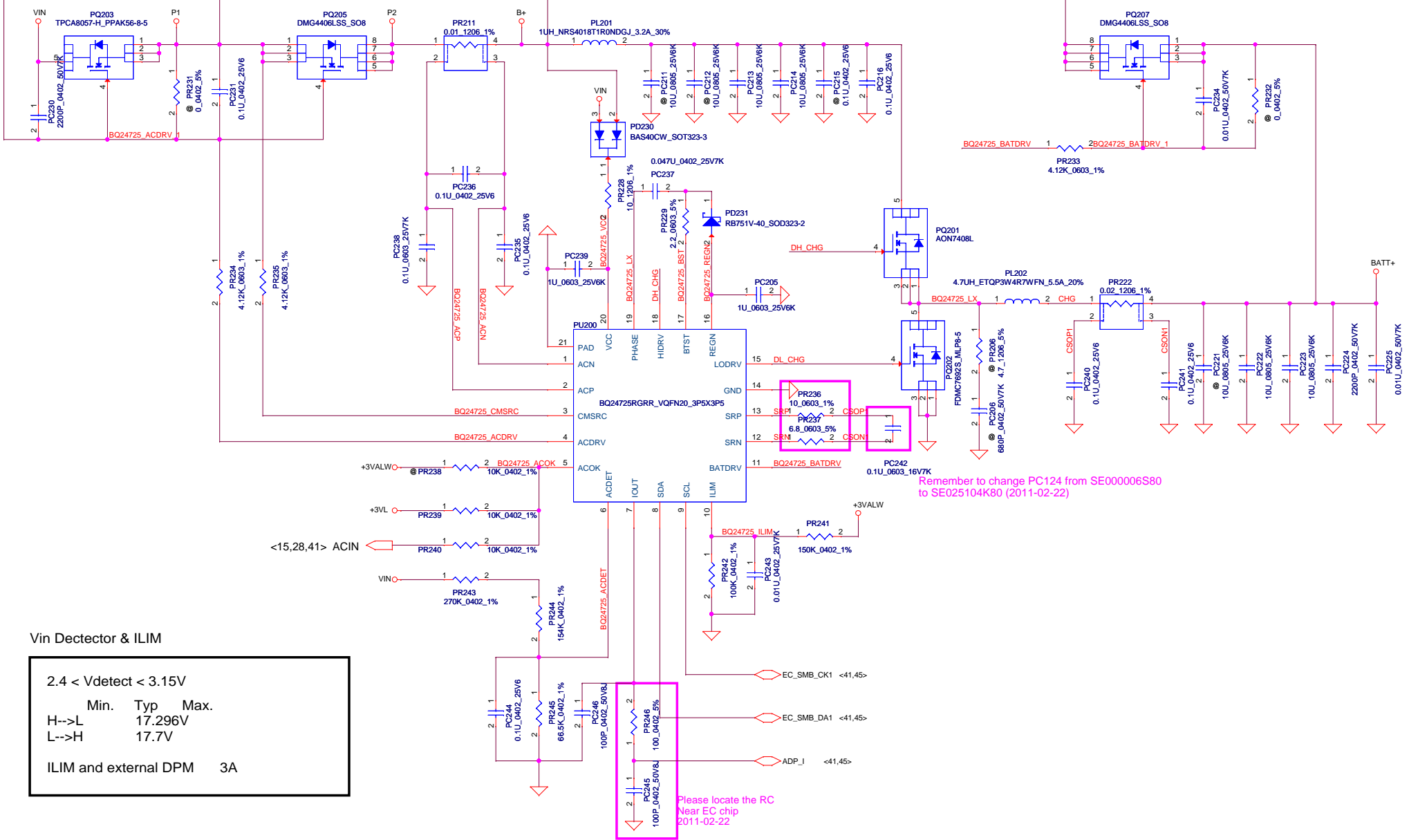
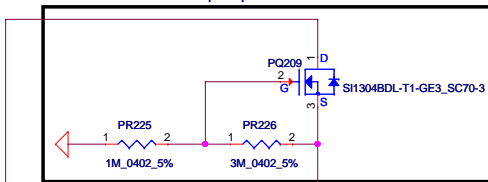
RTC Battery



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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title PWR-DCIN / BATT CONN / OTP	
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for reverse input protection



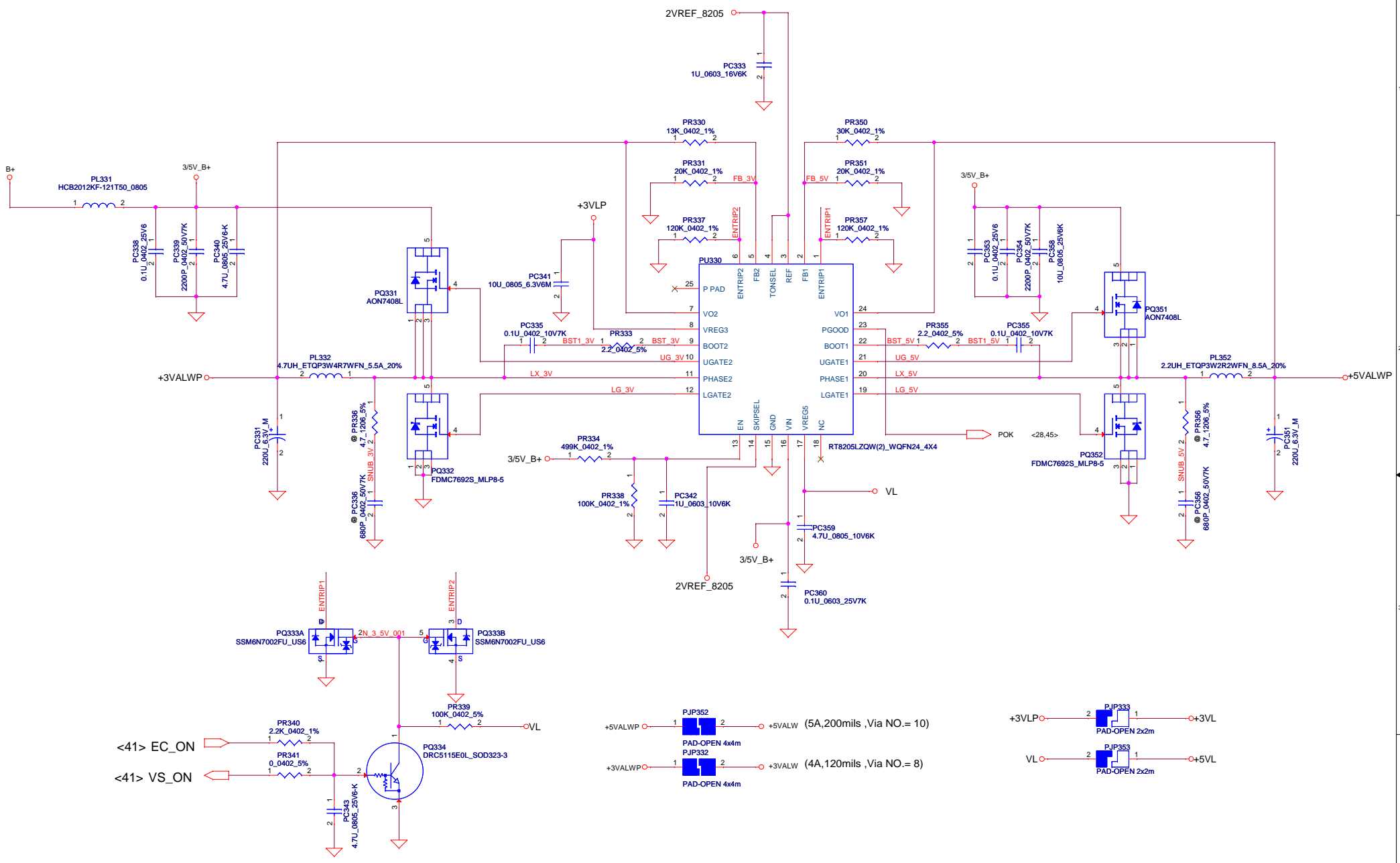
Vin Dectector & ILIM

$2.4 < V_{detect} < 3.15V$
 Min. Typ Max.
 H-->L 17.296V
 L-->H 17.7V
 ILIM and external DPM 3A

Remember to change PC124 from SE00006S80 to SE025104K80 (2011-02-22)

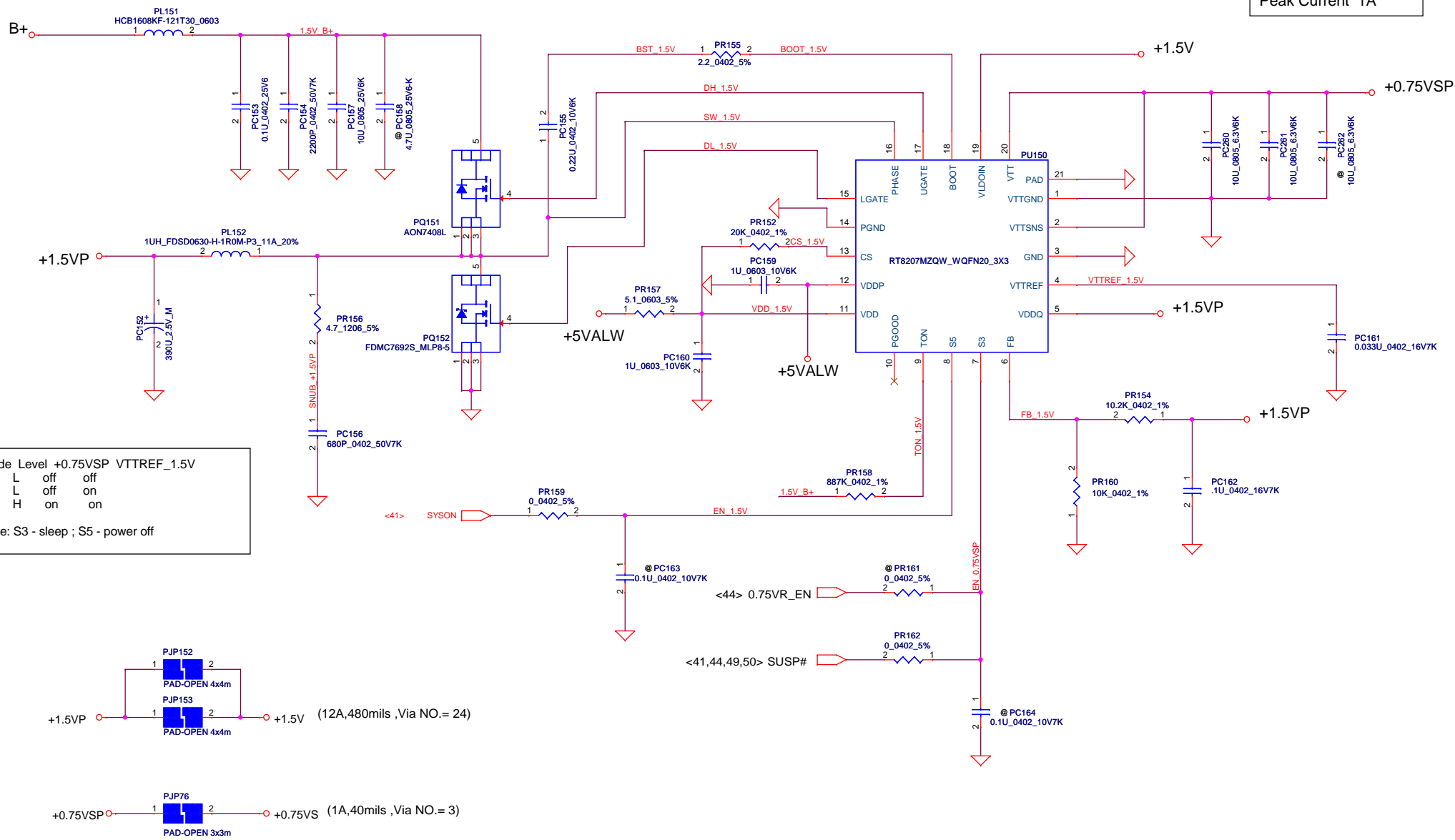
Please locate the RC Near EC chip 2011-02-22

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	PWR-CHARGER
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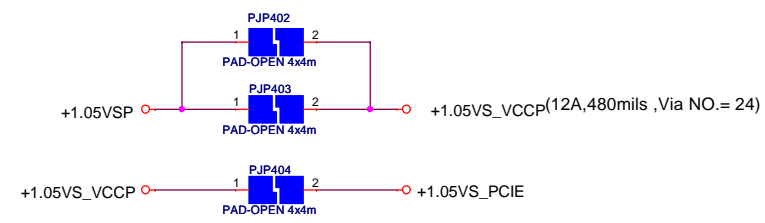
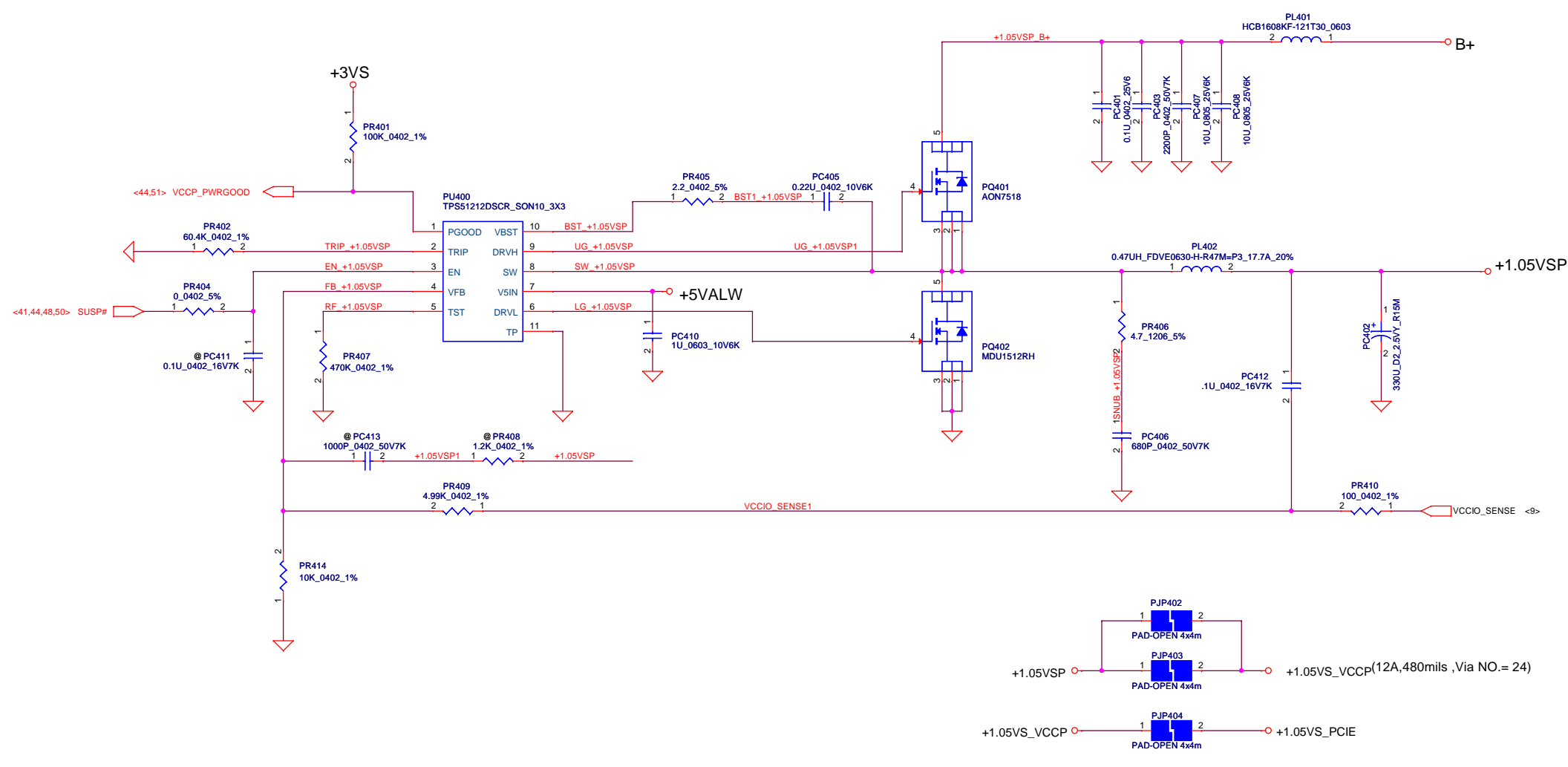
Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



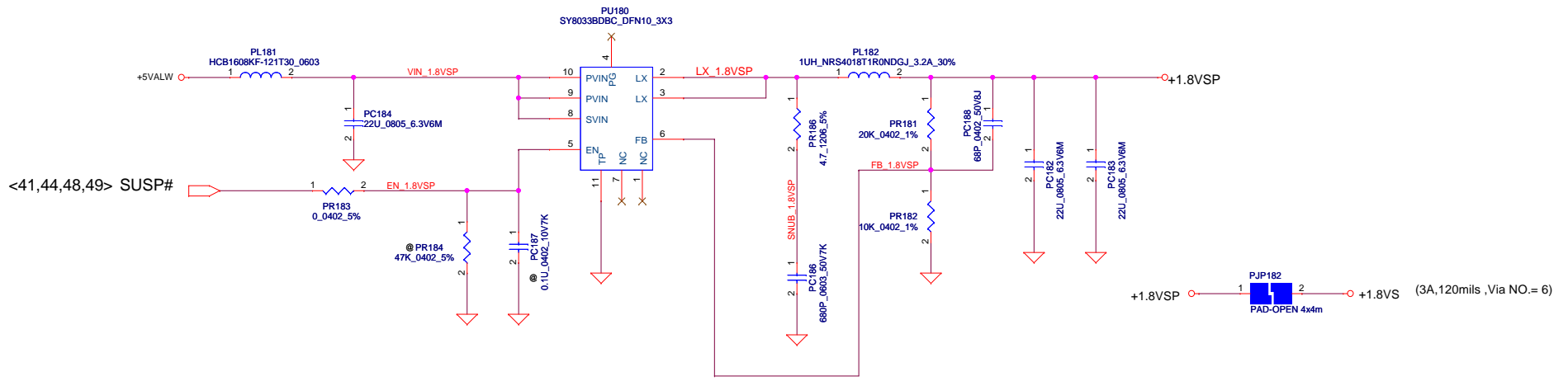
www.pdzbwx.com

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Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	
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Size	Custom	Document Number	SAMSUNG	Rev	0.2
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Size	Document Number	SAMSUNG		Rev	0.2
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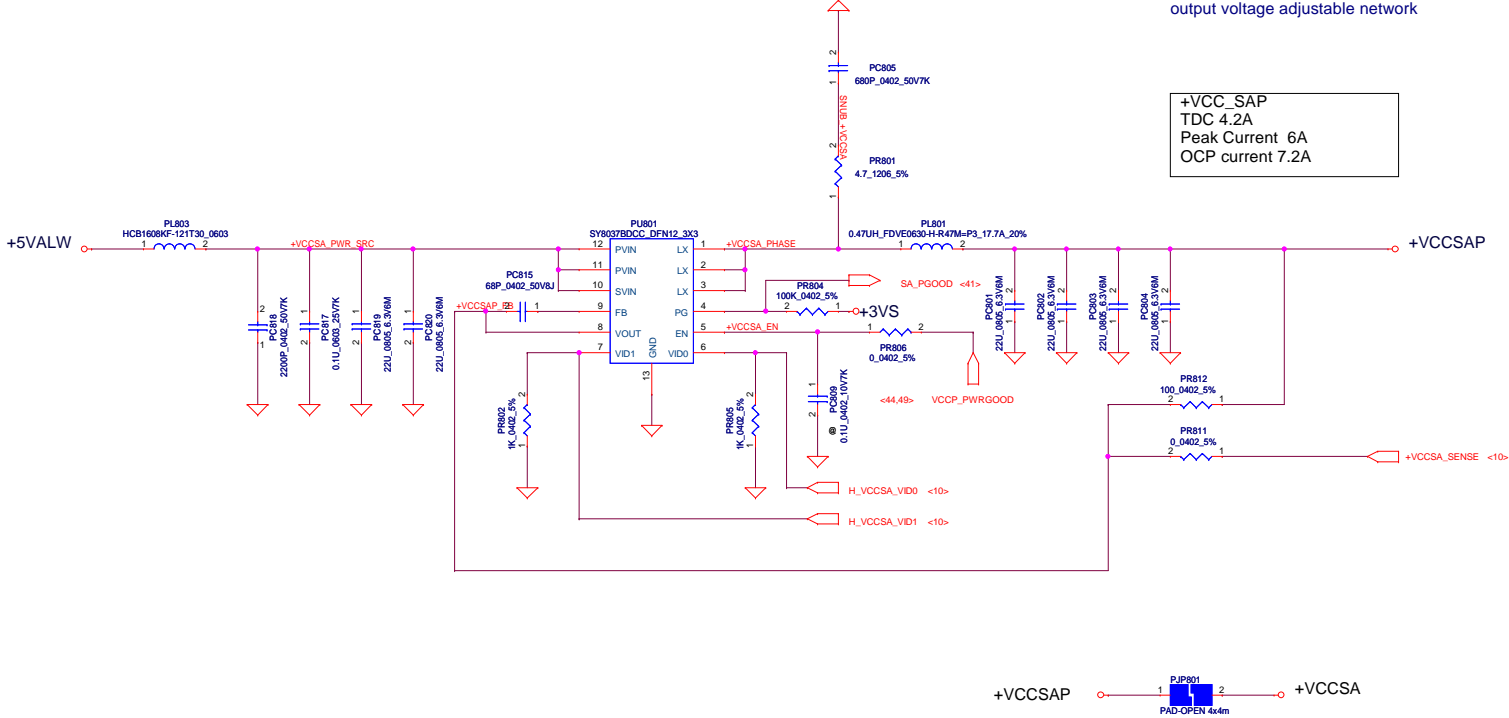
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2012/12/31	Title	
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The 1k PD on the VCCSA VID's are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

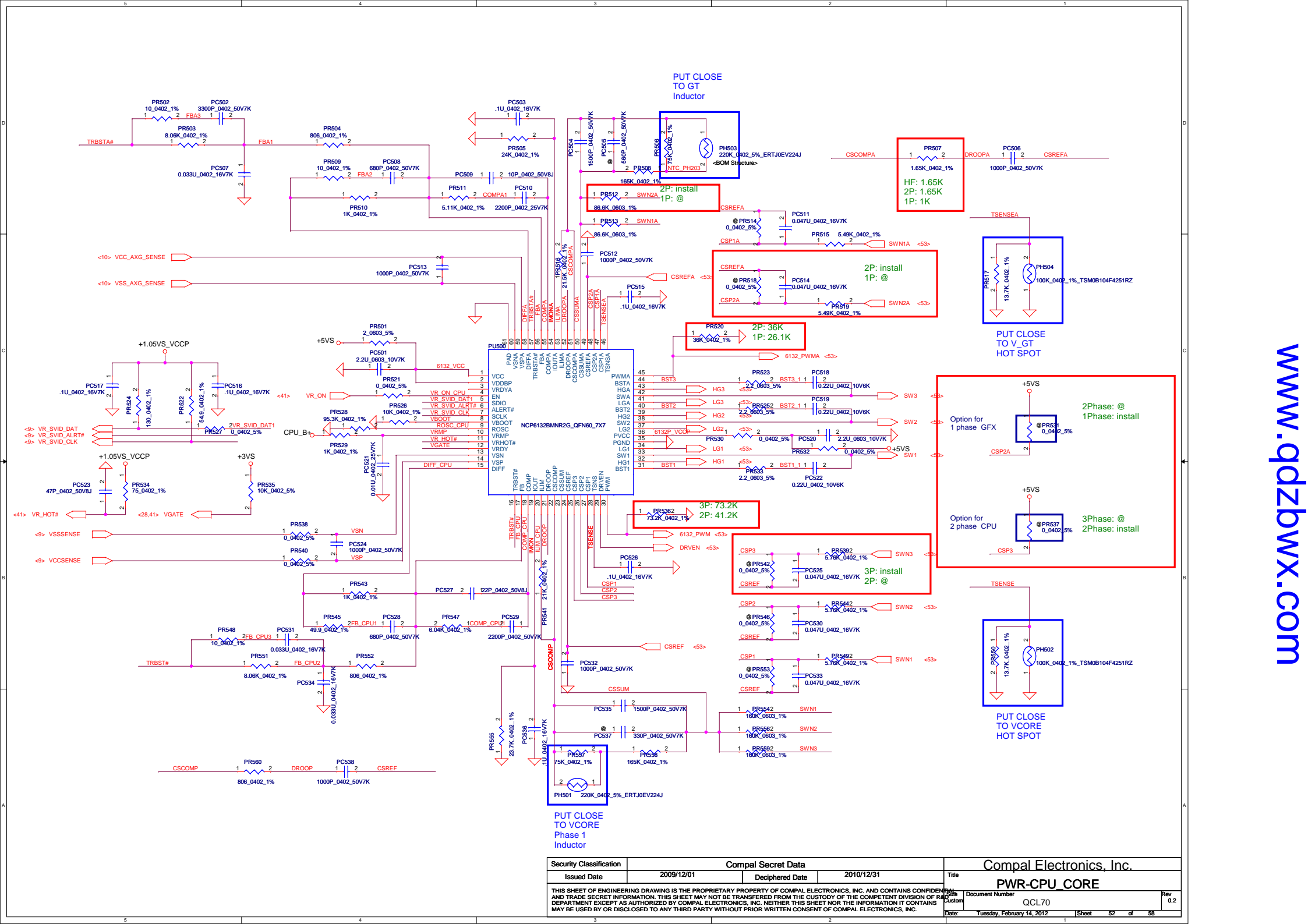
output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



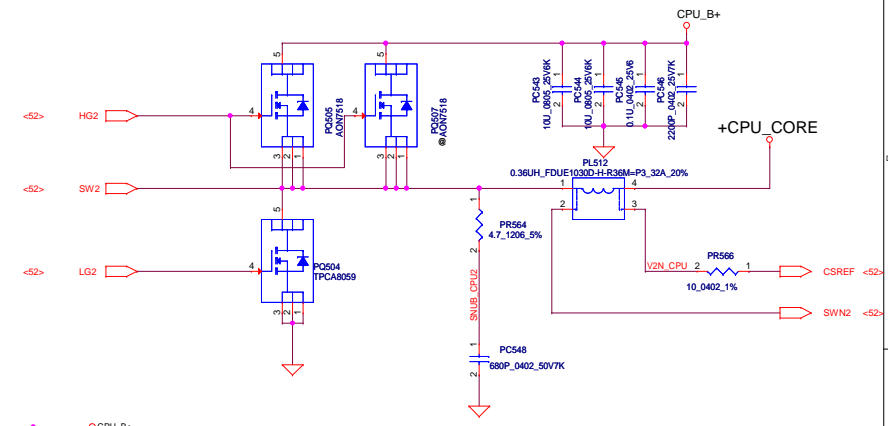
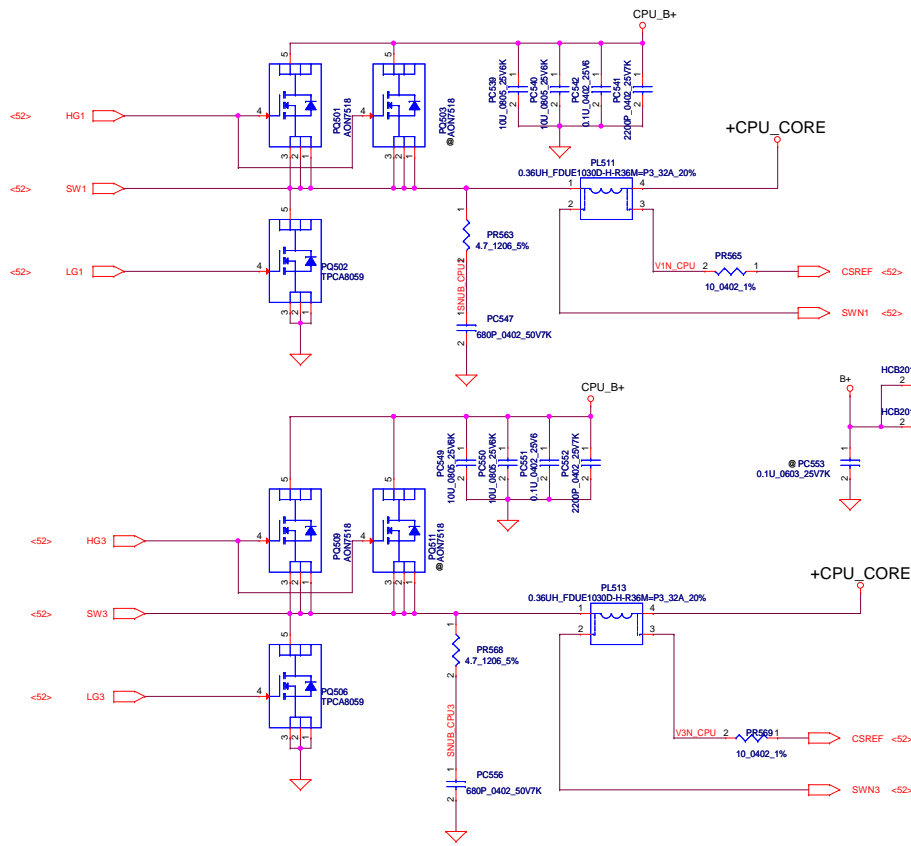
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Size	C	Document Number	SAMSUNG	Rev
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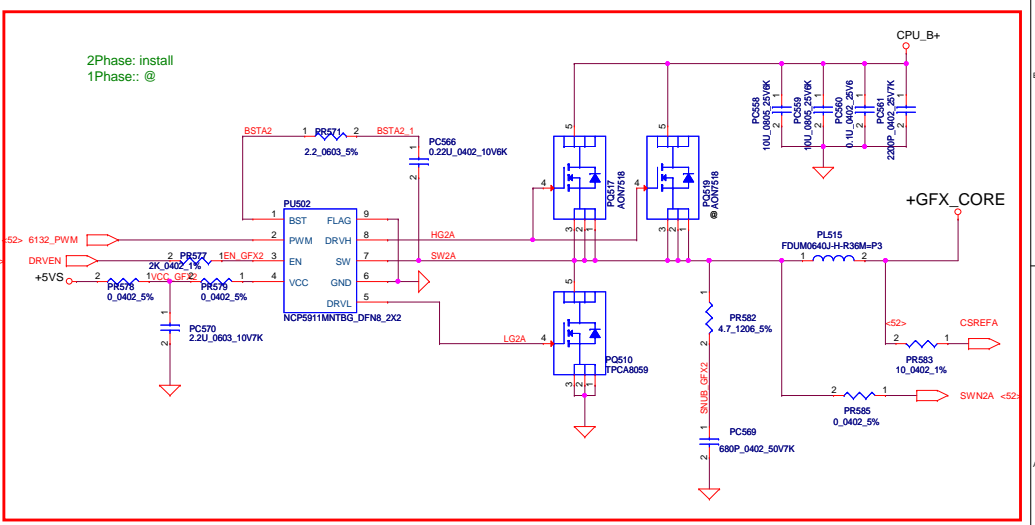
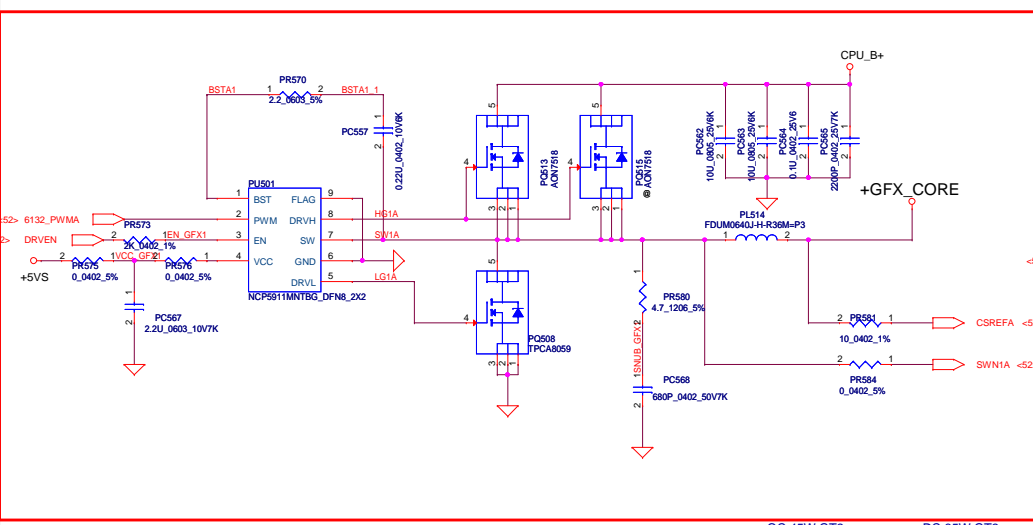
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title
				PWR-CPU_CORE
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				Rev 0.2 Sheet 52 of 58



QC 45W CPU (HF) solution: 3+2 MOS: cpu_core --> Gfx_core -->	2(AON7518) 2(AON7518)	1(FDMS0308AS) 1(FDMS0308AS)
QC 45W CPU solution: 3+2 MOS: cpu_core --> Gfx_core -->	1(AON7518) 1(AON7518)	1(FDMS0308AS) 1(FDMS0308AS)
DC 35W CPU solution: 2+1 MOS: cpu_core --> Gfx_core -->	1(AON7518) 1(AON7518)	1(FDMS0308AS) 1(FDMS0308AS)

QC 45W CPU
VID1=1.05V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=56A
R_LL=1.9m ohm
OCP=110A

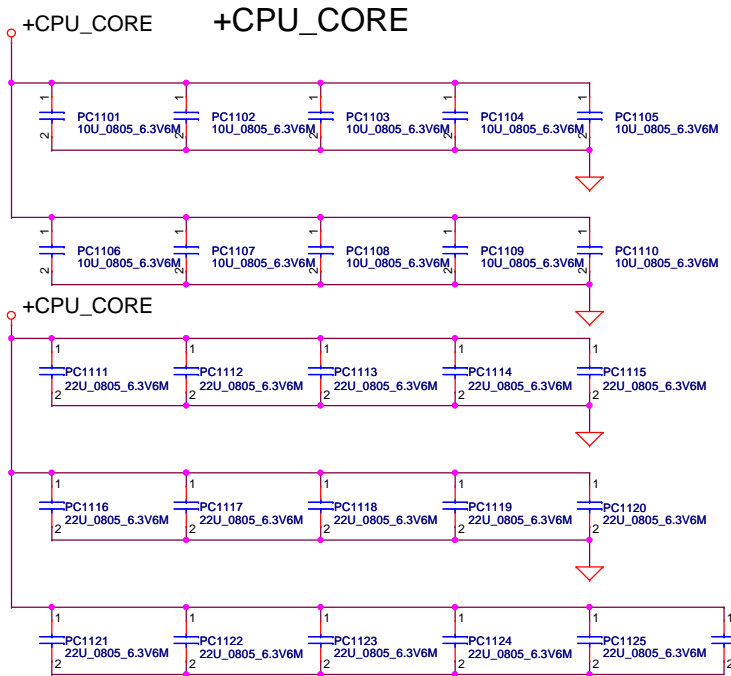
DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=33A
Icc_TDC=33A
R_LL=1.9m ohm
OCP=65A



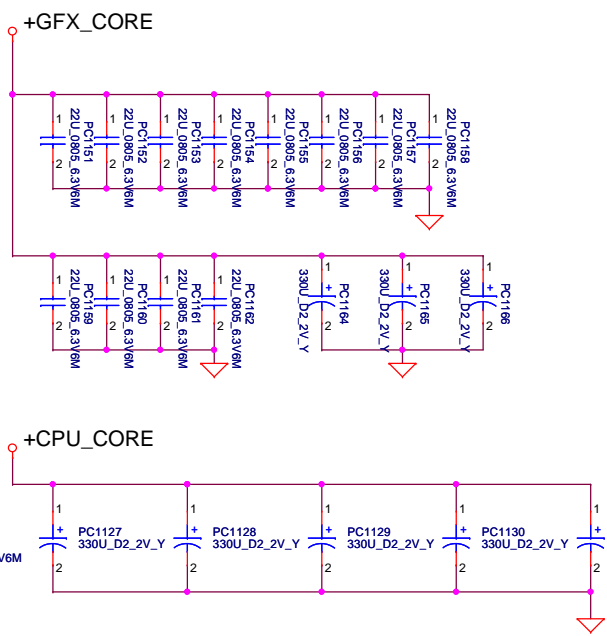
QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP=55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP=40A

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				QCL70
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				Date: Tuesday, February 14, 2012 Sheet 53 of 58



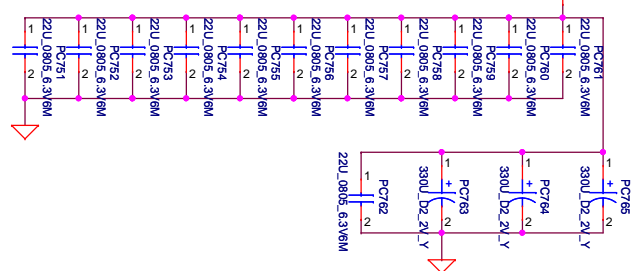
+GFX_CORE



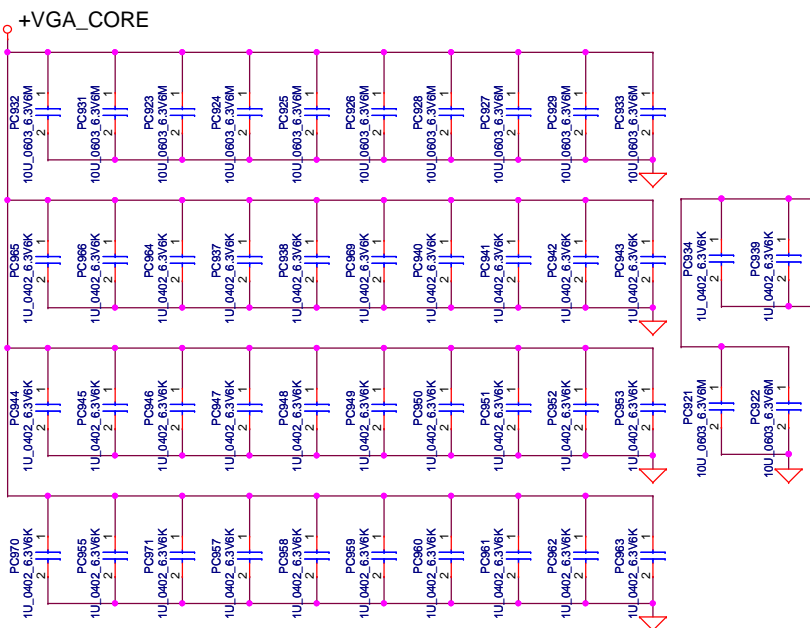
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 F (0805) 2 x (0805) no-stuff sites

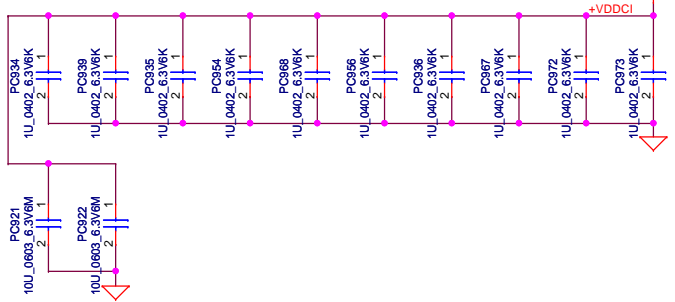
+1.05VS_VCCP



+VGA_CORE

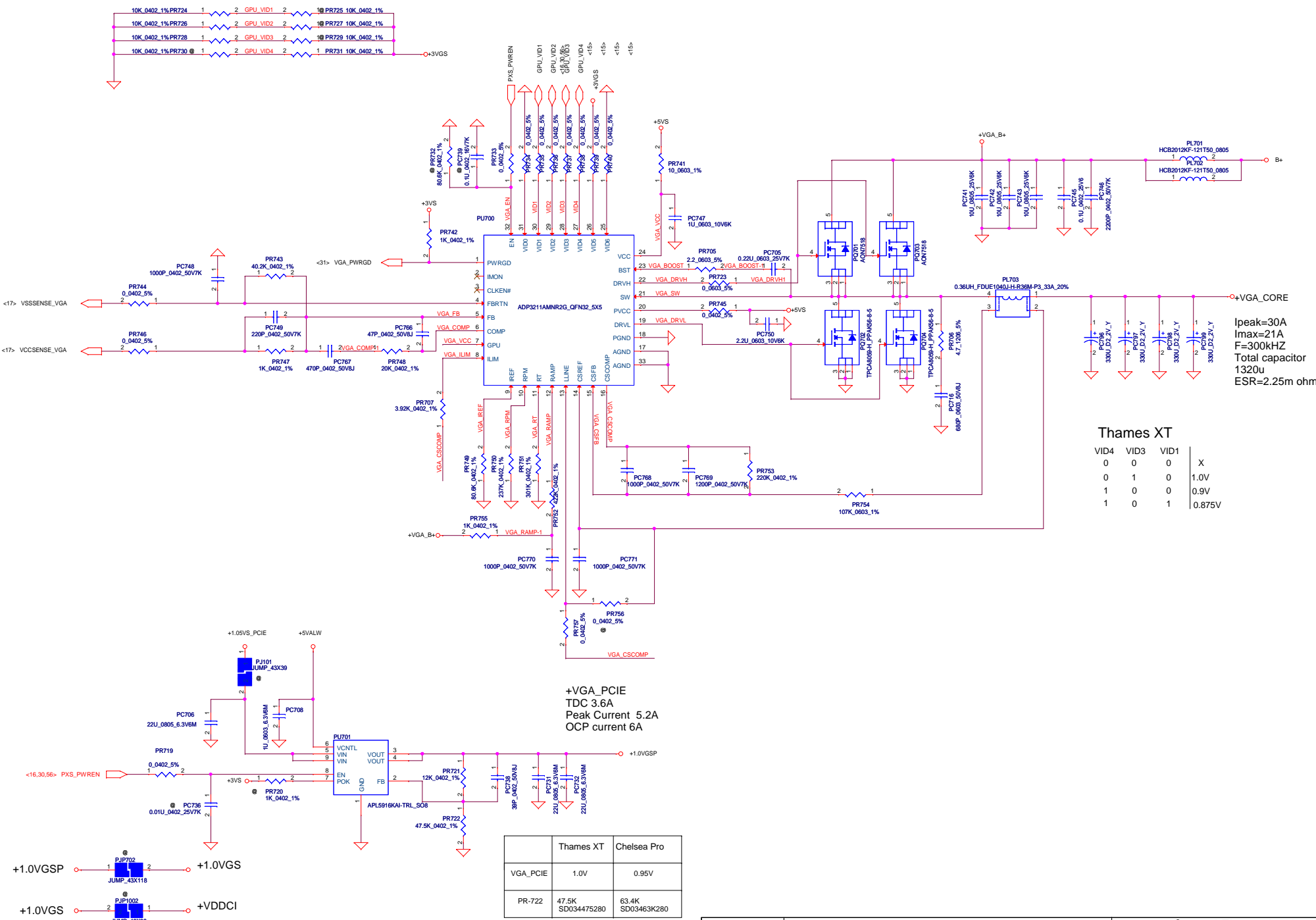


+VDDCI



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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				Document Number	
				QCLA4 LA-8861P M/B	
				Rev 0.2	
Date		Tuesday, February 14, 2012		Sheet 54 of 58	



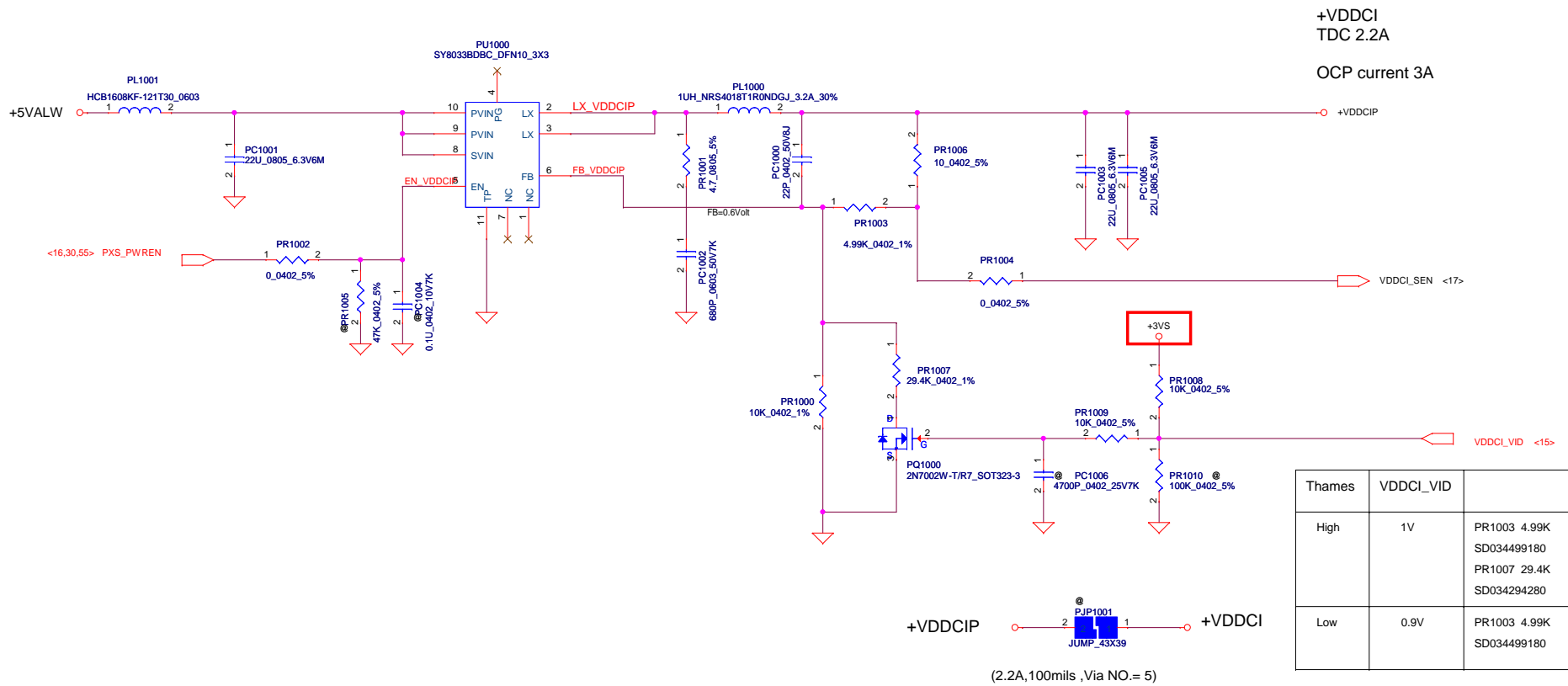
Ipeak=30A
 Imax=21A
 F=300kHz
 Total capacitor
 1320u
 ESR=2.25m ohm

Thames XT

VID4	VID3	VID1	
0	0	0	X
0	1	0	1.0V
1	0	0	0.9V
1	0	1	0.875V

	Thames XT	Chelsea Pro
VGA_PCIE	1.0V	0.95V
PR-722	47.5K SD034475280	63.4K SD034463K280

Security Classification	Compal Secret Data		Title	
Issued Date	2011/08/16	Deciphered Date	2012/08/15	+VGA_COREP / +VGA_PCIE(+1.0VGS)
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Thames	VDDCI_VID	
High	1V	PR1003 4.99K SD034499180 PR1007 29.4K SD034294280
Low	0.9V	PR1003 4.99K SD034499180

Chelsea	VDDCI_VID	
High	0.95V	PR1003 5.23K SD034523180 PR1007 86.6K SD034866280
Low	0.91V	PR1003 5.23K SD034523180

- | | | | | | |
|-----|------------|----------------------------|----|--------------------------------------|-----------------------------------|
| 1. | 2011/09/29 | P51-PWR_+3VALWP/+5VALWP | | Change PU330 to RT8205L | Change source |
| 2. | 2011/09/29 | P53-PWR_+1.05VS_VCCP/+16V | SP | Change PU400 to RT8237C | Change source |
| 3. | 2011/09/29 | P54-PWR_+VCCSAP/1.8VSP | | Change PU450 to SY8037B | Change source |
| 4. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change HMOS to MDV1525 | Change source |
| 5. | 2011/09/29 | P53-PWR_+1.05VS_VCCP/+16V | SP | Change HMOS to MDV1525 | Change source |
| 6. | 2011/09/29 | P49-PWR_BATTERY CONN / OTP | | Change PD5,PD6 to SCA00001G00 | ESD team request |
| 7. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PR589 from 348 to 8.06k | FAE suggestion |
| 8. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PR590 from 3.65k to 806 | FAE suggestion |
| 10. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PC574 from 680P to 0.033u | FAE suggestion |
| 11. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PC577 from 4700P to 0.033u | FAE suggestion |
| 12. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PR548 from 1.21k to 8.06k | FAE suggestion |
| 13. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PR550 from 10.7k to 806 | FAE suggestion |
| 14. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PC547 from 680P to 0.033u | FAE suggestion |
| 15. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Change PC551 from 4700P to 0.033u | FAE suggestion |
| 16. | 2011/09/29 | P57-PWR +CPU_CORE DECOUPLI | NG | Add snubber and boost resistor | For 3x3 H-MOS solution |
| 17. | 2011/09/29 | P49-PWR_BATTERY CONN / OTP | | Add PR22 120k, PR27 100k, PR32 0 Ohm | For 120W adapter protect(9012) |
| 18. | 2011/09/29 | P58-PWR_VGA_CORE | | Remove PC803, PC804 add PC806 47u | For Nvidia suggestion |
| 19. | 2011/09/29 | P51-PWR_+3VALWP/+5VALWP | | Change PC360 to SE000006R80 | Change source |
| 20. | 2011/09/29 | P58-PWR_VGA_CORE | | Change PC702 to SE000000H180 | Change source |
| 21. | 2011/09/29 | P49-PWR_BATTERY CONN / OTP | | Add PR17 14k, PR33 0 Ohm | For CPU temperature protect(9012) |
| 22. | 2011/09/29 | P51-PWR_+3VALWP/+5VALWP | | Add PR373 0 Ohm | For 3/5 V always power on(9012) |

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HW PIR (Product Improve Record)

QCLA4 LA-8861P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1 TO 0.2

NO DATE PAGE MODIFICATION LIST

1. 02/01 16 Remove PX_MODE and BACO components
 2. 02/01 18 Remove PX_EN and RV125
 3. 02/01 12 Change RD9.2 to GND
 4. 02/01 13 Change RD15.1 to +3VS
 5. 02/01 26 Stuff BIOS 2M ROM:UH4,RH267,RH269,
 6. 02/01 27 Change JTP footprint to ACES_50504
 7. 02/01 40 Add JMIC ACES_50271-0020N-001_2P
 8. 02/01 36 Change JWLAN footprint to ACES_889
 9. 02/01 38 Remove INT_MIC from JCRI0.1
 10. 02/01 37 Reserve PJ31 from +3VALW_PCH to +3
 11. 02/06 38 Swap LR9
 12. 02/06 36 Add UM5,RM21;Reserve RM19,PJ33,Lin
 13. 02/06 43 Connect AOAC_WLAN_PWR_EN# to EC pin
 14. 02/06 38 Change JCRI0.1 netname to NBA_PLUG
 15. 02/06 40 Remove CA64 and add RA32,RA33 to I
 16. 02/09 37 Add TL1 on UL1.37
 17. 02/09 31 Change UH1.T7 from HDMI_HPD to CHP
 18. 02/09 24 Delete T66 and link CHP3_SERDBG to
 19. 02/09 10 Remove CC58
 19. 02/09 25 Add D94,D95,D96 on HDMI signal
 20. 02/09 24 DEL D3~D5 and add D97,D98 on CRT s
 21. 02/09 37 Add D99,D100 on LAN signal
 22. 02/09 35 Add R1000~R1003 between JODD and J
 23. 02/09 08 Reserve DRAMRST_CNTRL_EC to QC3
 24. 02/09 41 Reserve DRAMRST_CNTRL_EC to EC pin

CH100,RH271,RH69,CH21
 -0120N-001_12P
 11-5204_52P
 V_LAN
 k AOAC_WLAN_PWR_EN# to +3V_WLAN
 n38; Connect WLAN_RST# to EC pin91
 and change JCRI0.2 to MIC_SENSE
 ink SENSE_A to UA1.13
 3_SERDBG and add RH216 PH 1Kohm
 JCRT.4
 ignal
 ODDB
 89

PURPOSE

No support PX4.0 by K99's request
 No support PX4.0 by K99's request
 Correct the DDR SPD address
 Correct the DDR SPD address
 For win8 common design
 Follow connector list
 From K99's request to change AMIC
 Follow connector list
 From K99's request to change AMIC
 To save power consumption
 For layout smoothly
 For WLAN ON/OFF feature
 For WLAN ON/OFF feature
 Remove AMic solution on sub/B
 Remove AMic solution on sub/B
 Reserved from vendor's suggestion
 For Serial POST debugger feature
 For Serial POST debugger feature
 To prevent from short with thermal
 For ESD request
 For ESD request
 For ESD request
 Reserve for reducing SATA signal refle
 Reserved for DS3 feature
 Reserved for DS3 feature

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