

Compal Confidential

Tablet 10" M/B Schematics Document Intel Pineview-M Processor with DDRIII + Tigerpoint

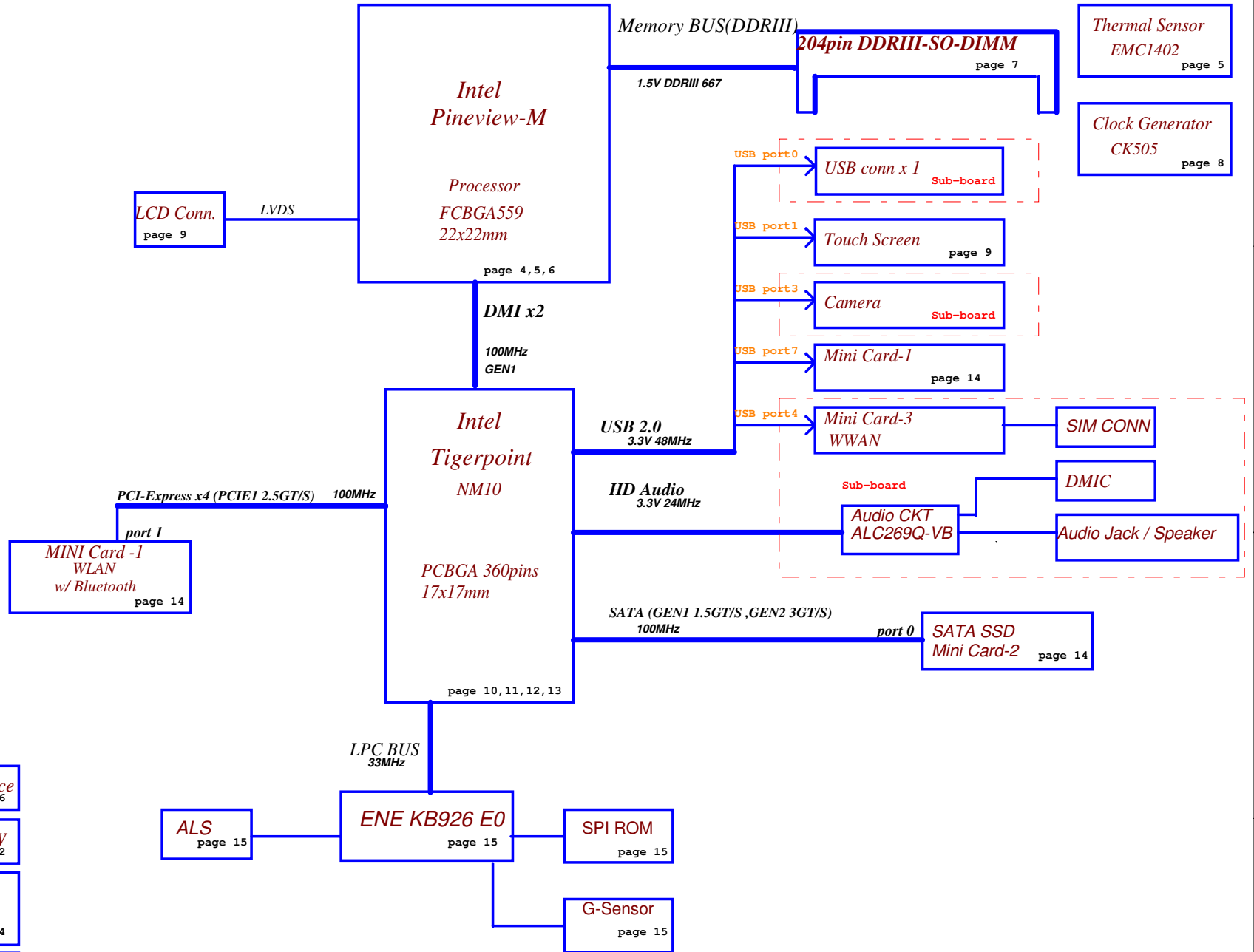
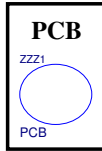
2010-05-07

REV : 0 . 1

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Model Name : PAU00
File Name : LA-6371P



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0.75VSP** page 24
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	100_1100

Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

USB table

		Port	Ext USB Conn.
EHCI1	UHCI1	Port0	Ext USB Conn.
		Port1	Touch Screen
		Port2	
EHCI2	UHCI2	Port3	Camera
		Port4	WWAN
		Port5	
EHCI2	UHCI3	Port6	
		Port7	WLAN
		Port8	
		Port9	
		Port10	
		Port11	

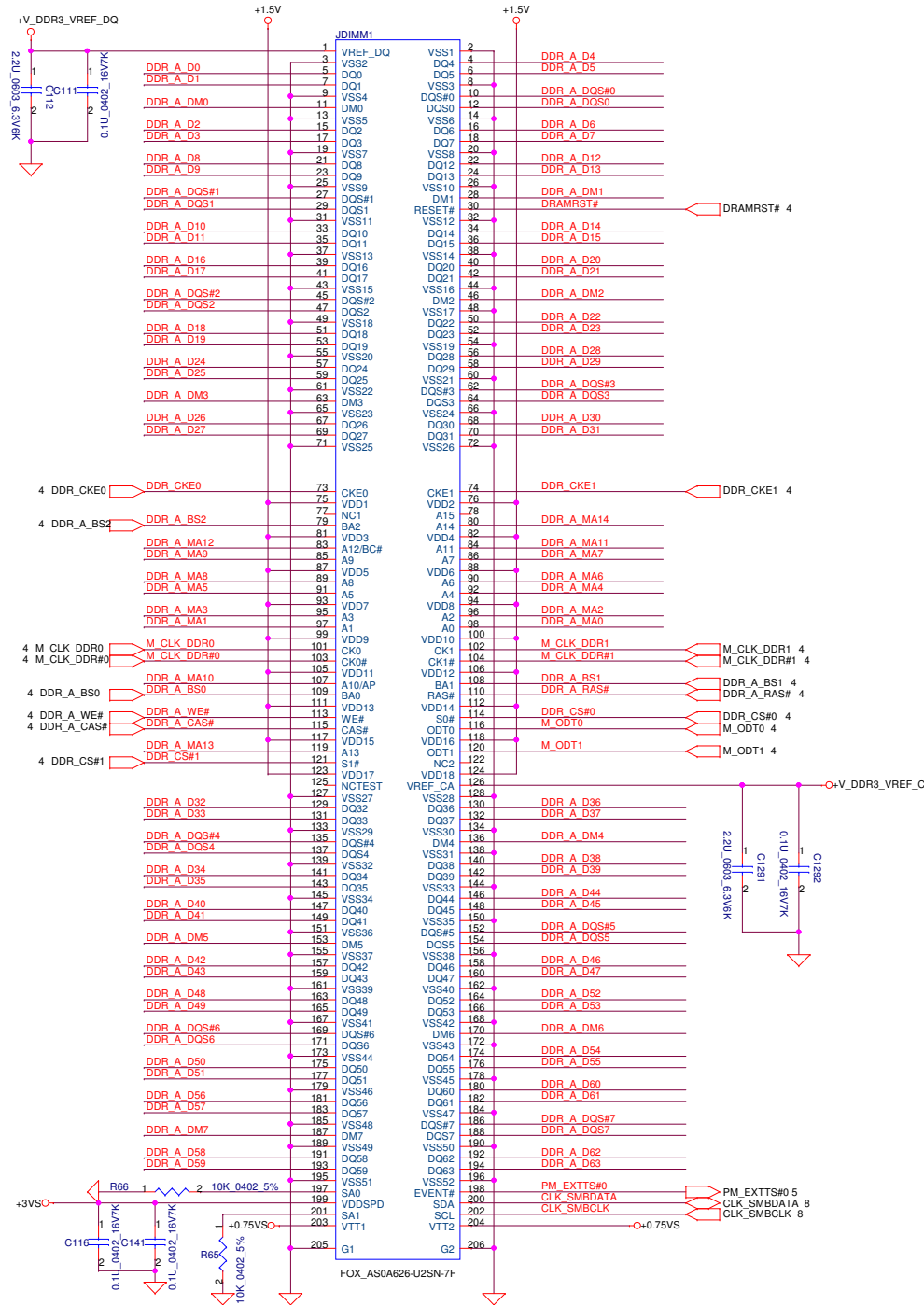
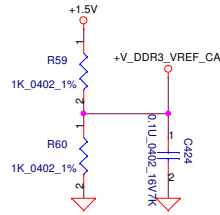
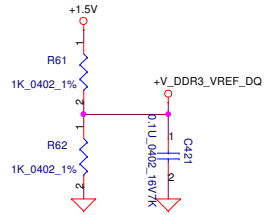
PCIE table

PCIE port	
PCIE port1	
PCIE port2	WLAN
PCIE port3	
PCIE port4	
PCIE port5	
PCIE port6	

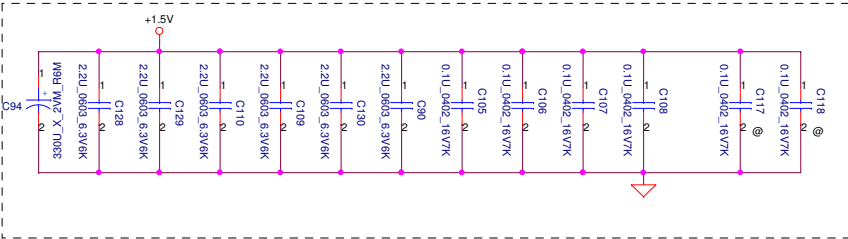
SATA table

SATA port	
SATA port0	SSD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	

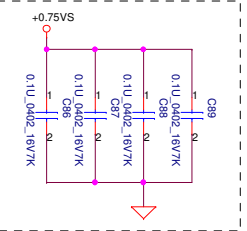
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Layout Note:
Place near JDIMM1



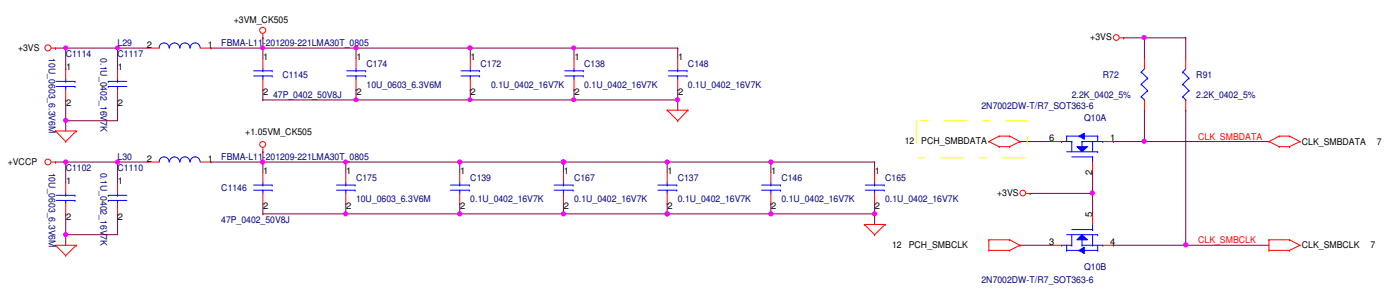
Layout Note:
Place near JDIMM1.203 & JDIMM1.204



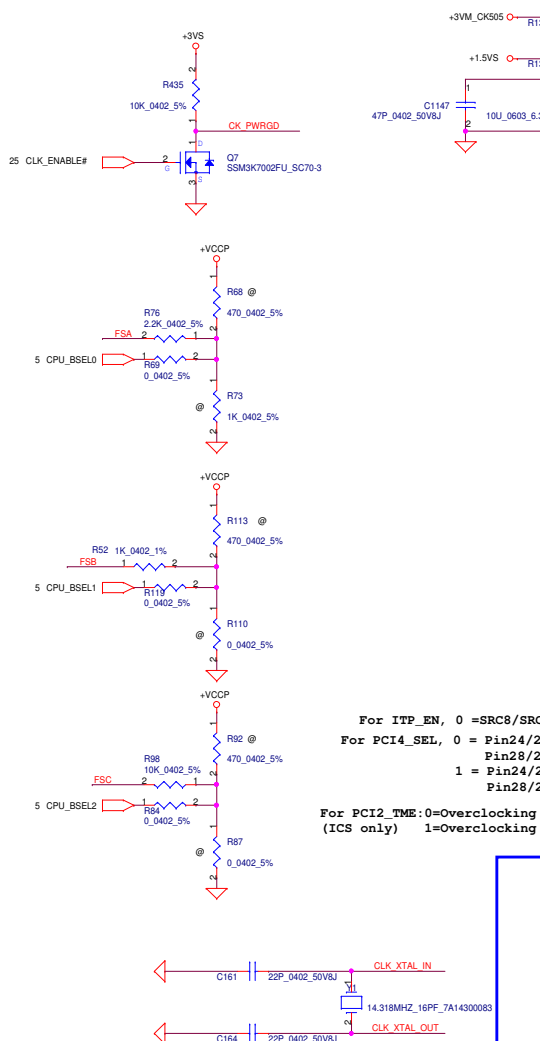
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Compal Electronics, Inc.
DDRIII SO-DIMM A

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
Reserved								

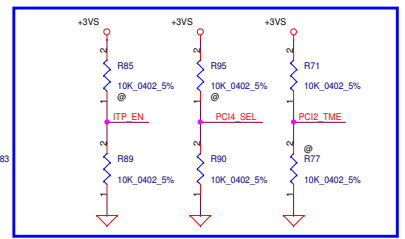


SA00003H730 (Realtek :RTM890N-397-VC-GRT)

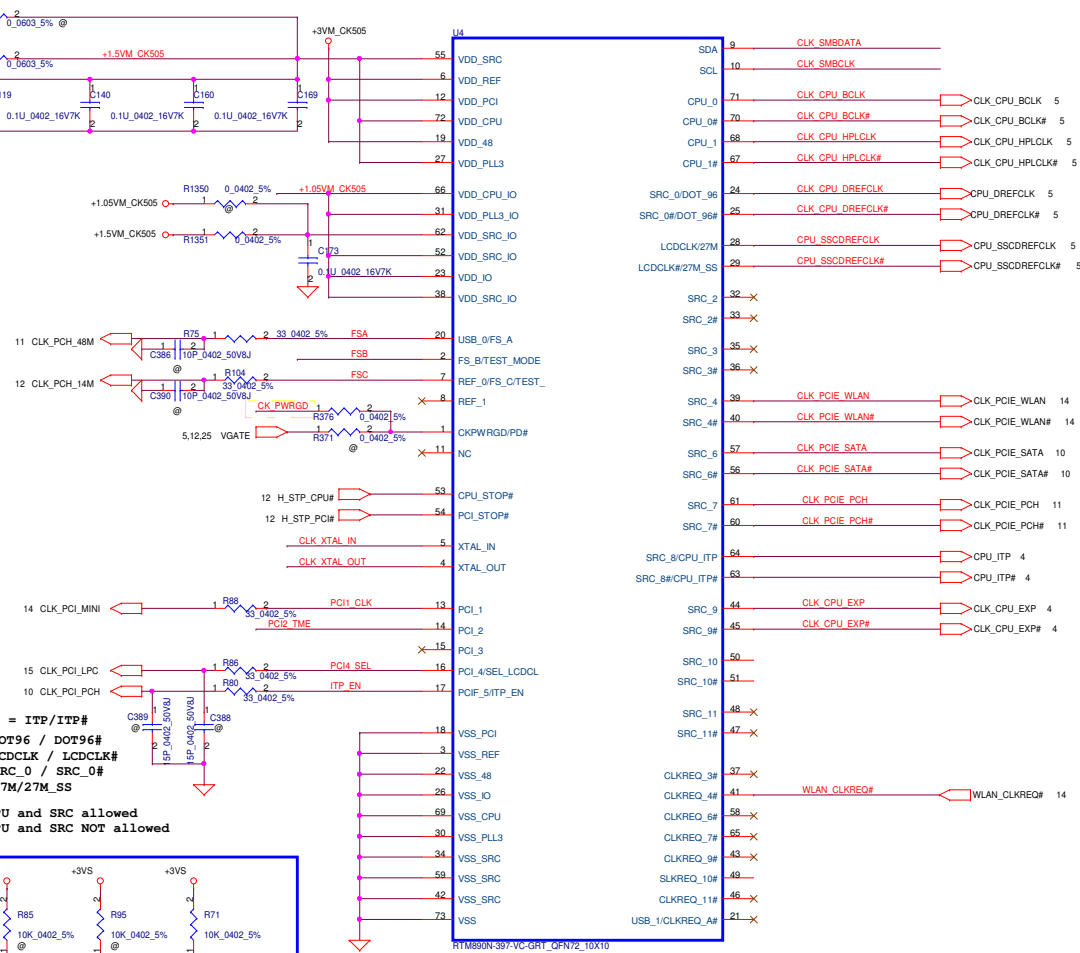


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
 For PCIA_SEL, 0 = Pin24/25 : DOT96 / DOT96#
 Pin28/29 : LCDCLK / LCDCLK#
 1 = Pin24/25 : SRC_0 / SRC_0#
 Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
 (ICS only) 1=Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil
 Placed within 500 mil



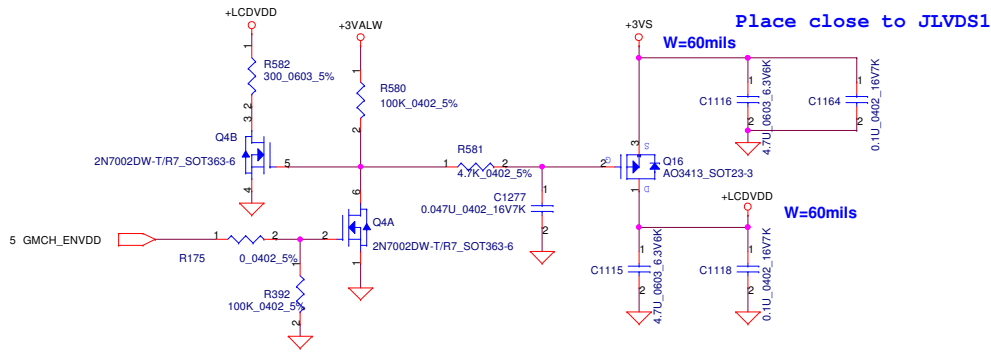
SRC PORT LIST

PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	

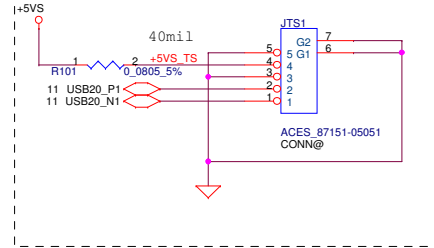
REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	
REQ_A#	

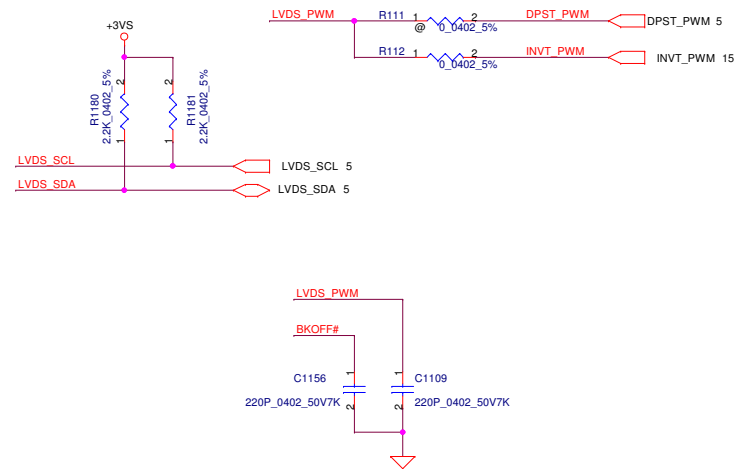
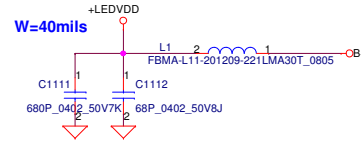
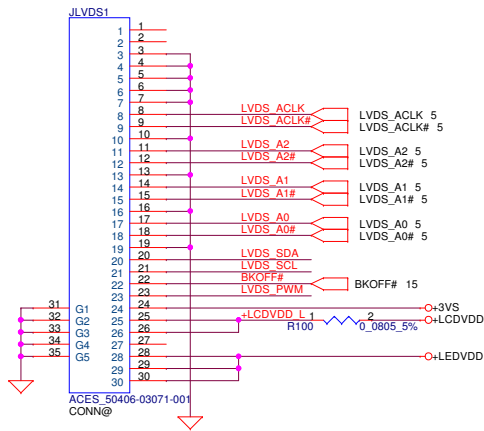
LCD POWER CIRCUIT



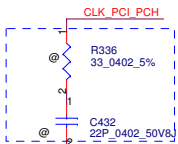
Touch Screen Conn.



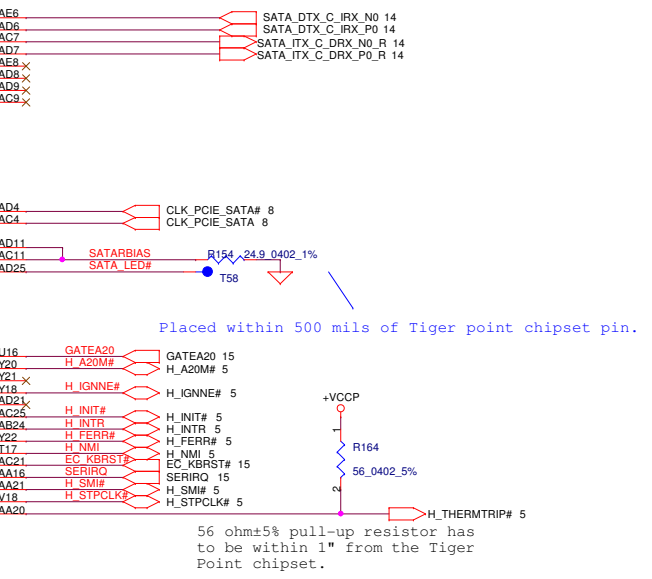
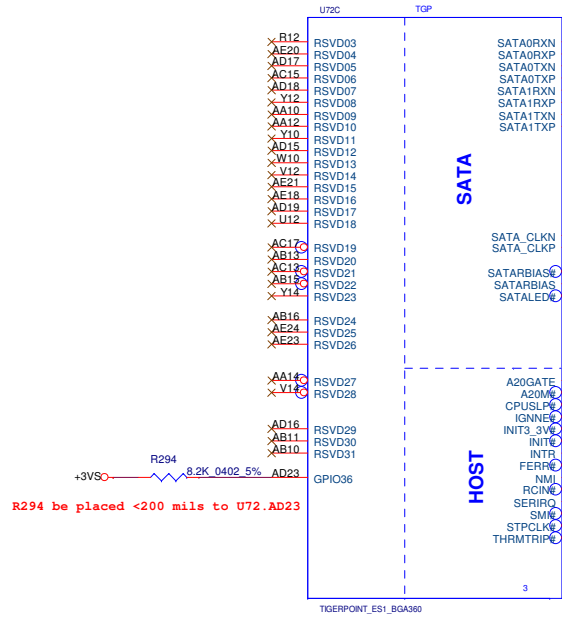
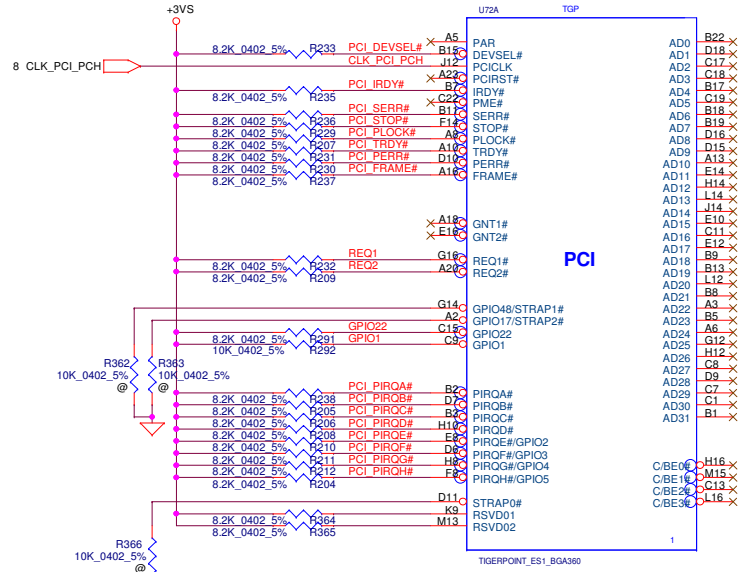
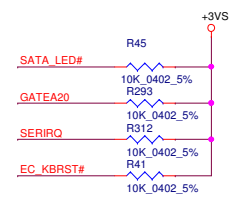
LCD/PANEL Conn.



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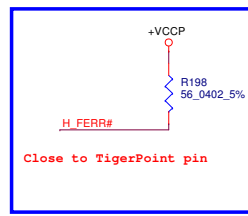


For EMI, close to TigerPoint



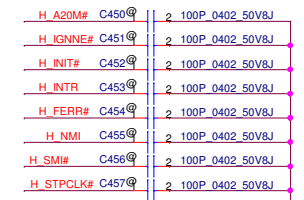
56 ohm±5% pull-up resistor has to be within 1" from the Tiger Point chipset.

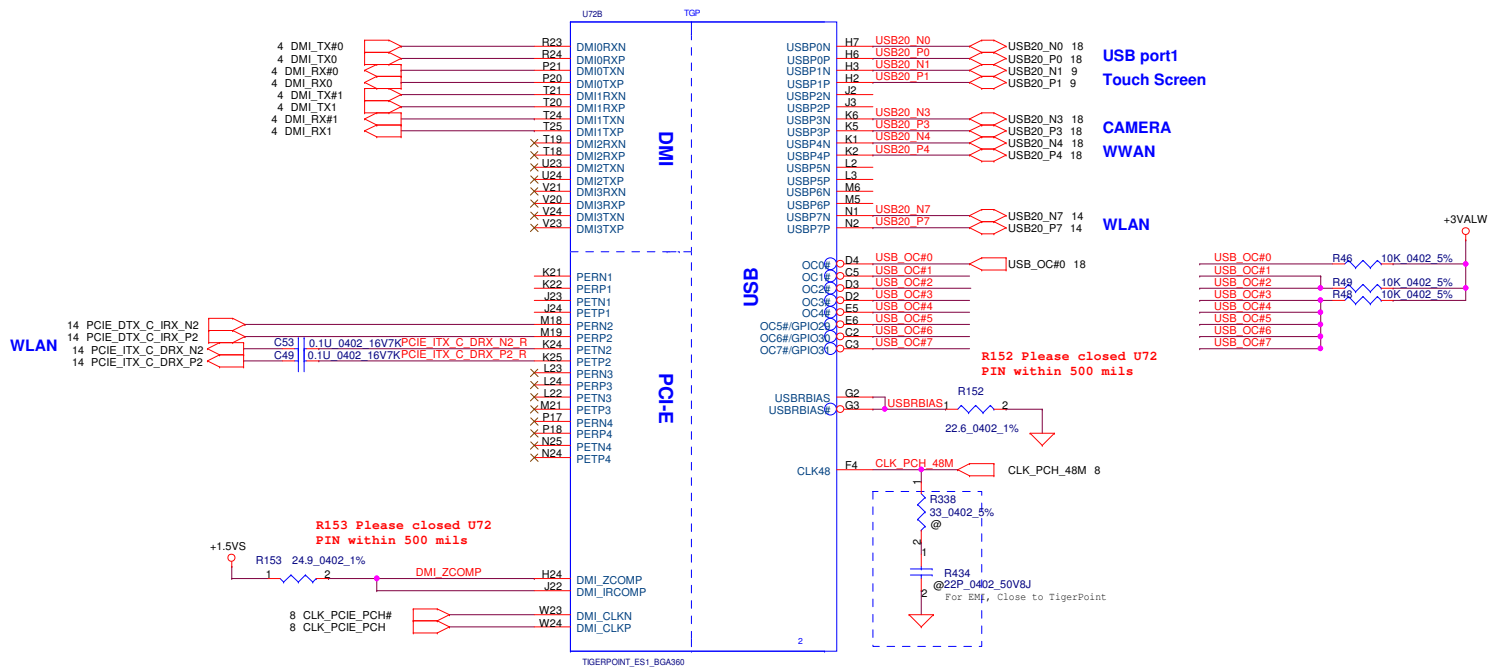
STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC



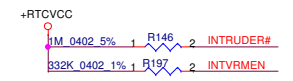
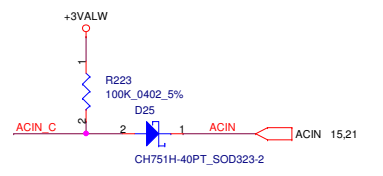
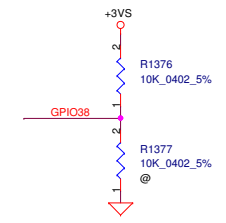
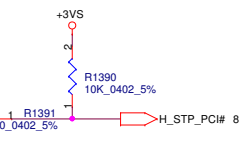
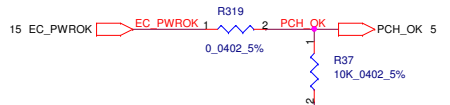
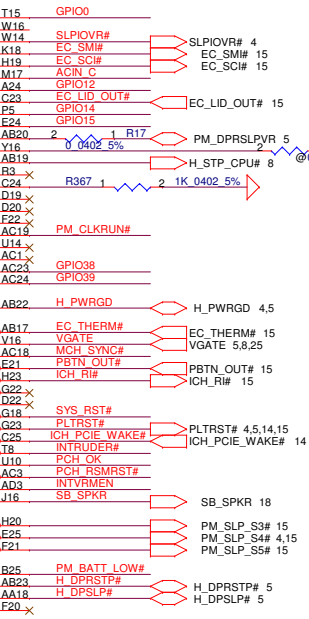
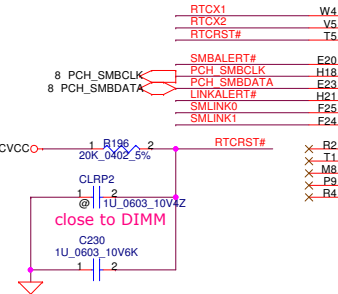
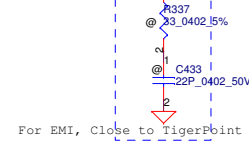
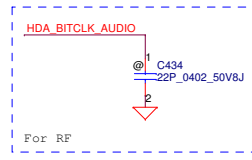
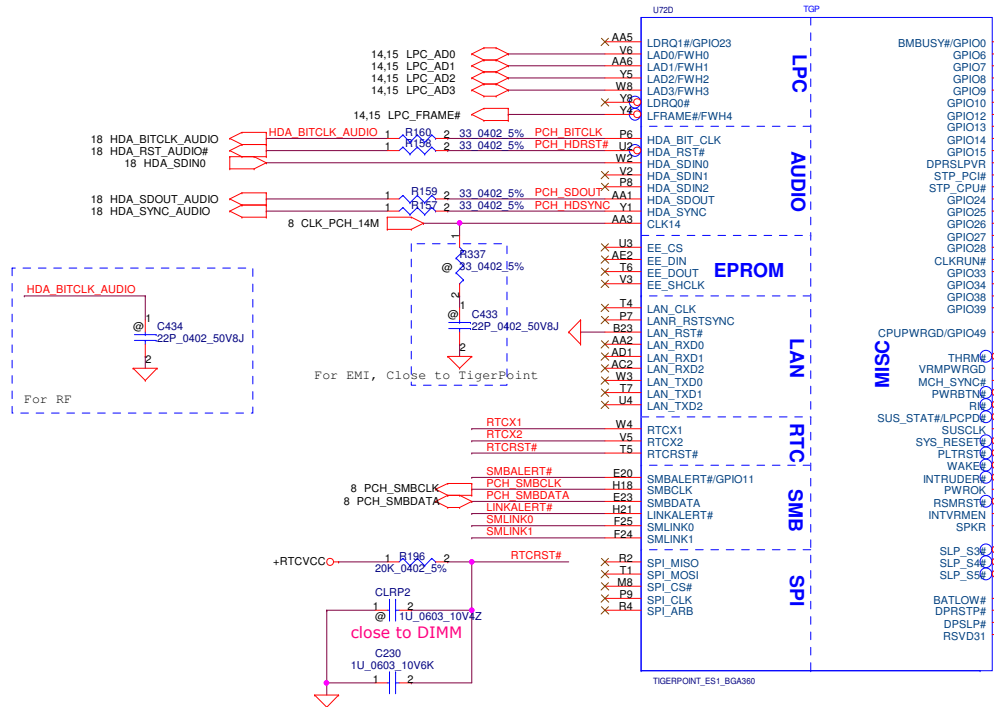
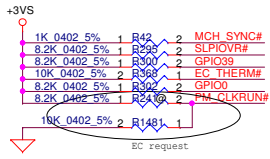
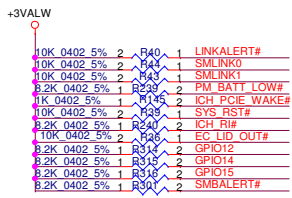
Close to TigerPoint pin

ESD request

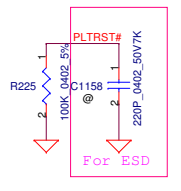
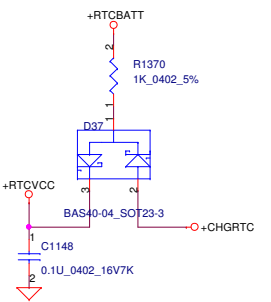
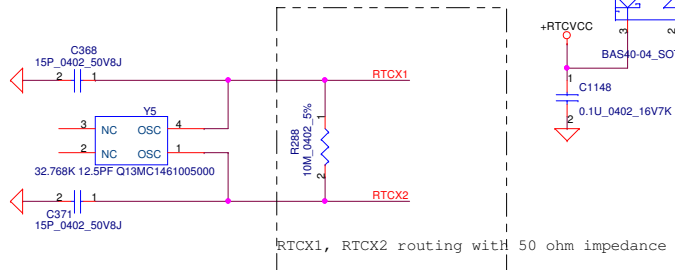
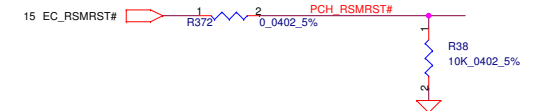




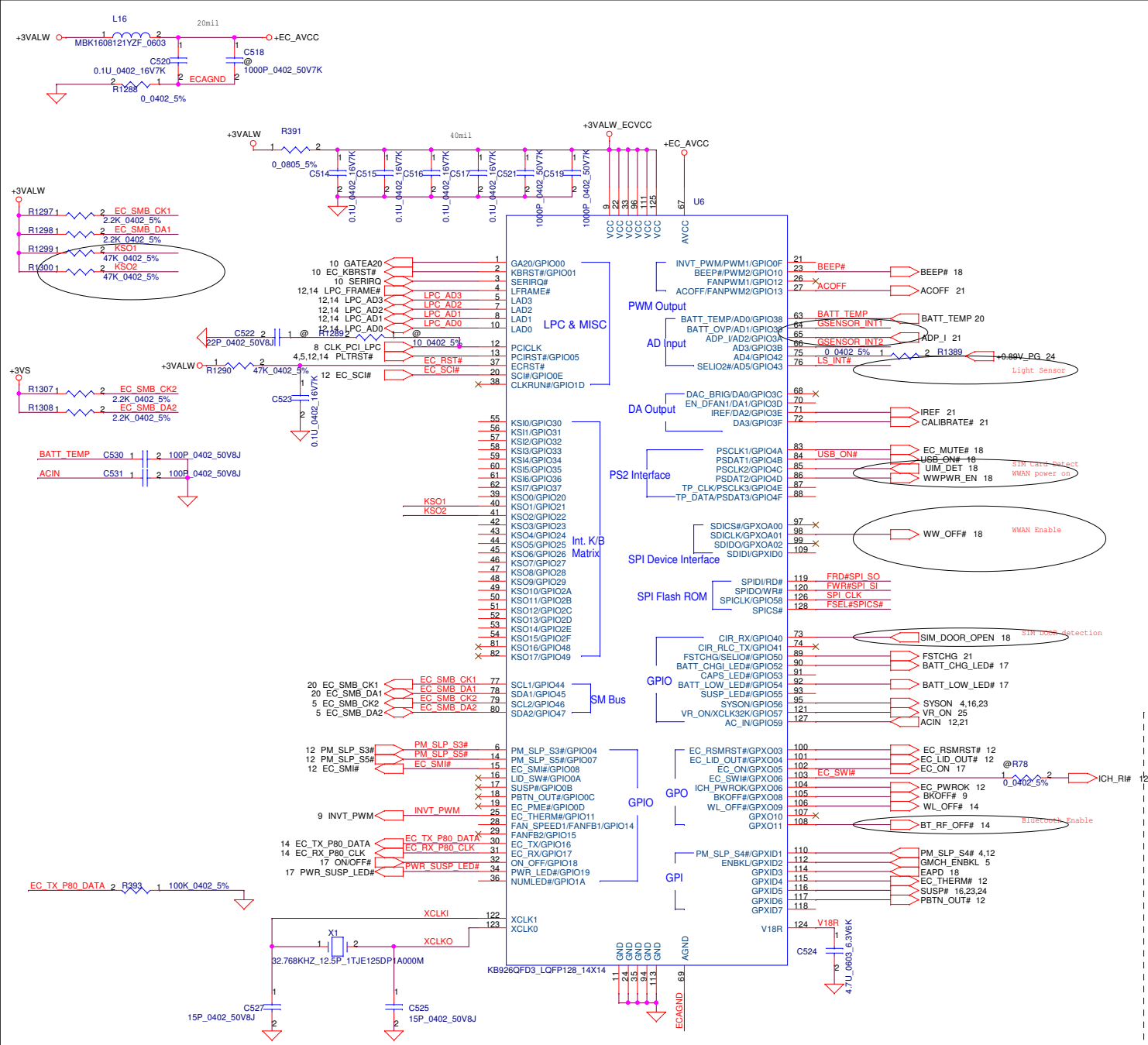
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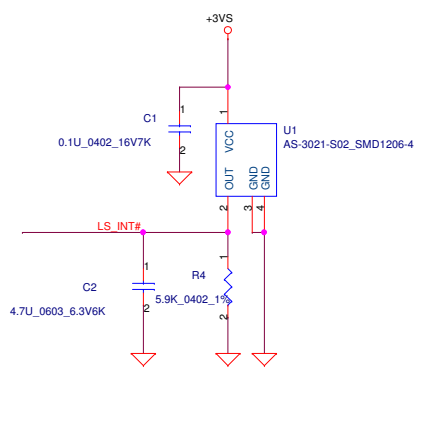
RSMRST circuit



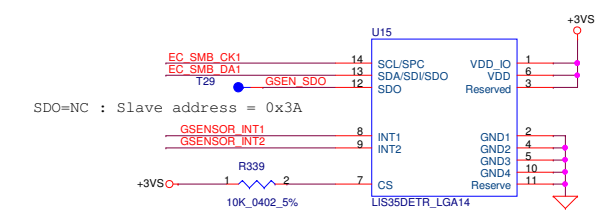
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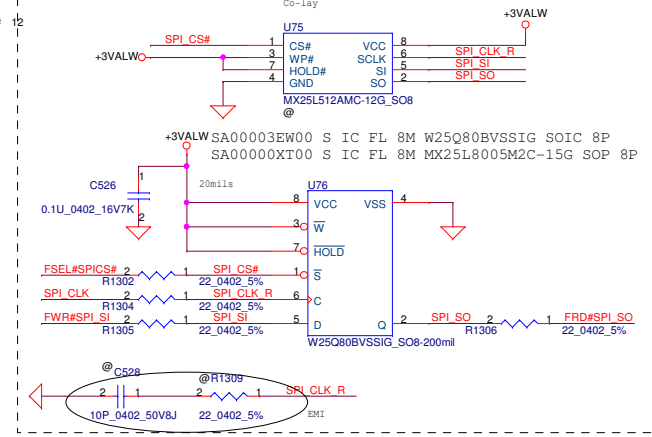
Light Sensor



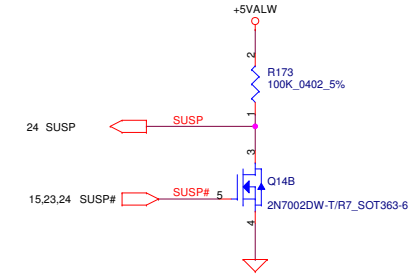
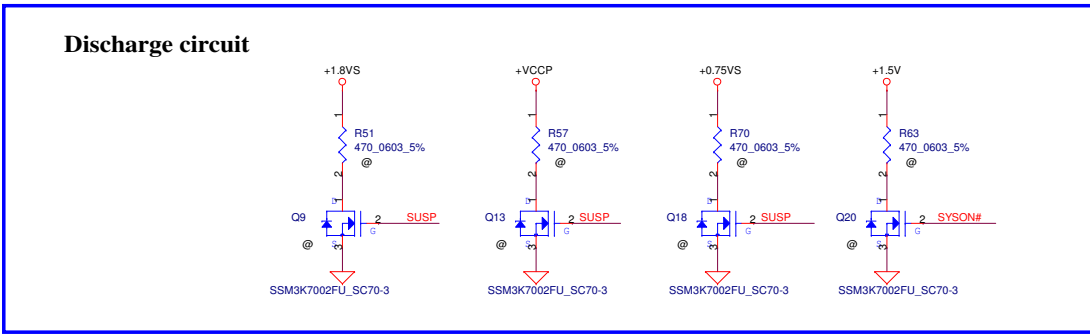
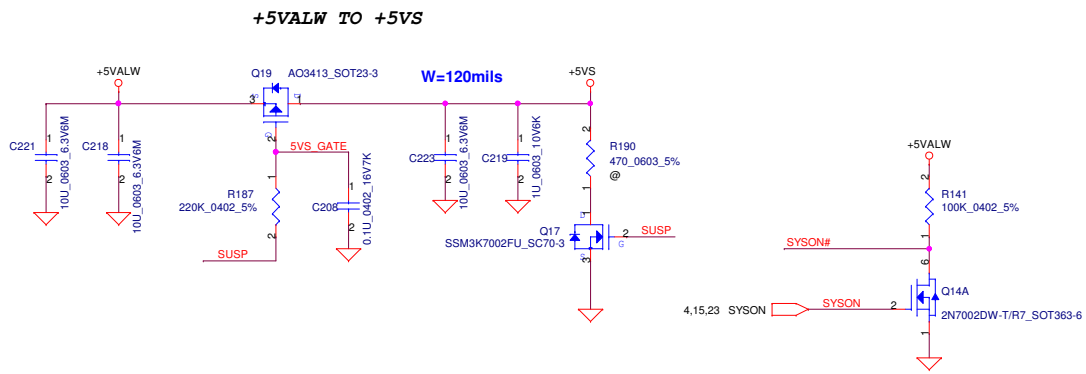
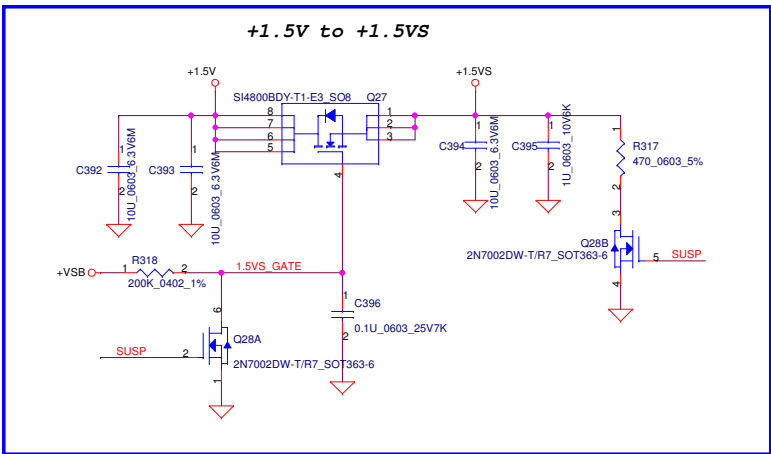
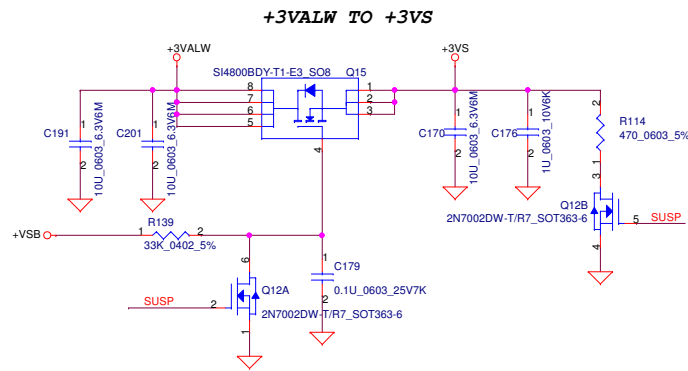
APS G-Sensor



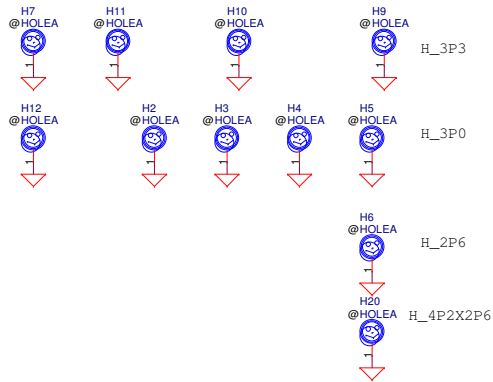
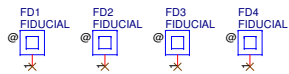
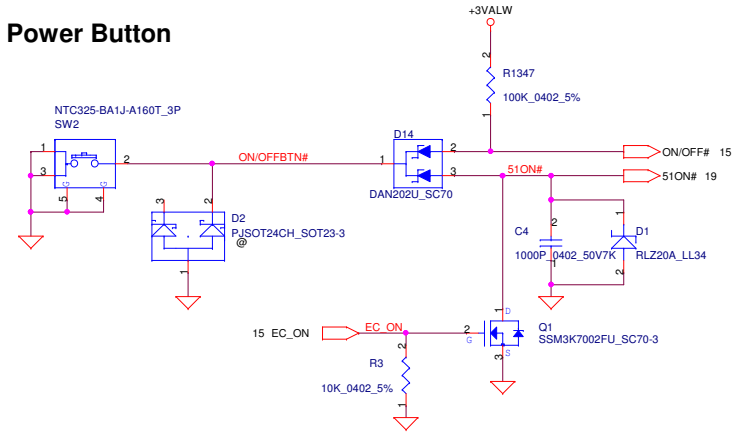
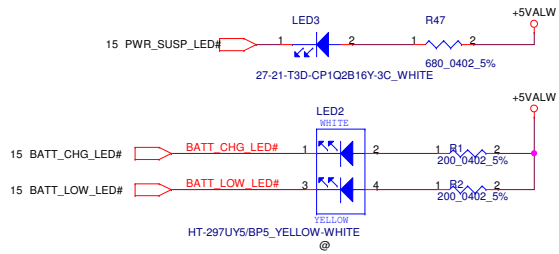
8M SPI ROM



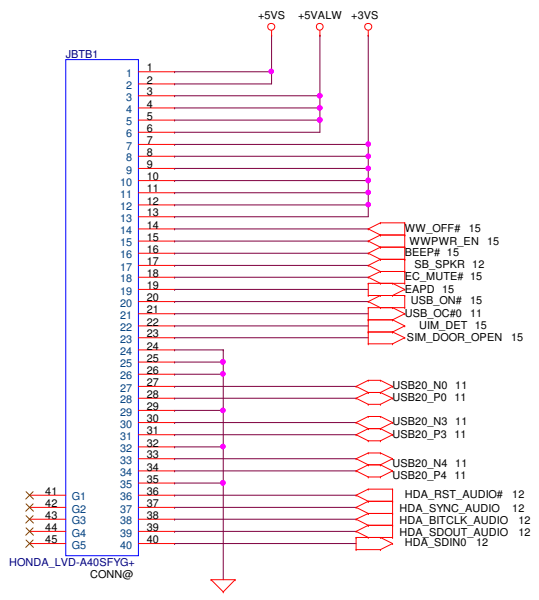
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Power Button

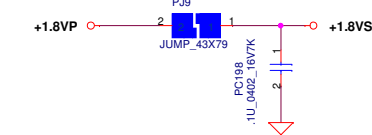
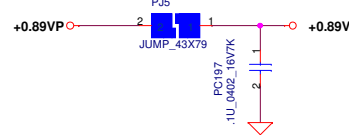
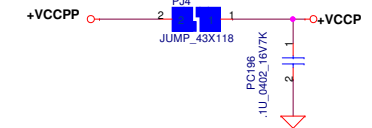
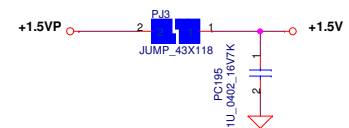
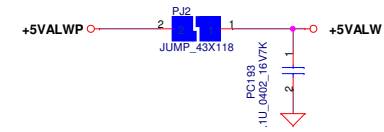
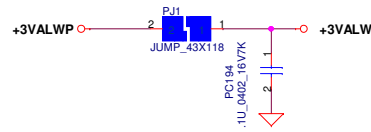
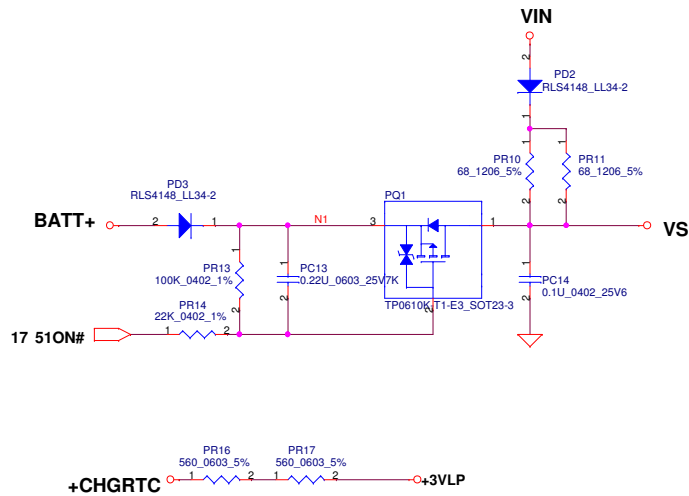
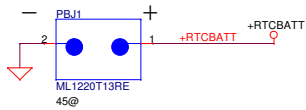
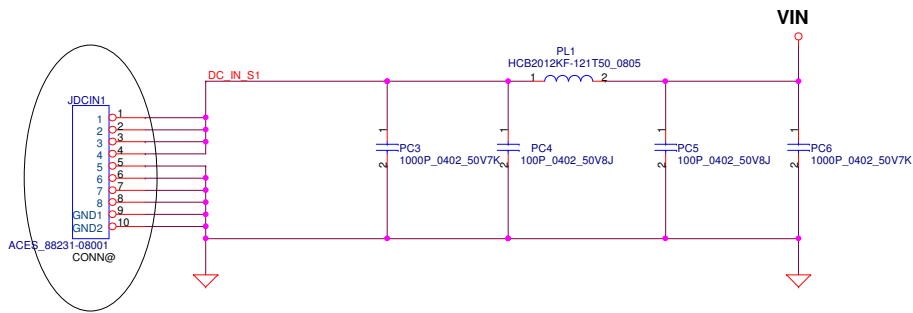


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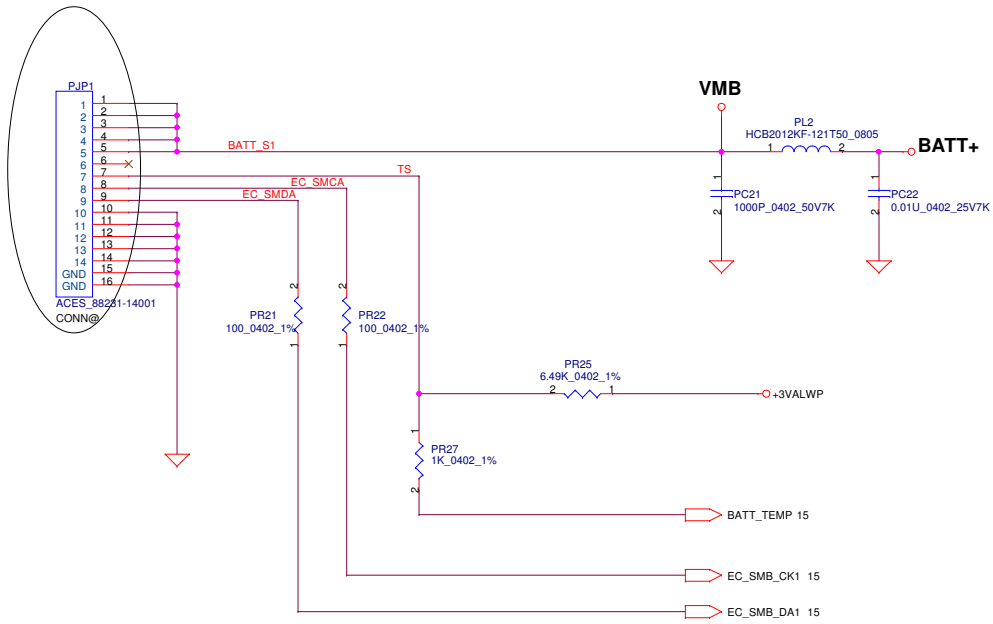


USB CONN
 CAM
 WWAN

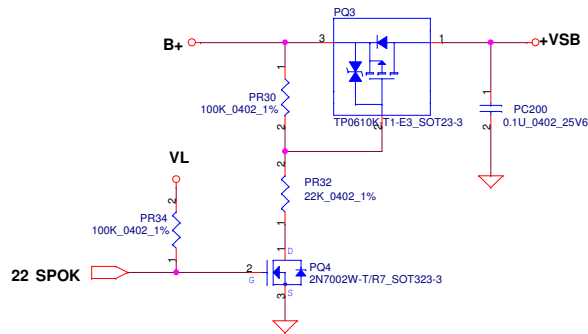
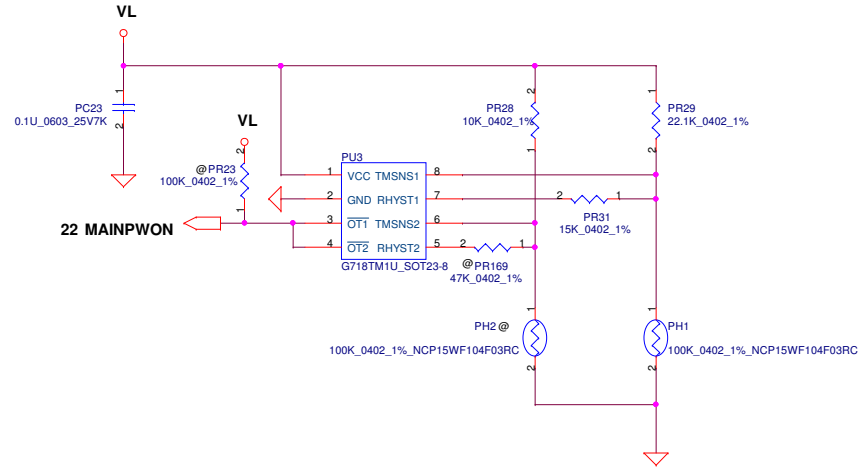
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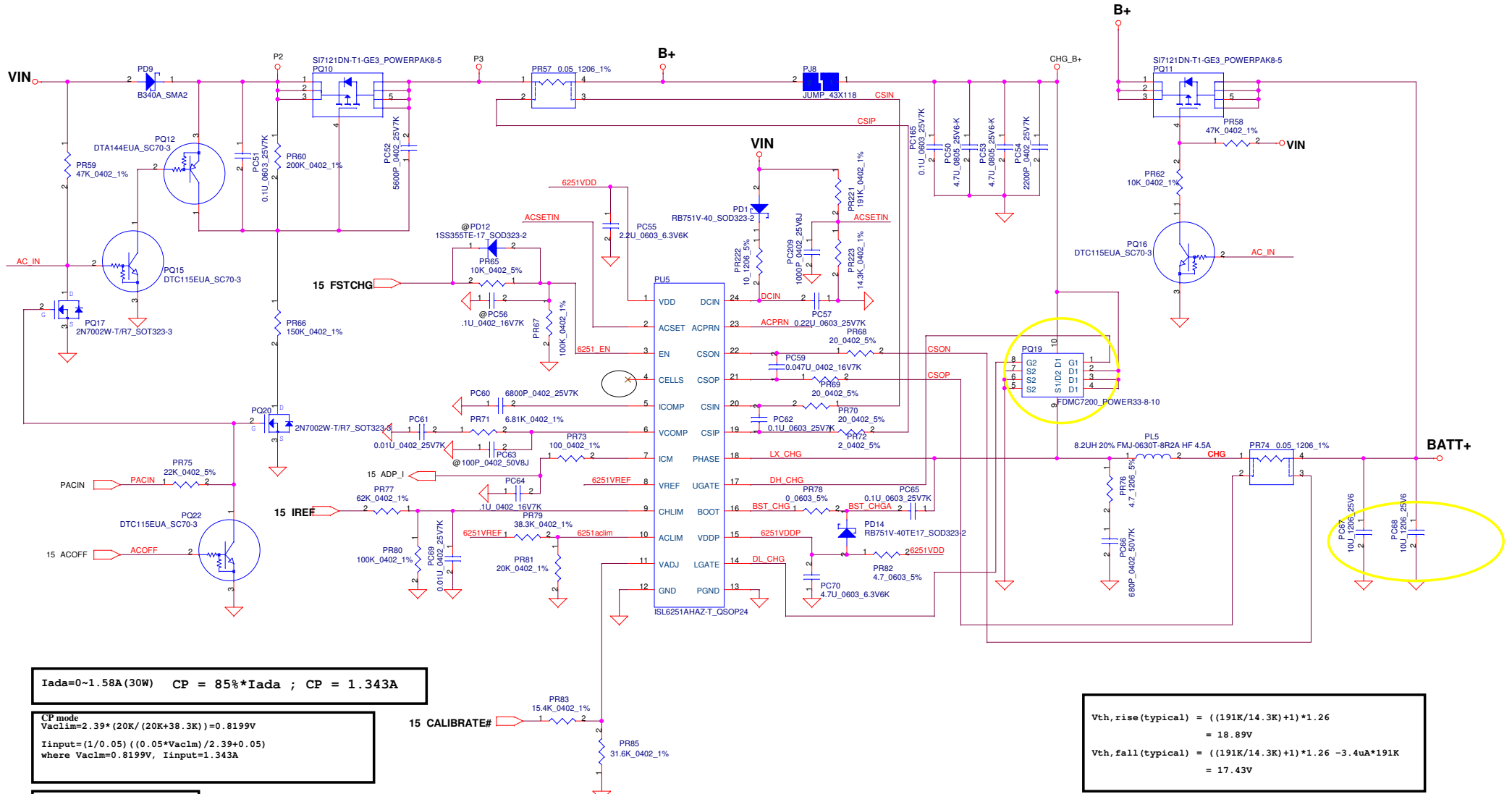
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PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 72 degree C



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$I_{ada} = 0 \sim 1.58A (30W)$ $CP = 85\% \cdot I_{ada}$; $CP = 1.343A$

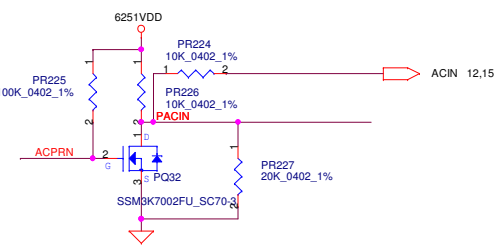
CP mode
 $V_{aclm} = 2.39 \cdot (20K / (20K + 38.3K)) = 0.8199V$
 $I_{input} = (1/0.05) \cdot ((0.05 \cdot V_{aclm}) / 2.39 + 0.05)$
 where $V_{aclm} = 0.8199V$, $I_{input} = 1.343A$

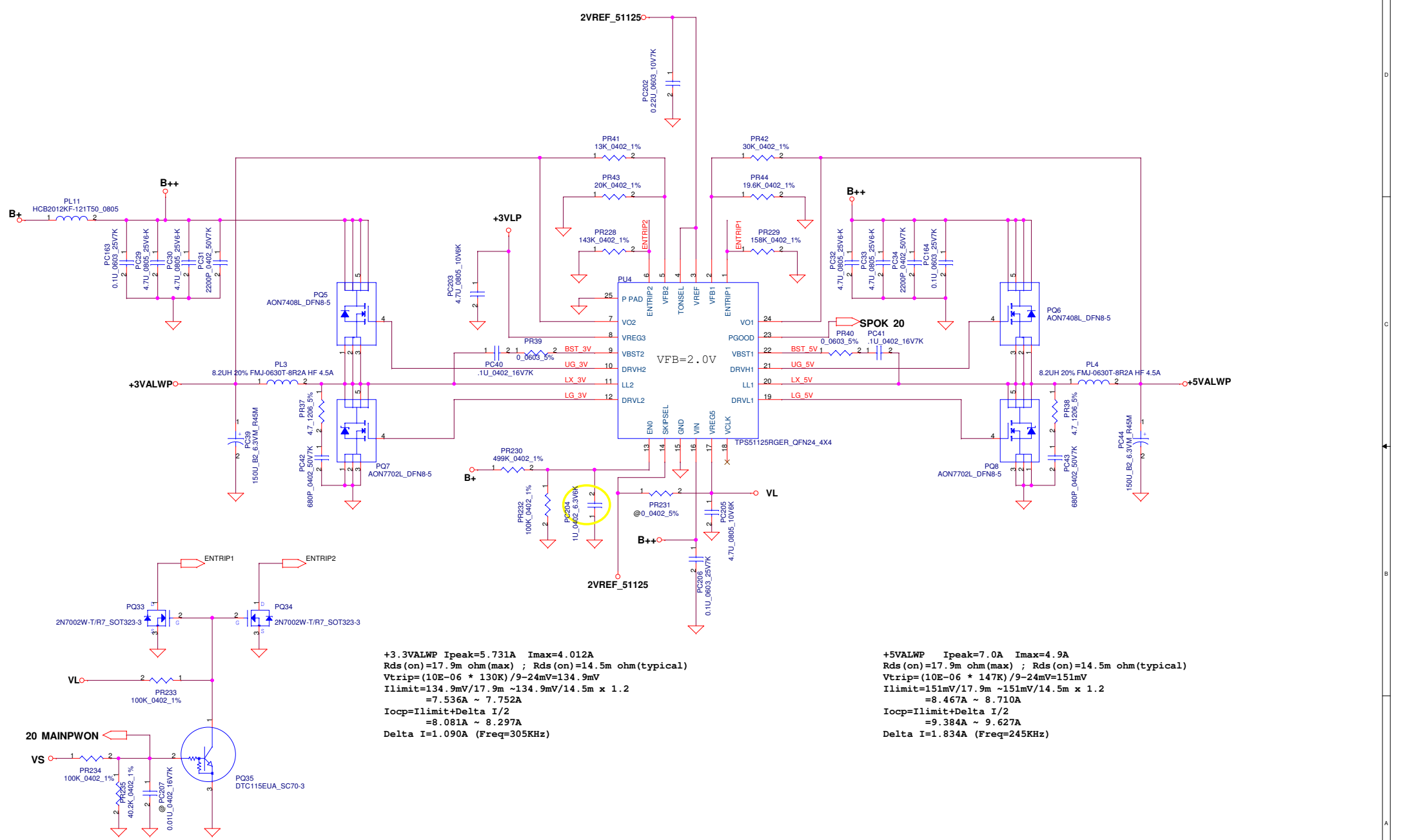
$CC = 0.3 \sim 1.76A$
 $I_{REF} = 1.62 \cdot I_{charge}$
 $I_{REF} = 0.486V \sim 2.85V$
 $3.24V \implies 2A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

$V_{ADJ} \rightarrow V_{REF} \rightarrow 4.41V$
 $V_{ADJ} \rightarrow \text{Ground} \rightarrow 3.39V$
 $V_{cell} = (0.175 \cdot V_{ADJ} + 3.99)$

$V_{th, rise (typical)} = ((191K / 14.3K) + 1) \cdot 1.26$
 $= 18.89V$
 $V_{th, fall (typical)} = ((191K / 14.3K) + 1) \cdot 1.26 - 3.4\mu A \cdot 191K$
 $= 17.43V$

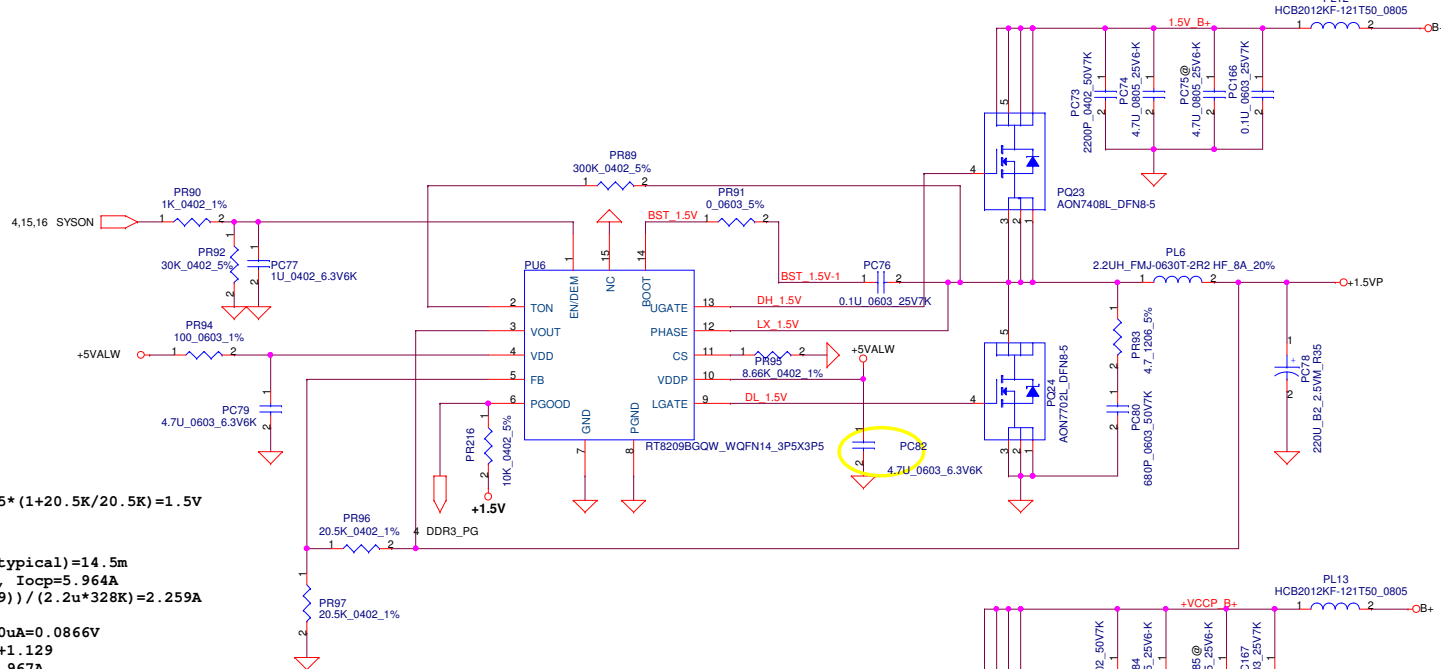




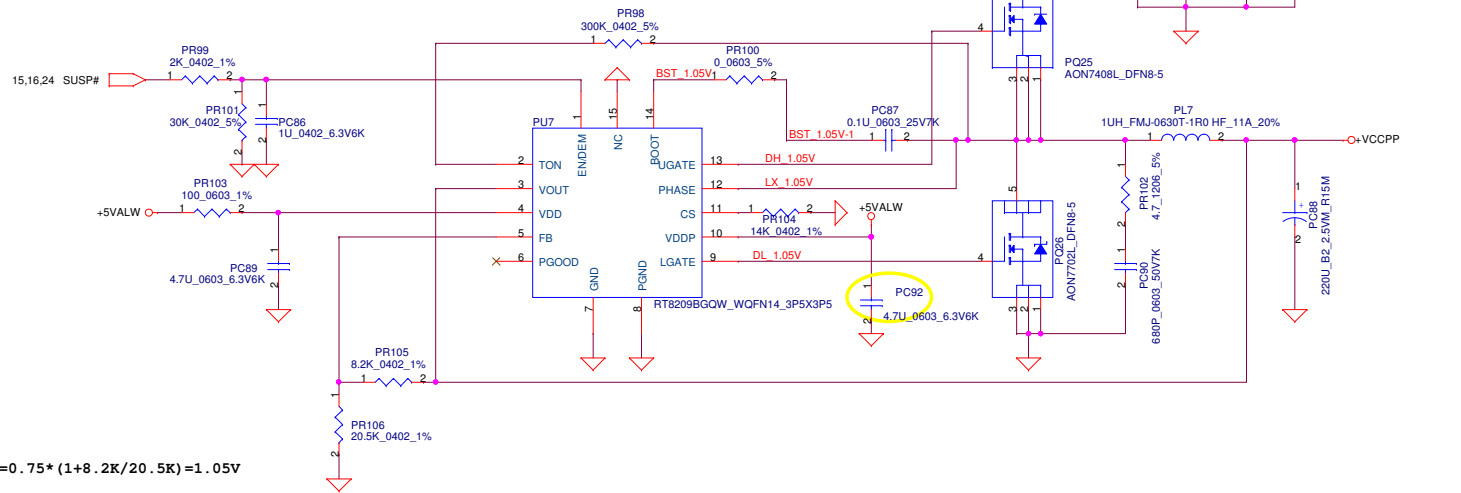
+3.3VALWP Ipeak=5.731A I_{max}=4.012A
 R_{ds(on)}=17.9m ohm(max) ; R_{ds(on)}=14.5m ohm(typical)
 V_{trip}=(10E-06 * 130K)/9-24mV=134.9mV
 I_{limit}=134.9mV/17.9m ~134.9mV/14.5m x 1.2
 =7.536A ~ 7.752A
 I_{ocp}=I_{limit}+Delta I/2
 =8.081A ~ 8.297A
 Delta I=1.090A (Freq=305KHz)

+5VALWP Ipeak=7.0A I_{max}=4.9A
 R_{ds(on)}=17.9m ohm(max) ; R_{ds(on)}=14.5m ohm(typical)
 V_{trip}=(10E-06 * 147K)/9-24mV=151mV
 I_{limit}=151mV/17.9m ~151mV/14.5m x 1.2
 =8.467A ~ 8.710A
 I_{ocp}=I_{limit}+Delta I/2
 =9.384A ~ 9.627A
 Delta I=1.834A (Freq=245KHz)

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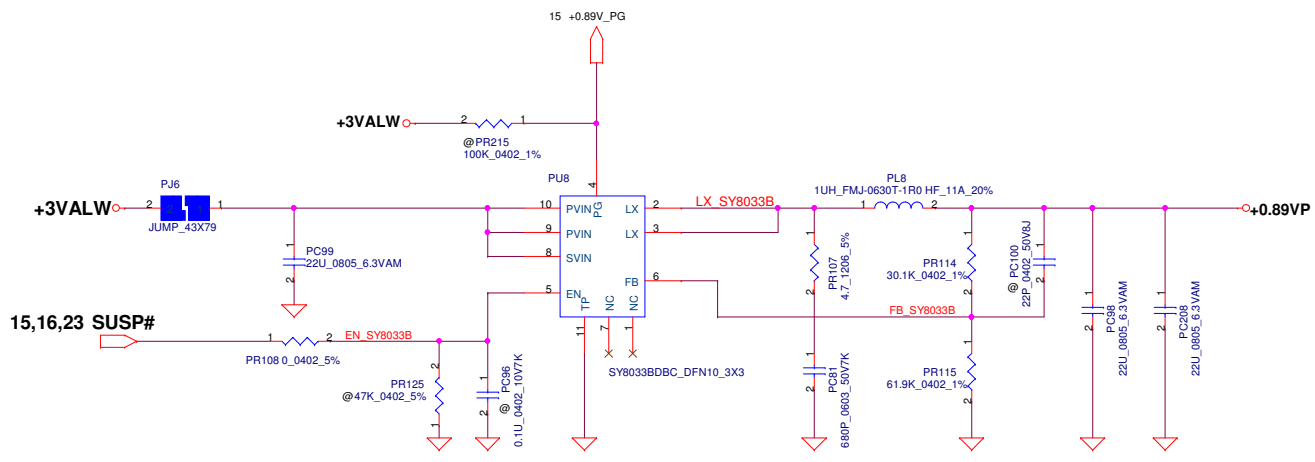


$V_o=1.5V$ $V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR96/PR97)=0.75 \cdot (1+20.5K/20.5K)=1.5V$
 $f_{sw}=328KHz$
 $C_{out} ESR=15m\ \Omega$
 $R_{dson(max)}=17.9m\ \Omega$ $R_{dson(typical)}=14.5m\ \Omega$
 $I_{peak}=4.97A$, $I_{max}=3.479A$, $I_{ocp}=5.964A$
 $\Delta I = ((19-1.8) \cdot (1.8/19)) / (2.2\mu \cdot 328K) = 2.259A$
 $\Rightarrow 1/2\Delta I = 1.129A$
 $V_{trip} = R_{trip} \cdot 10\mu A = 8.66K \cdot 10\mu A = 0.0866V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.129$
 $= 0.0866 / (0.0179) + 1.129 = 5.967A$
 $I_{ocpmax} = (0.0866 / (0.0145 \cdot 1.2)) + 1.129 = 6.106A$
 $I_{ocp} = 5.967A \sim 6.106A$

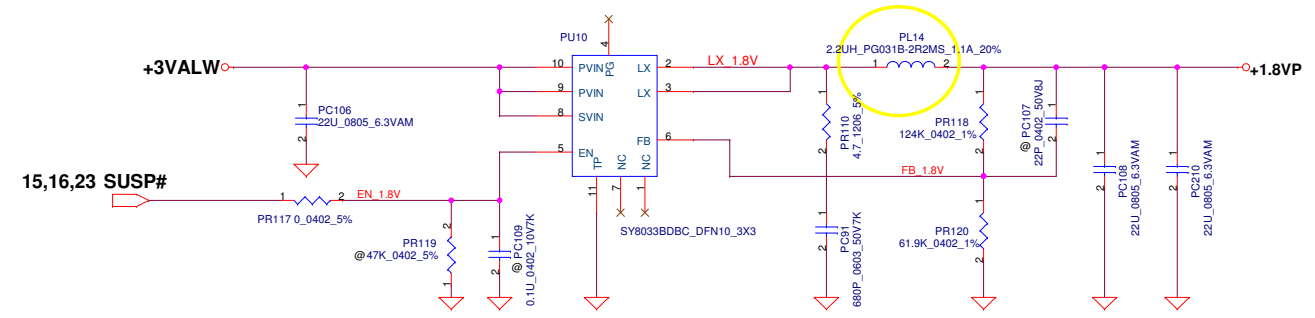


$V_o=1.05V$ $V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR105/PR106)=0.75 \cdot (1+8.2K/20.5K)=1.05V$
 $f_{sw}=280KHz$
 $C_{out} ESR=15m\ \Omega$ $R_{dson(max)}=17.9m\ \Omega$ $R_{dson(typical)}=14.5m\ \Omega$
 $I_{peak}=3.124A$, $I_{max}=2.187A$, $I_{ocp}=3.749A$
 $\Delta I = ((19-1.05) \cdot (1.05/19)) / (1.5\mu \cdot 280K) = 3.549A$
 $\Rightarrow 1/2\Delta I = 1.774A$
 $V_{trip} = R_{trip} \cdot 10\mu A = 14K \cdot 10\mu A = 0.14V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.774$
 $= 0.14 / (0.0179) + 1.774 = 9.596A$
 $I_{ocpmax} = (0.14 / (0.0145 \cdot 1.2)) + 1.774 = 9.820A$
 $I_{ocp} = 9.596A \sim 9.820A$

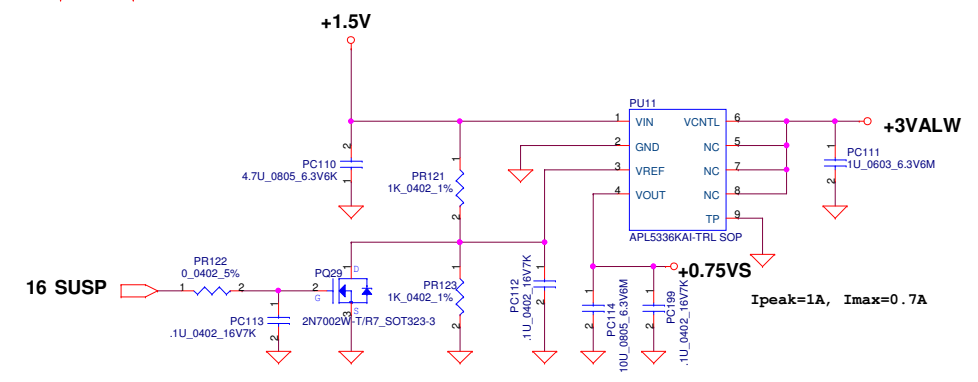
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$\langle V_o = 0.89V \rangle$ $V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR114 / PR115) = 0.6 * (1 + 30.1K / 61.9) = 0.89V$
 $I_{peak} = 2.64A$, $I_{max} = 1.848A$

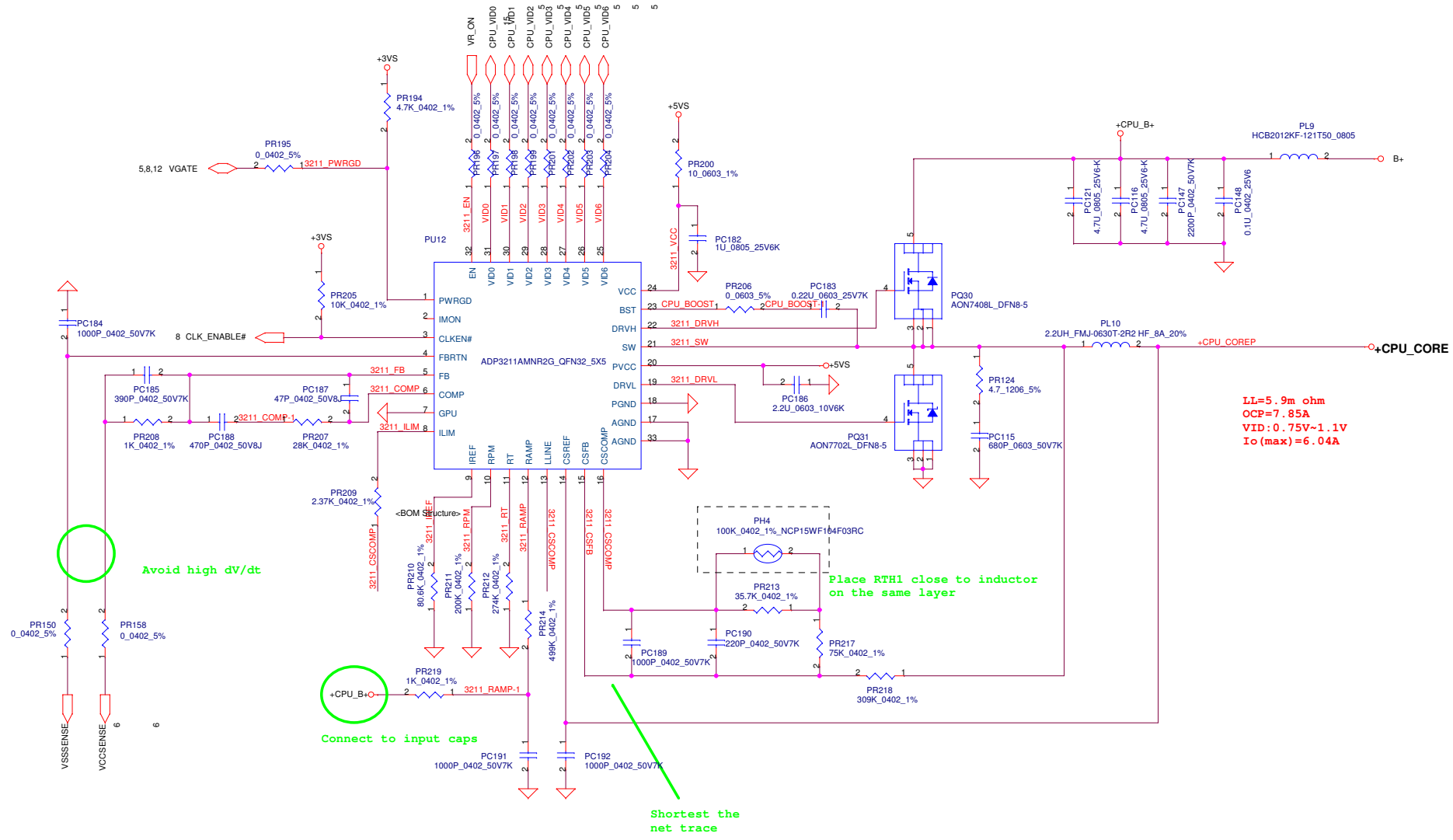


$\langle V_o = 1.8VP \rangle$ $V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR118 / PR120) = 0.6 * (1 + 124K / 61.9) = 1.8VP$
 $I_{peak} = 0.318A$, $I_{max} = 0.223A$



$I_{peak} = 1A$, $I_{max} = 0.7A$

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LI=5.9m ohm
 OCP=7.85A
 VID:0.75V~1.1V
 Io(max)=6.04A

Avoid high dv/dt

Connect to input caps

Shortest the net trace

Place RTH1 close to inductor on the same layer

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