Garda-3 Block Diagram

(Discrete)

Project code: 91.4P401.001
PCB P/N : 55.4P401.XXX
REVISION : 06208-2
(Hannstar, GCE)

DATE:2006/0?/??

CLK GEN.
IDT CV125PA
(ICS 954206) 3

Mobile CPU
Yonah 478
4, 5

G791/G792
19

HOST BUS 400/533/667MHz

DDR2
533 MHz
11,12

DDR2
533 MHz
11,12

533/667MHz

533/667MHz

Calistoga
Ver.:A2 :71.945PM.00U / QK46
6,7,8,9,10

PCI Express x16

M56 Ver.: B24
M52 Ver.: A12
M54 Ver.: A12

ATI
M54P / M52P
45,46,47,48,49

VRAM x4
128/256M 50,51

LVDS

TVO 14

14"WSXGA+ LCD 13

RGB CRT

CRT 14

DMI I/F 100MHz

ICH7M
Ver. : B0, 71.ICH7M.A0U / QK65
15,16,17,18

Line In
30

MIC In
30

INT.MIC

Codec
ALC883
29

AZALIA

Line Out
(SPDIF)
30

OP AMP
MAX4411
30

30
INT.SPKR

OP AMP
G1432Q
30

RJ11

MODEM
MDC Card
21

PCI Express

New card
31

PWR SW
TPS2231 31

SATA

PATA

HDD 20

CDROM 20

USB
3 PORT 21

MINI USB 21
Blue-tooth

PCI BUS

ENE CB1410
CARDBUS
24,25

PCMCIA I/F

PWR SW
TPS2211
25

PCMCIA
SLOT
Support
TypeII 25

RICOH
R5C832
1394
CardReader
27,28

1394
CONN 28

MS/MS Pro/xD/
MMC/SD/SDIO
6 in 1 28

Mini-PCI
802.11A/B/G 31

LAN
GIGA or 10/100
RTL8110 or RTL8100CL
22

TXFM
23

RJ45 23

PCIEx1

Mini Card*1
802.11A/B/G 26

SPI I/F

BIOS
SST25LF080A
35

LPC BUS

SIO
NS87381
34

FIR 34

KBC
Renesas
RE144B
32

Touch Pad 33

INT. KB 33

Thermal
G792SFUF
FAN CONN
19

LPC
DEBUG
CONN. 35

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM
TPS51120 40

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC
APL5912 43

INPUTS	OUTPUTS
1D8V_S3	1D05V_S0

TPS51116 41

DCBATOUT	1D8V_S3 DDR_VREF_S0

APL5332KAC

3D3V_S0	2D5V_S0 43

APL5912

1D8V_S3	1D5V_S0 43

MAXIM CHARGER
ISL6255 42

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU
ISL6262 38,39

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 44A

ATI M52 DC/DC
ISL6269 52

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

APL5331 43

1D8V_S0	1D2V_S0

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
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Date: Thursday, April 20, 2006 Sheet 1 of 55

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
1410	22	A->G	0
MiniPCI	21	A/C -> E B/D -> E	1
LAN	23	A -> H	2
1394	17	A->B, B->F,	3

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

History

BOM

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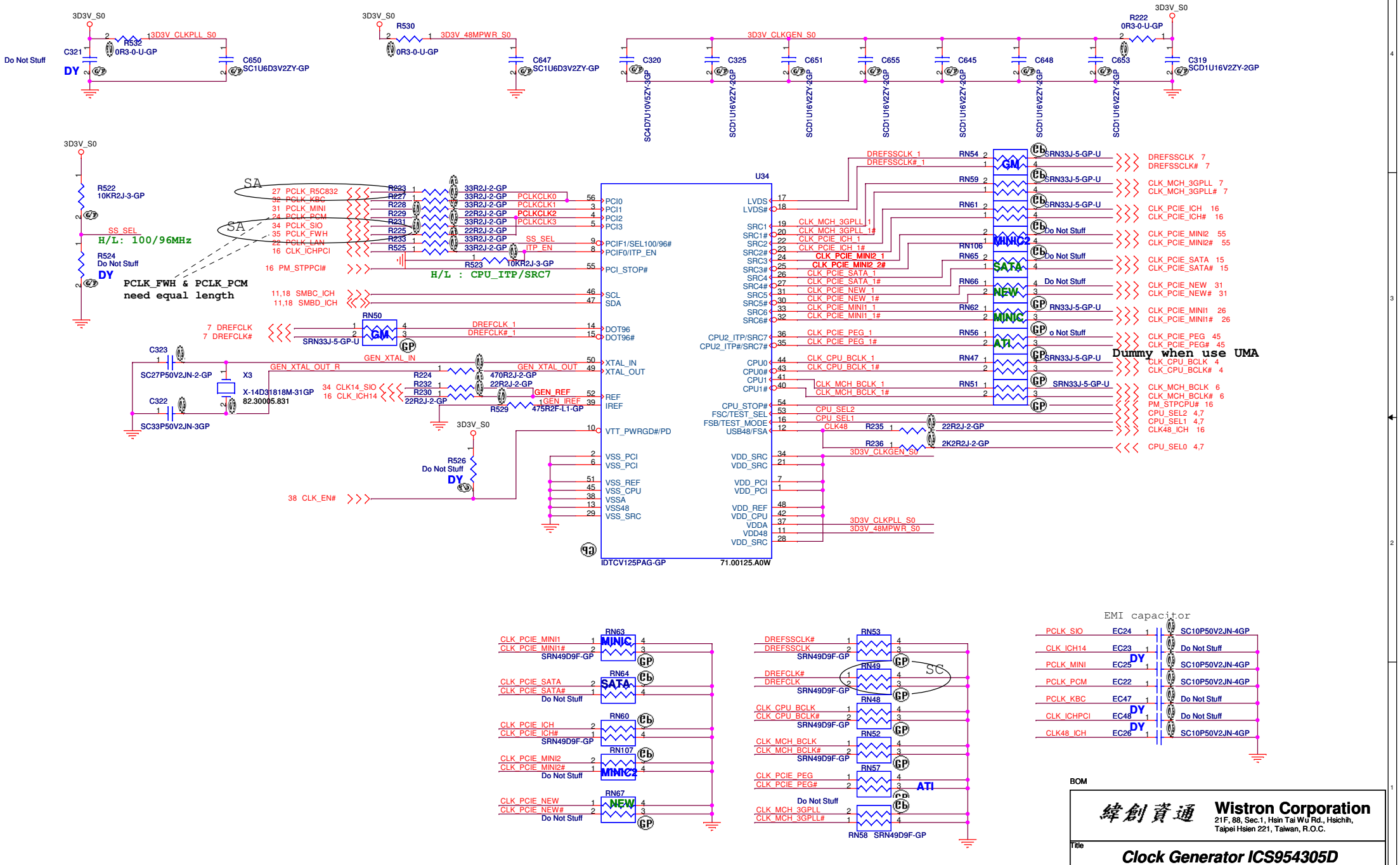
Title: Reference

Size: A3 | Document Number: AG3 | Rev: 2

Date: Thursday, April 20, 2006 | Sheet 2 of 55


3D3V_S0
R532 0R3-0-U-GP
3D3V_CLKPLL_S0
C321 Do Not Stuff DY
C650 SC1U6D3V2ZY-GP
R530 0R3-0-U-GP
3D3V_48MPWR_S0
C647 SC1U6D3V2ZY-GP
3D3V_CLKGEN_S0
C320 SC4D7U10V5ZY-3GP
C325 C651 C655 C645 C648 SCD1U16V2ZY-2GP
C653 SCD1U16V2ZY-2GP
R222 0R3-0-U-GP
C319 SCD1U16V2ZY-2GP
R522 10KR2J-3-GP
R524 Do Not Stuff DY
SS_SEL
H/L: 100/96MHz
PCLK_FWH & PCLK_PCM
need equal length
SA
27 PCLK_R5C832
32 PCLK_KBC
31 PCLK_MINI
24 PCLK_PCM
34 PCLK_SIO
35 PCLK_FWH
22 PCLK_LAN
16 CLK_ICHPCI
16 PM_STPPCI#
R223 R227 R228 R229 R231 R225 R233 R525 33R2J-2-GP
22R2J-2-GP
PCLKCLK0
PCLKCLK1
PCLKCLK2
PCLKCLK3
SS_SEL
ITP_EN
R523 10KR2J-3-GP
H/L : CPU_ITP/SRC7
11,18 SMBC_ICH
11,18 SMBD_ICH
7 DREFCLK
7 DREFCLK#
RN50 SRN33J-5-GP-U
DREFCLK_1
DREFCLK#_1
C323 SC27P50V2JN-2-GP
C322 SC33P50V2JN-3GP
X3 X-14D31818M-31GP 82.30005.831
GEN_XTAL_OUT_R
GEN_XTAL_IN
GEN_XTAL_OUT
R224 470R2J-2-GP
R232 22R2J-2-GP
R230 22R2J-2-GP
34 CLK14_SIO
16 CLK_ICH14
GEN_REF
GEN_IREF
R529 475R2F-L1-GP
R526 Do Not Stuff DY
38 CLK_EN#
U34
PCI0 PCI1 PCI2 PCI3
PCIF1/SEL100/96#
PCIF0/ITP_EN
PCI_STOP#
SCL SDA
DOT96 DOT96#
XTAL_IN XTAL_OUT
REF IREF
VTT_PWRGD#/PD
VSS_PCI VSS_PCI VSS_REF VSS_CPU VSSA VSS48 VSS_SRC
LVDS LVDS#
SRC1 SRC1# SRC2 SRC2# SRC3 SRC3# SRC4 SRC4# SRC5 SRC5# SRC6 SRC6#
CPU2_ITP/SRC7 CPU2_ITP#/SRC7#
CPU0 CPU0# CPU1 CPU1#
CPU_STOP# FSC/TEST_SEL FSB/TEST_MODE USB48/FSA
VDD_SRC VDD_SRC VDD_PCI VDD_PCI VDD_REF VDD_CPU VDDA VDD48 VDD_SRC
IDTCV125PAG-GP 71.00125.A0W
DREFSSCLK_1 DREFSSCLK#_1
CLK_MCH_3GPLL_1 CLK_MCH_3GPLL_1#
CLK_PCIE_ICH_1 CLK_PCIE_ICH_1#
CLK_PCIE_MINI2_1 CLK_PCIE_MINI2_2#
CLK_PCIE_SATA_1 CLK_PCIE_SATA_1#
CLK_PCIE_NEW_1 CLK_PCIE_NEW_1#
CLK_PCIE_MINI1_1 CLK_PCIE_MINI1_1#
CLK_PCIE_PEG_1 CLK_PCIE_PEG_1#
CLK_CPU_BCLK_1 CLK_CPU_BCLK_1#
CLK_MCH_BCLK_1 CLK_MCH_BCLK_1#
CPU_SEL2 CPU_SEL1
CLK48 R235 22R2J-2-GP R236 2K2R2J-2-GP
3D3V_CLKGEN_S0
3D3V_CLKPLL_S0
3D3V_48MPWR_S0
RN54 RN59 RN61 RN106 RN65 RN66 RN62 RN56 RN47 RN51 SRN33J-5-GP-U
GM MINIC2 SATA NEW MINIC ATI
Do Not Stuff
DREFSSCLK_7 DREFSSCLK#_7
CLK_MCH_3GPLL_7 CLK_MCH_3GPLL#_7
CLK_PCIE_ICH_16 CLK_PCIE_ICH#_16
CLK_PCIE_MINI2_55 CLK_PCIE_MINI2#_55
CLK_PCIE_SATA_15 CLK_PCIE_SATA#_15
CLK_PCIE_NEW_31 CLK_PCIE_NEW#_31
CLK_PCIE_MINI1_26 CLK_PCIE_MINI1#_26
CLK_PCIE_PEG_45 CLK_PCIE_PEG#_45
CLK_CPU_BCLK_4 CLK_CPU_BCLK#_4
CLK_MCH_BCLK_6 CLK_MCH_BCLK#_6
PM_STPCPU#_16
CPU_SEL2_4,7
CPU_SEL1_4,7
CLK48_ICH_16
CPU_SEL0_4,7
Dummy when use UMA
RN63 SRN49D9F-GP
CLK_PCIE_MINI1 CLK_PCIE_MINI1#
RN64 Do Not Stuff
CLK_PCIE_SATA CLK_PCIE_SATA#
RN60 SRN49D9F-GP
CLK_PCIE_ICH CLK_PCIE_ICH#
RN107 Do Not Stuff
CLK_PCIE_MINI2 CLK_PCIE_MINI2#
RN67 Do Not Stuff
CLK_PCIE_NEW CLK_PCIE_NEW#
RN53 SRN49D9F-GP
DREFSSCLK# DREFSSCLK
RN49 SRN49D9F-GP
DREFCLK# DREFCLK
SC
RN48 SRN49D9F-GP
CLK_CPU_BCLK CLK_CPU_BCLK#
RN52 SRN49D9F-GP
CLK_MCH_BCLK CLK_MCH_BCLK#
RN57 ATI
CLK_PCIE_PEG CLK_PCIE_PEG#
Do Not Stuff
RN58 SRN49D9F-GP
CLK_MCH_3GPLL CLK_MCH_3GPLL#
EMI capacitor
PCLK_SIO EC24 SC10P50V2JN-4GP
CLK_ICH14 EC23 Do Not Stuff
PCLK_MINI EC25 DY SC10P50V2JN-4GP
PCLK_PCM EC22 SC10P50V2JN-4GP
PCLK_KBC EC47 Do Not Stuff
CLK_ICHPCI EC48 DY Do Not Stuff
CLK48_ICH EC26 DY SC10P50V2JN-4GP
BOM
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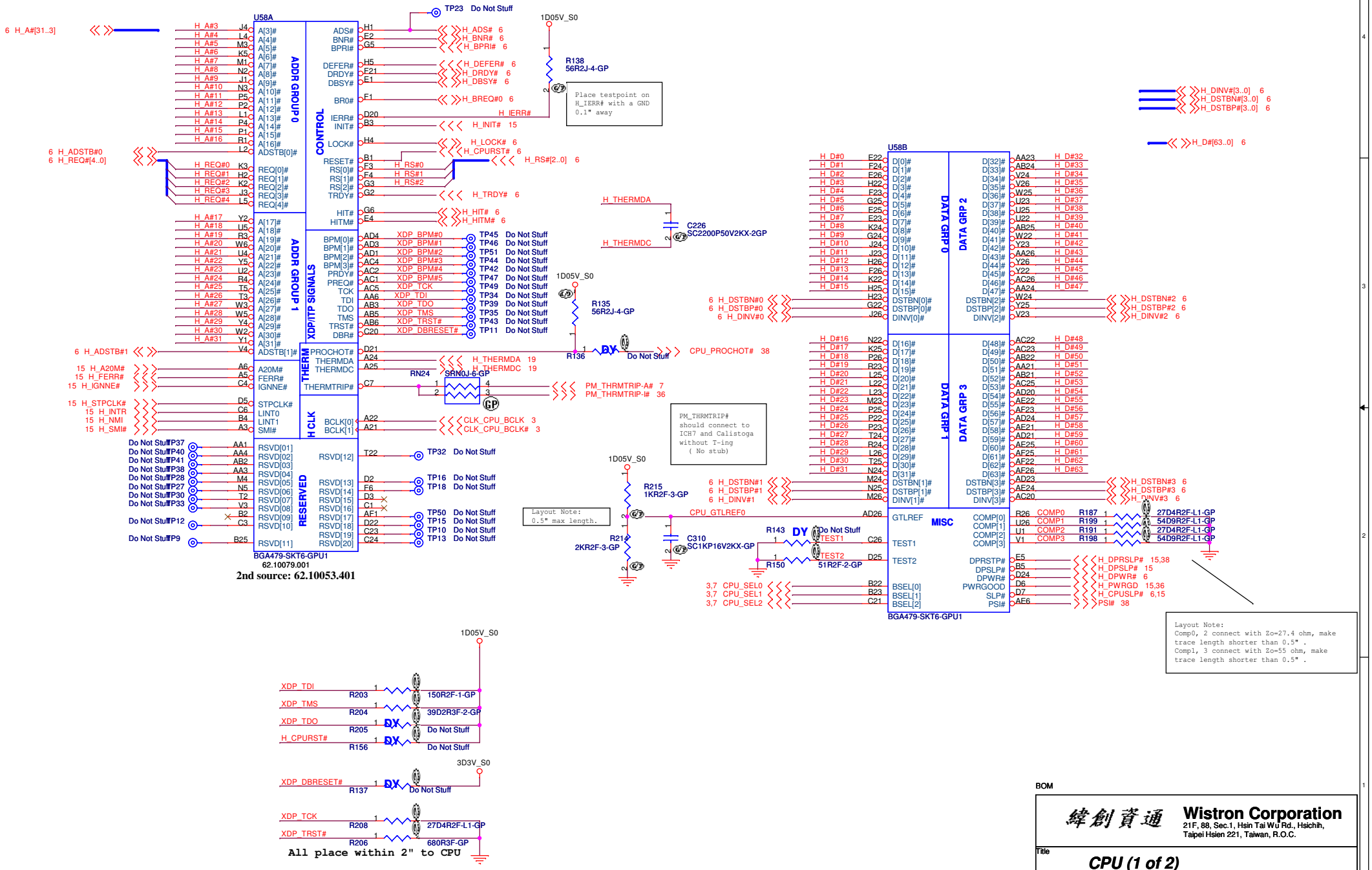
Title
Clock Generator ICS954305D
Size A3
Document Number AG3
Rev 2
Date: Friday, April 21, 2006
Sheet 3 of 55



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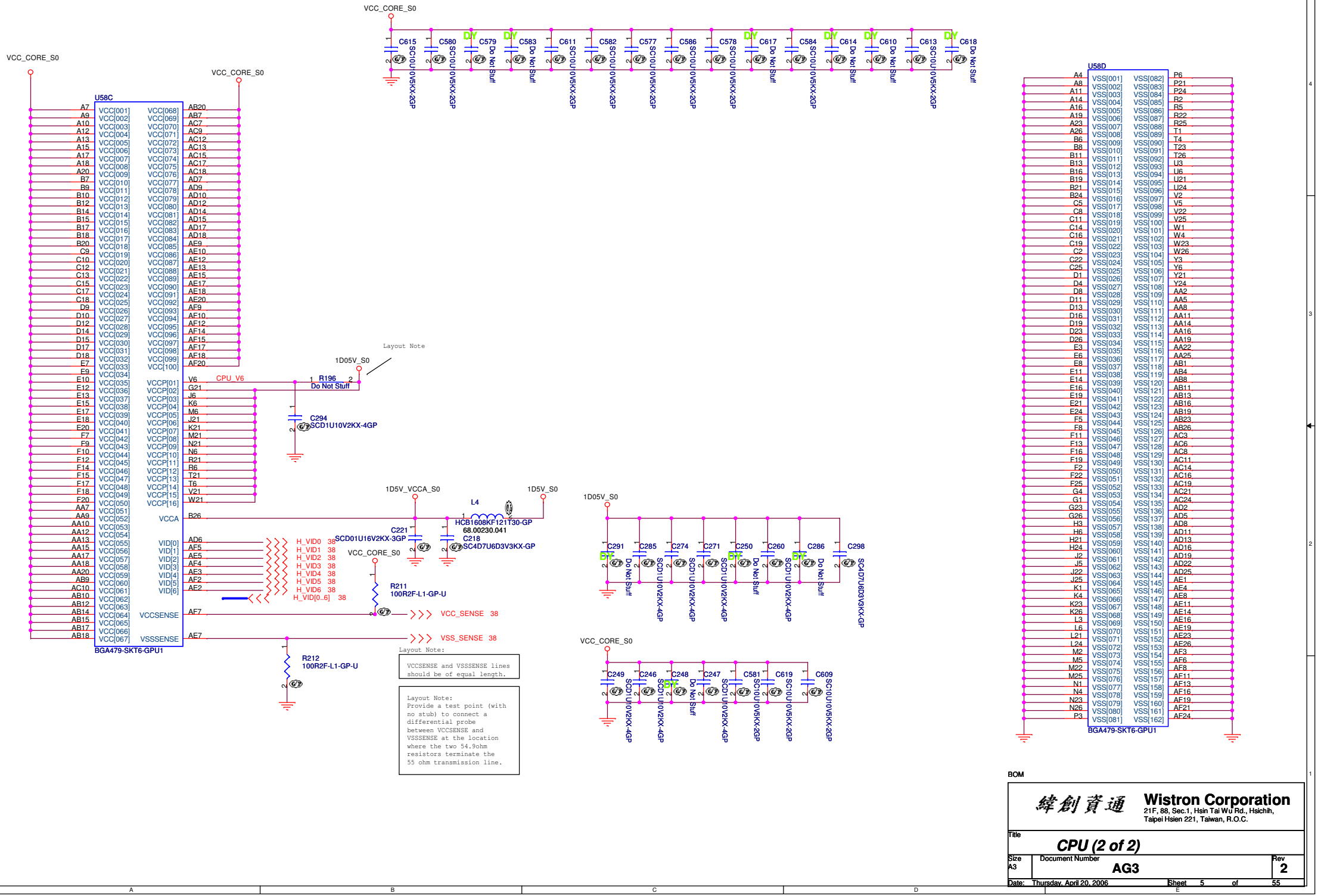
Title: **CPU (1 of 2)**

Size	Document Number	Rev
A3	AG3	2

Date: Thursday, April 20, 2006 Sheet 4 of 55



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Title: ***CPU (2 of 2)***

Size	Document Number	Rev
A3	AG3	2

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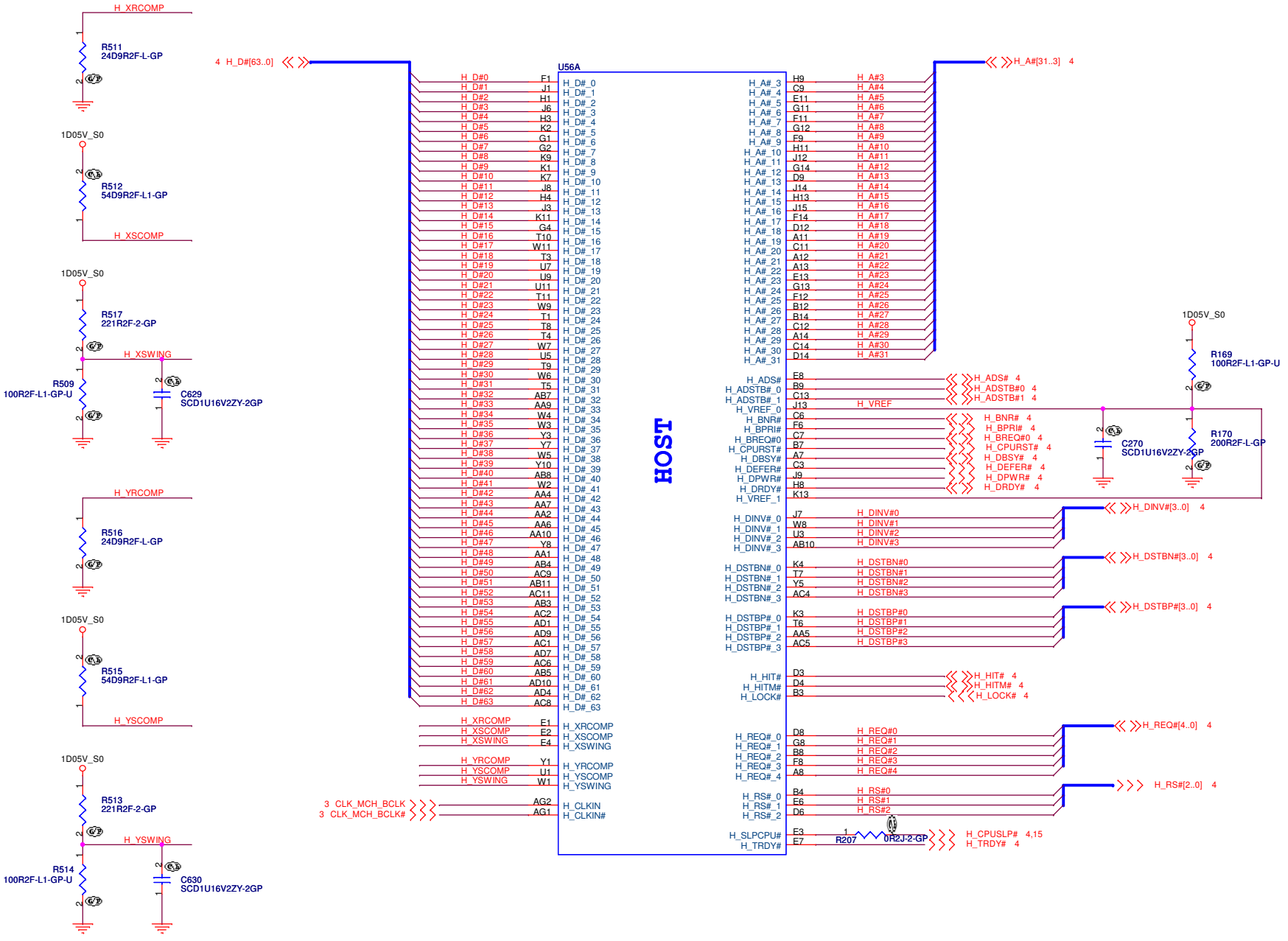

Place them near to the chip (< 0.5")

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Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
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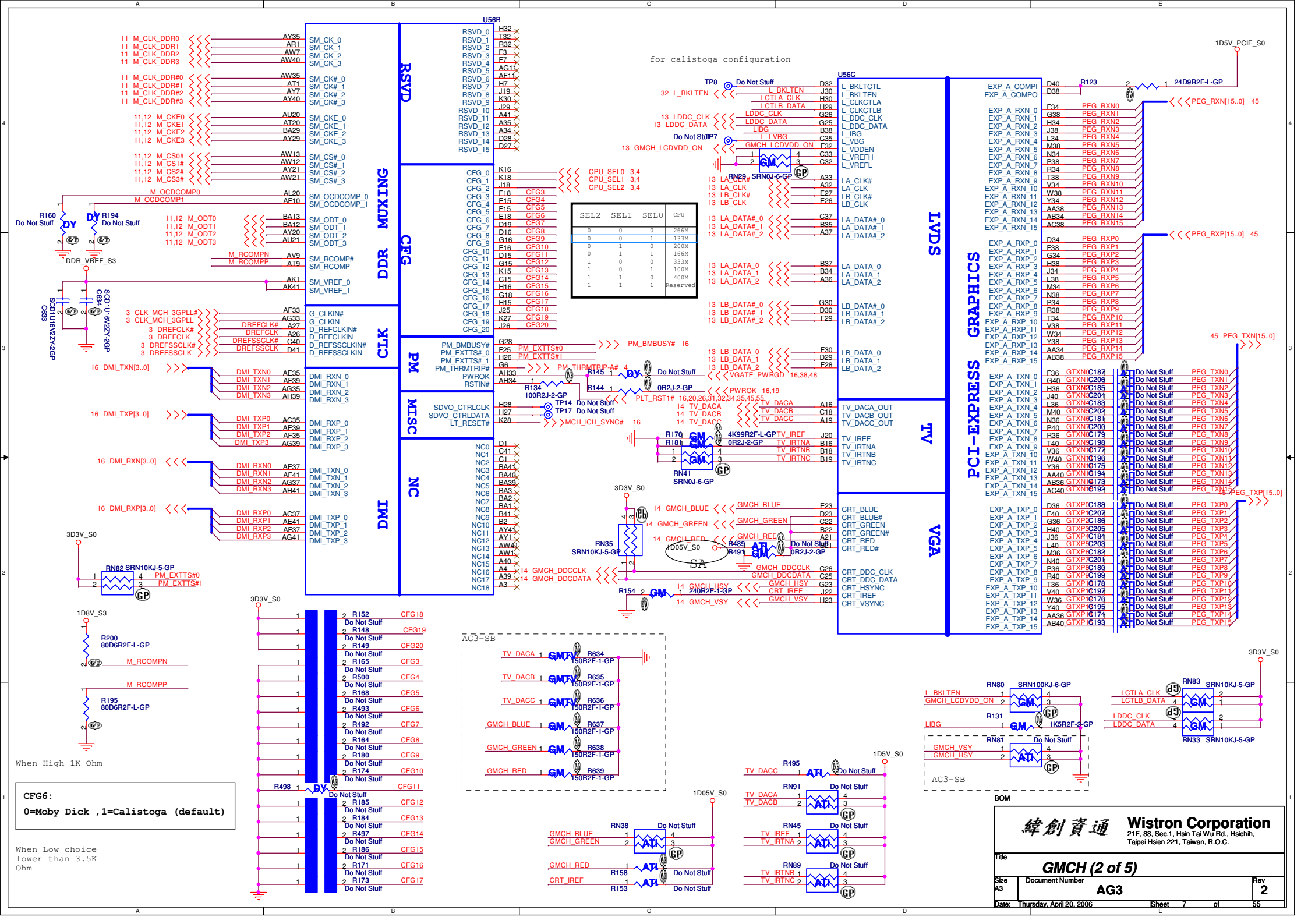
for calistoga configuration
U56B
U56C
DDR MUXING
CFG
CLK
PM
MISC
NC
DMI
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
SEL2 SEL1 SEL0 CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
CFG6:
0=Moby Dick ,1=Calistoga (default)
When High 1K Ohm
When Low choice lower than 3.5K Ohm
AG3-SB
BOM
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GMCH (2 of 5)
Size A3
Document Number AG3
Rev 2
Date: Thursday, April 20, 2006
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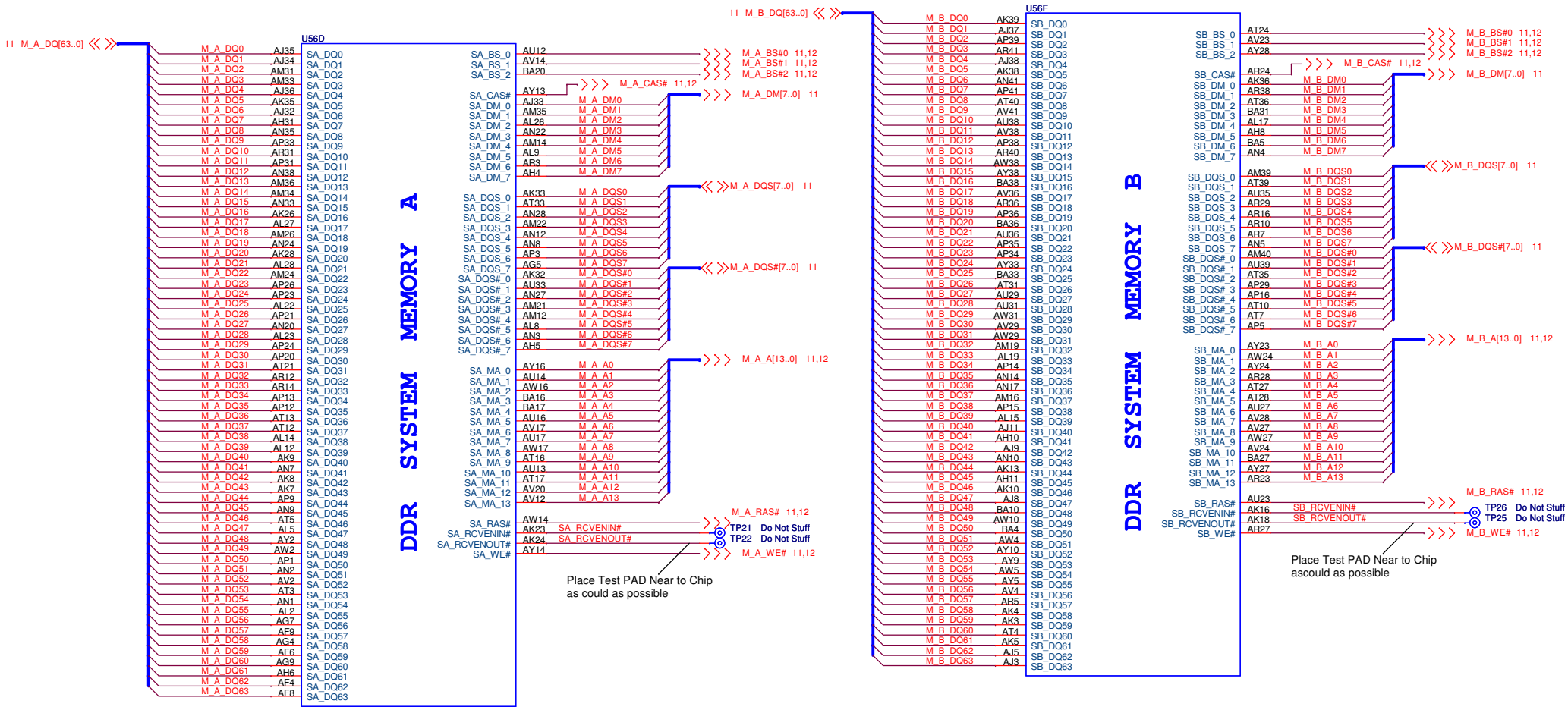

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Title: **GMCH (3 of 5)**

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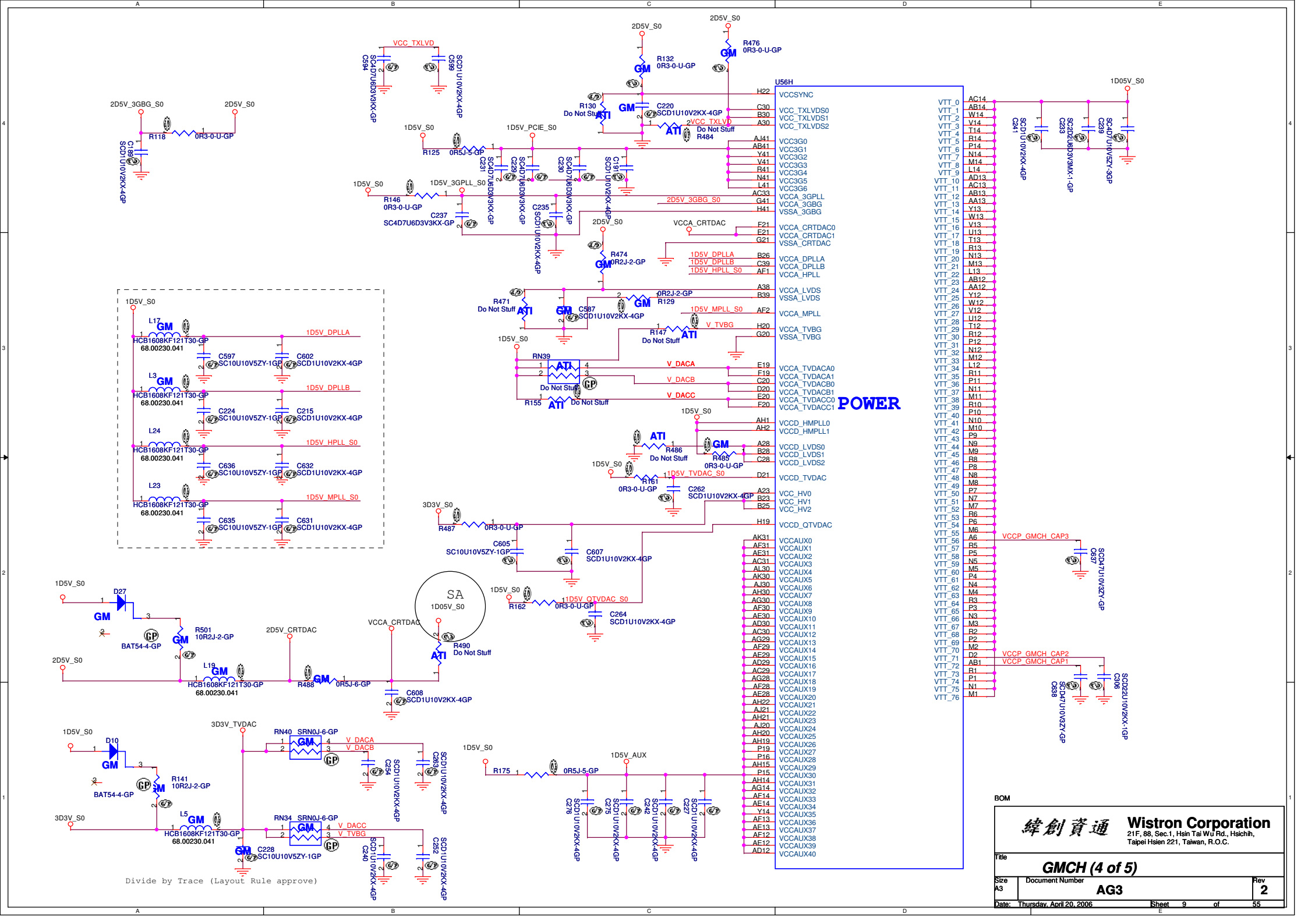
U56H
POWER
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
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VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
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VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
VCC_TXLVD
2D5V_S0
1D5V_S0
1D5V_PCIE_S0
2D5V_3GBG_S0
1D5V_3GPLL_S0
VCCA_CRTDAC
1D5V_DPLLA
1D5V_DPLLB
1D5V_HPLL_S0
V_TVBG
1D5V_MPLL_S0
V_DACA
V_DACB
V_DACC
1D5V_TVDAC_S0
3D3V_S0
1D5V_QTVDAC_S0
1D5V_AUX
VCCP_GMCH_CAP3
VCCP_GMCH_CAP2
VCCP_GMCH_CAP1
2D5V_CRTDAC
3D3V_TVDAC
SA
Do Not Stuff
Divide by Trace (Layout Rule approve)
BOM
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Title
GMCH (4 of 5)
Size
A3
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Date: Thursday, April 20, 2006
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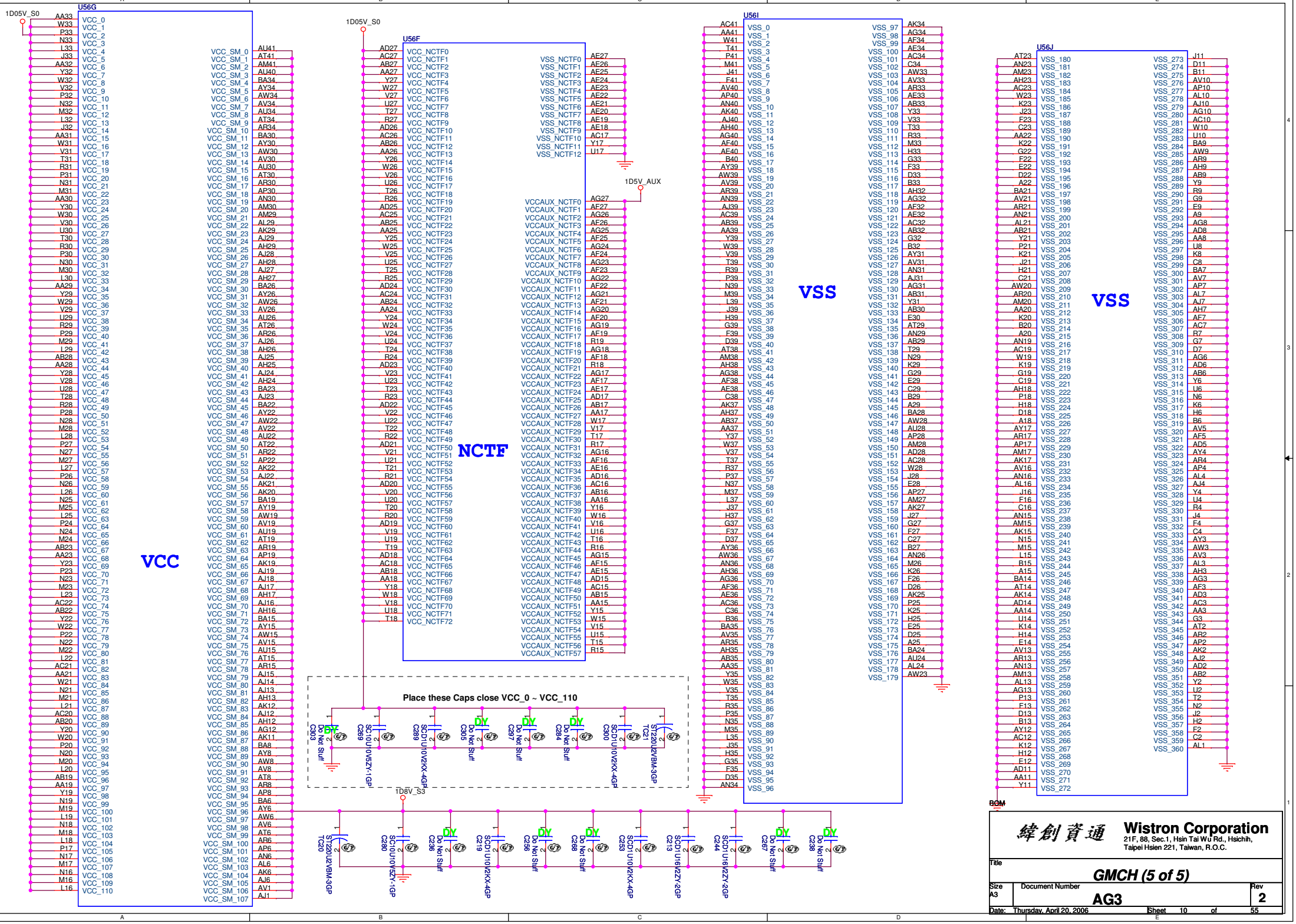
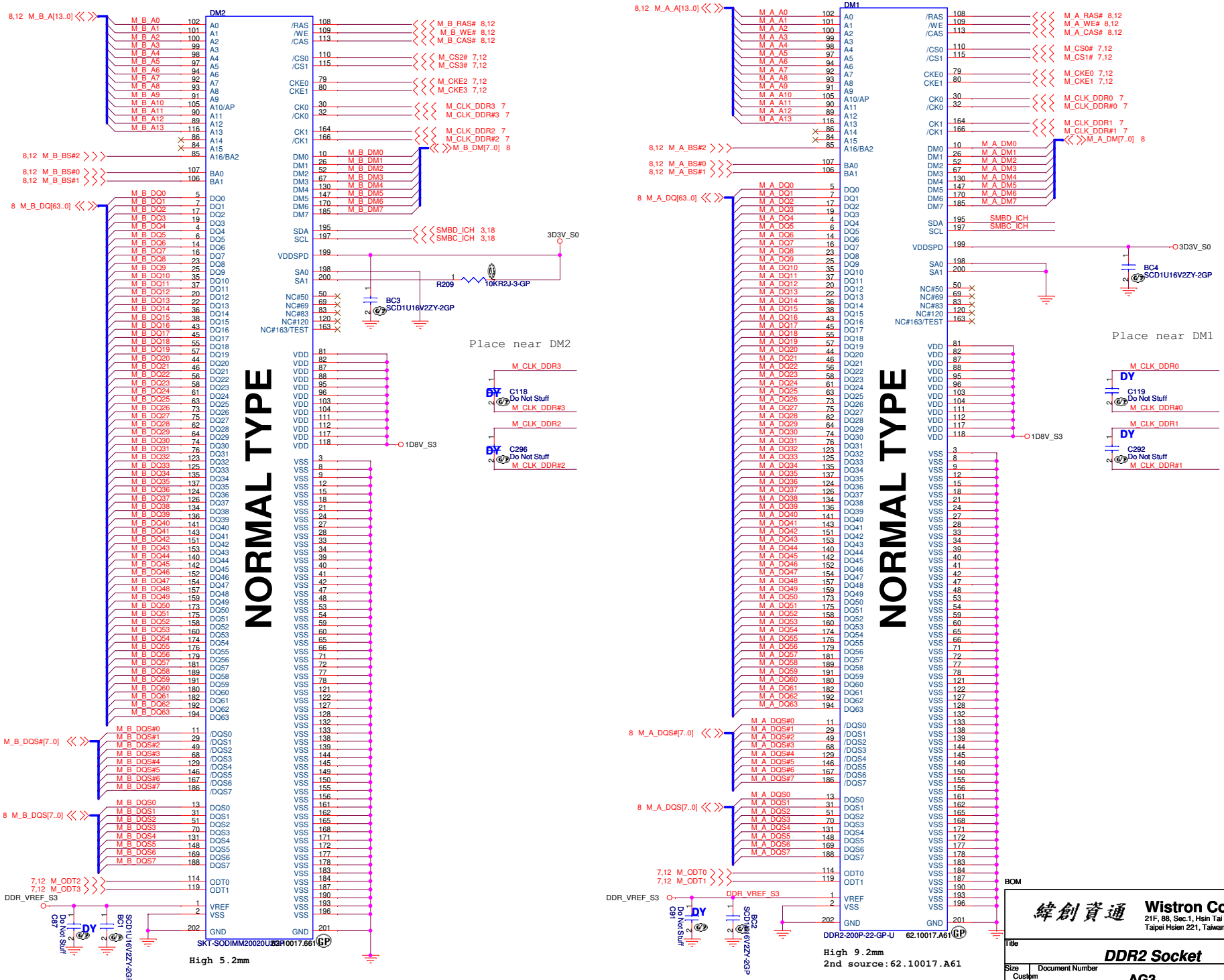
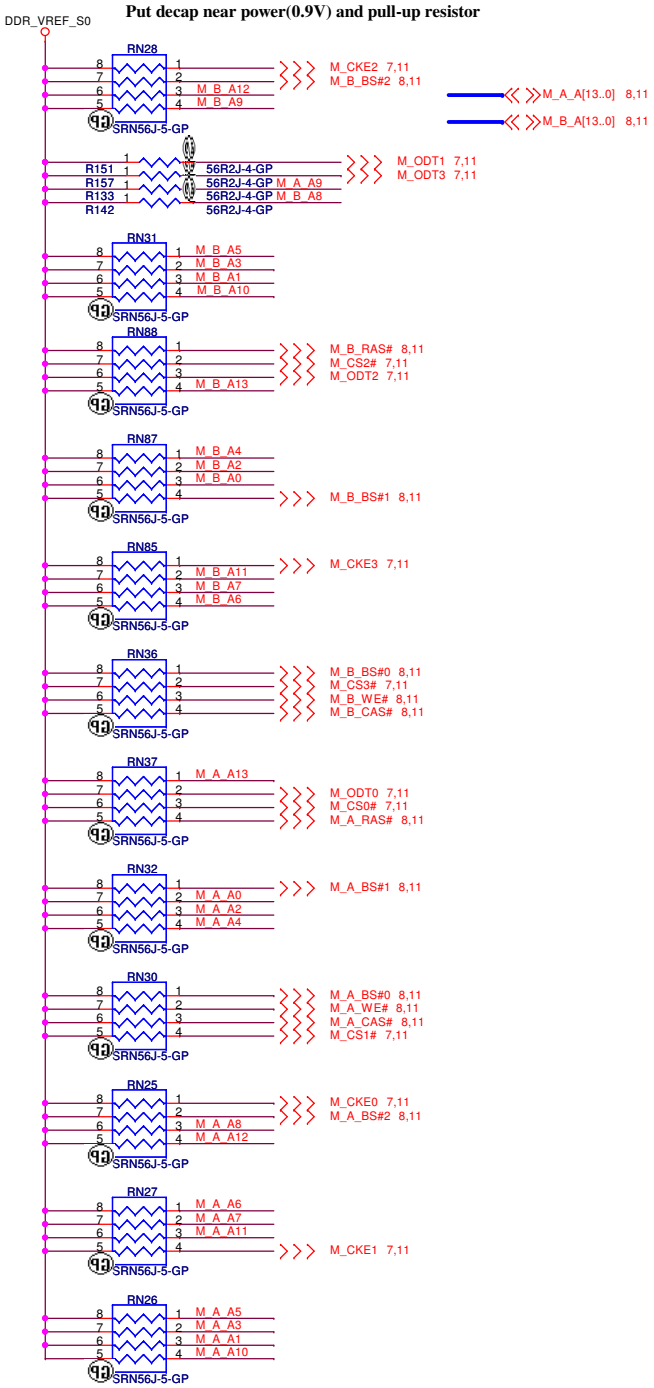


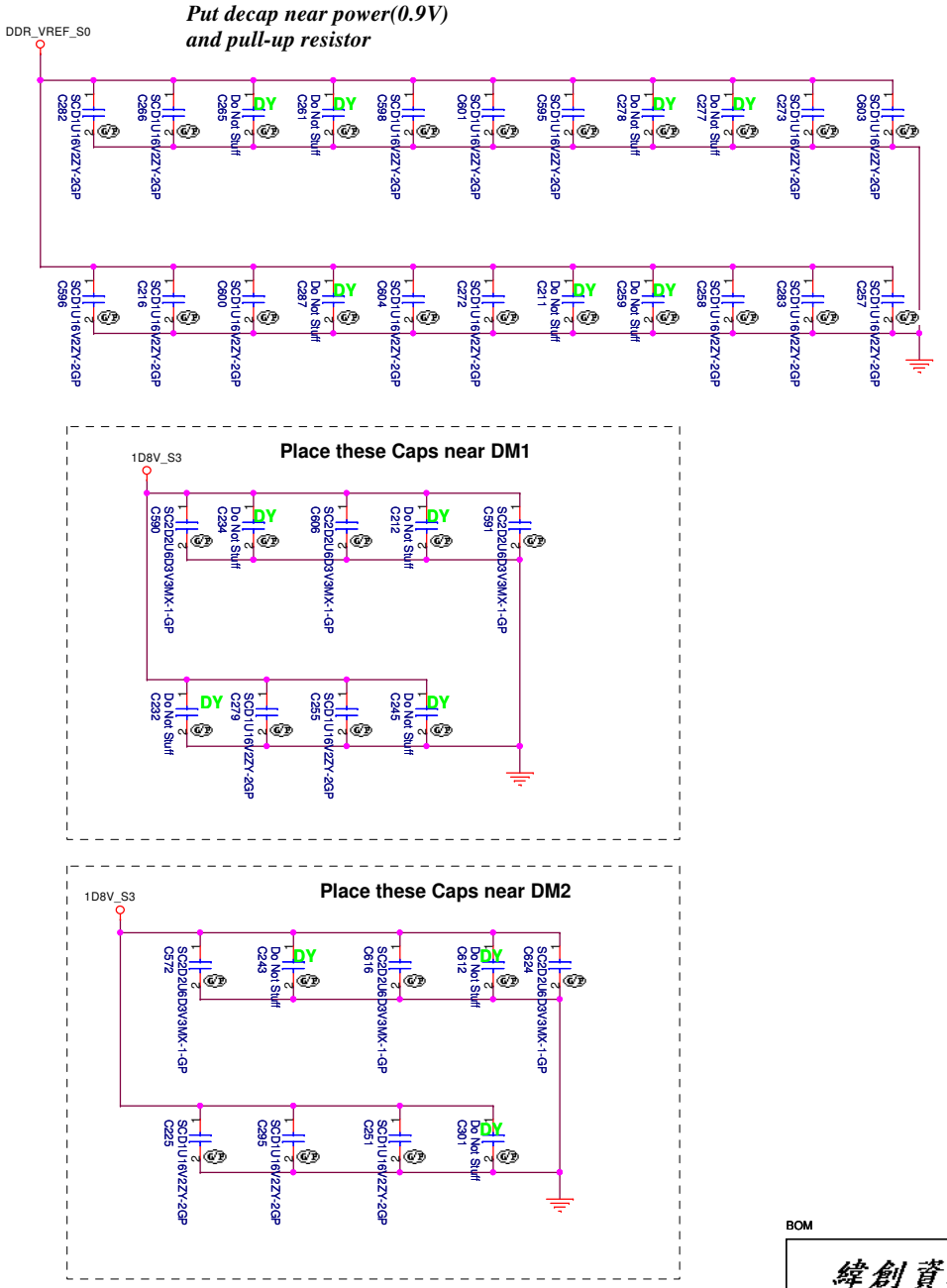
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GMCH (5 of 5)
Size A3	Document Number AG3
Rev	2
Date: Thursday, April 20, 2006	Sheet 10 of 55


DM2
NORMAL TYPE
SKT-SODIMM200U2GR0017.661
High 5.2mm
Place near DM2
DM1
NORMAL TYPE
DDR2-200P-22-GP-U
62.10017.A61
High 9.2mm
2nd source:62.10017.A61
Place near DM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR2 Socket
AG3
Size Custom
Document Number
Rev 2
Date: Thursday, April 20, 2006
Sheet 11 of 55

PARALLEL TERMINATION



Decoupling Capacitor



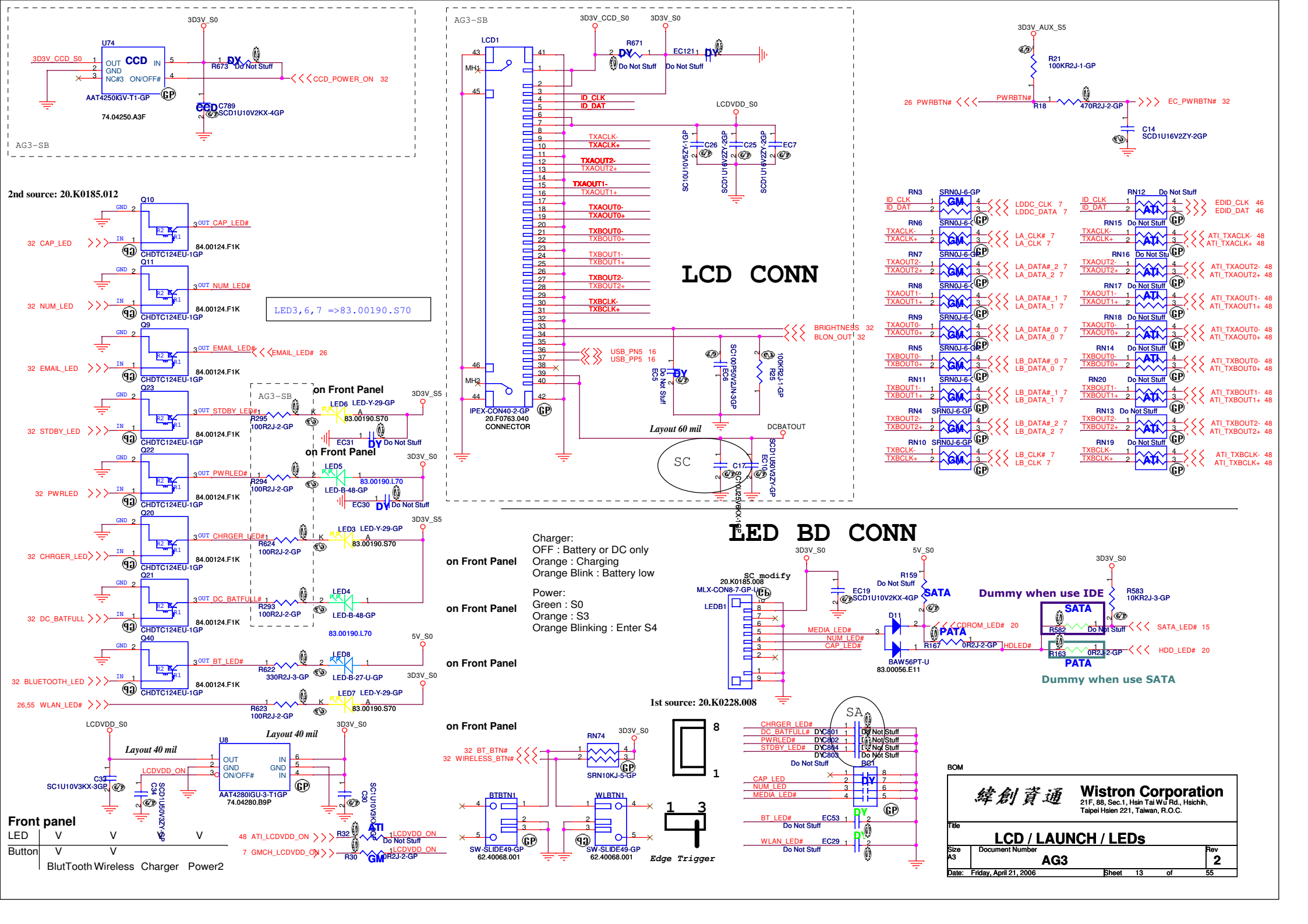
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

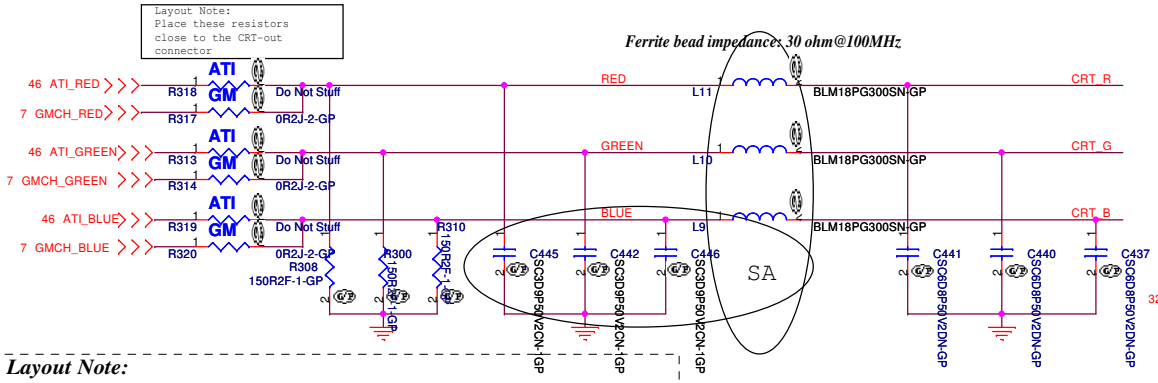
Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	AG3	2

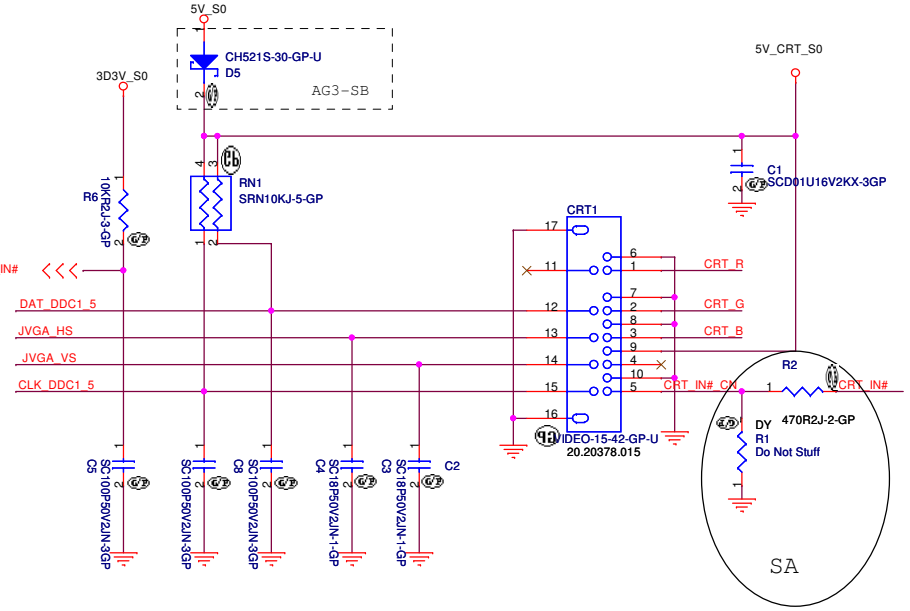
Date: Friday, April 21, 2006 Sheet 12 of 55


LCD CONN
LED BD CONN
2nd source: 20.K0185.012
1st source: 20.K0228.008
LED3,6,7 =>83.00190.S70
Charger:
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low
Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4
on Front Panel
Front panel
LED V V V V
Button V V
BlutTooth Wireless Charger Power2
Layout 60 mil
Layout 40 mil
Edge Trigger
Dummy when use IDE
Dummy when use SATA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LCD / LAUNCH / LEDs
AG3
Friday, April 21, 2006

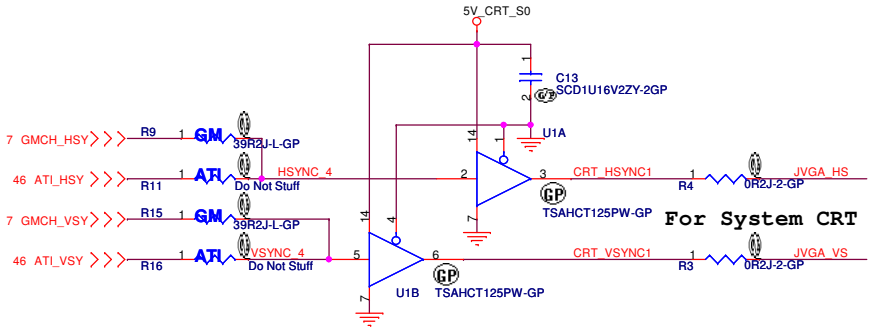
CRT I/F & CONNECTOR



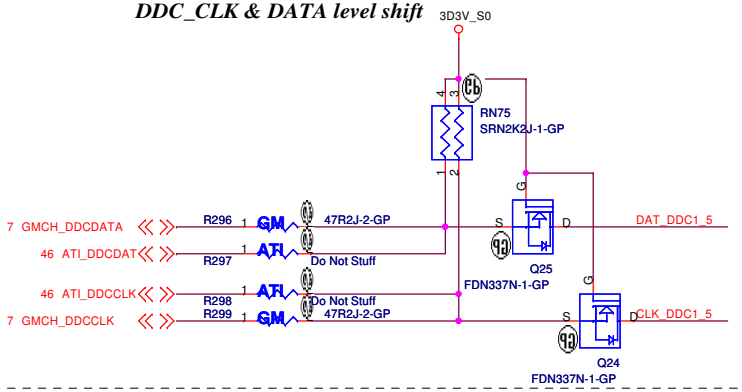
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



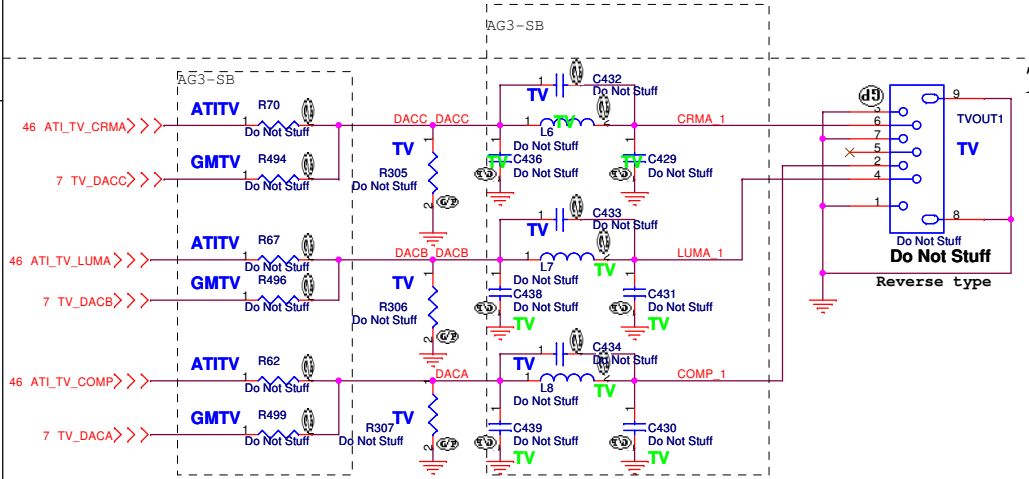
Hsync & Vsync level shift

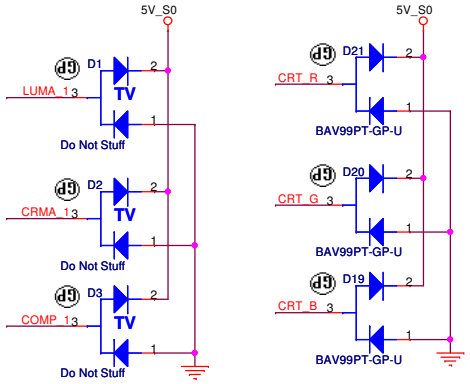


DDC_CLK & DATA level shift



TV OUT CONN





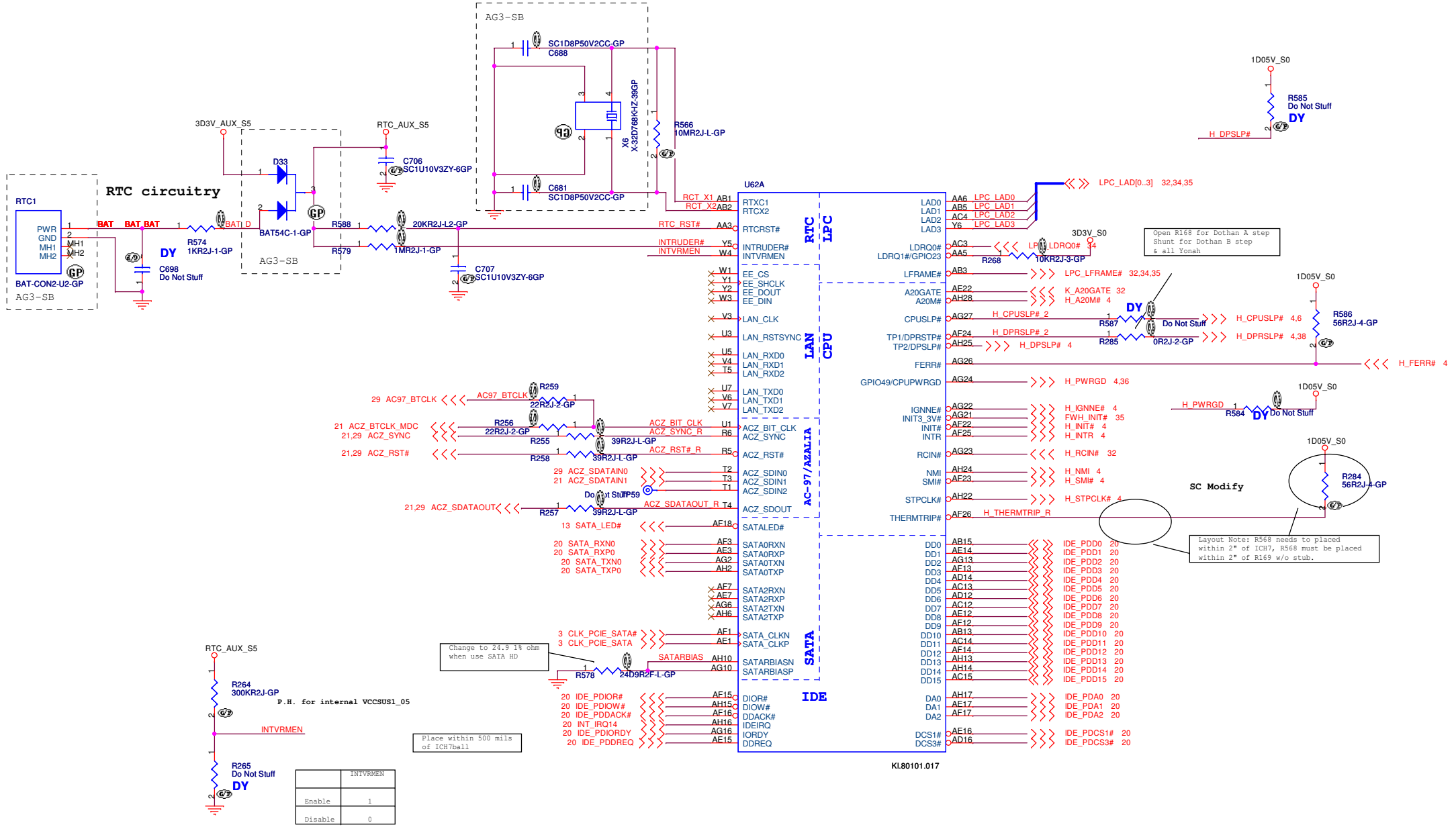
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT/TV Connector***

Size	Document Number	Rev
A3	AG3	2

Date: Thursday, April 20, 2006 Sheet 14 of 55



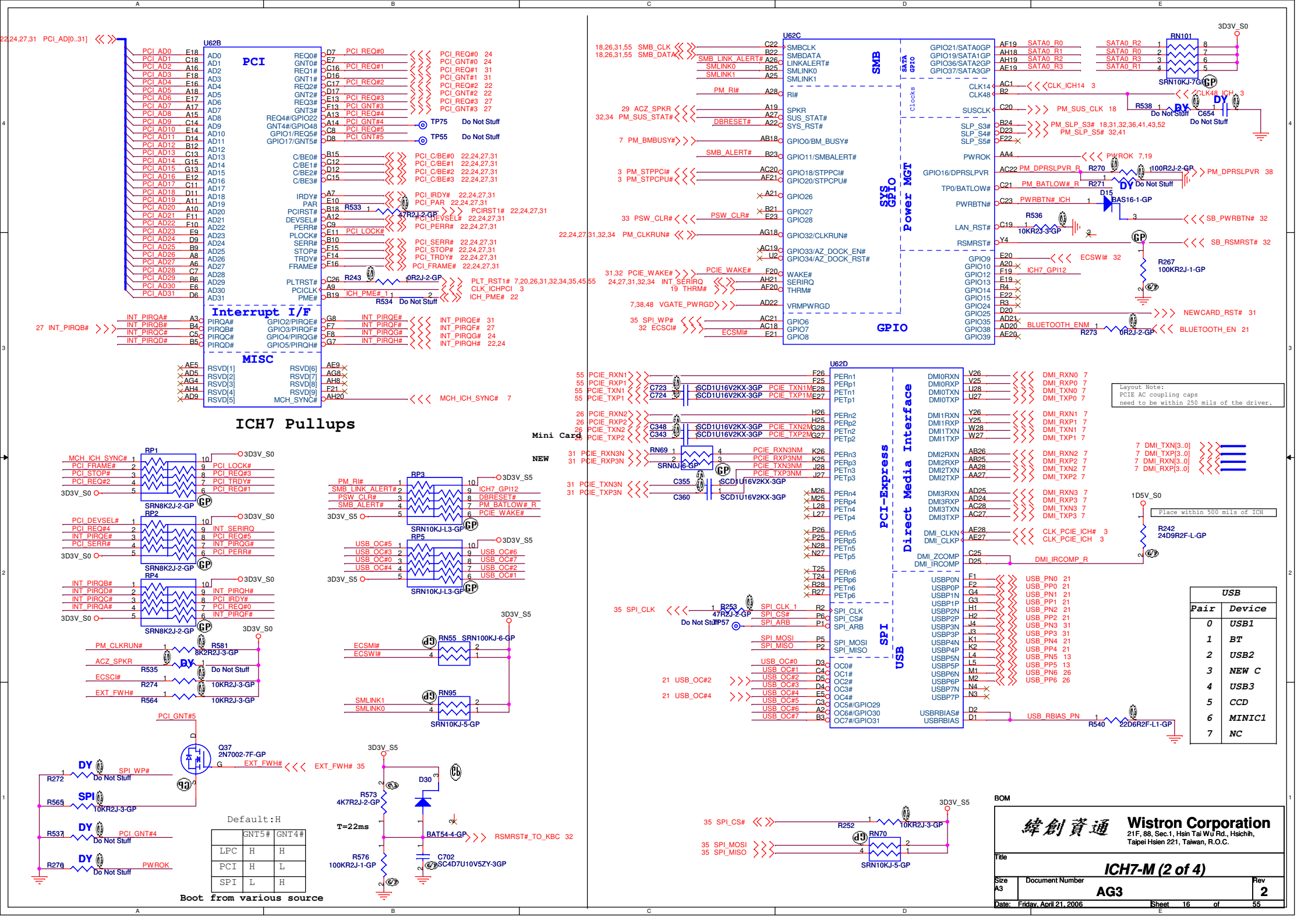
BOM

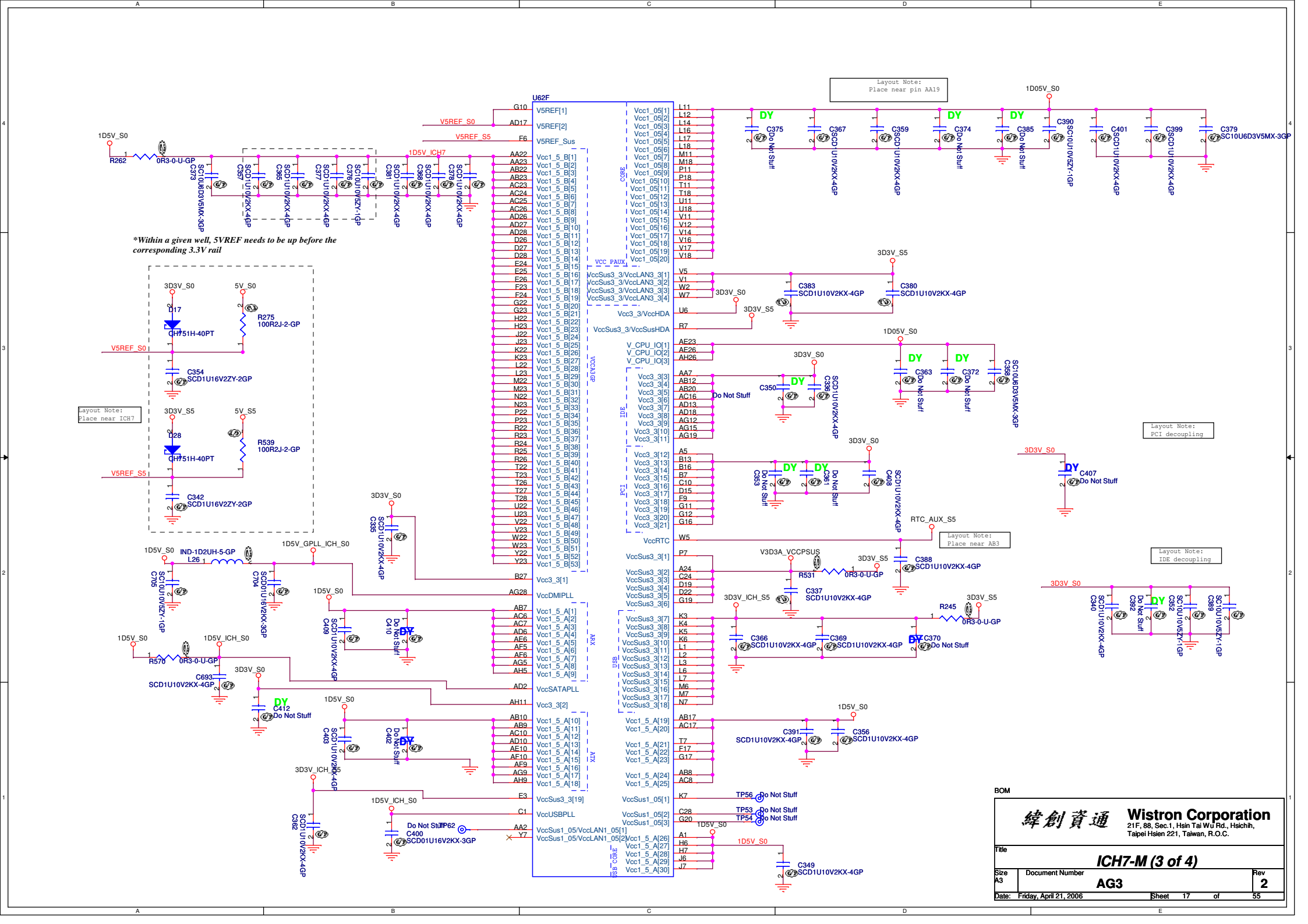
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

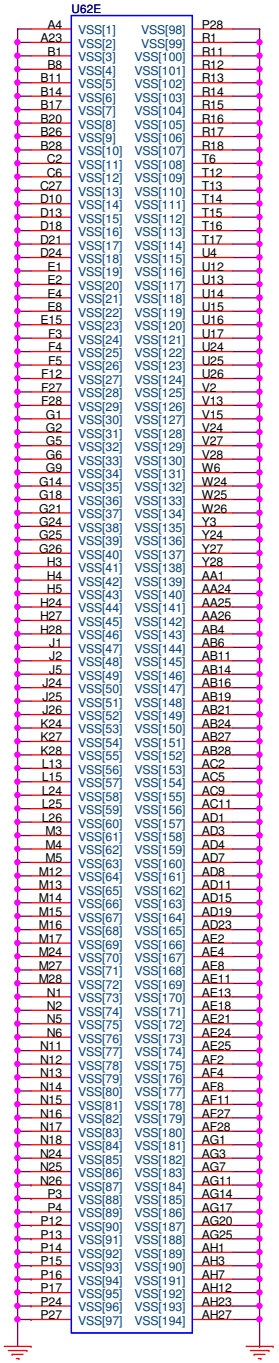
Title: ***ICH7-M (1 of 4)***

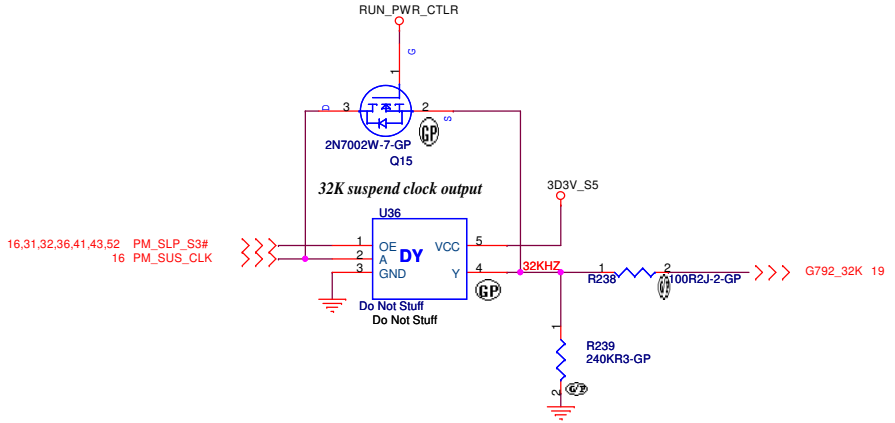
Size	Document Number	Rev
A3	AG3	2

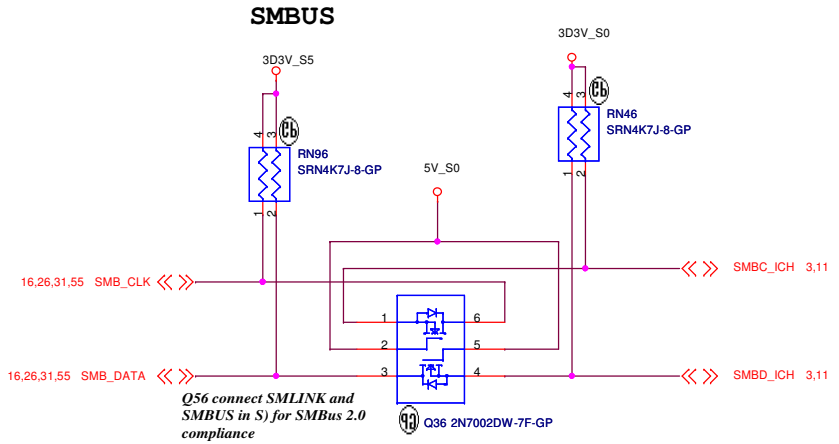
Date: Friday, April 21, 2006 Sheet 15 of 55


U62B
PCI
Interrupt I/F
MISC
U62C
SMB
SYS GPIO
Power MGT
GPIO
Clocks
U62D
PCI-Express
Direct Media Interface
USB
SPI
ICH7 Pullups
Mini Card
NEW
Default:H
Boot from various source
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
USB
Pair Device
0 USB1
1 BT
2 USB2
3 NEW C
4 USB3
5 CCD
6 MINIC1
7 NC
BOM
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size A3
Document Number AG3
Rev 2
Date: Friday, April 21, 2006
Sheet 16 of 55


U62F
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: PCI decoupling
Layout Note: Place near AB3
Layout Note: IDE decoupling
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number AG3
Rev 2
Date: Friday, April 21, 2006
Sheet 17 of 55







BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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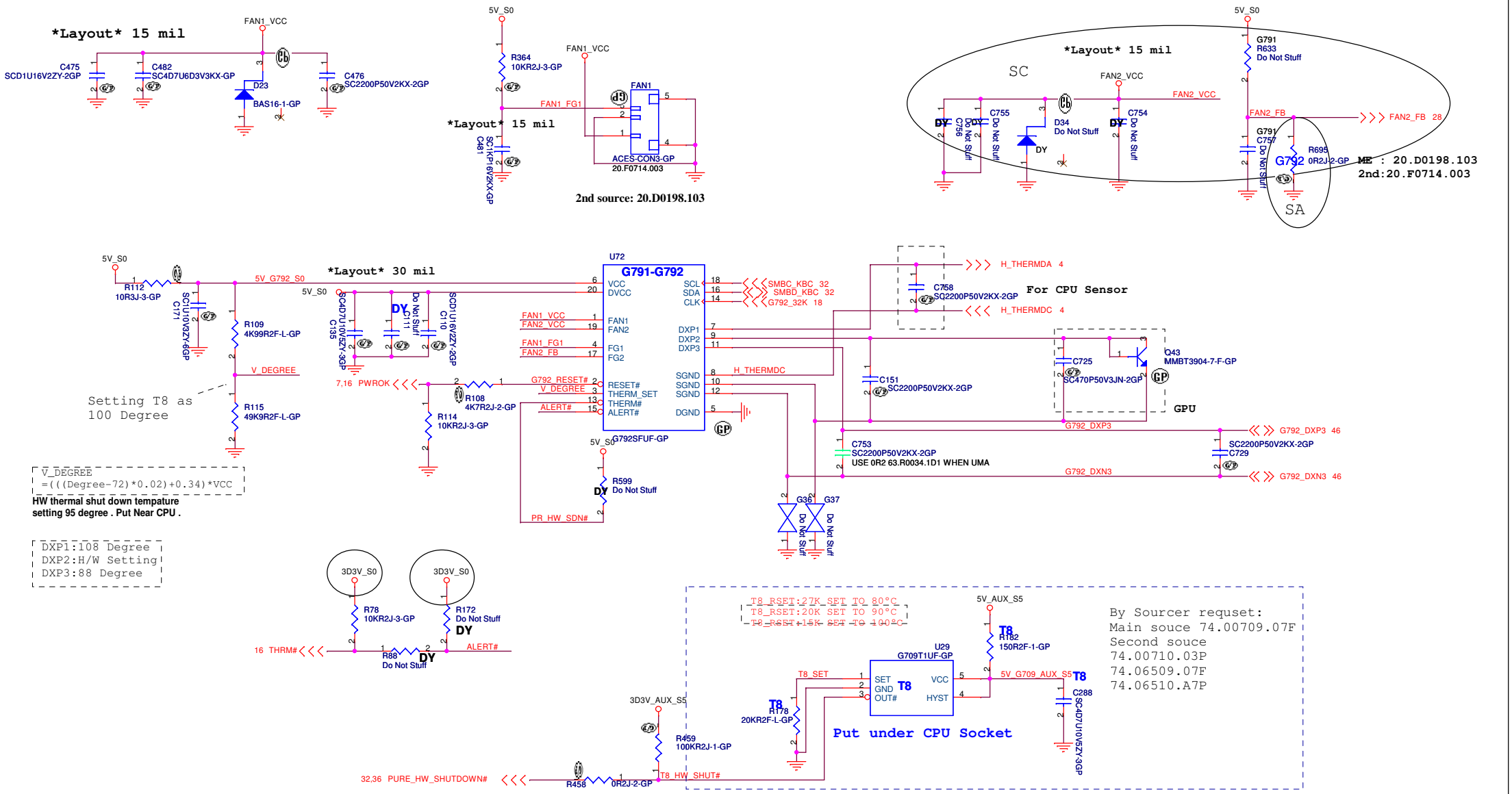
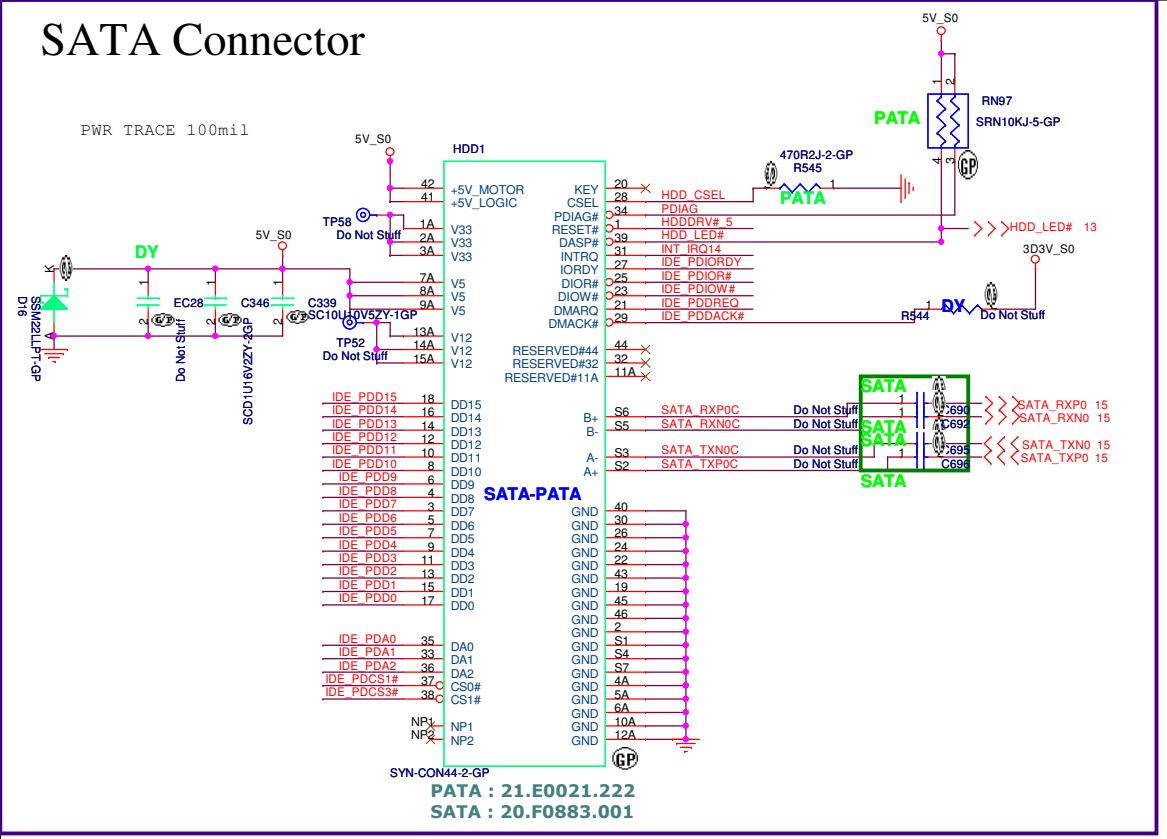
Title	ICH7-M (4 of 4)	
Size A3	Document Number AG3	Rev 2
Date: Friday, April 21, 2006	Sheet 18 of 55	



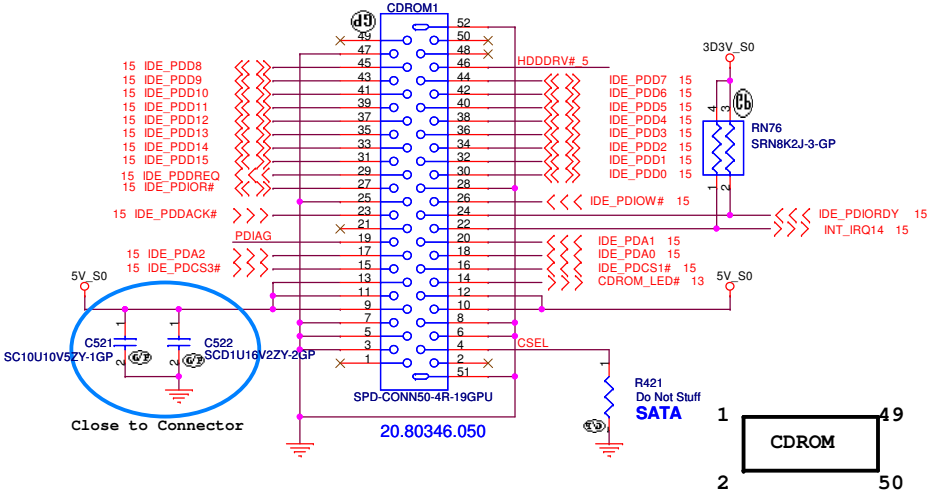
BOM

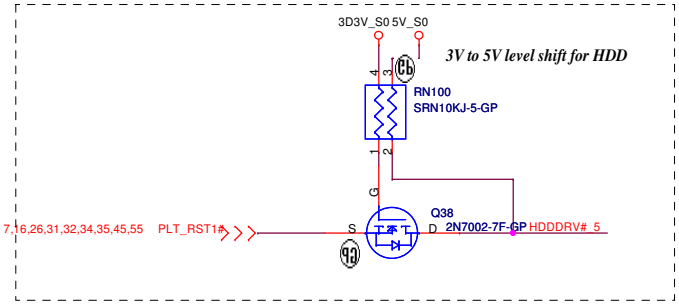
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Thermal/Fan Controllor G792***	
Size A3	Document Number **AG3**	Rev **2**
Date: Friday, April 21, 2006	Sheet 19 of 55	

SATA Connector



CDROM Connector





BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA/PATA HDD / ODD

Size	Document Number	Rev
A3	AG3	2

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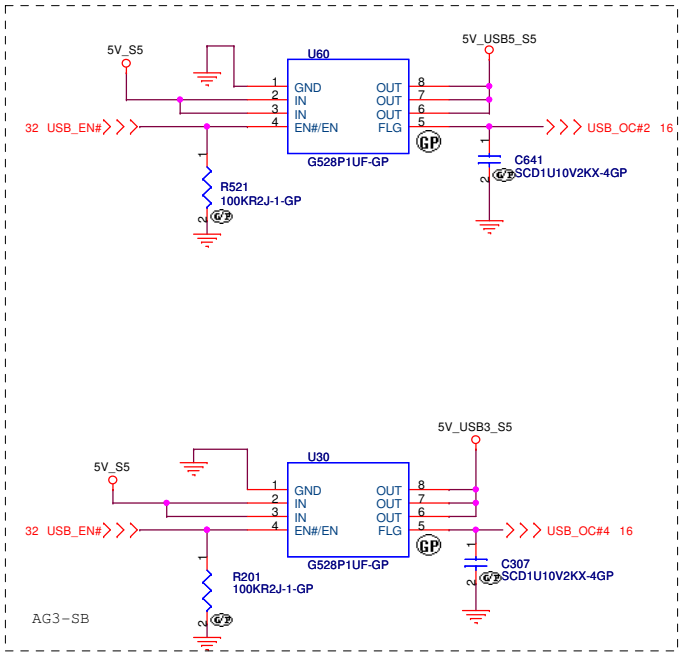
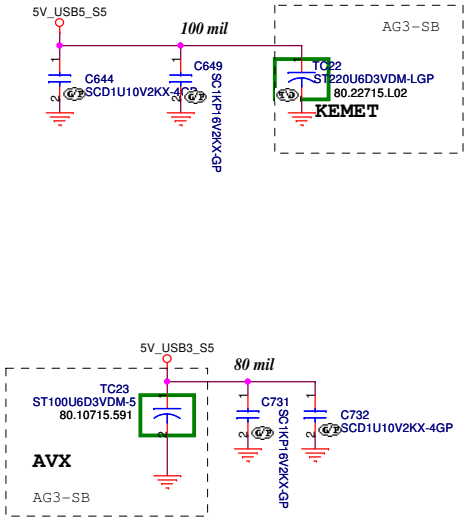
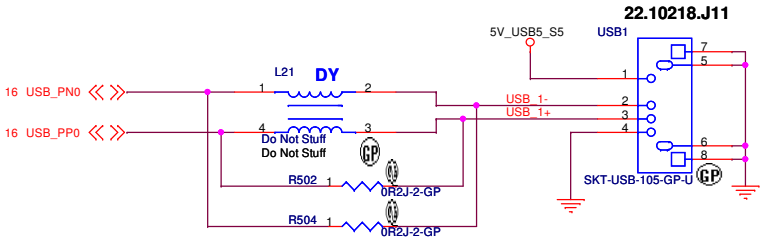
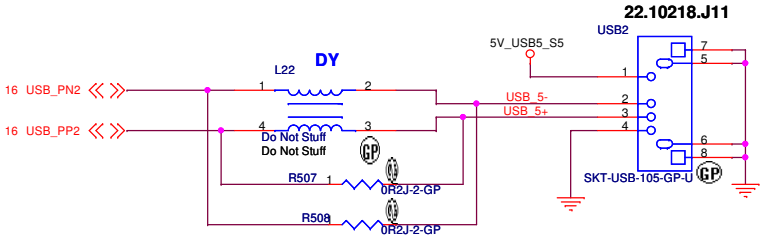
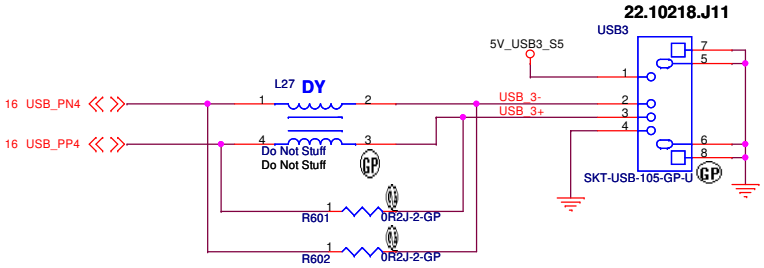
USB PORT



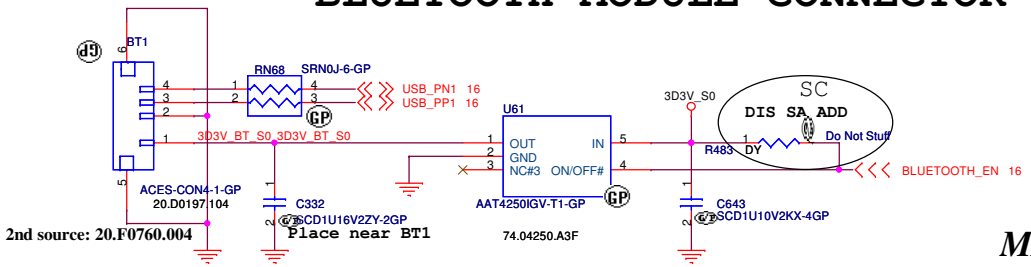




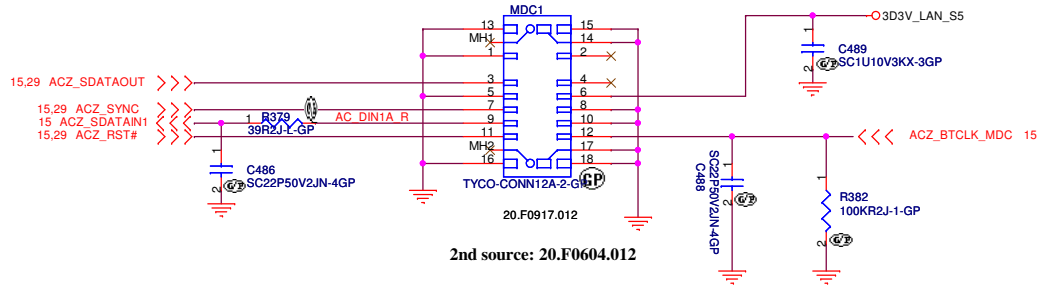




BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONN



BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC I/F

Size	Document Number	Rev
A3	AG3	2

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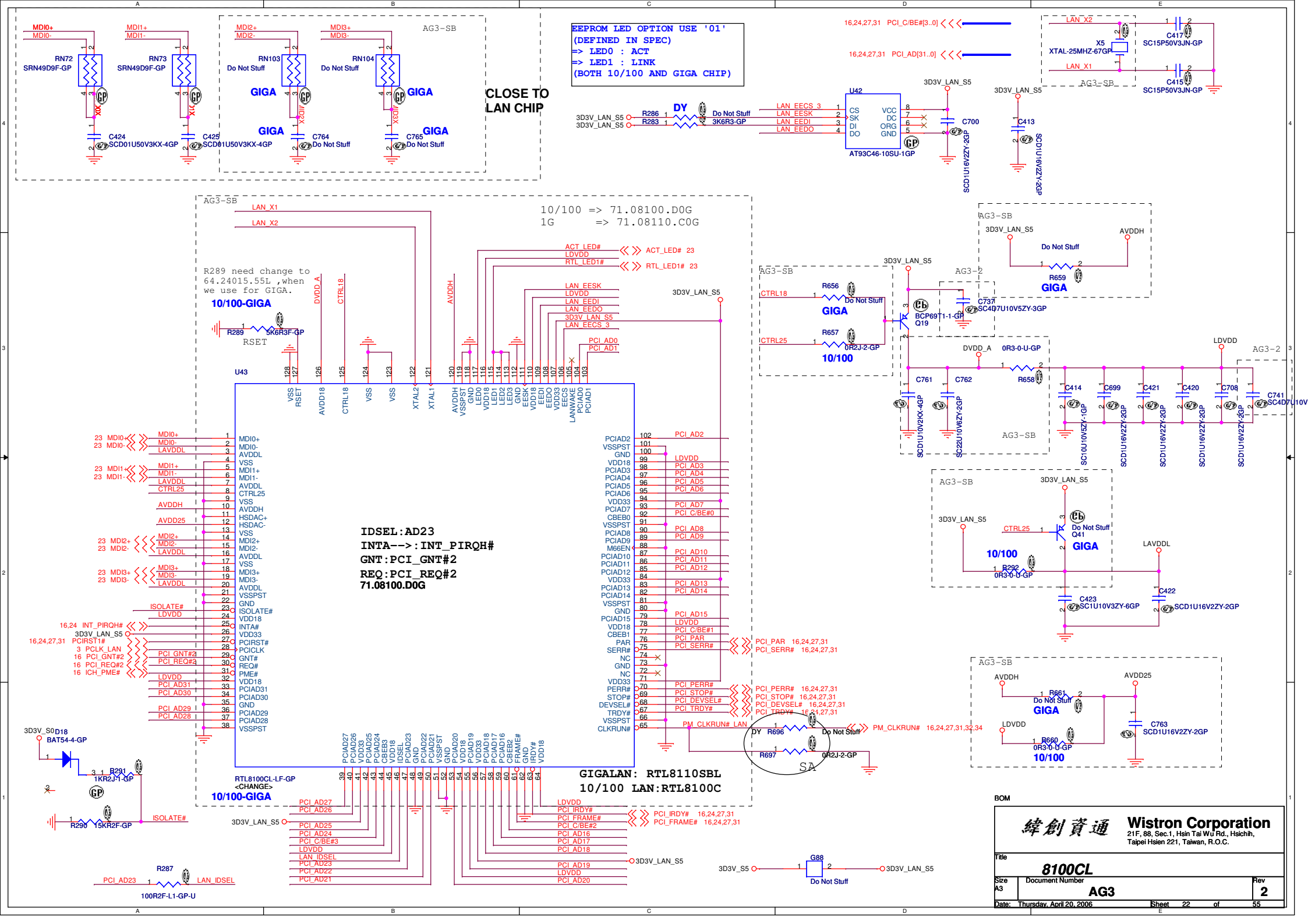
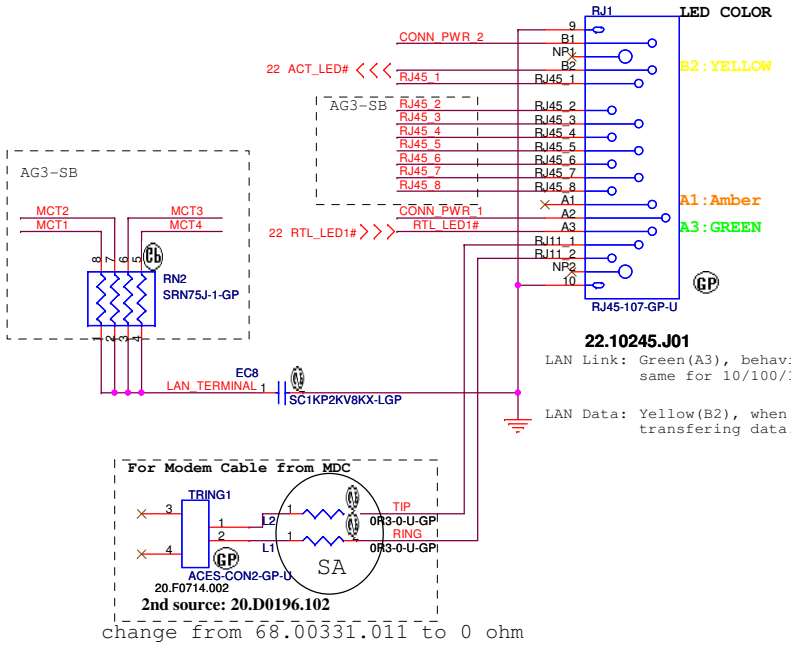
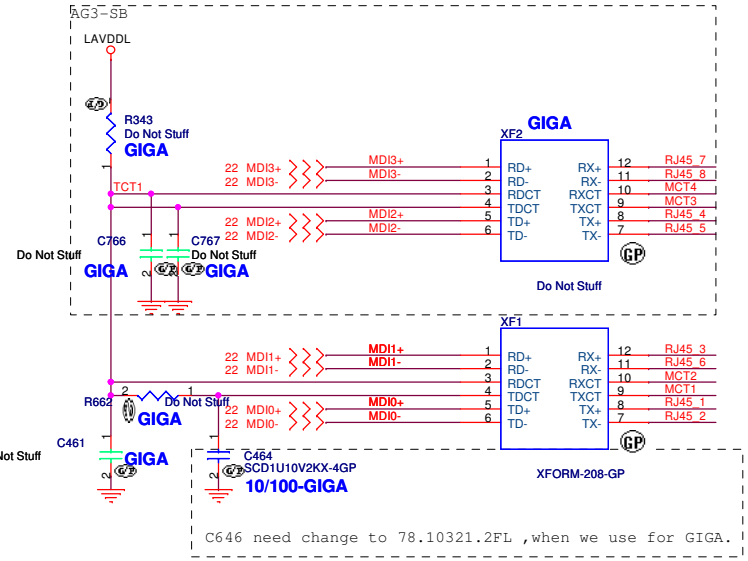
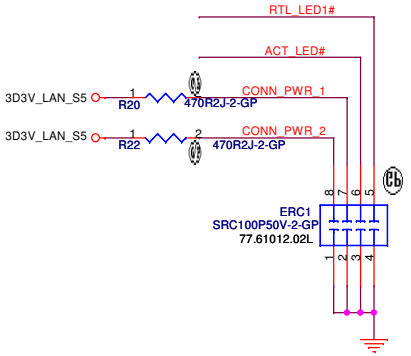

AG3-SB
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
RN72
SRN49D9F-GP
RN73
SRN49D9F-GP
RN103
Do Not Stuff
RN104
Do Not Stuff
GIGA
C424
SCD01U50V3KX-4GP
C425
SCD01U50V3KX-4GP
C764
Do Not Stuff
C765
Do Not Stuff
CLOSE TO
LAN CHIP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
16,24,27,31 PCI_C/BE#[3..0]
16,24,27,31 PCI_AD[31..0]
LAN_X2
LAN_X1
X5
XTAL-25MHZ-67GP
C417
SC15P50V3JN-GP
C415
SC15P50V3JN-GP
3D3V_LAN_S5
R286
R283
DY
Do Not Stuff
3K6R3-GP
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
U42
CS
SK
DI
DO
VCC
DC
ORG
GND
AT93C46-10SU-1GP
C700
SCD1U16V2ZY-2GP
C413
SCD1U16V2ZY-2GP
10/100 => 71.08100.D0G
1G => 71.08110.C0G
R289 need change to
64.24015.55L ,when
we use for GIGA.
10/100-GIGA
R289
5K6R3F-GP
RSET
U43
ACT_LED#
RTL_LED1#
ACT_LED# 23
RTL_LED1# 23
LAN_EESK
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
VSS
RSET
AVDDH
CTRL18
XTAL2
XTAL1
VSSPST
GND
LED0
LED1
LED2
LED3
EESK
EEDI
EEDO
VDD33
EECS
LANWAKE
PCIAD0
PCIAD1
MDI0+
MDI0-
LAVDDL
AVDDL
MDI1+
MDI1-
CTRL25
AVDDH
AVDD25
HSDAC+
HSDAC-
MDI2+
MDI2-
MDI3+
MDI3-
ISOLATE#
LDVDD
INTA#
VDD33
PCIRST#
PCICLK
GNT#
REQ#
PME#
PCIAD31
PCIAD30
PCIAD29
PCIAD28
VSSPST
PCIAD2
PCIAD3
PCIAD4
PCIAD5
PCIAD6
PCIAD7
CBEB0
M66EN
PCIAD10
PCIAD11
PCIAD12
PCIAD13
PCIAD14
PCIAD15
CBEB1
PAR
SERR#
NC
PERR#
STOP#
DEVSEL#
TRDY#
CLKRUN#
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_C/BE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_C/BE#1
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PM_CLKRUN# LAN
IDSEL:AD23
INTA-->:INT_PIRQH#
GNT:PCI_GNT#2
REQ:PCI_REQ#2
71.08100.D0G
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
RTL8100CL-LF-GP
<CHANGE>
10/100-GIGA
PCIAD27
PCIAD26
PCIAD25
PCIAD24
CBEB3
VDD18
IDSEL
PCIAD23
GND
PCIAD22
PCIAD21
VSSPST
GND
PCIAD20
VDD18
PCIAD19
VDD33
PCIAD18
PCIAD17
PCIAD16
CBEB2
FRAME#
GND
IRDY#
VDD18
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_C/BE#3
LDVDD
LAN_IDSEL
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD19
PCI_AD20
PCI_IRDY#
PCI_FRAME#
PCI_C/BE#2
PCI_AD16
PCI_AD17
PCI_AD18
R287
100R2F-L1-GP-U
D18
BAT54-4-GP
R291
1KR2J-1-GP
R290
15KR2F-GP
3D3V_S0
R696
R697
SA
PM_CLKRUN# 16,24,27,31,32,34
G88
3D3V_S5
R656
CTRL18
CTRL25
R657
10/100
BCP69T1-1-GP
Q19
C737
SC4D7U10V5ZY-3GP
R659
C761
C762
R658
DVDD_A
0R3-0-U-GP
SCD1U10V2KX-4GP
SC22U10V6ZY-2GP
C414
C699
C421
C420
C708
C741
SC4D7U10V
SC1U10V5ZY-1GP
SCD1U16V2ZY-2GP
Q41
R292
C422
C423
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
R661
R660
C763
SCD1U16V2ZY-2GP
AG3-2
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
8100CL
Size
A3
Document Number
AG3
Rev
2
Date: Thursday, April 20, 2006
Sheet 22 of 55

LAN Connector

PIN NAME	8110SBL (Giga)	8100CL (10/100)	SIGNAL NAME
VDD33	3.3	3.3	3D3V_LAN_S5
AVDDH	3.3	N.C.	AVDDH
VDD18	1.2	2.5	DVDD
AVDD18	1.2	2.5	DVDD_A
AVDDL	2.5	3.3	AVDDL
V_12P	3.3	2.5	V_12P







1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

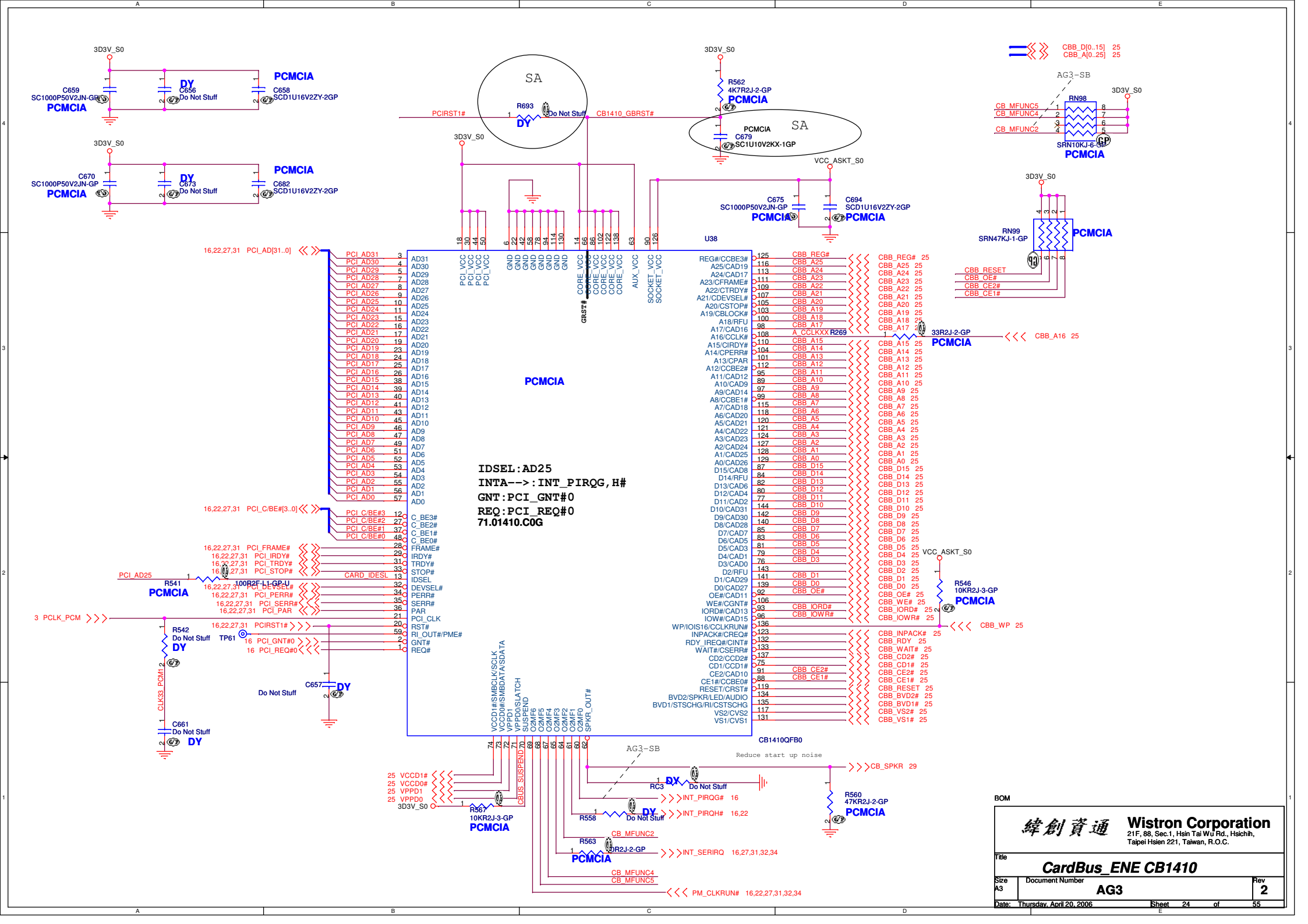
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

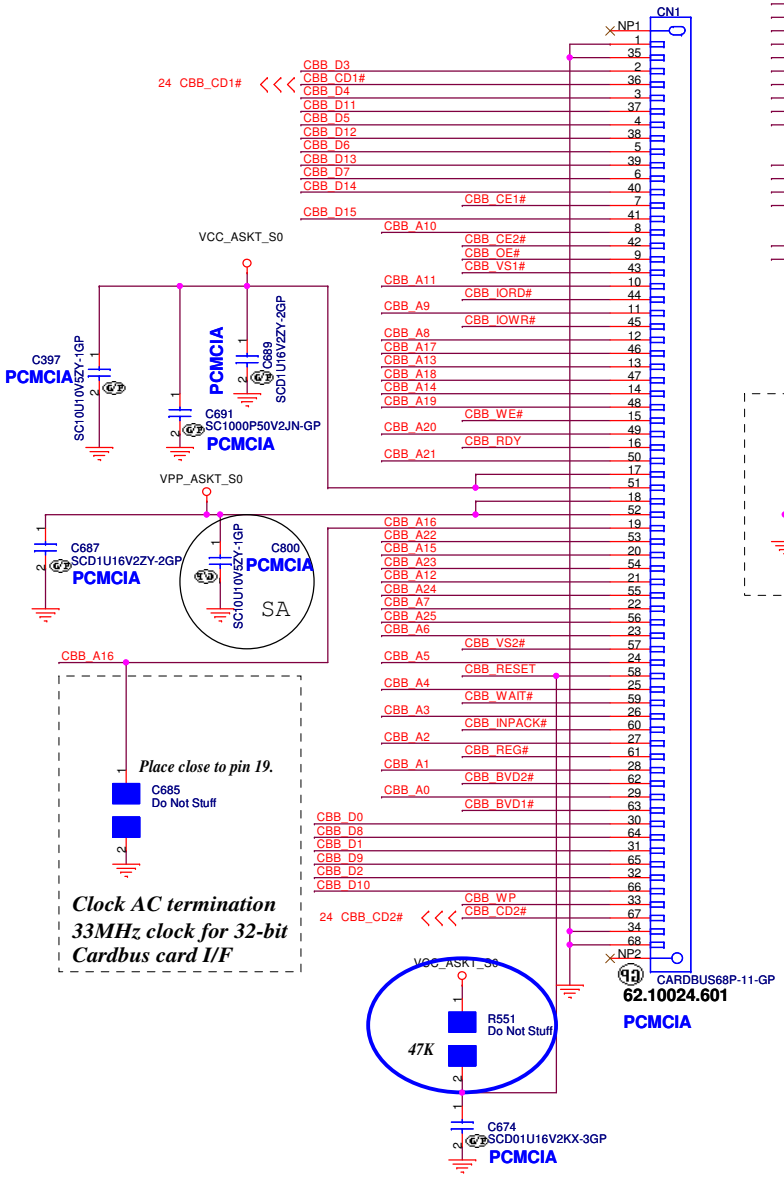
Title: **LAN Connector**

Size	Document Number	Rev
A3	AG3	2

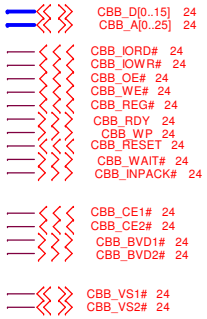
Date: Thursday, April 20, 2006 Sheet 23 of 55

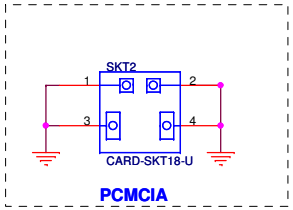

IDSEL:AD25
INTA-->:INT_PIRQG,H#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
71.01410.C0G
U38
CB1410QFB0
SA
PCMCIA
DY
Do Not Stuff
AG3-SB
Reduce start up noise
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CardBus_ENE CB1410
Size A3
Document Number AG3
Rev 2
Date: Thursday, April 20, 2006
Sheet 24 of 55

PCMCIA Socket

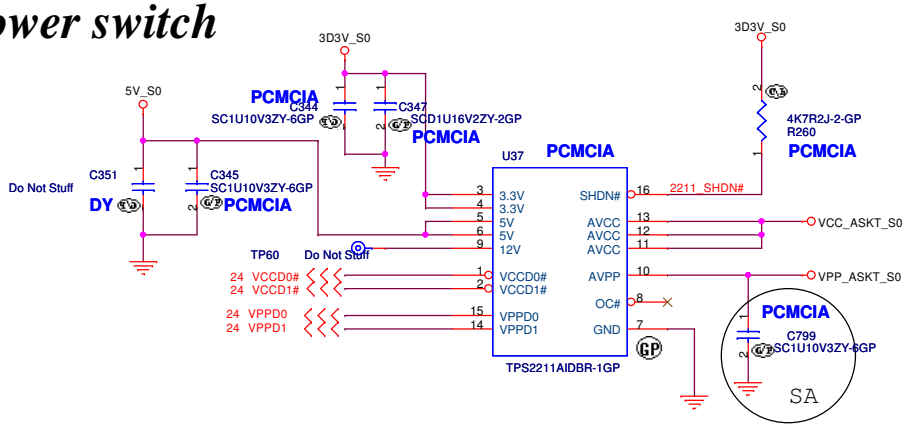


Cardbus I/F





Power switch

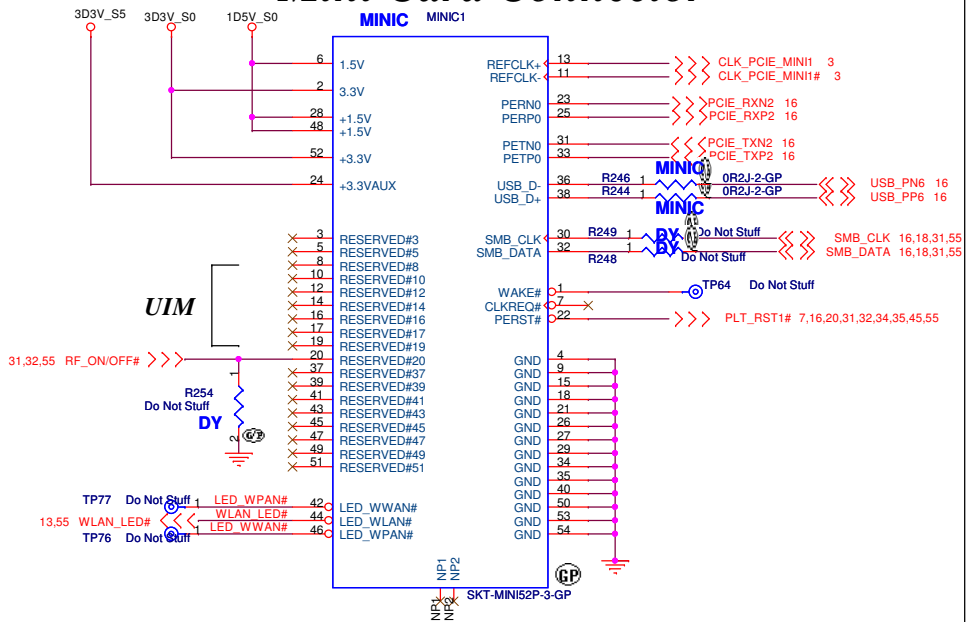


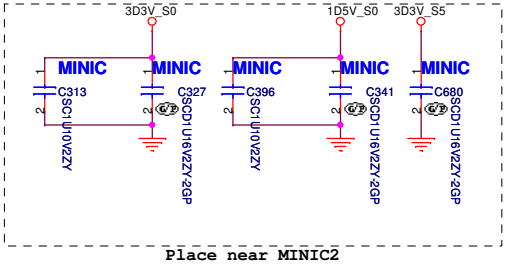
BOM

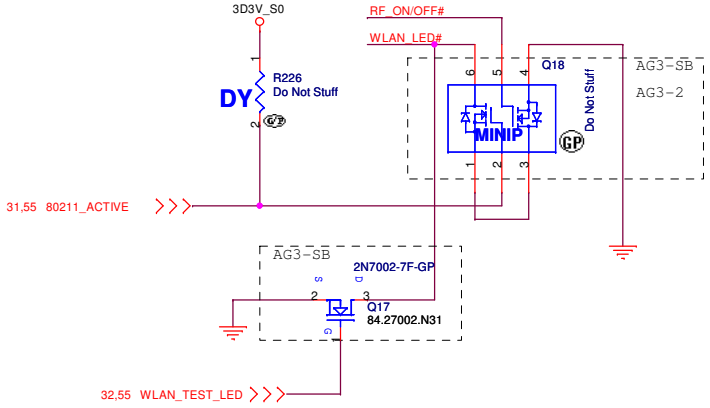
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

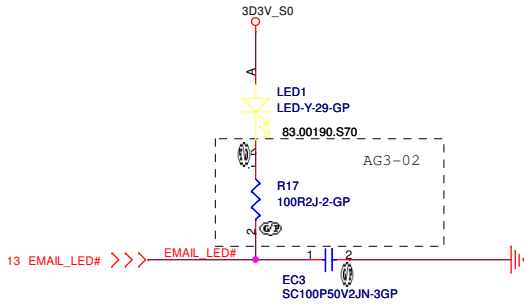
Title: **PCMCIA**		
Size: A3	Document Number: **AG3**	Rev: **2**
Date: Thursday, April 20, 2006	Sheet 25 of 55	

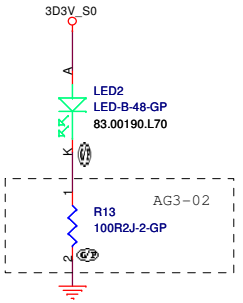
Mini Card Connector



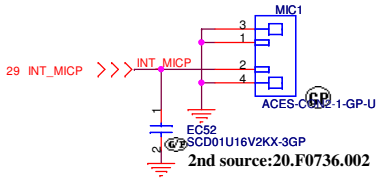


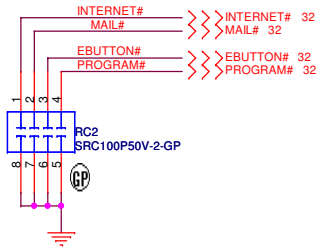




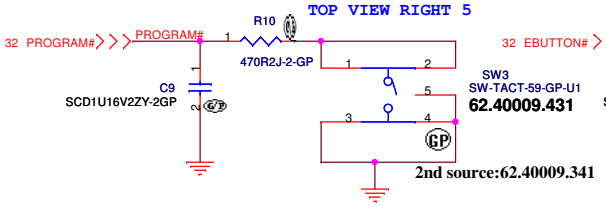


Internal Microphone

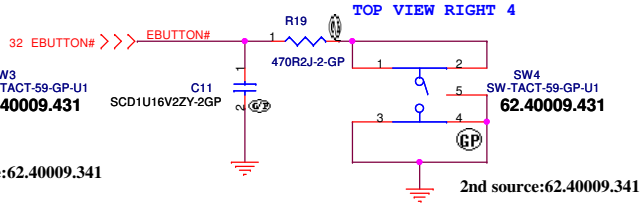




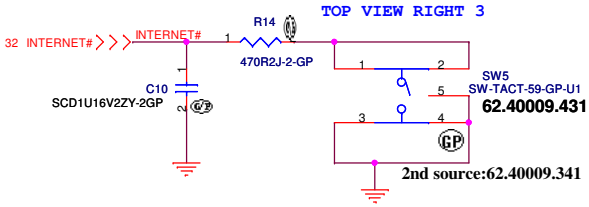
Program Button



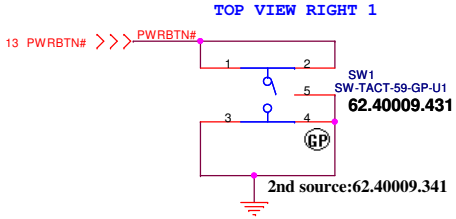
E-Button



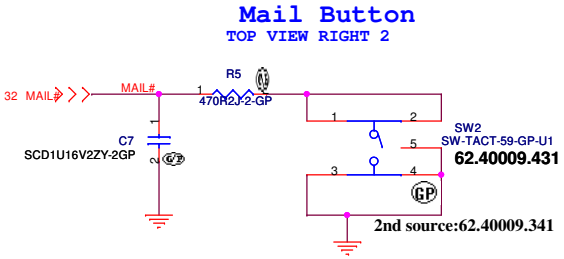
Internet Button



Power Button



Mail Button



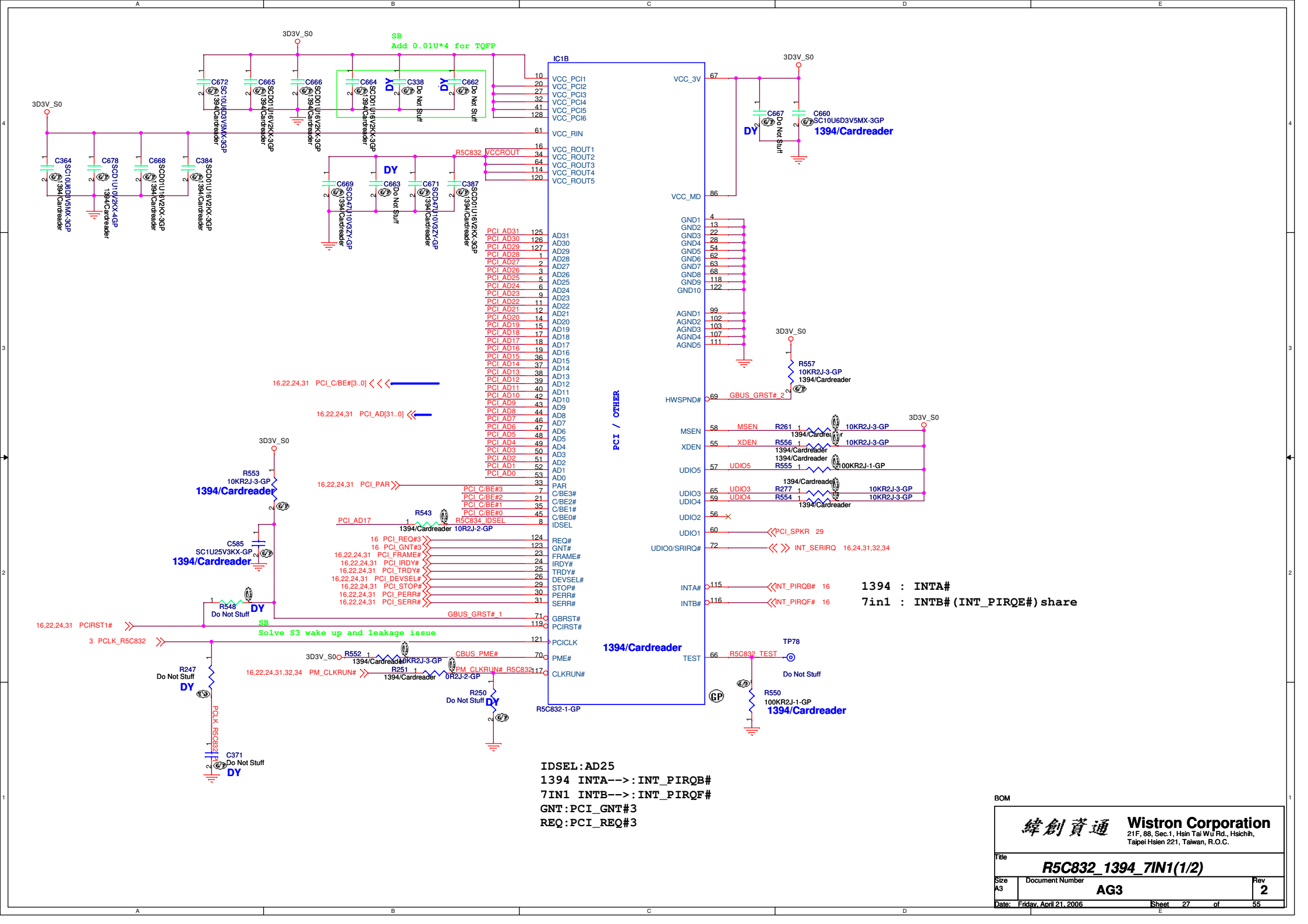
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / Button**

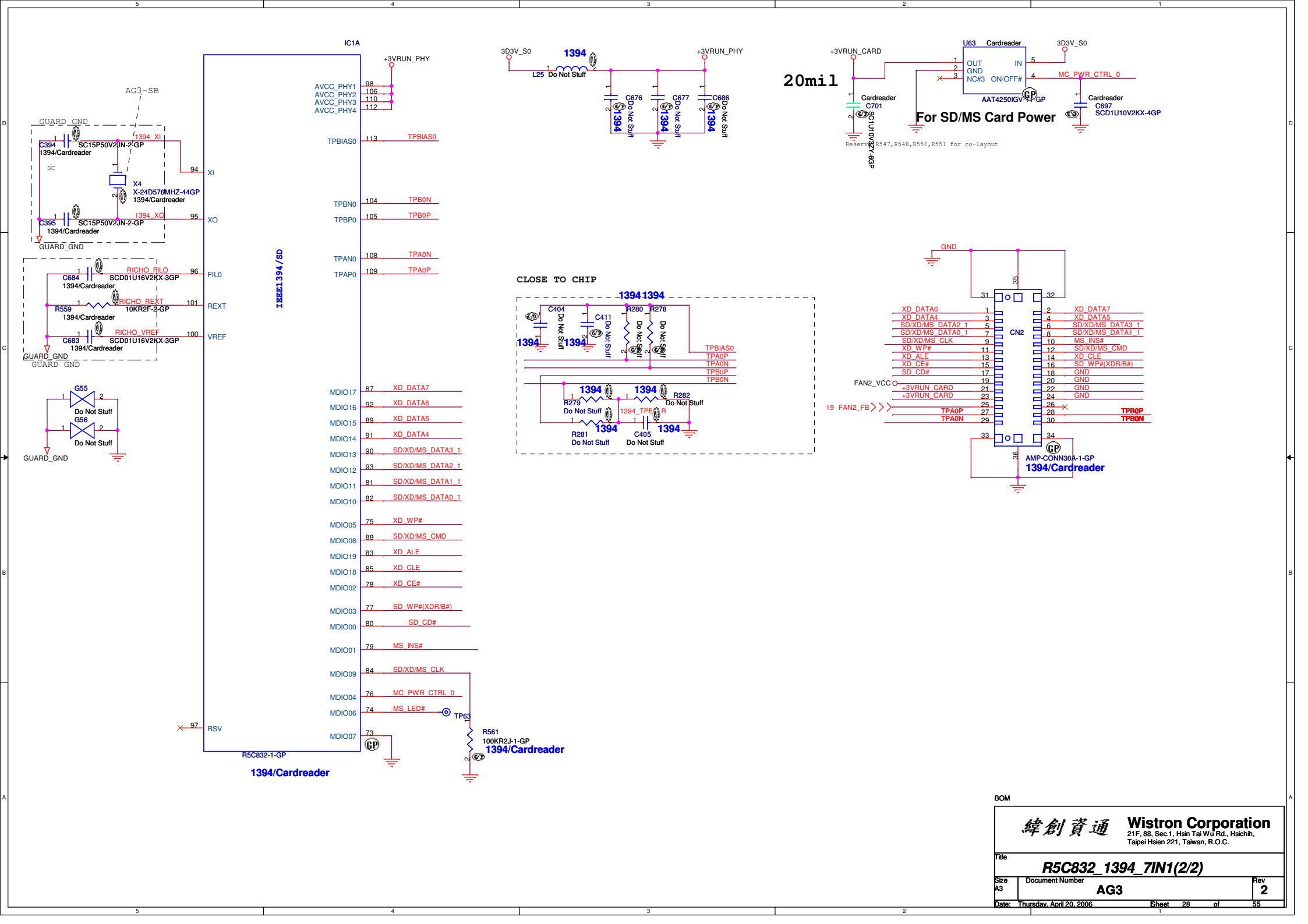
Size	Document Number	Rev
A3	AG3	2

Date: Wednesday, April 26, 2006 Sheet 26 of 55



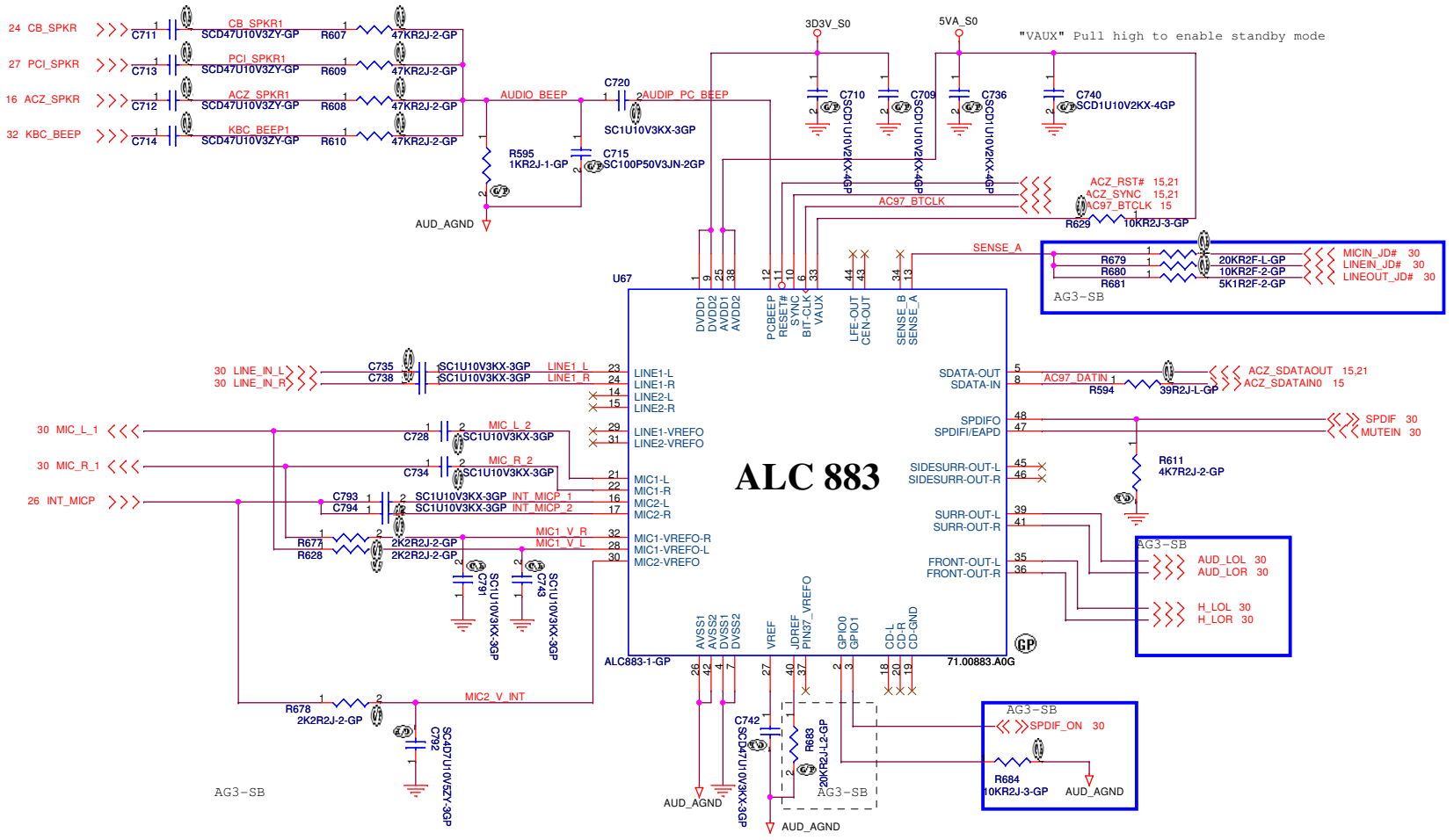
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: R5C832_1394_7IN1(1/2)		
Size: A3	Document Number: AG3	Rev: 2
Date: Friday, April 21, 2006	Sheet 27 of 55	



BOM

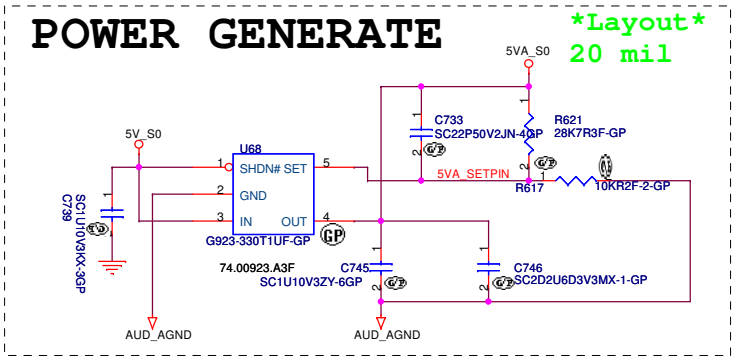
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***R5C832_1394_7IN1(2/2)***	
Size A3	Document Number **AG3**	Rev **2**
Date: Thursday, April 20, 2006	Sheet 28 of 55	



1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

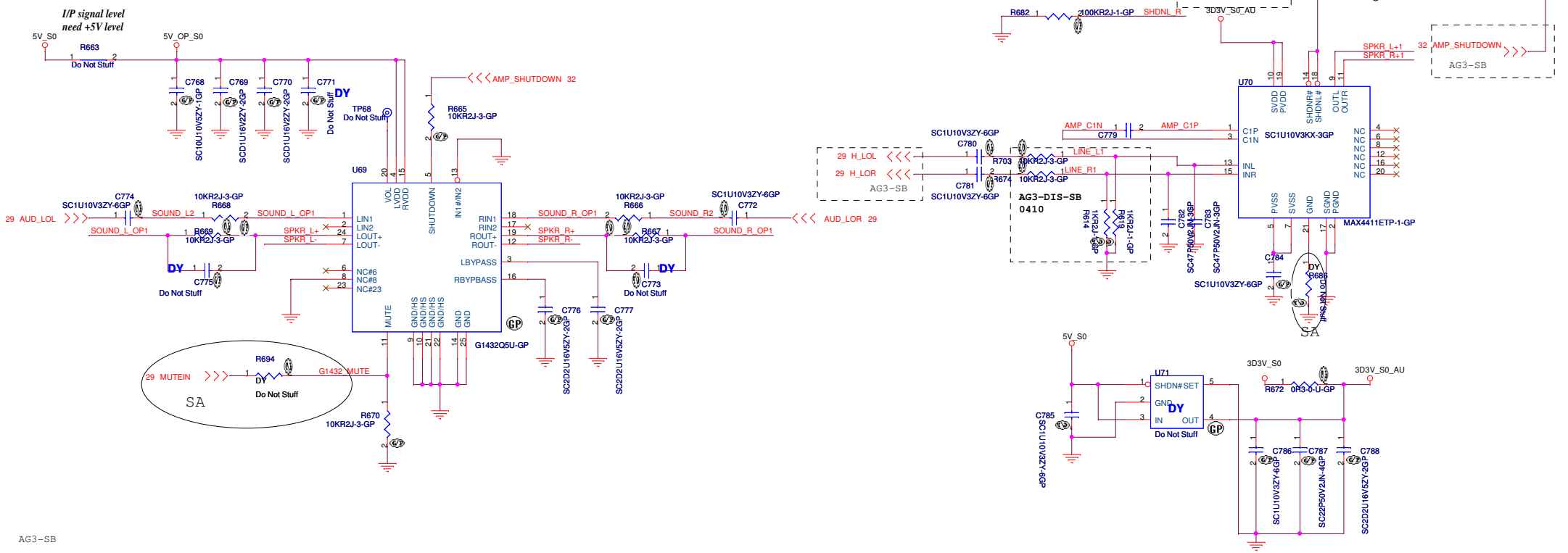
Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	*Symbol*	*Location*	*Re-tasking*
35/36	*FRONT*	*AMP,Jack1*	AMP output, line input
39/41	*SURR*	*X*	X
43/44	*CEN/LEFT*	*X*	SURR-VREFO-L/R
45/46	*SIDESURR*	*X*	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	*LINE1*	*Jack 2*	Line input, line output
21/22	*MIC1*	*Jack 3*	Mic input, line output
14/15	*LINE2*	*X*	X
16/17	*MIC2*	*Int. Mic*	Mic input



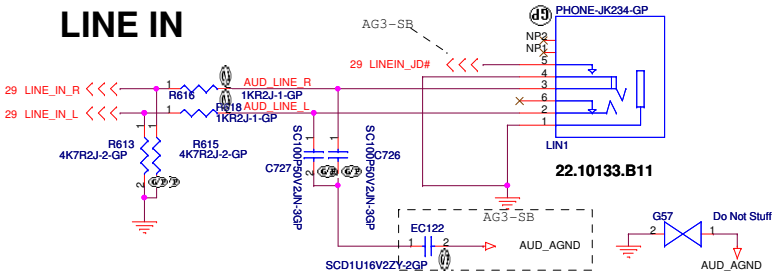
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC883***	
Size A3	Document Number **AG3**	Rev **2**
Date: Thursday, April 20, 2006	Sheet 29 of 55	

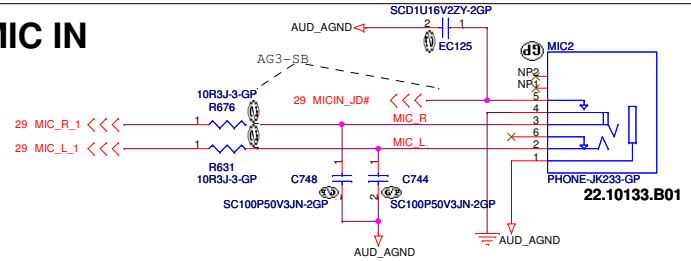


AG3-SB

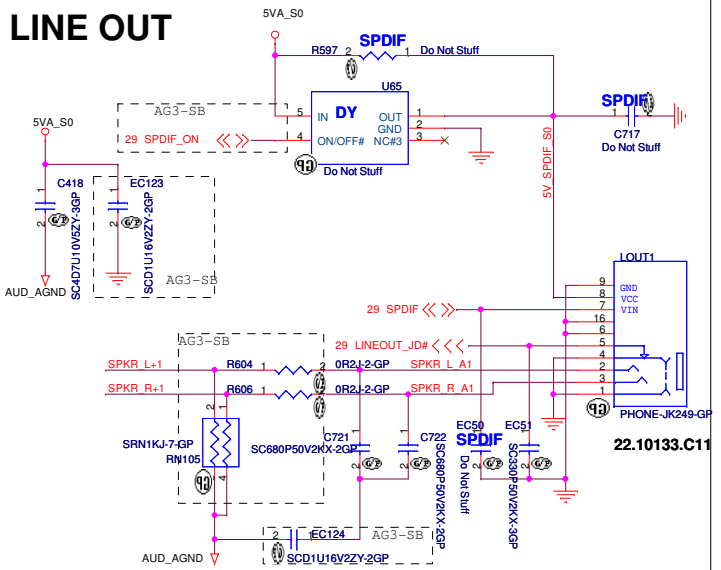
LINE IN



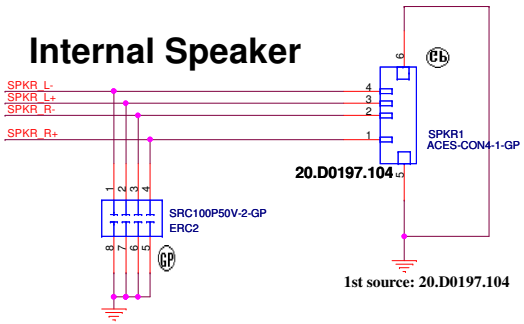
MIC IN



LINE OUT



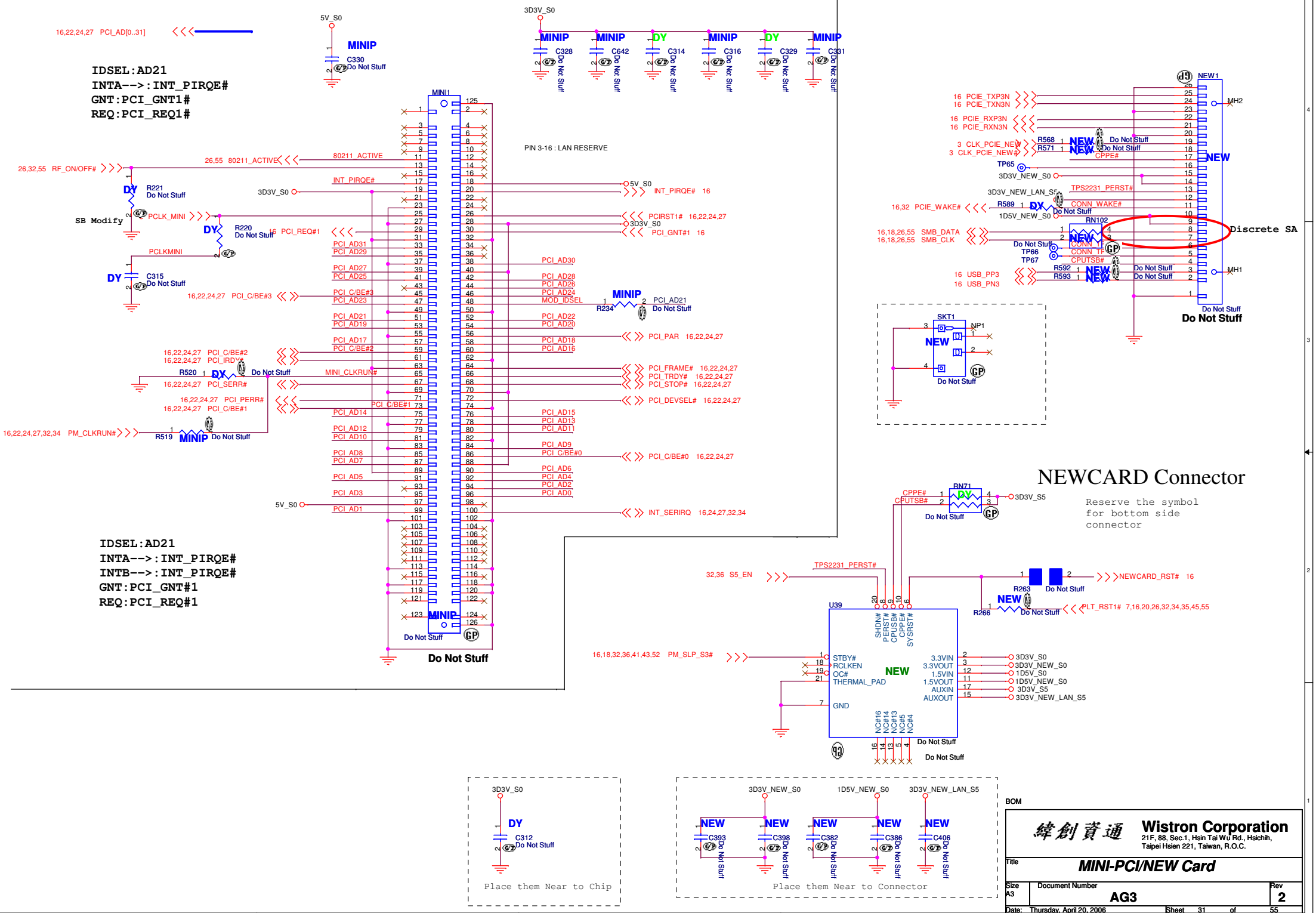
Internal Speaker

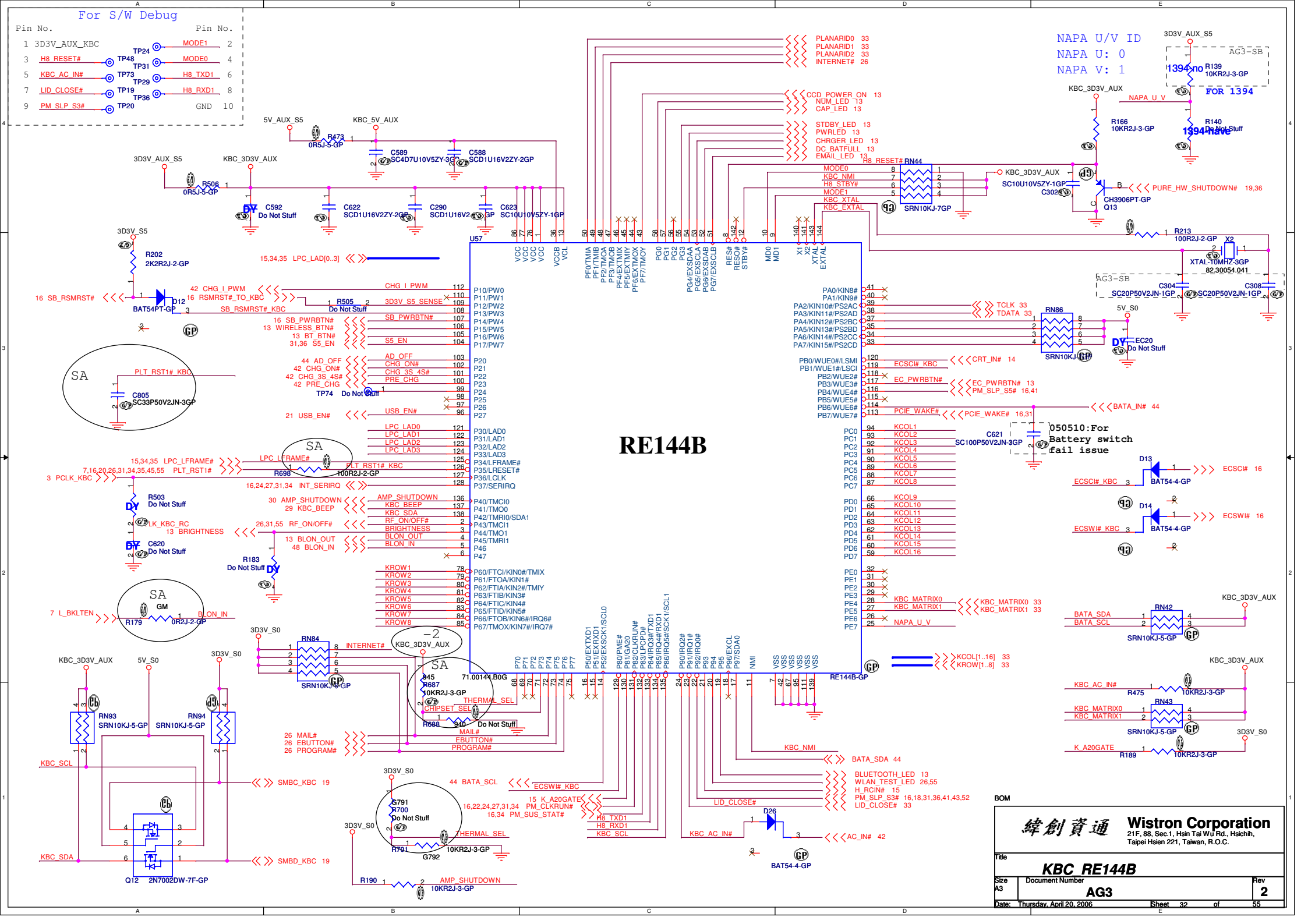


1st source: 20.D0197.104

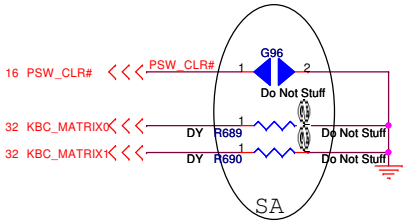
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP AND JACK	
Size: Custom	Document Number: AG3	Rev: 2
Date: Friday, April 21, 2006	Sheet 30 of 55	


IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#
PIN 3-16 : LAN RESERVE
MINI1
Do Not Stuff
IDSEL:AD21
INTA-->:INT_PIRQE#
INTB-->:INT_PIRQE#
GNT:PCI_GNT#1
REQ:PCI_REQ#1
NEWCARD Connector
Reserve the symbol for bottom side connector
Discrete SA
Do Not Stuff
Place them Near to Chip
Place them Near to Connector
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MINI-PCI/NEW Card
AG3
2
Thursday, April 20, 2006
31
55

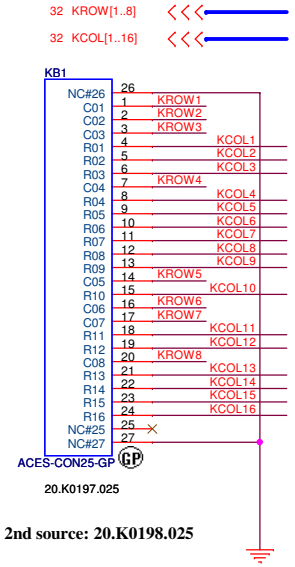

For S/W Debug
Pin No.
Pin No.
1 3D3V_AUX_KBC
TP24
MODE1 2
3 H8_RESET#
TP48
MODE0 4
TP31
5 KBC_AC_IN#
TP73
H8_TXD1 6
TP29
7 LID_CLOSE#
TP19
H8_RXD1 8
TP36
9 PM_SLP_S3#
TP20
GND 10
NAPA U/V ID
NAPA U: 0
NAPA V: 1
3D3V_AUX_S5
AG3-SB
1394 no
R139 10KR2J-3-GP
FOR 1394
KBC_3D3V_AUX
NAPA_U_V
R166 10KR2J-3-GP
R140 Do Not Stuff
1394 have
5V_AUX_S5
KBC_5V_AUX
R473 0R5J-5-GP
C589 SC4D7U10V5ZY-3GP
C588 SCD1U16V2ZY-2GP
3D3V_AUX_S5
KBC_3D3V_AUX
R506 0R5J-5-GP
C592 Do Not Stuff
C622 SCD1U16V2ZY-2GP
C290 SCD1U16V2ZY-2GP
C623 SC10U10V5ZY-1GP
3D3V_S5
R202 2K2R2J-2-GP
16 SB_RSMRST#
D12 BAT54PT-GP
42 CHG_I_PWM
16 RSMRST#_TO_KBC
SB_RSMRST#_KBC
R505 Do Not Stuff
3D3V_S5_SENSE
16 SB_PWRBTN#
13 WIRELESS_BTN#
13 BT_BTN#
31,36 S5_EN
SB_PWRBTN#
S5_EN
44 AD_OFF
42 CHG_ON#
42 CHG_3S_4S#
42 PRE_CHG
TP74 Do Not Stuff
21 USB_EN#
SA
PLT_RST1#_KBC
C805 SC33P50V2JN-3GP
15,34,35 LPC_LAD[0..3]
15,34,35 LPC_LFRAME#
7,16,20,26,31,34,35,45,55 PLT_RST1#
3 PCLK_KBC
R698 100R2J-2-GP
16,24,27,31,34 INT_SERIRQ
R503 Do Not Stuff
LK_KBC_RC
13 BRIGHTNESS
C620 Do Not Stuff
30 AMP_SHUTDOWN
29 KBC_BEEP
26,31,55 RF_ON/OFF#
13 BLON_OUT
48 BLON_IN
R183 Do Not Stuff
7 L_BKLTEN
GM
R179 0R2J-2-GP
BLON_IN
3D3V_S0
RN84 SRN10KJ-5-GP
INTERNET#
KBC_3D3V_AUX
-2
SA
R945
R687 10KR2J-3-GP
THERMAL_SEL
CHIPSET_SEL
R688 Do Not Stuff
26 MAIL#
26 EBUTTON#
26 PROGRAM#
MAIL#
EBUTTON#
PROGRAM#
KBC_3D3V_AUX
5V_S0
3D3V_S0
RN93 SRN10KJ-5-GP
RN94 SRN10KJ-5-GP
KBC_SCL
KBC_SDA
SMBC_KBC 19
SMBD_KBC 19
Q12 2N7002DW-7F-GP
3D3V_S0
G791
R700 Do Not Stuff
THERMAL_SEL
R701
G792 10KR2J-3-GP
R190 10KR2J-3-GP
AMP_SHUTDOWN
U57
RE144B
RE144B-GP
71.00144.B0G
PLANARID0 33
PLANARID1 33
PLANARID2 33
INTERNET# 26
CCD_POWER_ON 13
NUM_LED 13
CAP_LED 13
STDBY_LED 13
PWRLED 13
CHRGER_LED 13
DC_BATFULL 13
EMAIL_LED 13
H8_RESET#
RN44 SRN10KJ-7GP
MODE0
KBC_NMI
H8_STBY#
MODE1
KBC_XTAL
KBC_EXTAL
KBC_3D3V_AUX
SC10U10V5ZY-1GP
C302
PURE_HW_SHUTDOWN# 19,36
CH3906PT-GP
Q13
R213 100R2J-2-GP
X2
XTAL-10MHZ-3GP
32.30054.041
AG3-SB
C304 SC20P50V2JN-1GP
C308 SC20P50V2JN-1GP
5V_S0
RN86 SRN10KJ-5-GP
EC20 Do Not Stuff
TCLK 33
TDATA 33
CRT_IN# 14
ECSCI#_KBC
EC_PWRBTN# 13
PM_SLP_S5# 16,41
PCIE_WAKE#
PCIE_WAKE# 16,31
BATA_IN# 44
C621 SC100P50V2JN-3GP
050510:For
Battery switch
fail issue
D13 BAT54-4-GP
ECSCI# 16
ECSCI#_KBC
D14 BAT54-4-GP
ECSWI# 16
ECSWI#_KBC
KBC_MATRIX0 33
KBC_MATRIX1 33
KCOL[1..16] 33
KROW[1..8] 33
KBC_3D3V_AUX
BATA_SDA
BATA_SCL
RN42 SRN10KJ-5-GP
KBC_AC_IN#
R475 10KR2J-3-GP
KBC_MATRIX0
KBC_MATRIX1
RN43 SRN10KJ-5-GP
3D3V_S0
K_A20GATE
R189 10KR2J-3-GP
KBC_NMI
BATA_SDA 44
BLUETOOTH_LED 13
WLAN_TEST_LED 26,55
H_RCIN# 15
PM_SLP_S3# 16,18,31,36,41,43,52
LID_CLOSE# 33
LID_CLOSE#
D26 BAT54-4-GP
KBC_AC_IN#
AC_IN# 42
44 BATA_SCL
ECSWI#_KBC
15 K_A20GATE
16,22,24,27,31,34 PM_CLKRUN#
16,34 PM_SUS_STAT#
H8_TXD1
H8_RXD1
KBC_SCL
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC_RE144B
Size A3
Document Number AG3
Rev 2
Date: Thursday, April 20, 2006
Sheet 32 of 55

Internal KeyBoard Connector



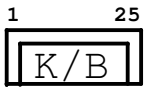
Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

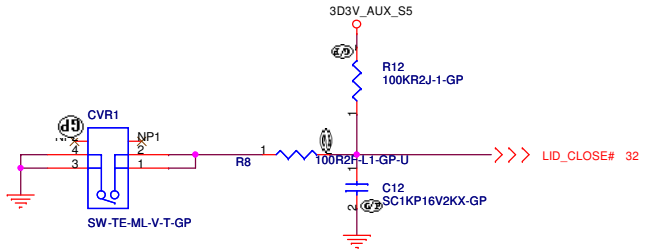


2nd source: 20.K0198.025

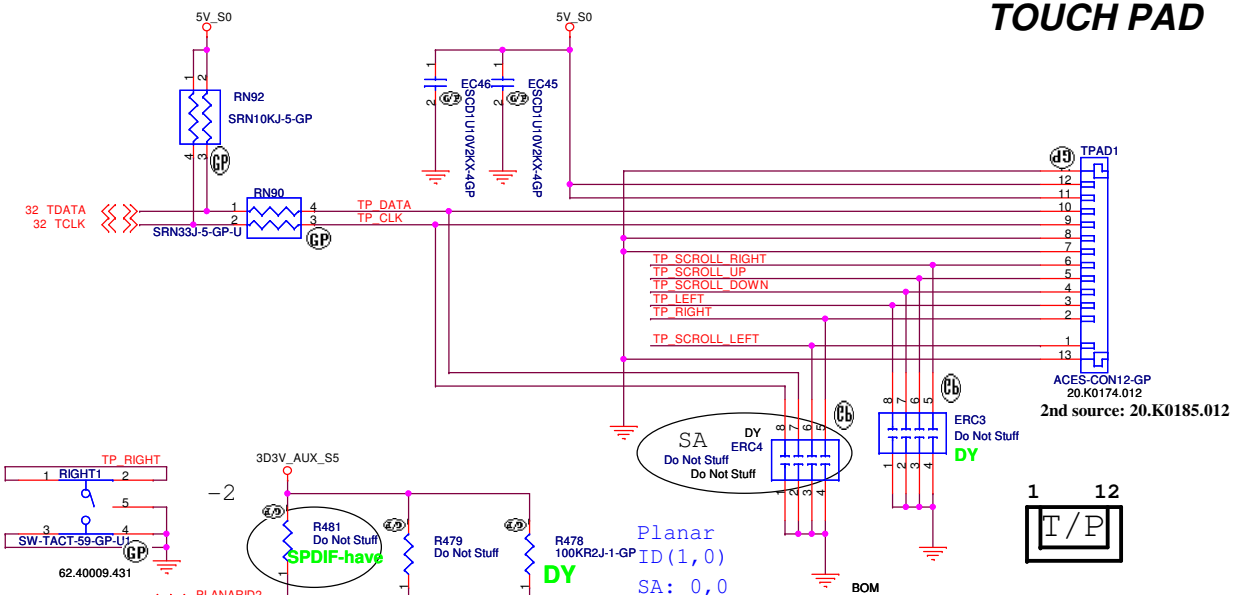
	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON



COVER SWITCH

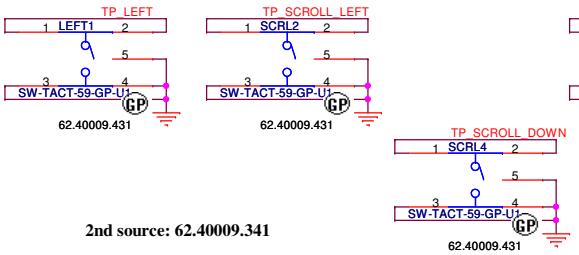


TOUCH PAD

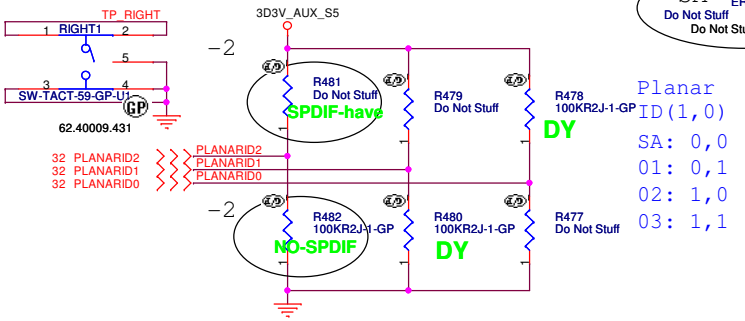


2nd source: 20.K0185.012

SCROLL KEY

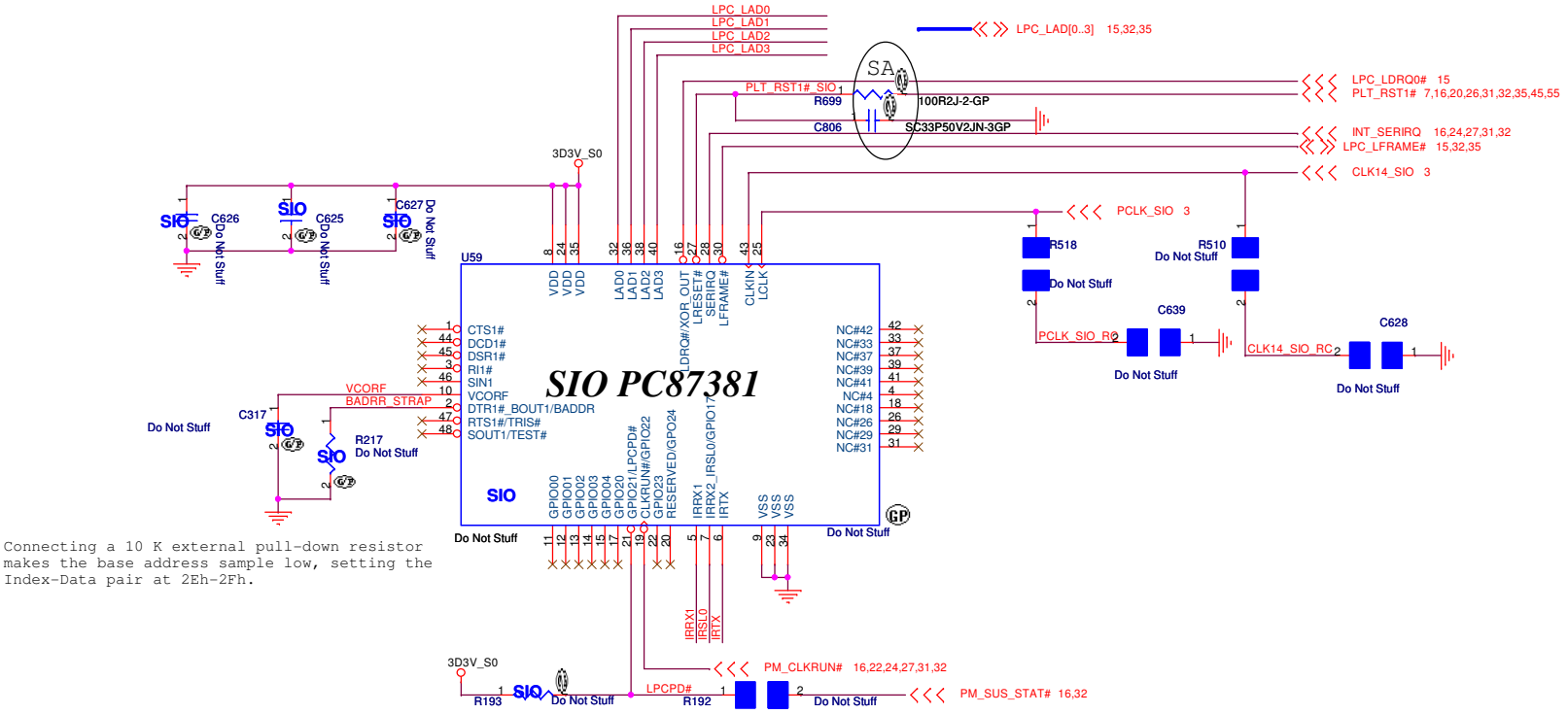


2nd source: 62.40009.341



BOM

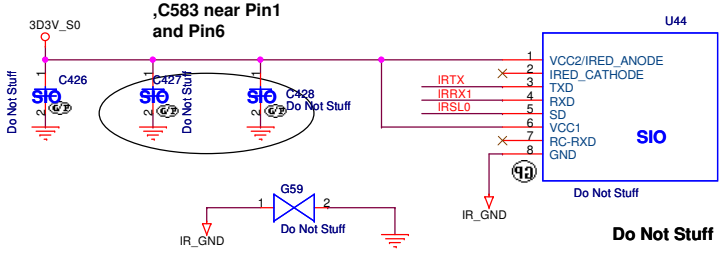
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: KEYBOARD/TOUCHPAD		
Size: A3	Document Number: AG3	Rev: 2
Date: Friday, April 21, 2006	Sheet 33 of 55	



VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

Place C581 ,C583 near Pin1 and Pin6



Do Not Stuff

BOM

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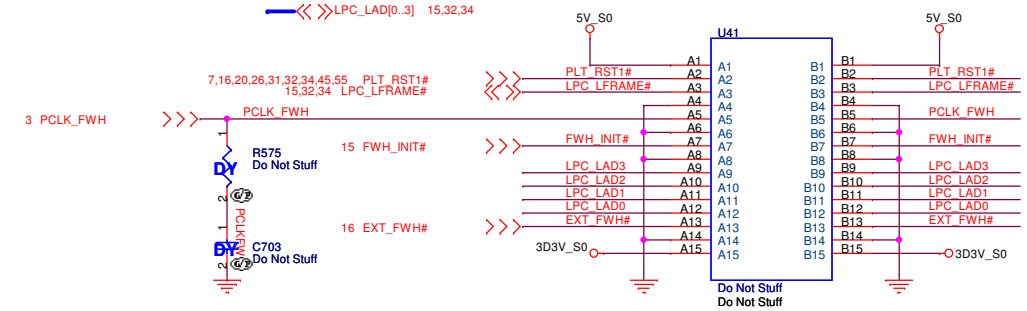
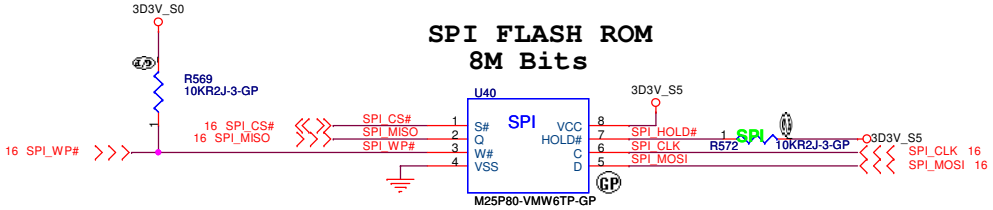
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SIO 87381 / FIR***		
Size: A3	Document Number: **AG3**	Rev: **2**
Date: Thursday, April 20, 2006	Sheet 34 of 55	

GOLDEN FINGER FOR DEBUG BOARD





72.25P80.001

SPI FLASH ROM
8M Bits

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
ST M25P80:

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

BOM

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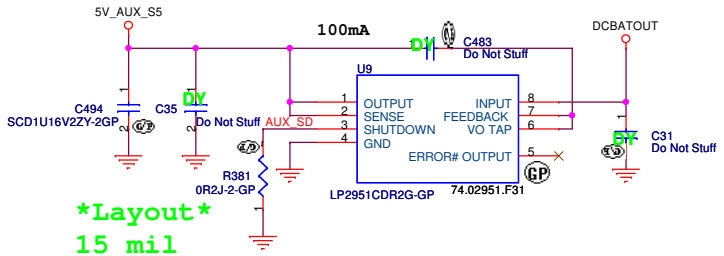
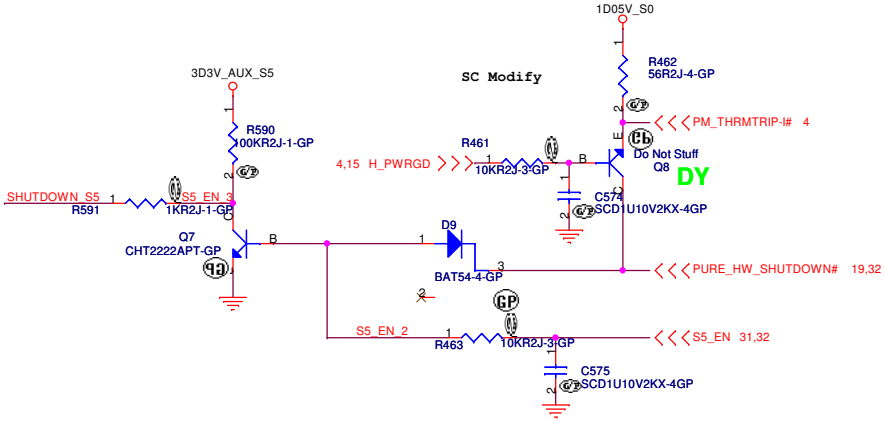
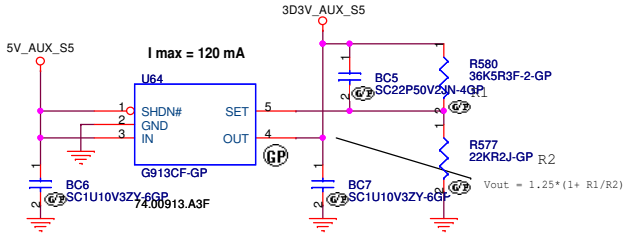
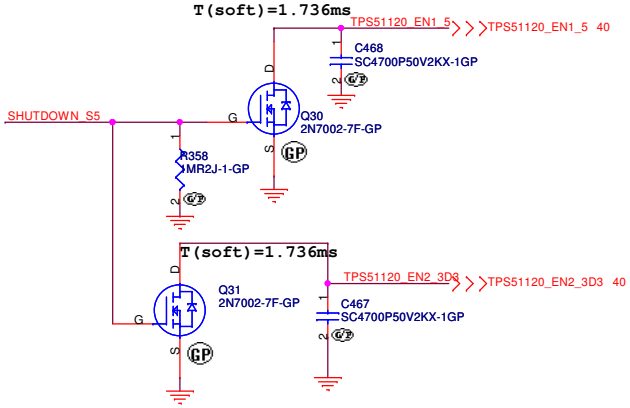
Title	***BIOS : SPI***	
Size A3	Document Number **AG3**	Rev **2**
Date: Thursday, April 20, 2006	Sheet 35 of 55	

Aux Power

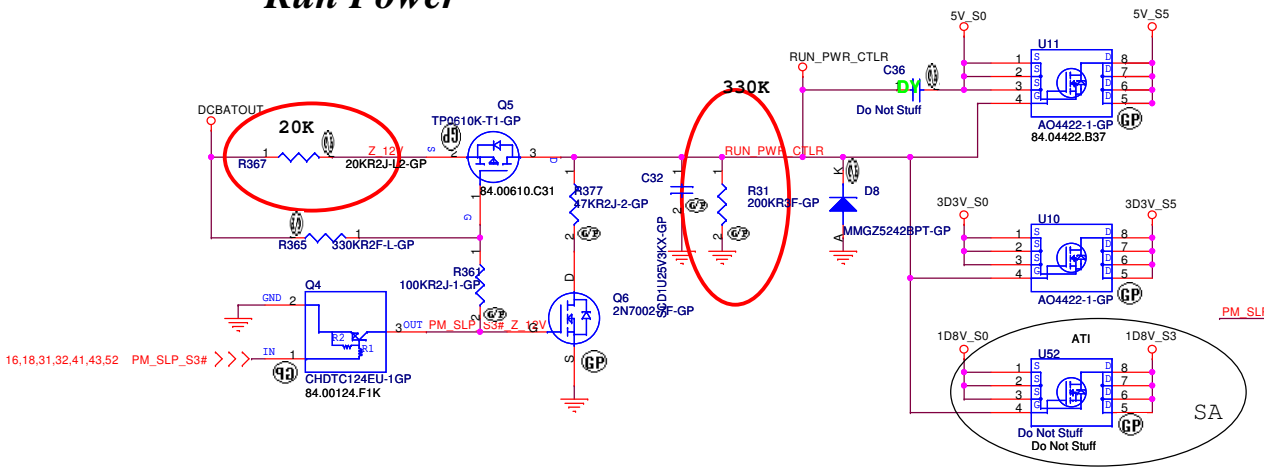








Run Power



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**RUN and AUX POWER**	
Size A3	Document Number **AG3**	Rev **2**
Date: Thursday, April 20, 2006	Sheet 36 of 55	

CPU_CORE
Intersil ISL6262

VID Setting
- VID0 (I / 1.05V)
- VID1 (I / 1.05V)
- VID2 (I / 1.05V)
- VID3 (I / 1.05V)
- VID4 (I / 1.05V)
- VID5 (I / 1.05V)
- VID6 (I / 1.05V)

H_VID0, H_VID1, H_VID2, H_VID3, H_VID4, H_VID5, H_VID6

Input Signal
- PSI# (I / 3.3V)
- PGD_IN (I / 3.3V)
- DPRSLPVR (I / 3.3V)
- DPRSTP# (I / 3.3V)

PSI#, CPUCORE_ON, PM_DPRSLPVR, H_DPRSTP#

Voltage Sense
- VSEN (I / Vcore)
- RTN (I / Vcore)

VCC_SENSE, VSS_SENSE

Input Power
- VCC (I) — DCBATOUT_6262
- VCC (I) — 5V_S0
- VCC (I) — 3D3V_S0

Output Signal
- PGOOD (OD / 3.3V) — 6262_PWRGOOD
- CLK_EN# (O) — CLK_EN#

Output Power
- VCC_CORE_PWR (O) — VCC_CORE_S0 (Imax=48A)

TI TPS51116
1.8V / 0.9V

Input Signal
- S5
- S3

PM_SLP_S5#

Input Power
- VCC (I) — DCBATOUT
- VCC (I) — 5V_S5

Output Signal
- PGOOD (OD / 3.3V) — CPUCORE_ON

Output Power
- VCC (O) — 1.8V_S3
- VCC (O) — 0.9V_S0

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5332KAC

1D5V_S0

1D8V_S3 → INPUT / OUT → 1D5V_S0

APL5912-KAC-GP

1D05V_S0

1D8V_S3 → INPUT / OUT → 1D05V_S0

APL5912-KAC-GP* 2

ISL6269_1D2V

Input Signal
- SS_STBY1 (I / 5V) FOR 1.2V

1D2V_S0_EN

Input Power
- VCC — DCBATOUT_6269
- VIN

Output Power
- 1D2V_PWR

1D2V_S0

1D8V_S0 → INPUT / OUT → 1D2V_S0

APL5331KAC-TRL

TPS51120
5V/3D3V

Input Signal
- EN1 — TPS51120_EN1_5
- EN2 — TPS51120_EN2_3D3

Input Power
- VIN — DCBATOUT_TPS51120

Output Signal
- PGOOD1 (OD / 5V) — CPUCORE_ON
- PGOOD2 (OD / 5V) — CPUCORE_ON

Output Power
- 5V (O) — 5V_DC_S5 (6A)
- 3D3V (O) — 3D3V_DC_S5 (5A)

CHARGER ISL6225

Input Signal
- ICTL — CHGON#/OFF
- PKPRES — BT_TH

Input Power
- ACIN — AD+

Output Signal
- BATT — BT+SENSE
- ACOK — AC_IN

Output Power
- VOUT (O) — BT+
- VOUT (O) — DCBATOUT

3D3V_AUX_S5

5V_S5_G913 → INPUT / OUT → 3D3V_AUX_S5

G913CF

5V_AUX_S5

DCBATOUT → INPUT / OUT → 5V_AUX_2591

LP2951ACM

Adapter

Input Signal
- (I) — AD_OFF

Input Power
- VCC (I) — AD_JK
- VCC (I) — 5V_AUX_S5

Output Signal
- (O) — AD_IN

Output Power
- VCC (O) — AD+

BOM

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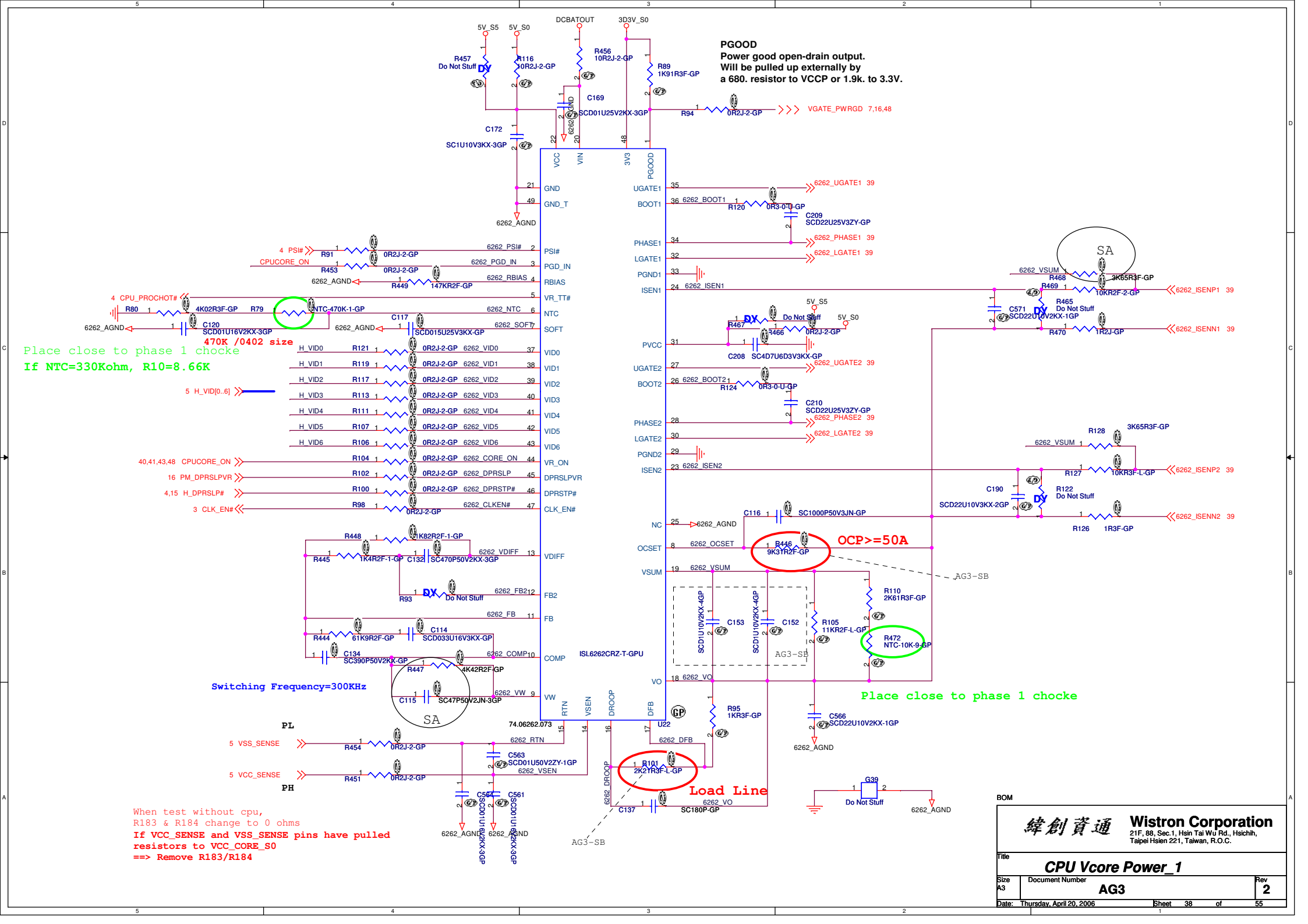
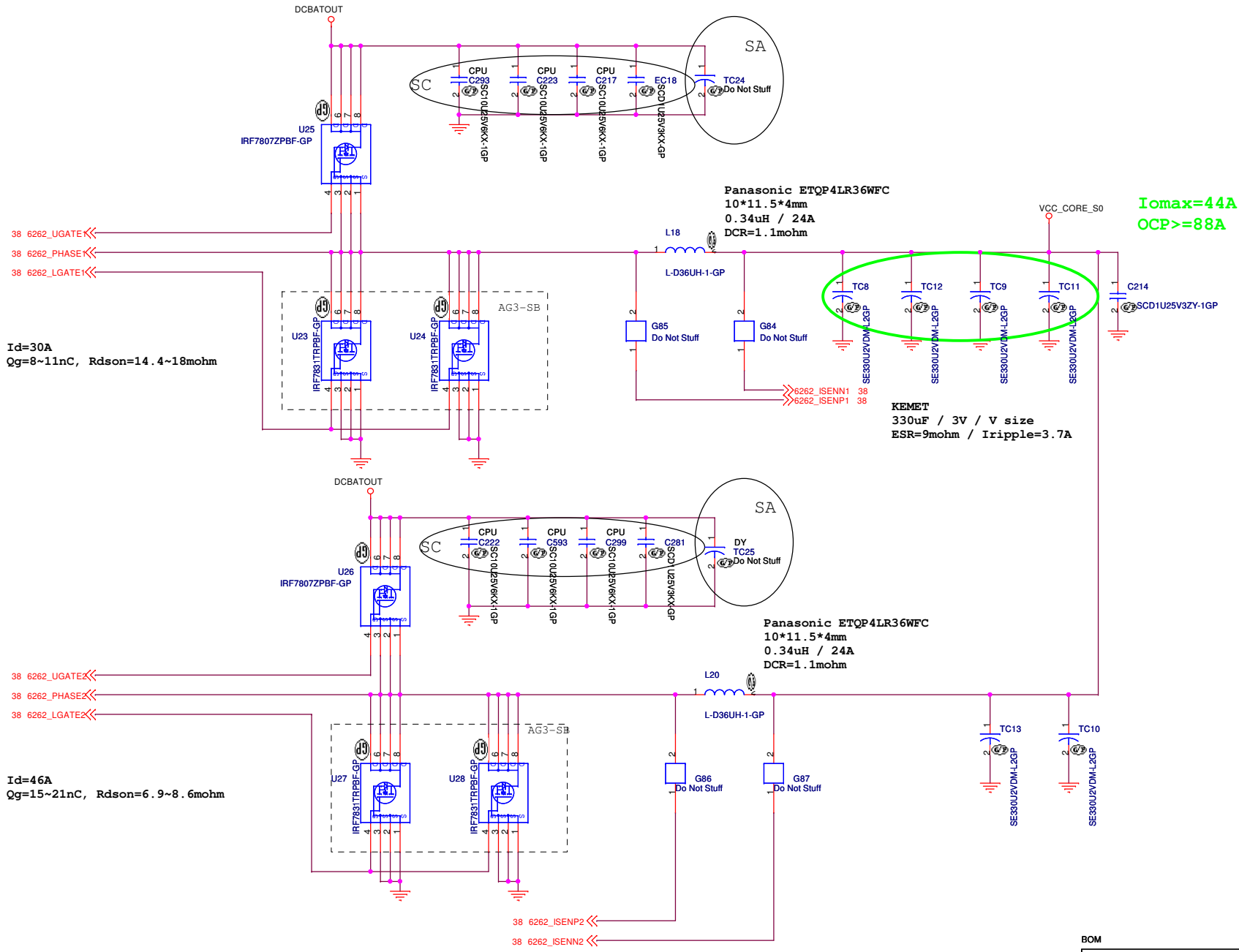
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	AG3	2

Date: Thursday, April 20, 2006 Sheet 37 of 55


PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
470K /0402 size
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
Switching Frequency=300KHz
OCP>=50A
Load Line
Place close to phase 1 chocke
When test without cpu,
R183 & R184 change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R183/R184
ISL6262CRZ-T-GPU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
AG3
Thursday, April 20, 2006



BOM

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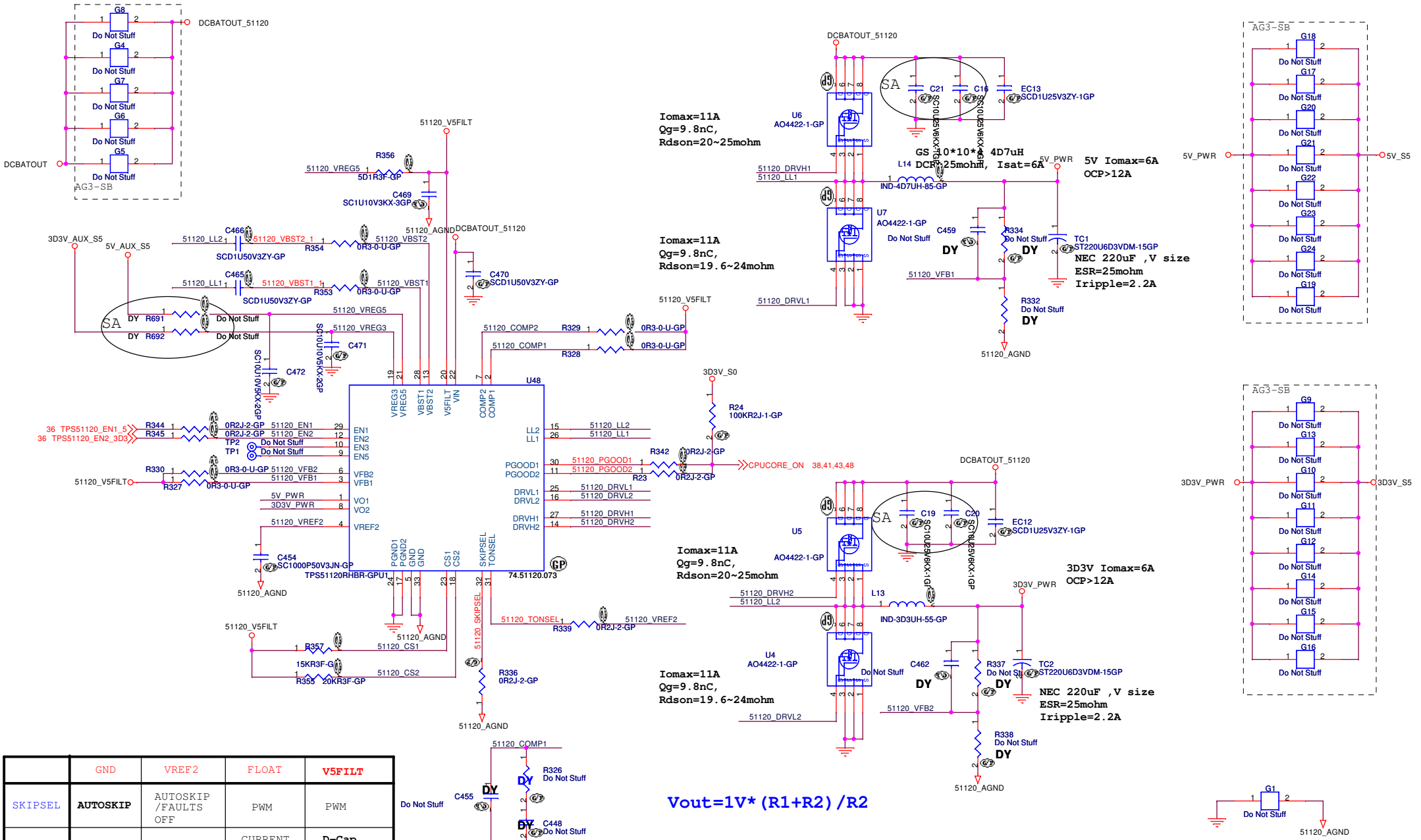
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU Vcore Power_2/2***

Size	Document Number	Rev
A3	AG3	2

Date: Friday, April 21, 2006 Sheet 39 of 55



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

BOM

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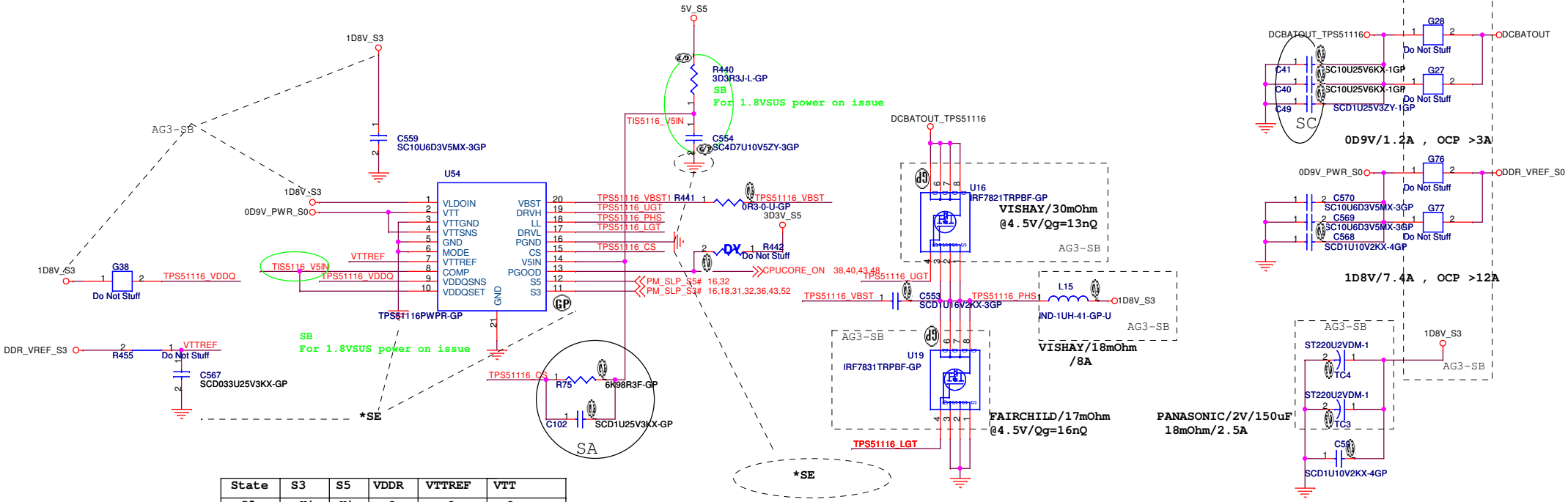
Title: **5V_UP_S5/3D3V_S5/5V_S5**

Size: A3 | Document Number: **AG3** | Rev: **2**

Date: Thursday, April 20, 2006 | Sheet 40 of 55

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

BOM

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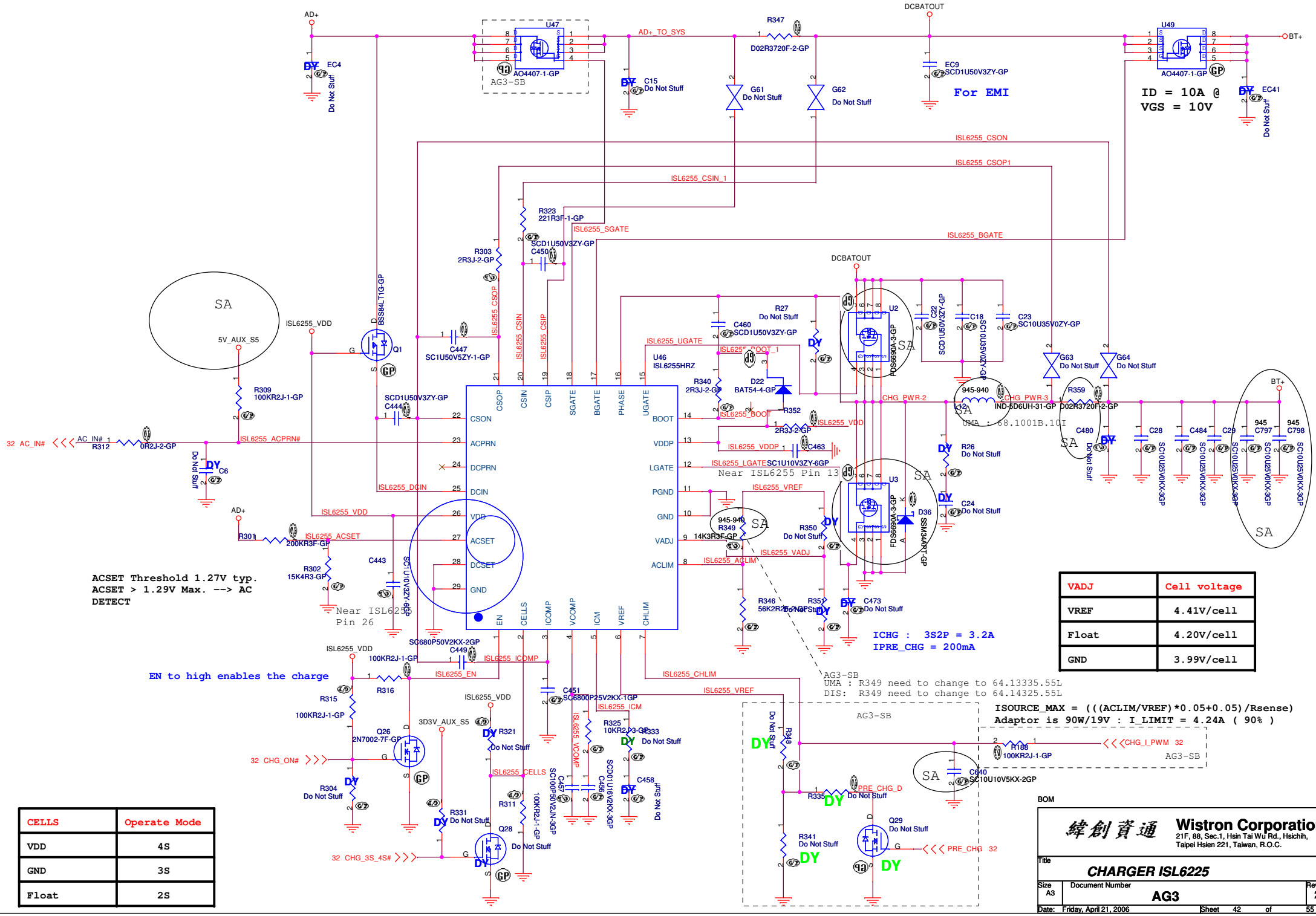
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC to DC 1.8V & 0.9V***

Size	Document Number	Rev
A3	AG3	2

Date: Friday, April 21, 2006 Sheet 41 of 55



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

BOM

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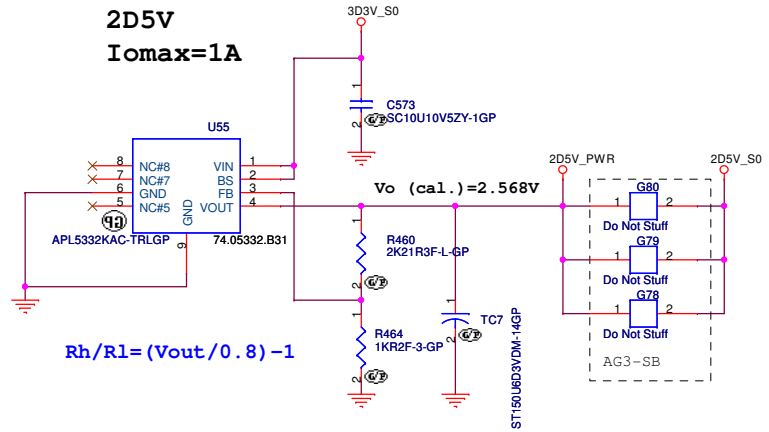
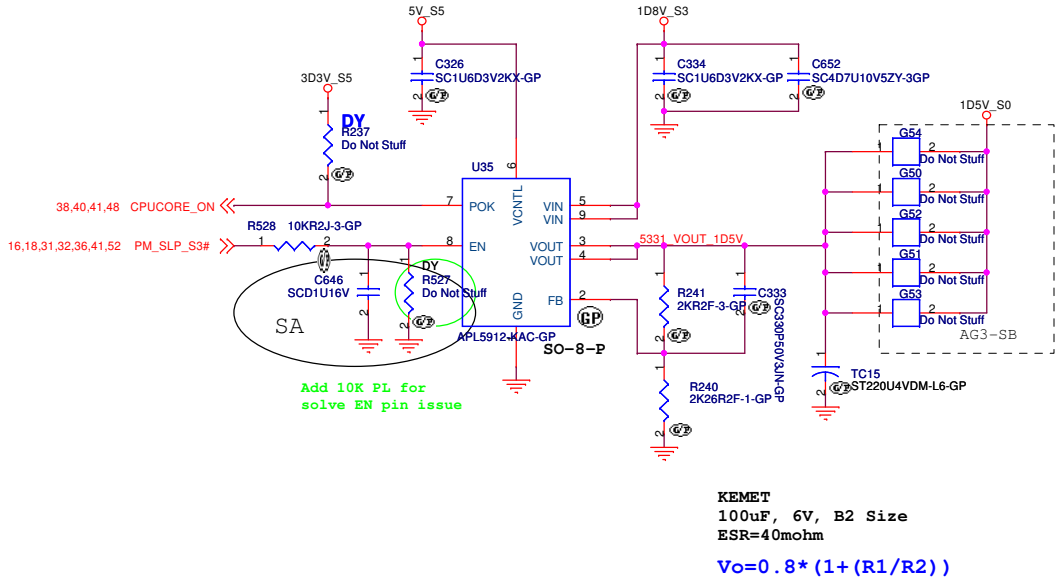
Taipei Hsien 221, Taiwan, R.O.C.

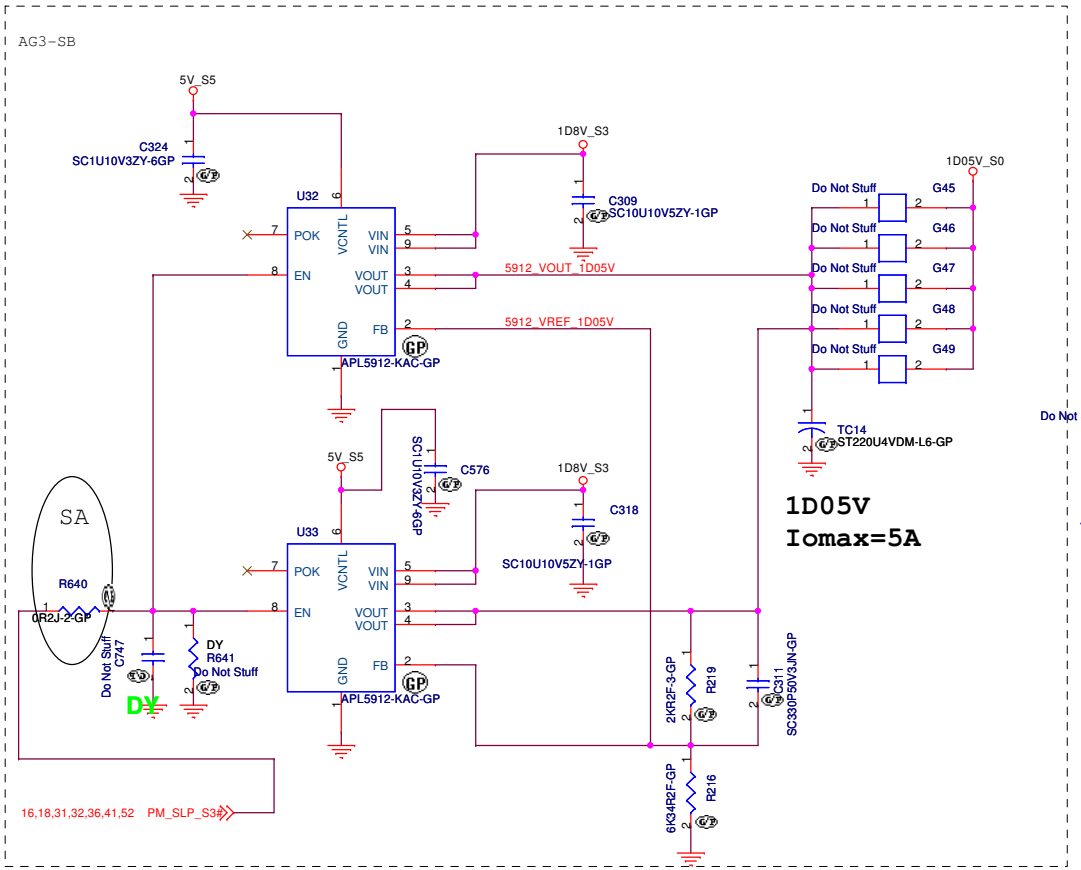
Title: CHARGER ISL6225

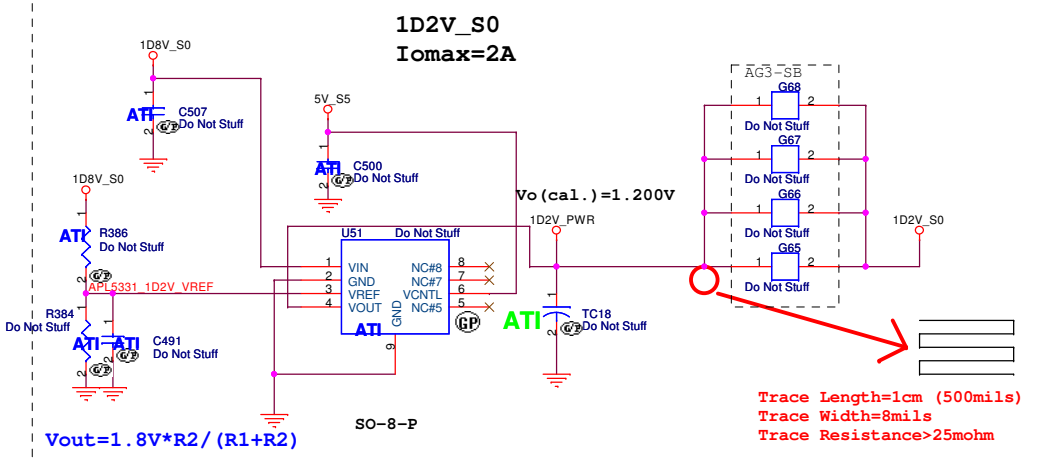
Size	Document Number	Rev
A3	AG3	2

Date: Friday, April 21, 2006 Sheet 42 of 55





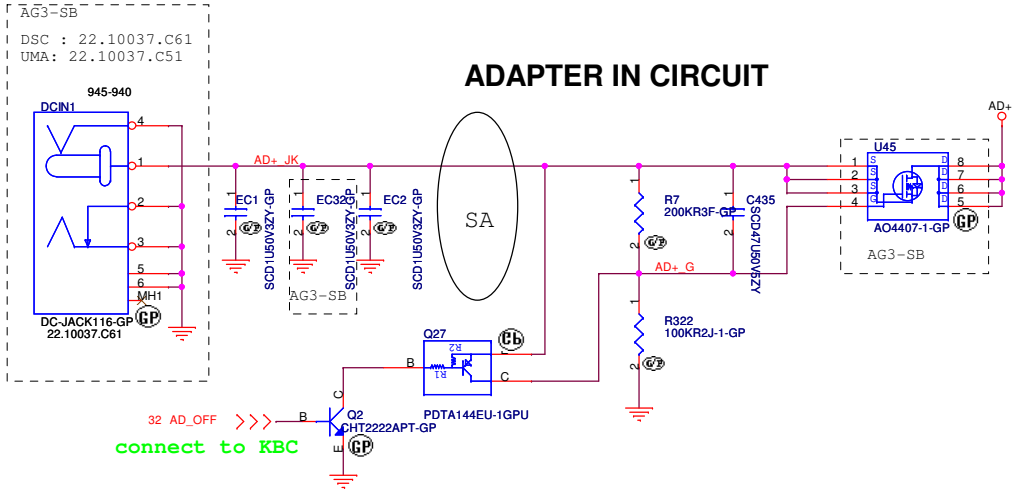




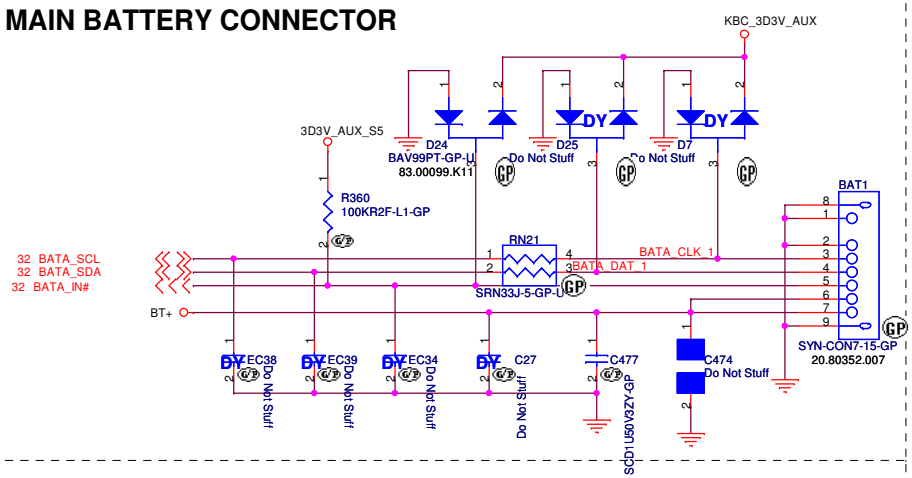
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D2V/1D5V/2D5V/1D05V_S0		
Size: A3	Document Number: AG3	Rev: 2
Date: Thursday, April 20, 2006	Sheet 43 of 55	

ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***AD/BATT CONN***	
Size A3	Document Number **AG3**	Rev **2**
Date: Friday, April 21, 2006	Sheet 44 of 55	

PCIE TEST PADS

PCIE TEST POINTS MUST BE WITHIN 250 MILS OF THE ASIC BALL WITH POSITIVE AND NEGATIVE SIGNALS THE SAME DISTANCE

PCIE SIGNALS CONNECT TO ROOT COMPLEX

REFER TO PCI EXPRESS DESIGN GUIDE FOR RECOMMENDED AC COUPLING CAPS PLACEMENT ALONG THE TX INTERCONNECT

U53A

PART 1 OF 7

PCI-EXPRESS INTERFACE

PEG_TXP0	AJ31	PCIE_RX0P	PCIE_TX0P
PEG_TXN0	AH31	PCIE_RX0N	PCIE_TX0N
PEG_TXP1	AH30	PCIE_RX1P	PCIE_TX1P
PEG_TXN1	AG30	PCIE_RX1N	PCIE_TX1N
PEG_TXP2	AG32	PCIE_RX2P	PCIE_TX2P
PEG_TXN2	AF32	PCIE_RX2N	PCIE_TX2N
PEG_TXP3	AF31	PCIE_RX3P	PCIE_TX3P
PEG_TXN3	AE31	PCIE_RX3N	PCIE_TX3N
PEG_TXP4	AE30	PCIE_RX4P	PCIE_TX4P
PEG_TXN4	AD30	PCIE_RX4N	PCIE_TX4N
PEG_TXP5	AD32	PCIE_RX5P	PCIE_TX5P
PEG_TXN5	AC32	PCIE_RX5N	PCIE_TX5N
PEG_TXP6	AC31	PCIE_RX6P	PCIE_TX6P
PEG_TXN6	AB31	PCIE_RX6N	PCIE_TX6N
PEG_TXP7	AB30	PCIE_RX7P	PCIE_TX7P
PEG_TXN7	AA30	PCIE_RX7N	PCIE_TX7N
PEG_TXP8	AA32	PCIE_RX8P	PCIE_TX8P
PEG_TXN8	Y32	PCIE_RX8N	PCIE_TX8N
PEG_TXP9	Y31	PCIE_RX9P	PCIE_TX9P
PEG_TXN9	W31	PCIE_RX9N	PCIE_TX9N
PEG_TXP10	W30	PCIE_RX10P	PCIE_TX10P
PEG_TXN10	V30	PCIE_RX10N	PCIE_TX10N
PEG_TXP11	V32	PCIE_RX11P	PCIE_TX11P
PEG_TXN11	U32	PCIE_RX11N	PCIE_TX11N
PEG_TXP12	U31	PCIE_RX12P	PCIE_TX12P
PEG_TXN12	T31	PCIE_RX12N	PCIE_TX12N
PEG_TXP13	T30	PCIE_RX13P	PCIE_TX13P
PEG_TXN13	R30	PCIE_RX13N	PCIE_TX13N
PEG_TXP14	R32	PCIE_RX14P	PCIE_TX14P
PEG_TXN14	P32	PCIE_RX14N	PCIE_TX14N
PEG_TXP15	P31	PCIE_RX15P	PCIE_TX15P
PEG_TXN15	N31	PCIE_RX15N	PCIE_TX15N

Do Not Stuff JP71 1 — PEG_TXP7
Do Not Stuff JP72 1 — PEG_TXN7

7 PEG_RXP[15..0] — PEG_RXP[15..0]
7 PEG_RXN[15..0] — PEG_RXN[15..0]
7 PEG_TXP[15..0] — PEG_TXP[15..0]
7 PEG_TXN[15..0] — PEG_TXN[15..0]

Clock

3 CLK_PCIE_PEG	CLK_PCIE_PEG	AL28 PCIE_REFCLKP
3 CLK_PCIE_PEG#	CLK_PCIE_PEG#	AK28 PCIE_REFCLKN

Calibration

PCIE_CALRN	AE24	PCIE_CALRN	R84 1 — Do Not Stuff — 1D2V_S0
PCIE_CALRP	AD24	PCIE_CALRP	R81 1 — Do Not Stuff
PCIE_CALI	AB24	PCIE_CALI	R73 1 — Do Not Stuff

FOR M26X
PCIE_CALRN = 100R
PCIE CALRP = 150R
PCIE CALI = 10K
FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE CALRP = 562R
PCIE CALI = 1.47K

PERSTB	AG24	R99 1 — Do Not Stuff — C133 — Do Not Stuff	PLT_RST1# 7,16,20,26,31,32,34,35,55
PCIE_TEST	AA24		
PERSTB_MASK	AF24	R86 1 — Do Not Stuff	

Tie To VSS

Do Not Stuff — ATI

M56: 71.0M56P.M01
M54: 71.0M54P.B0U
M52: 71.0M52P.B0U

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0)	GPIO[9,13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM	1011
MEMORY APERTURE SIZE	GPIO[13:11]	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPs
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

3D3V_S0

46 GPIO0 — ATI R33 1 — Do Not Stuff
46 GPIO1 — ATI R415 1 — Do Not Stuff
46 GPIO2 — DY R412 1 — Do Not Stuff
46 GPIO3 — DY R419 1 — Do Not Stuff
46 GPIO4 — DY R396 1 — Do Not Stuff
46 GPIO5 — ATI R408 1 — Do Not Stuff
46 GPIO6 — DY R413 1 — Do Not Stuff
46 GPIO8 — DY R36 1 — Do Not Stuff
46 GPIO11 — DY R389 1 — Do Not Stuff
46 GPIO12 — 256M R392 1 — Do Not Stuff
46 GPIO13 — DY R34 1 — Do Not Stuff
46 GPIO9 — ATI R35 1 — Do Not Stuff

GPIO[9,13:11]=0000 for 128M

46 MEM_ID3 — DY R44 1 — Do Not Stuff
46 MEM_ID2 — DY R40 1 — Do Not Stuff
46 MEM_ID1 — 128in256 R46 1 — Do Not Stuff
46 MEM_ID0 — 128hy256 R47 1 — Do Not Stuff
46 DAC2_HSY — DY R65 1 — Do Not Stuff
46 DAC2_VSY — DY R66 1 — Do Not Stuff
46 GENERICC — DY R85 1 — Do Not Stuff
PCIE_TEST — DY R76 1 — Do Not Stuff

When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

BOM

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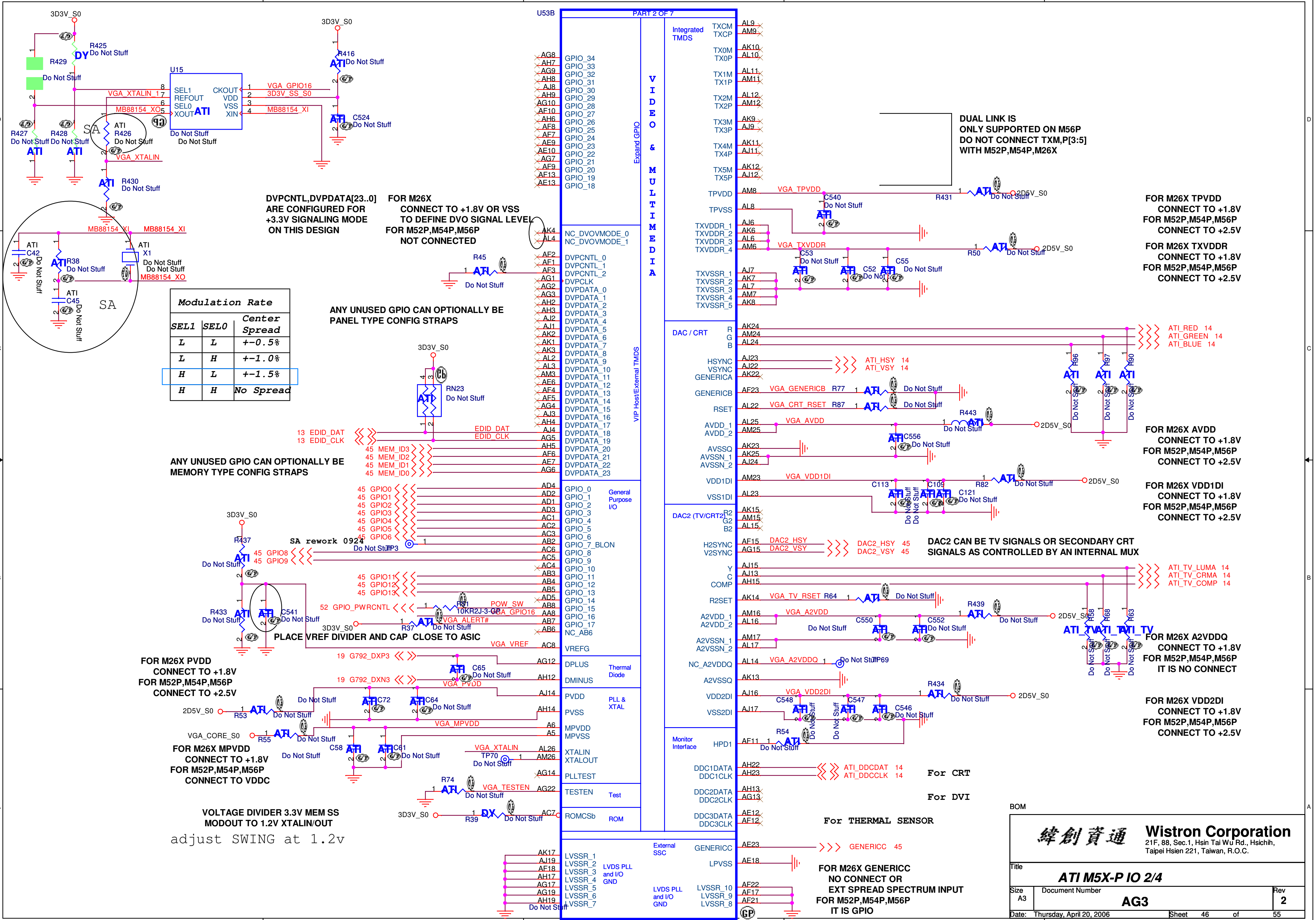
Title: ATI M5X-P PCIE 1/4

Size	Document Number	Rev
A3	AG3	2

Date: Thursday, April 20, 2006 Sheet 45 of 55



Modulation Rate

SEL1	SEL0	Center Spread
L	L	+-0.5%
L	H	+-1.0%
H	L	+-1.5%
H	H	No Spread

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Title: **ATI M5X-P IO 2/4**

Size: A3 | Document Number: AG3 | Rev: 2

Date: Thursday, April 20, 2006 | Sheet 46 of 55

U53C

Part 3 of 7

MEMORY INTERFACE A

ATI

Do Not Stuff

M31 DQA_0
M30 DQA_1
L31 DQA_2
L30 DQA_3
H30 DQA_4
G31 DQA_5
G30 DQA_6
F31 DQA_7
M27 DQA_8
M29 DQA_9
L28 DQA_10
L27 DQA_11
J27 DQA_12
H29 DQA_13
G29 DQA_14
G27 DQA_15
M26 DQA_16
L26 DQA_17
M25 DQA_18
L25 DQA_19
J25 DQA_20
G28 DQA_21
H27 DQA_22
H26 DQA_23
F26 DQA_24
G26 DQA_25
H25 DQA_26
H24 DQA_27
H23 DQA_28
H22 DQA_29
J23 DQA_30
J22 DQA_31
E23 DQA_32
D22 DQA_33
D23 DQA_34
E22 DQA_35
E20 DQA_36
F20 DQA_37
D19 DQA_38
D18 DQA_39
B19 DQA_40
B18 DQA_41
C17 DQA_42
B17 DQA_43
C14 DQA_44
B14 DQA_45
C13 DQA_46
B13 DQA_47
D17 DQA_48
E18 DQA_49
E17 DQA_50
F17 DQA_51
E15 DQA_52
E14 DQA_53
F14 DQA_54
D13 DQA_55
H18 DQA_56
H17 DQA_57
G18 DQA_58
G17 DQA_59
G15 DQA_60
G14 DQA_61
H14 DQA_62
J14 DQA_63

C31 MVREFD_0
C30 MVREFS_0

MAA_0 D26
MAA_1 F28
MAA_2 D28
MAA_3 D25
MAA_4 E24
MAA_5 E26
MAA_6 D27
MAA_7 F25
MAA_8 C26
MAA_9 B26
MAA_10 D29
MAA_11 B27
MAA_12 E27
MAA_13 E29
MAA_14 B25
MAA_15 C25

DQMAb_0 H31
DQMAb_1 J29
DQMAb_2 J26
DQMAb_3 G23
DQMAb_4 E21
DQMAb_5 B15
DQMAb_6 D14
DQMAb_7 J17

read strobe
QSA_0 J31
QSA_1 K29
QSA_2 K25
QSA_3 F23
QSA_4 D20
QSA_5 B16
QSA_6 D16
QSA_7 H15

write strobe
QSA_0B K31
QSA_1B K28
QSA_2B K26
QSA_3B G24
QSA_4B D21
QSA_5B C16
QSA_6B D15
QSA_7B J15

ODTA F29
ODTA1 D24

CLKA0 D31
CLKA0b E31

CKEA0 B30

RASA0b B28

CASA0b C29

WEA0b B31

CSA0b_0 B29
CSA0b_1 C28

CLKA1 B20
CLKA1b C19

CKEA1 C22

RASA1b B24

CASA1b B22

WEA1b B21

CSA1b_0 B23
CSA1b_1 C23

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

Ch-A
FOR M52P,M54P,M26X
PIN B25 IS MA12 (BA0)
PIN C25 IS MA13 (BA1)
PIN E29 IS MA15 (BA2)
PIN E27 IS MA14
FOR M56P
PIN B25 IS MA14 (BA0)
PIN C25 IS MA15 (BA1)
PIN E29 IS MA13 (BA2)
PIN E27 IS MA12

1D8V_S0

R48 Do Not Stuff

R49 Do Not Stuff

C54 Do Not Stuff

R47 Do Not Stuff

R42 Do Not Stuff

C51 Do Not Stuff

RN22 Do Not Stuff

R52 Do Not Stuff

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

U53D

Part 4 of 7

MEMORY INTERFACE B

ATI

Do Not Stuff

MDB0 B12
MDB1 C12
MDB2 B11
MDB3 C11
MDB4 C8
MDB5 B7
MDB6 C7
MDB7 B6
MDB8 F12
MDB9 D12
MDB10 E11
MDB11 F11
MDB12 F9
MDB13 D8
MDB14 D7
MDB15 F7
MDB16 G12
MDB17 G11
MDB18 H12
MDB19 H11
MDB20 H9
MDB21 E7
MDB22 F8
MDB23 G8
MDB24 G6
MDB25 G7
MDB26 H8
MDB27 J8
MDB28 K8
MDB29 L8
MDB30 K9
MDB31 L9
MDB32 K5
MDB33 L4
MDB34 K4
MDB35 L5
MDB36 N5
MDB37 N6
MDB38 P4
MDB39 R4
MDB40 P2
MDB41 R2
MDB42 T3
MDB43 T2
MDB44 W3
MDB45 W2
MDB46 Y3
MDB47 Y2
MDB48 T4
MDB49 R5
MDB50 T5
MDB51 T6
MDB52 V5
MDB53 W5
MDB54 W6
MDB55 Y4
MDB56 R8
MDB57 T8
MDB58 R7
MDB59 T7
MDB60 V7
MDB61 W7
MDB62 W8
MDB63 W9

DQB_0 DQB_1 DQB_2 DQB_3 DQB_4 DQB_5 DQB_6 DQB_7 DQB_8 DQB_9 DQB_10 DQB_11 DQB_12 DQB_13 DQB_14 DQB_15 DQB_16 DQB_17 DQB_18 DQB_19 DQB_20 DQB_21 DQB_22 DQB_23 DQB_24 DQB_25 DQB_26 DQB_27 DQB_28 DQB_29 DQB_30 DQB_31 DQB_32 DQB_33 DQB_34 DQB_35 DQB_36 DQB_37 DQB_38 DQB_39 DQB_40 DQB_41 DQB_42 DQB_43 DQB_44 DQB_45 DQB_46 DQB_47 DQB_48 DQB_49 DQB_50 DQB_51 DQB_52 DQB_53 DQB_54 DQB_55 DQB_56 DQB_57 DQB_58 DQB_59 DQB_60 DQB_61 DQB_62 DQB_63

MVREFD_1
MVREFS_1

DRAM_RST AA3
TEST_MCLK AA5
TEST_YCLK AA2
MEMTEST AA7

MAB_0 G4
MAB_1 E6
MAB_2 E4
MAB_3 H4
MAB_4 J5
MAB_5 G5
MAB_6 F4
MAB_7 H6
MAB_8 G3
MAB_9 G2
MAB_10 D4
MAB_11 F2
MAB_12 F5
MAB_13 D5
MAB_14 H2
MAB_15 H3

MAB0
MAB1
MAB2
MAB3
MAB4
MAB5
MAB6
MAB7
MAB8
MAB9
MAB10
MAB11

MAB12_14_50,51
TP6 Do Not Stuff
B_BA0 50,51
B_BA1 50,51

DQMBb_0 B8
DQMBb_1 D9
DQMBb_2 G9
DQMBb_3 K7
DQMBb_4 M5
DQMBb_5 V2
DQMBb_6 W4
DQMBb_7 T9

DQMB#0
DQMB#1
DQMB#2
DQMB#3
DQMB#4
DQMB#5
DQMB#6
DQMB#7

read strobe
QSB_0 B9
QSB_1 D10
QSB_2 H10
QSB_3 K6
QSB_4 N4
QSB_5 U2
QSB_6 U4
QSB_7 V8

RDQSB0
RDQSB1
RDQSB2
RDQSB3
RDQSB4
RDQSB5
RDQSB6
RDQSB7

write strobe
QSB_0B B10
QSB_1B E10
QSB_2B G10
QSB_3B J7
QSB_4B M4
QSB_5B U3
QSB_6B V4
QSB_7B V9

WDQSB0
WDQSB1
WDQSB2
WDQSB3
WDQSB4
WDQSB5
WDQSB6
WDQSB7

For GDDR2

ODTB D6
ODTB1 J4

ODTB0
ODTB1

ODTB0 50
ODTB1 50,51

CLKB0 B4
CLKB0b B5

CKEB0 C2

RASB0b E2

CASB0b D3

WEB0b B2

CSB0b_0 D2
CSB0b_1 E3

CSB0_0#
CSB0_1#

TP4 Do Not Stuff

CLKB1 N2
CLKB1b P3

CKEB1 L3

RASB1b J2

CASB1b L2

WEB1b M2

CSB1b_0 K2
CSB1b_1 K3

CSB1_0#
CSB1_1#

TP5 Do Not Stuff

Ch-B
FOR M52P,M54P,M26X
PIN H2 IS MAB12 (BA0)
PIN H3 IS MAB13 (BA1)
PIN D5 IS MAB15 (BA2)
PIN F5 IS MAB14
FOR M56P
PIN H2 IS MA14 (BA0)
PIN H3 IS MA15 (BA1)
PIN D5 IS MA13 (BA2)
PIN F5 IS MAB12

50 RASB0#
50,51 RASB1#
RASB0#
RASB1#

50 CASB0#
50,51 CASB1#
CASB0#
CASB1#

50 WEB0#
50,51 WEB1#
WEB0#
WEB1#

50 CSB0_0#
CSB0_0#

50,51 CSB1_0#
CSB1_0#

50 CKEB0
50,51 CKEB1
CKEB0
CKEB1

50 CLKB0
50 CLKB0#
CLKB0
CLKB0#

51 CLKB1
51 CLKB1#
CLKB1
CLKB1#

50,51 RDQSB[7..0]
RDQSB[7..0]

50,51 DQMB#[7..0]
DQMB#[7..0]

50,51 MDB[63..0]
MDB[63..0]

50,51 MAB[11..0]
MAB[11..0]

50,51 WDQSB[7..0]
WDQSB[7..0]

BOM

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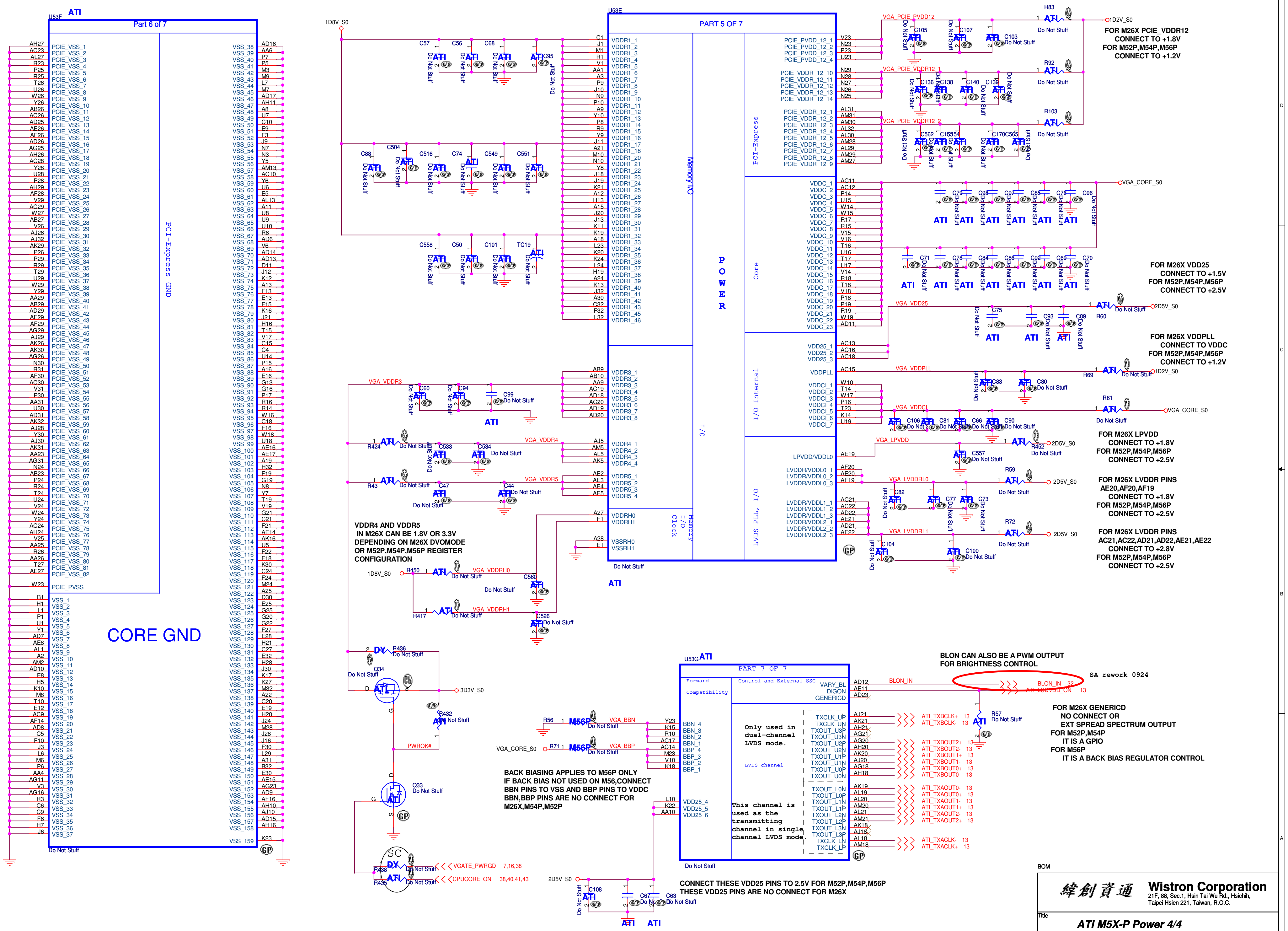
Title: ATI M5X-P MEM 3/4

Size: A3 | Document Number: AG3 | Rev: 2

Date: Thursday, April 20, 2006 | Sheet 47 of 55



BOM

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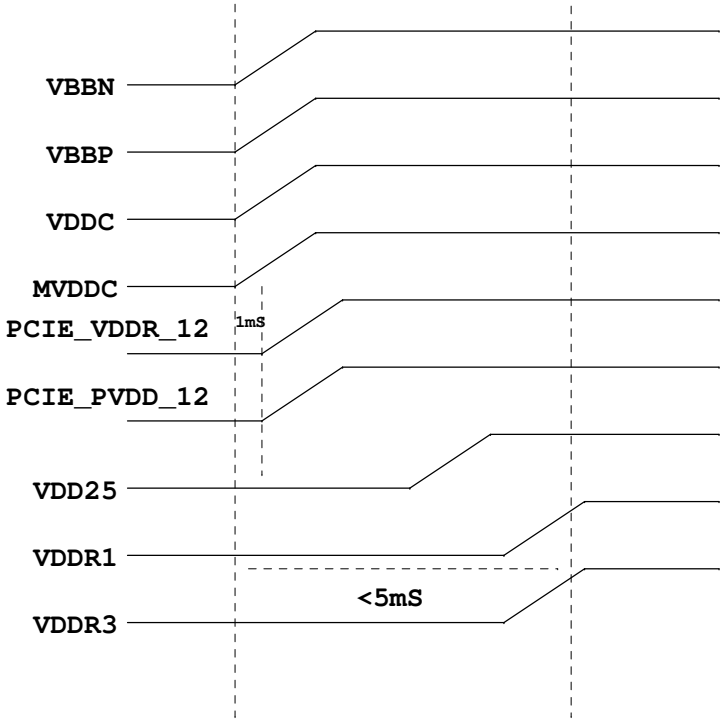
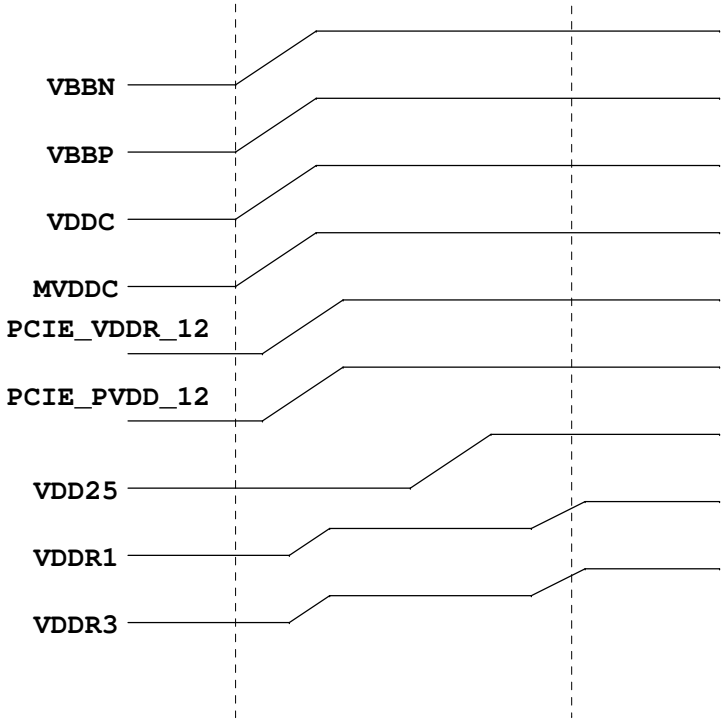
Title		
ATI M5X-P Power 4/4		
Size: C	Document Number: AG3	Rev: 2
Date: Thursday, April 20, 2006	Sheet 48 of 55	

Ideal Power Up Sequence



Real Power Up Sequence



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

General Guidelines:

- **BBN and BBP must ramp up before or at the same time as VDDC but not after.**
- **VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).**
- **All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).**
- **VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.**
- **The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.**

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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Title: ATI M5X-P POWER SEQUENCE

Size	Document Number	Rev
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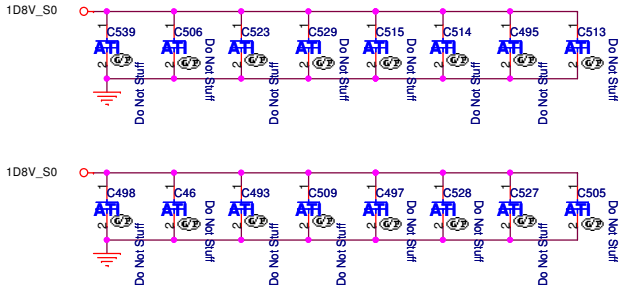
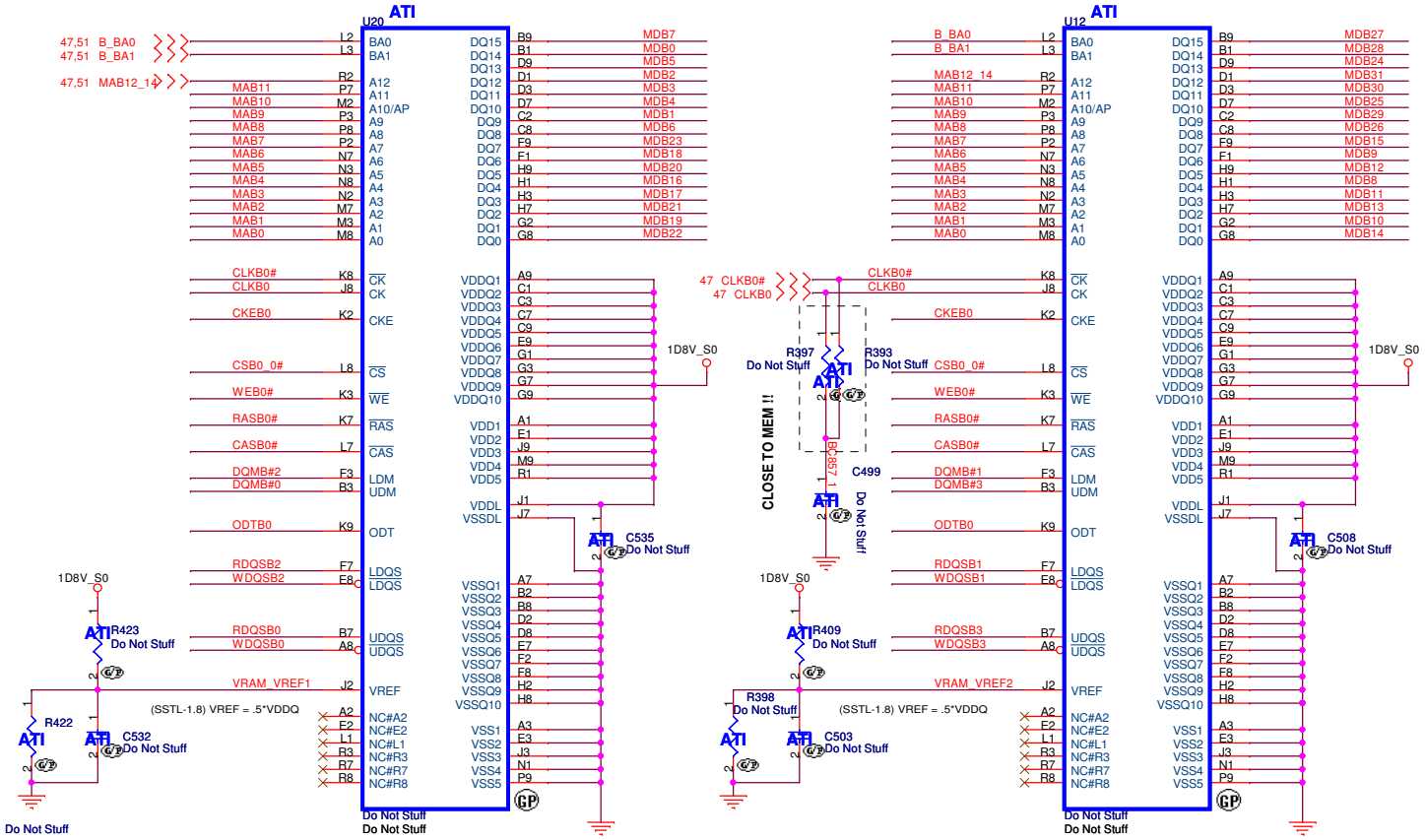
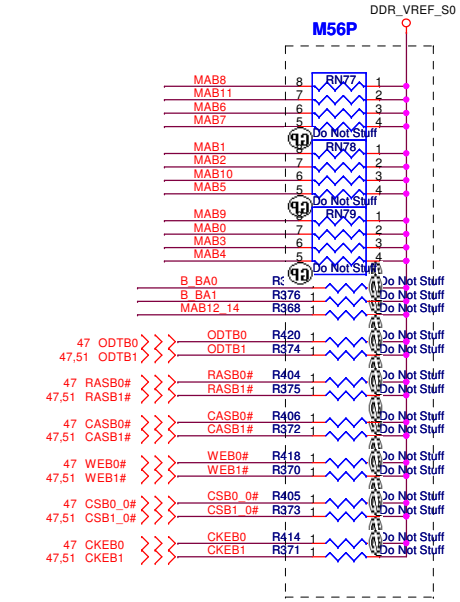
Date: Thursday, April 20, 2006 Sheet 49 of 55

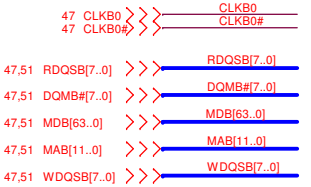
CHAN B DDR2 84BGA 32MX16 MEMORY







FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP TO A VTT RAIL (50% OF VDDQ)



72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 350Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA (16M*16, 350Mhz)
72.18512.A0U IC VRAM HYB18T512161BF-25 BGA (32M*16, 400Mhz)

BOM

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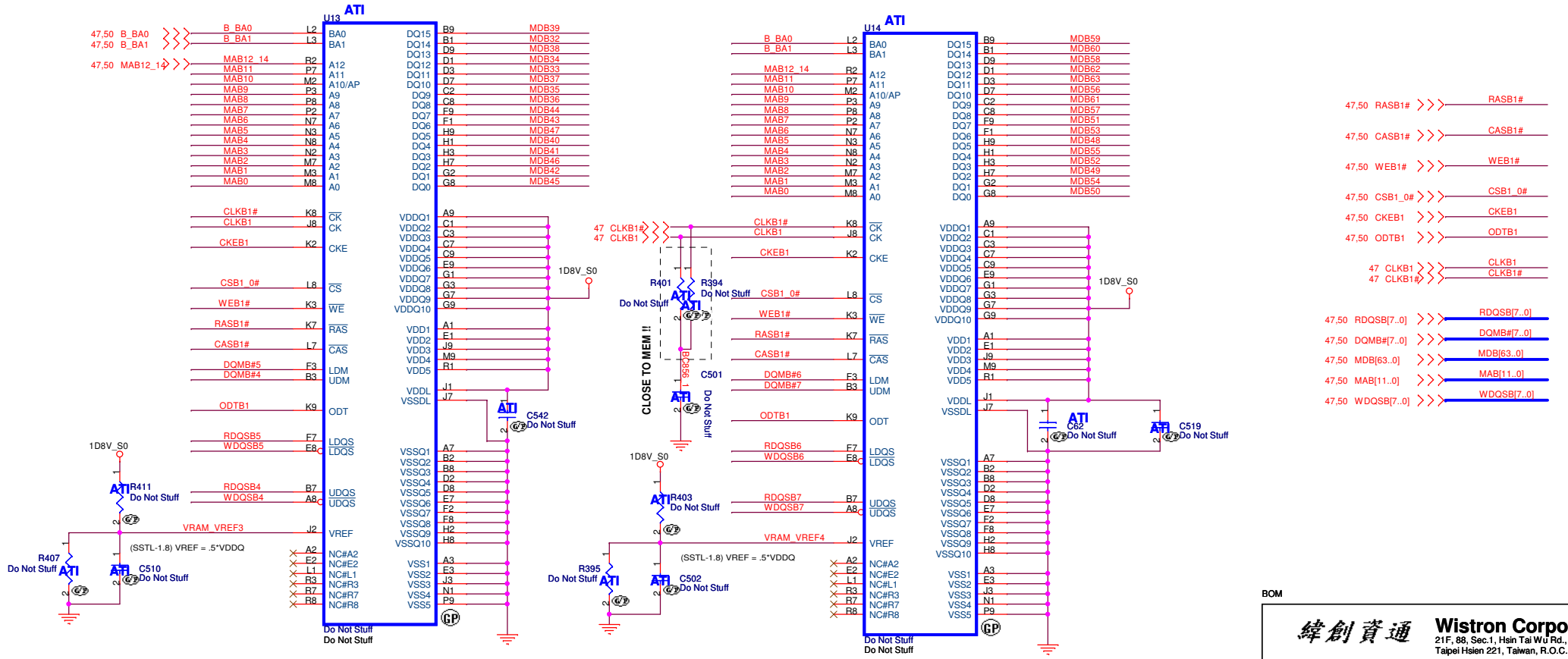
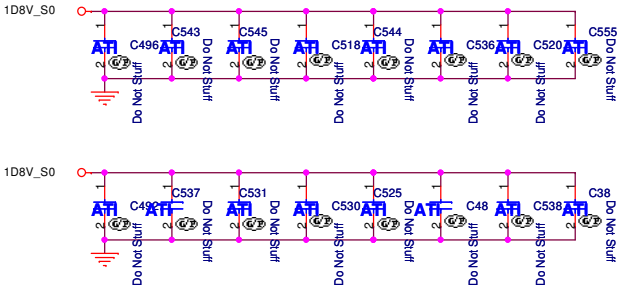
Title: ***VRAM 1/2***

Size	Document Number	Rev
A3	AG3	2

Date: Thursday, April 20, 2006 Sheet 50 of 55





47,50 RASB1# RASB1#
47,50 CASB1# CASB1#
47,50 WEB1# WEB1#
47,50 CSB1_0# CSB1_0#
47,50 CKEB1 CKEB1
47,50 ODTB1 ODTB1
47 CLKB1 CLKB1
47 CLKB1# CLKB1#
47,50 RDQSB[7..0] RDQSB[7..0]
47,50 DQMB#[7..0] DQMB#[7..0]
47,50 MDB[63..0] MDB[63..0]
47,50 MAB[11..0] MAB[11..0]
47,50 WDQSB[7..0] WDQSB[7..0]

BOM

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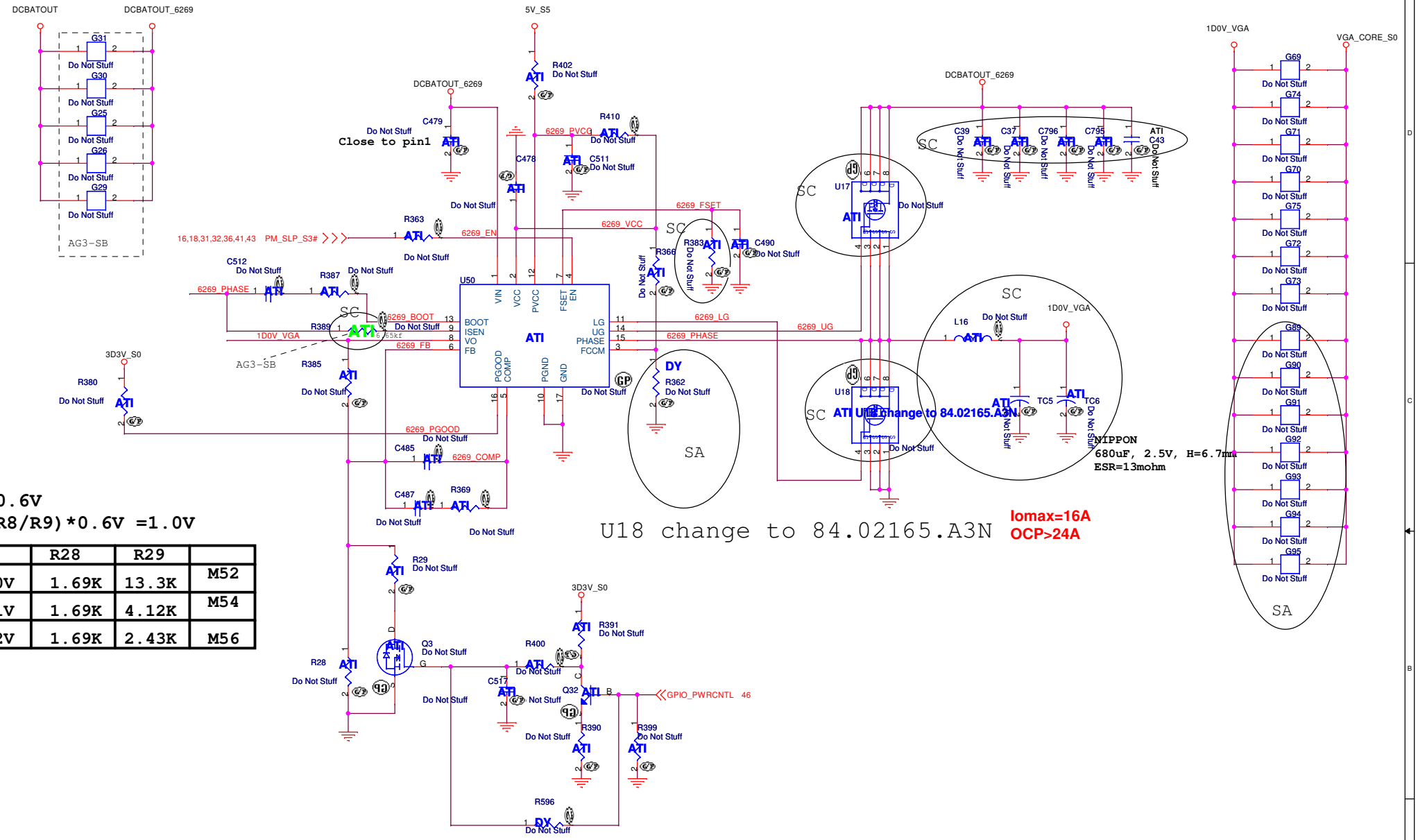
Title: ***VRAM 2/2***

Size	Document Number	Rev
A3	AG3	2

Date: Thursday, April 20, 2006 Sheet 51 of 55



Vref = 0.6V

Vo = (1+R8/R9)*0.6V =1.0V

Voltage	R28	R29	
0.95V-1.0V	1.69K	13.3K	M52
0.95V-1.1V	1.69K	4.12K	M54
0.95V-1.2V	1.69K	2.43K	M56

BOM

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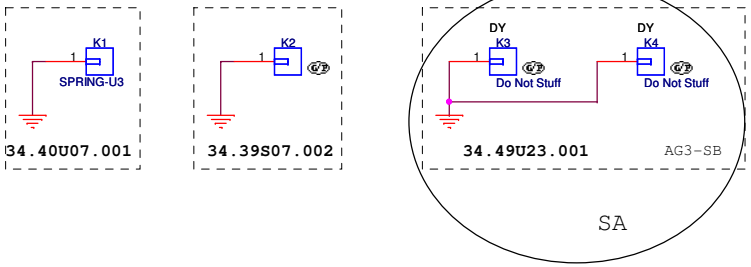
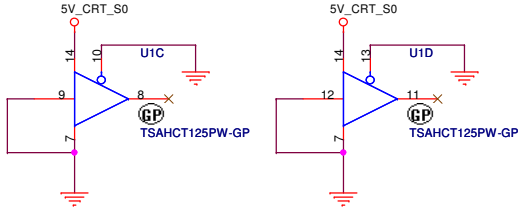
Taipei Hsien 221, Taiwan, R.O.C.

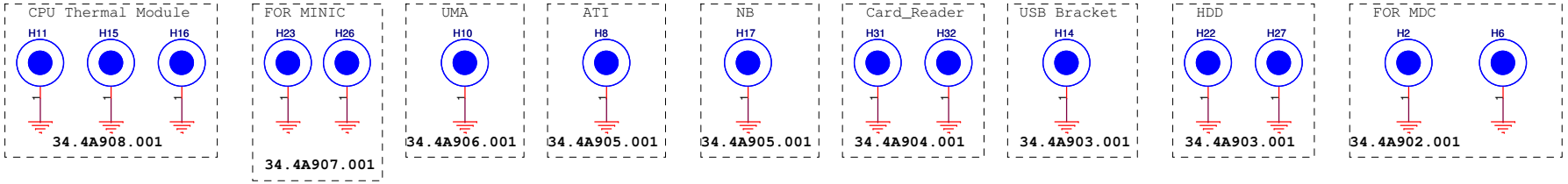
Title: **VGA CORE 1D1V**

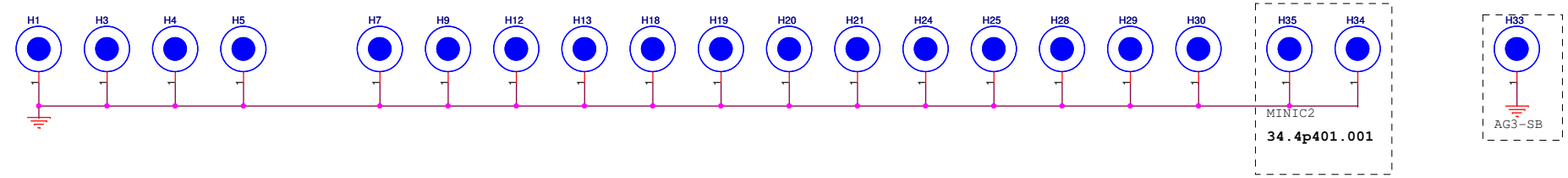
Size: A3 | Document Number: **AG3** | Rev: **2**

Date: Thursday, April 20, 2006 | Sheet 52 of 55









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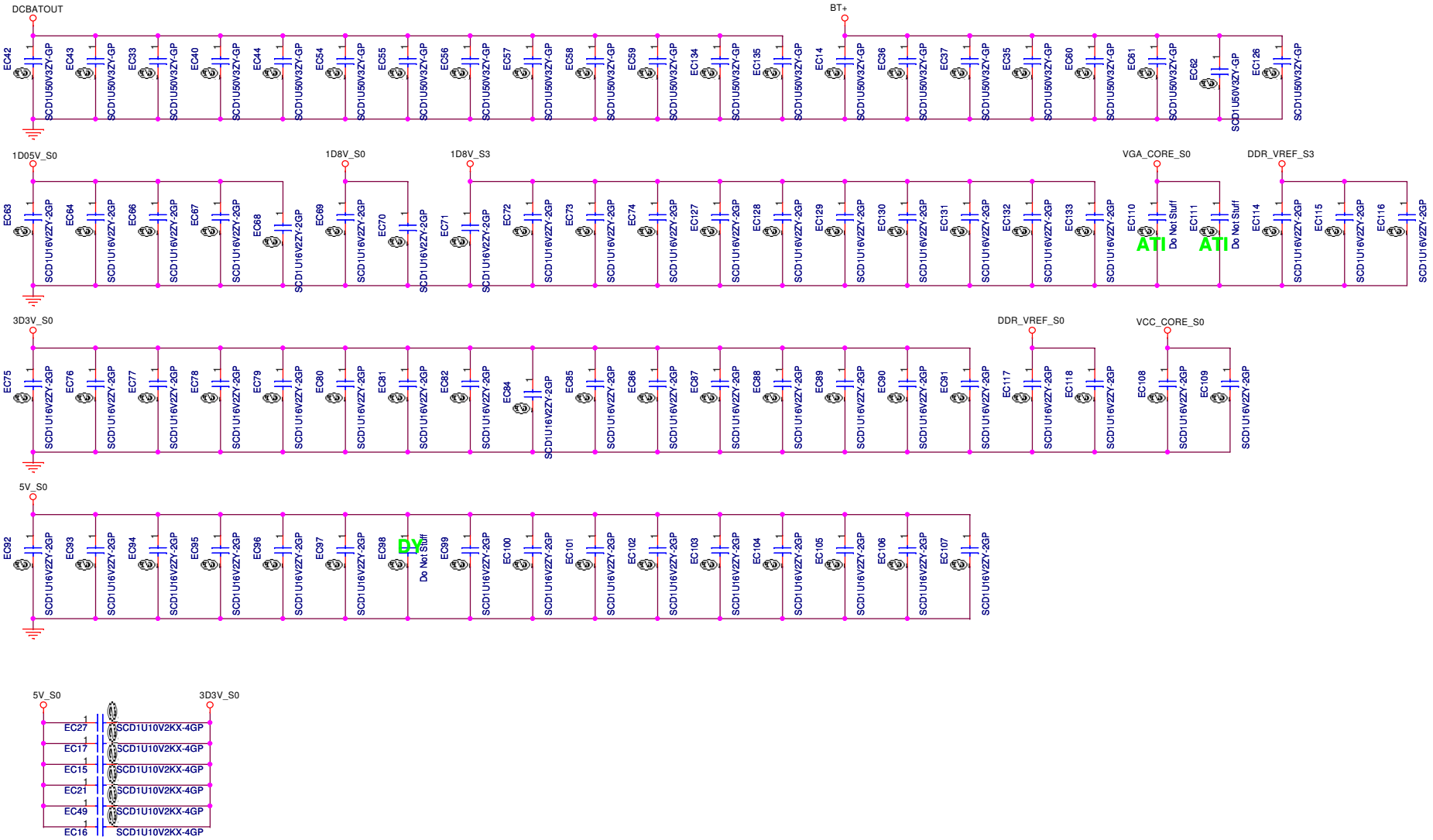

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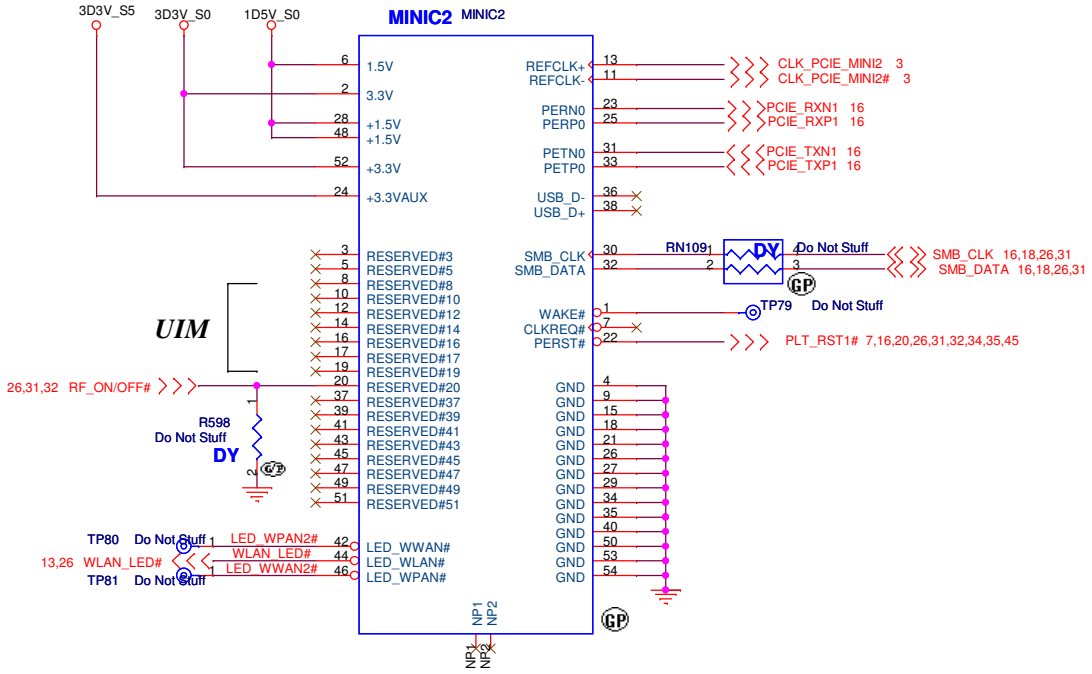
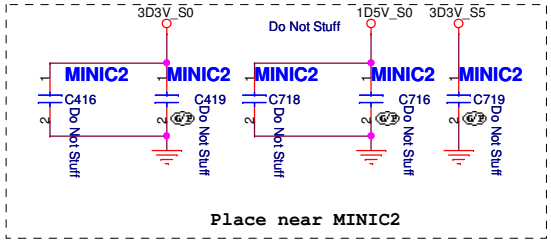
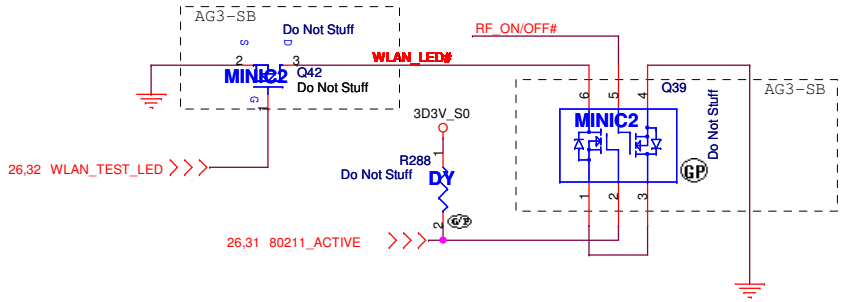
Mini Card Connector







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