

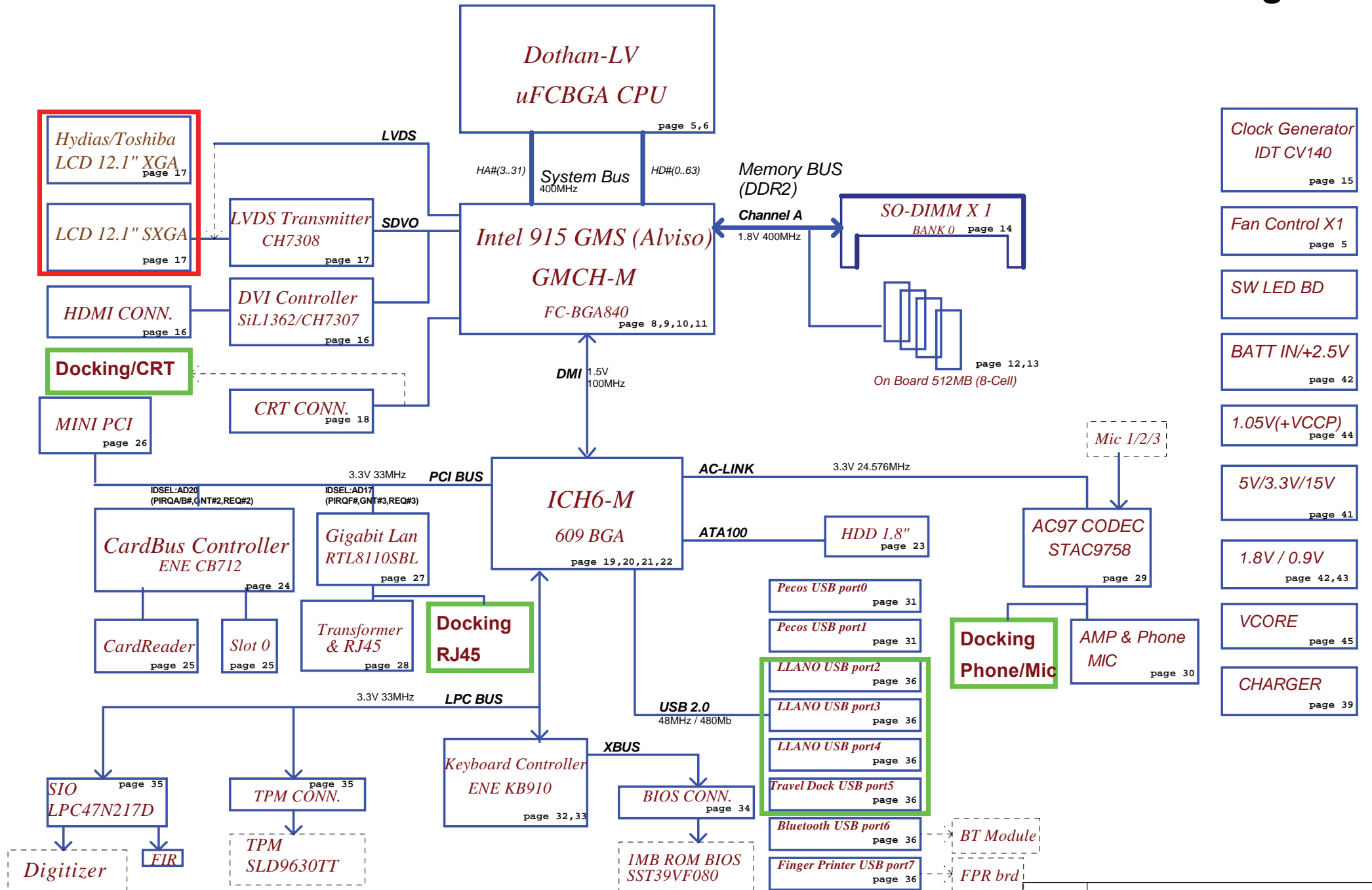
MODEL NAME : EDX20
PCB NO : LA-2481
PVT

COMPAL CONFIDENTIAL

EDX20 Schematics Document
2005-02-22
REV: 0.5

Compal Electronics, Inc.		
Title		
COVER SHEET		
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Block Diagram		
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External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
Mini-PCI	AD18	1	G, H
CARD BUS	AD20	2	A B
LAN	AD17	3	F

ICH6M SM Bus Address

DEVICE	Address
Clock Generator	1101 001Xb
DDR2 On Board	1010 000Xb
DDR2 DIMM1	1010 001Xb
TPM	

EC SM Bus1 Address

DEVICE	Address
Smart Battery 1	0001 011Xb
AT24C16AN-10SI-2.7(U24)	1011 XXX R/W#b

EC SM Bus2 Address

DEVICE	Address
Smart Battery 2	0001 011Xb
ALS TSL2550T	
ADM1032	1001 100Xb
TC74A1-5.0VCT(U34)	1001 001Xb
TC74A2-5.0VCT(U43)	1001 010Xb

Signal \ State	+12VALW +5VALW +3VALW	+1.8V	+5VS +3VS +1.8VS +2.5VS +1.5VS +0.9VS +VCCP +CPU_CORE
	S0	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

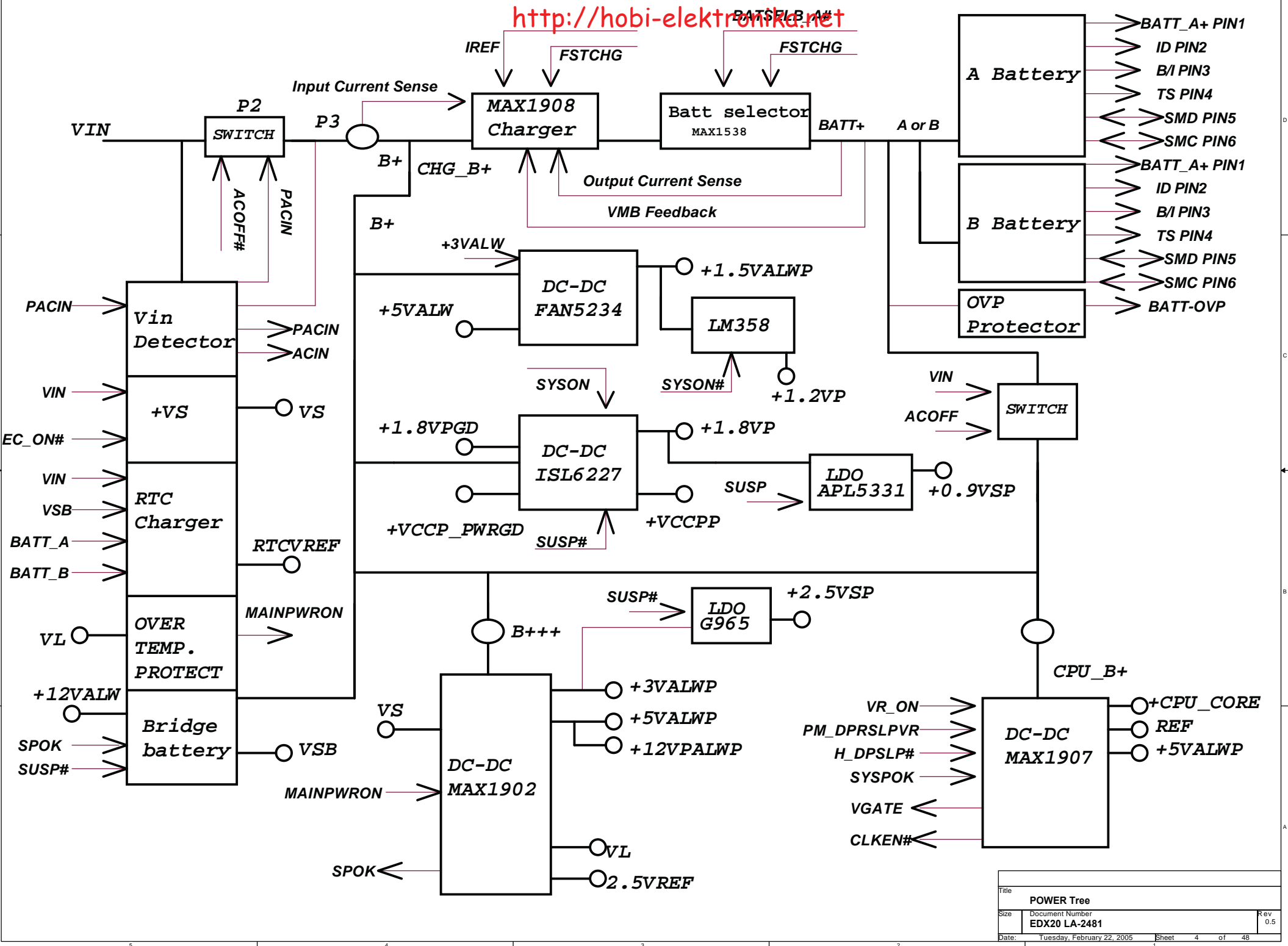
USB PORT TABLE

PORT	FUNCTION
PORT 0	PECOS PORT 0
PORT 1	PECOS PORT 1
PORT 2	LLANO PORT 2
PORT 3	LLANO PORT 0
PORT 4	LLANO PORT 1
PORT 5	TRAVEL DOCKING
PORT 6	BLUETOOTH
PORT 7	FINGERPRINTER

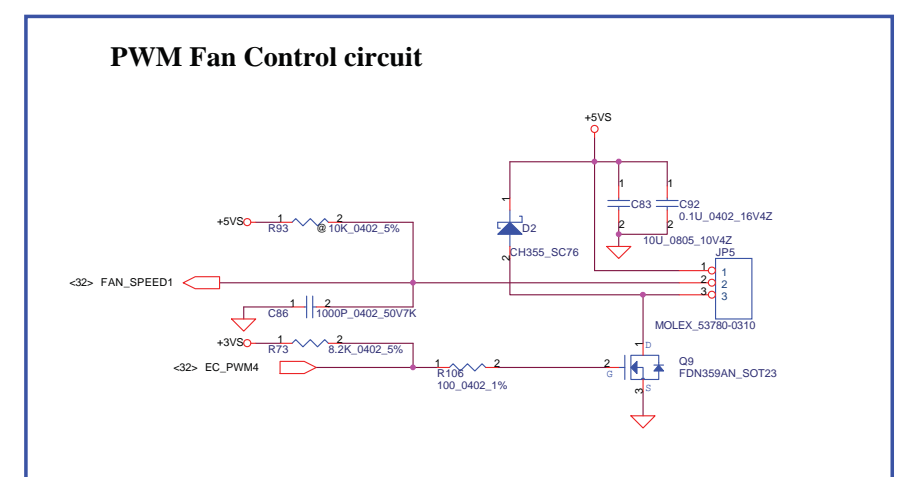
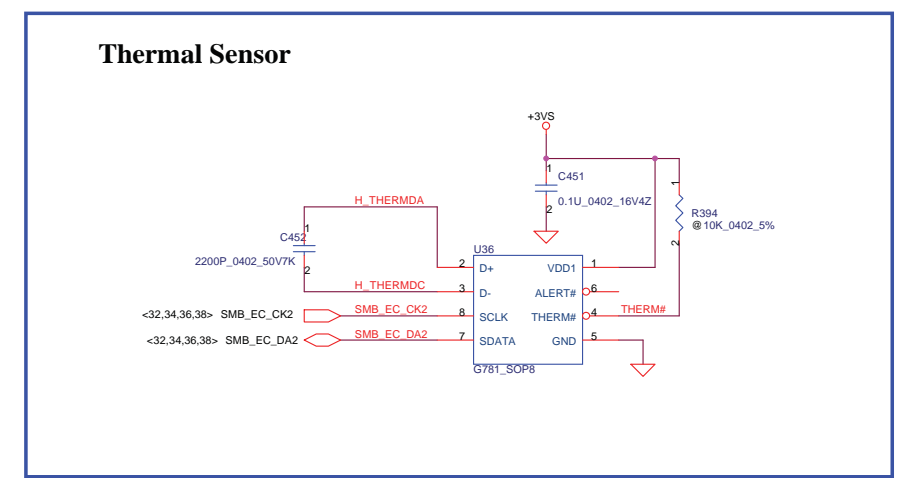
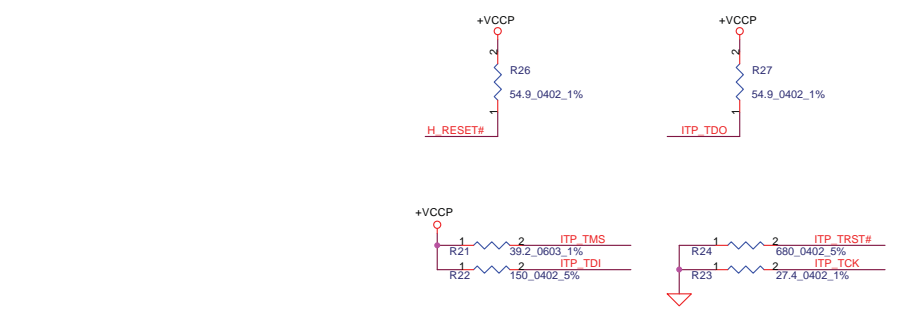
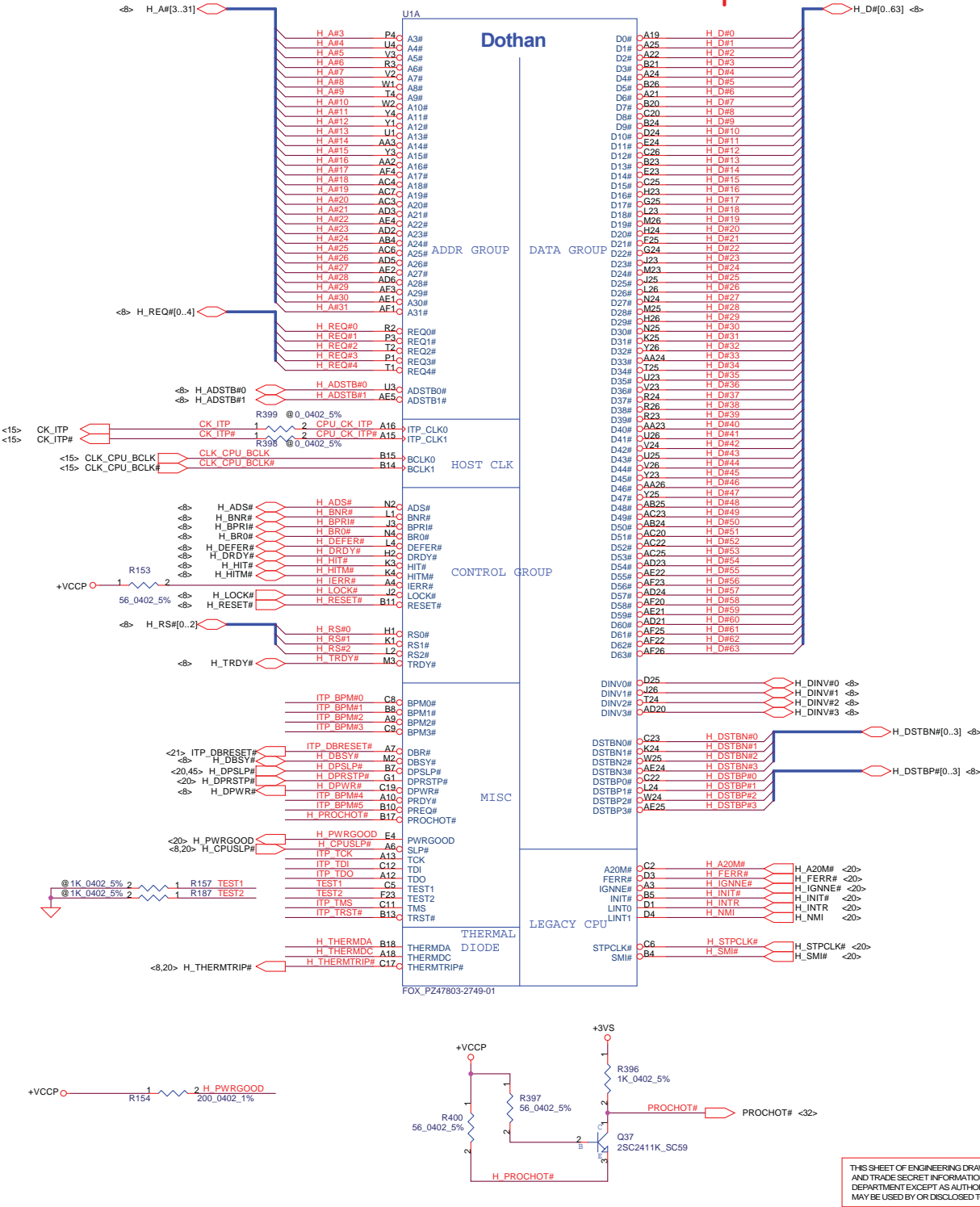
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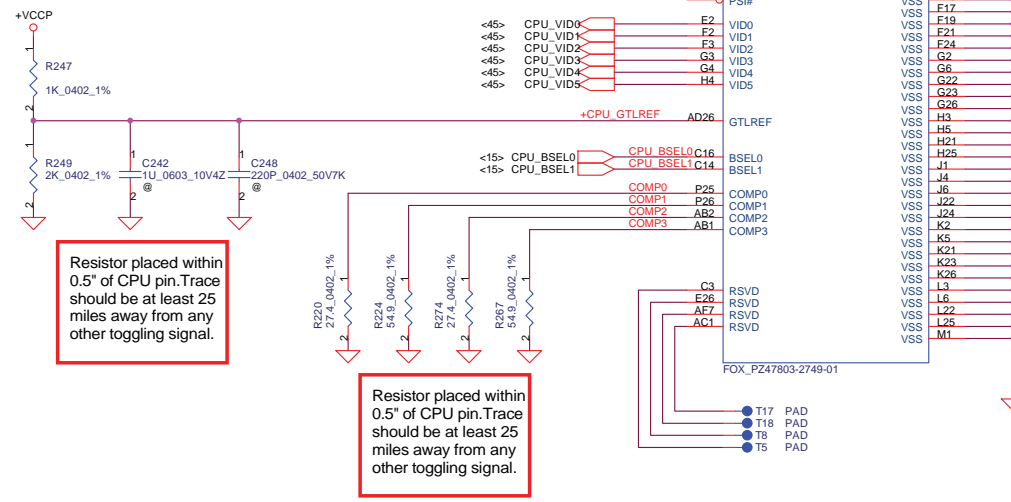
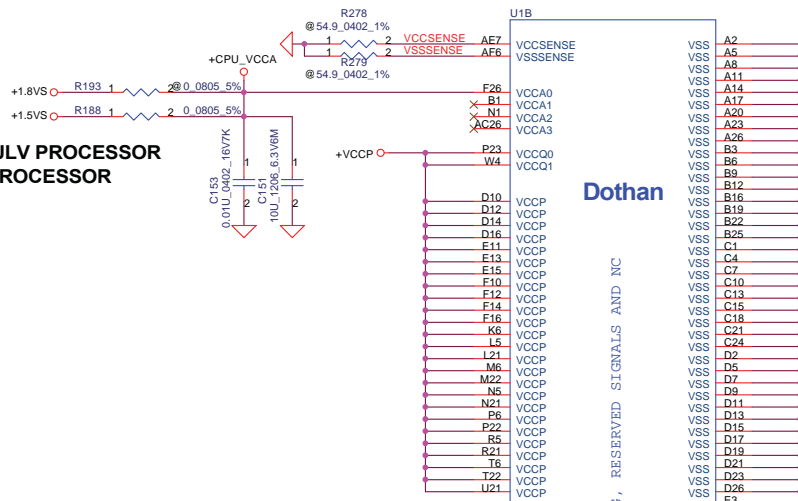
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+1.8VS FOR NON-LV/ULV PROCESSOR
+1.5VS FOR LV/ULV PROCESSOR

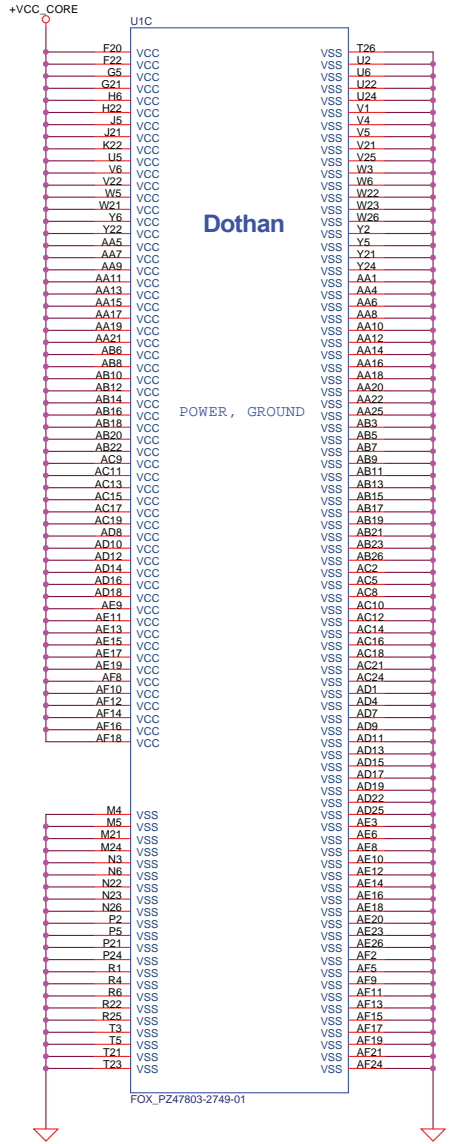


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.

Dothan

POWER, GROUND, RESERVED SIGNALS AND NC

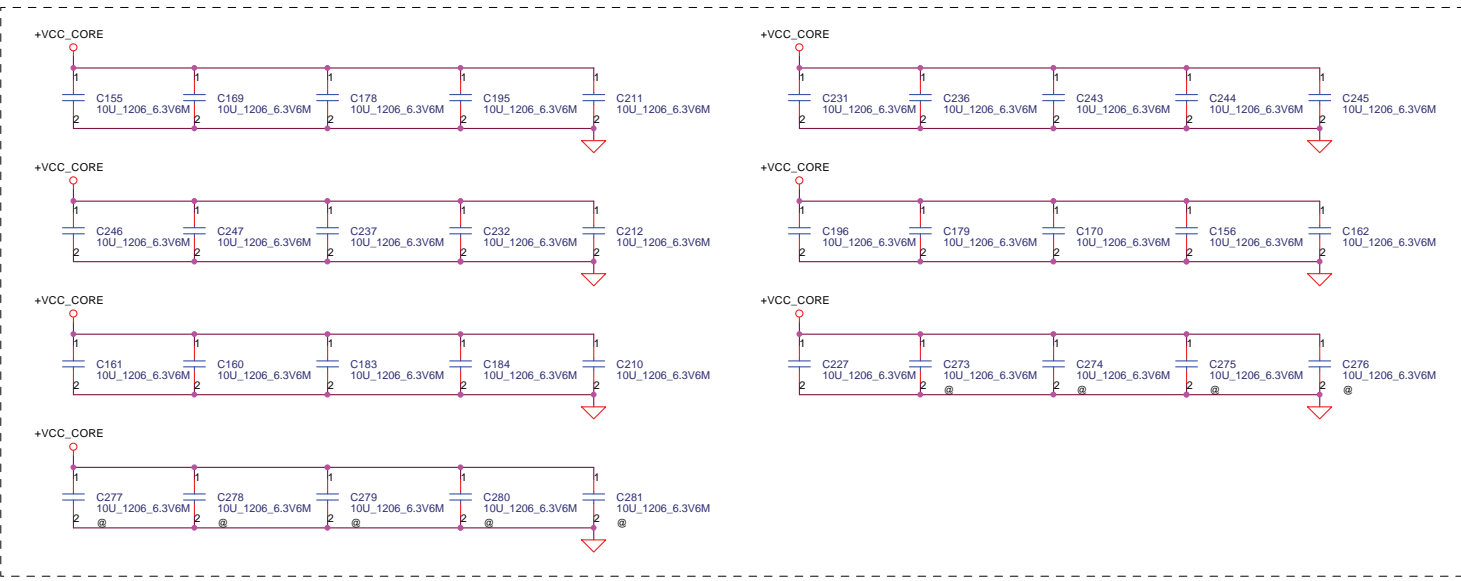


Dothan

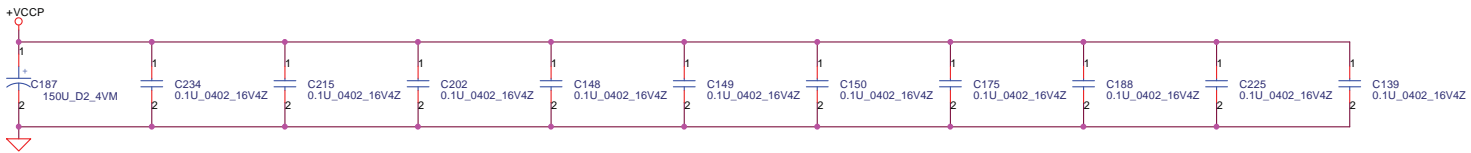
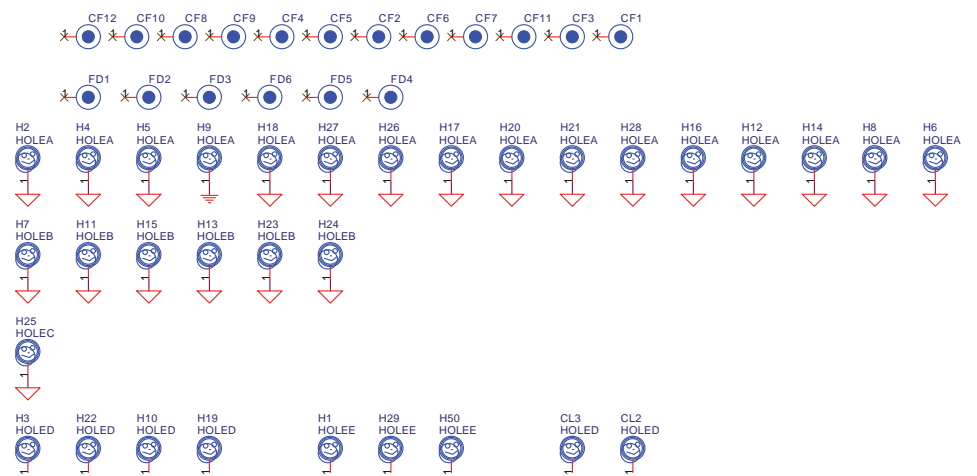
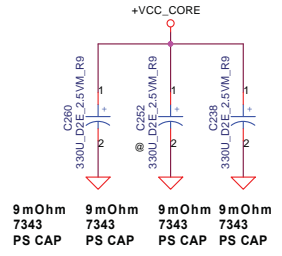
POWER, GROUND

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Dothan Processor in mFCPGA479			
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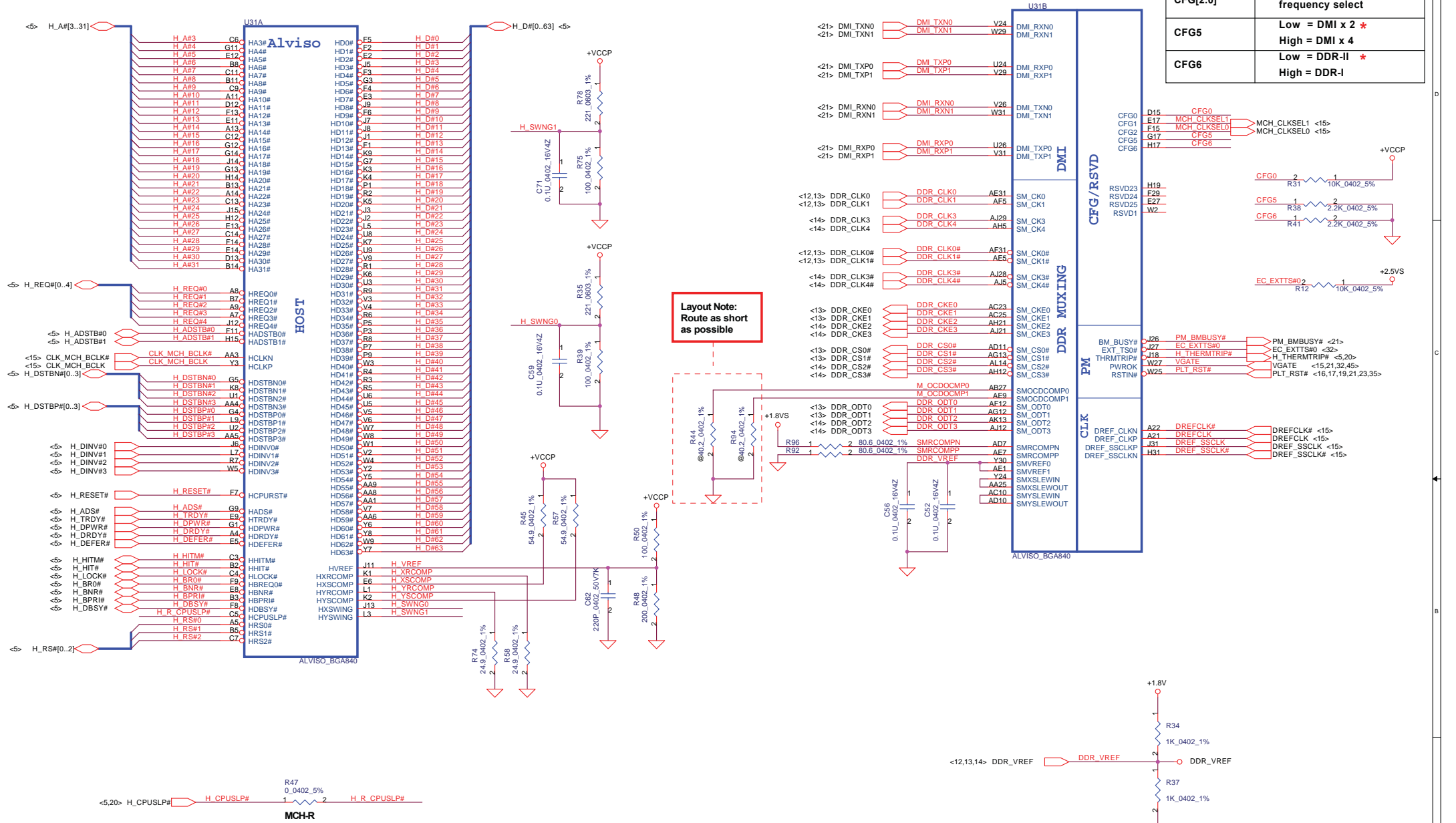


Near VCORE regulator.



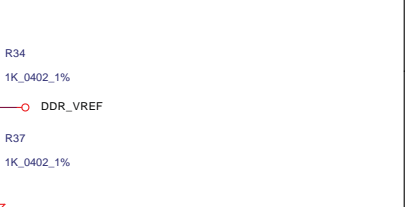
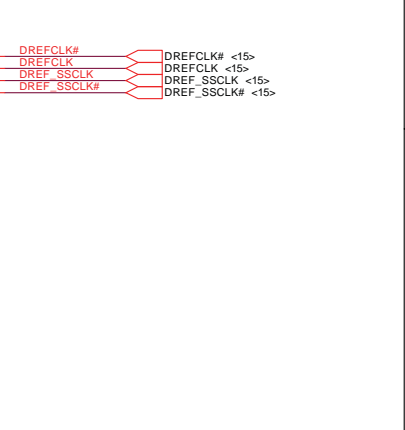
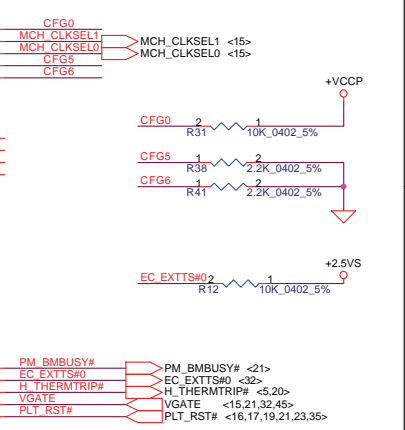
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CPU Bypass		
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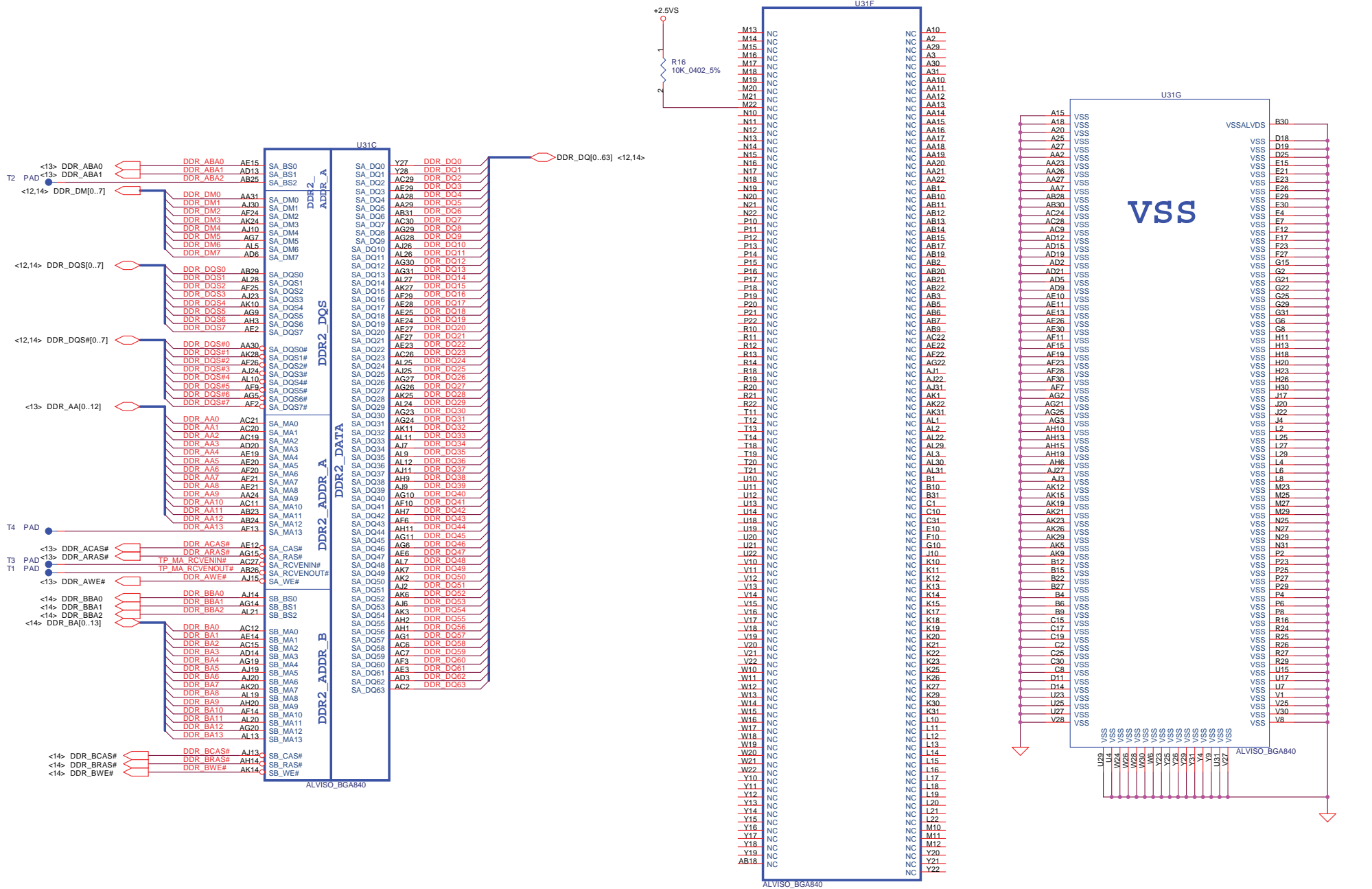


Note:
Not install MCH-R for Dothan-A,
Install MCH-R for Dothan-B"

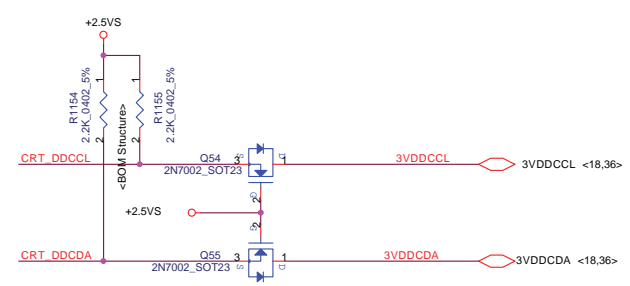
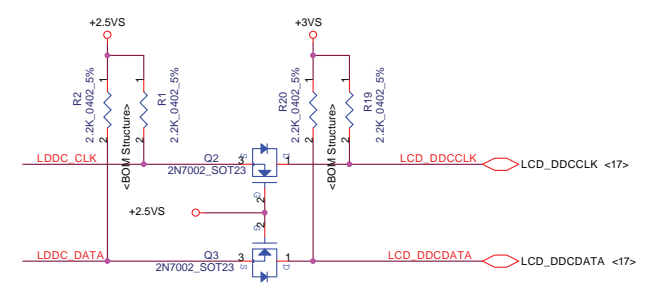
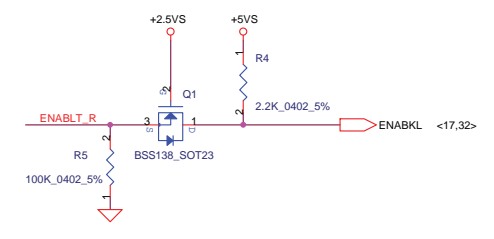
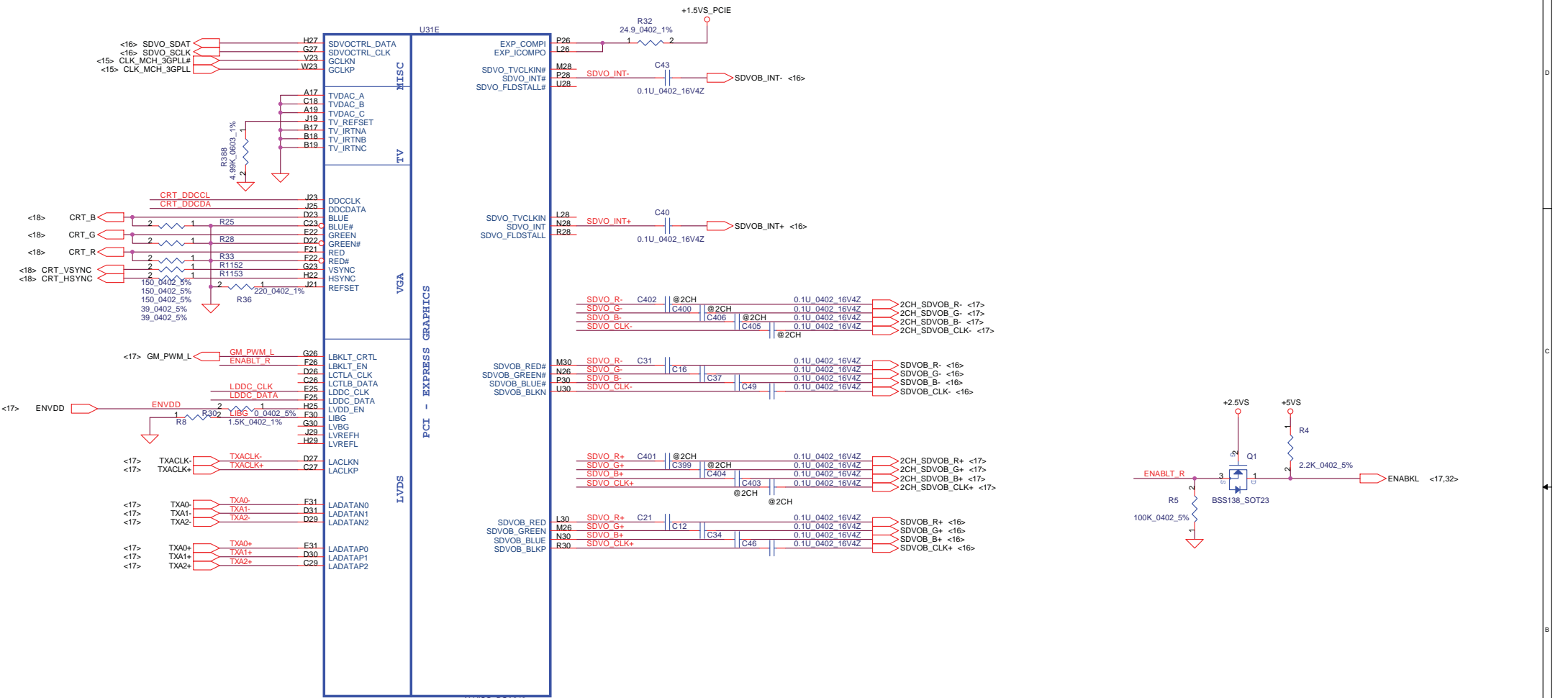
CFG2[0]	Refer to page15 for FSB frequency select
CFG5	Low = DMI x 2 * High = DMI x 4
CFG6	Low = DDR-I * High = DDR-I

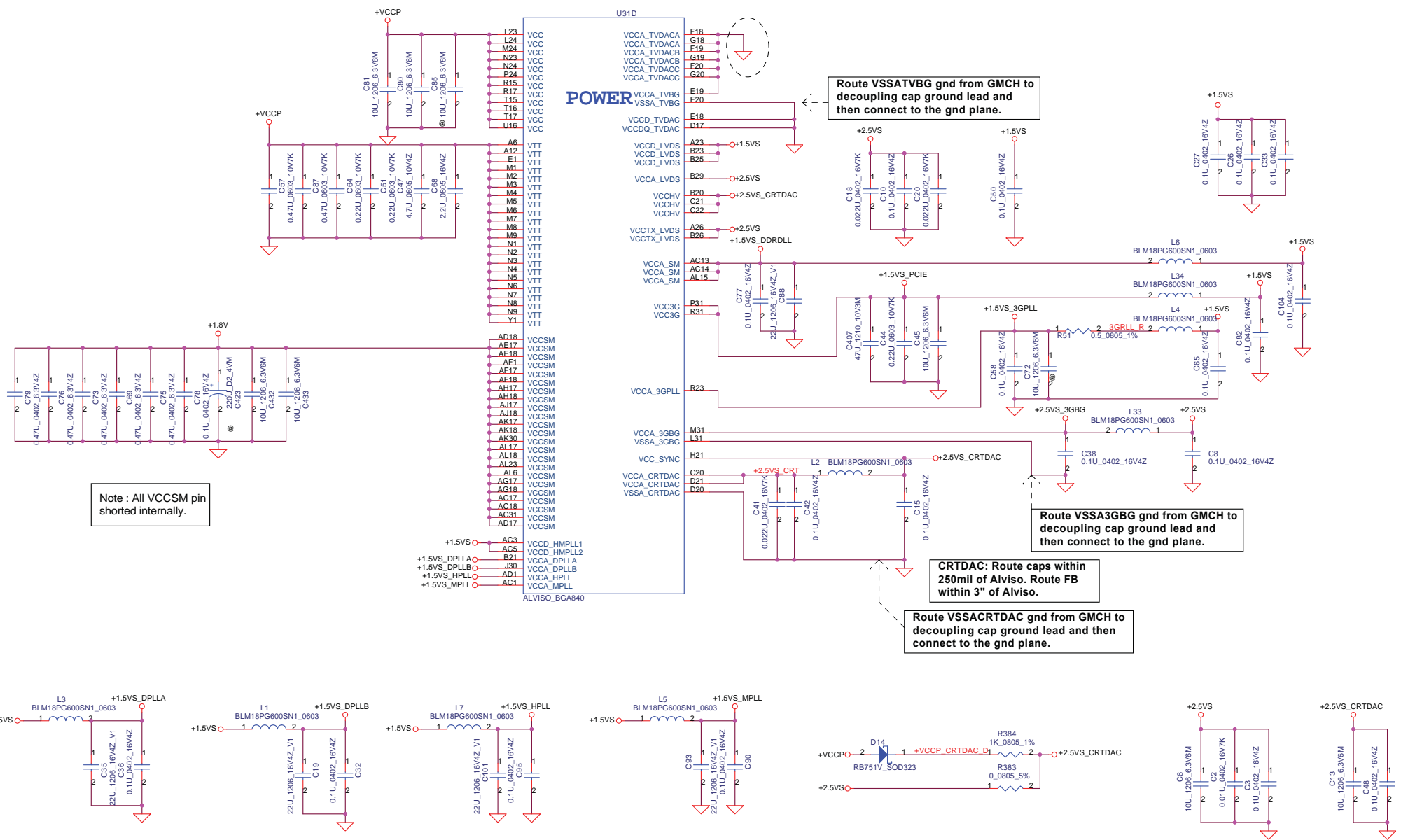


Sonoma_Platform_MOW_04WW25



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Note : All VCCSM pin shorted internally.

Route VSSATVBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Route VSSA3BGB gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

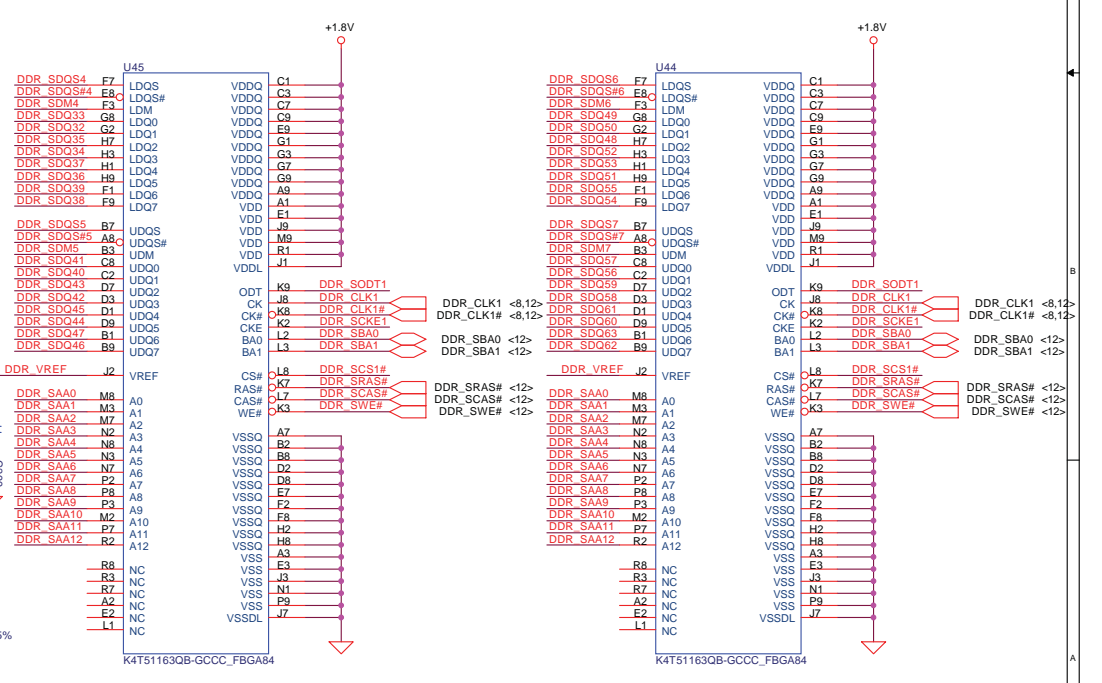
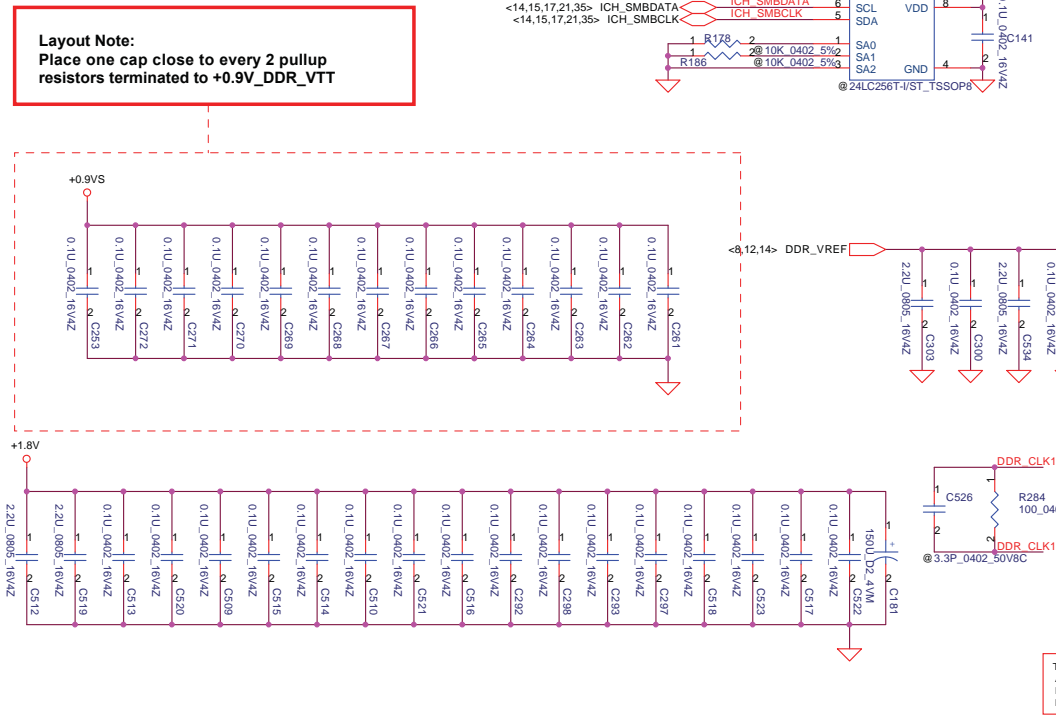
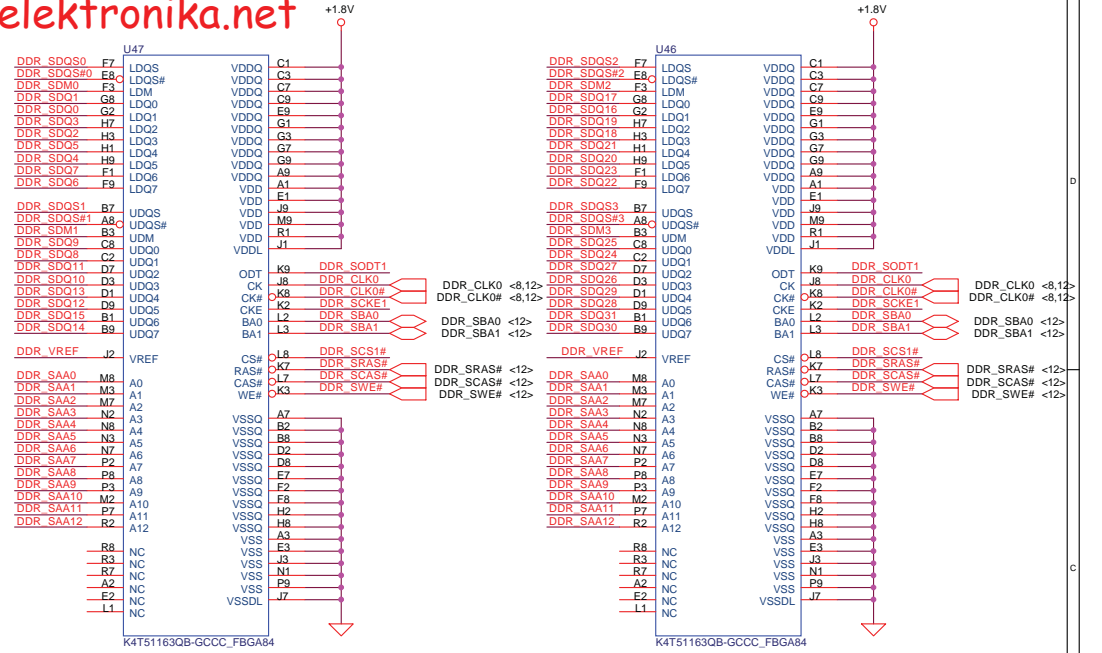
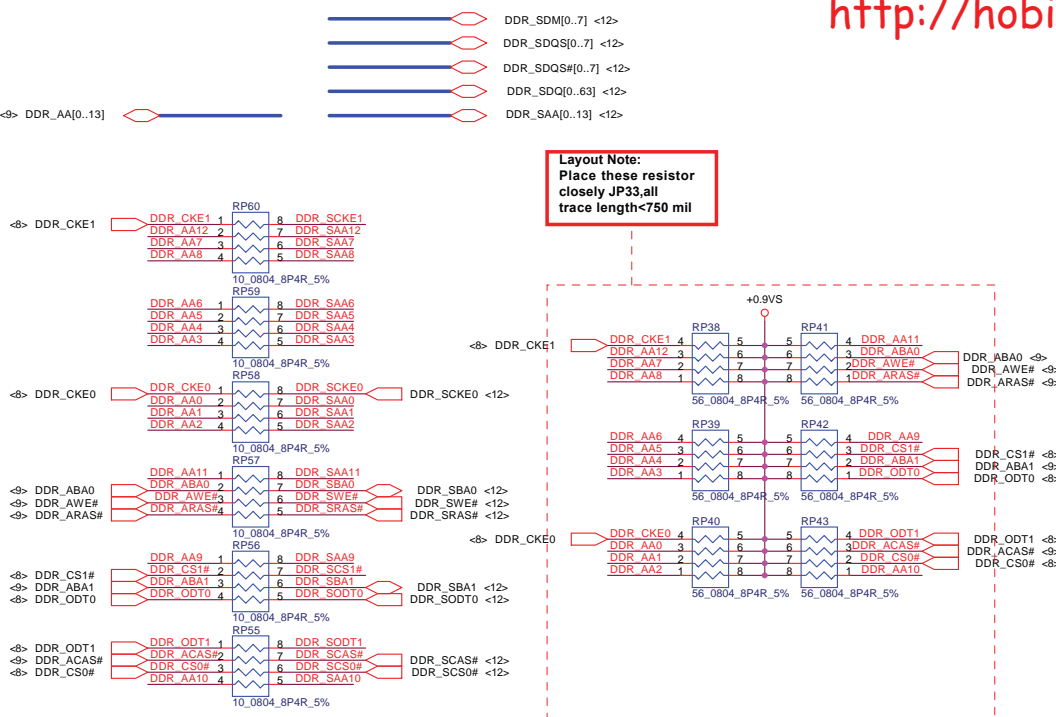
Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Route VSSA3BGB gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

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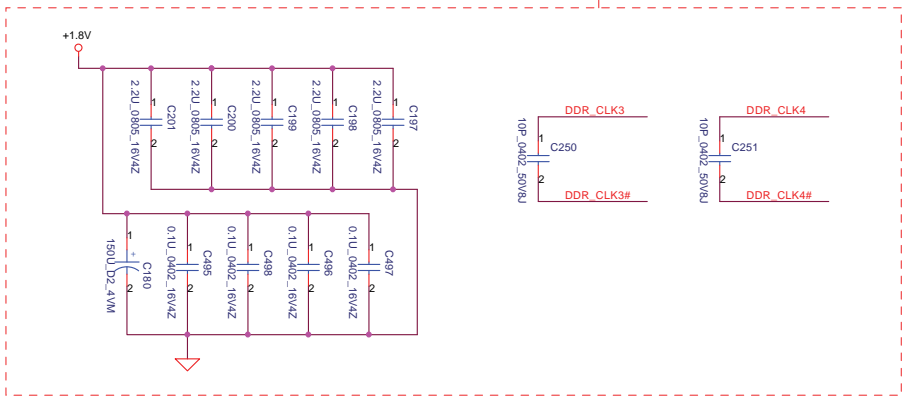
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Alviso (4 of 4)		
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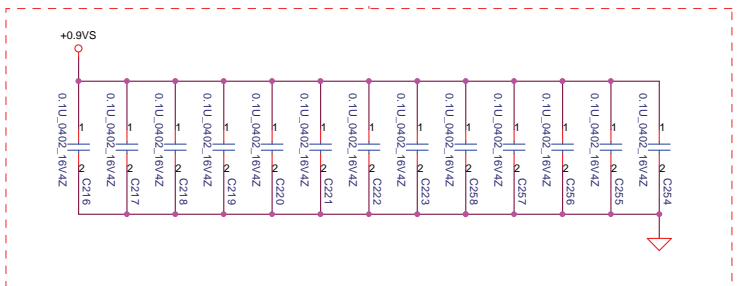
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- <9,12> DDR_DQS#[0..7]
- <9,12> DDR_DQ[0..63]
- <9,12> DDR_DM[0..7]
- <9,12> DDR_DQS#[0..7]
- <9,12> DDR_BA[0..13]

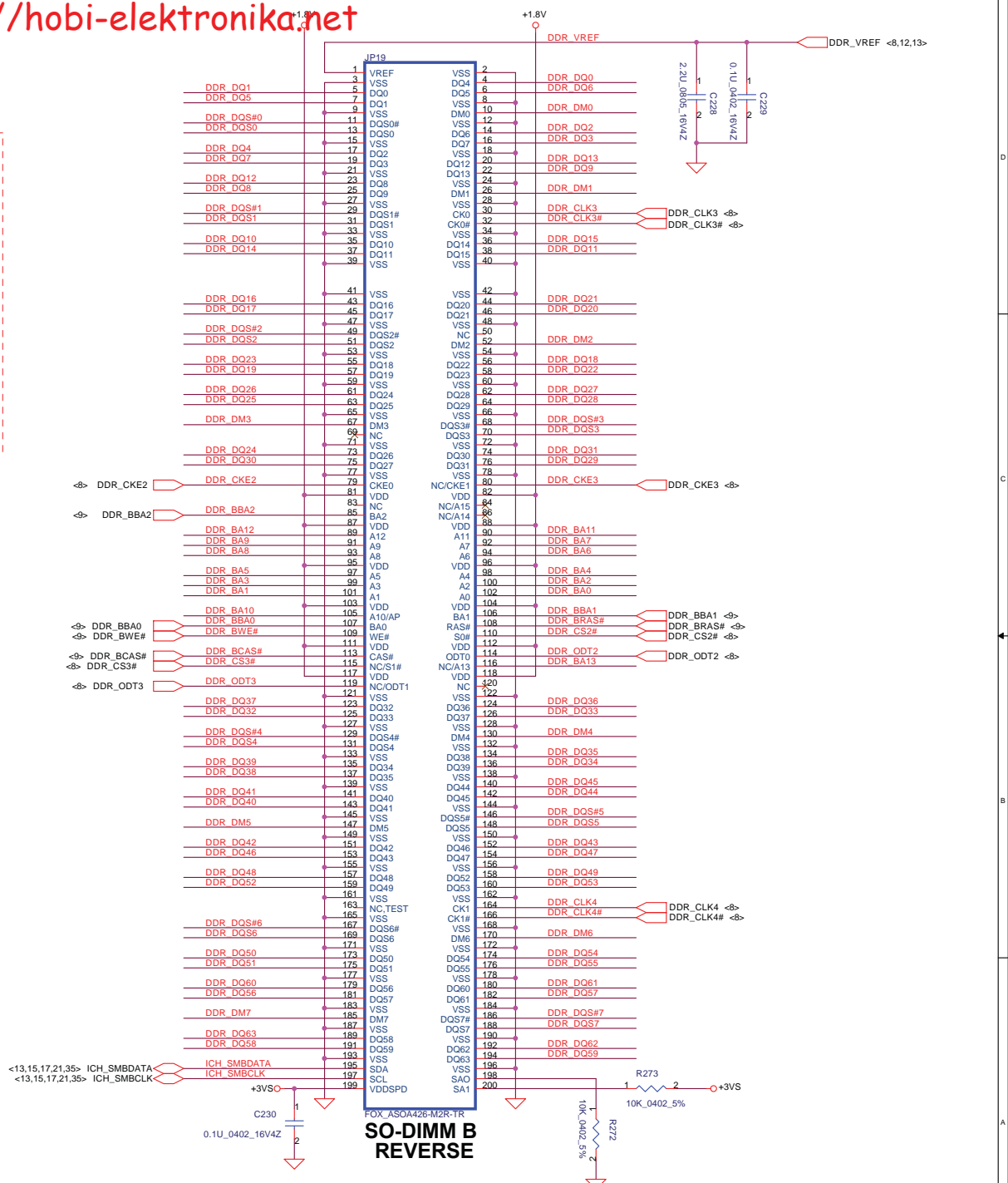
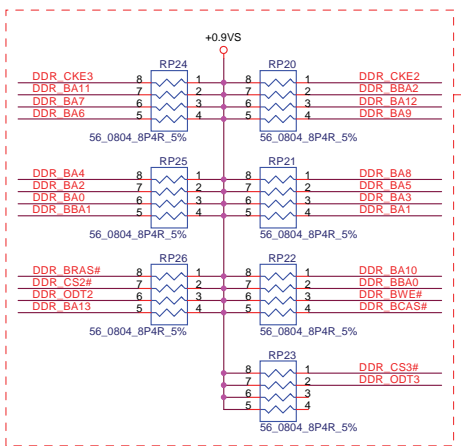
Layout Note:
Place near JP33



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely JP33, all trace length <750 mil



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DDR1-SODIMM SLOT2

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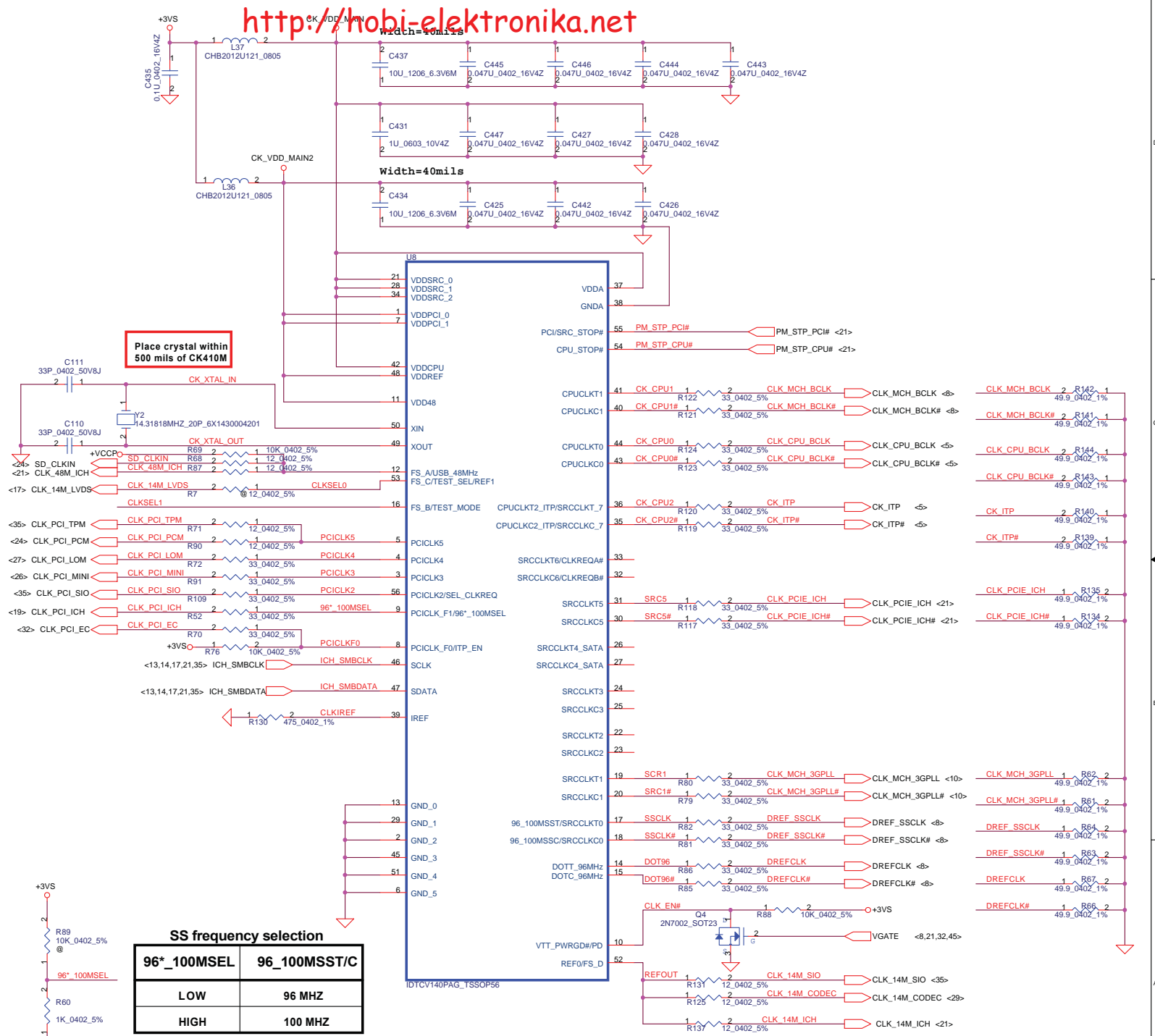
Dothan A step

FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
1	0	1	133	100	33.3
0	0	1	100	100	33.3

Dothan B step

FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
0	0	1	133	100	33.3
1	0	1	100	100	33.3

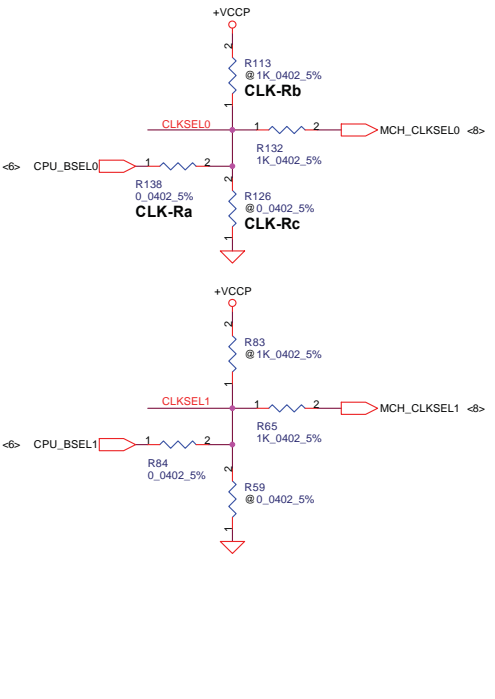
CPU Type	CLK-Ra	CLK-Rb	CLK-Rc
Dothan-A PSB400	OPEN	OPEN	0 Ohm
Dothan-A PSB533	OPEN	1K Ohm	OPEN
Dothan-B	0 Ohm	OPEN	OPEN



Place crystal within 500 mils of CK410M

SS frequency selection

96*_100MSEL	96_100MSST/C
LOW	96 MHZ
HIGH	100 MHZ



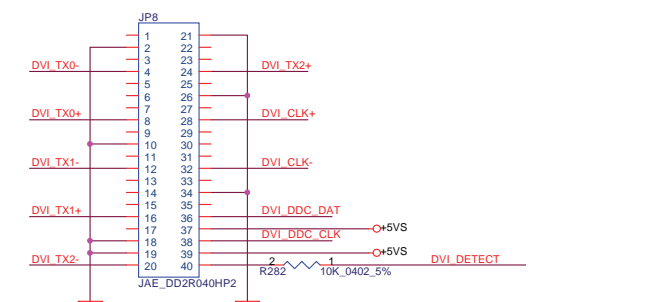
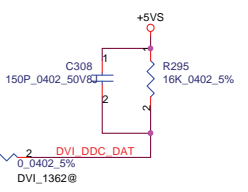
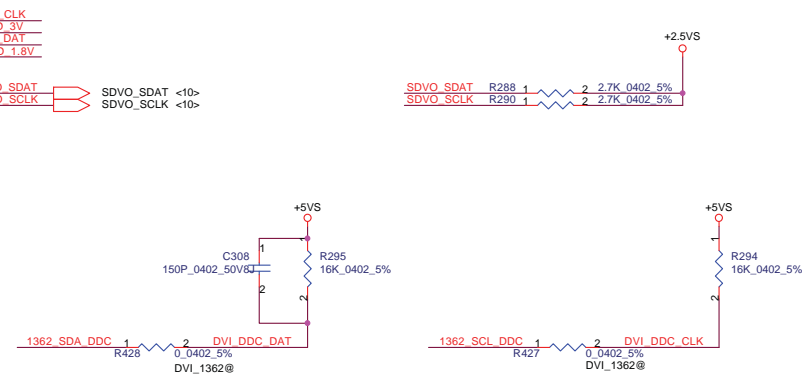
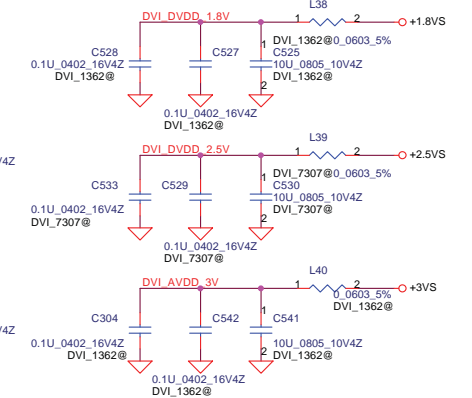
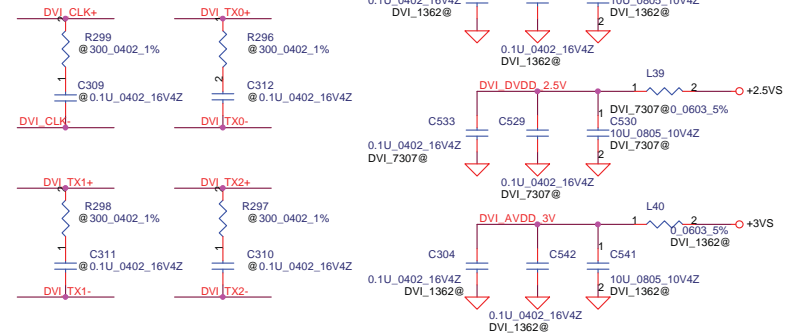
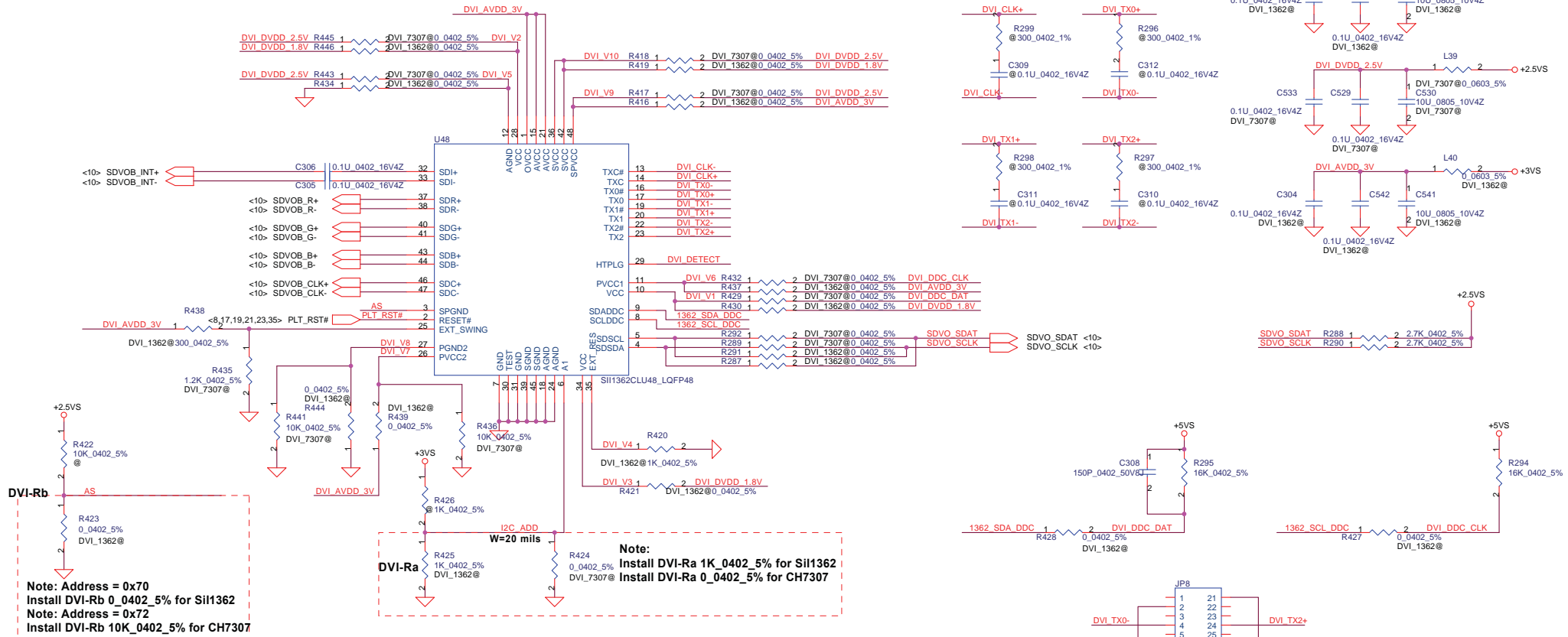
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Clock Generator

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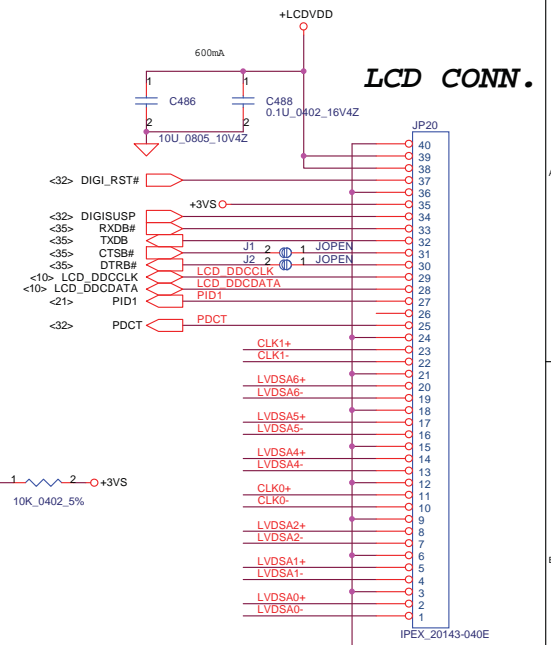
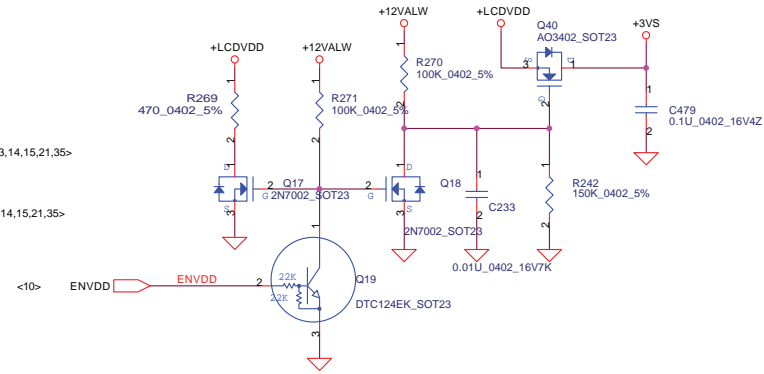
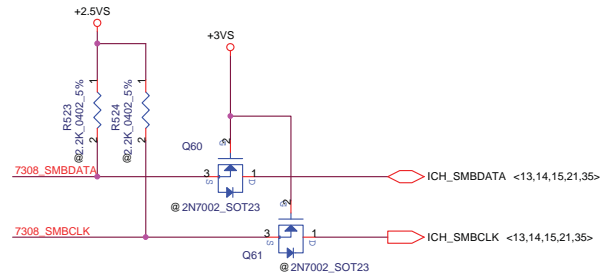
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DVI CONTROLLER

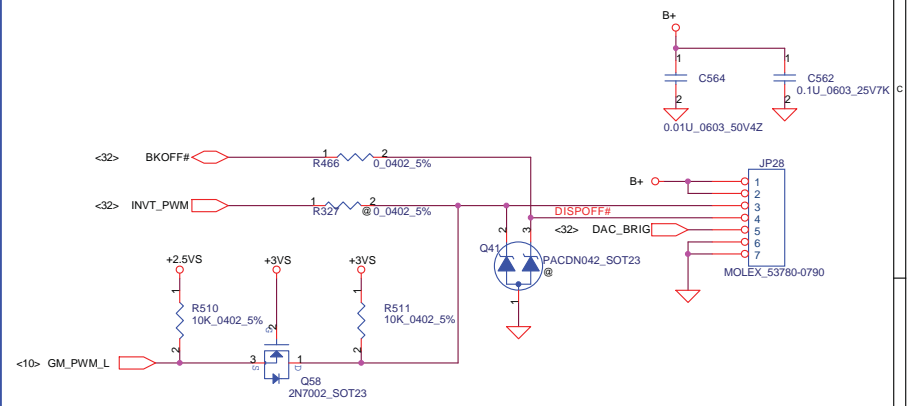
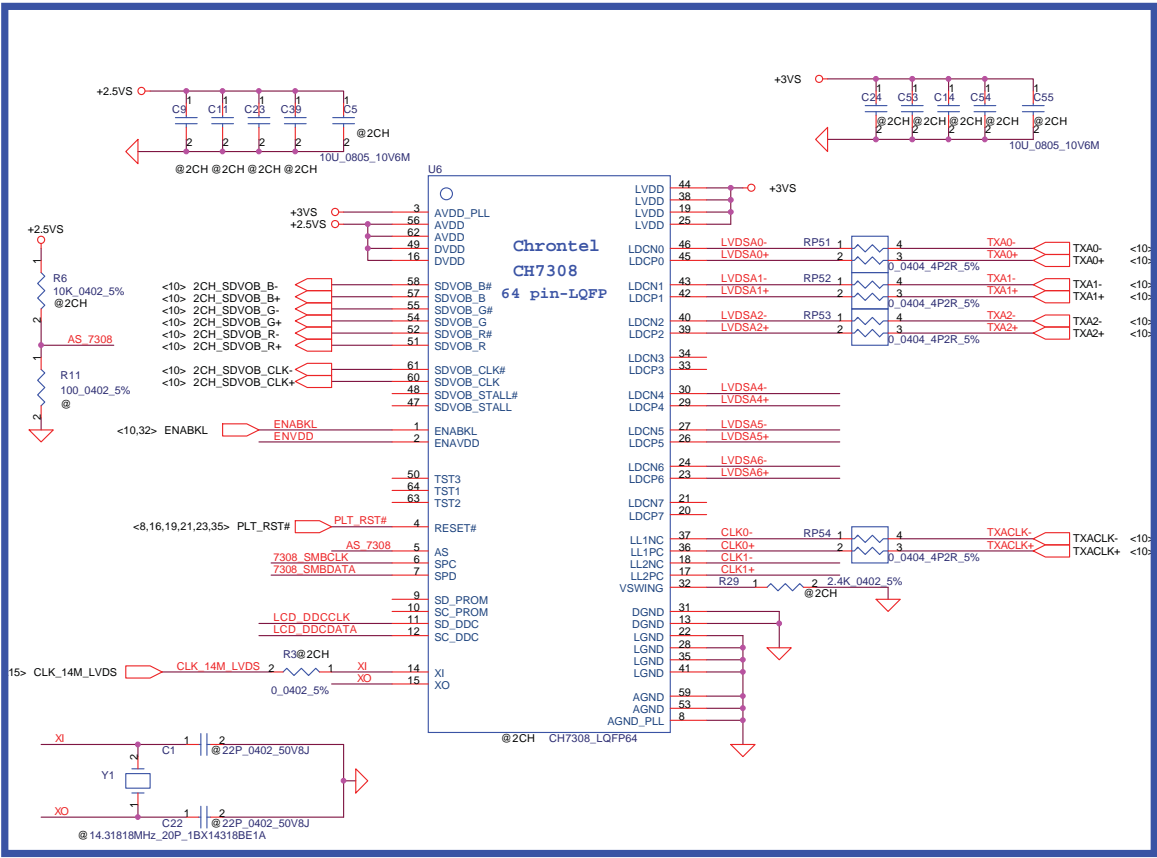


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Si1362/CH7307			
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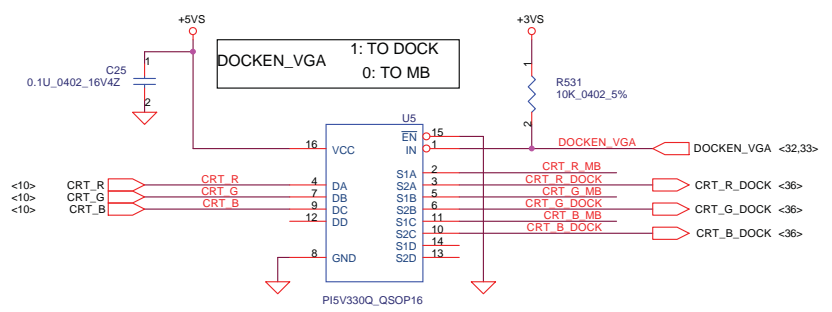
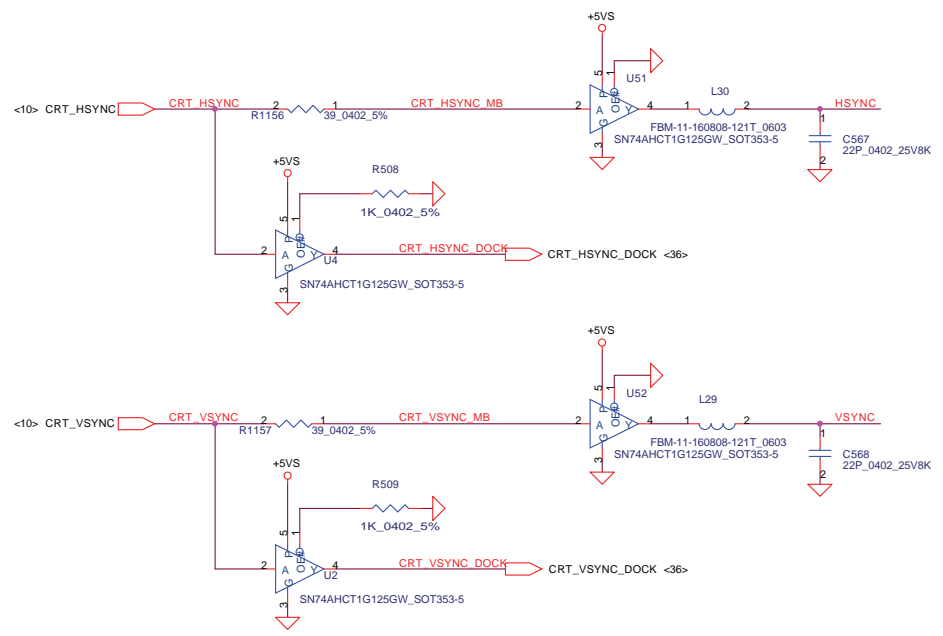
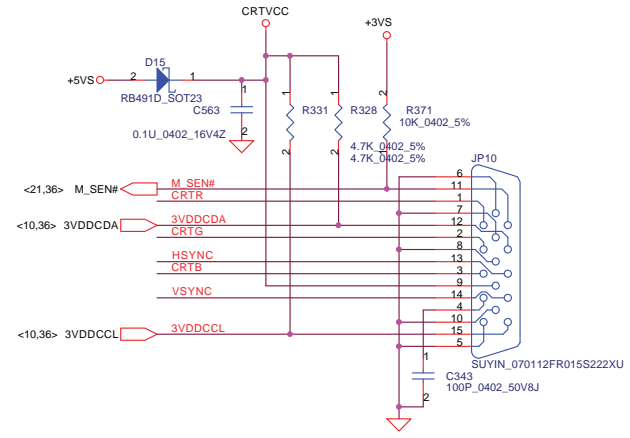
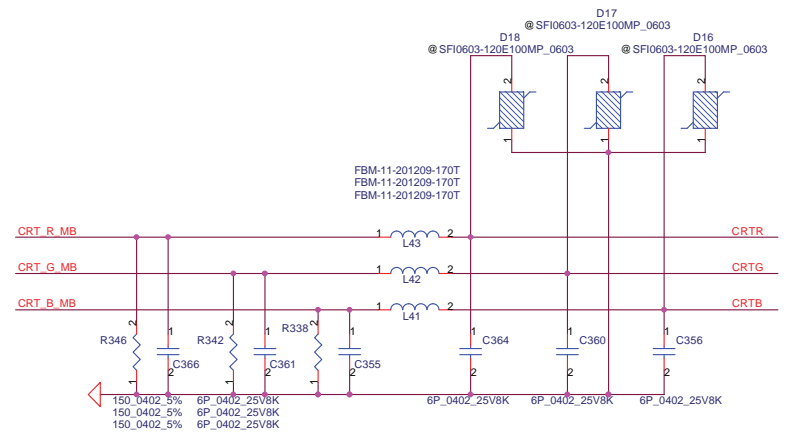


@2CH



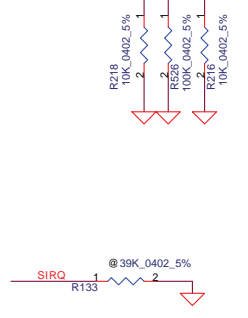
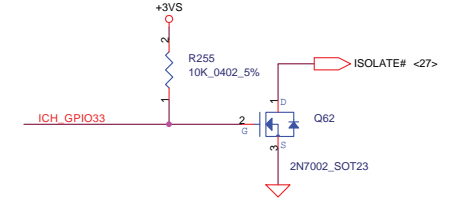
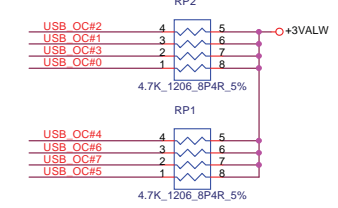
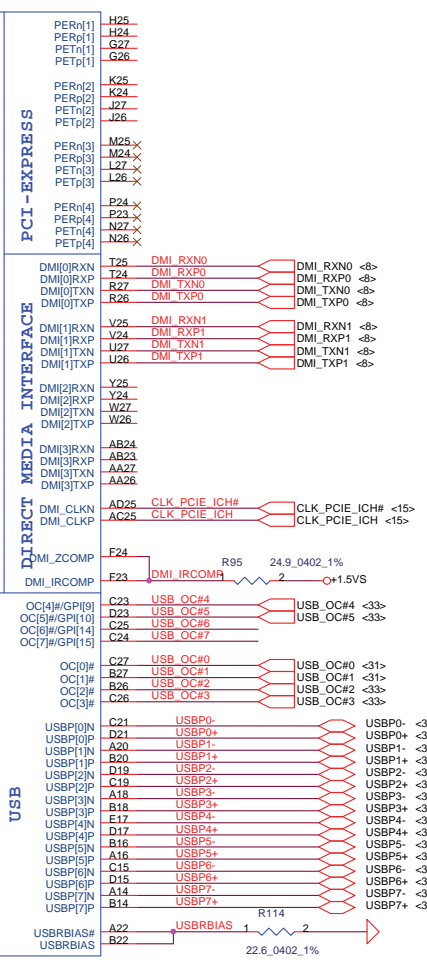
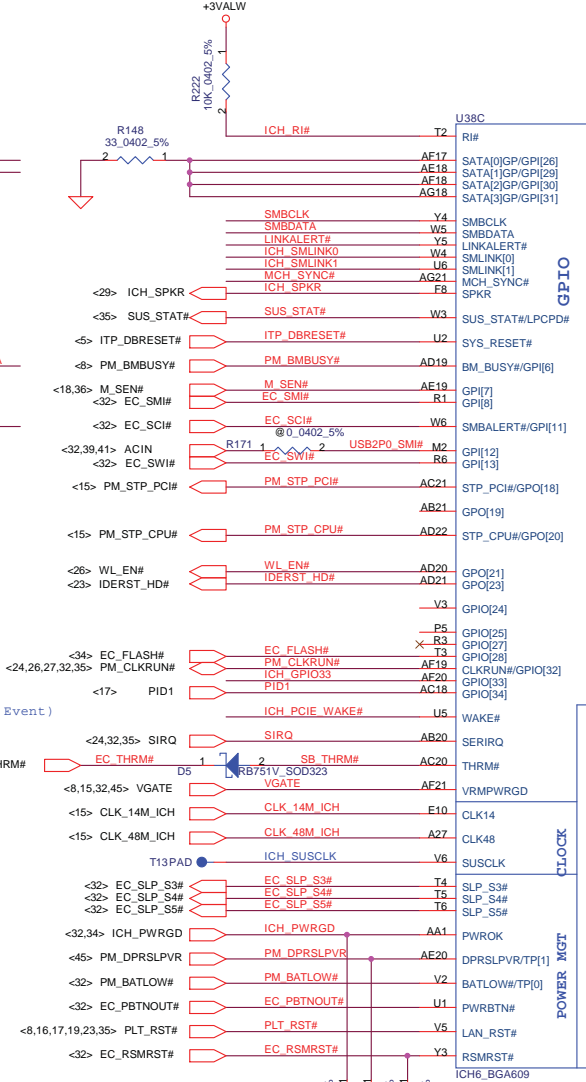
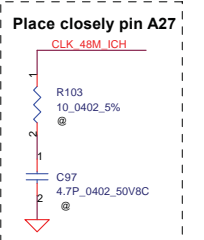
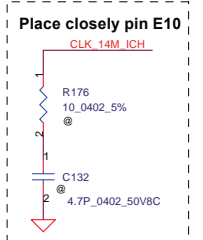
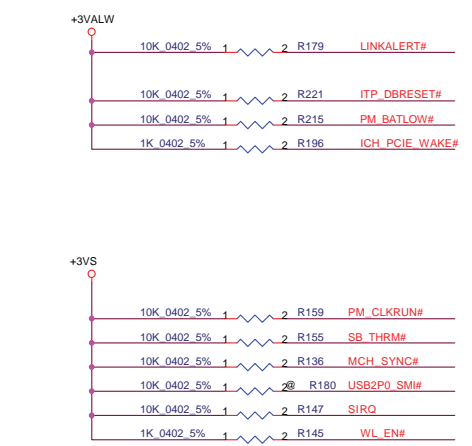
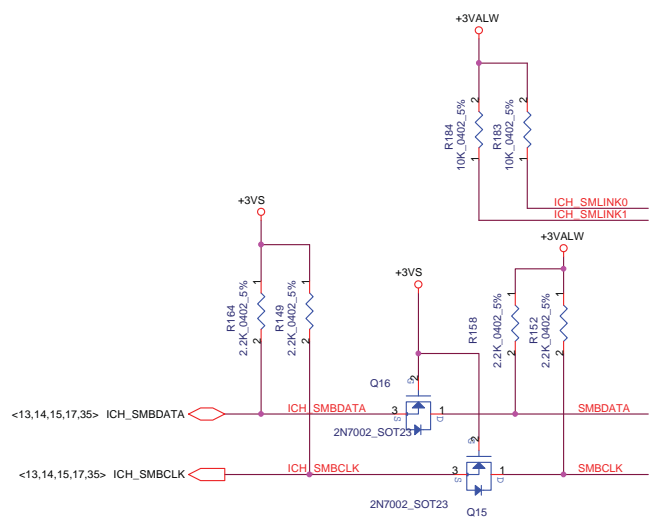
Compal Electronics, Inc.		
Title	LCD Conn&Inverter	
Size	Document Number	Rev
	EDX20 LA-2481	0.5
Date:	Tuesday, February 22, 2005	Sheet 17 of 48

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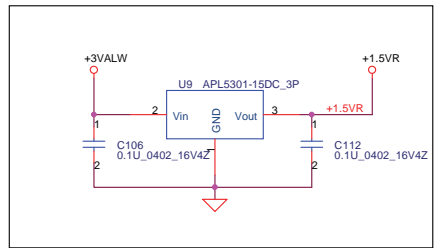
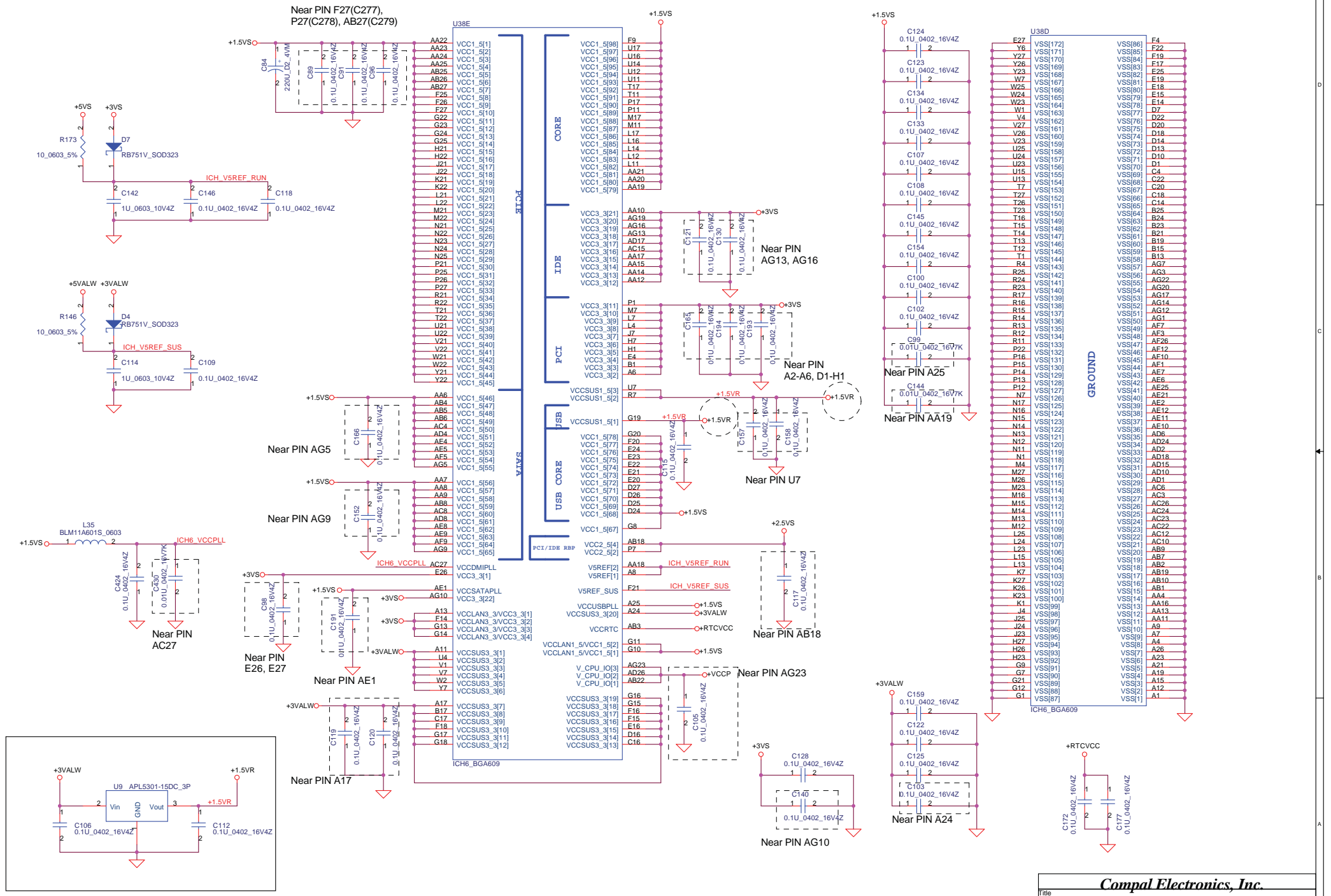


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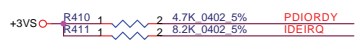
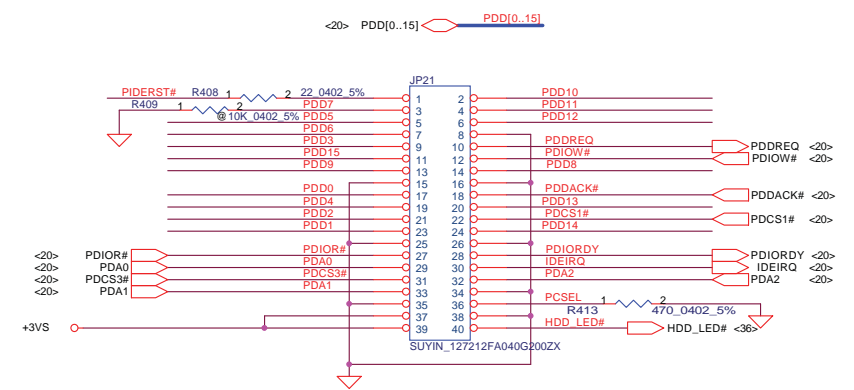
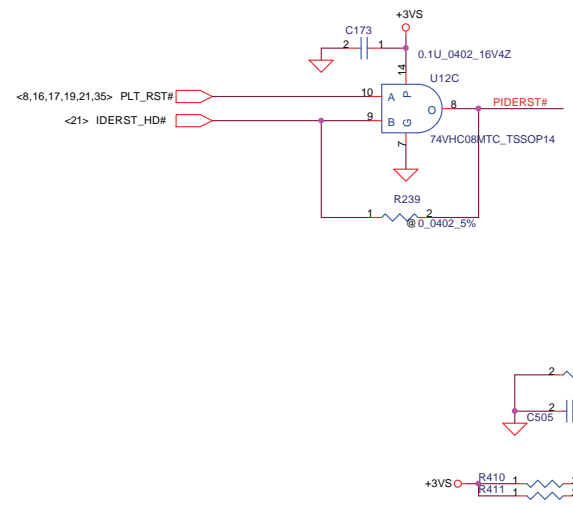
Compal Electronics, Inc.		
Title		
LCD Connector & CRT		
Size	Document Number	Rev
	EDX20 LA-2481	0.5
Date:	Tuesday, February 22, 2005	Sheet 18 of 48



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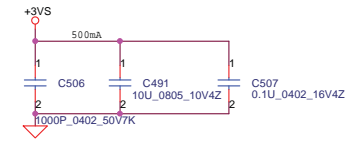


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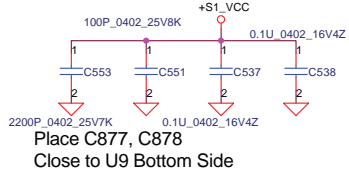
Place caps. near HDD CONN.

Layout Note: +VPHDD trace width 60 mil

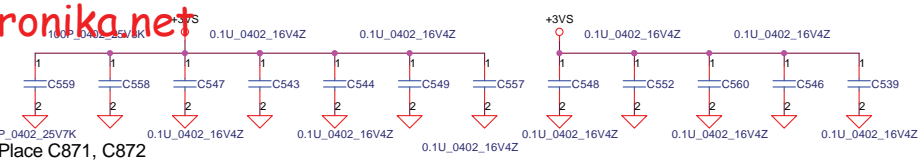


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Compal Electronics, Inc.		
Title ICH4-M PIDE&ICH Pull-up		
Size	Document Number	Rev
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Date:	Tuesday, February 22, 2005	Sheet 23 of 48



Place C877, C878
Close to U9 Bottom Side



Place C871, C872
Close to C694

<19.26.27> PCI_AD[0..31]

- PCI_AD31 C2
- PCI_AD30 C1
- PCI_AD29 D4
- PCI_AD28 D2
- PCI_AD27 D1
- PCI_AD26 E4
- PCI_AD25 E3
- PCI_AD24 E2
- PCI_AD23 F1
- PCI_AD22 F2
- PCI_AD21 G2
- PCI_AD20 G3
- PCI_AD19 H3
- PCI_AD18 H4
- PCI_AD17 J1
- PCI_AD16 J2
- PCI_AD15 N2
- PCI_AD14 M3
- PCI_AD13 N3
- PCI_AD12 K4
- PCI_AD11 M4
- PCI_AD10 K5
- PCI_AD9 L5
- PCI_AD8 M5
- PCI_AD7 K6
- PCI_AD6 M6
- PCI_AD5 N6
- PCI_AD4 M7
- PCI_AD3 N7
- PCI_AD2 L7
- PCI_AD1 K7
- PCI_AD0 N8

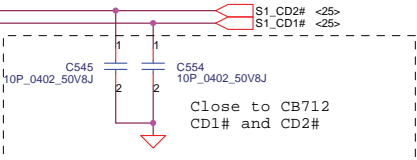
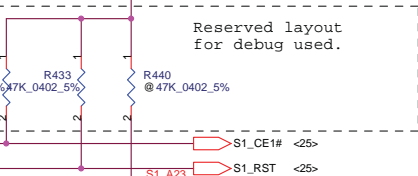
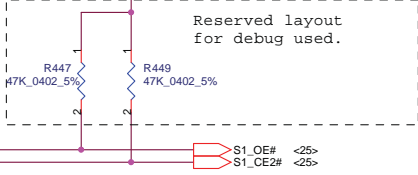
- AD31
- AD30
- AD29
- AD28
- AD27
- AD26
- AD25
- AD24
- AD23
- AD22
- AD21
- AD19
- AD18
- AD17
- AD16
- AD15
- AD14
- AD13
- AD12
- AD11
- AD10
- AD9
- AD8
- AD7
- AD6
- AD5
- AD4
- AD3
- AD1
- AD0

CARDBUS

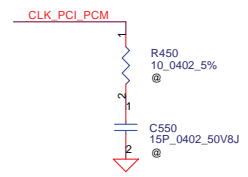
- CAD31/D10 C3
- CAD30/D9 B3
- CAD29/D1 A3
- CAD28/D8 C4
- CAD27/D0 A6
- CAD26/A0 D7
- CAD25/A1 C7
- CAD24/A2 D8
- CAD23/A3 A9
- CAD22/A4 C9
- CAD21/A5 A10
- CAD20/A6 B10
- CAD19/A25 D10
- CAD18/A7 B10
- CAD17/A24 E12
- CAD16/A17 D10
- CAD15/IOWR# F10
- CAD14/A9 E13
- CAD13/IORD# F11
- CAD12/A11 G10
- CAD11/E# G12
- CAD10/CE2# H12
- CAD9/A10 H10
- CAD8/D15 J11
- CAD7/D7 J11
- CAD6/D13 J12
- CAD5/D6 K13
- CAD4/D12 I10
- CAD3/D5 K10
- CAD2/D11 K12
- CAD1/D4 K12
- CAD0/D3 L13

- S1_D10
- S1_D9
- S1_D1
- S1_D8
- S1_D0
- S1_A0
- S1_A1
- S1_A2
- S1_A3
- S1_A4
- S1_A5
- S1_A6
- S1_A25
- S1_A7
- S1_A24
- S1_A17
- S1_IOWR#
- S1_A4
- S1_IORD#
- S1_A11
- S1_OE#
- S1_CE2#
- S1_D15
- S1_D7
- S1_D13
- S1_D6
- S1_D12
- S1_D5
- S1_D11
- S1_D4
- S1_D3
- S1_REG#
- S1_A12
- S1_A8
- S1_CE1#
- S1_A23
- S1_RST
- S1_A15
- S1_A22
- S1_A21
- S1_A20
- S1_A14
- S1_WAIT#
- S1_A13
- S1_INPACK#
- S1_WE#
- S1_A16
- S1_BVD1
- S1_WP
- S1_RDY#
- PCM_SPK#
- S1_BVD2
- S1_CD2#
- S1_CD1#
- S1_VS2
- S1_VS1
- S1_D14
- S1_A18
- S1_D2

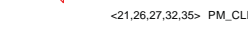
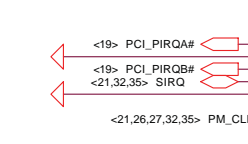
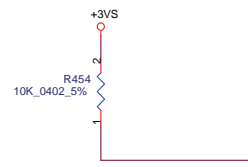
S1_A[0..25] <25>
S1_D[0..15] <25>



Place C8712
CD1# and CD2#

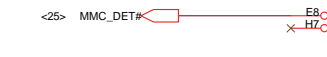
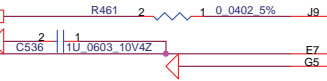


IDSEL:PCI_AD20



- PCI_AD20 F4
- PCI_PIRQA# R446
- PCI_PIRQB# R460
- SIRQ R459
- PM_CLKRUN# R457
- PCIRST# M10

- PCIRST# M10
- GRST#



- MFUNC7
- VCC_SD
- GND_SD
- SDCC#
- MSINS#
- MSCLK
- SDCLK
- SDCMD
- SDWP
- SDCLKI
- MSBS
- MSPVREN#
- SDPVREN#
- MSDATA3
- MSDATA2
- MSDATA1
- MSDATA0

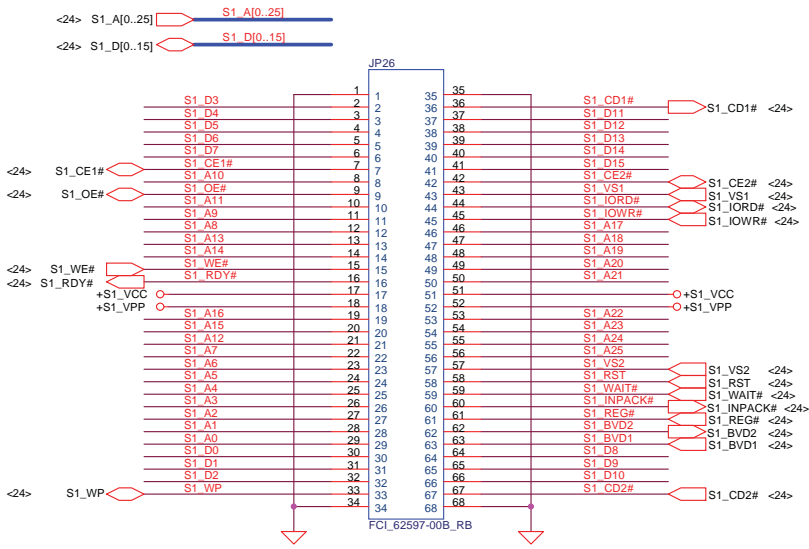
SD

- RSVD4
- RSVD3
- RSVD2
- RSVD1
- SDDAT0
- SDDAT1
- SDDAT2
- SDDAT3

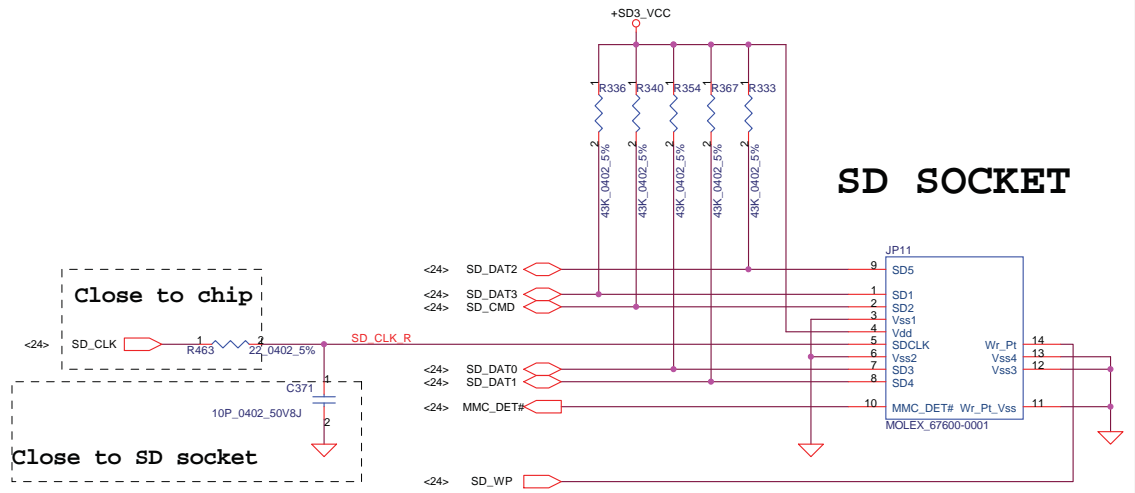
CB712_LFBGA_169P

Title		PCMCIA Controller ENE CB1410 & CB712	
Size	Document Number	EDX20 LA-2481	
Custom	Rev	0.5	
Date:	Tuesday, February 22, 2005	Sheet	24 of 48

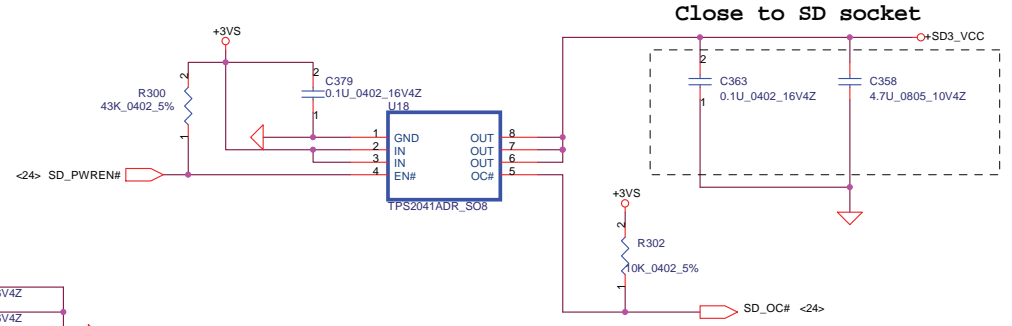
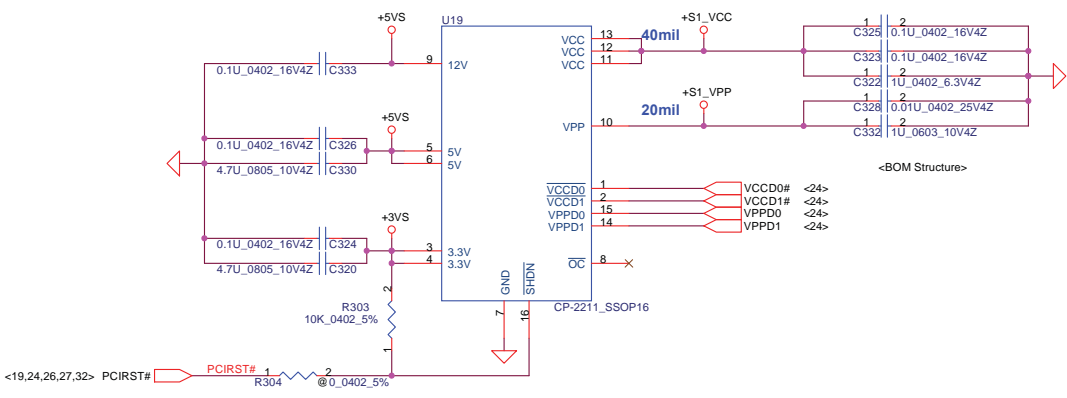
CARDBUS SOCKET



SD SOCKET

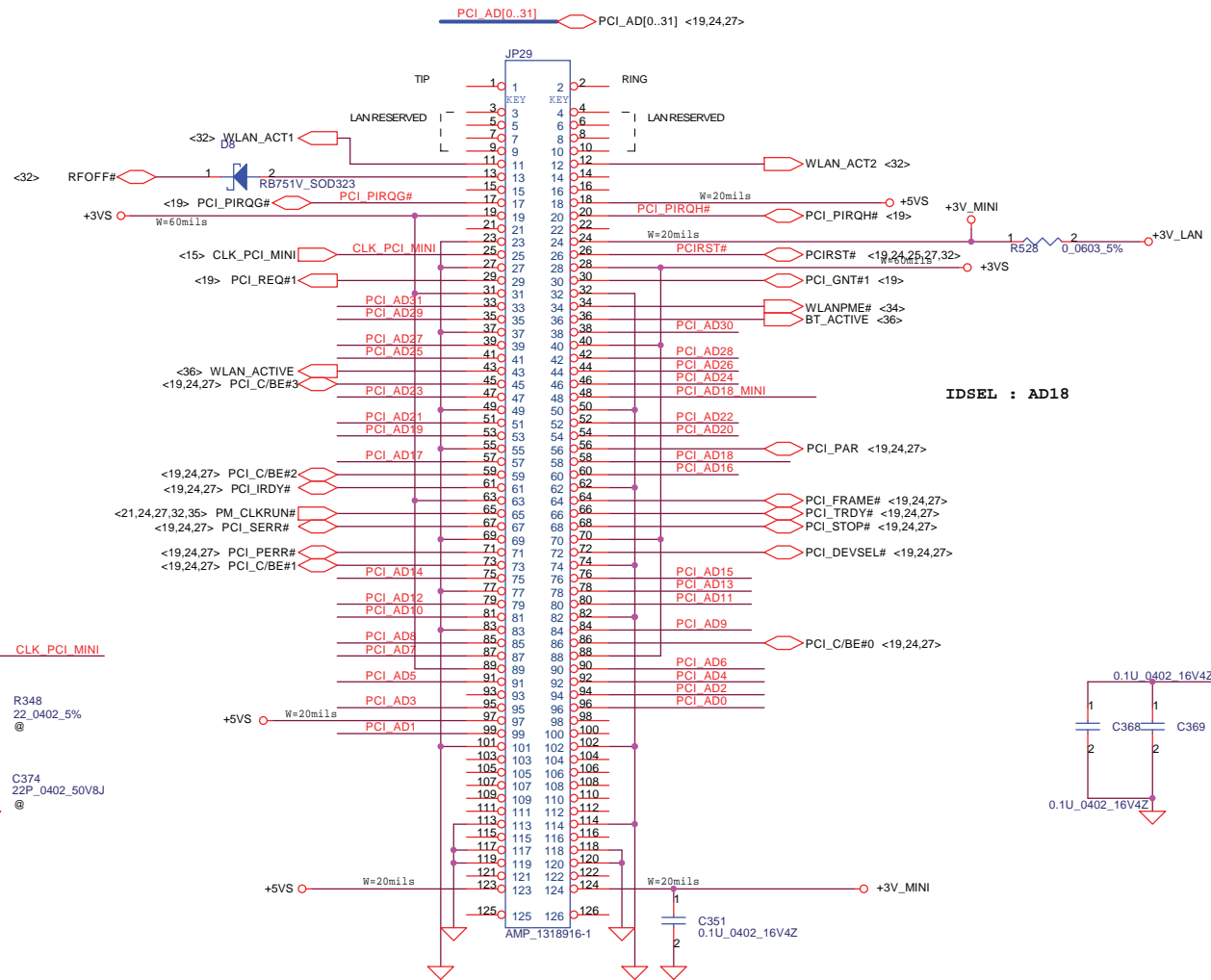
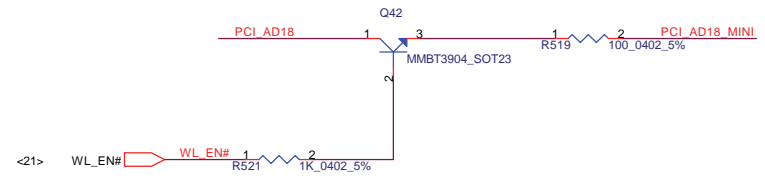


PCMCIA Power Controller

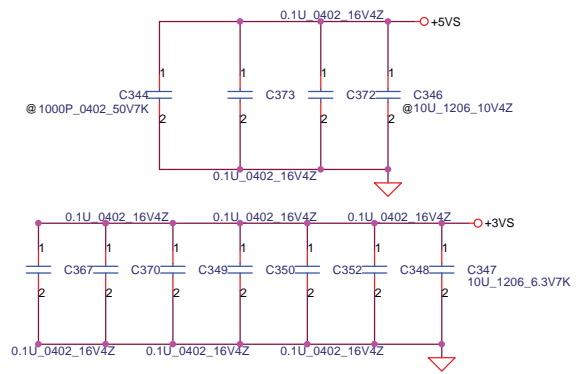


Compal Electronics, Inc.			
Title: PCMCIA/SD SOCKET			
Size: EDX20	Document Number: LA-2481	Rev: 0.5	
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-+5VS limited to 100mA
-+3.3VAUX--Normal:
375mA, D3: 200mA,
-+3VS_MINIPCI: 500mA
for wireless LAN



IDSEL : AD18

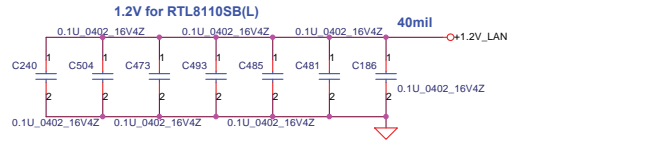
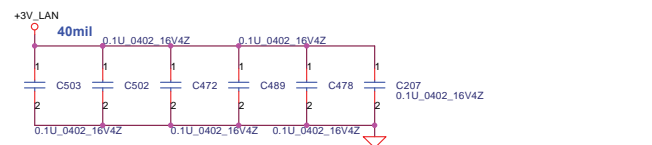
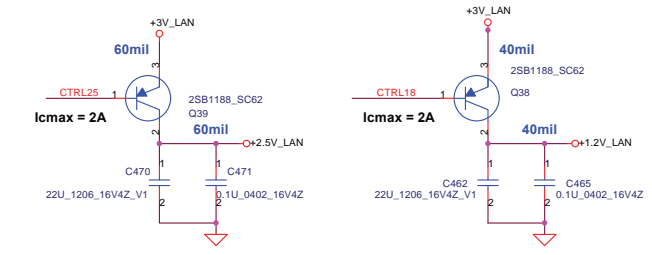
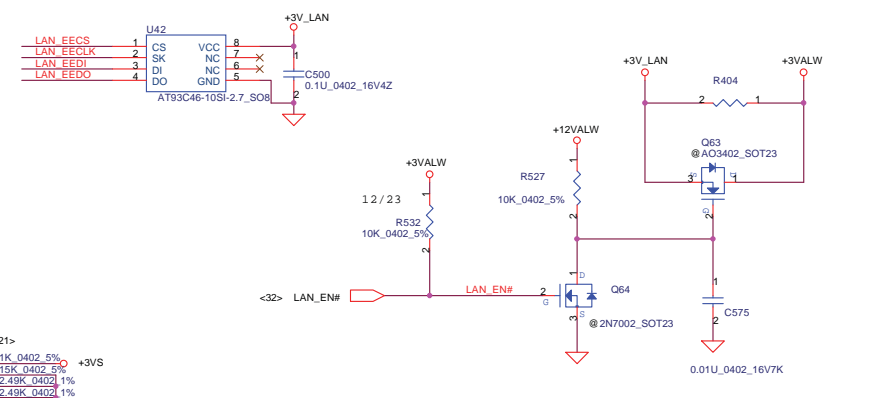
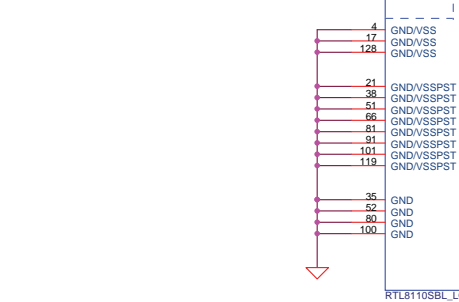
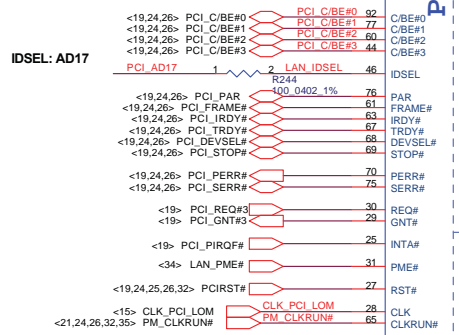
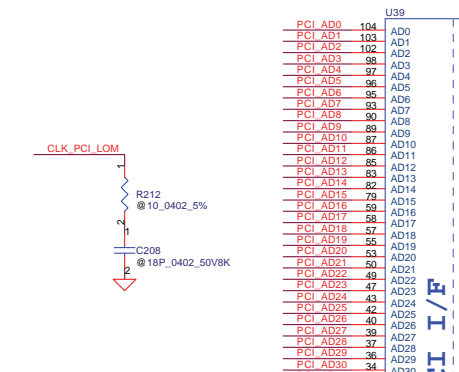


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Compal Electronics, Inc. Title MiniPCI TYPEIII Slot Size Document Number EDX20 LA-2481 Rev 0.5 Date: Tuesday, February 22, 2005 Sheet 26 of 48

LAN RTL8110SB(L)

<19,24,26> PCI_AD[0..31] PCI_AD[0..31]



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Compal Electronics, Inc.

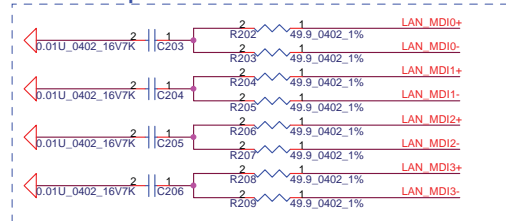
File: LAN CONTROLLER

Size: Document Number: EDX20 LA-2481

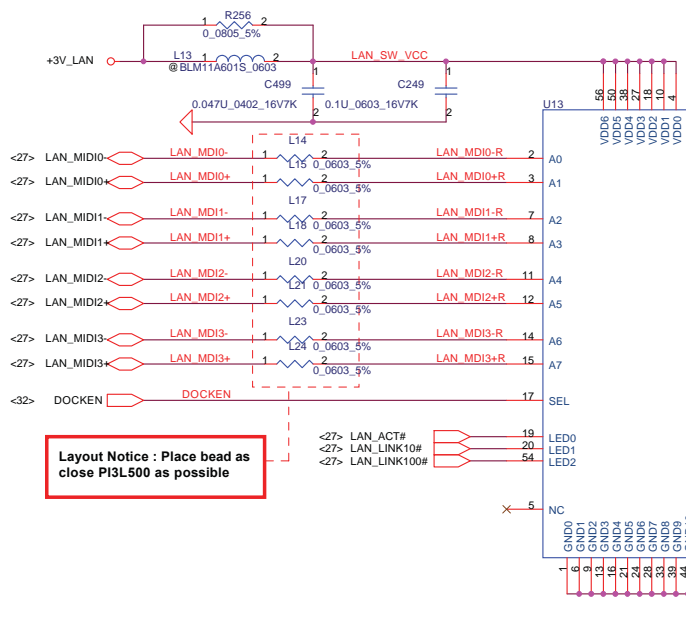
Date: Tuesday, February 22, 2005 Sheet 27 of 48

Rev: 0.5

Close to Chip side

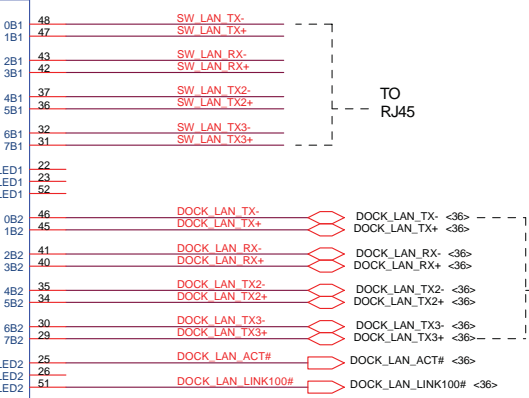


DOCKEN 1: TO DOCK
0: TO RJ45



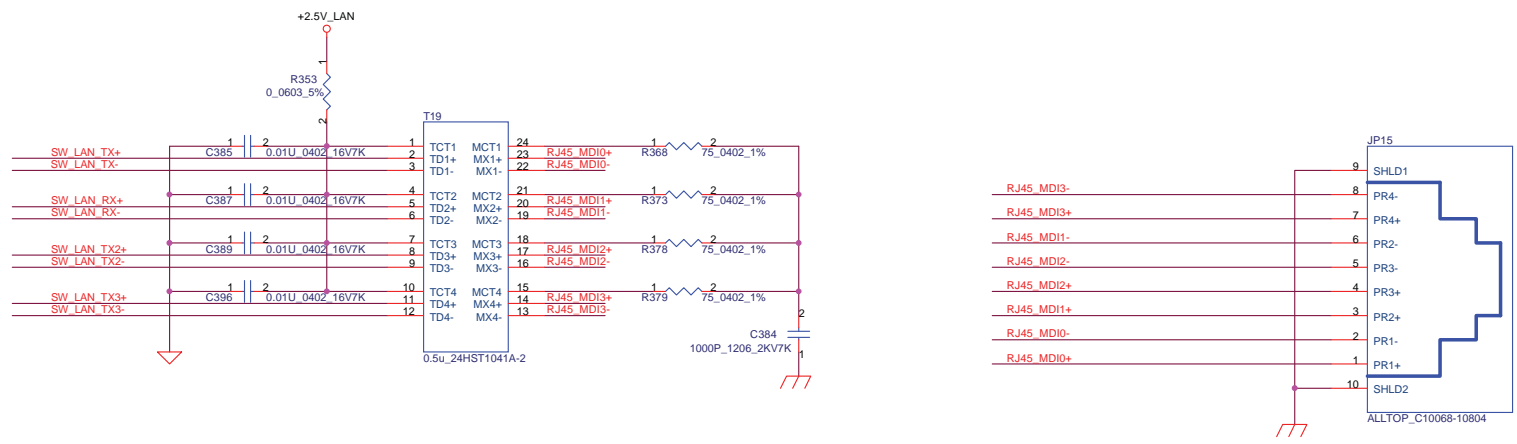
Layout Notice : Place bead as close P13L500 as possible

LAN ANALOG SWITCH

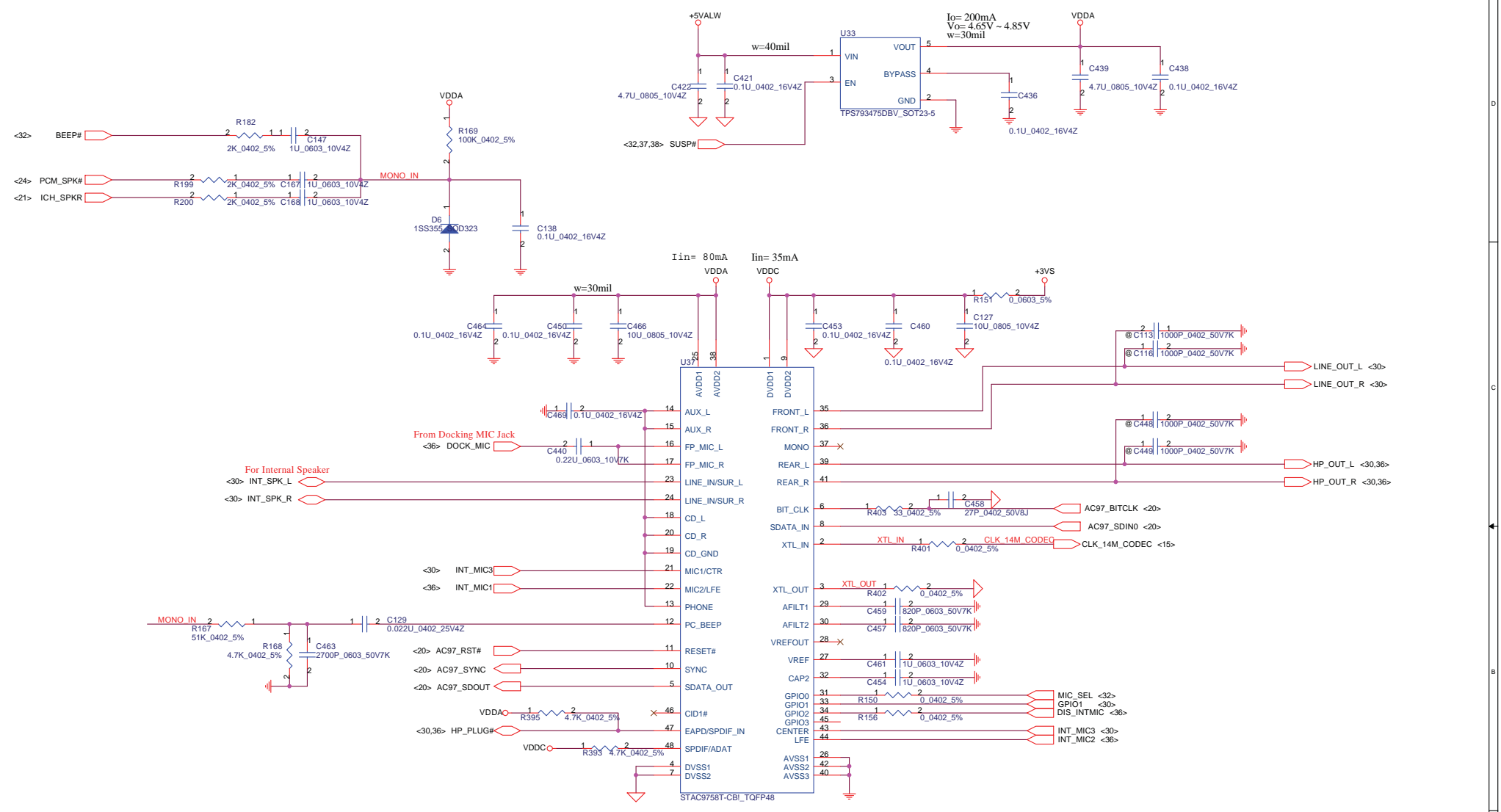


TO RJ45

TO DOCK



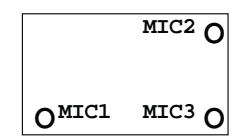
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DIS_INTMIC (PIN 34)	INT_MIC1 INT_MIC2 INT_MIC3	DOCK_MIC (PIN 16)
H	DISABLE	ENABLE
L	ENABLE	DISABLE

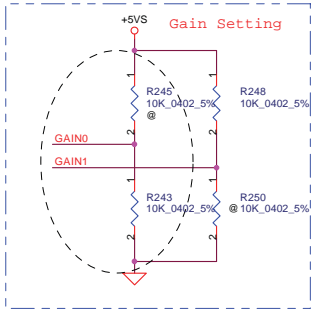
EAPD (PIN 47)	LINE_IN_L PIN23 LINE_IN_R PIN24
H	ENABLE
L	DISABLE

MIC_SEL (PIN 31)	INT_MIC1 (PIN 22)	INT_MIC2 (PIN 44)	INT_MIC3 (PIN 21,43)
L (Landscape)	ENABLE	DISABLE	ENABLE
H (Portrait)	DISABLE	ENABLE	ENABLE

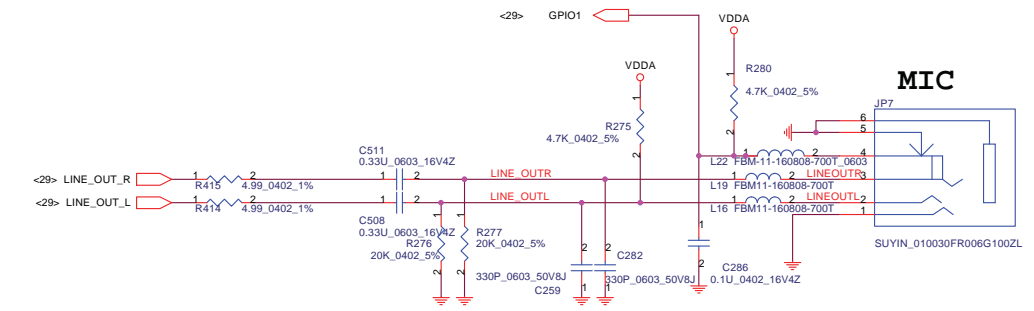
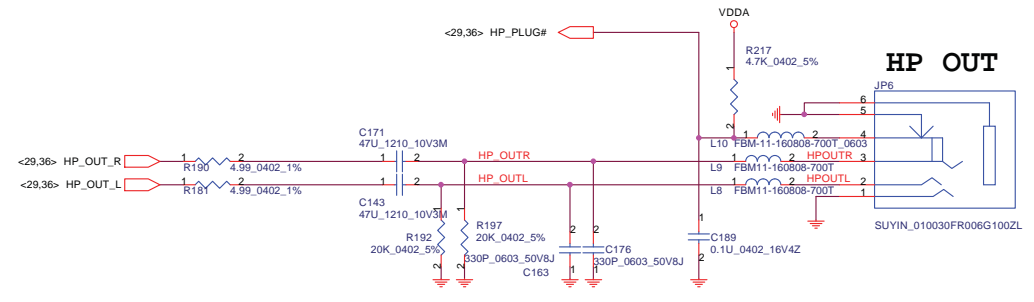
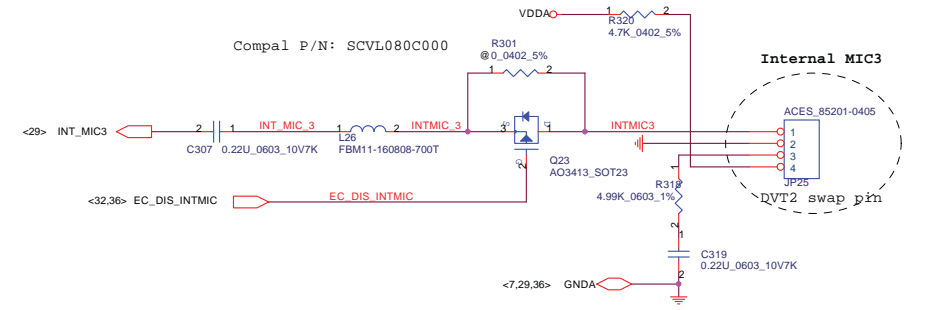
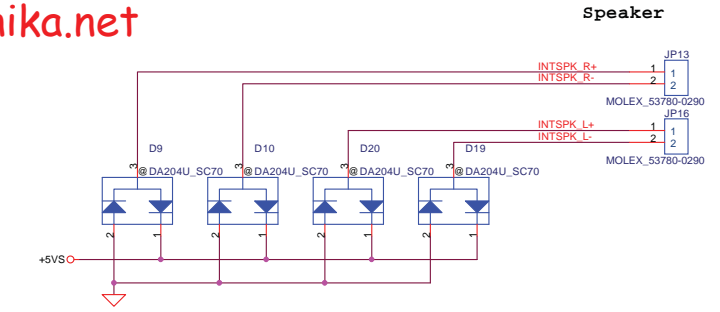
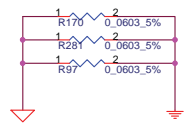
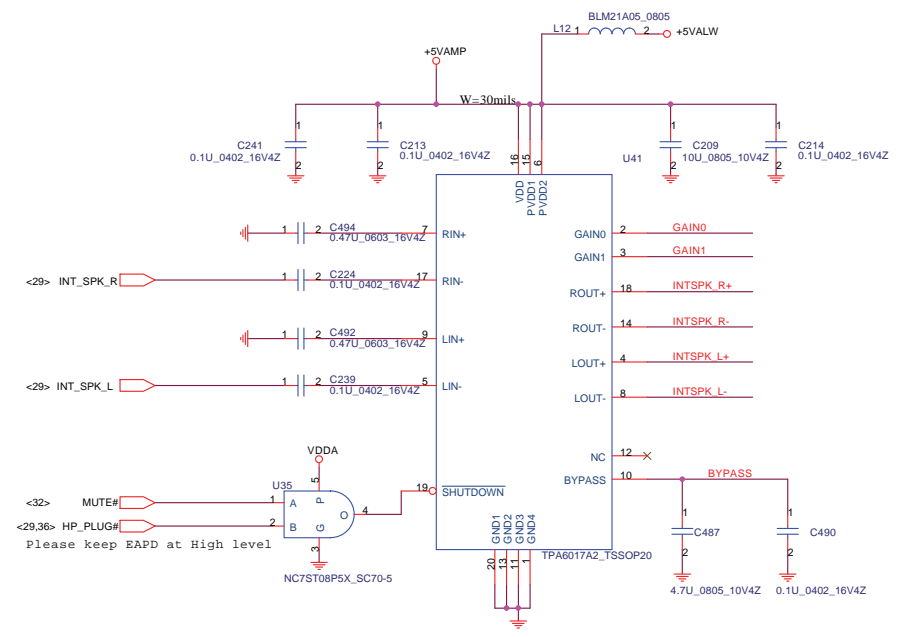


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Compal Electronics, Inc.		
Title		
AC97 STAC9758		
Size	Document Number	Rev
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Date:	Tuesday, February 22, 2005	Sheet 29 of 48

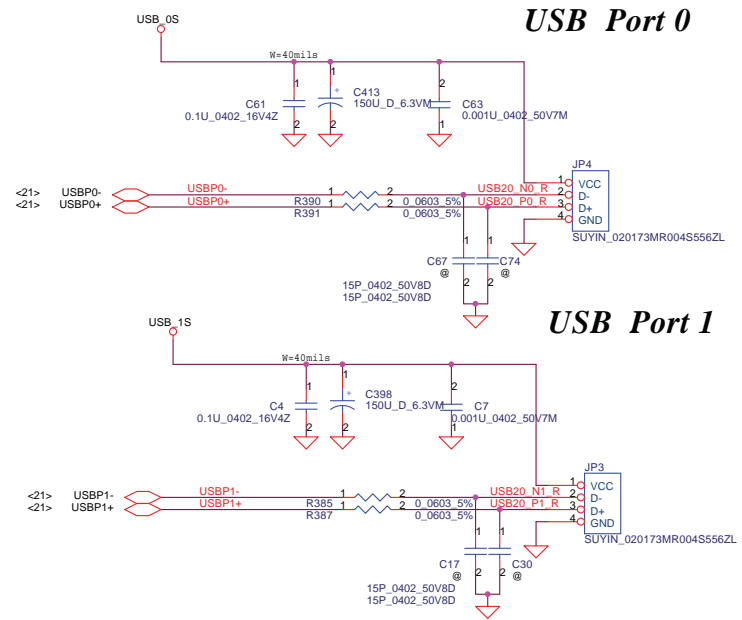
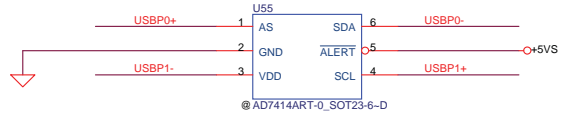
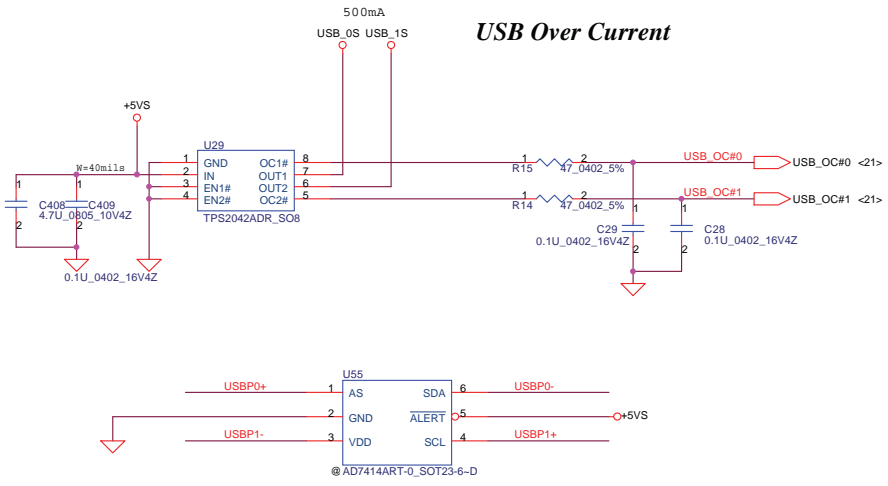


GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm



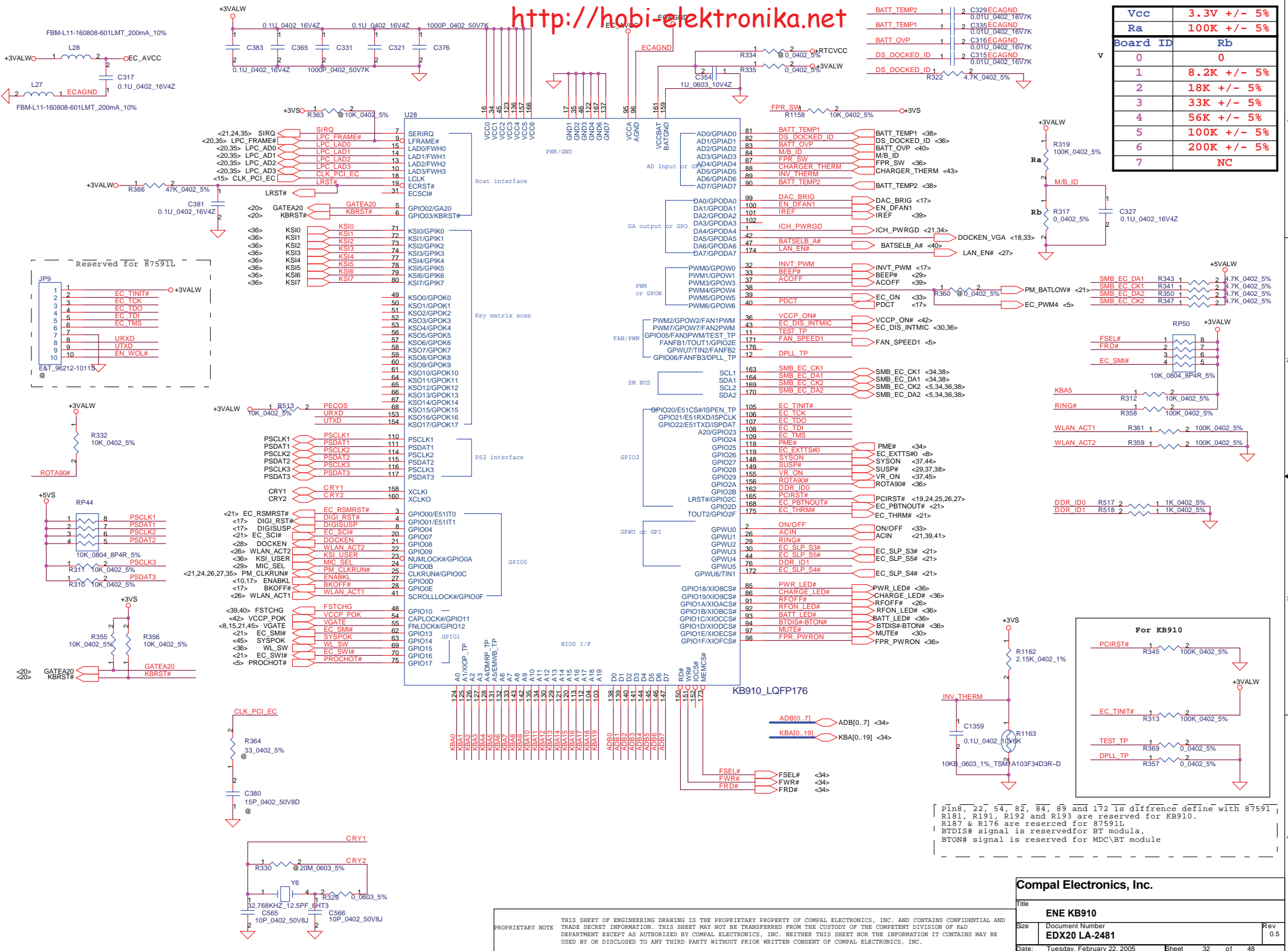
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Compal Electronics, Inc.
 Title: **AMP & Audio Jack**
 Document Number: **EDX20 LA-2481**
 Date: Tuesday, February 22, 2005 Sheet 30 of 48
 Rev 0.5

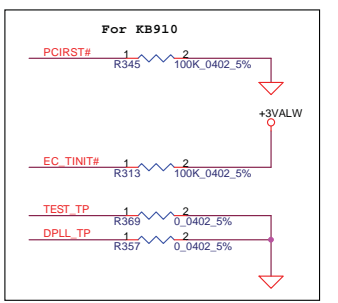


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Compal Electronics, Inc.		
Title		
USB Port x2		
Size	Document Number	Rev
	EDX20 LA-2481	0.5
Date:	Tuesday, February 22, 2005	Sheet 31 of 48

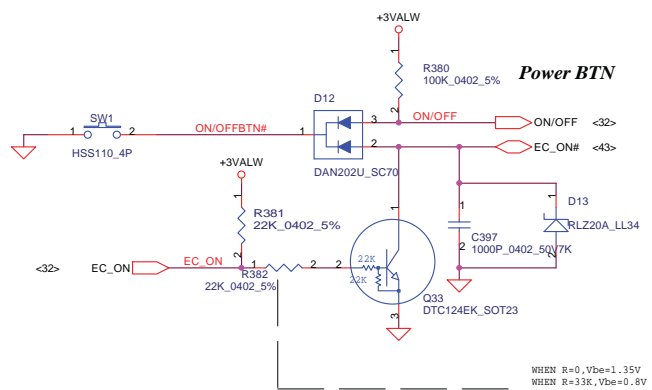
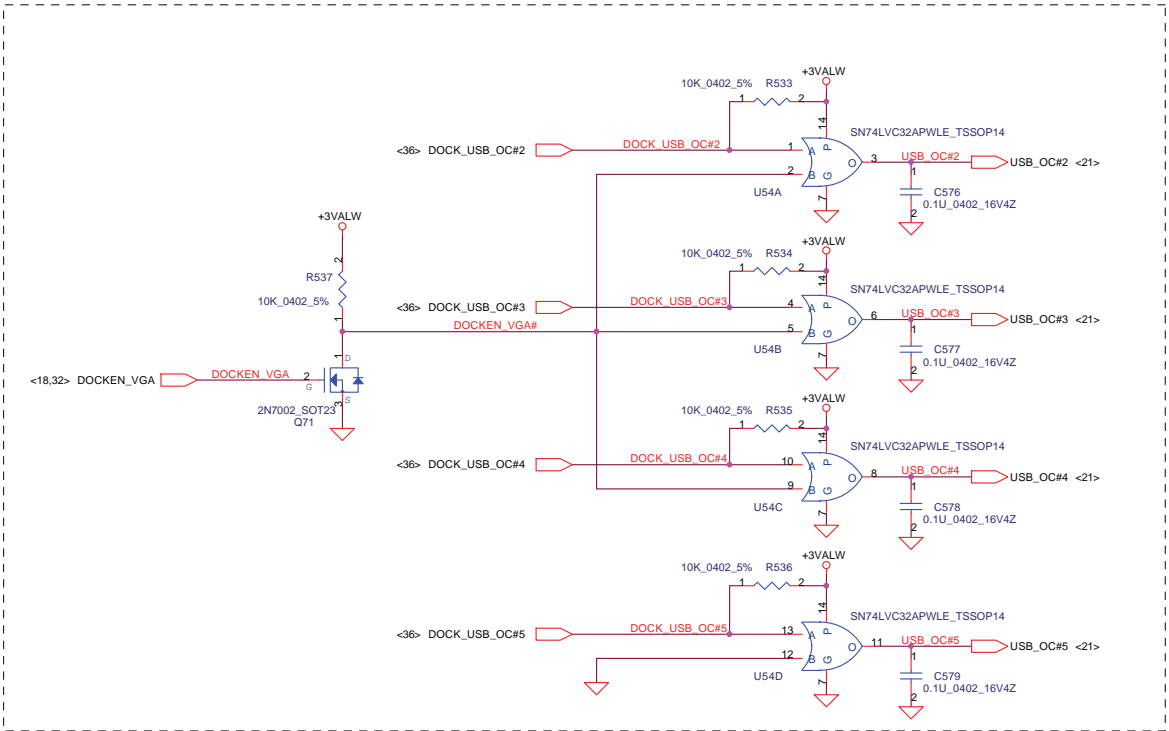


Vcc	3.3V +/- 5%
Ra	100K +/- 5%
Board ID	Rb
0	0
1	8.2K +/- 5%
2	18K +/- 5%
3	33K +/- 5%
4	56K +/- 5%
5	100K +/- 5%
6	200K +/- 5%
7	NC



Pin8, 22, 54, 82, 84, 89 and 172 is difference define with 87591
 R181, R191, R192 and R193 are reserved for KB910.
 R187 & R176 are reserved for 87591!
 BTDIS# signal is reservedfor BT modula,
 BTON# signal is reserved for MDC/BT module

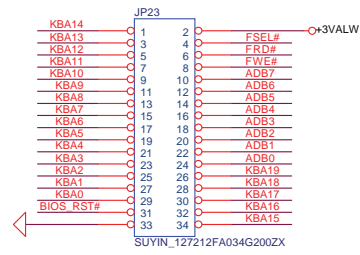
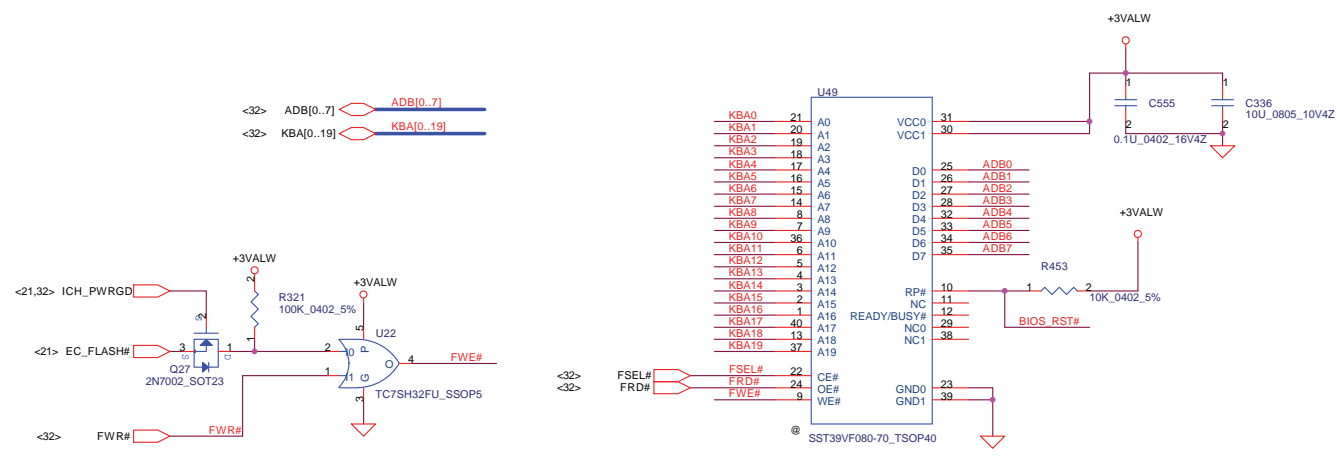
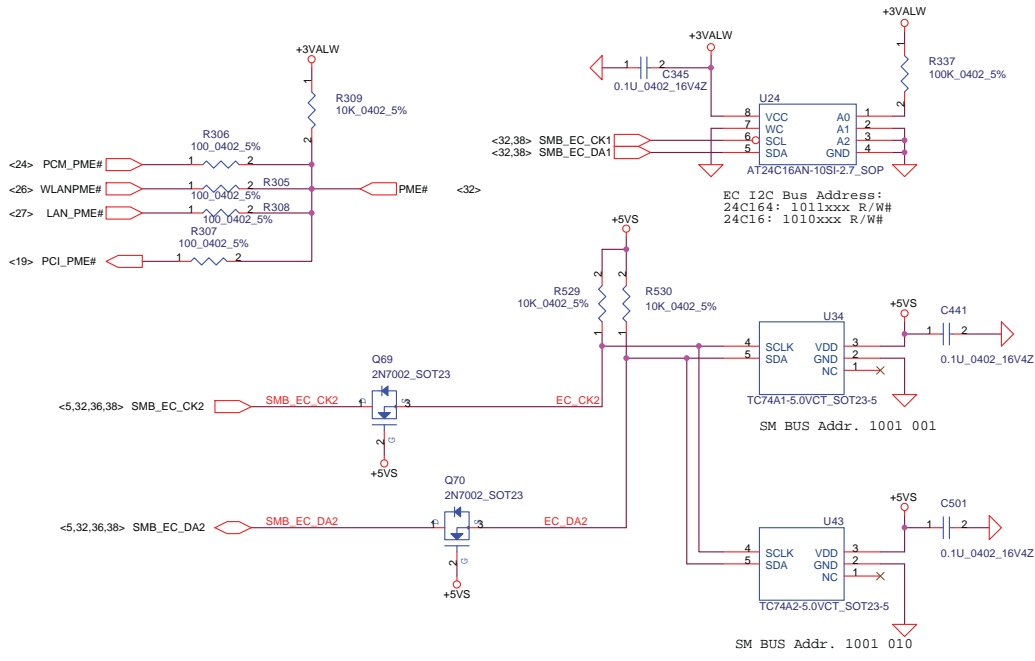
PVT



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Compal Electronics, Inc.		
Title	Power ON/OFF SW	
Size	Document Number	Rev
	EDX20 LA-2481	0.5
Date:	Tuesday, February 22, 2005	Sheet 33 of 48

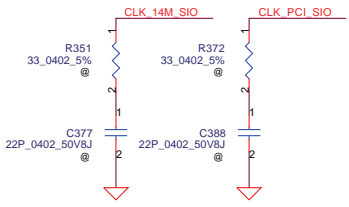
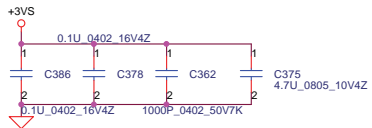
NM24C164 Address definition: 1 A2 A1# A0 B2 B1 B0 R/W#



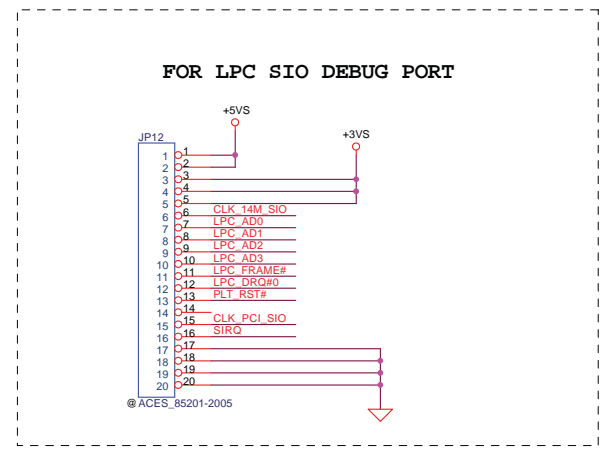
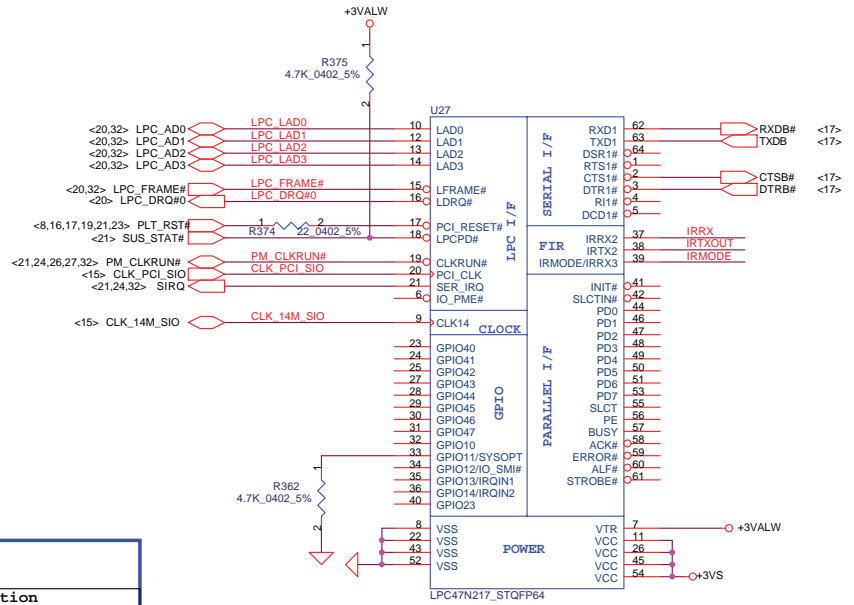
Alternative SA290080100 for U24

Compal Electronics, Inc.		
Title Thermal Sensor & BIOS		
Size	Document Number	Rev
	EDX20 LA-2481	0.5
Date:	Tuesday, February 22, 2005	Sheet 34 of 48

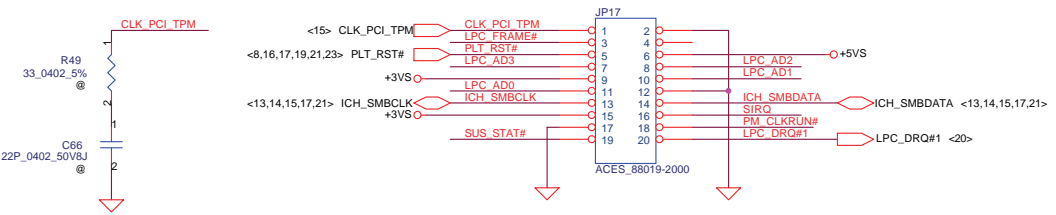
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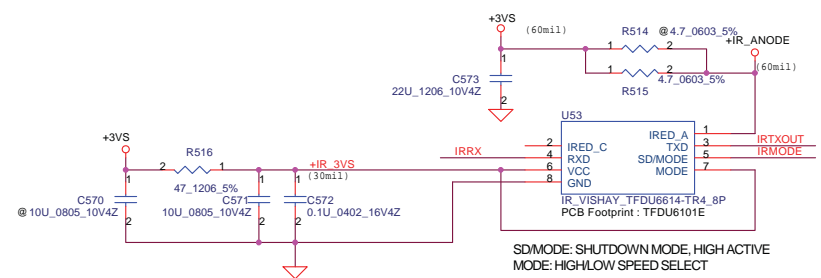
Strap pin	Pin #	Description
BADDR	33	BASE Address Selection "0": 2E-2F (Default) "1": 4E-4F



TPM



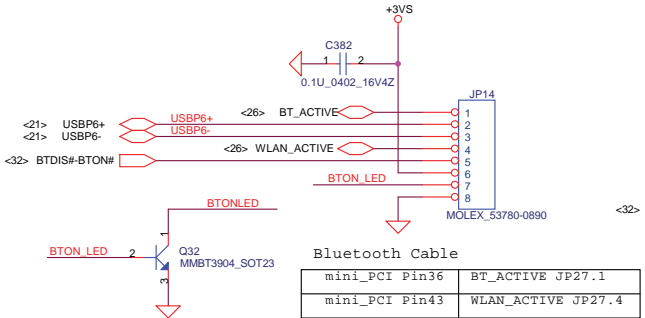
FIR



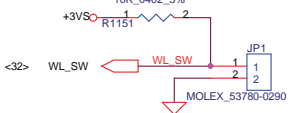
SDMODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT

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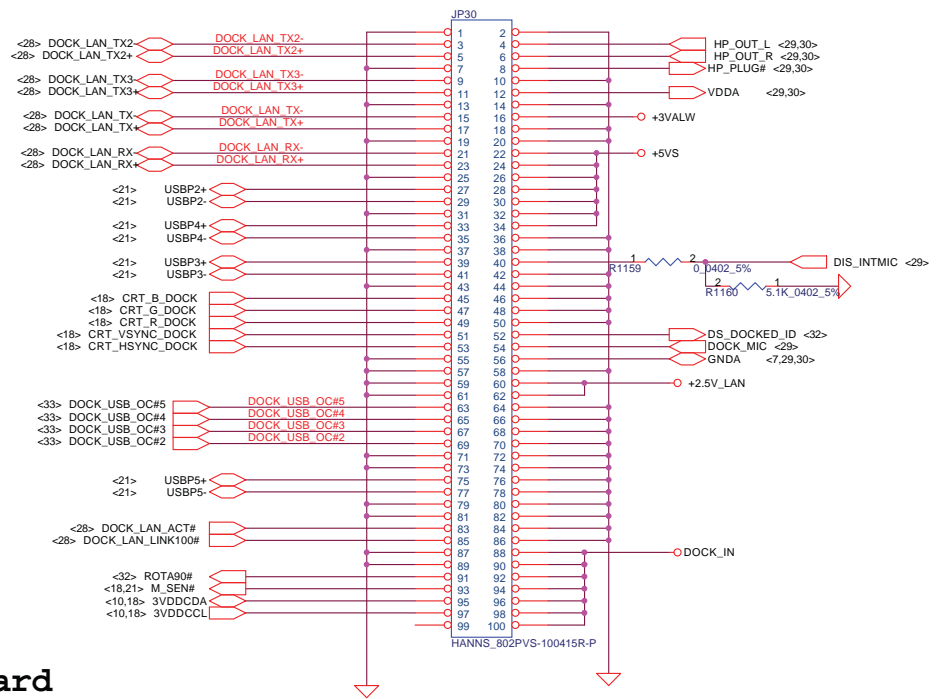
BT MODULE CONN



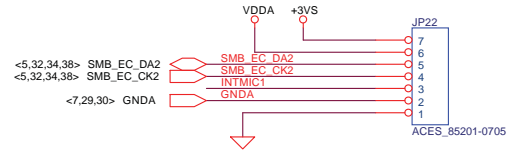
WIRELESS SW



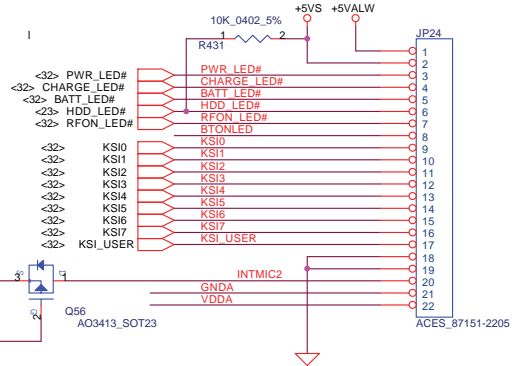
DOCKING BD.



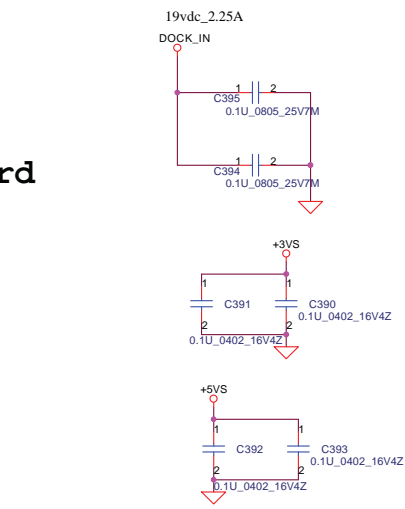
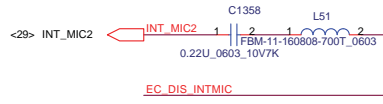
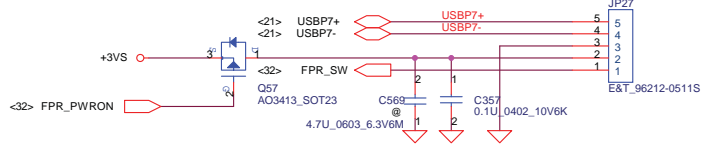
ALS/MIC board



BTN Board



Finger Print board



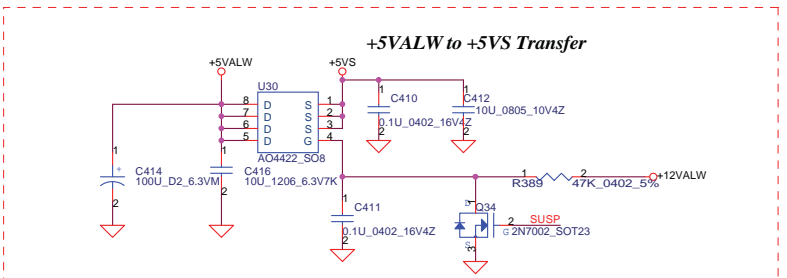
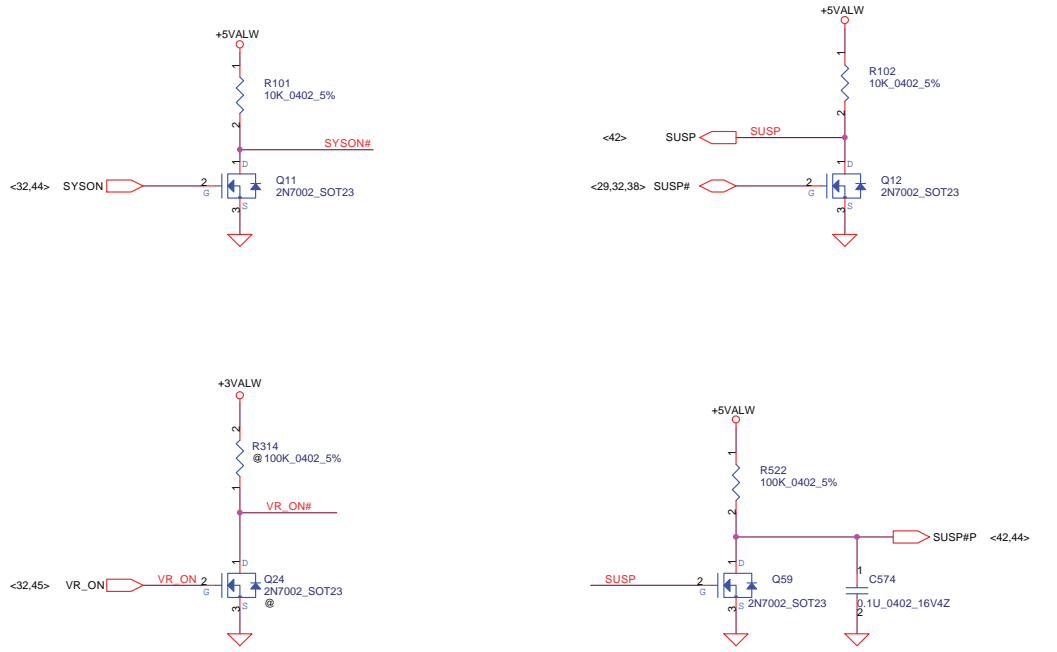
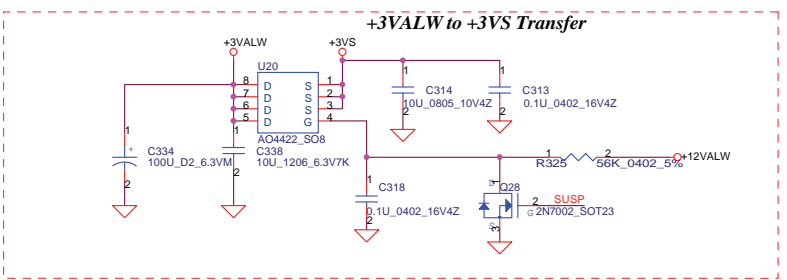
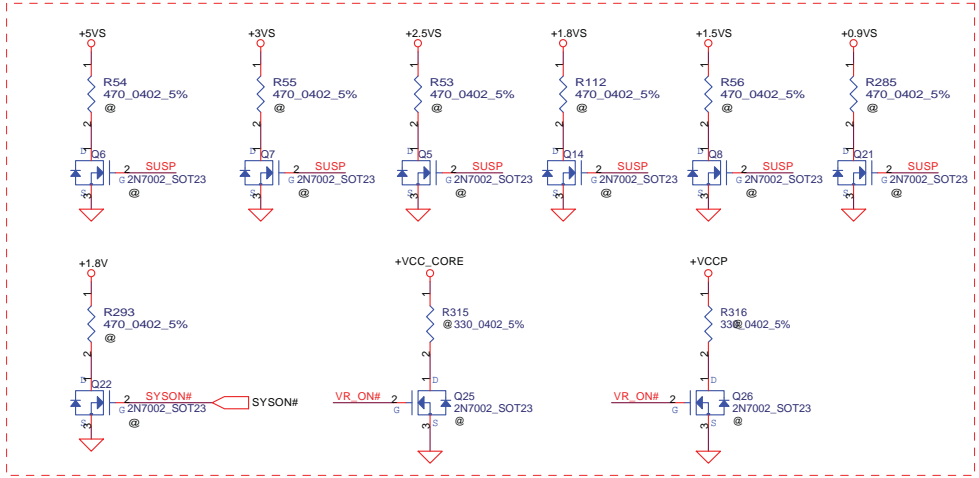
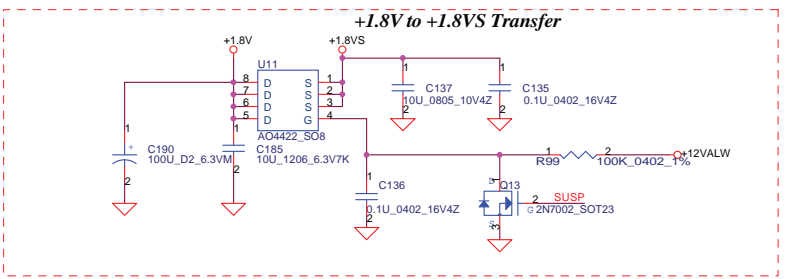
Compal Electronics, Inc.

Title: **DAUGHTER Brd I/F**

Size: Document Number **EDX20 LA-2481** Rev: 0.5

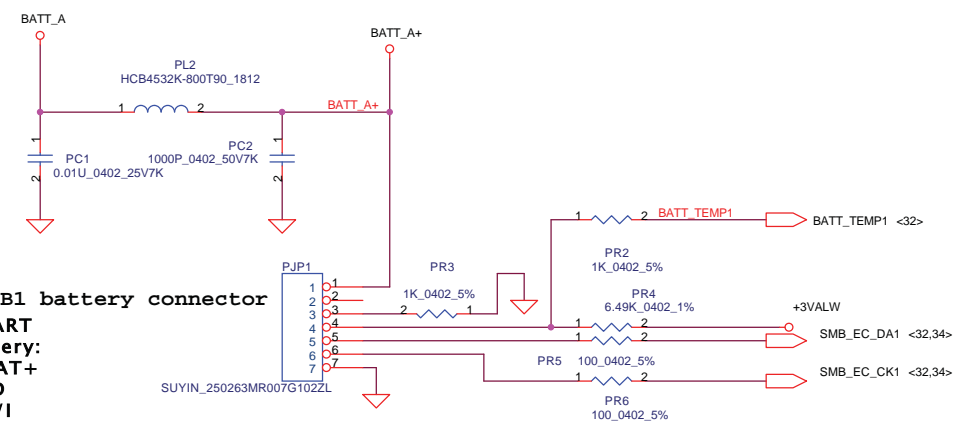
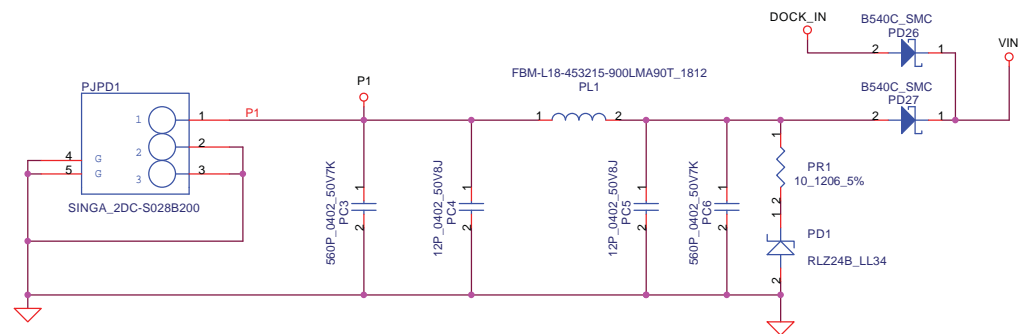
Date: Tuesday, February 22, 2005 Sheet 36 of 48

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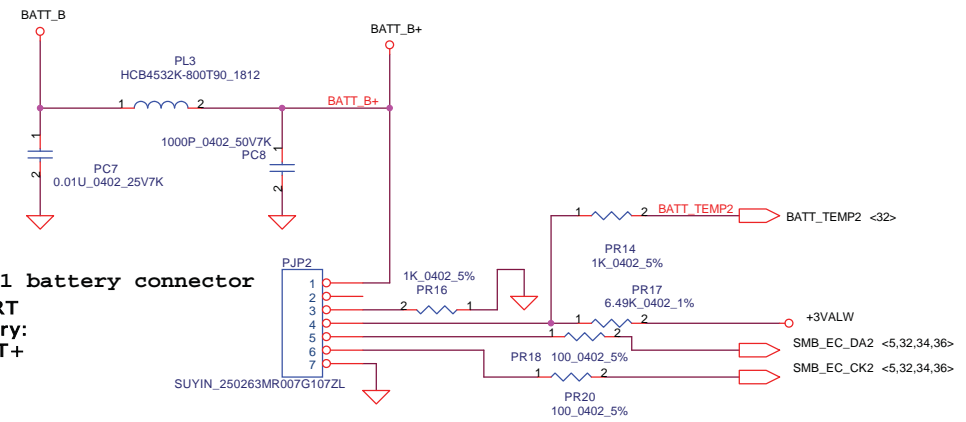
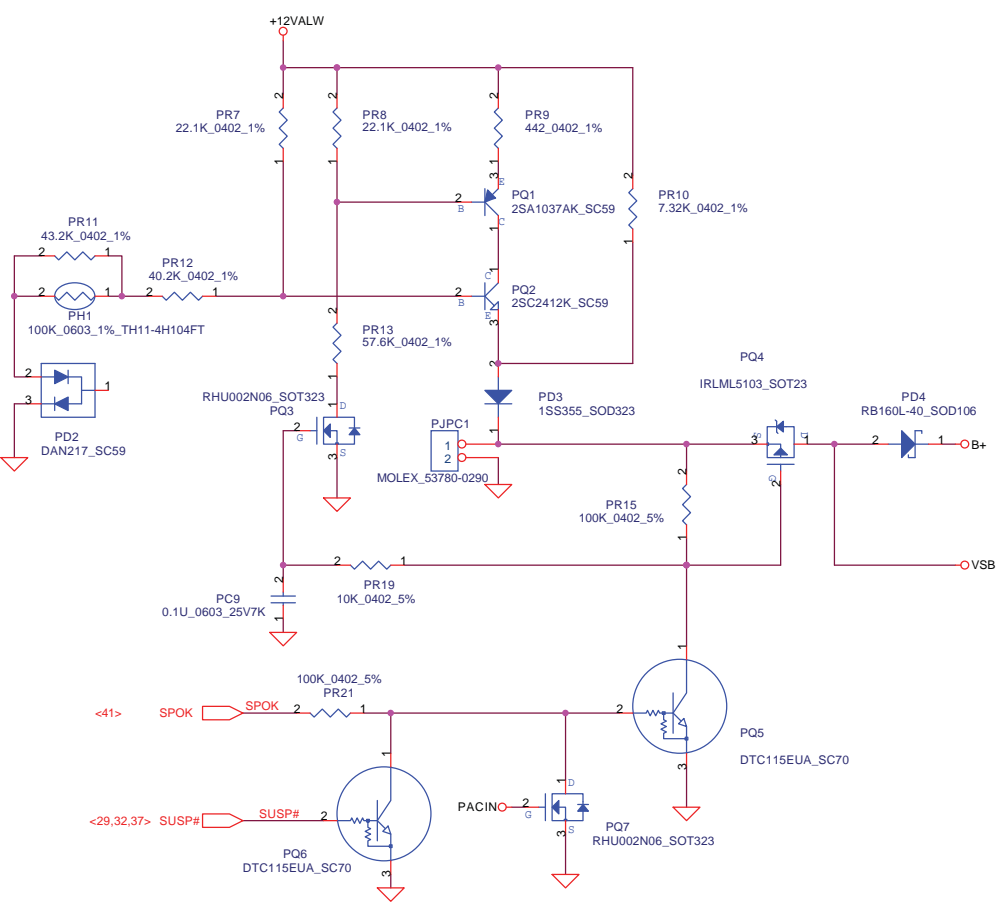


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Compal Electronics, Inc.		
Title	DC/DC Interface	
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PJPB1 battery connector
SMART Battery:
 1.BAT+
 2.ID
 3.B/I
 4.TS
 5.SMD
 6.SMC
 7.GND

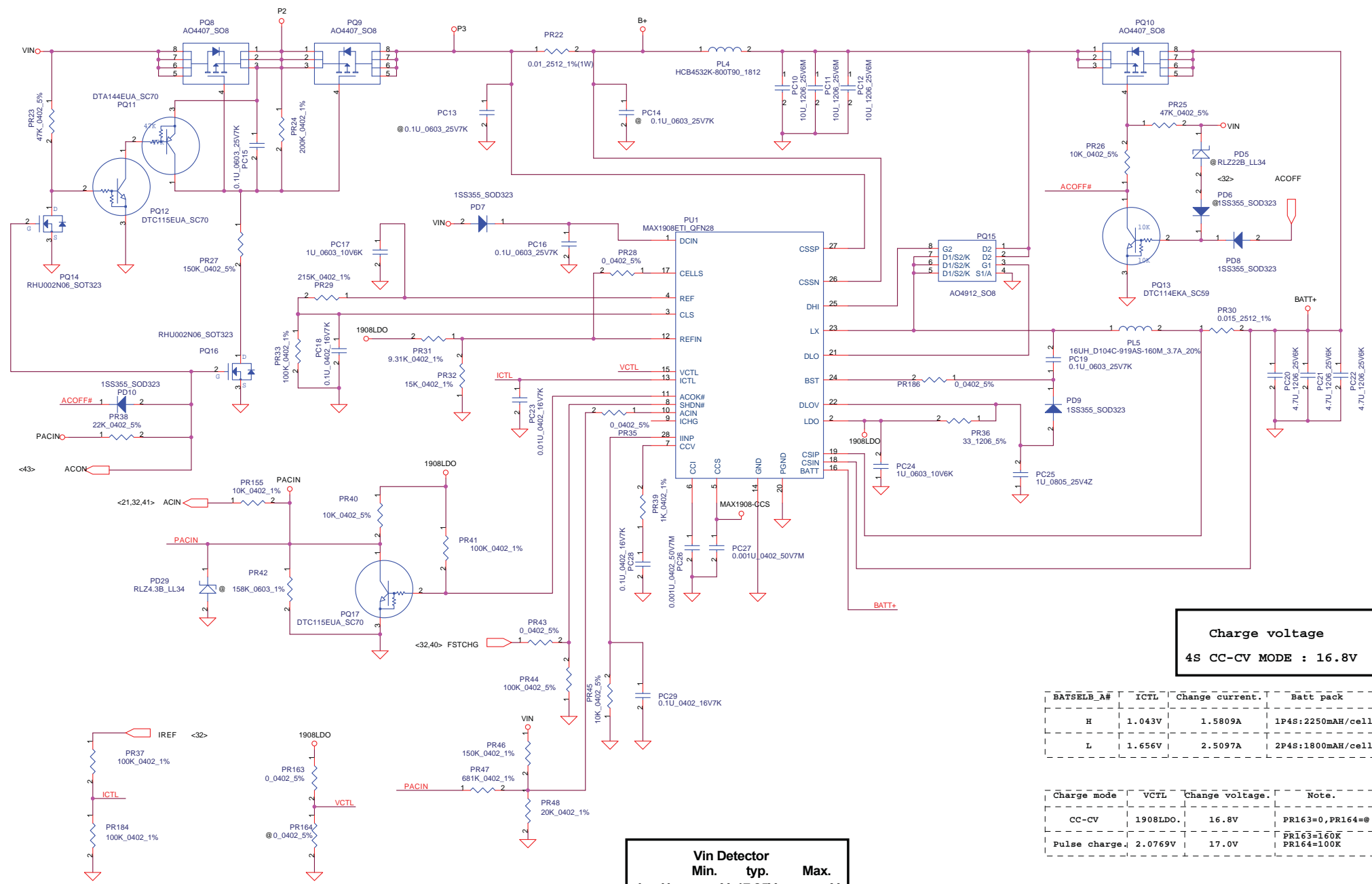


PJPB1 battery connector
SMART Battery:
 1.BAT+
 2.ID
 3.B/I
 4.TS
 5.SMD
 6.SMC
 7.GND

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COMPAL ELECTRONICS, INC			
Title Bridge batt & Batt conn & DC in			
Size	Document Number	Rev	
	EDX20 LA-2481	0.5	
Date: Tuesday, February 22, 2005		Sheet	38 of 48

I_{adp}=0~2.25A(42.75W)

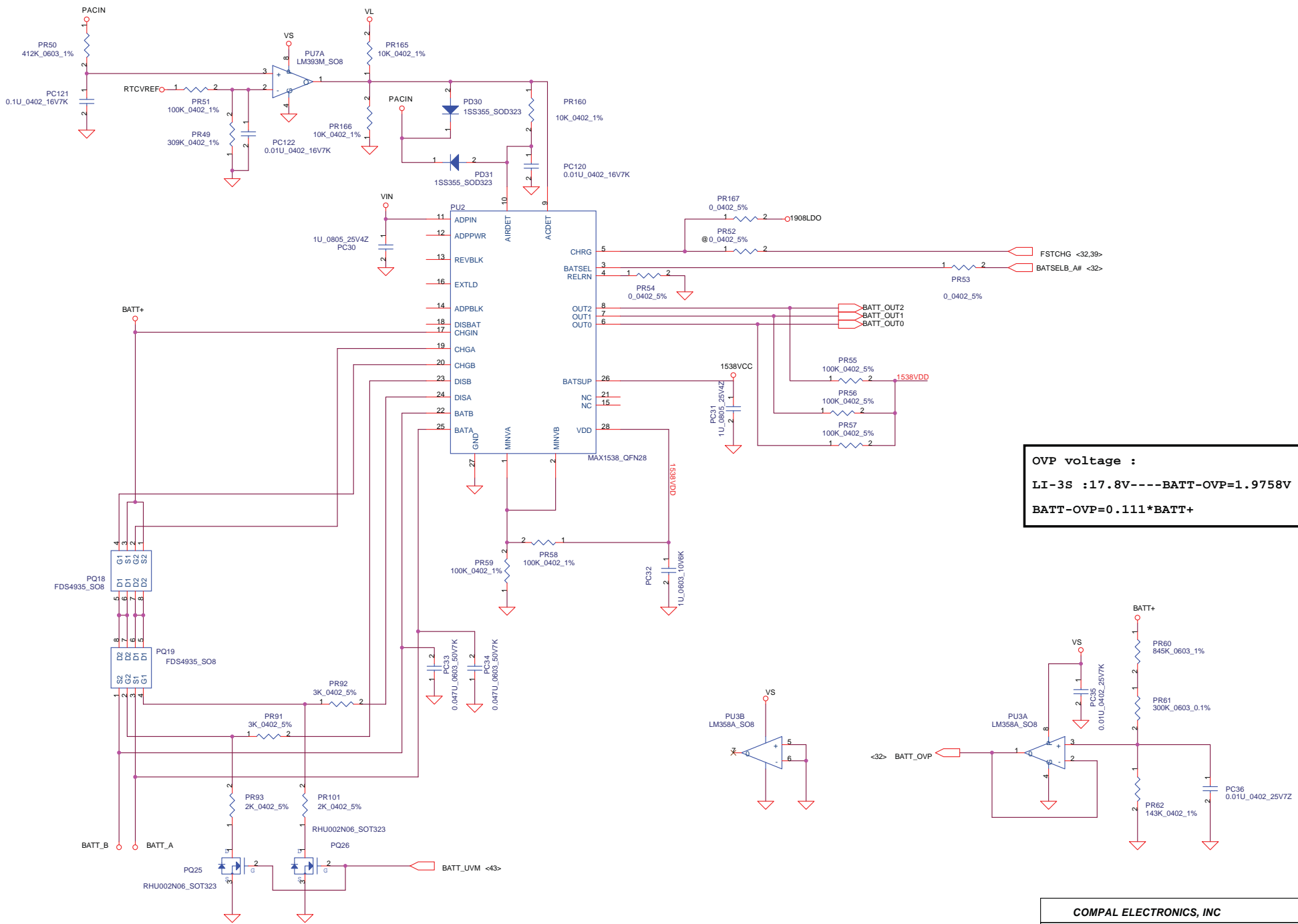


Charge voltage
4S CC-CV MODE : 16.8V

BATSELB_A#	ICTL	Change current.	Batt pack
H	1.043V	1.5809A	1P4S:2250MAH/cell
L	1.656V	2.5097A	2P4S:1800MAH/cell

Charge mode	VCTL	Change voltage.	Note.
CC-CV	1908LDO	16.8V	PR163=0, PR164=#
Pulse charge	2.0769V	17.0V	PR163=150K PR164=100K

Vin Detector		
Min.	typ.	Max.
L->H	V 17.85V	V
H->L	V 16.98V	V

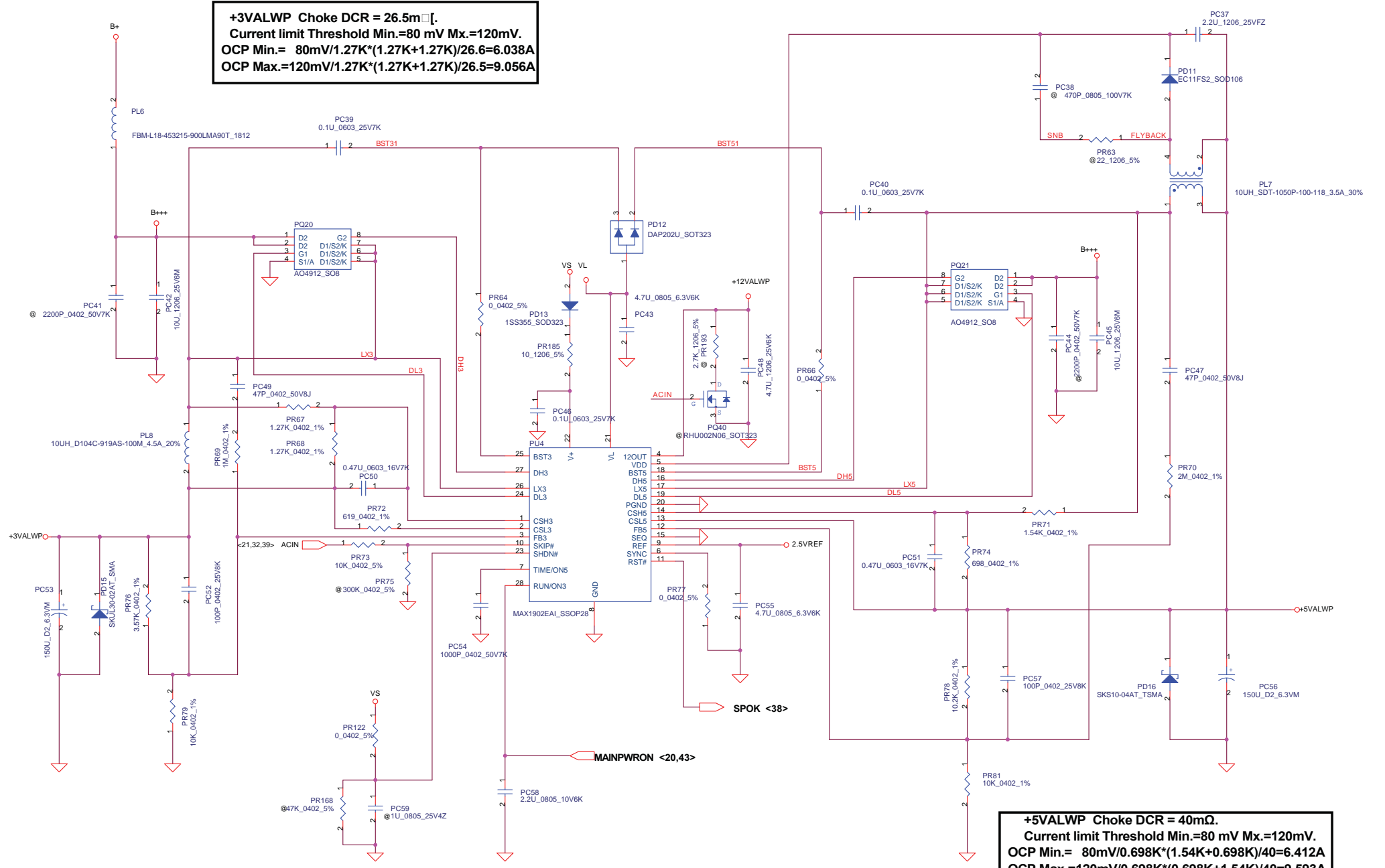


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+3VALWP Choke DCR = 26.5mΩ.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/1.27K*(1.27K+1.27K)/26.6=6.038A
OCP Max.=120mV/1.27K*(1.27K+1.27K)/26.5=9.056A

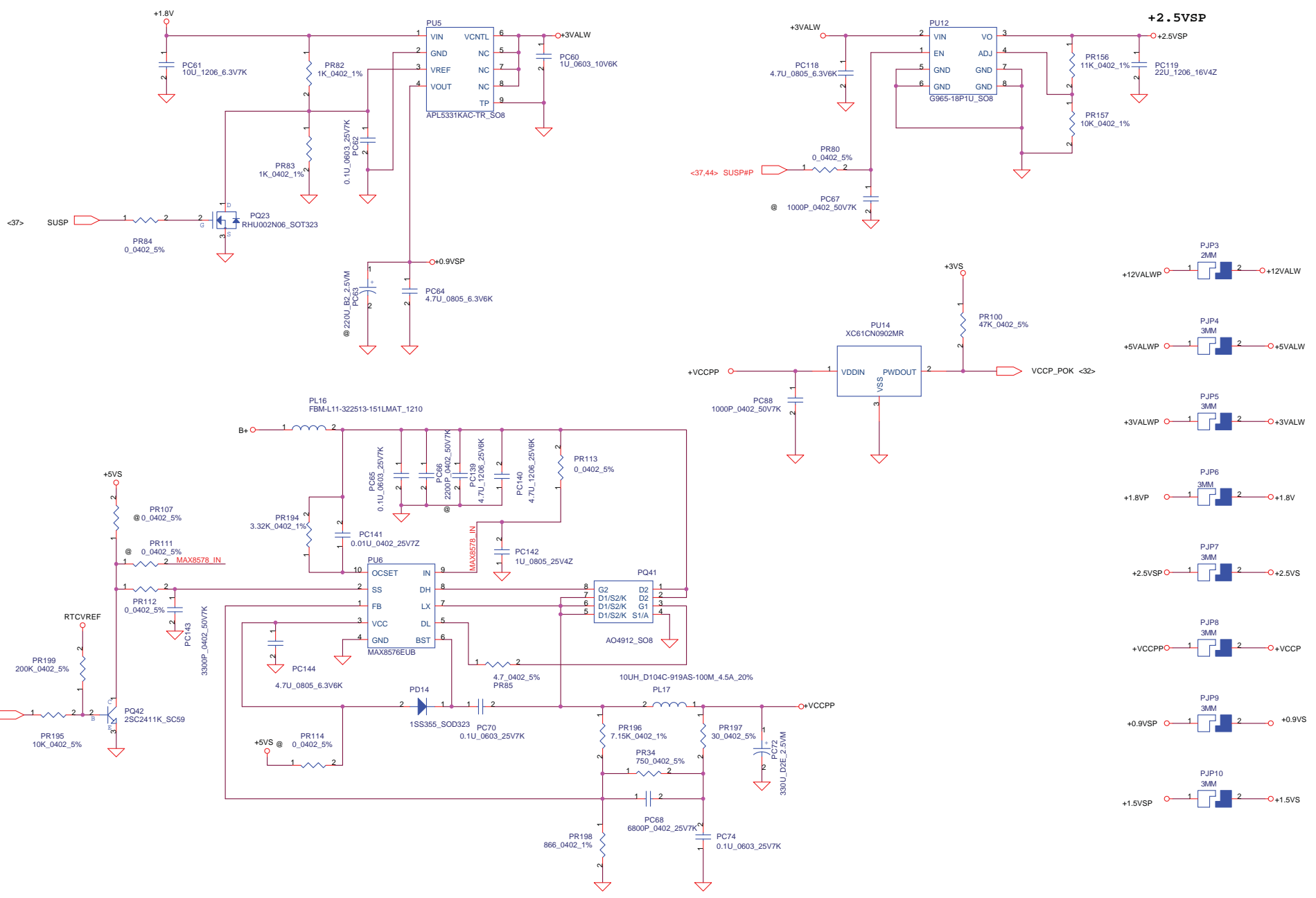
+5VALWP Choke DCR = 40mΩ.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/0.698K*(1.54K+0.698K)/40=6.412A
OCP Max.=120mV/0.698K*(0.698K+1.54K)/40=9.593A

$RS2(PR64)=RS1(PR58)*RS3(PR61)/(RS1+RS3)$
 $L/RL(DCR)=RS1*RS3(PR61)/(RS1+RS3)*Cs(PC56)$



COMPAL ELECTRONICS, INC		
Title +3VALWP & +5VALWP & +12VALWP		
Size	Document Number EDX20 LA-2481	Rev 0.5
Date: Tuesday, February 22, 2005	Sheet	41 of 48

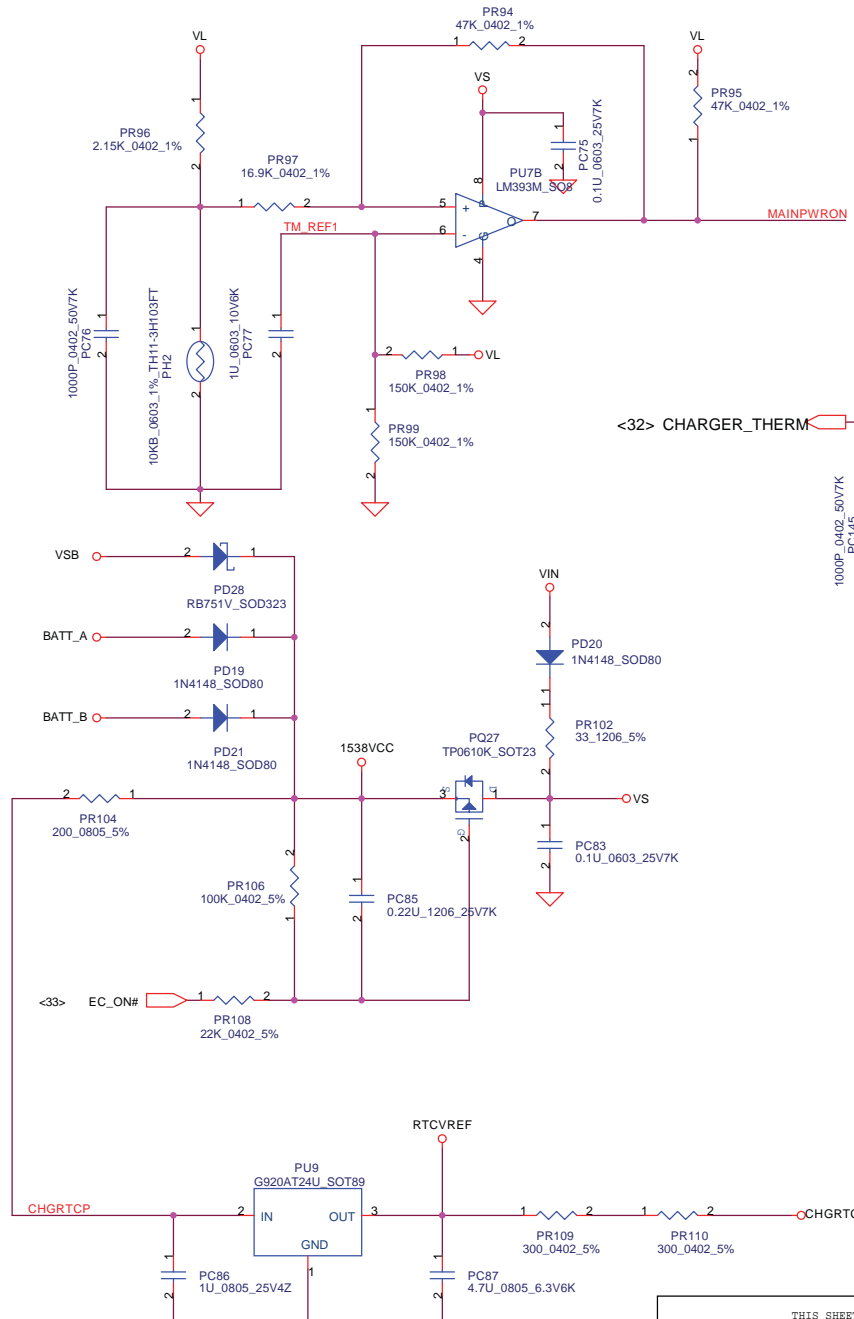
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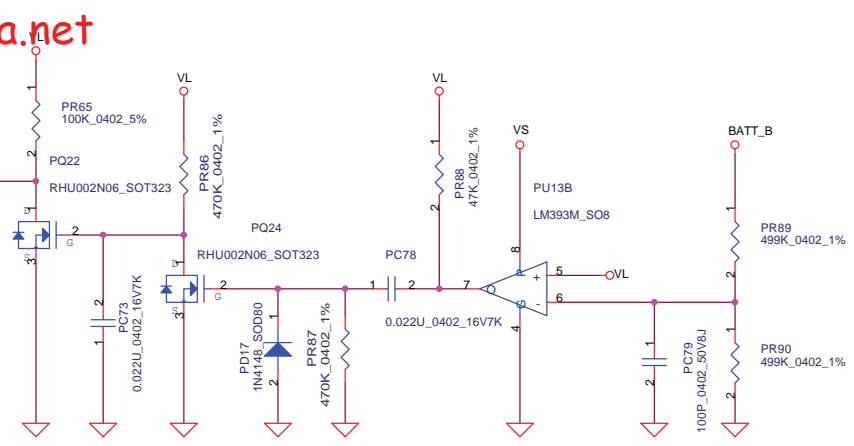
COMPAL ELECTRONICS, INC		
Title		
+VCCPP & +0.9VSP & +2.5VSP		
Size	Document Number	Rev
	EDX20 LA-2481	0.5
Date: Tuesday, February 22, 2005		
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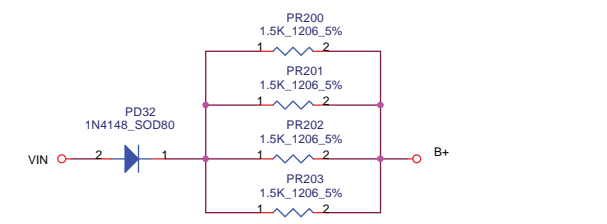
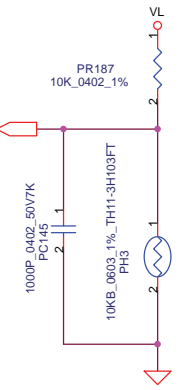
PH2 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C



<40> BATT_UVM

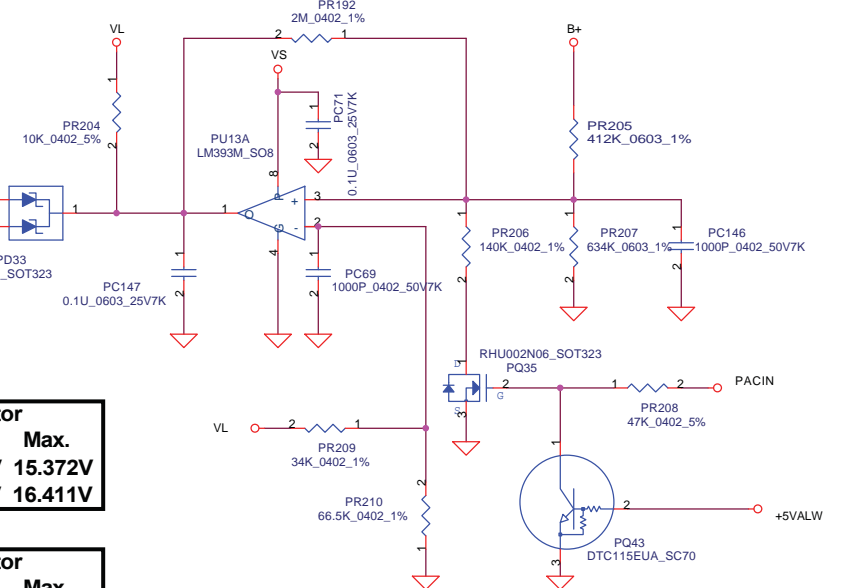


<32> CHARGER_THERM



<20,41> MAINPWON

<39> ACON



ACIN

Precharge detector			
	Min.	typ.	Max.
H->L	14.556V	14.807V	15.372V
L->H	15.276V	15.836V	16.411V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H->L	5.044V	5.096V	5.205V
L->H	6.008V	6.124V	6.243V

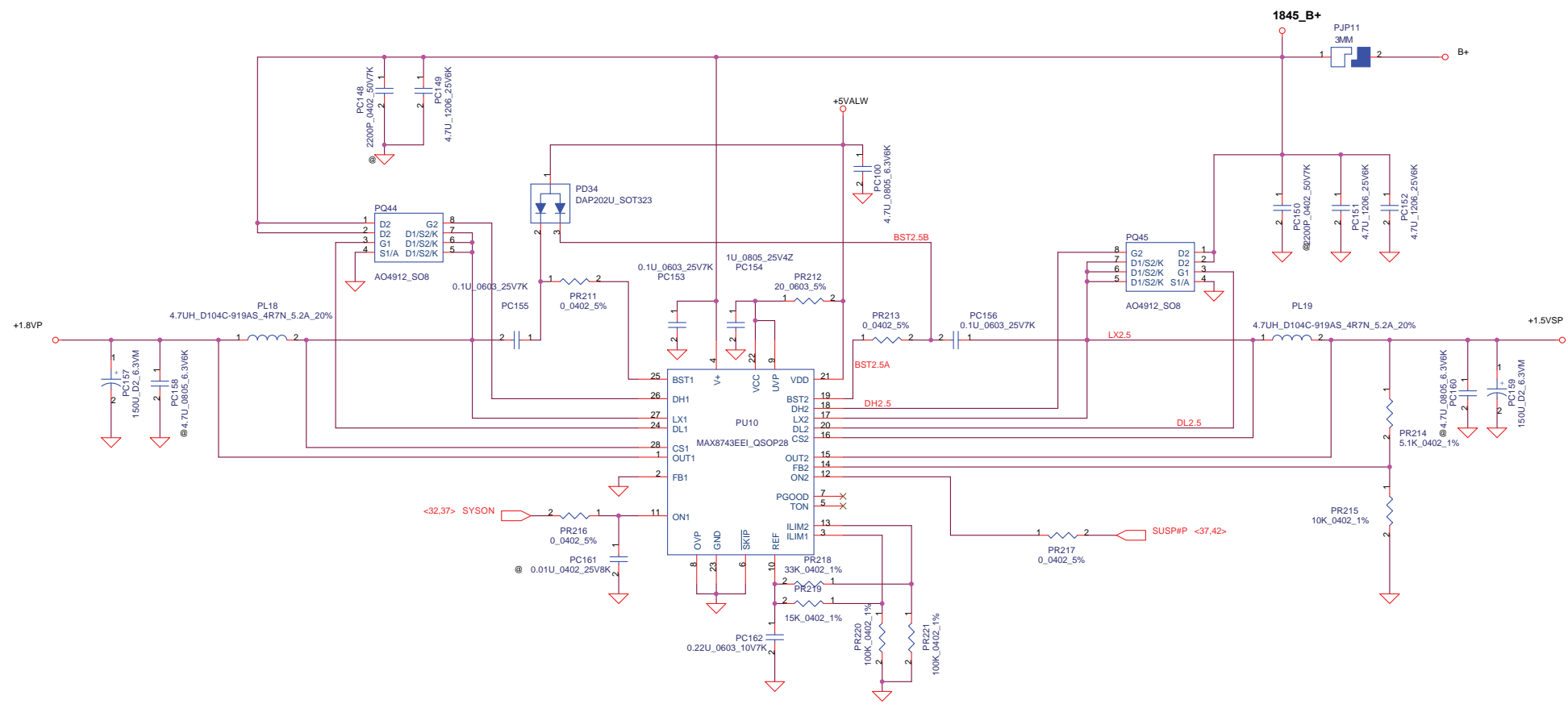
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COMPAL ELECTRONICS, INC

title **RTC batt & +1.2VP & OTP**

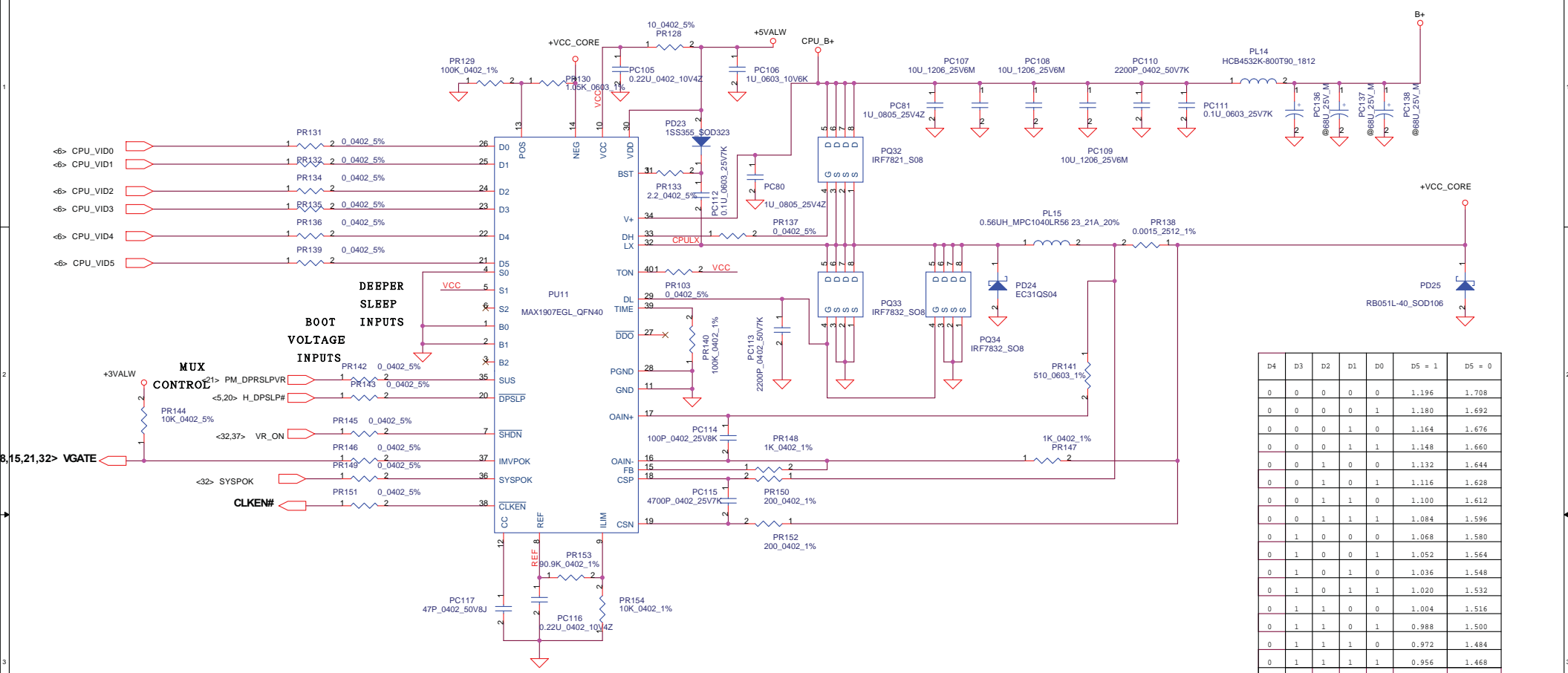
Size Document Number **EDX20 LA-2481** Rev **0.5**

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COMPAL ELECTRONICS, INC		
Title		
+1.5VSP & +1.8VP		
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Date: Tuesday, February 22, 2005		
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D4	D3	D2	D1	D0	D5 = 1	D5 = 0
0	0	0	0	0	1.196	1.708
0	0	0	0	1	1.180	1.692
0	0	0	1	0	1.164	1.676
0	0	0	1	1	1.148	1.660
0	0	1	0	0	1.132	1.644
0	0	1	0	1	1.116	1.628
0	0	1	1	0	1.100	1.612
0	0	1	1	1	1.084	1.596
0	1	0	0	0	1.068	1.580
0	1	0	0	1	1.052	1.564
0	1	0	1	0	1.036	1.548
0	1	0	1	1	1.020	1.532
0	1	1	0	0	1.004	1.516
0	1	1	0	1	0.988	1.500
0	1	1	1	0	0.972	1.484
0	1	1	1	1	0.956	1.468
1	0	0	0	0	0.940	1.452
1	0	0	0	1	0.924	1.436
1	0	0	1	0	0.908	1.420
1	0	0	1	1	0.892	1.404
1	0	1	0	0	0.876	1.388
1	0	1	0	1	0.860	1.372
1	0	1	1	0	0.844	1.356
1	0	1	1	1	0.828	1.340
1	1	0	0	0	0.812	1.324
1	1	0	0	1	0.796	1.308
1	1	0	1	0	0.780	1.292
1	1	0	1	1	0.764	1.276
1	1	1	0	0	0.748	1.260
1	1	1	0	1	0.732	1.244
1	1	1	1	0	0.716	1.228
1	1	1	1	1	0.700	1.212

$\Delta I = 0.0528A$ REF MAX = $2.01V * 10K / (10K + 90.2K) = 0.2005V$
 REF Min = $1.99V * 10K / (10K + 90.2K) = 0.1986V$
 Iimit Max = $0.2005V * 10 / 1.485m\Omega + 1/2 \Delta I = 13.528$
 Iimit Max = $0.1986V * 10 / 1.515m\Omega + 1/2 \Delta I = 13.135$

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1		Change FAN design	0.4	5	Change FAN circuit to PWM contrl		
2		Delete unused parts	0.4	7	Del C285		
3		Change CPU Ref Location name	0.4	5	Change CPU Ref location name from JP18 to U1		
4		Delete unused parts	0.4	17	Del R252,Del PID0 net on JP20 pin 26		
5		Design Change	0.4	21	Change PID0 net name to ICH_GPIO33 Add Q62(2N7002) to contrl ISOLATE# pin		
6		Design Change	0.4	27	Add net ISOLATE# on U39 pin23		
7		Delete SD card LED	0.4	24	Del D11,R377		
8	Save more power in S3 battery mode	Add LAN power control MOSFET	0.4	27	Add Q63(A03402),Q64(2N7002),R527(10K_0402),C575(0.01uF_0402)		
9		Add MOS on Docking USB_OVC pins	0.4	36	Add Q65,Q66,Q67 on USB_OVC#3, USB_OVC#4, USB_OVC#5		
10		ME change cable design to FFC	0.4	36	Swap JP27,JP22 pin assignment		
11		ME change cable design to FFC	0.4	30	Swap JP25		
12		decrease Audio Gain setting	0.4	30	Depop R245, Pop R243		
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1		Del MOS on Docking USB_OVC pins	0.5	36	Del Q65,Q66,Q67,Q68 on USB_OVC#3, USB_OVC#4, USB_OVC#5		
2		Add Docking USB_OVC circuit	0.5	33	Add U54,R533,534,R535,R536,R537,C576,C577,C578,C579		
3		Cost-Down	0.5	7	Del C252		
4		Design Change	0.5	31	Change USB Connector type		
5	External VGA display quality	Design Change	0.5	10	Change R36 to 220 ohm(EE Change List by Motion item 1)		
6	Support new version audio driver	Design Change	0.5	36	Change R1160 to 5.1K ohm(EE Change List by Motion item 2)		
7		Material Change	0.5	32	Change Y6 to KDS_SJ132P7KB10 part.(TXC EOL)		
8				5	Change CPU to C0 step		
9		Design Change	0.5	31	Change R14,R15 to 47 ohm		
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Add the pre-charge circuit.	Pre-charge function fail.	0.3	43	1.Add the Pre-charge circuit. Add the PD32,PR188,PR189,PR190,PR191,PR192,PR182,PD33,PC71,PC127,PC12,PR194,PR87,PR196,PQ35,PR198,PR199,PR197,PQ38	0.3	DVT
2	To adjust sequence for +5VALWP and +3VALWP.	To adjust sequence for +5VALWP and +3VALWP.	0.3	41	1.Delete PC59. 2.Change the PR122 from 100K to 0.	0.3	DVT
3	Chnage the power solution for +VCCP,+1.8VP and +1.5VSP.	Solve Digitizer issue.	0.3	42,44	1.Change the control IC of +1.5VALWP from FAN5234 to MAX8743. 2.Change the control IC of +1.8VP from ISL6227 to MAX8743. 3.Change the control IC of +VCCPP from ISL6227 to MAX8576.	0.3	DVT
4	Delete the circuit of 1.2VP.	Because H/W donot need.	0.3	43	1.Delete the PC100,PQ29,PR121,PR122,PC99,PC101,PR123,PR127,PQ30,PR158,PC102,PR125,PC103.	0.3	DVT
5	To adjust the input-current limit.	Change the input-cuurrent from 3A to 2.25A	0.3	39	1.Change the PR29 from 150K to 232K.	0.3	DVT
6	The jumping cursor when CPU_CORE heavy loading.	Improve Digitizer issue.	0.4	45	1.Change the PL15 form TOKIN .56UH to Panasoic .36UH.	0.4	DVT2
7	The system has shut down issue when swap battery.	The max1538 has some issue when sawp battery. So add the one shot circuit to improve the issue.	0.4	40,43	1.Add the 2n7002 on PQ22,PQ24,PQ25 and PQ26. 2. Add the 2K_0402_5% on PR93 and PR101. 3. Add the 3K_0402_5% on PR91 and PR92. 4.Add the 470K_0402_5% on PR86 and PR87. 5.Add the 100K_0402_5% on PR65. 6.Add the 47K_0402_1% on PR88. 7.Add the 499_0402_1% on PR89 and PR90. 8.Add the 1N4148 on PD17. 9.Add the .022U_0402_16V on PC73 and PC78. 10.Add the 100P_0402_50V on PC79.	0.4	DVT2
8	Battery drain issue when battery only on system off.	It did not turn off the +VCCP (1.05V) power no matter system was ON or OFF.Add pill down resistor.	0.4	42	1.Add the resistor on the PR199 and value is 100K_0402_5%.	0.4	DVT2
9	The customer request add the cap.	Improve Digitizer issue.	0.4	45	1.Add the 1U_0805_25V on PC80 and PC81.	0.4	DVT2
10	Disable Vin OVP function.	Disable Vin OVP function.	0.4	39	1.Delete the PD5 RLZ22B_LL34. 2.Delete the PD6 1SS355_SOT323.	0.4	DVT2
11.	Change Main battery connect.	For ME request.	0.4	39	1.Change the main battery from SUYIN_250263MR007G102ZL to SUYIN_250263MR007G110ZR.	0.4	DVT2
12.	Because the FDS4935A will phase out.	Because the FDS4935A will phase out.	0.4	40	1.Change the main battery from SUYIN_250263MR007G102ZL to SUYIN_250263MR007G110ZR.	0.4	DVT2

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