

EL8 Block Diagram

VCC_CORE

GMCH_CORE

VCC1.1
VCC1.2
VCC1.5
1.5VSUS

VCC3
3V_STBY

VCC5
5V_STBY
+12V

Intel
Yorkfield/Wolfdale
Q9000/E8000
LGA775

Page 3,4

CLOCK GENERATOR
CK505
CV193

Page 2

NB
Eaglelake
G45/P43
1254 pin

Page 5,7,8,9

CH A: DDRIII-UDIMMO/1
CH B: DDRIII-UDIMMO/1

Page 14,15,16,17

SATA - HDD(2.5) SATA 4
SATA - HDD(3.5) SATA 1
SATA - ODD SATA 2
eSATA SATA 3

Page 22

USB-10 USB 2.0
WLAN USB-10
Camera USB-1
Bluetooth USB-2
USB*4(Rear) USB-6,7,8,9
TV USB-11
USB*2(Side) USB-3,5
Touch Screen USB-0

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SB
ICH10
676 pin

Page 10,11,12,13

MXM CONNECTOR

Page 18

LCD PANEL
23" Full HD

LVDS Transmitter
CH7308B

Page 19

BT KB/Mouse

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PCI-Express 1X

PCI-E-2 MINI CARD-1 WLAN
PCI-E-3 MINI CARD-2 TV card
PCI-E-1 LAN RTL8111DL
PCI-E-4 Card Reader JMB385

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WLAN antenna
TV antenna
RJ45
Media Slot

HP
MIC IN
INT SPK
DMIC IN

Page 30
Page 30
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Page 30

AUDIO CODEC
ALC888S-VC2

Page 29

LINE IN
5.1 Channel

LPC

ITE8512

Page 26

IR Blaster
FAN
FLASH ROM
CIR

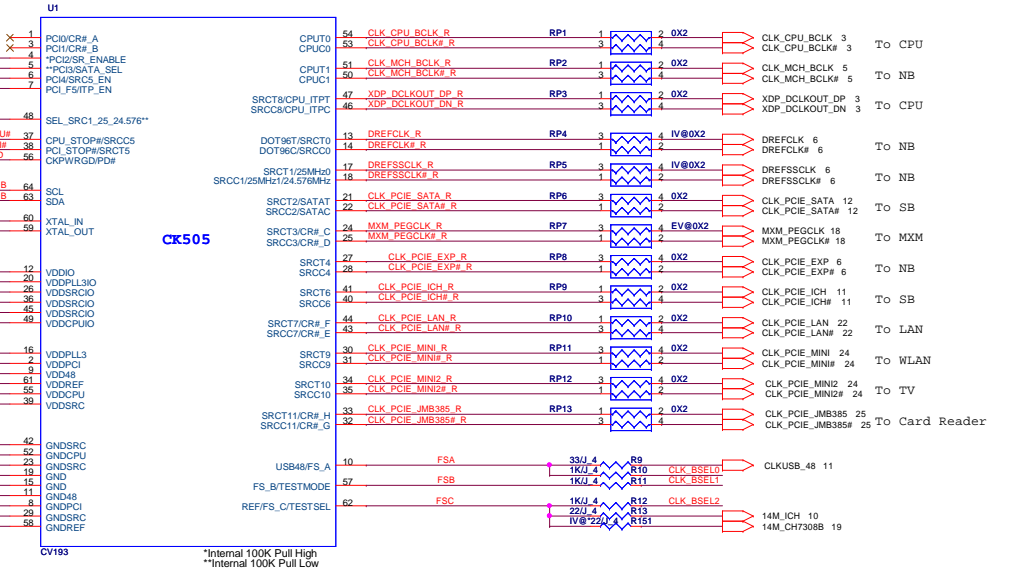
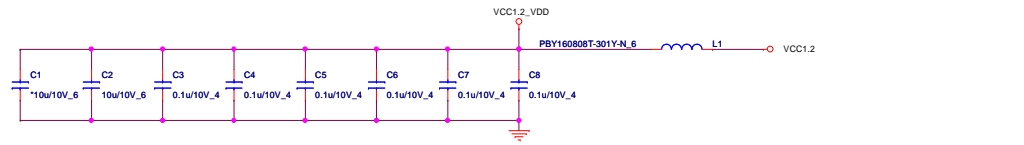
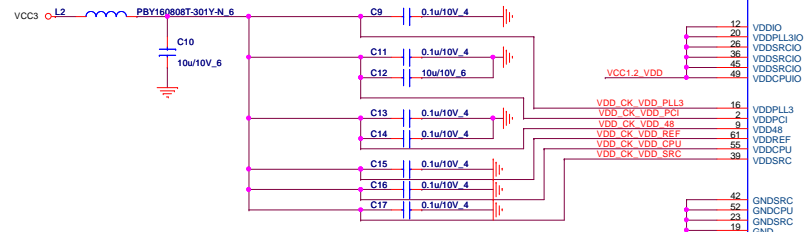
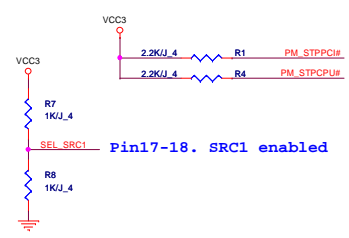
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32.768KHz

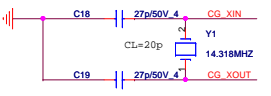
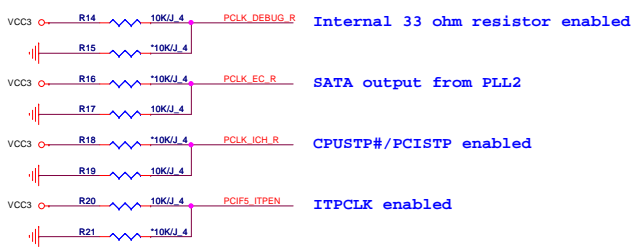
Daughter Board

MXM module 314 pin
B-CAS board 10 pin
Card Reader 20 pin
HP/MIC Light SW 10 pin
Power button LED TBD

Clock Generator



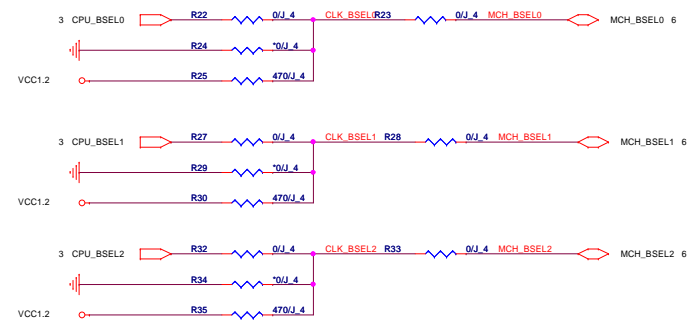
Strap Configuration



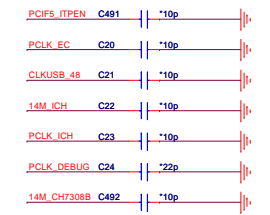
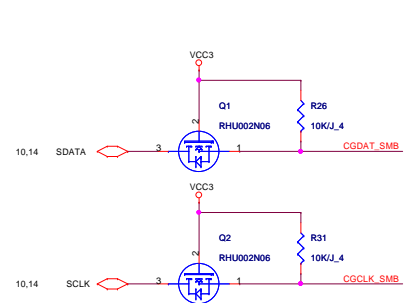
FREQ. SEL TABLE

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved

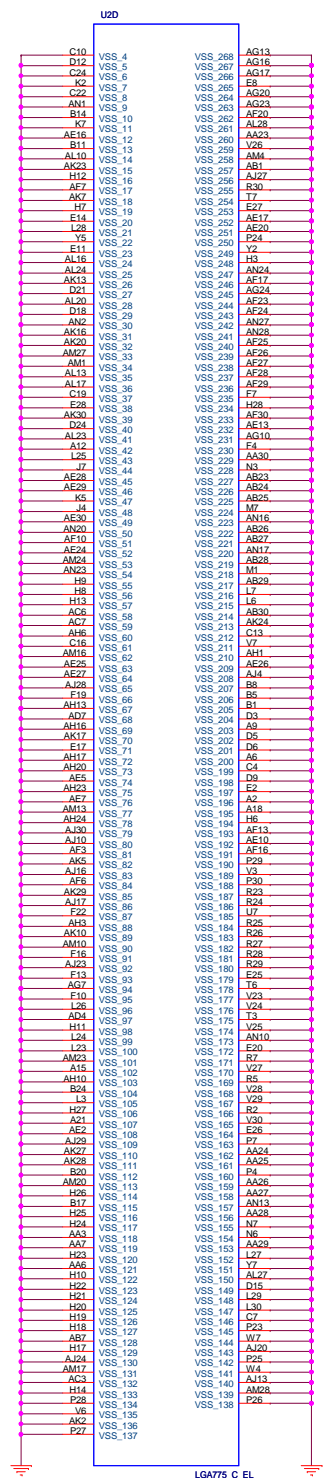


Clock Gen I2C

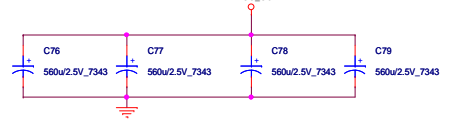
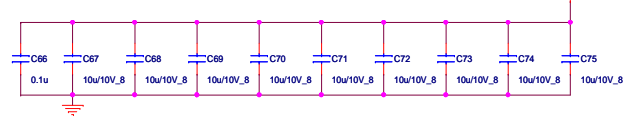
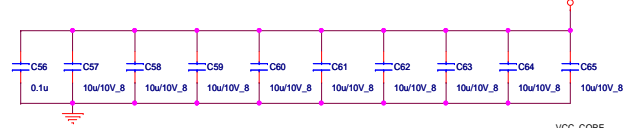
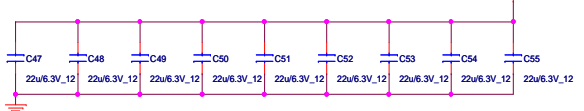
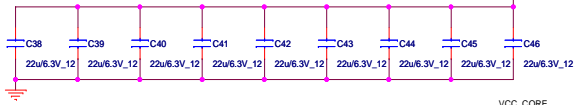


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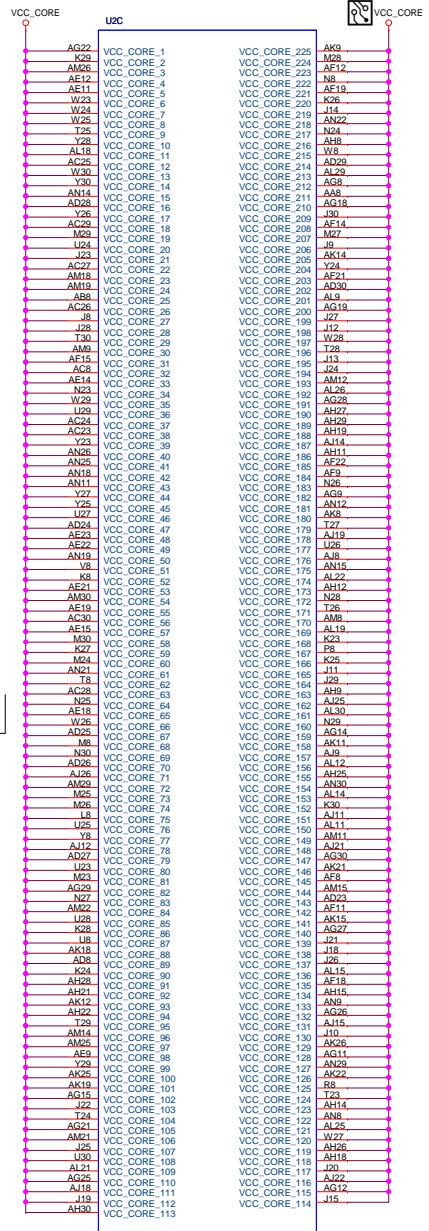
Size: Document Number: **CLK_GEN / CK505** Rev: 1A
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Place these parts reference to Intel demo board.

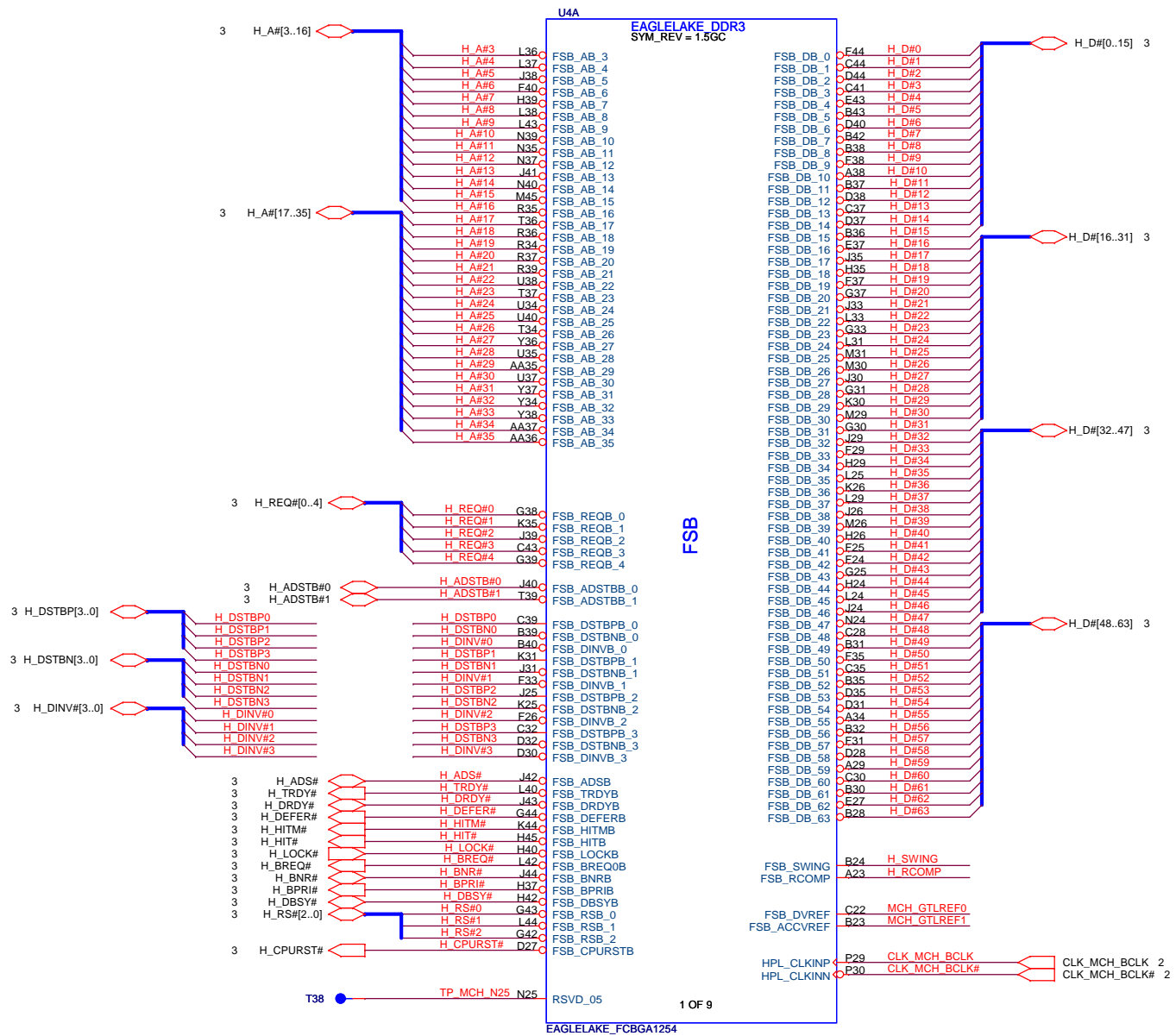
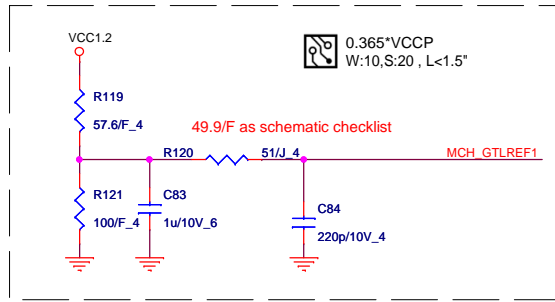
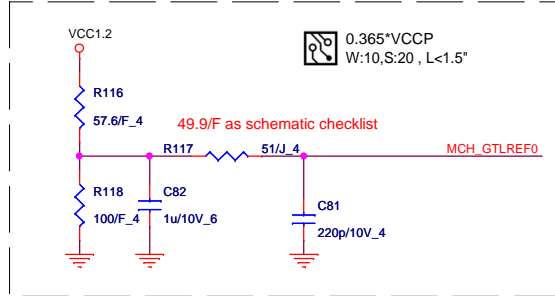
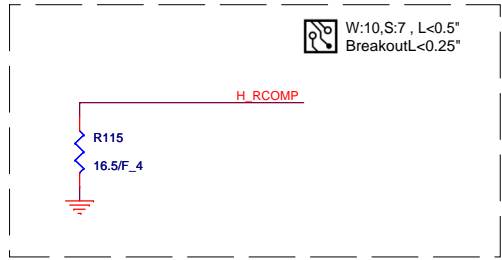
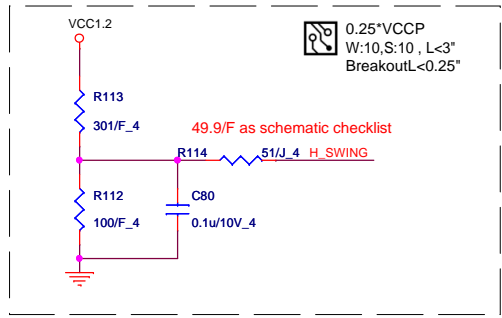


VCC_CORE Bulk CAPs place to BOT of CPU central



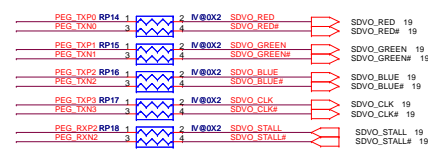
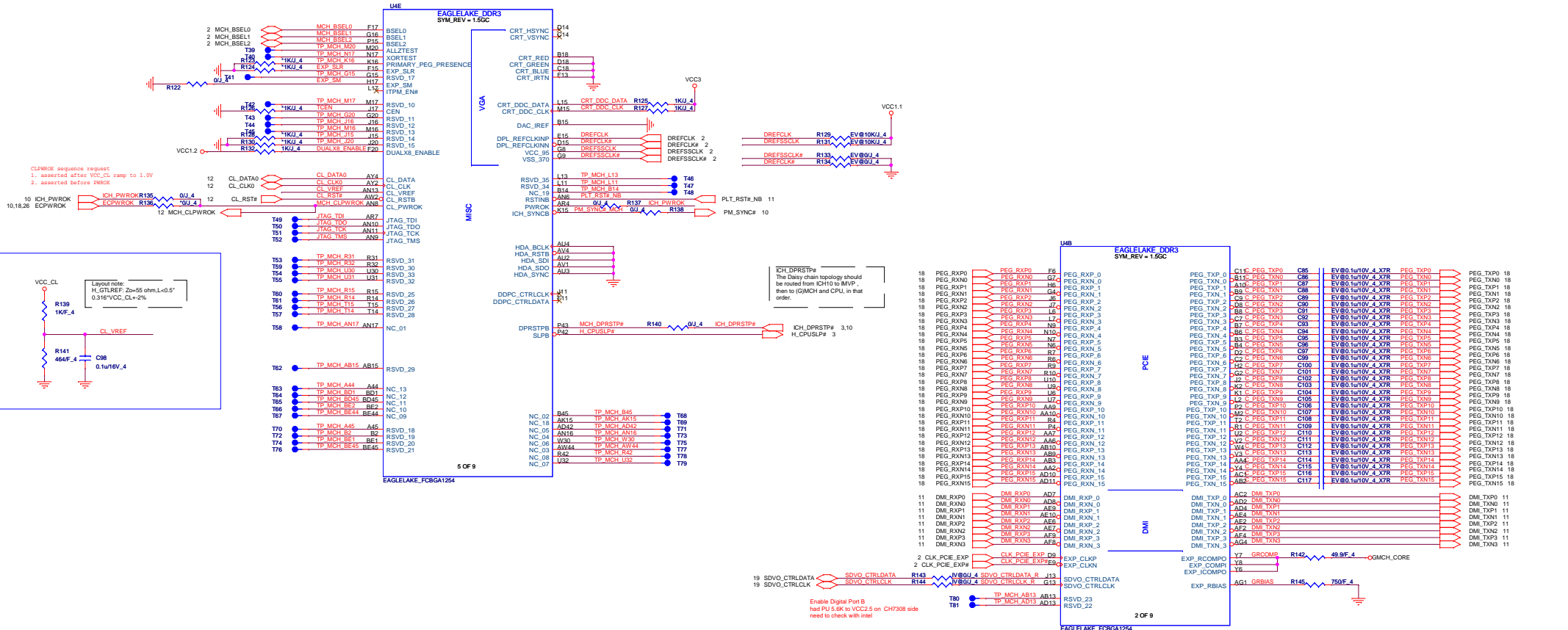
Yorkfield/Wolfdale CPU Power Status and max current table

POWER PLANE	So	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	100A	Yorkfield@65W
VCC_CORE	O	X	X	VID	75A	Wolfdale
VTT	O	X	X	VCC1.2	8A	After VCC stable
VTT	O	X	X	VCC1.2	7A	Before VCC stable
VCC_PLL	O	X	X	VCC1.5	260mA	



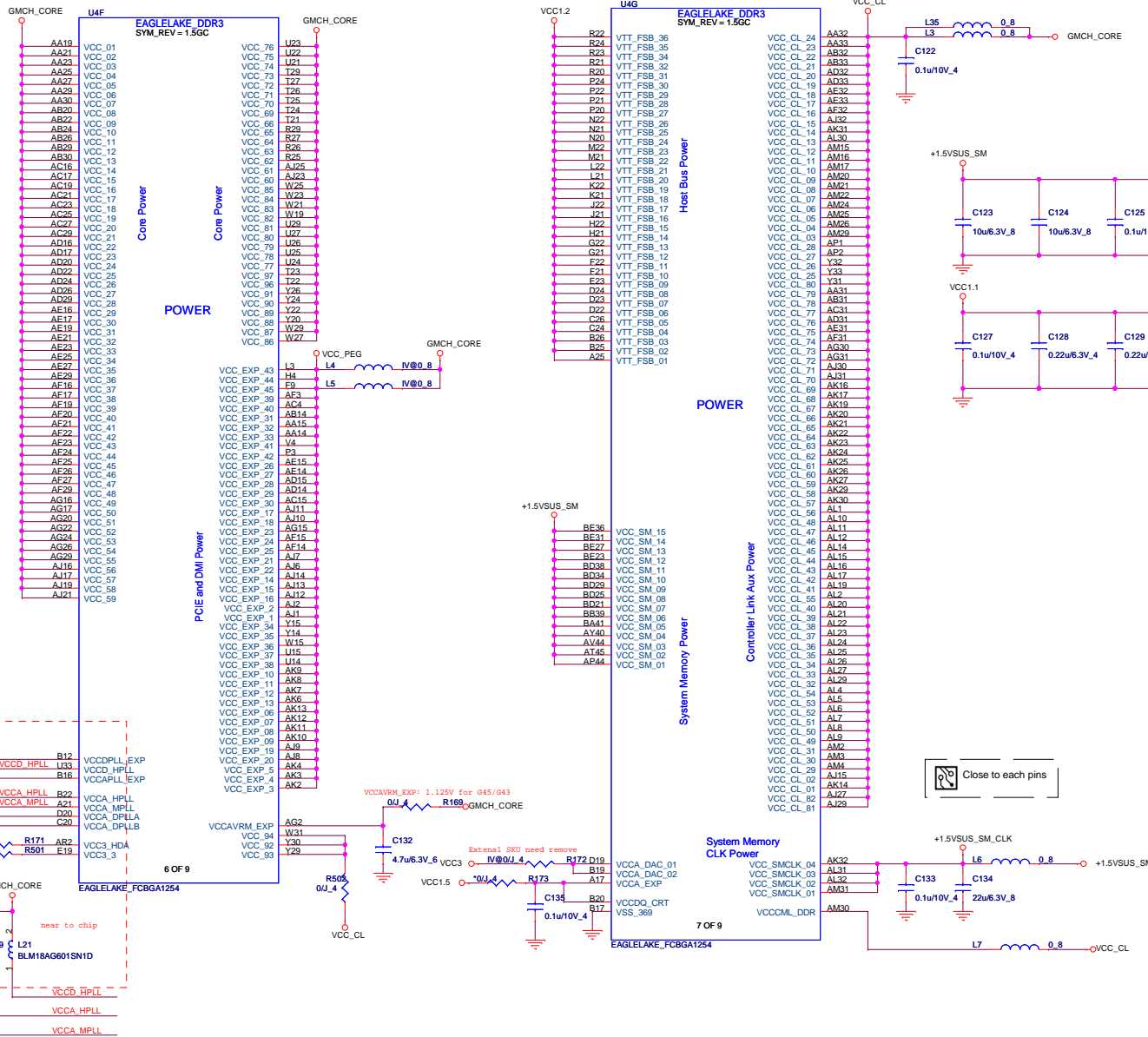
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Size	Document Number	Rev
	NB (2/5)-VGA, DMI, PCIE	1A
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SKU	G45	P43
GMCH_CORE	1.125V	1.1V

NB Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_SM	O	O	X	1.5VSUS	1963mA	
VCC_SMCLK	O	O	X	1.5VSUS	288mA	
VCC_EXP	O	X	X	GMCH_CORE	3082mA	SDVO, PCIE, DMI
VCCA_EXP	O	X	X	VCC1.5	6mA	SDVO, PCIE Analog
VTT_FSB	O	X	X	VCC1.2	914mA	
VCC	O	X	X	GMCH_CORE	17984mA	
VCC_CL	O	X	X	GMCH_CORE	4666mA	
VCC3_3	O	X	X	VCC3	14mA	
VCCA_DAC	O	X	X	VCC3	74mA	
VCCDO_CRT	O	X	X	VCC1.5	0mA	
VCCAPLL_EXP	O	X	X	VCC1.1	20mA	
VCCDLL_EXP	O	X	X	VCC1.1	X	
VCCA_DPLL	O	X	X	VCC1.1	59mA	
VCCA_DPLL	O	X	X	VCC1.1	59mA	
VCCA_HPLL	O	X	X	VCC1.1	31mA	
VCCD_HPLL	O	X	X	VCC1.1	X	
VCCA_MPLL	O	X	X	VCC1.1	83mA	

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EAGLELAKE_DDR3

W17	VSS_331	VSS_001
FEA	VSS_219	AI2
BA23	VSS_330	AU22
W16	VSS_181	BD43
A20	VSS_090	AI24
W1	VSS_179	BA5
AH4	VSS_269	AI26
UR	VSS_328	AI9
BS3	VSS_088	BD21
BS3	VSS_178	BD25
B44	VSS_004	AI36
B27	VSS_377	AI38
AH2	VSS_087	AI39
FEA	VSS_176	AI39
U38	VSS_086	AI44
AG45	VSS_085	AI44
R10	VSS_175	AI44
U20	VSS_325	AI45
U20	VSS_024	AI45
AV48	VSS_084	AI46
AG27	VSS_084	AI46
AC30	VSS_173	AI46
AC30	VSS_083	AI46
U17	VSS_323	AI46
A23	VSS_172	AI46
A23	VSS_081	AI46
AV21	VSS_321	AI46
U16	VSS_077	AI46
AG19	VSS_080	AI46
U13	VSS_320	AI46
AV1	VSS_170	AI46
AF7	VSS_076	AI46
AY15	VSS_169	AI46
U12	VSS_319	AI46
U12	VSS_075	AI46
AF4	VSS_078	AI46
AV1	VSS_318	AI46
AF30	VSS_167	AI46
AW30	VSS_077	AI46
L16	VSS_258	AI46
AV3	VSS_257	AI46
AF33	VSS_076	AI46
AW25	VSS_256	AI46
K45	VSS_255	AI46
AW24	VSS_164	AI46
AW24	VSS_074	AI46
AG3	VSS_254	AI46
AW22	VSS_254	AI46
AF12	VSS_073	AI46
AW20	VSS_162	AI46
K24	VSS_253	AI46
K24	VSS_072	AI46
AW17	VSS_161	AI46
AF10	VSS_071	AI46
AF10	VSS_250	AI46
AW11	VSS_070	AI46
AE4	VSS_159	AI46
AE4	VSS_069	AI46
K13	VSS_068	AI46
AE40	VSS_158	AI46
AV8	VSS_158	AI46
AV5	VSS_157	AI46
AE38	VSS_248	AI46
AE34	VSS_067	AI46
AV38	VSS_156	AI46
AV23	VSS_247	AI46
AV8	VSS_155	AI46
AE26	VSS_066	AI46
AV30	VSS_154	AI46
AC45	VSS_064	AI46
J4	VSS_245	AI46
AV21	VSS_153	AI46
AE22	VSS_063	AI46
AV2	VSS_062	AI46
AV2	VSS_243	AI46
AV16	VSS_151	AI46
AE13	VSS_061	AI46
AE12	VSS_242	AI46
H8	VSS_241	AI46
AV15	VSS_150	AI46
AV11	VSS_059	AI46
AV13	VSS_149	AI46
H8	VSS_239	AI46
H7	VSS_238	AI46
AV11	VSS_148	AI46
AV11	VSS_058	AI46
AV9	VSS_147	AI46
H44	VSS_057	AI46
AD9	VSS_056	AI46
AV6	VSS_146	AI46
AV5	VSS_237	AI46
AD39	VSS_055	AI46
H33	VSS_236	AI46
H31	VSS_144	AI46
AD36	VSS_235	AI46
H30	VSS_234	AI46
AD3	VSS_053	AI46
AV25	VSS_142	AI46
H25	VSS_233	AI46
AD27	VSS_141	AI46
AD27	VSS_232	AI46
AD25	VSS_050	AI46
U20	VSS_140	AI46
AT35	VSS_231	AI46
AD23	VSS_049	AI46
H13	VSS_229	AI46
AD21	VSS_138	AI46
AT24	VSS_137	AI46
H11	VSS_228	AI46
AD19	VSS_047	AI46
AV17	VSS_136	AI46

GND

U4H
EAGLELAKE_FCBGA1254
SYM_REF = 1.5GC
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U4H

EAGLELAKE_DDR3
SYM_REF = 1.5GC

N16	VSS_272	VSS_273	N26
N13	VSS_271	VSS_274	N29
F1	VSS_362	VSS_275	N30
N11	VSS_270	VSS_276	N33
C45	VSS_363	VSS_277	N36
C1	VSS_364	VSS_278	N38
M44	VSS_269	VSS_279	N8
M25	VSS_268	VSS_280	P16
BE43	VSS_356	VSS_281	P17
M24	VSS_267	VSS_282	P26
BE3	VSS_357	VSS_283	P26
BD44	VSS_358	VSS_284	P31
M1	VSS_266	VSS_285	R11
BD2	VSS_359	VSS_286	R12
L9	VSS_265	VSS_287	R16
BC45	VSS_360	VSS_288	R16
L8	VSS_264	VSS_289	R17
BC1	VSS_361	VSS_290	R2
L4	VSS_263	VSS_291	R30
L39	VSS_262	VSS_292	R38
B44	VSS_365	VSS_293	R38
A6	VSS_367	VSS_294	R45
L35	VSS_261	VSS_295	R5
A43	VSS_366	VSS_296	R8
L30	VSS_260	VSS_297	T10
A3	VSS_368	VSS_298	T11
L26	VSS_259	VSS_299	T12
Y9	VSS_355	VSS_300	T13
Y39	VSS_354	VSS_301	T16
Y35	VSS_353	VSS_302	T17
Y3	VSS_352	VSS_303	T19
Y27	VSS_351	VSS_304	T20
Y25	VSS_350	VSS_305	T3
Y23	VSS_349	VSS_306	T30
Y21	VSS_348	VSS_307	T31
Y2	VSS_347	VSS_308	T32
Y19	VSS_346	VSS_309	T33
Y17	VSS_345	VSS_310	T35
Y16	VSS_344	VSS_311	T38
Y12	VSS_343	VSS_312	T4
Y11	VSS_342	VSS_313	T40
Y10	VSS_340	VSS_314	T6
W45	VSS_339	VSS_315	T7
W44	VSS_338	VSS_316	T8
W26	VSS_337	VSS_317	T9
W24	VSS_336	VSS_318	U1
	VSS_335	VSS_334	W2
			W20
			W22

GND

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EAGLELAKE_FCBGA1254

NC_14	AD30
NC_15	AC30
NC_16	AF30
NC_17	AE30

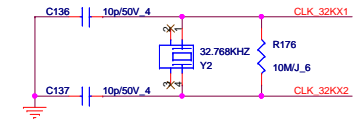


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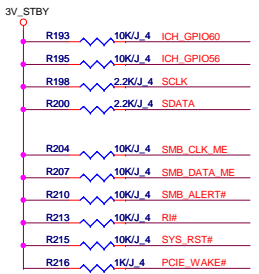
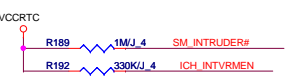
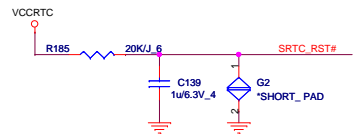
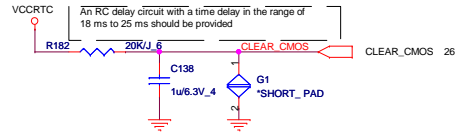
Size	Document Number	Rev
	NB (5/5)- VSS	1A

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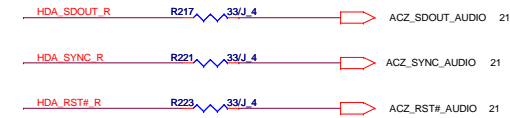
RTC CRYSTAL



RESET JUMP

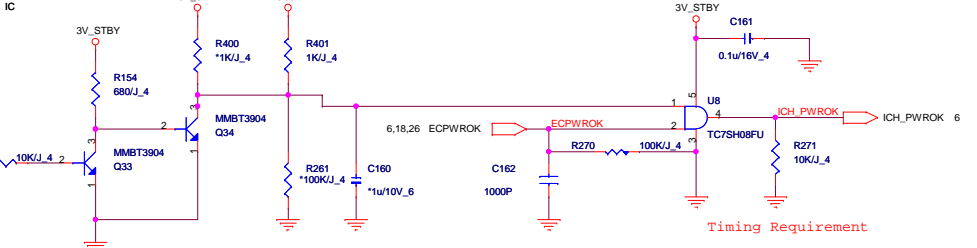
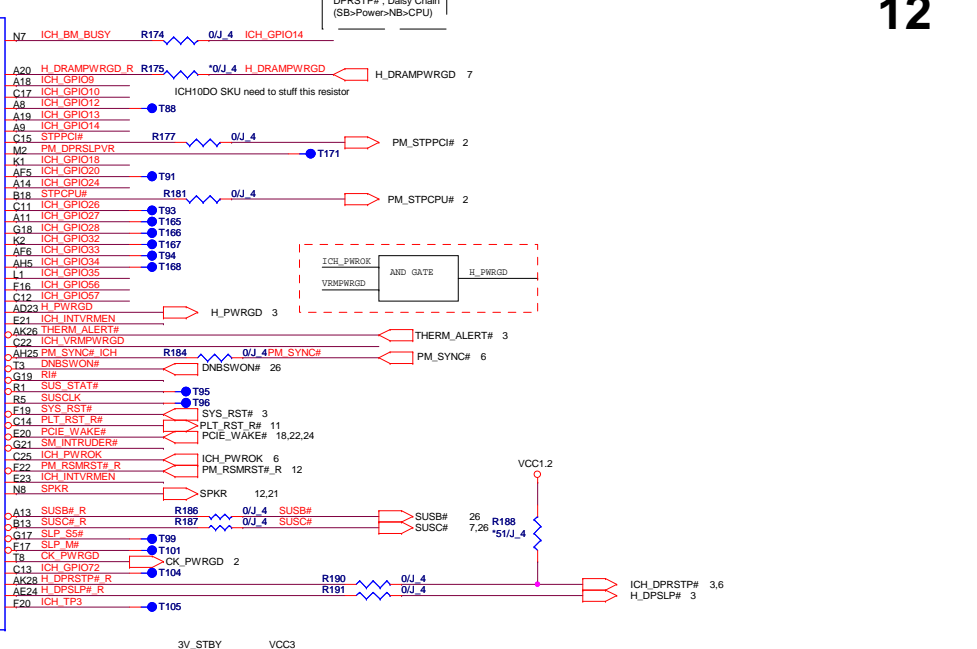
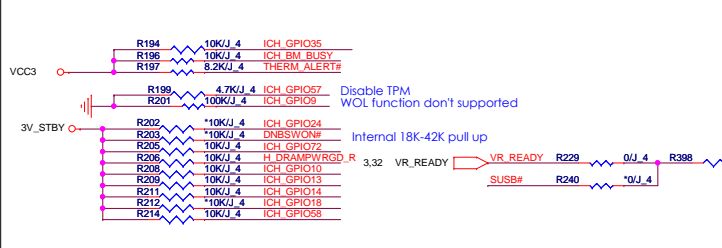
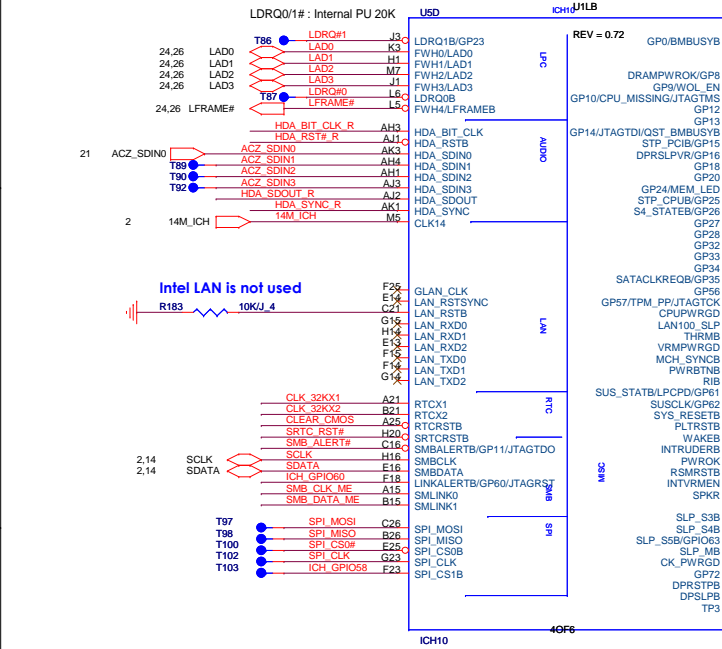


HD Audio I/F(CODEC& IHDMI)

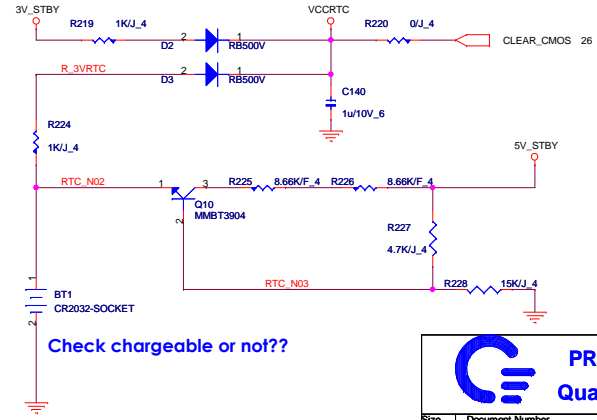


South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PUP/PD	
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.	
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU		
TP3	XOR Chain Entrance	PWROK	ICH_TP3	RSVD	ICH_TP3 R230 1KJ_4
			HDA_SDOUT	Description	Enter XOR Chain
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	Normal operation(Default)	HDA_SDOUT_R R231 3.3KJ_4
			1	Set PCIe port config bit 1	



RTC BATTERY

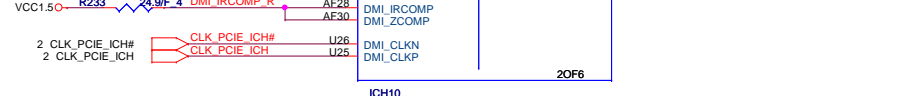
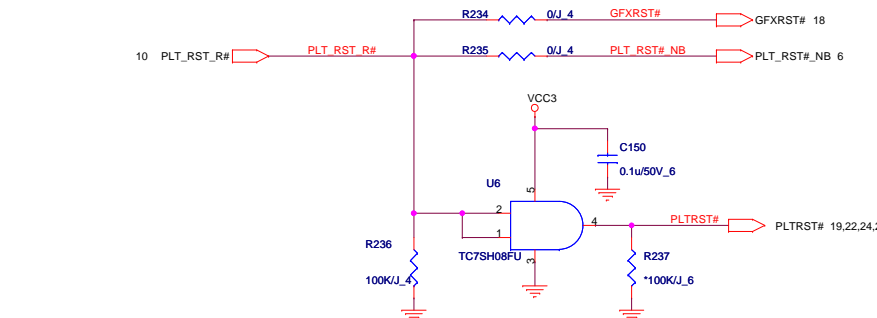
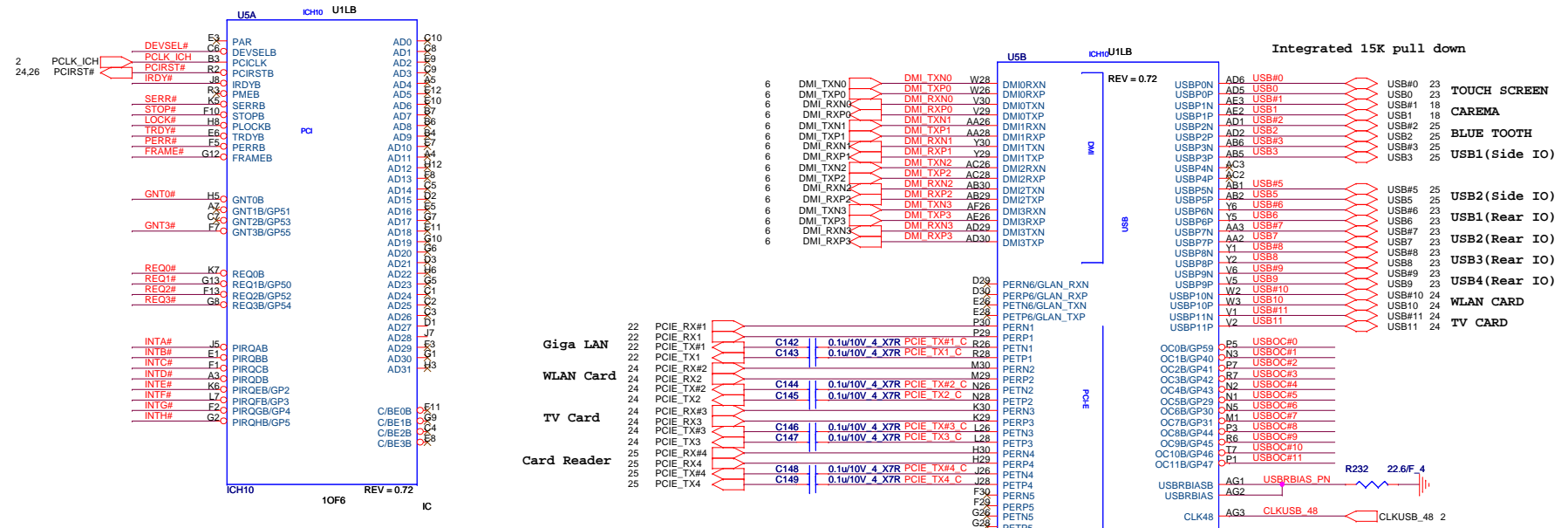


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Size: Document Number
SB (1/4)- HOST

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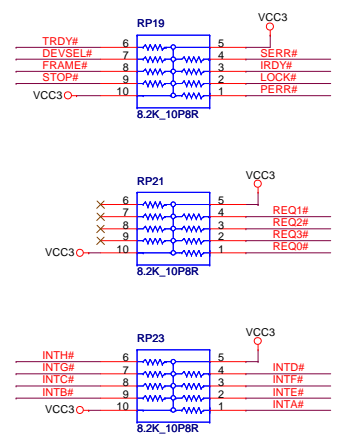
PCI/PCI-E/USB/DMI/SPI



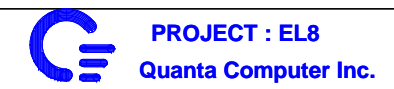
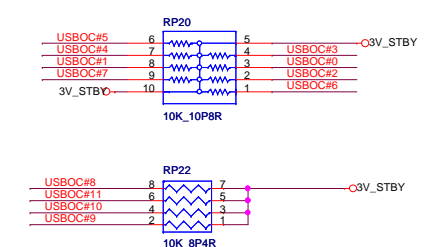
South Bridge Strap Pin (2/3)

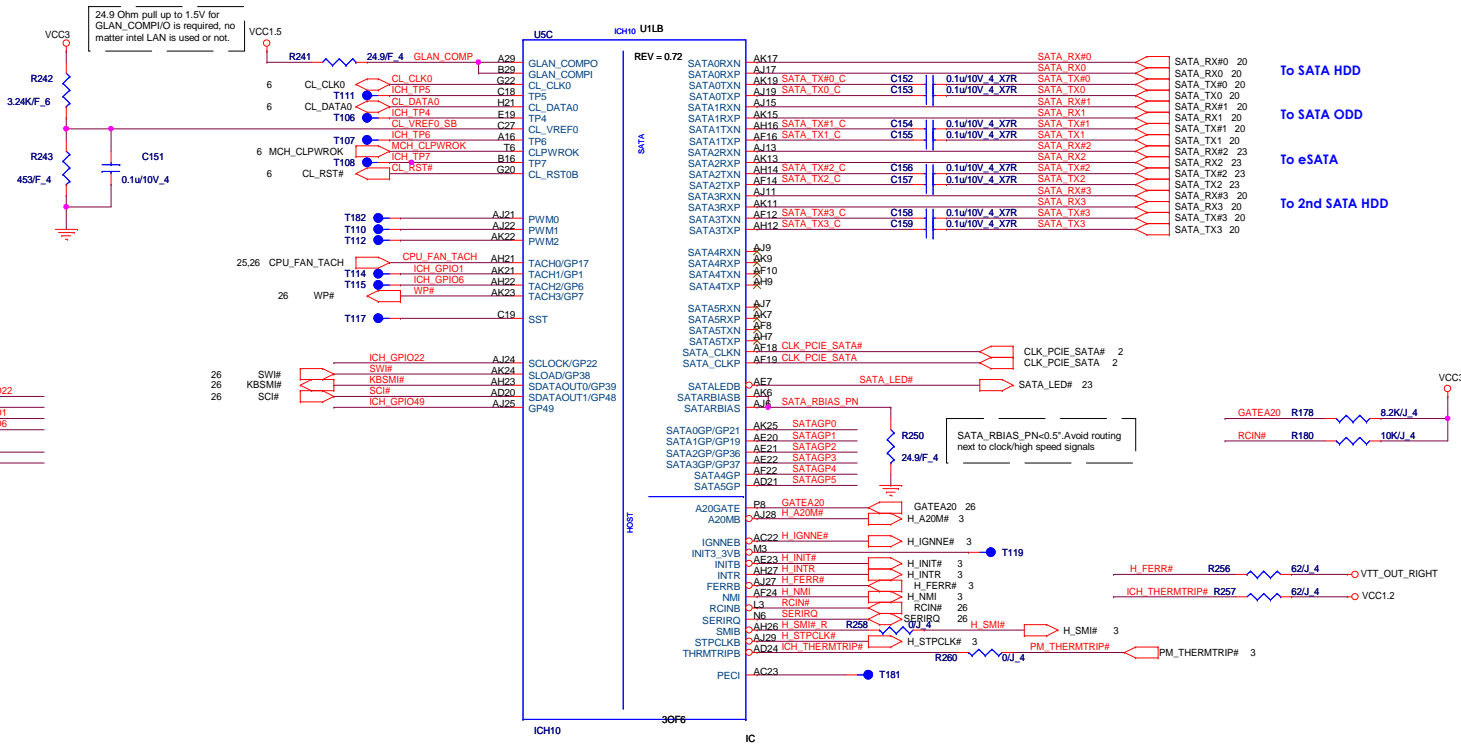
Pin Name	Strap description	Sampled	Configuration	PU/PD									
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0										
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default										
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R238 *1K/J_4									
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>0</td> <td>1</td> <td>SPI(Default)</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI(Default)	GNT0# R239 *1K/J_4			
PCI_GNT#0	SPI_CS#1	Boot Location											
0	1	SPI(Default)											
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>LPC</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	1	0	PCI	1	1	LPC	
PCI_GNT#0	SPI_CS#1	Boot Location											
1	0	PCI											
1	1	LPC											

PCI PULL-UP

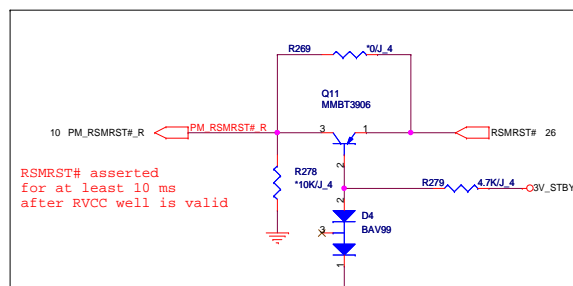
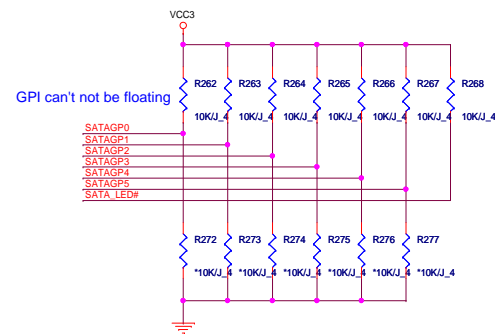


USBOC# PULL-UP





To SATA HDD
To SATA ODD
To eSATA
To 2nd SATA HDD



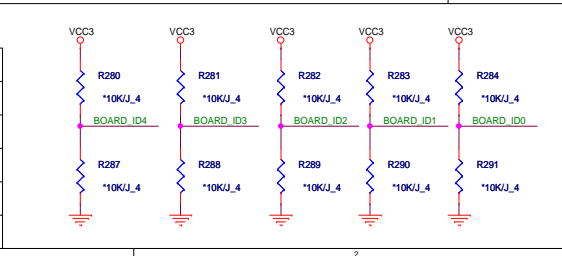
South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode 10,21	SPKR SPKR R286 10KJ_4 VCC3
GPIO49	DMI Termination Voltage	PWROK	0 = AC coupled 1 = DC coupled Internal PU	ICH_GPIO49 R292 10KJ_4

Board ID Table

BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV

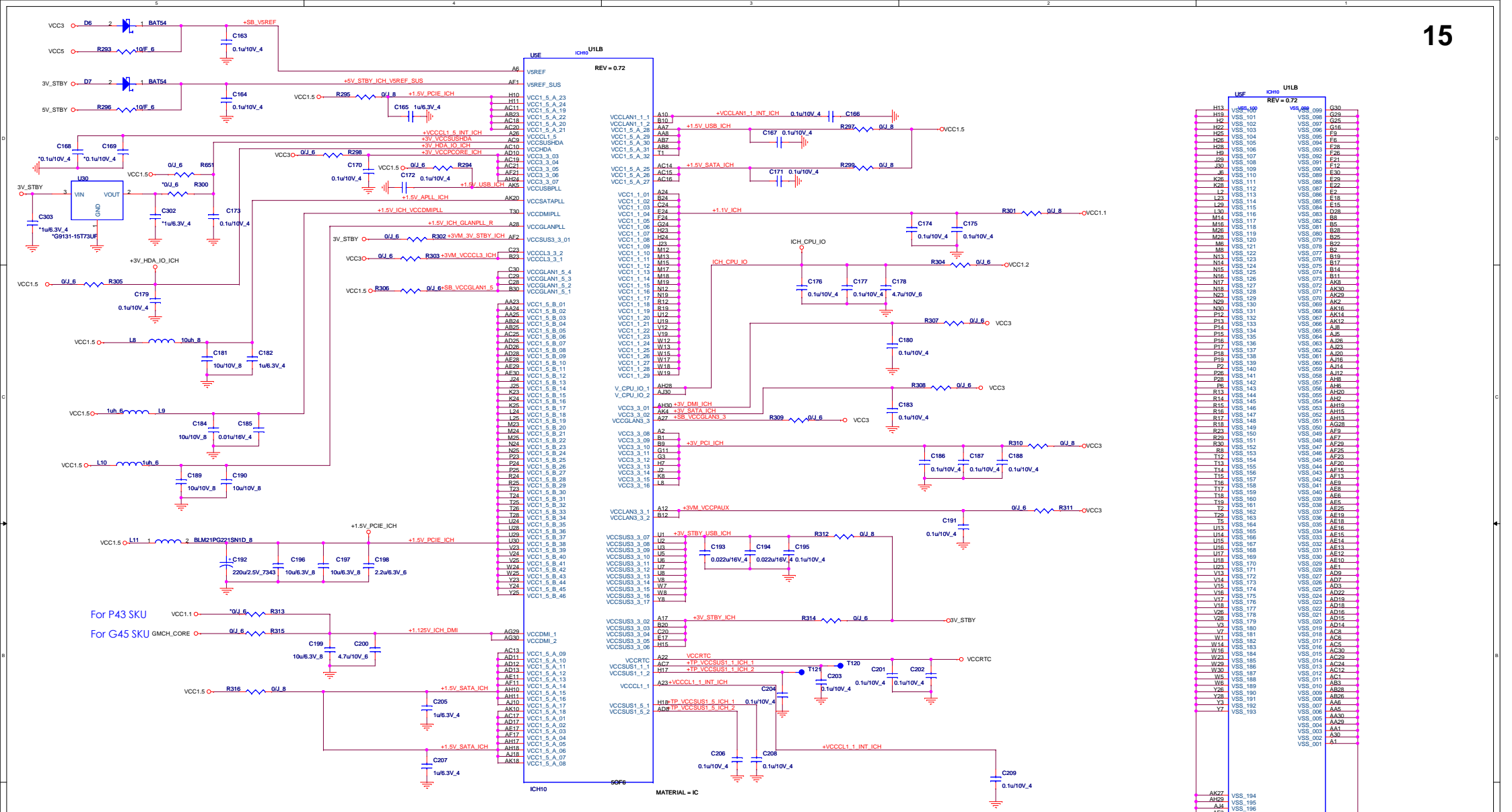
Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H
CCFL Panel LED Panel				H	L
W/ G-SENSOR W/O G-SENSOR			H	L	
W/ TV W/O TV		H	L		
W/ HDMI W/O HDMI	H	L			



PROJECT : EL8
Quanta Computer Inc.

Size Document Number Rev 1A
SB(3/4) SATA/GPIO

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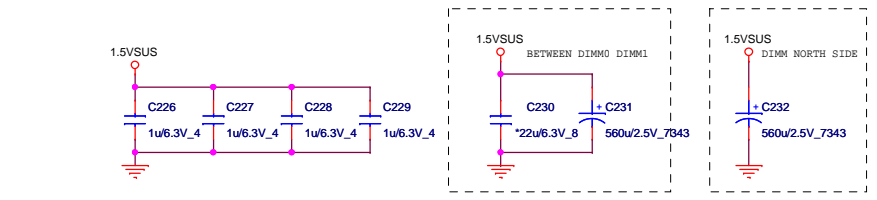
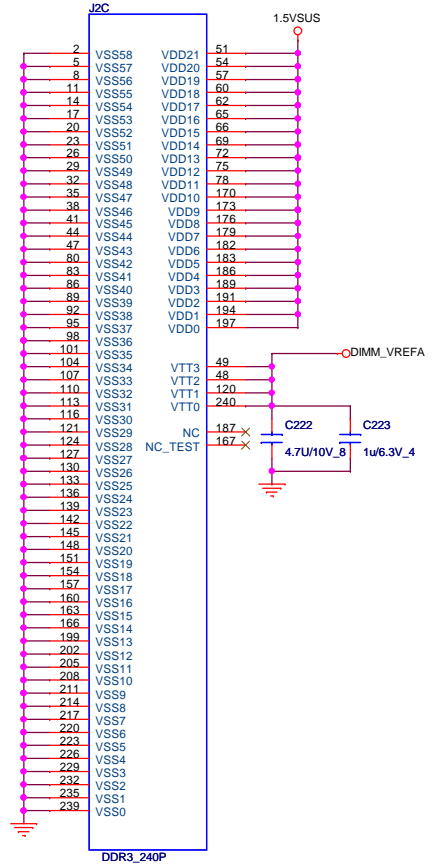
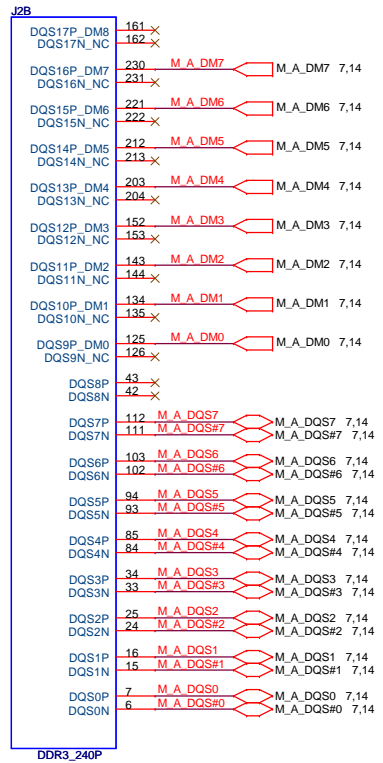
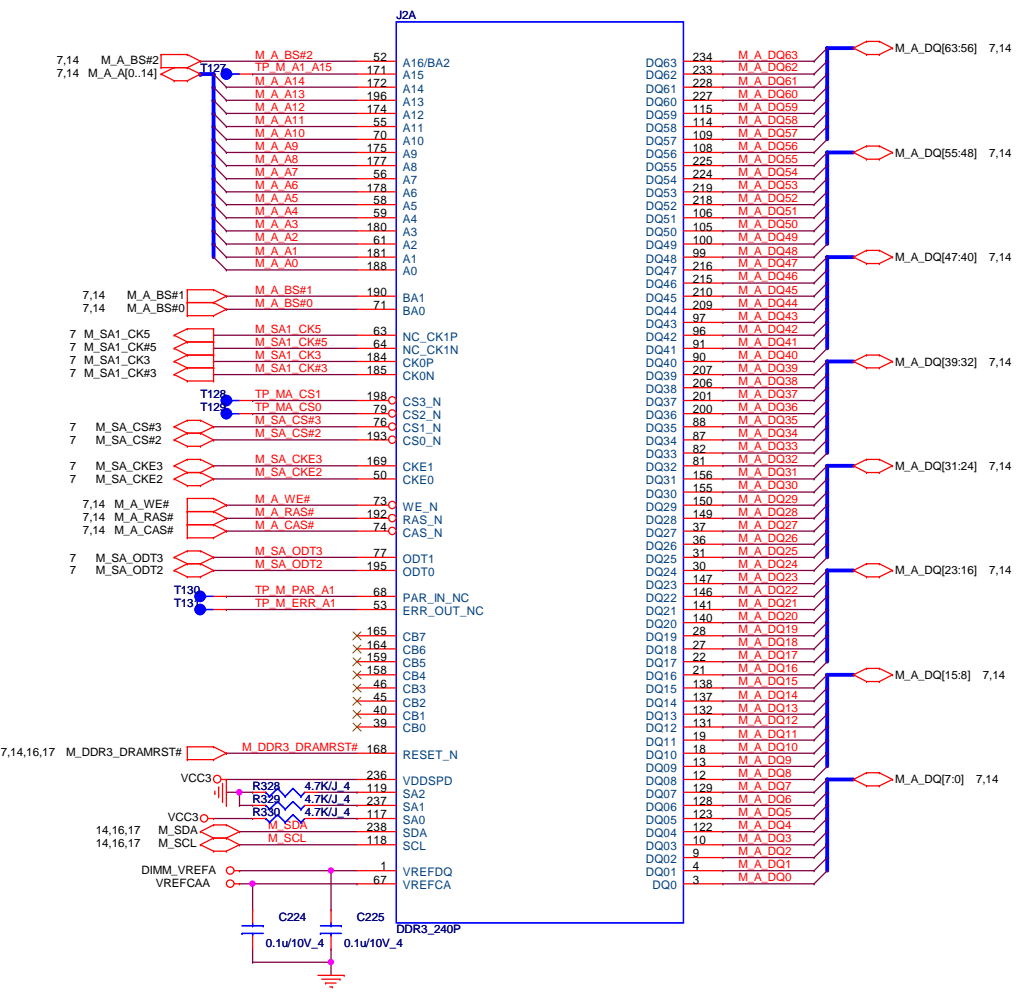
For P43 SKU
For G45 SKU

SB Power Status and max current table [1/2]

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	VCCRTC	6uA	6uA@G3
VSREF	O	X	X	VCC5	2mA	
VSREF_SUS	O	O	O	5V_STBY	2mA	2mA@S0,1mA@S3/S5
VCC1_5_B	O	X	X	VCC1.5	646mA	
VCCSATAPLL	O	X	X	VCC1.5	47mA	
VCC1_5_A	O	X	X	VCC1.5	1644mA	
VCCUSBPLL	O	X	X	VCC1.5	11mA	
VCCLAN1_1	X	X	X	1.1V	X	Internal VR powered, S3/S5 powered when AMT activated
VCCLAN3_3	O	X	X	VCC3	78mA	78mA@S3/S5 powered when AMT activated
VCCGLANPLL	O	X	X	VCC1.5	23mA	
VCCGLAN1_5	O	X	X	VCC1.5	80mA	
VCCGLAN3_3	O	X	X	VCC3	1mA	

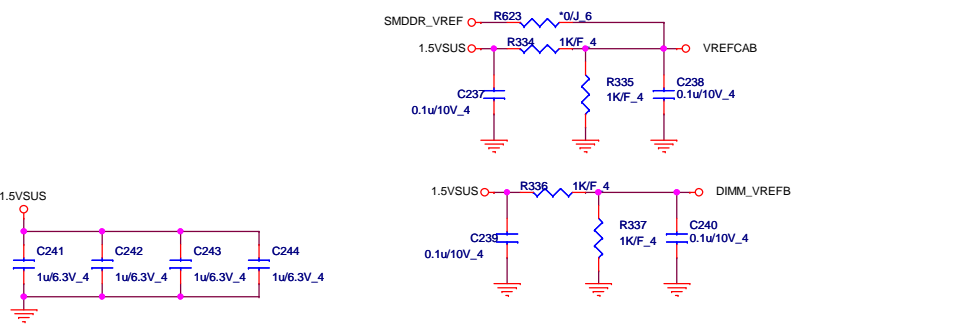
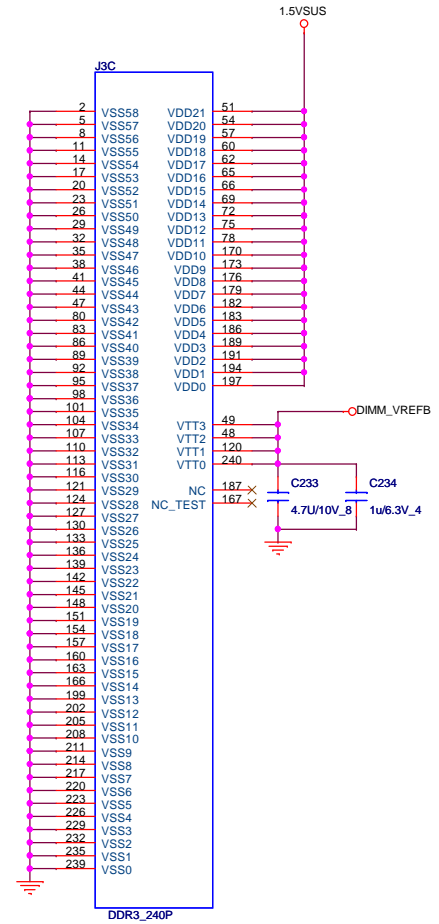
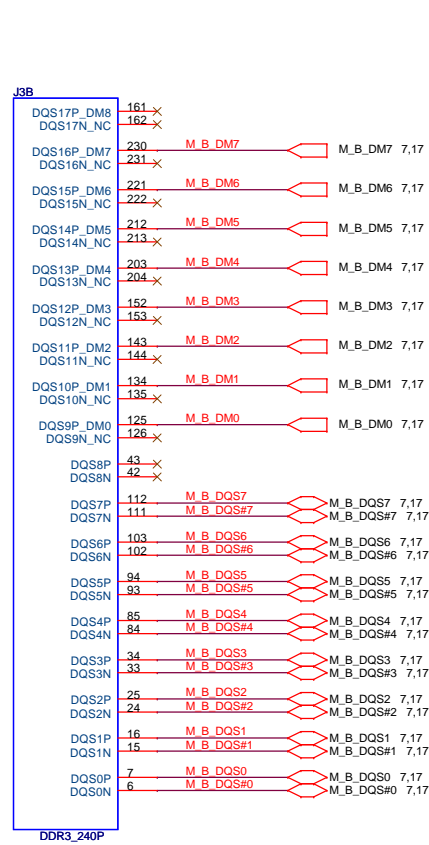
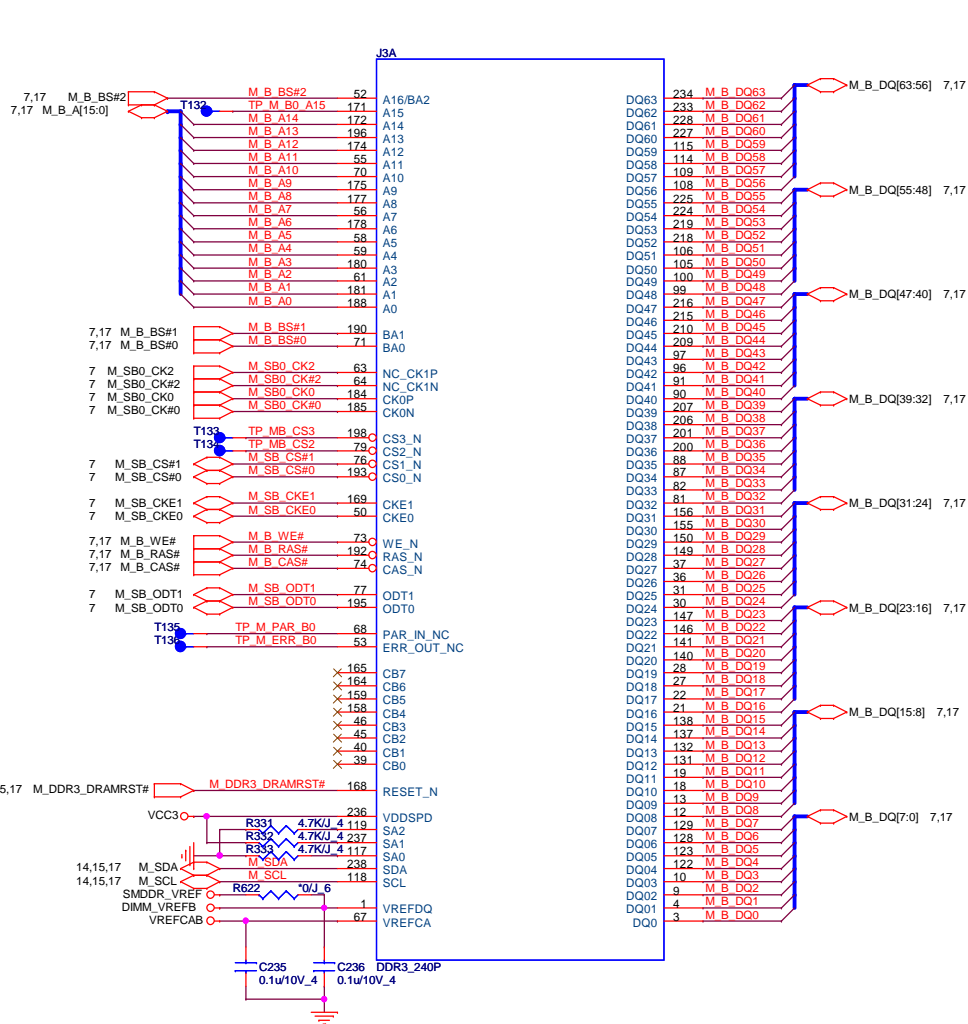
SB Power Status and max current table [2/2]

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_1	O	X	X	VCC1.1	1.634A	ICH CORE
VCCDMPPLL	O	X	X	VCC1.5	23mA	
VCC_DMI	O	X	X	GMCH_CORE	50mA	1.125V@G45, 1.1V@P43
V_CPU_IO	O	X	X	VCC1.2	2mA	
VCC3_3	O	X	X	VCC3	308mA	
VCCCHA	O	X	X	VCC1.5	70mA	
VCCSUSHDA	O	O	O	RVCC1.5	70mA	
VCCSUS1_1	X	X	X	1.1V	X	Internal VR powered
VCCSUS1_5	X	X	X	1.5V	X	Internal VR powered
VCCSUS3_3	O	O	O	3V_STBY	212mA	S3mA@S3/S5
VCCCL1_1	X	X	X	1.1V	X	Internal VR powered
VCCCL1_5	X	X	X	1.5V	X	Internal VR powered
VCCCL3_3	O	X	X	VCC3	73mA	S3/S5 powered when AMT activated



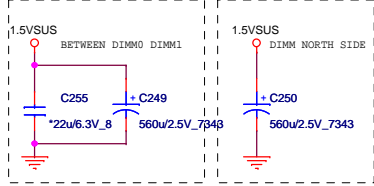
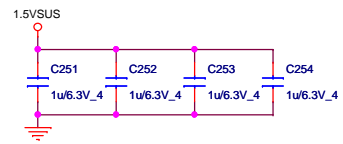
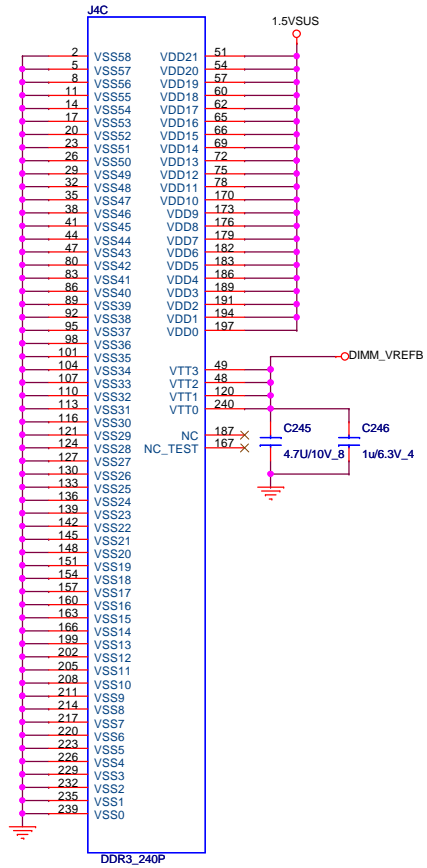
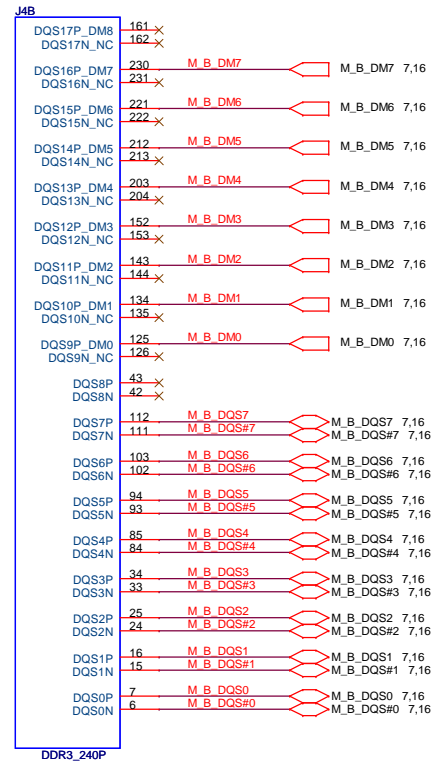
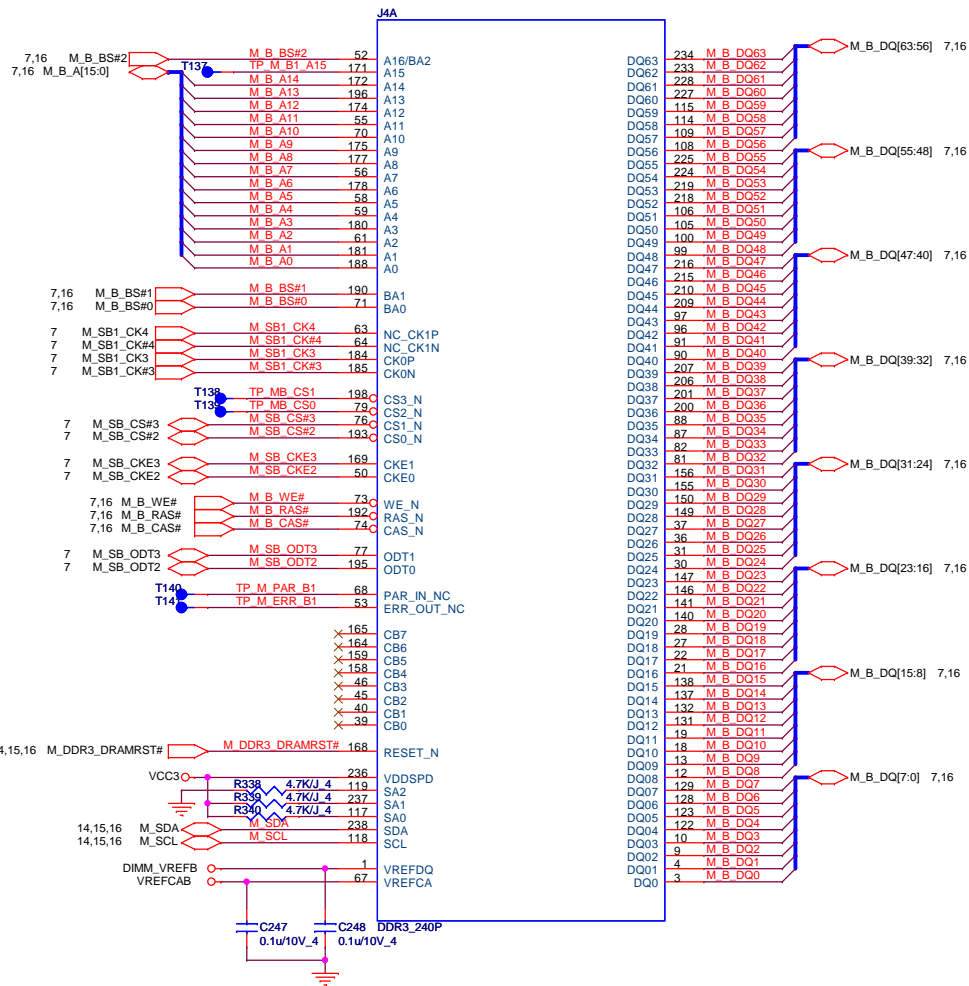
PROJECT : EL8
Quanta Computer Inc.

Size	Document Number DDR3 CHANNEL A DIMM1	Rev 1A
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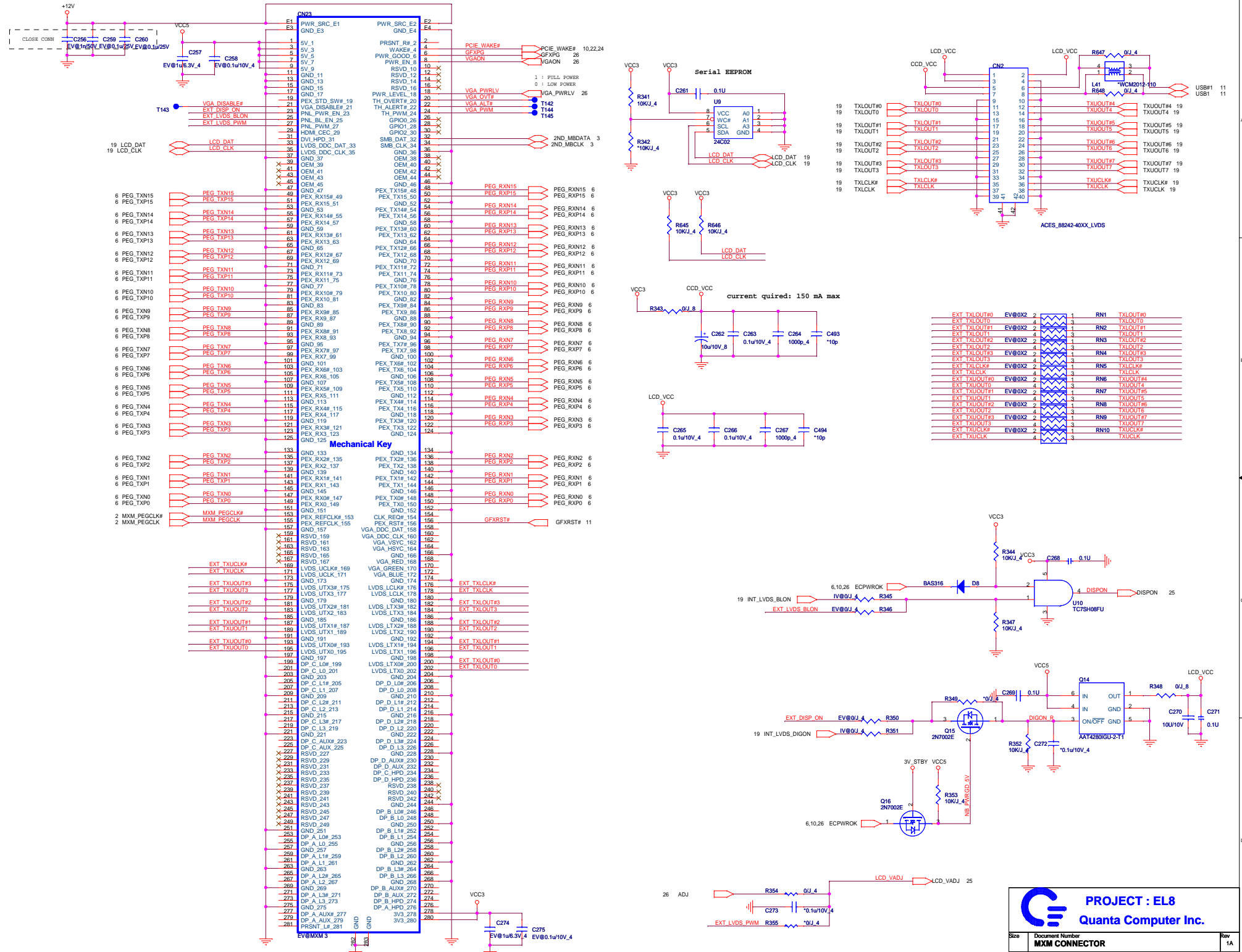
PROJECT : EL8
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 CHANNEL B DIMMO	1A
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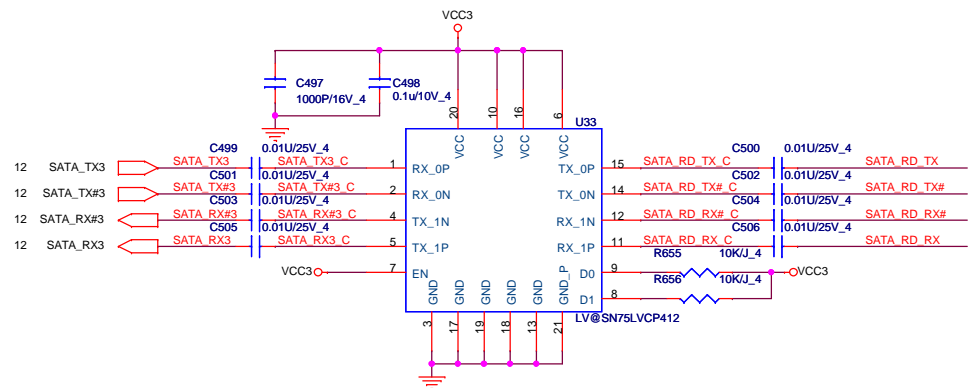
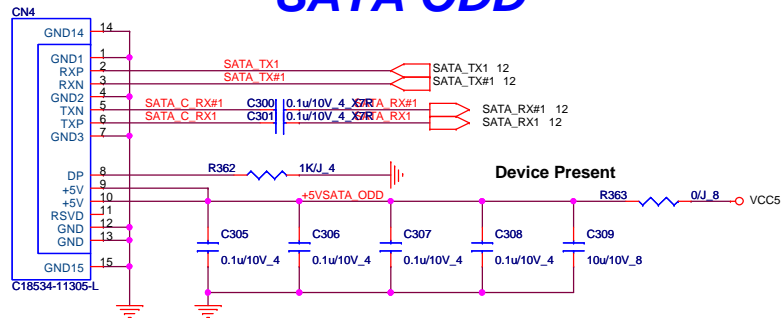
PROJECT : EL8
Quanta Computer Inc.

Size	Document Number DDR3 CHANNEL B DIMM1	Rev 1A
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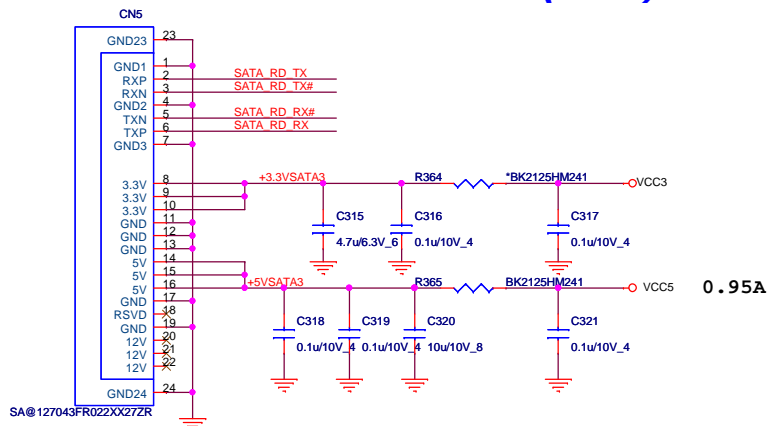


2.1A

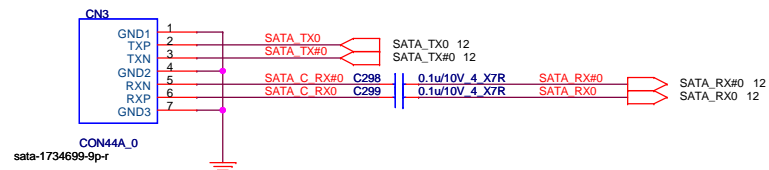
SATA ODD



2nd SATA HDD(2.5")

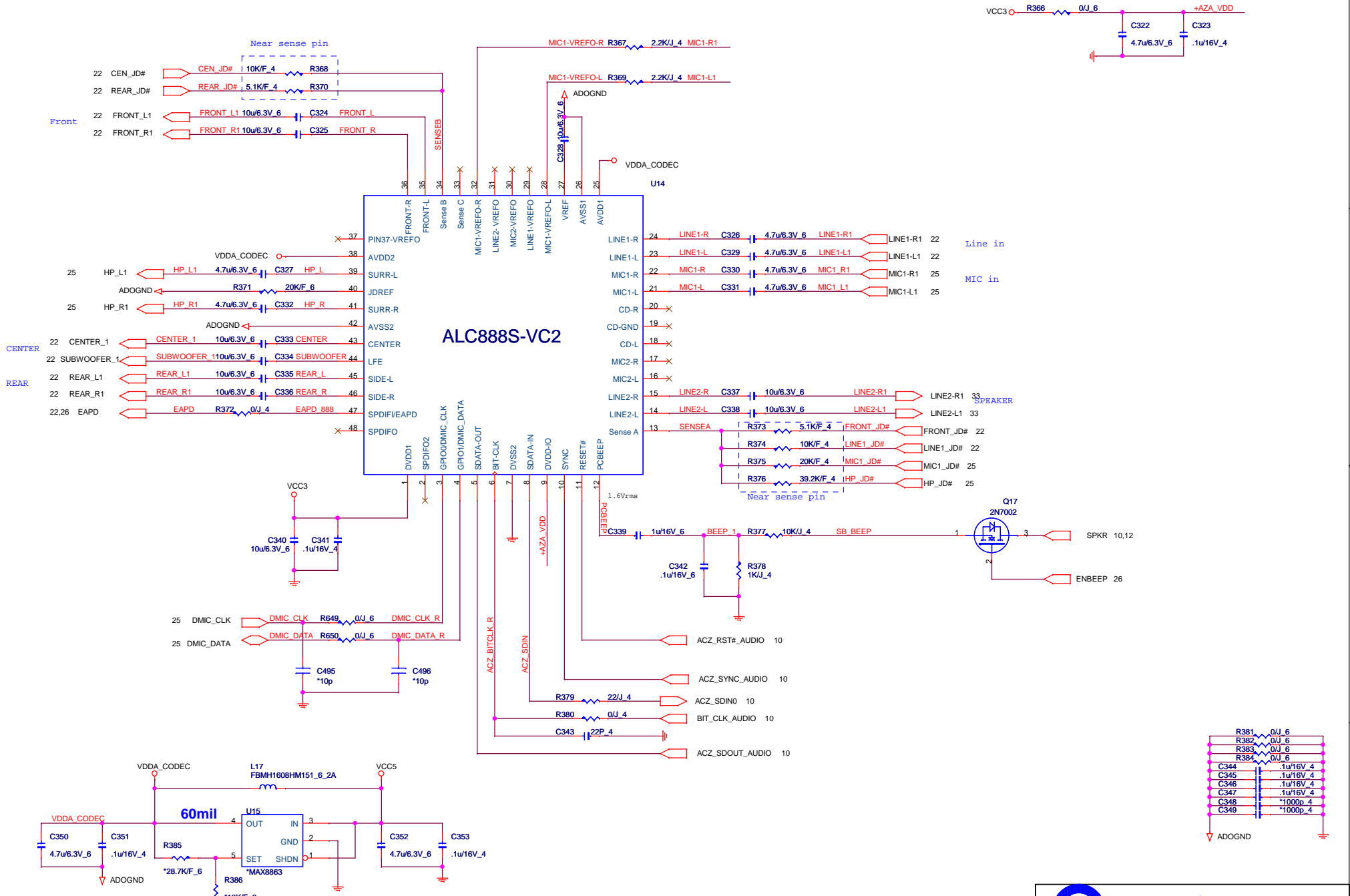


SATA HDD(3.5")



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Size	Document Number	Rev
	3.5HDD/2.5HDD/ODD	1A
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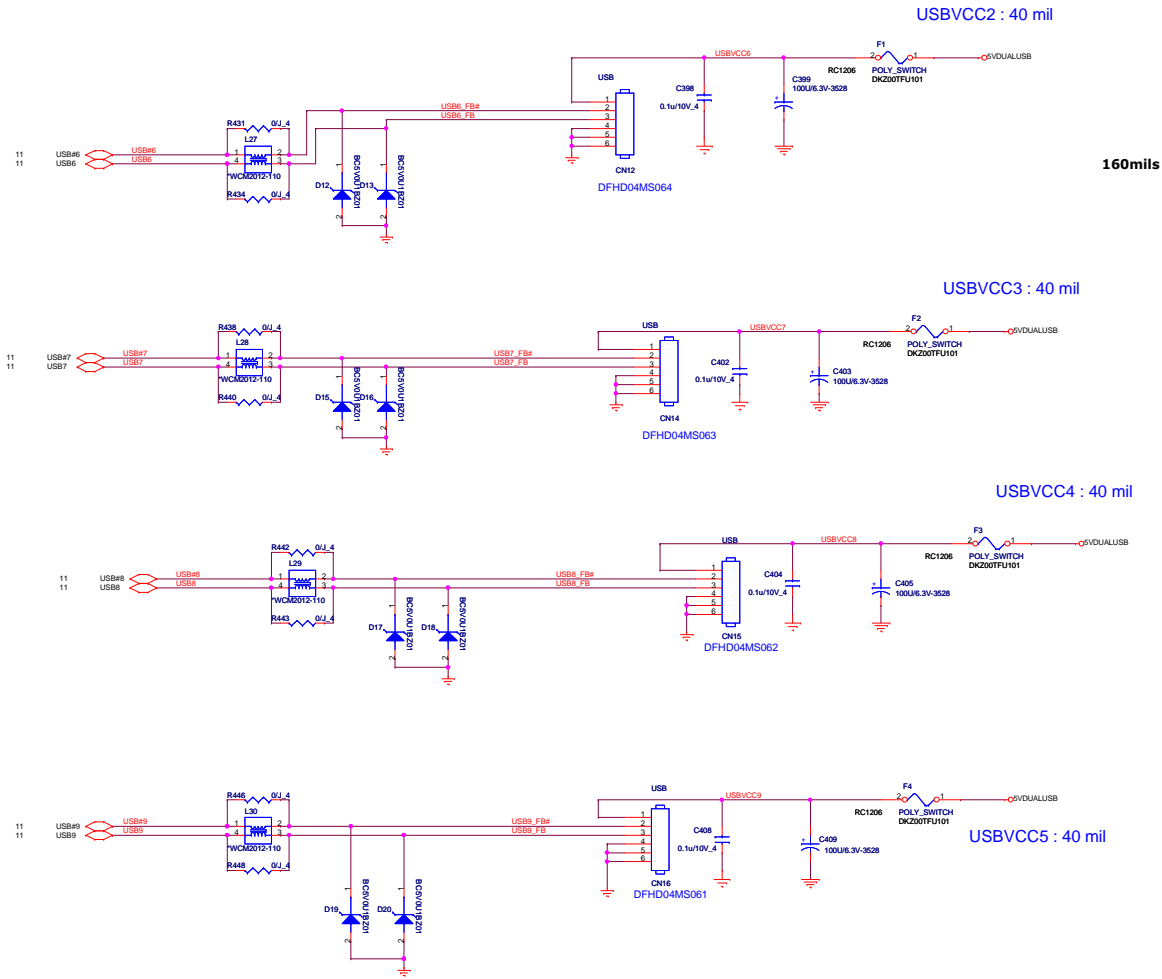
$V_{OUT} = 1.25 \left(1 + \frac{R1}{R2} \right)$
4.8375V 28.7K 10K

2nd source : G923-330T1U
AL000923003

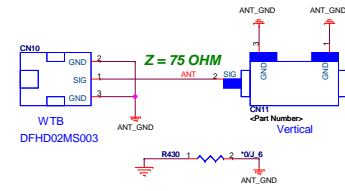
PROJECT : EL8
Quanta Computer Inc.

Size	Document Number	Rev
Date:	CODEC ALC888S-VC2	1A
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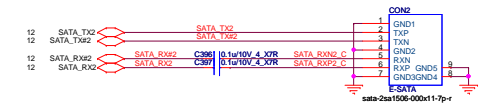
REAR USB PORT X4



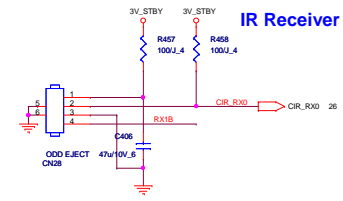
TV ANT. CONNECTOR



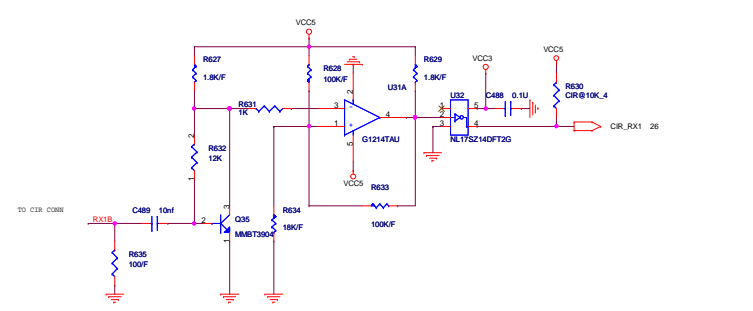
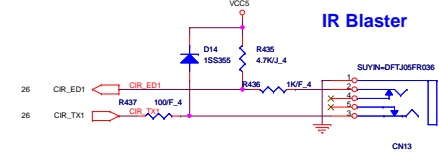
ESATA CONN



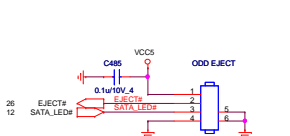
IR Receiver



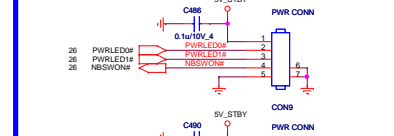
IR Blaster



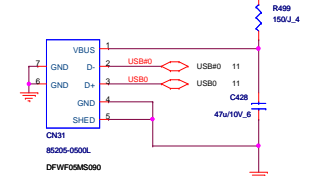
POWER BUTTON



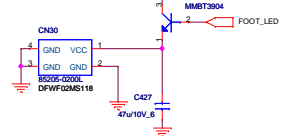
HOME BUTTON



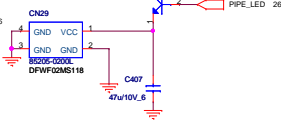
Touch Panel connector

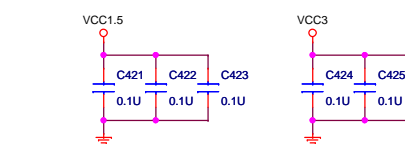
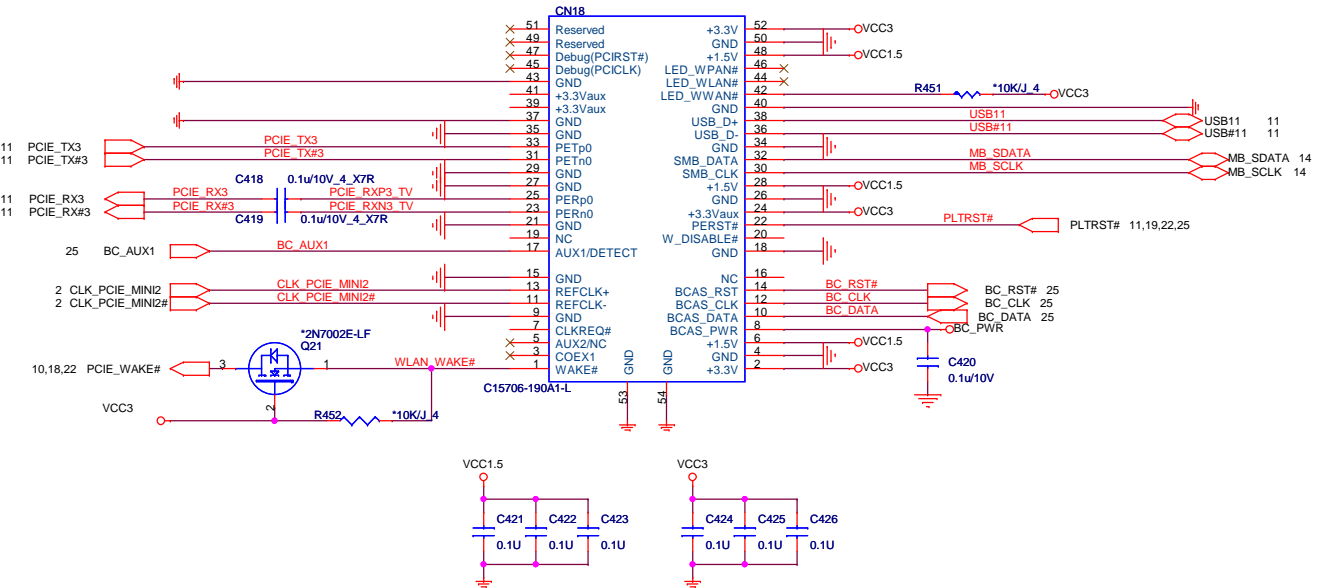
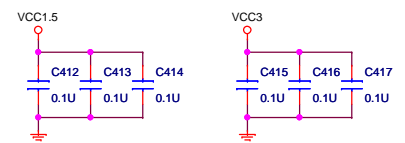
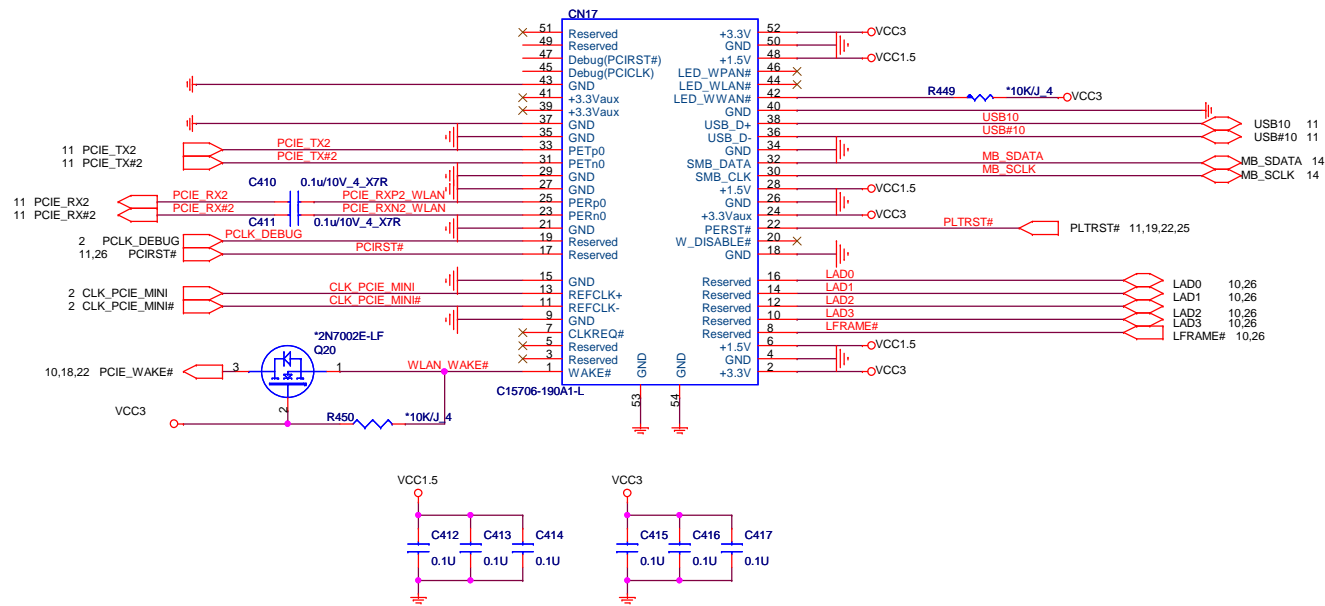


Light Foot



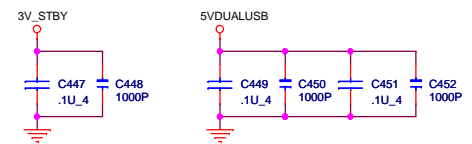
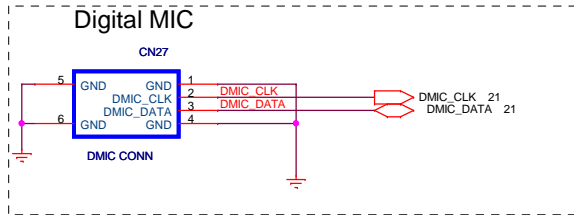
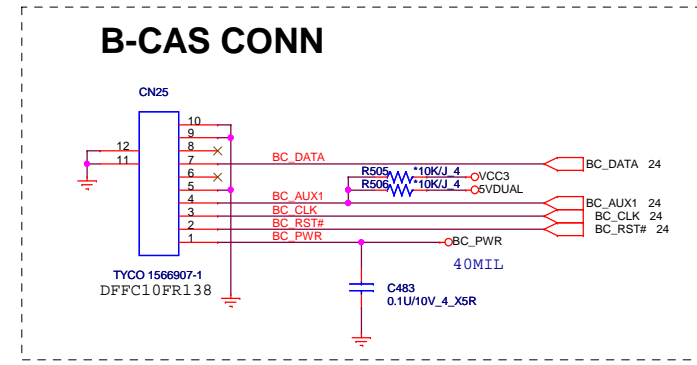
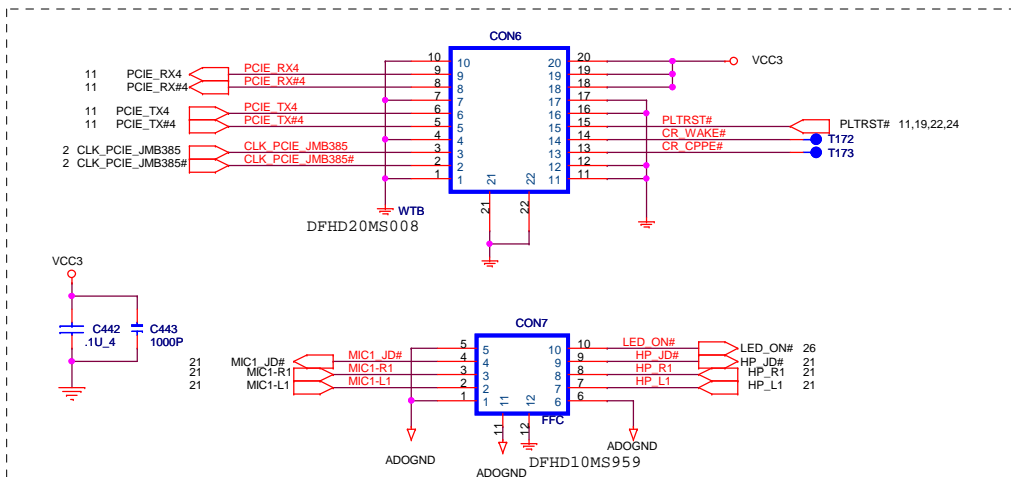
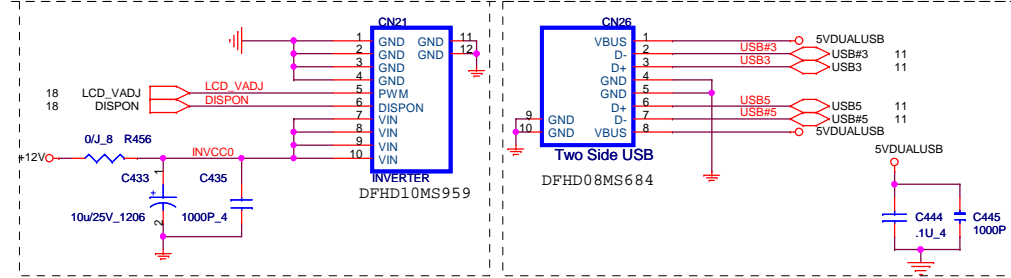
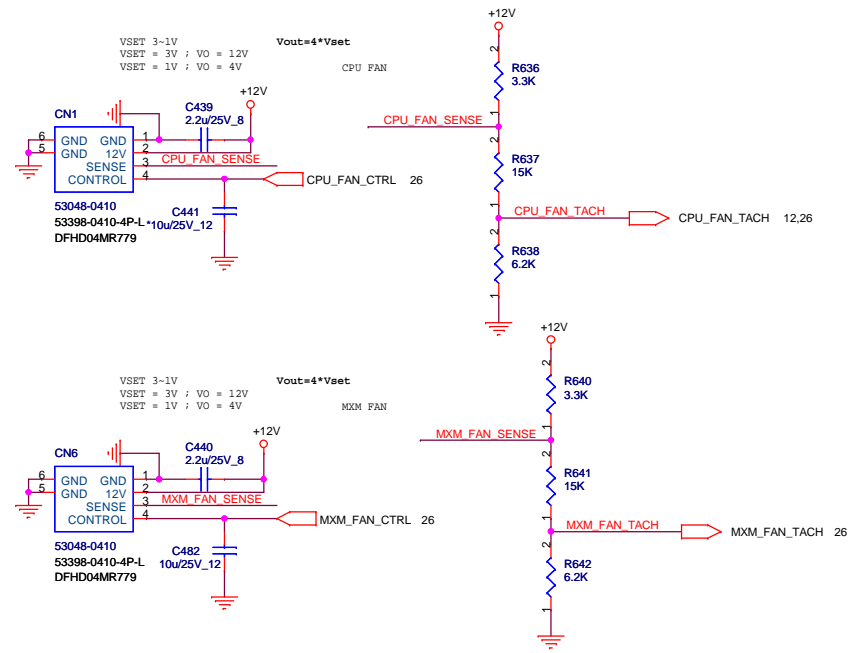
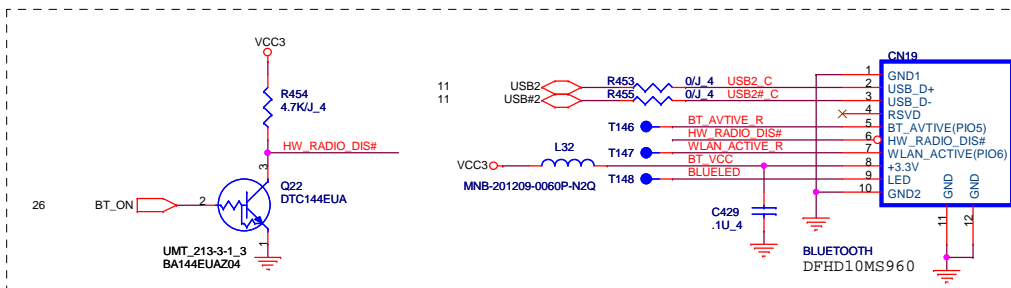
Light Pipe





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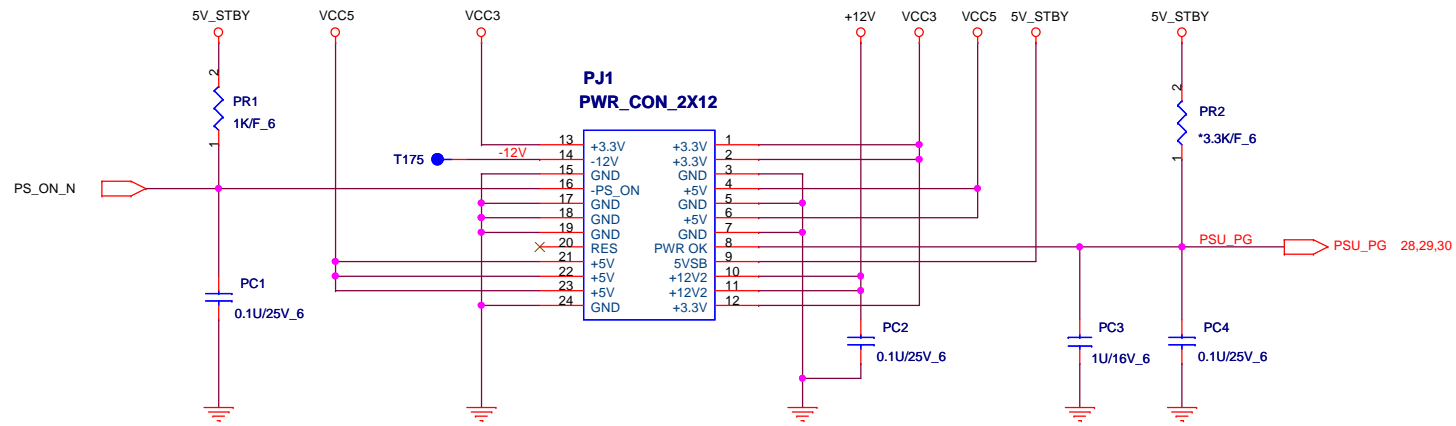
Size	Document Number	Rev
Date:	MINI PCIE(WLAN/TV)	1A
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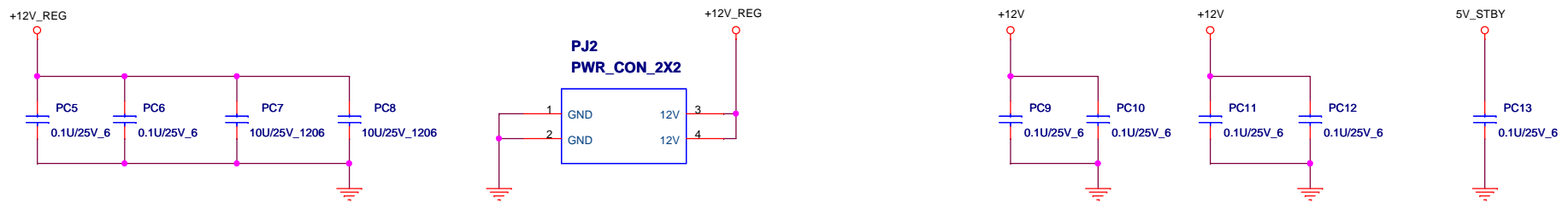
Size	Document Number	Rev
	CONNECTOR	1A
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PSU 24PIN Connector

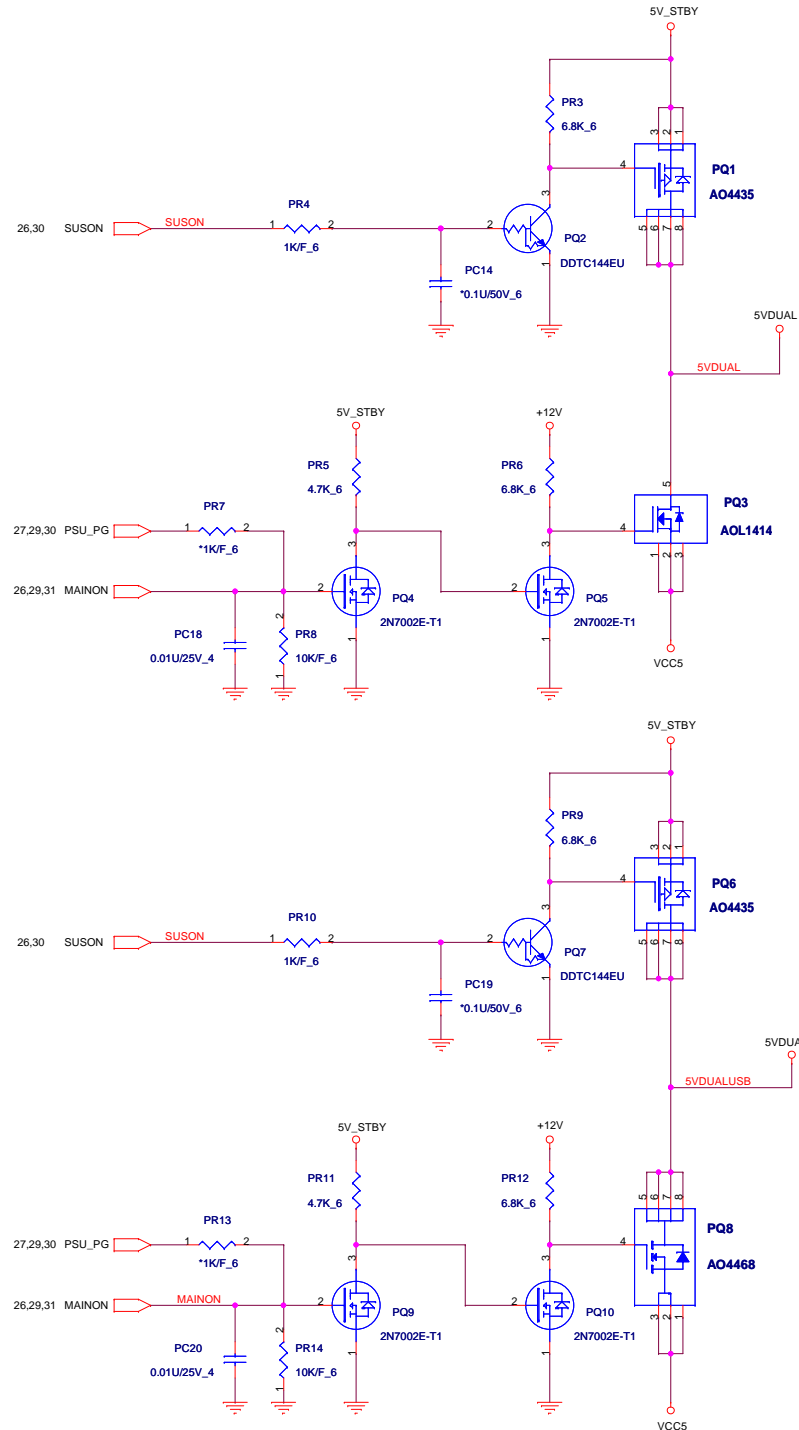


P3V3_STB : Stand-by power source only
 P3V3 : Normal power source only
 P3V3_DUAL : Both power source switching

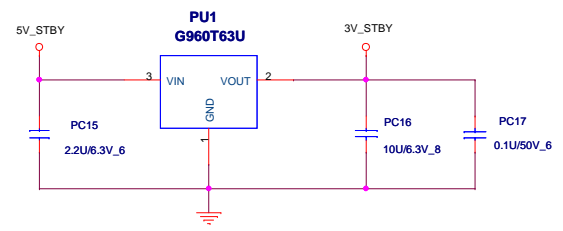
4PIN +12V_REG for CPU_CORE



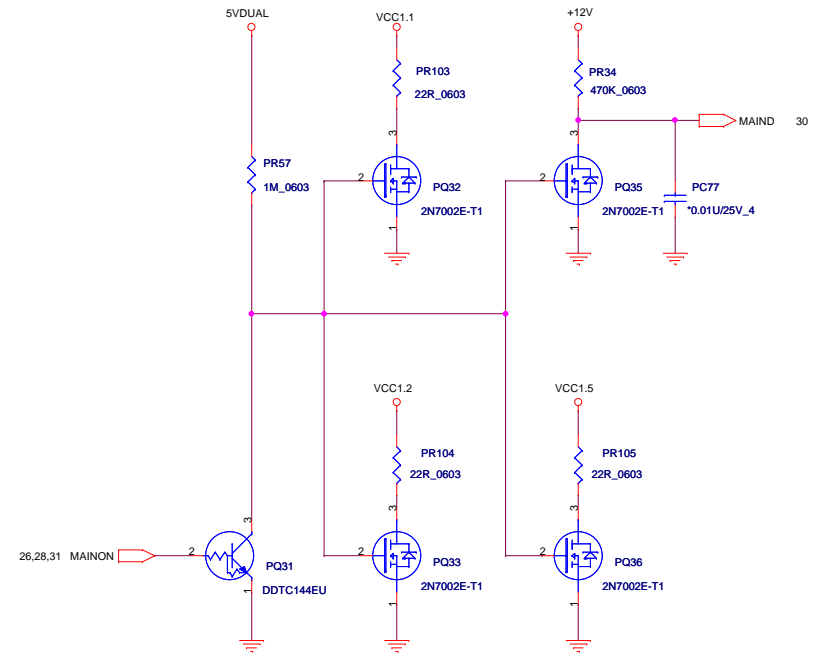
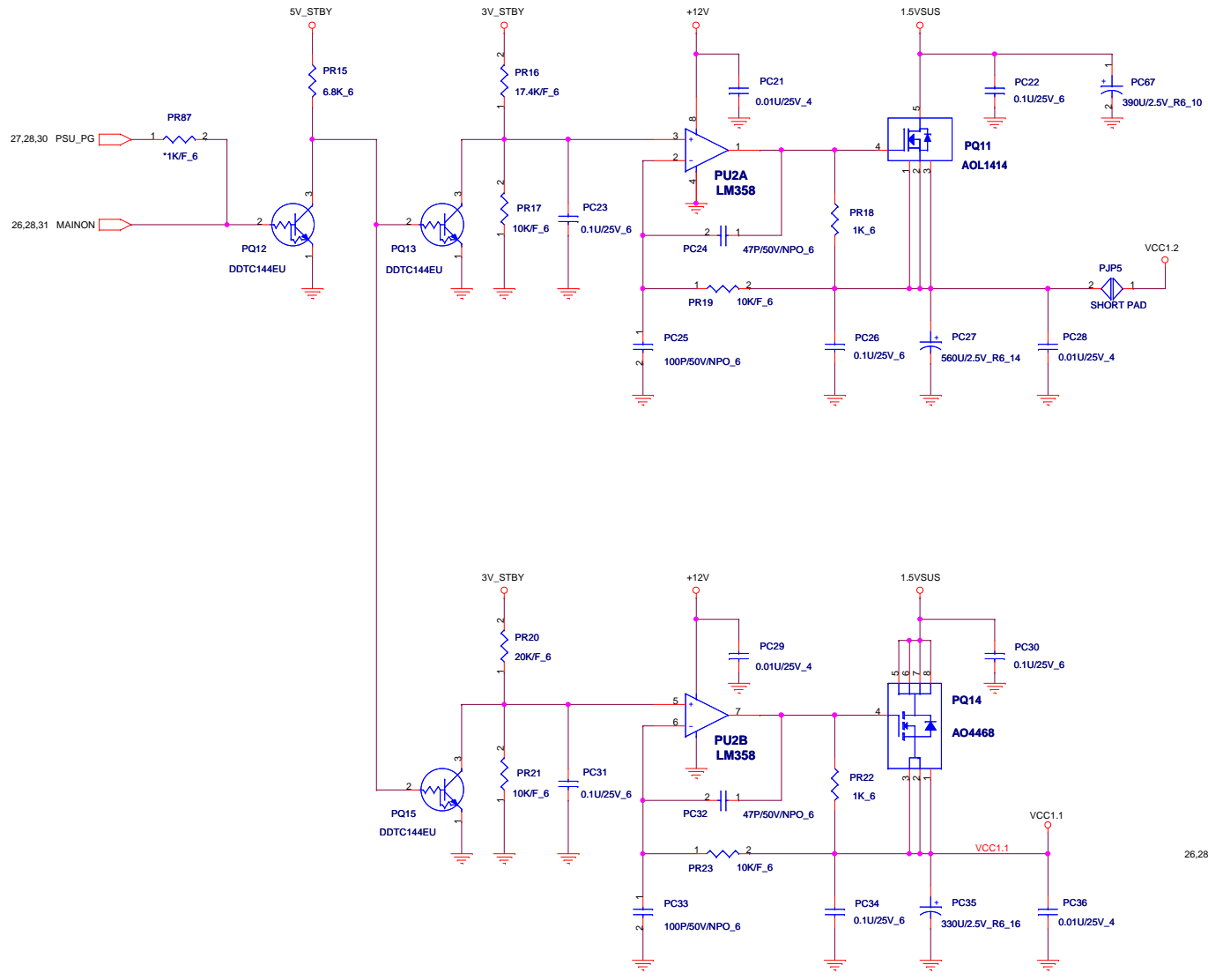
5VDUAL, 5VDUALUSB, 3V_STBY



for EC

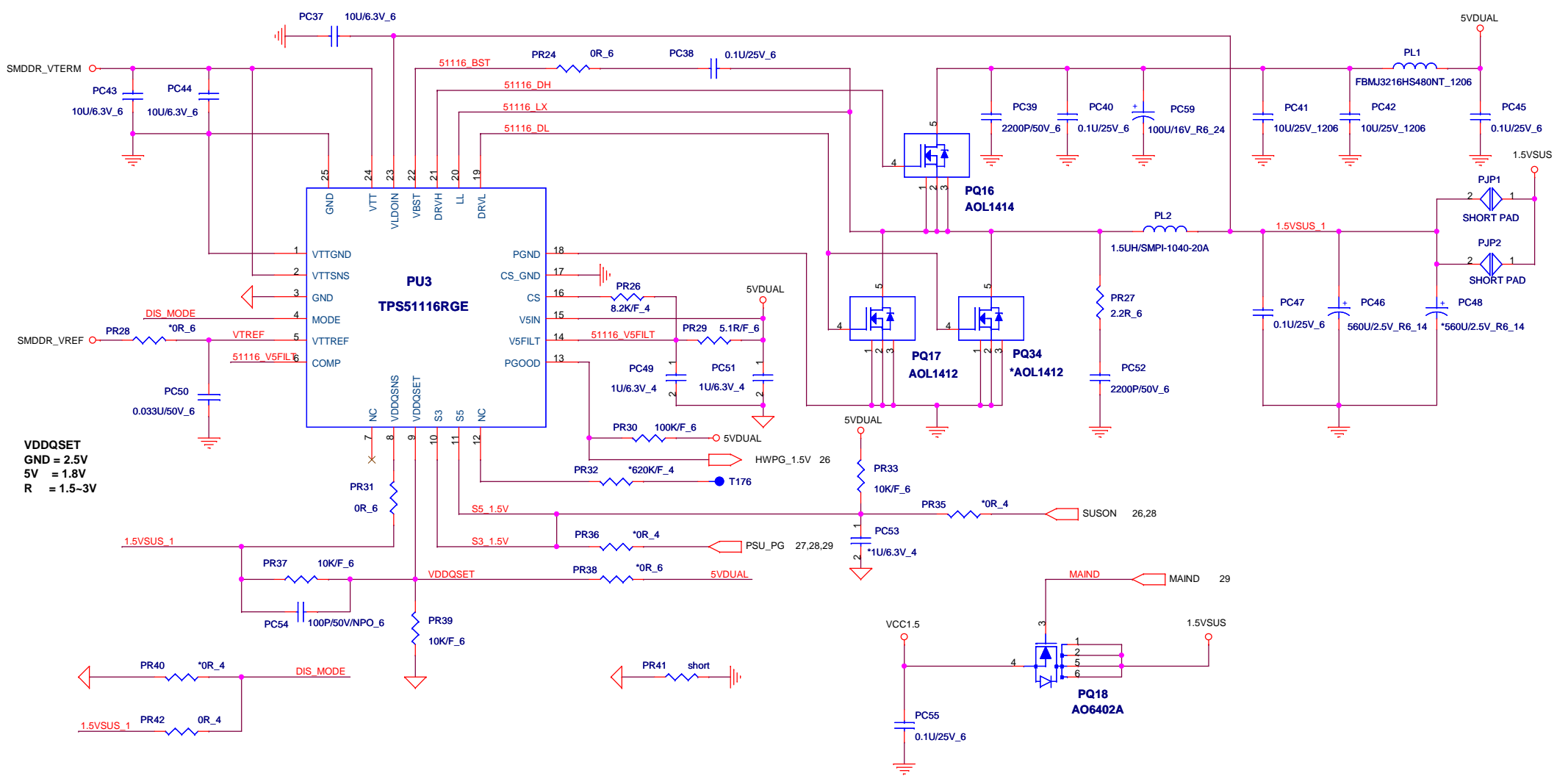


VCC1.2, VCC1.1



For ICH10

DDR3 1.5V(TPS51116)




VDDQSET
 GND = 2.5V
 5V = 1.8V
 R = 1.5-3V

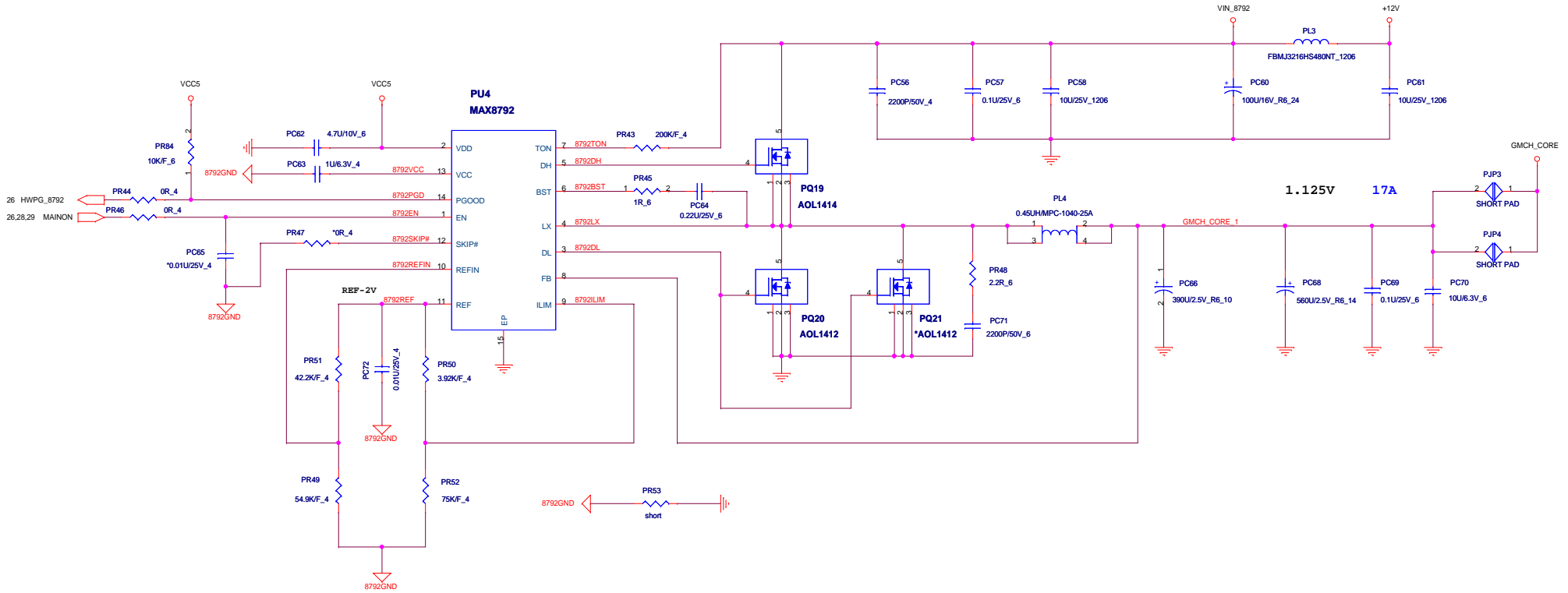
$$del_IL = (5V - 1.5V) \times 1.5V / (1.5 \mu A \times 400K \times 19V) = 4.6A$$

$$(10 \mu A \times PR26 / Rdson) + del_IL / 2 = Iocp$$

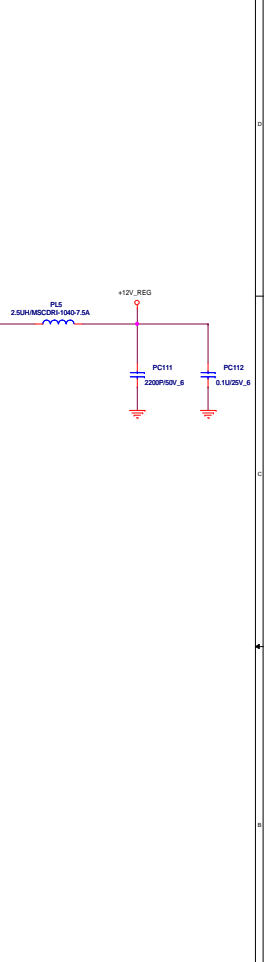
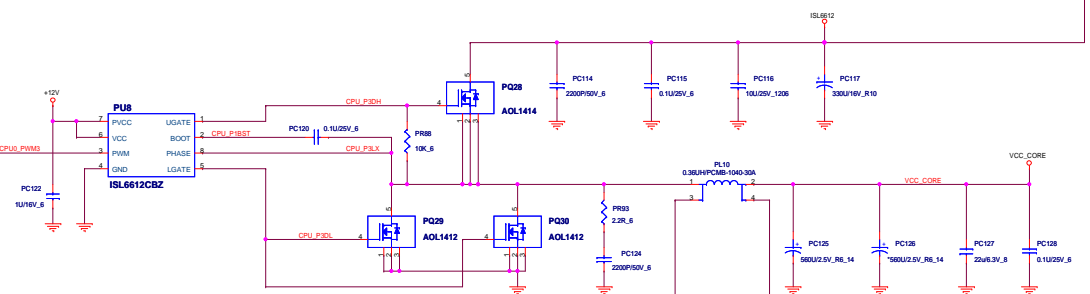
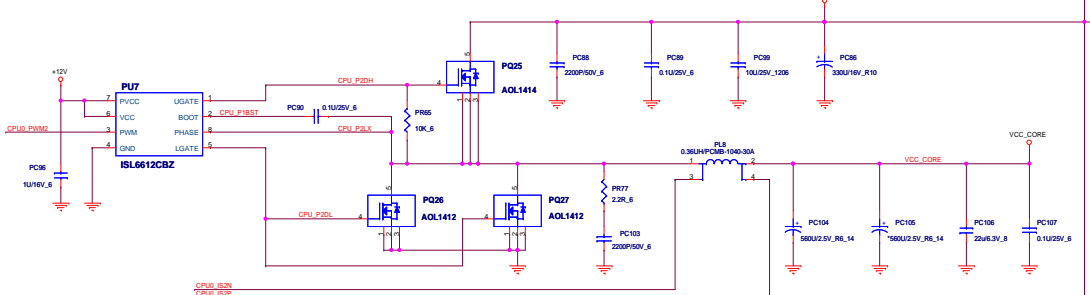
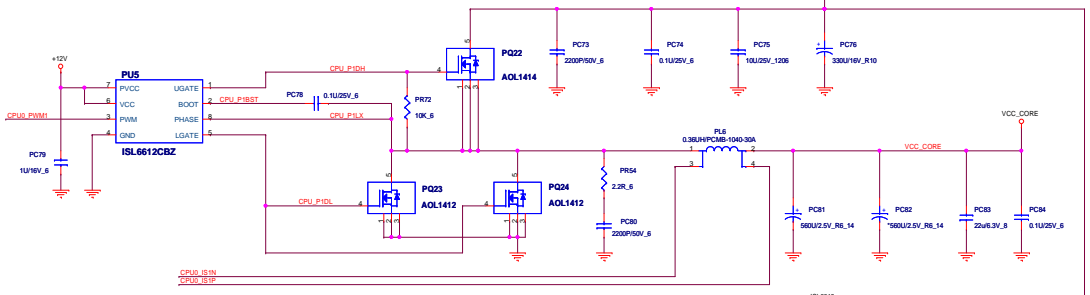
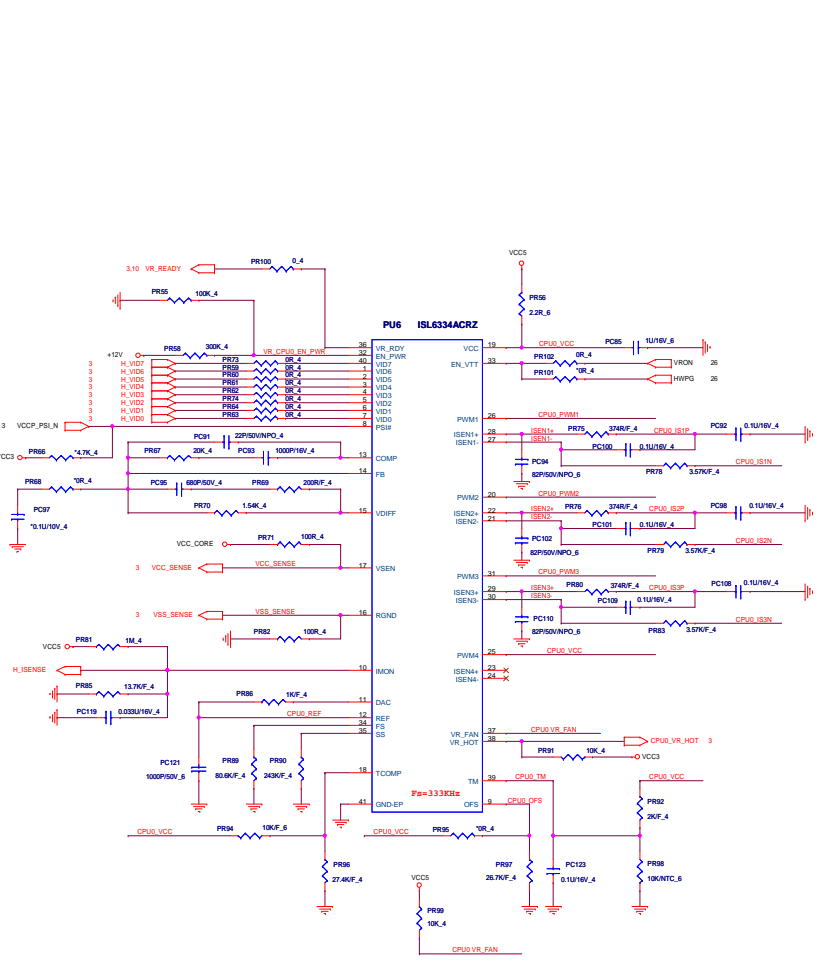
$$(10 \mu A \times 8.2K / 4.6m) + del_IL / 2 = 20.1A$$

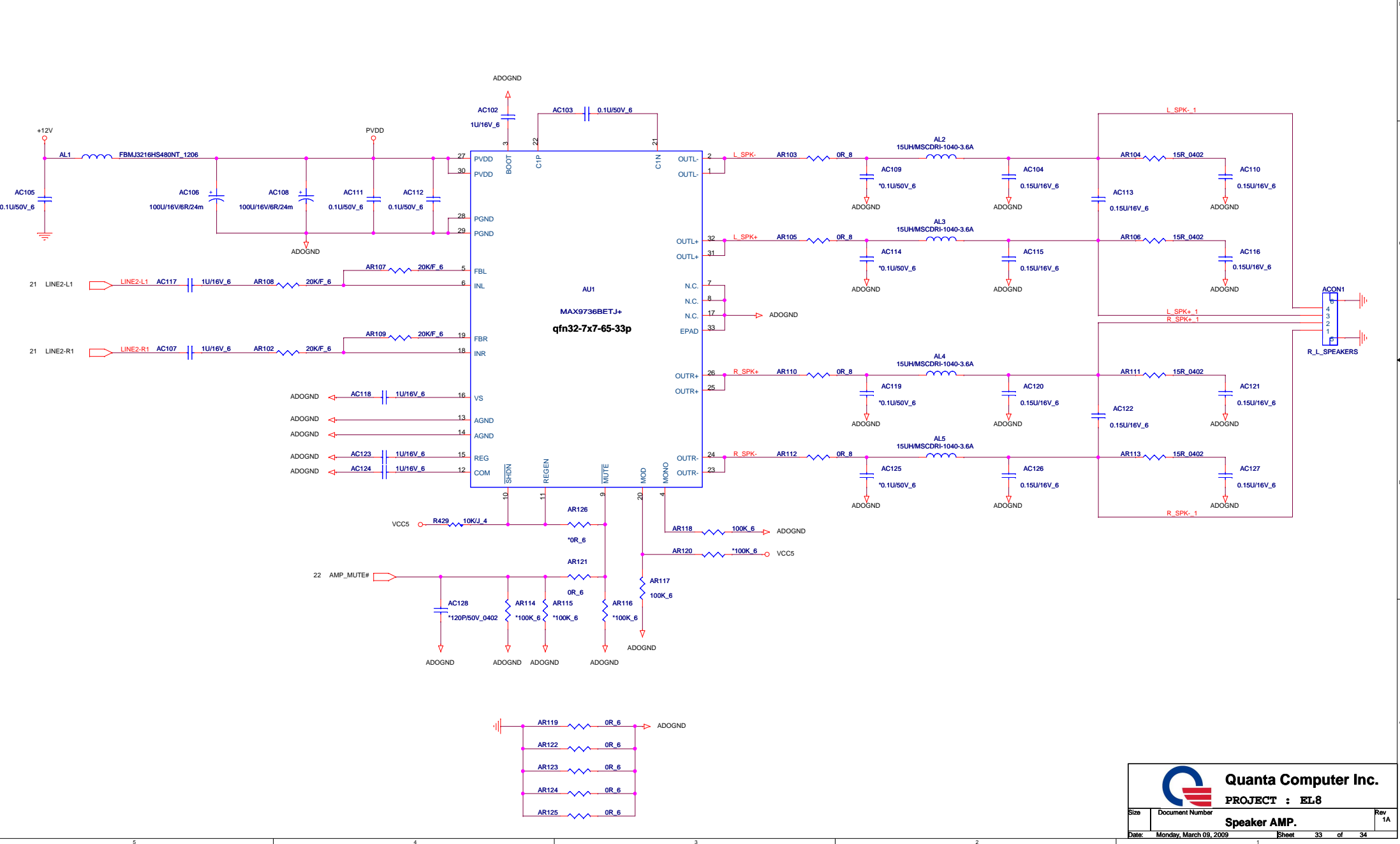
 Quanta Computer Inc. PROJECT : EL8		Rev
		1A
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G43 GMCH_CORE



VCC_CORE





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Speaker AMP.		
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C

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	Change List	1A
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