

ZZZ1



LA-7491P

DA60000N810

# Compal Confidential

## Brazos PCW20 LA7491 Schematics Document

AMD APU Ontario-FT1+ FCH Hudson-M1

2011-03-29

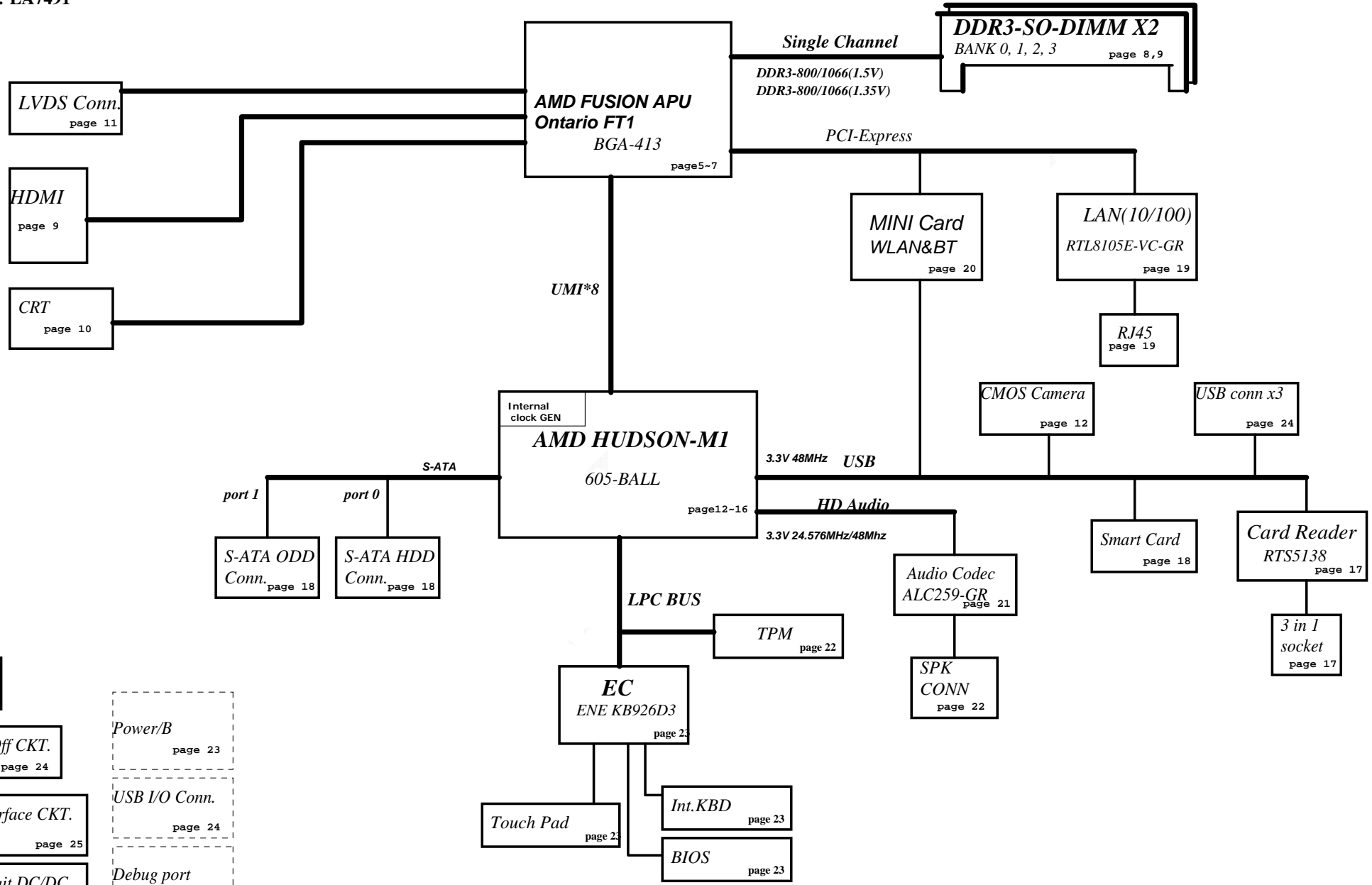
REV:1.0

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			Date: Friday, May 06, 2011	4019D2 B
			Sheet 1 of 36	

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Model Name : Brazos

File Name : LA7491



- RTC CKT. page 13
- Power On/Off CKT. page 24
- DC/DC Interface CKT. page 25
- Power Circuit DC/DC page 26, 28, 29, 30, 31, 32, 33
- CHARGER page 27

- Power/B page 23
- USB I/O Conn. page 24
- Debug port page 19
- LED page 21

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Date:	Friday, May 06, 2011	Sheet	2	of	36	

### DDR3 Voltage Rails

power plane / State	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +NB_CORE +1.8VS +0.75VS +1.1VS +1.0VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

@	Reserve
CONN@	ME CONNECTOR
8105E@	100M LAN function
8111E@	GLAN function
REAL@	ALC259-GR
VIA@	V1802T
ROM@	not support flash ROM
FROM@	Support flash ROM

### FCH SM Bus0 address

Device	HEX	Address
SDDIM I	A0	1010 0000
SDDIM II	A2	1010 0010

### FCH SM Bus1 address

Device	HEX	Address
WLAN		

### EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b

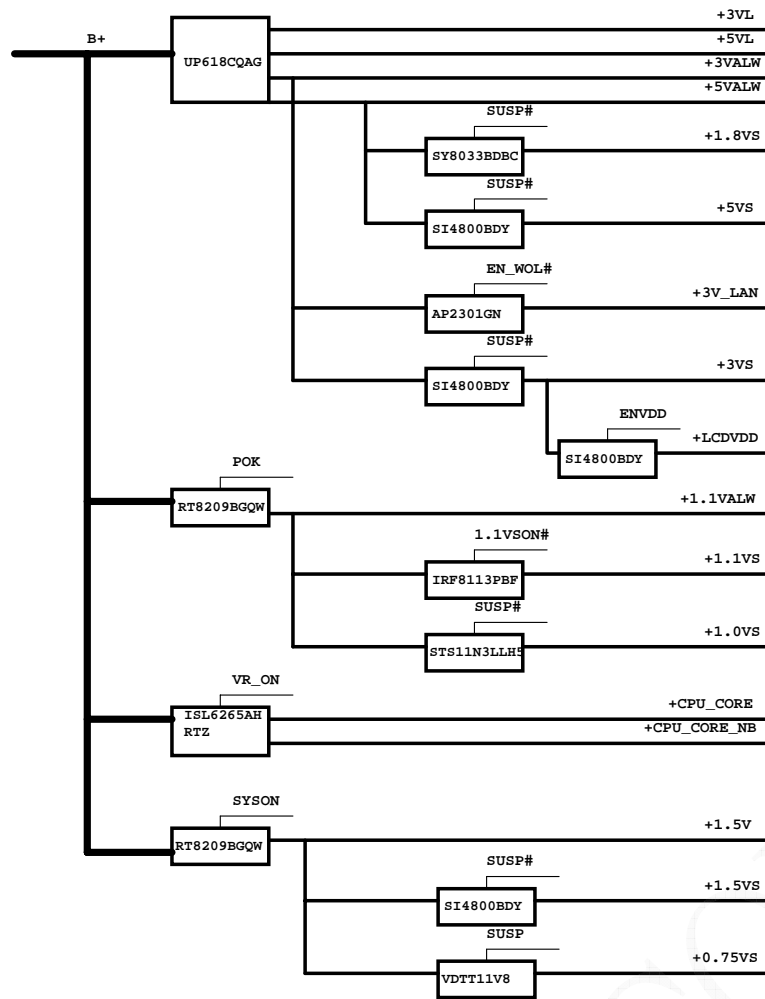
### EC SM Bus2 address

Device	HEX	Address
APU internal thermal sensor		1001 100X b

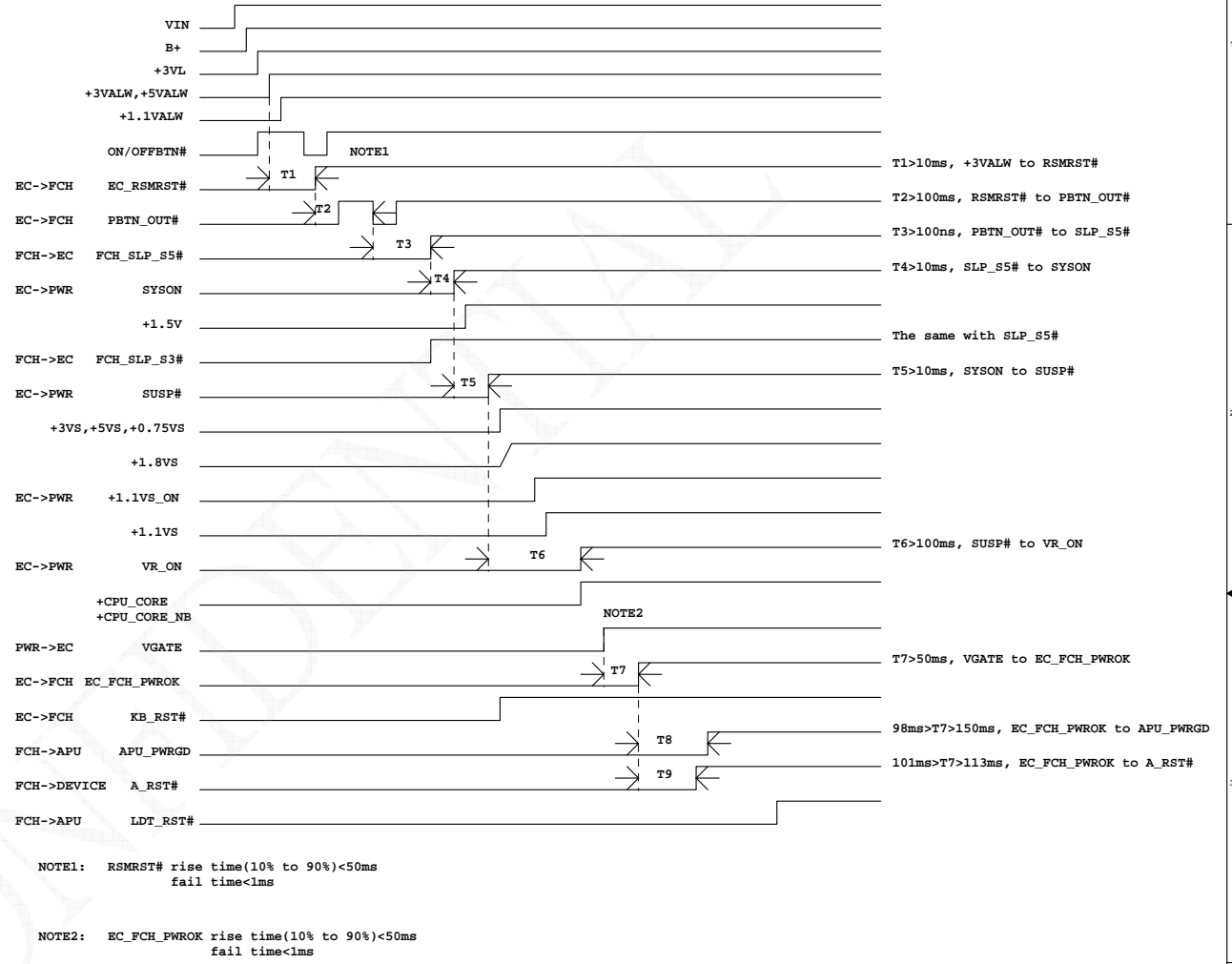
	SOURCE	POWER PLAN	HDMI	LVDS	CRT	FCH	CPU CORE	SDDIM I/II	WLAN	BATT	APU
TDP1_AUXP TDP1_AUXN	APU	+3VS	V								
LTDP0_AUXP LTDP1_AUXN	APU	+3VS		V +5VS							
DAC_SCL DAC_SDA	APU	+3VS			V +5VS						
SIC SID	APU	+3VS				V +3VALW					
SVC SVD	APU	+1.8VS					V				
SMB_FCH_CK0 SMB_FCH_DAO	FCH	+3VS						V			
SMB_FCH_CK1 SMB_FCH_DA1	FCH	+3VALW							V		
SMB_EC_CK1 SMB_EC_DA1	EC	+5VALW								V	
SMB_EC_CK2 SMB_EC_DA2	EC	+3VS									V

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			Date:	Friday, May 06, 2011	Sheet	3 of 36

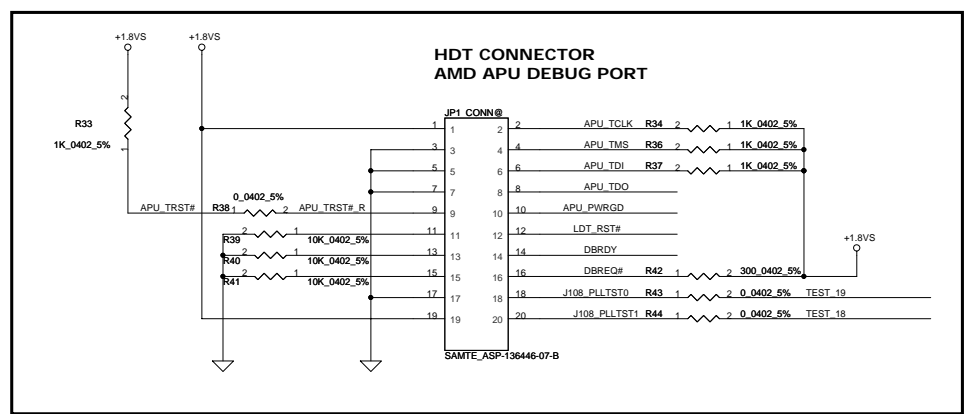
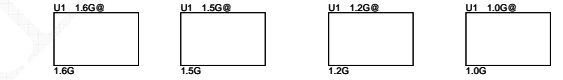
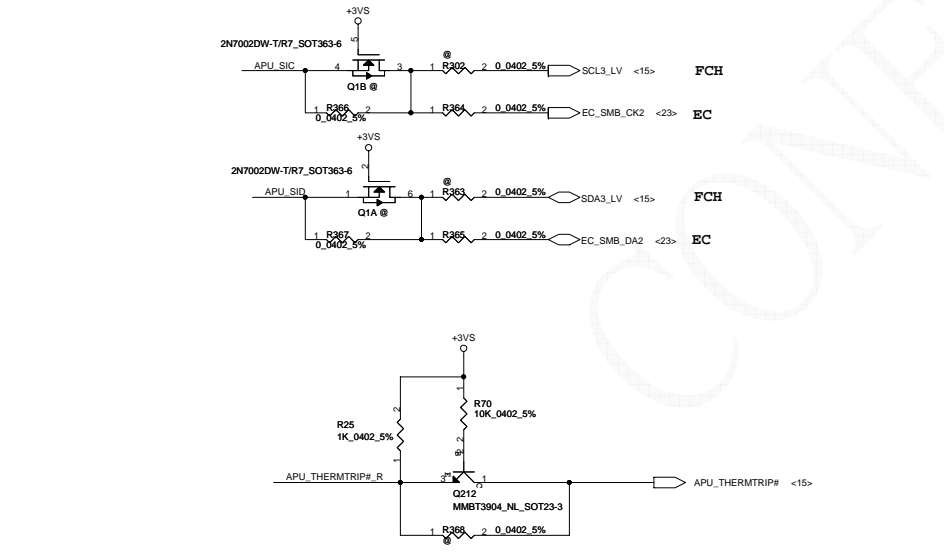
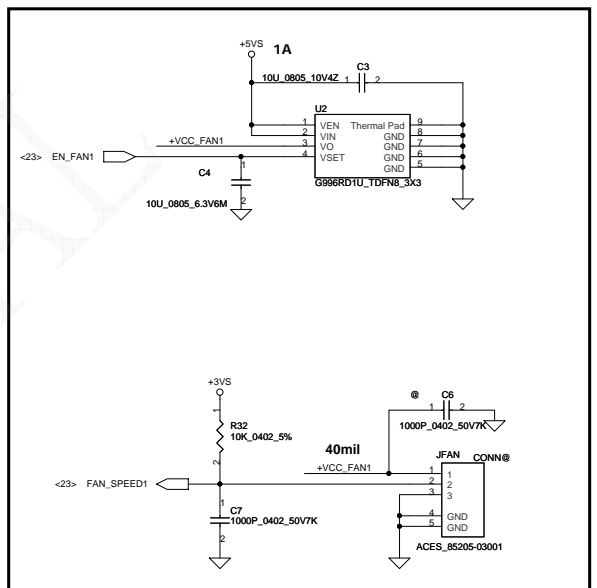
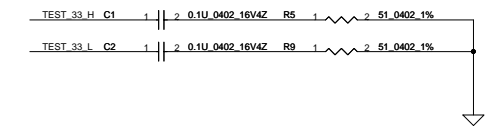
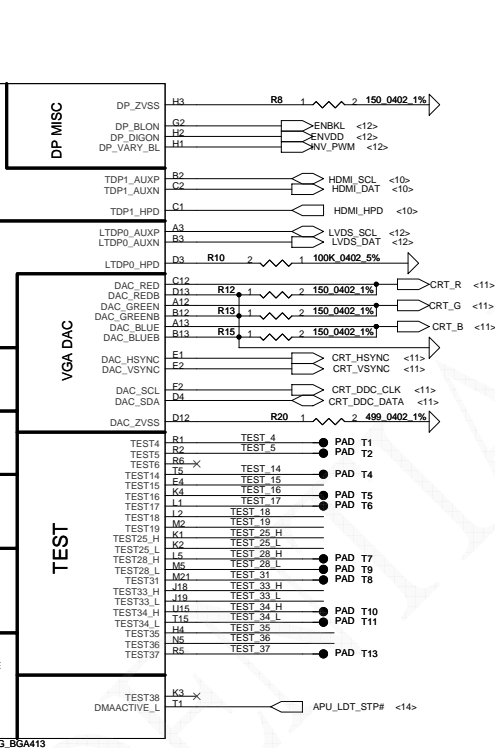
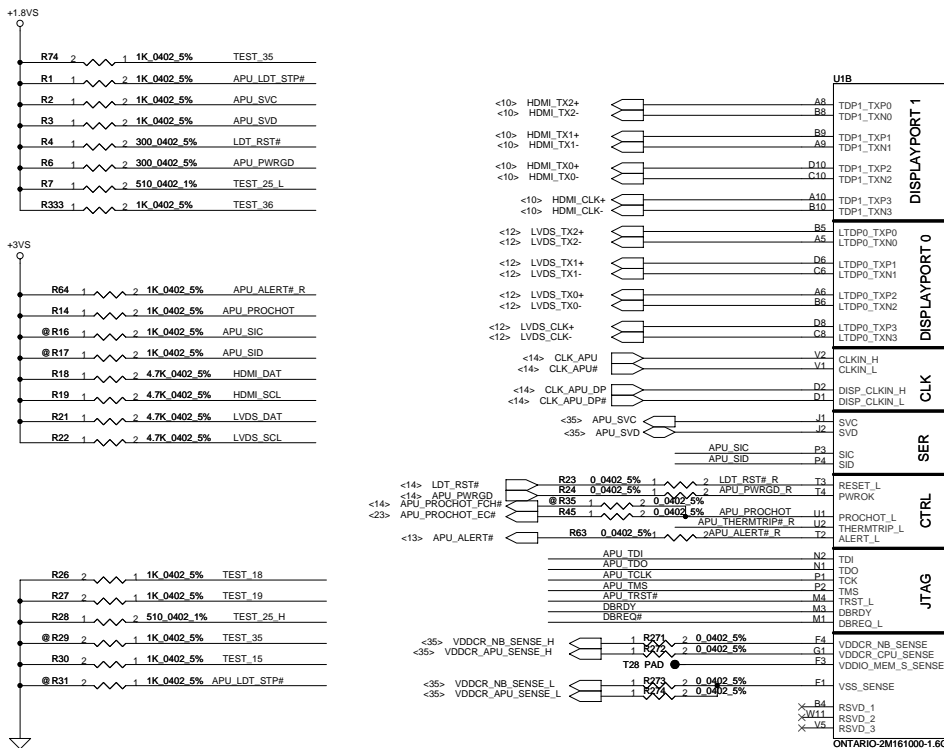
### POWER MAP



### POWER SEQUENCE



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			4019D2	B
			Date: Friday, May 06, 2011	Sheet 4 of 36



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			4019D2	B
			Date: Friday, May 06, 2011	Sheet 5 of 36

<8.9> DDR\_D[0..63]  
 <8.9> DDR\_DM[0..7]  
 <8.9> DDR\_DQS[0..7]  
 <8.9> DDR\_DQS[0..7]  
 <8.9> DDR\_MA[0..15]



UIE

DDR_MA0	R17	M_ADD0
DDR_MA1	H19	M_ADD1
DDR_MA2	H17	M_ADD2
DDR_MA3	H18	M_ADD3
DDR_MA4	H17	M_ADD4
DDR_MA5	G17	M_ADD5
DDR_MA6	H16	M_ADD6
DDR_MA7	G18	M_ADD7
DDR_MA8	F19	M_ADD8
DDR_MA9	E19	M_ADD9
DDR_MA10	T19	M_ADD10
DDR_MA11	F17	M_ADD11
DDR_MA12	E18	M_ADD12
DDR_MA13	W17	M_ADD13
DDR_MA14	E16	M_ADD14
DDR_MA15	G15	M_ADD15

DDR SYSTEM MEMORY

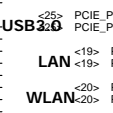
DDR_DM0	D15	M_DM0
DDR_DM1	B19	M_DM1
DDR_DM2	D21	M_DM2
DDR_DM3	H22	M_DM3
DDR_DM4	P23	M_DM4
DDR_DM5	V23	M_DM5
DDR_DM6	AB20	M_DM6
DDR_DM7	AA16	M_DM7
DDR_DQS0	A16	M_DQS_L0
DDR_DQS#0	B16	M_DQS_L1
DDR_DQS#1	A20	M_DQS_L2
DDR_DQS#2	E23	M_DQS_L3
DDR_DQS#3	J22	M_DQS_L4
DDR_DQS#4	R22	M_DQS_L5
DDR_DQS#5	V22	M_DQS_L6
DDR_DQS#6	AC20	M_DQS_L7
DDR_DQS#7	AC16	M_DQS_L8

DDR_A_CLK0	M17	M_CLK_H0
DDR_A_CLK#0	M16	M_CLK_L0
DDR_A_CLK1	M18	M_CLK_H1
DDR_B_CLK0	N18	M_CLK_H2
DDR_B_CLK#0	L18	M_CLK_L2
DDR_B_CLK1	L17	M_CLK_H3
DDR_B_CLK#1	L17	M_CLK_L3
DDR_RST#	L23	M_RESET_L
DDR_EVENT#	N17	M_EVENT_L
DDR_CKE0	F15	M_CKE0
DDR_CKE1	E15	M_CKE1
DDR_A_ODT0	W19	M0_ODT0
DDR_A_ODT1	V15	M0_ODT1
DDR_B_ODT0	U19	M1_ODT0
DDR_B_ODT1	W15	M1_ODT1
DDR_A_CS0#	T17	M0_CS_L0
DDR_A_CS1#	W16	M0_CS_L1
DDR_B_CS0#	U17	M1_CS_L0
DDR_B_CS1#	W16	M1_CS_L1
DDR_RAS#	U18	M_RAS_L
DDR_CAS#	V19	M_CAS_L
DDR_WE#	V17	M_WE_L

M\_VREF

ONTARIO-2M161000-1.6G\_BGA413 @

M_DATA0	B14	DDR_D0
M_DATA1	A15	DDR_D1
M_DATA2	A17	DDR_D2
M_DATA3	D18	DDR_D3
M_DATA4	A14	DDR_D4
M_DATA5	C14	DDR_D5
M_DATA6	C16	DDR_D6
M_DATA7	D16	DDR_D7
M_DATA8	C18	DDR_D8
M_DATA9	A19	DDR_D9
M_DATA10	B21	DDR_D10
M_DATA11	D20	DDR_D11
M_DATA12	A18	DDR_D12
M_DATA13	B18	DDR_D13
M_DATA14	A21	DDR_D14
M_DATA15	C20	DDR_D15
M_DATA16	C23	DDR_D16
M_DATA17	D23	DDR_D17
M_DATA18	F23	DDR_D18
M_DATA19	F22	DDR_D19
M_DATA20	C22	DDR_D20
M_DATA21	F20	DDR_D21
M_DATA22	F21	DDR_D22
M_DATA23	F21	DDR_D23
M_DATA24	H21	DDR_D24
M_DATA25	H23	DDR_D25
M_DATA26	K22	DDR_D26
M_DATA27	K21	DDR_D27
M_DATA28	H20	DDR_D28
M_DATA29	K20	DDR_D29
M_DATA30	K23	DDR_D30
M_DATA31	K23	DDR_D31
M_DATA32	N23	DDR_D32
M_DATA33	P21	DDR_D33
M_DATA34	T20	DDR_D34
M_DATA35	T23	DDR_D35
M_DATA36	M20	DDR_D36
M_DATA37	F20	DDR_D37
M_DATA38	R23	DDR_D38
M_DATA39	T22	DDR_D39
M_DATA40	V20	DDR_D40
M_DATA41	V21	DDR_D41
M_DATA42	Y23	DDR_D42
M_DATA43	Y22	DDR_D43
M_DATA44	T21	DDR_D44
M_DATA45	U23	DDR_D45
M_DATA46	W23	DDR_D46
M_DATA47	Y21	DDR_D47
M_DATA48	Y20	DDR_D48
M_DATA49	AB22	DDR_D49
M_DATA50	AC19	DDR_D50
M_DATA51	AA18	DDR_D51
M_DATA52	AA23	DDR_D52
M_DATA53	AA20	DDR_D53
M_DATA54	AB19	DDR_D54
M_DATA55	Y18	DDR_D55
M_DATA56	AC17	DDR_D56
M_DATA57	Y16	DDR_D57
M_DATA58	AB14	DDR_D58
M_DATA59	AC14	DDR_D59
M_DATA60	AC18	DDR_D60
M_DATA61	AB18	DDR_D61
M_DATA62	AB15	DDR_D62
M_DATA63	AC15	DDR_D63

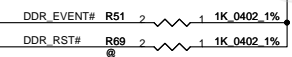
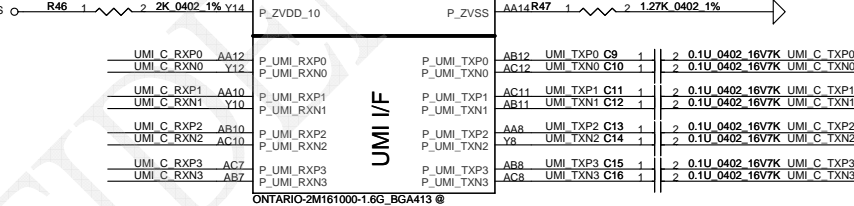
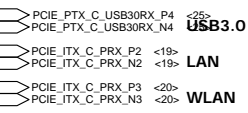


PCIE_PRX_C_USB30TX_P4	AB4
PCIE_PRX_C_USB30TX_N4	AC4
PCIE_PTX_C_IRX_P2	AA1
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PCIE_PTX_C_IRX_P3	Y4
PCIE_PTX_C_IRX_N3	Y3

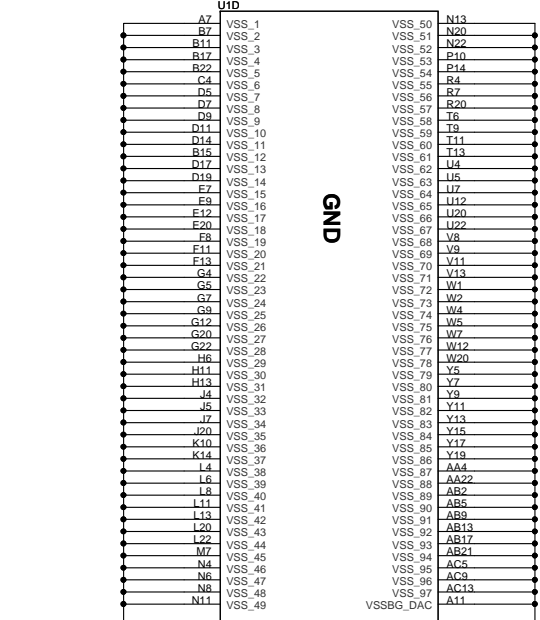
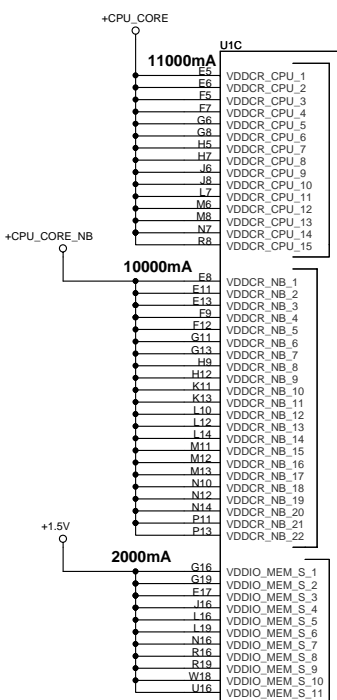
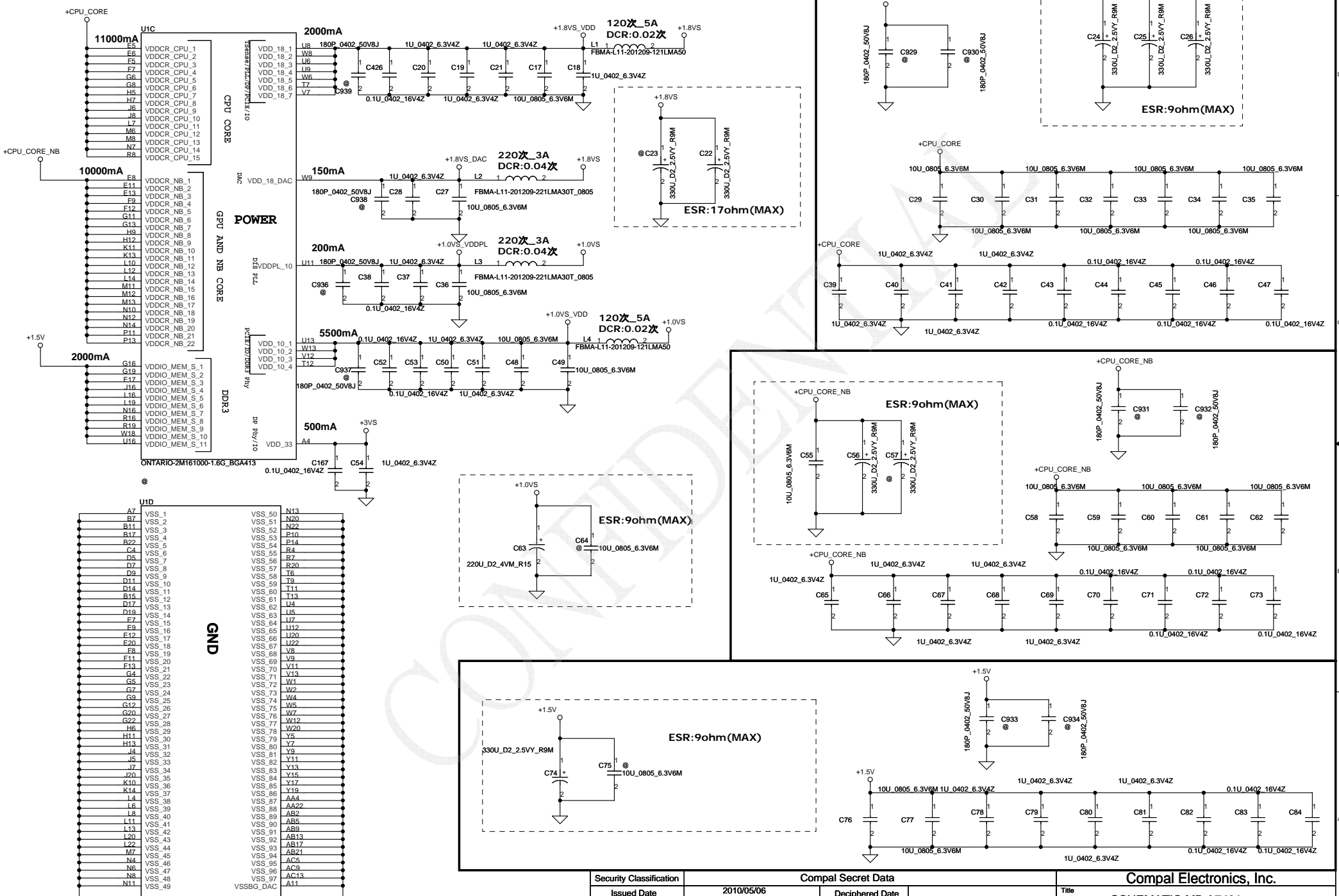
UIA

P_GPP_RXP0	AA6
P_GPP_RXN0	Y6
P_GPP_RXP1	AB4
P_GPP_RXN1	AC4
P_GPP_RXP2	AA1
P_GPP_RXN2	AA2
P_GPP_RXP3	Y4
P_GPP_RXN3	Y3
P_UMI_RXP0	AA12
P_UMI_RXN0	Y12
P_UMI_RXP1	AA10
P_UMI_RXN1	Y10
P_UMI_RXP2	AB10
P_UMI_RXN2	AC10
P_UMI_RXP3	AC7
P_UMI_RXN3	AB7

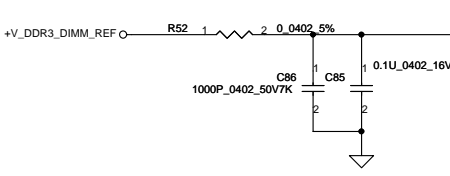
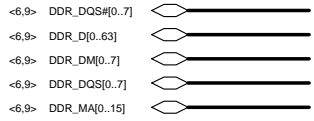
P_GPP_TXP0	AB6
P_GPP_TXN0	AC6
P_GPP_TXP1	AB3
P_GPP_TXN1	AC3
P_GPP_TXP2	Y1
P_GPP_TXN2	Y2
P_GPP_TXP3	V3
P_GPP_TXN3	V4
P_UMI_TXP0	AB12
P_UMI_TXN0	AC12
P_UMI_TXP1	AC11
P_UMI_TXN1	AB11
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P_UMI_TXP3	AB8
P_UMI_TXN3	AC8



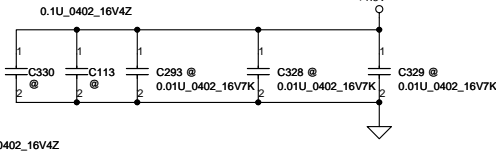
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			4019D2	
			Date: Friday, May 06, 2011	Sheet 6 of 36



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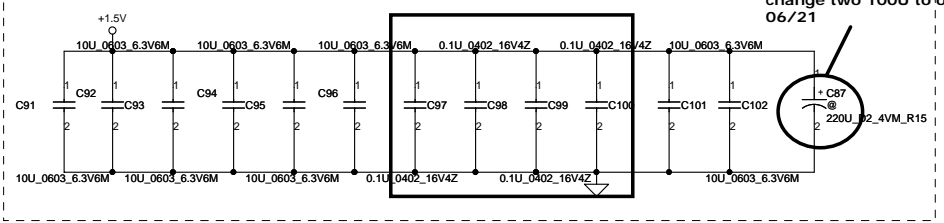


Put it between DDR3 +1.5VS shape and GND shape

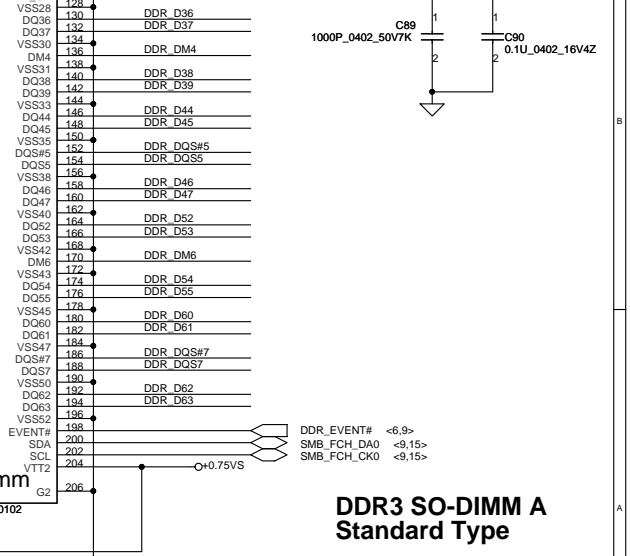
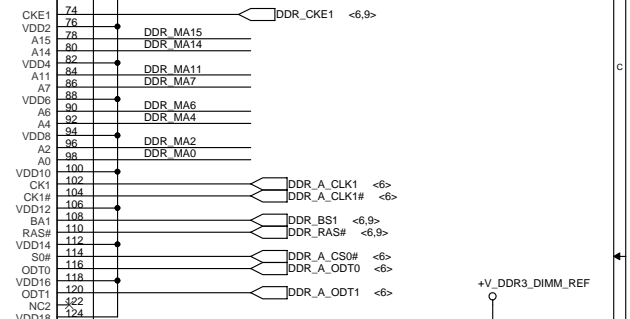
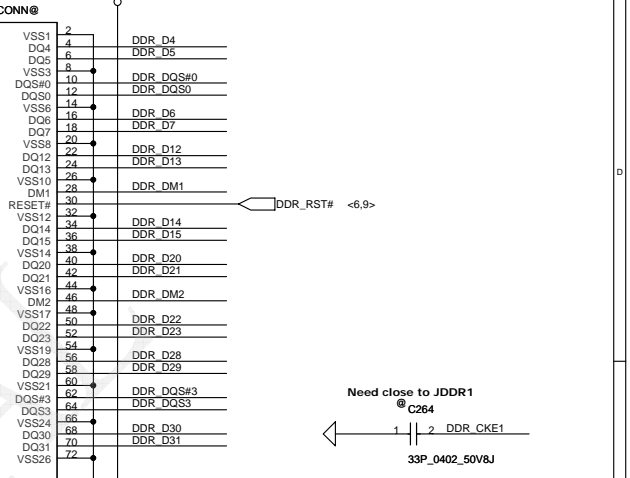
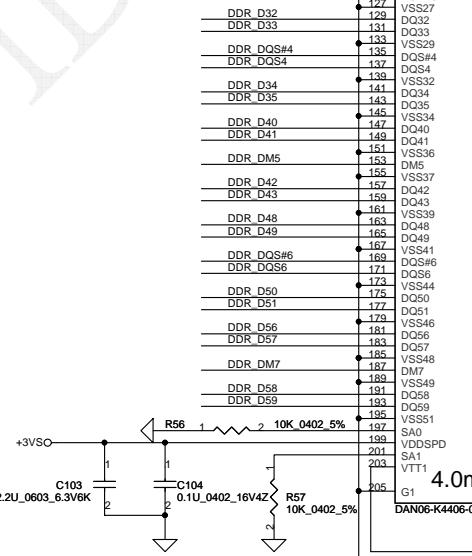
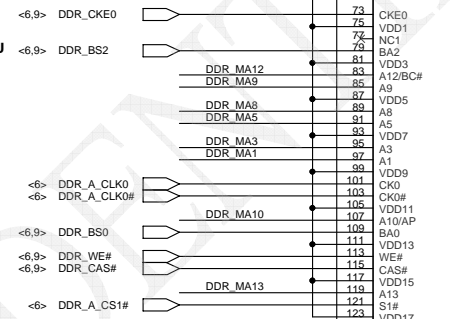
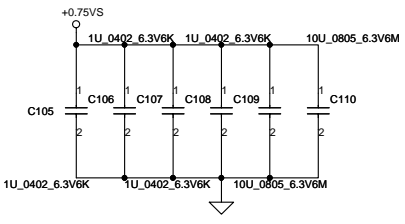


Layout Note:  
Place near JDDR1

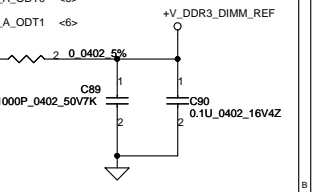
Layout Note: Place these 4 Caps near Command and Control signals of DIMM



Layout Note:  
Place near JDDR1.203 & JDDR1.204



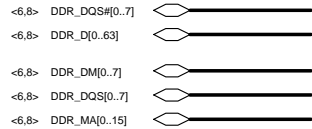
Need close to JDDR1  
C264  
33P\_0402\_50V8J



DDR3 SO-DIMM A  
Standard Type

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				Date: Friday, May 06, 2011	Sheet 8 of 36

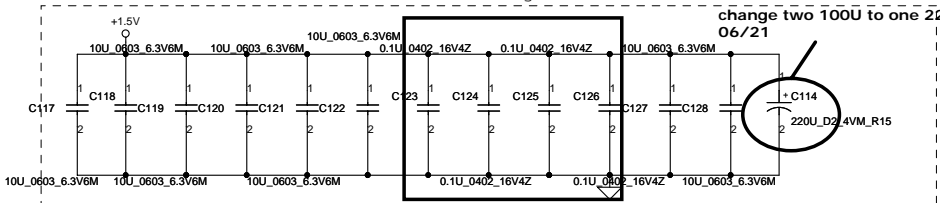




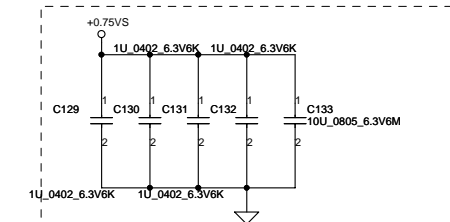
Layout Note:  
Place near JP3

Layout Note: Place these 4 Caps near Command and Control signals of DIMM

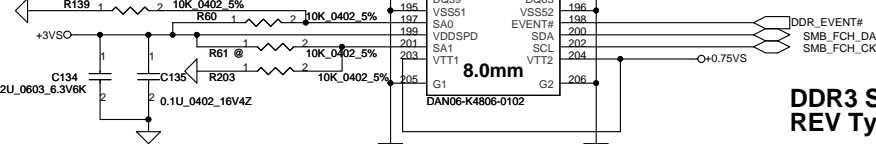
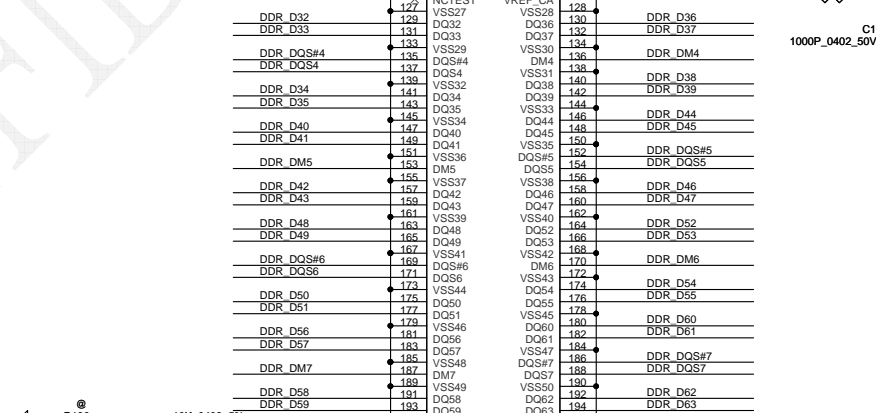
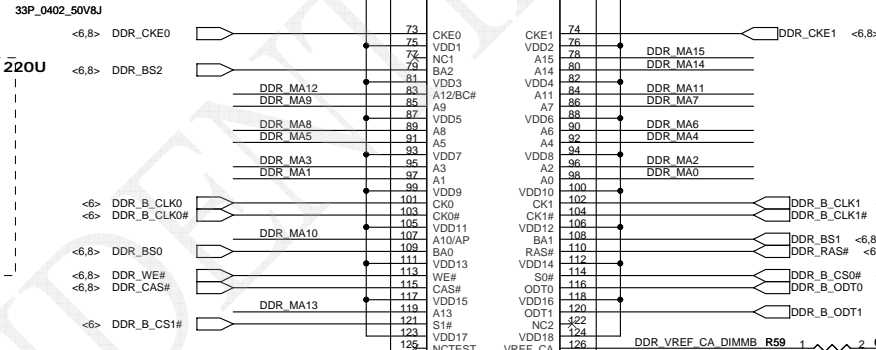
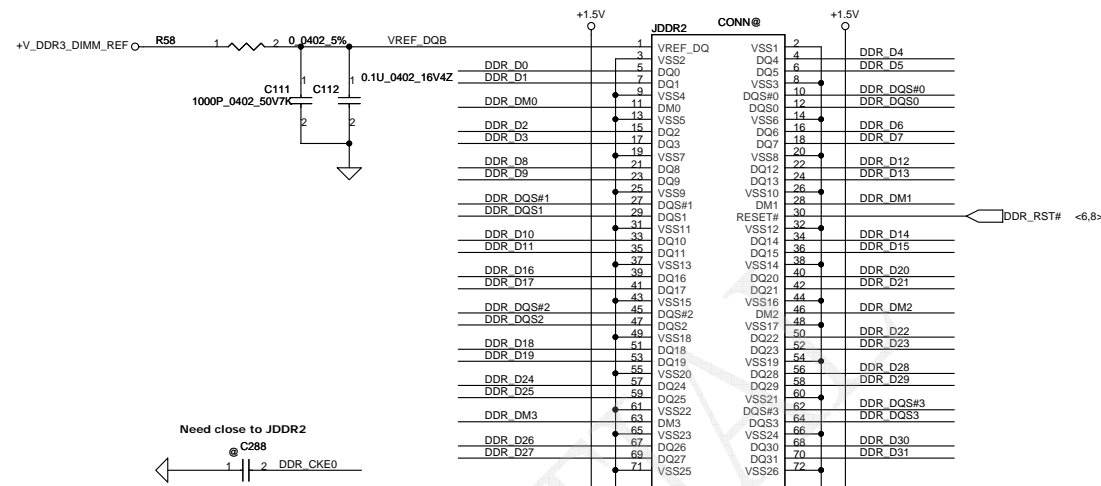
change two 100U to one 220U 06/21



Layout Note:  
Place near JP3.203 & JP3.204



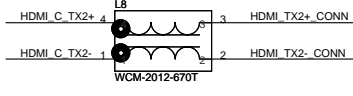
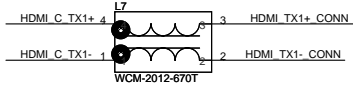
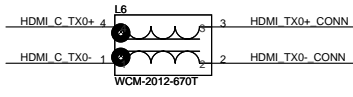
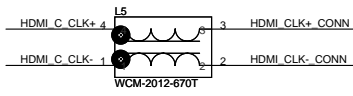
	SA0	SA1
Compal common design	0	1
ADM CRB	1	0



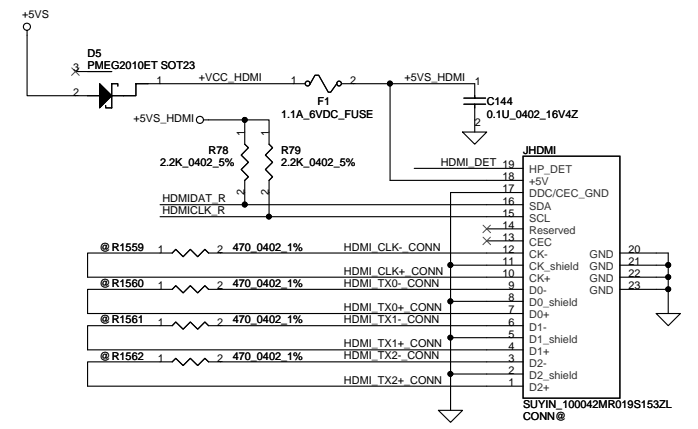
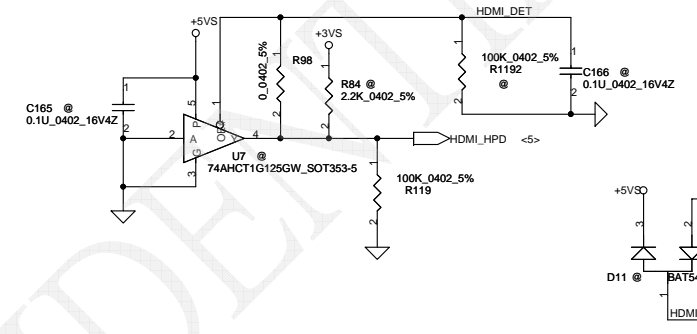
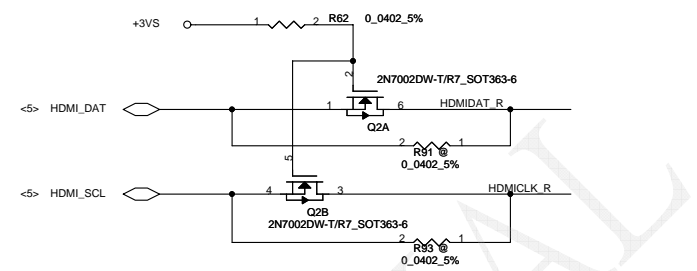
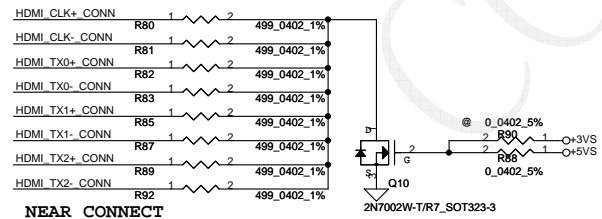
DDR3 SO-DIMM B  
REV Type

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			4019D2	B
			Date: Friday, May 06, 2011	Sheet 9 of 36

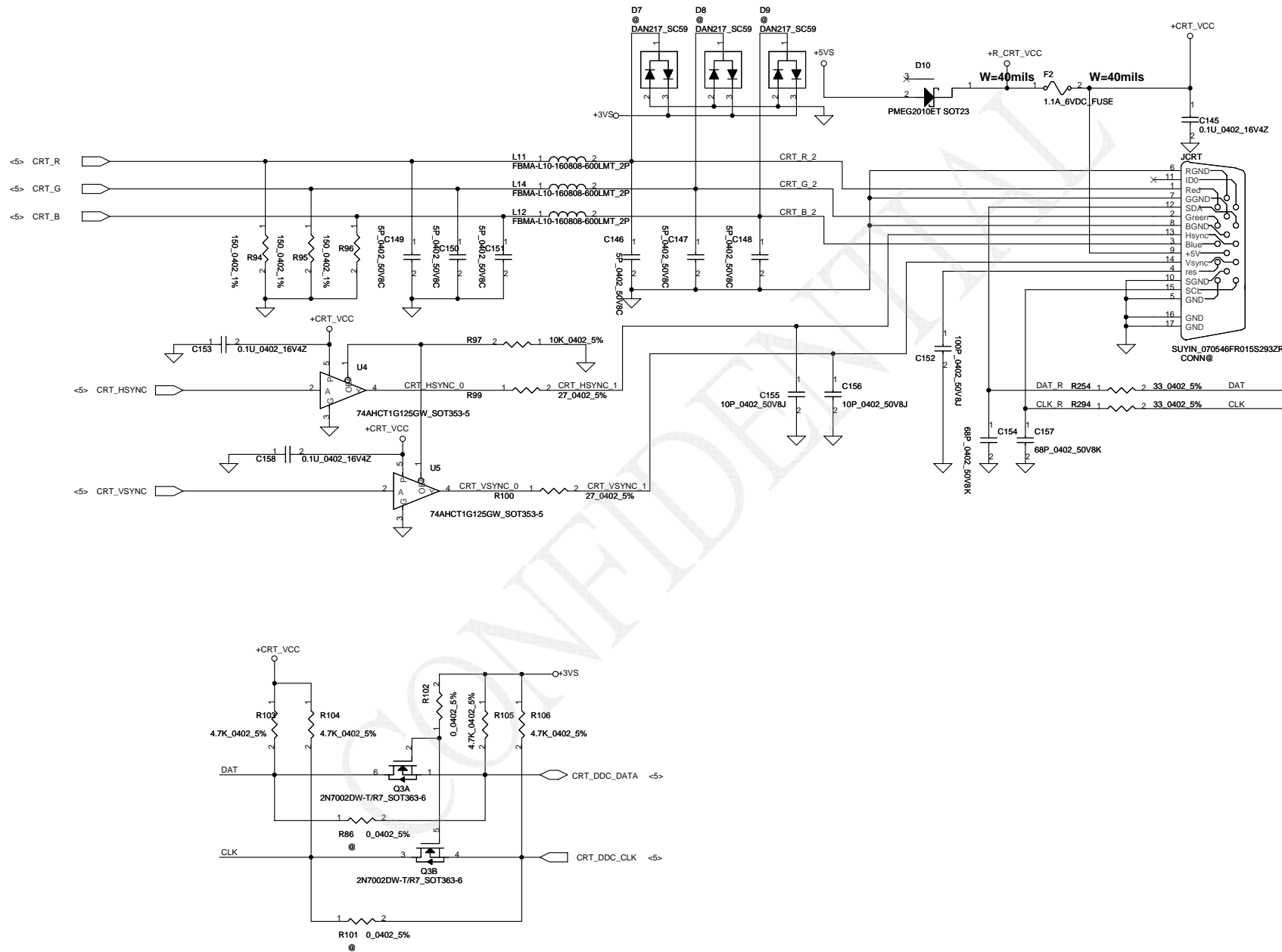
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<5>	HDMI_TX2+	HDMI_TX2+	C138	1	2	0.1U_0402_16V7K	HDMI_C_TX2+
<5>	HDMI_TX2-	HDMI_TX2-	C139	1	2	0.1U_0402_16V7K	HDMI_C_TX2-
<5>	HDMI_TX1+	HDMI_TX1+	C140	1	2	0.1U_0402_16V7K	HDMI_C_TX1+
<5>	HDMI_TX1-	HDMI_TX1-	C141	1	2	0.1U_0402_16V7K	HDMI_C_TX1-
<5>	HDMI_TX0+	HDMI_TX0+	C142	1	2	0.1U_0402_16V7K	HDMI_C_TX0+
<5>	HDMI_TX0-	HDMI_TX0-	C143	1	2	0.1U_0402_16V7K	HDMI_C_TX0-



HDMI_C_CLK+	@	R65	1	2	0.0402_5%	HDMI_CLK+ CONN
HDMI_C_CLK-	@	R66	1	2	0.0402_5%	HDMI_CLK- CONN
HDMI_C_TX0+	@	R67	1	2	0.0402_5%	HDMI_TX0+ CONN
HDMI_C_TX0-	@	R68	1	2	0.0402_5%	HDMI_TX0- CONN
HDMI_C_TX1+	@	R71	1	2	0.0402_5%	HDMI_TX1+ CONN
HDMI_C_TX1-	@	R72	1	2	0.0402_5%	HDMI_TX1- CONN
HDMI_C_TX2+	@	R73	1	2	0.0402_5%	HDMI_TX2+ CONN
HDMI_C_TX2-	@	R75	1	2	0.0402_5%	HDMI_TX2- CONN

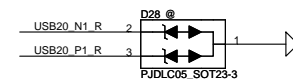
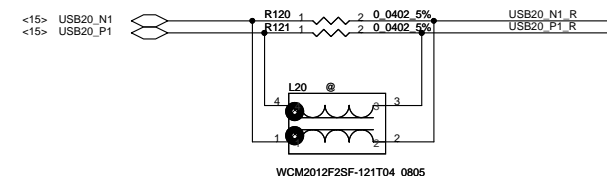
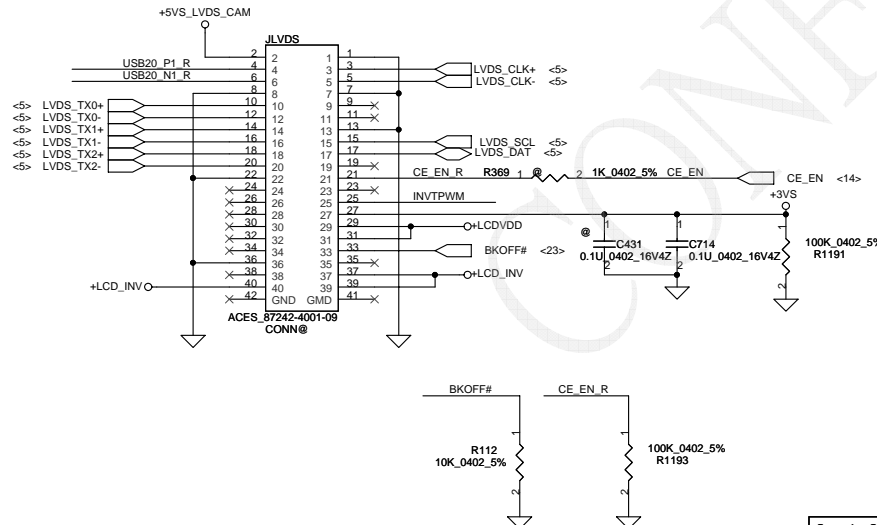
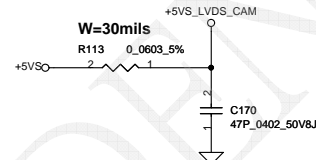
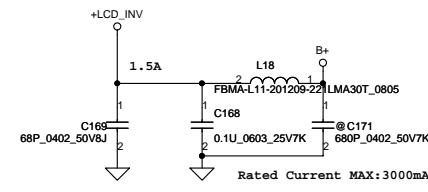
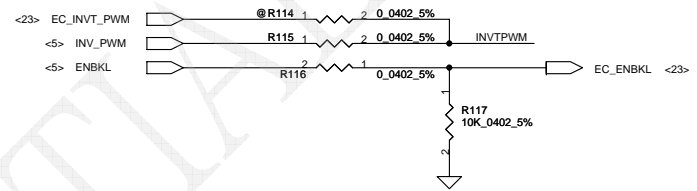
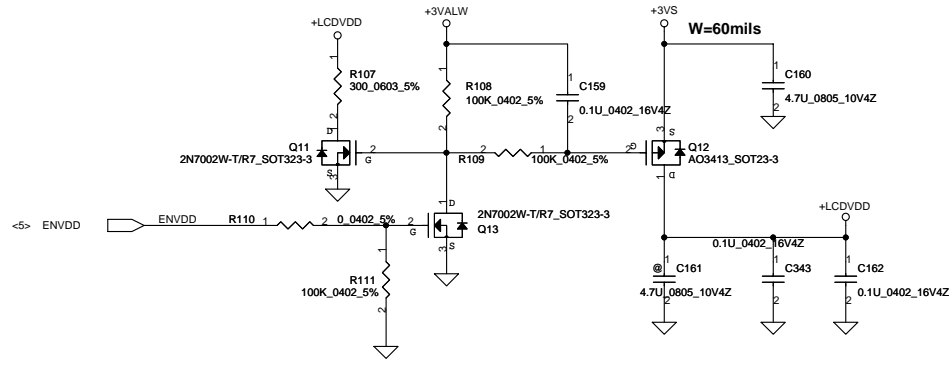


# CRT Connector



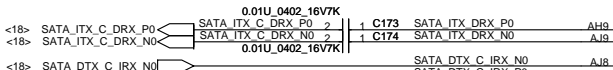
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			4019D2	
			Date: Friday, May 06, 2011	Sheet 11 of 36

# LCD POWER CIRCUIT

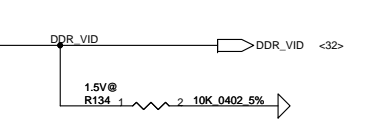
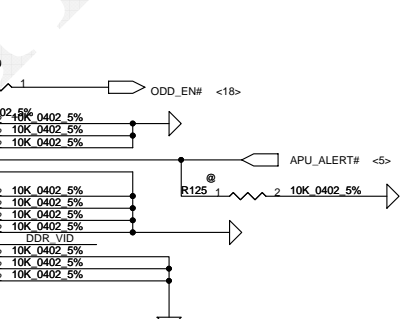
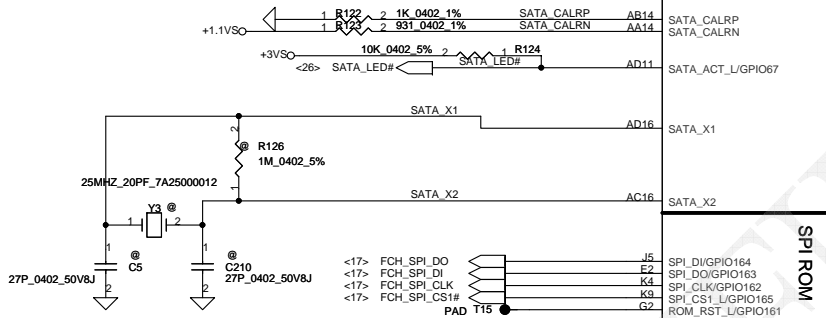
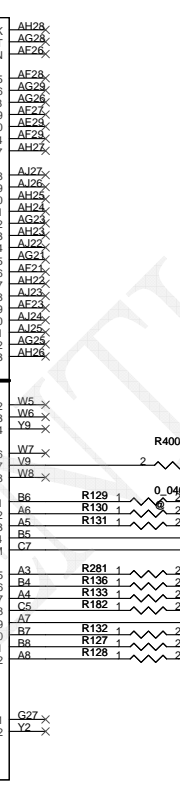
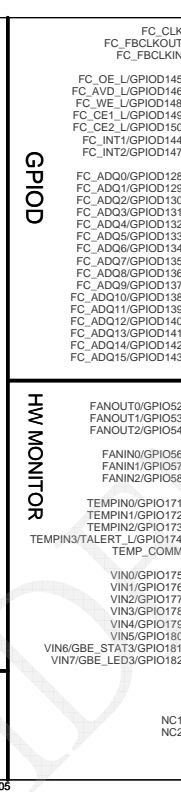
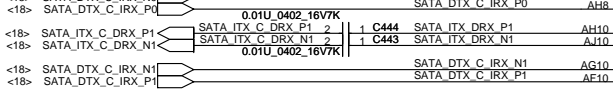


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				4019D2	B
Date: Friday, May 06, 2011				Sheet	12 of 36

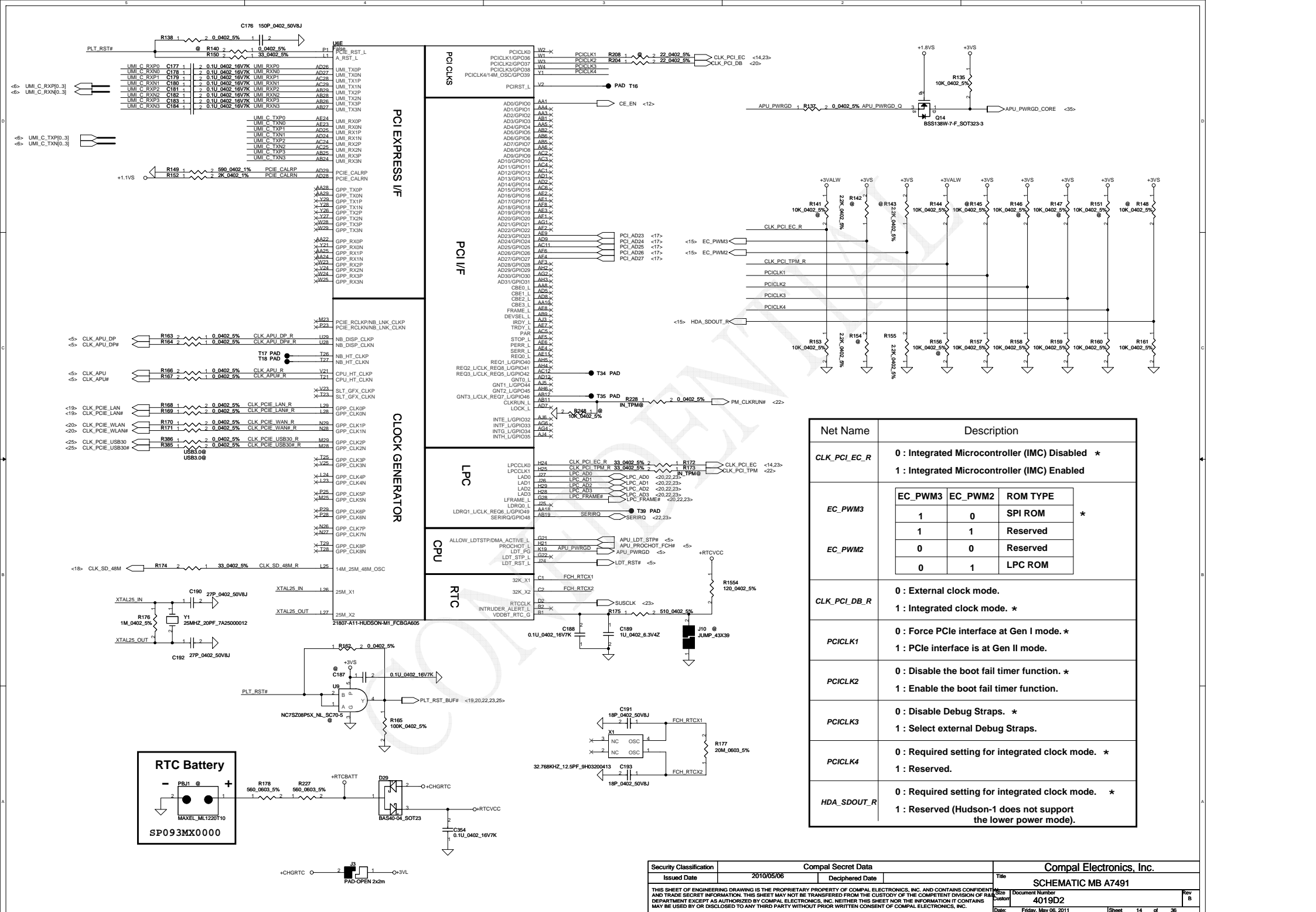
SATA for HDD



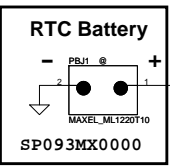
SATA for ODD

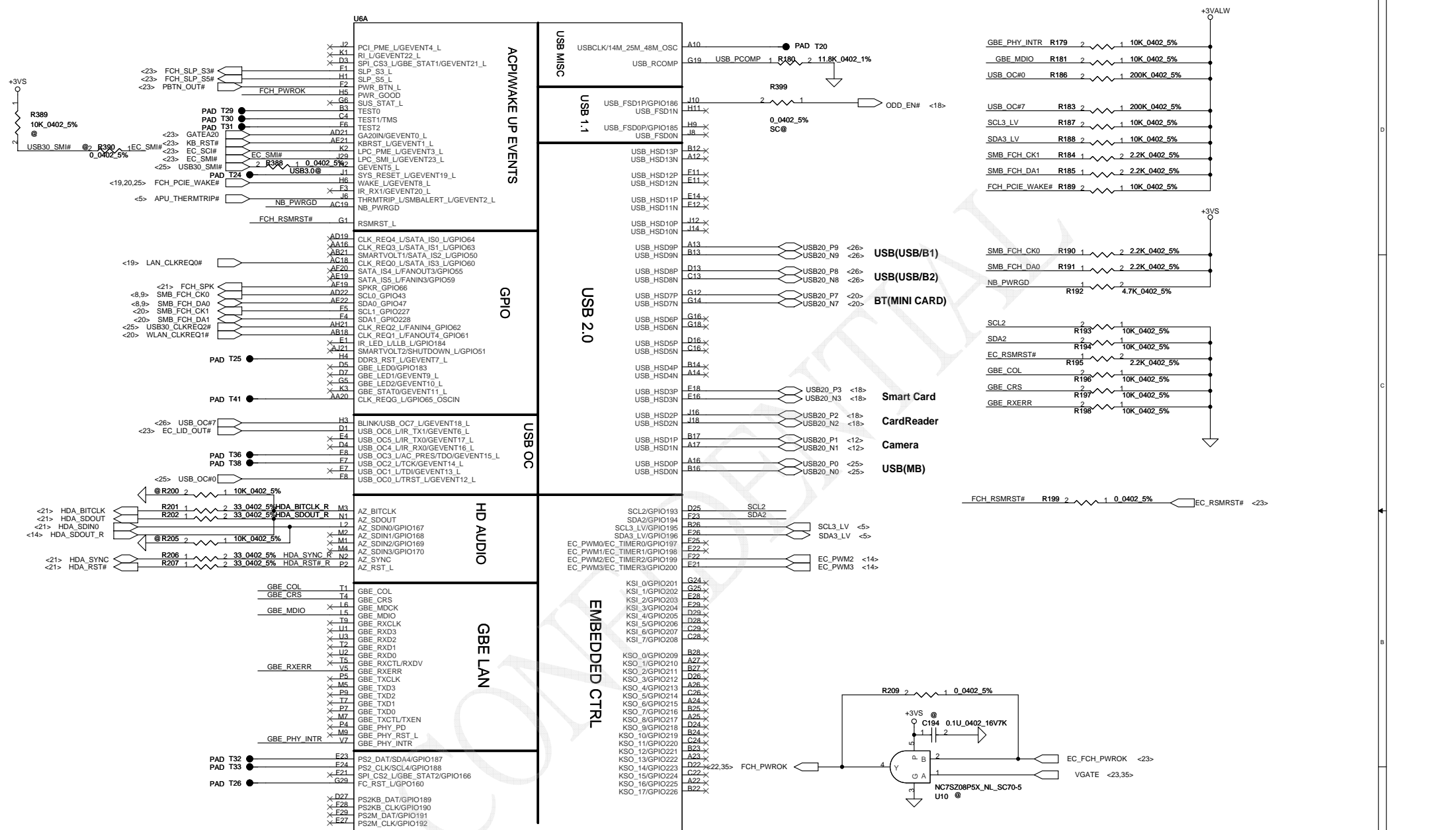


DDR_VID	DDR voltage
0	+1.5V
1	+1.35V



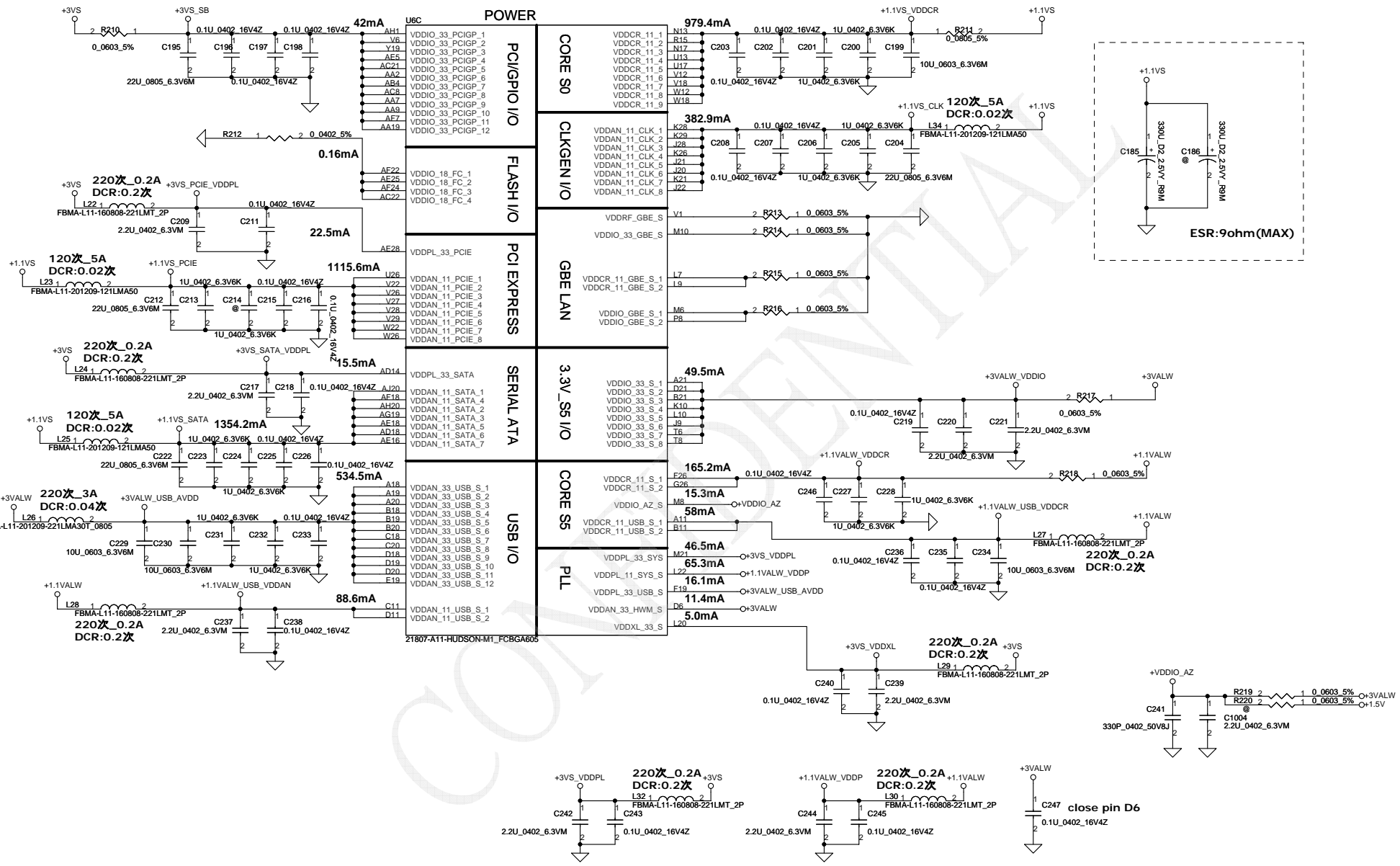
Net Name	Description															
<b>CLK_PCI_EC_R</b>	0 : Integrated Microcontroller (IMC) Disabled * 1 : Integrated Microcontroller (IMC) Enabled															
<b>EC_PWM3</b>	<table border="1"> <thead> <tr> <th>EC_PWM3</th> <th>EC_PWM2</th> <th>ROM TYPE</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>SPI ROM *</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>LPC ROM</td> </tr> </tbody> </table>	EC_PWM3	EC_PWM2	ROM TYPE	1	0	SPI ROM *	1	1	Reserved	0	0	Reserved	0	1	LPC ROM
EC_PWM3	EC_PWM2	ROM TYPE														
1	0	SPI ROM *														
1	1	Reserved														
0	0	Reserved														
0	1	LPC ROM														
<b>CLK_PCI_DB_R</b>	0 : External clock mode. 1 : Integrated clock mode. *															
<b>PCICLK1</b>	0 : Force PCIe interface at Gen I mode. * 1 : PCIe interface is at Gen II mode.															
<b>PCICLK2</b>	0 : Disable the boot fail timer function. * 1 : Enable the boot fail timer function.															
<b>PCICLK3</b>	0 : Disable Debug Straps. * 1 : Select external Debug Straps.															
<b>PCICLK4</b>	0 : Required setting for integrated clock mode. * 1 : Reserved.															
<b>HDA_SDOUT_R</b>	0 : Required setting for integrated clock mode. * 1 : Reserved (Hudson-1 does not support the lower power mode).															





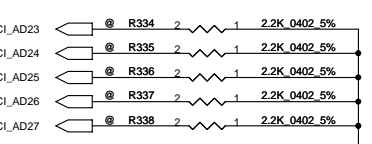
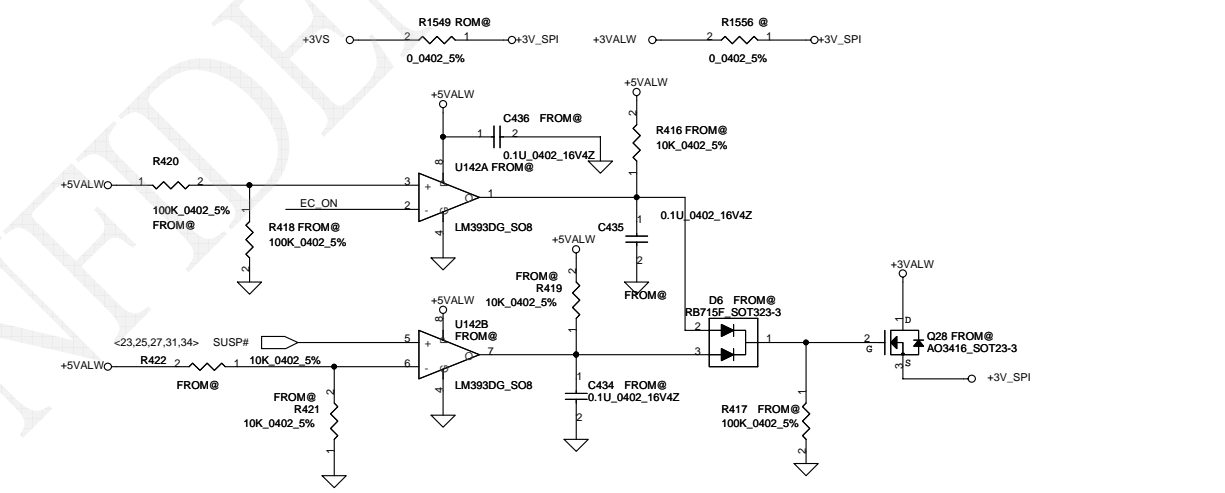
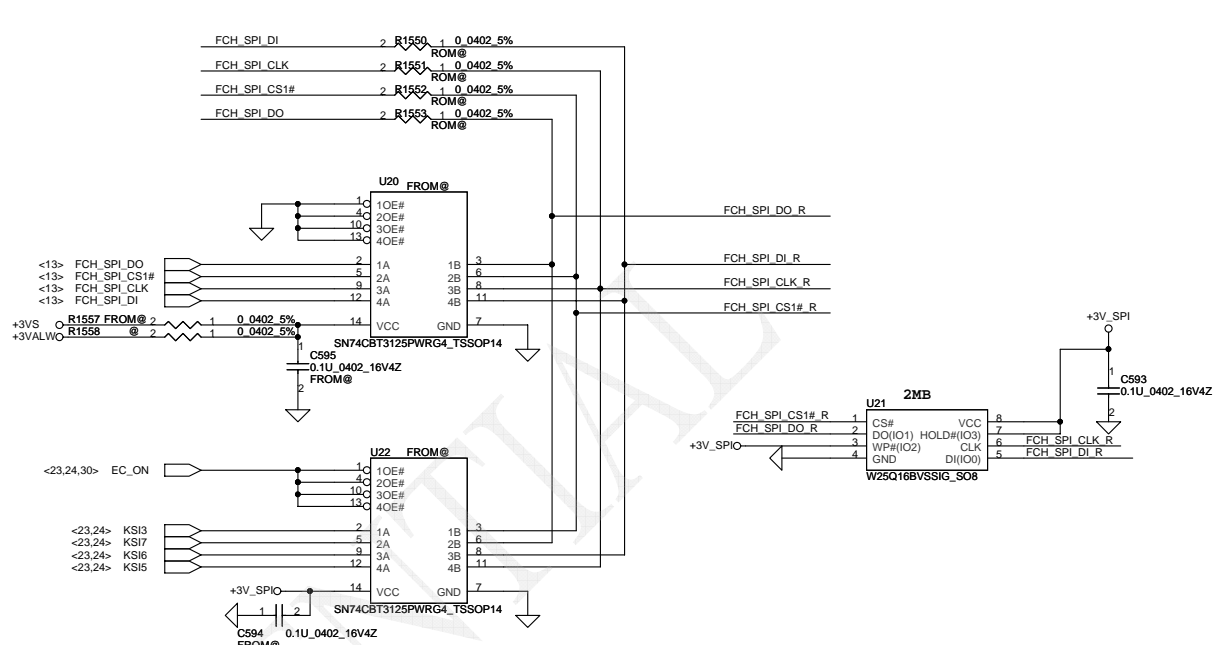
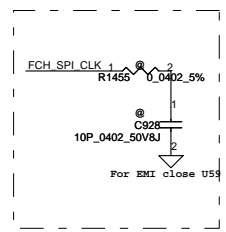
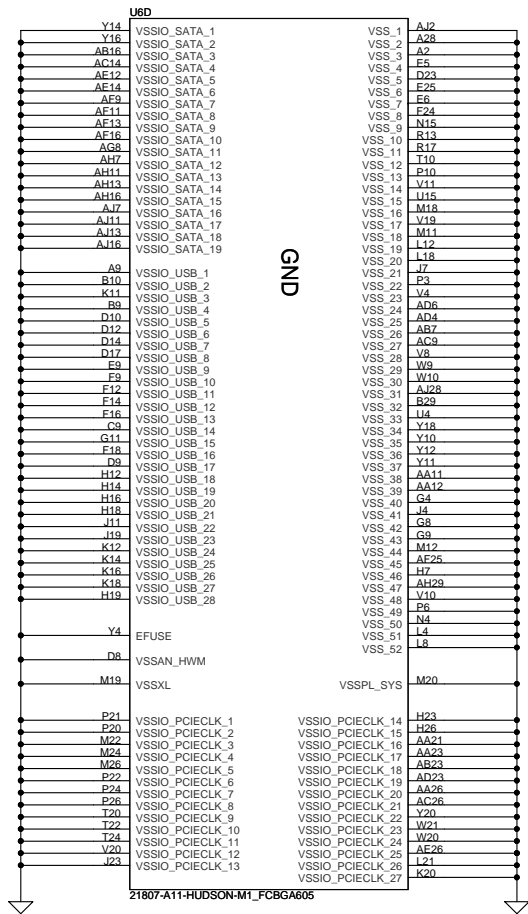
21807-A11-HUDSON-M1\_FCBGA605

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				4019D2	
				Date: Friday, May 06, 2011	Sheet 15 of 36

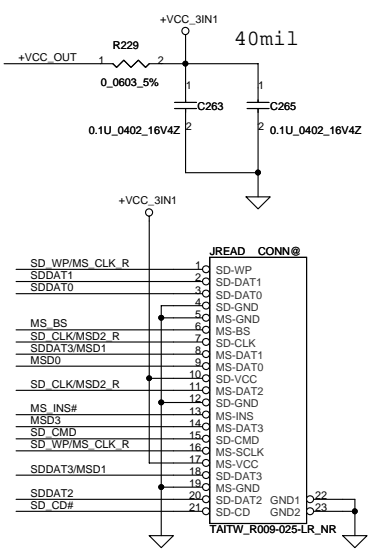
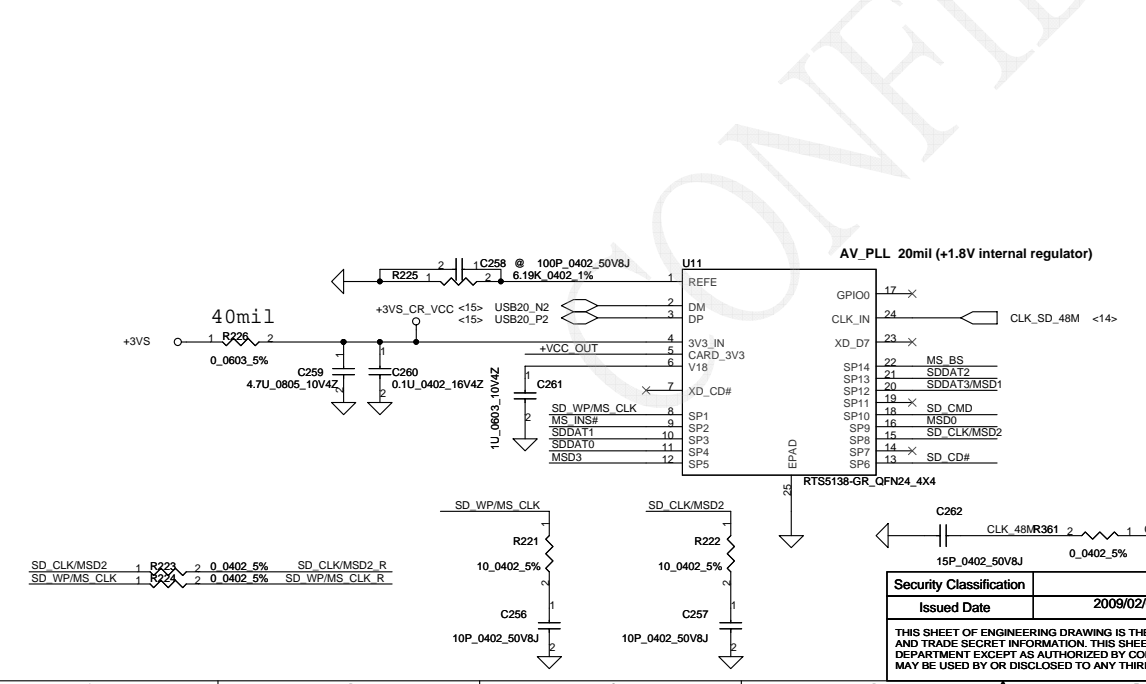
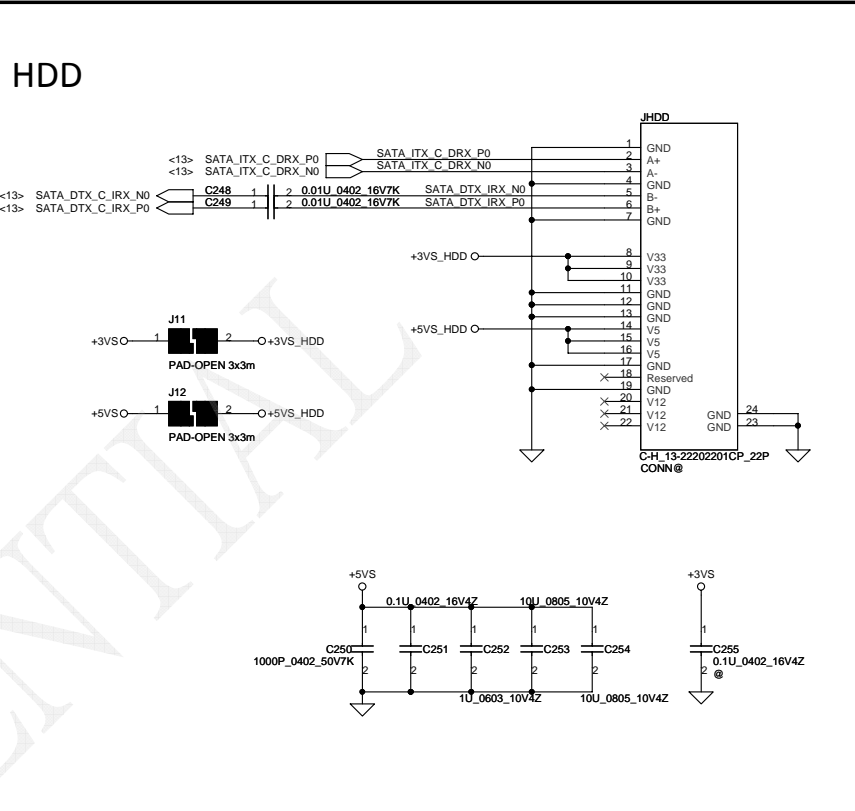
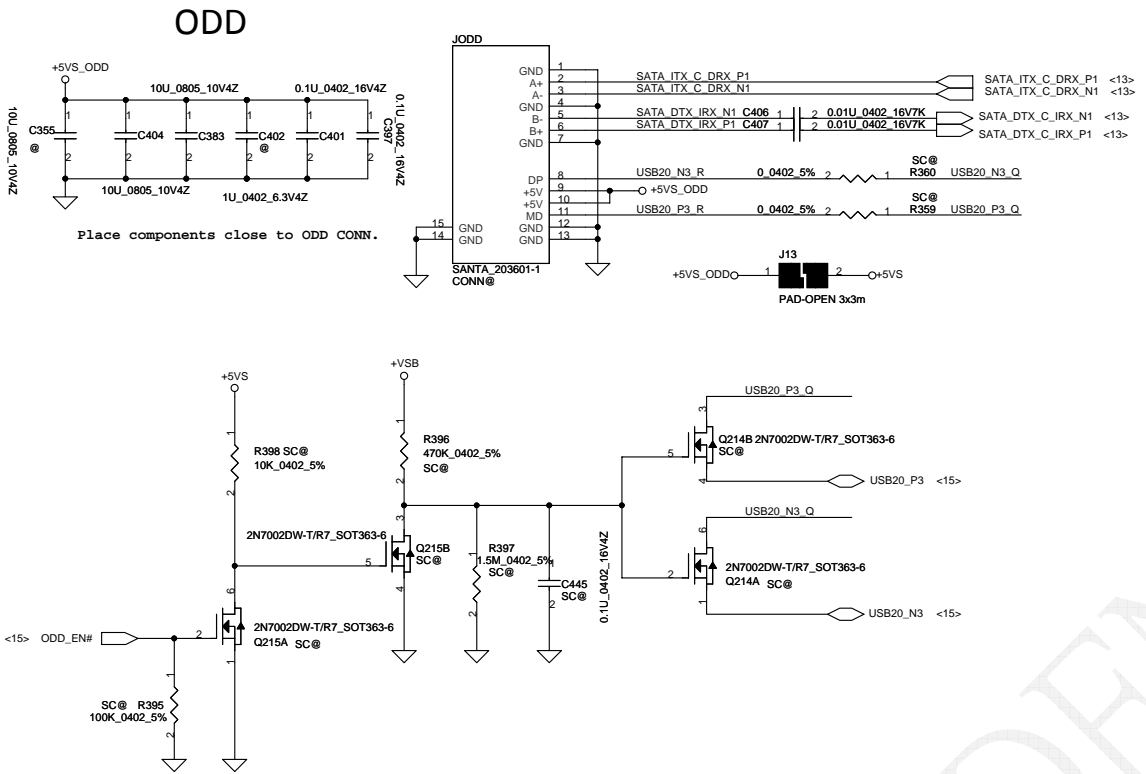


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Document Number	4019D2			Rev B
Date:	Friday, May 06, 2011	Sheet	16 of 36	





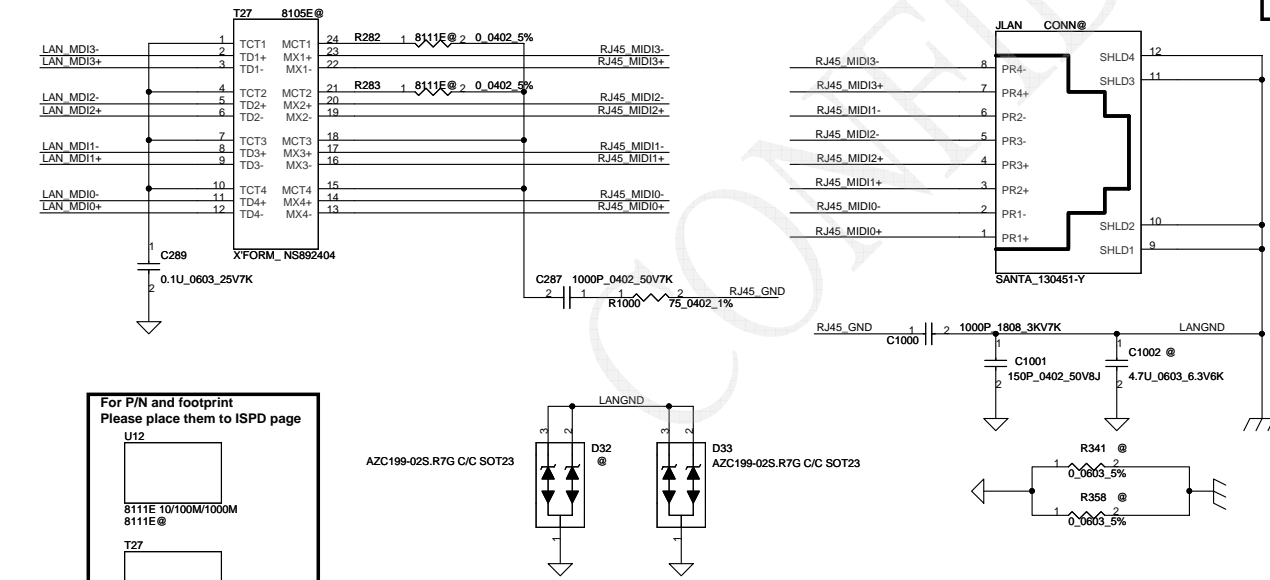
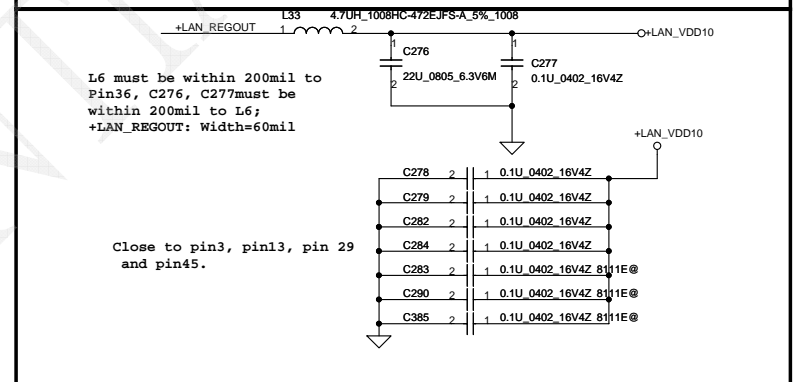
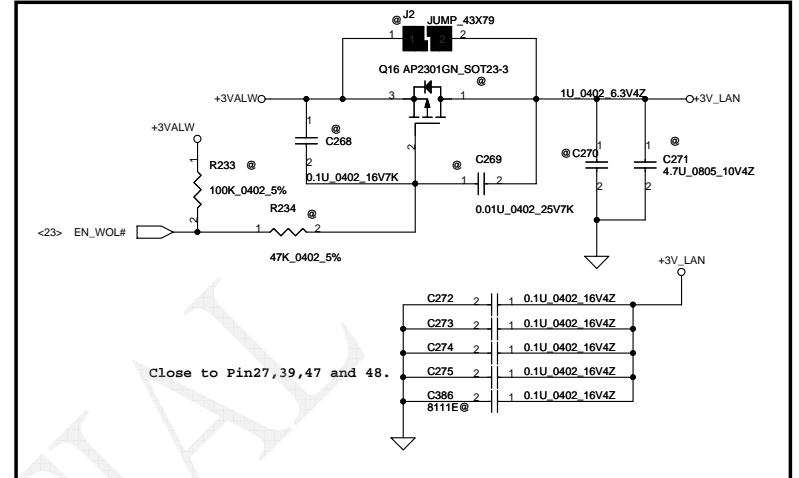
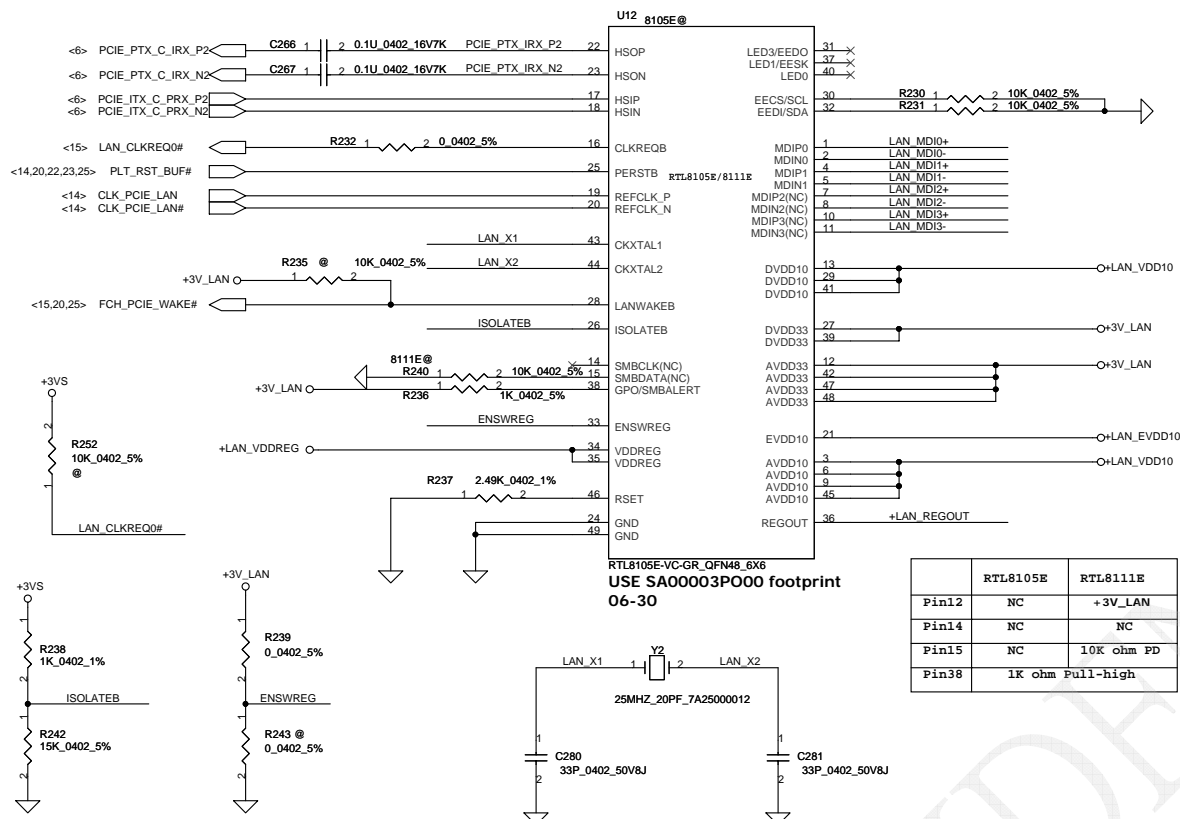
Net Name	Description
PCI_AD27	0 : Bypass internal PLL clock 1 : Use internal PLL-generated PLL CLK *
PCI_AD26	0 : ILA auto run enable 1 : ILA auto run disable *
PCI_AD25	0 : Bypass internal FC Clk 1 : Use internal PLL FC Clk * NEED CHECK
PCI_AD24	0 : Getting the value from I2C EPROM 1 : Disable I2C ROM * NEED CHECK
PCI_AD23	0 : Reserved 1 : Required setting (use ROMTYPE straps to * determine the ROM type)



**SD,MMC,MS multi-function pin define**

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1	SP1		SP1
SP2			
SP3			
SP4			
SP5			
SP6			
SP7			
SP8			
SP9			
SP10			
SP11			
SP12			
SP13			
SP14			
SP15			
SP16			
SP17			
SP18			
SP19			

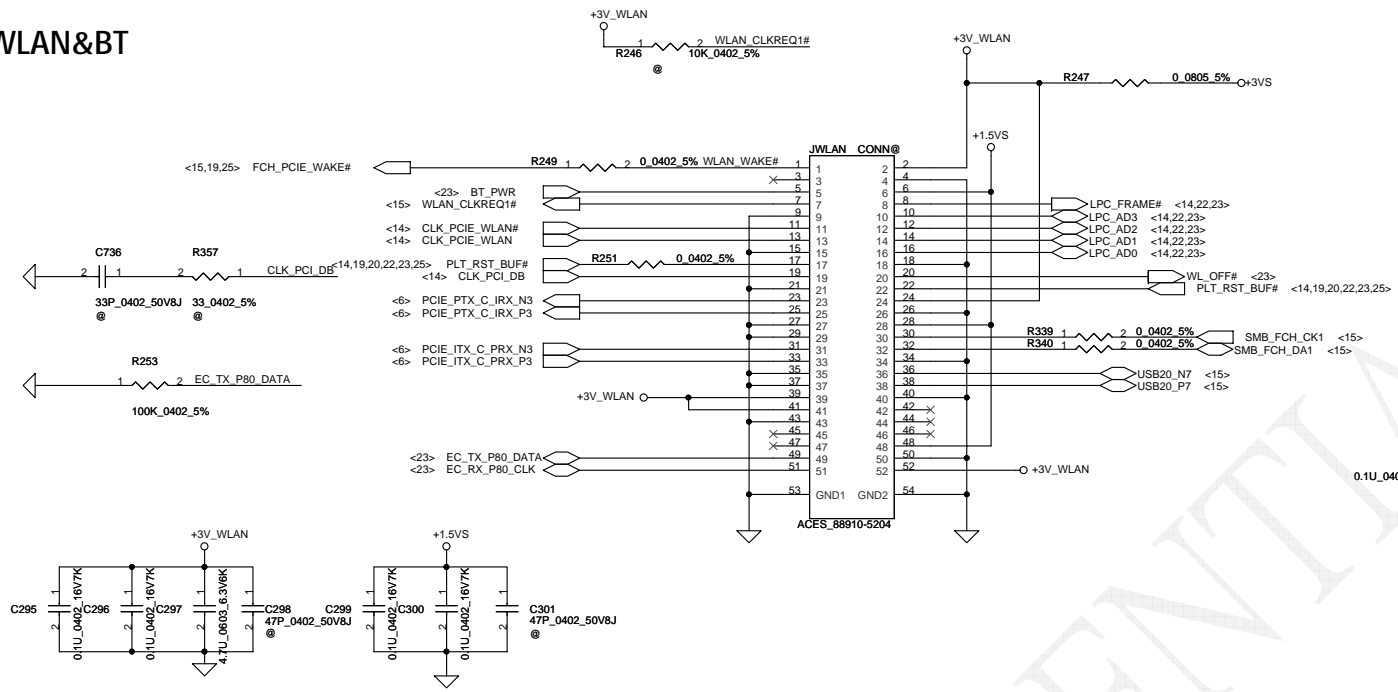
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<b>Date</b>		<b>Friday, May 06, 2011</b>	
<b>Sheet</b>		<b>18 of 36</b>	



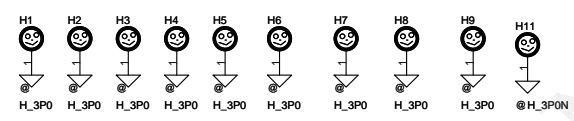
For P/N and footprint  
Please place them to ISPD page  
U12  
8111E 10/100M/1000M  
8111E@  
T27  
10/100M/1000M transformer  
8111E@

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				Customer	4019D2
				Date:	Sheet 19 of 36

# WLAN&BT



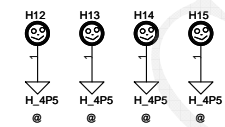
## Screw Hole



## NPTH



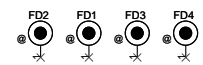
## CPU



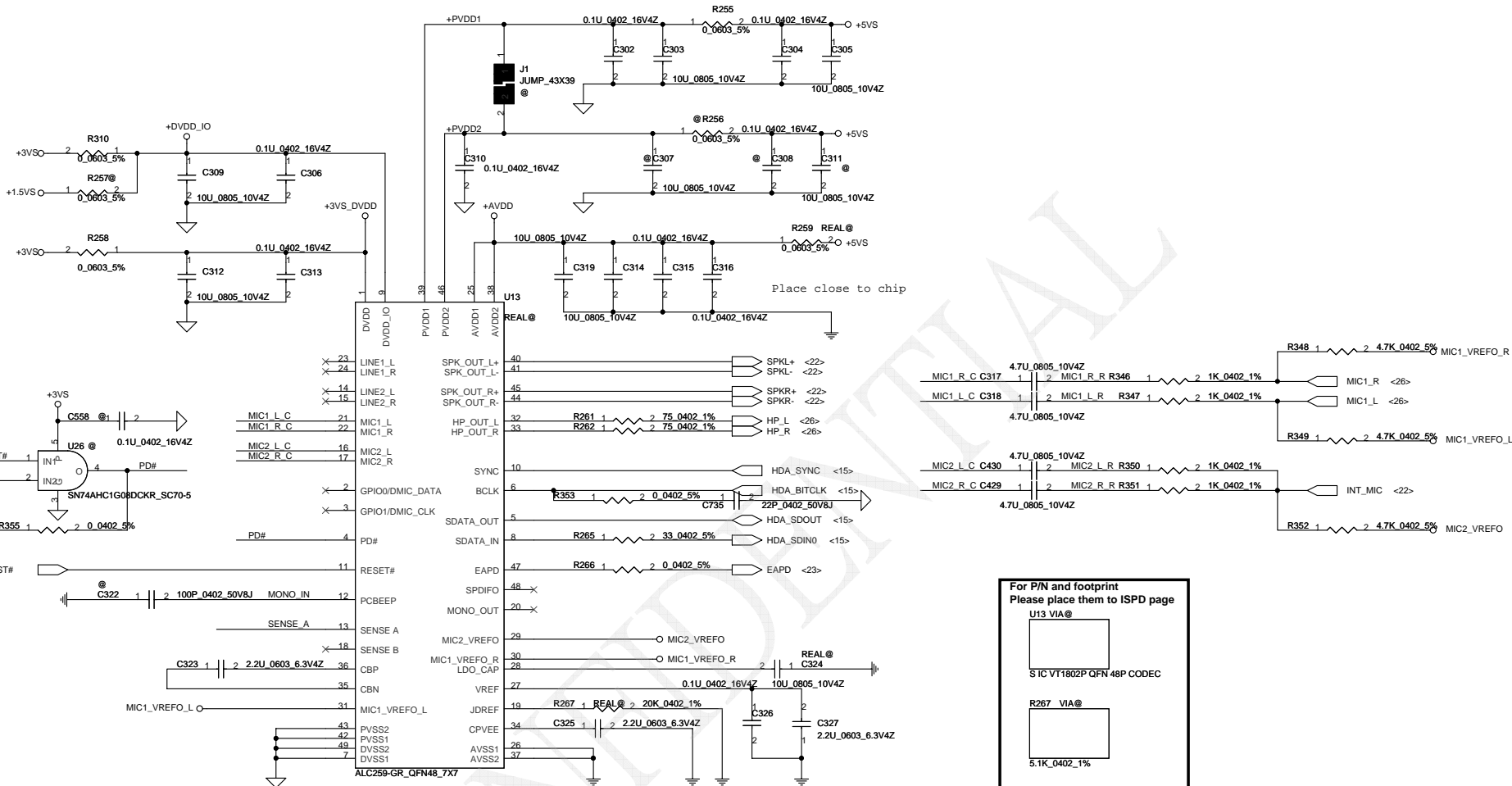
## JWLAN



## PCB Fedical Mark PAD



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Date:				Sheet	20 of 36

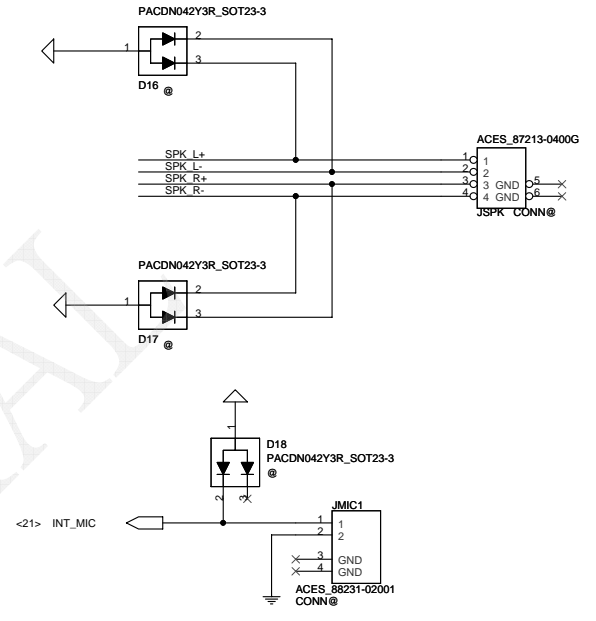
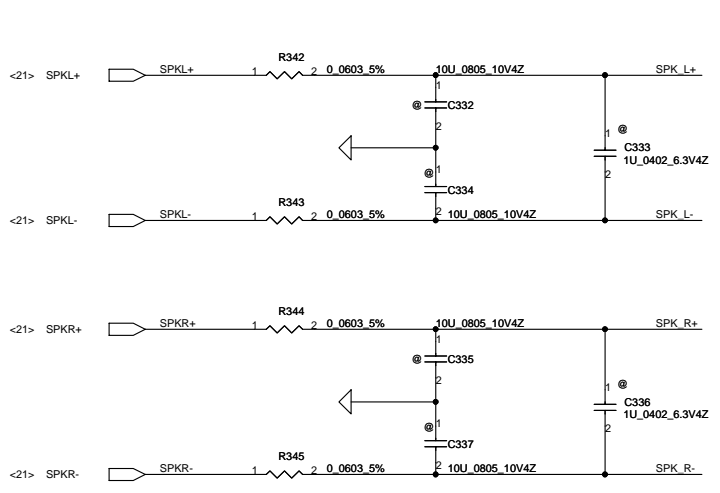


For P/N and footprint  
Please place them to ISPD page  
U13 VIA@  
S IC VT1802P QFN 48P CODEC  
R267 VIA@  
5.1K\_0402\_1%

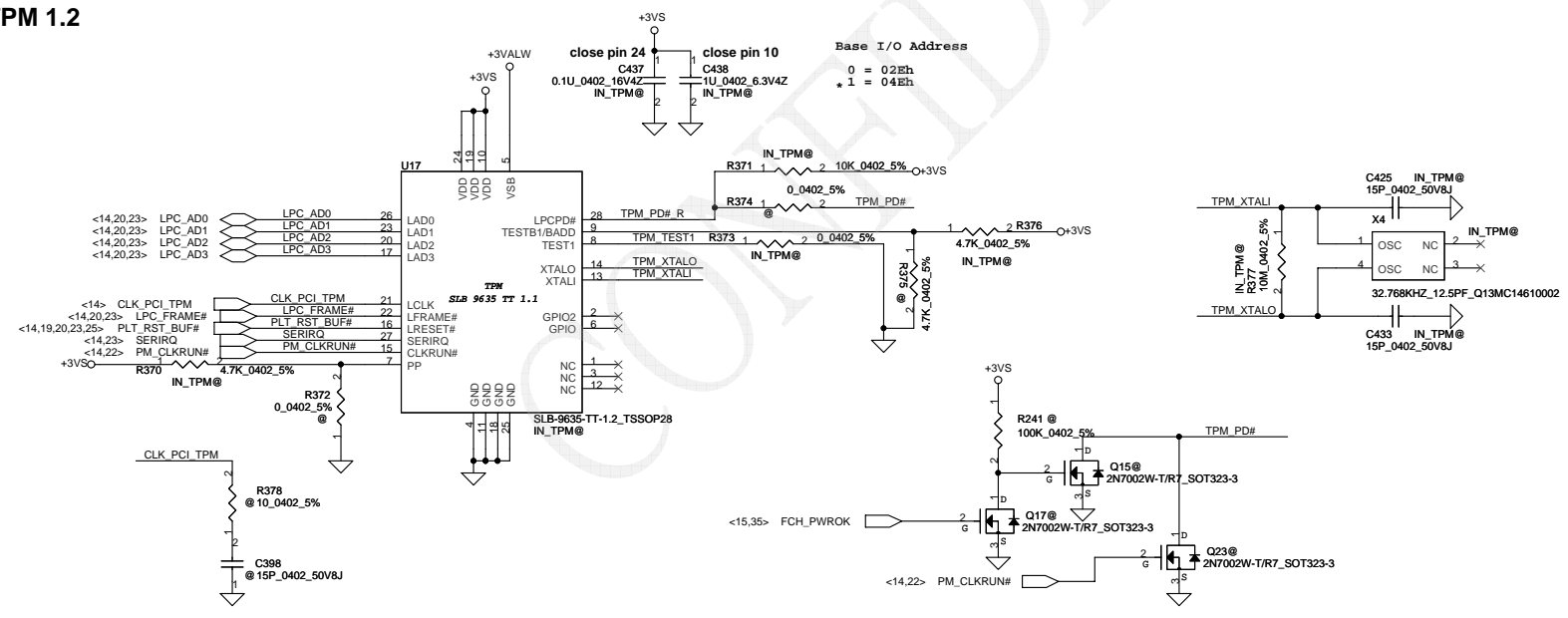
USE SA00003QR00 footprint

Sense Pin	Impredance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32,33)	Headphone out
	20K	PORT-I (PIN 21,22)	EXT.MIC
	10K		
	5.1K		
SENSE B	39.2K		
	20K		
	10K		
	5.1K		

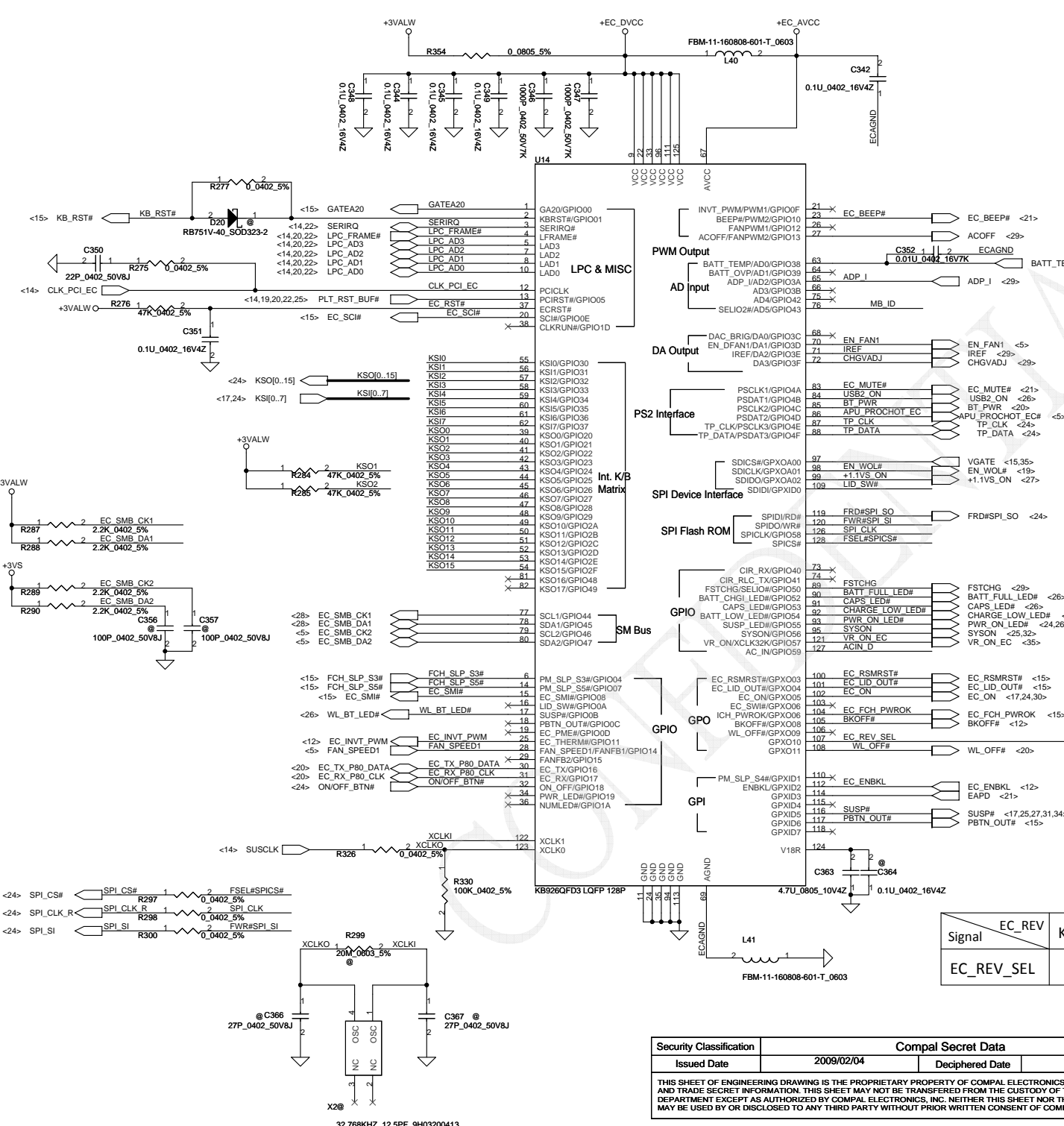
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Date:	Friday, May 06, 2011		Sheet	21 of 36		



**TPM 1.2**

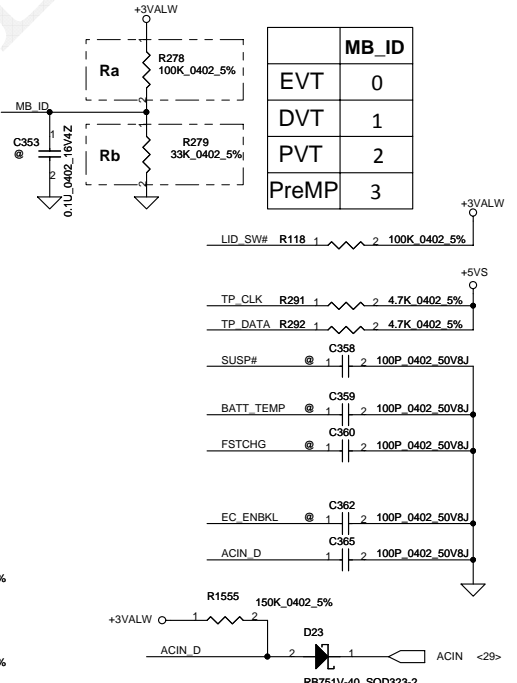


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			4019D2	
			Date: Friday, May 06, 2011	Sheet 22 of 36

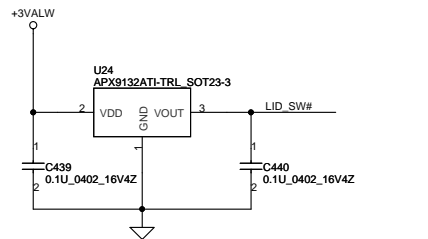


**Board ID / SKU ID Table for AD channel**

Vcc	3.3V			
Ra	100K 5%			
Board ID	Rb / Rd	VAD_BRD min	VAD_BRD typ	VAD_BRD max
0	0	0V	0V	0V
1	8.2K 5%	0.216V	0.250V	0.289V
2	18K 5%	0.436V	0.503V	0.538V
3	33K 5%	0.712V	0.819V	0.875V
4	56K 5%	1.036V	1.185V	1.264V
5	100K 5%	1.453V	1.650V	1.759V
6	200K 5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V



### LID SWITCH

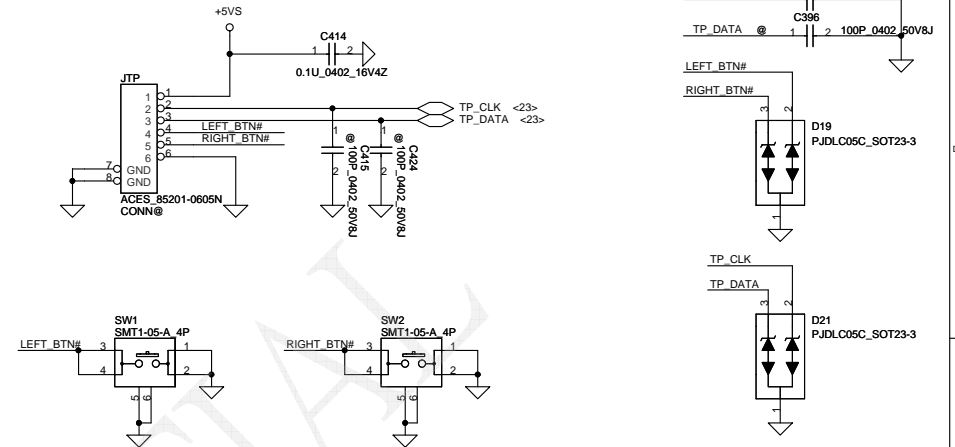
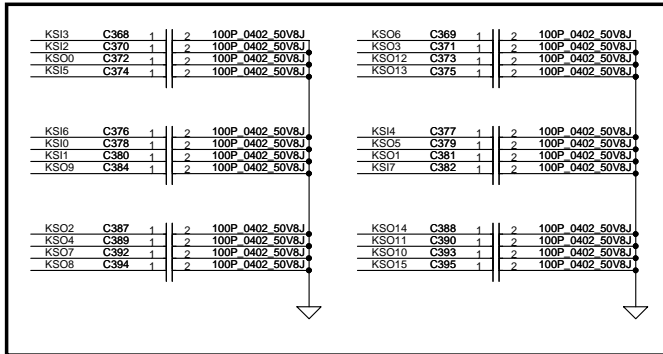
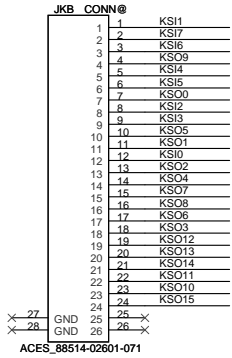
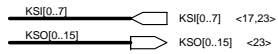


Signal	KB926 D3	KB926 E0
EC_REV_SEL	1	0

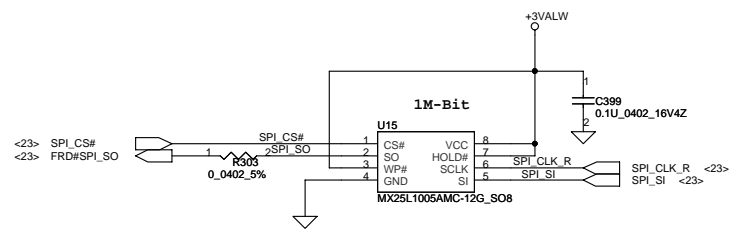
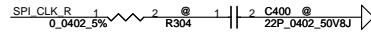
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Document Number	4019D2		Rev	B	
Date	Friday, May 06, 2011	Sheet	23	of 36	

32.768KHz\_12.5PF\_9H03200413

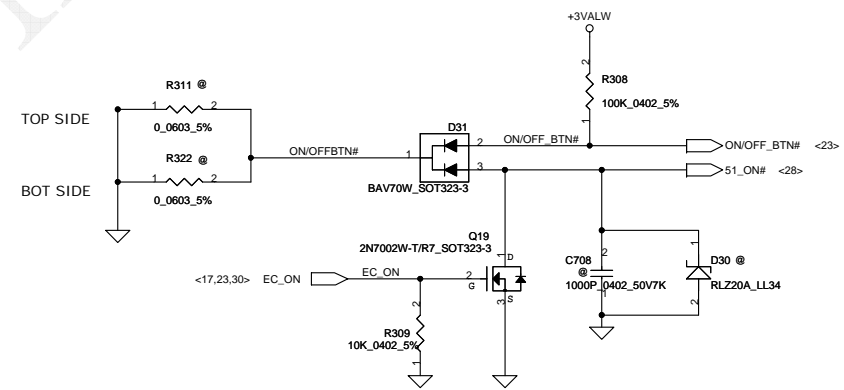
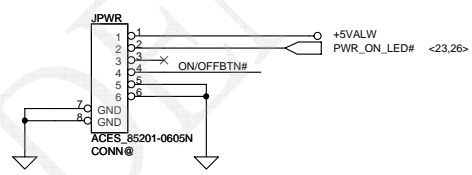
# INT\_KBD Conn.



# EC ROM



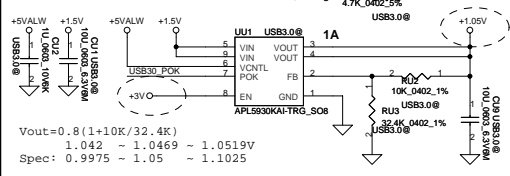
# Power BTN Board Conn



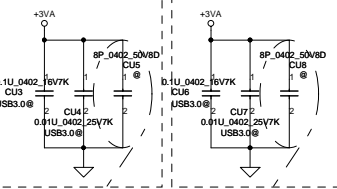
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Date:	Friday, May 06, 2011	Sheet	24	of	36	Rev B



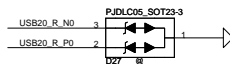
# +1.5V to +1.05V Transfer



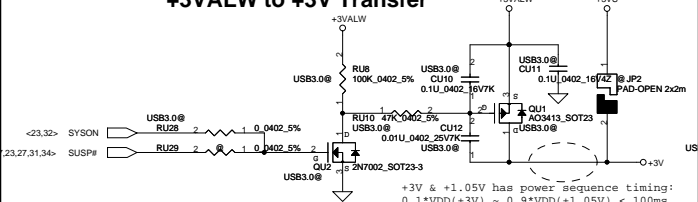
Close to U102.D7 Close to U102.P13



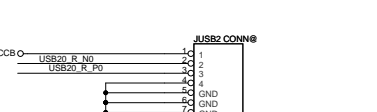
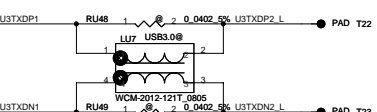
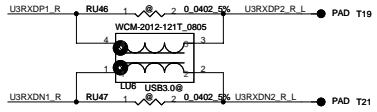
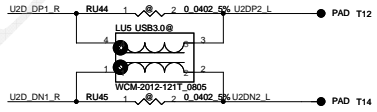
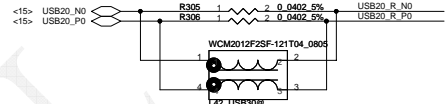
Follow Vendor recommend.



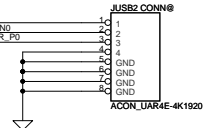
# +3VALW to +3V Transfer



+3V:200mA +1.05V:80mA



must be close to JUSB30



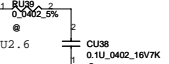
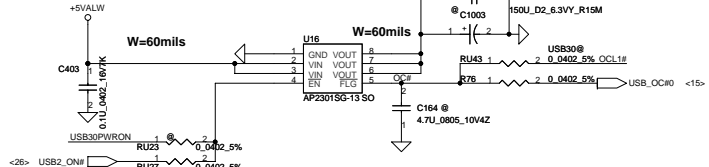
Place as close as possible to U22.N14 and U22.M14

CSEL=0 : 24MHZ XTAL CSEL=1 : 48MHZ Clock

2.5A

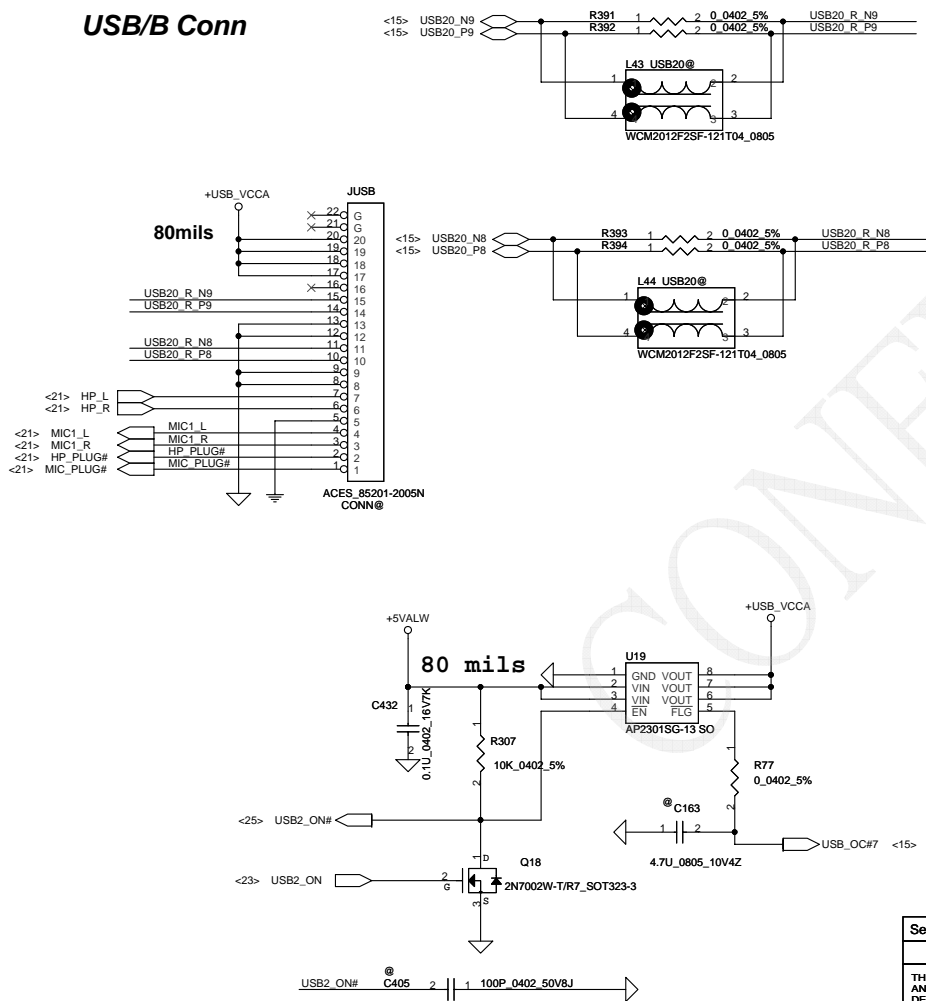
W=60mils

W=60mils



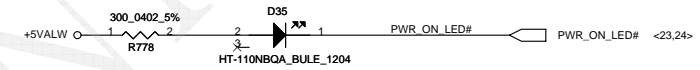
Close to U22.6

### USB/B Conn



### LEDs

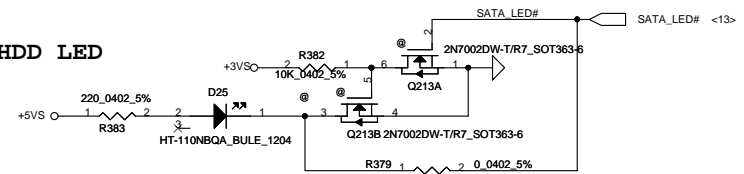
#### Power on LED



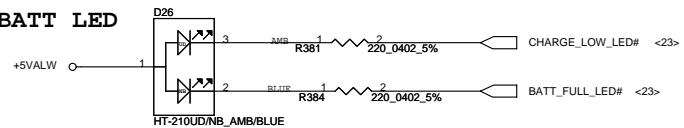
#### WL&BT LED



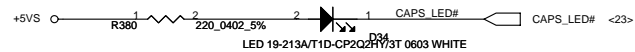
#### HDD LED



#### BATT LED

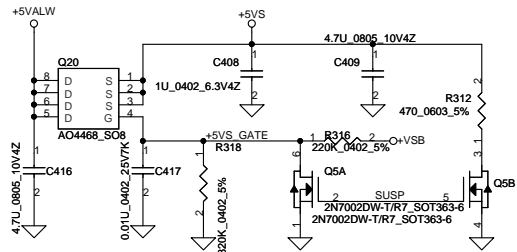


#### CAP LOCK LED

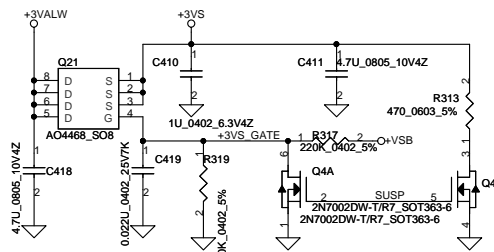


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Date: Friday, May 06, 2011				Rev B
Sheet 26 of 36				

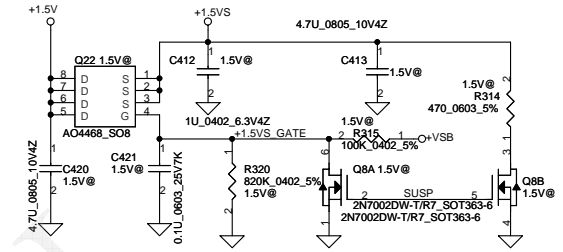
**+5VALW TO +5VS**



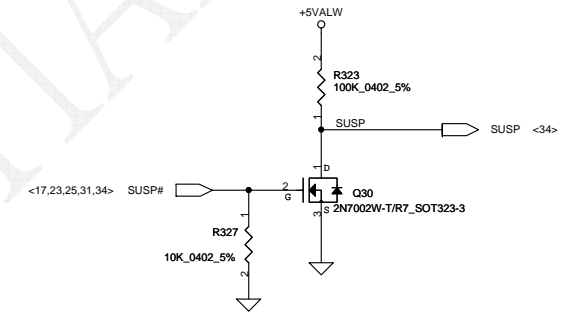
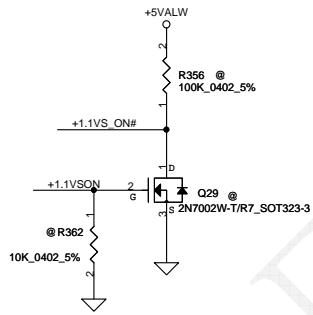
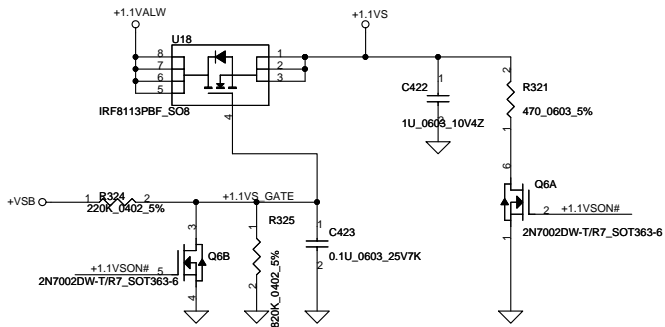
**+3VALW TO +3VS**



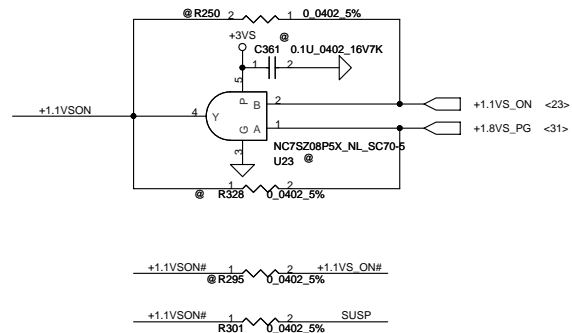
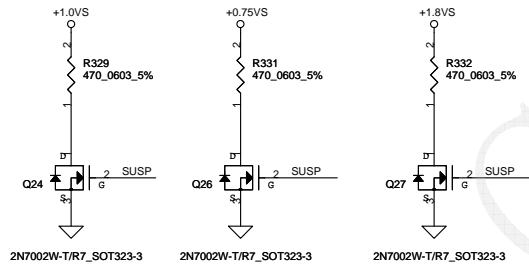
**+1.5V TO +1.5VS**



**+1.1VALW TO +1.1VS**

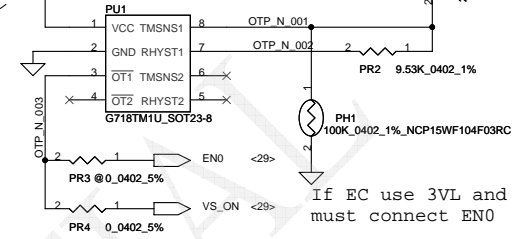
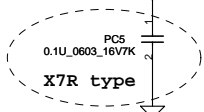
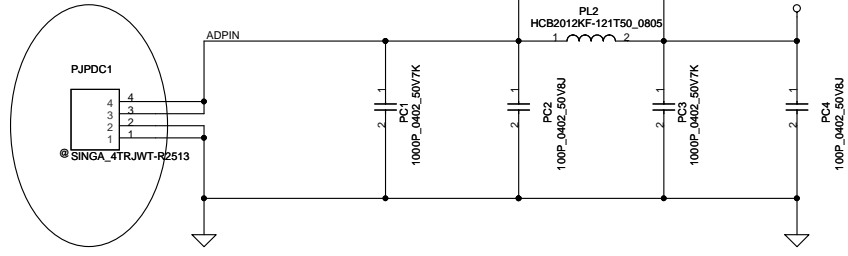


**DISCHARGE**



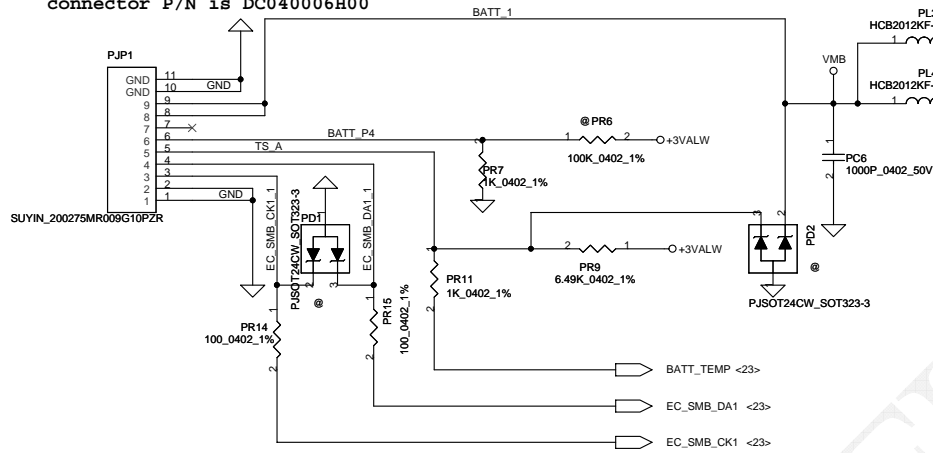
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Date:	Friday, May 06, 2011	Sheet	27	of 36

PH1 under CPU bottom side :  
 CPU thermal protection at 93 +-3 degree C  
 Recovery at 56 +-3 degree C

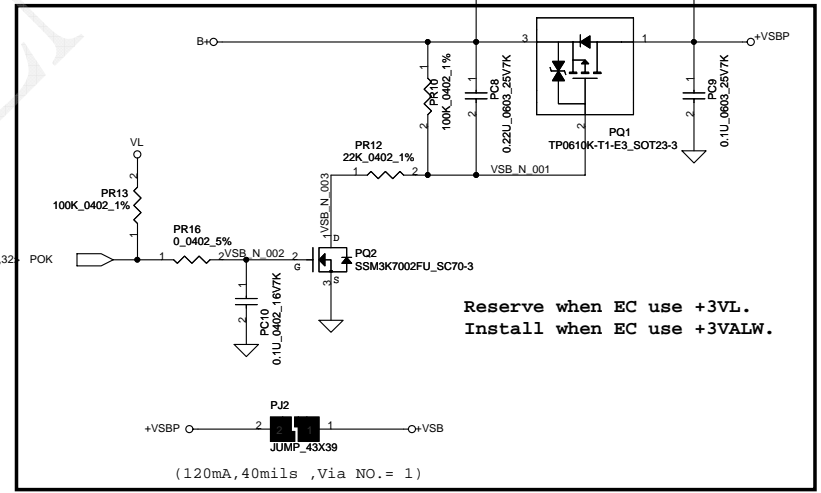


If EC use 3VL and can not detect VGATE, must connect ENO

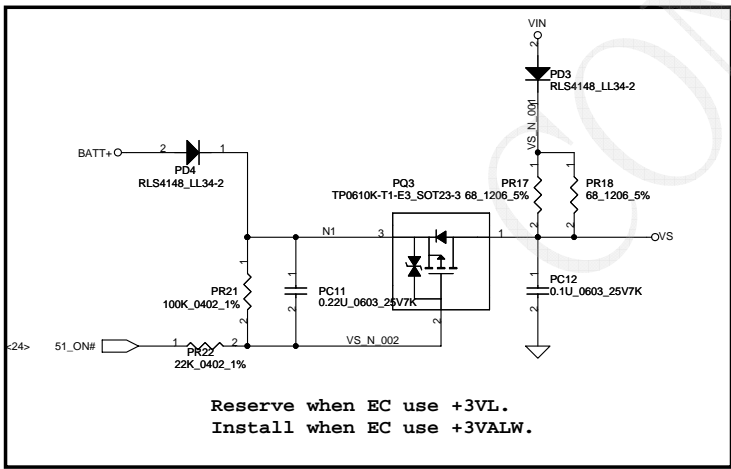
need confirm: ME give us battery connector P/N is DC040006H00



Install when EC use +3VL and SUSP was Pull high to +3VL.  
 Reserve when EC use +3VALW.

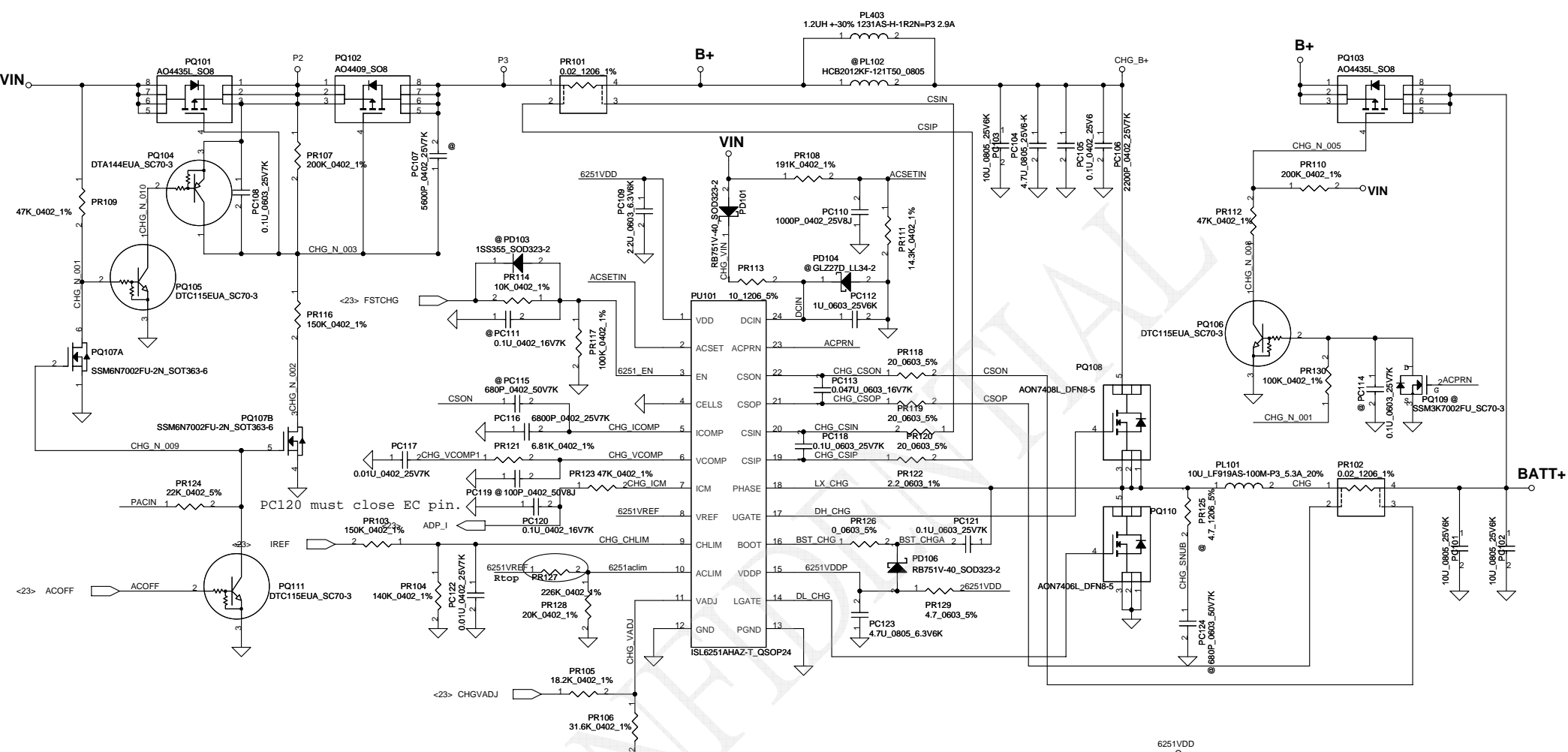


Reserve when EC use +3VL. Install when EC use +3VALW.



Reserve when EC use +3VL. Install when EC use +3VALW.

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				4019D2
				Rev B
Date: Friday, May 06, 2011			Sheet 27 of 35	



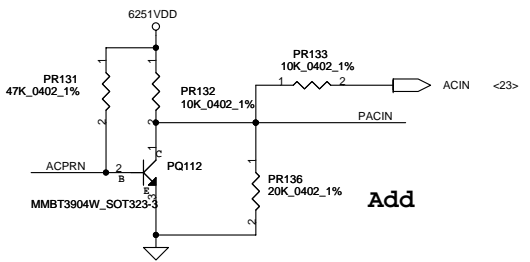
$CP = 85\% \cdot I_{ada}$ ;  
 $I_{ada} = 0 \sim 3.421A (65W); CP = 2.91A;$

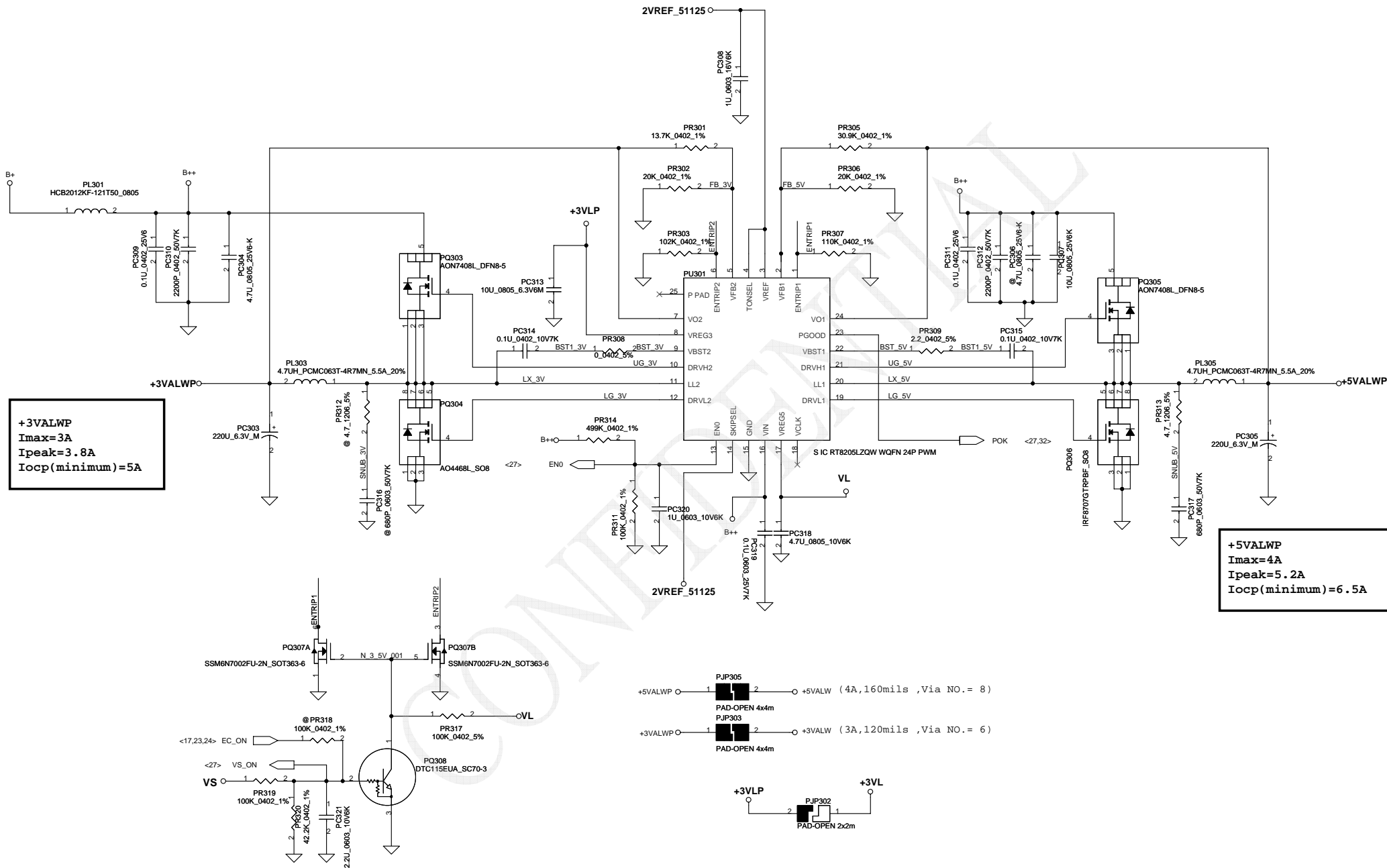
**CP mode**  
 $V_{acim} = V_{REF} \cdot (R_{bot} // R_{internal} / (R_{top} // R_{internal} + R_{bot} // R_{internal}))$   
 $65W \text{ } V_{acim} = 2.39 \cdot (20K / 152K / (20K // 152K + 226K // 152K)) = 0.38914V$   
 $I_{input} = (1 / R_{acdet}) \cdot ((0.05 \cdot V_{acim} / V_{REF} + 0.05))$   
 $65W, I_{input} = (1 / 0.02) \cdot (0.05 \cdot 0.38914 / 2.39 + 0.05) = 2.92A$

$CC = 0.25A \sim 3A$   
 $I_{REF} = 1.016 \cdot I_{charge}$   
 $I_{REF} = 0.254V \sim 3.048V$   
 $V_{CHLIM}$  need over 95mV

$CHG_{VADJ} = (V_{cell} - 4) / 0.10627$ 

V <sub>cell</sub>	CHG <sub>VADJ</sub>
4V	0V
4.2V	1.882V



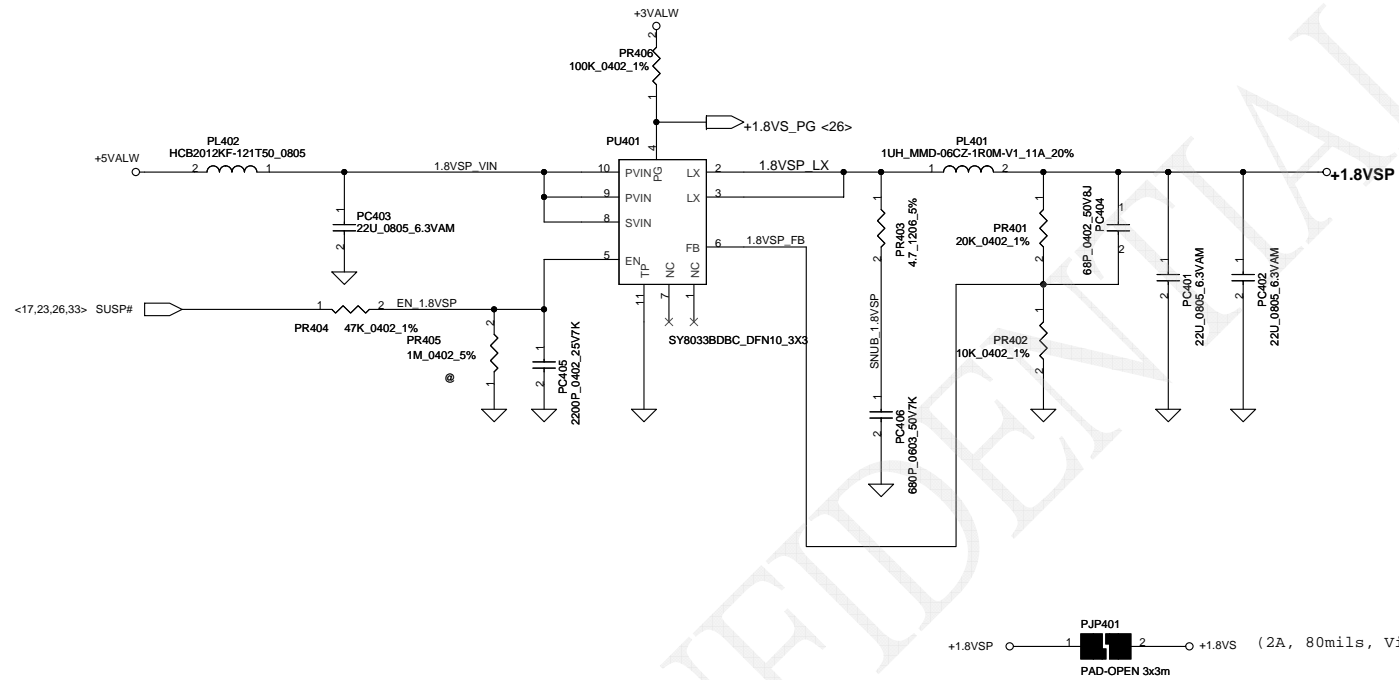


**+3VALWP**  
**I<sub>max</sub>=3A**  
**I<sub>peak</sub>=3.8A**  
**I<sub>ocp</sub>(minimum)=5A**

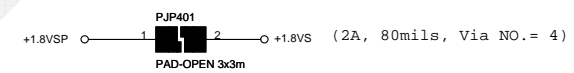
**+5VALWP**  
**I<sub>max</sub>=4A**  
**I<sub>peak</sub>=5.2A**  
**I<sub>ocp</sub>(minimum)=6.5A**

EC:+3VL, reserve PR319, install PR318, PR320 100K  
 EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

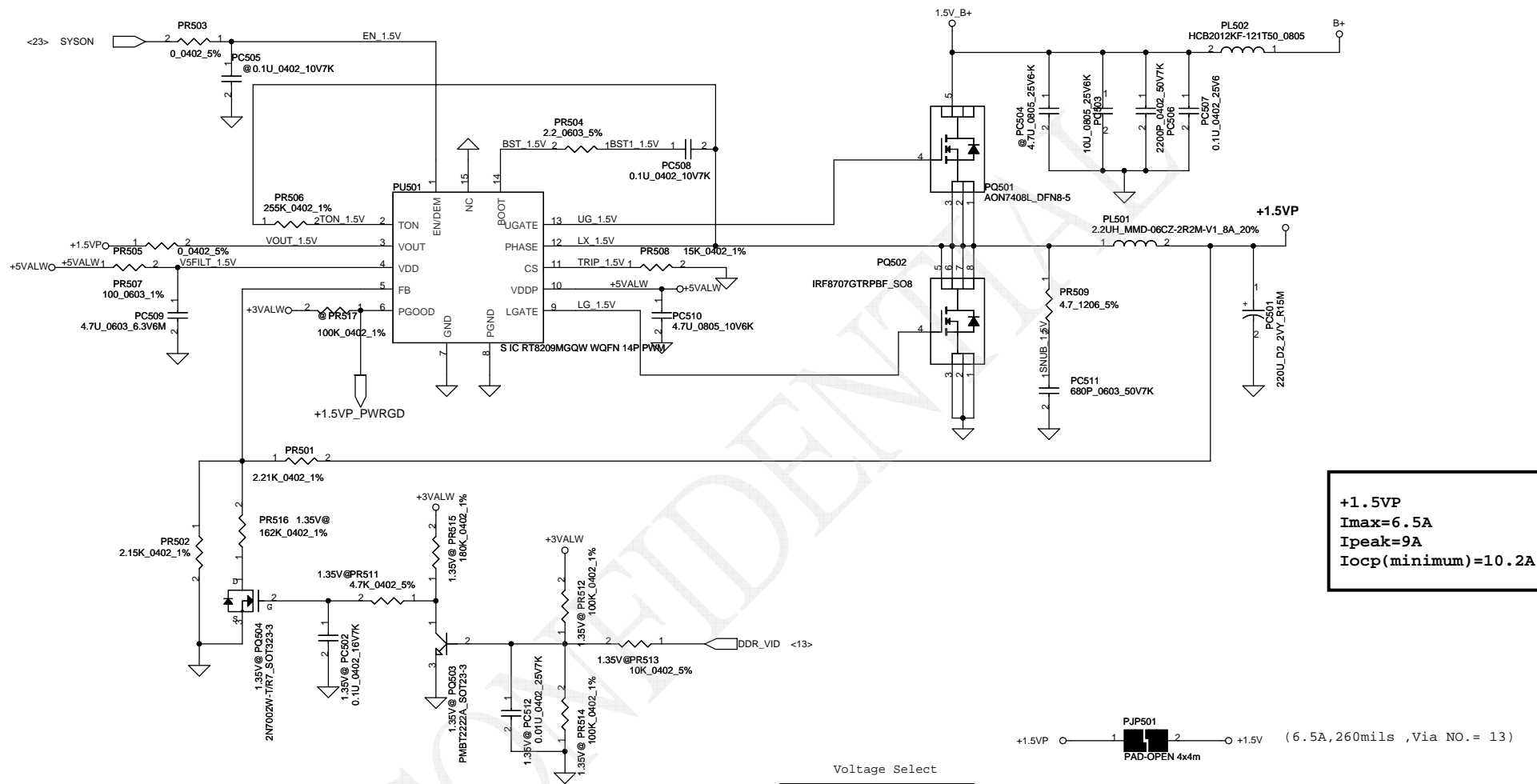
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Date:	Friday, May 06, 2011	Sheet	29	of	35



$V_o = 1.8V$      $V_{FB} = 0.6V$   
 $V_o = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$



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				4019D2	B
				Date: Friday, May 06, 2011	Sheet 30 of 35



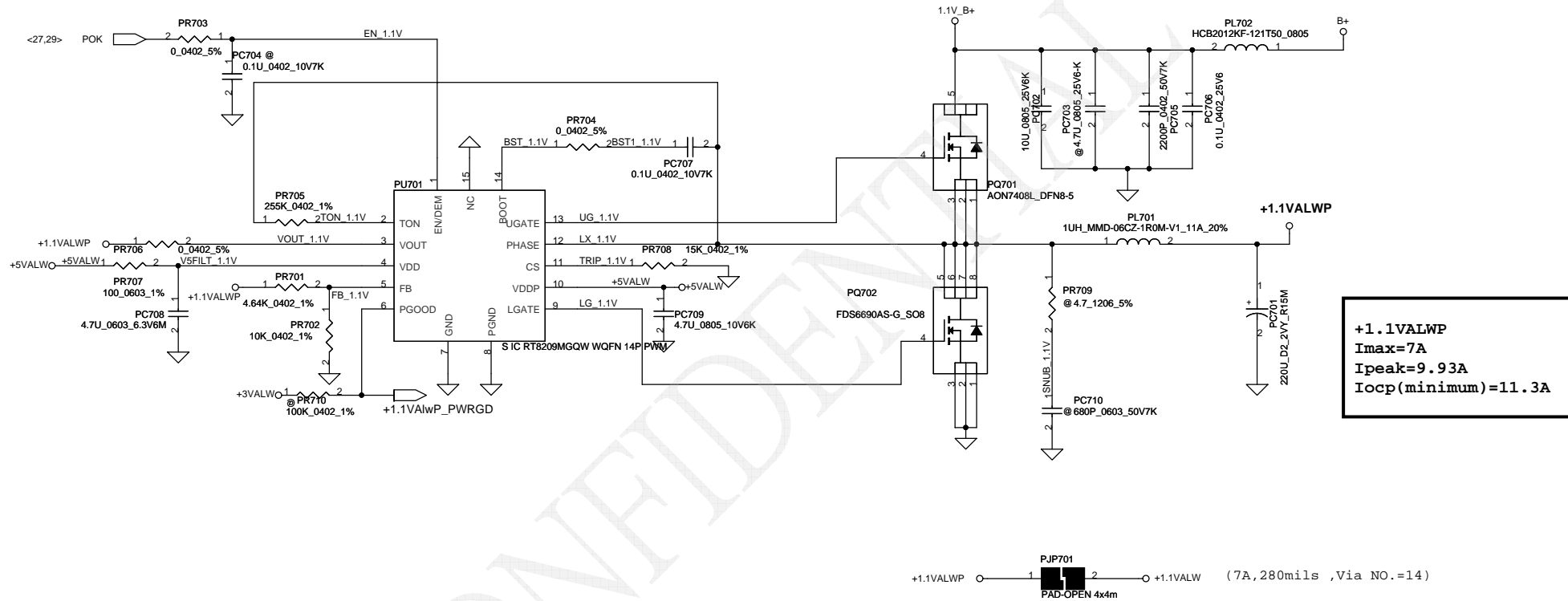
**+1.5VP**  
**I<sub>max</sub>=6.5A**  
**I<sub>peak</sub>=9A**  
**I<sub>ocp</sub>(minimum)=10.2A**

PJP501  
 PAD-OPEN 4x4m  
 +1.5VP 1 2 +1.5V (6.5A, 260mils, Via NO.= 13)

Voltage Select

DDR_VID	DDR voltage
0	+1.5V
1	+1.35V

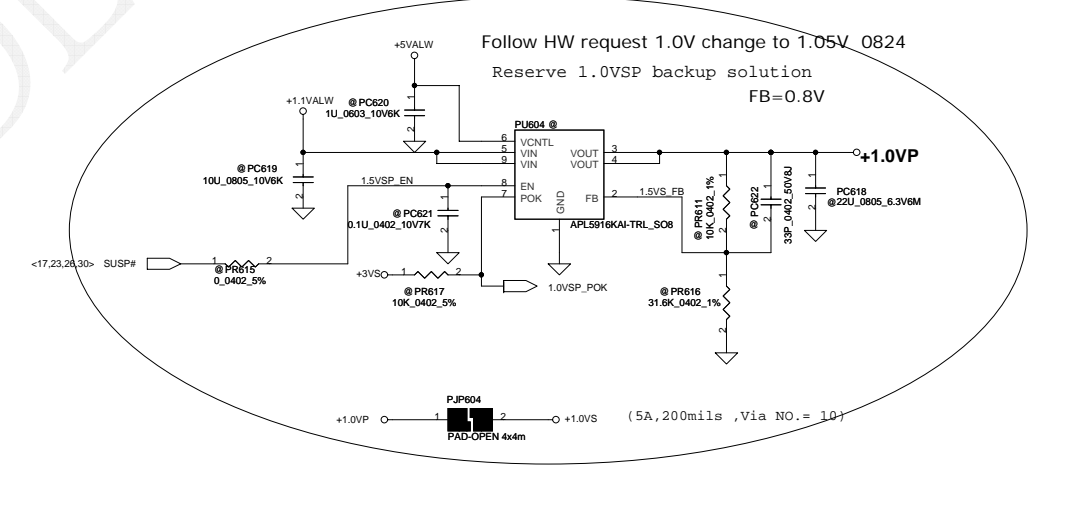
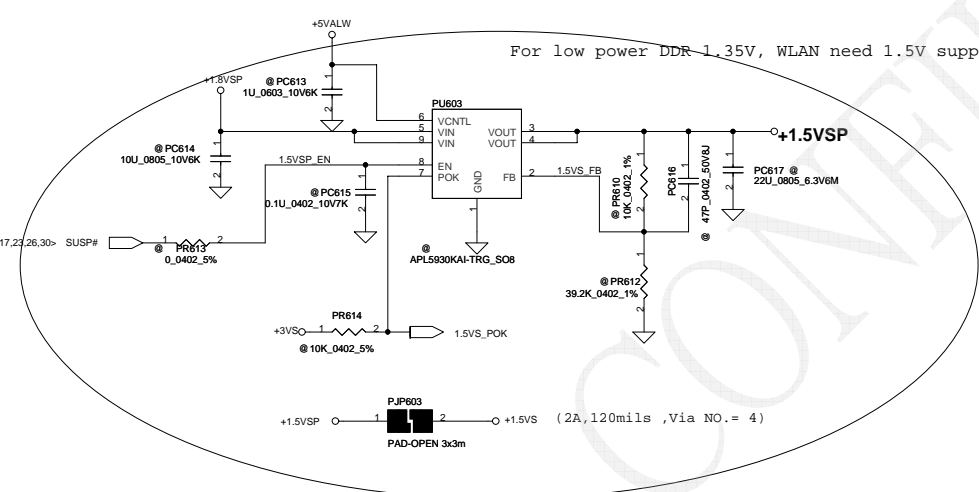
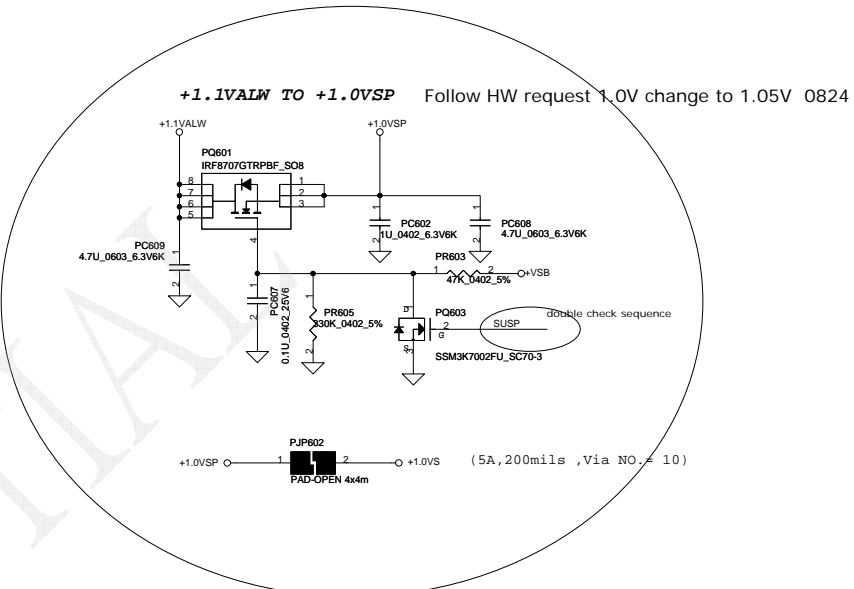
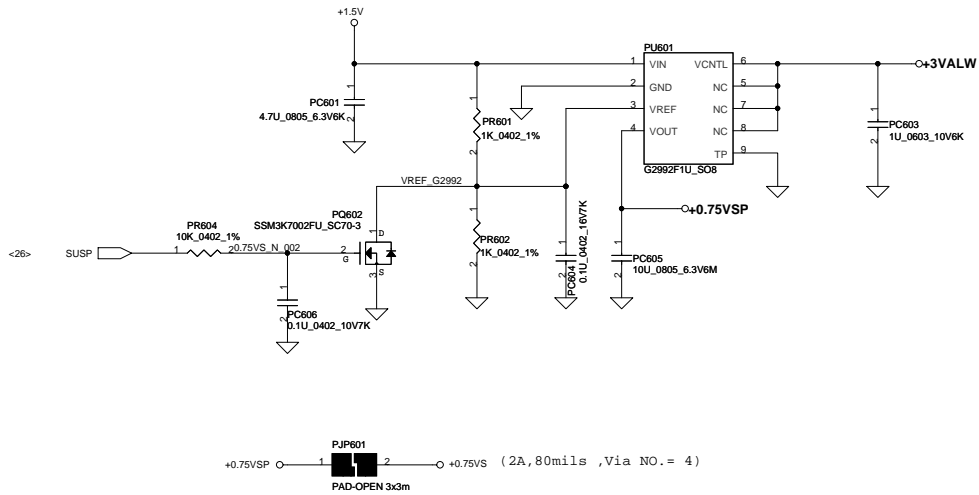




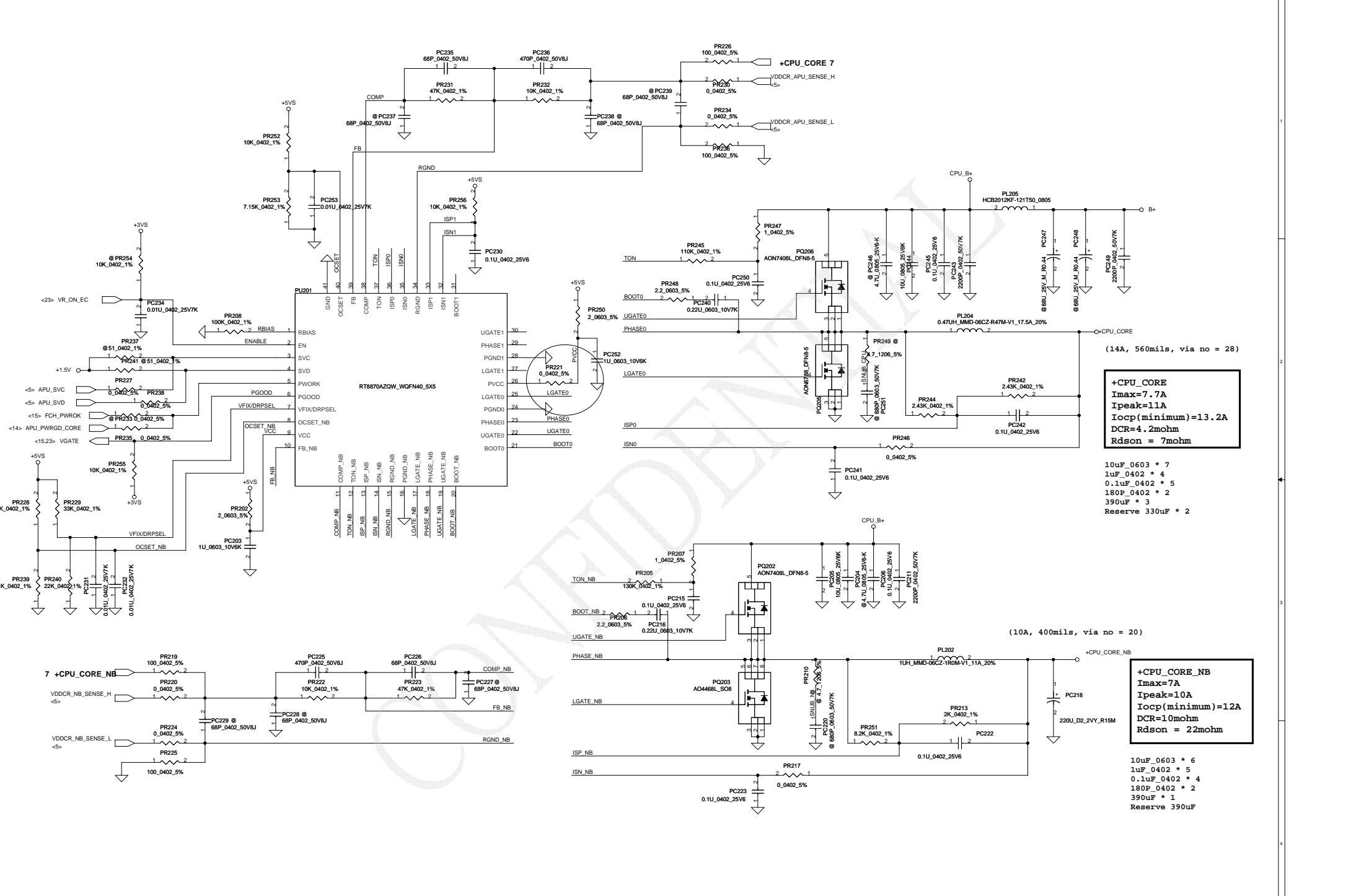
**+1.1VALWP**  
**I<sub>max</sub>=7A**  
**I<sub>peak</sub>=9.93A**  
**I<sub>ocp</sub>(minimum)=11.3A**

PJP701  
 +1.1VALWP — 1 — 2 — +1.1VALW (7A,280mils ,Via NO.=14)  
 PAD-OPEN 4x4m

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				4019D2	B
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				4019D2
				Rev B
Date: Friday, May 06, 2011				Sheet 33 of 35



(14A, 560mils, via no = 28)

**+CPU\_CORE**  
**I<sub>max</sub>=7.7A**  
**I<sub>peak</sub>=11A**  
**I<sub>ocp</sub>(minimum)=13.2A**  
**DCR=4.2mohm**  
**R<sub>dson</sub> = 7mohm**

10uF\_0603 \* 7  
 1uF\_0402 \* 4  
 0.1uF\_0402 \* 5  
 180pF\_0402 \* 2  
 390uF \* 3  
 Reserve 330uF \* 2

(10A, 400mils, via no = 20)

**+CPU\_CORE\_NB**  
**I<sub>max</sub>=7A**  
**I<sub>peak</sub>=10A**  
**I<sub>ocp</sub>(minimum)=12A**  
**DCR=10mohm**  
**R<sub>dson</sub> = 22mohm**

10uF\_0603 \* 6  
 1uF\_0402 \* 5  
 0.1uF\_0402 \* 4  
 380pF\_0402 \* 2  
 390uF \* 1  
 Reserve 390uF

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				4019D2
				Rev B
Date: Friday, May 06, 2011		ISheet 34 of 34		

# Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Reason for change	Description	phase	modify	Rev.
1	31	Follow EMI request to add PR54, PR59, PC511 for EMI issue.	add PR54, PR59, PC511	PVT	add PR54, PR59, PC511	
2	34	Follow ME request change PQ205 for height issue	Change PQ205 from AO4726L AON6788	PVT	Change PQ205 from AO4726L AON6788	
3	28	For common desgin	Delete PC107	Pre-MP	Remove PC107	
4	28	For common desgin	PR110 from 47K change to 200K	Pre-MP	PR110 from 47K change to 200K	
5	28	For common desgin	PR112 from 10K change to 47K	Pre-MP	PR110 from 10K change to 47K	
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				Sheet 35 of 35	