JASAA

Orlando 10A/10AG

LA3831P REV 1.0 Schematic

AMD Turion,Sempron/ATI RX690/RS690MC / ATI SB600

2007-08-06 Rev. 1.0

Security Classification	Compal Secret Data		
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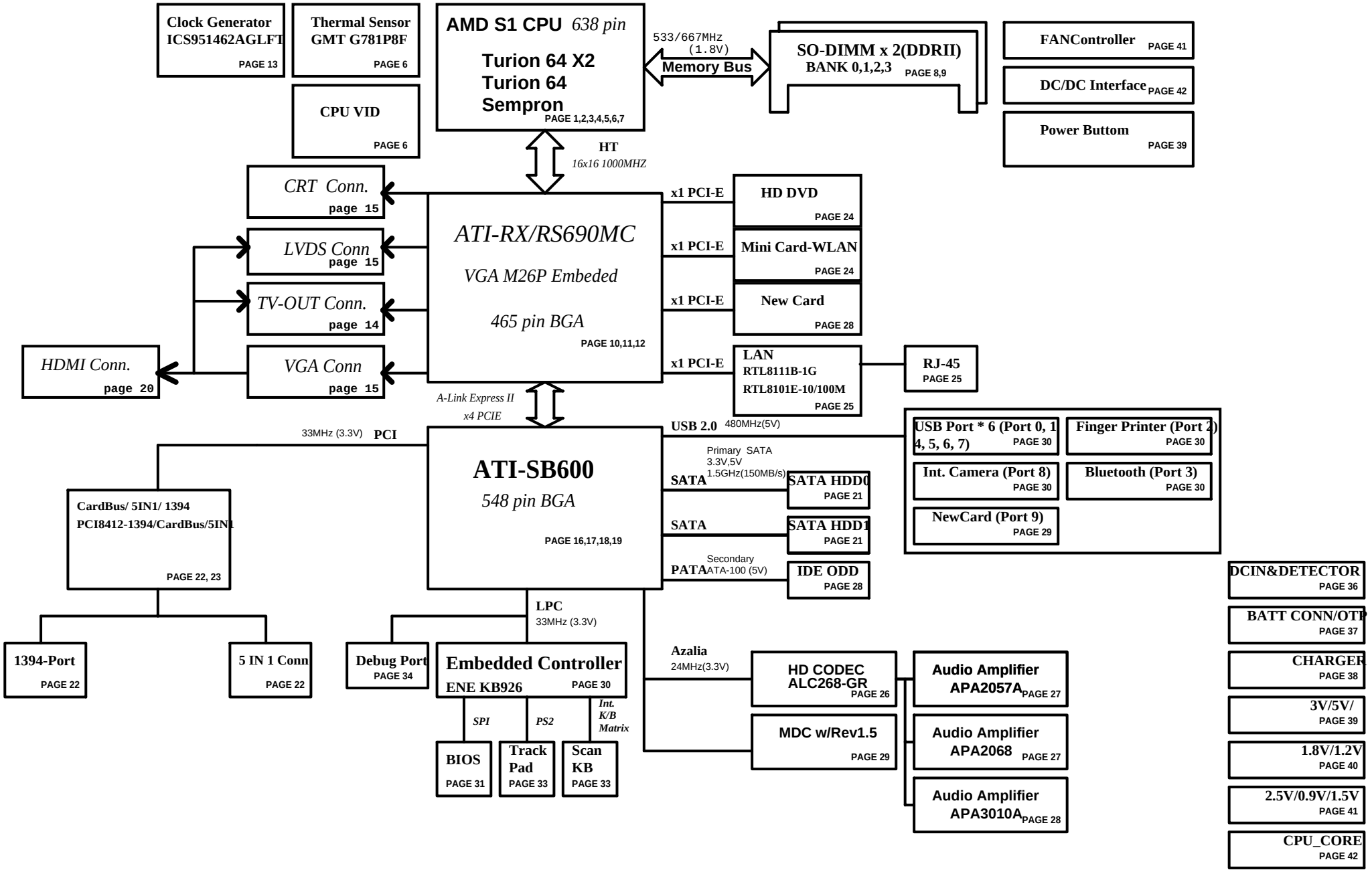
Compal confidential

JASAA Orlando10A FUNCTION BLOCK DIAGRAM

File Name : JASAA Orlando10A LA3831P

P/N :



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON
+VSB	B+ switched power rail	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+1.2VALW	1.2V always on power rail	ON	ON	ON
+1.8V	1.8V power rail	ON	ON	OFF
+0.9V	0.9V switched power rail	ON	ON	OFF
+5VS	5VS switched power rail	ON	OFF	OFF
+3VS	3.3VS switched power rail	ON	OFF	OFF
+2.5VS	2.5VS switched power rail	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V_HT	1.2VS switched power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/ CardBus/ 5IN1	AD20	2/ 2	PIRQE/F/G

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
24C16	A0H	1010 000X b

EC SM Bus2 address

Device	HEX	Address
CPU Thermal-G781P8F	98H	1001 100X b
VGA Thermal-		

ATi SB600 SM Bus address

SM Bus0 address

SM Bus1 address

Device	HEX	Address
Clock GEN. (ICS951462AGLFT)		
DDR DIMM0	A4	
DDR DIMM1	A6	
Mini Card-WLAN		
Mini Card-3G		
New Card		

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BTN_ID	
0	
1	
2	
3	
4	
5	
6	
7	

BTO	BOM STURCTURE

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10 H_CADIP[0..15] — H_CADIP[0..15]
10 H_CADIN[0..15] — H_CADIN[0..15]
H_CADOP[0..15] — H_CADOP[0..15] 10
H_CADON[0..15] — H_CADON[0..15] 10

+1.2V_HT

VLDT=500mA

JP27A

D4	VLDT_A3	VLDT_B3	AE5		
D3	VLDT_A2	VLDT_B2	AE4		
D2	VLDT_A1	VLDT_B1	AE3		
D1	VLDT_A0	VLDT_B0	AE2		
H_CADIP15 N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15	
H_CADIN15 P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15	
H_CADIP14 M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14	
H_CADIN14 M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14	
H_CADIP13 L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13	
H_CADIN13 M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13	
H_CADIP12 K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12	
H_CADIN12 K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12	
H_CADIP11 H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11	
H_CADIN11 H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11	
H_CADIP10 G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10	
H_CADIN10 H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10	
H_CADIP9 E3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9	
H_CADIN9 F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9	
H_CADIP8 E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8	
H_CADIN8 F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8	
H_CADIP7 N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7	
H_CADIN7 N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7	
H_CADIP6 L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6	
H_CADIN6 M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6	
H_CADIP5 L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5	
H_CADIN5 L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5	
H_CADIP4 J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4	
H_CADIN4 K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4	
H_CADIP3 G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3	
H_CADIN3 H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3	
H_CADIP2 G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2	
H_CADIN2 G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2	
H_CADIP1 E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1	
H_CADIN1 F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1	
H_CADIP0 E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0	
H_CADIN0 E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0	

HTT Interface

10 H_CLKIP1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	H_CLKOP1 10
10 H_CLKIN1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	H_CLKON1 10
10 H_CLKIP0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	H_CLKOP0 10
10 H_CLKIN0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	H_CLKON0 10
		L0_CTLIN_H1	L0_CTLOUT_H1	J5	
	P3	L0_CTLIN_L1	L0_CTLOUT_L1	R5	
H_CTLIP0	N1				
10 H_CTLIP0		L0_CTLIN_H0	L0_CTLOUT_H0	R2	H_CTLOP0 H_CTLOP0 10
10 H_CTLIN0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	H_CTLON0 H_CTLON0 10

+1.2V_HT
R52 2 1 51_0402_1%
R51 2 1 51_0402_1%

FOX_PZ63823-284S-41F

Athlon 64 S1
Processor Socket

AMD : 49.9 1%
ATI : 51 1%

C107 1 2 4.7U_0805_10V4Z

VLDT CAP.

+1.2V_HT
250 mil

C102	C103	C101	C104	C106	C112
4.7U_0805_10V4Z	4.7U_0805_10V4Z	0.22U_0603_16V4Z	0.22U_0603_16V4Z	180P_0402_50V8J	180P_0402_50V8J

Near CPU Socket

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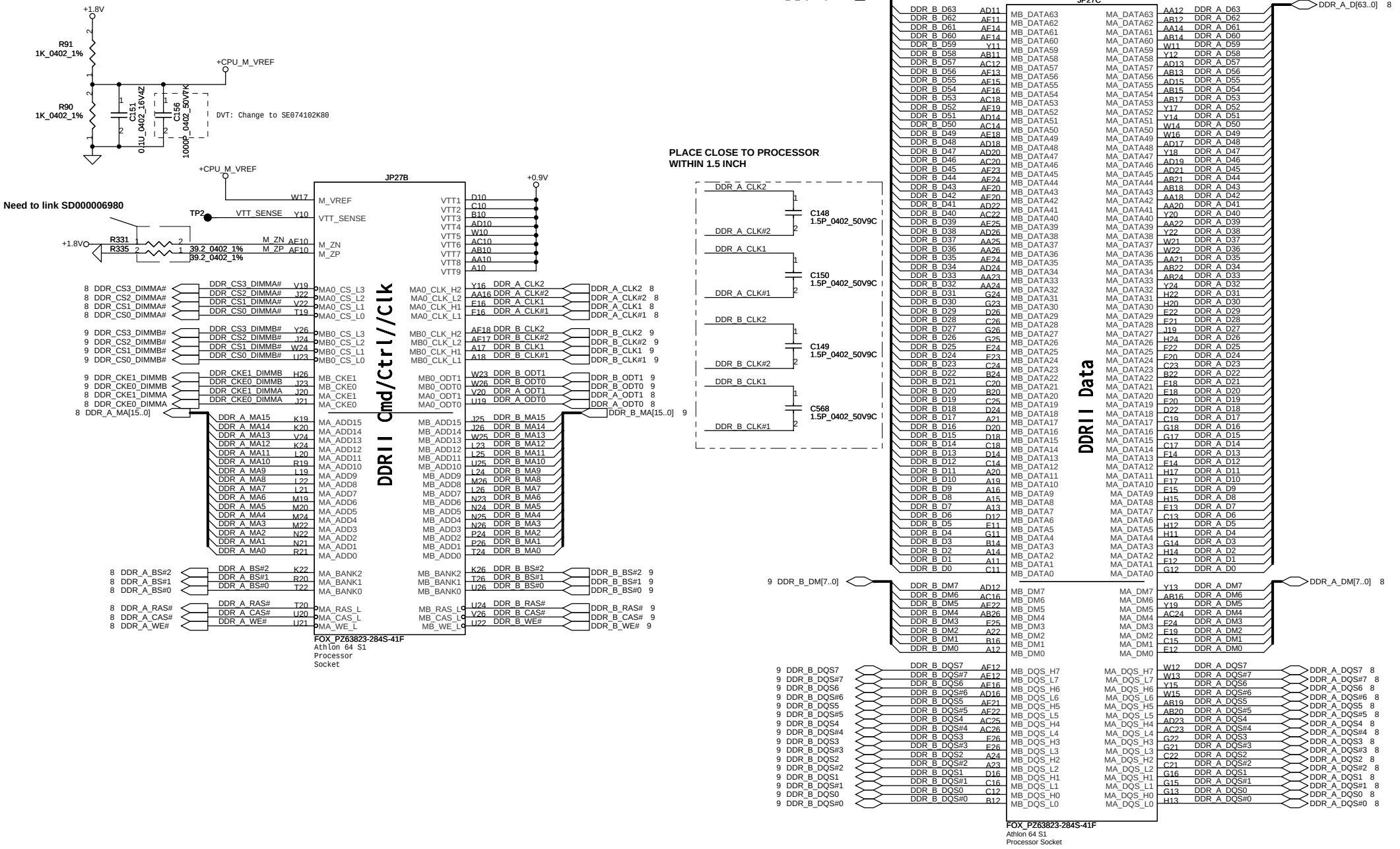
Processor DDR2 Memory Interface



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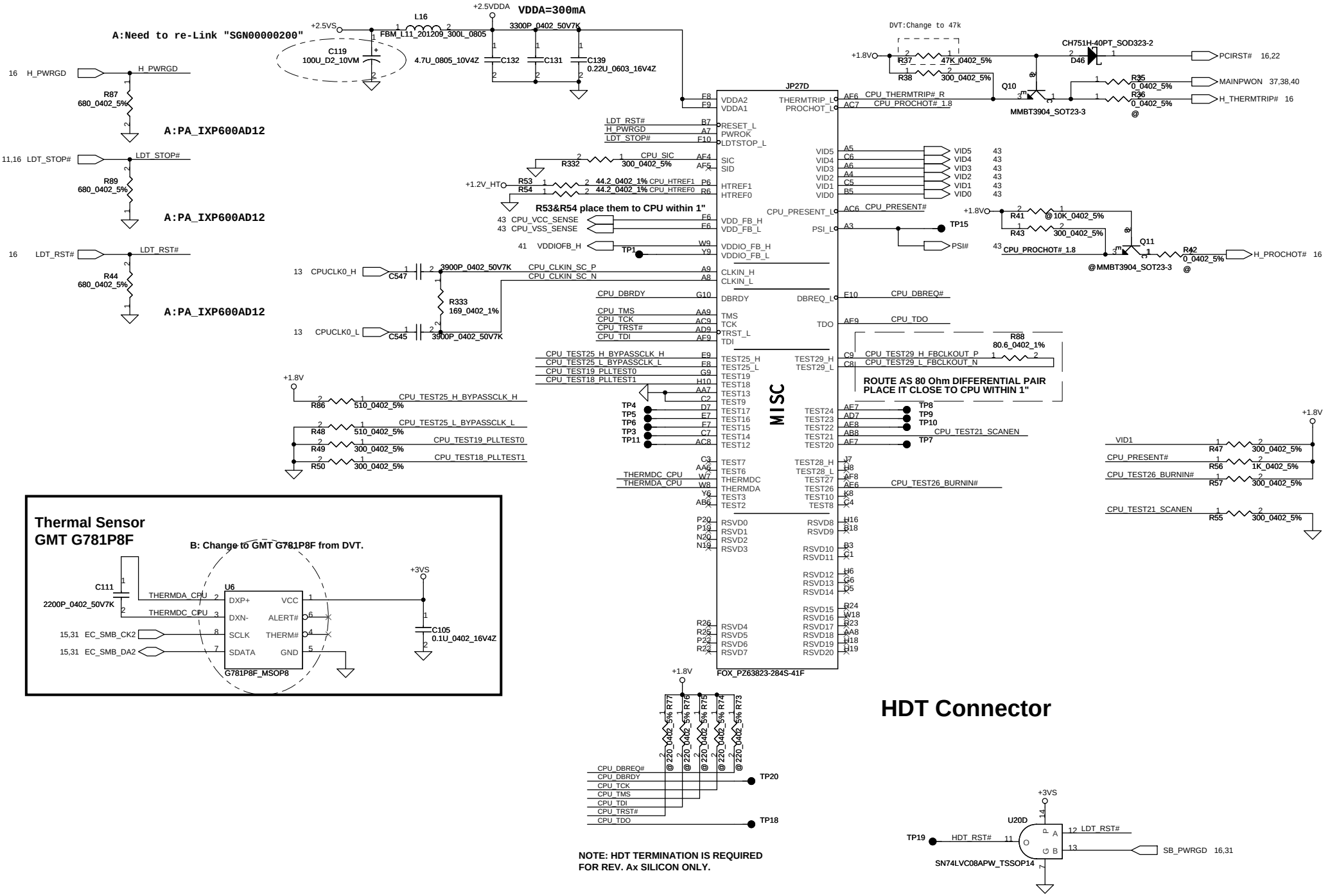

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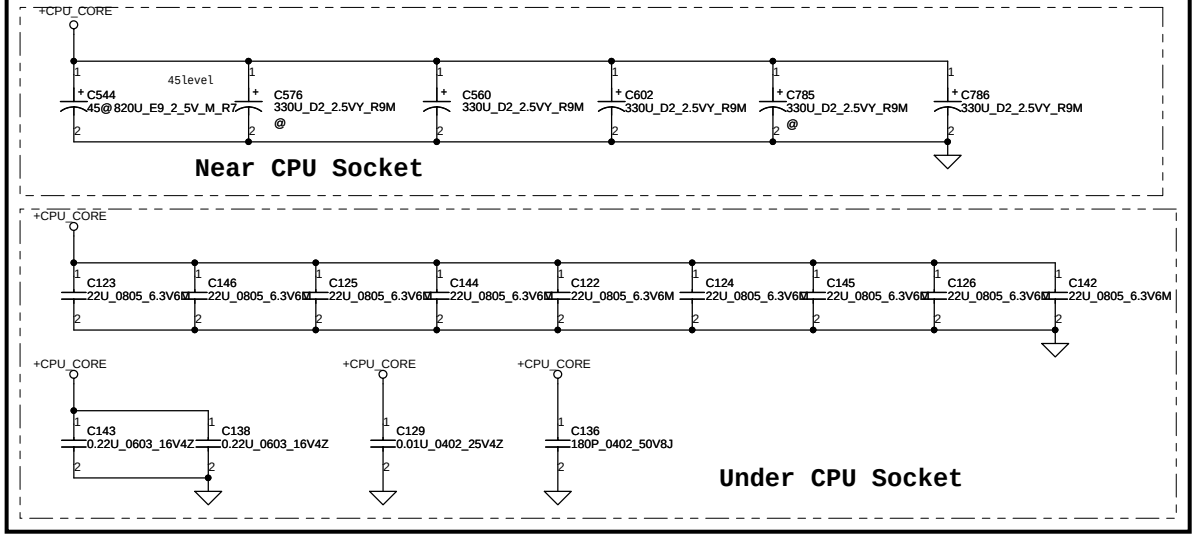
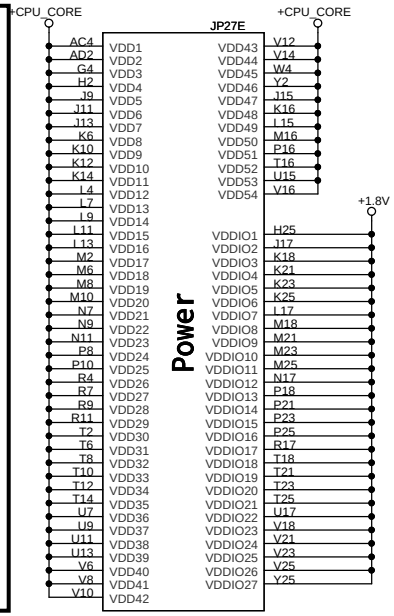
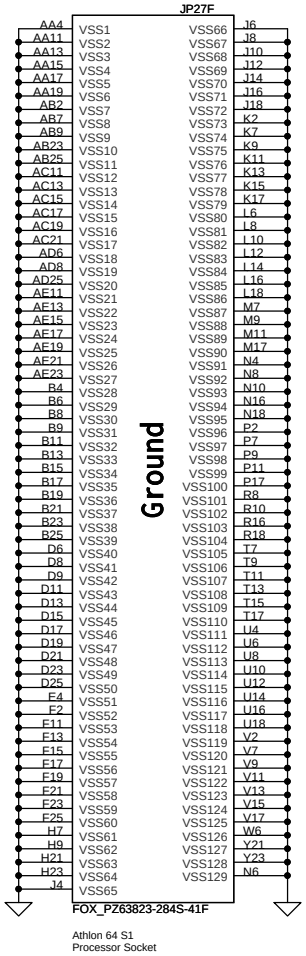
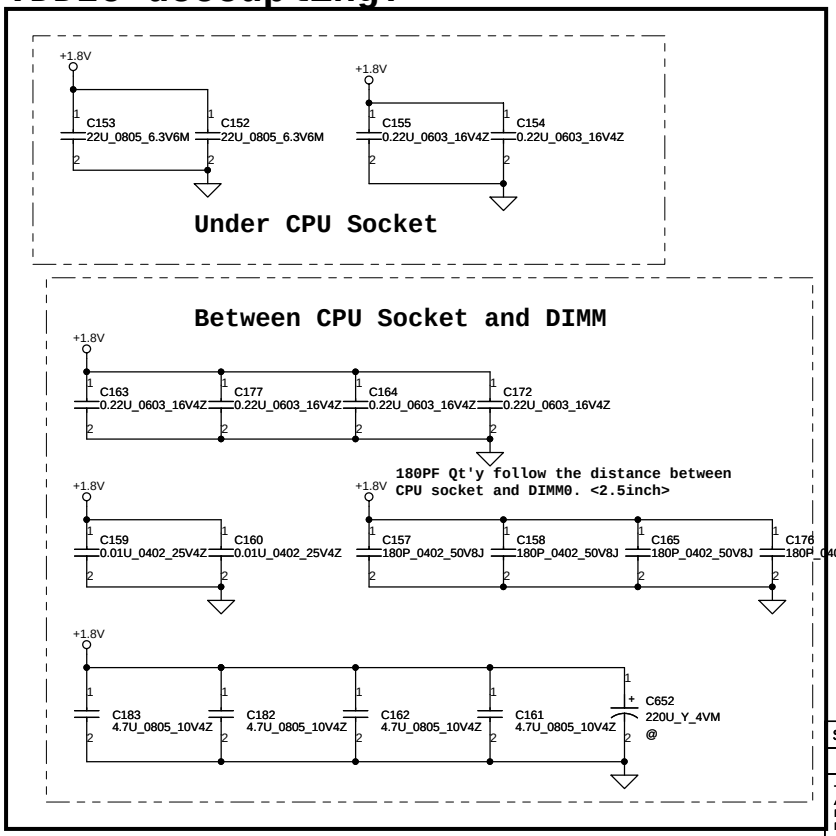
VDD(+CPU_CORE) decoupling.



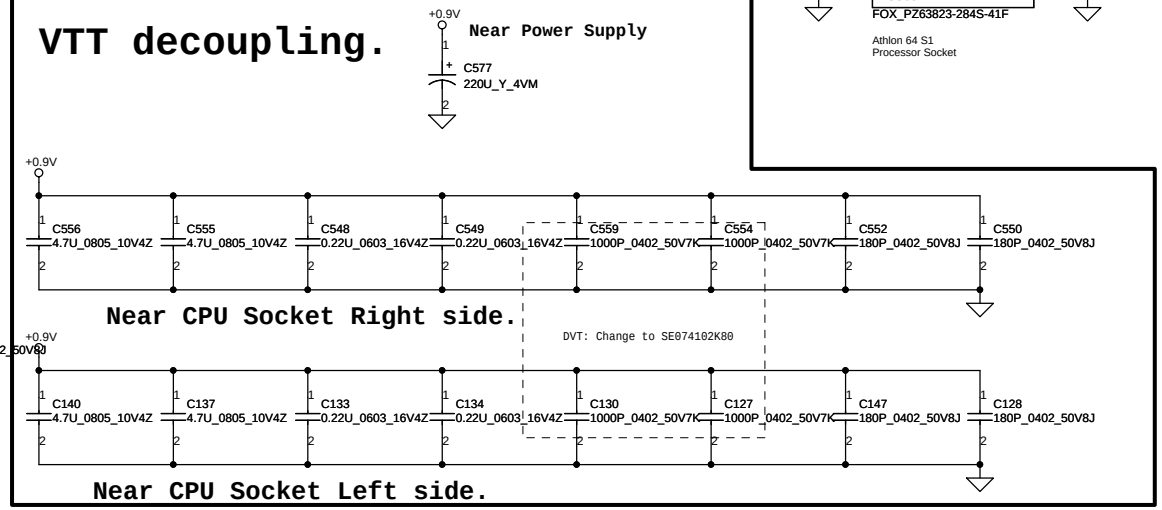




VDDIO decoupling.



VTT decoupling.



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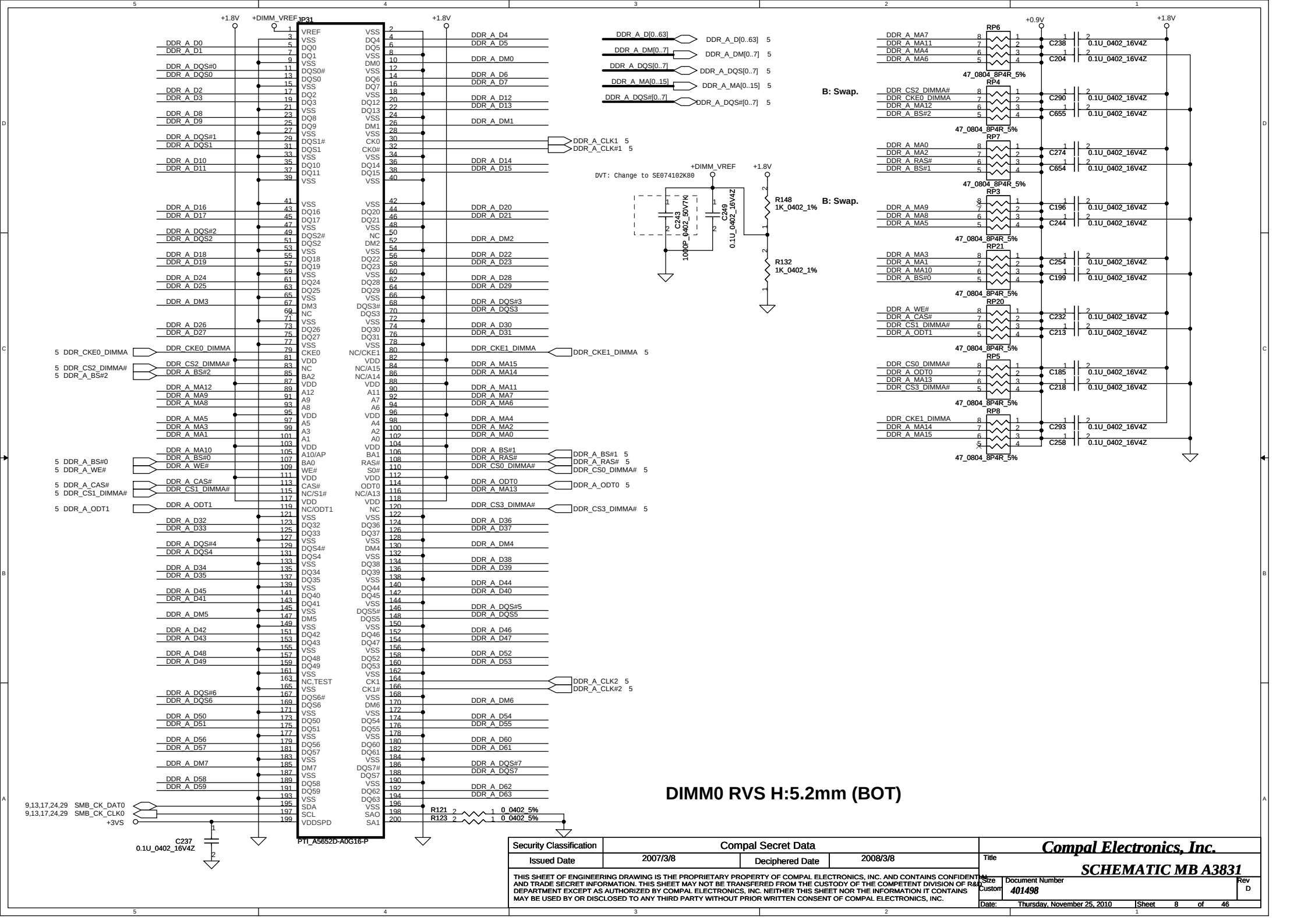

DIMM0 RVS H:5.2mm (BOT)

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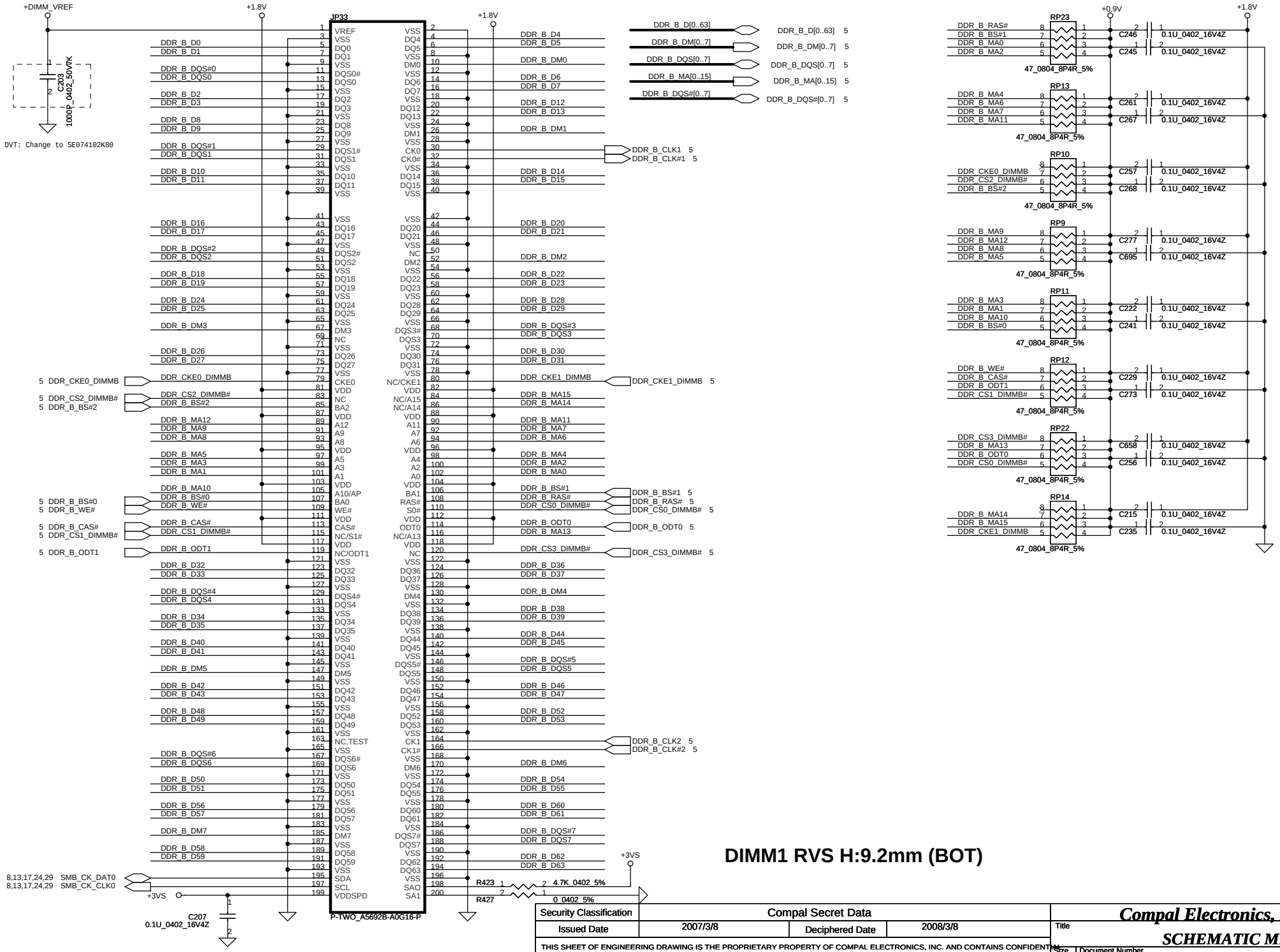

DIMM1 RVS H:9.2mm (BOT)

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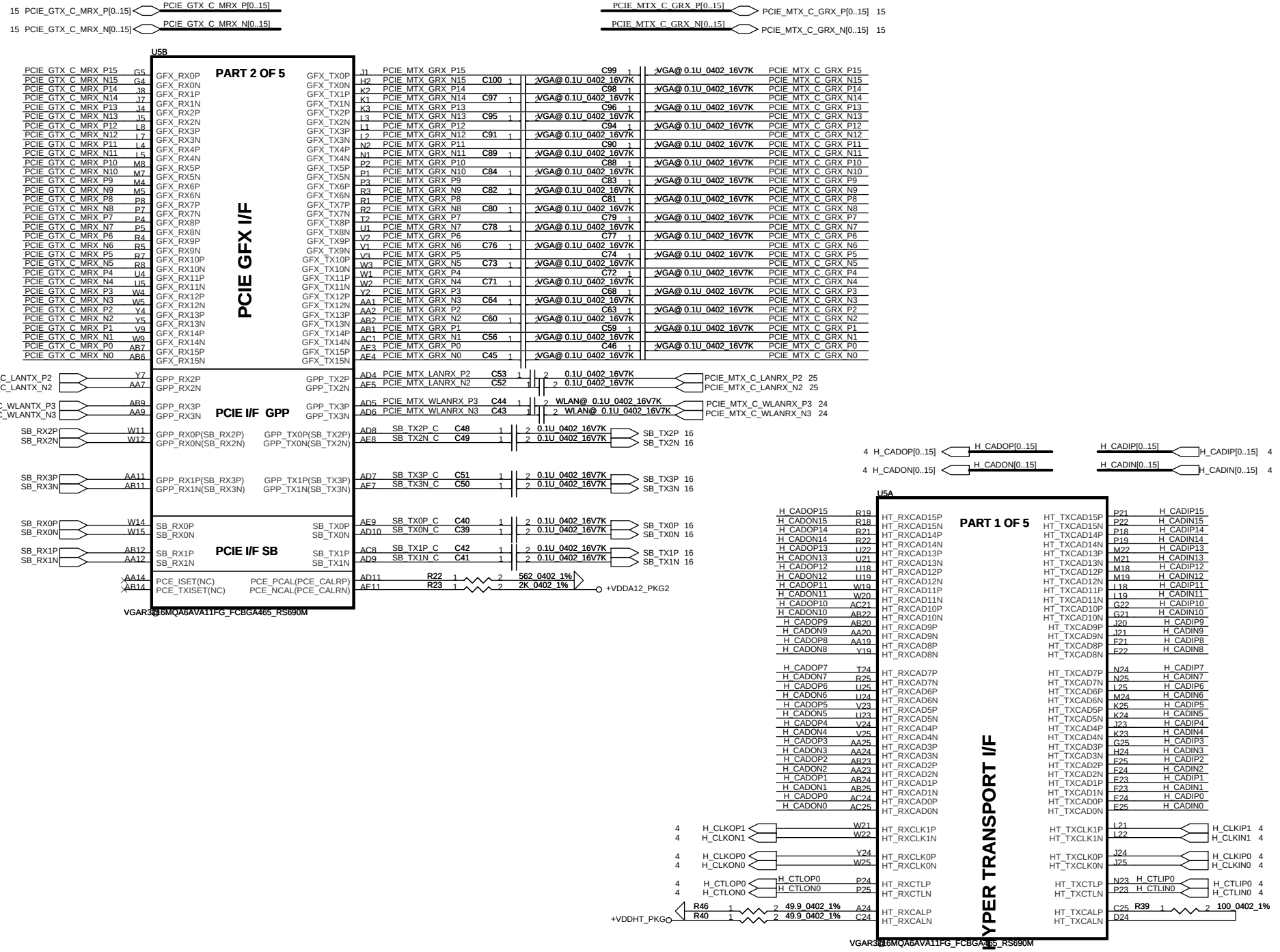

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	RS690		RS690 only	
	DFT_GPIO0	DFT_GPIO1	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Memory side port not available DEFAULT	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) DEFAULT 110: 4-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D 010: 4-1-1-1-1 Config E others: register defined (register default to Config E)	Enable debug bus via the memory IO pads, if available in the package use default values DEFAULT
PULL LOW	Memory side port available	I2C Master can load strap values from EEPROM if connected, or use default values if not connected		use the memory data bus to output the debug bus

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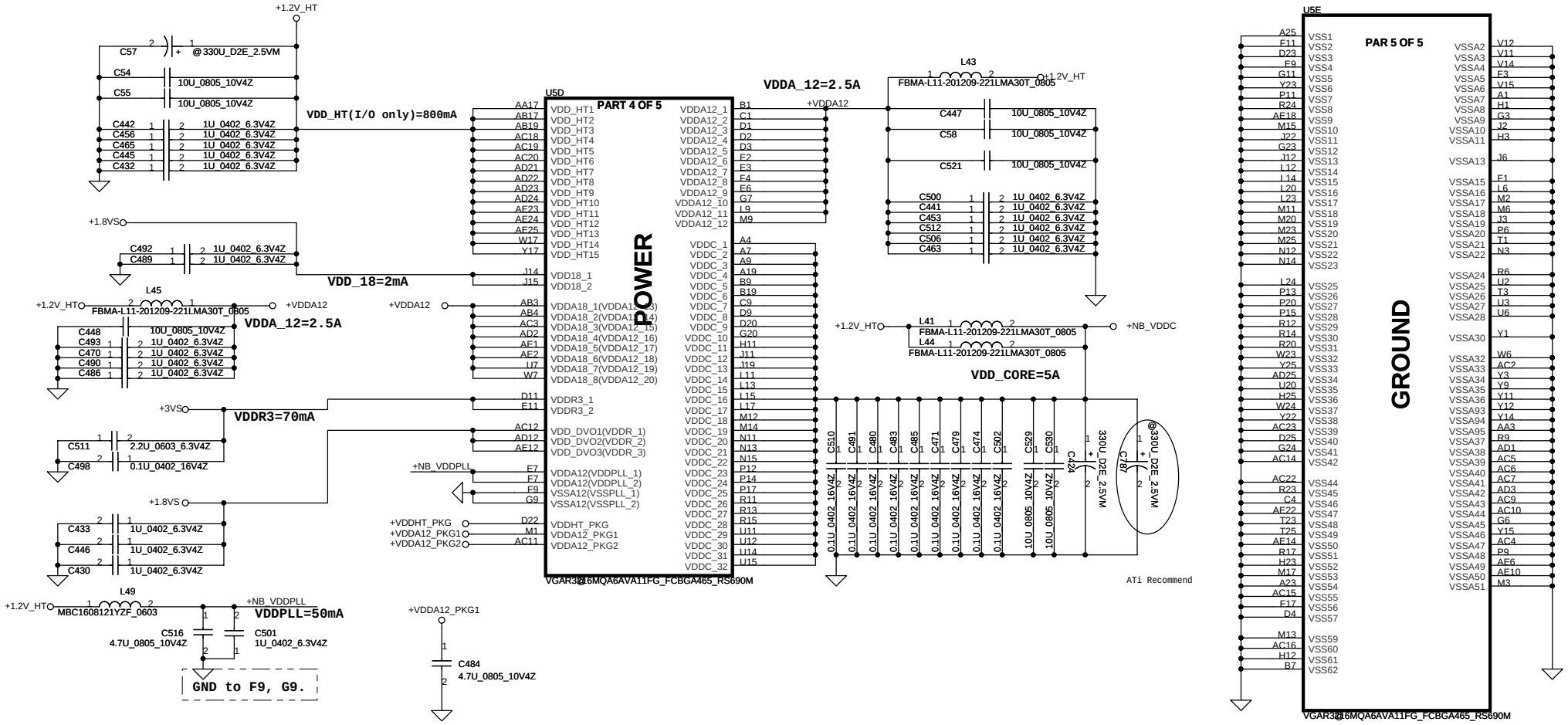

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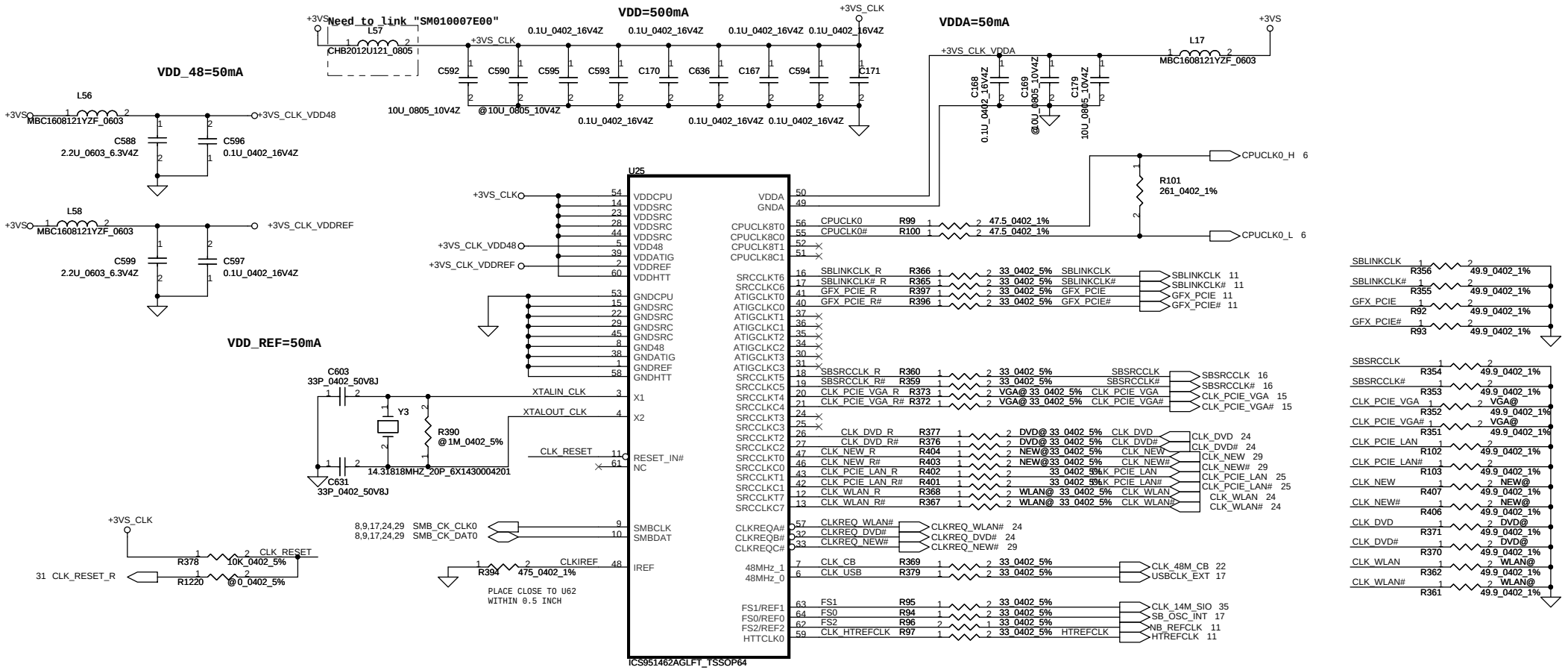

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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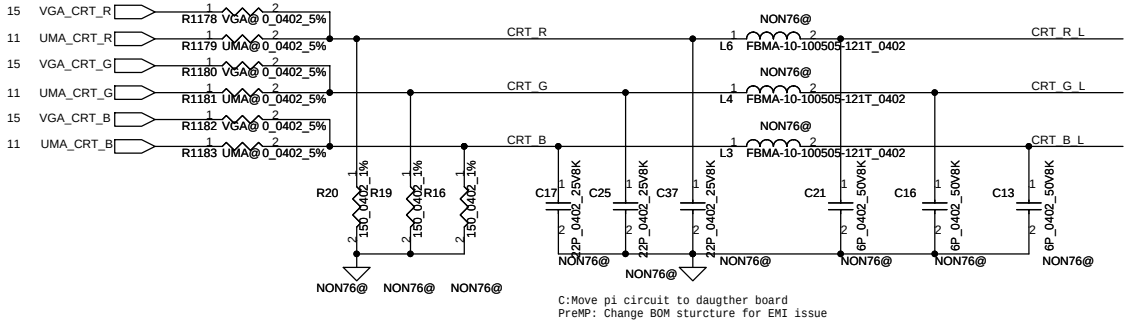
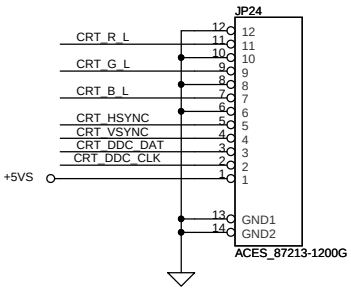
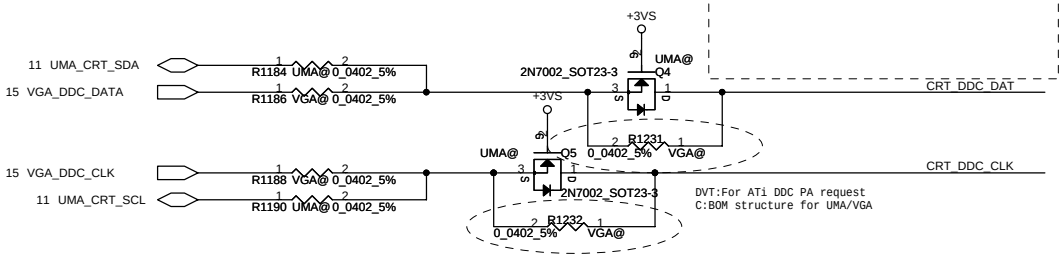
CRT CONNECTOR



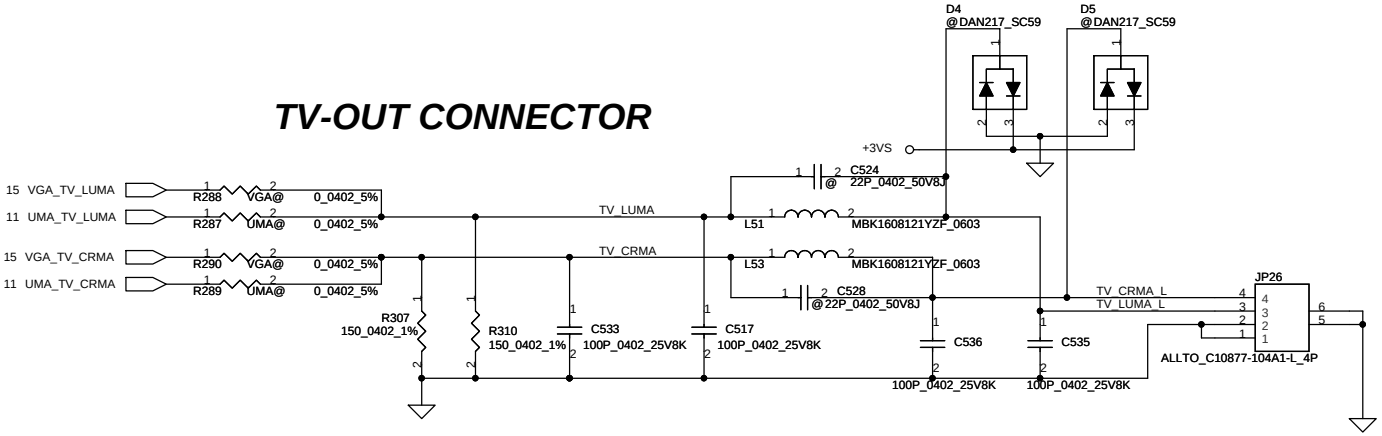
CRT Conn.





DVT:For ATi DDC PA request
C: VGA level shift
circuit on VGA/B, remove
extra components

TV-OUT CONNECTOR



TV-OUT Conn.

1. Y ground
2. C ground
3. Y (luminance+sync)
4. C (crominance)

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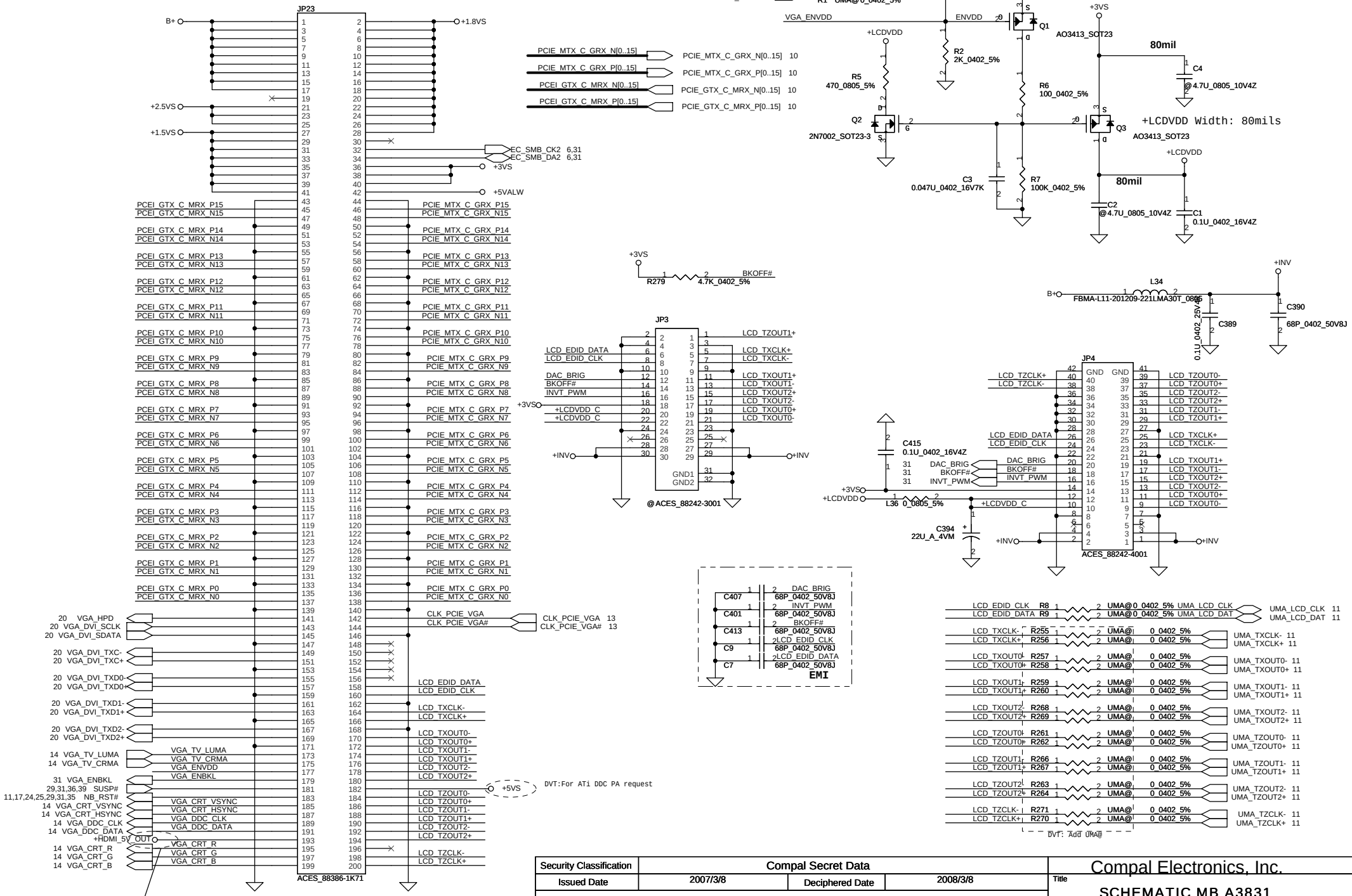
VGA BOARD Conn. (ATi Support Only)



LCD/PANEL BD. Conn.

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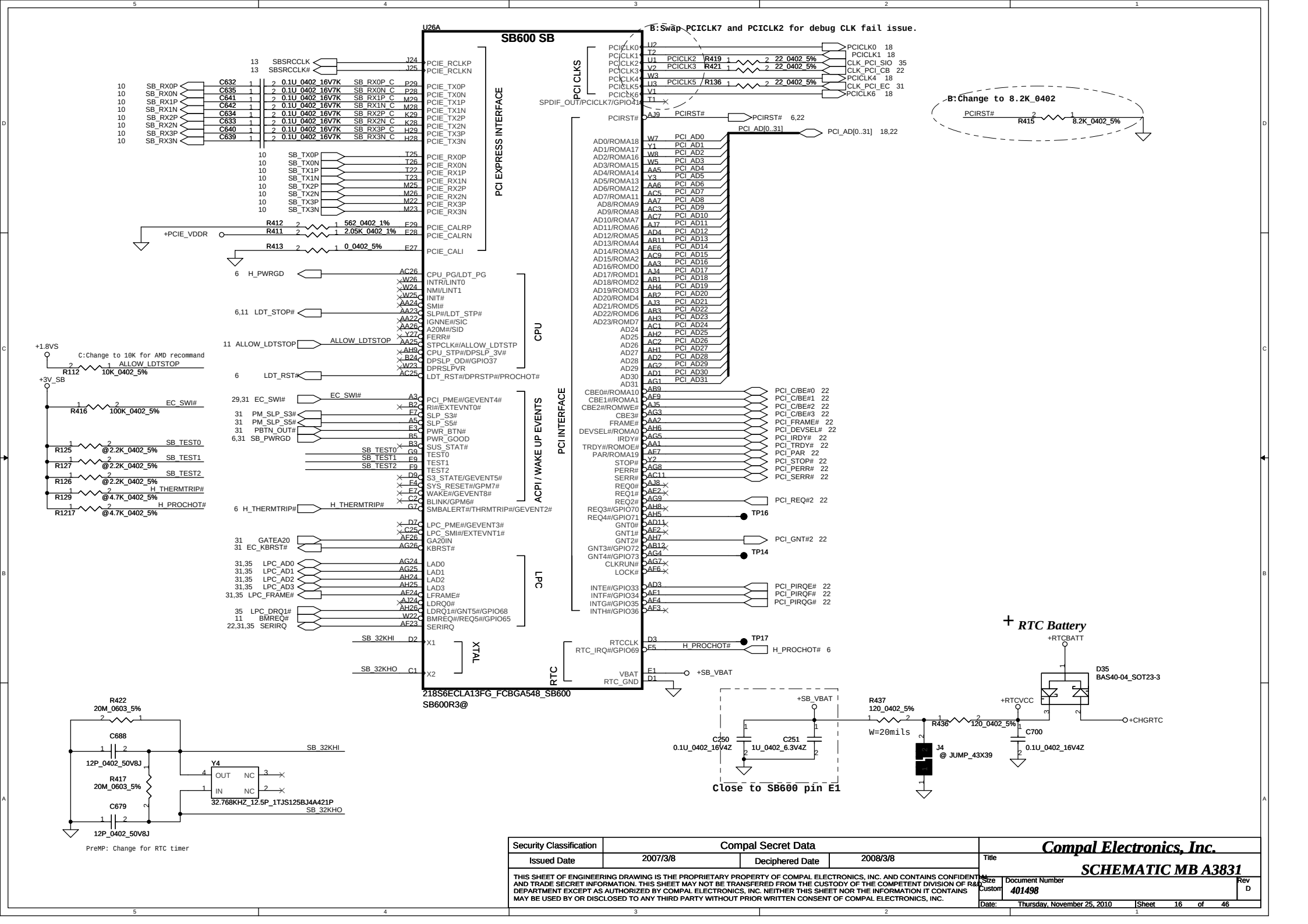
B:Swap PCICLK7 and PCICLK2 for debug CLK fail issue.
U26A
SB600 SB
PCI EXPRESS INTERFACE
PCI CLKS
CPU
PCI INTERFACE
ACPI / WAKE UP EVENTS
LPC
XTAL
RTC
B:Change to 8.2K_0402
C:Change to 10K for AMD recommand
218S6ECLA13FG_FCBGA548_SB600
SB600R3@
PreMP: Change for RTC timer
+ RTC Battery
Close to SB600 pin E1
W=20mils
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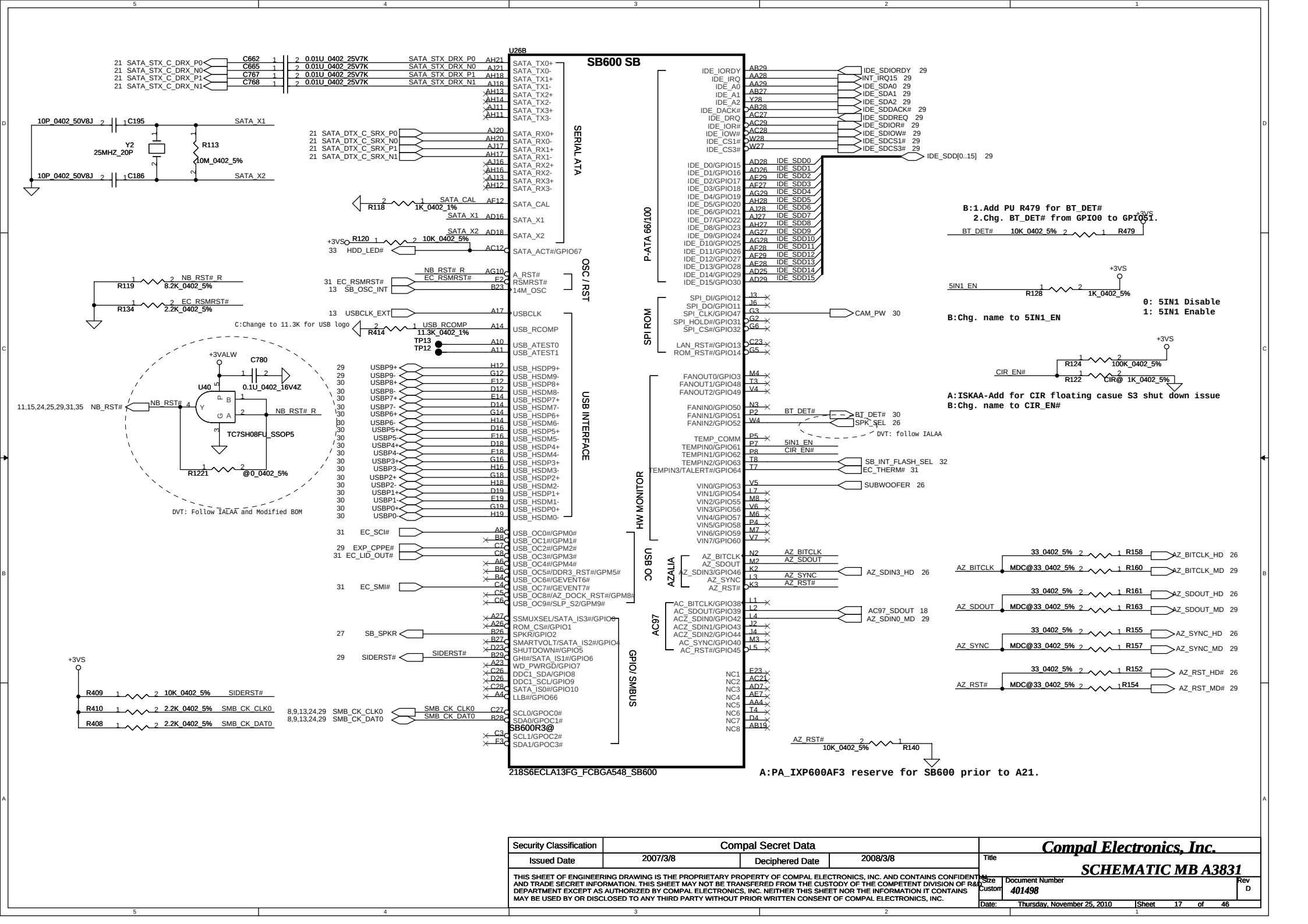

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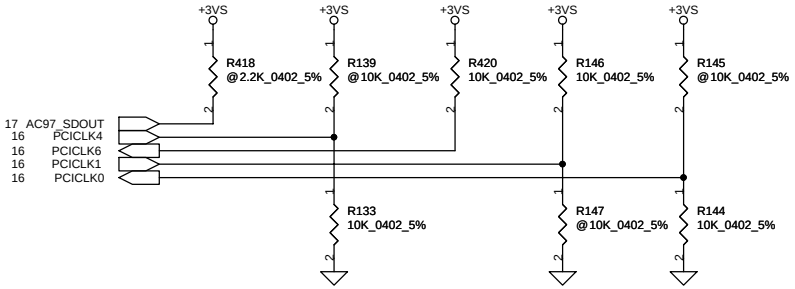
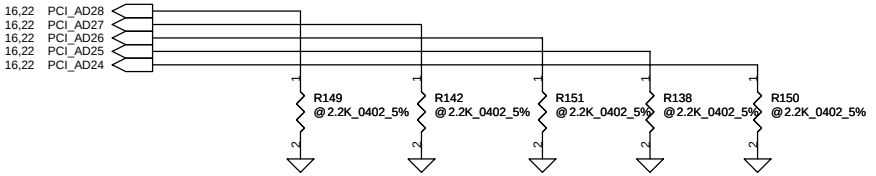
Standard Straps



Debug Straps



	AC_SDOUT	PCI_CLK4 <PCICLK4>	PCI_CLK6 <PCICLK6>	PCI_CLK1 <CLK_PCI_LAN> PCI_CLK0 <PCICLK0>
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=AMD DEFAULT	ROM TYPE: H, H = Reserve; H, L = LPC ROM DEFAULT; L, H = SPI ROM; L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS <int'l PD> DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=Intel	

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 <A11 only>
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE BOOTFAIL TIMER DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	ENABLE BOOTFAIL TIMER

Un-Used Inputs Setting--GPIO pins

GPIO4/SMARTVOLT/SATA_IS2#	Config. GPIO to Output Mode.
GPIO5/SHUTDOWN#	Config. GPIO to Output Mode.
GPIO7/WD_PWRGD	Config. GPIO to Output Mode.
GPIO8/DDC1_SDA	Config. GPIO to Output Mode.
GPIO9/DDC1_SCL	Config. GPIO to Output Mode.
GPIO10/SATA_IS0#	Config. GPIO to Output Mode.
GPIO41/PCICLK7/SPDIF_OUT	Config. GPIO to Output Mode.
GPIO50/FANIN0	Config. GPIO to Output Mode.
GPIO51/FANIN1	Config. GPIO to Output Mode.
GPIO52/FANIN2	Config. GPIO to Output Mode.
GPIO53/VIN0	Config. GPIO to Output Mode.
GPIO54/VIN1	Config. GPIO to Output Mode.
GPIO55/VIN2	Config. GPIO to Output Mode.

Un-Used Inputs Setting--GPM pins

GPIO56/VIN3	Config. GPIO to Output Mode.
GPIO57/VIN4	Config. GPIO to Output Mode.
GPIO58/VIN5	Config. GPIO to Output Mode.
GPIO59/VIN6	Config. GPIO to Output Mode.
GPIO60/VIN7	Config. GPIO to Output Mode.
GPIO61/TEMPIN0	Config. GPIO to Output Mode.
GPOC2#/SCL1	Config. GPIO to Output Mode.
GPOC3#/SDA1	Config. GPIO to Output Mode.

Un-Used Inputs Setting--GPM pins

GPM5#/DDR3_RST#/USB_OC5#	Config. for internal PU.
GEVENT5#/S3_STATE	Config. for internal PU.

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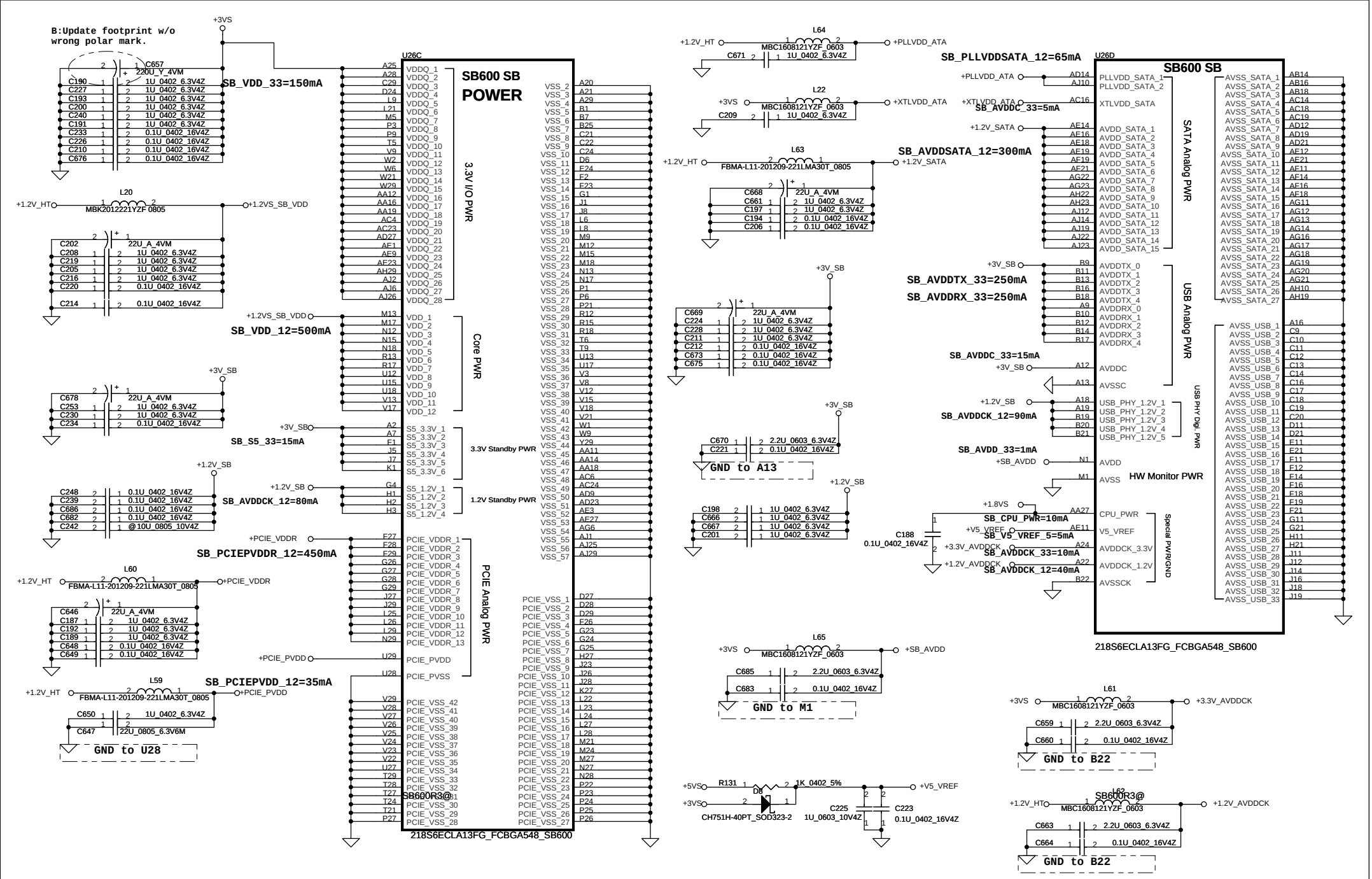

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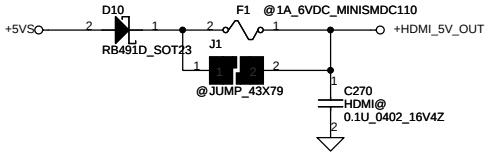
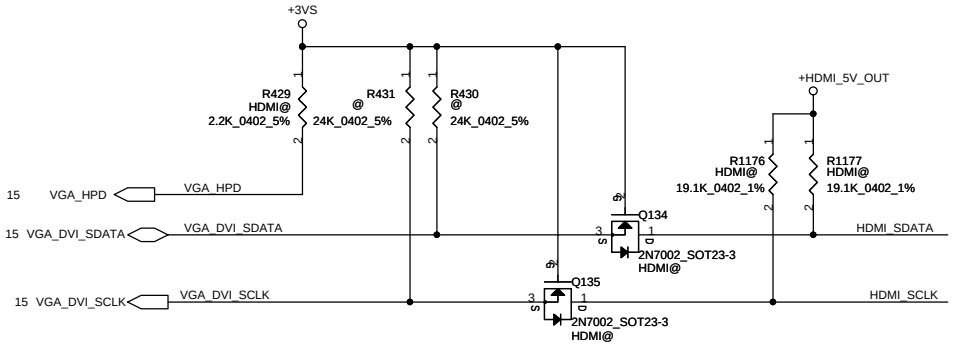
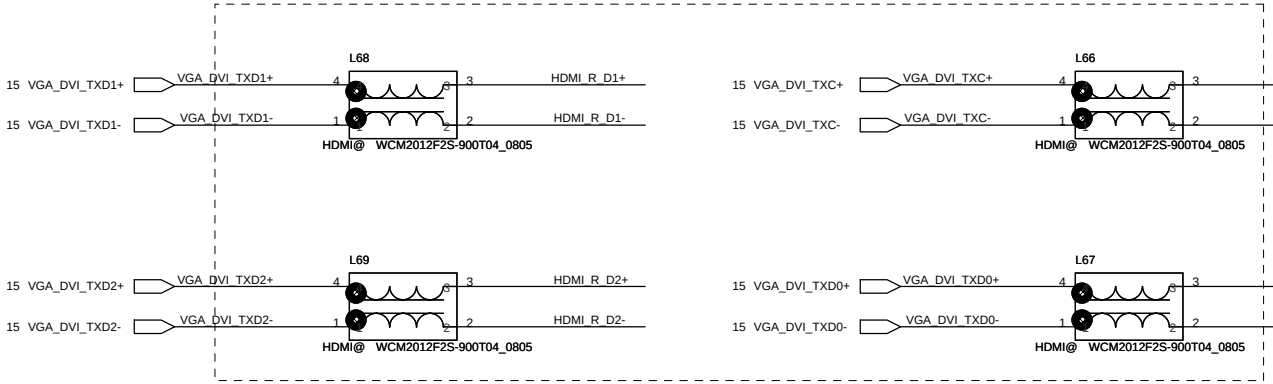
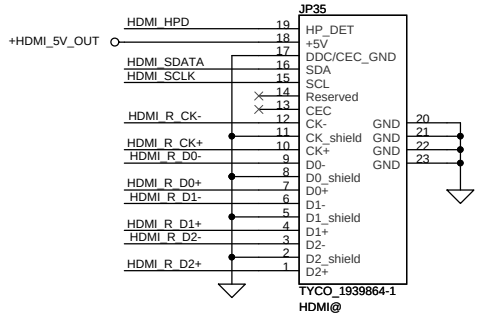


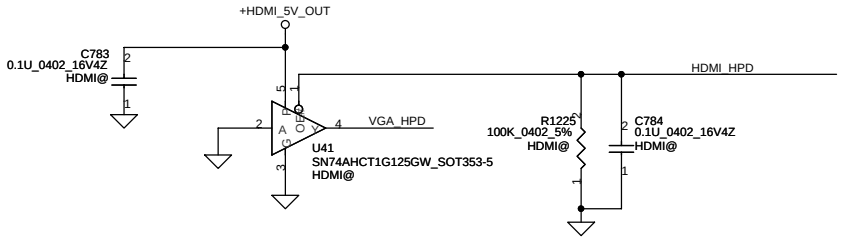


HDMI Connector





PVT: Delete all co-lay resistors.



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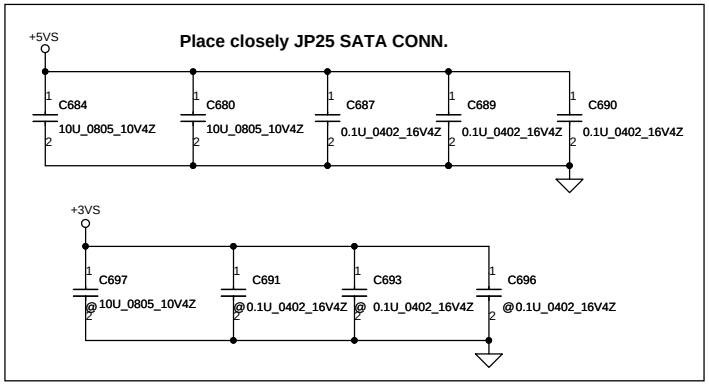
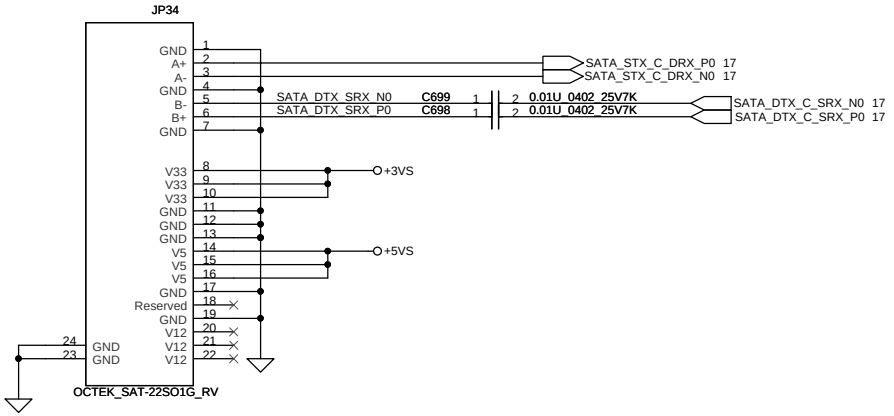
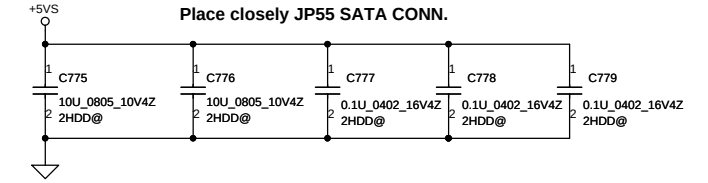
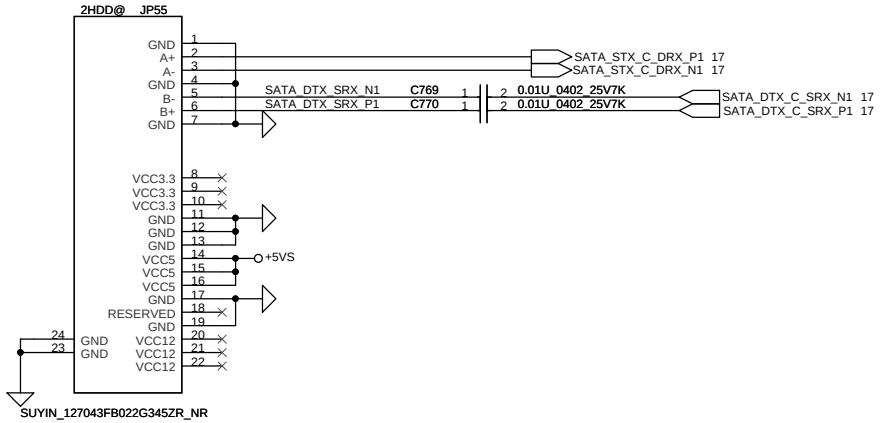
SATA HDD Conn.









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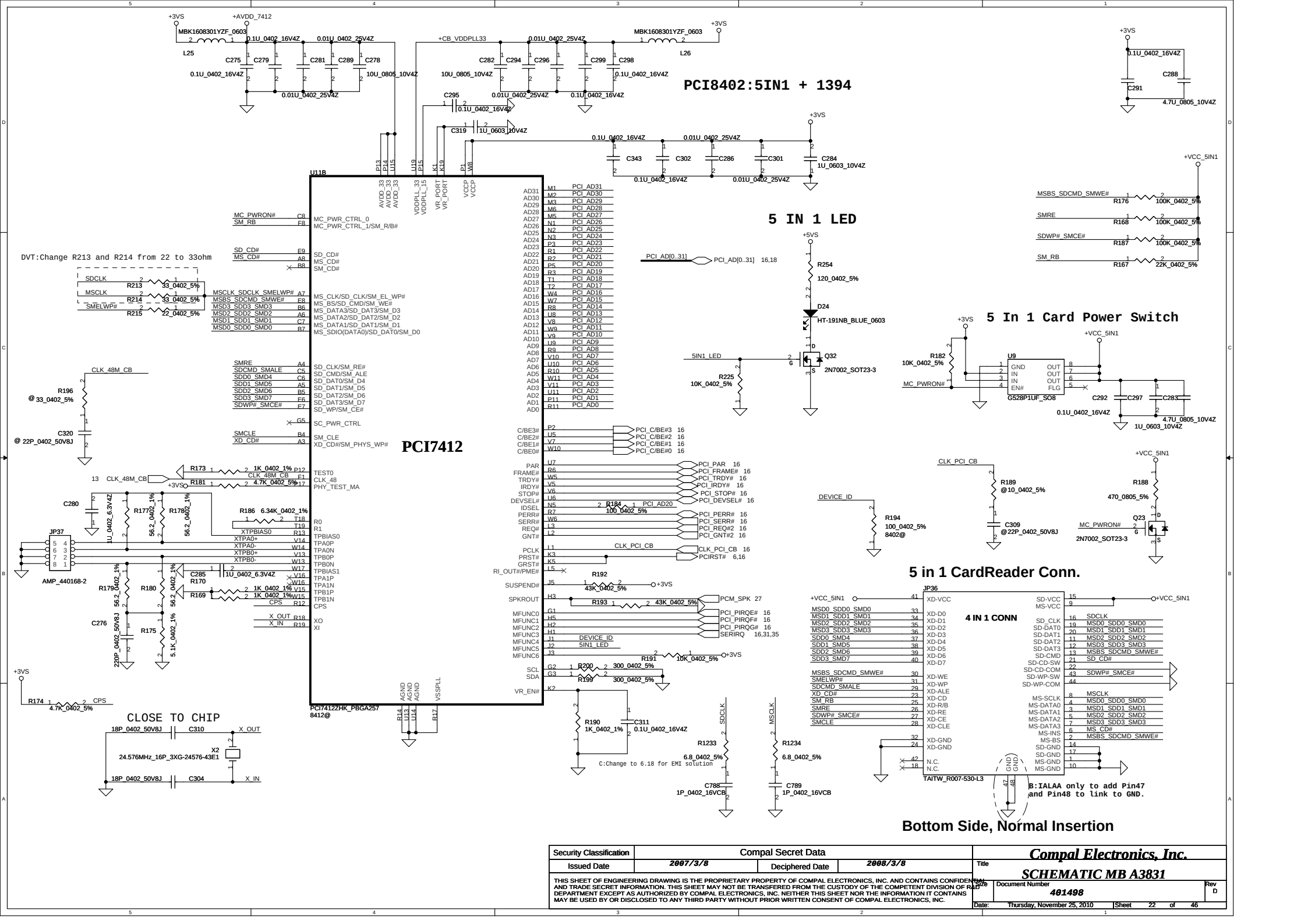
PCI8402:5IN1 + 1394
5 IN 1 LED
PCI7412
5 In 1 Card Power Switch
5 in 1 CardReader Conn.
4 IN 1 CONN
CLOSE TO CHIP
Bottom Side, Normal Insertion
DVT:Change R213 and R214 from 22 to 33ohm
C:Change to 6.18 for EMI solution
B:IALAA only to add Pin47 and Pin48 to link to GND.
PCI7412HK_PBGA257
8412@
TAITW_R007-530-L3
G528P1UF_SO8
AMP_440168-2
24.576MHz_16P_3XG-24576-43E1
Security Classification
Compal Secret Data
Issued Date
2007/3/8
Deciphered Date
2008/3/8
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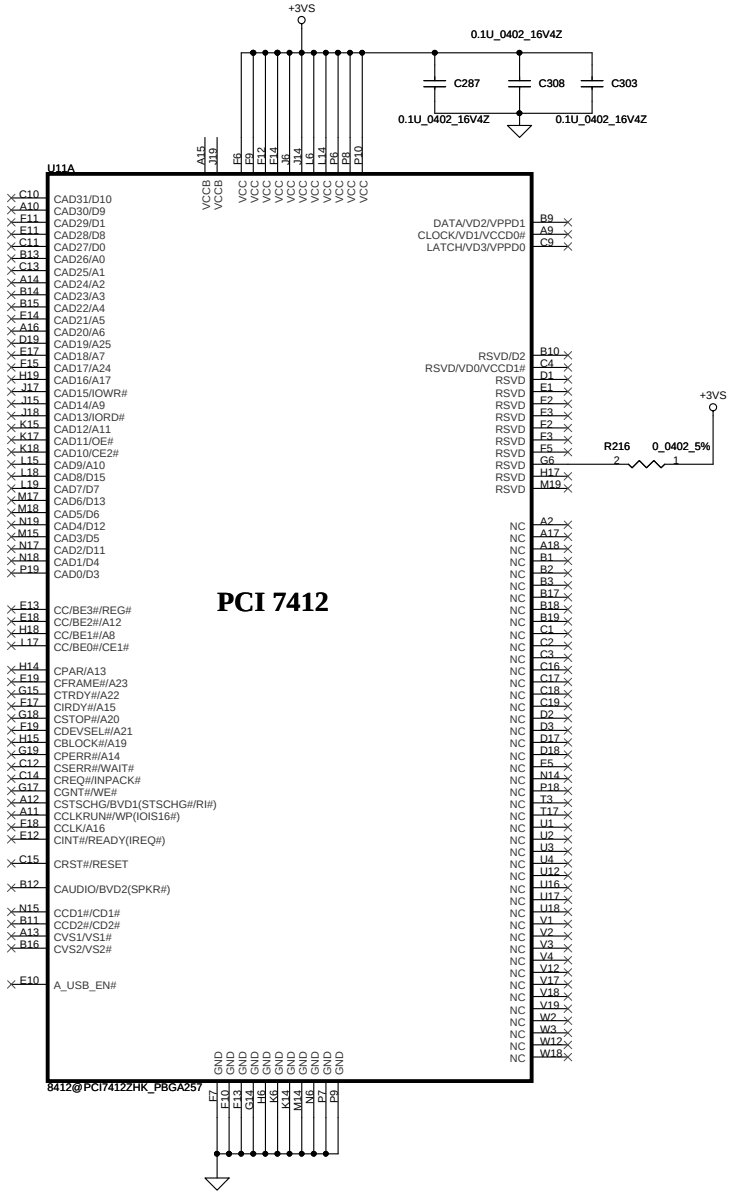

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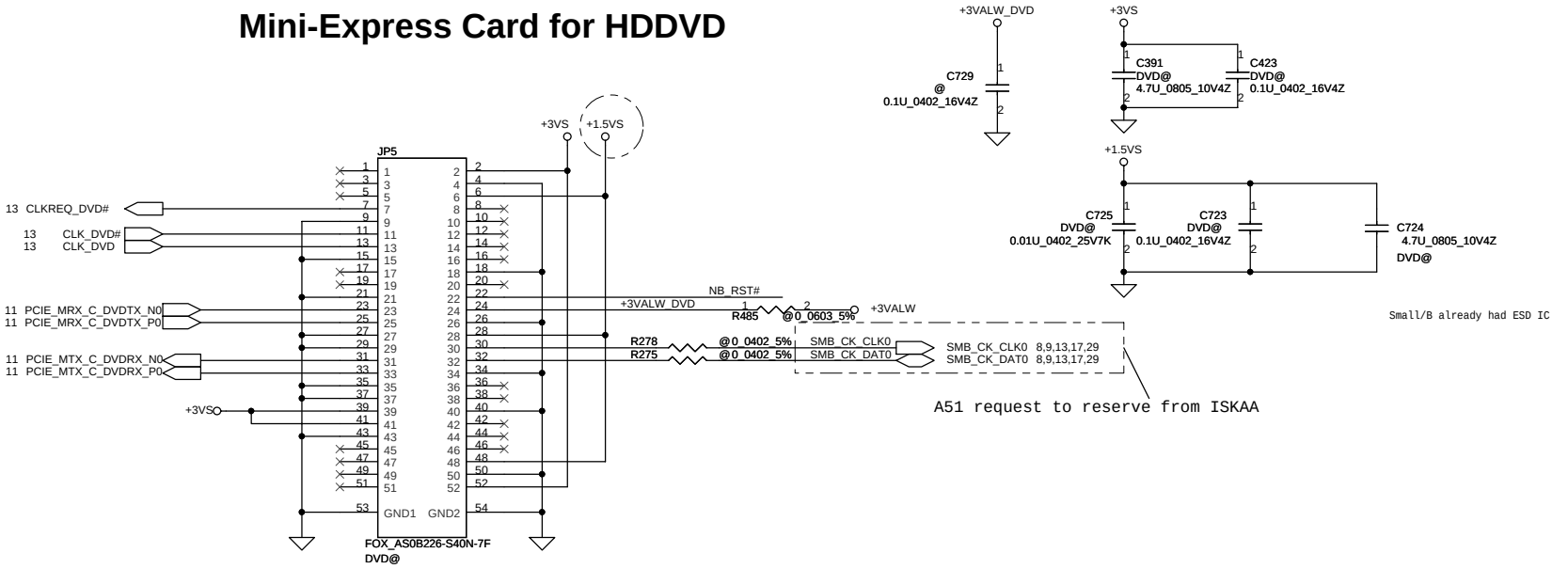
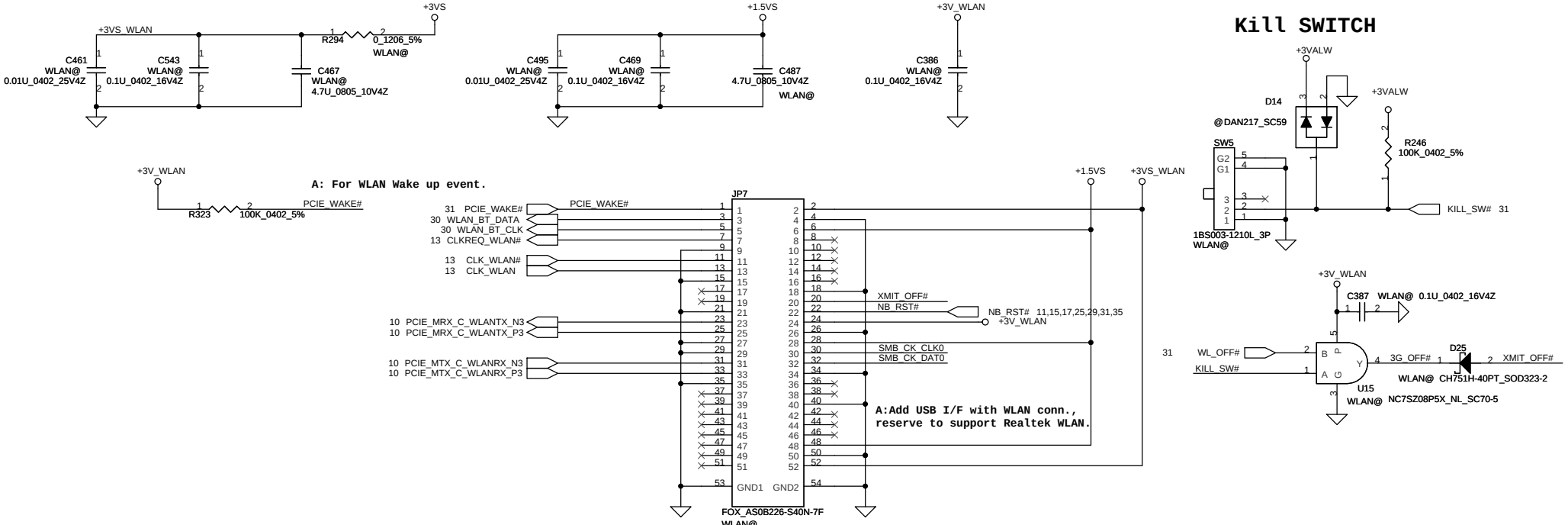
Mini-Express Card for HDDVD



Mini-Express Card for WLAN



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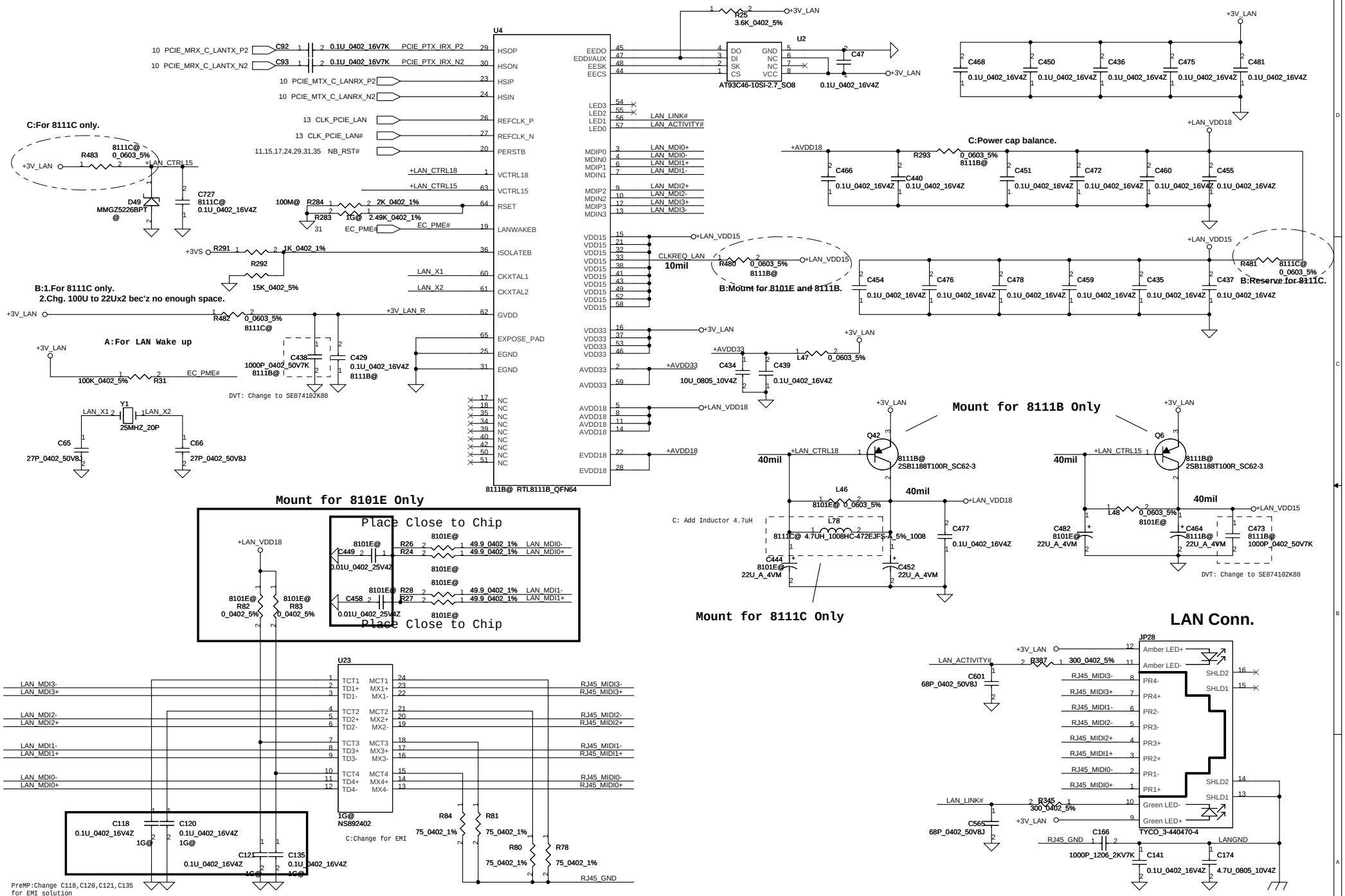

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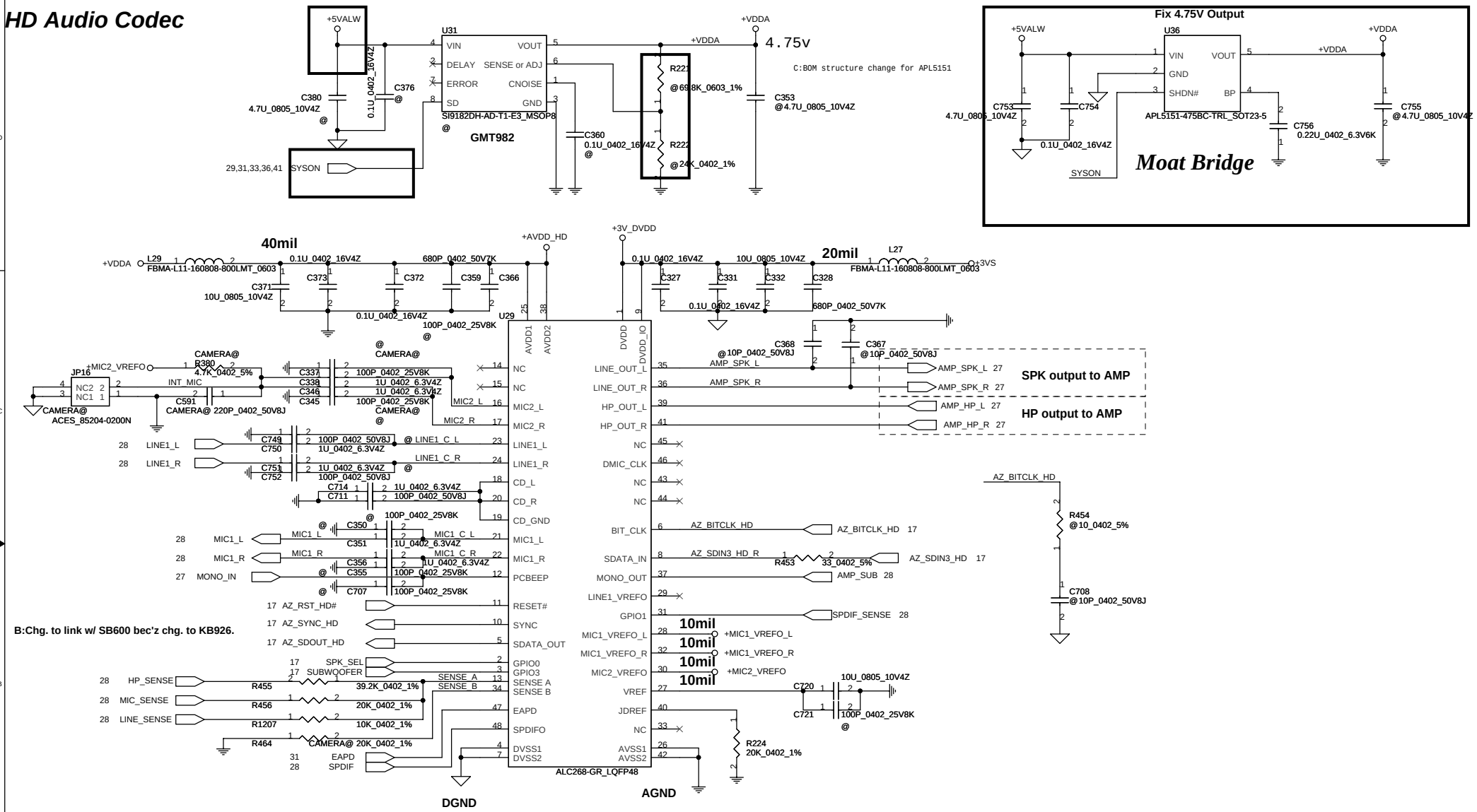
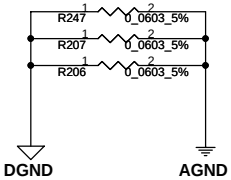
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

DGND To AGND Bypass



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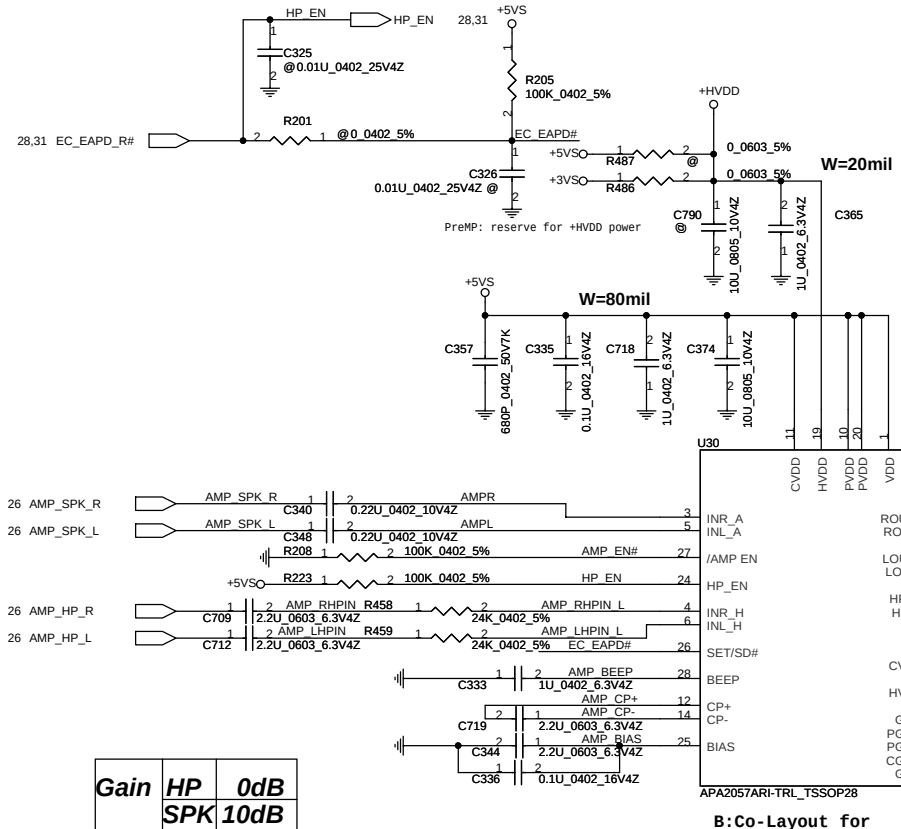
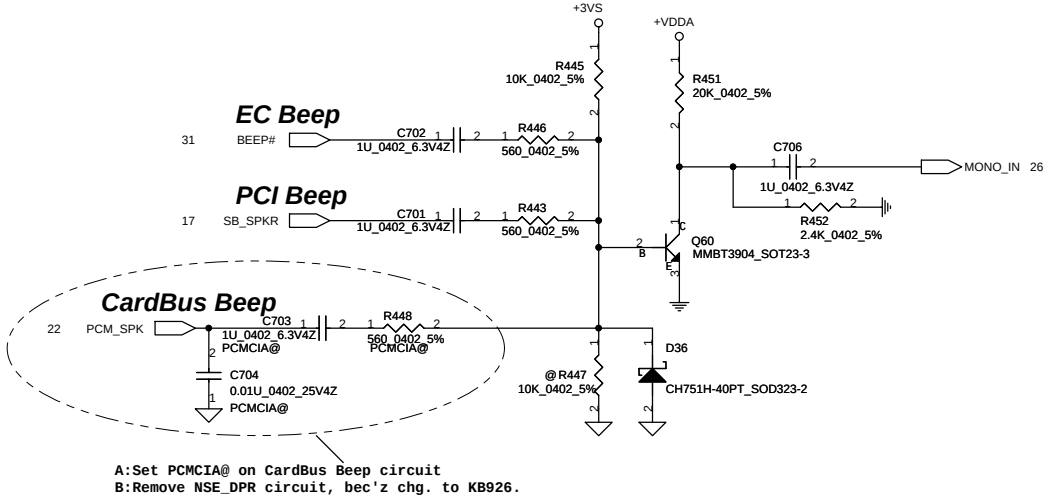


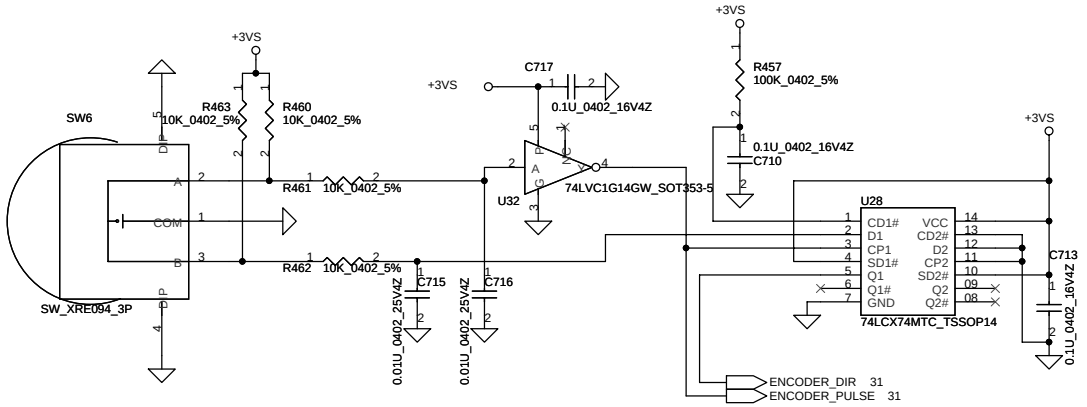
Gain	HP	0dB
	SPK	10dB

B:Co-Layout for APA2056A and APA2057A

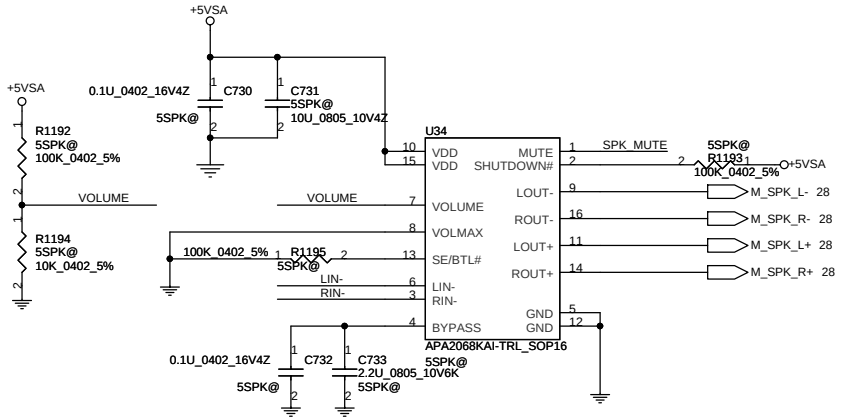


A:Set PCMCIA@ on CardBus Beep circuit
B:Remove NSE_DPR circuit, bec'z chg. to KB926.

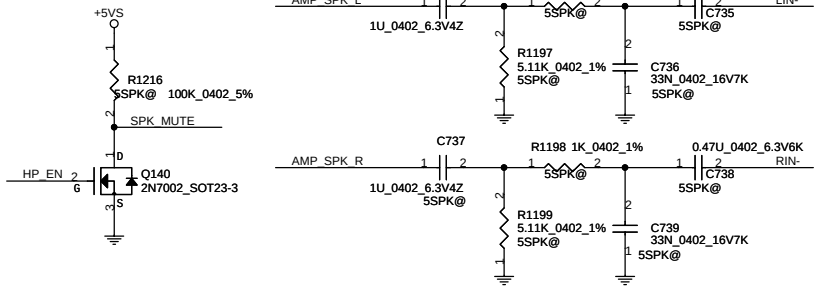
Volume Control



APA2068 Medium Range Amplifier



Pin2 /SD should be tied to 5V always and mute pin controled by EC_EAPD



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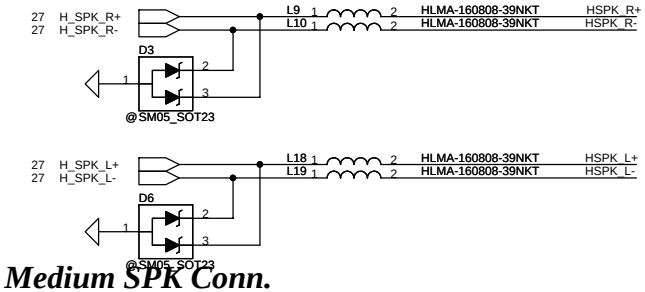
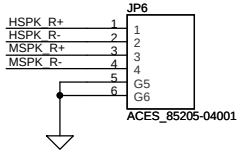
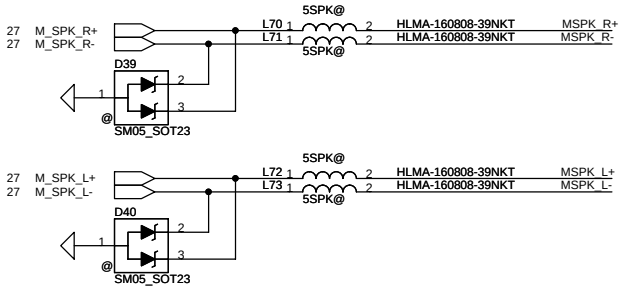
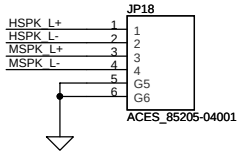
Tweeter Conn.



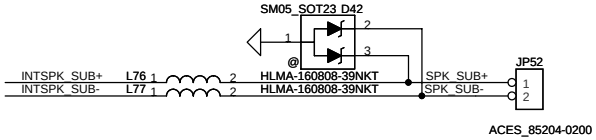


Medium SPK Conn.

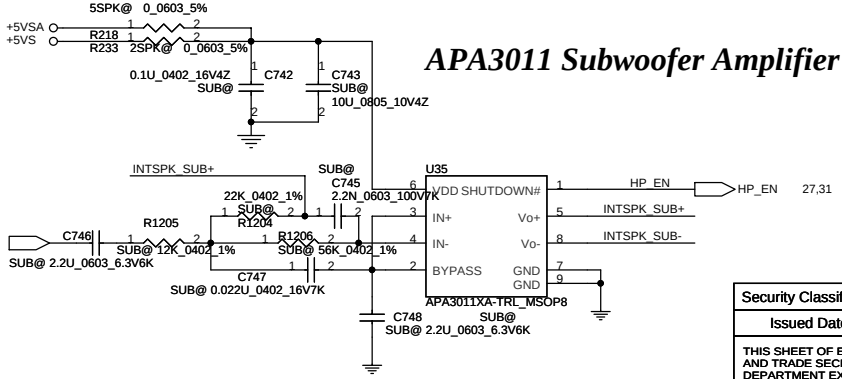




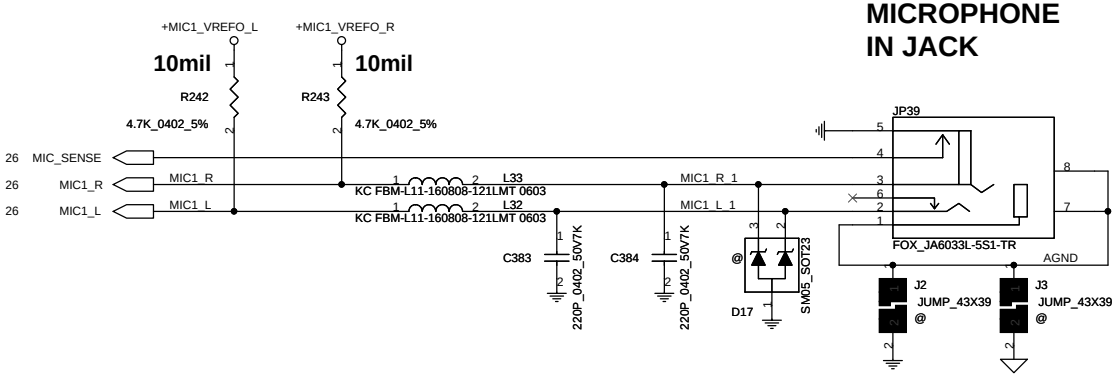
Sub-woofer Conn.



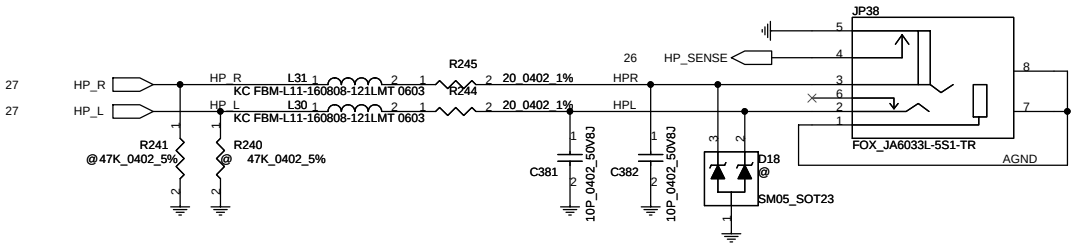
APA3011 Subwoofer Amplifier



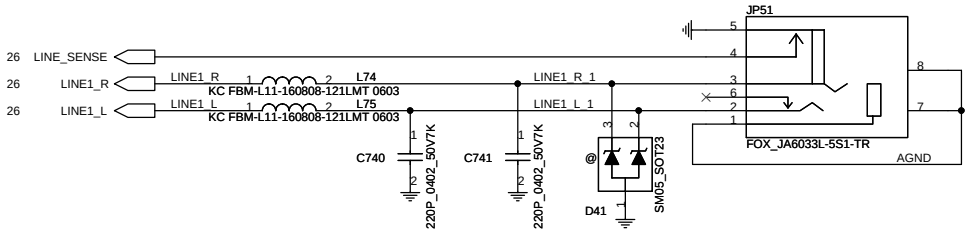
MICROPHONE IN JACK



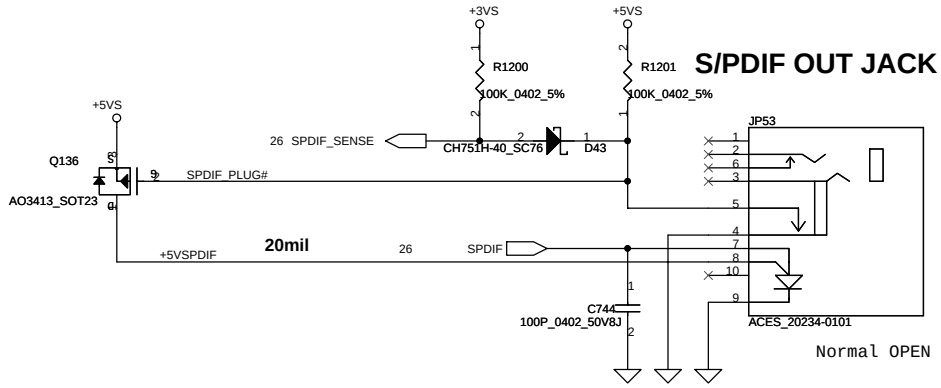
HEADPHONE OUT JACK



LINE IN JACK



S/PDIF OUT JACK



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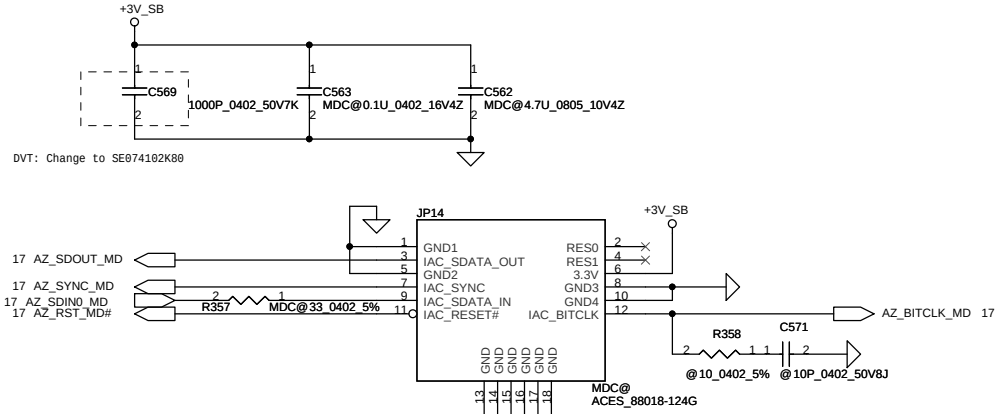
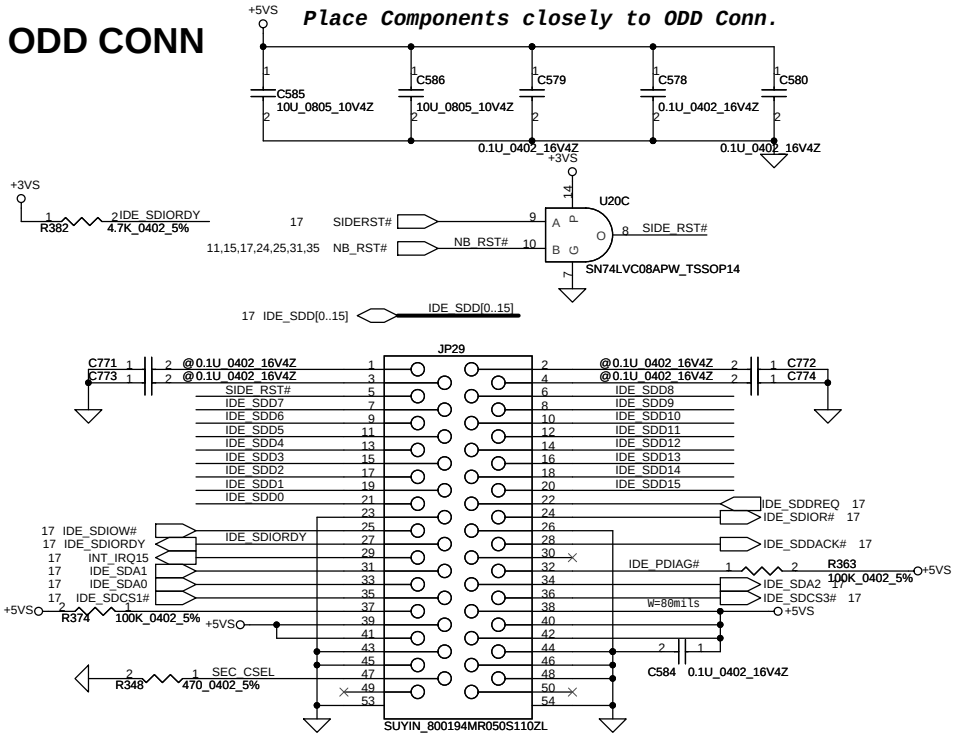
MDC 1.5 Conn.

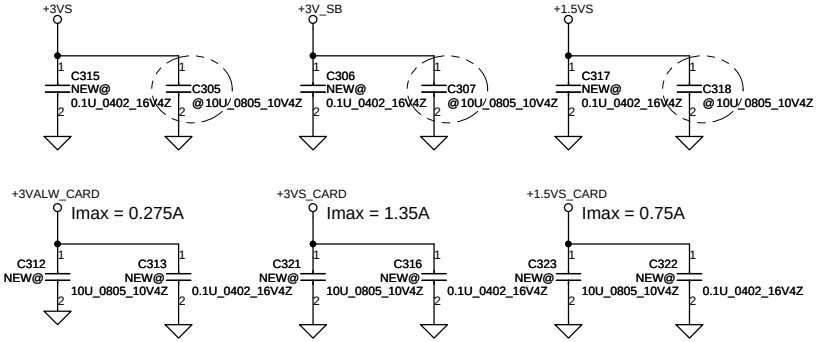


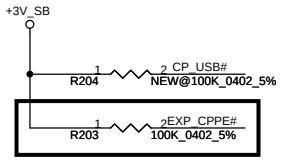
Connector for MDC Rev1.5

ODD CONN

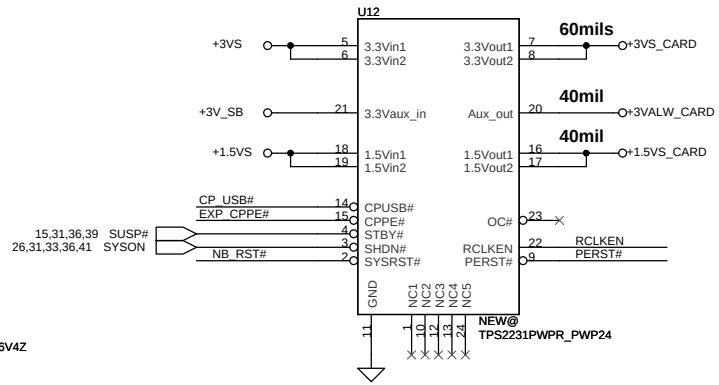


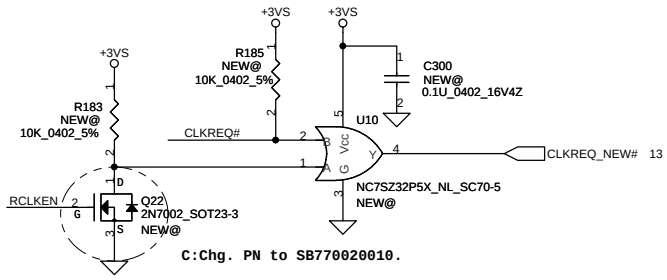
A:This symbol is for IALAA only, to add these two pins for Boss Hole.





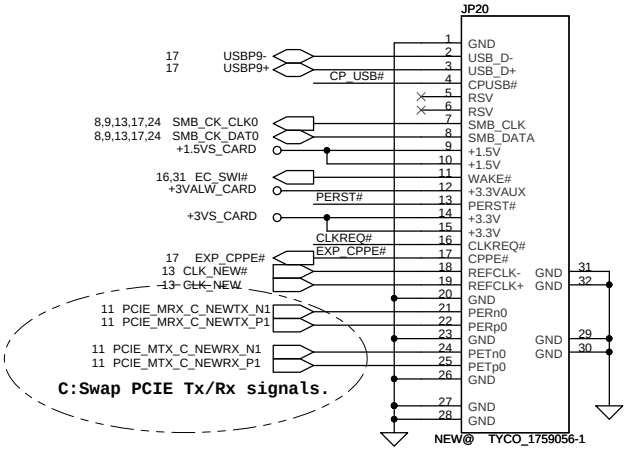
share with USB OC PIN need always pull high





C:Chg. PN to SB770020010.

B:relink DC030006O00.



C:Swap PCIE Tx/Rx signals.

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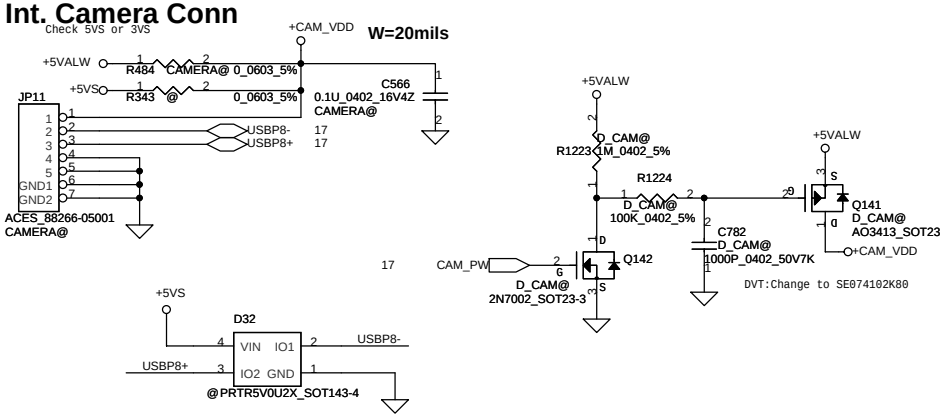
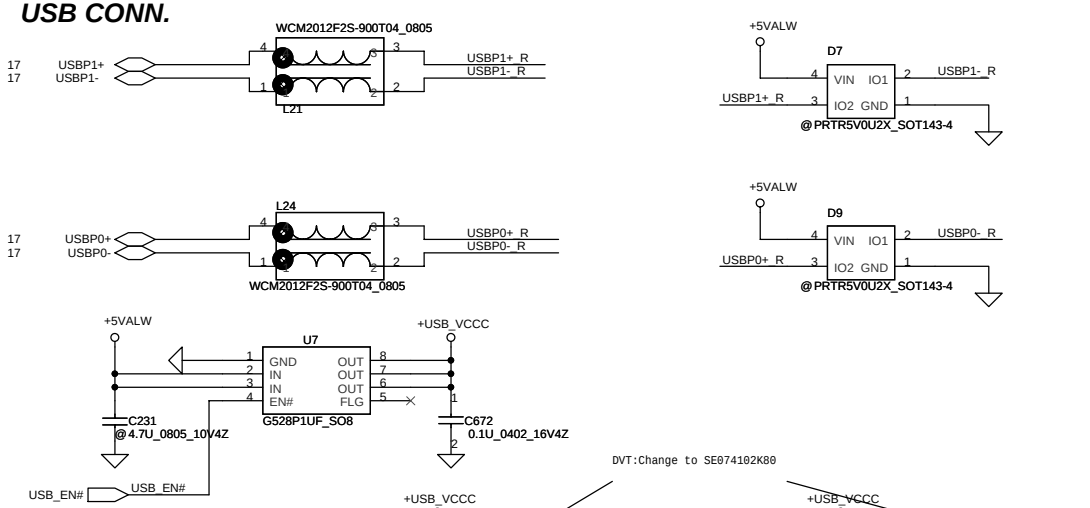
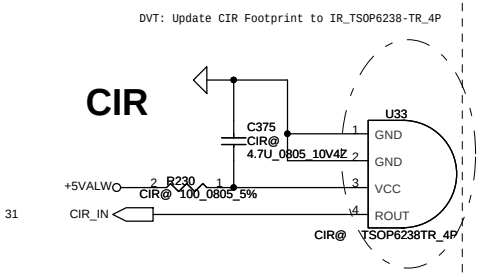
Int. Camera Conn



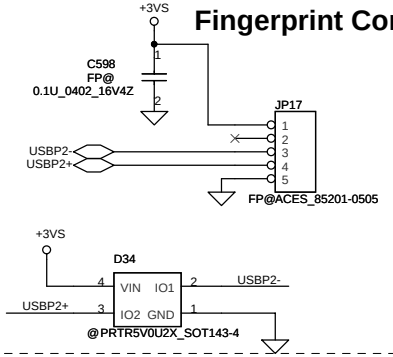
USB CONN.



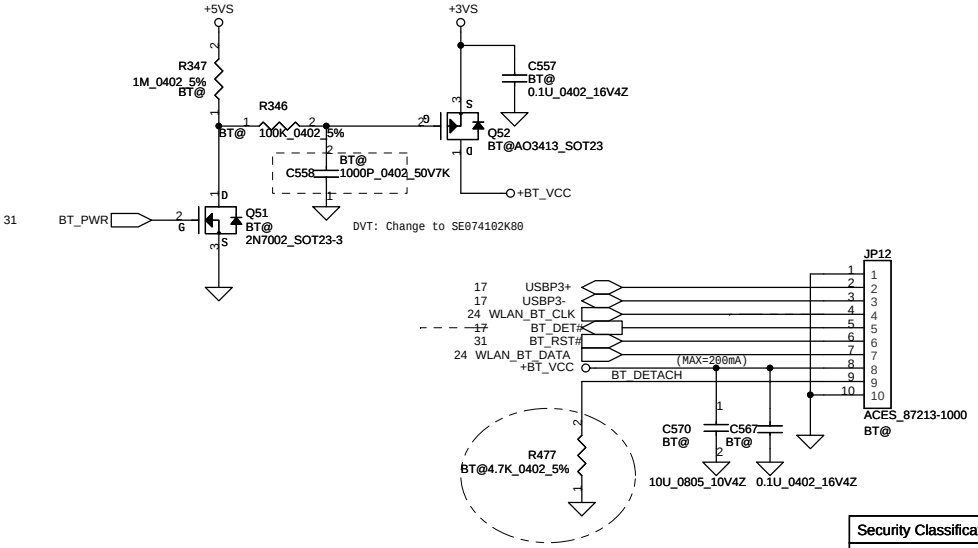
CIR



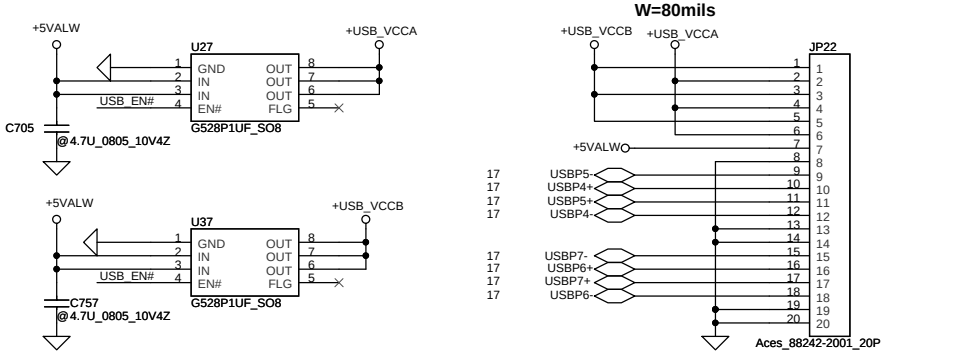
Fingerprint Conn



BlueTooth Interface



USB Small Board



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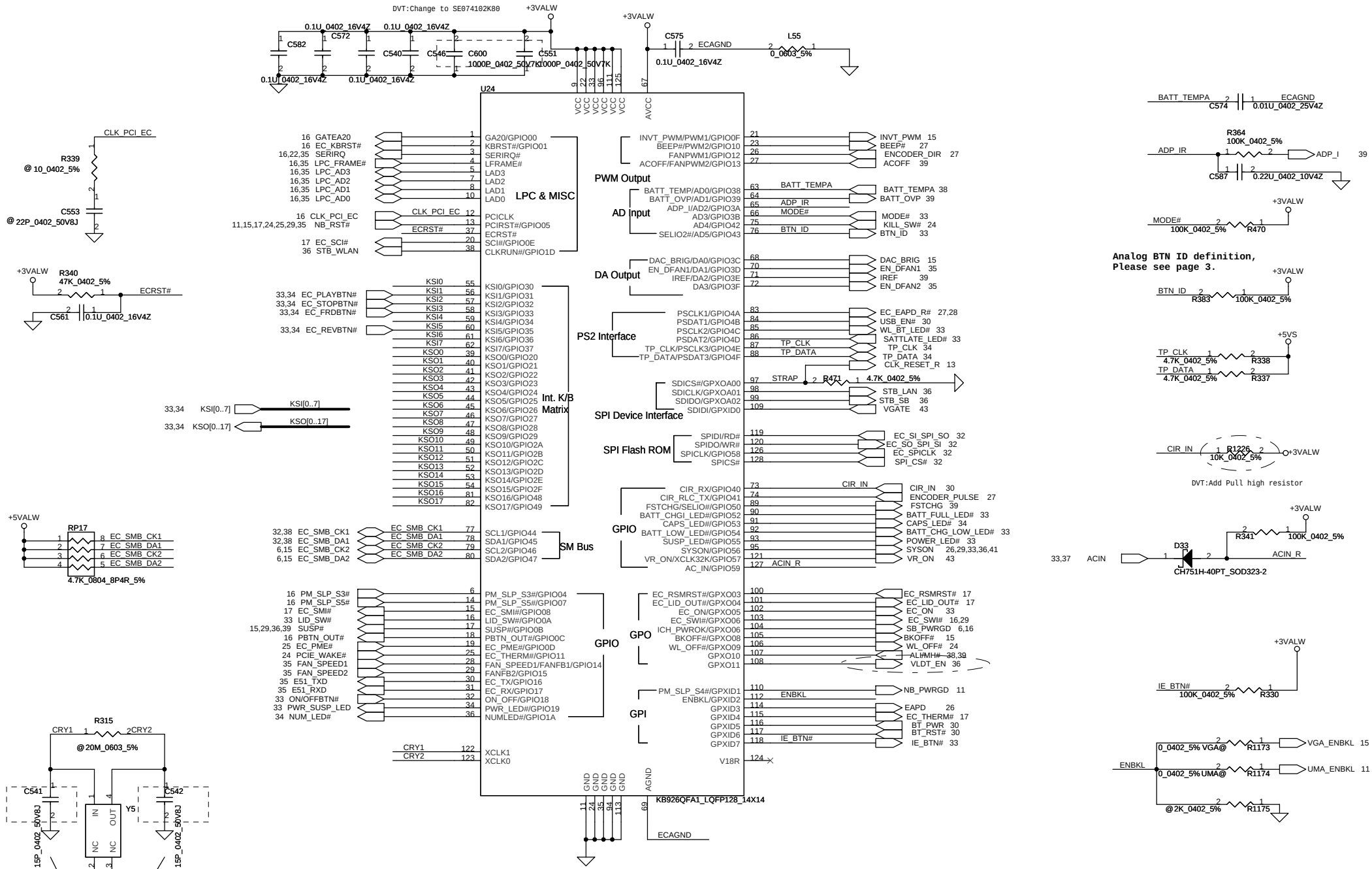

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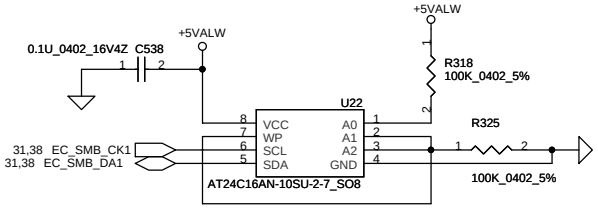
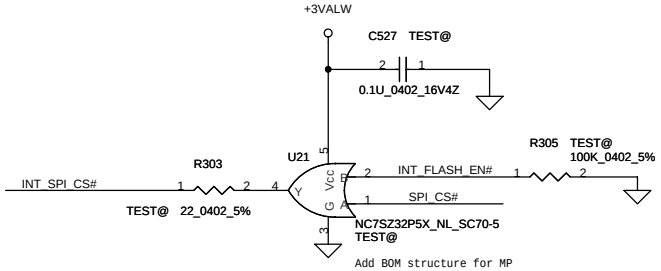
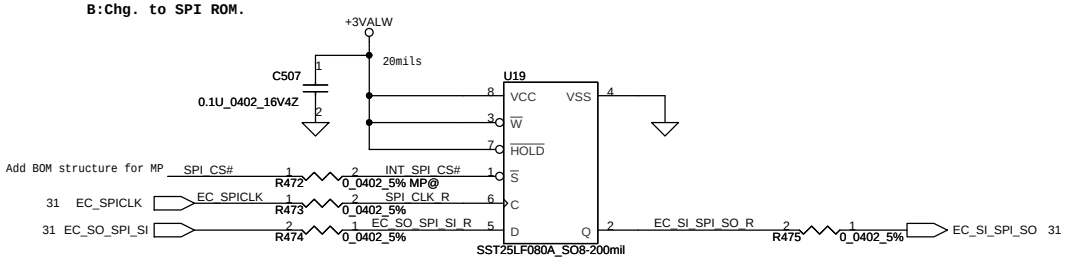
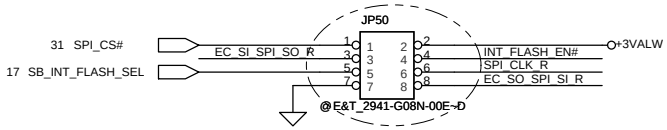




SPI Flash (8Mb*1)

B:Chg. to SPI ROM.





C:Chg. PN to LTC00000200

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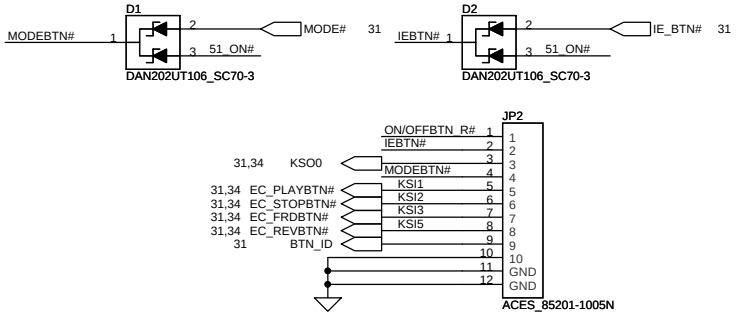
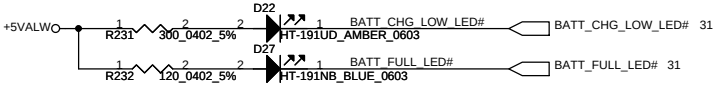
SW/LED Connector

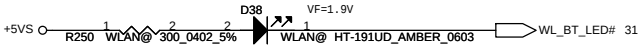


AC IN LED

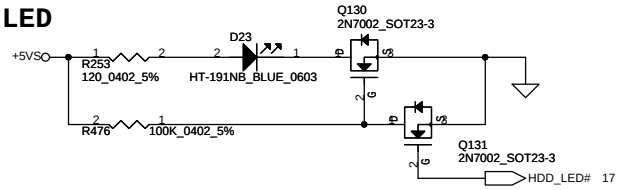
BATT CHARGE/FULL LED



WL&BT LED



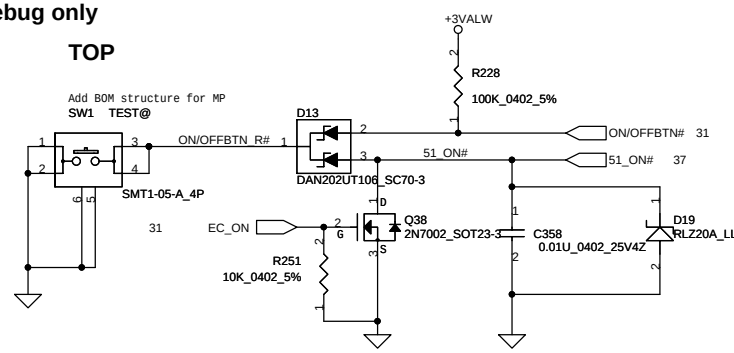
HDD LED



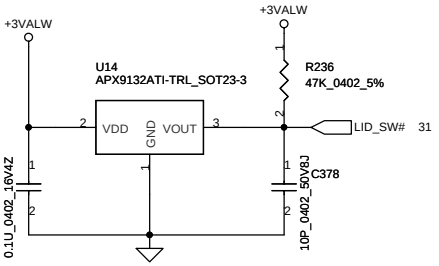
Power Button

For debug only

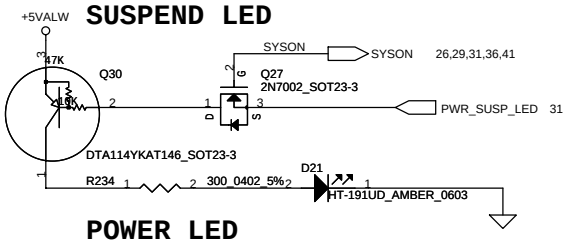
BTN TOP



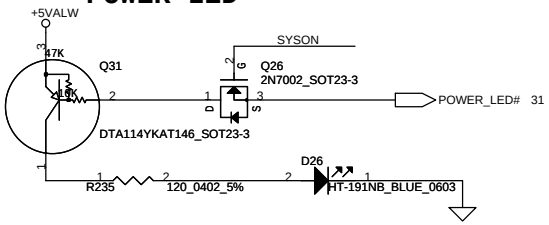
Lid SW



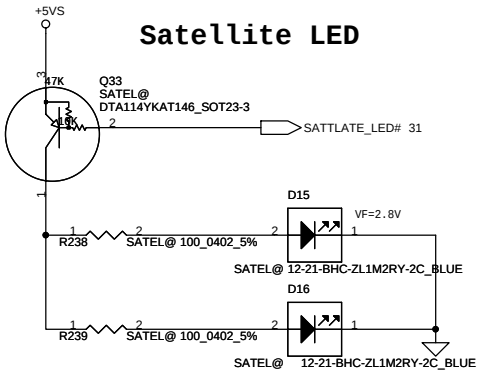
SUSPEND LED



POWER LED



Satellite LED



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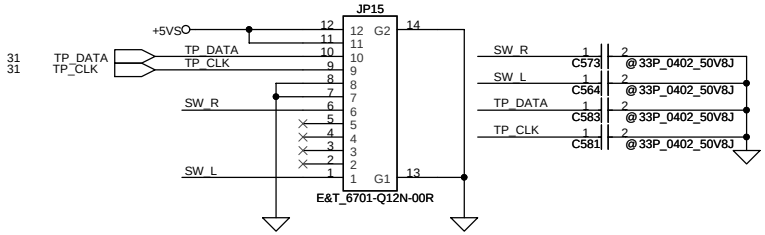
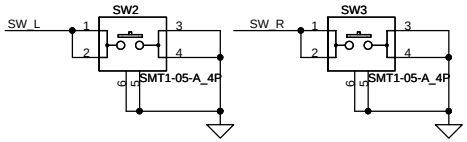
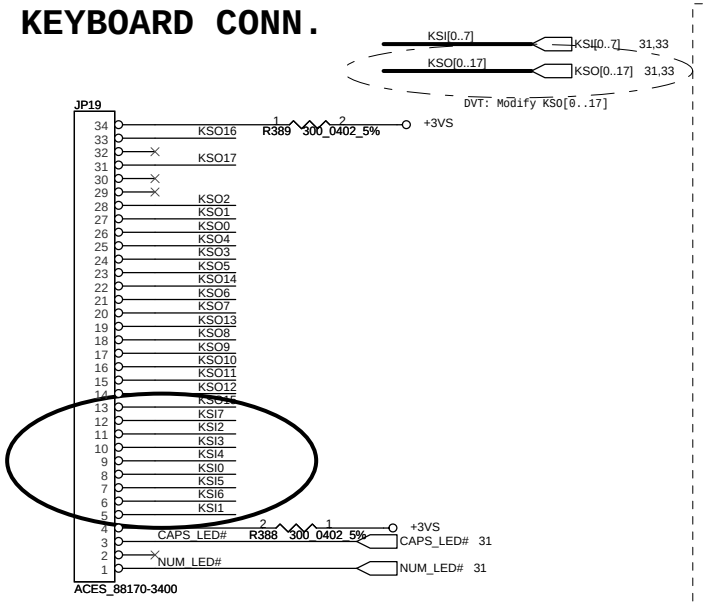
TP CONN.

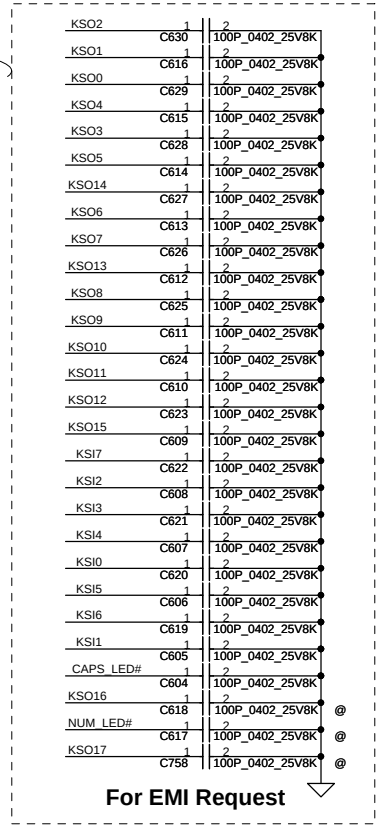


TP Button



KEYBOARD CONN.





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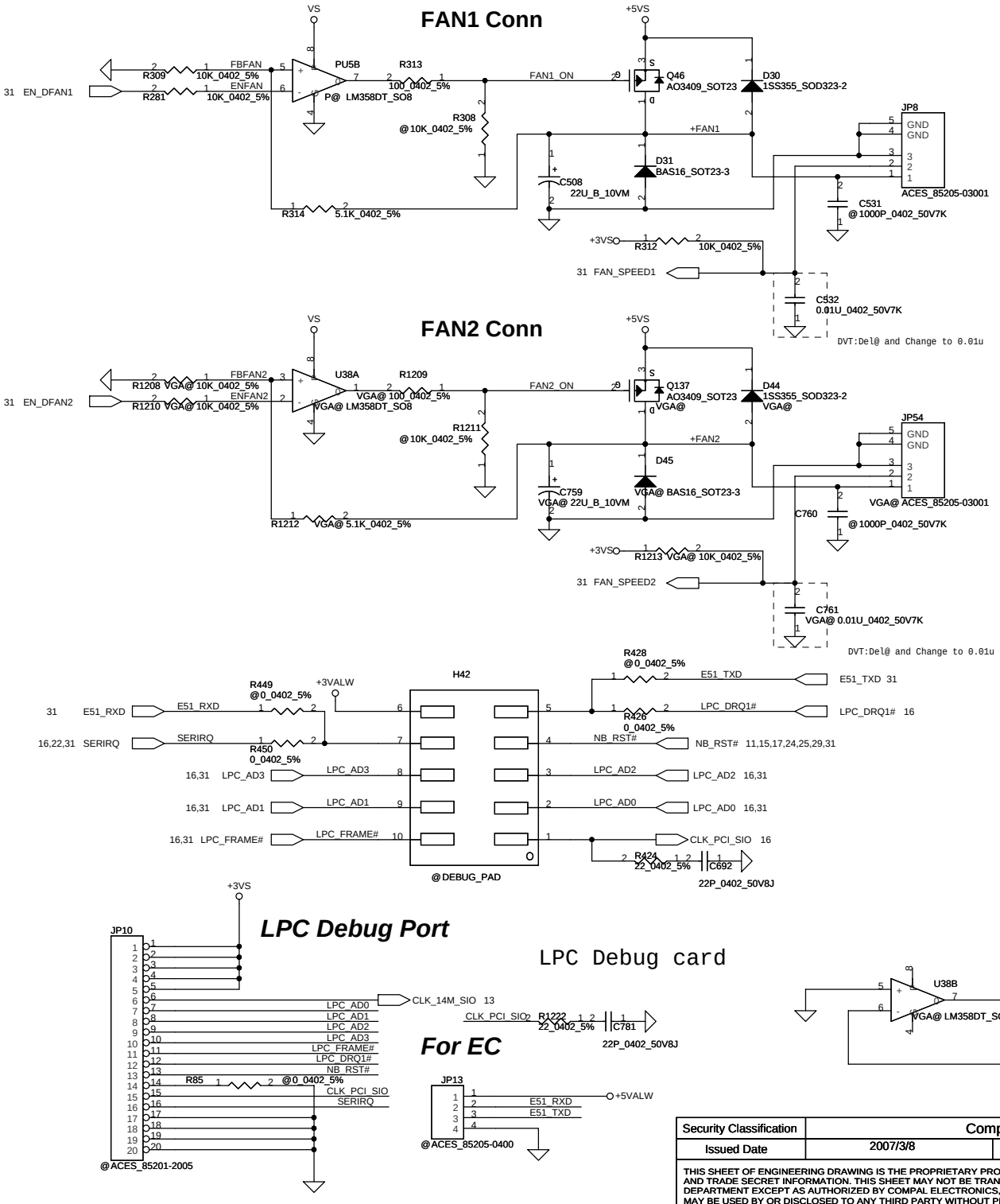

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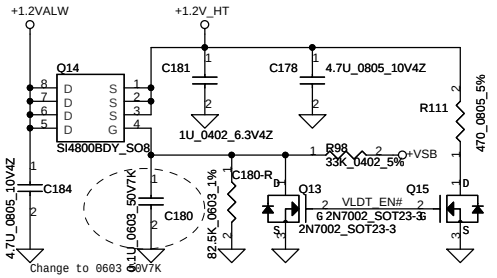
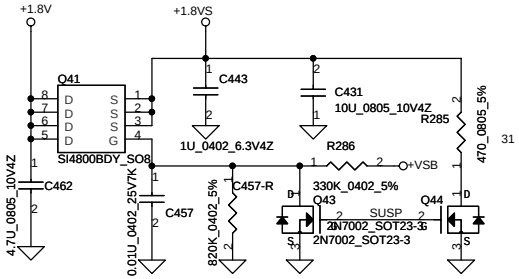
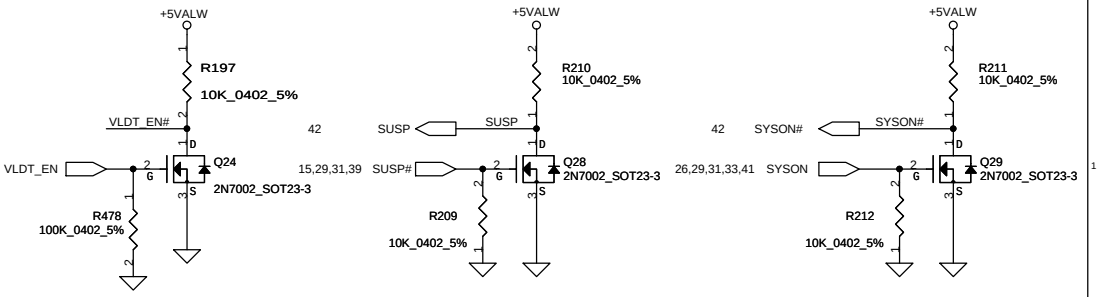
+1.2VALW TO +1.2V_HT

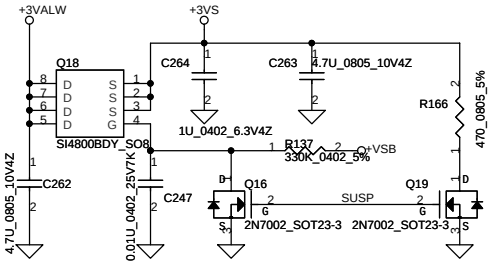


+1.8V TO +1.8VS

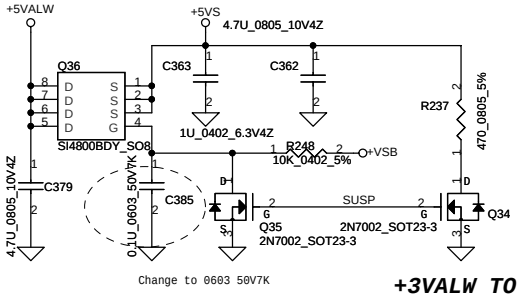


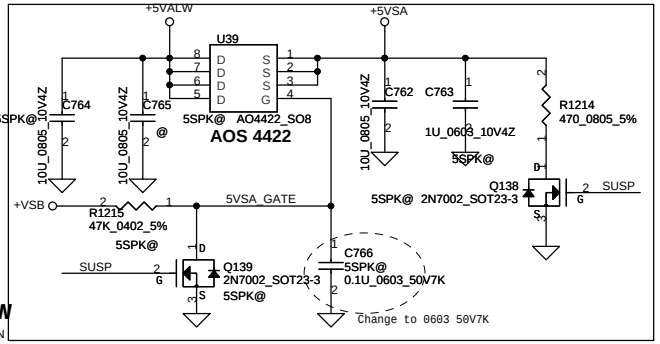


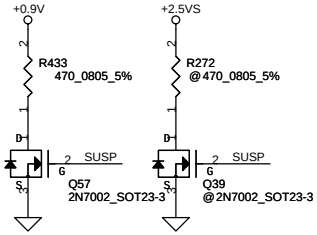
+3VALW TO +3VS



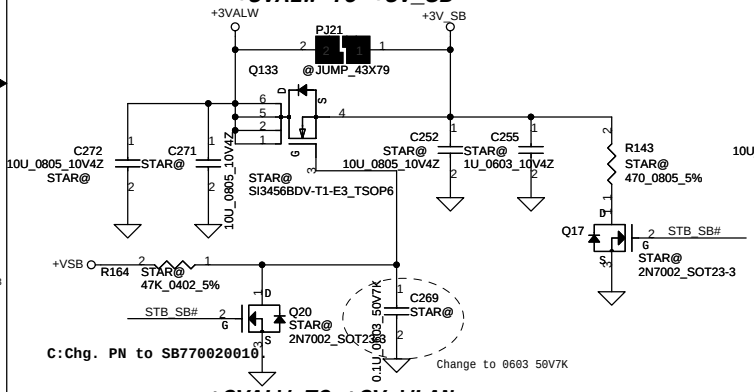
+5VALW TO +5VS





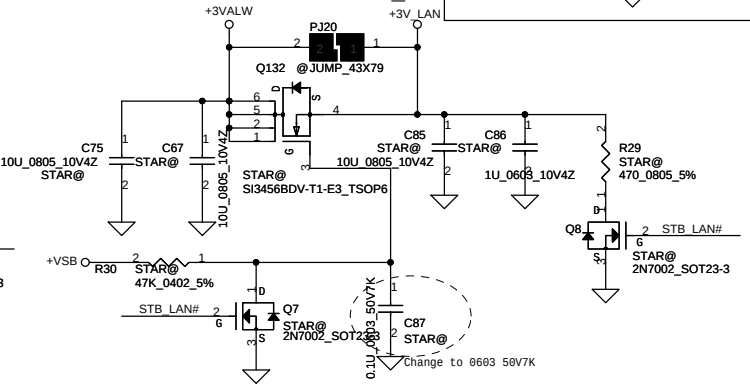


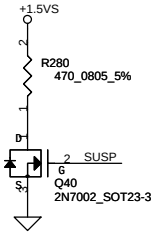
+3VALW TO +3V_SB

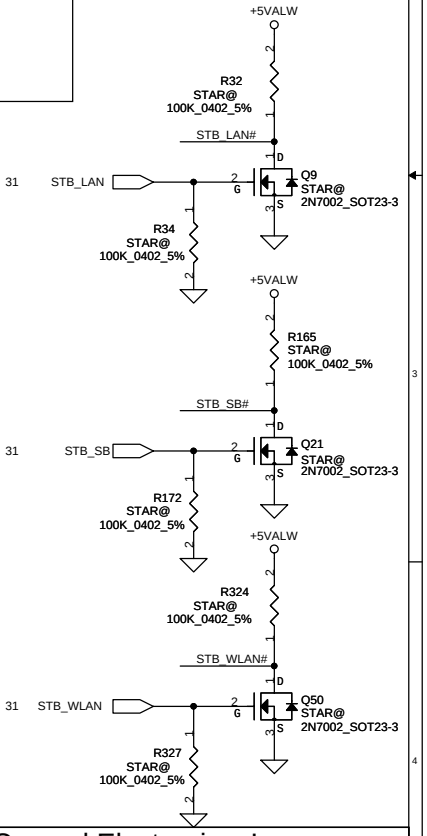


C:Chg. PN to SB770020010.

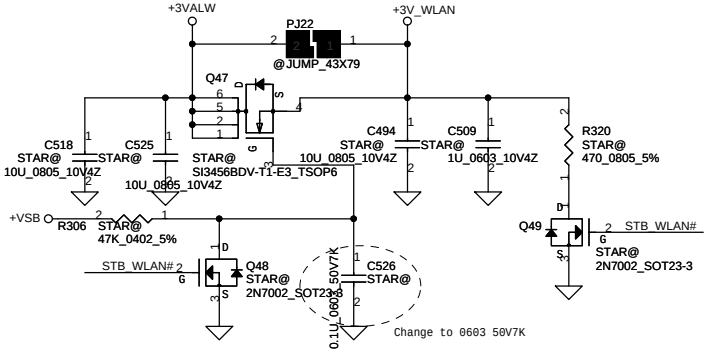
+3VALW TO +3V_LAN



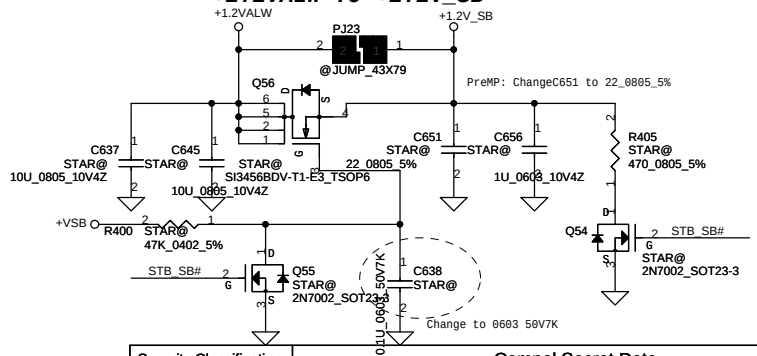




+3VALW TO +3V_WLAN



+1.2VALW TO +1.2V_SB



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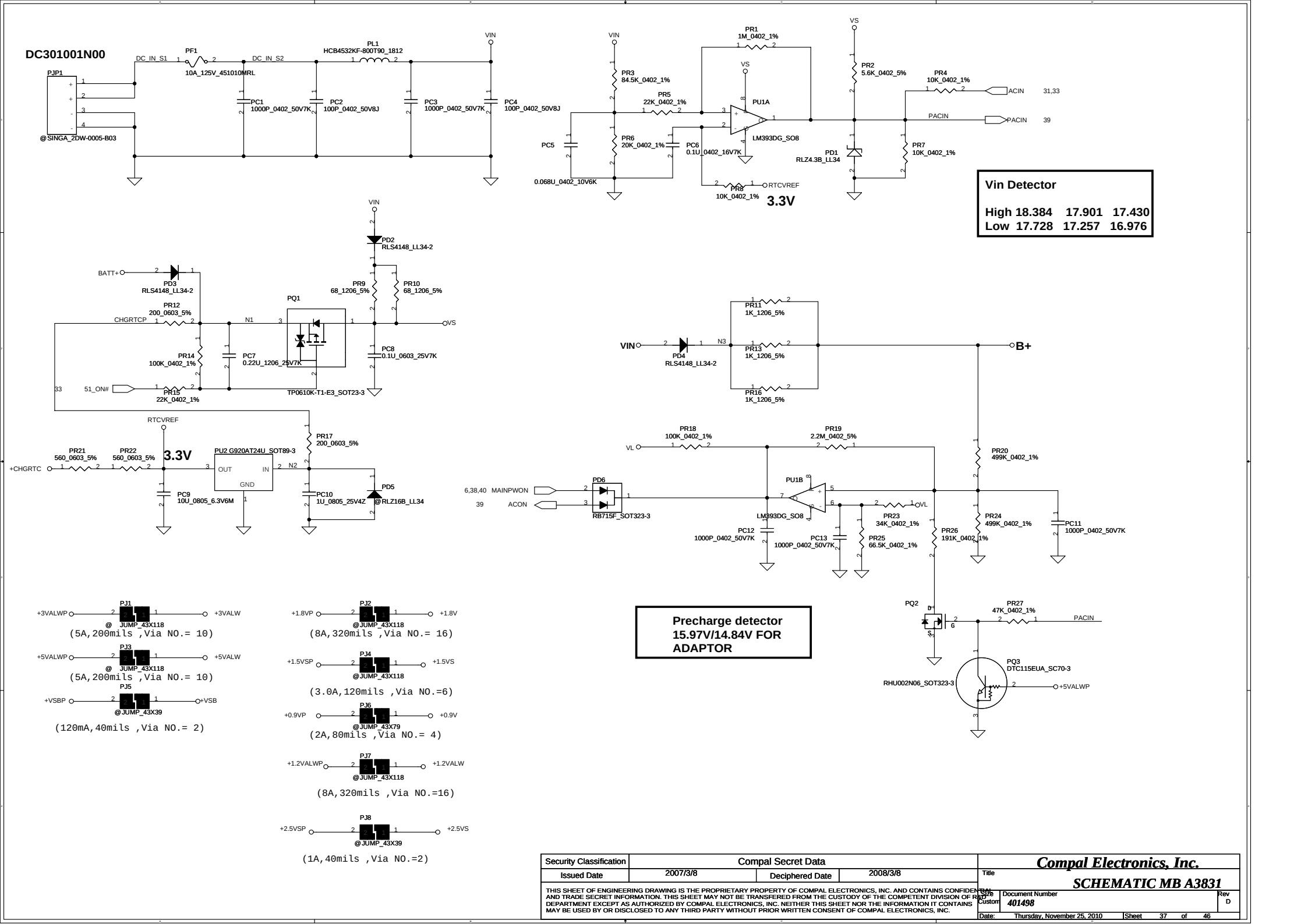

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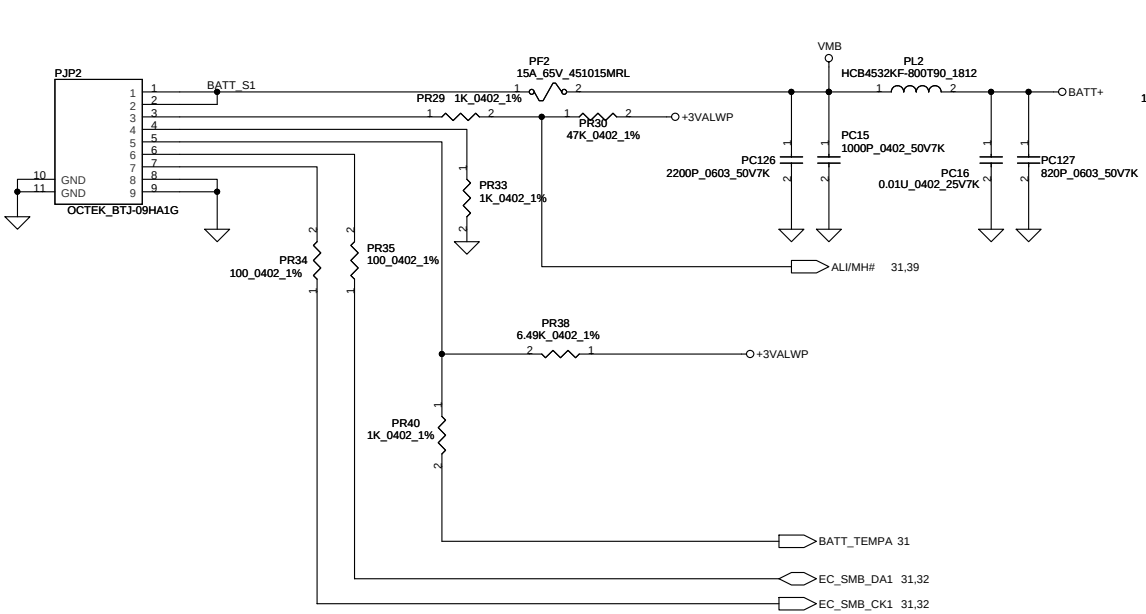
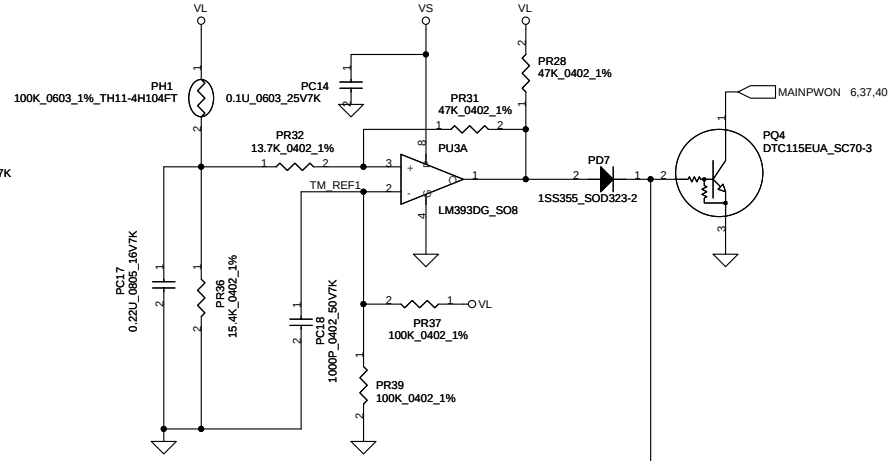
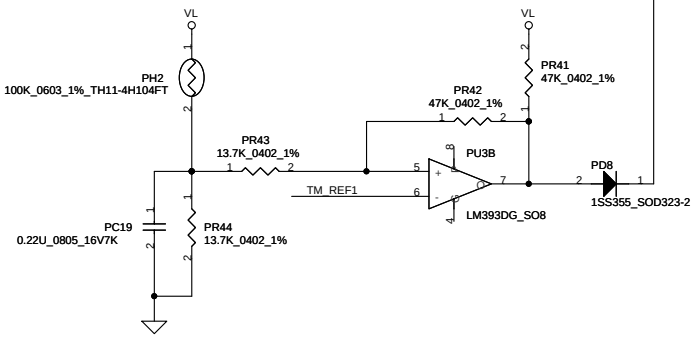
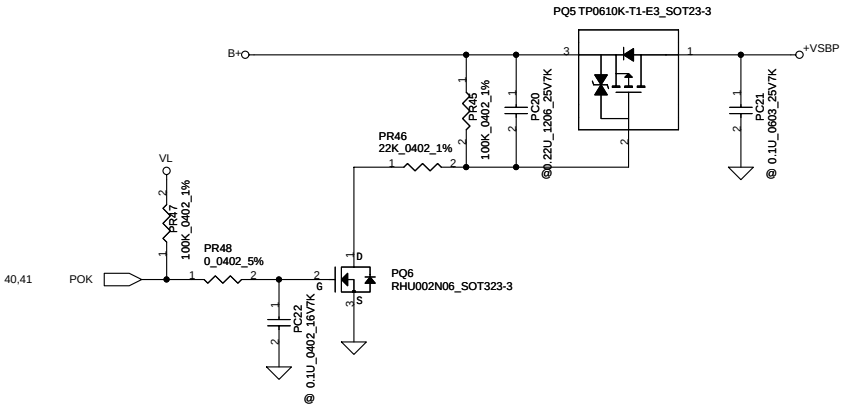
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 95 degree C
Recovery at 59 degree C





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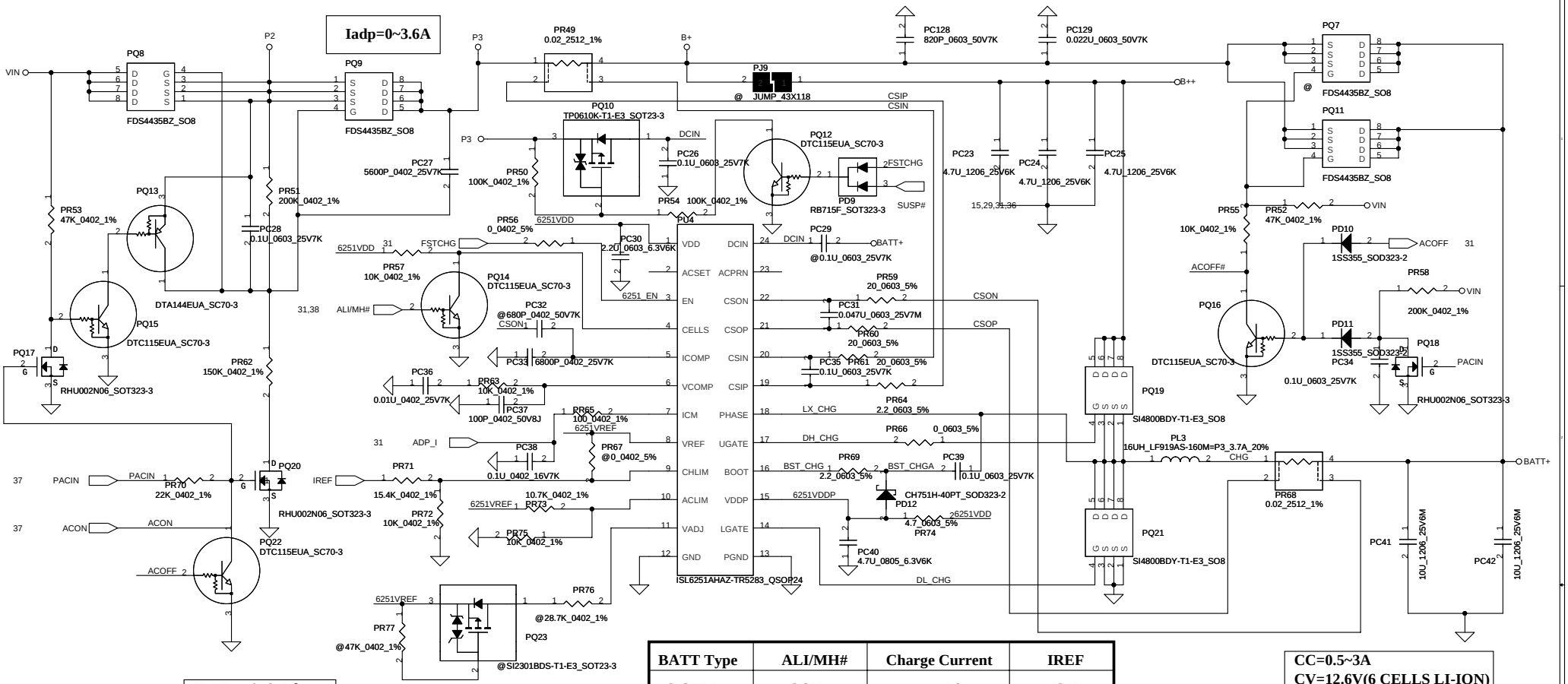


IREF=1.016*Icharge
IREF=0.508V~3.048V

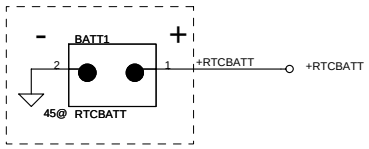
BATT Type	ALI/MH#	Charge Current	IREF
3 CELL	3.3V	1.5A	1.524V
6 CELL	3.3V	3.0A	3.048V
9 CELL	3.3V	3.0A	3.048V

CC=0.5~3A
CV=12.6V(6 CELLS LI-ION)

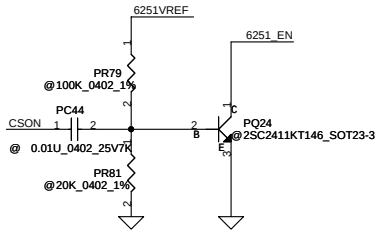
RTC Battery

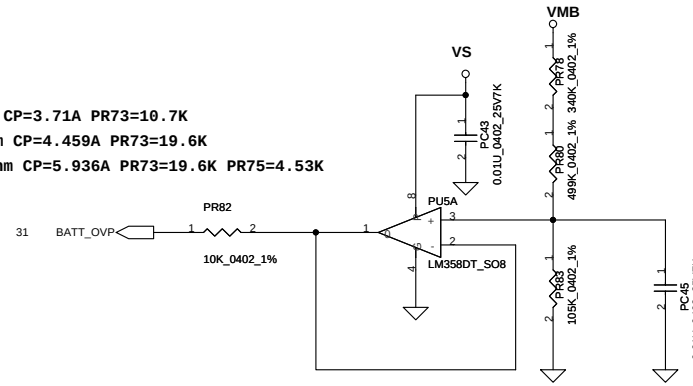
Layout Note:

1. Under BATT1 battery Body, no Trace no Via
2. BATT1 + - PIN keep out 80mil from other component ,trace and via



75W Iadapter=0~3.947A PR49=0.02 ohm CP=3.71A PR73=10.7K
90W Iadapter=0~4.737A PR49=0.015 ohm CP=4.459A PR73=19.6K
120W Iadapter=0~6.315A PR49=0.010 ohm CP=5.936A PR73=19.6K PR75=4.53K





LI-3S :13.5V----BATT-OVP=1.5V
LI-4S :18V----BATT-OVP=2V
BATT-OVP=0.111*BATT+

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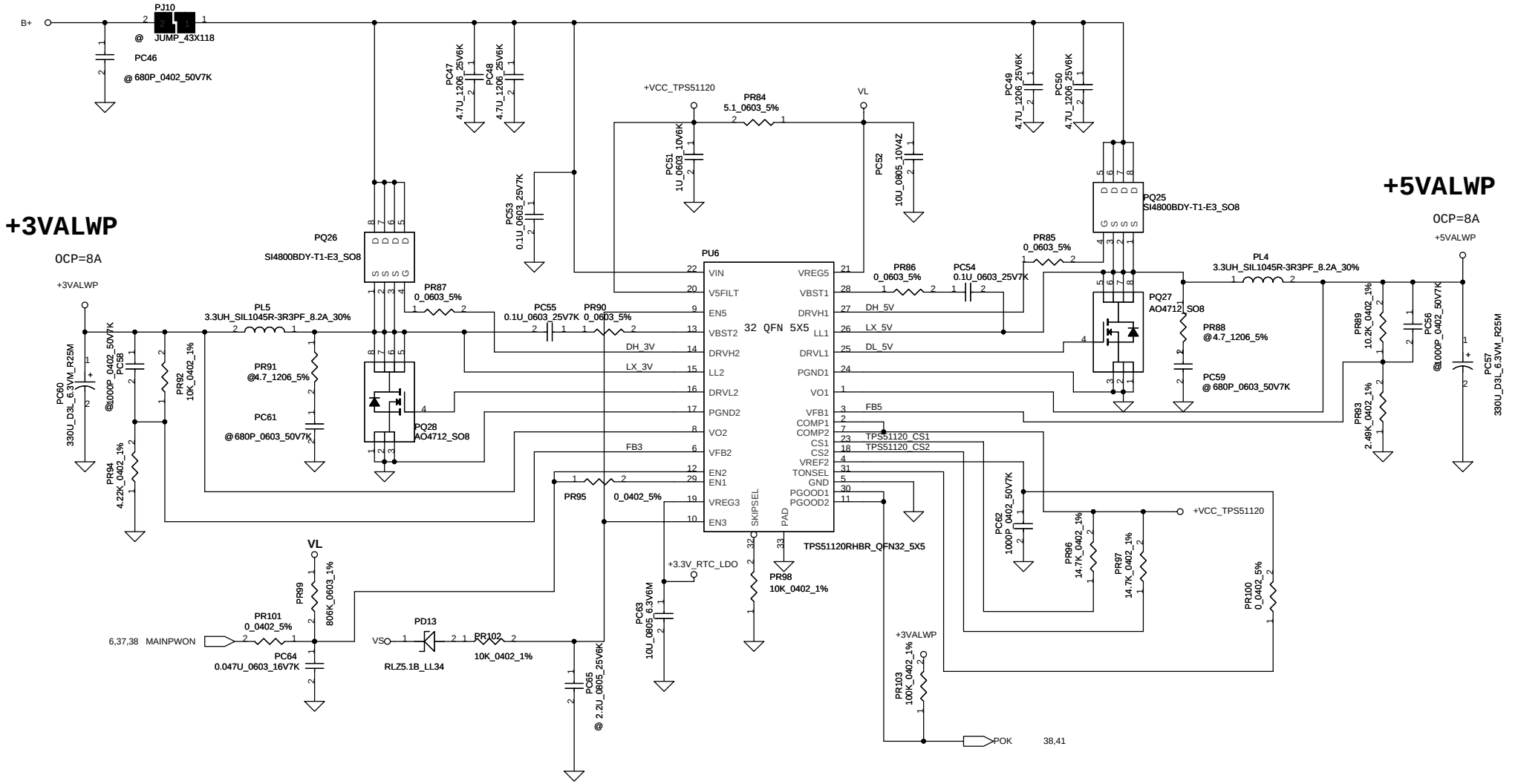

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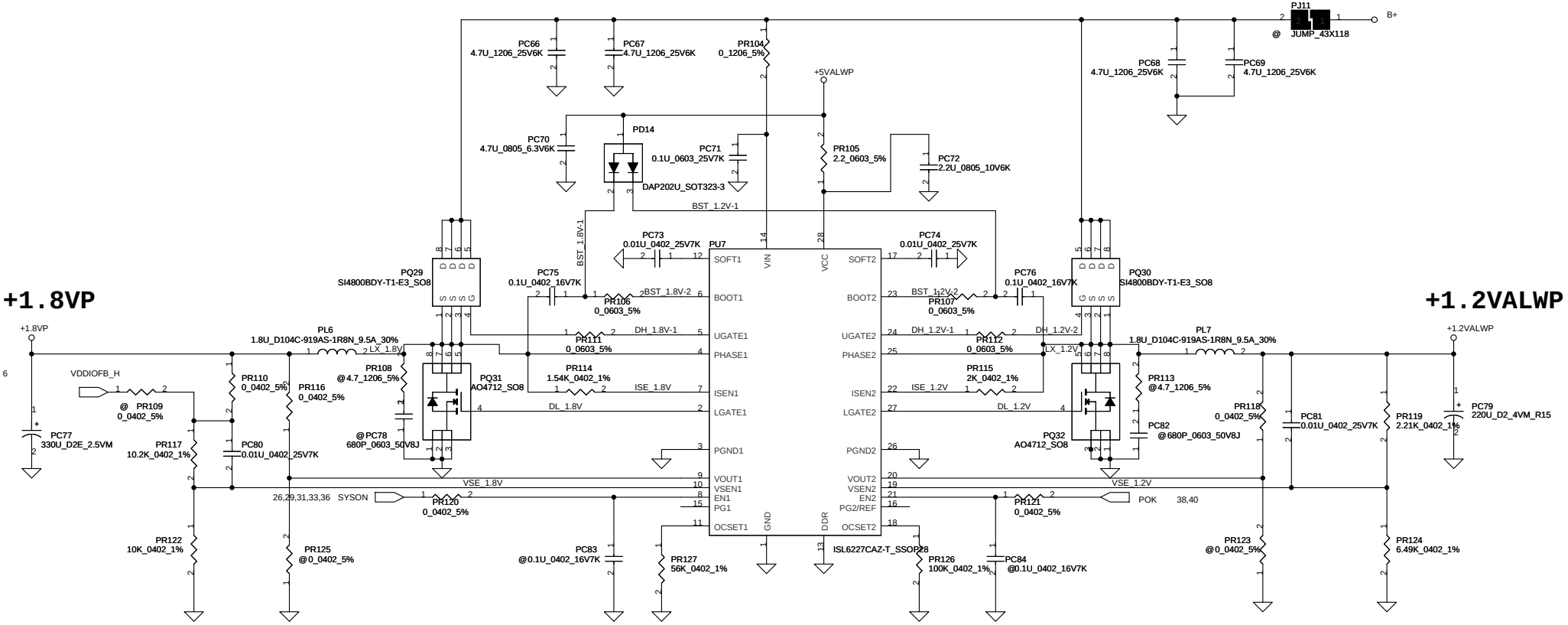

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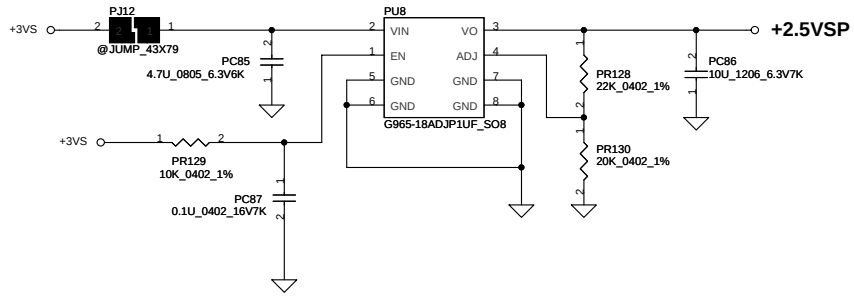

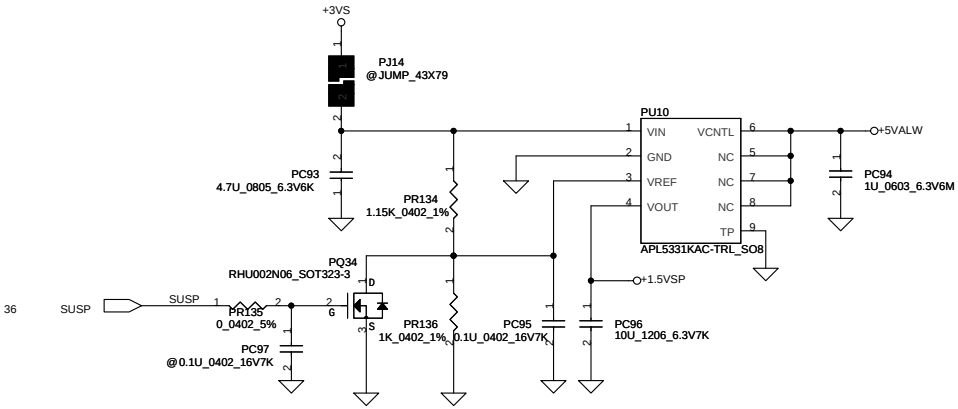

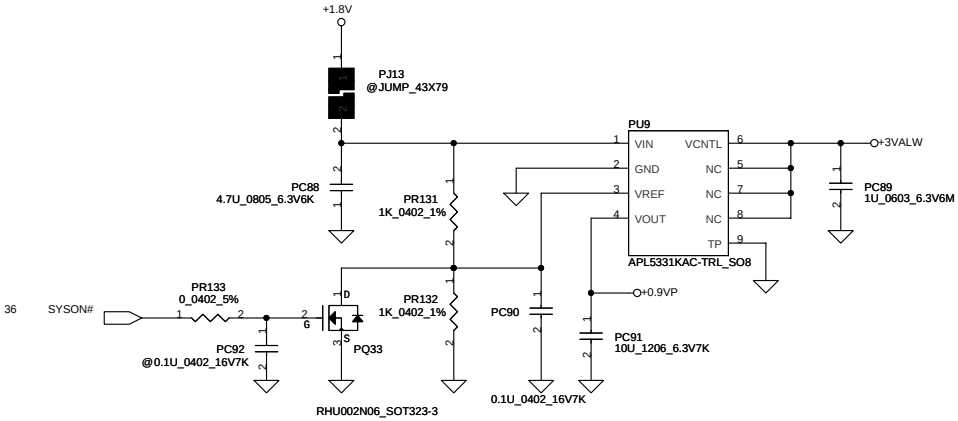

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Issued Date	2007/3/8	Deciphered Date	2008/3/8

Compal Electronics, Inc.

Title: **SCHEMATIC MB A3831**

Size	Document Number	Rev
Custom	401498	D

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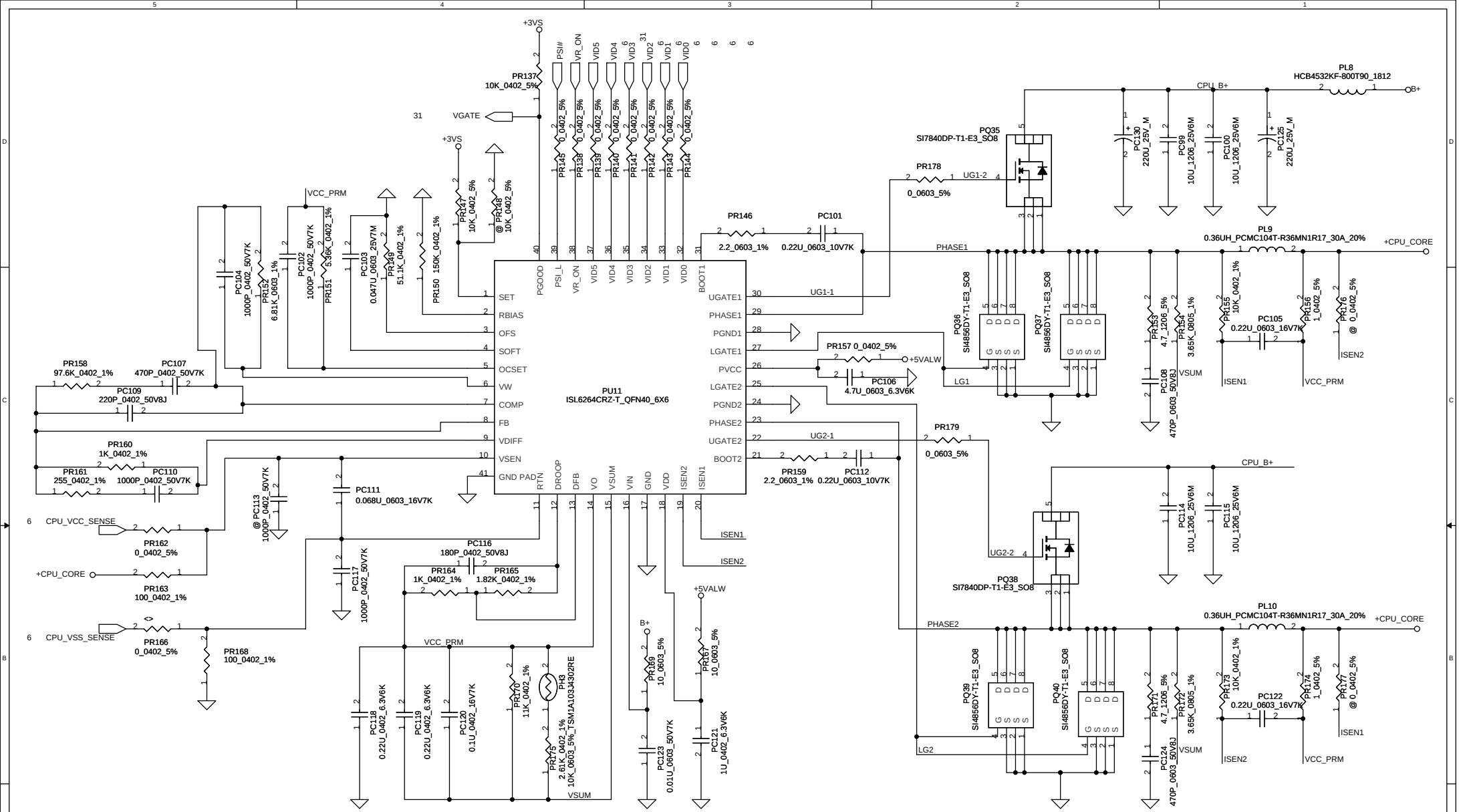

Security Classification	Compal Secret Data		
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POWER PIR LIST

	page	Reason for change	Modify list
EVT	43	design change	change PQ36,PQ37,PQ39,PQ40 from SI4856ADY(SB000001Y00) to SI4856DY(SB000003800).
DVT	43	offset	change PR149 to 51.1K
	43	ocp	change PR151 to 5.36K
	43	Vsense feedback	PR163 change to mount
	43	transient modification	PC120 change to 0.1uF
	43	EMI solution	PR153, PR171 change to 4.7Ohm. PC108, PC124 change to 470pF.
PVT	38	EMI solution	add PC126 2200P and PC127 820P
	39	EMI solution	add PC128 820P and PC129 0.022U
	38	OTP setting design change	change PR43 to 13.7K, PR44 to 13.7K
	41	OCP solution	change PR114 to 2.61K, change PQ27, PQ28, PQ31, PQ32 to AO4712
	40	HW design change	change PR89 to 10.2K
	43	noise solution	add PC130, 100U 25V
	39	component version change	change PU4 from ISL6251AHAZ-T to ISL6251AHAZ-TR5283
PreMP	41	OCP solution	change PR114 to 3K
	41	HW design change	change PR117 to 10.2K
	43	noise solution	change PC130 to 220U 25V
MP	41	1.8V shutdown solution	change PR114 to 1.54K, PR127 to 56K, PC77 to 330U(SGA19331D00)

HW4 Product Improvement Record (P.I.R.)

Phase: A to B — Date: 0601 — Writer: Timo Teng

Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
7	Add @	C576, C785	330U_D2_2.5VY_R9M	@330U_D2_2.5VY_R9M	After Power Jeff meausre CPU core ripple, we can unmount the 2 capacitors.		
14	Del @	CRT Pi-Filter circuit	R16, R20....and so on		Remove pi filter from CRT board from S/B to M/B for EMI solution		
	Add	CRT DDC circuit	D47, R1231 ...and so on.		Follow AMD PA		
15	Add	+HDMI_DDC_CLK, +5VS	NC	AT JP23.193, J23.182	Follow AMD PA		
17	Del @	C780, U40	@0.1u and @7408	0.1u and 7408	Add buffer avoid the leakage issue from LAN CHIP		
	Add @	R1221	0 ohm	@0 ohm			
22	Add	R1233, R1234, C788, C789	NC	10ohm and 1p	Add RC for reduce EMI noise		
31	Add	R1226	NC	10k	For CIR function.		
34	Change	KSO[0..15]	KSO[0..15]	KSO[0..17]	For Keyboard some keys function.		
36	Change	C180, C385, C87, C269 C638, C526	0.1uF 0402	0.1uF 0603	Change X7R		

Phase: B to C — Date: 0628 — Writer: Gino Lu

Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
14	Del	R1227, R1228	0_0402_5%	NC	AMD CRT level shift solution already be implement on VGA/B		
		R1229, R1230	19.2K_0402_5%	NC			
		D47	CH491D_SC59	NC			
	BOM Structure	Q4, Q5		UMA@			
		R1231, R1232	@	VGA@			
25	DEL	C727, C728	22U_A_4VM		Update RTL8101E/8102E/8111B/8111C co-layout circuit		
	Add	L78		4.7uH_1008HC			
	Net	C727, R293					

Phase: C to PreMP — Date: 0723 — Writer: Gino Lu

Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
27	Add	R486, R487		0_0603_5%	Reserve for +HVDD power select		
	Add	C790		10U_0805_10V4Z			
16	Add	C679, C688	12P_0402_50V8J	18P_0402_50V8J	For Real time clock adjust		
25	Change	C118,C120,C121,C135	0.01U_0402_25V4Z	0.1U_0402_16V4Z	for Gigalan EMI solution		
25	BOM structure change	C728	CAM@	D_CAM@	For Camera reserve		
		C558		BT@	For Bluetooth select		

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45@ Part

PJP1
45@ DC-IN JACK

PCB

ZZZ
[illegible]/BDA800009C00

CHIPSET

U5
UMAR3@ RS690MC

U5
UMAR1@ RS690MC

U5
VGAR1@ RS690MC

U26
SB600R1@ 218S6ECLA13FG_FCBGA548_SB600

LAN

8101E C: Modify BOM

U4
8101E@ RTL8101E

C473
8101E@ 1000P_0402_25V8J

R293
8101E@ 0_0603_5%

C429
8101E@ 0.1U_0402_16V4Z

C464
8101E@ 22U_A_4VM

C438
8101E@ 1000P_0402_50V7K

R480
8101E@ 0_0603_5%

8111C

U4
8111C@ RTL8111C SA00001WM00

R293
8111C@ MBC1608121YZF_0603

C482
8111C@ 22U_A_4VM

8102E

U4
8102E@ RTL8102E

L48
8102E@ 0_0603_5%

C482
8102E@ 22U_A_4VM

C473
8102E@ 1000P_0402_50V7K

L46
8102E@ 0_0603_5%

C464
8102E@ 22U_A_4VM

C444
8102E@ 22U_A_4VM

TRANSFORMER

U23
100M@ TST1284

C135
100M@ 0.01U_0402_25V4Z

C120
100M@ 0.01U_0402_25V4Z

C118
100M@ 0.01U_0402_25V4Z

C121
100M@ 0.01U_0402_25V4Z

PreMP:Change C118,C120,C121,C135 for EMI solution

Card BUS

U11
8402@ PCI8402

M76 CRT

L6
76@ FBMA-11-100505-900T

L3
76@ FBMA-11-100505-900T

L4
76@ FBMA-11-100505-900T

PreMP: Add BOM sturcture for EMI issue

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