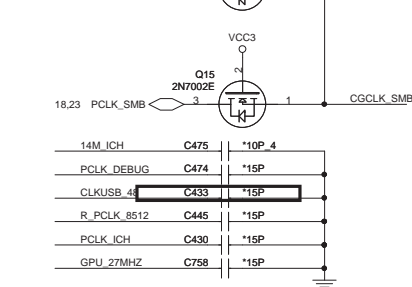
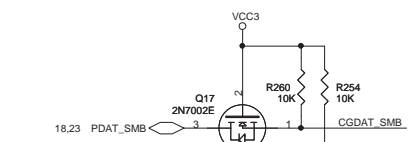
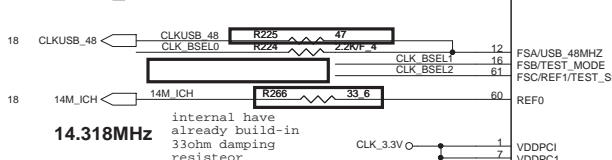
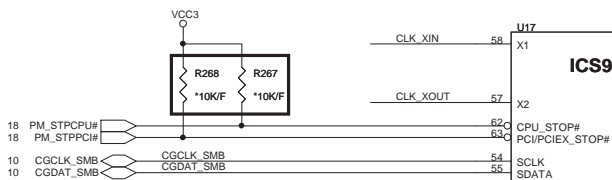
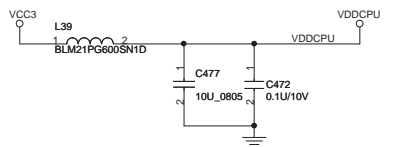
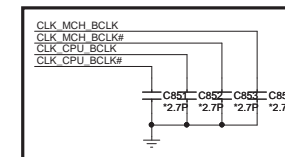
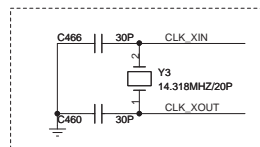
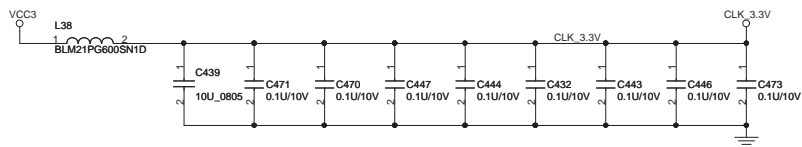
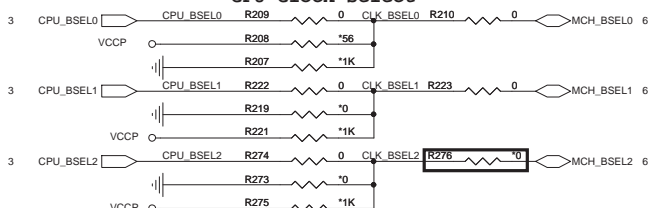


QUANTA COMPUTER

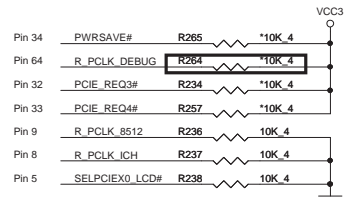
Size	Document Number	Rev
	PB3 Main Board	1A
Date:	Wednesday, October 03, 2007	Sheet 1 of 35



CPU Clock select



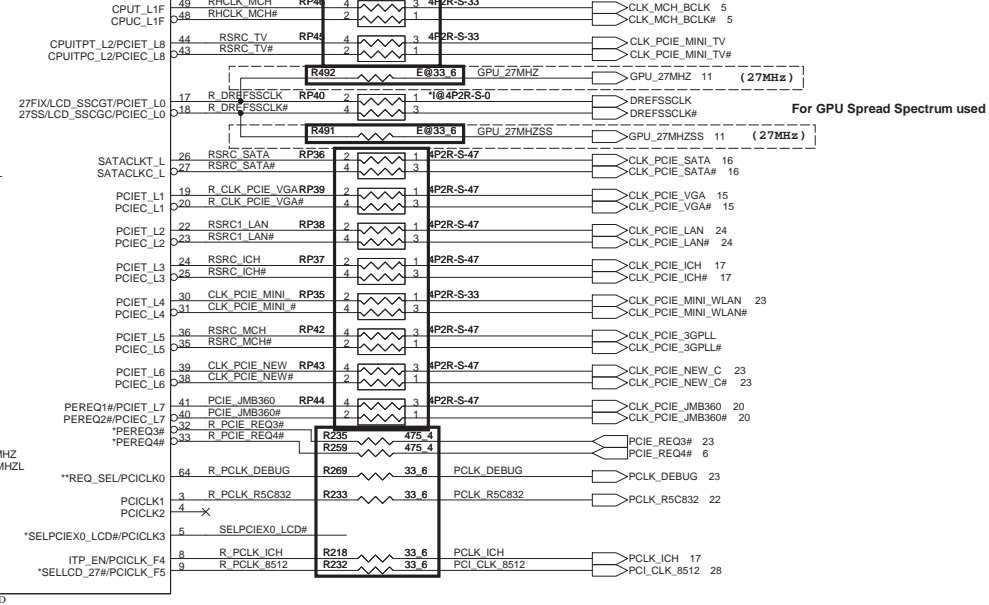
FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down



ITP_EN (PIN8)			
LOW : PIN43/44 SRC			
HIGH : PIN43,44 CPUITP			
PCIE_REQ1#	PCIE_L0	PCIE_L6	
PCIE_REQ2#	PCIE_L1	PCIE_L8	
PCIE_REQ3#	PCIE_L2	PCIE_L4	
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7

PIN 64 : High for REQ_SEL
Low for PCICLK output

ICS9PR363BGLF



VREF

Keep Rpull-up=1K ohm and variable Rpull-down to measure CPU and PCIe Vtop

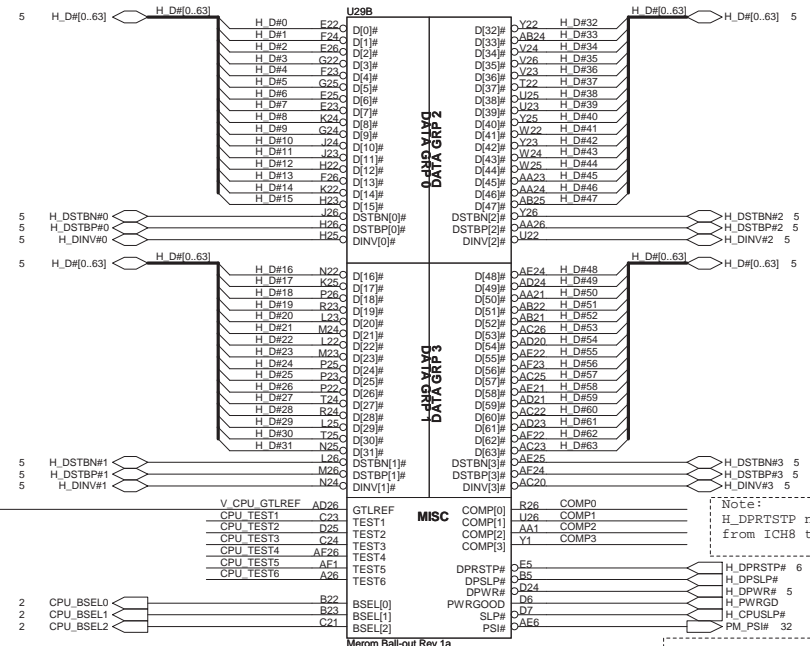
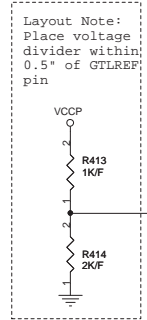
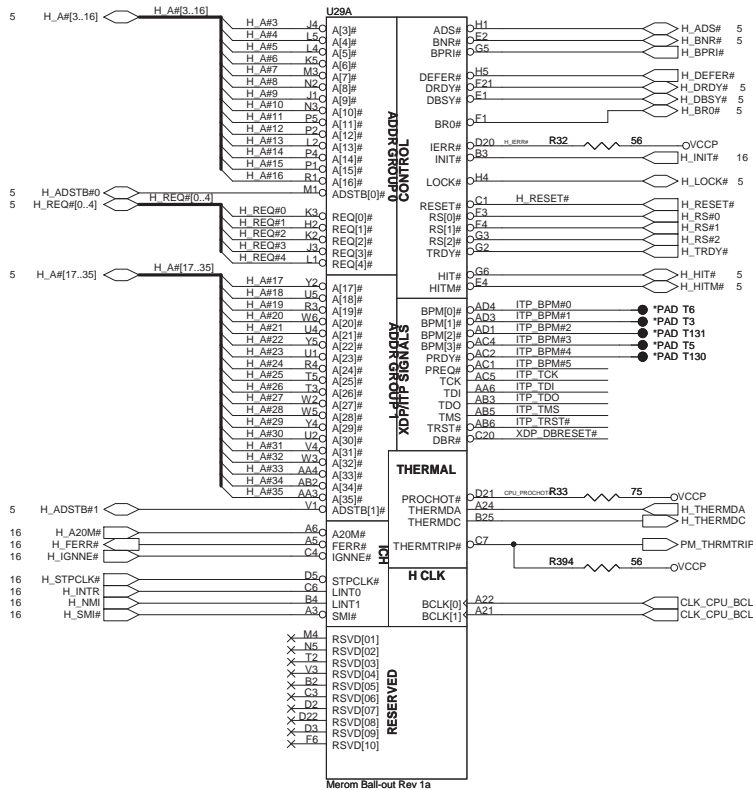
Rpull-up R703	Rpull-down R704	CPU-T Vtop (mV)	PCIEX-T Vtop (mV)
1K	203	836	933
1K	222	799	906
1K	236	774	868
1K	275	721	834
1K	298	688	797
1K	329	664	778
1K	362	615	720
1K	372	595	706
1K	380	566	671
1K	385	513	634

PIN 5 R717	PIN 9 R715	PIN 14/15
LO (10K)	LO (10K)	PCIEX9
	HI (NC)	DOT96
HI (NC)	LO (10K)	PCIEX9
	HI (NC)	DOT96

QUANTA COMPUTER

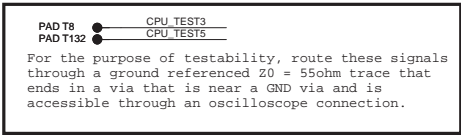
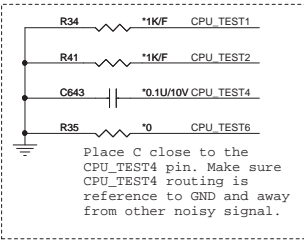
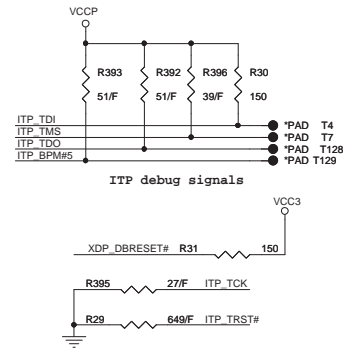
Size	Document Number	Rev
	Clock Generator	1A
Date:	Wednesday, October 03, 2007	Sheet 2 of 35

CPU-Host Bus

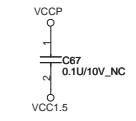


Note:
H_DPRTSTP need to daisy chain from ICH8 to IMPV6 to CPU.

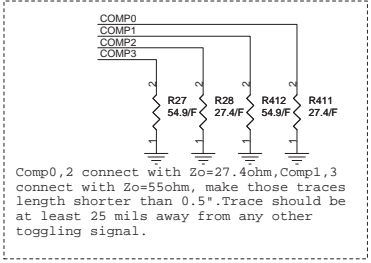
Populate ITP700Flex for bringup
Layout Note:
Place R4,R361,R346 & R7 close to CPU.



Reserved for EMI.



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



ITP disable guidelines

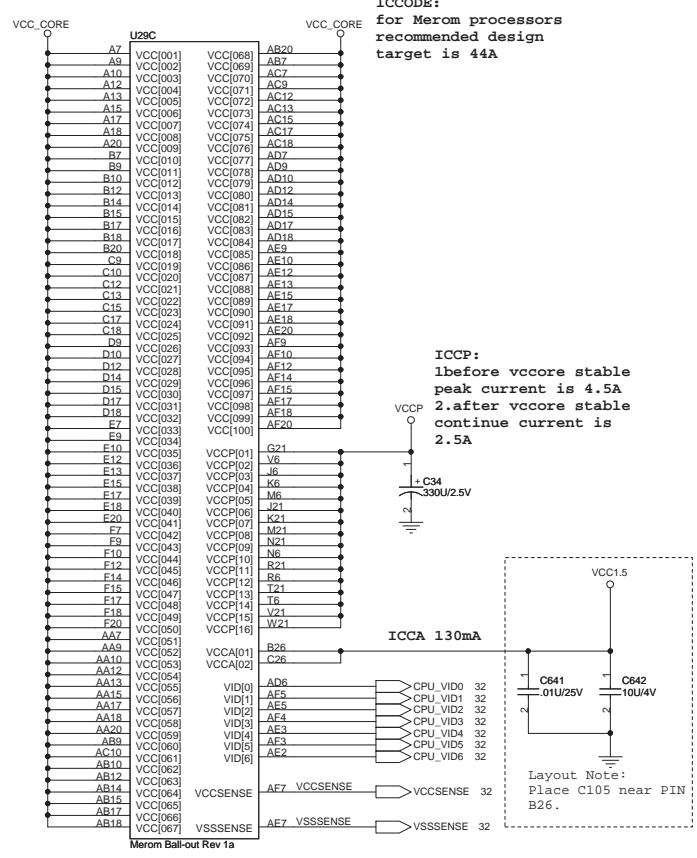
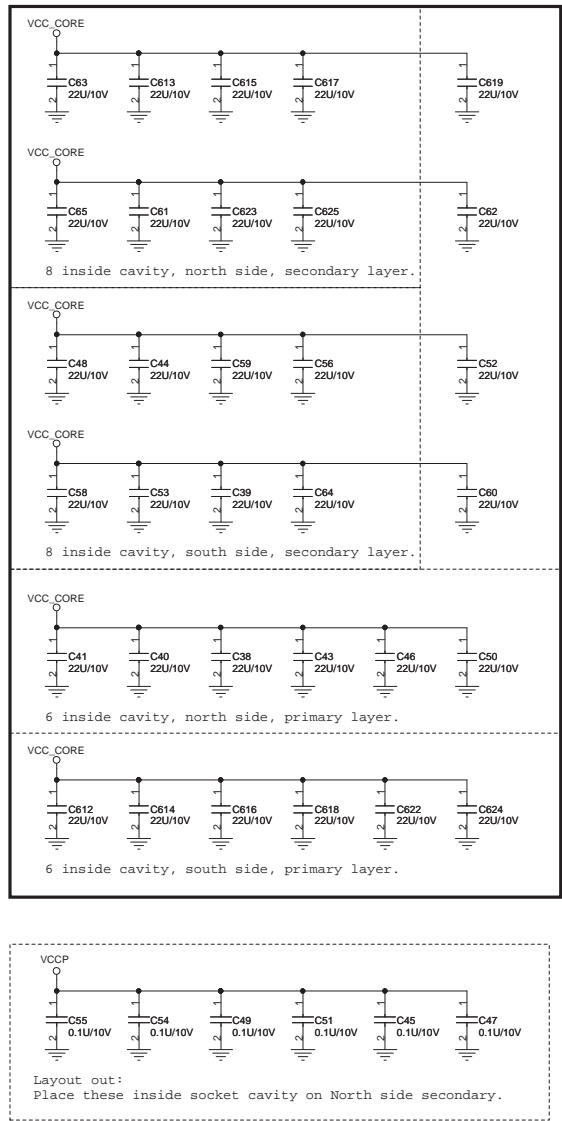
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

QUANTA COMPUTER

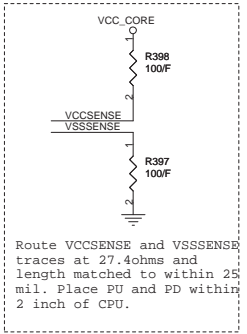
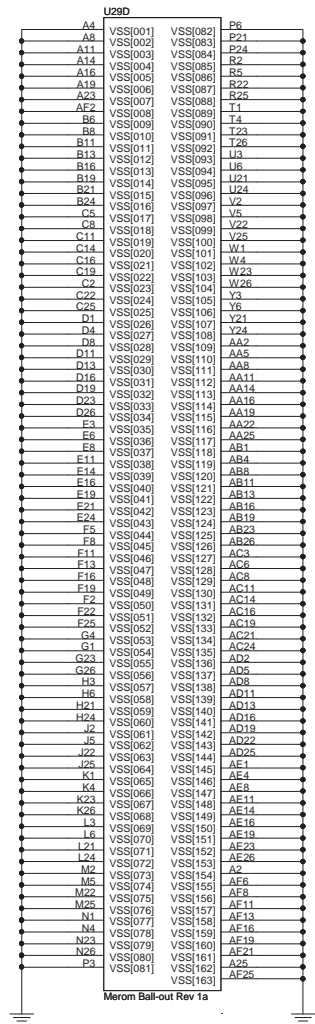
Size	Document Number	Rev
	CPU-Host Bus	1A
Date:	Wednesday, October 03, 2007	Sheet 3 of 35

CPU Power & GND



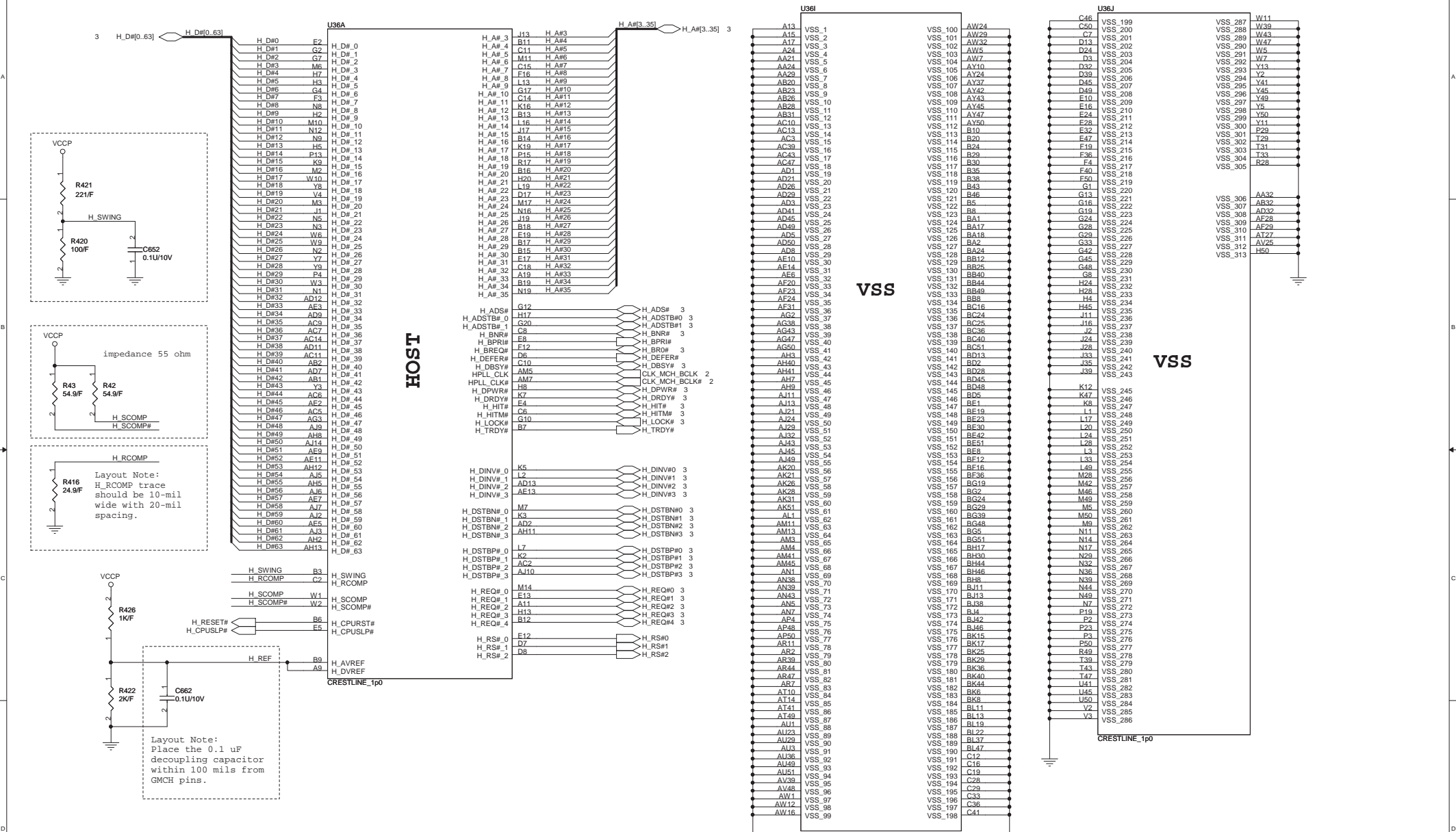
ICCODE:
for Merom processors
recommended design
target is 44A

ICCP:
1.before vccore stable
peak current is 4.5A
2.after vccore stable
continue current is
2.5A



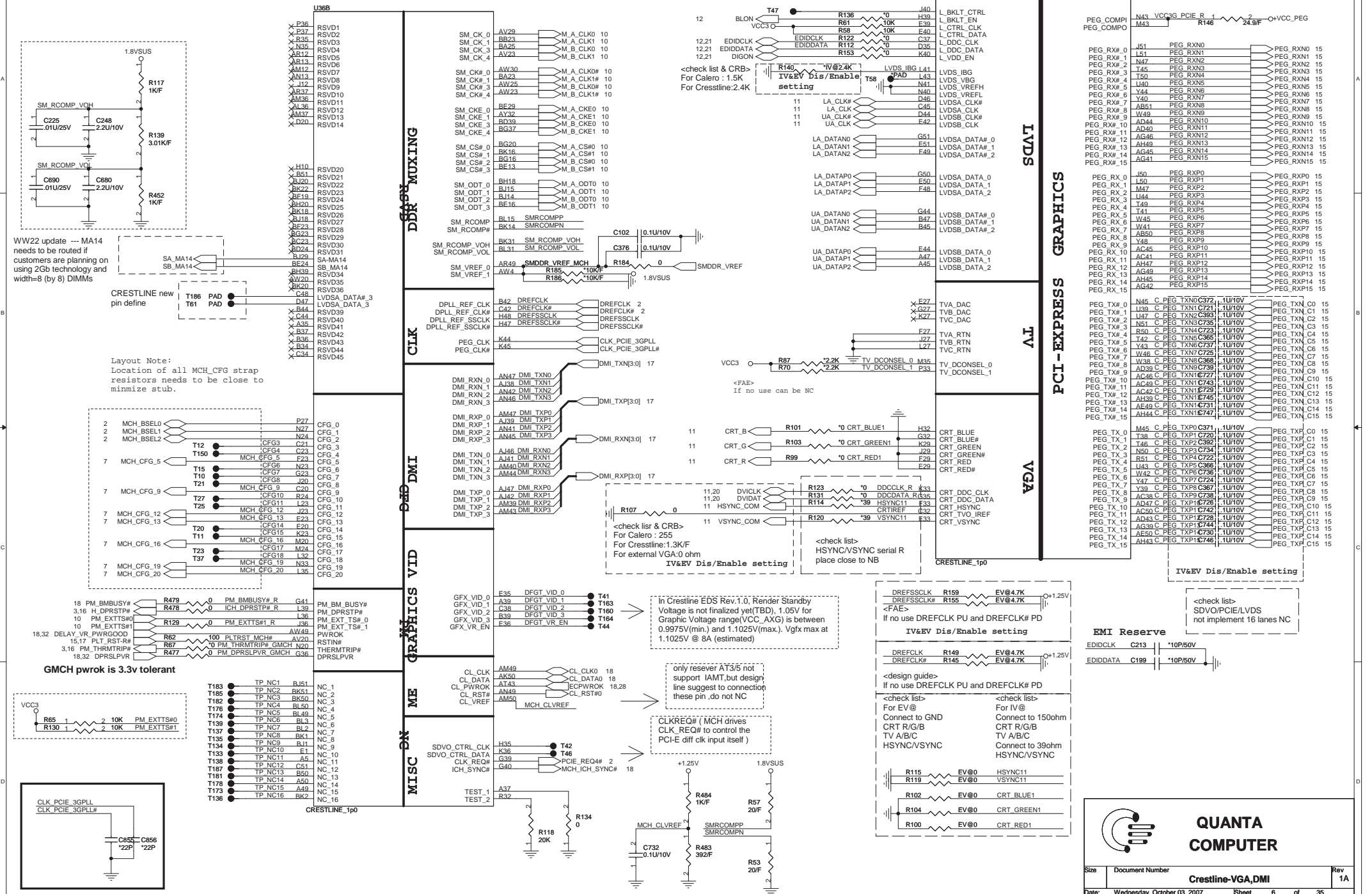
**QUANTA
COMPUTER**

Size	Document Number	Rev
	CPU-Power/NC	1A
Date:	Wednesday, October 03, 2007	Sheet 4 of 35



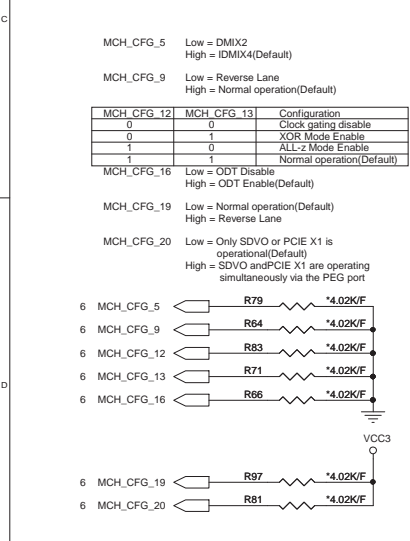
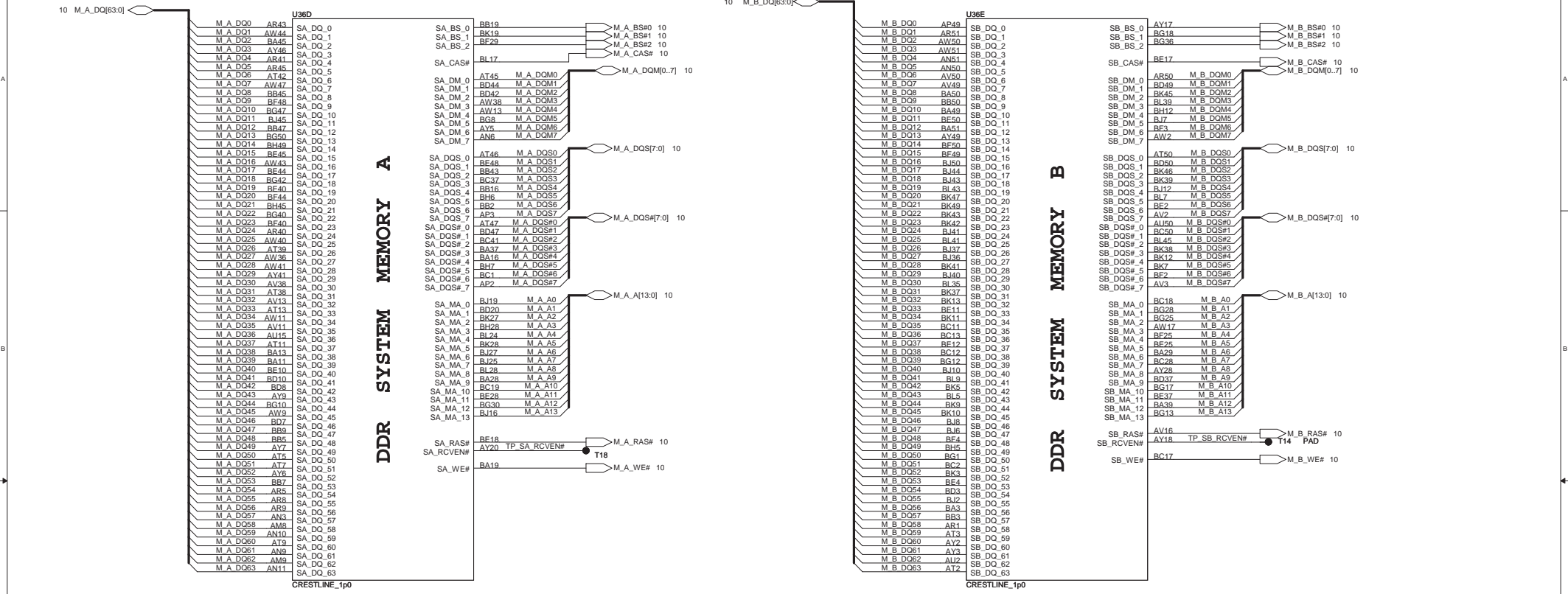
**QUANTA
COMPUTER**

Size	Document Number	Rev
		1A
Date:	Wednesday, October 03, 2007	Sheet 5 of 35




QUANTA COMPUTER

Size Document Number
 Crestline-VGA,DMI
 Date: Wednesday, October 03, 2007 Sheet 6 of 35 Rev 1A



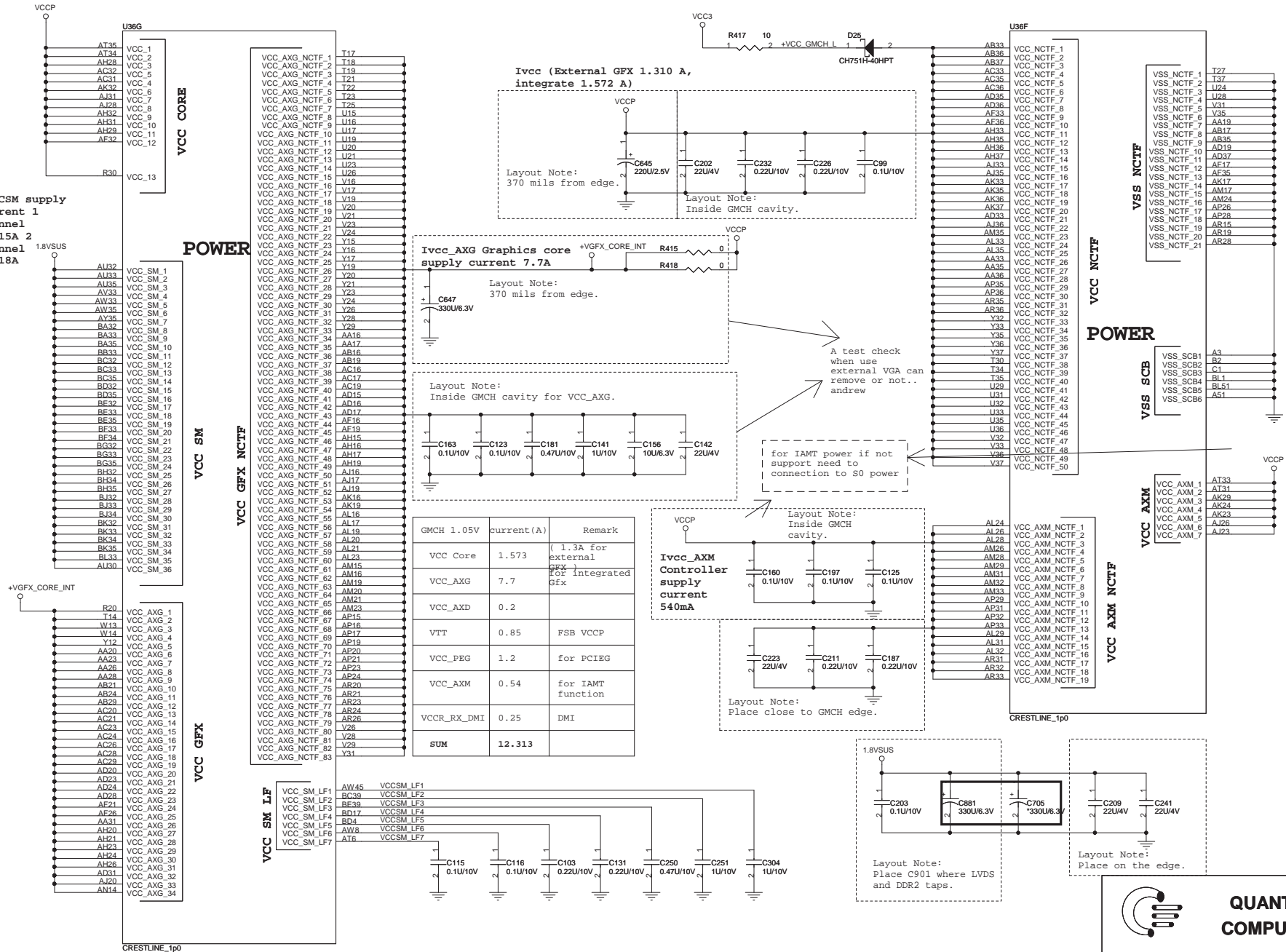
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIe x1 is operation(Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
 CFG[17:3] Have internal Pull-up
 CFG[18:19] Have internal Pull-down
 Any CFG signal strapping option not list below should be left NC Pin



**QUANTA
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Size	Document Number	Rev
	Crestline-DDR II	1A
Date: Wednesday, October 03, 2007 Sheet 7 of 35		



A test check when use external VGA can remove or not.. andrew

for IAMT power if not support need to connection to S0 power

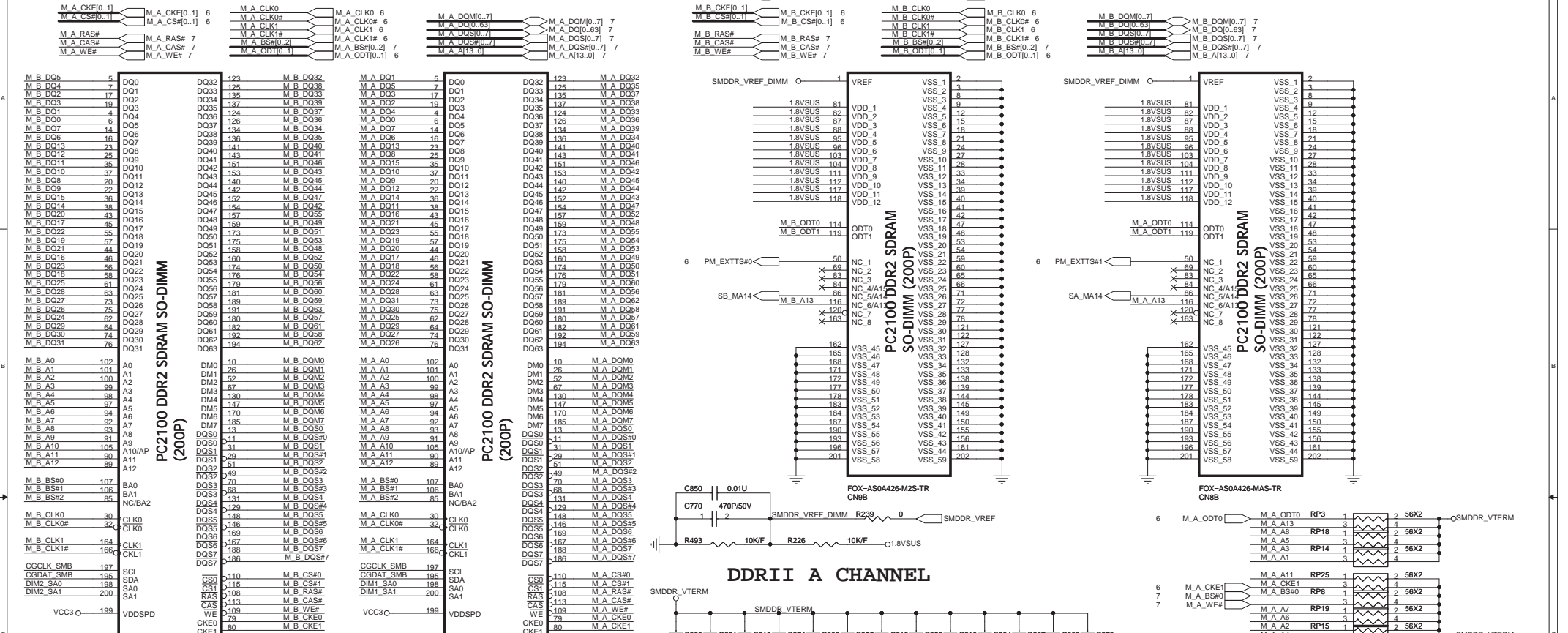
**QUANTA
COMPUTER**

Size: Document Number: Crestline-VCC,NCTF Rev 1A
Date: Wednesday, October 03, 2007 Sheet 8 of 35

DDRII-SO DIMM

<http://hobi-elektronika.net>

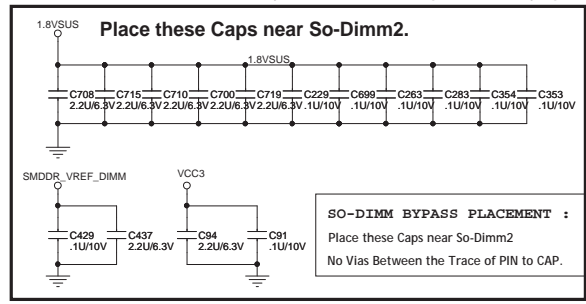
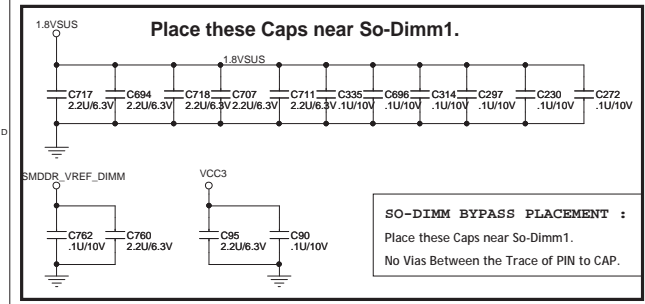
10



DDRII A CHANNEL

DDRII B CHANNEL

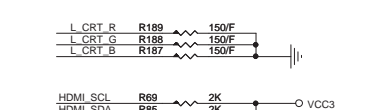
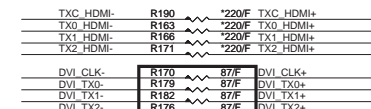
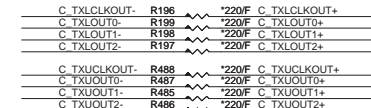
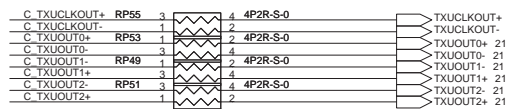
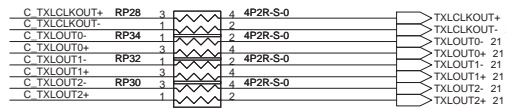
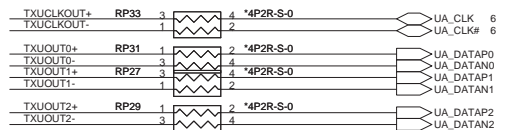
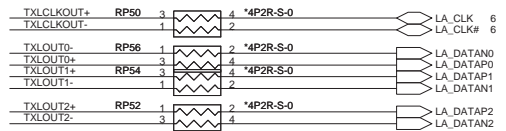
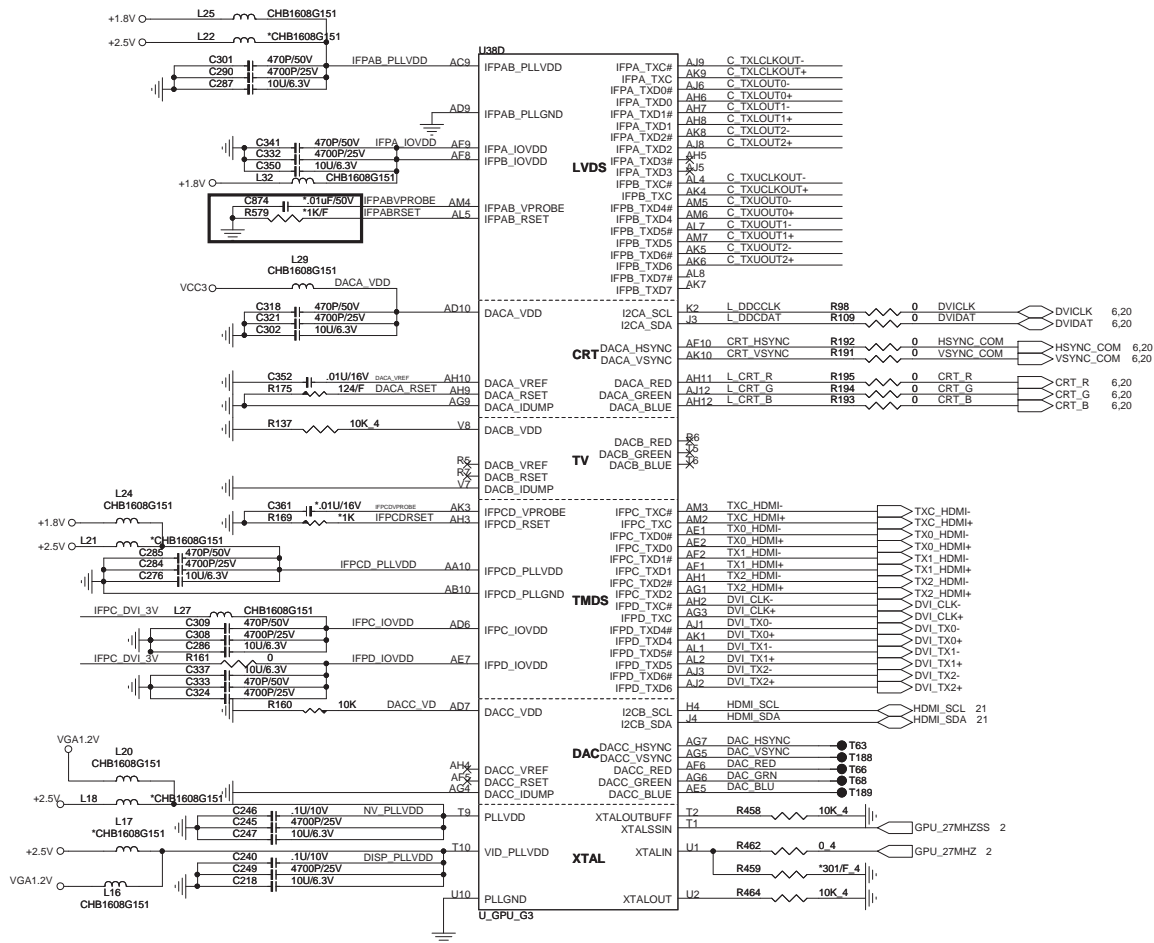
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



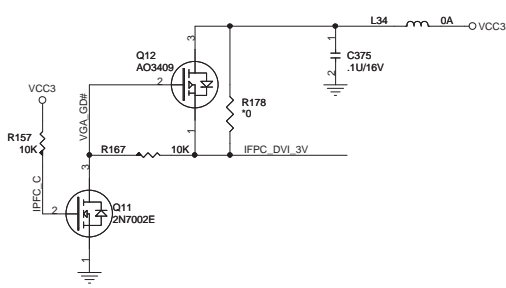
QUANTA COMPUTER

Size: Document Number: **DDRII SO-DIMM** Rev 1A

Date: Wednesday, October 03, 2007 Sheet 10 of 35

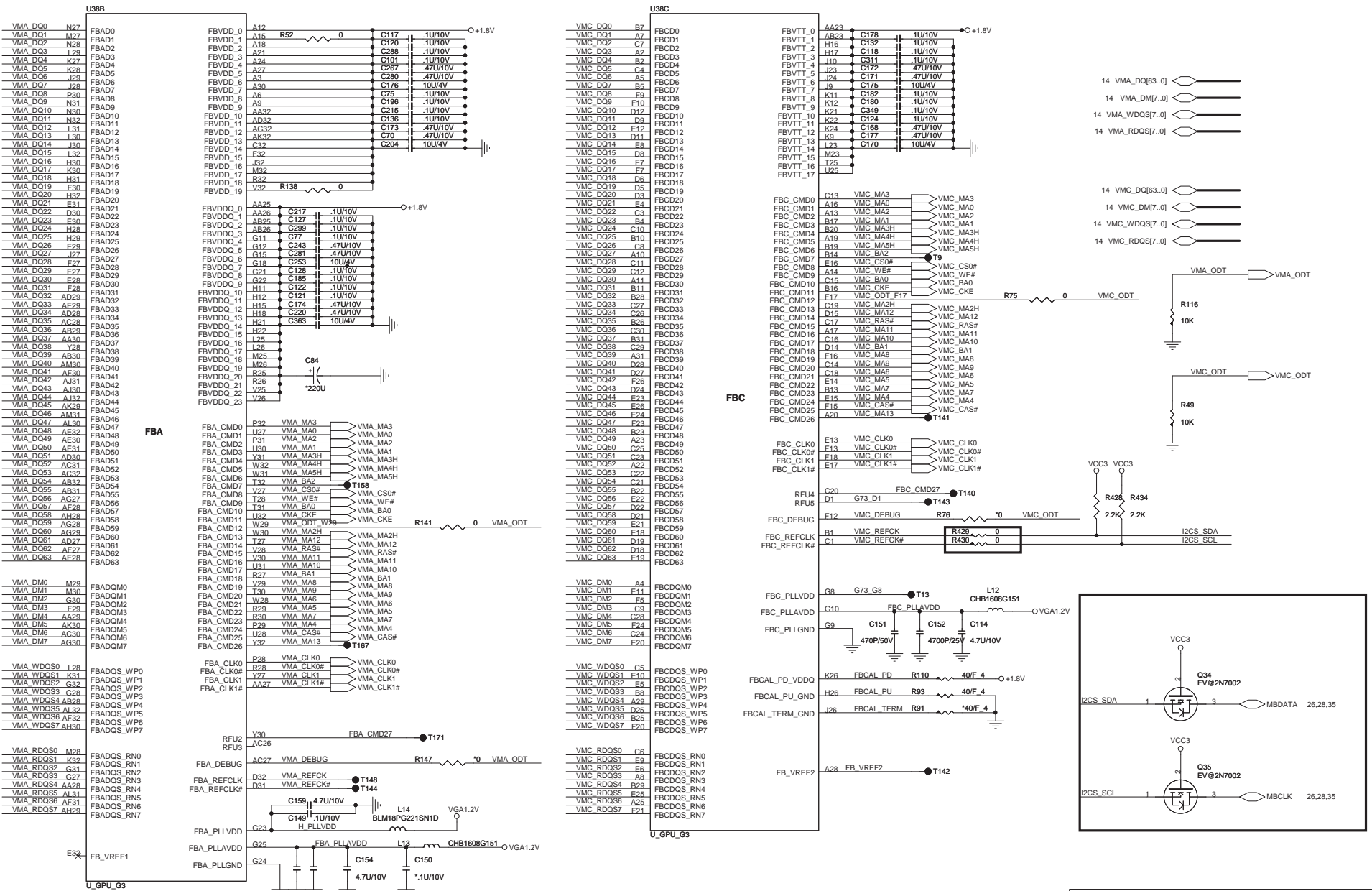


HDMI I2C pull-high to 5V



**QUANTA
COMPUTER**

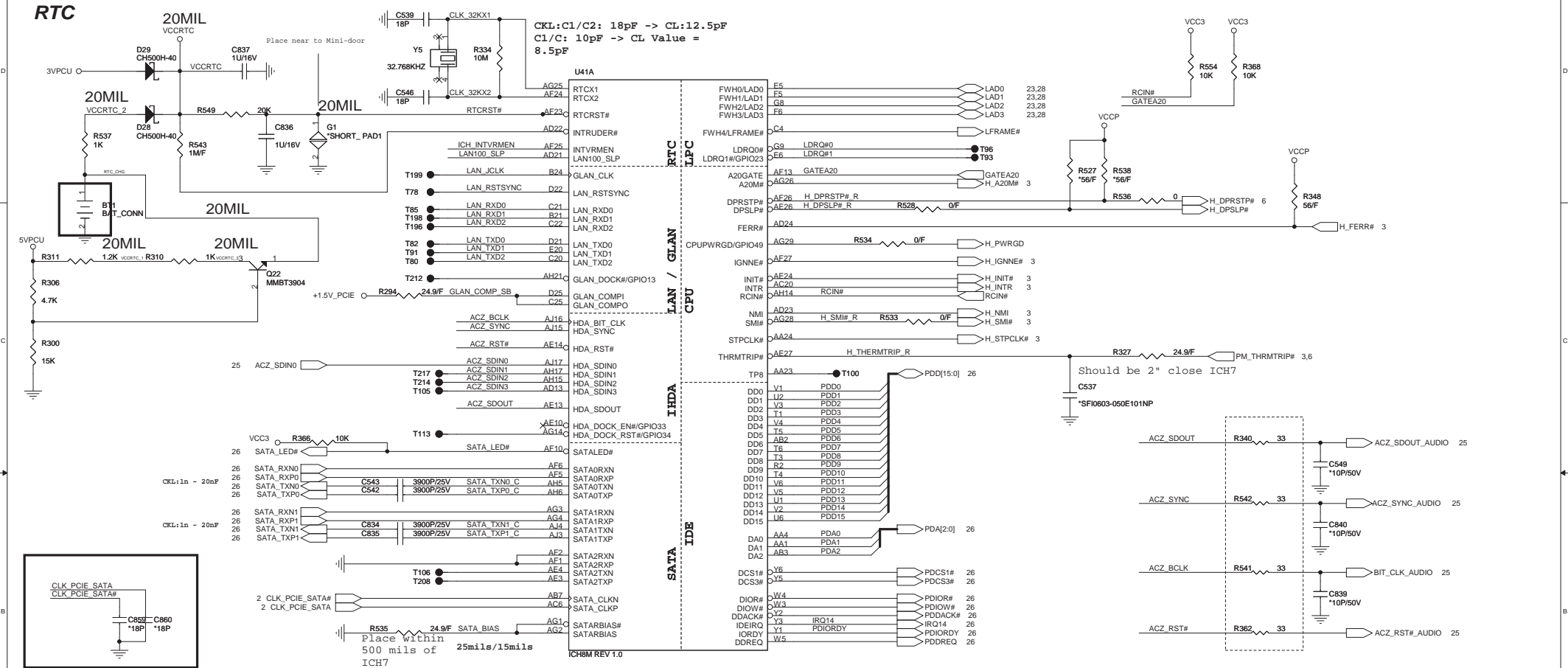
Size	Document Number	Rev
	NVG73M-LVDS,DVI,CRT,TV	1A
Date: Wednesday, October 03, 2007 Sheet 11 of 35		



QUANTA COMPUTER

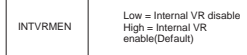
Size: Document Number: **NVG73M Memory I/F** Rev 1A

Date: Wednesday, October 03, 2007 Sheet 13 of 35

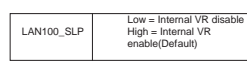


SB Strap

ICH8-M Internal VR Enable strap
 (Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

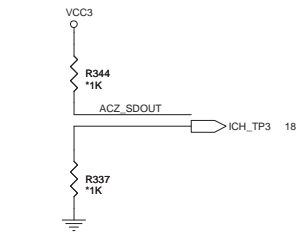


ICH8-M LAN100_SLP Strap
 (Internal VR for VccLAN1_05 and VccCL1_05)



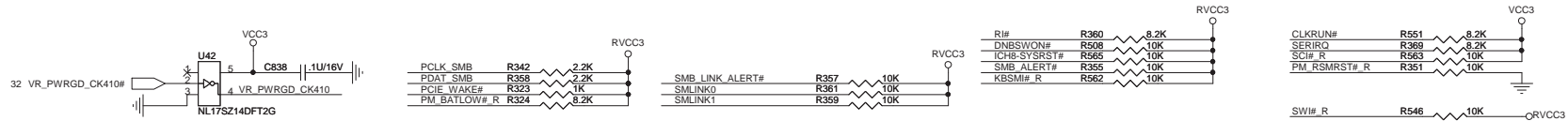
XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

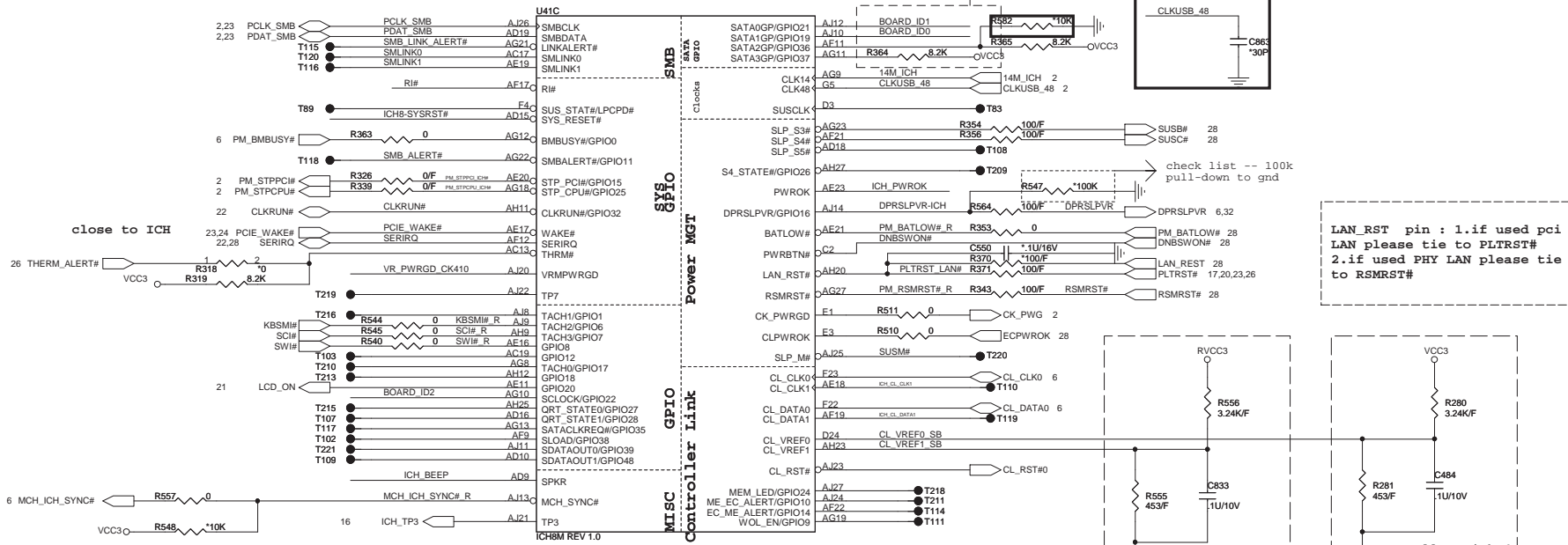


QUANTA COMPUTER

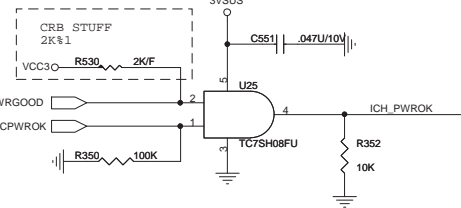
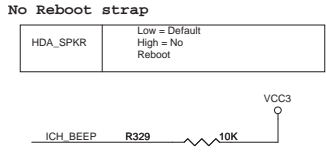
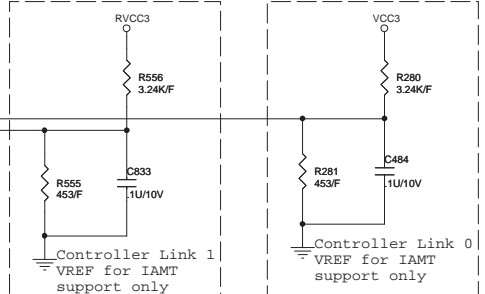
Size	Document Number	Rev
	ICH8-M Host	1A
Date:	Wednesday, October 03, 2007	Sheet 16 of 35



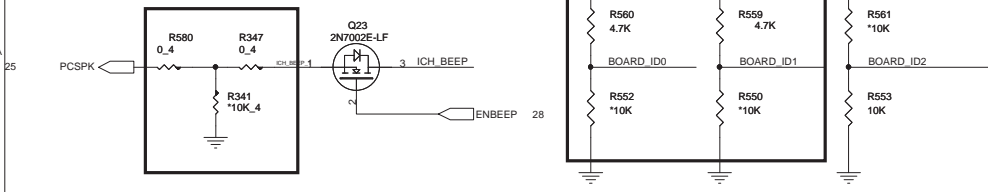
these pin if unused require 8.2k to 10k pull-up to +3v




LAN_RST pin : 1.if used pci LAN please tie to PLTRST#
2.if used PHY LAN please tie to RSMRST#



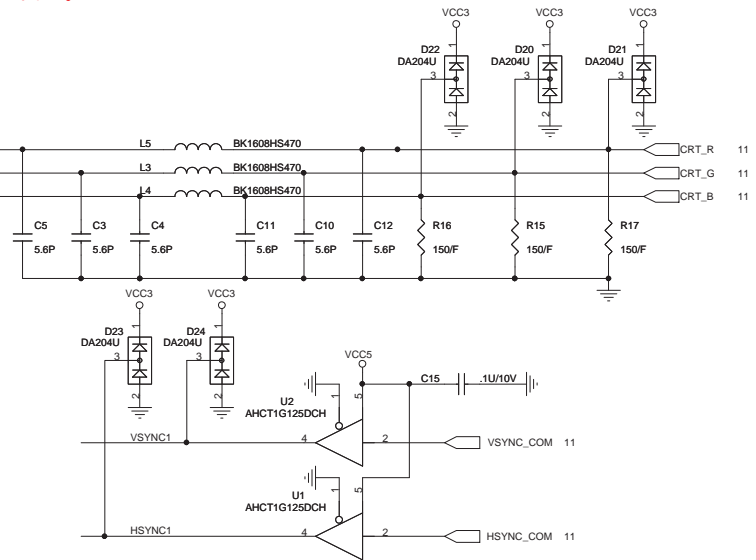
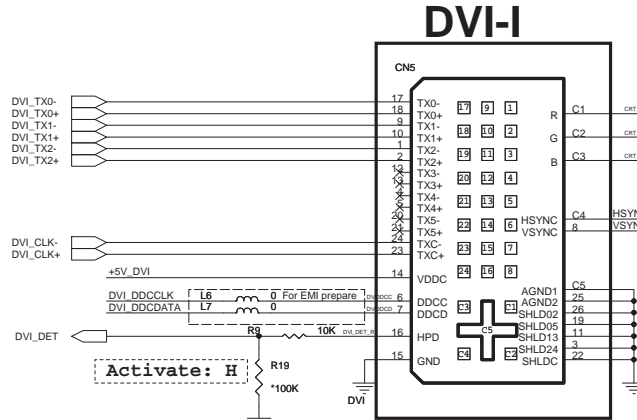
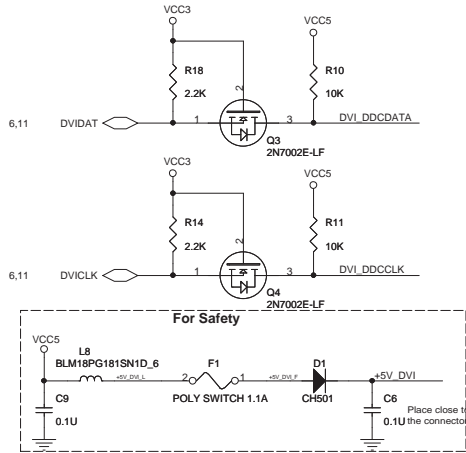
Board ID	940 GML (0:0)	945GM (0:1)	PM+G72 (1:0)	PM+G73 (1:1)
ID0	R658 Stuff	R658 Stuff	R655 Stuff	R655 Stuff
ID1	R668 Stuff	R669 Stuff	R668 Stuff	R669 Stuff



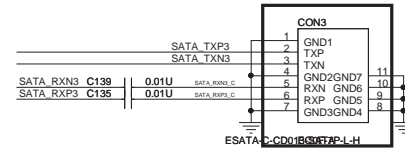
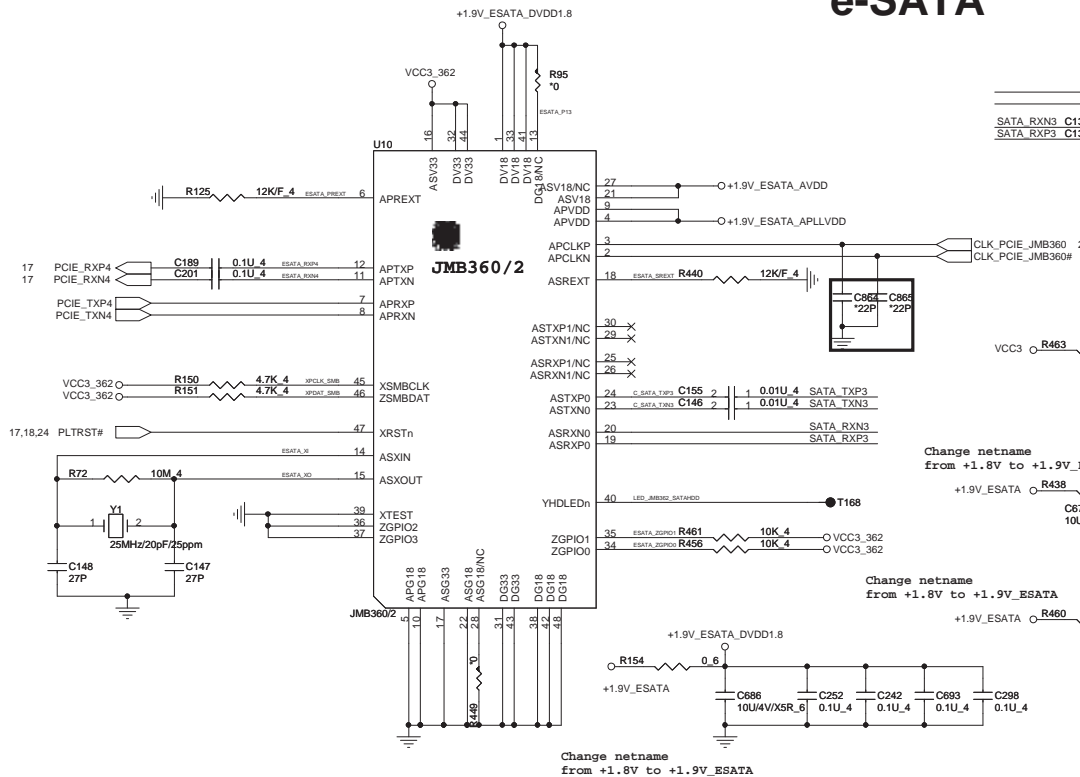


**QUANTA
COMPUTER**

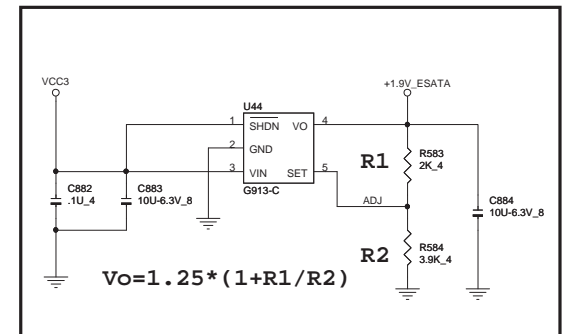
Size	Document Number	Rev
	ICH8-M GPIO, SM Bus, PMU	1A
Date: Wednesday, October 03, 2007 Sheet 18 of 35		



e-SATA



For E version change

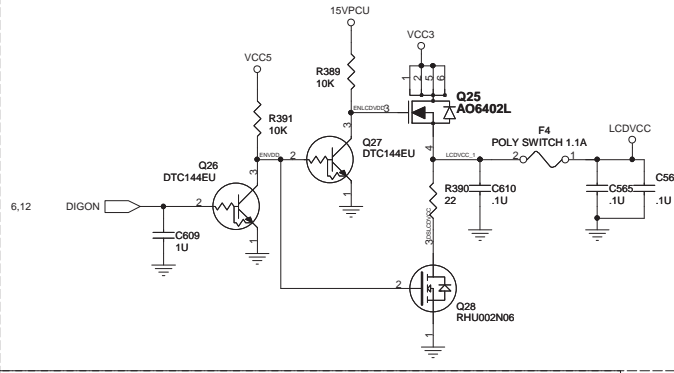


$$V_o = 1.25 * (1 + R1/R2)$$

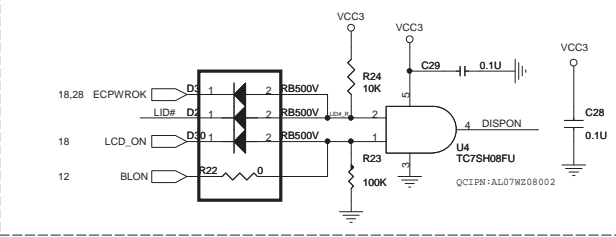
QUANTA COMPUTER

Size	Document Number	Rev
	DVI, eSATA	1A
Date:	Friday, October 05, 2007	Sheet 20 of 35

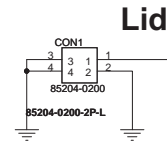
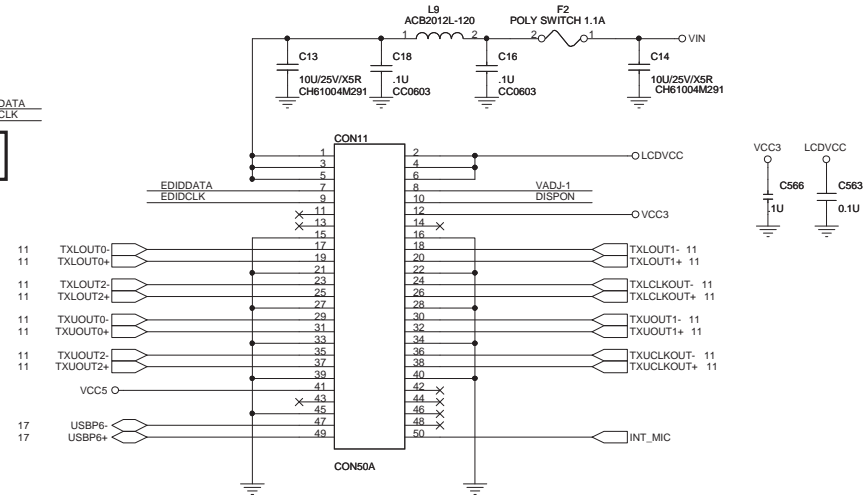
Panel VCC Control



Backlight Control

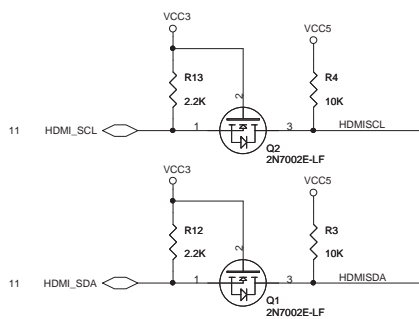


LCD Connector

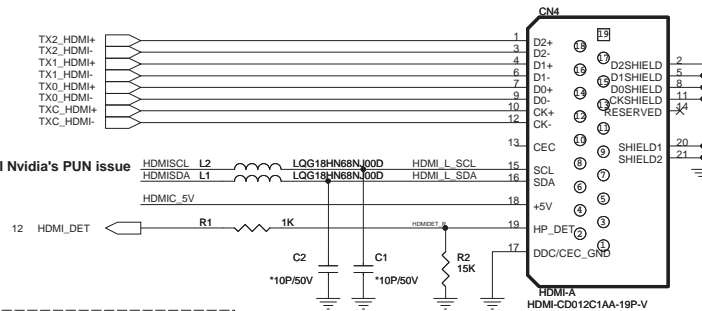


HDMI

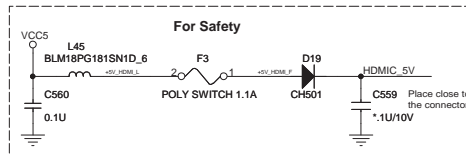
HDMI I2C pull-high to 5V



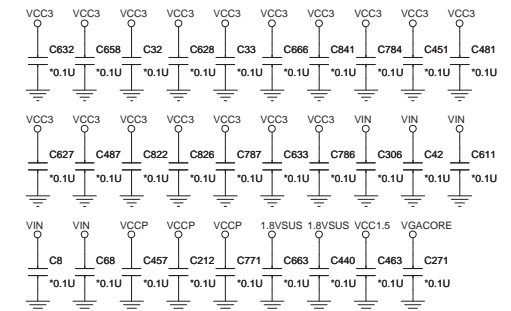
For HDMI Nvidia's PUN issue




For Safety



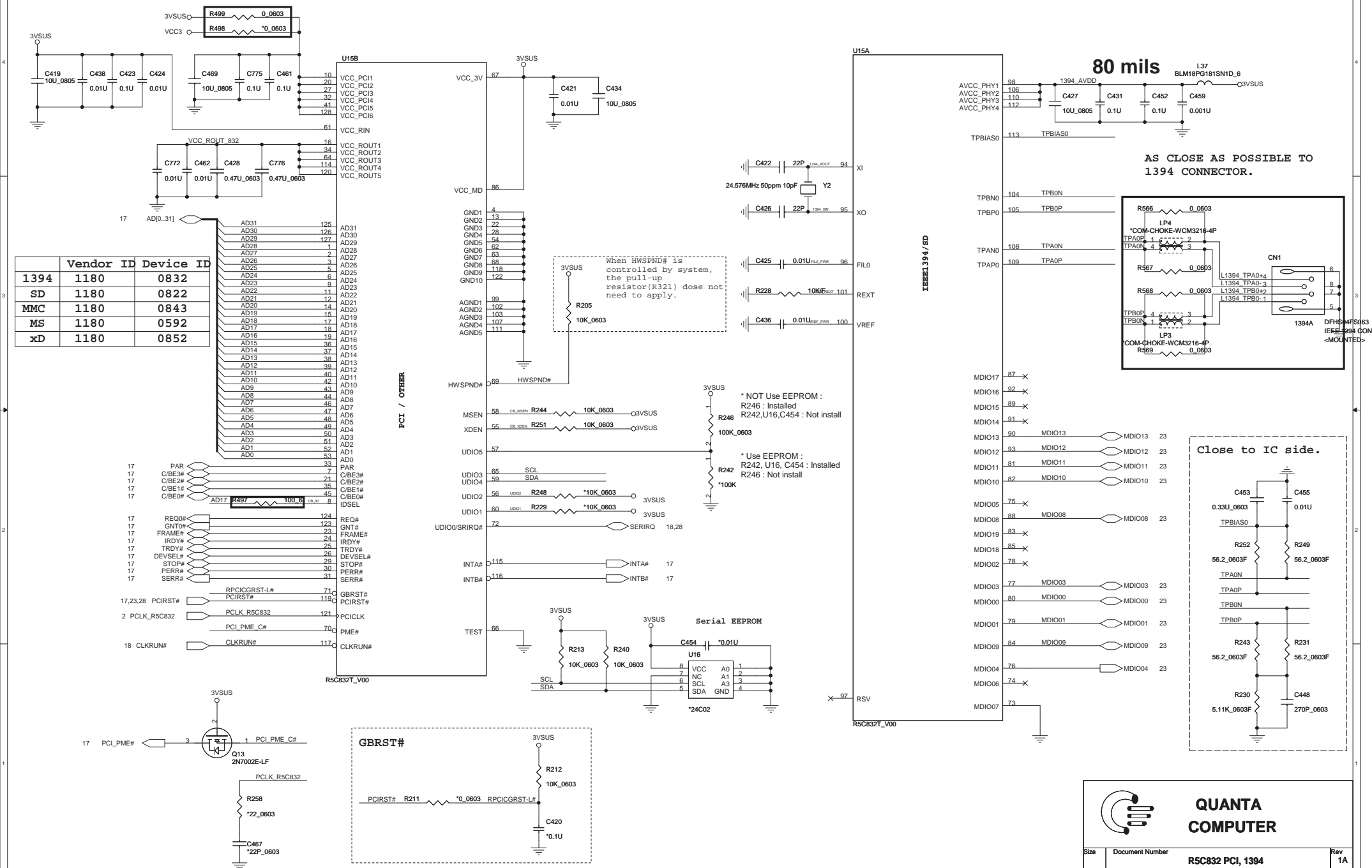
EMI Reserve





**QUANTA
COMPUTER**

Size	Document Number	LCD, HDMI	Rev
			1A
Date: Wednesday, October 03, 2007		Sheet	21 of 35



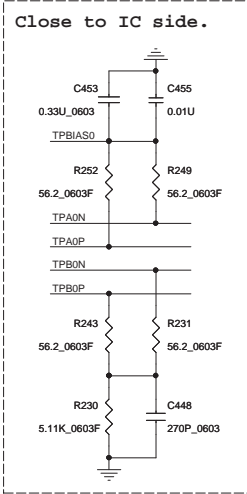
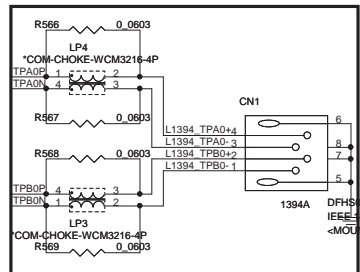
	Vendor ID	Device ID
1394	1180	0832
SD	1180	0822
MMC	1180	0843
MS	1180	0592
xD	1180	0852


Pin	Signal	Pin	Signal
AD31	125	AD31	125
AD30	126	AD30	126
AD29	127	AD29	127
AD28	128	AD28	128
AD27	2	AD27	2
AD26	3	AD26	3
AD25	4	AD25	4
AD24	5	AD24	5
AD23	6	AD23	6
AD22	7	AD22	7
AD21	8	AD21	8
AD20	9	AD20	9
AD19	10	AD19	10
AD18	11	AD18	11
AD17	12	AD17	12
AD16	13	AD16	13
AD15	14	AD15	14
AD14	15	AD14	15
AD13	16	AD13	16
AD12	17	AD12	17
AD11	18	AD11	18
AD10	19	AD10	19
AD9	20	AD9	20
AD8	21	AD8	21
AD7	22	AD7	22
AD6	23	AD6	23
AD5	24	AD5	24
AD4	25	AD4	25
AD3	26	AD3	26
AD2	27	AD2	27
AD1	28	AD1	28
AD0	29	AD0	29
PAR	30	PAR	30
C/BE3#	31	C/BE3#	31
C/BE2#	32	C/BE2#	32
C/BE1#	33	C/BE1#	33
C/BE0#	34	C/BE0#	34
AD17	35	AD17	35
IDSEL	36	IDSEL	36
REQ0#	37	REQ0#	37
GNT0#	38	GNT0#	38
FRAME#	39	FRAME#	39
IRDY#	40	IRDY#	40
TRDY#	41	TRDY#	41
DEVSEL#	42	DEVSEL#	42
STOP#	43	STOP#	43
PERR#	44	PERR#	44
SERR#	45	SERR#	45
RPCICGRST-L#	46	RPCICGRST-L#	46
PCIRST#	47	PCIRST#	47
PCLK_R5C832	48	PCLK_R5C832	48
PCI_PME_C#	49	PCI_PME_C#	49
CLKRUN#	50	CLKRUN#	50

When HWSPND# is controlled by system, the pull-up resistor (R205) dose not need to apply.

* NOT Use EEPROM :
R246 : installed
R242, U16, C454 : Not install

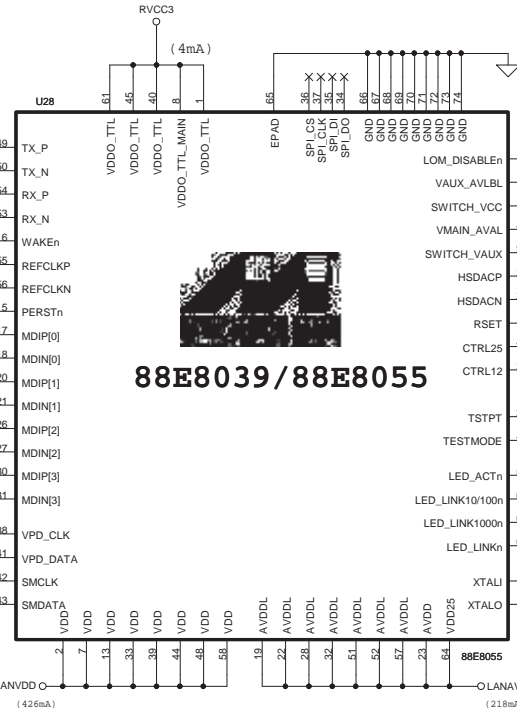
* Use EEPROM :
R242, U16, C454 : installed
R246 : Not install





**QUANTA
COMPUTER**

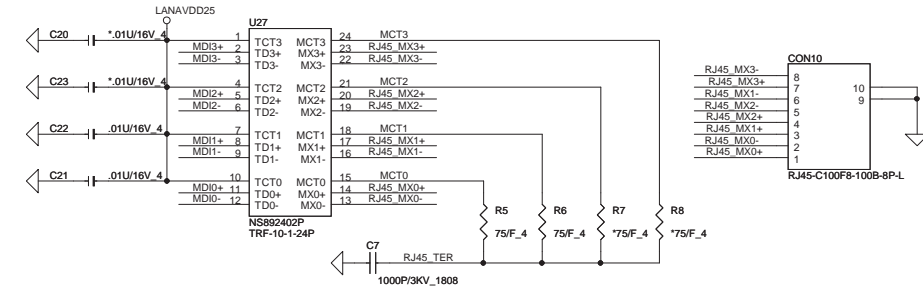
Size	Document Number	Rev
	R5C832 PCI, 1394	1A
Date: Wednesday, October 03, 2007 Sheet 22 of 35		



88E8039/88E8055

Giga: P/N: AJ080550002
10/100M: P/N: AJ080390005

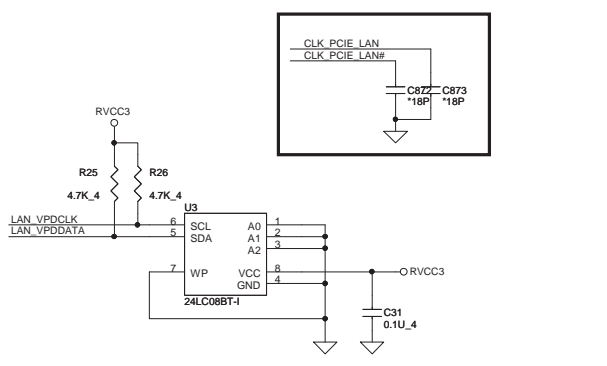
FCE P/N: BG625000C03
P/N: BG625000486



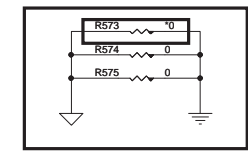
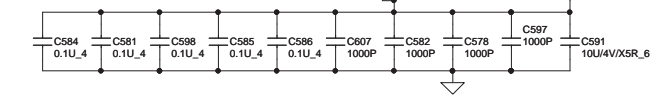
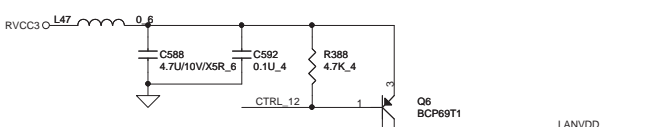
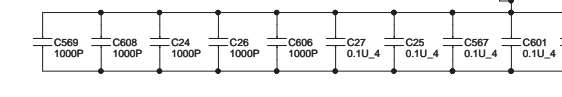
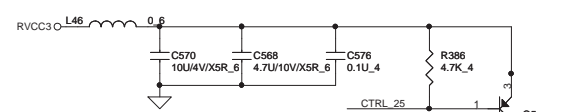
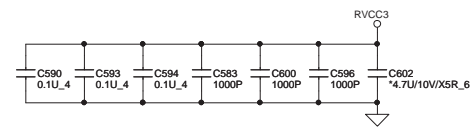
1G -- FCE NS892402P DB0ZH1LAN06
10/100 -- FCE NS892404 DBED2LLAN05

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COMPUTER**

Size	Document Number	Rev
	Marvell 10/100, Gigabit LAN	1A
Date: Wednesday, October 03, 2007 Sheet 24 of 35		



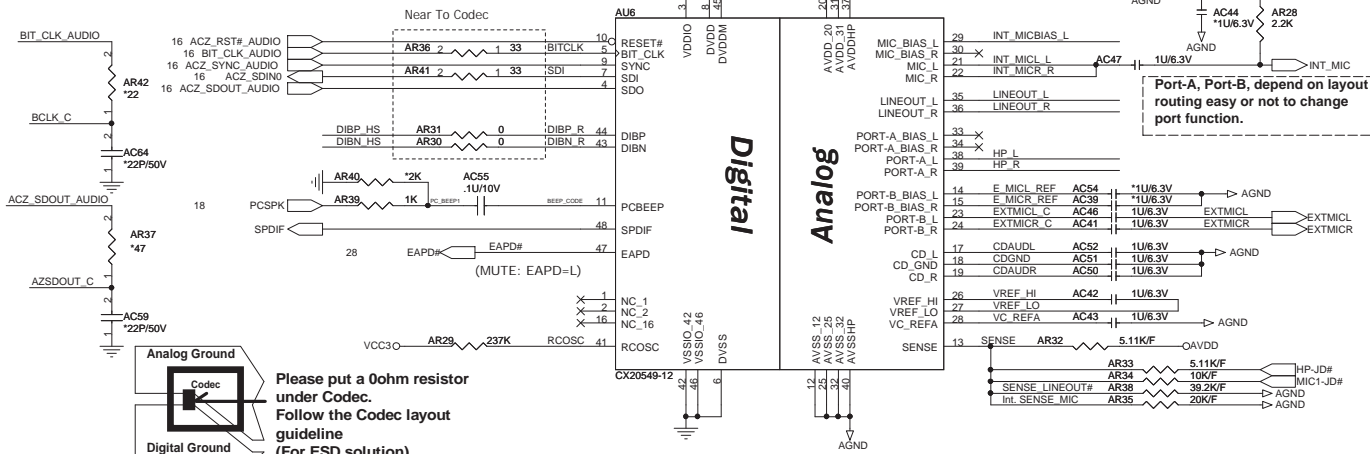
Place close IC side



Codec Conexant & Amp.

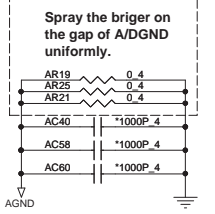
<http://hobi-elektronika.net>

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5V signaling on the HDA interface pins; when VDDIO is +3.3V, the device will use 3.3V signaling on the HDA interface pins.

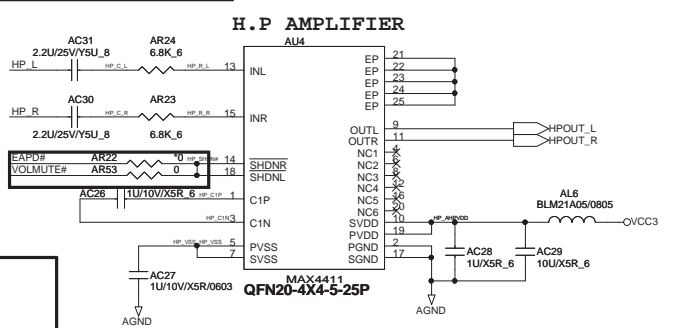
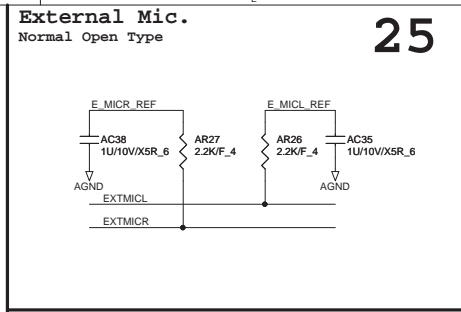


Analog Ground
Digital Ground

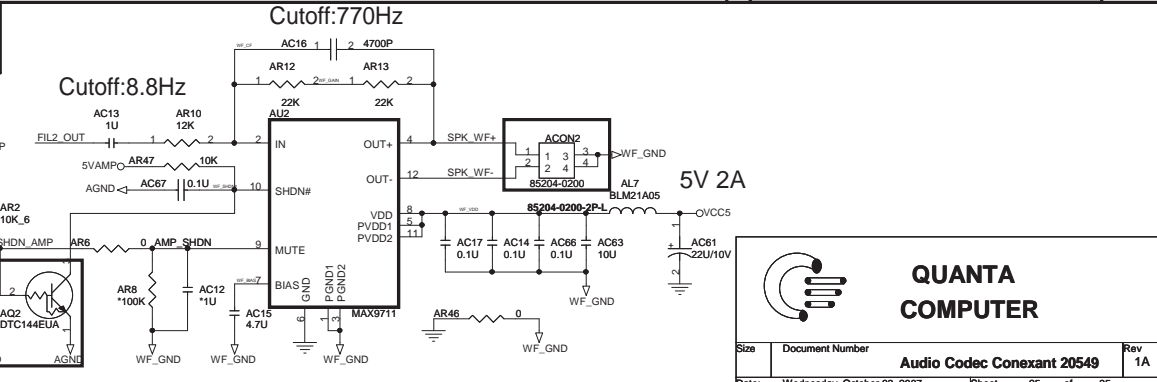
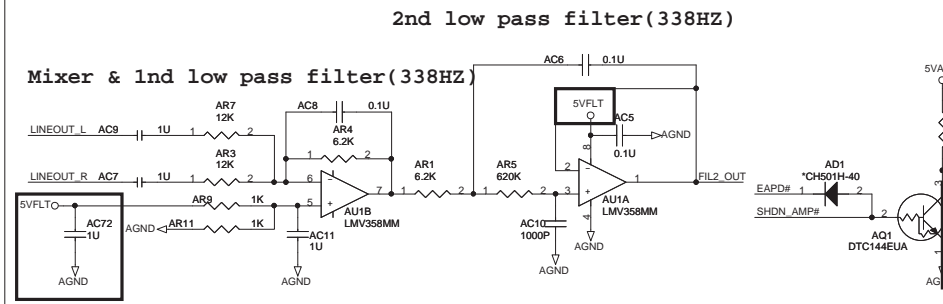
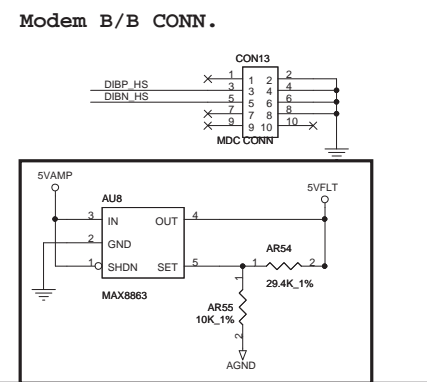
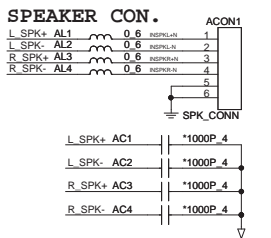
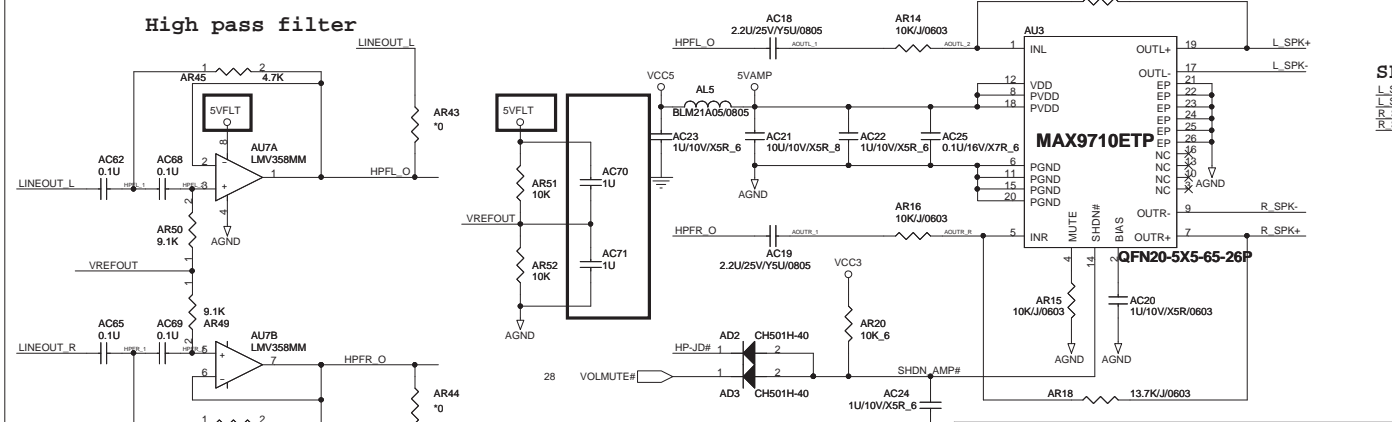
Please put a 0ohm resistor under Codec. Follow the Codec layout guideline (For ESD solution)



Port-A, Port-B, depend on layout routing easy or not to change port function.



Int. Speaker Amplifier



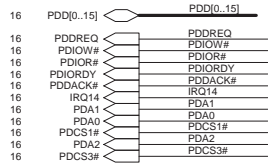
QUANTA COMPUTER

Size Document Number **Audio Codec Conexant 20549** Rev 1A

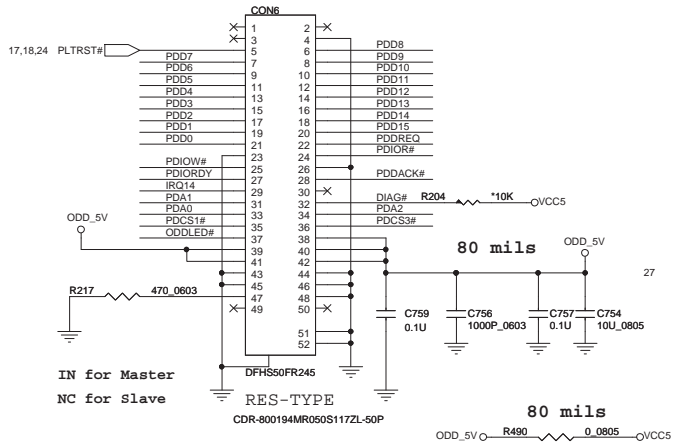
Date: Wednesday, October 03, 2007 Sheet 25 of 35

<http://hobi-elektronika.net>

ODD

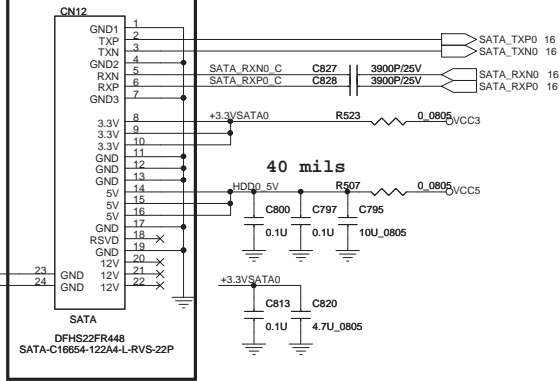


CD-ROM CONNECTOR
SMT TYPE CNN

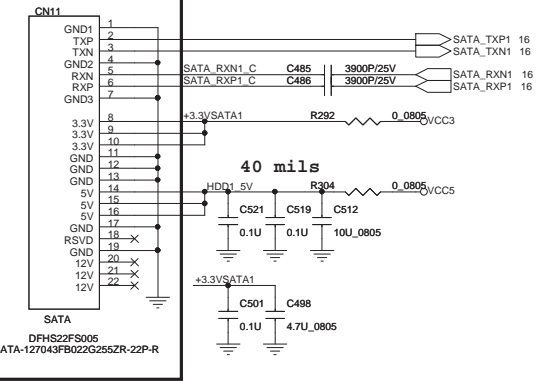


Layout rotate 180 degree

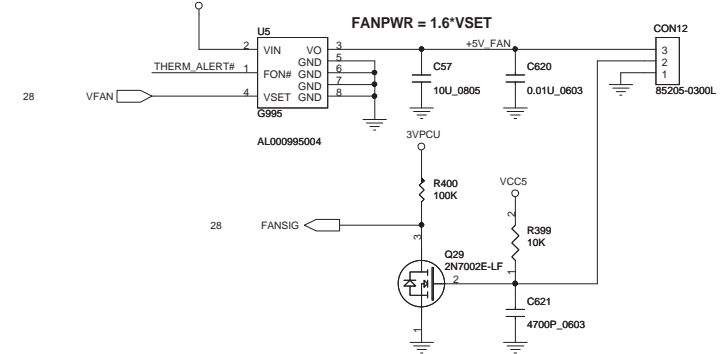
SATA0 HDD



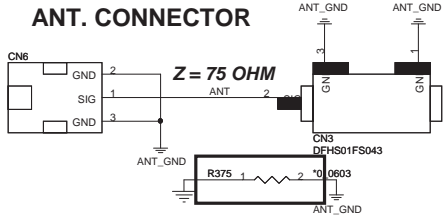
SATA1 HDD



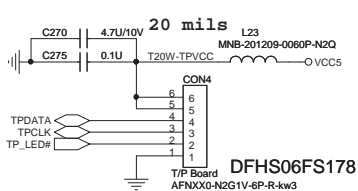
FAN CONN



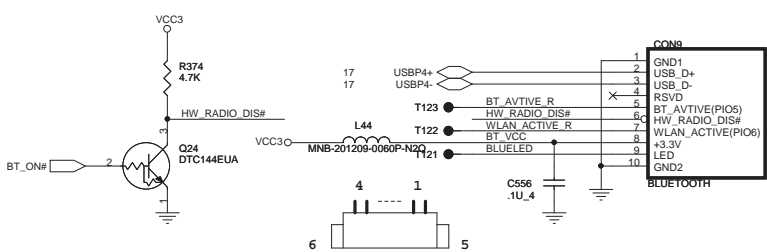
ANT. CONNECTOR



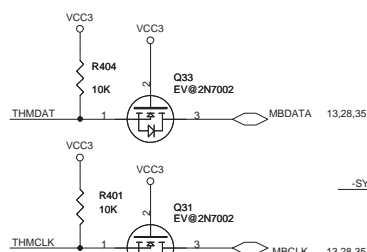
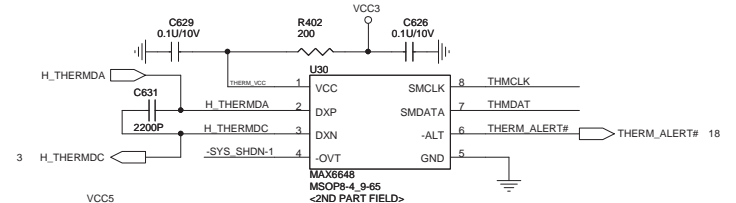
TOUCH PAD



BT Connector



Thermal Sensor



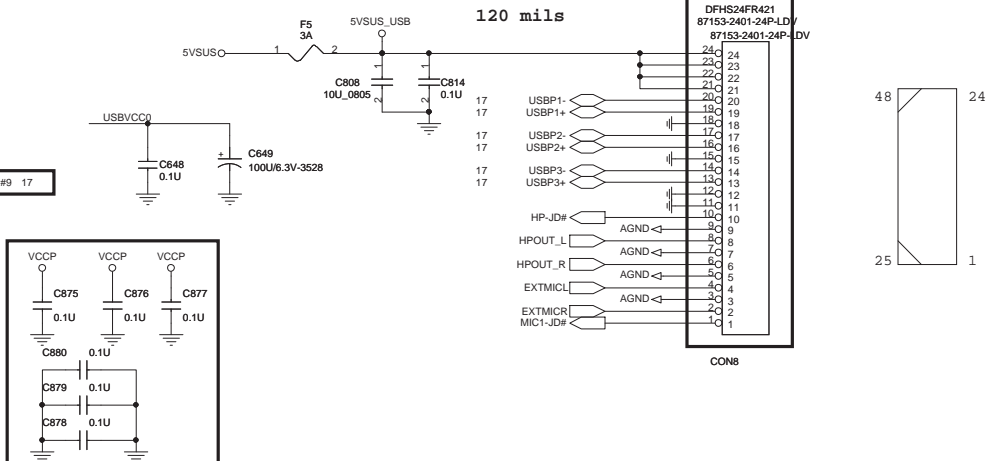
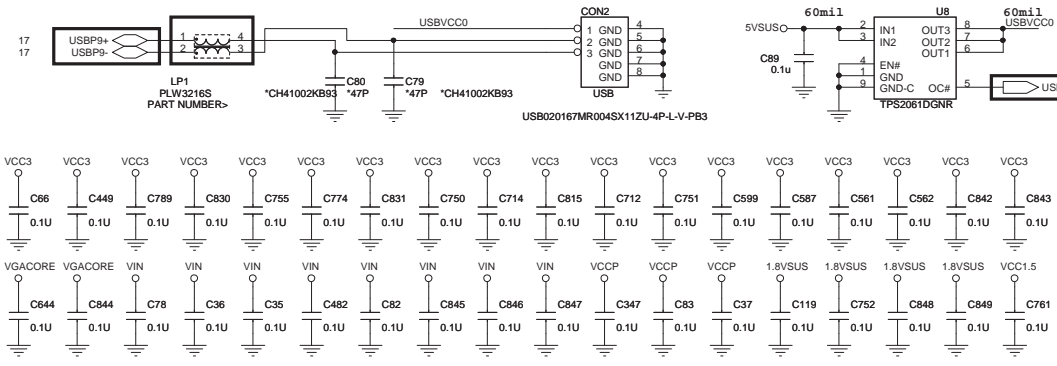
QUANTA COMPUTER

Size: Document Number: **SATA, ODD, Thermal, BT, FP, TP, FAN** Rev: 1A

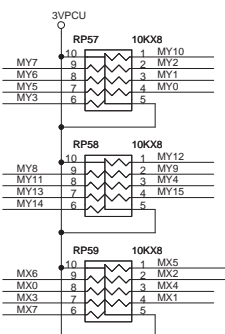
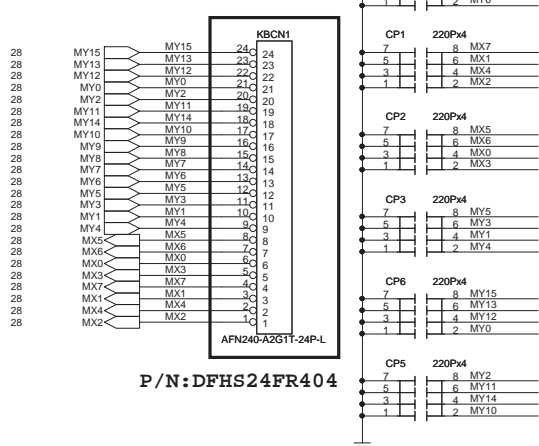
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USB Right

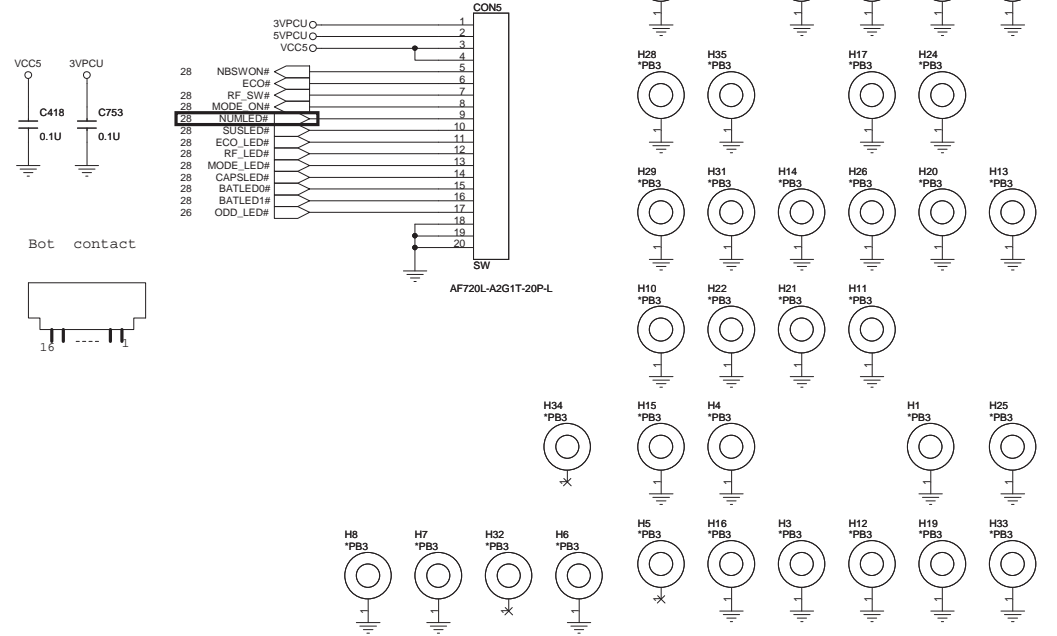
USB Left



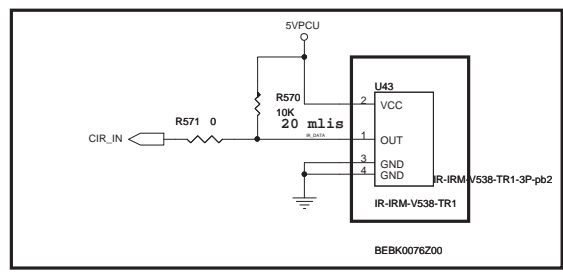
INT Keyboard



SWITCH BOARD



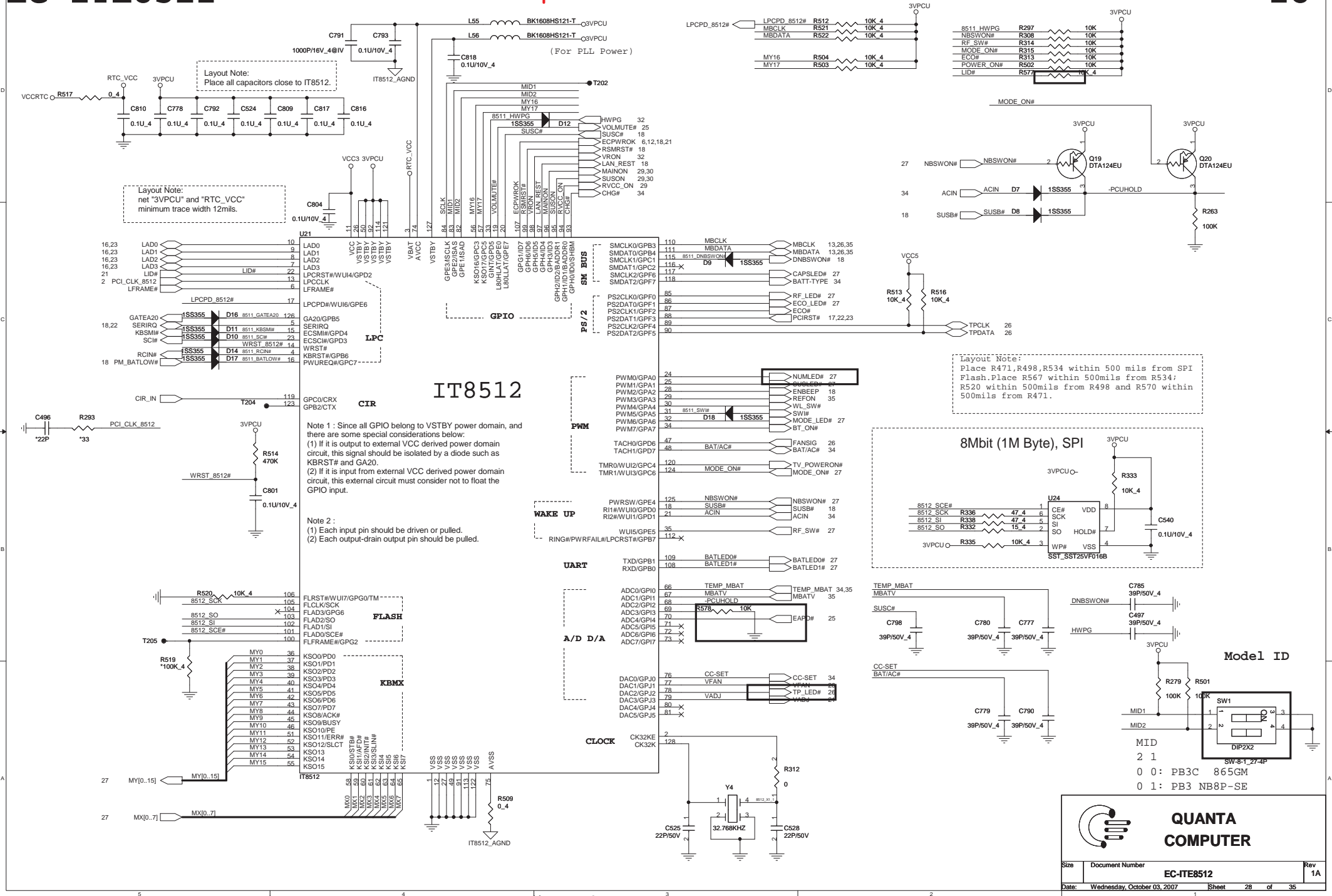
CIR



QUANTA COMPUTER

Size: Document Number: **Keyboard, USB, CIR, SW** Rev: 1A

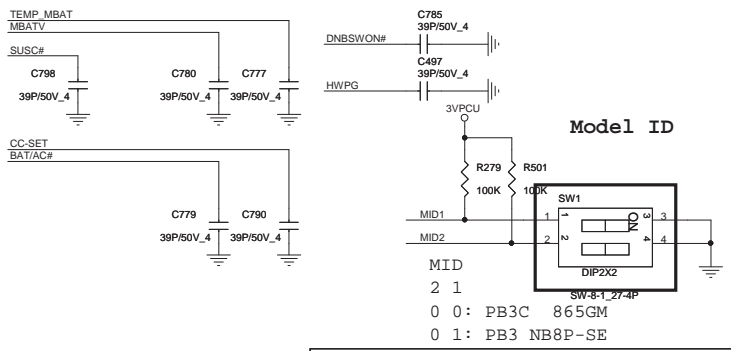
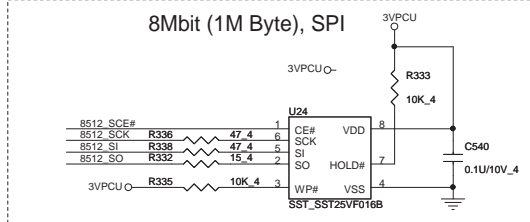
Date: Wednesday, October 03, 2007 Sheet: 27 of 35



Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

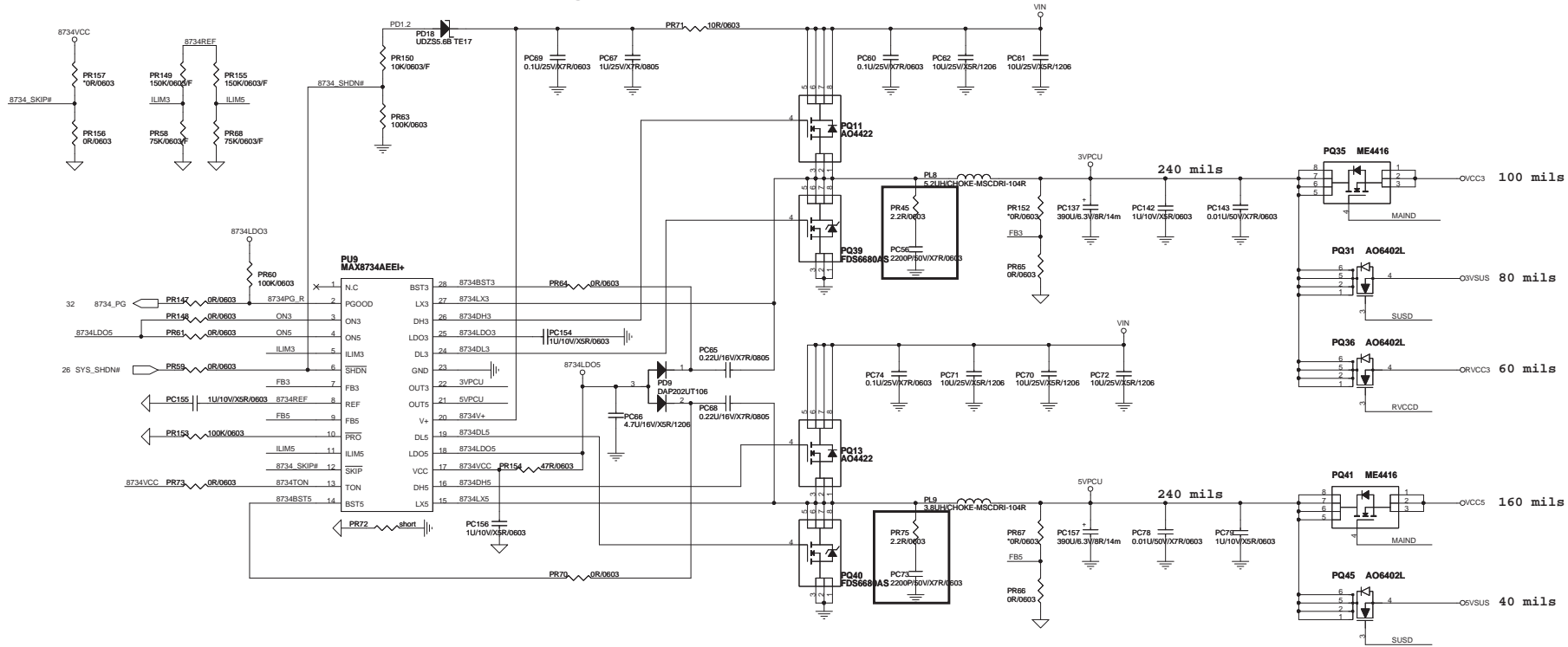
Layout Note:
Place R471,R498,R534 within 500 mils from SPI
Flash.Place R567 within 500mils from R534;
R520 within 500mils from R498 and R570 within
500mils from R471.



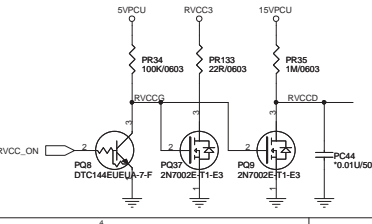
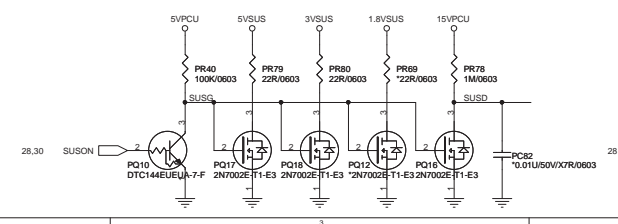
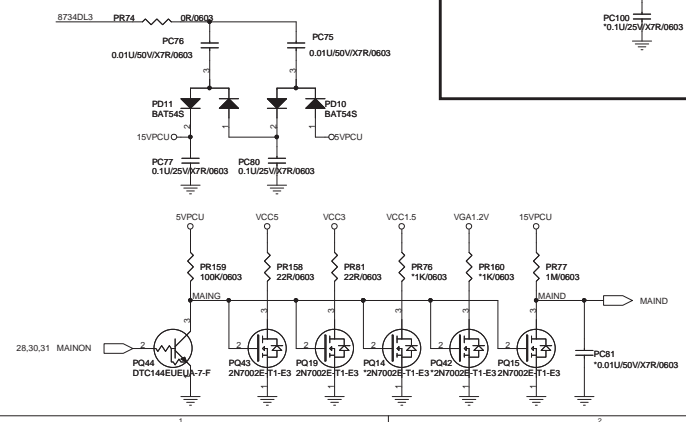
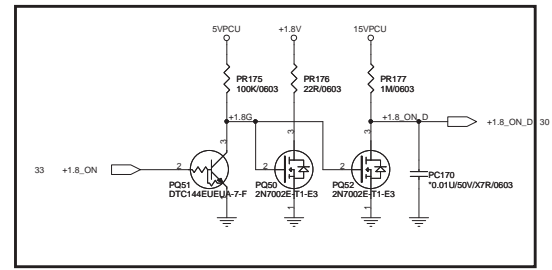
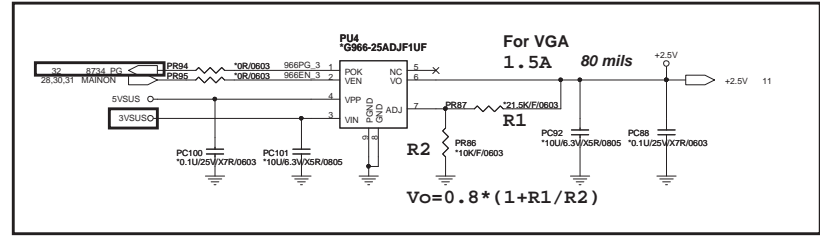
QUANTA COMPUTER

Size Document Number
EC-ITE8512 Rev 1A

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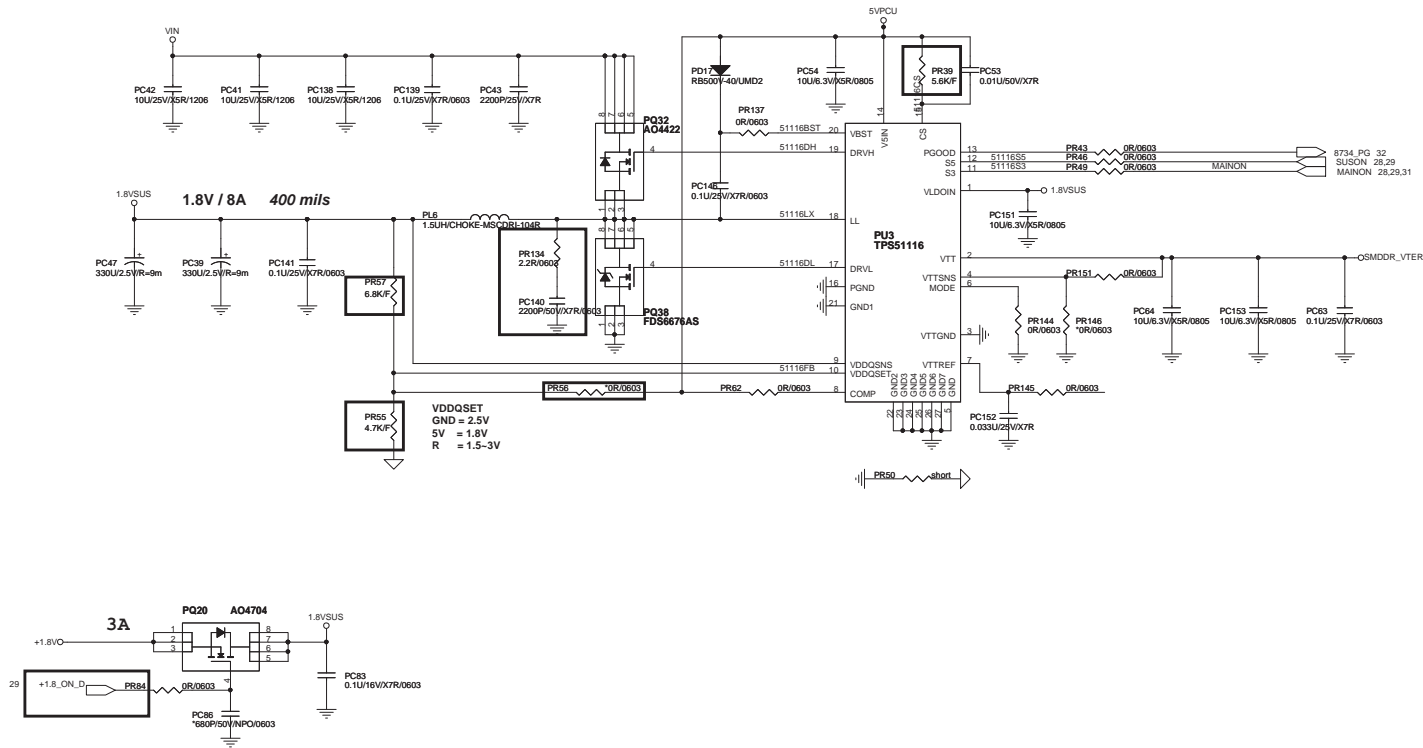



For E version change



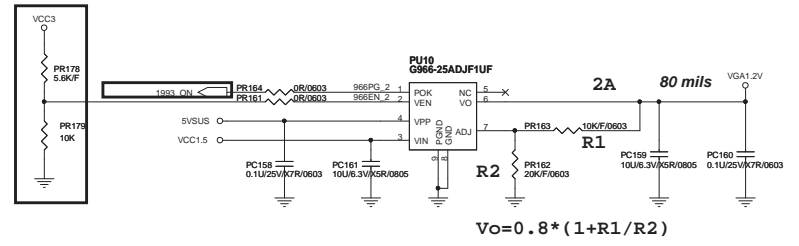
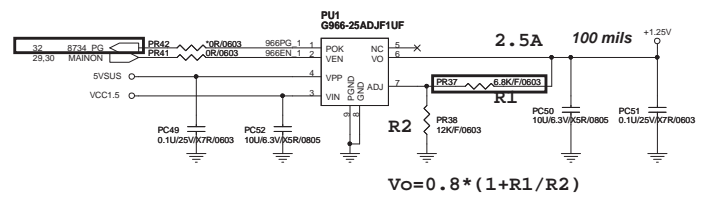
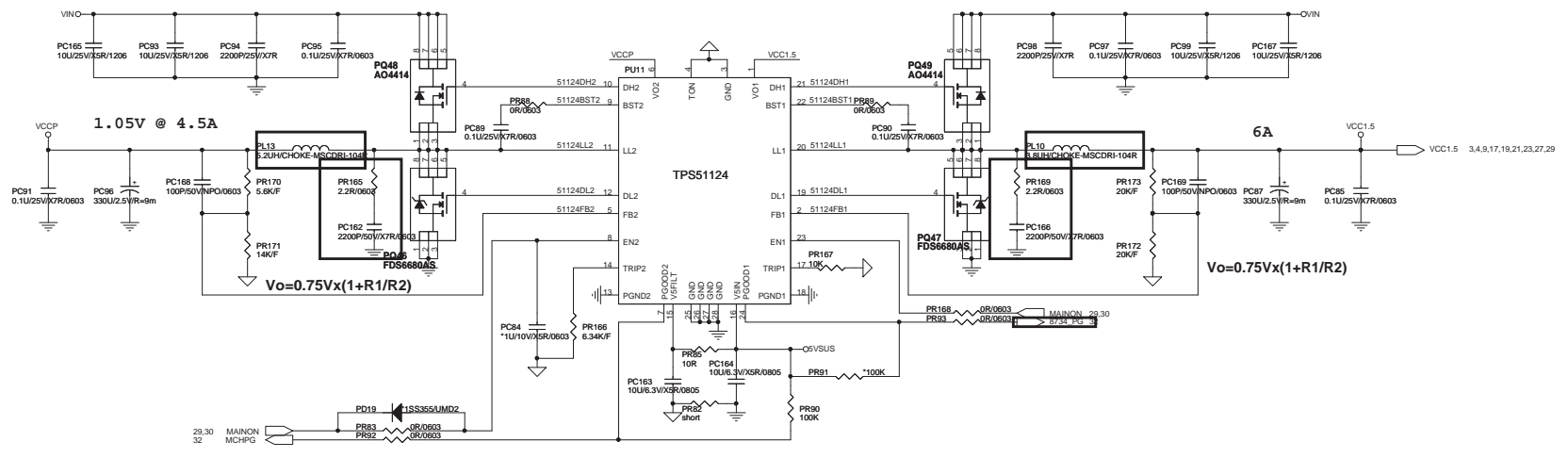
QUANTA COMPUTER

Size	Document Number	3VPCU, 5VPCU	Rev	1A
Date:	Wednesday, October 03, 2007	Sheet	29	of 35



 QUANTA COMPUTER			
Size	Document Number	1.8VSUS, SMDDR_VTERM	Rev
			1A
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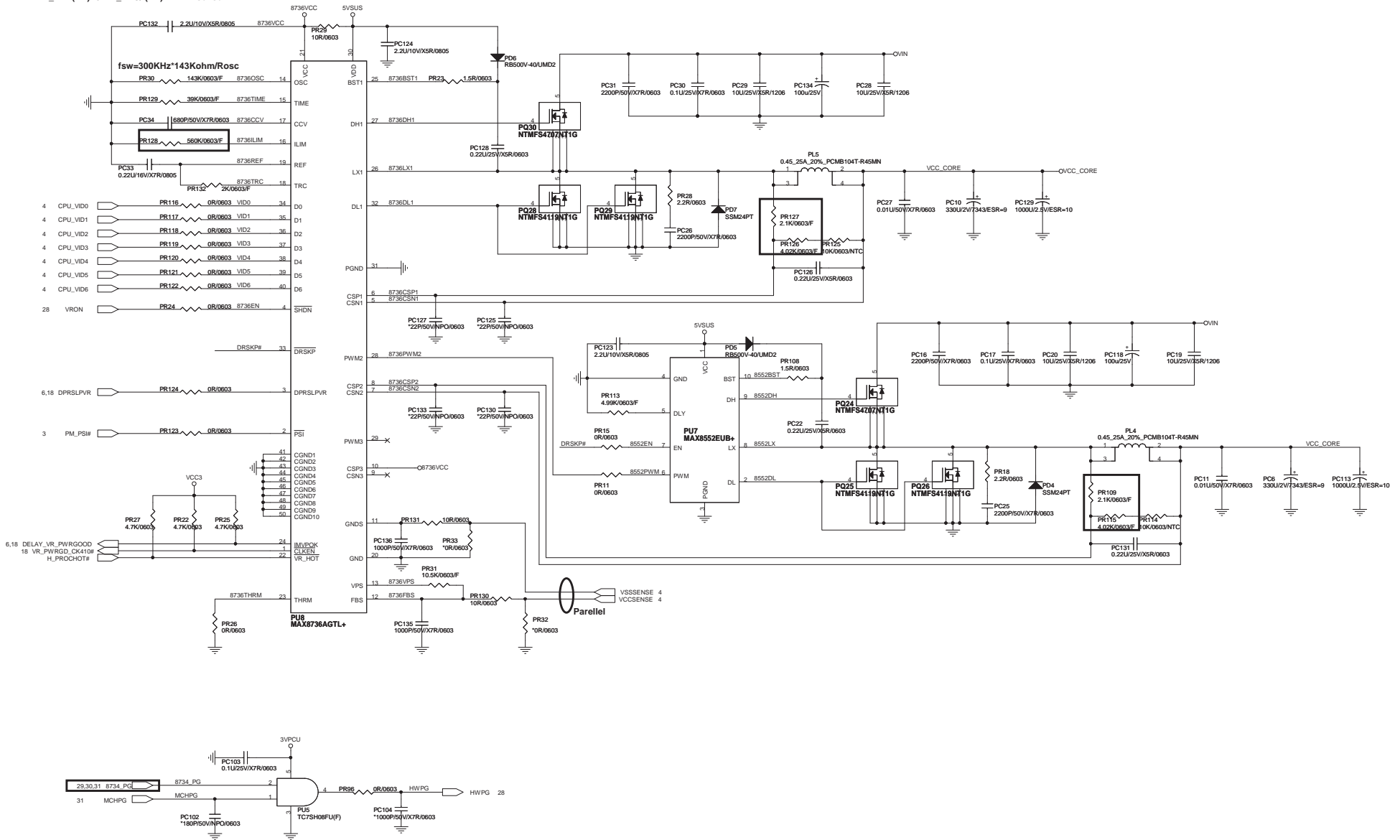
- 2,3,4,5,8,8,16,19,21,27 VCCP
- 3,4,9,17,19,21,23,27,29 VCC1.5
- 6,8,19 +1.25V
- 11,13,29 VGA1.2V




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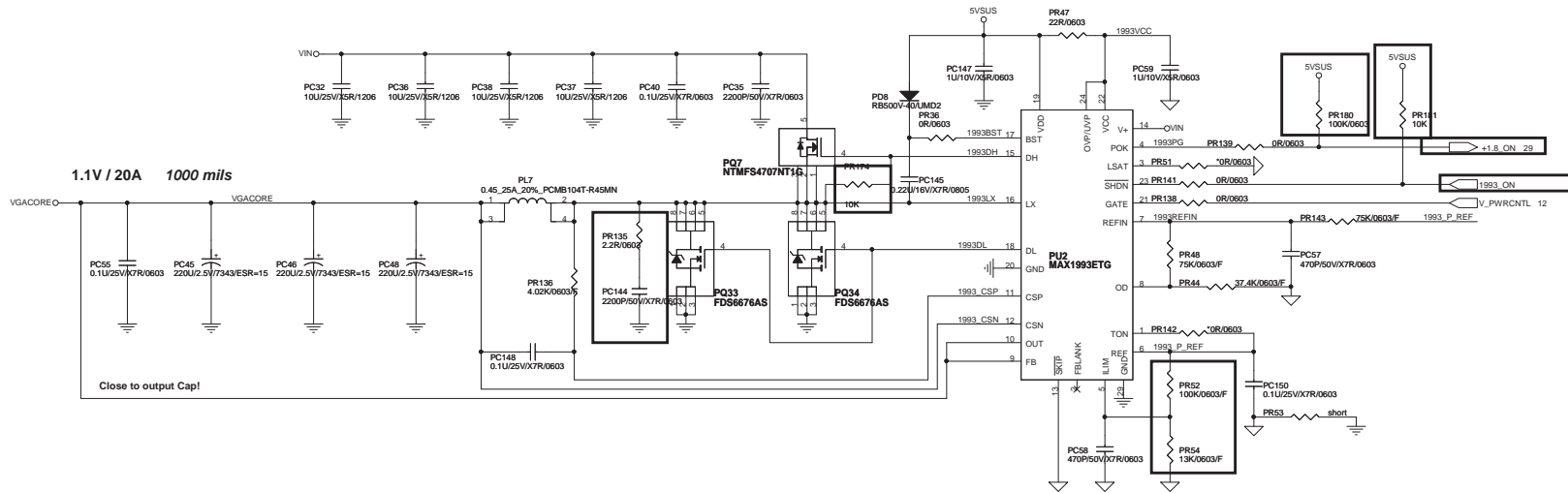
Size	Document Number	Rev
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dV_Target/dt=12.5mV/us*71.5kohm/R_TIME
R_ILIM(PK)=8V*R_TRC/(PK)LIMIT*Rsense

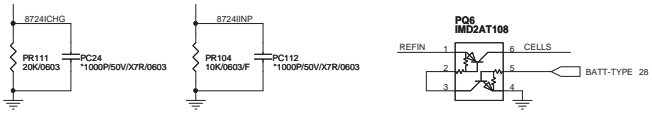
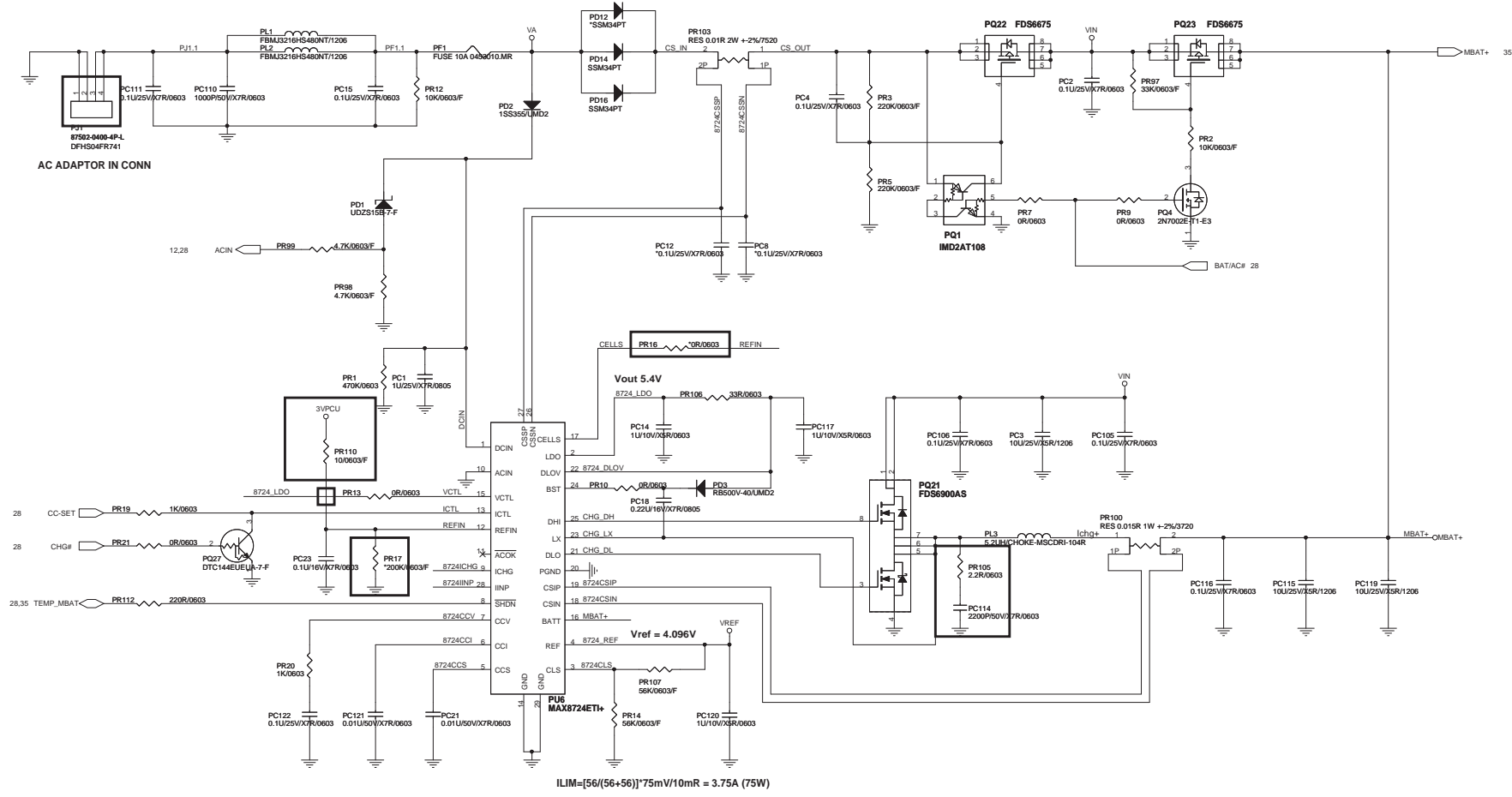



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Size	Document Number	CPU Core	Rev
			1A
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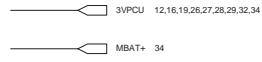
 QUANTA COMPUTER		Size	Document Number	Rev
			VGA Core	1A
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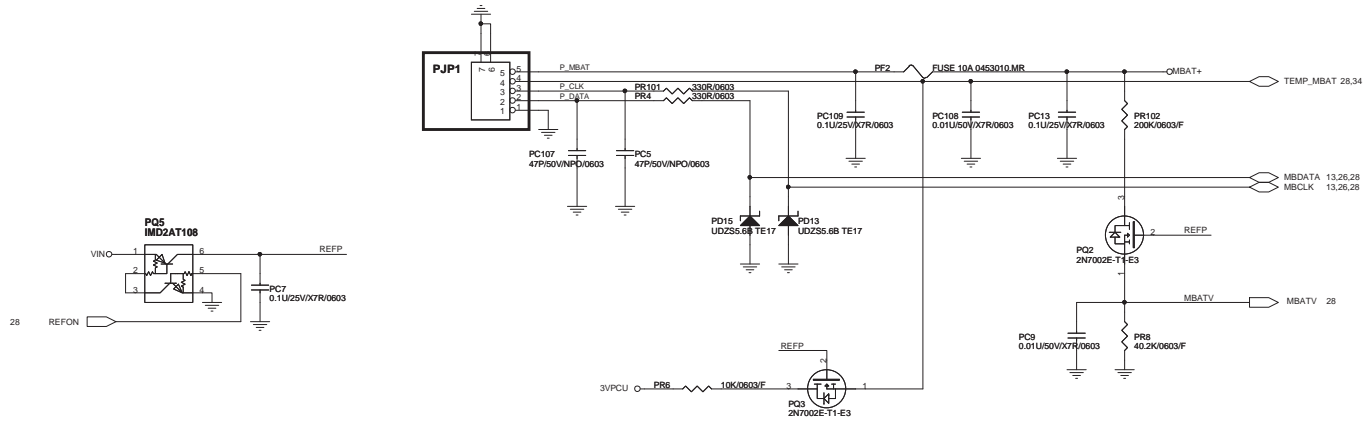
**QUANTA
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Size Document Number **Battery Charger** Rev 1A

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Battery Connector



TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :	
Li-ion 4S*P	$16.8V * 40.2 / (200 + 40.2) = 2.812V$ $12.0V * 40.2 / (200 + 40.2) = 2.008V$
Ni-MH 8S1P	$8.0V * 40.2 / (200 + 40.2) = 1.34V$

**QUANTA
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			1A
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