

# Compal Confidential

## Z5WAE Schematics Document

AMD "Beema" Platform

AMD 25W APU With Puma+ Core

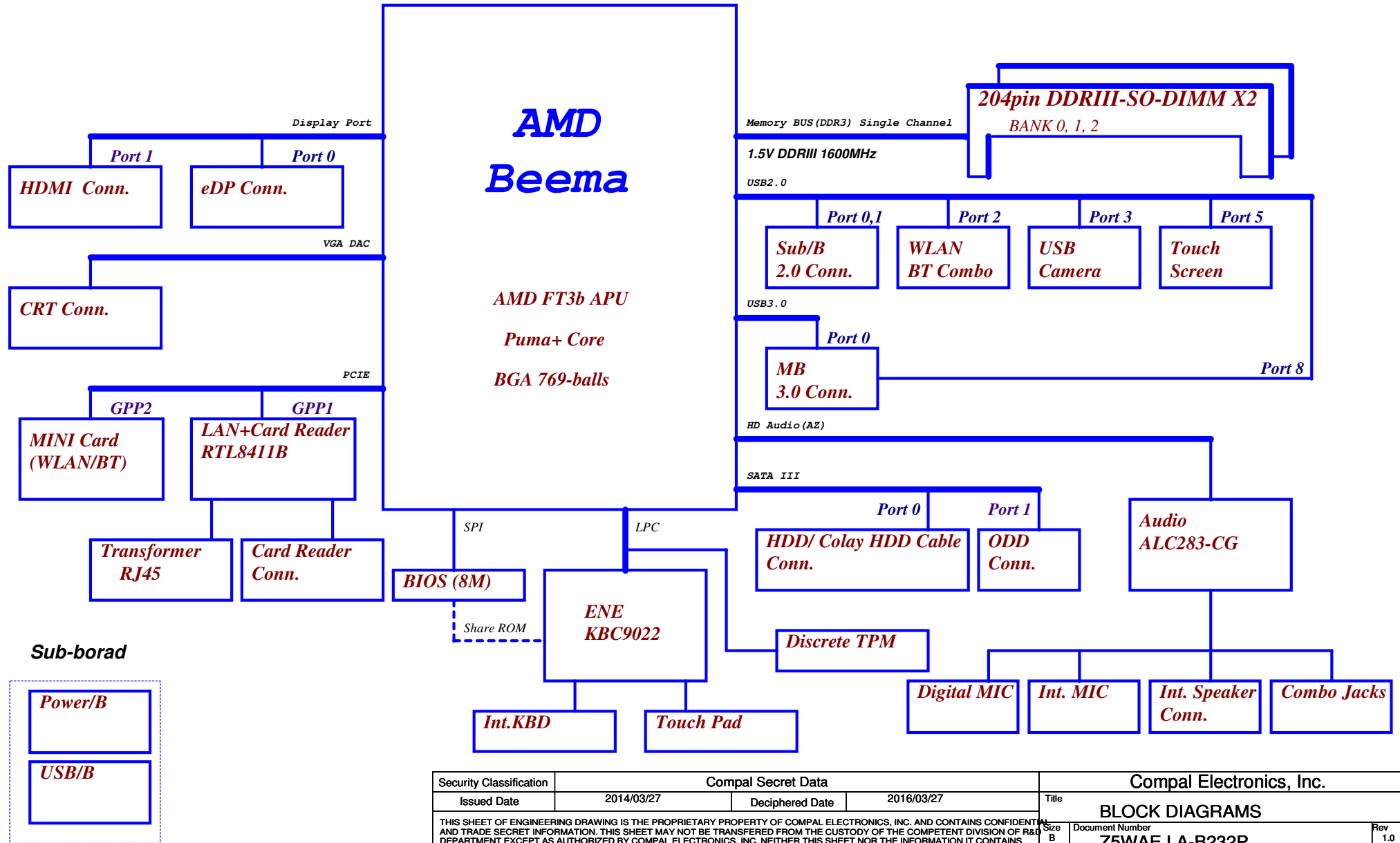
LA-B232P REV: 1.0

2014-03-27

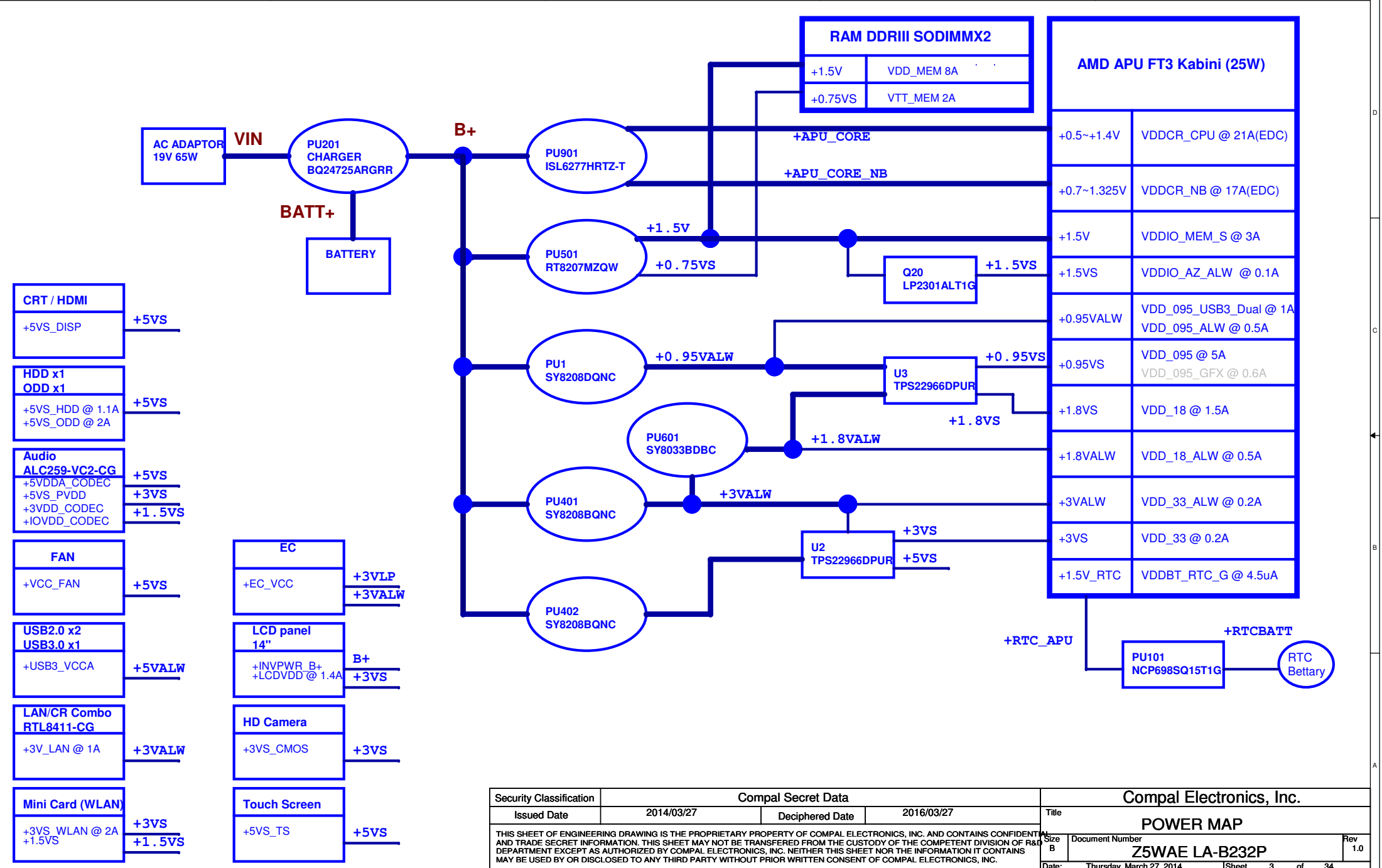
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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	COVER PAGE
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Model Name : Z5WAE



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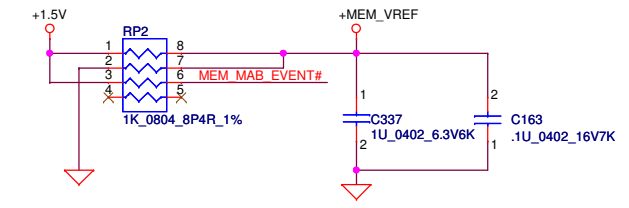


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				Rev 1.0
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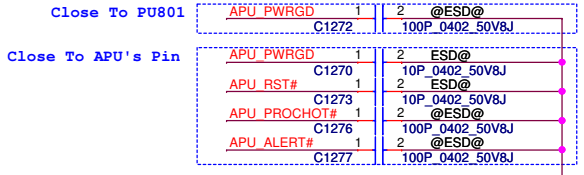
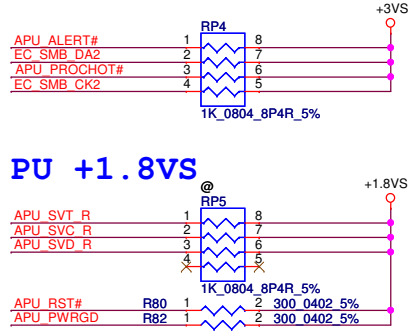
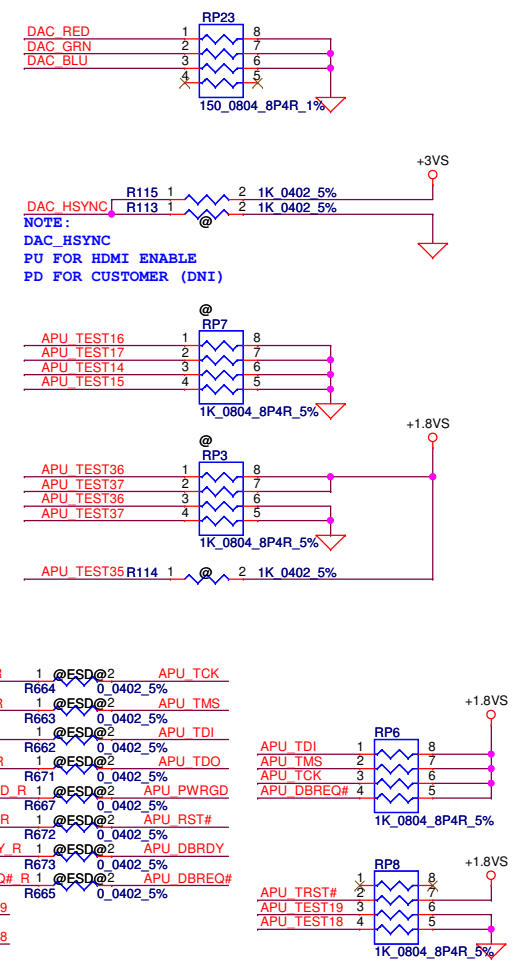
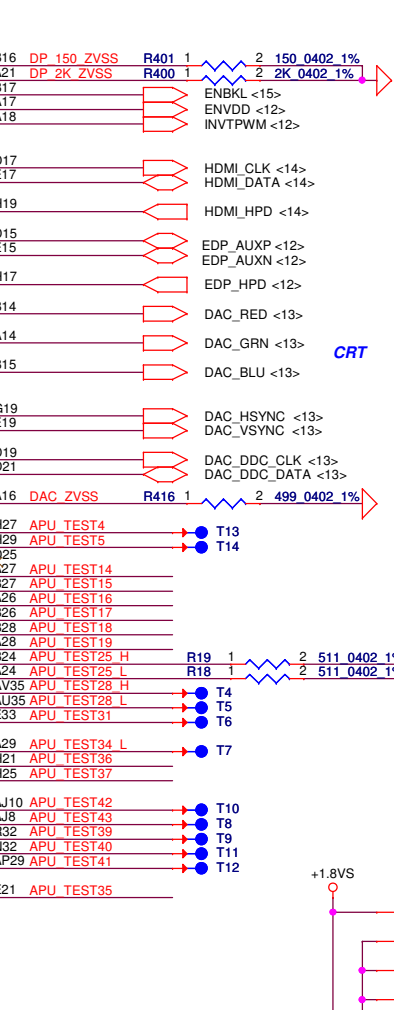
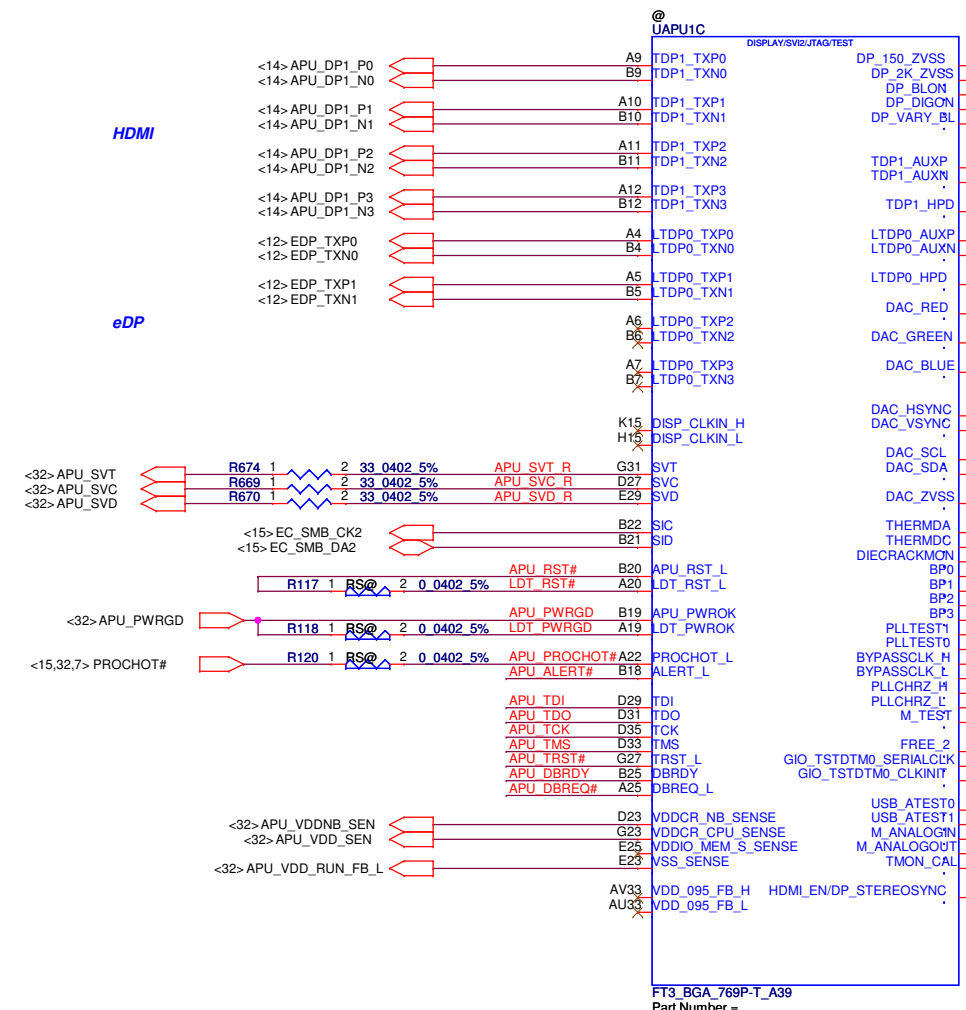




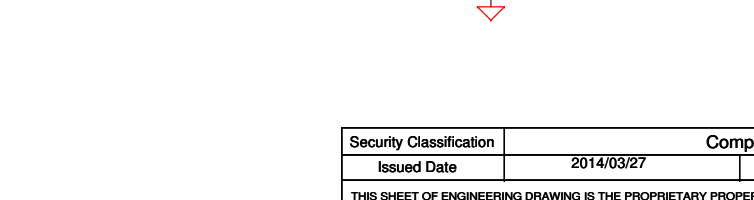
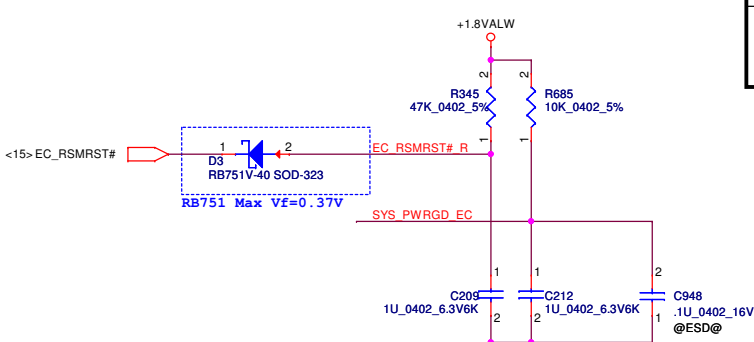
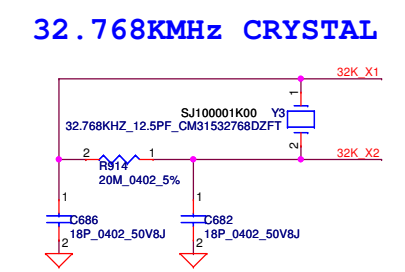
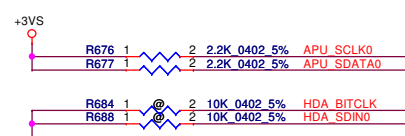
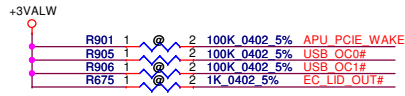
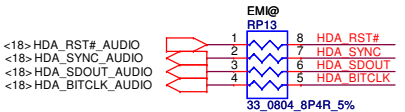
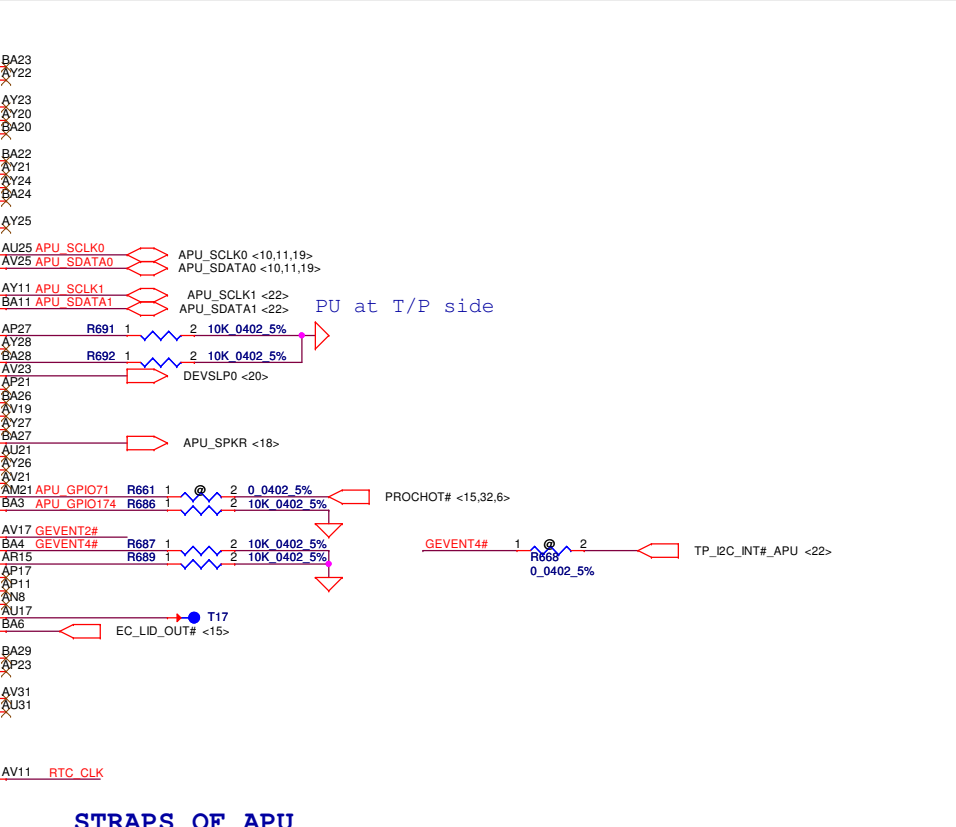
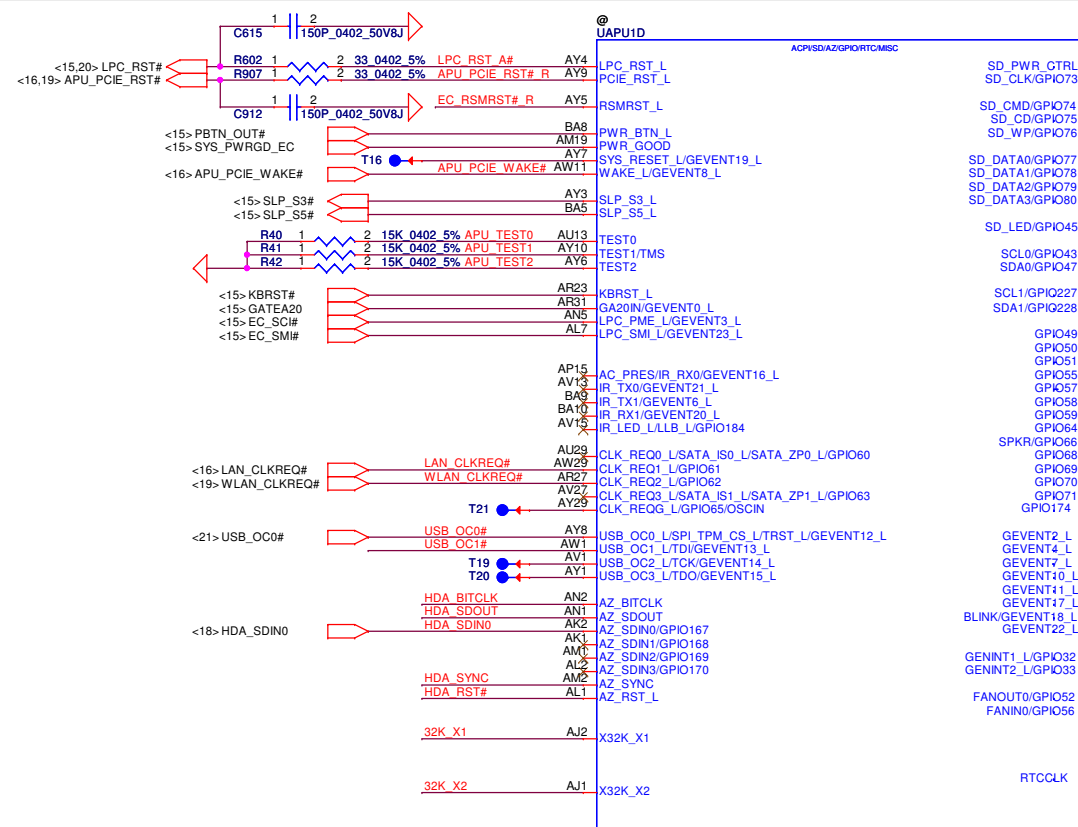
**MEMORY VREF**



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	B	Document Number	Z5WAE LA-B232P	Rev	1.0
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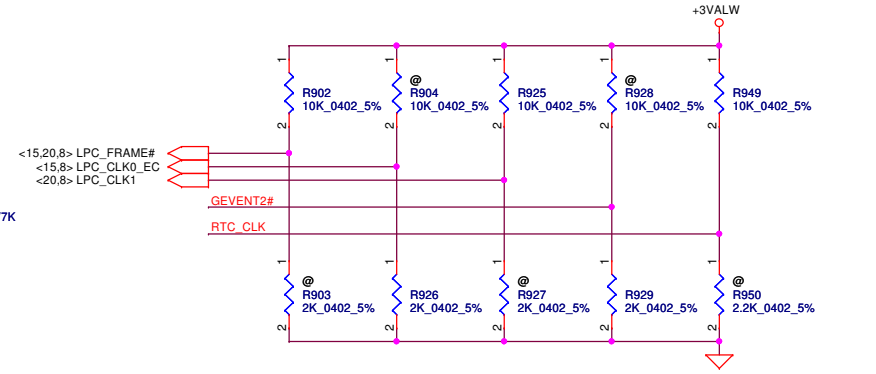


Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2014/03/27	Deciphered Date	2016/03/27	FT3 DISP/MISC/HDT	
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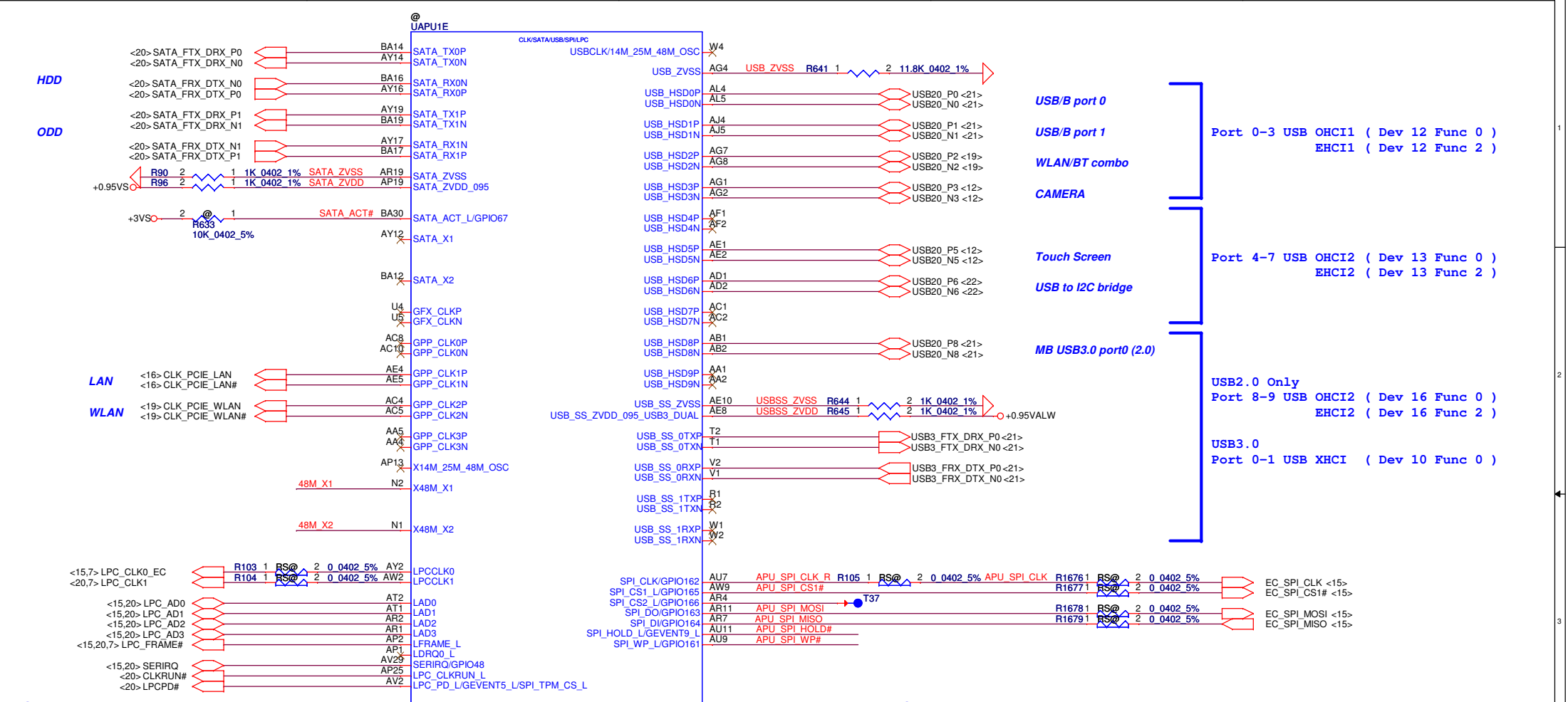


**STRAPS OF APU**

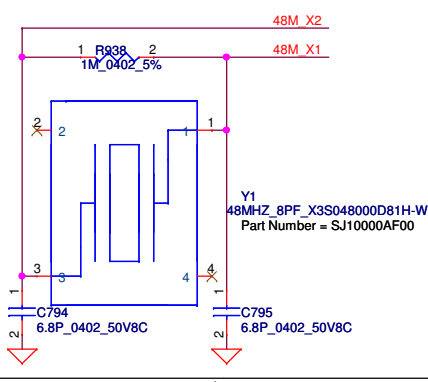
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWER UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION



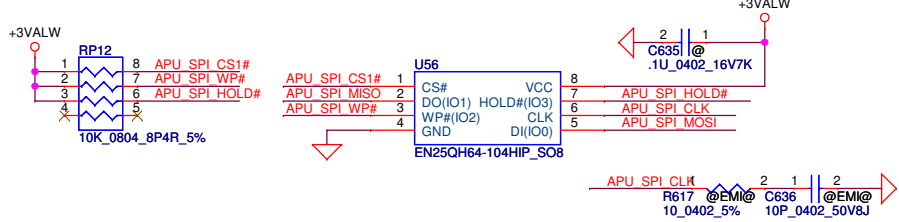
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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title
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**48MHz CRYSTAL**



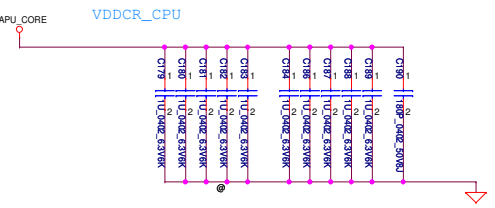
**8MB SPI ROM**



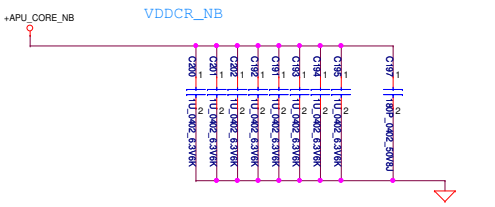
Security Classification	Compal Secret Data		Title	
Issued Date	2014/03/27	Deciphered Date	2016/03/27	FT3 SATA/CLK/USB/SPI
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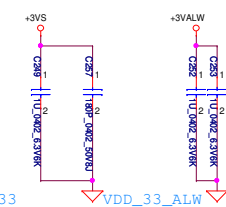
**CORE POWER OF APU**



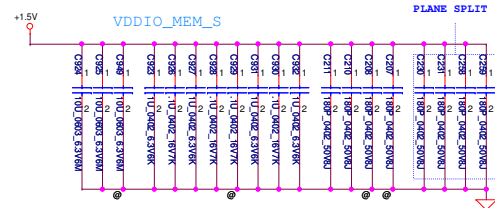
**INTEGRATED GPU POWER OF APU**



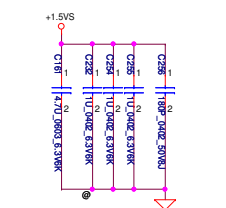
**+3VALW/+3VS OF APU**



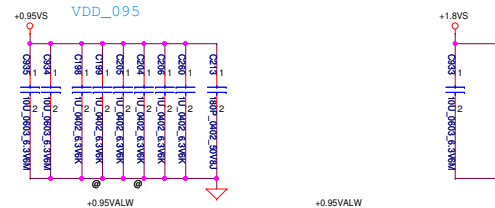
**+1.5V/+1.5VS OF APU**



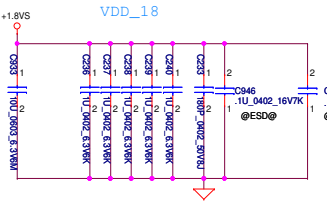
**VDDIO\_AZ\_ALW**  
(Could be S0 or S5 power rail)



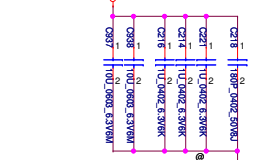
**+0.95VALW/+0.95VS OF APU**



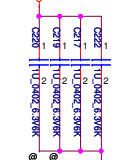
**+1.8VALW/+1.8VS OF APU**



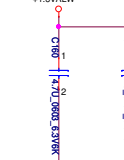
**VDD\_095\_USB3\_DUAL**



**VDD\_095\_ALW**

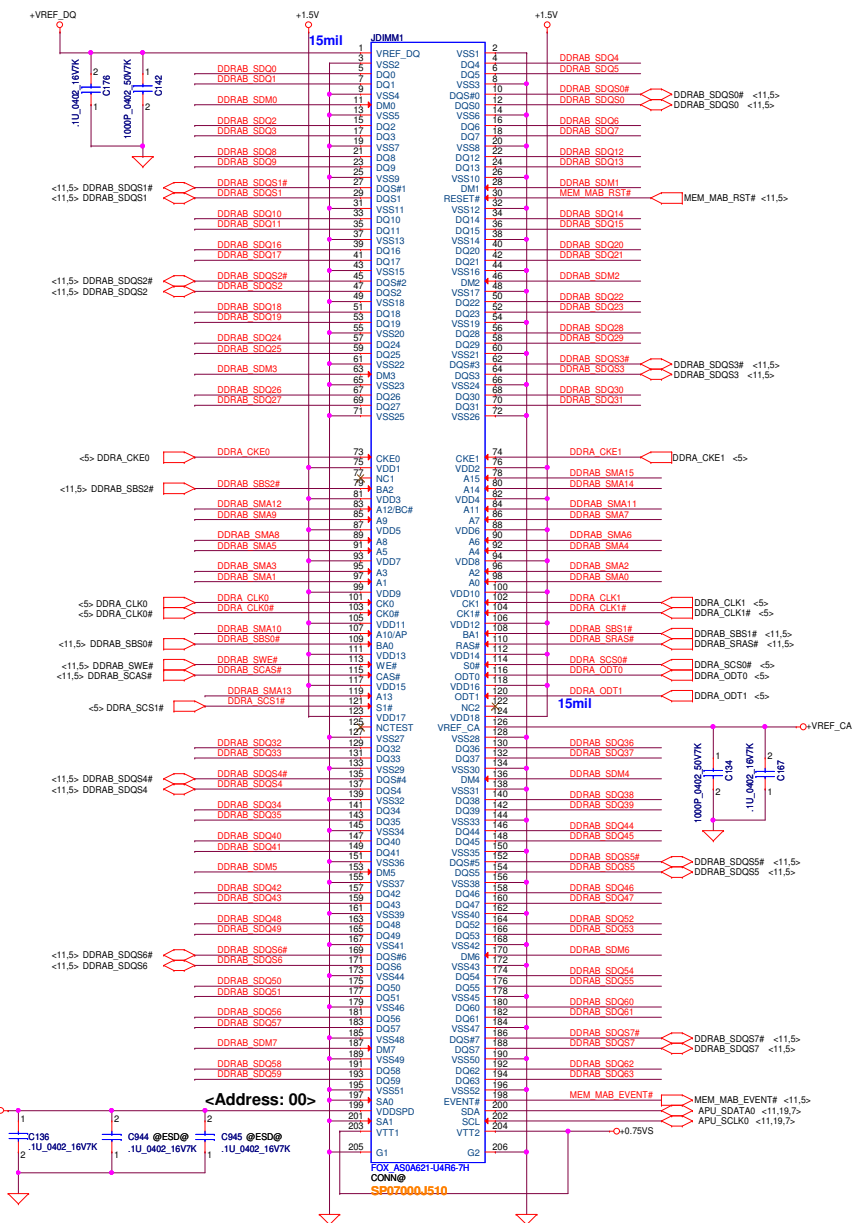


**VDD\_18\_ALW**

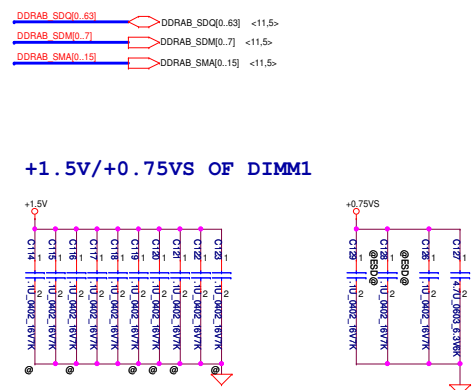


3A

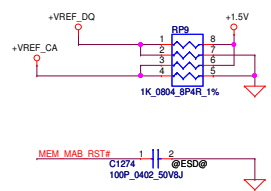
POWER	UAPUIF	UAPUIG	UAPUIH
VDDCR_CPU_1	L21	VSS_1	W29
VDDIO_MEM_S_2	L23	VSS_2	W39
VDDCR_CPU_2	L25	VSS_3	W41
VDDIO_MEM_S_3	L27	VSS_4	W42
VDDCR_CPU_3	L29	VSS_5	W43
VDDIO_MEM_S_4	L31	VSS_6	W44
VDDCR_CPU_4	L33	VSS_7	W45
VDDIO_MEM_S_5	L35	VSS_8	W46
VDDCR_CPU_5	L37	VSS_9	W47
VDDIO_MEM_S_6	L39	VSS_10	W48
VDDCR_CPU_6	L41	VSS_11	W49
VDDIO_MEM_S_7	L43	VSS_12	W50
VDDCR_CPU_7	L45	VSS_13	W51
VDDIO_MEM_S_8	L47	VSS_14	W52
VDDCR_CPU_8	L49	VSS_15	W53
VDDIO_MEM_S_9	L51	VSS_16	W54
VDDCR_CPU_9	L53	VSS_17	W55
VDDIO_MEM_S_10	L55	VSS_18	W56
VDDCR_CPU_10	L57	VSS_19	W57
VDDIO_MEM_S_11	L59	VSS_20	W58
VDDCR_CPU_11	L61	VSS_21	W59
VDDIO_MEM_S_12	L63	VSS_22	W60
VDDCR_CPU_12	L65	VSS_23	W61
VDDIO_MEM_S_13	L67	VSS_24	W62
VDDCR_CPU_13	L69	VSS_25	W63
VDDIO_MEM_S_14	L71	VSS_26	W64
VDDCR_CPU_14	L73	VSS_27	W65
VDDIO_MEM_S_15	L75	VSS_28	W66
VDDCR_CPU_15	L77	VSS_29	W67
VDDIO_MEM_S_16	L79	VSS_30	W68
VDDCR_CPU_16	L81	VSS_31	W69
VDDIO_MEM_S_17	L83	VSS_32	W70
VDDCR_CPU_17	L85	VSS_33	W71
VDDIO_MEM_S_18	L87	VSS_34	W72
VDDCR_CPU_18	L89	VSS_35	W73
VDDIO_MEM_S_19	L91	VSS_36	W74
VDDCR_CPU_19	L93	VSS_37	W75
VDDIO_MEM_S_20	L95	VSS_38	W76
VDDCR_CPU_20	L97	VSS_39	W77
VDDIO_MEM_S_21	L99	VSS_40	W78
VDDCR_CPU_21	L101	VSS_41	W79
VDDIO_MEM_S_22	L103	VSS_42	W80
VDDCR_CPU_22	L105	VSS_43	W81
VDDIO_MEM_S_23	L107	VSS_44	W82
VDDCR_CPU_23	L109	VSS_45	W83
VDDIO_MEM_S_24	L111	VSS_46	W84
VDDCR_CPU_24	L113	VSS_47	W85
VDDIO_MEM_S_25	L115	VSS_48	W86
VDDCR_CPU_25	L117	VSS_49	W87
VDDIO_MEM_S_26	L119	VSS_50	W88
VDDCR_CPU_26	L121	VSS_51	W89
VDDCR_NB_1	L13	VSS_52	W90
VDDCR_NB_2	L17	VSS_53	W91
VDDCR_NB_3	N11	VSS_54	W92
VDDCR_NB_4	N13	VSS_55	W93
VDDCR_NB_5	N17	VSS_56	W94
VDDCR_NB_6	R11	VSS_57	W95
VDDCR_NB_7	R13	VSS_58	W96
VDDCR_NB_8	R17	VSS_59	W97
VDDCR_NB_9	U13	VSS_60	W98
VDDCR_NB_10	U17	VSS_61	W99
VDDCR_NB_11	W13	VSS_62	W100
VDDCR_NB_12	AA13	VSS_63	W101
VDDCR_NB_13	AA17	VSS_64	W102
VDDCR_NB_14	AA19	VSS_65	W103
VDDCR_NB_15	AA21	VSS_66	W104
VDDCR_NB_16	AA23	VSS_67	W105
VDDCR_NB_17	AA25	VSS_68	W106
VDDCR_NB_18	AA27	VSS_69	W107
VDDCR_NB_19	AA29	VSS_70	W108
VDDCR_NB_20	AA31	VSS_71	W109
VDDCR_NB_21	AA33	VSS_72	W110
VDDCR_NB_22	AA35	VSS_73	W111
VDDCR_NB_23	AA37	VSS_74	W112
VDDCR_NB_24	AA39	VSS_75	W113
VDDCR_NB_25	AA41	VSS_76	W114
VDDCR_NB_26	AA43	VSS_77	W115
VDDCR_NB_27	AA45	VSS_78	W116
VDDCR_NB_28	AA47	VSS_79	W117
VDDCR_NB_29	AA49	VSS_80	W118
VDDCR_NB_30	AA51	VSS_81	W119
VDDCR_NB_31	AA53	VSS_82	W120
VDDCR_NB_32	AA55	VSS_83	W121
VDDCR_NB_33	AA57	VSS_84	W122
VDDCR_NB_34	AA59	VSS_85	W123
VDDCR_NB_35	AA61	VSS_86	W124
VDDCR_NB_36	AA63	VSS_87	W125
VDDCR_NB_37	AA65	VSS_88	W126
VDDCR_NB_38	AA67	VSS_89	W127
VDDCR_NB_39	AA69	VSS_90	W128
VDDCR_NB_40	AA71	VSS_91	W129
VDDCR_NB_41	AA73	VSS_92	W130
VDDCR_NB_42	AA75	VSS_93	W131
VDDCR_NB_43	AA77	VSS_94	W132
VDDCR_NB_44	AA79	VSS_95	W133
VDDCR_NB_45	AA81	VSS_96	W134
VDDCR_NB_46	AA83	VSS_97	W135
VDDCR_NB_47	AA85	VSS_98	W136
VDDCR_NB_48	AA87	VSS_99	W137
VDDCR_NB_49	AA89	VSS_100	W138
VDDCR_NB_50	AA91	VSS_101	W139
VDDCR_NB_51	AA93	VSS_102	W140
VDDCR_NB_52	AA95	VSS_103	W141
VDDCR_NB_53	AA97	VSS_104	W142
VDDCR_NB_54	AA99	VSS_105	W143
VDDCR_NB_55	AA101	VSS_106	W144
VDDCR_NB_56	AA103	VSS_107	W145
VDDCR_NB_57	AA105	VSS_108	W146
VDDCR_NB_58	AA107	VSS_109	W147
VDDCR_NB_59	AA109	VSS_110	W148
VDDCR_NB_60	AA111	VSS_111	W149
VDDCR_NB_61	AA113	VSS_112	W150
VDDCR_NB_62	AA115	VSS_113	W151
VDDCR_NB_63	AA117	VSS_114	W152
VDDCR_NB_64	AA119	VSS_115	W153
VDDCR_NB_65	AA121	VSS_116	W154
VDDCR_NB_66	AA123	VSS_117	W155
VDDCR_NB_67	AA125	VSS_118	W156
VDDCR_NB_68	AA127	VSS_119	W157
VDDCR_NB_69	AA129	VSS_120	W158
VDDCR_NB_70	AA131	VSS_121	W159
VDDCR_NB_71	AA133	VSS_122	W160
VDDCR_NB_72	AA135	VSS_123	W161
VDDCR_NB_73	AA137	VSS_124	W162
VDDCR_NB_74	AA139	VSS_125	W163
VDDCR_NB_75	AA141	VSS_126	W164
VDDCR_NB_76	AA143	VSS_127	W165
VDDCR_NB_77	AA145	VSS_128	W166
VDDCR_NB_78	AA147	VSS_129	W167
VDDCR_NB_79	AA149	VSS_130	W168
VDDCR_NB_80	AA151	VSS_131	W169
VDDCR_NB_81	AA153	VSS_132	W170
VDDCR_NB_82	AA155	VSS_133	W171
VDDCR_NB_83	AA157	VSS_134	W172
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VDDCR_NB_85	AA161	VSS_136	W174
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VDDCR_NB_90	AA171	VSS_141	W179
VDDCR_NB_91	AA173	VSS_142	W180
VDDCR_NB_92	AA175	VSS_143	W181
VDDCR_NB_93	AA177	VSS_144	W182
VDDCR_NB_94	AA179	VSS_145	W183
VDDCR_NB_95	AA181	VSS_146	W184
VDDCR_NB_96	AA183	VSS_147	W185
VDDCR_NB_97	AA185	VSS_148	W186
VDDCR_NB_98	AA187	VSS_149	W187
VDDCR_NB_99	AA189	VSS_150	W188
VDDCR_NB_100	AA191	VSS_151	W189
VDDCR_NB_101	AA193	VSS_152	W190
VDDCR_NB_102	AA195	VSS_153	W191
VDDCR_NB_103	AA197	VSS_154	W192
VDDCR_NB_104	AA199	VSS_155	W193
VDDCR_NB_105	AA201	VSS_156	W194
VDDCR_NB_106	AA203	VSS_157	W195
VDDCR_NB_107	AA205	VSS_158	W196
VDDCR_NB_108	AA207	VSS_159	W197
VDDCR_NB_109	AA209	VSS_160	W198
VDDCR_NB_110	AA211	VSS_161	W199
VDDCR_NB_111	AA213	VSS_162	W200
VDDCR_NB_112	AA215	VSS_163	W201
VDDCR_NB_113	AA217	VSS_164	W202
VDDCR_NB_114	AA219	VSS_165	W203
VDDCR_NB_115	AA221	VSS_166	W204
VDDCR_NB_116	AA223	VSS_167	W205
VDDCR_NB_117	AA225	VSS_168	W206
VDDCR_NB_118	AA227	VSS_169	W207
VDDCR_NB_119	AA229	VSS_170	W208
VDDCR_NB_120	AA231	VSS_171	W209
VDDCR_NB_121	AA233	VSS_172	W210
VDDCR_NB_122	AA235	VSS_173	W211
VDDCR_NB_123	AA237	VSS_174	W212
VDDCR_NB_124	AA239	VSS_175	W213
VDDCR_NB_125	AA241	VSS_176	W214
VDDCR_NB_126	AA243	VSS_177	W215
VDDCR_NB_127	AA245	VSS_178	W216
VDDCR_NB_128	AA247	VSS_179	W217
VDDCR_NB_129	AA249	VSS_180	W218
VDDCR_NB_130	AA251	VSS_181	W219
VDDCR_NB_131	AA253	VSS_182	W220
VDDCR_NB_132	AA255	VSS_183	W221
VDDCR_NB_133	AA257	VSS_184	W222
VDDCR_NB_134	AA259	VSS_185	W223
VDDCR_NB_135	AA261	VSS_186	W224
VDDCR_NB_136	AA263	VSS_187	W225
VDDCR_NB_137	AA265	VSS_188	W226
VDDCR_NB_138	AA267	VSS_189	W227
VDDCR_NB_139	AA269	VSS_190	W228
VDDCR_NB_140	AA271	VSS_191	W229
VDDCR_NB_141	AA273	VSS_192	W230
VDDCR_NB_142	AA275	VSS_193	W231
VDDCR_NB_143	AA277	VSS_194	W232
VDDCR_NB_144	AA279	VSS_195	W233
VDDCR_NB_145	AA281	VSS_196	W234
VDDCR_NB_146	AA283	VSS_197	W235
VDDCR_NB_147	AA285	VSS_198	W236
VDDCR_NB_148	AA287	VSS_199	W237
VDDCR_NB_149	AA289	VSS_200	W238
VDDCR_NB_150	AA291	VSS_201	W239
VDDCR_NB_151	AA293	VSS_202	W240
VDDCR_NB_152	AA295	VSS_203	W241
VDDCR_NB_153	AA297	VSS_204	W242
VDDCR_NB_154	AA299	VSS_205	W243
VDDCR_NB_155	AA301	VSS_206	W244
VDDCR_NB_156	AA303	VSS_207	W245
VDDCR_NB_157	AA305	VSS_208	W246
VDDCR_NB_158	AA307	VSS_209	W247
VDDCR_NB_159	AA309	VSS_210	W248
VDDCR_NB_160	AA311	VSS_211	W249
VDDCR_NB_161	AA313	VSS_212	W250
VDDCR_NB_162	AA315	VSS_213	W251
VDDCR_NB_163	AA317	VSS_214	W252
VDDCR_NB_164	AA319	VSS_215	W253
VDDCR_NB_165	AA321	VSS_216	W254
VDDCR_NB_166	AA323	VSS_217	W255
VDDCR_NB_167	AA325	VSS_218	W256
VDDCR_NB_168	AA327	VSS_219	W257
VDDCR_NB_169	AA329	VSS_220	W258
VDDCR_NB_170	AA331	VSS_221	W259
VDDCR_NB_171	AA333	VSS_222	W260
VDDCR_NB_172	AA335	VSS_223	W261
VDDCR_NB_173	AA337	VSS_224	W262
VDDCR_NB_174	AA339	VSS_225	W263
VDDCR_NB_175	AA341	VSS_226	W264
VDDCR_NB_176	AA343	VSS_227	W265
VDDCR_NB_177	AA345	VSS_228	W266
VDDCR_NB_178	AA347	VSS_229	W267
VDDCR_NB_179	AA349	VSS_230	W268
VDDCR_NB_180	AA351	VSS_231	W269
VDDCR_NB_181	AA353	VSS_232	W270
VDDCR_NB_182	AA355	VSS_233	W271
VDDCR_NB_183	AA357	VSS_234	W272
VDDCR_NB_184	AA359	VSS_235	W273
VDDCR_NB_185	AA361	VSS_236	W274
VDDCR_NB_186	AA363	VSS_237	W275
VDDCR_NB_187	AA365	VSS_238	W276
VDDCR_NB_188	AA367	VSS_239	W277
VDDCR_NB_189	AA369	VSS_240	W278
VDDCR_NB_190	AA371	VSS_241	W279
VDDCR_NB_191	AA373	VSS_242	W280
VDDCR_NB_192	AA375	VSS_243	W281
VDDCR_NB_193	AA377	VSS_244	W282
VDDCR_NB_194	AA379	VSS_245	W283
VDDCR_NB_195	AA381	VSS_246	W284
VDDCR_NB_196	AA383	VSS_247	W285
VDDCR_NB_197	AA385	VSS_248	W286
VDDCR_NB_198	AA387	VSS_249	W287
VDDCR_NB_199	AA389	VSS_250	W288
VDDCR_NB_200	AA391	VSS_251	W289
VDDCR_NB_201	AA393	VSS_252	W290
VDDCR_NB			



**DIMM\_A H:4mm RVS**



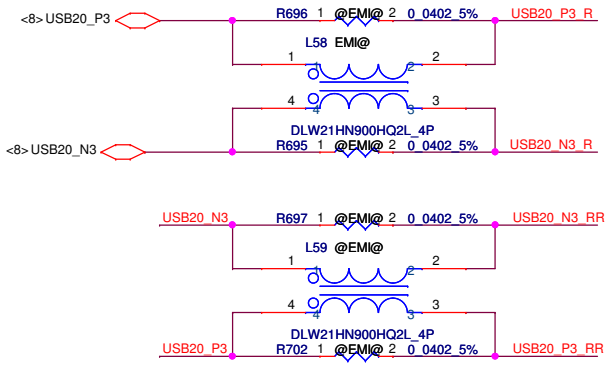
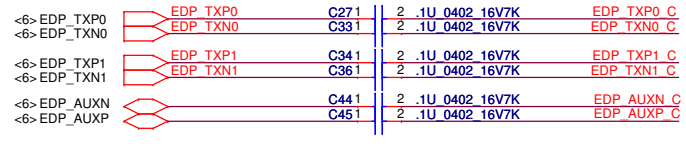
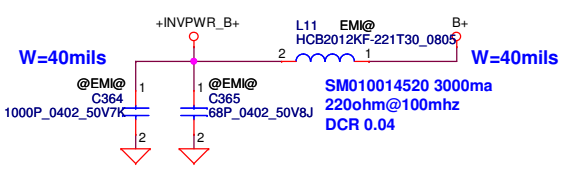
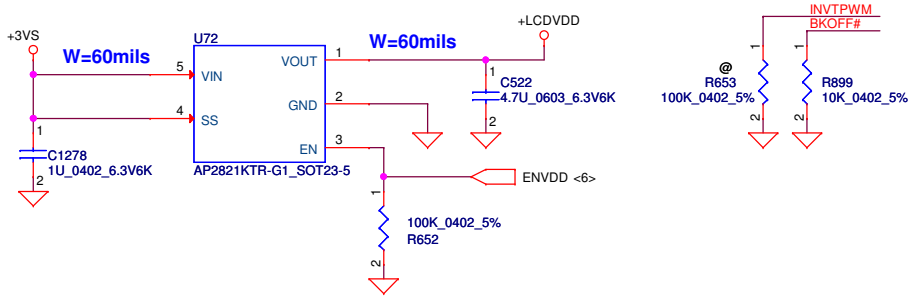
**VREF for DIMM1,2**



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				Z5WAE LA-B232P
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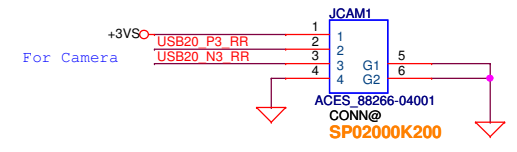
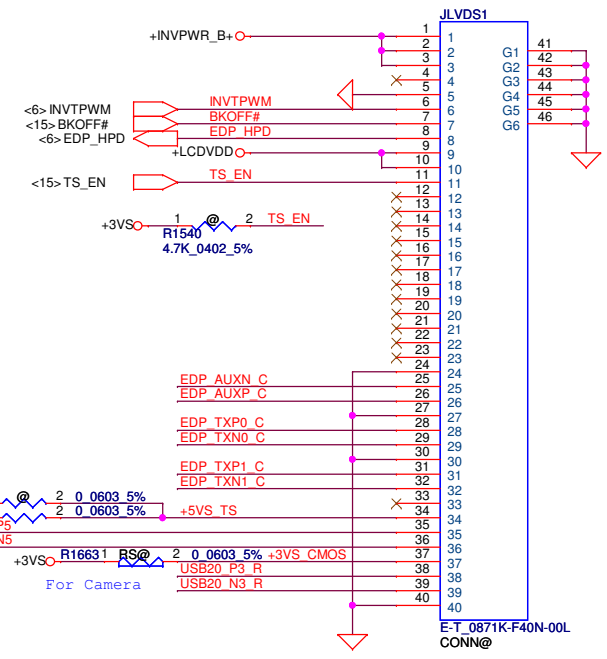


# LCD POWER CIRCUIT

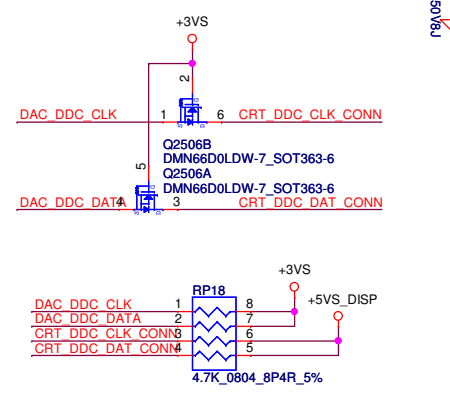
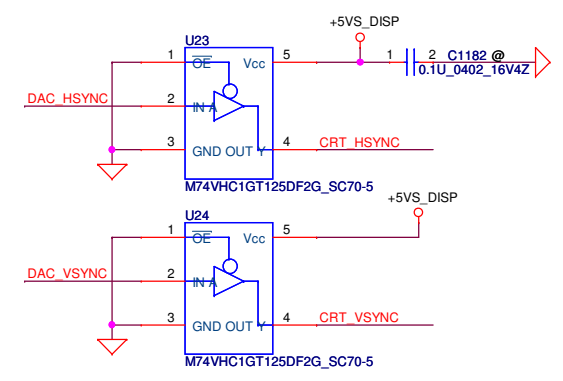
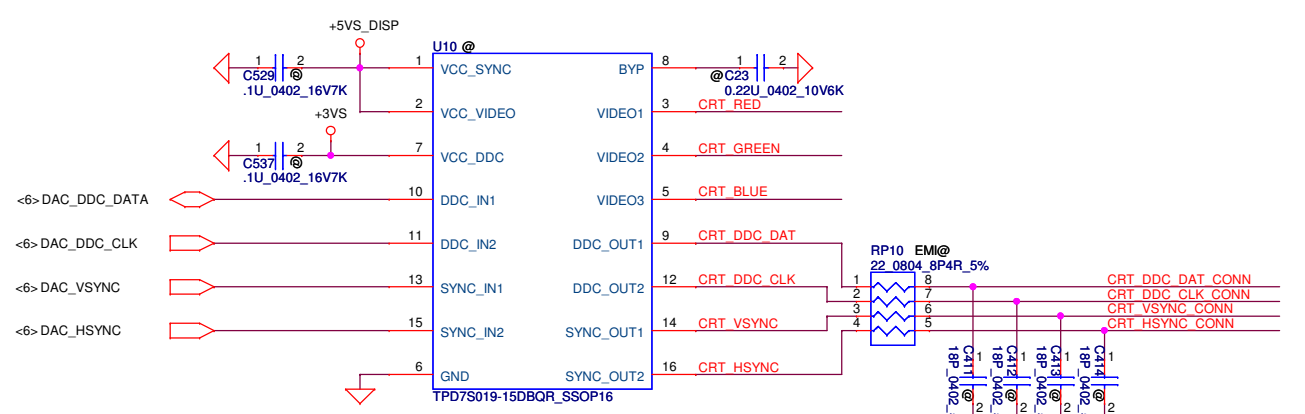
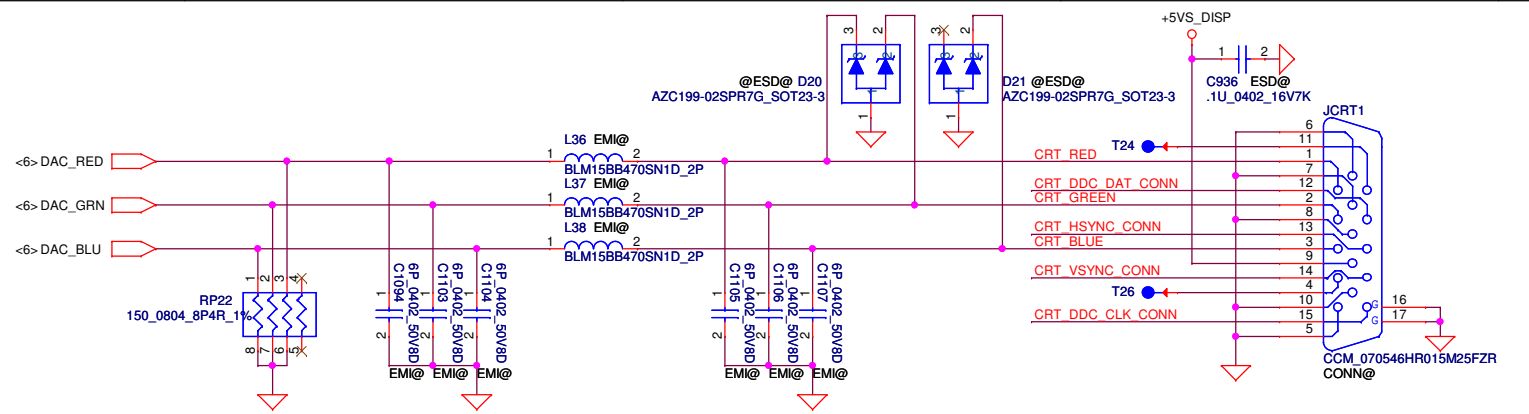


Touch Screen

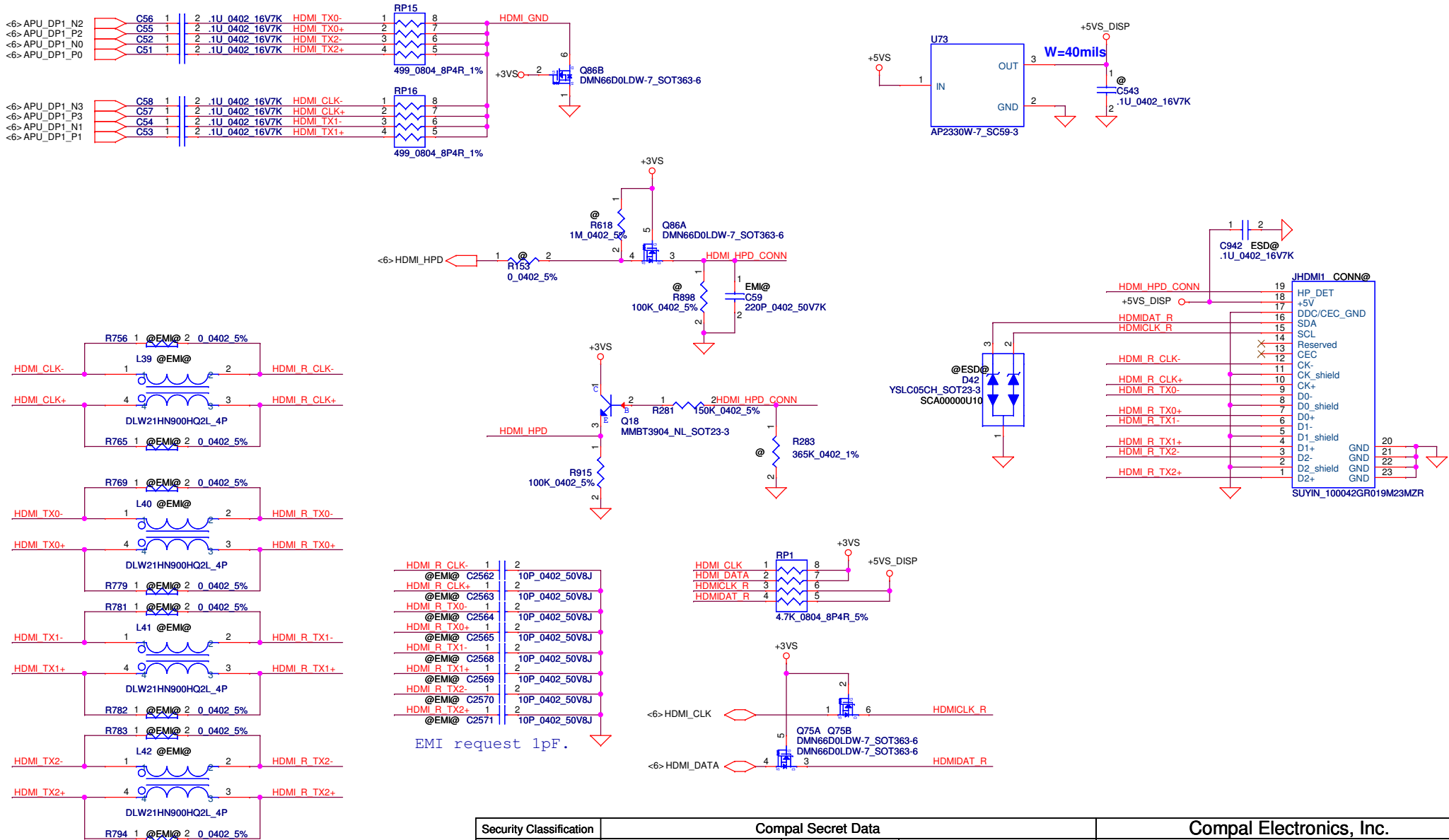
# eDP PANEL Conn.



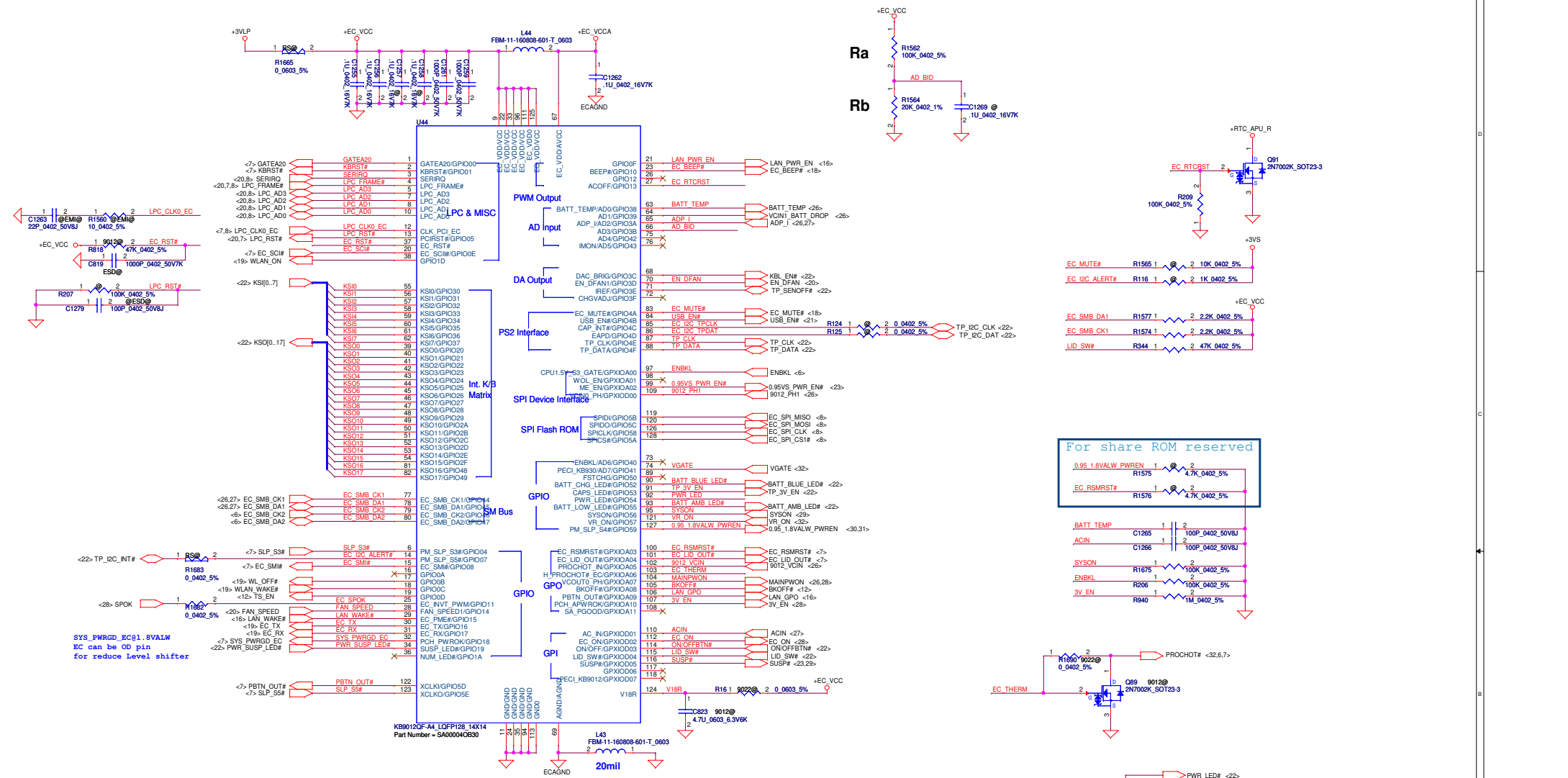
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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title		
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				HDMI CONN		
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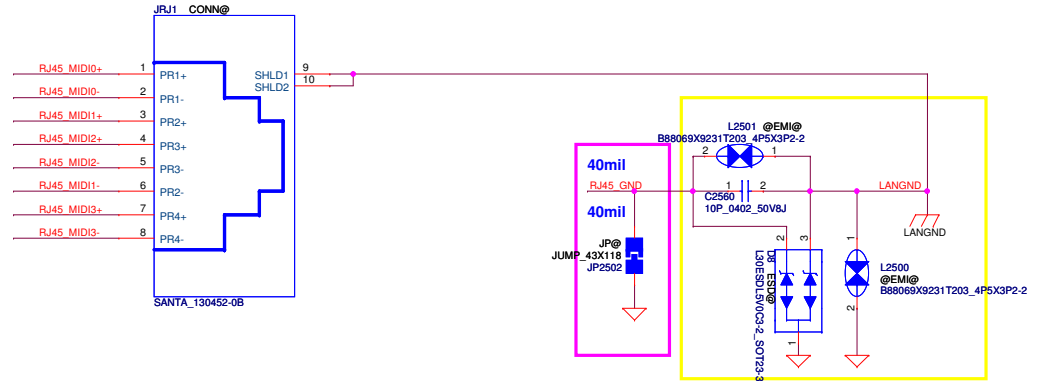
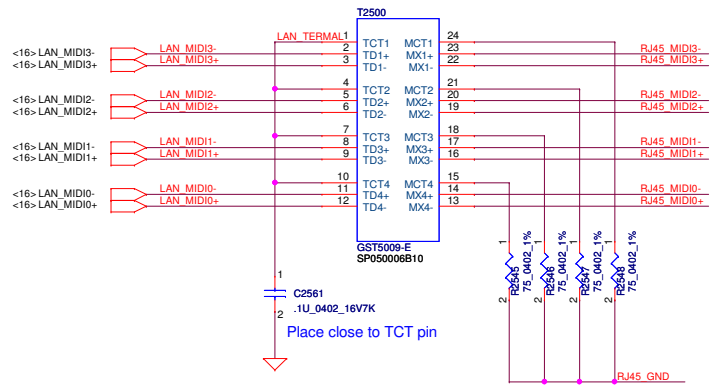


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Date:	Friday, March 28, 2014	Sheet	15	of 34

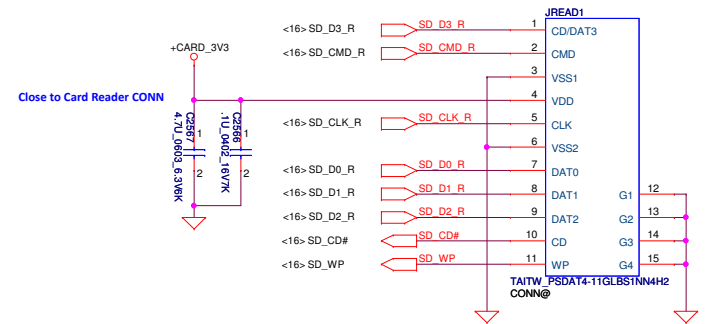




## LAN Connector



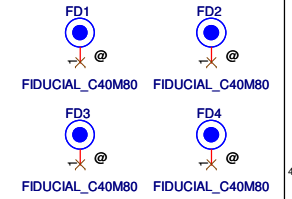
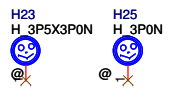
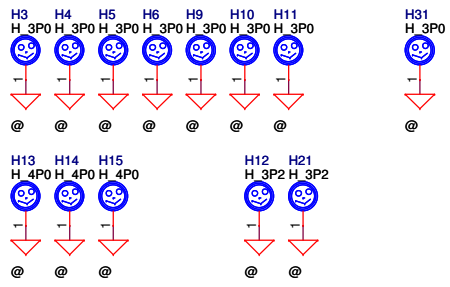
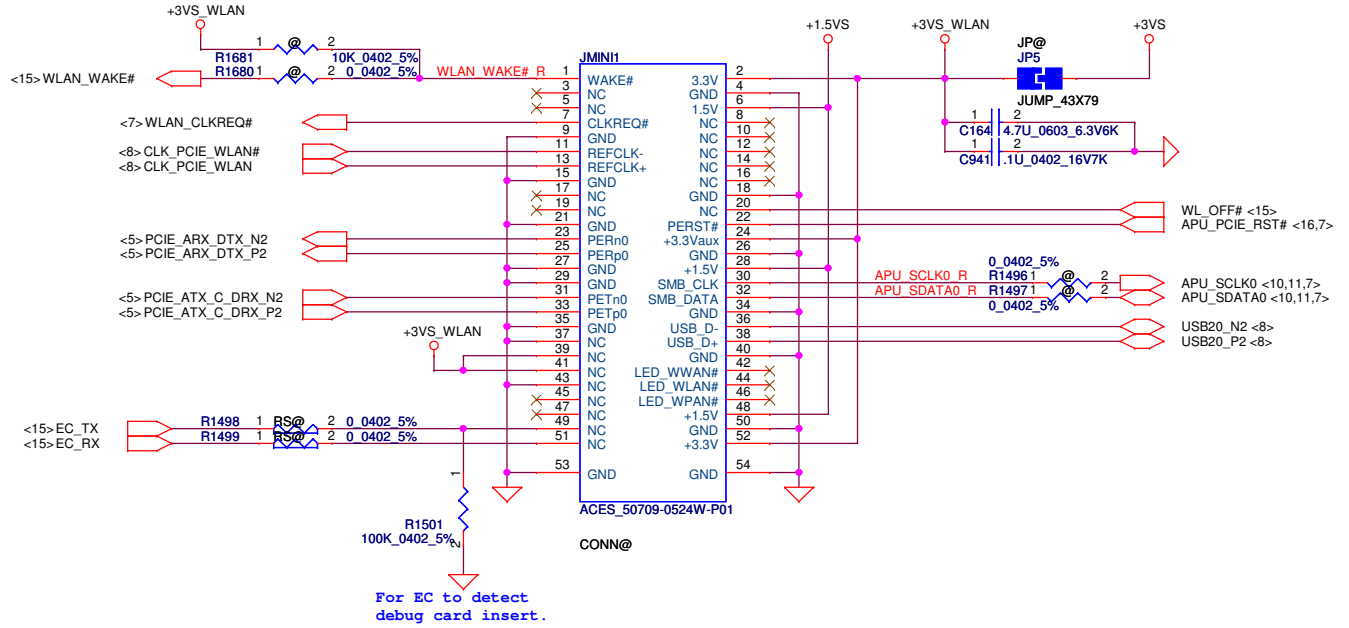
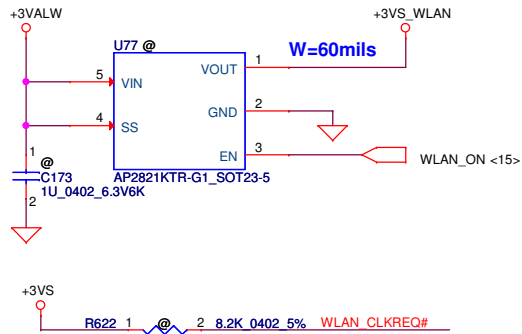
## Card Reader Connector



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Issued Date	2014/03/27	Deciphered Date	2016/03/27	LAN RJ45/CR SD Connector	
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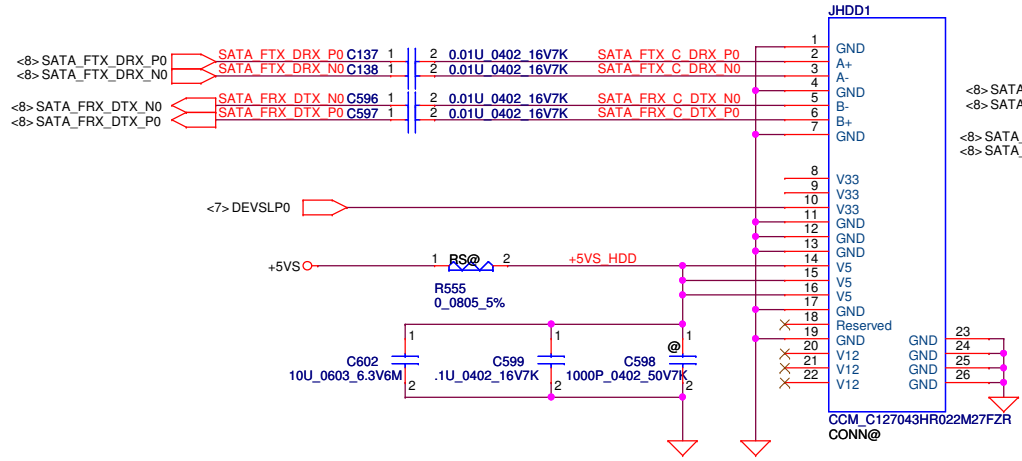


# Mini-Express Card(WLAN/WiMAX) H=4mm

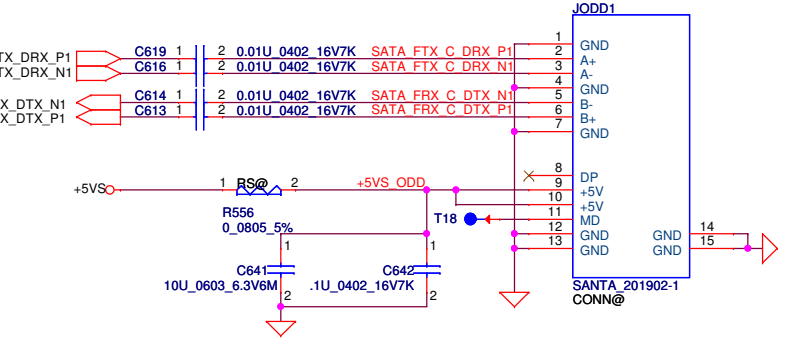


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				Document Number	Rev
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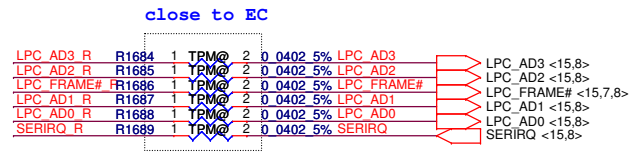
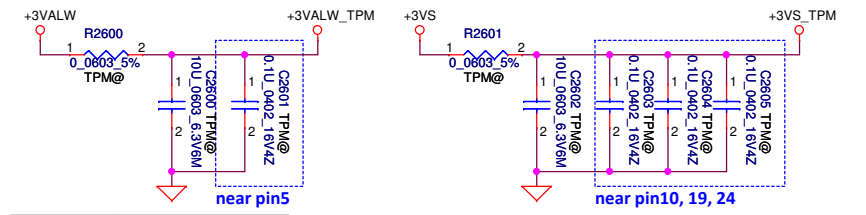
# SATA HDD Conn.



# SATA ODD Conn.



# TPM

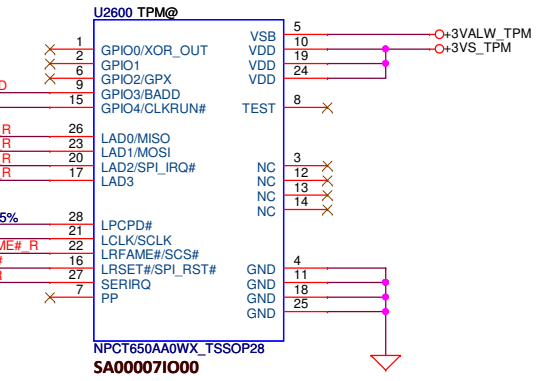


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

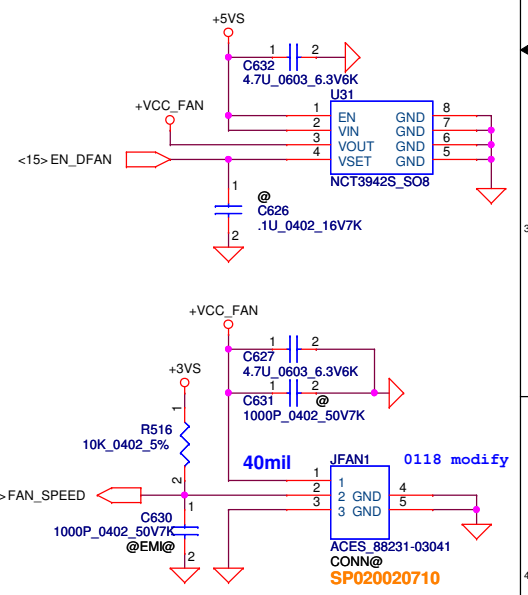
GPIO3/BADD with Internal PH (default)  
 AMD CLKRUN# no need PH (DG1.1)

LPCPD# had internal PH  
 SERIRQ no need PH

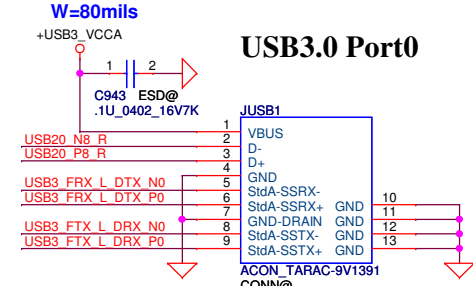
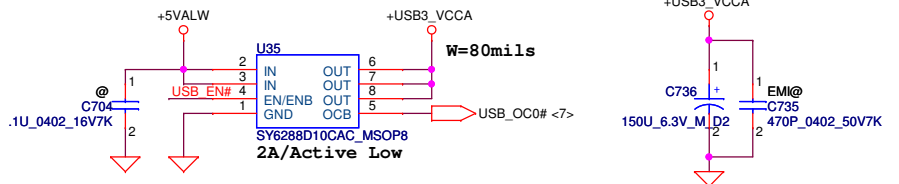
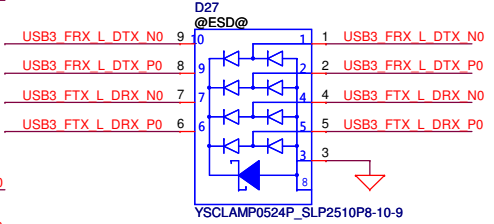
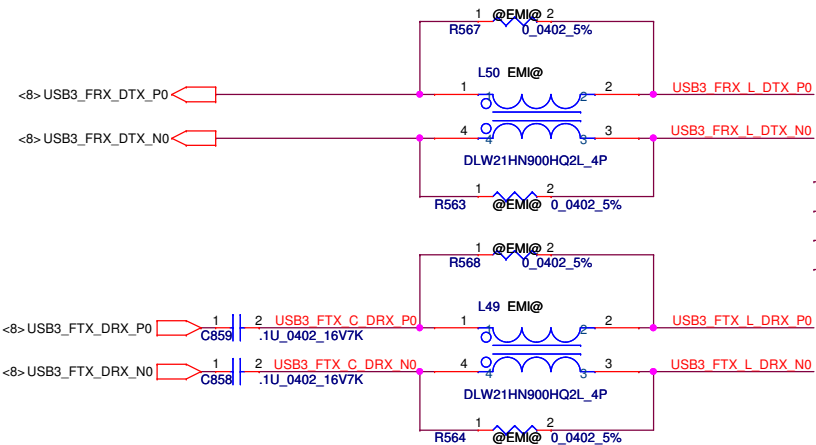
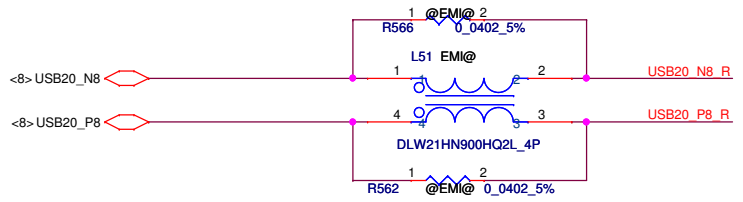
CLKRUN# PH request by TPM chip DG 1/22



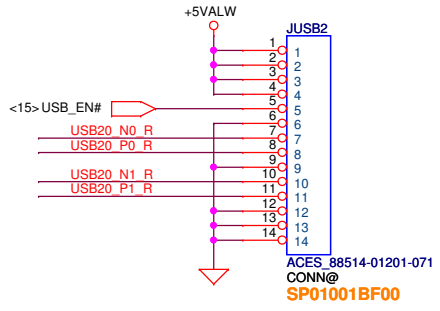
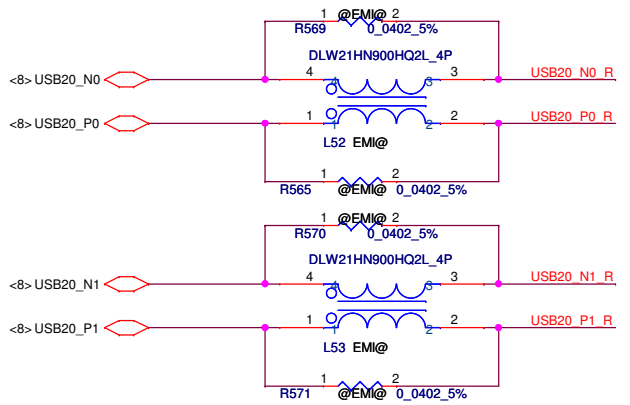
# FAN Conn



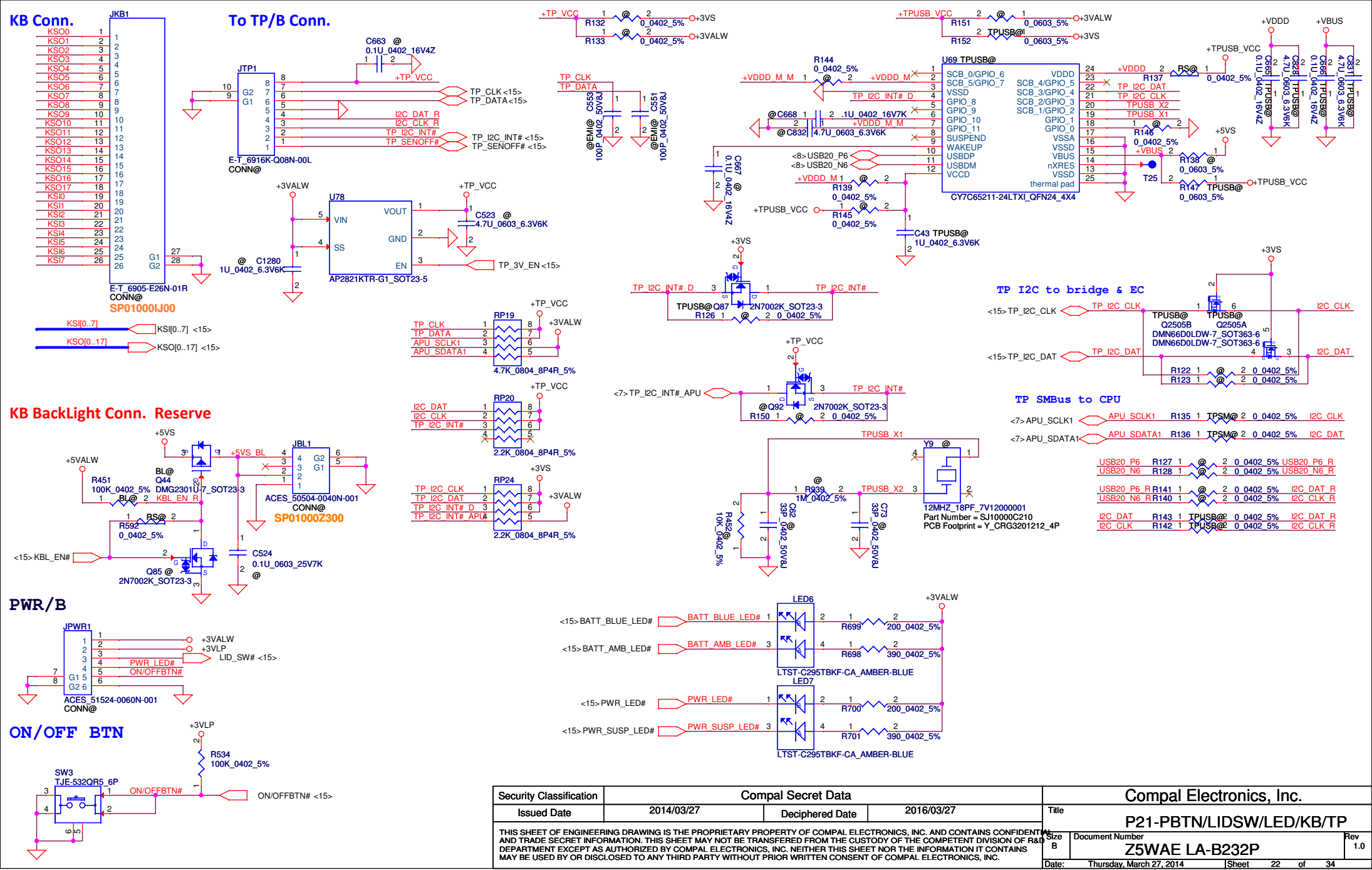
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**USB/B(USB Port 0, Port1)**



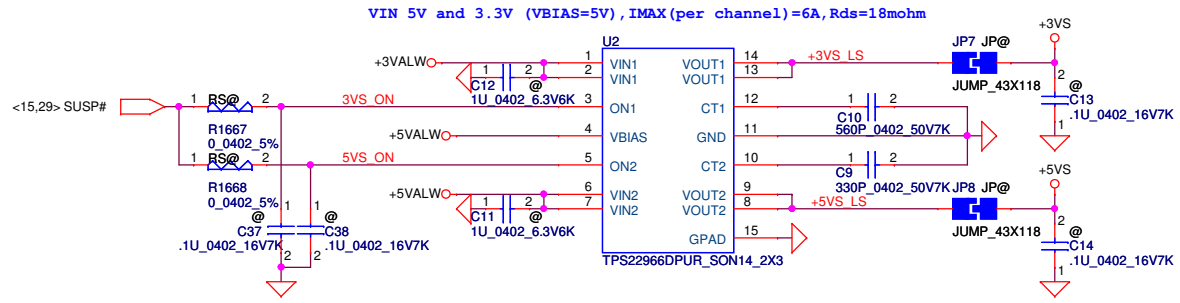
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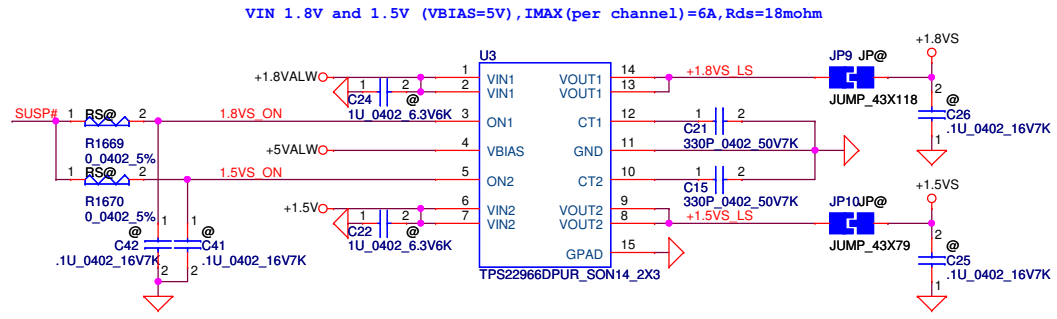
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Title		Compal Electronics, Inc.	
Document Number		P21-PBTN/LIDSW/LED/KB/TP	
Date		Z5WAE LA-B232P	
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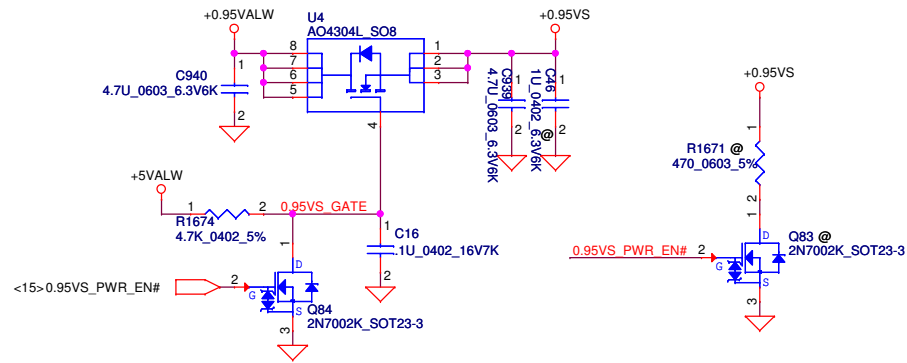
**+5VALW TO +5VS**  
**+3VALW TO +3VS**  
**Load switch**



**+1.8VALW TO +1.8VS**  
**+1.5V TO +1.5VS**  
**Load switch**



**+0.95VALW to +0.95VS**



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**0.1**

1. Add R139 for colay CY7C65211 and MA723C
2. Change Y3 to SJ100001K00
3. Change Q9 to MESS138
4. Reserve C607 pad for ESD request
5. Swap D10.2, D10.3 and change D10.3 to RING2
6. Delete L22, C950, C203
7. Change R404, R73 connect to +0.95VS
8. Connect R139 to U69.2
9. Change R452 to 10K
10. Change C43 to 4.7U
11. Change C43 to 1U
12. Add T18, T24, T25
13. Chagne U2 and U3 P/N to SA00006FD00
14. Change U2 and U3 P/N to SA00004MM00
15. Unpop Q2505,Q87, RP24; Pop R122,R123,R134,R1683

**0.2**

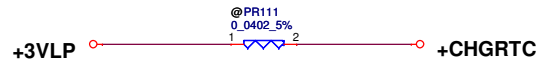
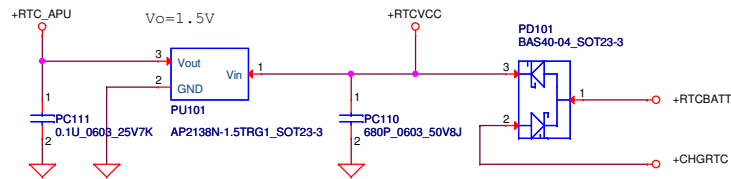
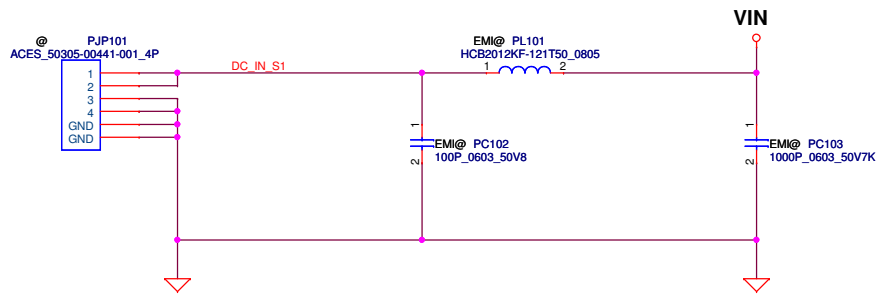
1. Change R119 to Rshort
2. Add U23,U24,Q2506,D20 and D21 for D-sub
3. Change U69 power to +3VALW and +5VALW; modify Q2505 body diode issue.
4. Add L52,L53,R565,R569,R570 and R571 for EMI request.
5. Add R127,R128,R140,R141,R142,R143 for reserve USB TP
6. Add R209 to prevent EC out of control
7. Change LAN\_WAKE# PU to +3V\_LAN
8. Change BID to 1 for DVT
9. Change C99,C100 to 10p for crystal test
10. Change R238 and R237 to 59ohm
11. Add L76,L77,C2142 and C2140 for ESD request
12. Change R756,R765,R769,R779,R781,R782,R783 and R794 to Rshort for EMI request
13. Pop Q89, unpop R1690
14. Change D10 to SCA00001B00
15. Add C609 for ESD request
16. Change L11 to SM01000EJ00
17. Add C668 and C832 for vendor request
18. Remove APU\_ALERT#\_R
19. Add H12,remove H30,swap H21 and H31

**0.3**

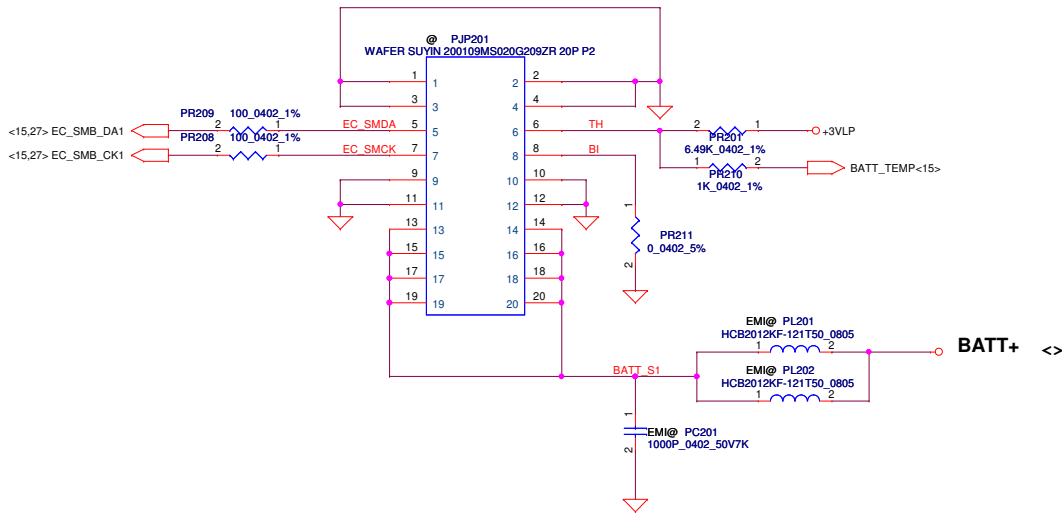
1. Change JTP1
2. Add U78 for TP +3V power plane
3. Change C736 to 150u D2 type.
4. Change R699, R700 to 330ohm; R698, R701 to 560ohm
5. Change U69 +3VALW to +3VS
6. Add C366, C367, C368, C369 for EMI request
7. Add on board TPM
8. Add R619

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---Battery\_pin define---

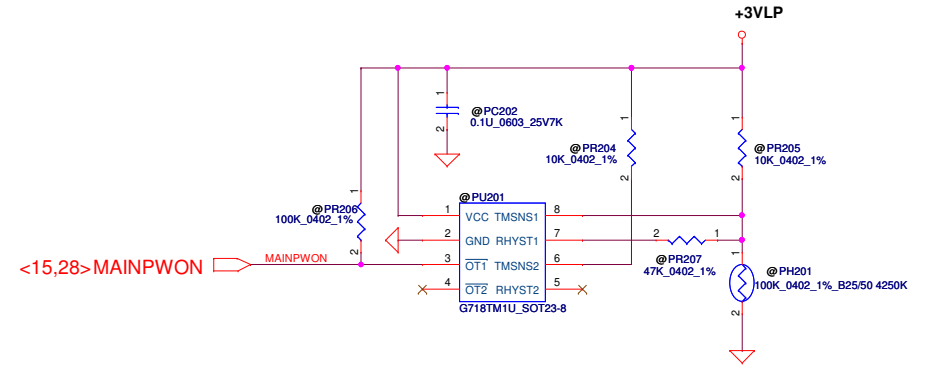
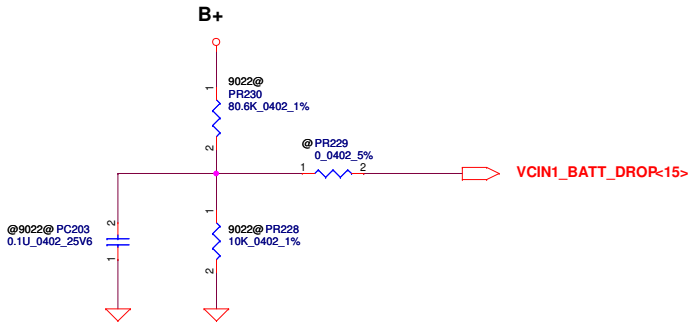
PIN1 GND  
 PIN2 GND  
 PIN3 SMD  
 PIN4 SMC  
 PIN5 TS  
 PIN6 B/I  
 PIN7 Batt+  
 PIN8 Batt+

---Battery Con\_pin define---

PIN8 GND  
 PIN7 GND  
 PIN6 SMD  
 PIN5 SMC  
 PIN4 TS  
 PIN3 B/I  
 PIN2 Batt+  
 PIN1 Batt+

**2013/10/02**  
 Add for ENE9022 Battery Voltage drop detection.  
 Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.  
 B+=9V



	For KB9012 OTP	For KB9022 OTP
92°C		1.0V
56°C		2.0V
PR216		16.9K ohm

**2014/01/02 update**

For KB9022 sense 20mΩ	Active	Recovery
40W	43W, 0.73V	34.4W, 0.59V

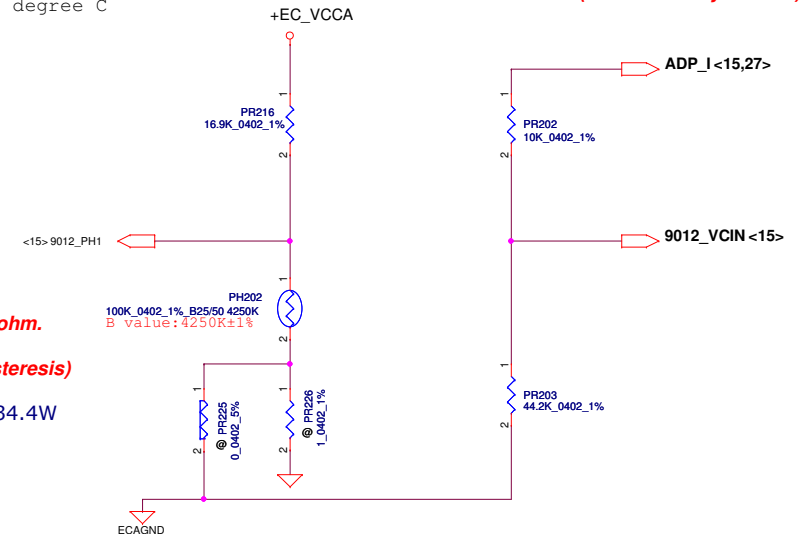
**2013/10/22 Modify**  
 PH201, PH202 change to common part.

**2013/12/16 Modify**  
 Delete PR223.(remove HW hysteresis)

PH201 under CPU bottom side :  
 CPU thermal protection at 92 degree C ( shutdown )  
 Recovery at 56 degree C

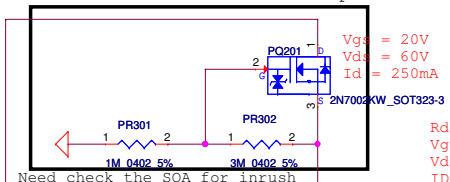
**2013/10/25 Modify**  
 PR227(9012@) change to 26.1K ohm.  
**2014/02/07 Modify**  
 Delete @PR227.(remove HW hysteresis)

For 40W adapter==>action 43W , Recovery 34.4W



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				<b>BATTERY CONN / OTP</b>	
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Protection for reverse input

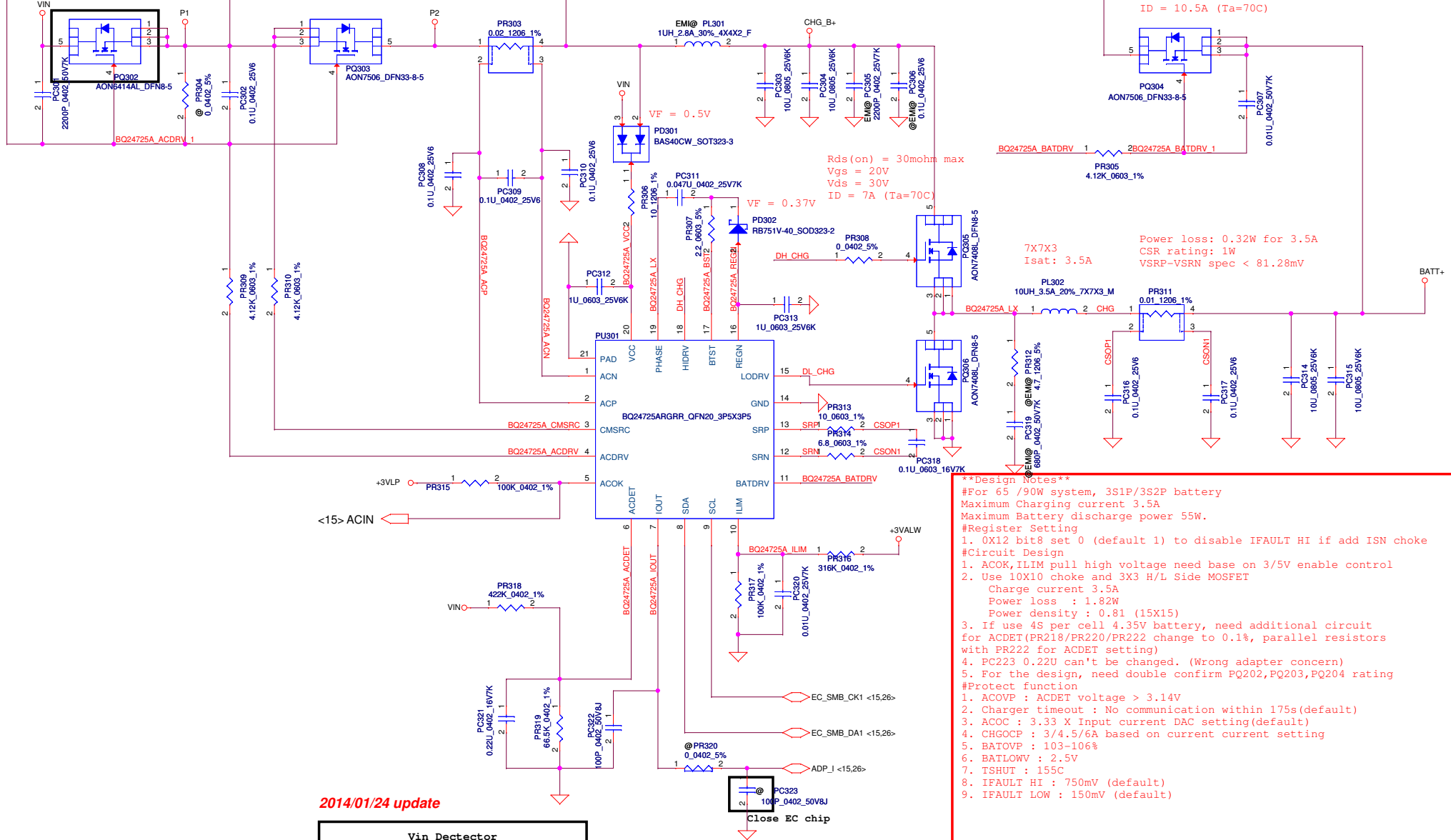


2013/10/14  
PR303 10m ohm chang -->20m ohm  
SD0000S120

Rds(on) = 15.8mohm max  
Vgs = 20V  
Vds = 30V  
ID = 10.5A (Ta=70C)

2013/10/16 Modify  
PQ305,PQ306 change to AON7408L.  
2013/10/22 Modify  
PL302 change to common part.  
2013/11/29 Modify  
PL301 change to common part.

Rds(on) = 15.8mohm max  
Vgs = 20V  
Vds = 30V  
ID = 10.5A (Ta=70C)



**\*\*Design Notes\*\***

#For 65 /90W system, 3S1P/3S2P battery  
Maximum Charging current 3.5A  
Maximum Battery discharge power 55W.

#Register Setting  
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke

#Circuit Design  
1. ACOK,ILIM pull high voltage need base on 3/5V enable control  
2. Use 10X10 choke and 3X3 H/L Side MOSFET  
Charge current 3.5A  
Power loss : 1.82W  
Power density : 0.81 (15X15)

3. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)

4. PC223 0.22U can't be changed. (Wrong adapter concern)

5. For the design, need double confirm PQ202,PQ203,PQ204 rating

#Protect function  
1. ACOVP : ACDET voltage > 3.14V  
2. Charger timeout : No communication within 175s(default)  
3. ACOC : 3.33 X Input current DAC setting(default)  
4. CHGOCP : 3/4.5/6A based on current current setting  
5. BATOVP : 103-106%  
6. BATLOWV : 2.5V  
7. TSHUT : 155C  
8. IFAULT HI : 750mV (default)  
9. IFAULT LOW : 150mV (default)

2014/01/24 update

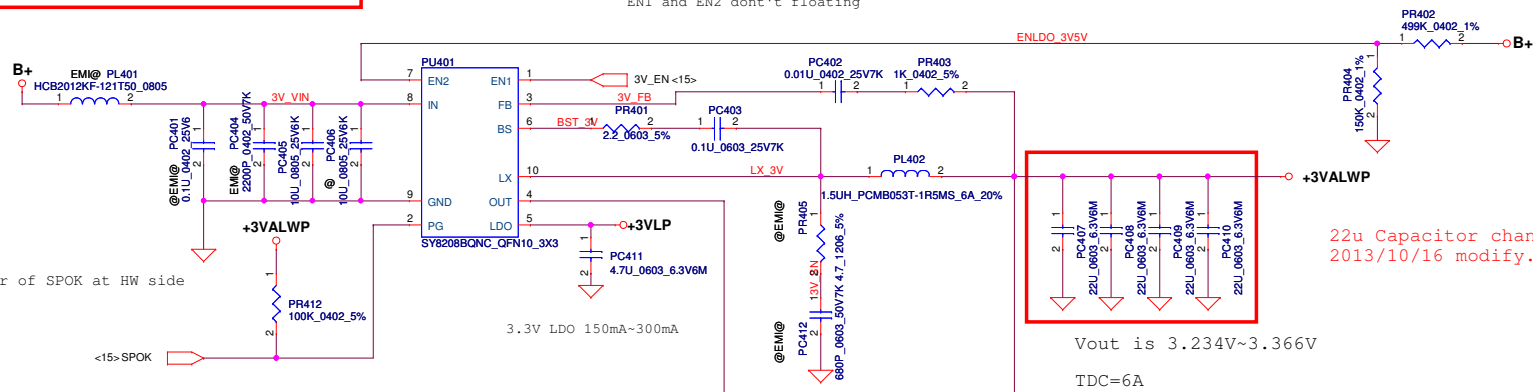
Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20\*ILIM\*Rsr  
ILIM = 3.3\*100/(100+316)/20/0.01  
= 3.966 A

Module model information

SY8208B\_V2.mdd  
SY8208C\_V2.mdd

EN1 and EN2 dont't floating

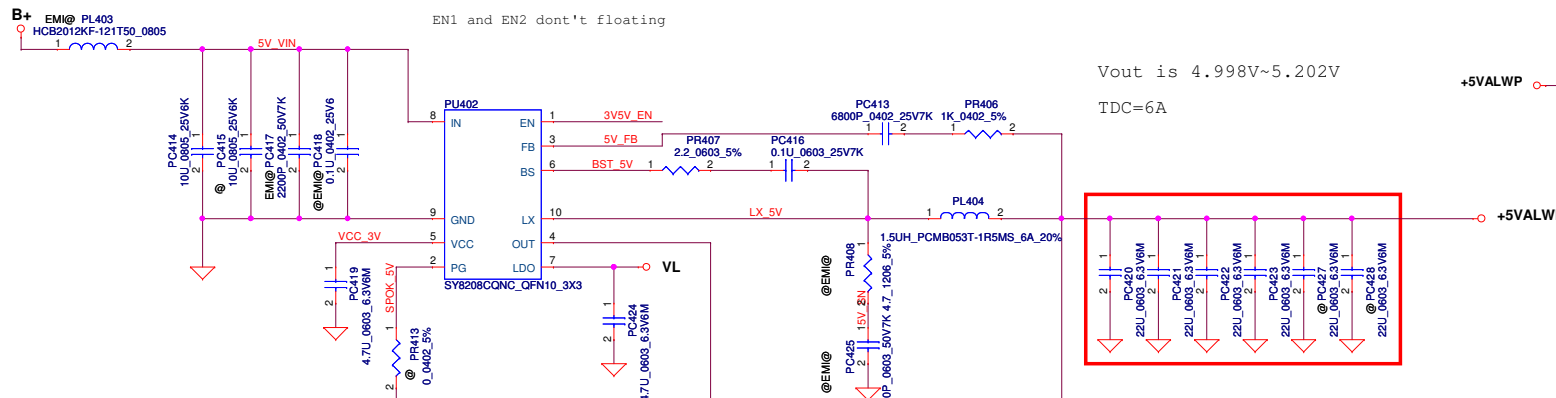


22u Capacitor change to 0603 size.  
2013/10/16 modify.

Vout is 3.234V~3.366V  
TDC=6A



EN1 and EN2 dont't floating



Vout is 4.998V~5.202V  
TDC=6A

22u Capacitor change to 0603 size.  
2013/10/16 modify.  
reserve PC427, PC428 for IC Application.  
2013/11/29 modify.

Add non-pop PR413 for Test.  
2013/11/04 modify.

Check pull up resistor of SPOK at HW side

<15>-SPOK

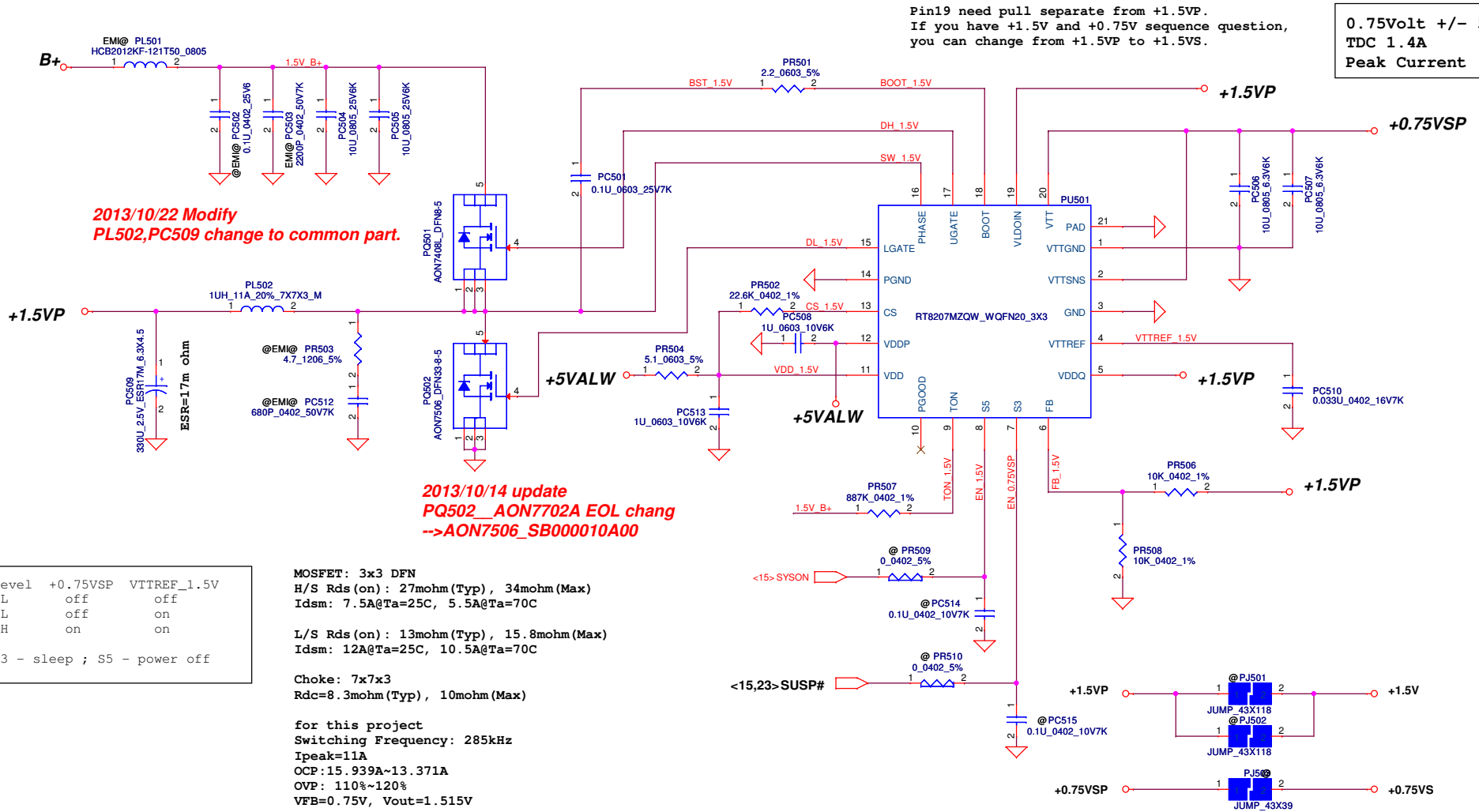
<15>EC\_ON  
<15,26> MAINPWON

EC VDD0 is +3VL, PC13 UNPOP  
EC VDD0 is +3VALW, PC13 POP

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Module model information

RT8207M\_v1.mdd For Single layer  
RT8207M\_v2.mdd For Dual layer



Pin19 need pull separate from +1.5VP.  
If you have +1.5V and +0.75V sequence question,  
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%  
TDC 1.4A  
Peak Current 2A

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN  
H/S Rds (on): 27mohm (Typ), 34mohm (Max)  
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on): 13mohm (Typ), 15.8mohm (Max)  
Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3  
Rdc=8.3mohm (Typ), 10mohm (Max)

for this project  
Switching Frequency: 285kHz  
Ipeak=11A  
OCP: 15.939A~13.371A  
OVP: 110%~120%  
VFB=0.75V, Vout=1.515V

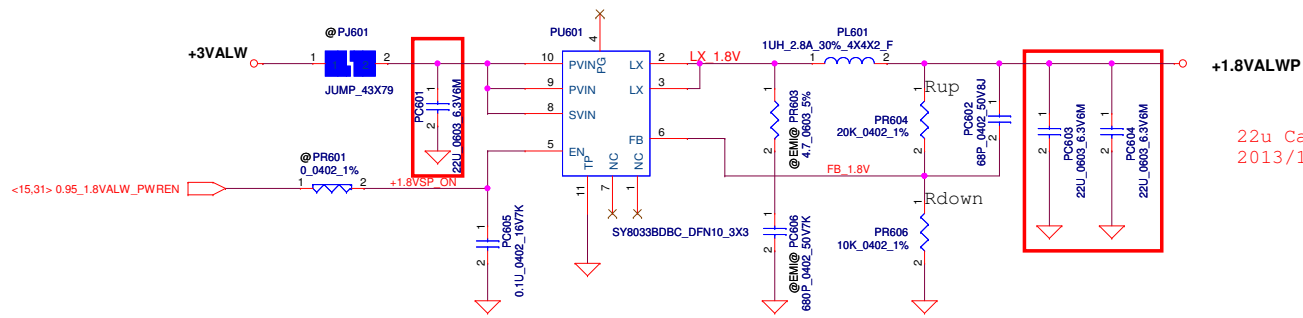
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Module model information  
SY8033\_V1.mdd

22u Capacitor change to 0603 size.  
2013/10/16 modify.

2013/10/22 Modify  
PL601 change to common part.

FB=0.6V  
Note: Iload (max)=3.5A

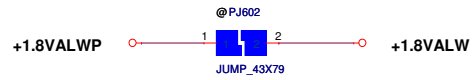


22u Capacitor change to 0603 size.  
2013/10/16 modify.

Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

Delete PR605, because same net name have two PD resister in circuit.  
2013/11/29 modify.

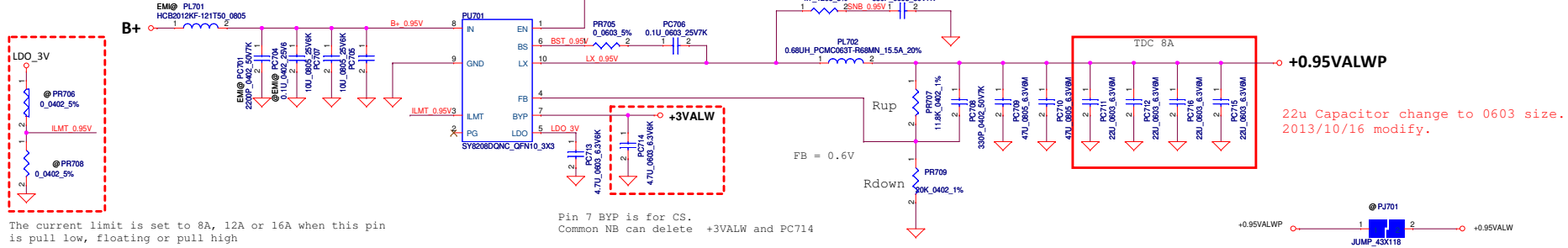


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Module model information  
SY8208D\_V1.mdd

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2

for this project  
Ipeak=8A  
Add 22u\*2 capacitor,  
Chock change to 0.68u.  
meet DC-DC design check form.  
2013/10/02 Modify.



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.  
Common NB can delete +3VALW and PC714

22u Capacitor change to 0603 size.  
2013/10/16 modify.

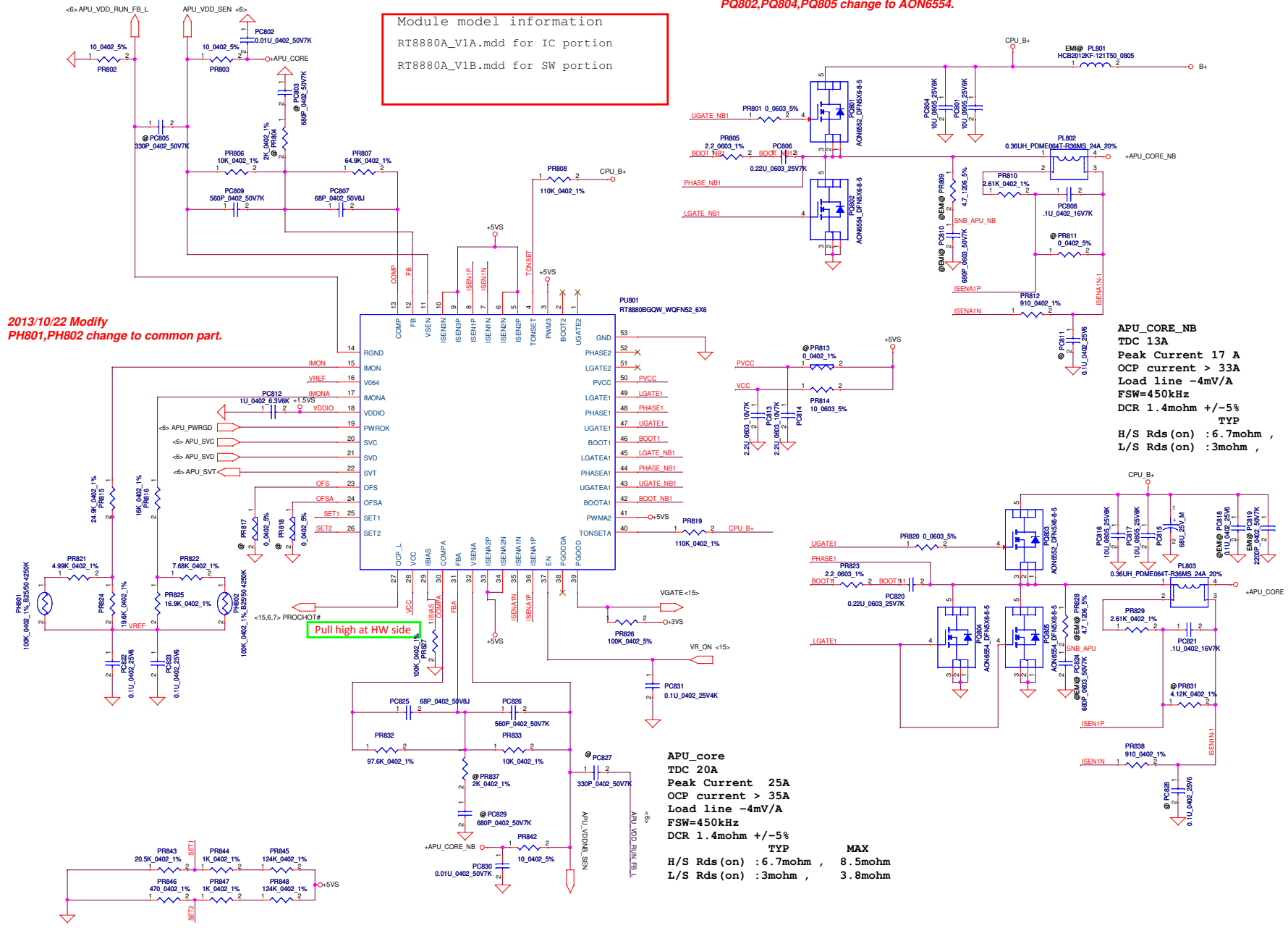
VFB=0.6V  
Vout=0.6V\* (1+Rup/Rdown)  
Vout=0.954V

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2013/10/16 Modify  
 PQ801,PQ803 change to AON6552.  
 PQ802,PQ804,PQ805 change to AON6554.

Module model information  
 RT8880A\_V1A.mdd for IC portion  
 RT8880A\_V1B.mdd for SW portion

2013/10/22 Modify  
 PH801,PH802 change to common part.



**APU\_CORE\_NB**  
 TDC 13A  
 Peak Current 17 A  
 OCP current > 33A  
 Load line -4mV/A  
 FSW=450kHz  
 DCR 1.4mohm +/-5%  
 TYP  
 H/S Rds (on) : 6.7mohm , 8.5mohm  
 L/S Rds (on) : 3mohm , 3.8mohm

**APU\_core**  
 TDC 20A  
 Peak Current 25A  
 OCP current > 35A  
 Load line -4mV/A  
 FSW=450kHz  
 DCR 1.4mohm +/-5%  
 TYP  
 H/S Rds (on) : 6.7mohm , 8.5mohm  
 L/S Rds (on) : 3mohm , 3.8mohm

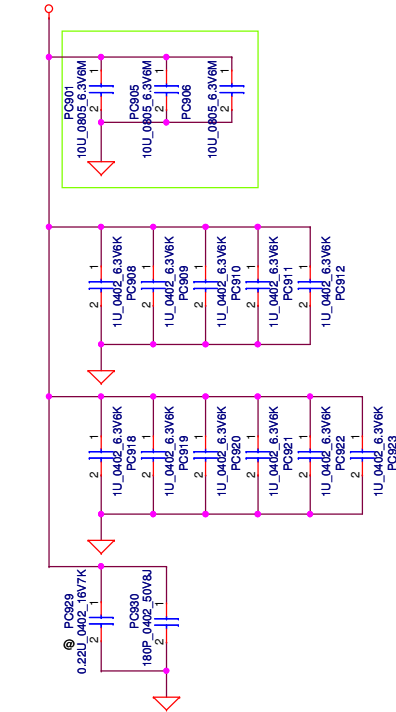
Delete PR834.PR835.PR836.PR839.PR840.PR841,  
 follow vender FAE suggest.  
 2013/11/29 modify.

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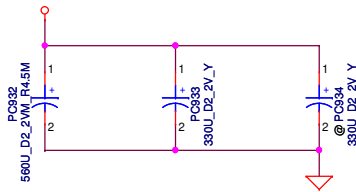


**+APU\_CORE (36.4)**

**+APU\_CORE**

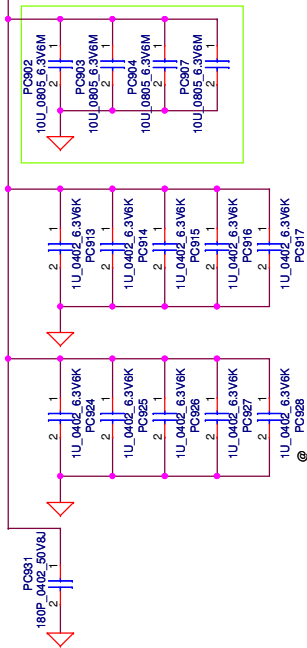


**+APU\_CORE**

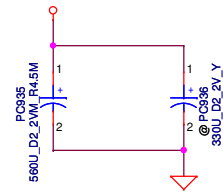


**+APU\_CORE\_NB (36.5)**

**+APU\_CORE\_NB**



**+APU\_CORE\_NB**



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design Change.	Design Change of Diode Application.	0.2	25	Change PD101 to SCS4004010(S SCH DIO BAS40-04 SOT23).	2013/11/29	DVT
2	Design Change.	Design Change of IC Application.	0.2	28	Add non-pop component PC427,PC428.	2013/11/29	DVT
3	Design Change.	reduce part count.	0.2	30	Delete PR605 PD resister.	2013/11/29	DVT
4	Design Change.	reduce part count.	0.2	32	Delete @PR834.@PR835.@PR836.@PR839.@PR840.@PR841.	2013/11/29	DVT
5	Design Change.	Design Change of common part.	0.2	27	Change PL301 to SH00000YG00 (S COIL 1UH +-30% 2.8A 4X4X2 FERRITE).	2013/11/29	DVT
6	Design Change.	Design Change of EC Type Application.	0.2	28	Add PD401 SCS00000200(S SCH DIO RB751V-40 SOD-323)	2013/11/29	DVT
7	Design Change.	Design Change of Circuit Application.	0.2	26	Delete PR223.(remove HW hysteresis)	2013/12/16	DVT
8	Design Change.	Design Change of Circuit Application.	0.2	27	Change PQ303,PQ304 to SB000010A00(S TR AON7506 1N DFN).	2013/12/19	DVT
9	Design Change.	Design Change of Circuit Application.	0.2	26	Add PL202 SM01000C000 (S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2013/12/19	DVT
10	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR211 to SD028000080(S RES 1/16W 0 +-5% 0402).	2013/12/25	DVT
11	Design Change.	Design Change of Circuit Application.	0.2	28	Change PC426 to pop.	2013/12/25	DVT
12	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR216 to SD034162280(S RES 1/16W 16.2K +1% 0402).	2013/12/25	DVT
13	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR216 to SD034169280(S RES 1/16W 16.9K +-1% 0402).	2014/01/02	DVT
14	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR202 to SD034100280(S RES 1/16W 10K +-1% 0402).	2014/01/02	DVT
15	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR203 to SD034442280(S RES 1/16W 44.2K +-1% 0402).	2014/01/02	DVT
16	Design Change.	Design Change of Circuit Application.	0.3	30.31.32	Change PR813,PR601,PR706,PR702, to SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT

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