

MODEL NAME :VAW03

PCB NO : LA-9103P

BOM P/N : DA60000UT00 LA-9103P M/B  
DA40001FO00 LS-9101P POWER BUTTON/B  
DA40001FP00 LS-9102P USB/B  
DA40001FQ00 LS-9103P TP BUTTON/B

*Inspiron Value OAK(Essentials) 15 UMA (Comal Richland)*  
*Inspiron Value OAK(Essentials) 15 Discrete#1 (Comal Richland, AMD Mars Pro)*  
*Inspiron MainStream OAK(Essentials) 15 UMA (Comal Richland)*  
*Inspiron MainStream OAK(Essentials) 15 Discrete#2 (Comal Richland, AMD Mars Pro)*  
*Vostro Value OAK(Essentials) 15 UMA (Comal Richland)*

# Dell / Compal Confidential

## Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH

AMD VGA Sun XT

46@ : for 46 level  
@ : Nopop Component  
CONN@ : Connector Component  
UMA@ : Only for UMA  
DIS@ : Only for Discrete  
GCLK@ : Green CLK implemented  
NGCLK@ : Non Green CLK implemented  
@3221: ALC 3221  
@3223 : ALC 3223  
EMC@ : EMC Parts  
2nd@ : for APL3512 2nd source control  
(RN9, RV32, RL22)

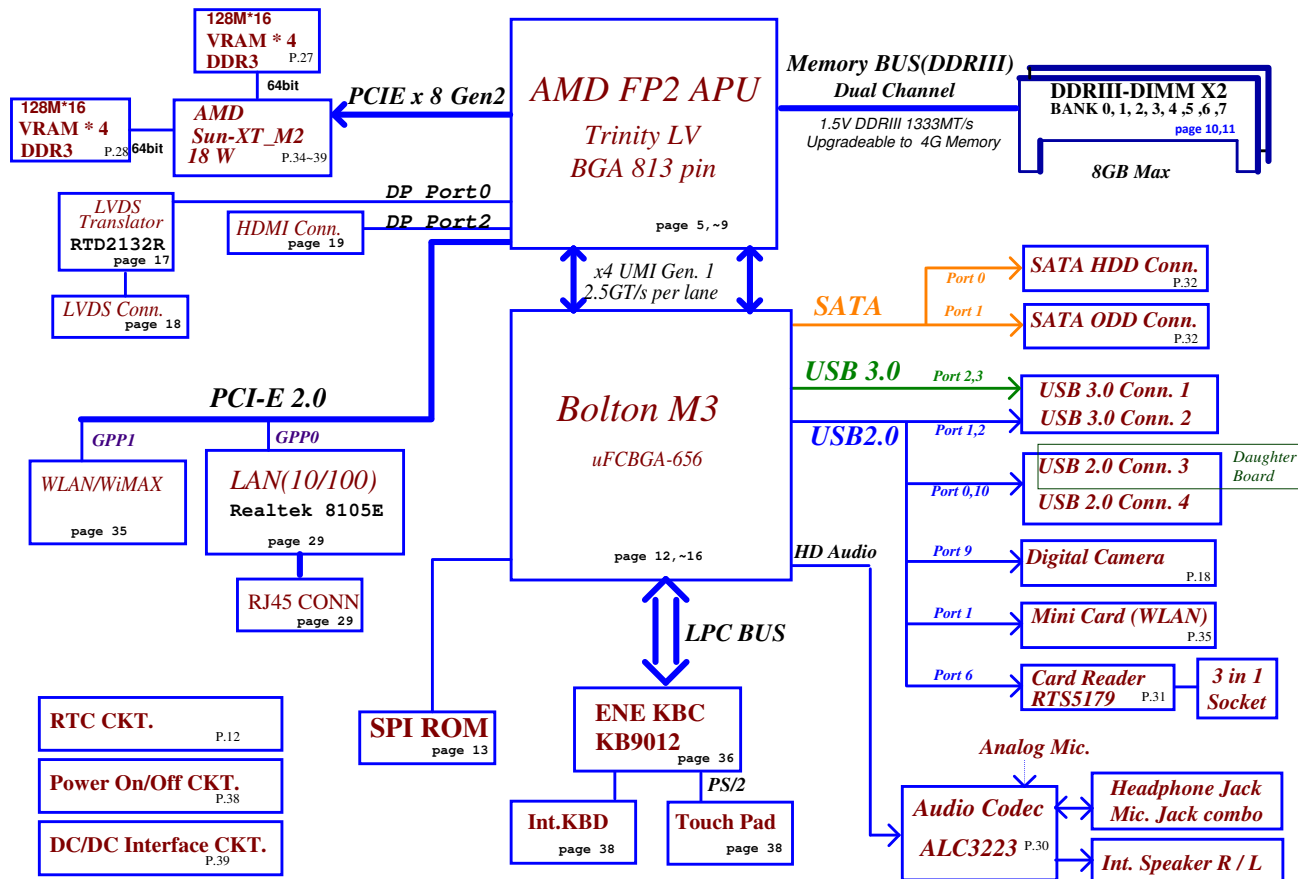
2012-11-26

Rev: 0.2

R1@ : R1 P/N for PCB  
R3@ : R3 P/N for PCB  
THR1@ : Thames-XT R1 P/N  
THR3@ : Thames-XT R3 P/N  
CHR1@ : Chelsea-Pro R1 P/N  
CHR3@ : Chelsea-Pro R3 P/N  
R@ : RTD2132-R  
S@ : RTD2132-S

X76@ : VRAM Group  
CH@ : Chelsea M2  
SE@ : Seymour M2  
TH@ : Thames-XT  
Mars@ : Mars Pro M2  
A4R1@ : A4 APU-R1  
A6R1@ : A6 APU-R1  
A8R1@ : A8 APU-R1  
A8@ : A8 APU Symbol  
Hud@ : HUDSON-M3  
Bol@ : BOLTON-M3

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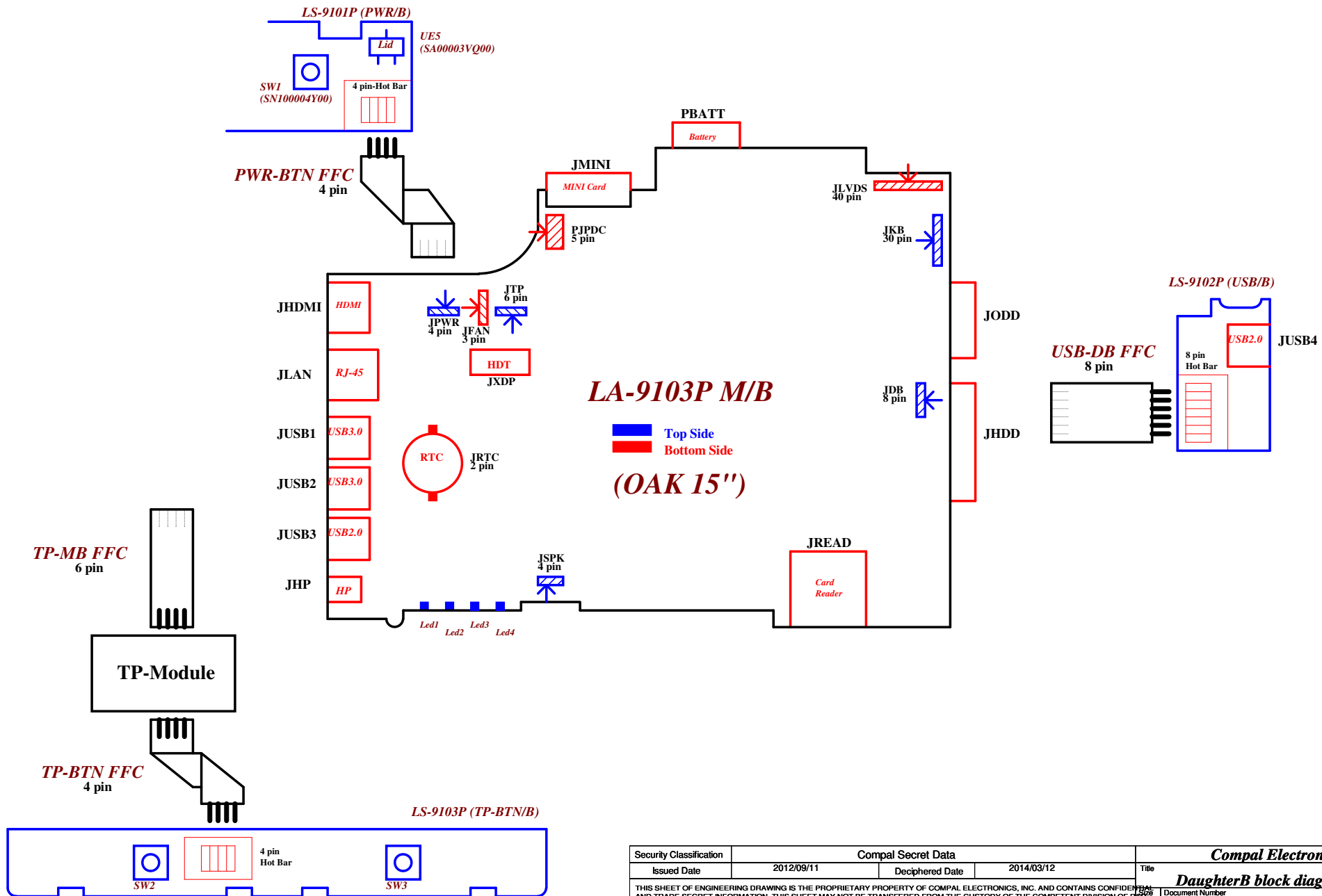


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Size	Document Number	Rev		
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Project Code : VAW03

File Name : LA-9103P



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**Board ID Table for AD channel**

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

**BOARD ID Table**

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB PORT#	DESTINATION
0	USB conn.3 DEBUG PORT
1	MINI CARD (WLAN)
2	USB conn.4
3	NC
4	NC
5	NC
6	Card Reader
7	NC
8	NC
9	Camera
10	USB conn.2
11	NC
12	NC
13	USB conn.1

**EC SM Bus1 address**

**EC SM Bus2 address**

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2132	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

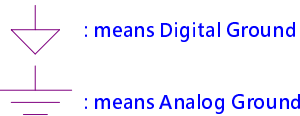
**SM Bus Controller 0** (FCH\_SMB1 ~ FCH\_SMB4, SMB\_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

**SM Bus Controller 1** (FCH\_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

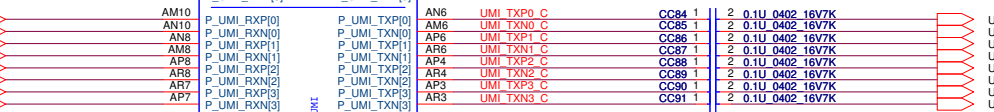
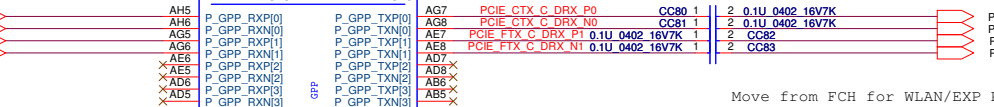
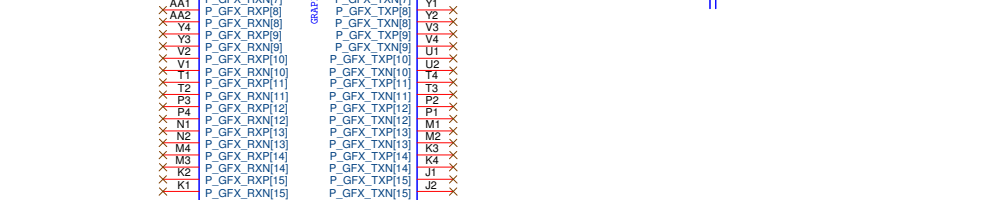
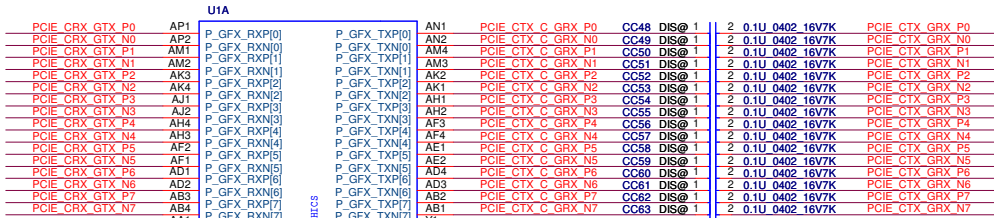
**Symbol Note :**



CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	None
	CLKOUT_PCIE2	10/100 LAN
	CLKOUT_PCIE3	MINI CARD WLAN
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
CLKOUT_PEG_B	None	

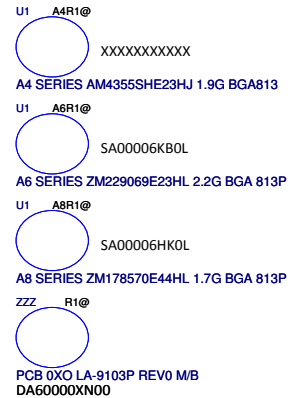
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

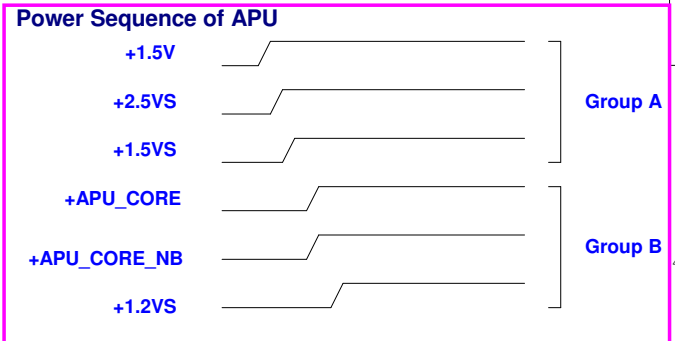


TRINITY-A8-SERIES\_BGA813

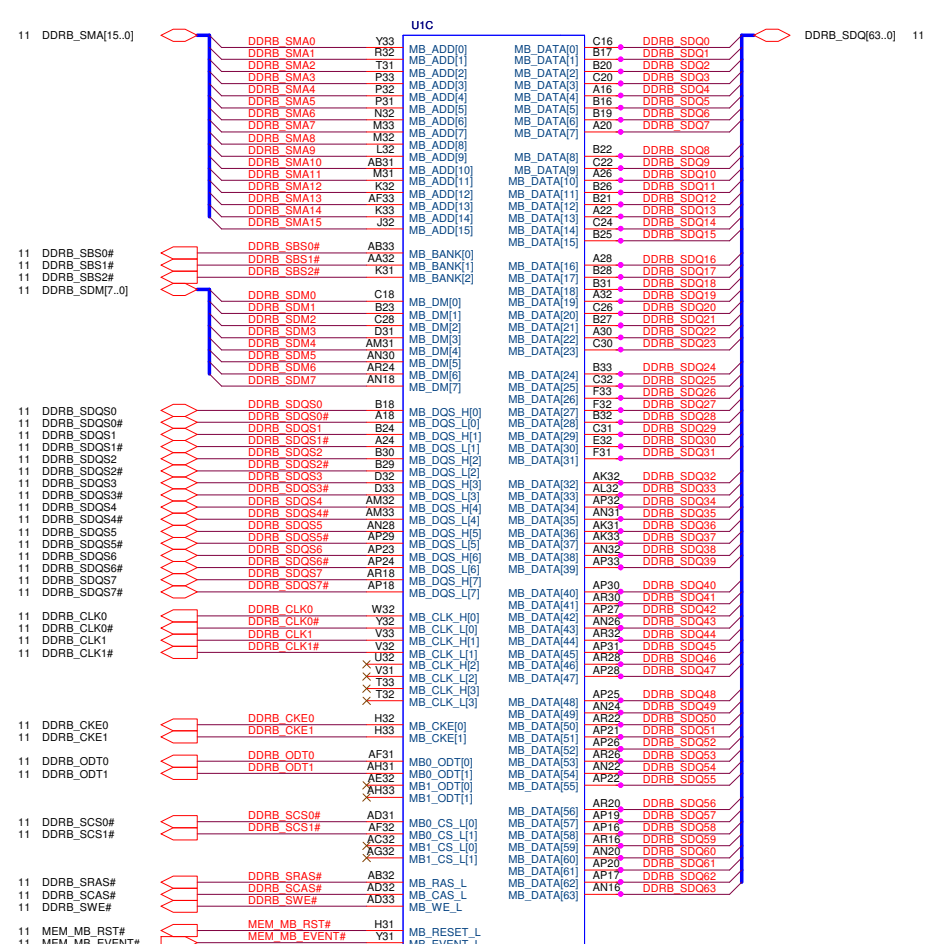
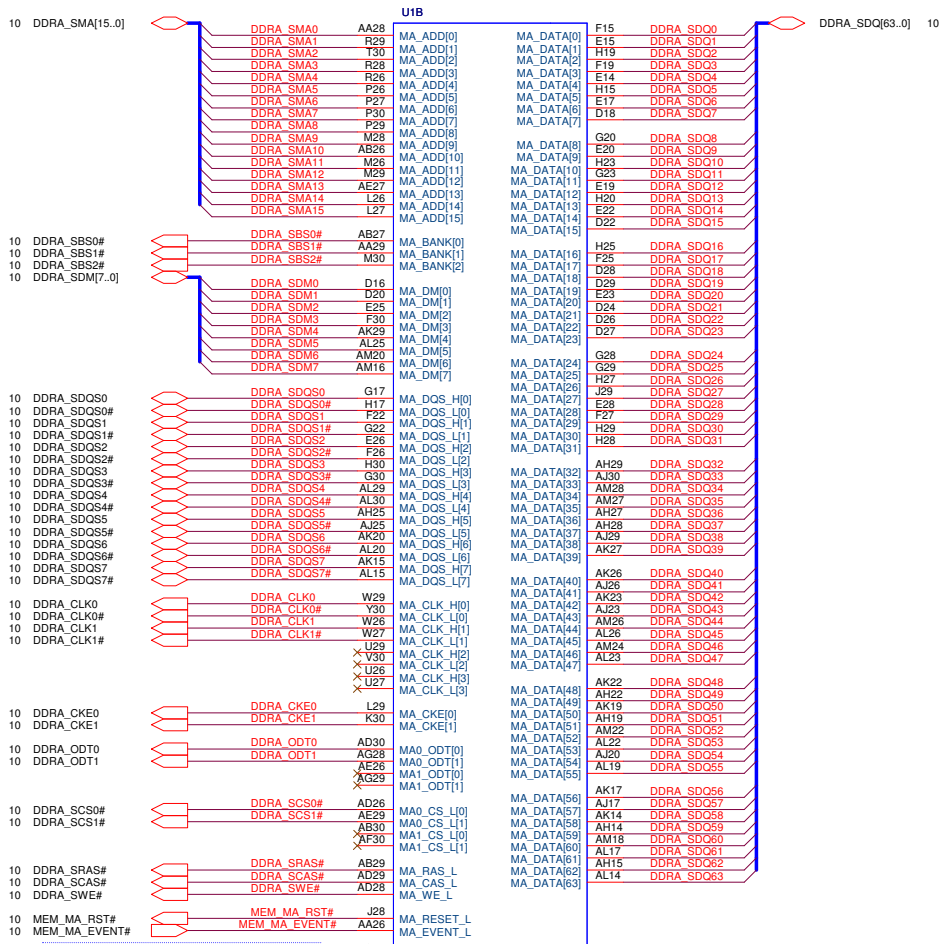
A8@



Move from FCH for WLAN/EXP PCIE I/F. 20110819



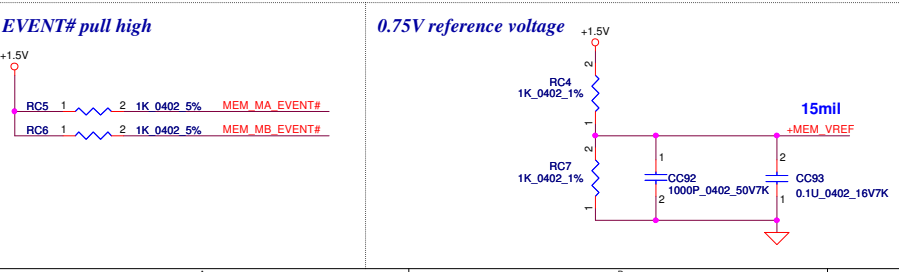
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				FP2 PCIE/UMI
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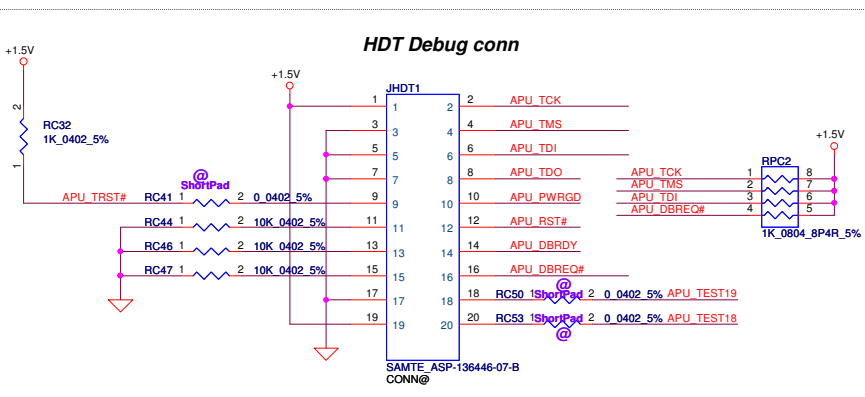
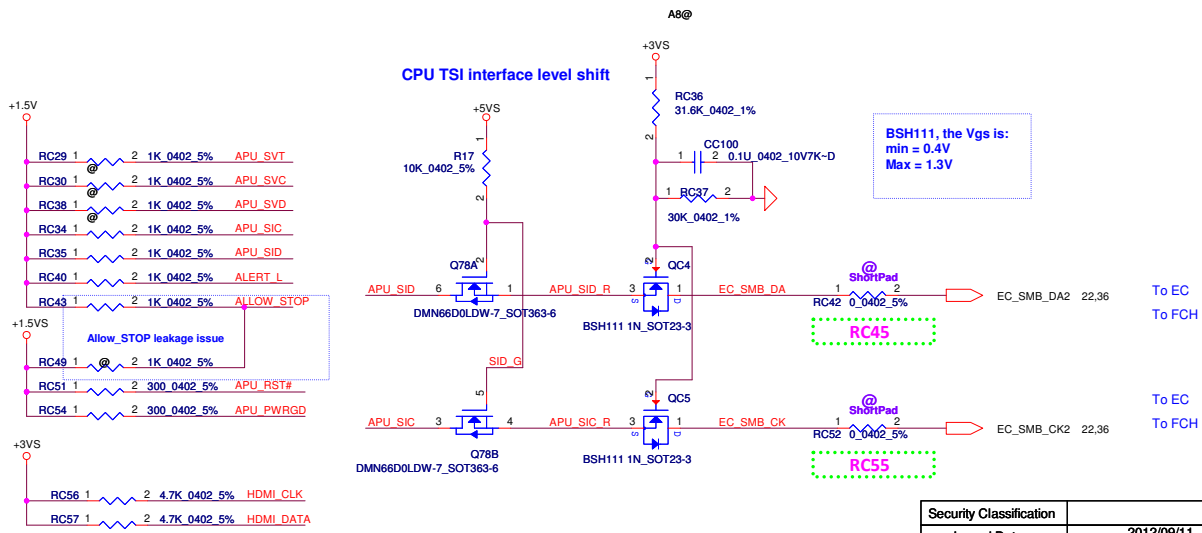
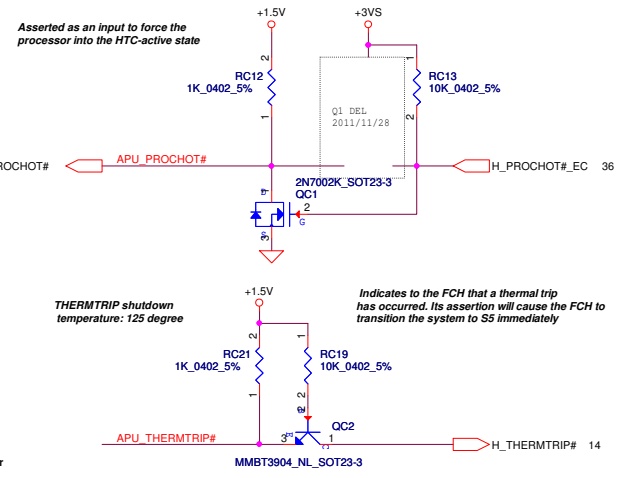
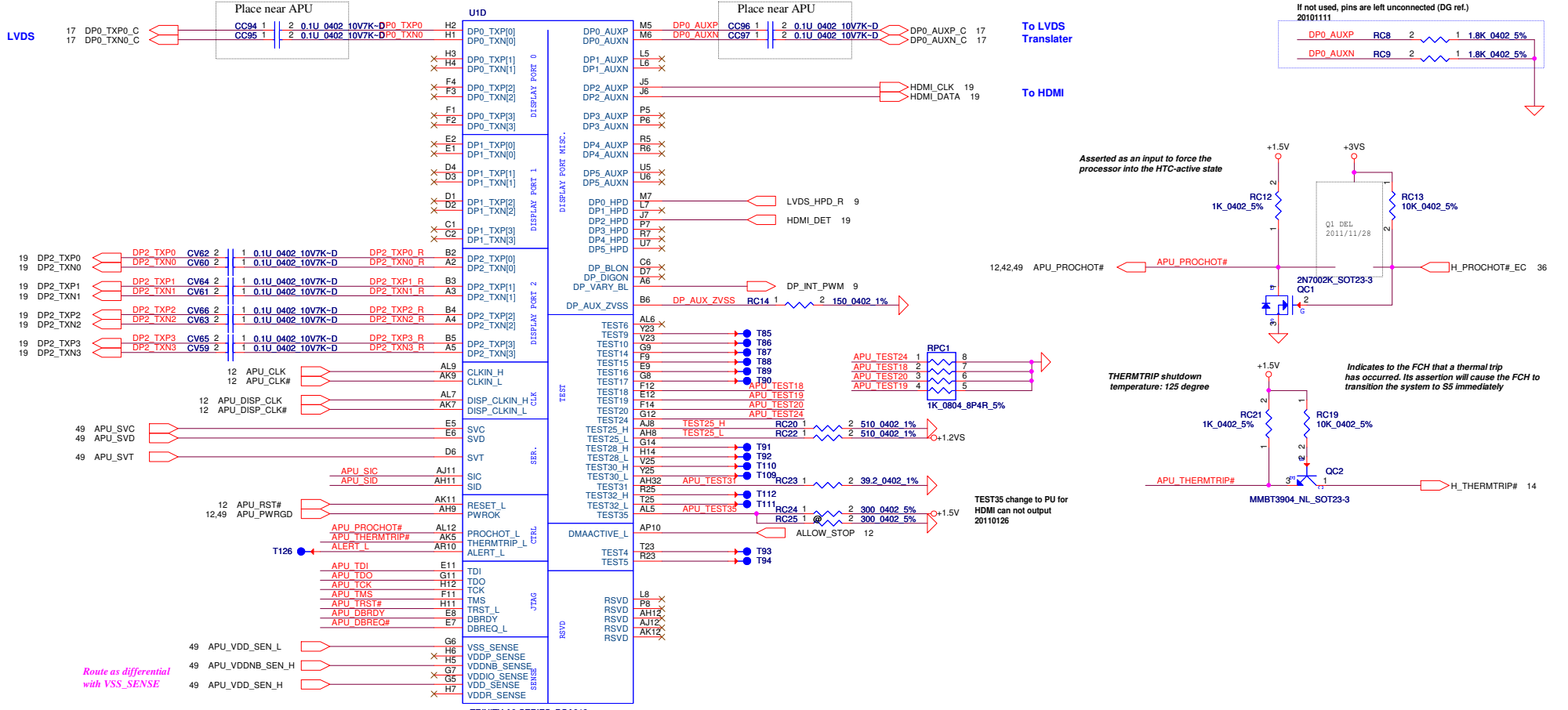
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A8@

A8@



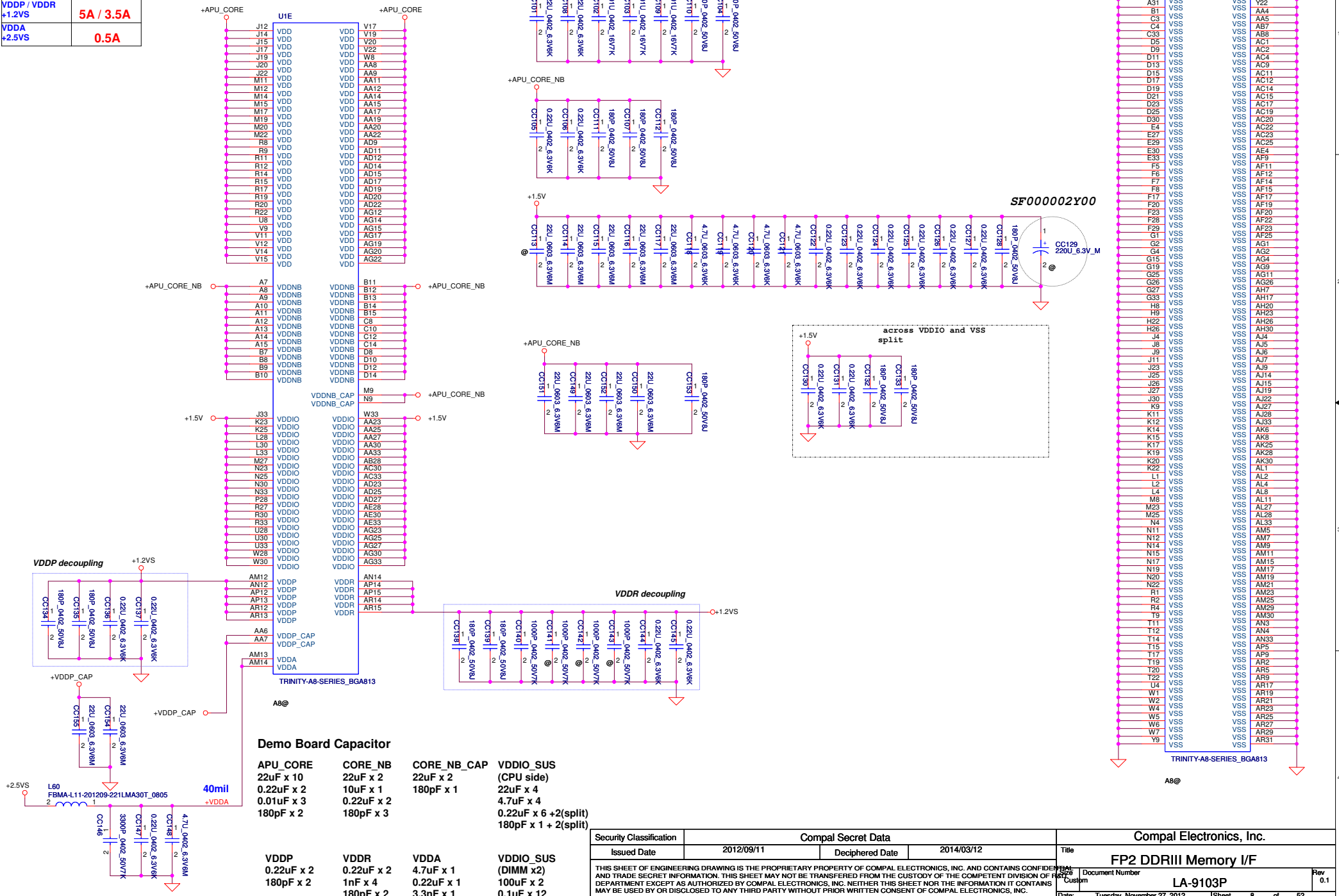
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Aux signal are re-configured as I2C signals for DDC. APU AUX pin are 3.3V tolerant Default follow PAWGX setting for pull-high resistor value

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Power Name	Consumption
VDD	
+APU_CORE	<b>60A</b>
VDDNB	
+APU_CORE_NB	<b>29A</b>
VDDIO	
+1.5V	<b>3.2A</b>
VDDP / VDDR	
+1.2VS	<b>5A / 3.5A</b>
VDDA	
+2.5VS	<b>0.5A</b>



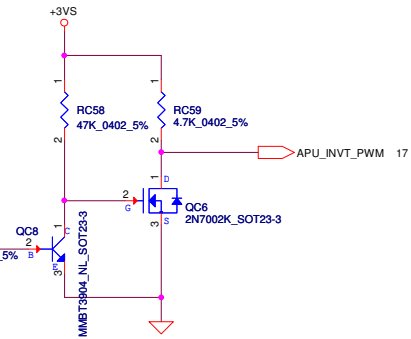
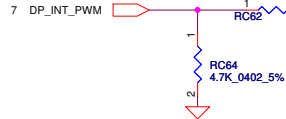
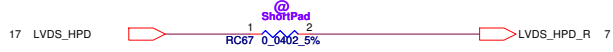
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	FP2 DDRIII Memory I/F
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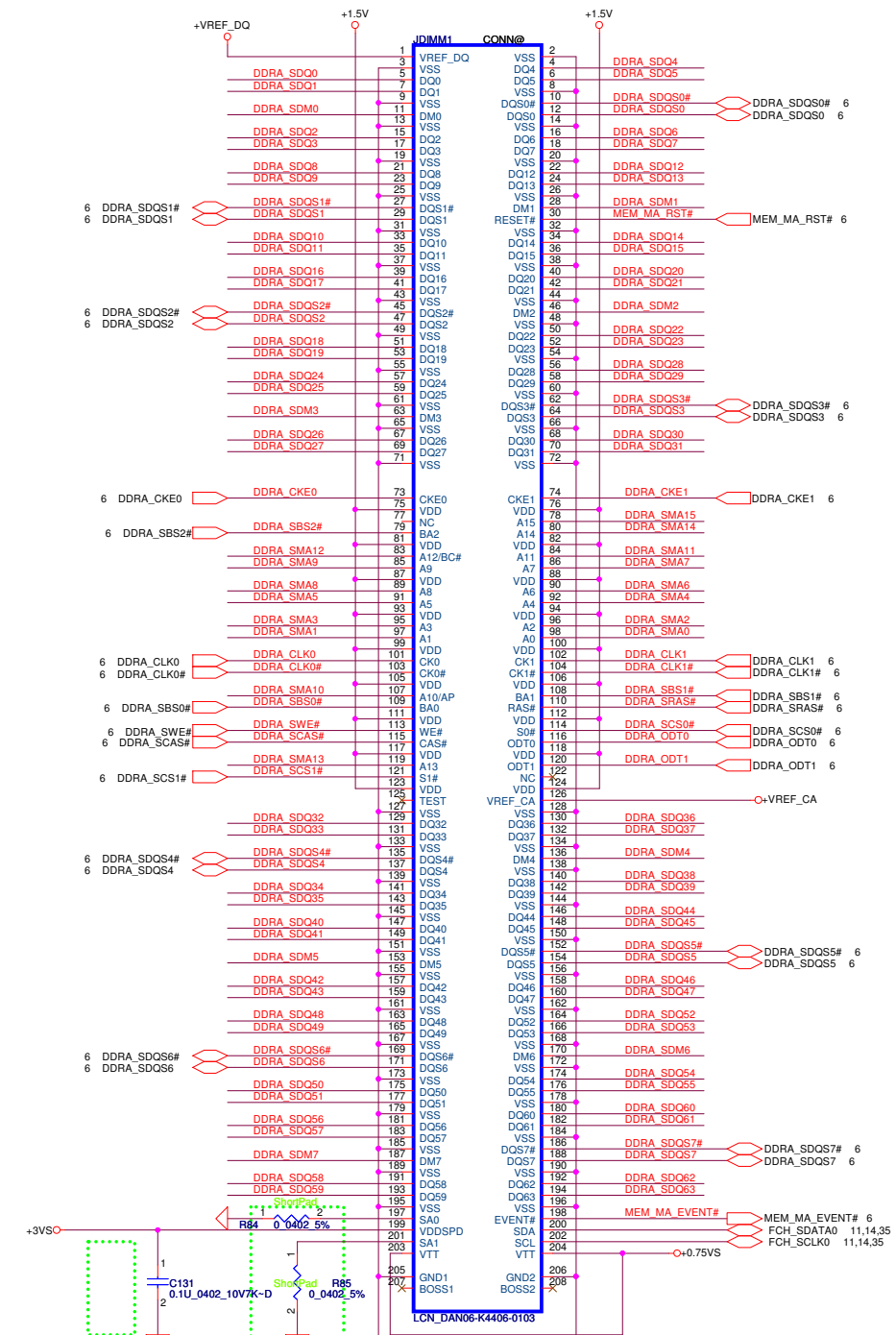
# HPD

# Panel PWM

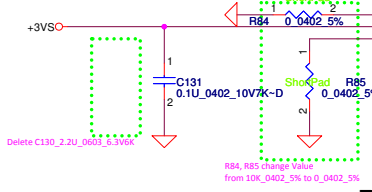
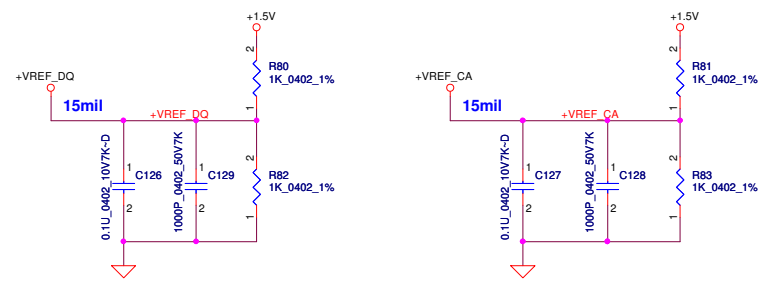
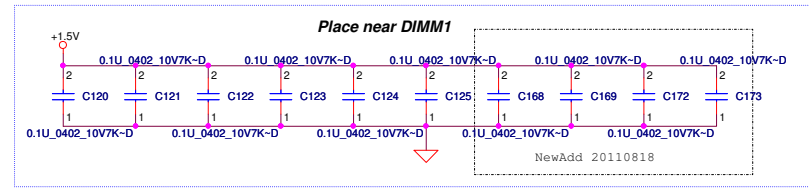
## Translator HPD



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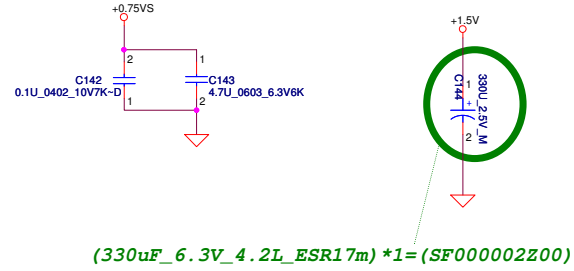
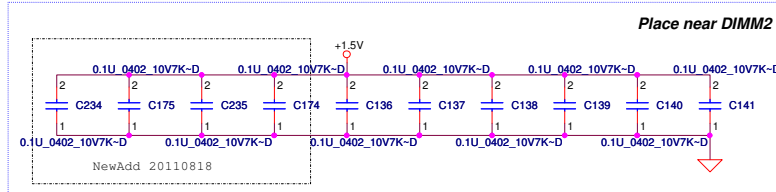
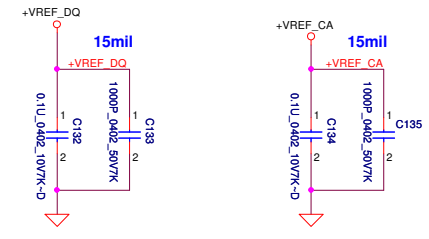
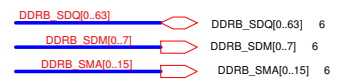
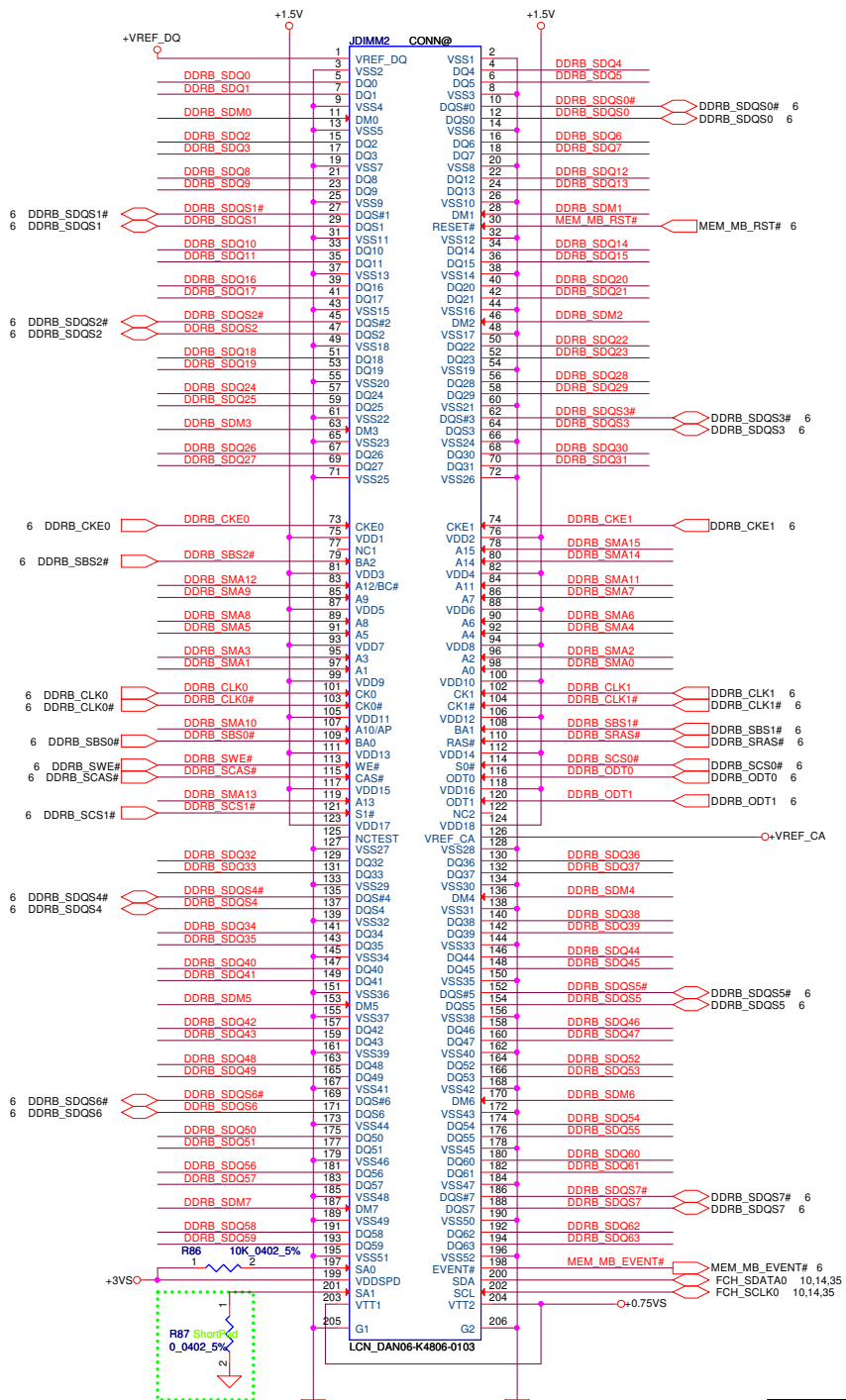


- DDRA\_SDQ[0..63] 6
- DDRA\_SDM[0..7] 6
- DDRA\_SMA[0..15] 6



**Reverse H:4mm**  
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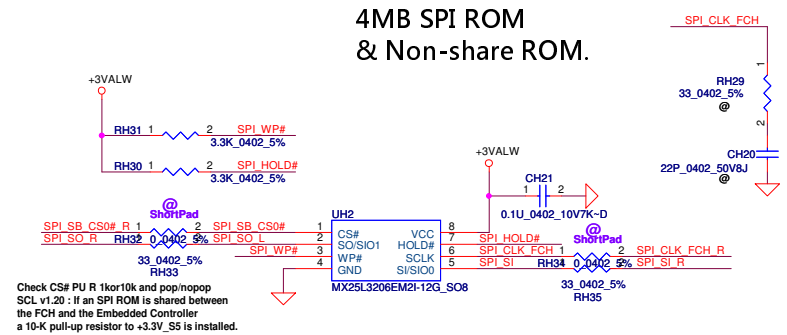
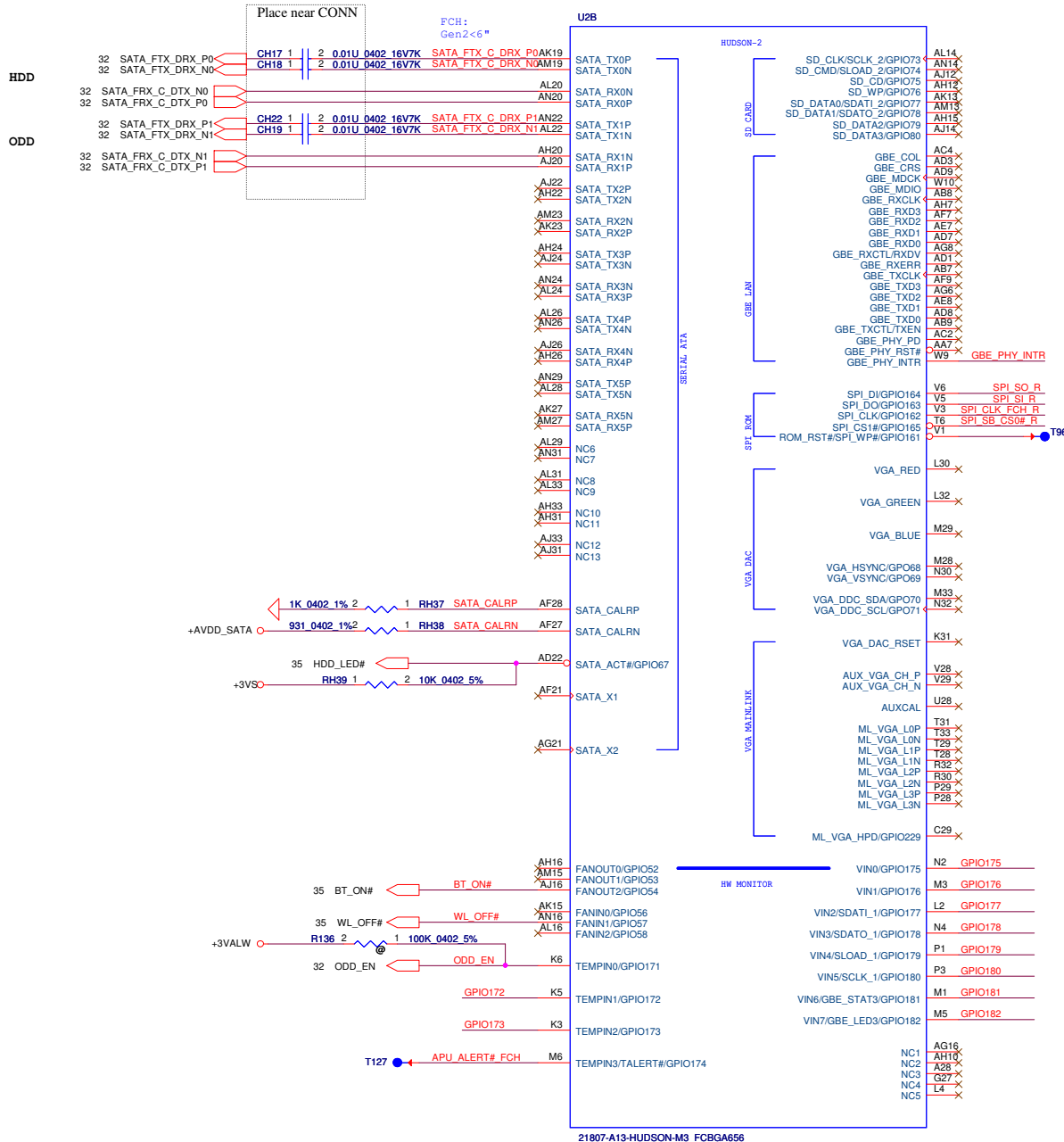


**Reserve H:8mm**  
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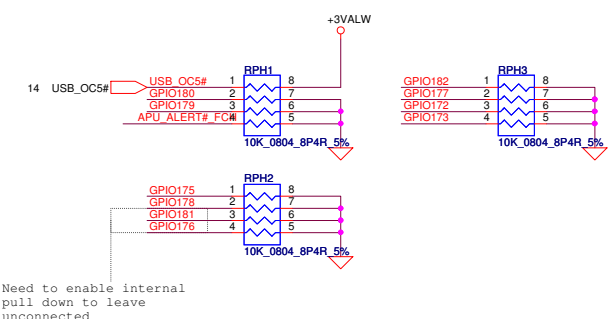


# 4MB SPI ROM & Non-share ROM.



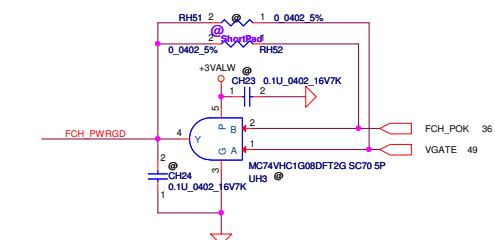
GBE\_PHY\_INTR  
Pulled-up to +3.3V\_S5 with a 10-KΩ 5% resistor.  
FCH SCL v1.20 #19-85

Removed RGMII/MII support and updated termination requirements for GBE\_COL, GBE\_CRS, GBE\_RXERR and GBE\_MDIO when RGMII/MII interface is not used.  
FCH DGv1.20 / SCL v1.20

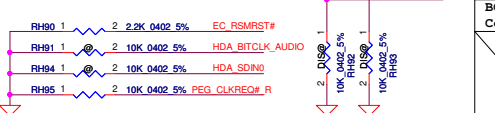
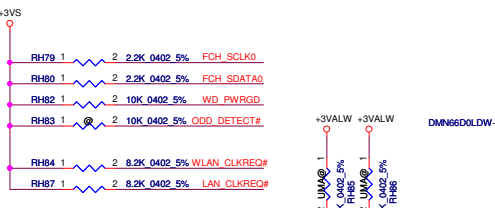
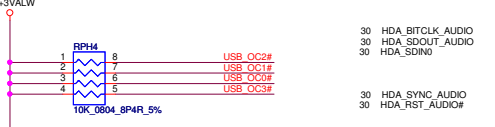
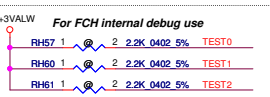
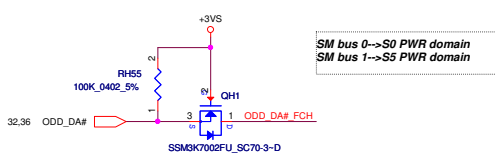


21807-A13-HUDSON-M3\_FCBGA656

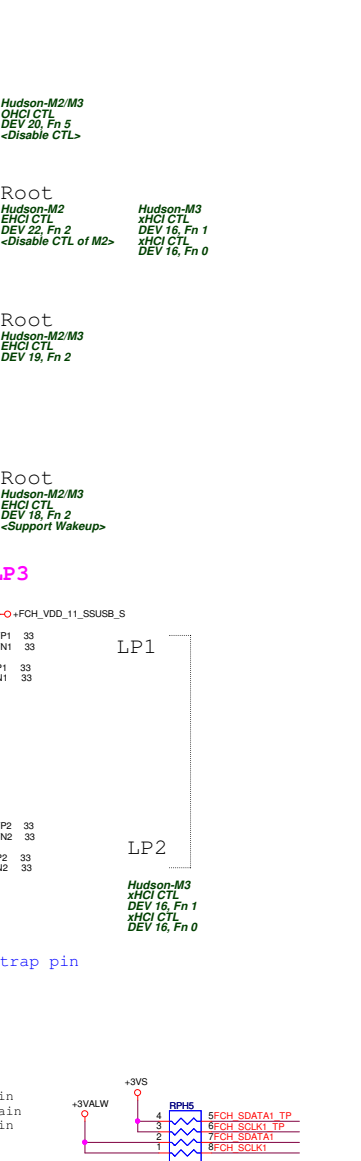
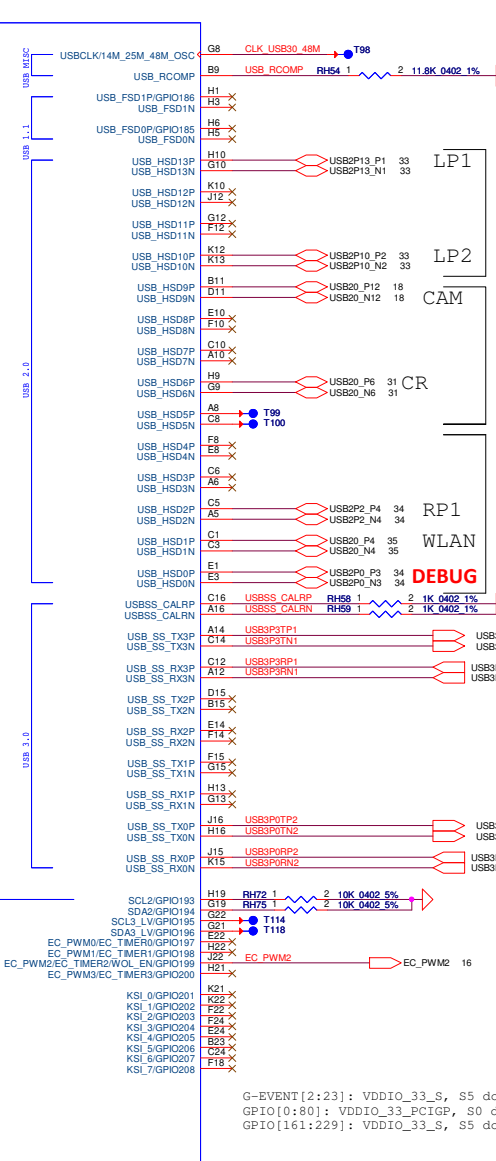
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<p>21807-A13-HUDSON-M3_FCBGA656</p>				<p>Document Number LA-9103P</p>	<p>Rev 0.1</p>
<p>Date: Tuesday, November 27, 2012   Sheet 13 of 52</p>					

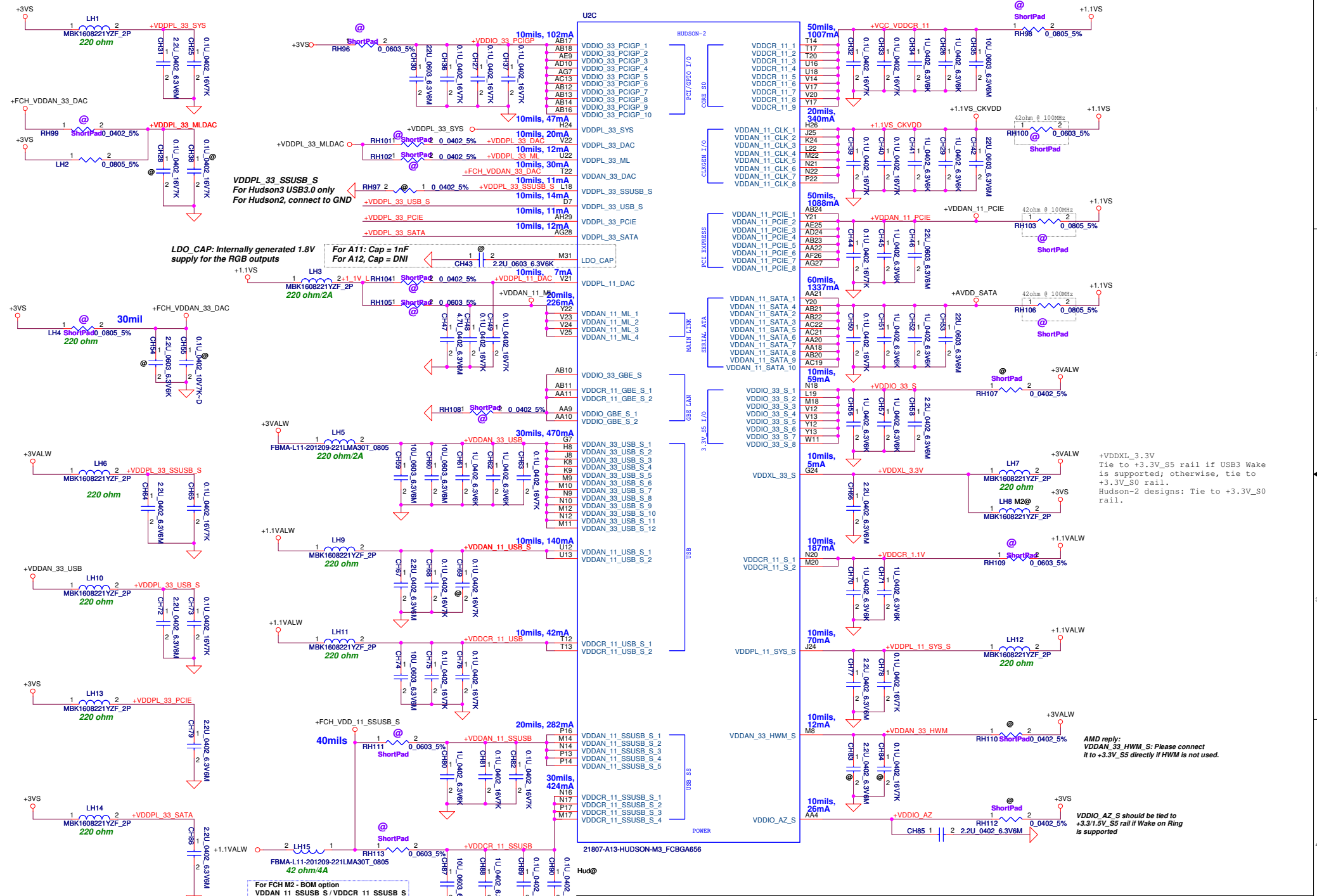


**THERMTRIP:**  
Need level shift from +3VALW to +1.5V  
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.



BOARD Config.	GPIO189	GPIO190	Function
	0	0	DIS-PX4
	0	1	Reserved
	1	0	DIS-PURE
	1	1	UMA





LDO\_CAP: Internally generated 1.8V supply for the RGB outputs

For A11: Cap = 1nF  
For A12, Cap = DN1

+VDDXL\_3.3V  
Tie to +3.3V\_S5 rail if USB3 Wake is supported; otherwise, tie to +3.3V\_S0 rail.  
Hudson-2 designs: Tie to +3.3V\_S0 rail.

AMD reply:  
VDDAN\_33\_HWM\_S: Please connect it to +3.3V\_S5 directly if HWM is not used.

VDDIO\_AZ\_S should be tied to +3.3/1.5V\_S5 rail if Wake on Ring is supported

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				FCH-PWR		
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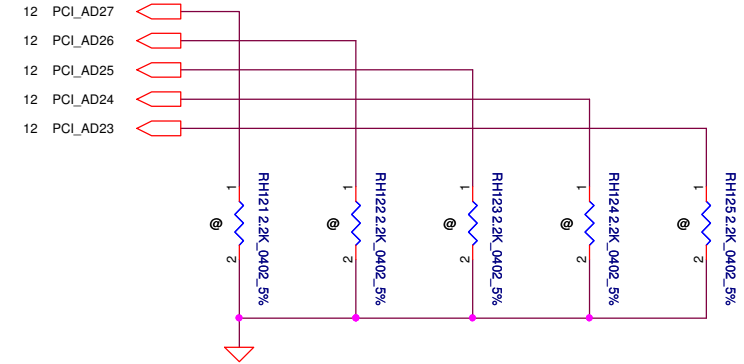
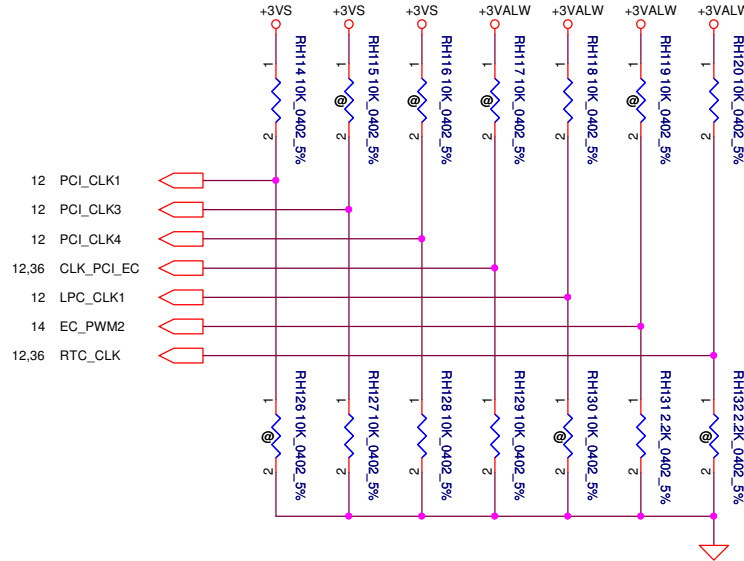
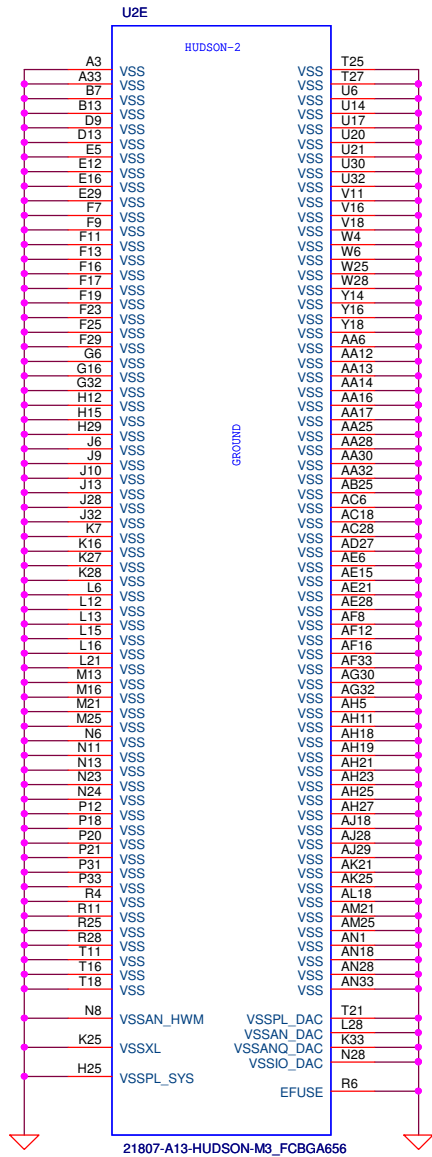
# DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

## STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 <i>DEFAULT</i>	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED <i>DEFAULT</i>	LPC ROM	S5 PLUS MODE DISABLED <i>DEFAULT</i>
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP <i>DEFAULT</i>	FUSION CLOCK MODE <i>DEFAULT</i>	EC DISABLED <i>DEFAULT</i>	CLKGEN DISABLE	SPI ROM <i>DEFAULT</i>	S5 PLUS MODE ENABLED

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL <i>DEFAULT</i>	DISABLE ILA AUTORUN <i>DEFAULT</i>	USE FC PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	DISABLE PCI MEM BOOT <i>DEFAULT</i>
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

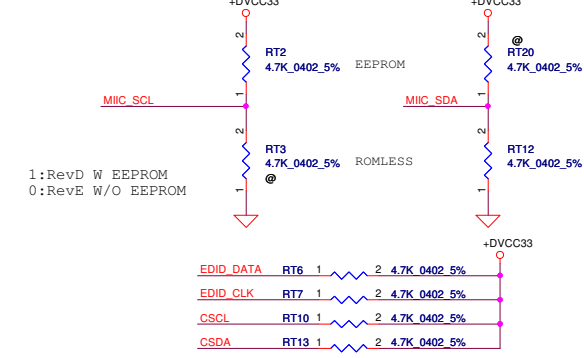
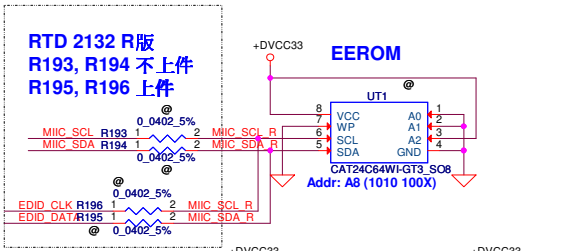
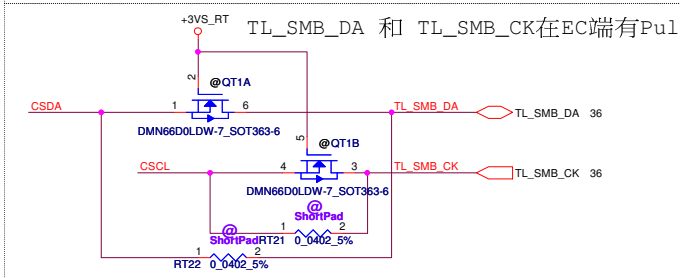
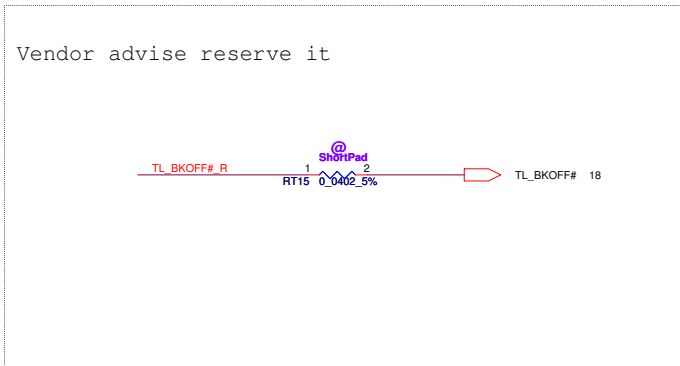
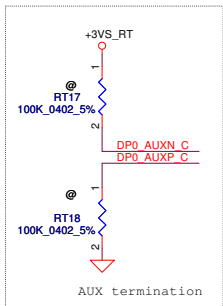
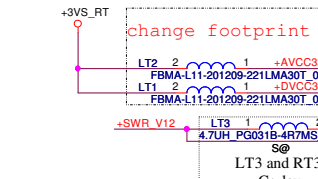
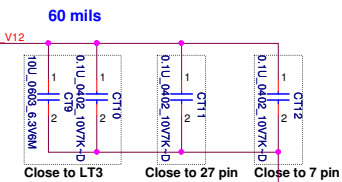
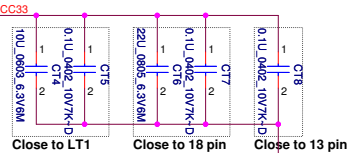
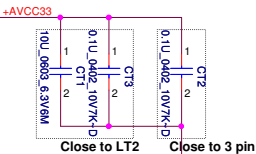


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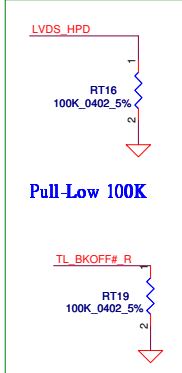


**Power Consumption:**

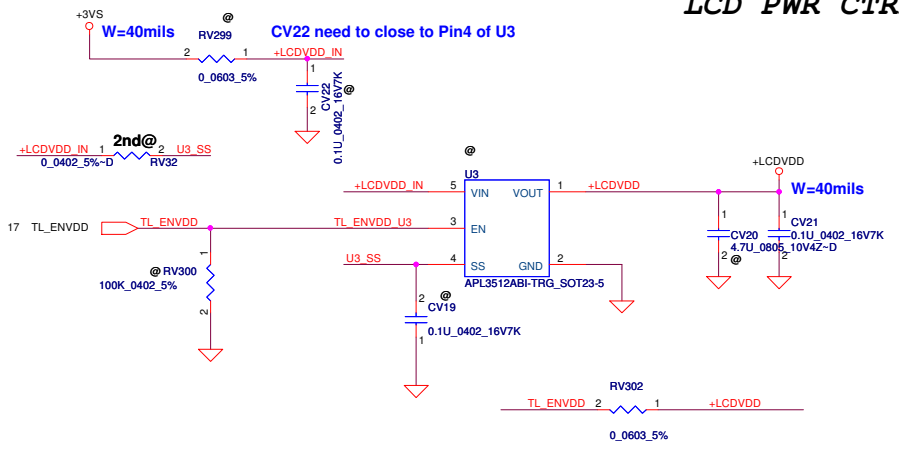
- Pin3 (DPV33) < 20mA
- Pin 7 (DP\_V12) < 100mA
- Pin 11 (SWR\_VCCK) < 100mA (layout trace > 60 mil)
- Pin 12 (SWR\_LX) < 600mA (layout trace > 60 mil)
- Pin 13 (SWR\_VDD) < 200mA (layout trace > 40 mil)
- Pin 18 (PVCC) < 50 mA
- Pin 27 (VCCK) < 50mA



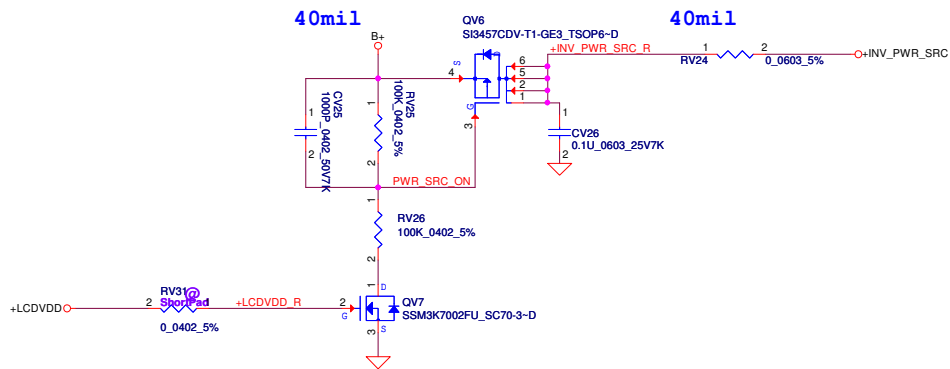
Pin30			
		0	1
Pin31	0	x	EP MODE
	1	ROM	EEROM



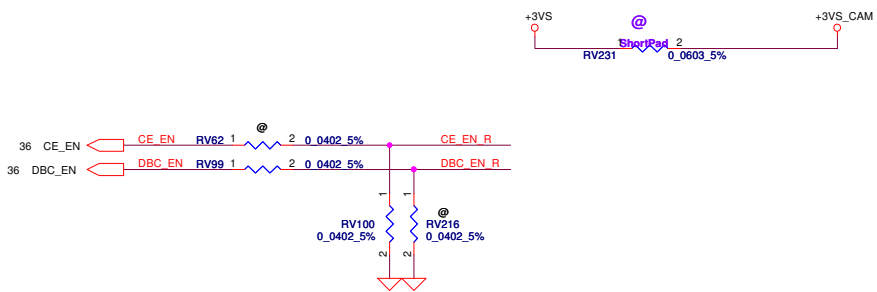
### LCD PWR CTRL



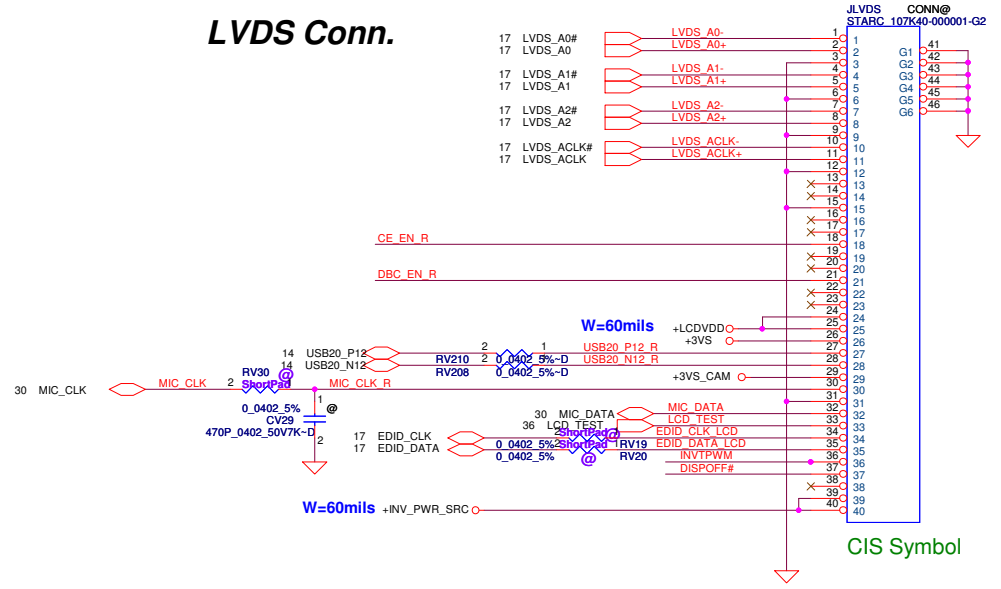
### LCD backlight PWR CTRL



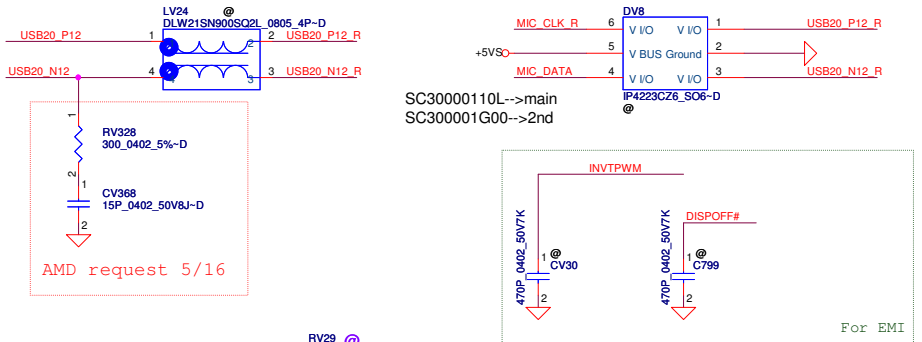
### Wedcam PWR CTRL



### LVDS Conn.

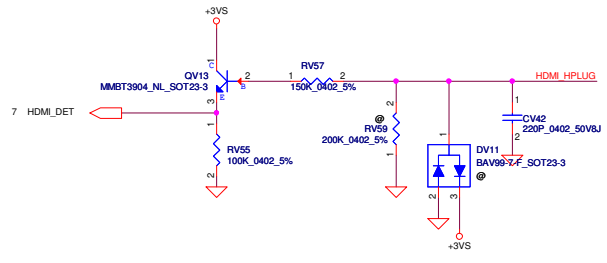
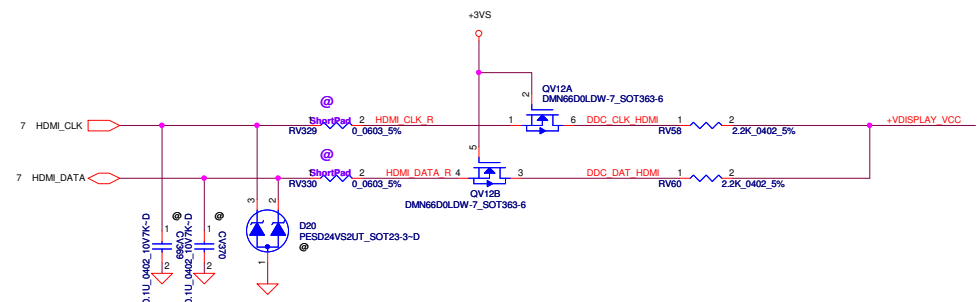
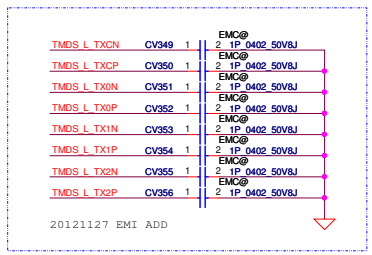
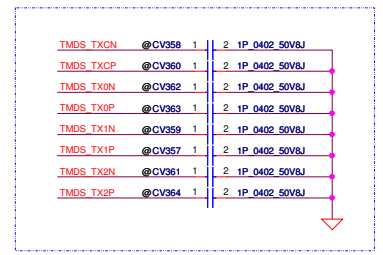
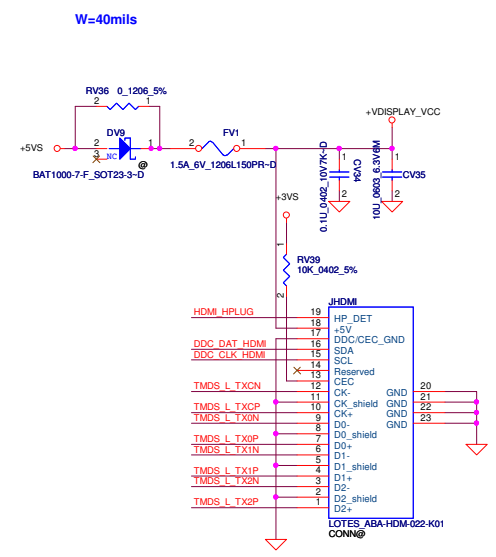
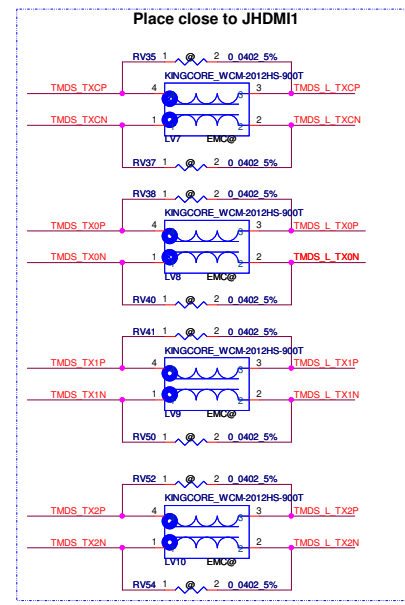
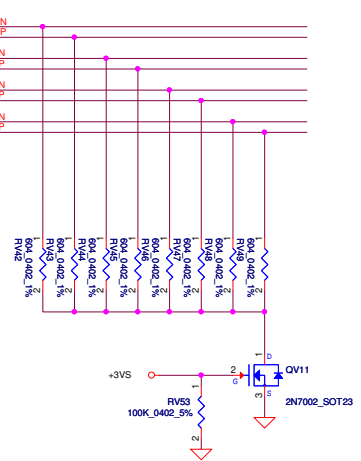


**\* Reserved for EMI/ESD/RF need to close to JLVDS**



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				Date: Tuesday, November 27, 2012   Sheet 18 of 52

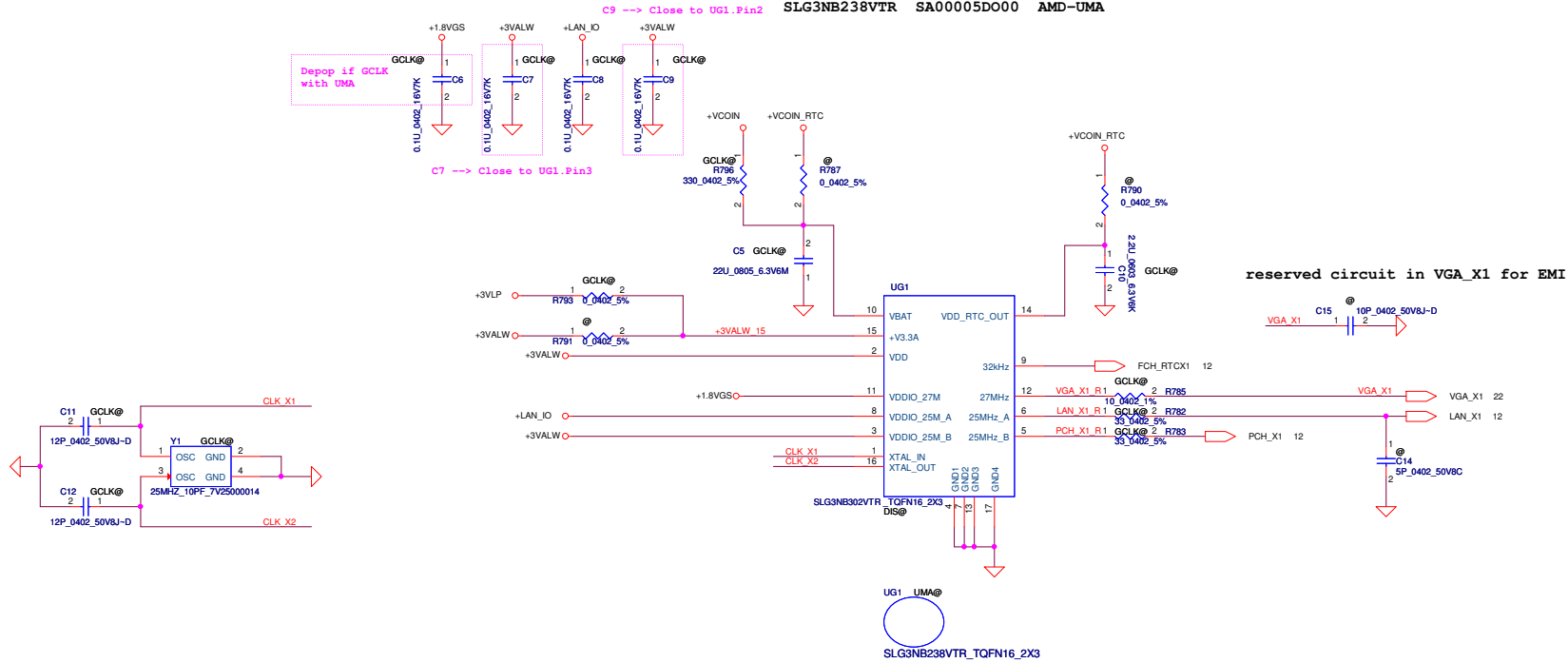
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7	DP2_TXP3	CV33	0.0402 5%	TMDS TXCP
7	DP2_TXN2	CV36	0.0402 5%	TMDS TXCN
7	DP2_TXP2	CV37	0.0402 5%	TMDS TXCP
7	DP2_TXN1	CV38	0.0402 5%	TMDS TXCN
7	DP2_TXP1	CV39	0.0402 5%	TMDS TXCP
7	DP2_TXN0	CV40	0.0402 5%	TMDS TXCN
7	DP2_TXP0	CV41	0.0402 5%	TMDS TXCP



CV365, CV367  
Please close APU side

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SLG3NB244VTR SA000057I00 Intel-UMA  
 SLG3NB300VTR SA00005RS00 Intel-DIS  
 SLG3NB302VTR SA00006D500 AMD-DIS  
 SLG3NB238VTR SA00005D000 AMD-UMA



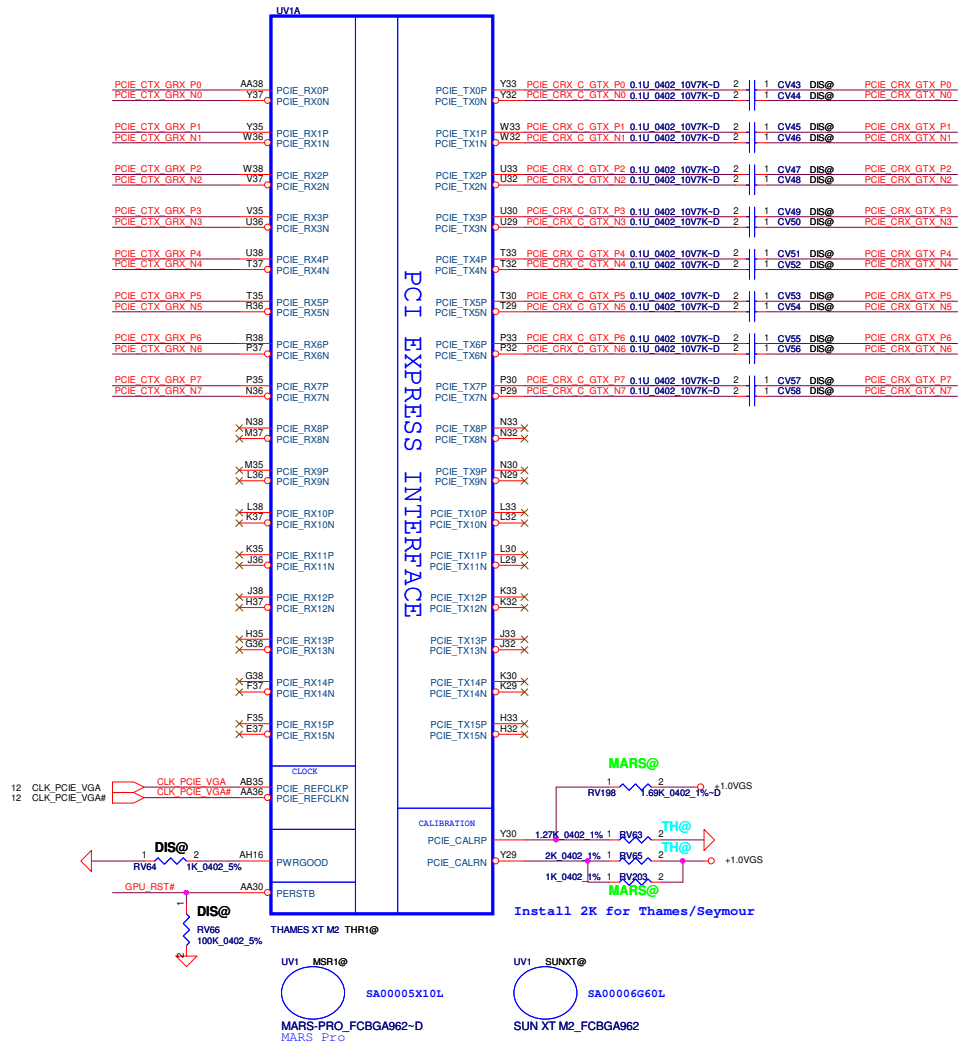
UG1 UMA@  
 SLG3NB238VTR\_TQFN16\_2X3

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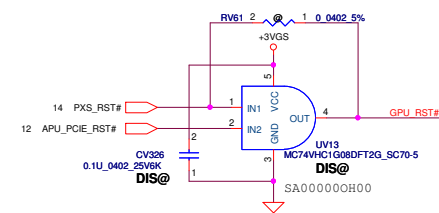
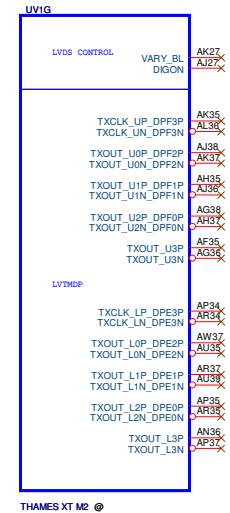
5 PCIE\_CTX\_GRX\_P7.0] PCIE\_CTX\_GRX\_P7.0]  
 5 PCIE\_CTX\_GRX\_N7.0] PCIE\_CTX\_GRX\_N7.0]

PCIE\_CRX\_GTX\_P7.0] PCIE\_CRX\_GTX\_P7.0] 5  
 PCIE\_CRX\_GTX\_N7.0] PCIE\_CRX\_GTX\_N7.0] 5

### GFX PCIE LANE REVERSAL



### LVDS Interface



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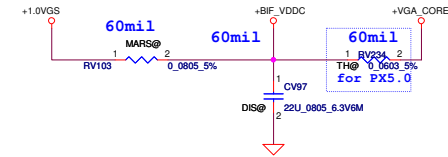
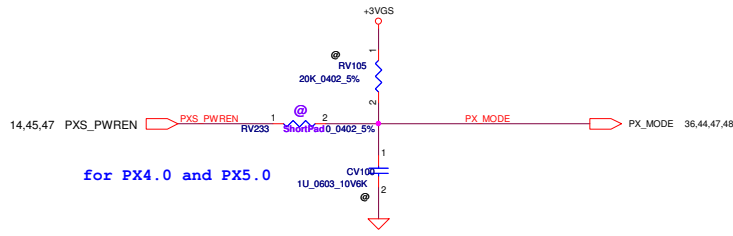


PX\_MODE=1 for Normal Operation

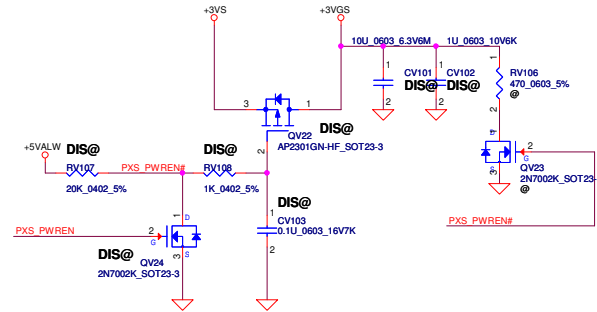
PX\_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE\_VDDC and 1.8V rail

### Switch circuits in BACO desings for Thames/Seymour only

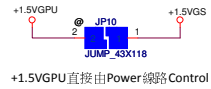
55mA@1.0V, in BACO mode



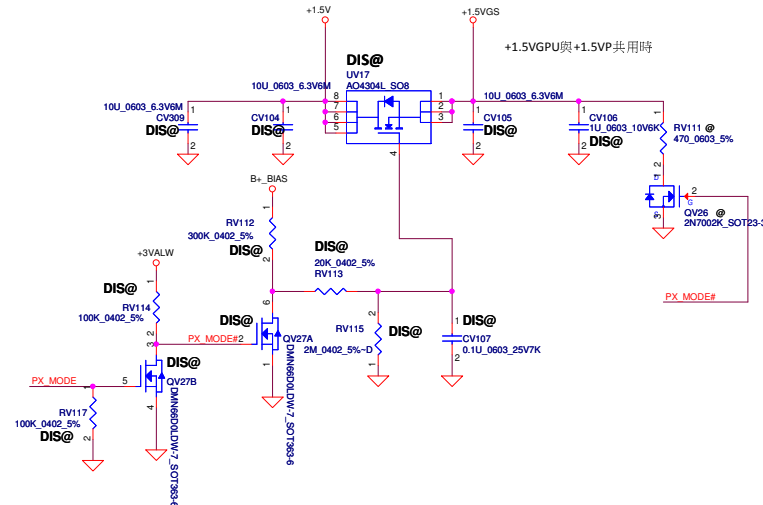
### +3.3VS TO +3.3VGS



### +1.5VGPU TO +1.5VGS

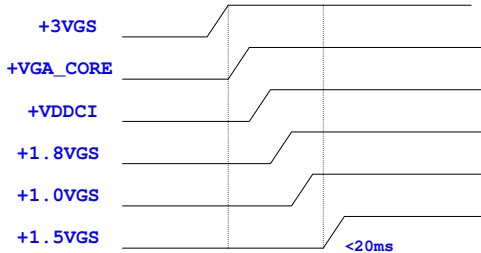


### +1.5V TO +1.5VGS

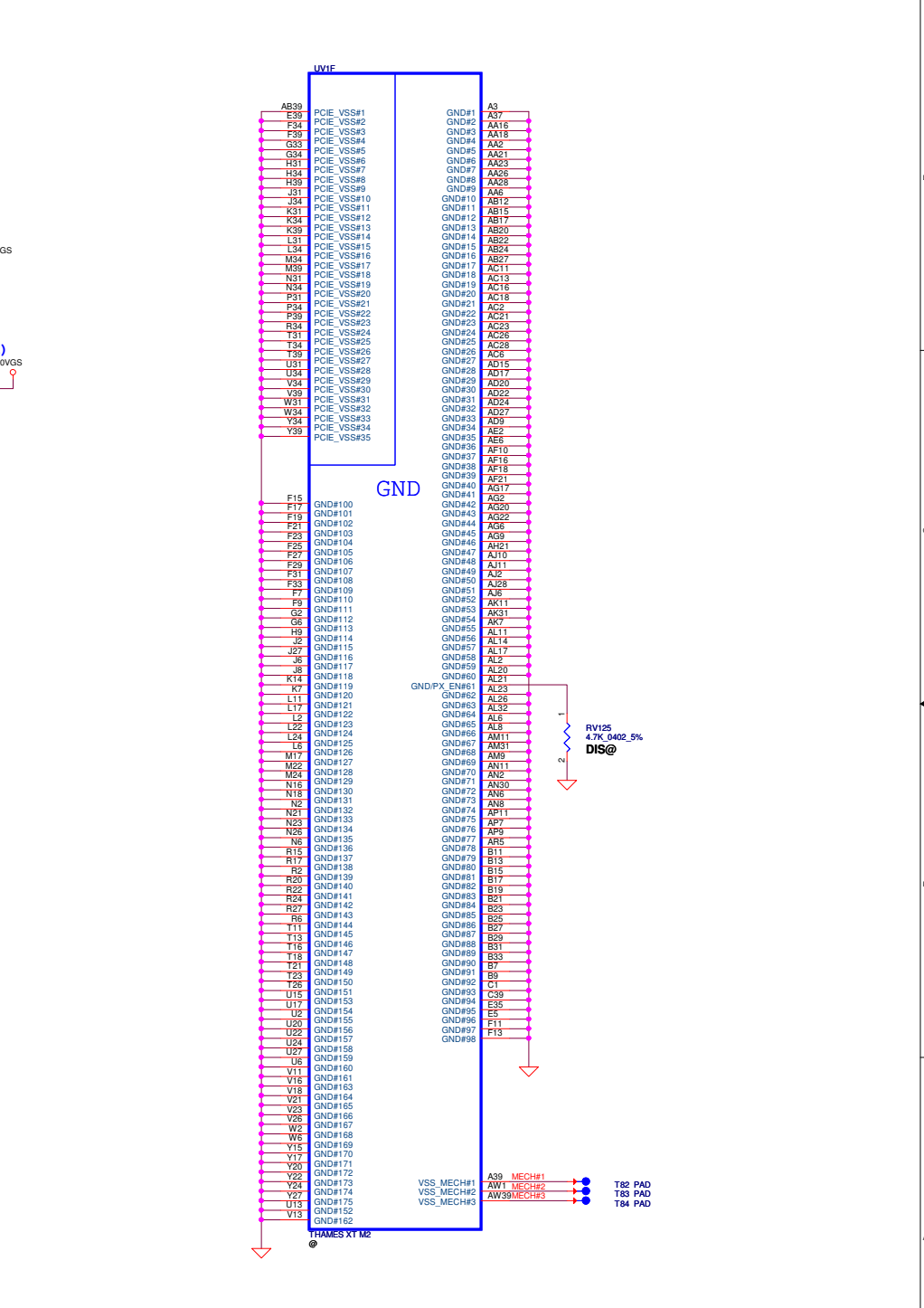
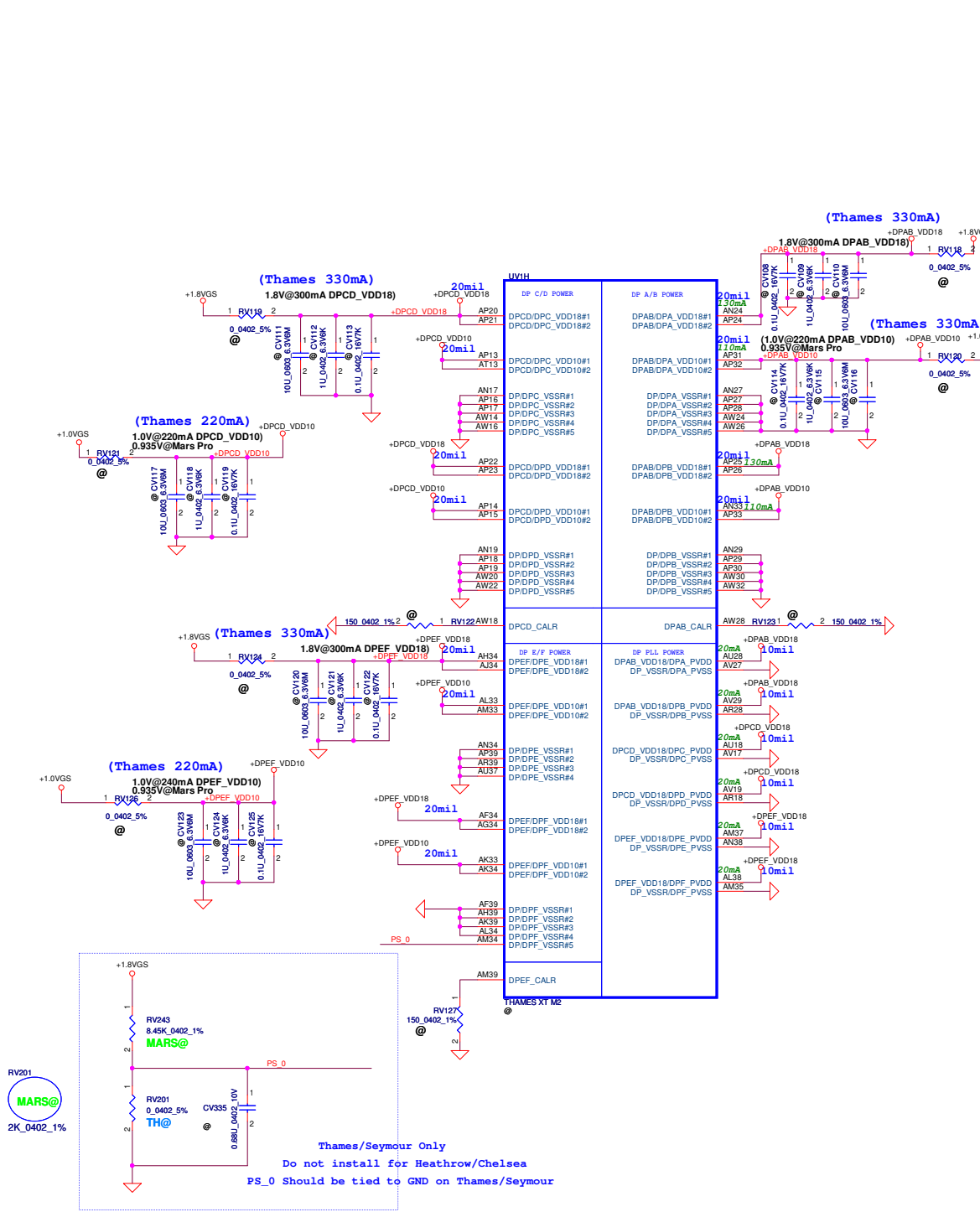


**Note:**  
 PX4.0 +VGA\_CORE, VDDCI, +1.5VGS OFF  
 PX4.0 +3VGS, +1.0VGS, +1.8VGS ON  
 PX5.0 +3VGS, +VGA\_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

### Power Sequence of Thames and Chelsea

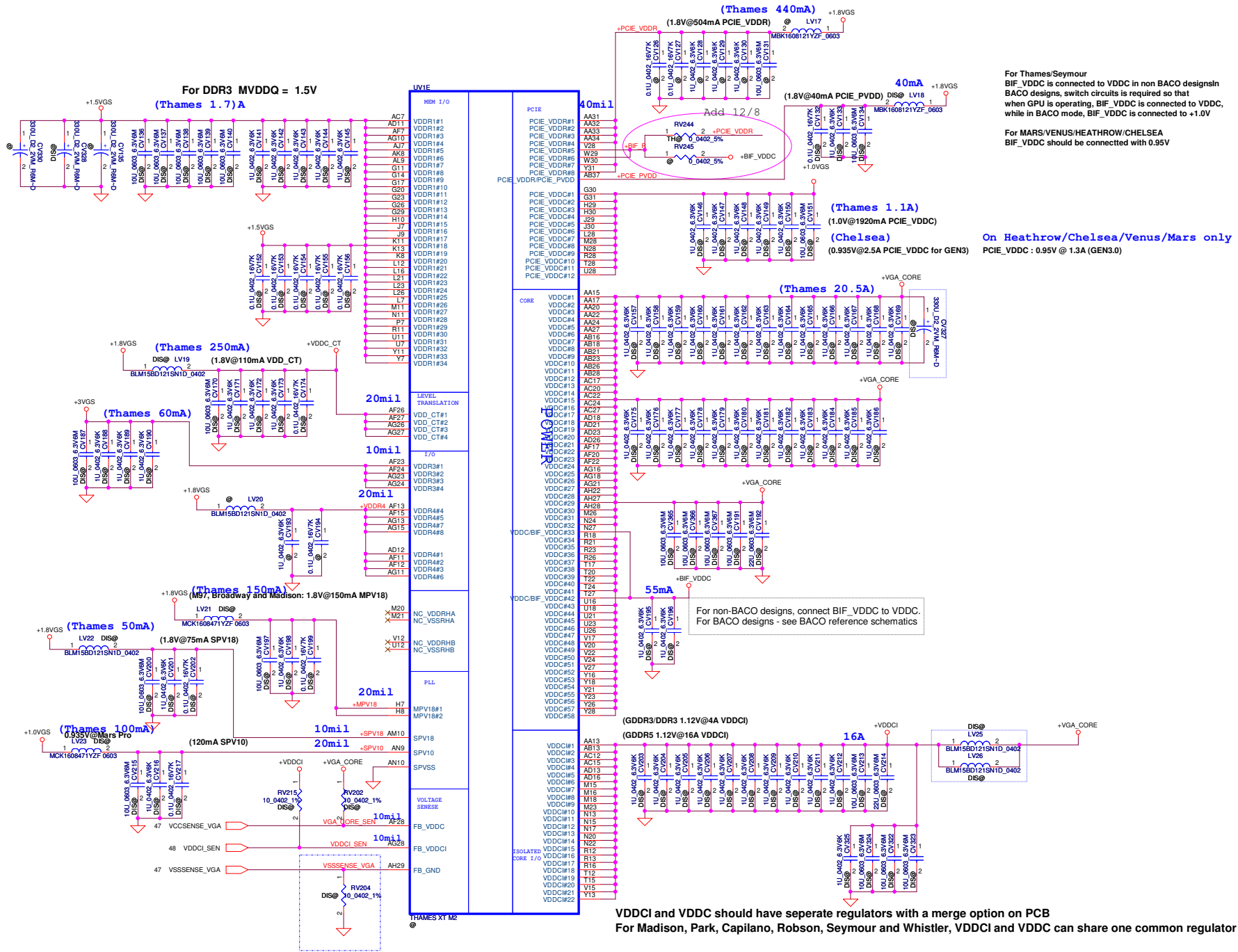


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Thames/Seymour Only  
 Do not install for Heathrow/Chelsea  
 PS\_0 Should be tied to GND on Thames/Seymour





For Thames/Seymour BIF\_VDDC is connected to VDDC in non BACO designsin BACO designs, switch circuits is required so that when GPU is operating, BIF\_VDDC is connected to VDDC, while in BACO mode, BIF\_VDDC is connected to +1.0V

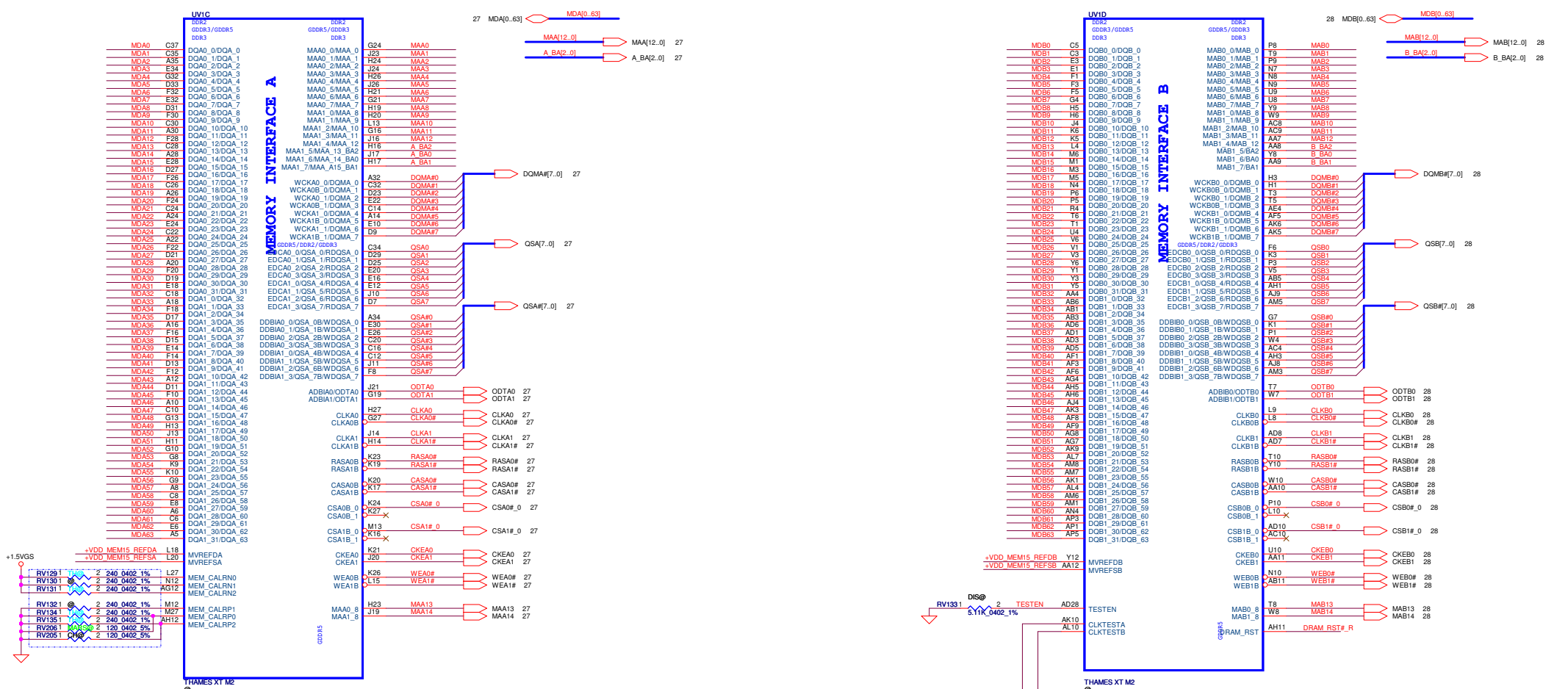
For MARS/VENUS/HEATHROW/CHESEA BIF\_VDDC should be connected with 0.95V

On Heathrow/Chelsea/Venus/Mars only  
PCIE\_VDDC : 0.95V @ 1.3A (GEN3.0)

For non-BACO designs, connect BIF\_VDDC to VDDC.  
For BACO designs - see BACO reference schematics

VDDCI and VDDC should have separate regulators with a merge option on PCB  
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

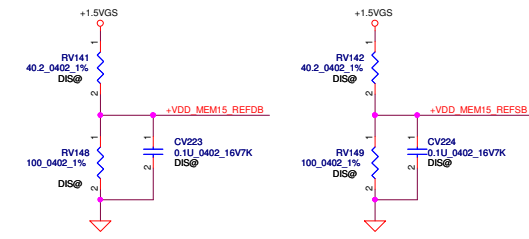
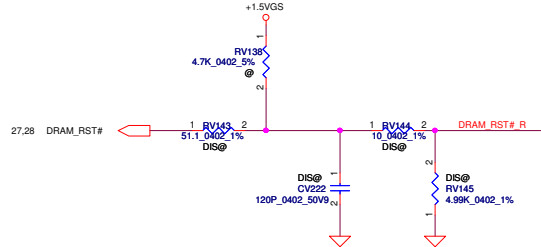
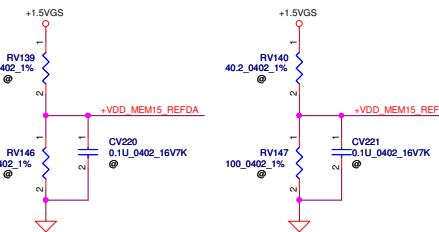
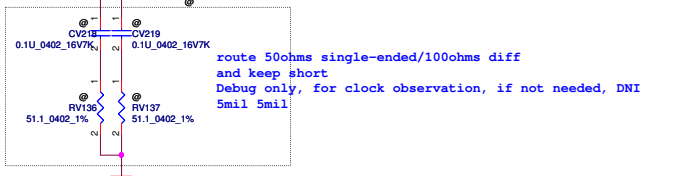
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	ATI ThamesXT M2 Power
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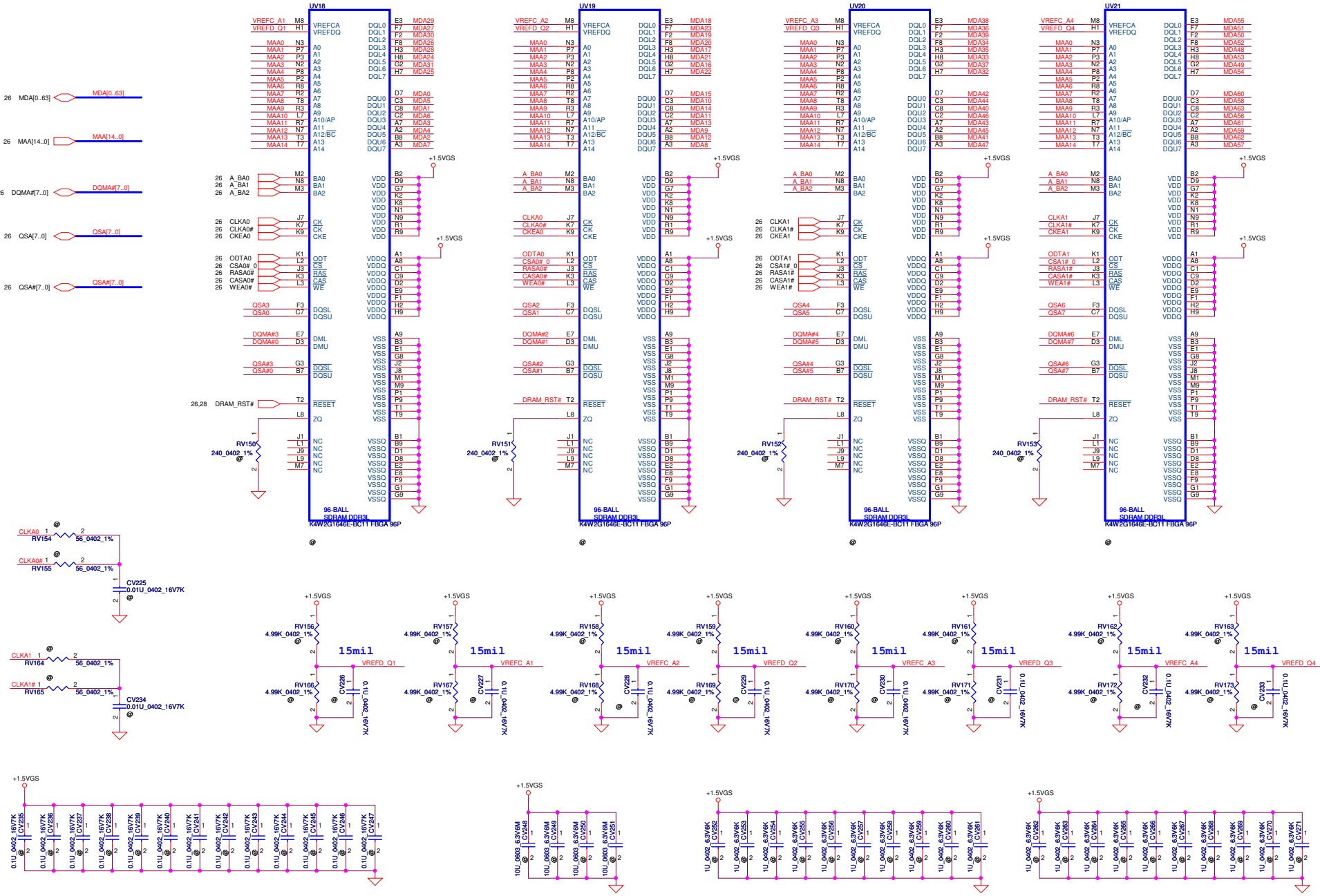
**Co-lay Thames/Mars Pro/Chelsea**

	Thames M2	Mars Pro	Chelsea M2
RV129	POP	@	@
RV130	@	@	@
RV131	POP	@	@
RV132	@	@	@
RV134	POP	@	@
RV135	POP	@	@
RV206	@	MARS@	@
RV205	@	@	POP

This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

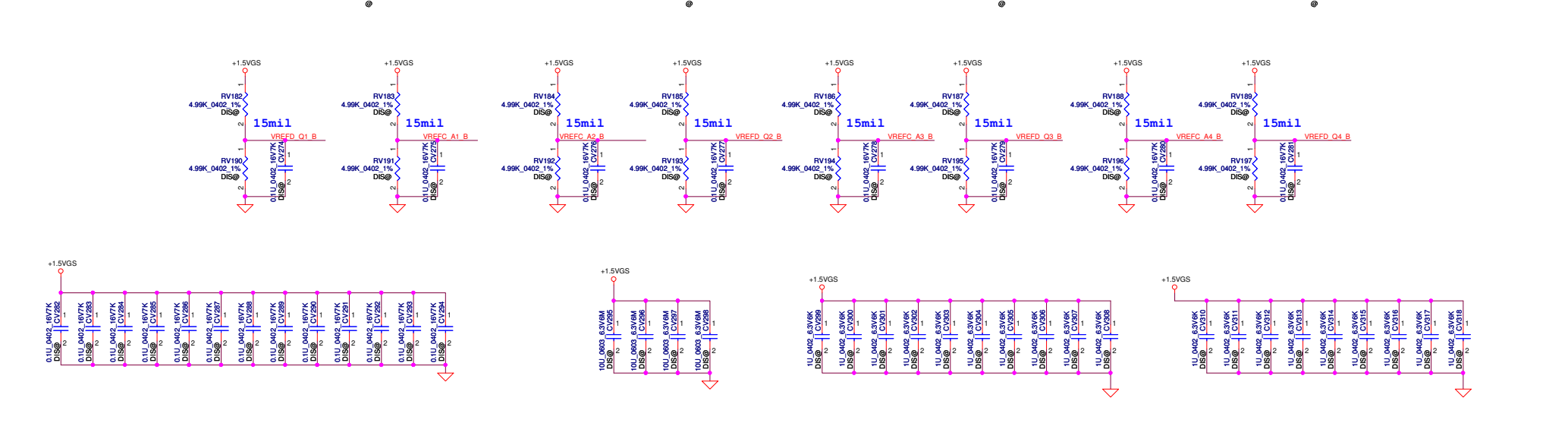
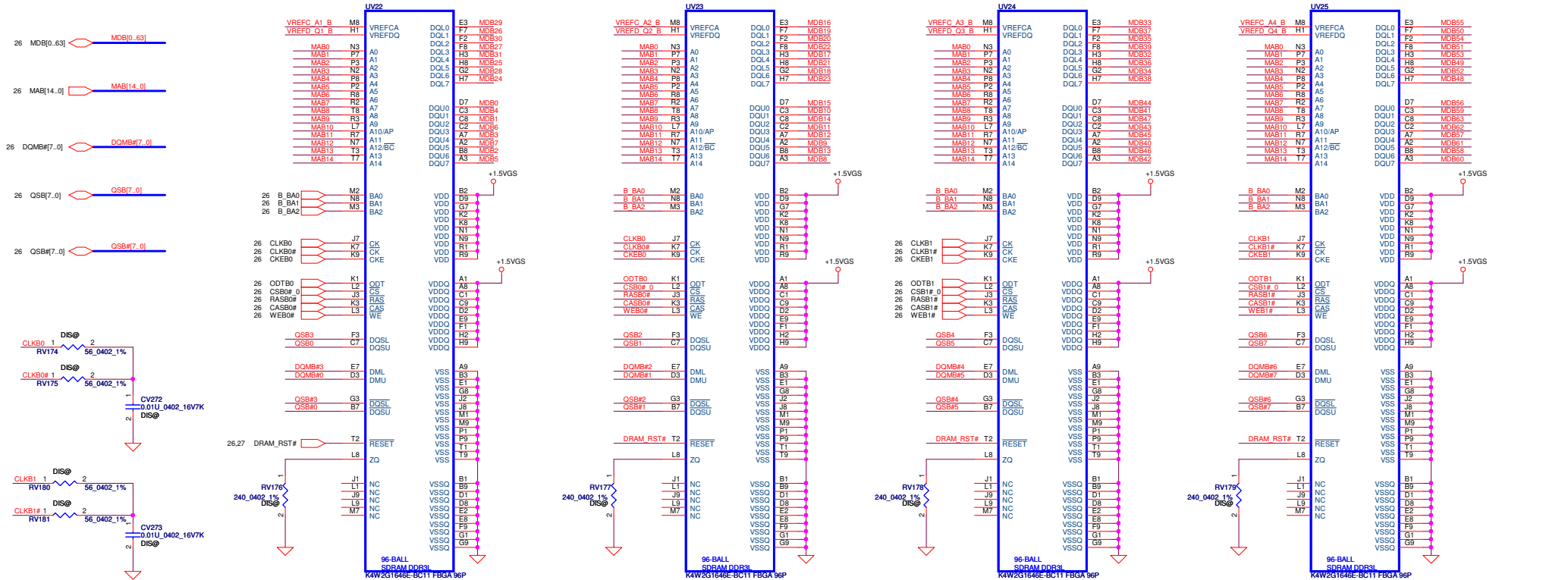


CHANNEL A: 256MB/512MB DDR3

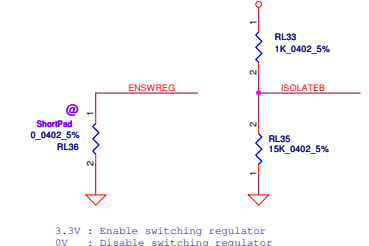
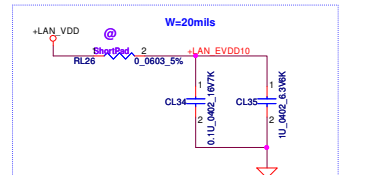
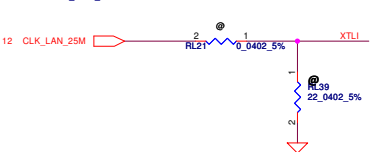
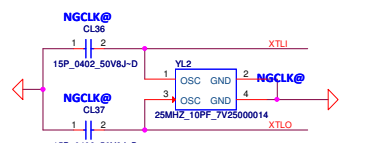
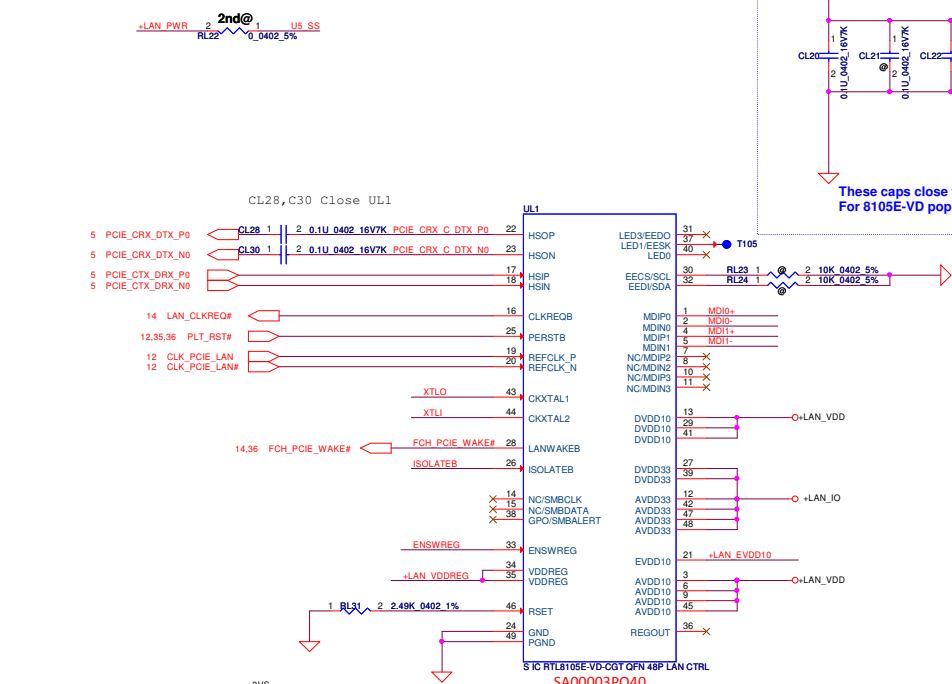
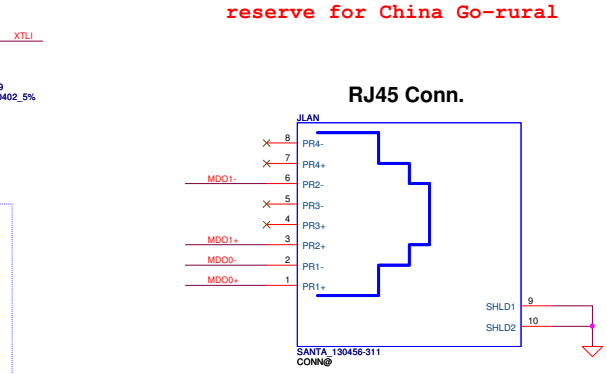
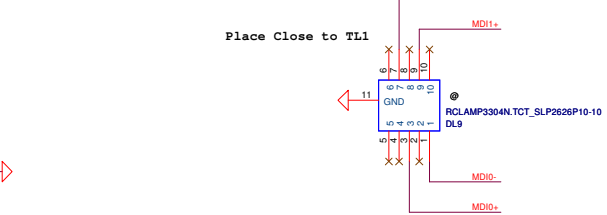
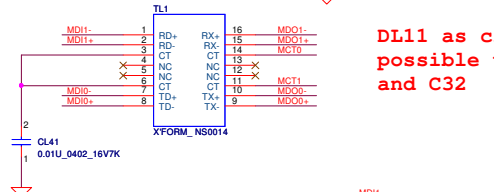
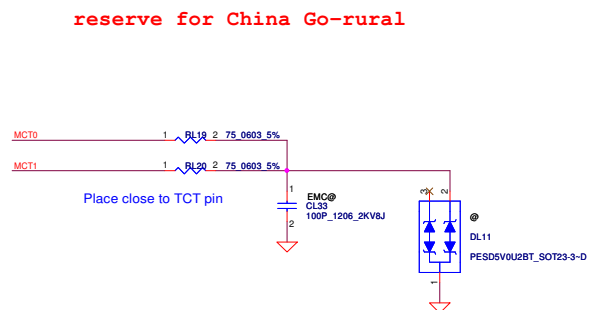
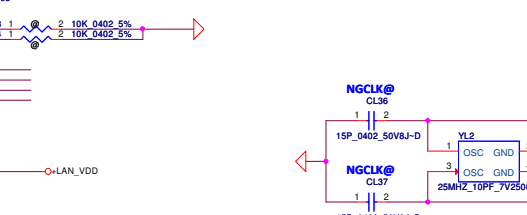
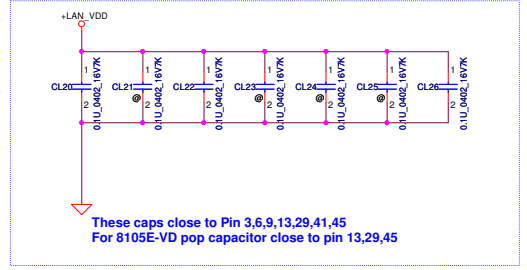
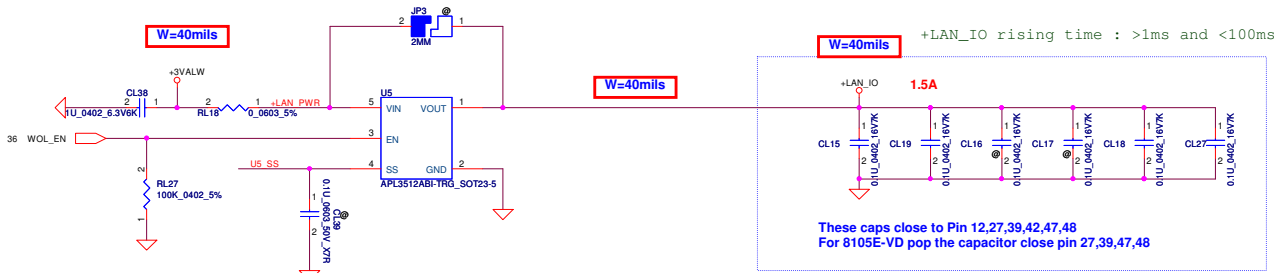


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# CHANNEL B : 256MB/512MB DDR3



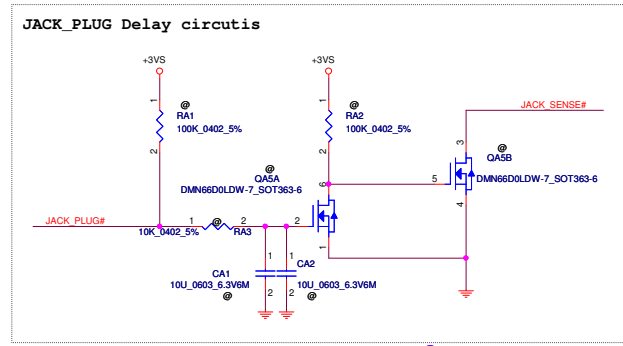
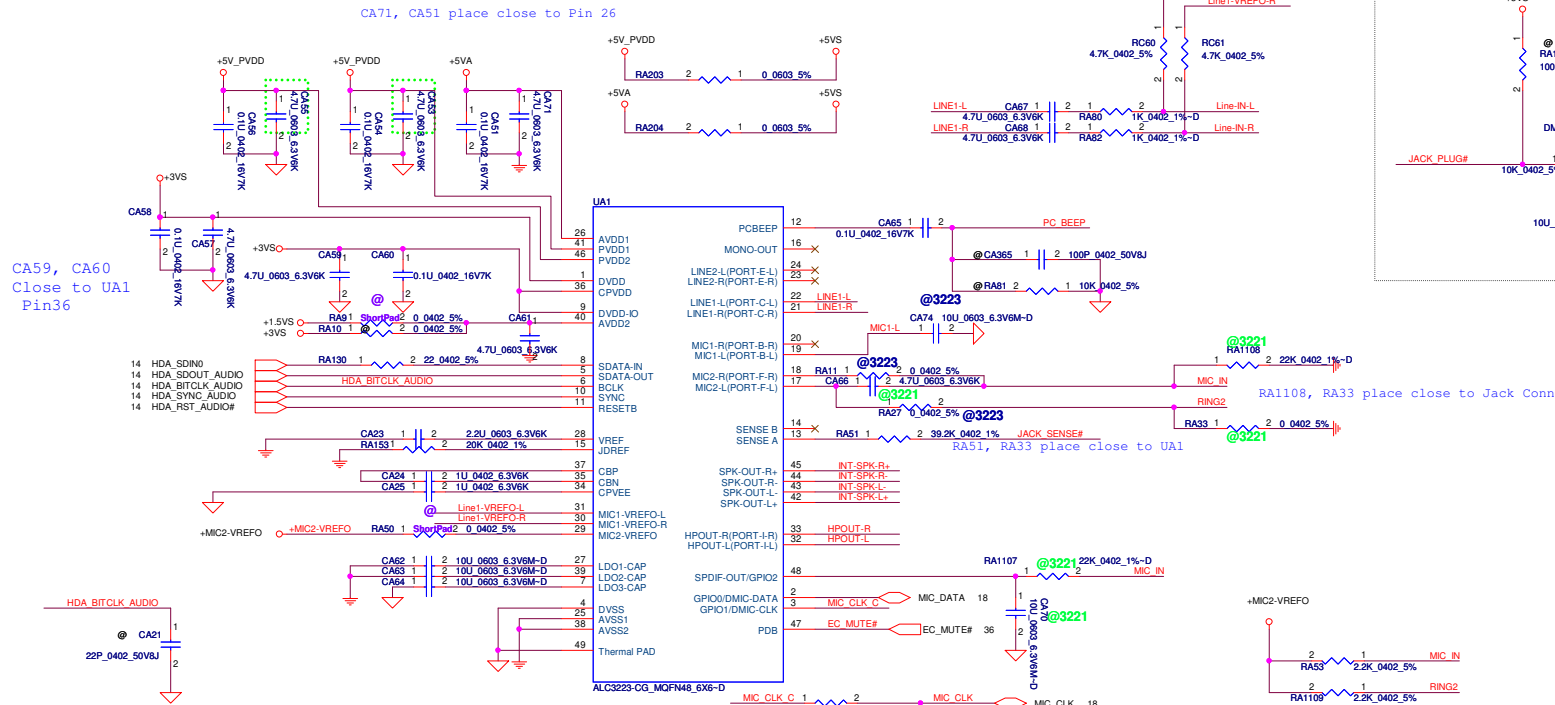
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		ATI ThamesXT M2 VRAM B	
2012/09/11		2014/03/12		Size Document Number	
				LA-9103P	
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Date: Tuesday, November 27, 2012				Sheet 26 of 52	



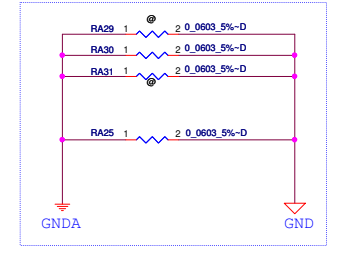
10/100 : 100@ (LDO mode used)

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Size	Document Number	Rev	LA-9103P		
Date	Issued By	November 27, 2012	Sheet	29	of 52

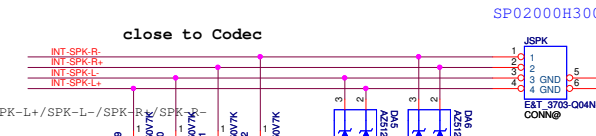
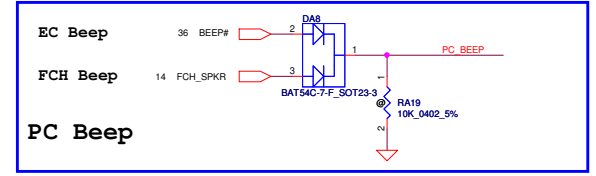
SP011207090  
DC234004V00 (OLD)



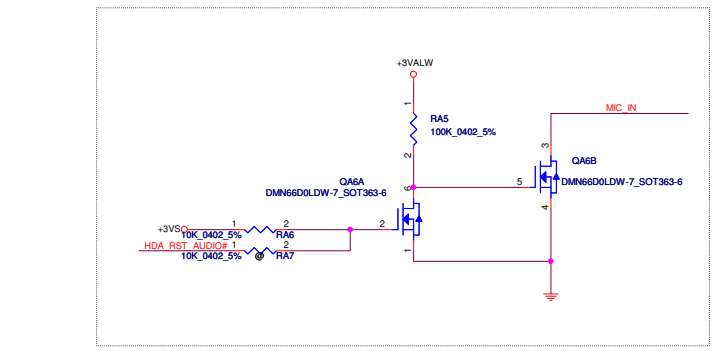
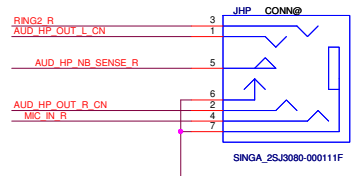
JACK\_PLUG# RA1 100K\_0402\_5% JACK\_SENSE#  
Reserve for cancel Delay circuitis



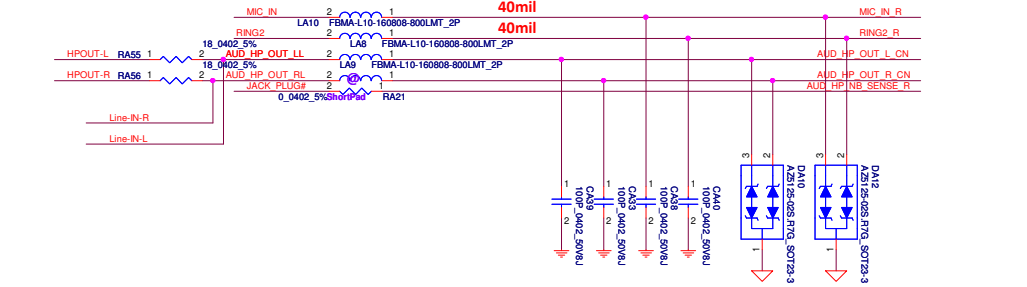
Place on the moat between GND & GNDA.



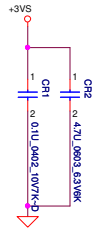
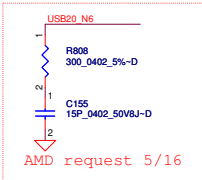
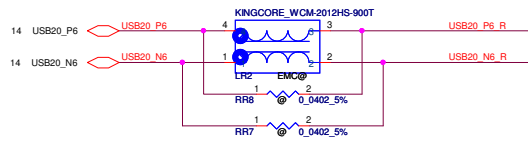
Trace width for SPK-L+/SPK-L-/SPK-L-  
Speaker 4 ohm : 40mil  
Speaker 8 ohm : 20mil



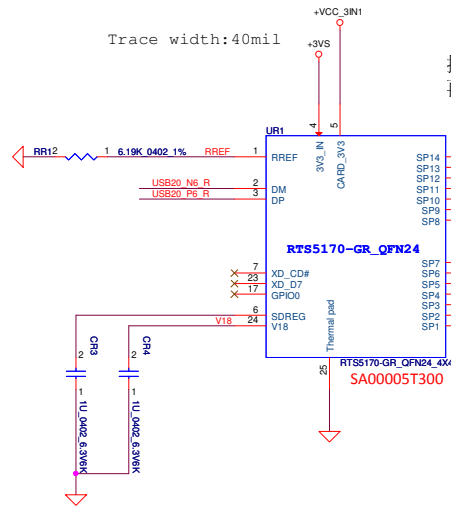
### iPhone and Nokia type Combo Jack



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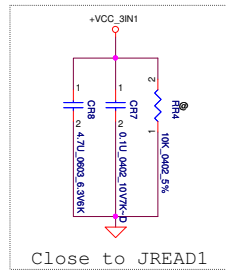
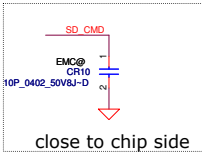
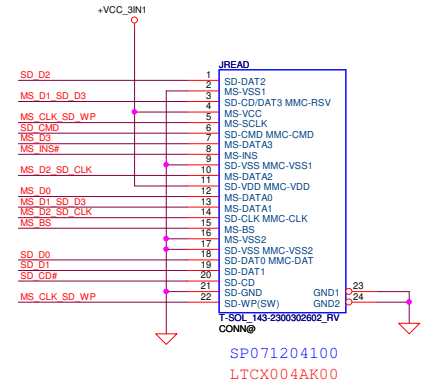
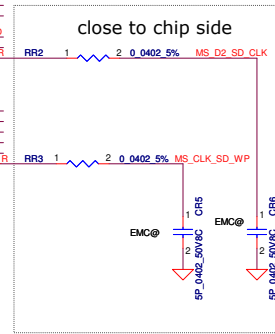


Trace width: 40mil



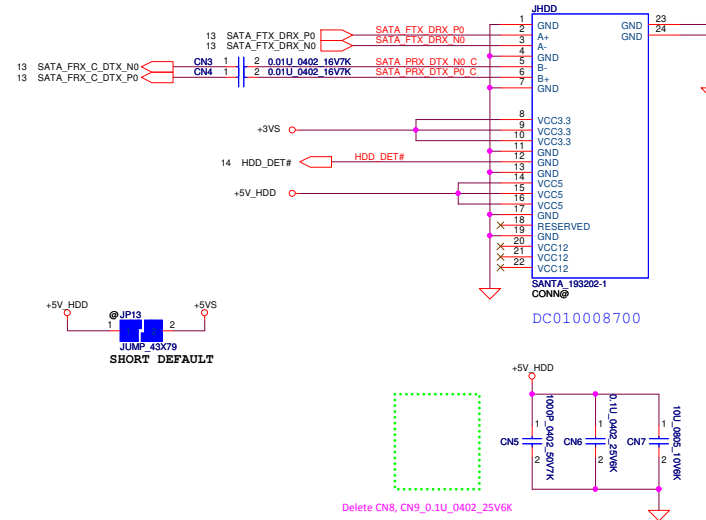
拉MS\_D2\_SD\_CLK到Conn pin 14 SD\_CLK  
再打Via拉到pin 10 MS\_D2

拉MS\_CLK\_SD\_WP到Conn pin 5 MS\_CLK  
再打Via拉到pin 22 SD\_WP



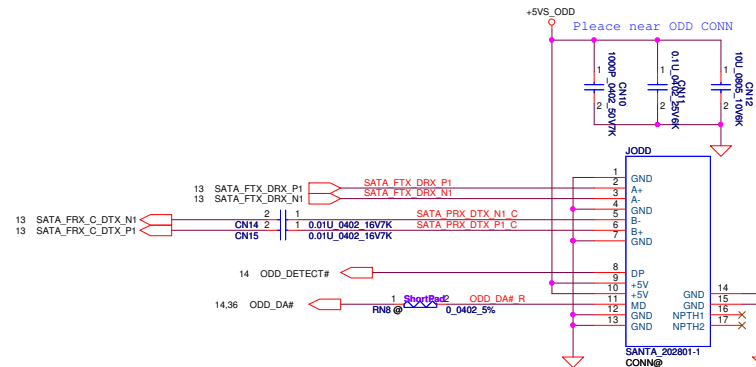
Security Classification	2012/09/11		Compal Secret Data		Deciphered Date		2014/03/12		Title		Compal Electronics, Inc.		
Issued Date	2012/09/11		Deciphered Date		2014/03/12				Document Number		Card Reader RT55179		
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										Date:	Tuesday, November 27, 2012	Sheet	31 of 52

### SATA HDD Conn.

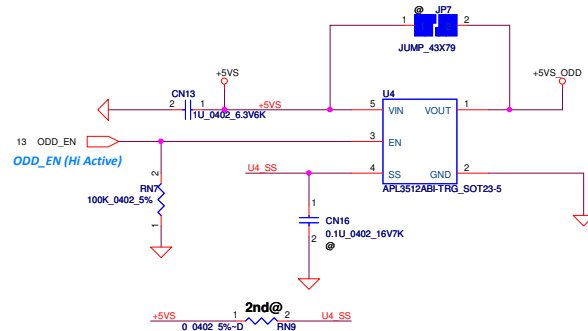


### +5V\_HDD Source

### SATA ODD Conn.



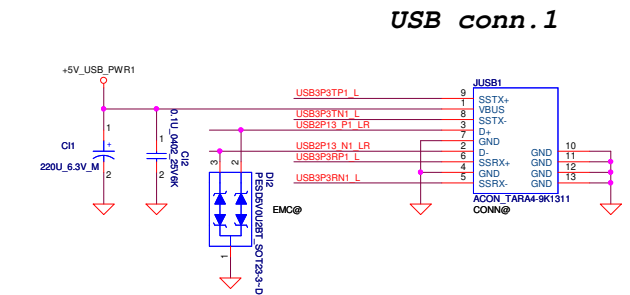
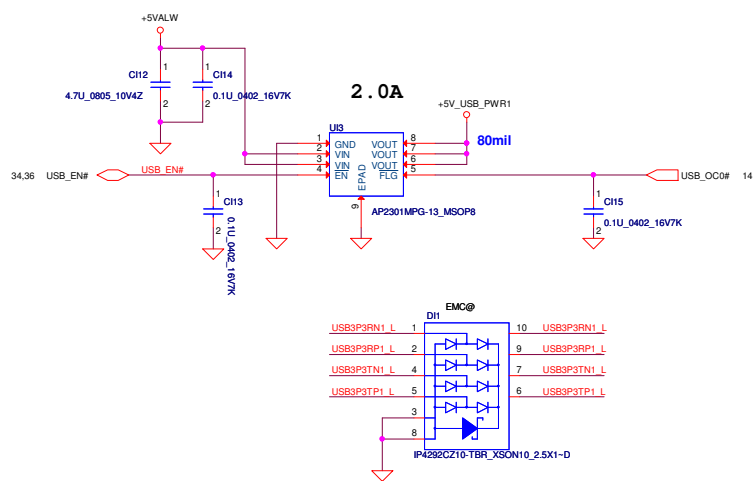
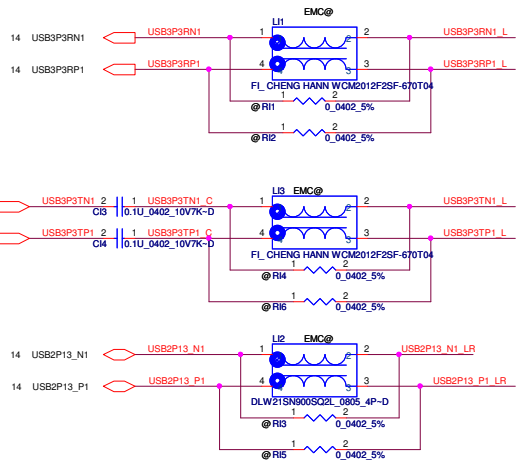
### ODD Power Control



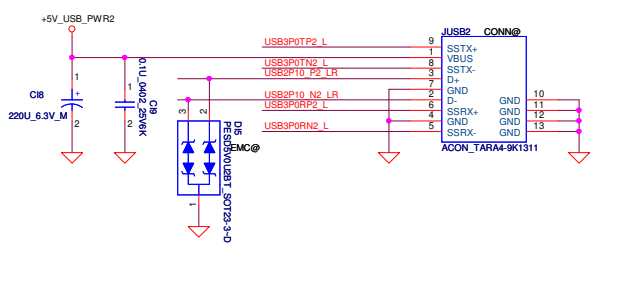
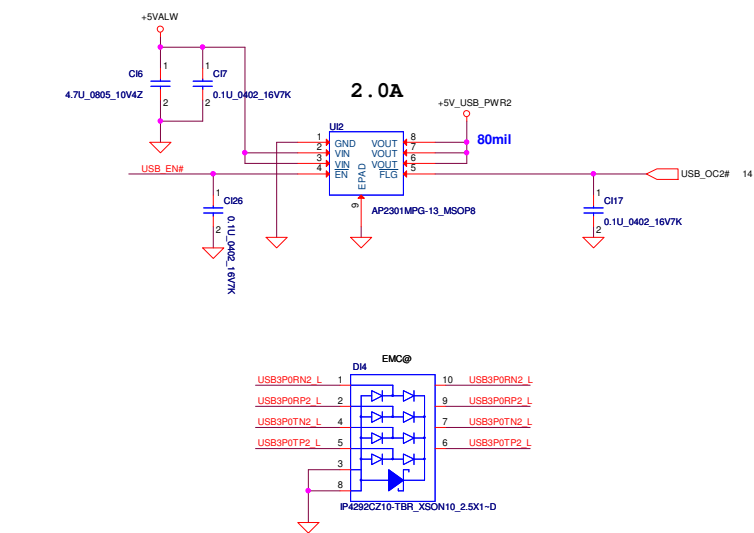
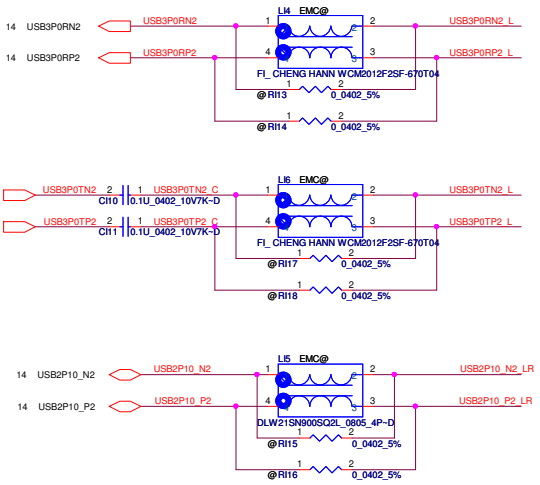
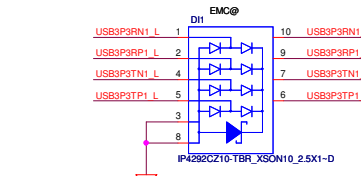
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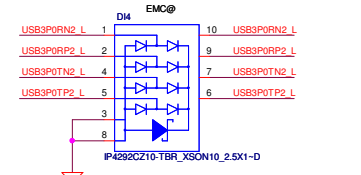
9/20 OAK Intel USB3.0 issue  
 Change LI1, LI3, LI4, LI6 Part  
 PN: from SM01002080L (S SUPPRE\_MURATA DLW21SN900SQ2L 0805)  
 To SM07000580 (S COM FL\_CHENG HANN WCM2012F2SF-670T04)



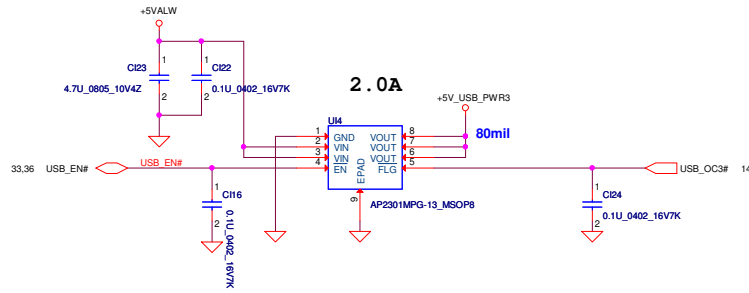
USB conn. 1



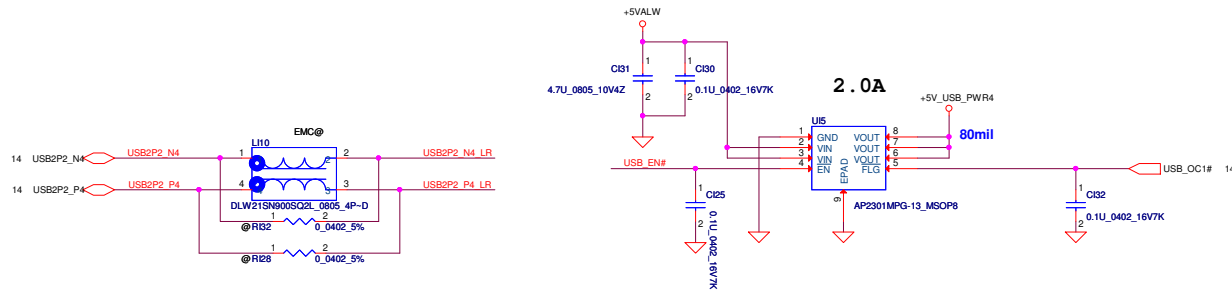
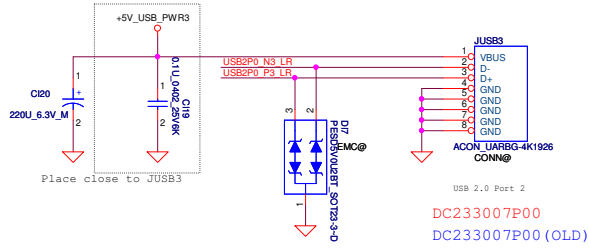
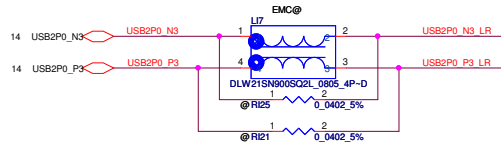
USB conn. 2



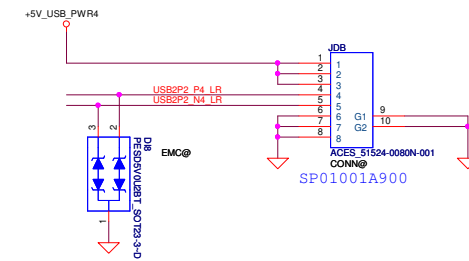
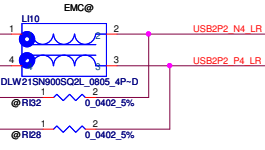
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**USB conn. 3**

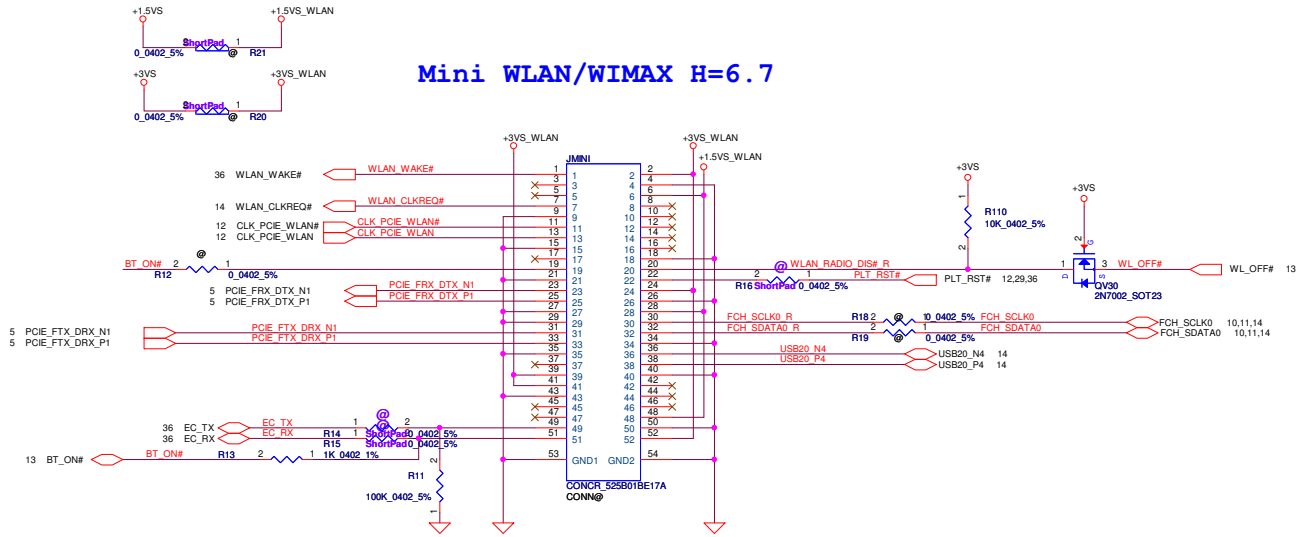


**USB conn. 4**

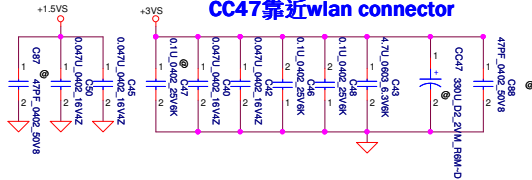


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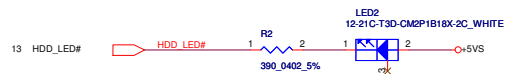
# Mini WLAN/WIMAX H=6.7



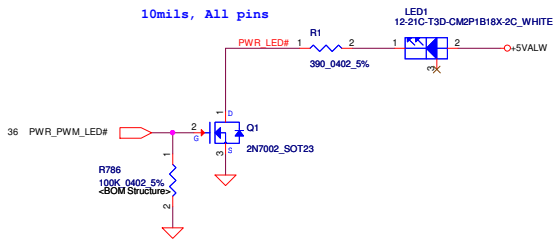
## CC47靠近wlan connector



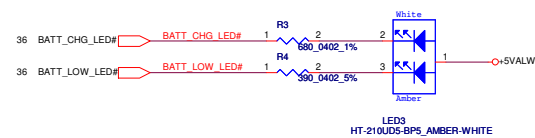
## HDD LED



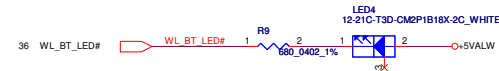
## Power LED



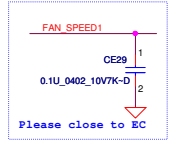
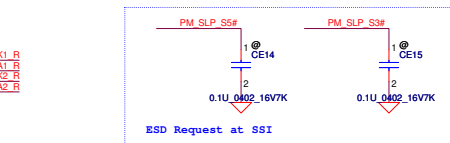
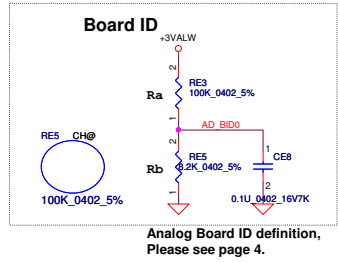
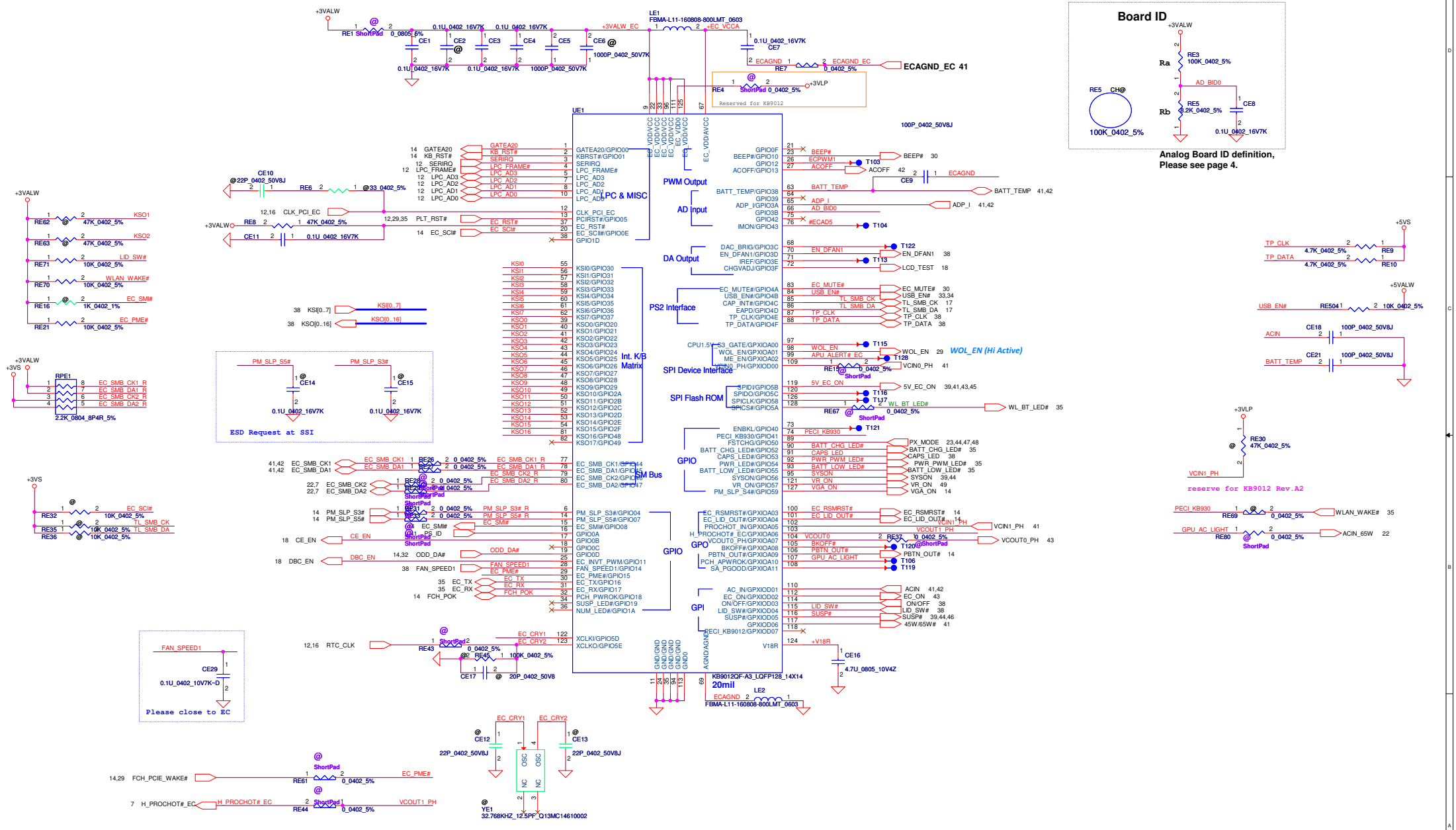
## Battery LED



## Wireless LED

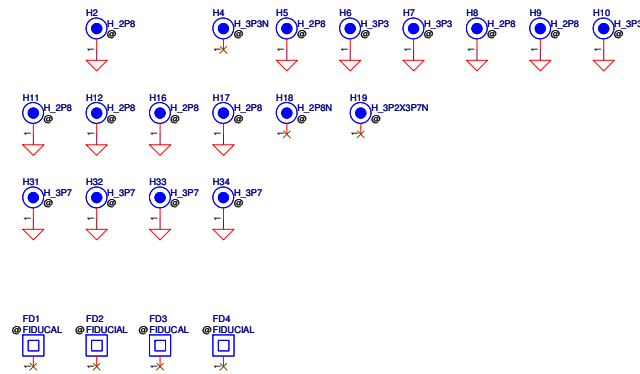


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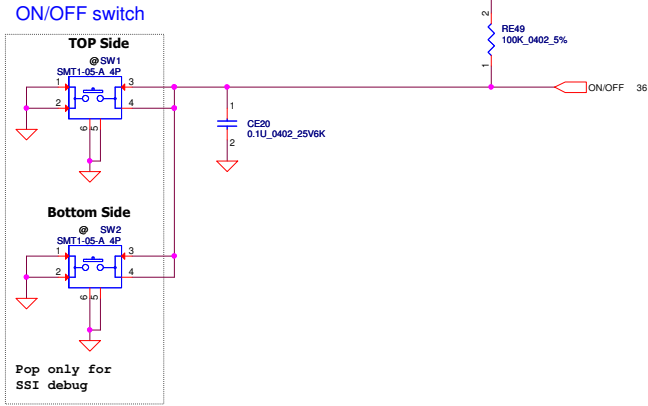
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		EC ENE-KB9012	
2012/09/11		2014/03/12		Document Number	
				LA-9103P	
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Date:		Tuesday, November 27, 2012		Sheet 36 of 52	

### Screw Hole

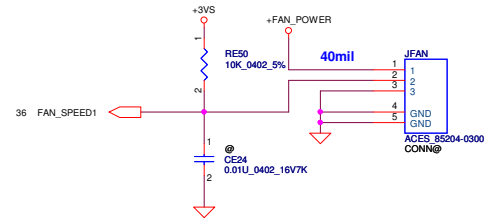
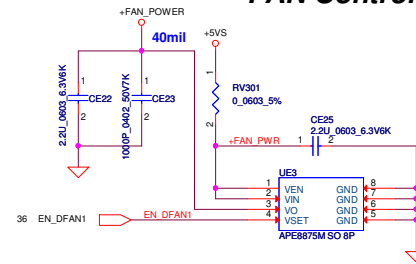


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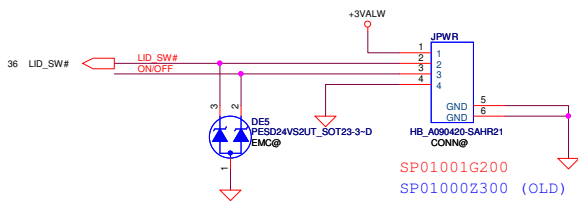
### Power ON Circuit



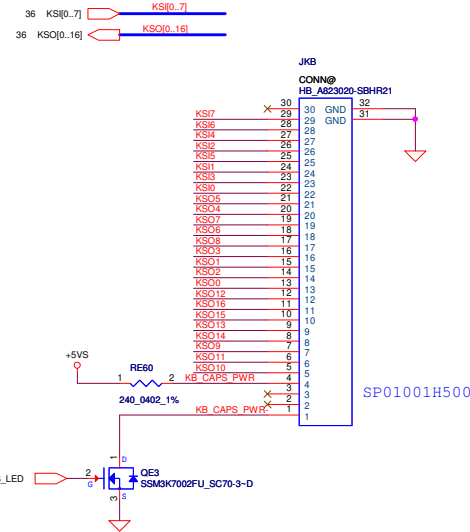
### FAN Control circuit



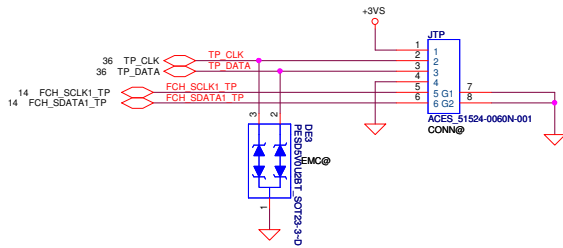
### POWER/B



### INT\_KBD Conn.

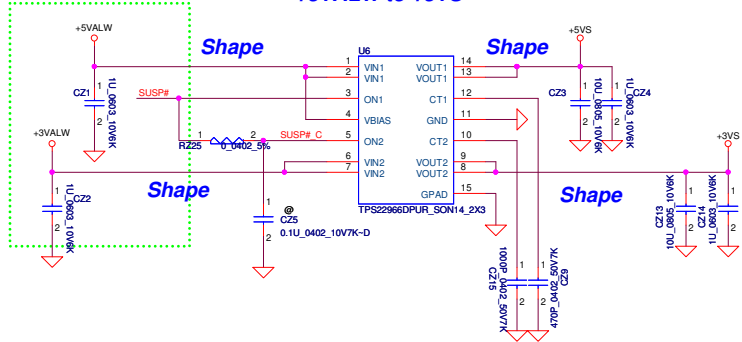


### Touch pad

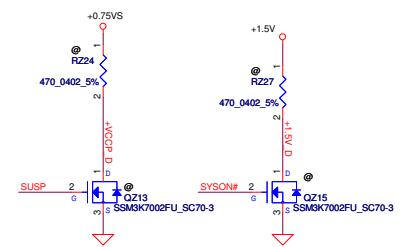
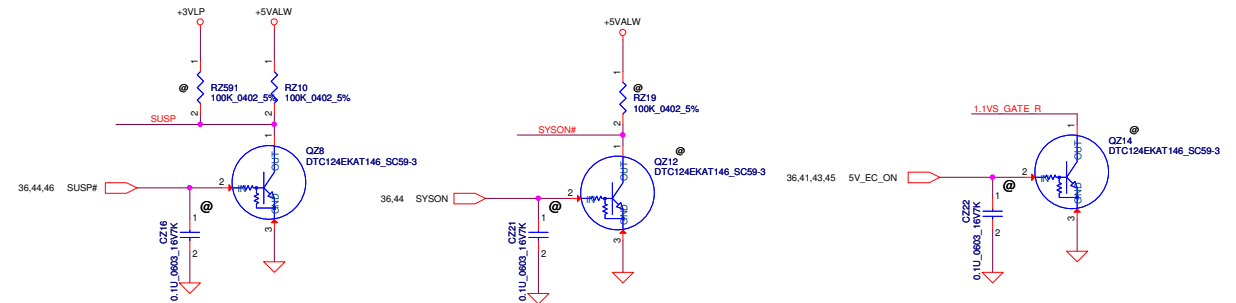
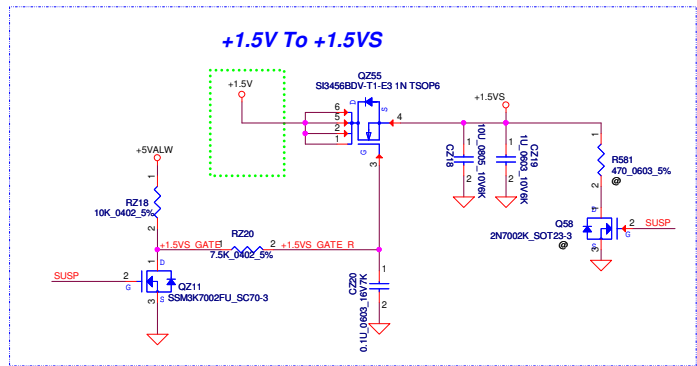
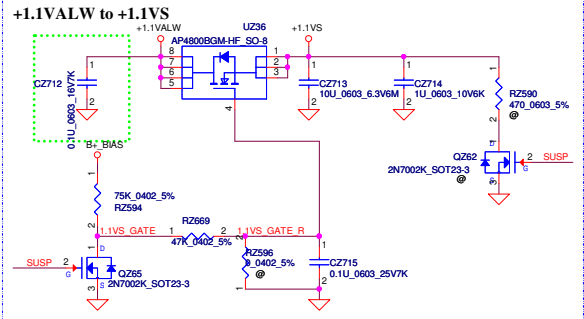


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				Rev 0.1

**+5VALW to +5VS**  
**+3VALW to +3VS**



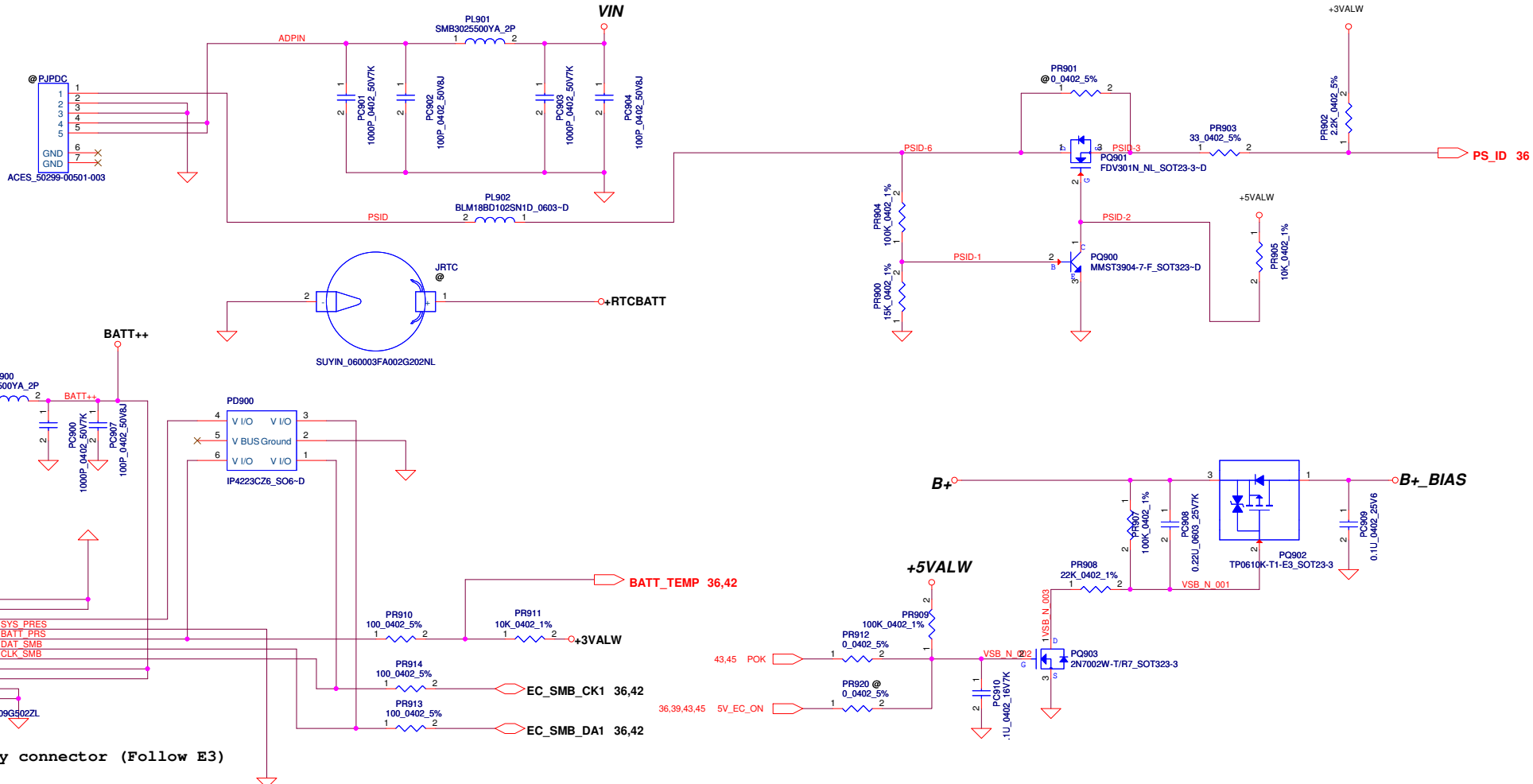
CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



*Version Change List (P. I. R. List)*

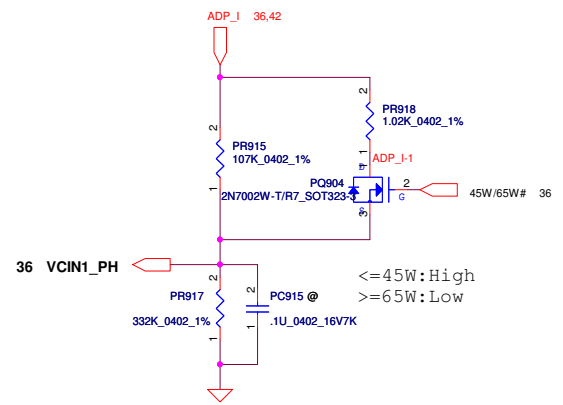
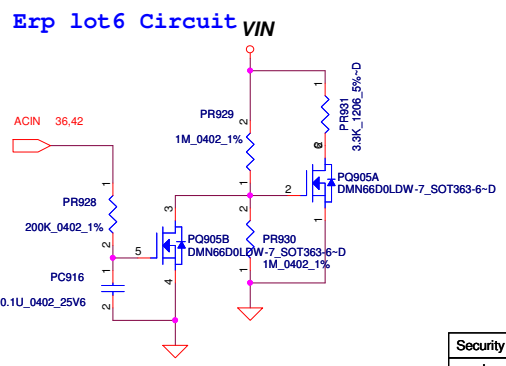
<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
1	08,11,12	DIMM	11/07/28	COMPAL	The M3 traces are routed to the Sandy Bridge Processor reserved pins for DDR3 VREF	Intel CHKLST Rev1.5 required	0.1
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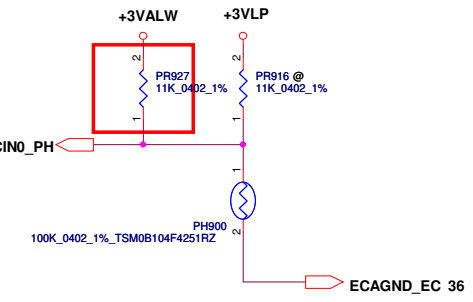


PBATT1 battery connector (Follow E3)

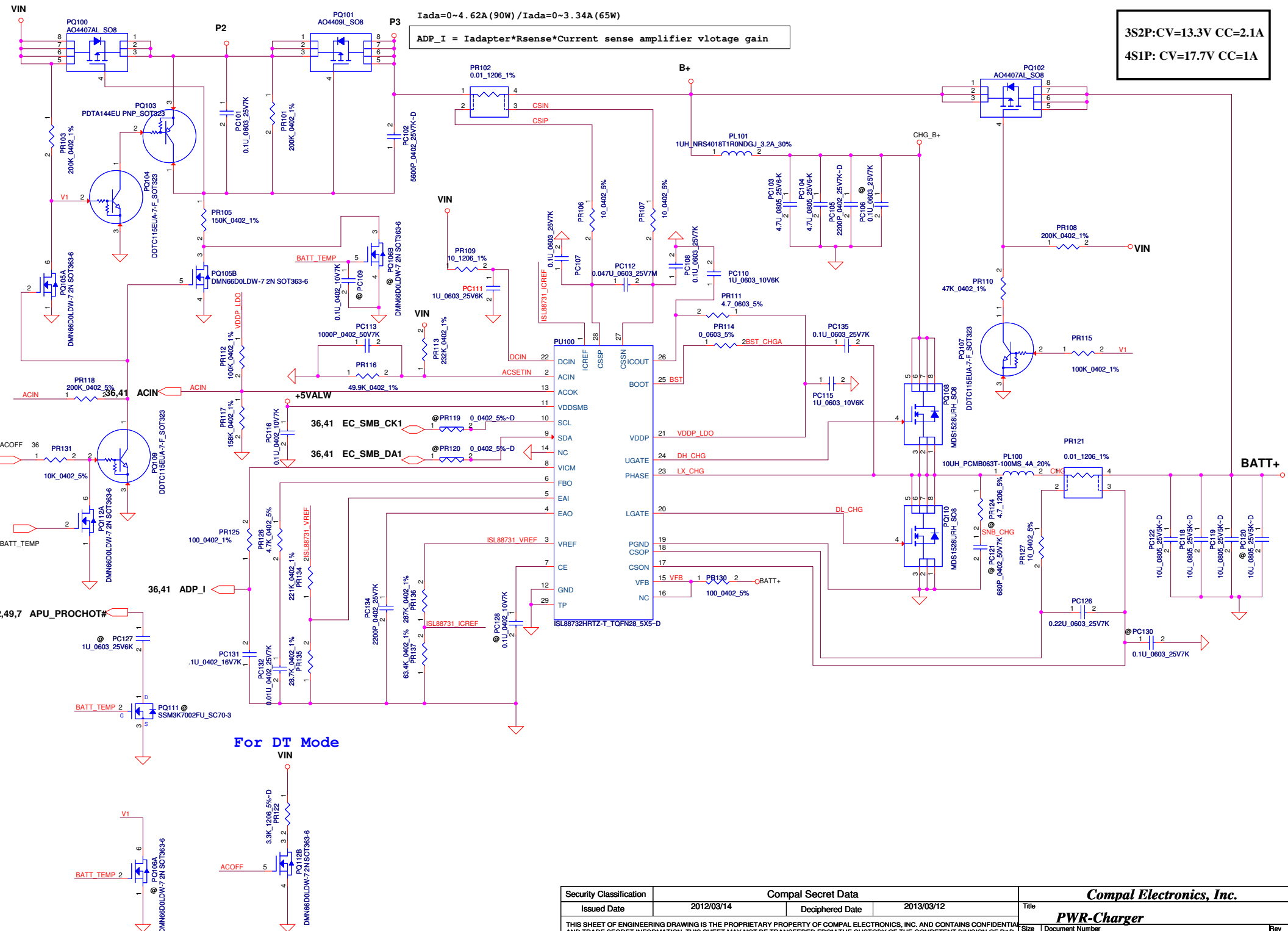
- SMART Battery:**
- 01.GND1
  - 02.GND2
  - 03.BAT\_ALERT
  - 04.SYS\_PRES
  - 05.BATT\_PRS
  - 06.DAT\_SMB
  - 07.CLK\_SMB
  - 08.BATT1 +
  - 09.BATT2+



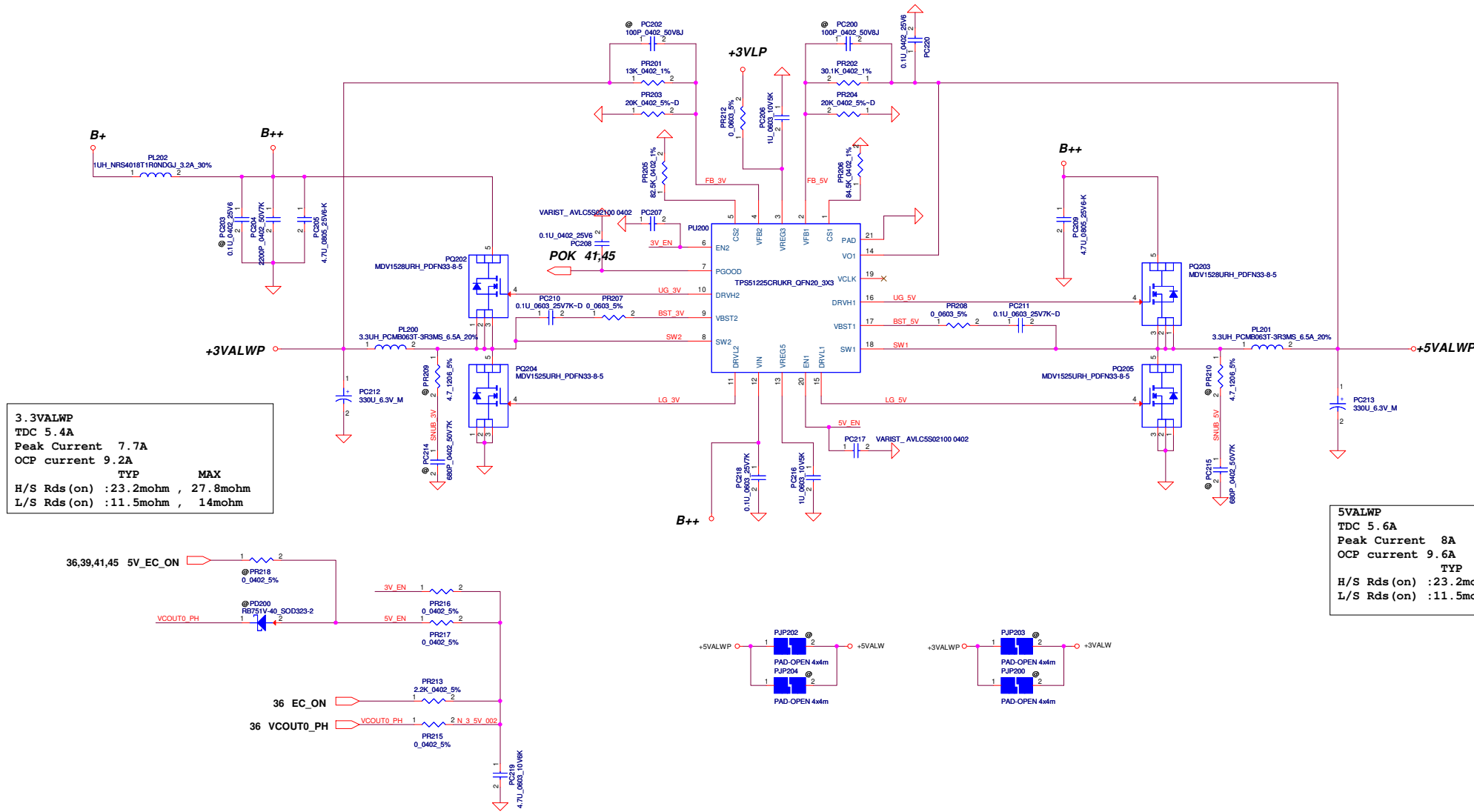
PH900 under CPU bottom side :  
CPU thermal protection at 96 degree C



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Size	Document Number	Rev	0.1	Date:	Tuesday, November 27, 2012
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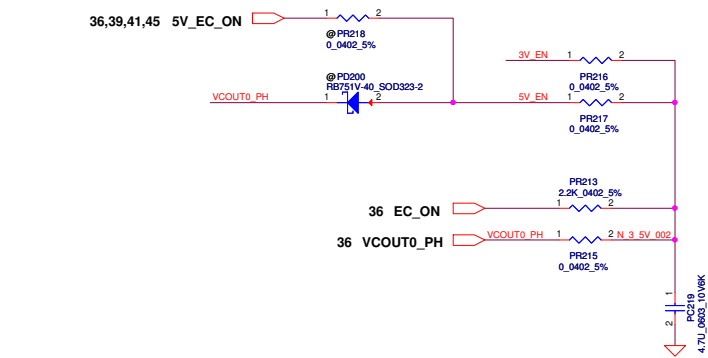


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				Document Number	
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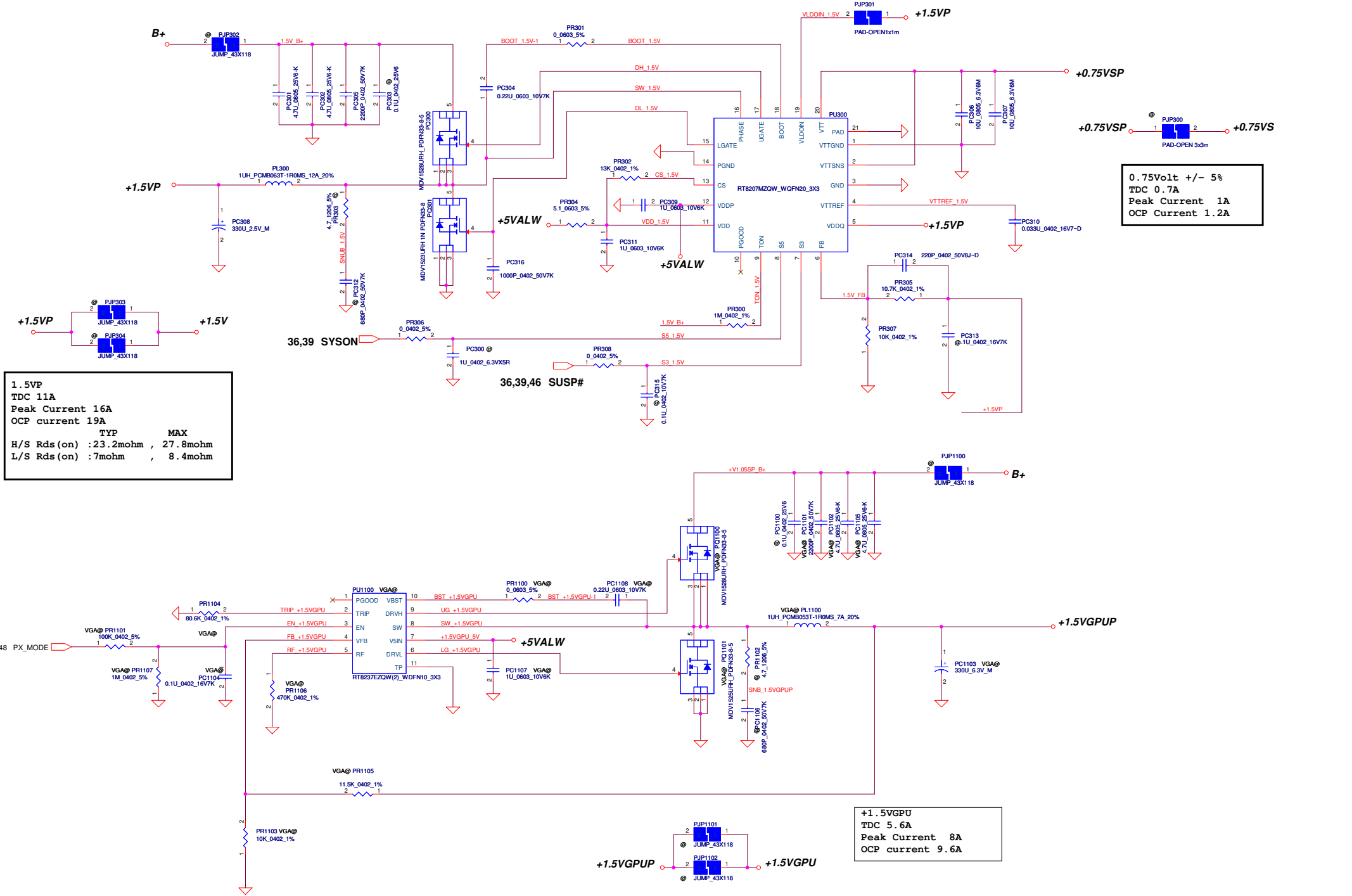


**3.3VALWP**  
 TDC 5.4A  
 Peak Current 7.7A  
 OCP current 9.2A  
 TYP            MAX  
 H/S Rds (on) : 23.2mohm , 27.8mohm  
 L/S Rds (on) : 11.5mohm , 14mohm

**5VALWP**  
 TDC 5.6A  
 Peak Current 8A  
 OCP current 9.6A  
 TYP            MAX  
 H/S Rds (on) : 23.2mohm , 27.8mohm  
 L/S Rds (on) : 11.5mohm , 14mohm



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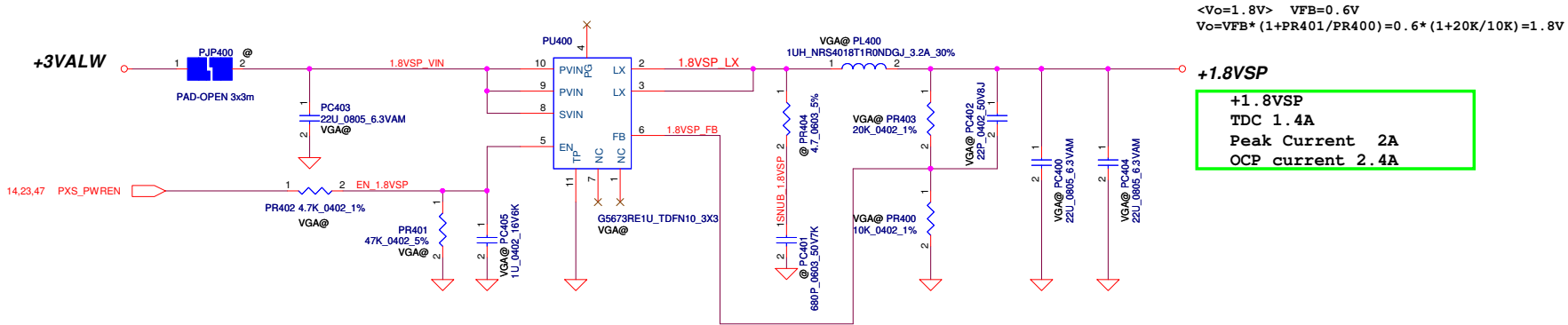


**1.5VP**  
 TDC 11A  
 Peak Current 16A  
 OCP current 19A  
 TYP            MAX  
 H/S Rds (on) : 23.2mohm , 27.8mohm  
 L/S Rds (on) : 7mohm       , 8.4mohm

0.75VOLT +/- 5%  
 TDC 0.7A  
 Peak Current 1A  
 OCP Current 1.2A

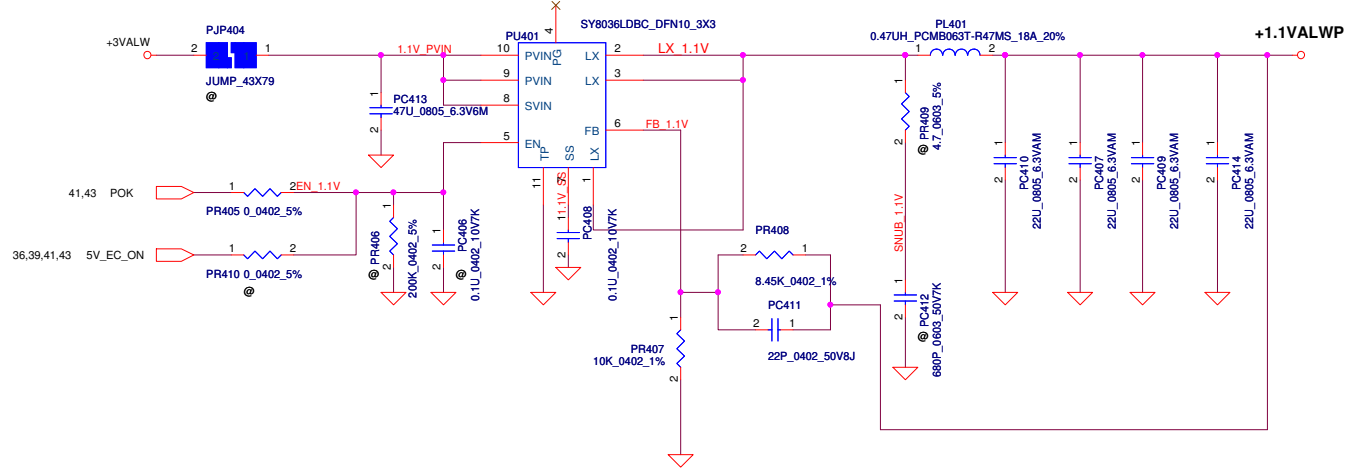
**+1.5VGPU**  
 TDC 5.6A  
 Peak Current 8A  
 OCP current 9.6A

Security Classification	Compal Secret Data		Title	
Issued Date	2012/03/14	Deciphered Date	2013/03/12	<b>PWR +1.5VP/+1.5VGPUP/0.75VSP</b>
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<V<sub>o</sub>=1.8V> VFB=0.6V  
 $V_o = VFB * (1 + PR401 / PR400) = 0.6 * (1 + 20K / 10K) = 1.8V$

**+1.8VSP**  
 TDC 1.4A  
 Peak Current 2A  
 OCP current 2.4A

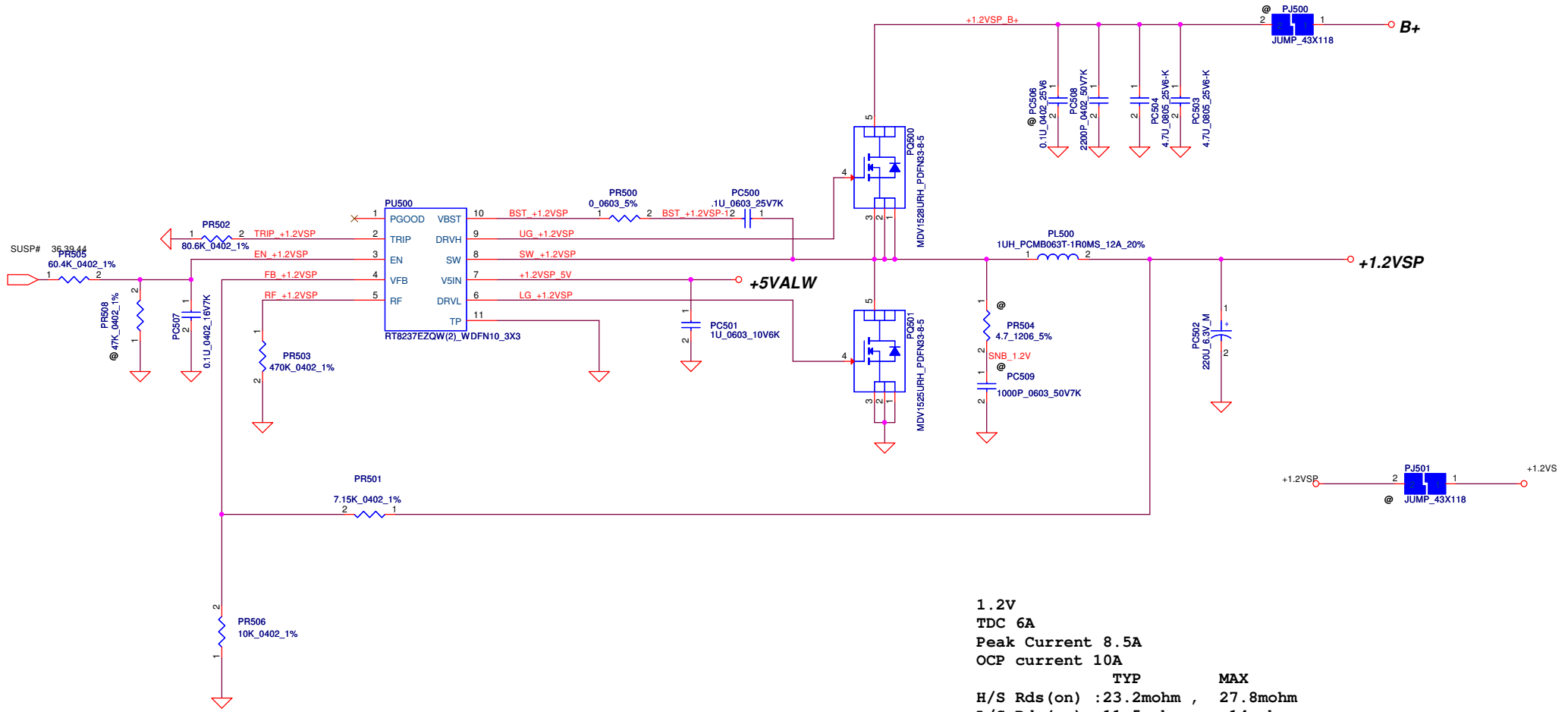


**1.1V**  
 TDC 3.5A  
 Peak Current 5A  
 OCP current 6A

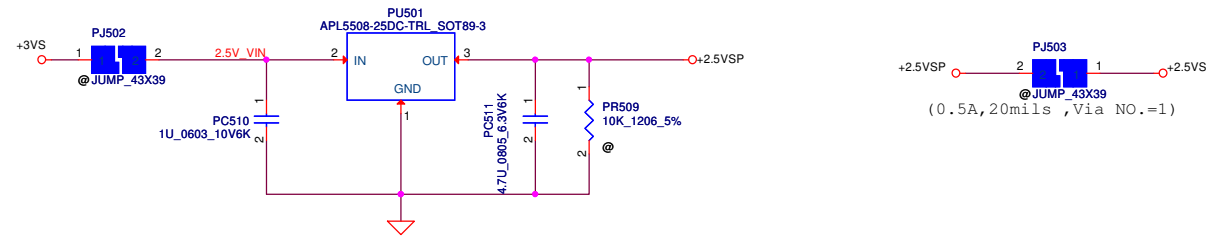
	TYP	MAX
H/S Rds (on)	: 27mohm	, 34mohm
L/S Rds (on)	: 11mohm	, 14mohm



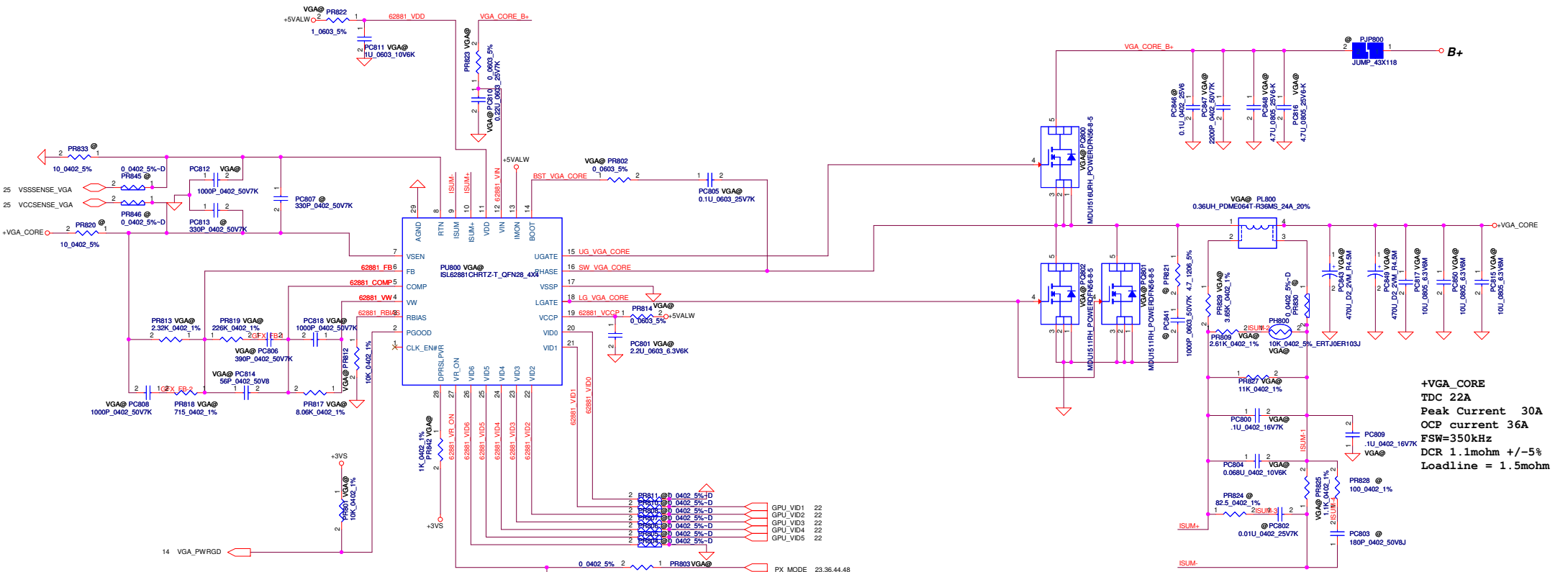
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
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**1.2V**  
**TDC 6A**  
**Peak Current 8.5A**  
**OCP current 10A**  
**TYP                    MAX**  
**H/S Rds (on) :23.2mohm , 27.8mohm**  
**L/S Rds (on) :11.5mohm , 14mohm**



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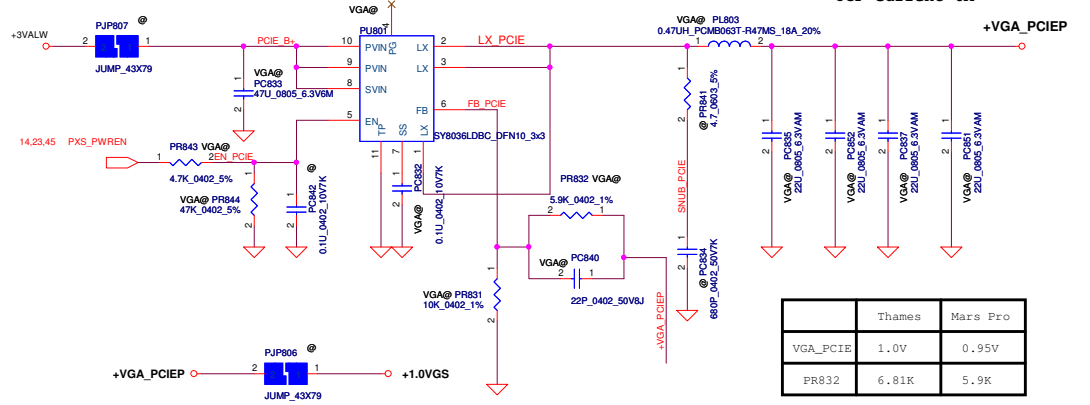
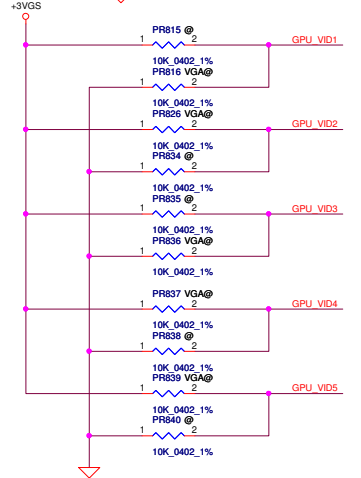


**+VGA\_CORE**  
 TDC 22A  
 Peak Current 30A  
 OCP current 36A  
 FSW=350kHz  
 DCR 1.1mohm +/-5%  
 Loadline = 1.5mohm

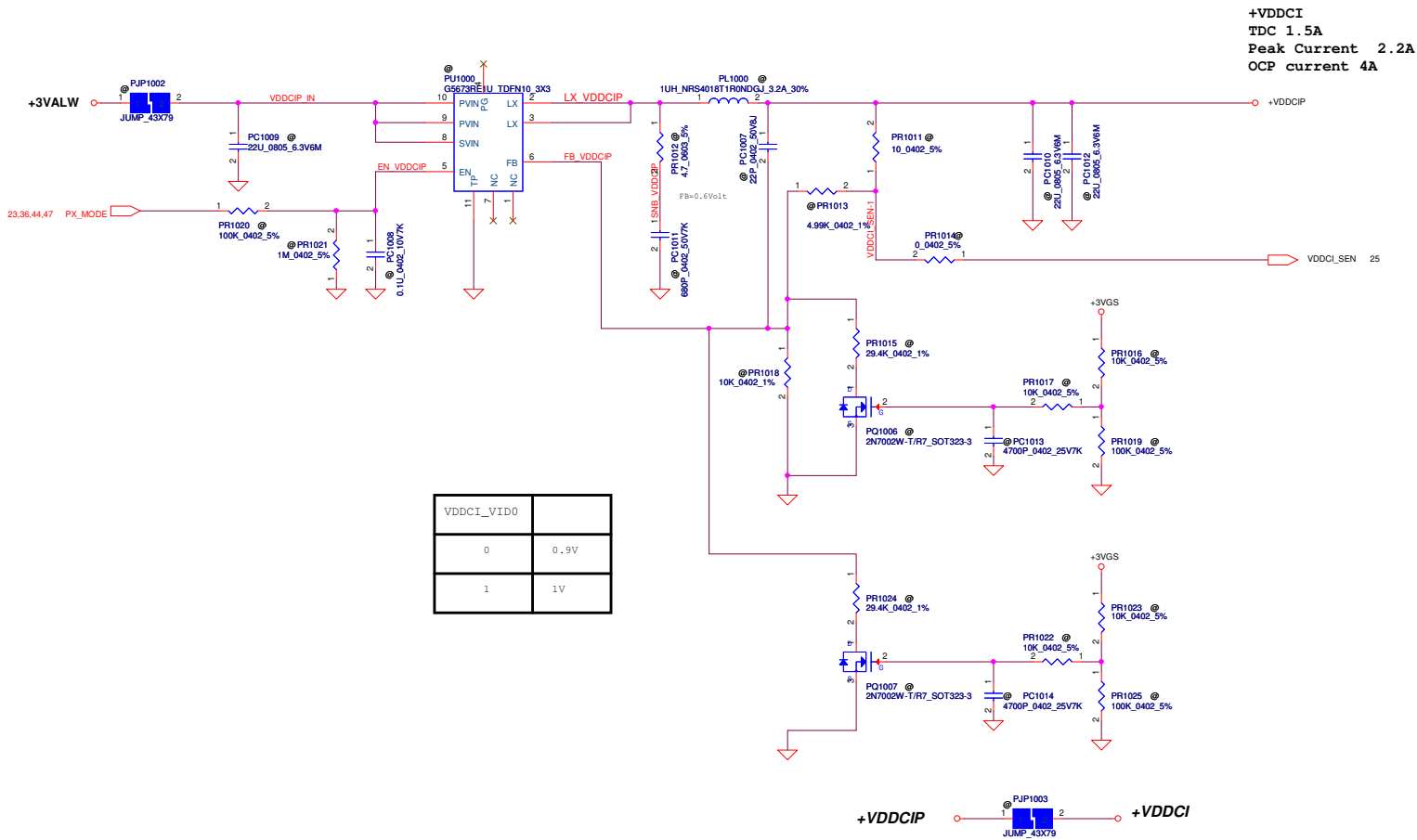
**+VGA\_PCIE**  
 TDC 3.6A  
 Peak Current 5.2A  
 OCP current 6A

Mars Pro

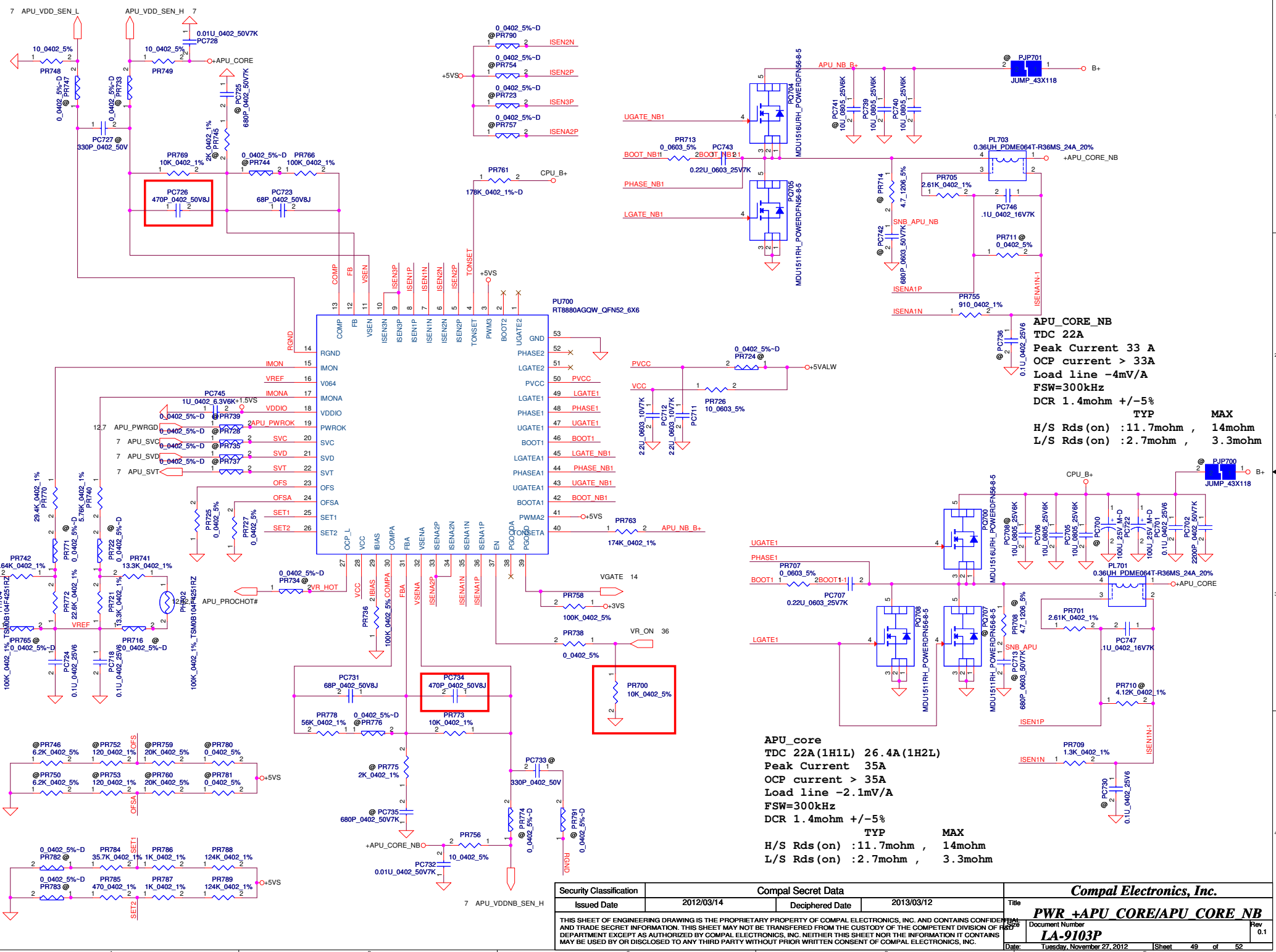
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V



	Thames	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K



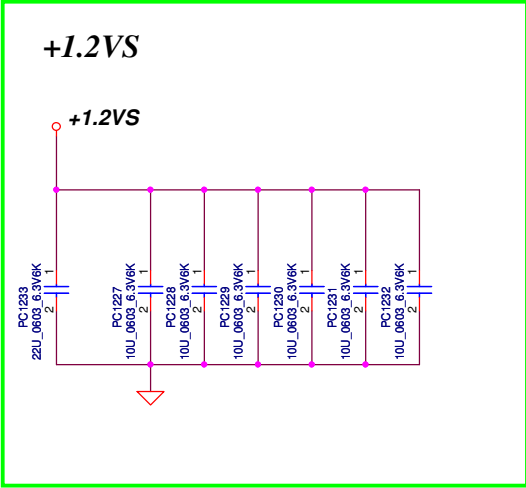
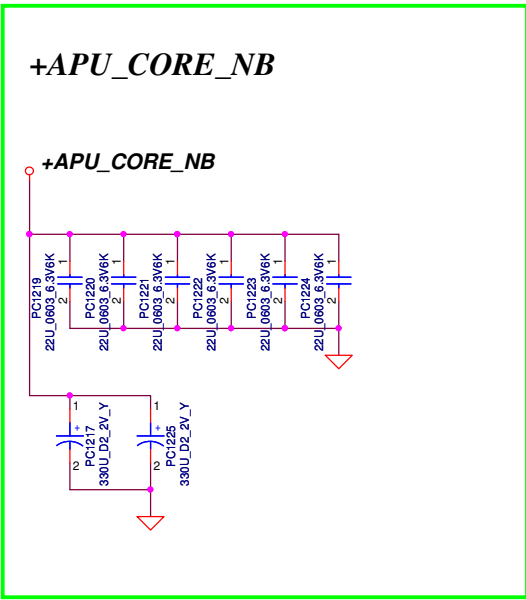
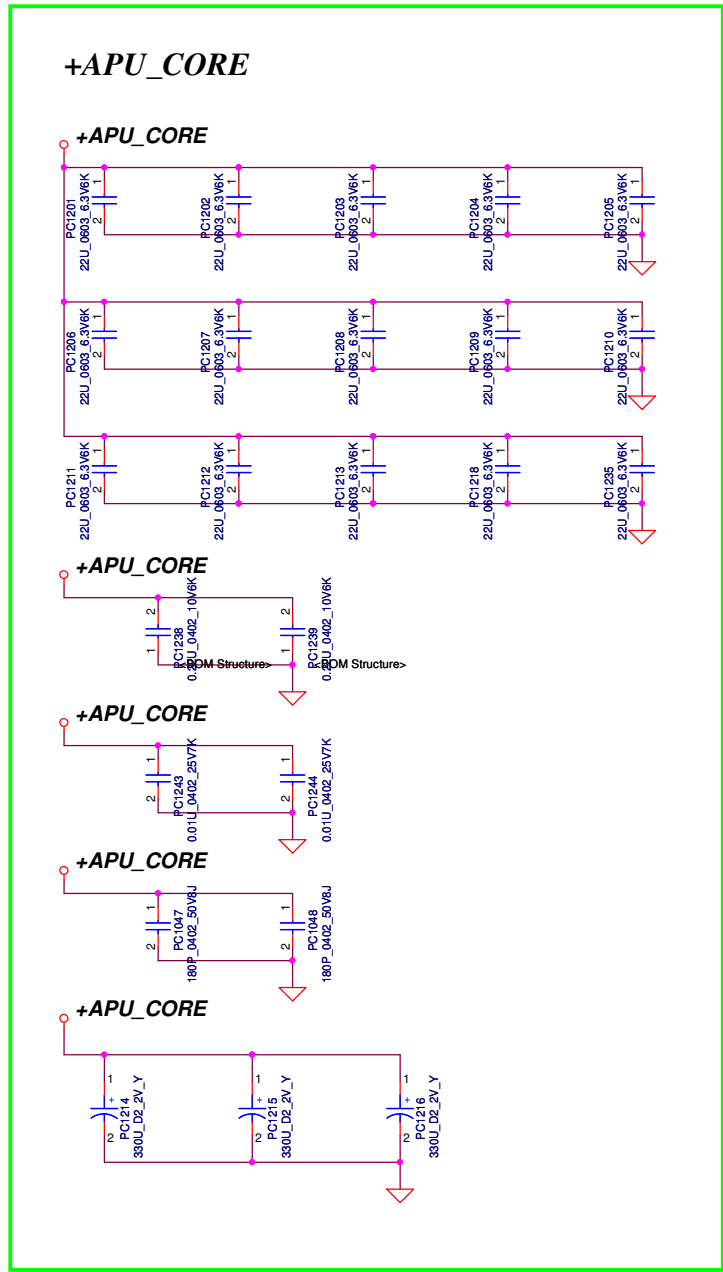




**APU\_CORE\_NB**  
**TDC 22A**  
 Peak Current 33 A  
 OCP current > 33A  
 Load line -4mV/A  
 FSW=300kHz  
 DCR 1.4mohm +/-5%  
 TYP MAX  
 H/S Rds (on) : 11.7mohm , 14mohm  
 L/S Rds (on) : 2.7mohm , 3.3mohm

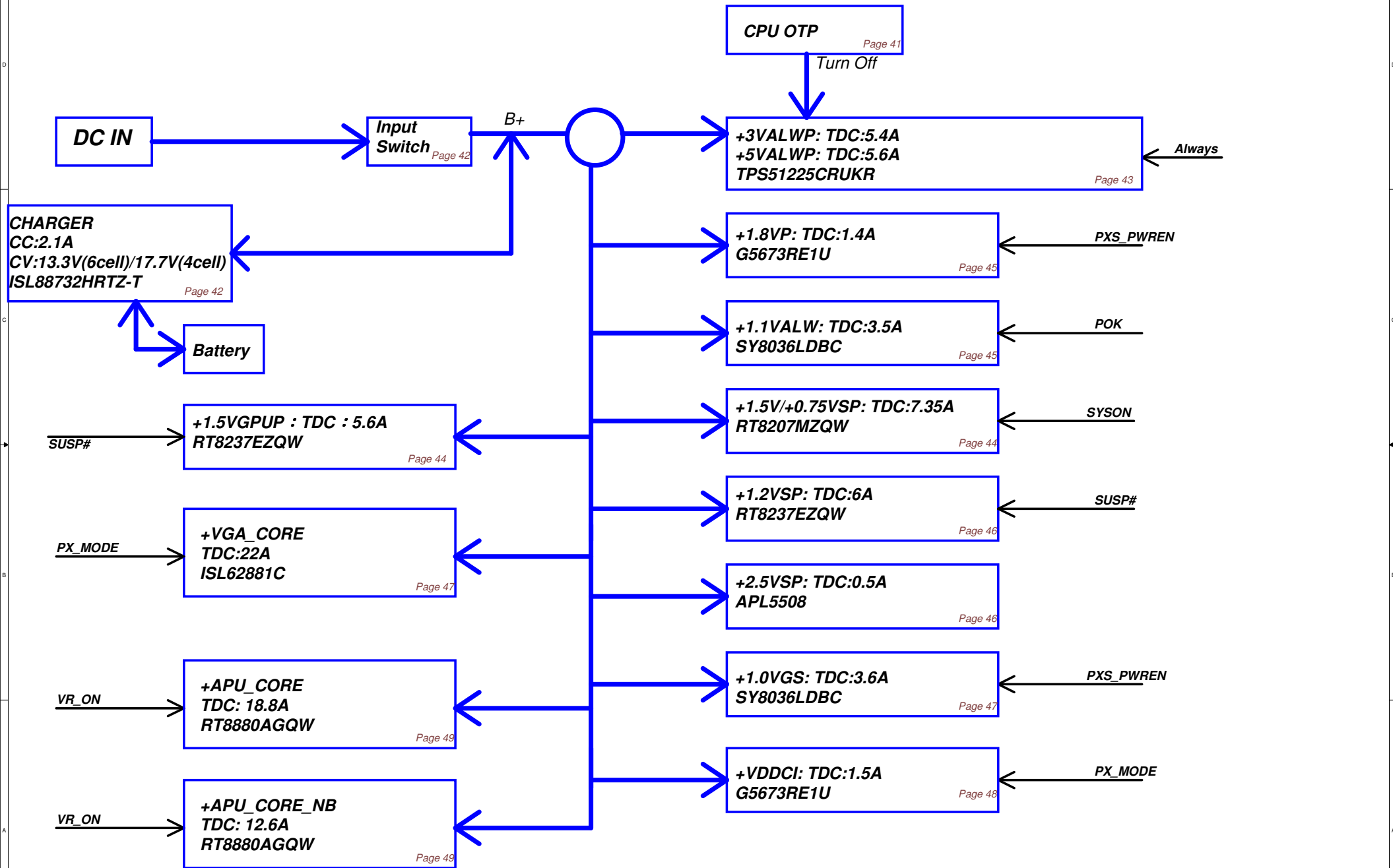
**APU\_core**  
**TDC 22A(1H1L) 26.4A(1H2L)**  
 Peak Current 35A  
 OCP current > 35A  
 Load line -2.1mV/A  
 FSW=300kHz  
 DCR 1.4mohm +/-5%  
 TYP MAX  
 H/S Rds (on) : 11.7mohm , 14mohm  
 L/S Rds (on) : 2.7mohm , 3.3mohm

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# Power block



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