

1 2 3 4 5
Compal Confidential

Model Name : ZIPS1

File Name : LA-A341P

BOM P/N:



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Stella M/B Schematics Document

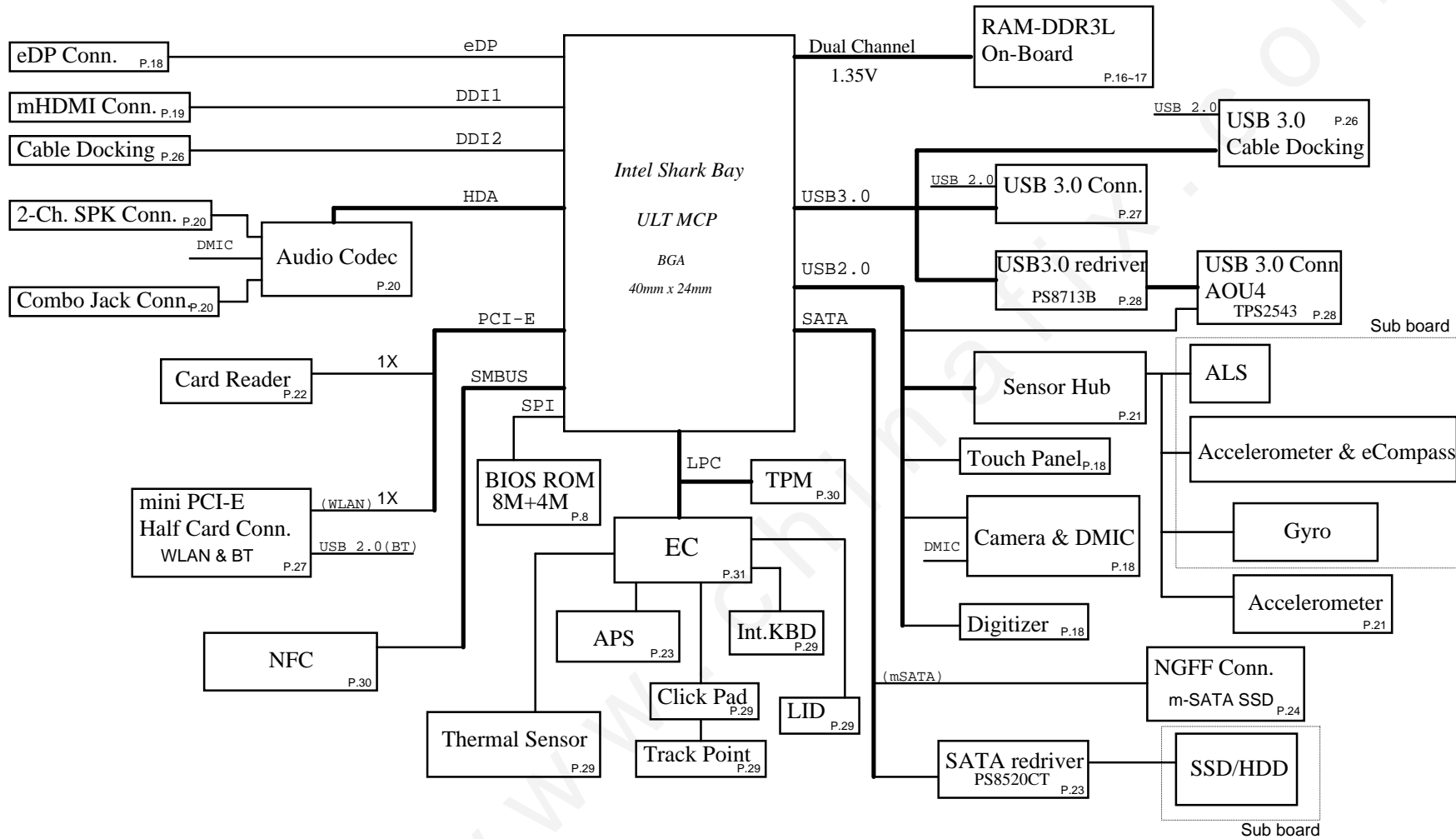
Intel Shark Bay ULT Processor with DDR3L

Rev. 1A_20130902A

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Model Name : ST-Note
File Name : Block Diagram



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Voltage Rails

power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +VCCP +CPU_CORE	+3VM +1.05VM
				+0.675VS +1.05VS	
State					
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only (AOU Disable)	X	X	X	X	
S5 S4/AC & Battery don't exist (AOU Disable)	X	X	X	X	

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger	0001 011X b	12H

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor Fintek F75303M	1001_101xb	9AH
Synaptics Inter Touch Click Pad	0010_110xb	2CH

PCH SM Bus address

Device	Address	HEX
Security Rom	1010 100xb	A8H

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
EMI Mount	EMI@
dGPU	DIS@
Intel UMA	UMA@
AOAC	AOAC@
TPM	TPM@
SBA	SBA@
Non-SBA	NOSBA@
DRAM Option	DDR1@
Unpop	@
EMI Un-Mount	@EMI@

USB 2.0 Port Table

USB 2.0 Port	3 External USB Port
0	USB 3.0 Port + AOU (Left)
1	USB 3.0 Port (Right)
2	USB 3.0 Port (Docking)
3	Mini Card (WLAN/BT)
4	Touch Screen
5	Camera
6	Sensor Hub
7	Digitizer

USB 3.0 Port Table

Port	
1	USB 3.0 Port (Left)
2	USB 3.0 Port (Right)
3	USB 3.0 Port (Docking)
4	

PCIe Port Table

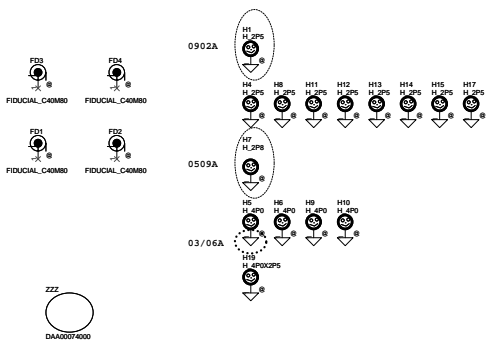
Port	Lane	
1		
2		
3		WLAN
4		Cardreader
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

SATA Port Table

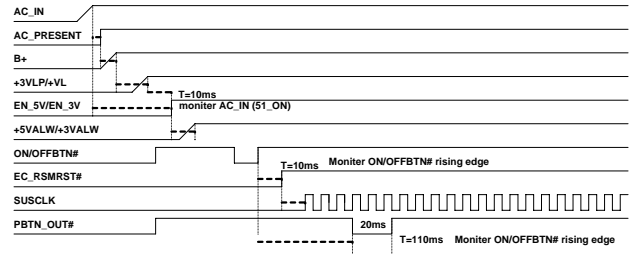
Port	
0	HDD
1	NGFF SSD
2	
3	



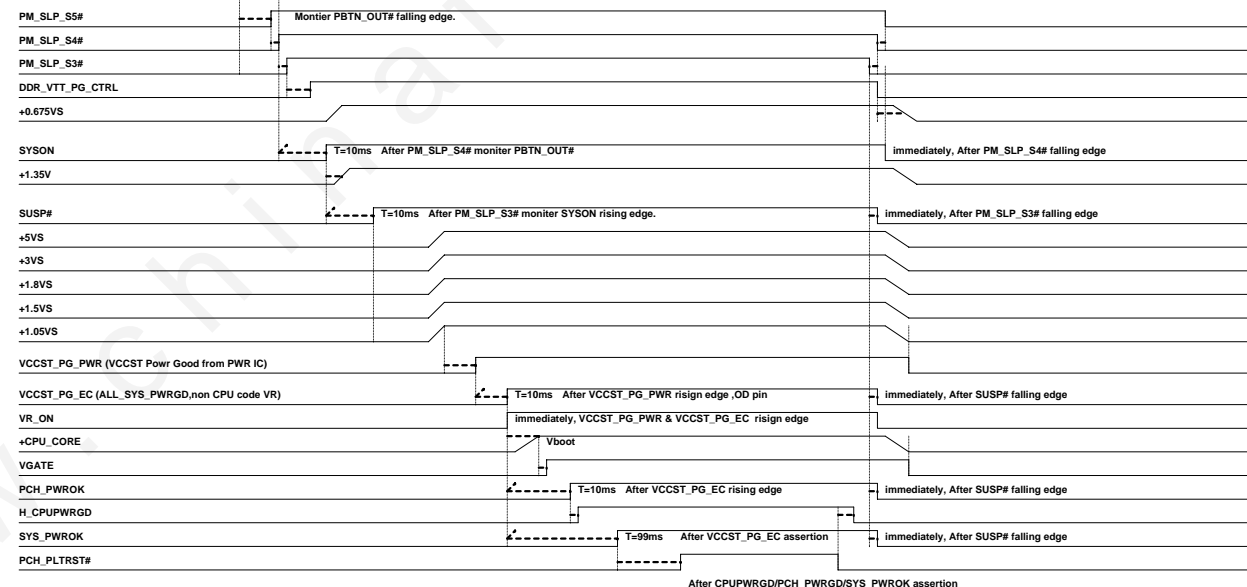
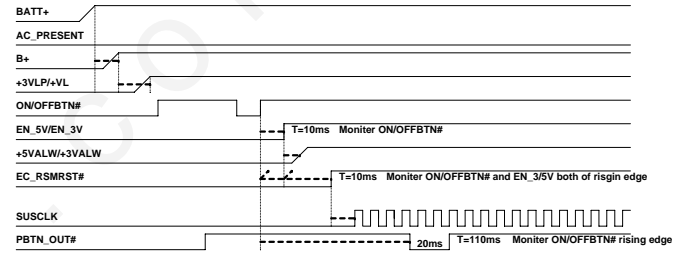
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[AC Mode]

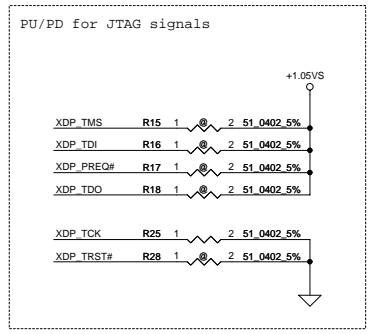
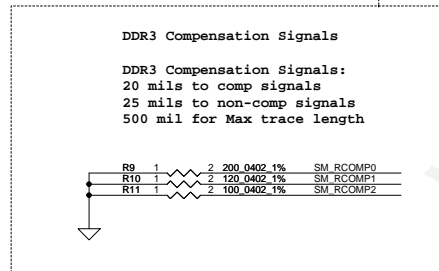
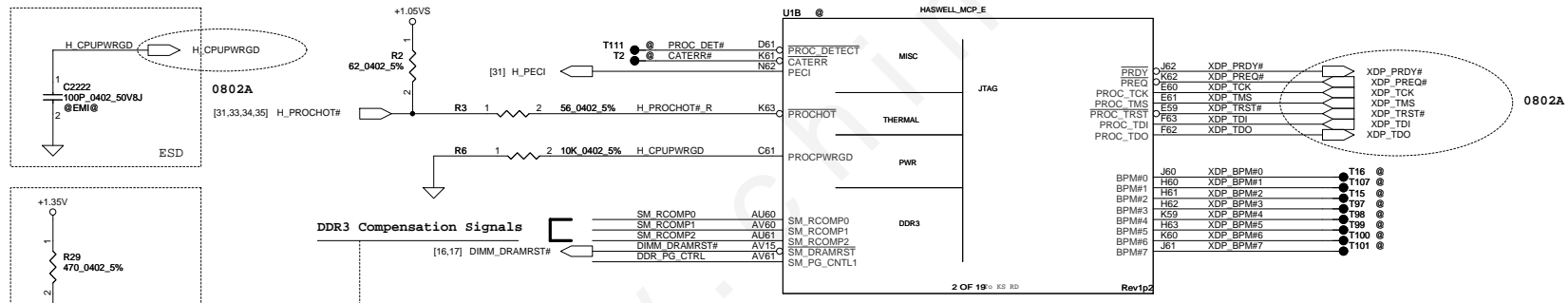
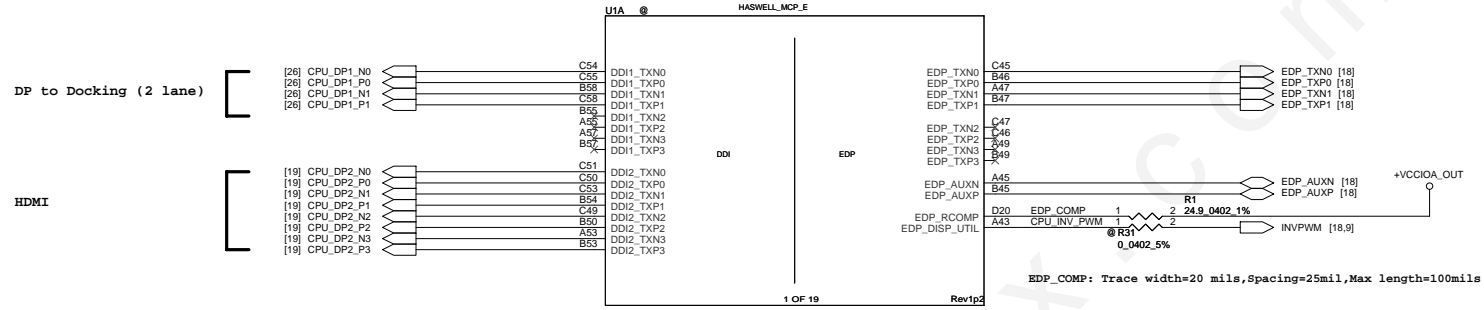


[DC Mode]



RAM_ID3 GPIO4E	RAM_ID2 GPIO47	RAM_ID1 GPIO48	RAM_ID0 GPIO49	RAM
0	0	0	0	HYNIX 4GB
0	0	0	1	SAMSUNG 4GB
0	0	1	0	MICRON 4GB
0	0	1	1	ELPIDA 4GB
0	1	0	0	SAMSUNG 8GB
0	1	0	1	ELPIDA 8GB
0	1	1	0	MICRON 8GB
0	1	1	1	HYNIX 8GB
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

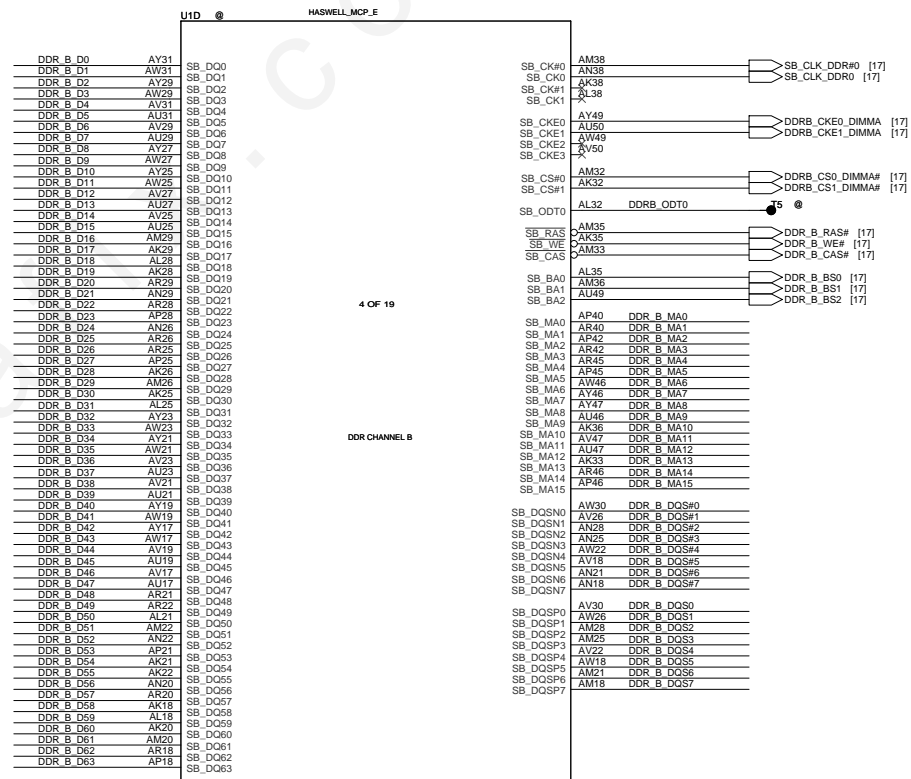
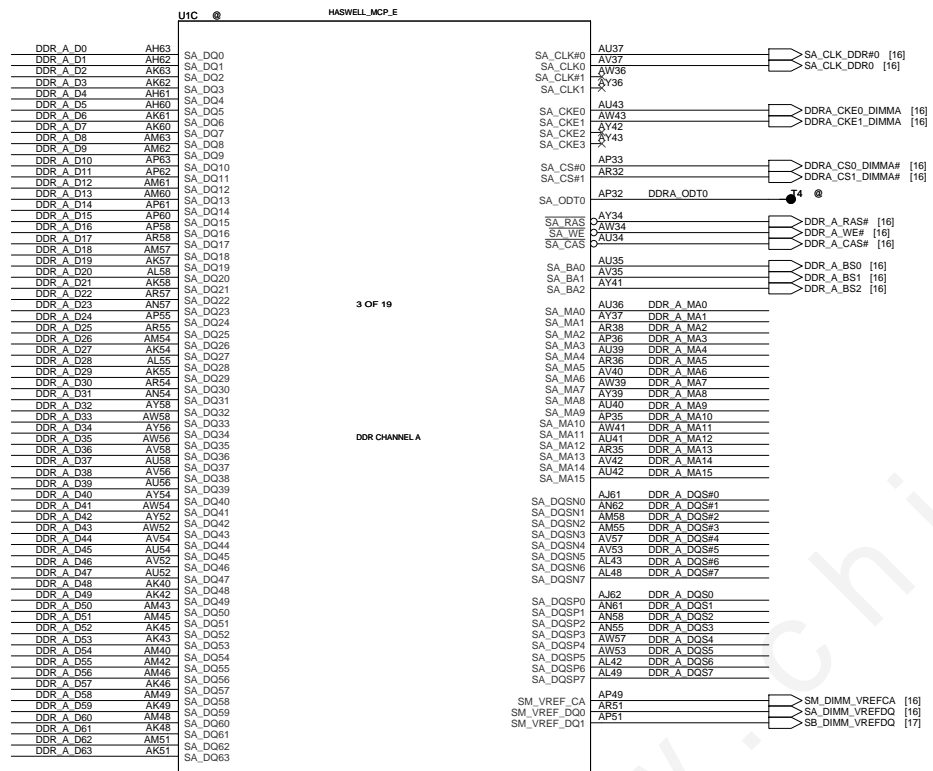
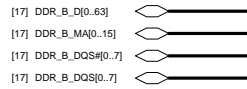
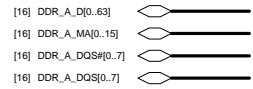
DDI/ MSIC/ XDP

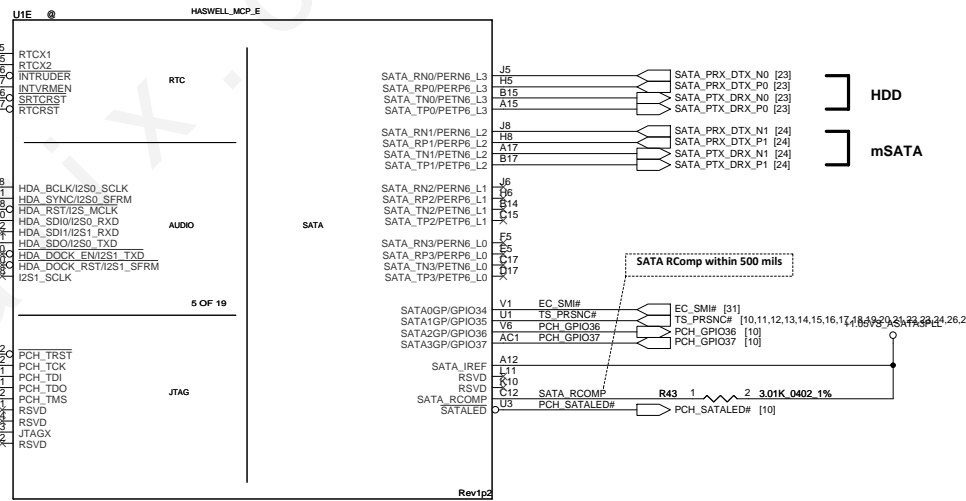
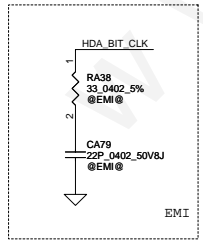
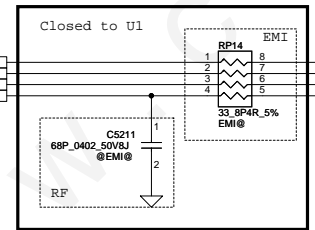
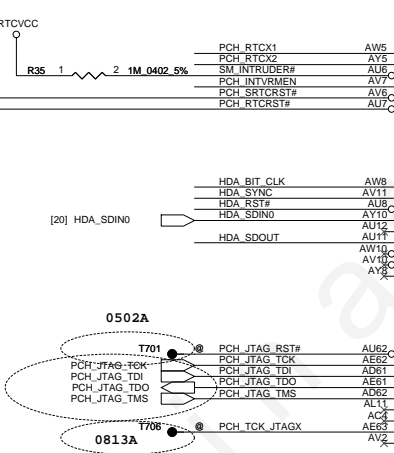
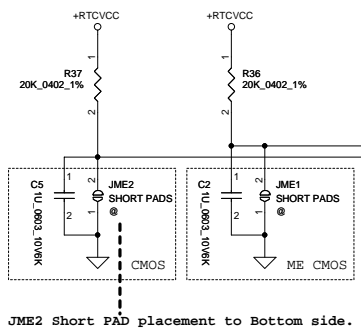
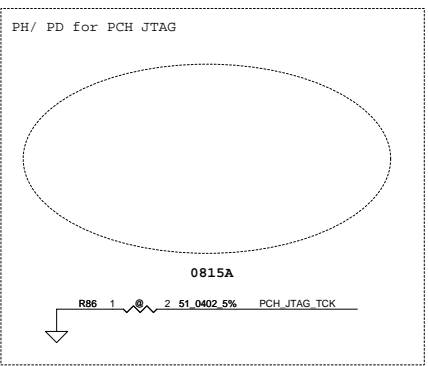
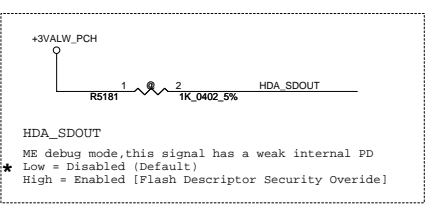
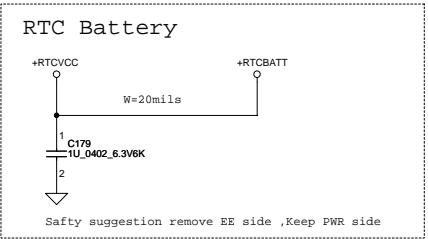
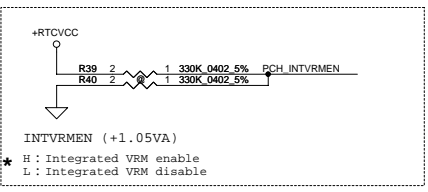
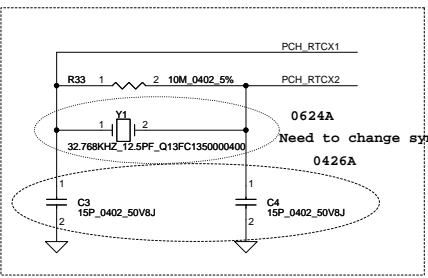


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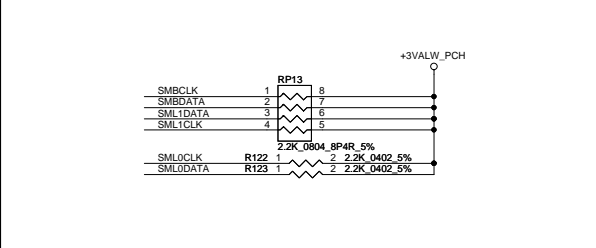
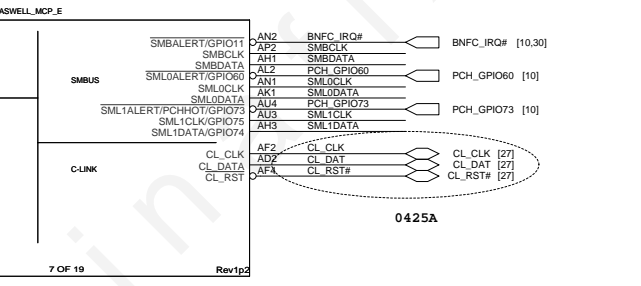
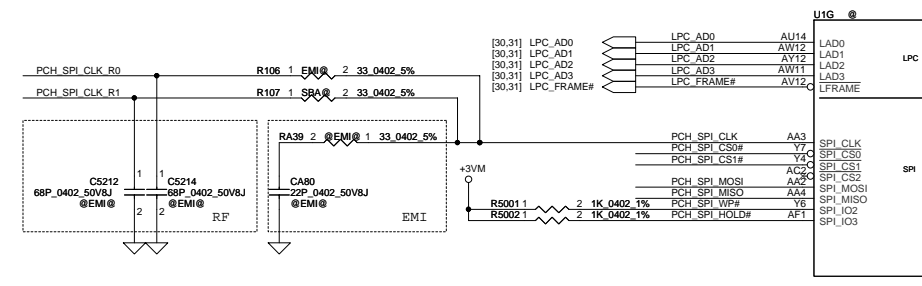
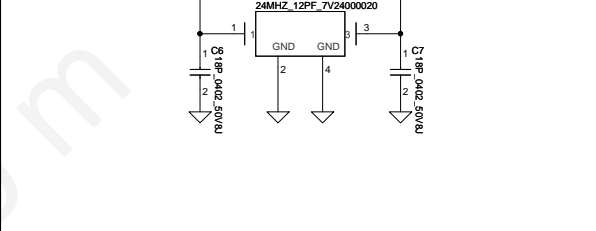
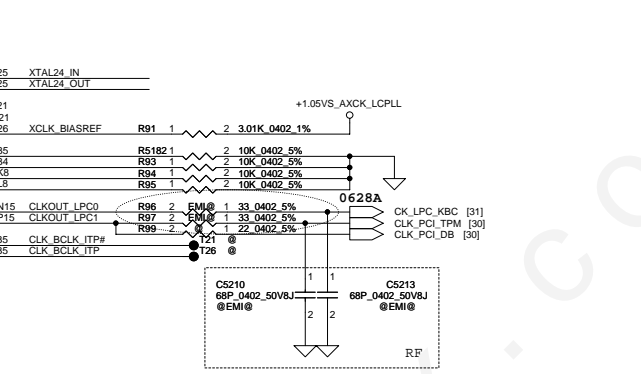
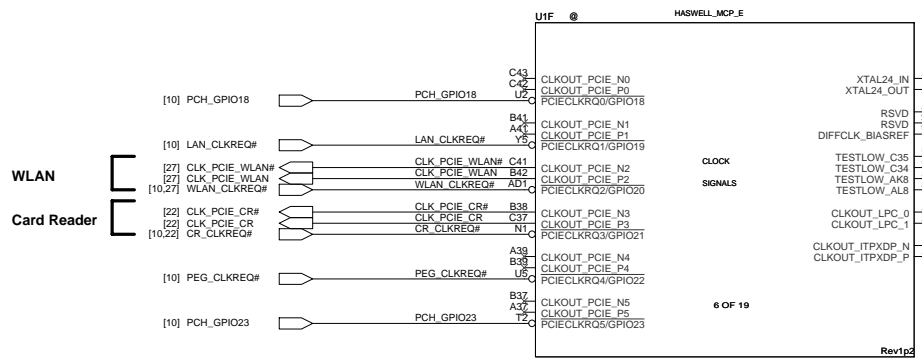


Memory I/F

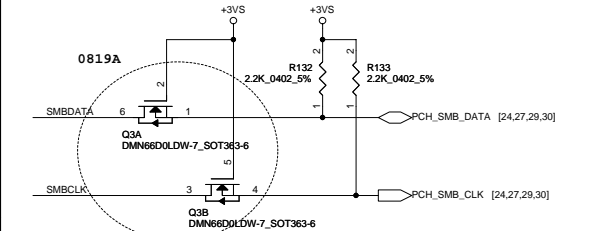




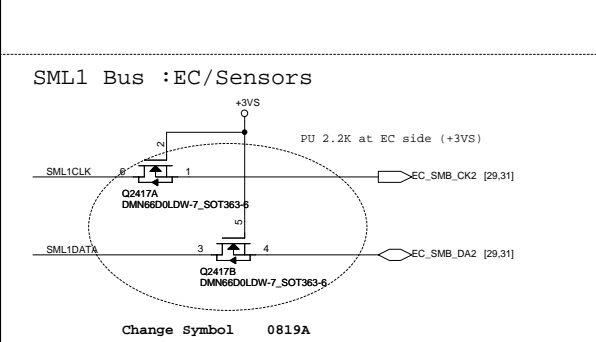
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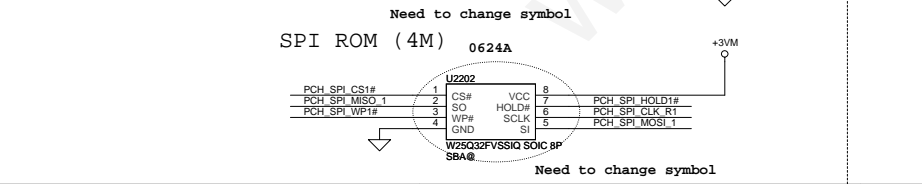
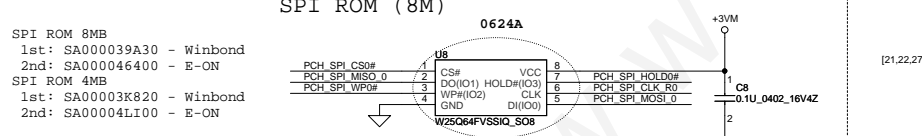
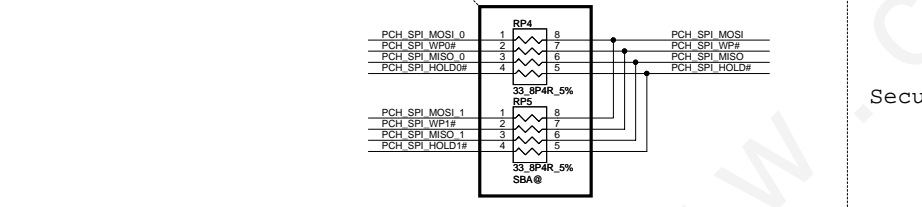
SMBus : SPD/PCIe/Security/TP/NFC



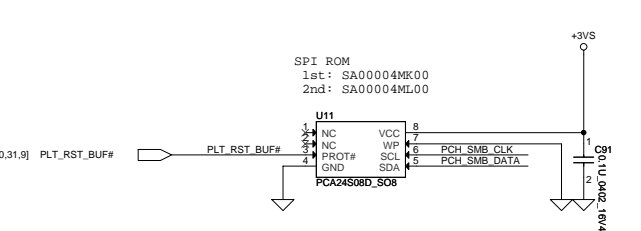
SML1 Bus : EC/Sensors



Non-SBA - 1 SPI Device = 15 ohm - P/N: SD300001P00

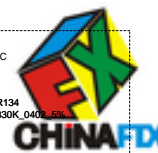


Security ROM



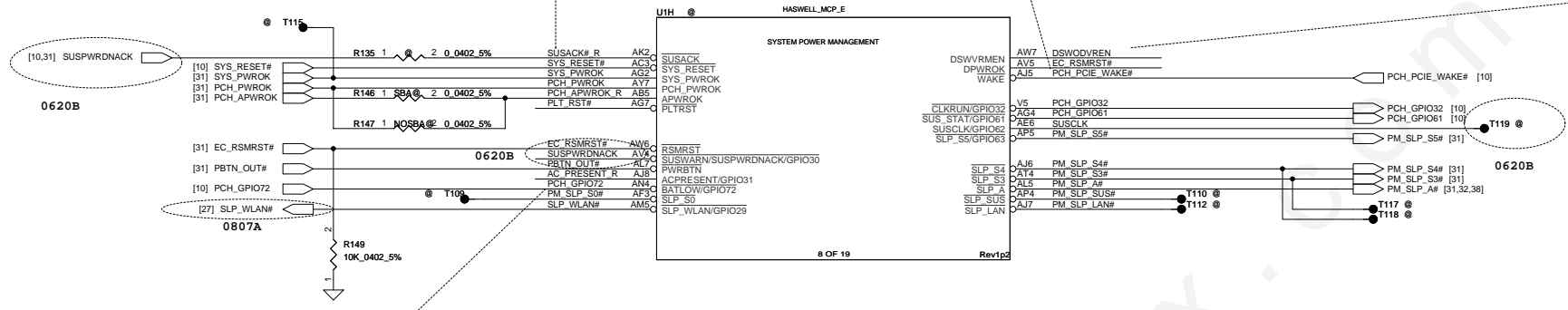
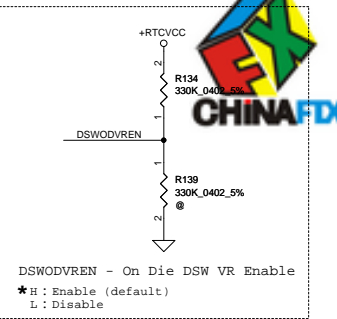
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PM/ GPIO/ DDI

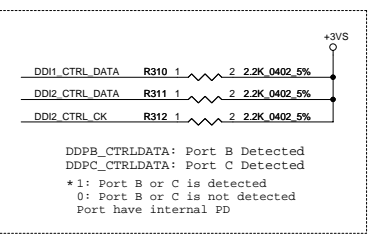
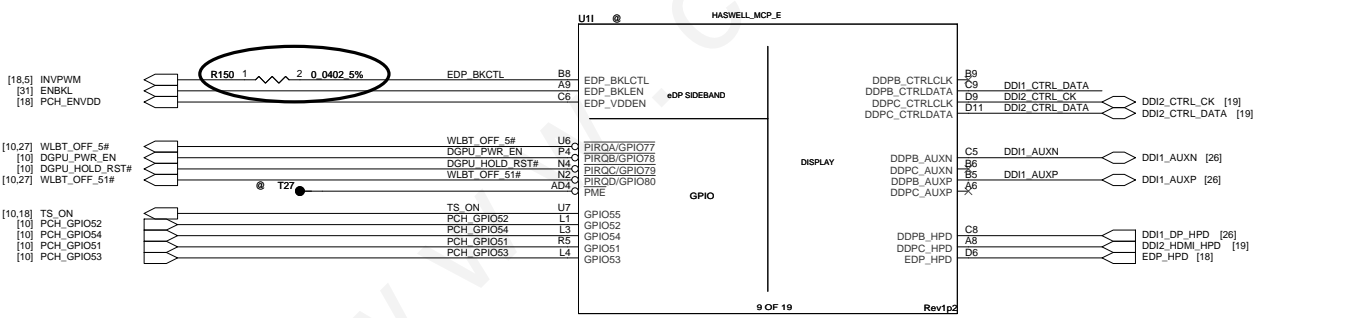
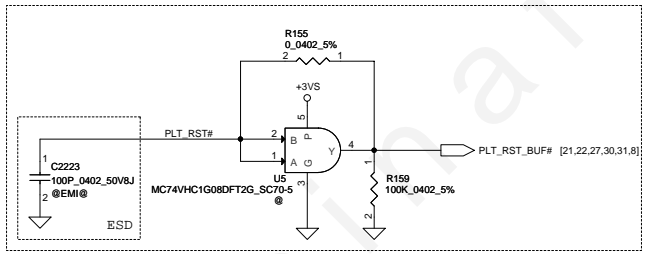
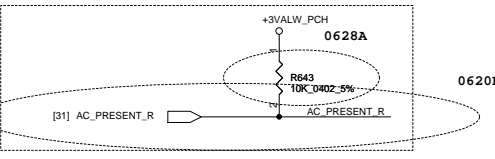


Note: SUSACK# and SUSWRN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit. CAN be NC, if not support Deep Sx

DPWROK: Tied together with RSMRST# that do not support Deep Sx



PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx, connect to VCCSUS3_3)

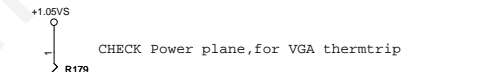
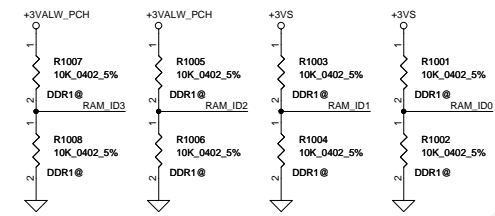
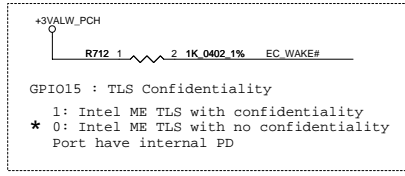
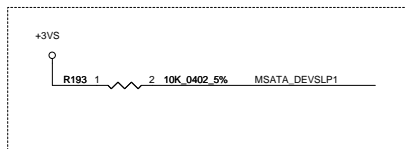


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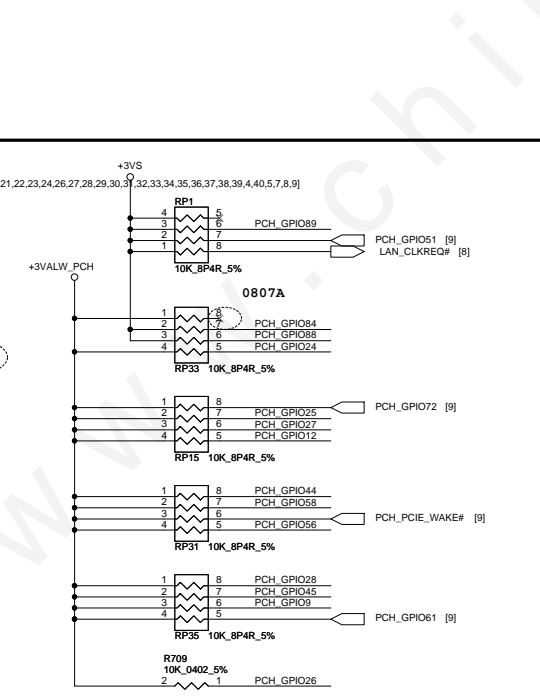
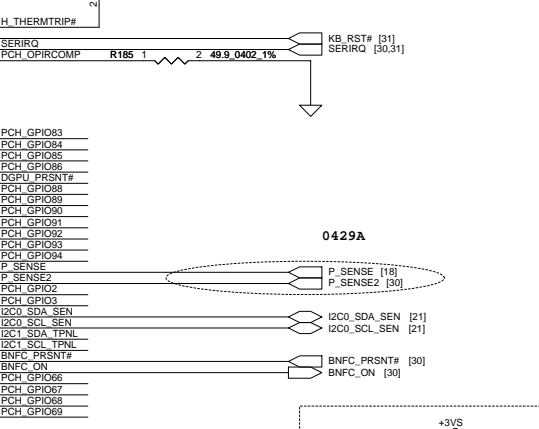
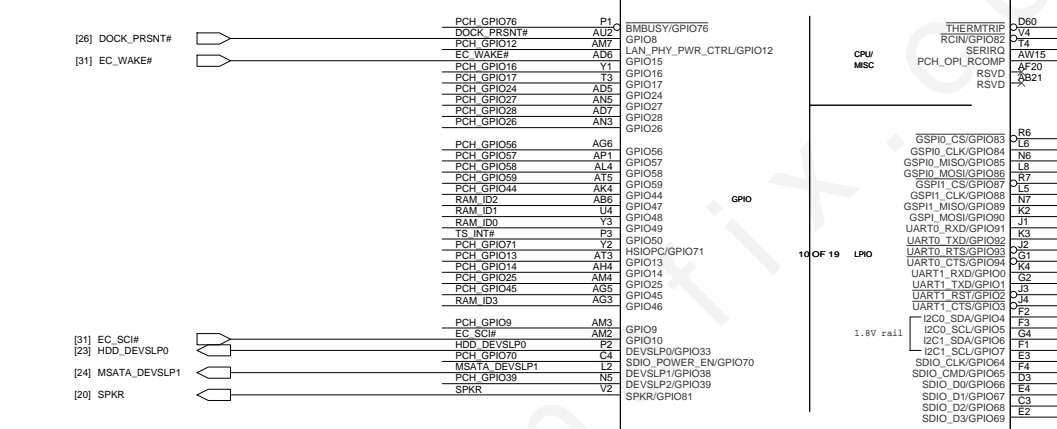
GPIO/ LPIO



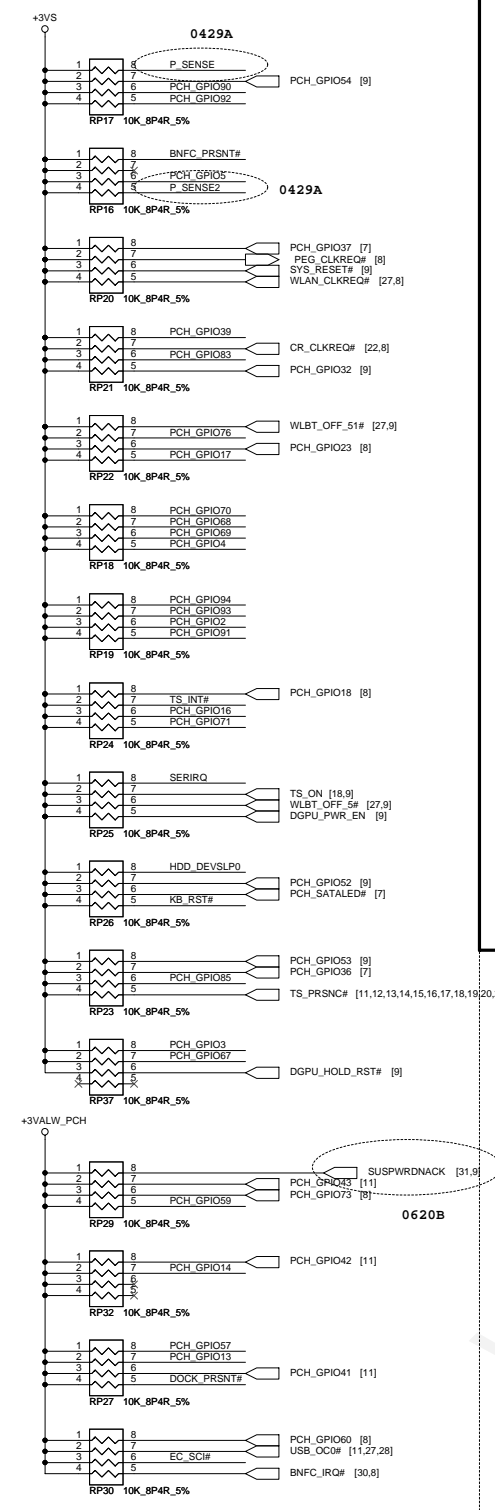
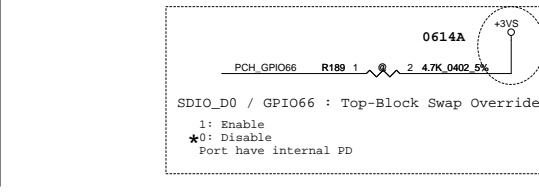
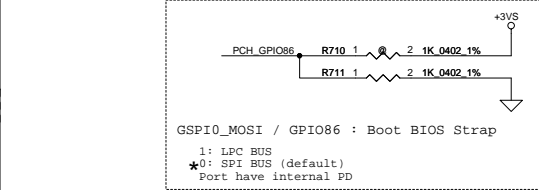
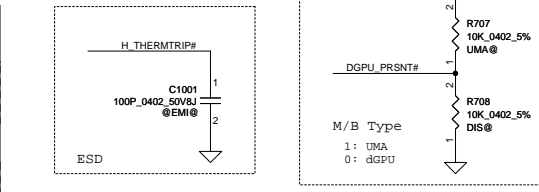
I2C0_SDA_SEN	R114	2	1	1K_0402_5%
I2C0_SCL_SEN	R115	2	1	1K_0402_5%
I2C1_SDA_TPNL	R117	2	1	1K_0402_5%
I2C1_SCL_TPNL	R116	2	1	1K_0402_5%



CHECK Power plane, for VGA thermtrip

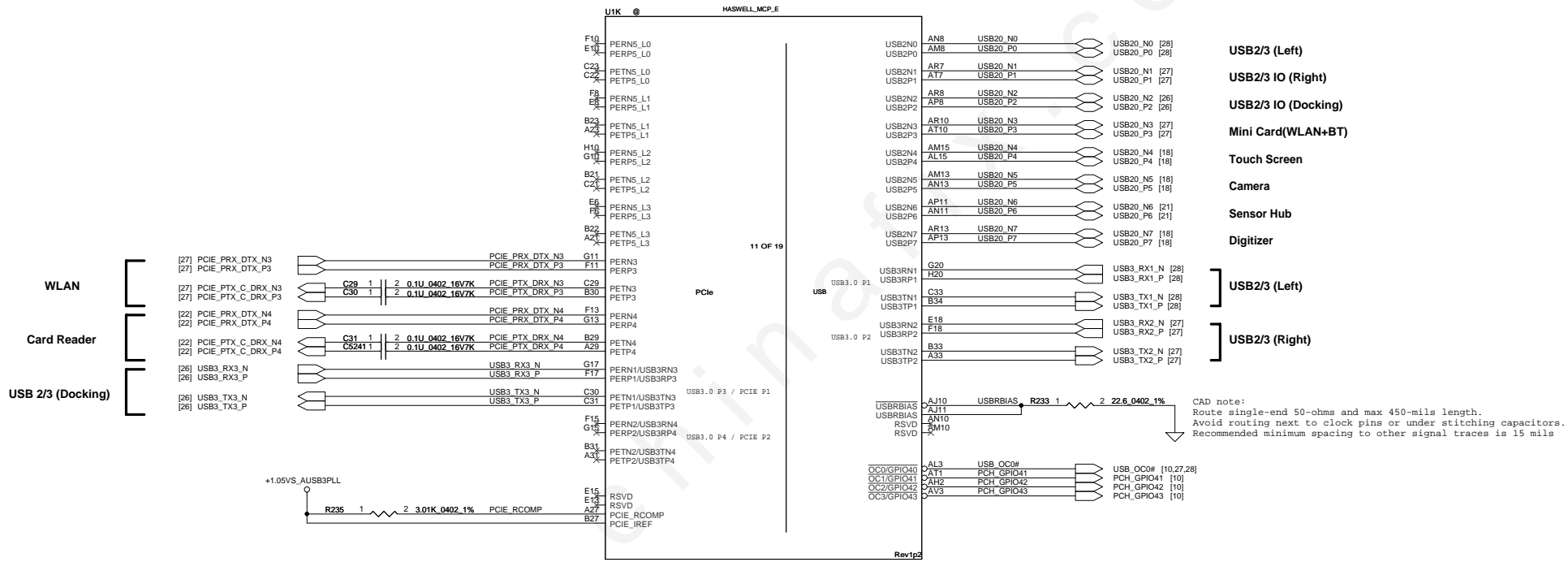


RAM_ID3 GPIO46	RAM_ID2 GPIO47	RAM_ID1 GPIO48	RAM_ID0 GPIO49	RAM
0	0	0	0	HYNIX 4GB
0	0	0	1	SAMSUNG 4GB
0	0	1	0	MICRON 4GB
0	0	1	1	ELPIDA 4GB
0	1	0	0	SAMSUNG 8GB
0	1	0	1	ELPIDA 8GB
0	1	1	0	MICRON 8GB
0	1	1	1	HYNIX 8GB
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD





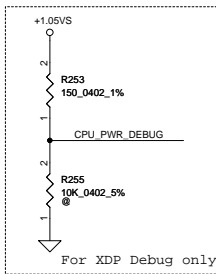
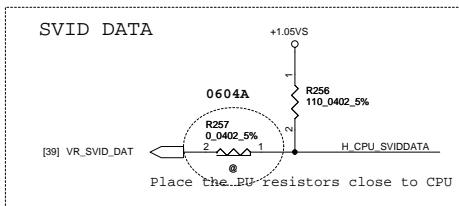
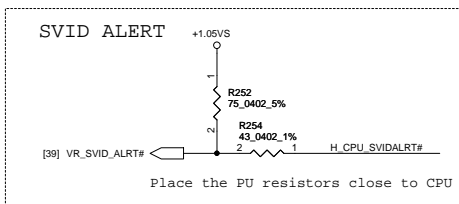
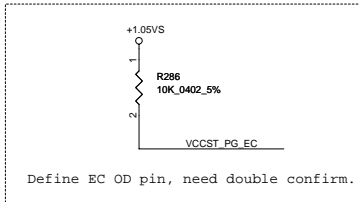
PCIE/ USB



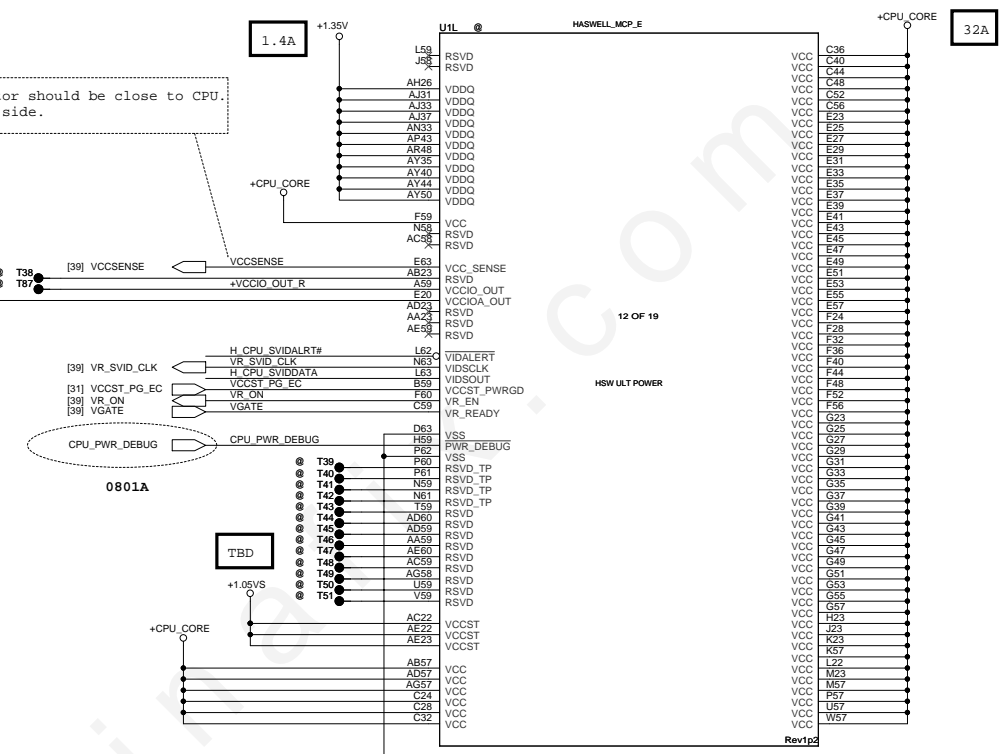
- USB2/3 (Left)
- USB2/3 IO (Right)
- USB2/3 IO (Docking)
- Mini Card(WLAN+BT)
- Touch Screen
- Camera
- Sensor Hub
- Digitizer
- USB2/3 (Left)
- USB2/3 (Right)

CAD note:
Route single-end 50-ohms and max 450-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils

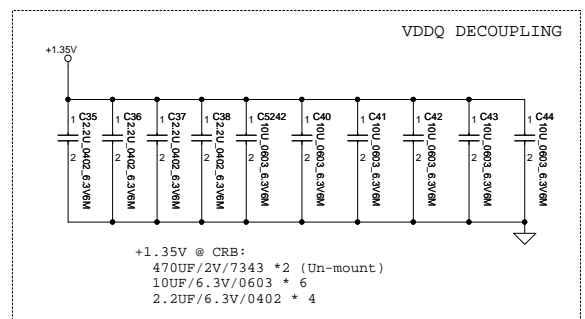
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Issued Date	2013/03/08	Deciphered Date	2015/03/08	Title	SCHEMATIC, MB AA341
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CAD Note: PU resistor should be close to CPU.
Pull-High at Power side.

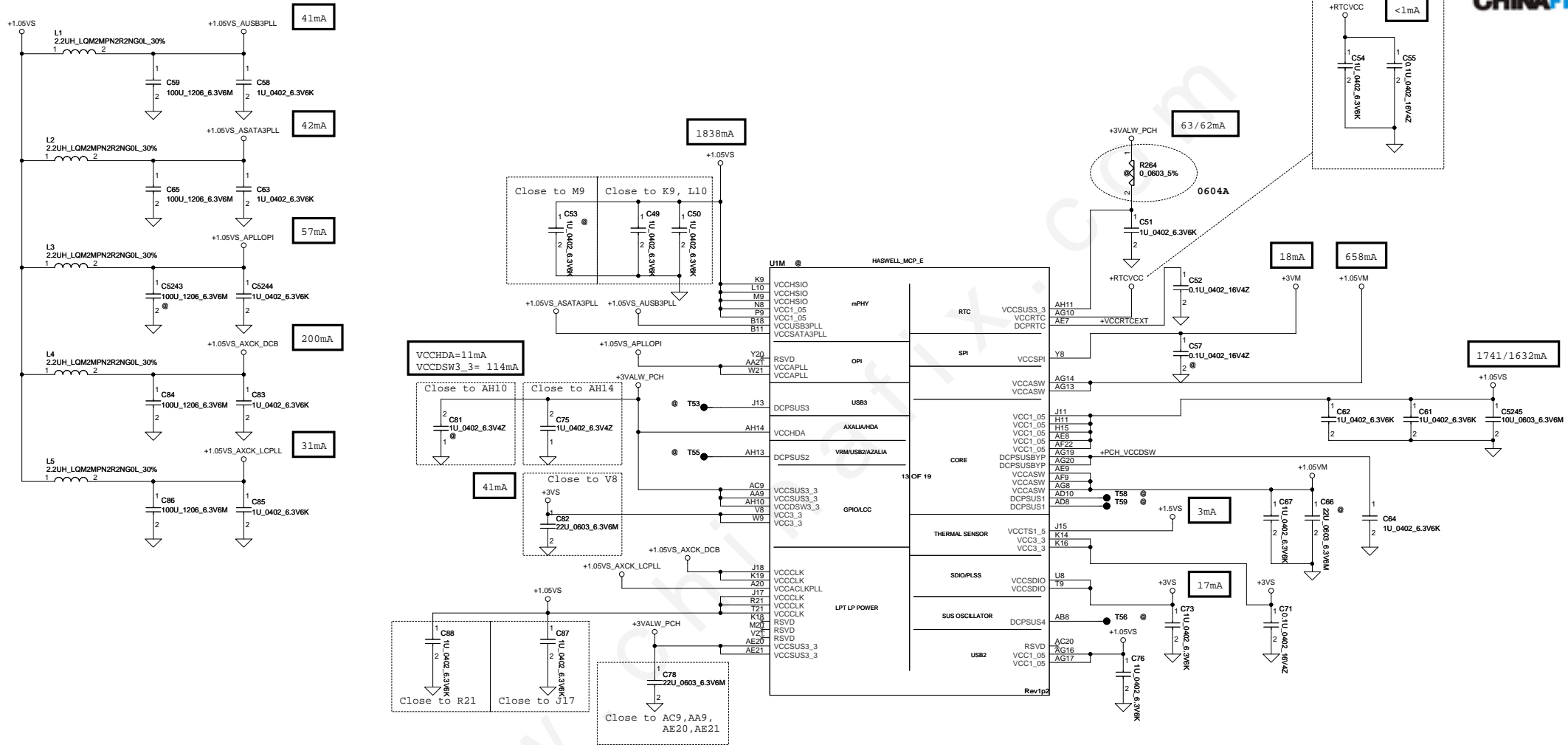


0801A



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				Custom	4019P2
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Power

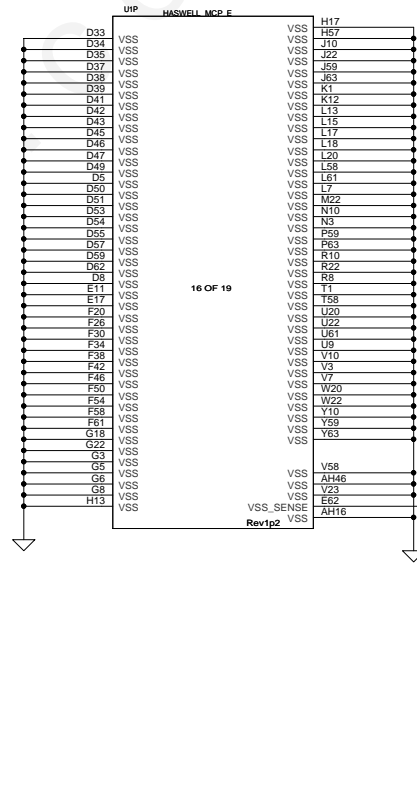
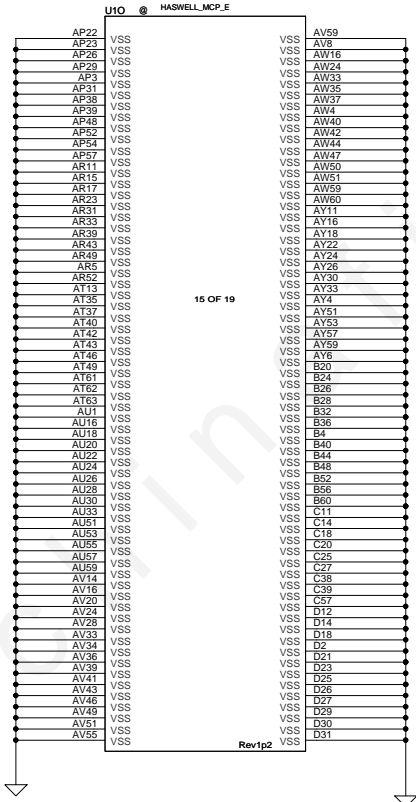
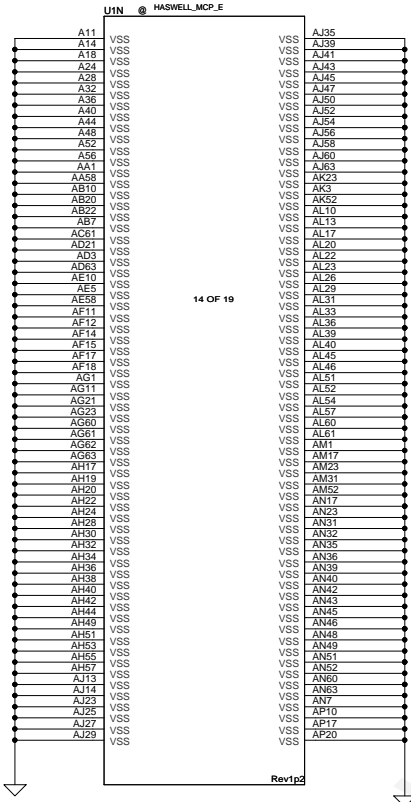


Only available on External Suspend VR powered.
 DcpSus1= 109mA
 DcpSus2= 25mA
 DcpSus3= 10mA
 DcpSus4= 1mA

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Date:	Friday, March 07, 2014	Sheet	13	of 42	

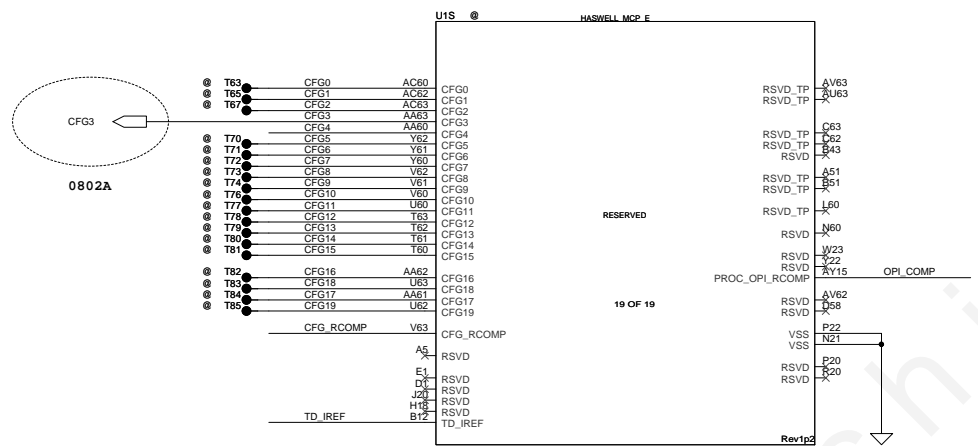
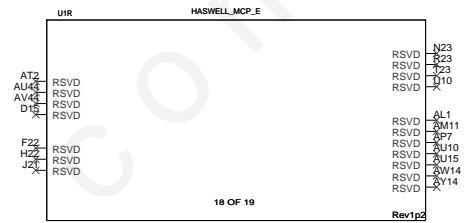
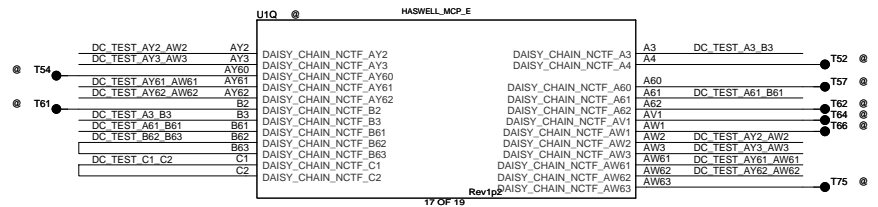


GND

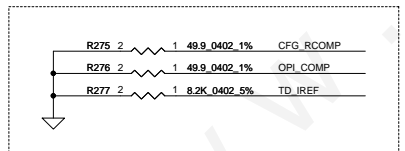
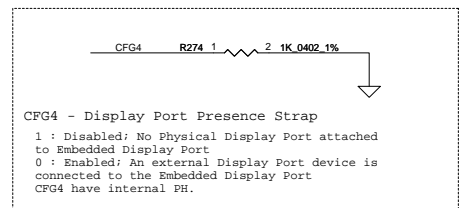
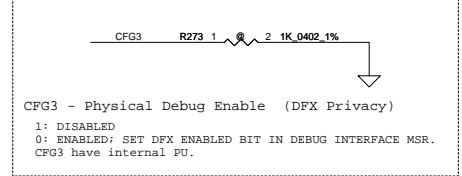


VSS_SENSE [39] AH16

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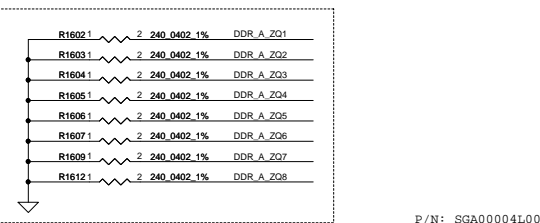
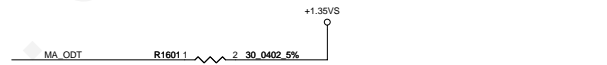
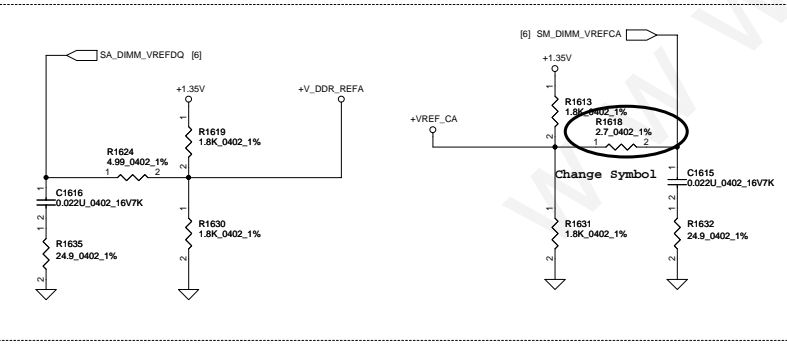
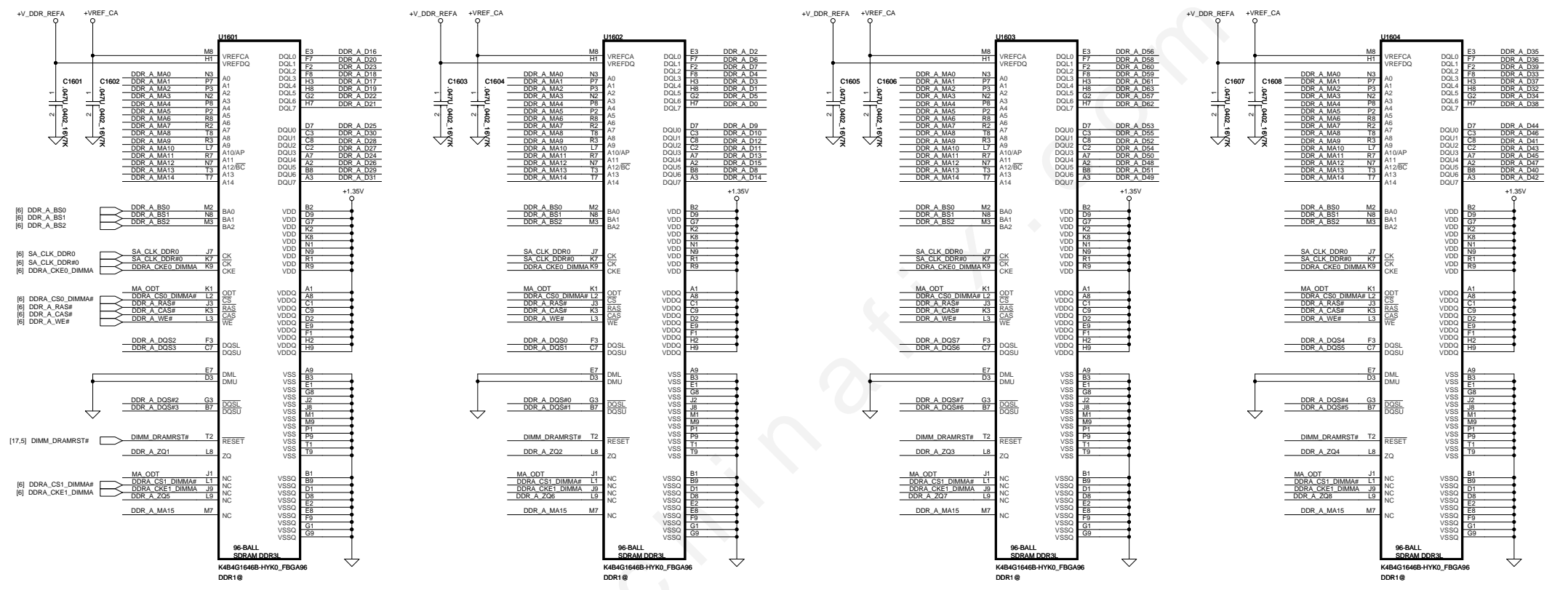
CFG Straps for Processor



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				Rev C
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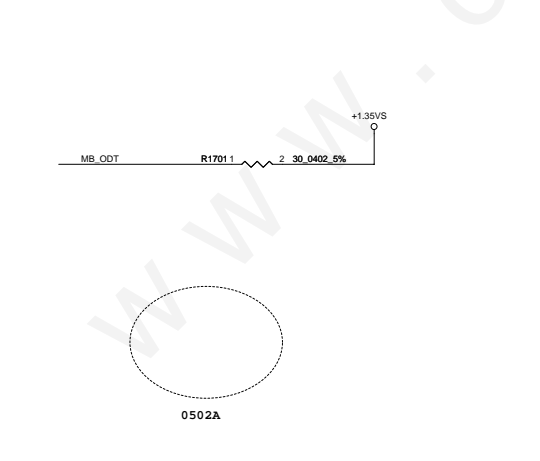
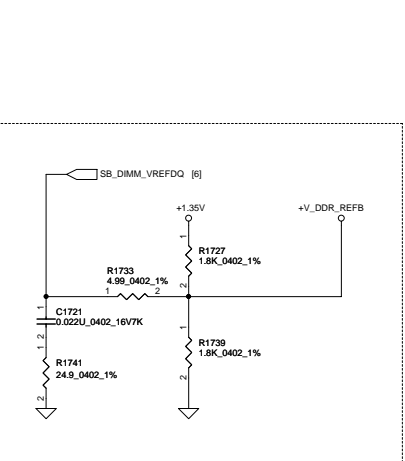
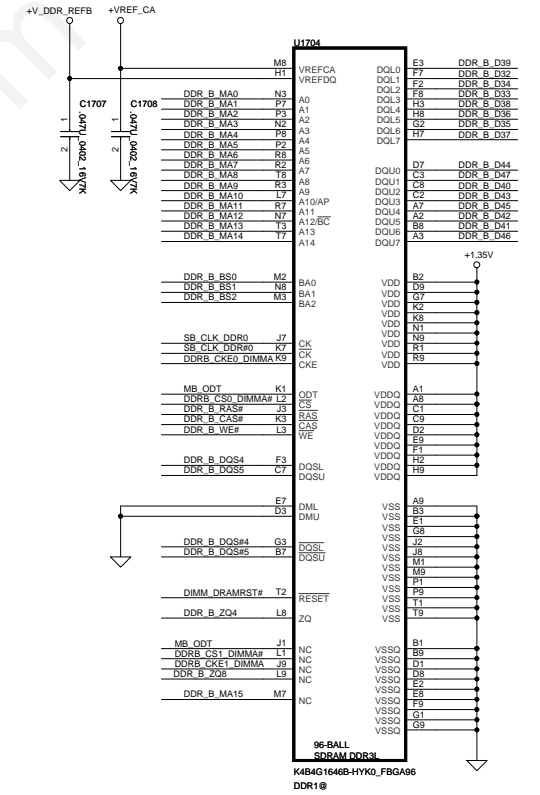
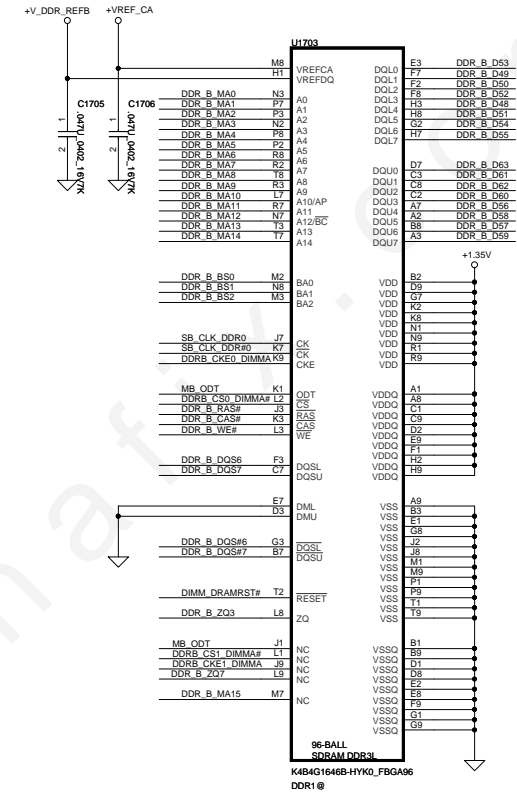
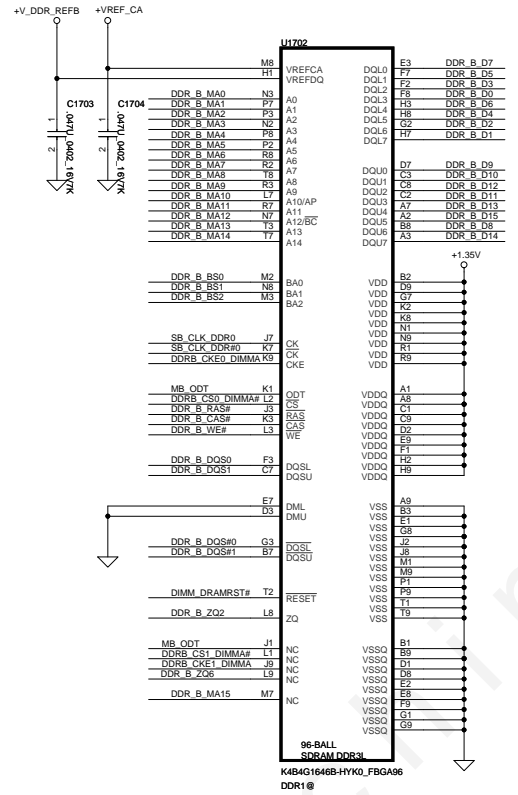
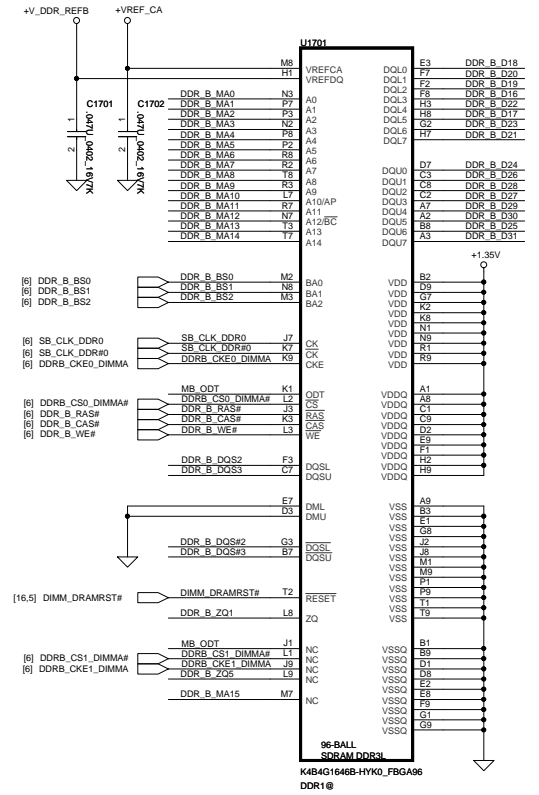
- [6] DDR_A_MA[0..15] DDR_A_MA[0..15]
- [6] DDR_A_DQS[0..7] DDR_A_DQS[0..7]
- [6] DDR_A_DS[0..7] DDR_A_DS[0..7]
- [6] DDR_A_D[0..63] DDR_A_D[0..63]



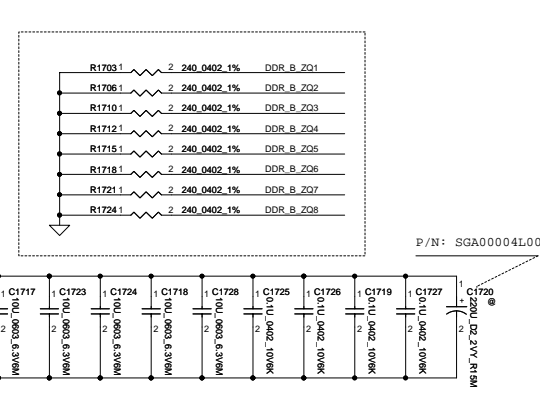
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DDR_A_MA1	R1511	1	2	34.8	0.402	1%
DDR_A_MA2	R1511	1	2	34.8	0.402	1%
DDR_A_MA3	R1514	1	2	34.8	0.402	1%
DDR_A_MA4	R1515	1	2	34.8	0.402	1%
DDR_A_MA5	R1517	1	2	34.8	0.402	1%
DDR_A_MA6	R1518	1	2	34.8	0.402	1%
DDR_A_MA7	R1521	1	2	34.8	0.402	1%
DDR_A_MA8	R1521	1	2	34.8	0.402	1%
DDR_A_MA9	R1522	1	2	34.8	0.402	1%
DDR_A_MA10	R1523	1	2	34.8	0.402	1%
DDR_A_MA11	R1525	1	2	34.8	0.402	1%
DDR_A_MA12	R1526	1	2	34.8	0.402	1%
DDR_A_MA13	R1528	1	2	34.8	0.402	1%
DDR_A_MA14	R1529	1	2	34.8	0.402	1%
DDR_A_MA15	R1527	1	2	34.8	0.402	1%
DDR_A_WE#	R1533	1	2	34.8	0.402	1%
DDR_A_CAS#	R1534	1	2	34.8	0.402	1%
DDR_A_RAS#	R1535	1	2	34.8	0.402	1%
DDR_A_BS0	R1537	1	2	34.8	0.402	1%
DDR_A_BS1	R1538	1	2	34.8	0.402	1%
DDR_A_BS2	R1539	1	2	34.8	0.402	1%
DDRA_CS0_DIMMA#	R1541	1	2	34.8	0.402	1%
DDRA_CS1_DIMMA#	R1541	1	2	34.8	0.402	1%
DDRA_CKE0_DIMMA	R1541	1	2	34.8	0.402	1%
SA_CLK_DDR0	R1543	1	2	26.1	0.402	1%
SA_CLK_DDR#0	R1545	1	2	26.1	0.402	1%



- [6] DDR_B_MA[0..15] DDR_B_MA[0..15]
- [6] DDR_B_DQS[0..7] DDR_B_DQS[0..7]
- [6] DDR_B_DQS[0..7] DDR_B_DQS[0..7]
- [6] DDR_B_DQ[0..63] DDR_B_DQ[0..63]



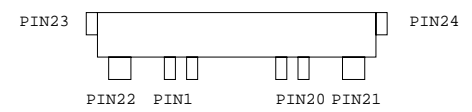
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DDR_B_MA2	R1705	2	34.8_0402_1%
DDR_B_MA3	R1707	2	34.8_0402_1%
DDR_B_MA4	R1708	2	34.8_0402_1%
DDR_B_MA5	R1711	2	34.8_0402_1%
DDR_B_MA6	R1709	2	34.8_0402_1%
DDR_B_MA7	R1713	2	34.8_0402_1%
DDR_B_MA8	R1714	2	34.8_0402_1%
DDR_B_MA9	R1716	2	34.8_0402_1%
DDR_B_MA10	R1717	2	34.8_0402_1%
DDR_B_MA11	R1719	2	34.8_0402_1%
DDR_B_MA12	R1721	2	34.8_0402_1%
DDR_B_MA13	R1722	2	34.8_0402_1%
DDR_B_MA14	R1723	2	34.8_0402_1%
DDR_B_MA15	R1725	2	34.8_0402_1%
DDR_B_WE#	R1726	2	34.8_0402_1%
DDR_B_CAS#	R1728	2	34.8_0402_1%
DDR_B_RAS#	R1729	2	34.8_0402_1%
DDR_B_BSD0	R1730	2	34.8_0402_1%
DDR_B_BSD1	R1731	2	34.8_0402_1%
DDR_B_BSD2	R1732	2	34.8_0402_1%
DDR_B_CS0_DIMM#	R1734	2	34.8_0402_1%
DDR_B_CS1_DIMM#	R1735	2	34.8_0402_1%
DDR_B_CKE1_DIMM#	R1737	2	34.8_0402_1%
DDR_B_CKE2_DIMM#	R1738	2	34.8_0402_1%
SB_CLK_DDR0	R1738	2	28.1_0402_1%
SB_CLK_DDR#0	R1740	2	28.1_0402_1%



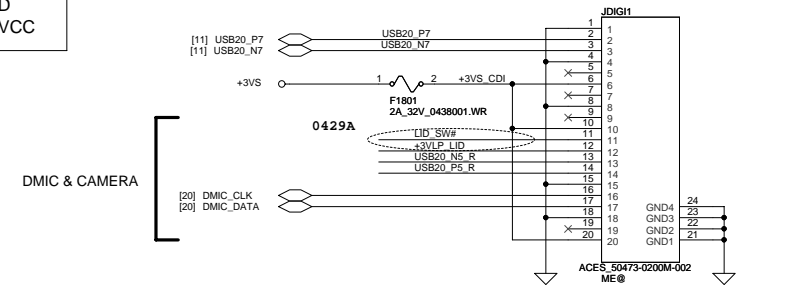
Digitizer & CMOS Conn

DMIC & CAMERA module pin define

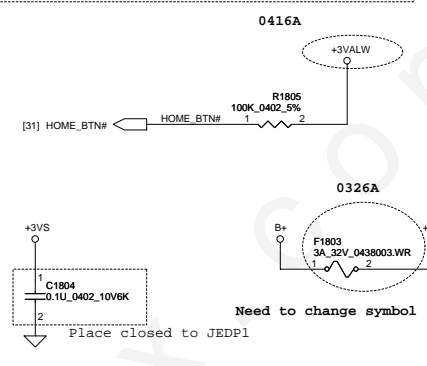
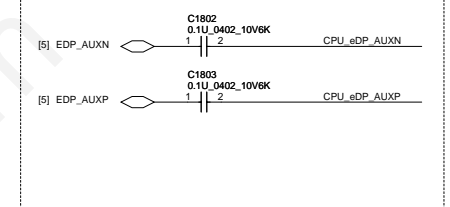
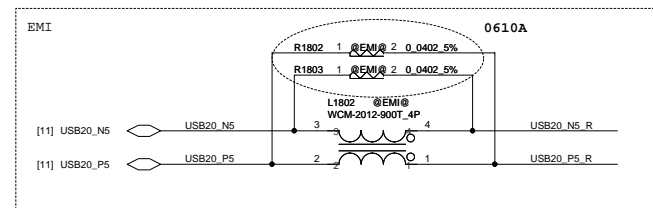
No	SIGNAL
1	VCC (3.3V)
2	D-
3	D+
4	GND_CAM
5	GND_DMIC
6	MIC_C
7	MIC_D
8	MIC_VCC



P/N: SP011211150

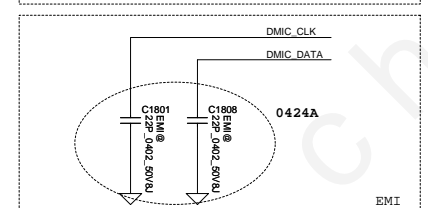
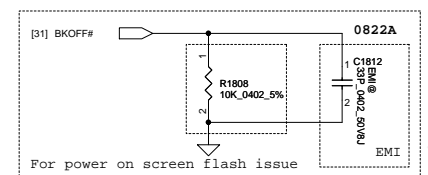
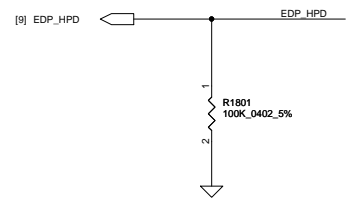


eDP Panel Conn



P/N: SP011302062

HPD Inversion for eDP



LCD Panel (10 PIN)

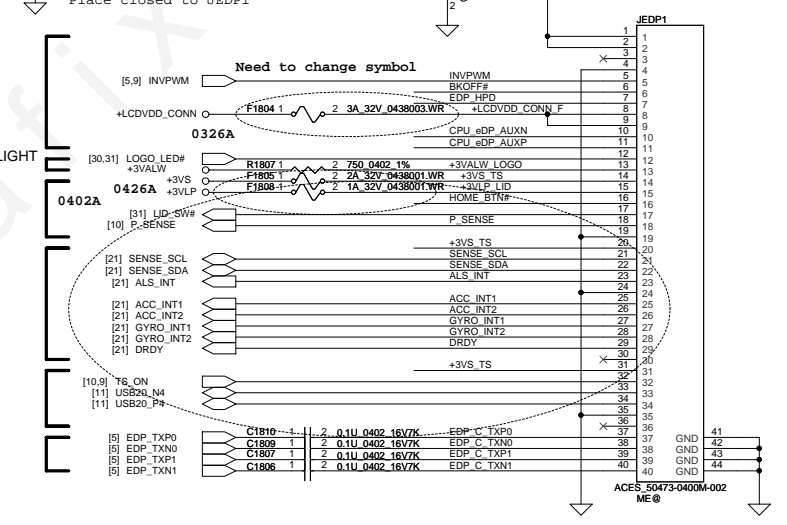
A LOGO RED LIGHT (2 PIN)

Home Button (6 PIN)

Sensor/B (10 PIN)

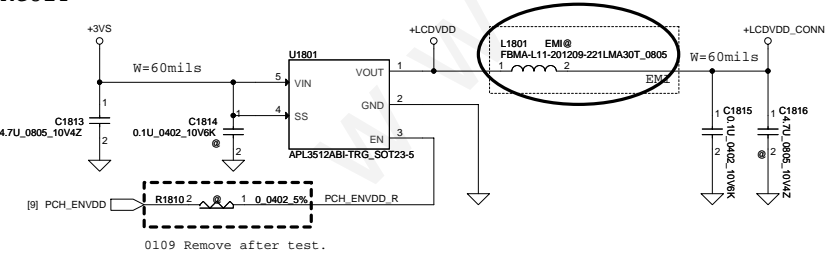
Touch Panel (6 PIN)

LCD Panel (4 PIN)

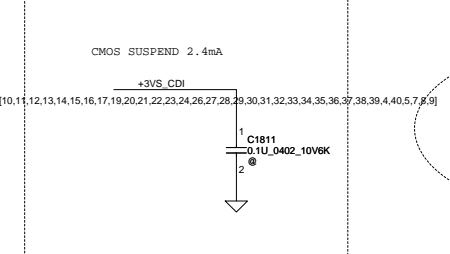


LCD POWER CIRCUIT

Ces	Tes
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



Camera Modul POWER CIRCUIT



Touch PANEL module pin define

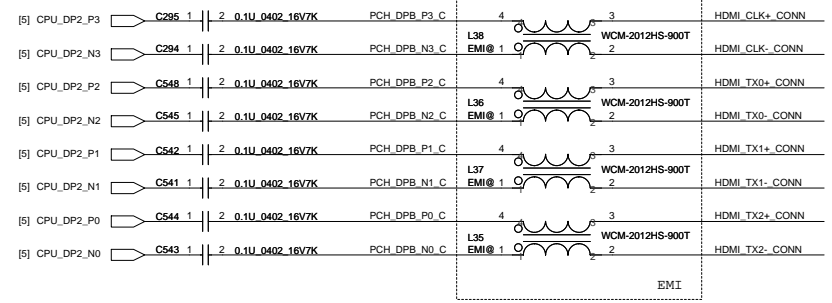
No	USB/I2C
1	VCC (3.3V)
2	Reset
3	GND
4	D-
5	D+
6	GND
7	SCL
8	SDA
9	INT
10	PRSENT

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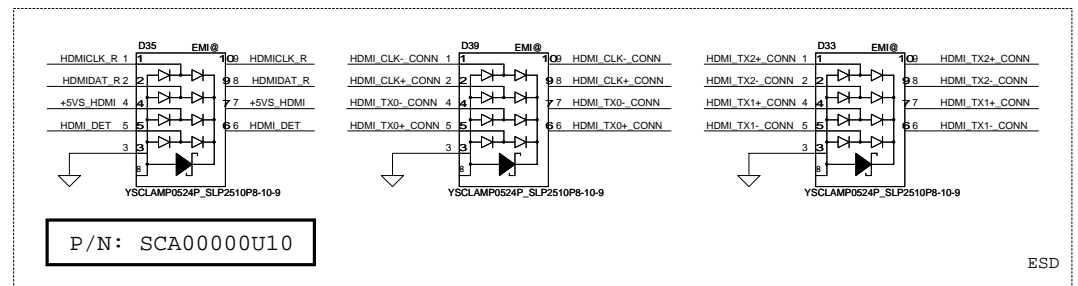
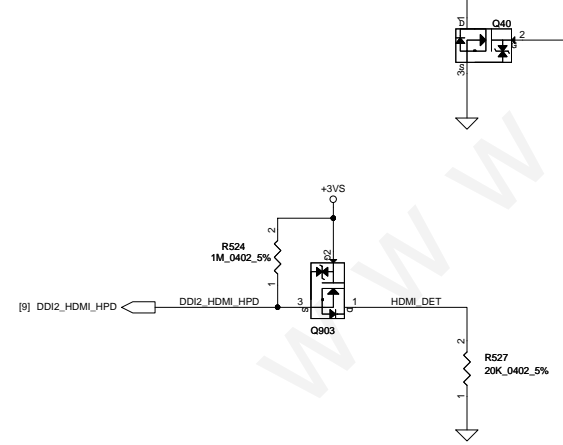
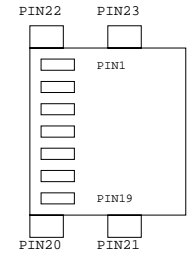
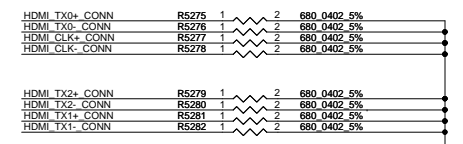
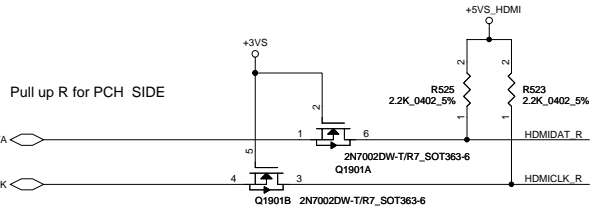
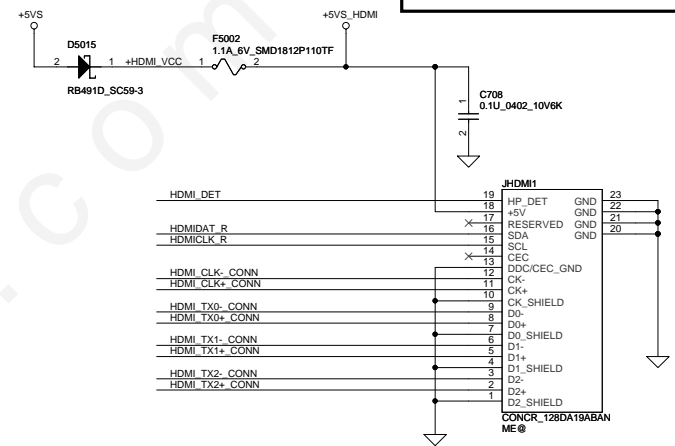


HDMI

P/N: SM070001S00

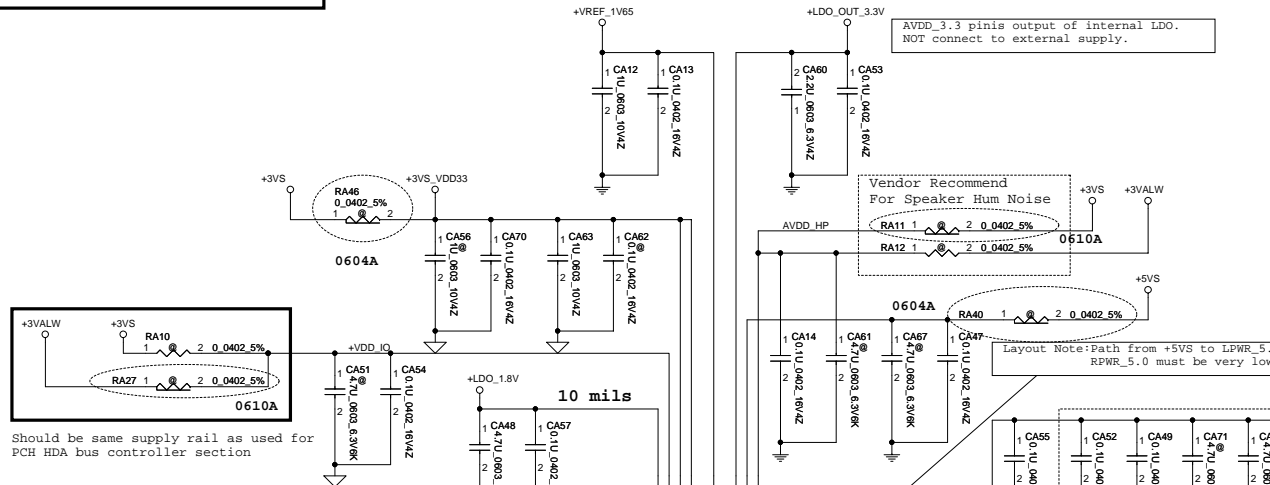


P/N: SP060005JB0
TYPE C Connector



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Audio CX20751

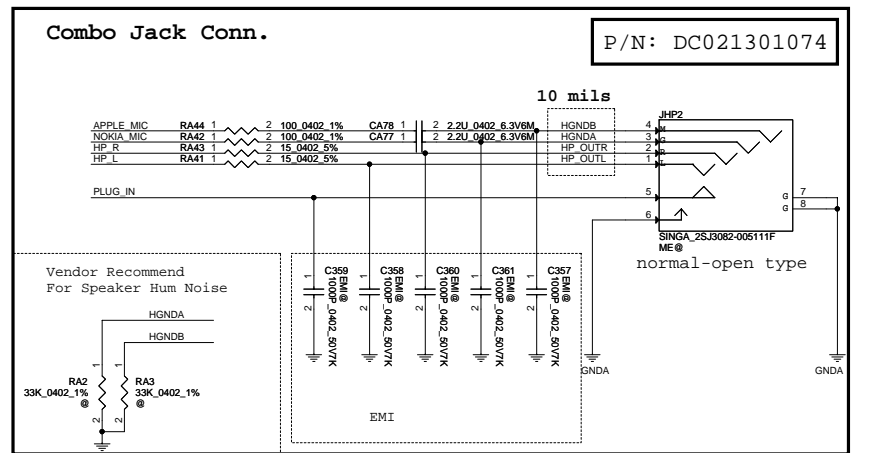
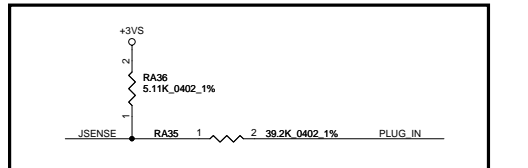
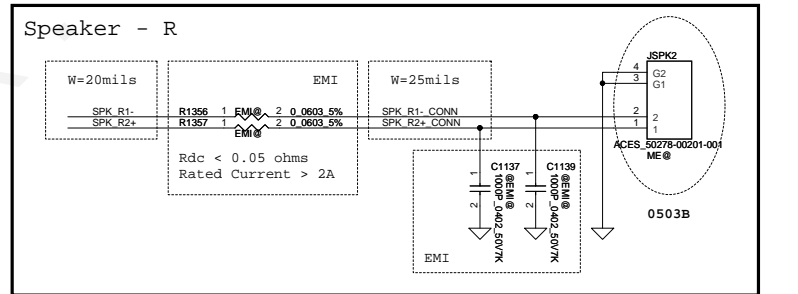
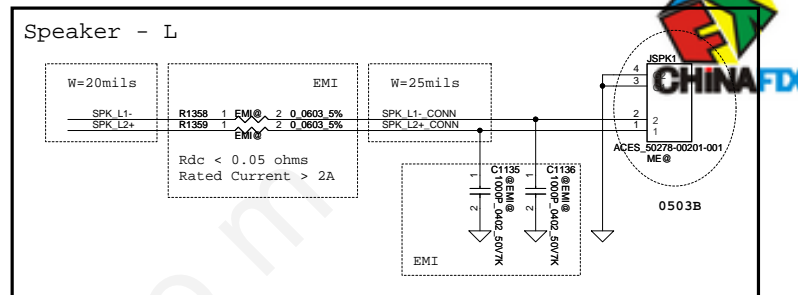
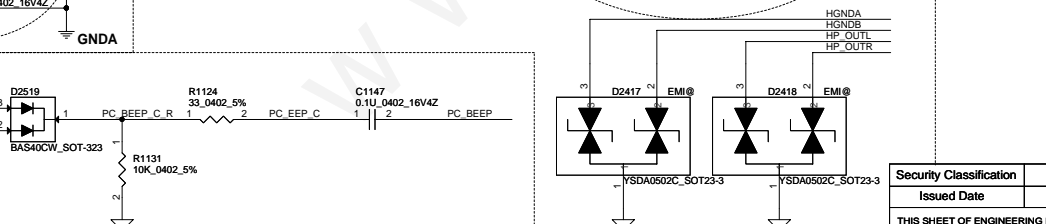
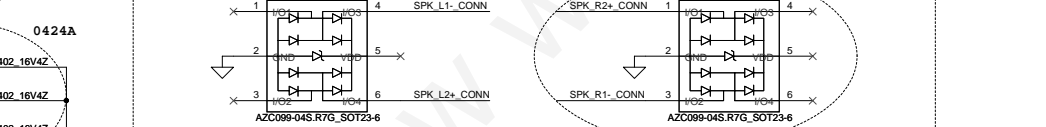
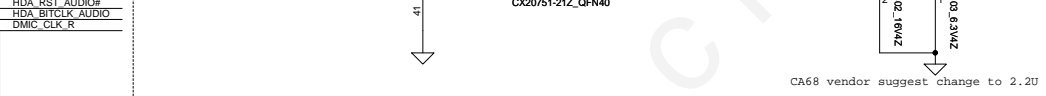
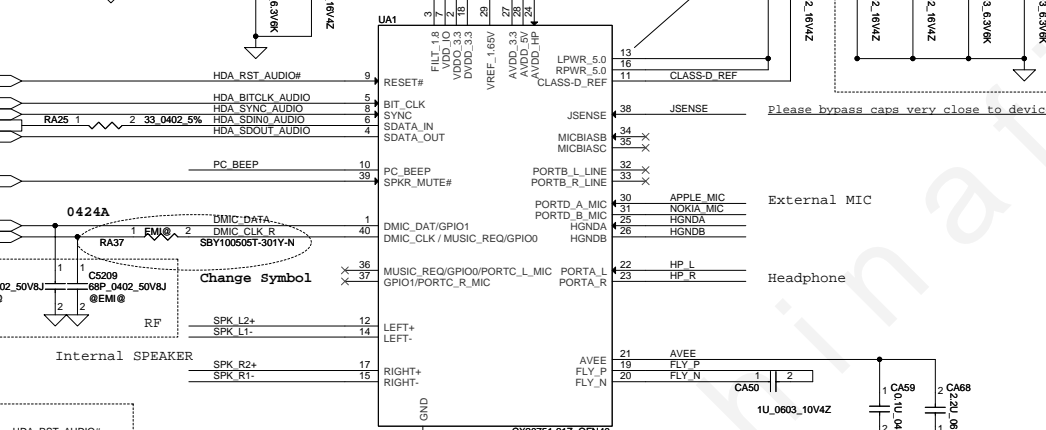
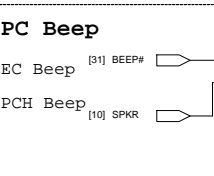
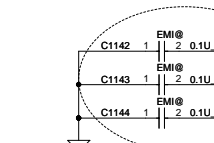
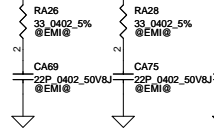


Should be same supply rail as used for PCH HDA bus controller section

- [7] HDA_RST_AUDIO#
- [7] HDA_BITCLK_AUDIO
- [7] HDA_SYNC_AUDIO
- [7] HDA_SDIN0
- [7] HDA_SDOUT_AUDIO
- [31] EC_MUTE#
- [18] DMIC_DATA
- [18] DMIC_CLK

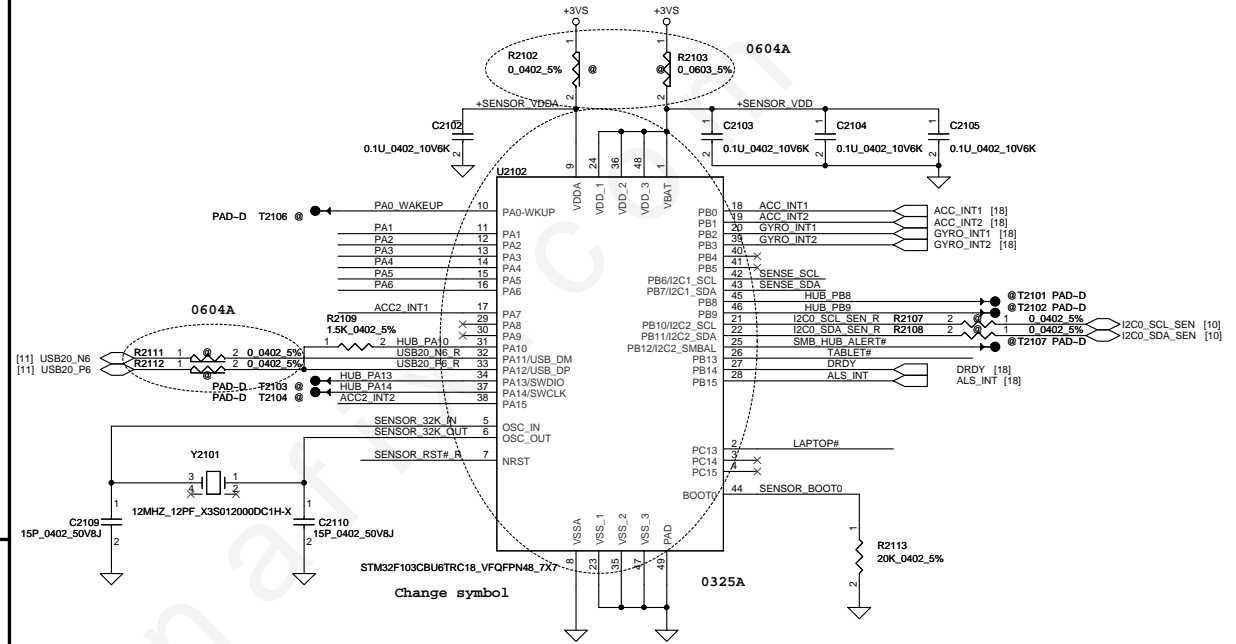
- [18] DMIC_DATA
- [18] DMIC_CLK

- [36] SPK L2+
- [14] SPK L1-
- [17] SPK R2+
- [15] SPK R1-

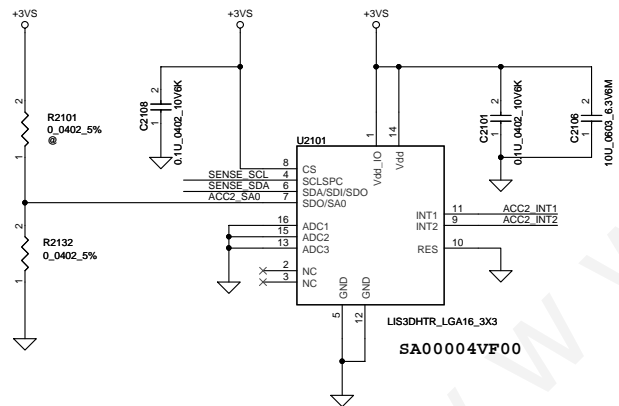


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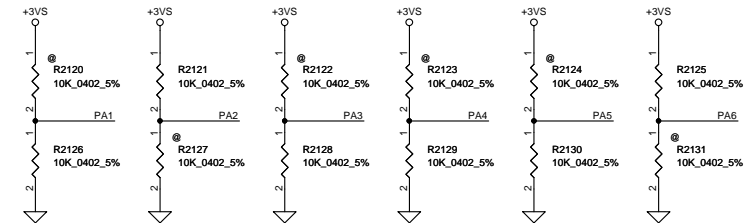
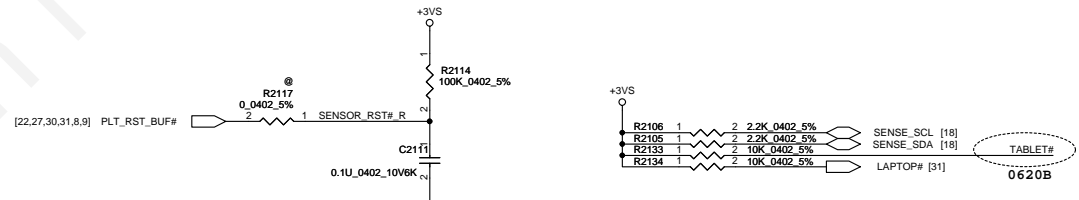
Sensor Hub



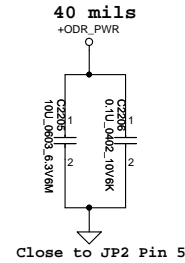
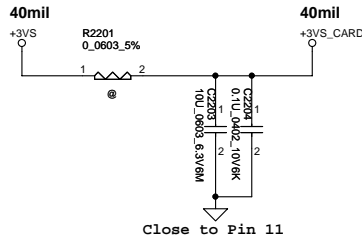
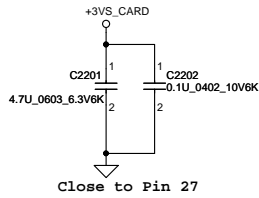
2nd G-sensor



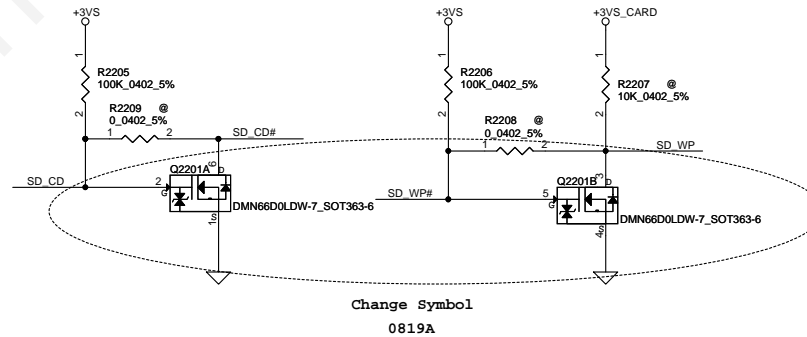
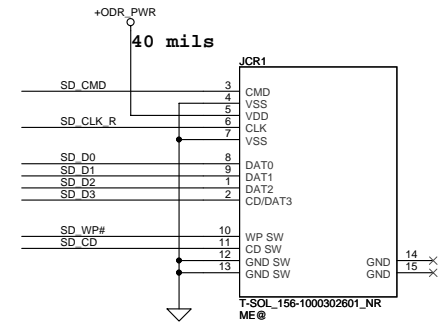
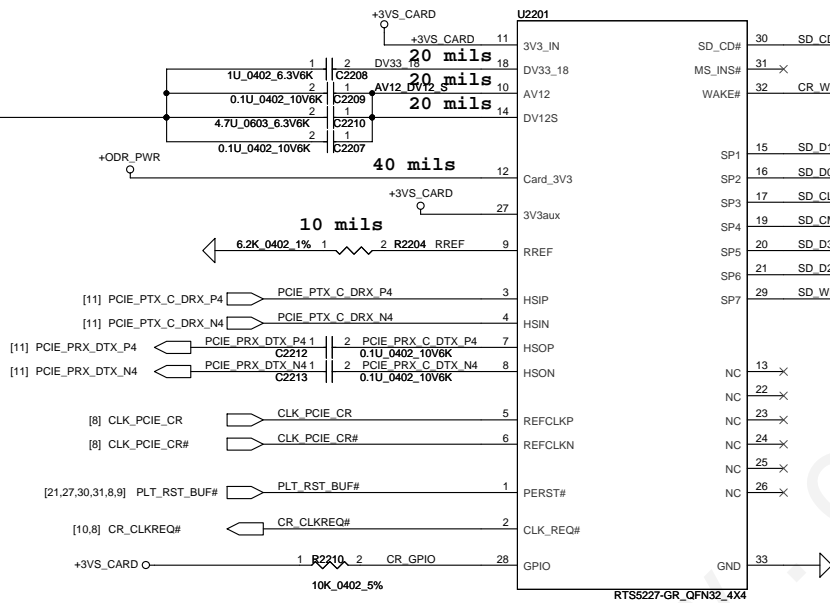
	ACC2_SA0
H	0x33h 0x32h
L	0x31h 0x30h



Card Reader RTS5227-QFN32



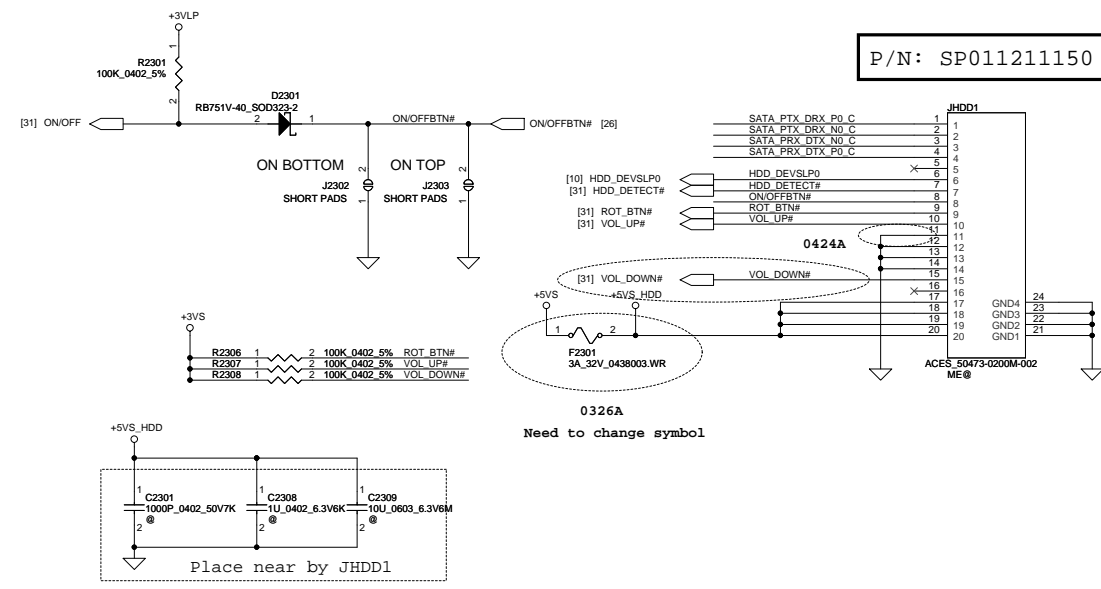
P/N: SP07000TF00



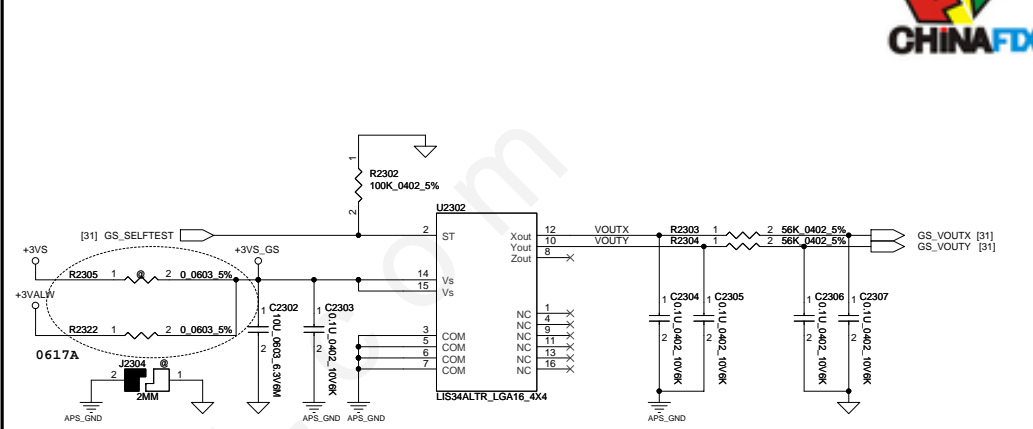
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Issued Date	2013/03/08	Deciphered Date	2015/03/08	SCHEMATIC, MB AA341	
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Document Number	4019P2		Rev	C	
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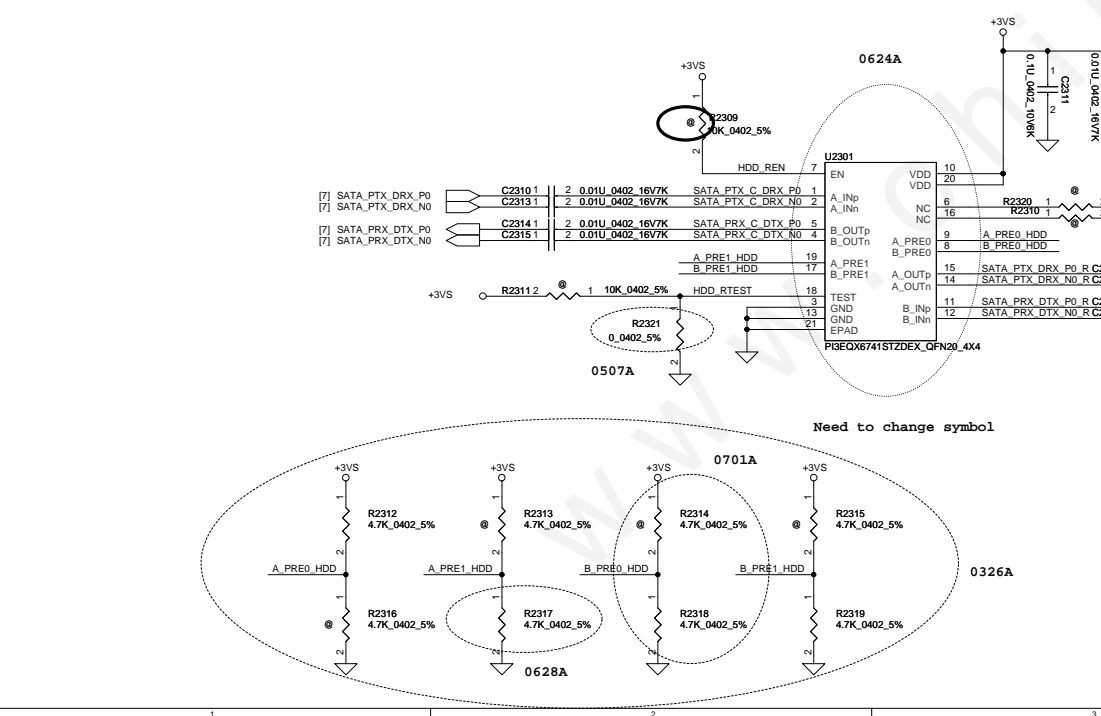
SATA HDD WTB Conn



APS G-Sensor



HDD SATA Redriver



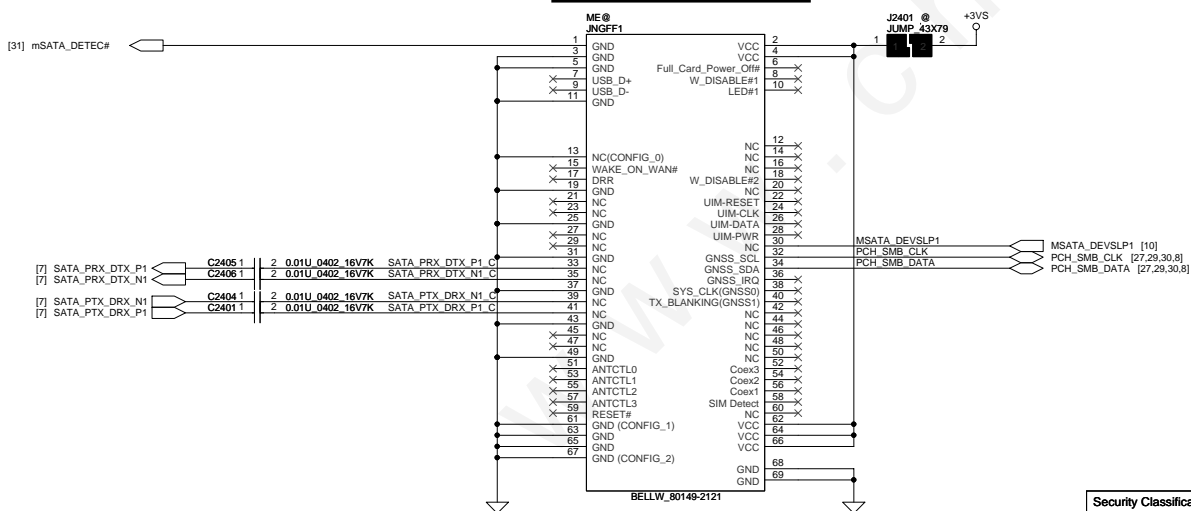
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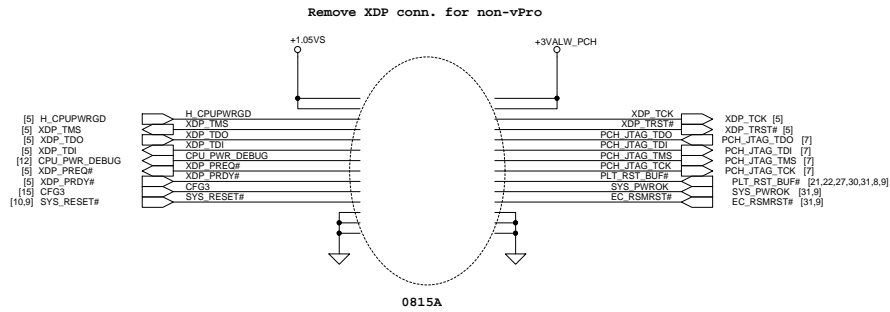
NGFF SATA Redriver

NGFF mSATA Conn

P/N: SP071212280



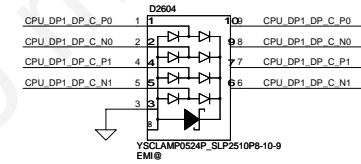
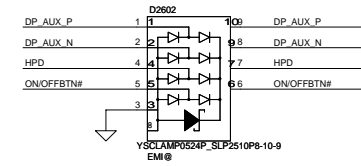
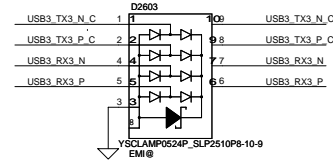
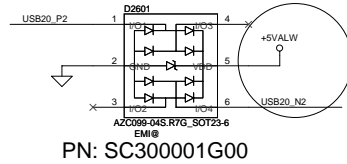
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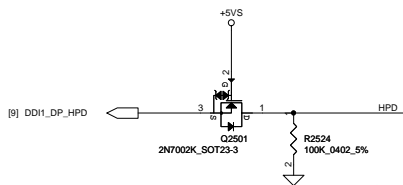
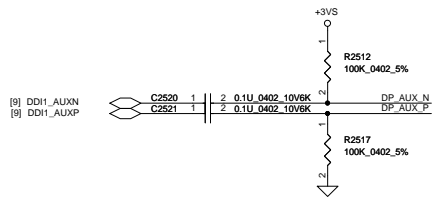
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				Date:	Friday, March 07, 2014

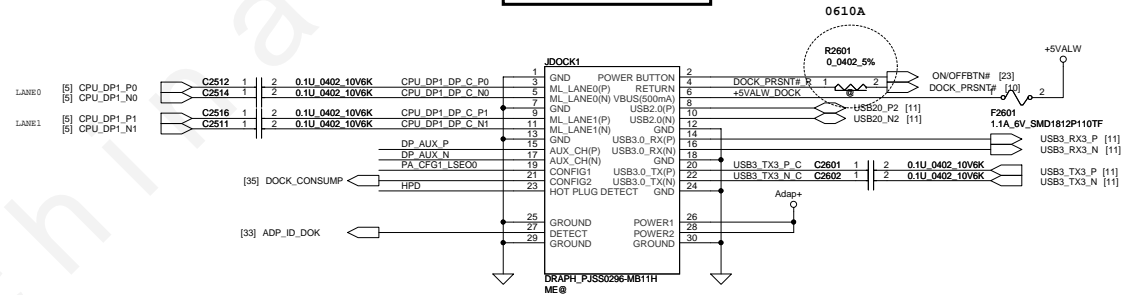
Docking (USB3.0)



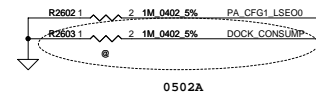
Docking (Display Port)



P/N: DC0212121

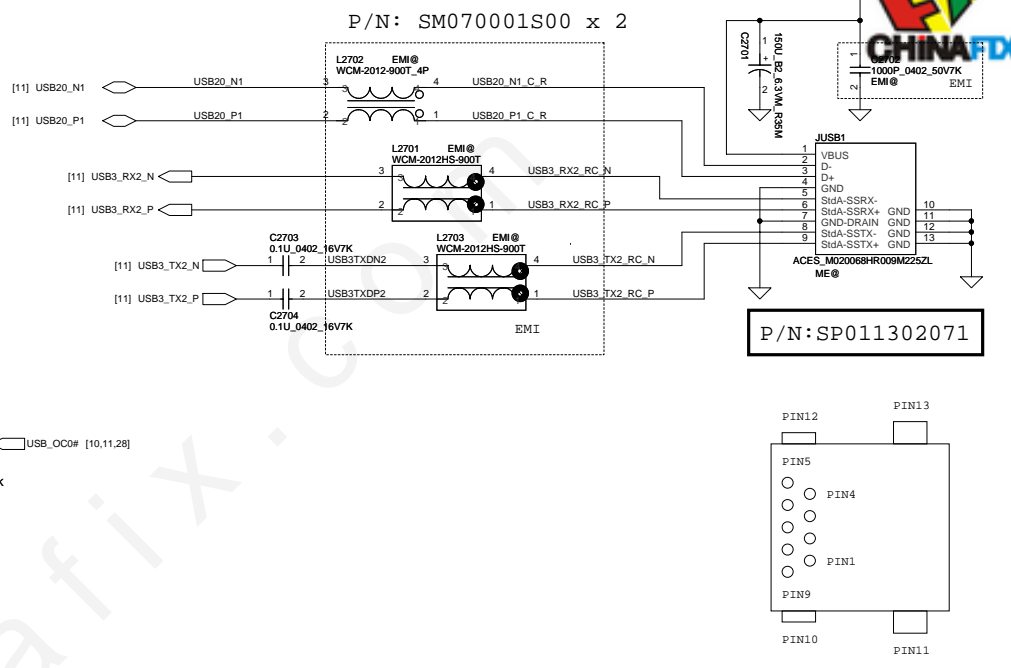
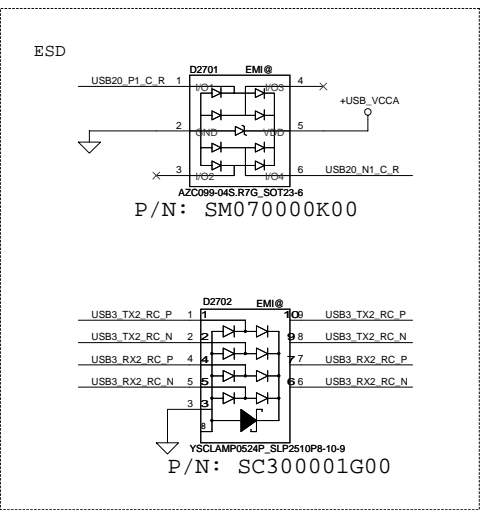


Footprint: DRAPH_PJSS0296-MB11H_24P-T



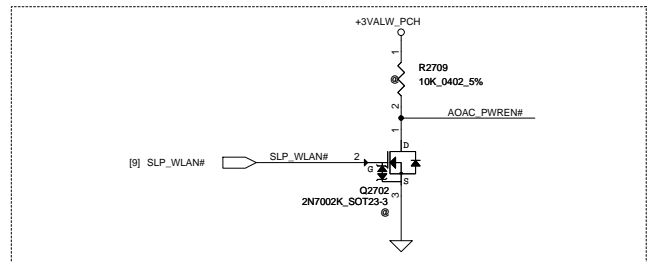
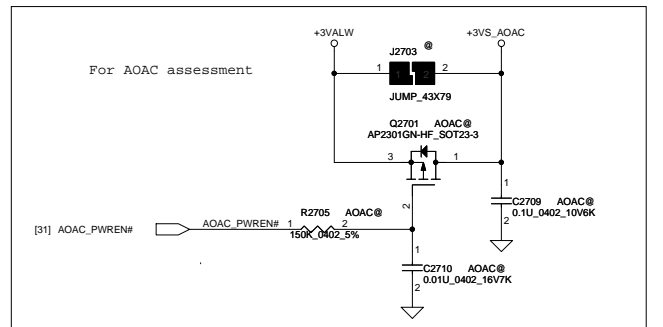
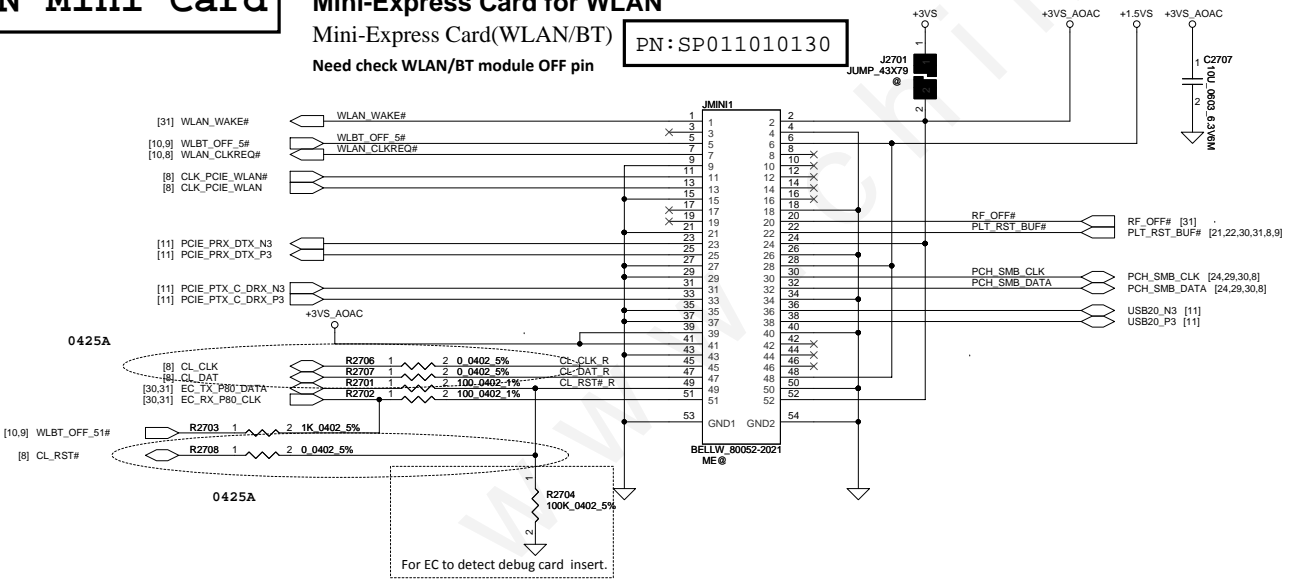
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USB30 Conn



WLAN Mini Card

Mini-Express Card for WLAN
 Mini-Express Card(WLAN/BT)
 Need check WLAN/BT module OFF pin
 P/N: SP011010130

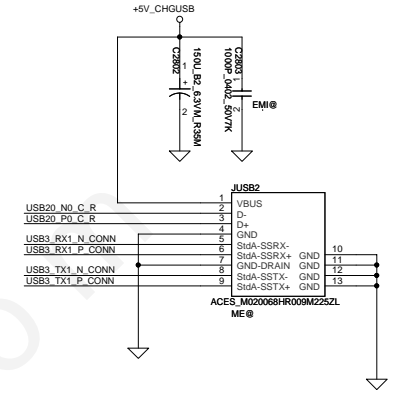
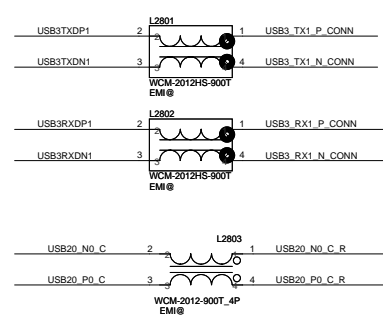
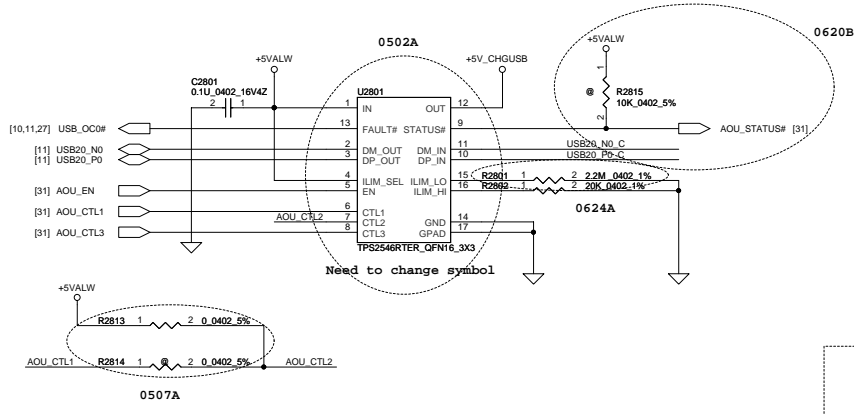


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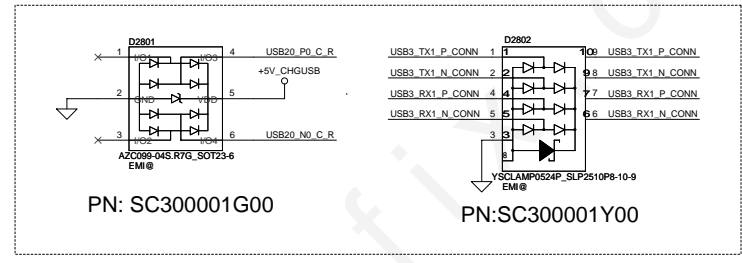


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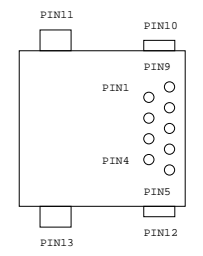
USB 3.0 Charger & Conn.



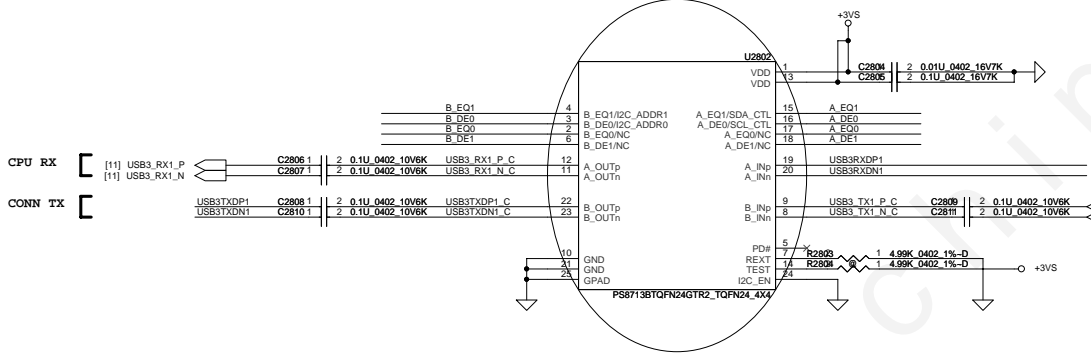
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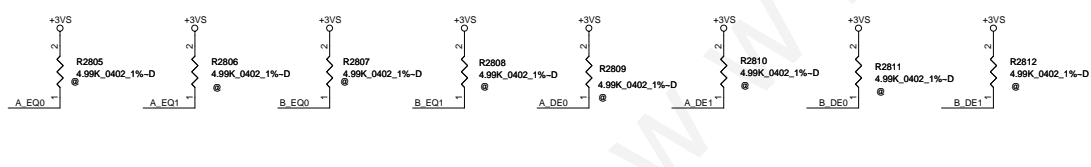
P/N: SP011302071



SA000050R20
6 / 25



	A_EQ1/B_EQ1 (Internal pull Low)	A_EQ0/B_EQ0 (Internal pull Low)
reserved	Low	Low
program EQ for channel loss up to 7dB	Low	High
program EQ for channel loss up to 14.5dB	High	Low
program EQ for channel loss up to 11.5dB	High	High



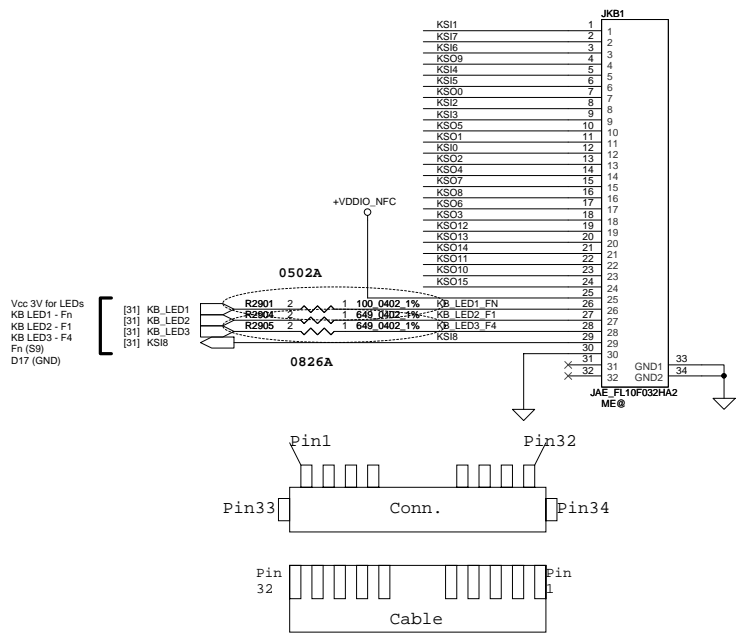
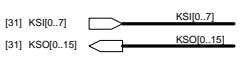
	TEST (Internal pull Low)
Normal operation (default)	Low
Test mode enable	High

	A_DE1/B_DE1 (Internal pull Low)	A_DE0/B_DE0 (Internal pull Low)
3.5dB de-emphasis	Low	Low
No de-emphasis	Low	High
2.7dB de-emphasis	High	Low
5dB with boost output swing	High	High

PN: SA000059H00

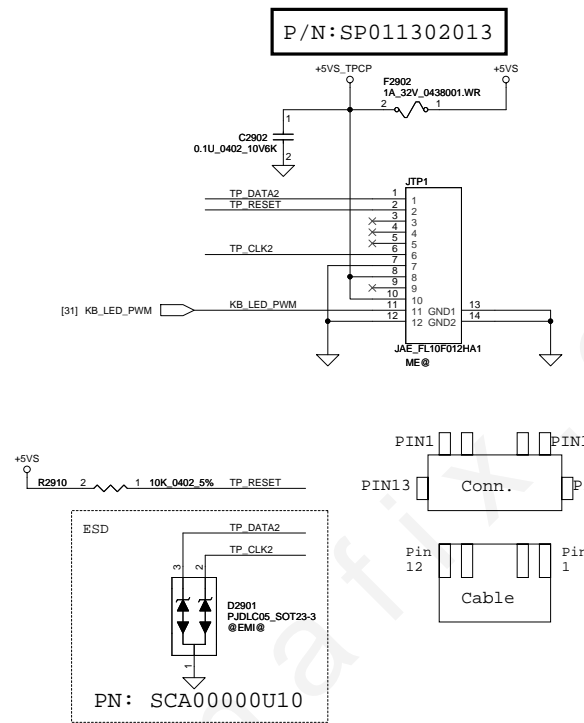
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Int KB Conn



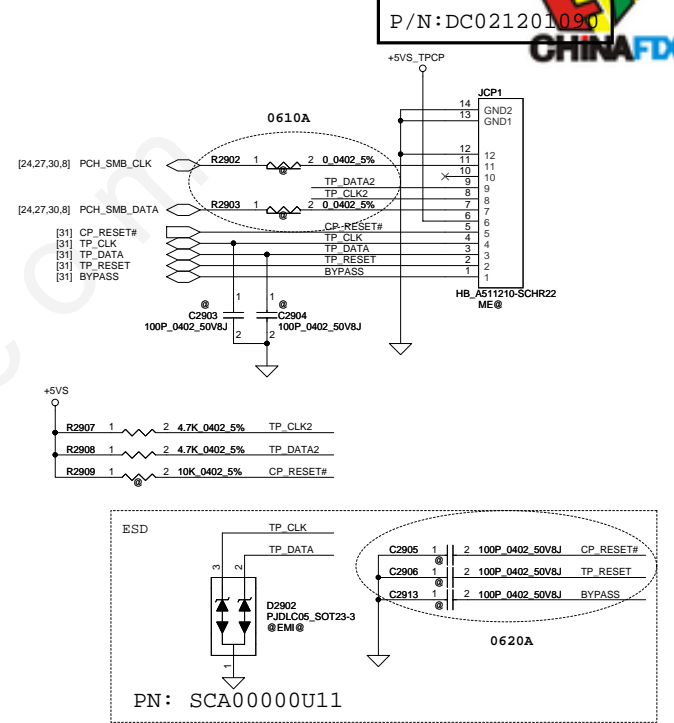
P/N: SP011302012

Track Point



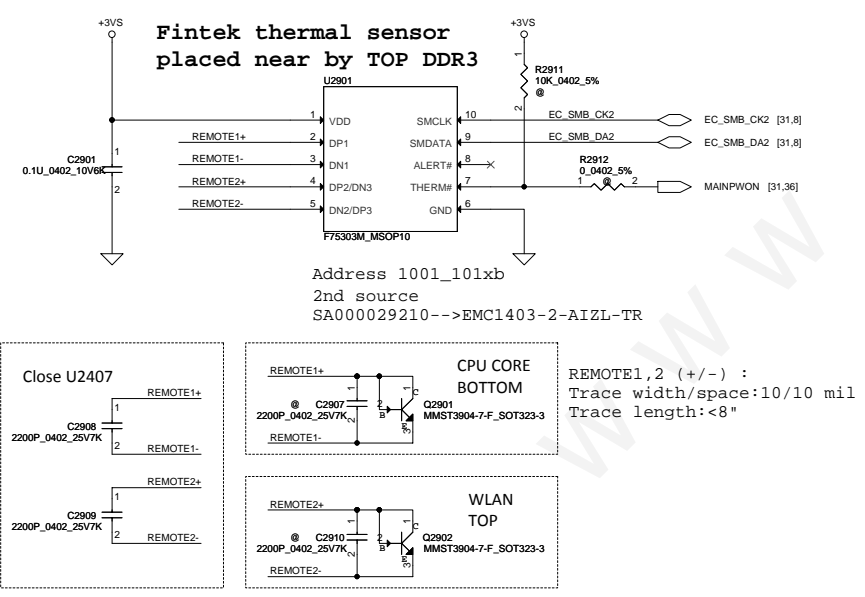
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Click PAD

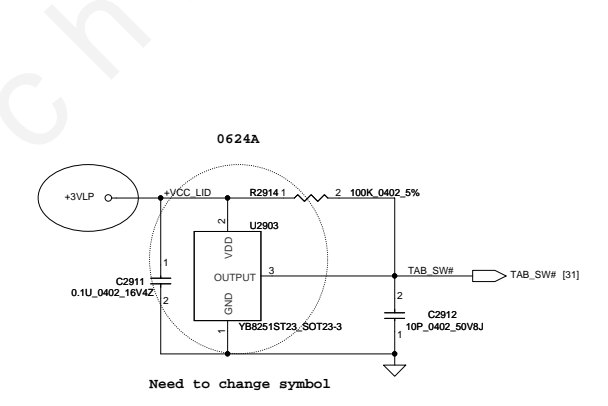


P/N: DC021201090

THRM Sensor



Tablet Switch



Track Point pin define

NO	Signal
1	IPD DATA
2	IPD RST
3	NC
4	NC
5	NC
6	IPD CLK
7	GND
8	VCC5
9	BKLITE DEC
10	LED VCC5
11	LED PWM
12	LED GND

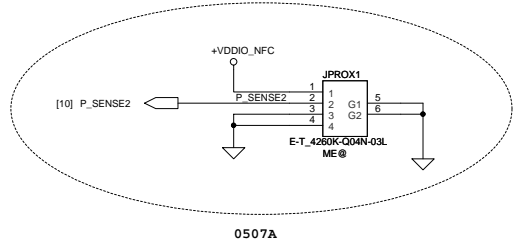
Click PAD pin define

NO	Signal
1	GND
2	SMB CLK
3	NC
4	DATA-TP
5	CLK-TP
6	SMB-DATA
7	VDD
8	RESET
9	CLK
10	DATA
11	TP4RST
12	BYPASS

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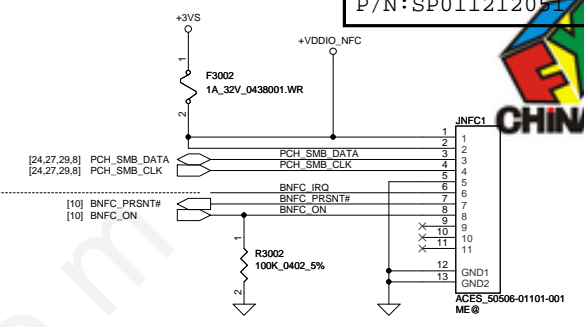
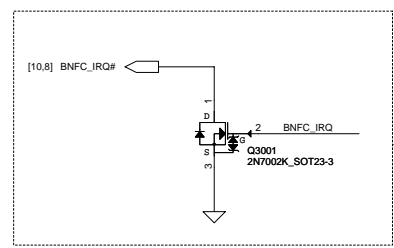


P-Sensor Conn



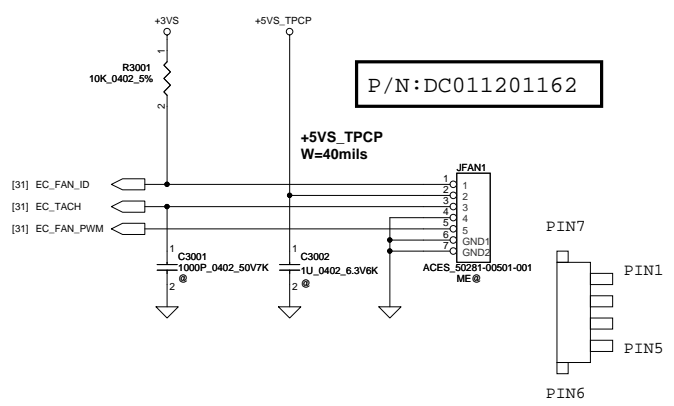
NFC

- Module Pin define
- 1.IP/VBAT
 - 2.IP/VDDIO
 - 3.IO/I2C-SDA
 - 4.I/I2C-SCL
 - 5.G/GND
 - 6.O/IRQ-NFC
 - 7.O/NFC_Presence#
 - 8.I/REG_UP
 - 9.OP/VDD_Ext_SE
 - 10.IP/UIM_PWR
 - 11.IO/SWP

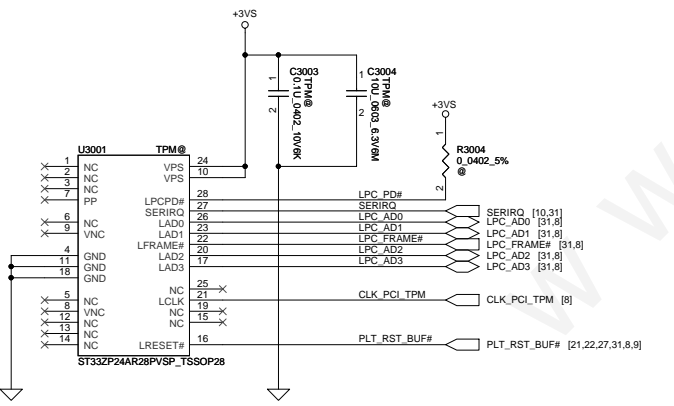


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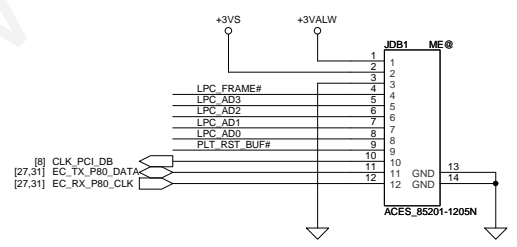
FAN Conn



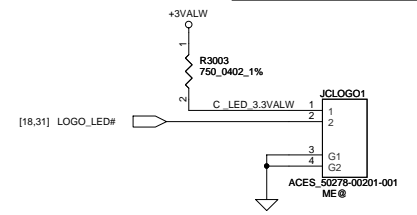
TPM



Debug Conn



C-logo Conn



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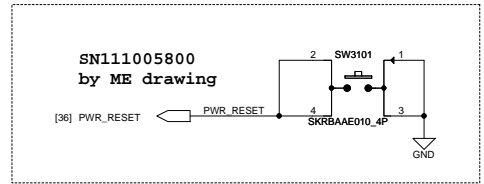
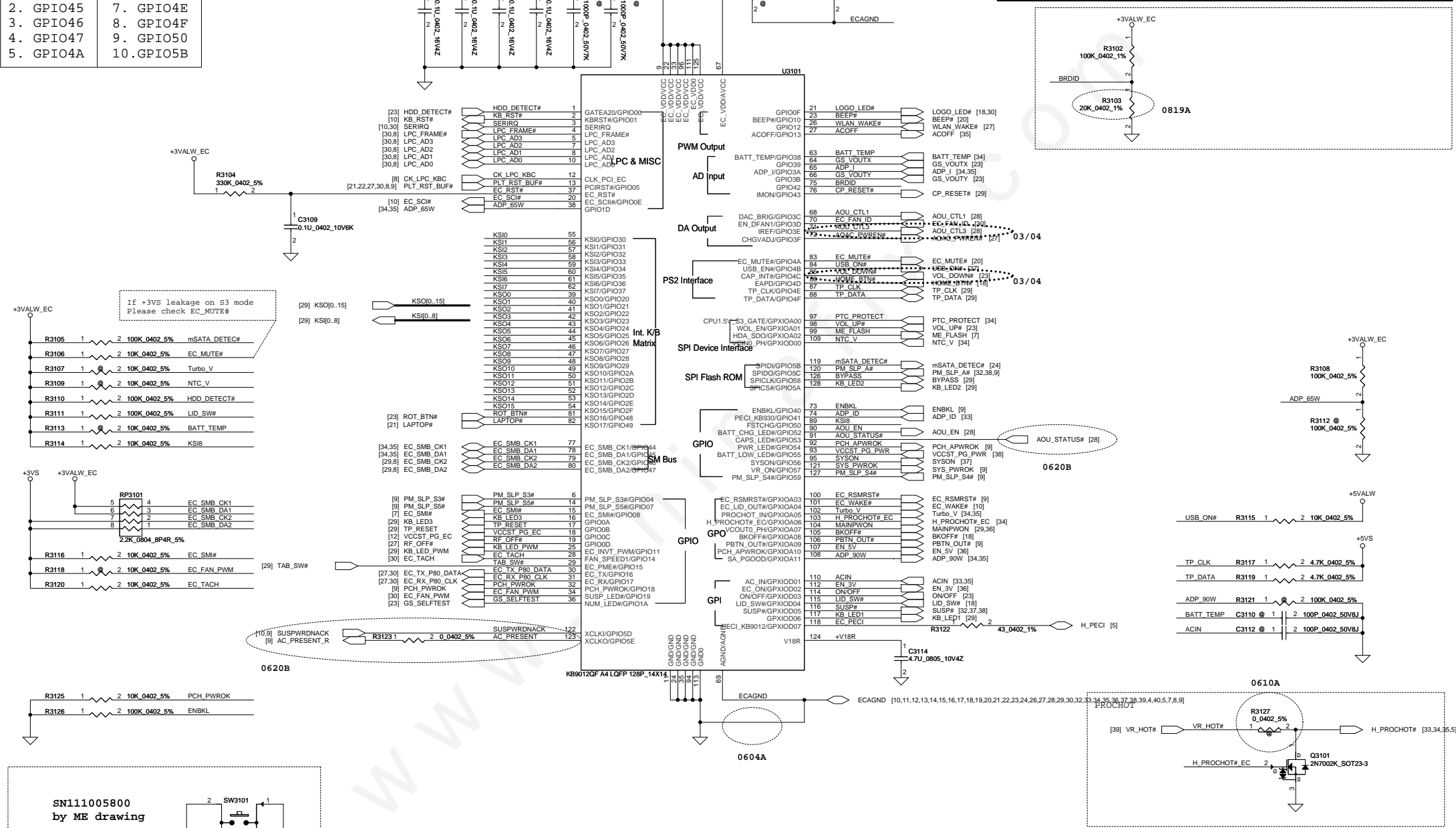
EC KB9012

KB9012 A4 v.22

GPIO W/O internal-PH:

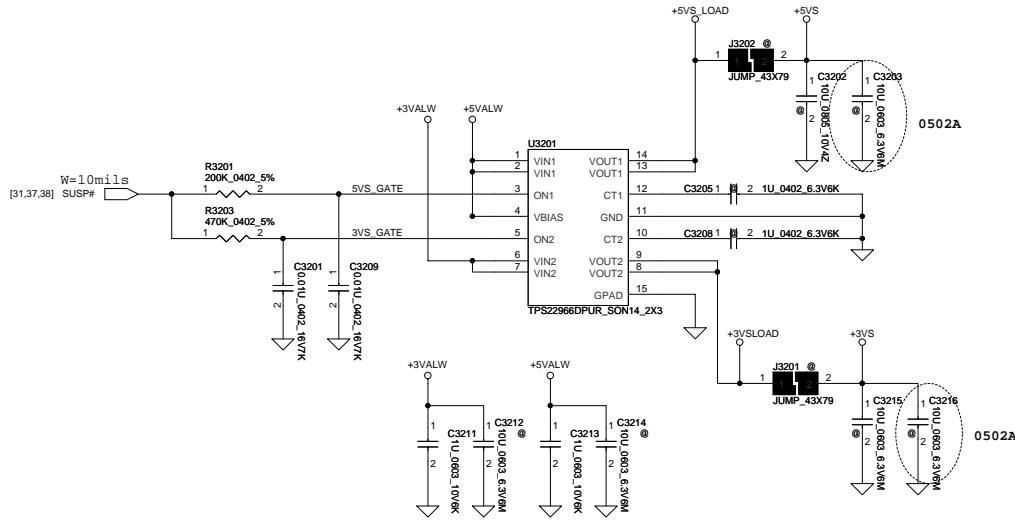
1. GPIO44	6. GPIO4B
2. GPIO45	7. GPIO4E
3. GPIO46	8. GPIO4F
4. GPIO47	9. GPIO50
5. GPIO4A	10. GPIO5B

Vcc	3.3V +/- 5%				
R3102	100K +/- 1%				
Board ID	R3103	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30

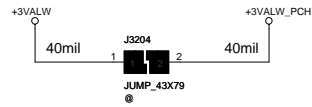


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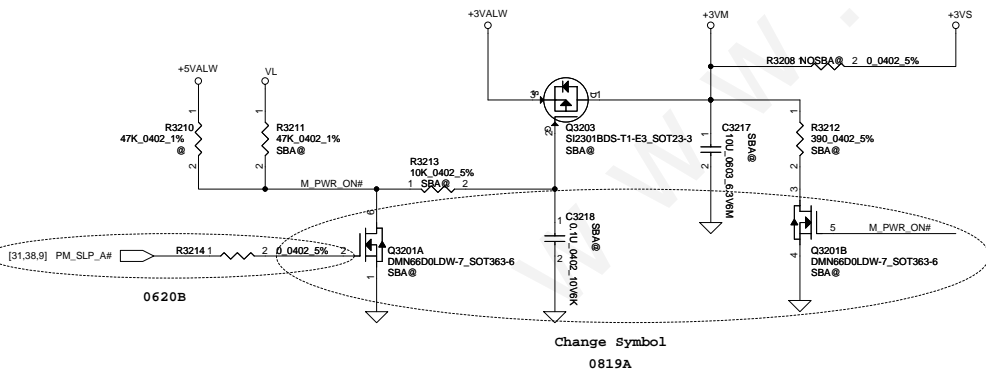
+5VALW TO +5VS
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)



+3VALW TO +3VM (SBA)



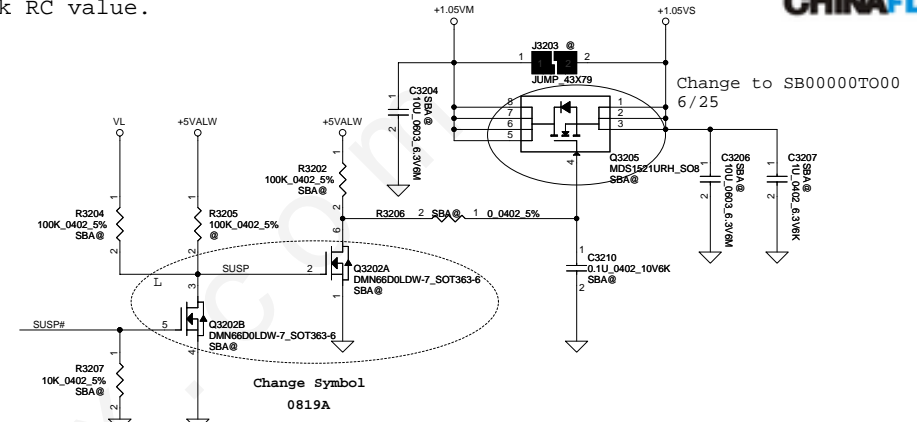
Change Symbol
0819A



PJ703 Short => NOSBA
PJ703 Open => SBA

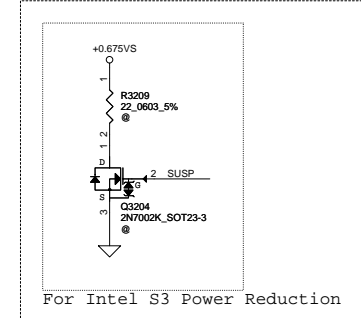
Check RC value.

Rds(on) VGS=4.5V, ID=8.5A, 7mOhm(Max)

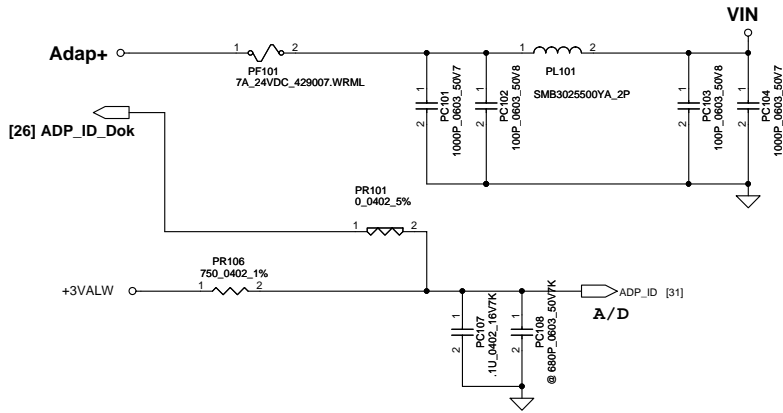


Change Symbol
0819A

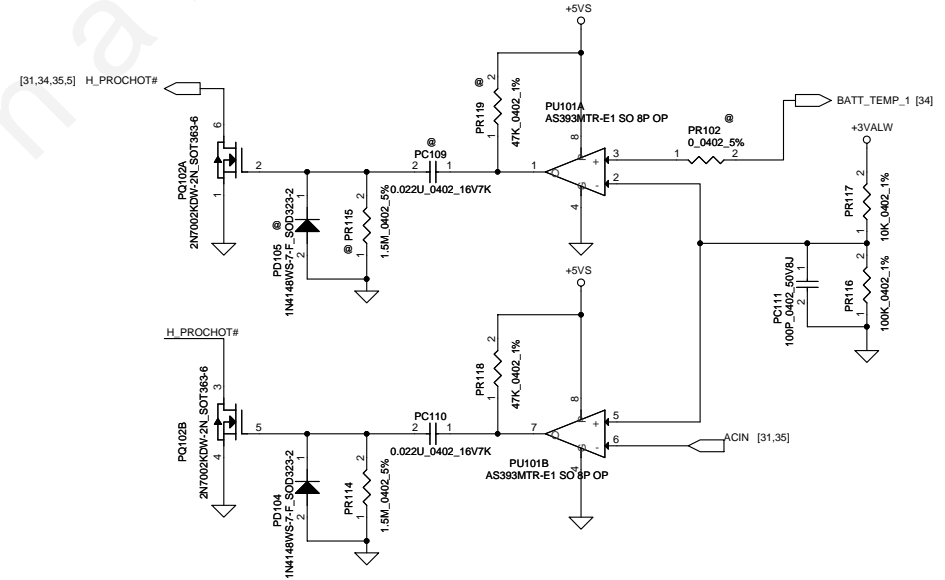
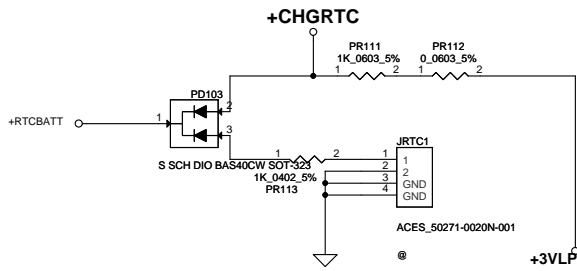
Change to SB00000T000
6/25



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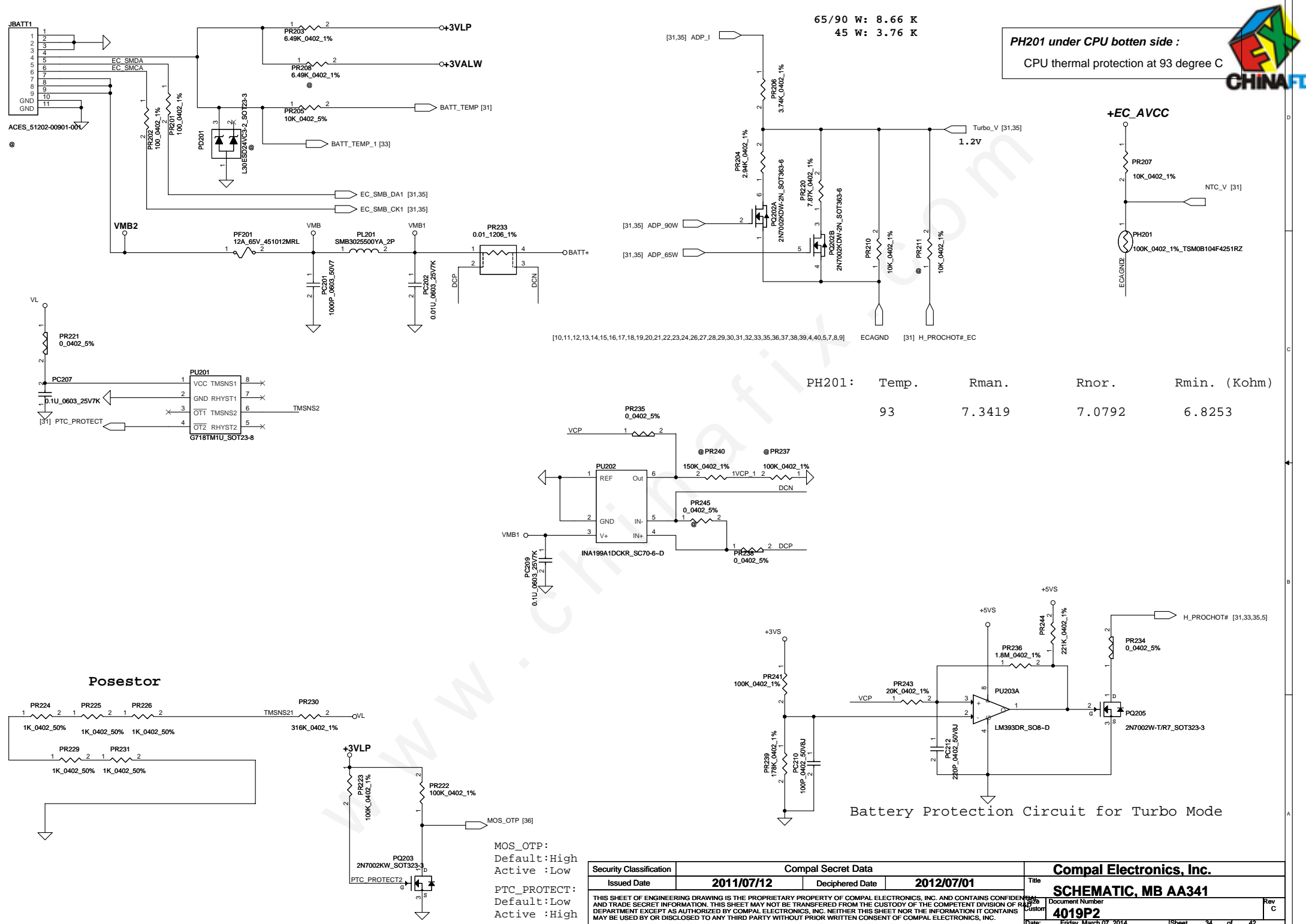


ADP_ID			
AC Adapter	45W	65W	90W
R(ohm)	118	287	549
ADP_ID(V)	0.449	0.913	1.395
Detection	≤ 0.663 ,	≤ 1.134 ,	≤ 1.618
-Voltage(V)	> 0.234	> 0.693	> 1.172

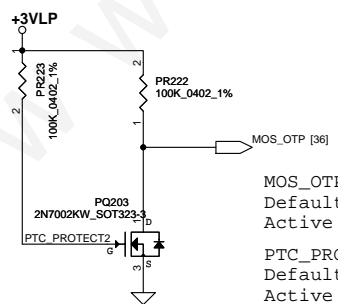
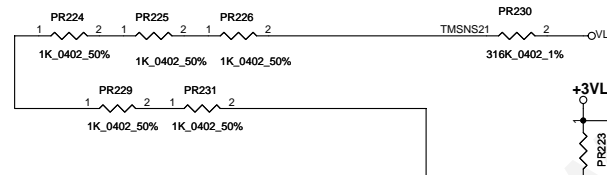




PH201 under CPU bottom side :
CPU thermal protection at 93 degree C



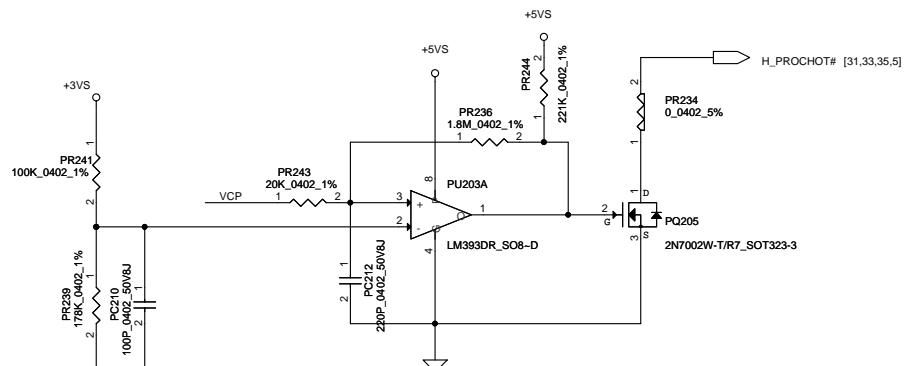
Posistor



MOS_OTP:
Default:High
Active:Low

PTC_PROTECT2:
Default:Low
Active:High

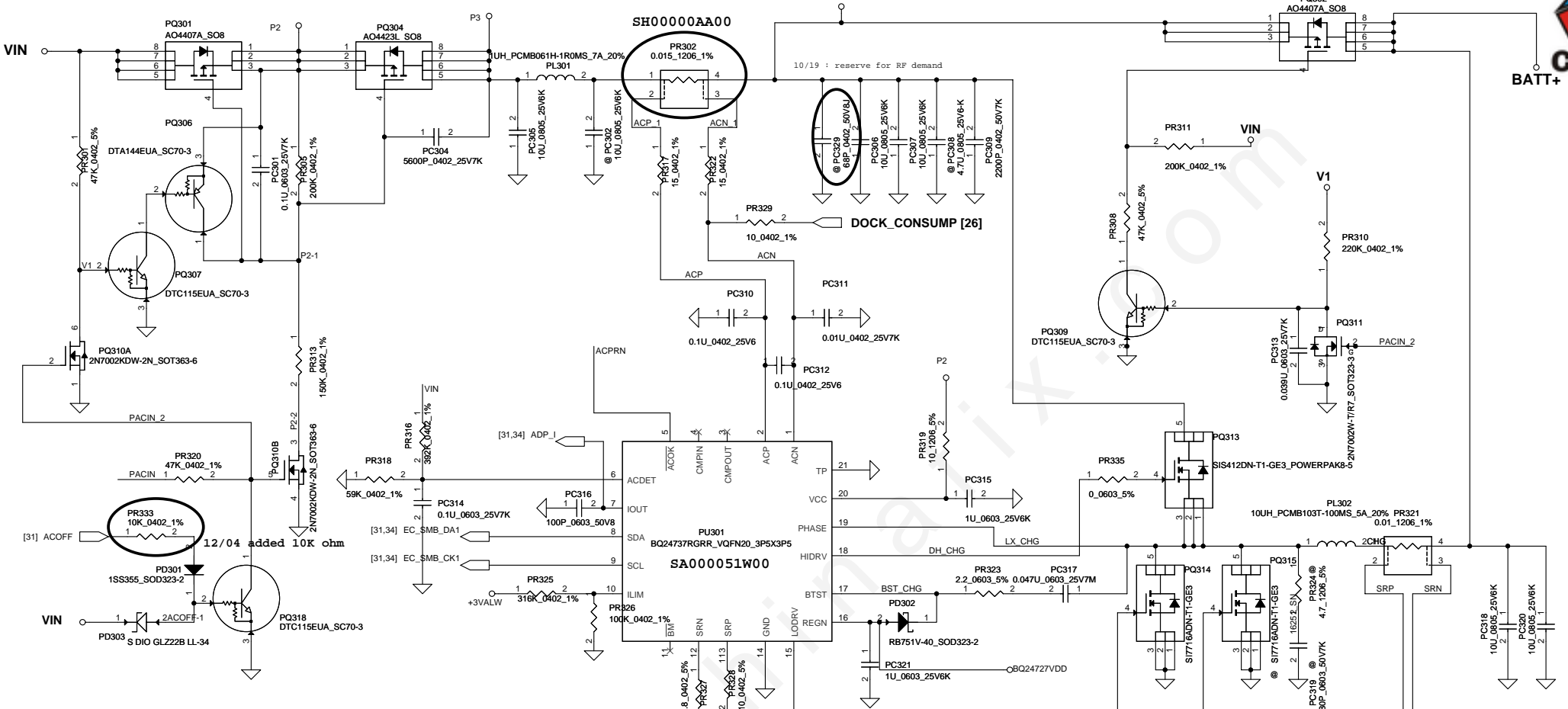
Battery Protection Circuit for Turbo Mode



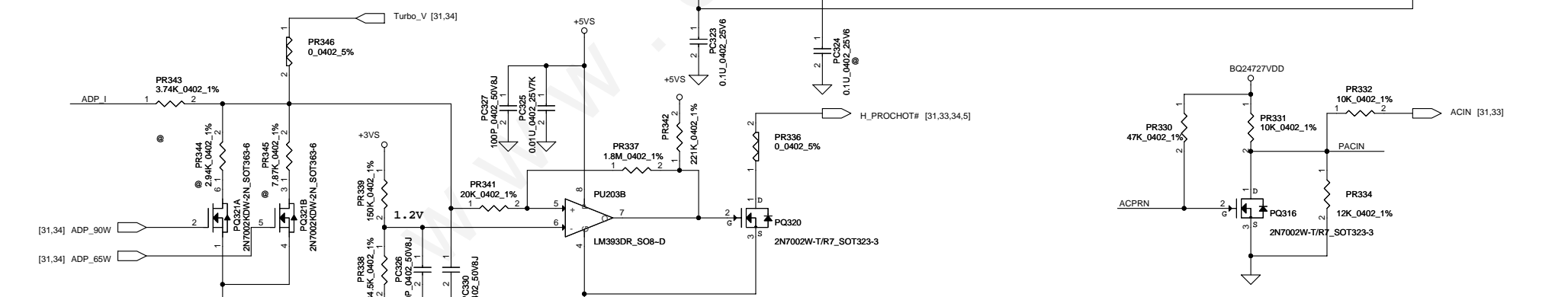
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DCR 换成 15m ohm,CP,Throttling...need redefine with EC

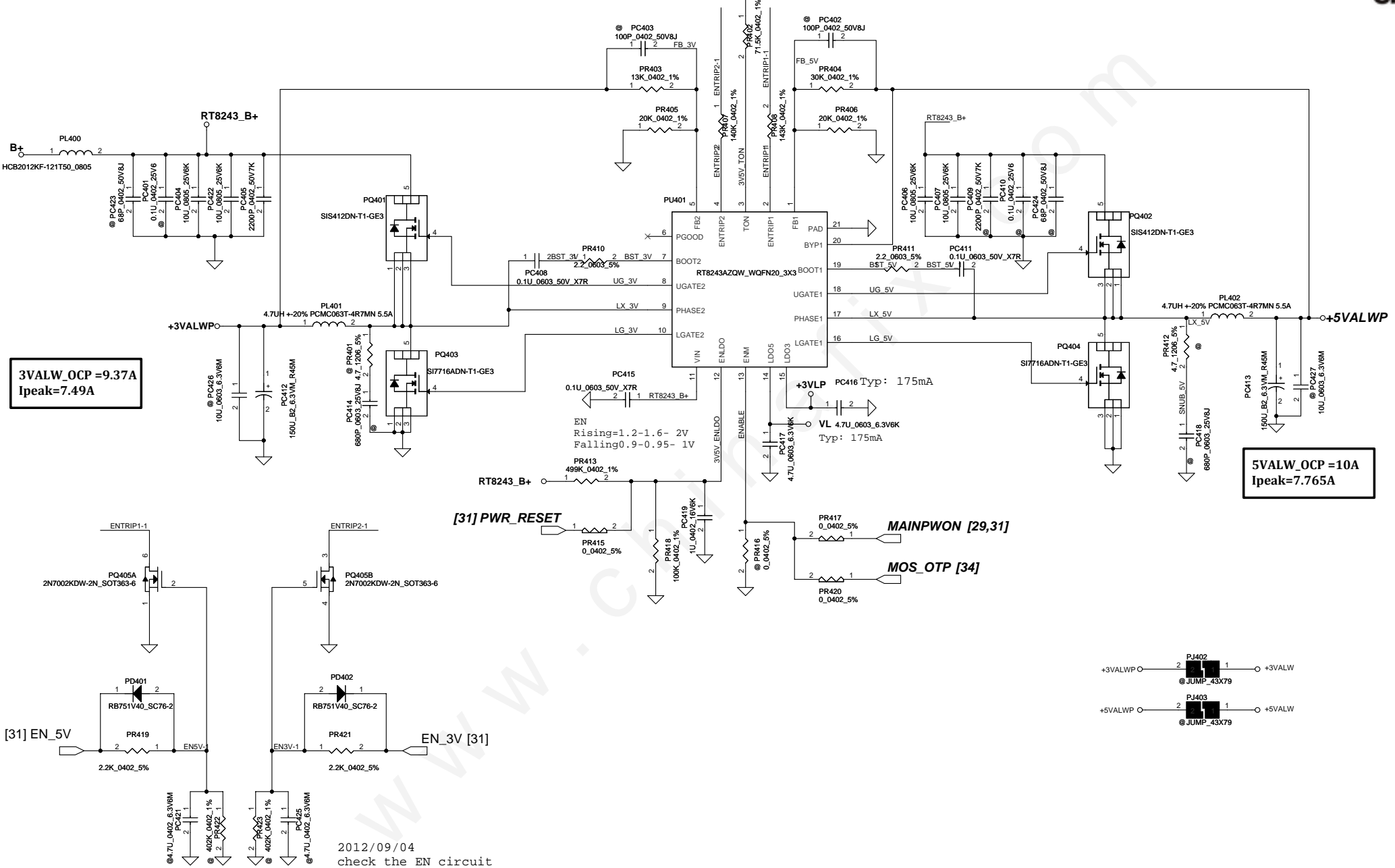


Adapter Protection Circuit for Turbo Mode



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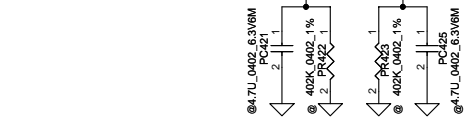
TON (1)SMPS1=305KHZ (+5VALWP)
(2)SMPS2=357KHZ(+3VALWP)



3VALW_OCP = 9.37A
Ipeak = 7.49A

5VALW_OCP = 10A
Ipeak = 7.765A

[31] EN_5V



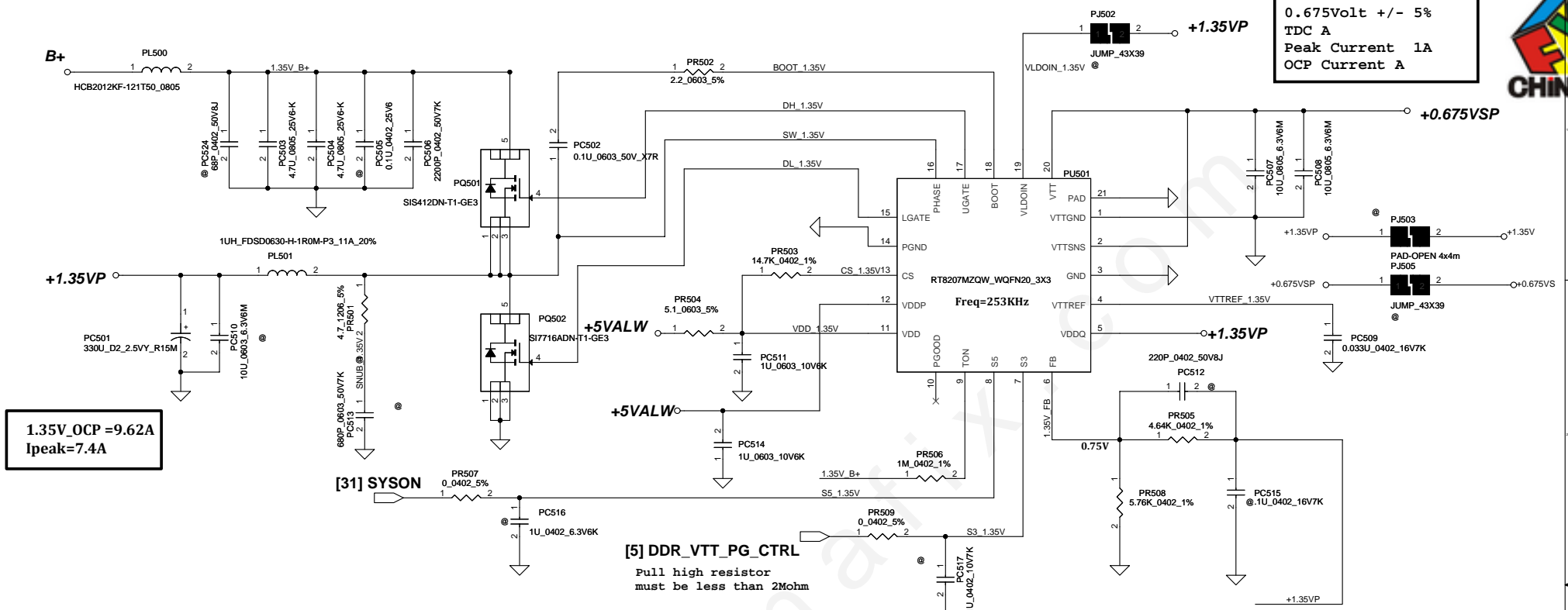
2012/09/04
check the EN circuit



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0.675Volt +/- 5%
TDC A
Peak Current 1A
OCP Current A



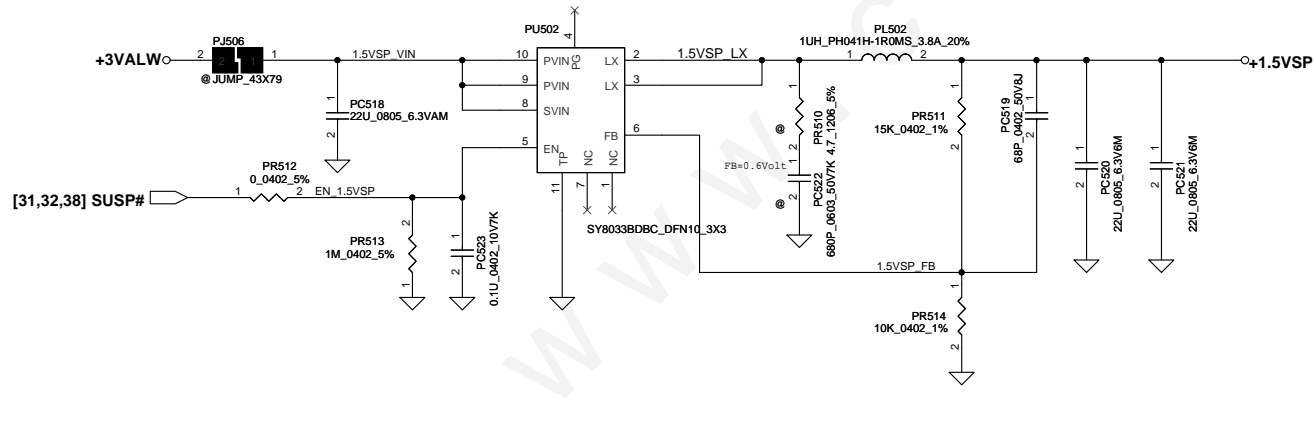
1.35V_OCP = 9.62A
Ipeak = 7.4A

[31] SYSON

[5] DDR_VTT_PG_CTRL
Pull high resistor must be less than 2Mohm

	S3	S5	VDDQ	VTTREF	VTT
STATE	S0	Hi	On	On	On
	S3	Lo	On	On	Off (Hi-Z)
	S4/S5	Lo	Off	Off	Off

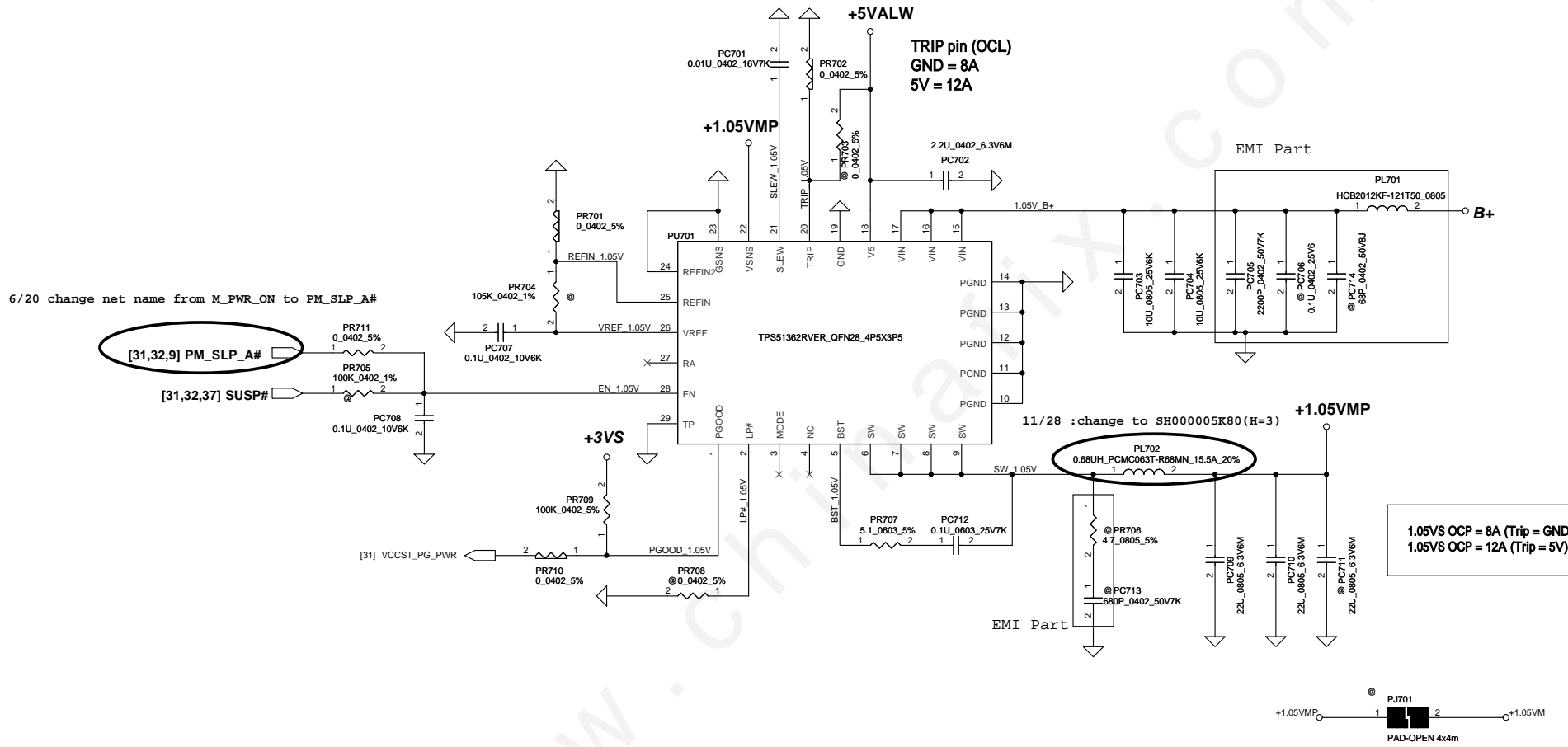
(Discharge) (Discharge) (Discharge)



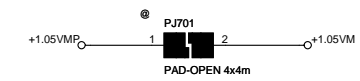
[31,32,38] SUSP#



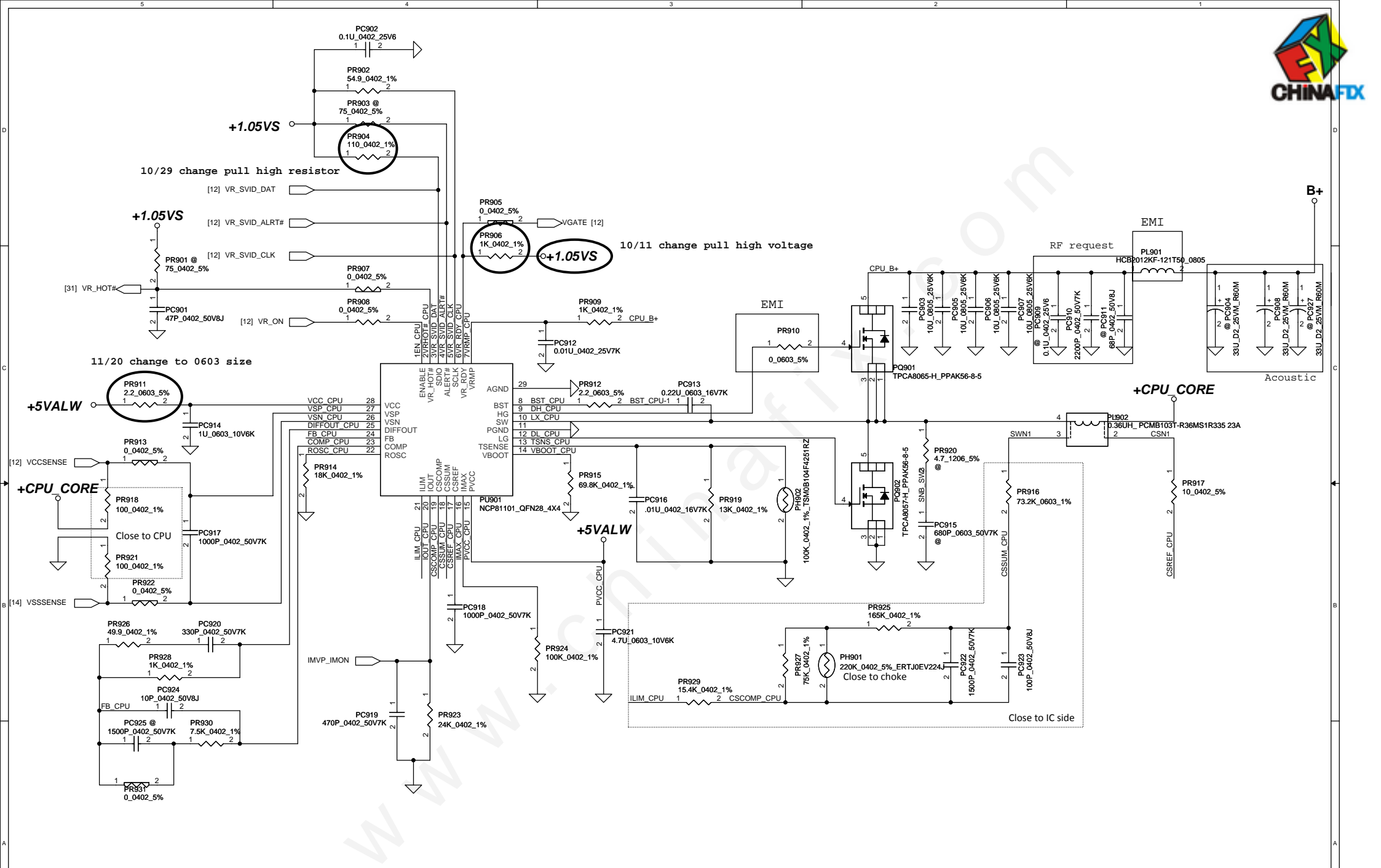
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1.05VS OCP = 8A (Trip = GND)
1.05VS OCP = 12A (Trip = 5V)



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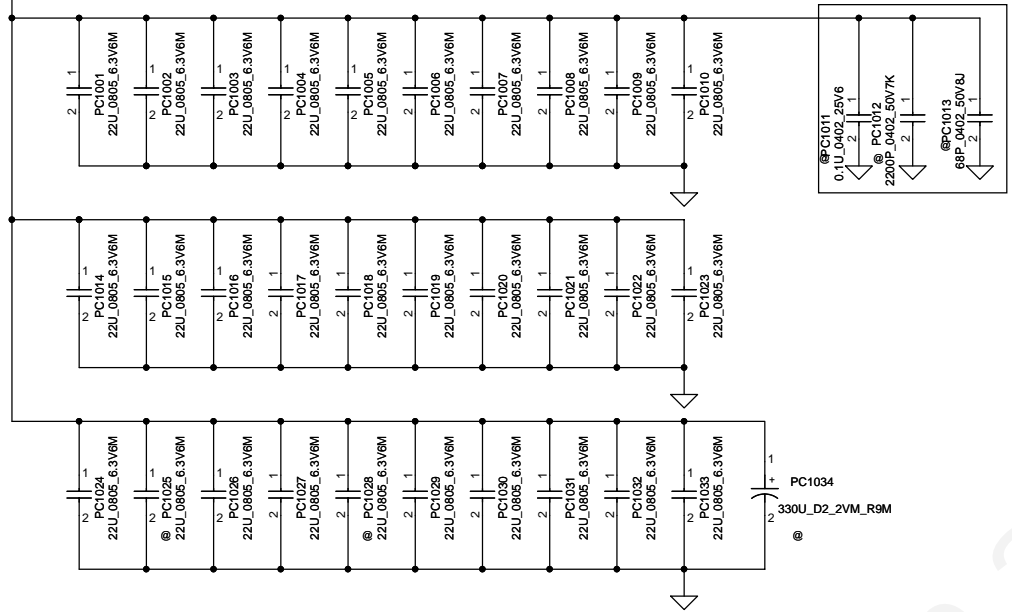


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+CPU_CORE

30 X 22u/0805

RF request



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Item	Reason for change	PG#	Modify List	Date	Phase
1	We just have adpter over-load protection circuit to replace the one-shot circuit, so we can reserve the one-shot circuit.	P33	Un-mount PR119, PC109, PR115, PD105.	2013.04.24	SDV
2	We want to tune the switching ring to meet the derating spec.	P37	Change PC502 from 0.22u to 0.1u.	2013.04.24	SDV
3	For fine tune LL & trainsient of CPU core, we must to change R/C value to meet Intel's spec.	P39	Change PR916 from 47k to 73.2k and PC923 from 560p to 100p, PC1025, PC1028, PC1034 to un-mount.	2013.04.24	SDV
4	For aviod EMI/EMI to damage OP or other components through the loop of BATT_TEMP.	P34	Reserve PD201	2013.04.30	SDV
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function

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