

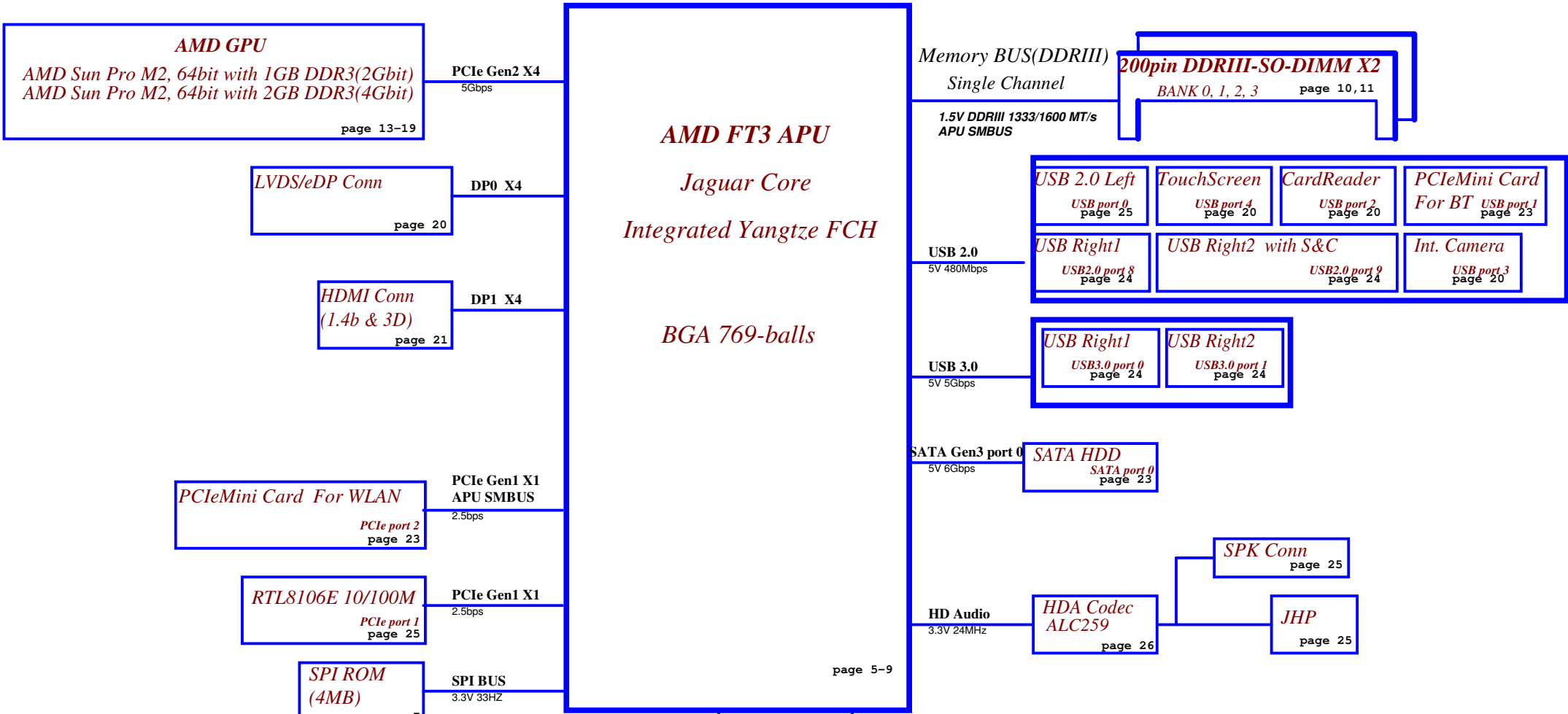
ZRMAE/ZEMAE

Juno/Iakros 10AN/10ANG

LA-A551P REV 1.0 Schematic

AMD KABINI Quad Core 25W for UMA+DIS
AMD KABINI Quad Core 15W
2013-07-05 Rev 1.0

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Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title	Cover Page	
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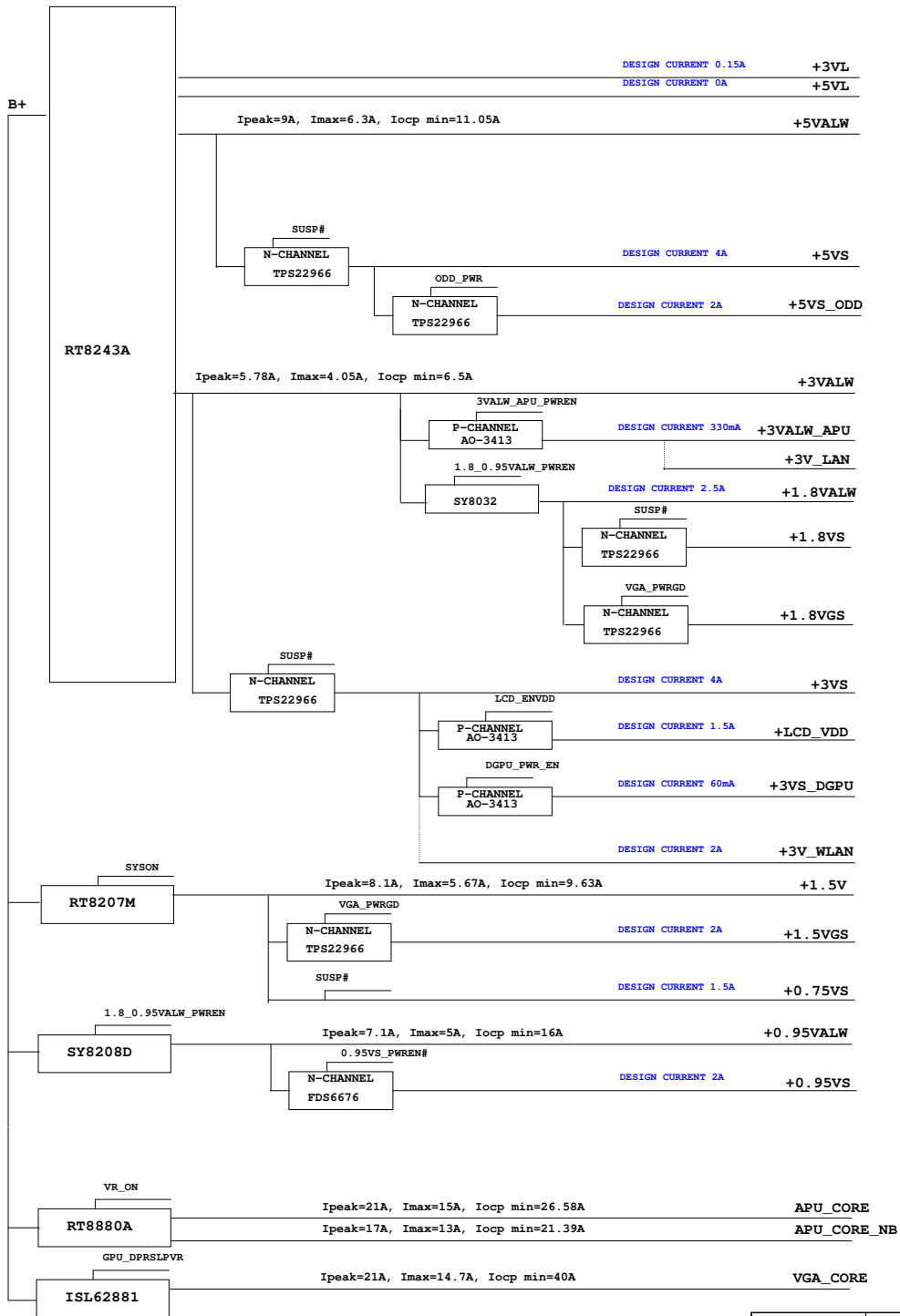


- RTC CKT:** page 30
- Touch Screen Control/B:** page 20
- DC/DC Interface CKT.:** page 29
- Power Circuit DC/DC:** page 30-38
- Power On/Off CKT & Power/B:** page 29

Sub Boards

- CardReader GL834L(USB20 port 3) +USB (USB20 port0) +Audio Combo jack:** page 25
- Touch pad/LED B:** page 25

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Voltage Rails

(O MEANS ON X MEANS OFF)

UMA

BTO Option Table

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.8VALW +0.95VALW +VSB	+1.5V	+5VS +3VS +0.95VS +1.8VS +1.5VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

Function	APU	
description	CPU A4-5000	CPU A6-5200
explain	15W 4C	25W 4C
BTO	A4R1@	A6R1@

Function	GPU	EC		LVDS-eDP		Camera & Mic			KB Light	
description	Sun-Pro M2	9012	885		LVDS-eDP		Camera & Mic			KB Light
explain	VGA	9012	w/	w/ EMI	LVDS	eDP	Camera & Mic			KB Light
BTO	VGA@	9012@	885@	885_EMI@	LVDS@	IEDP@	CAM@	CAM@EMI@	@CAM@EMI@	KBL@

Function	LAN	S&C		Size		Codec	Touch Screen	
description	8106E	TI solution		Size		ALC259	Touch Screen	
explain	8106E	TPS2546	TPS2544	14"	15"	ALC259	W/ Touch	W/O EMI Touch
BTO	8106E@	2546@	2544@	14@	15@	259@	Touch_EMI@	@Touch_EMI@

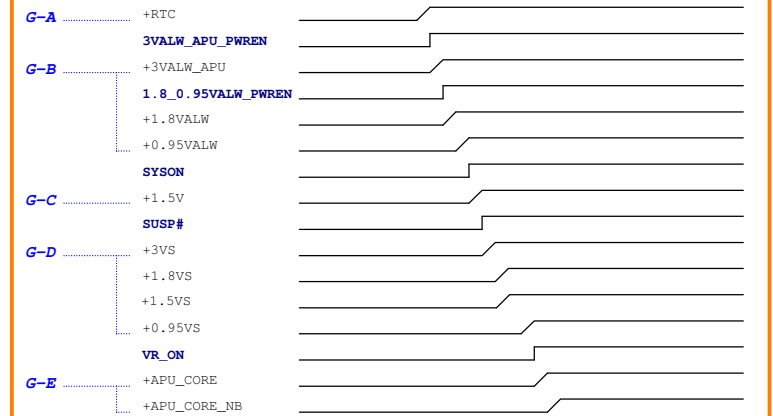
Function	EMI/ESD/RF part				
description	EMI/ESD/RF part				
explain	EMI/ESD/RF part				
BTO	EMI@	@EMI@	ESD@	@ESD@	@RF@

APU SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM A	A0H	1010 0000 b
+3VS	DDR SO-DIMM B	A2H	1010 0010 b
+3VS	WLAN		

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

APU POWER SEQUENCE

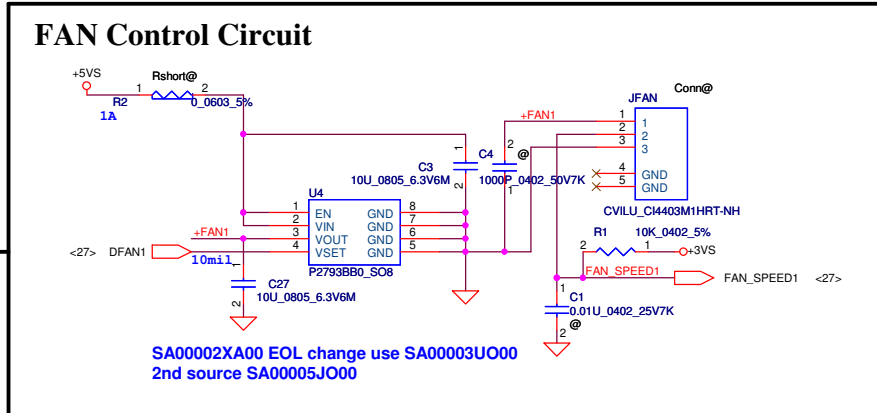
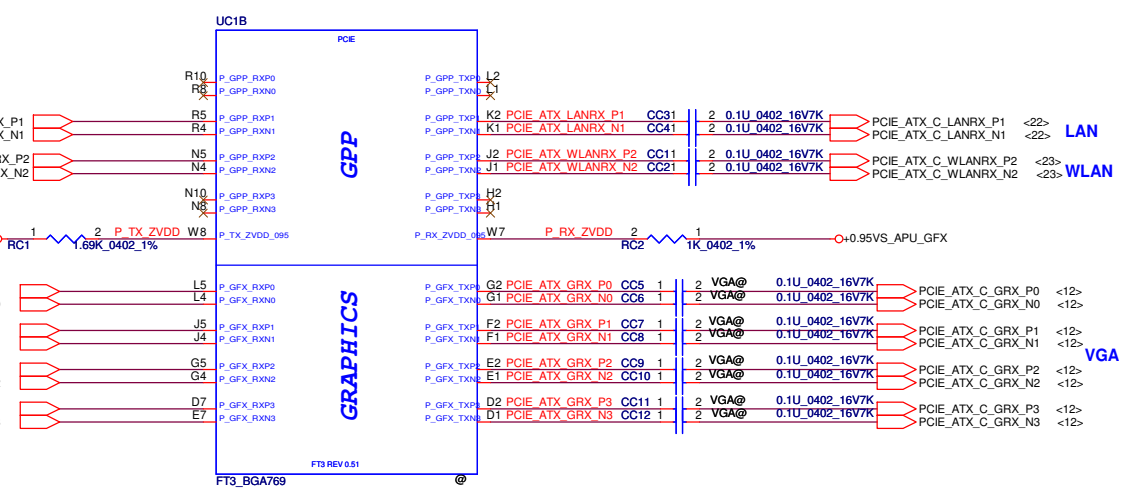
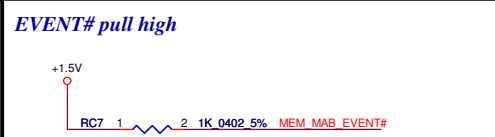
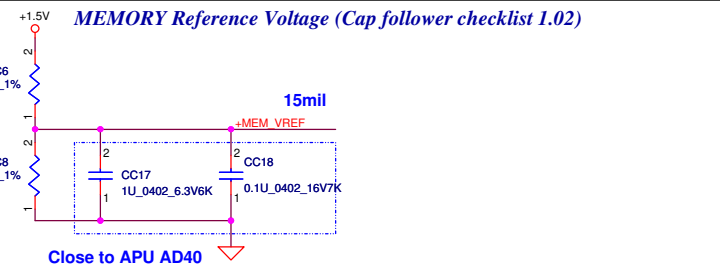
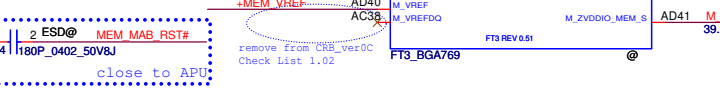
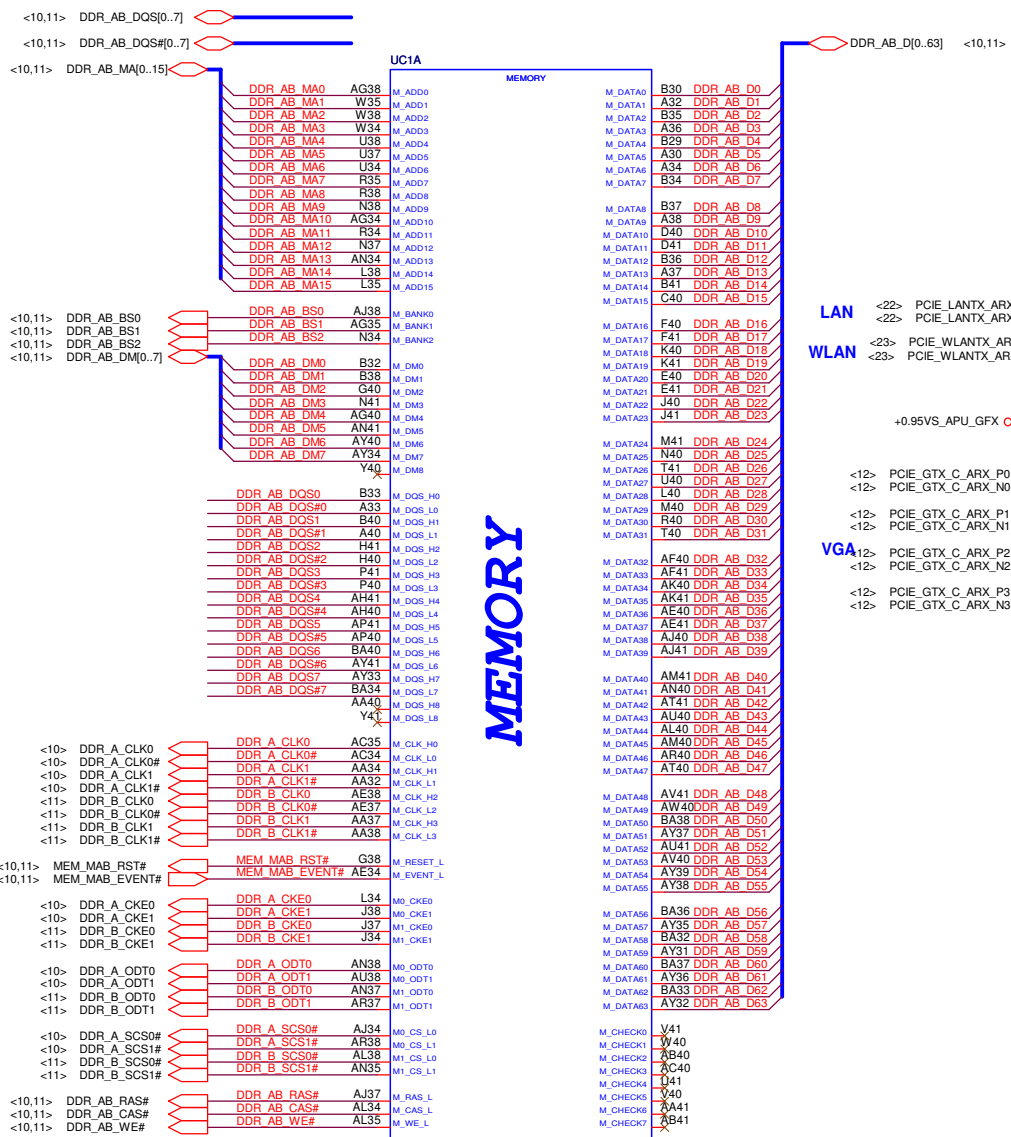


EC SM Bus1 Address

EC SM Bus2 Address

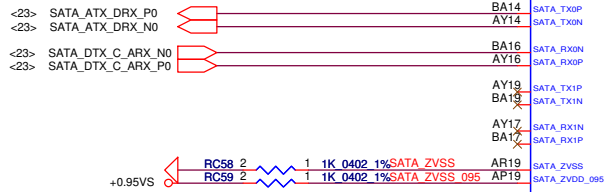
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16H	0001 0110 b	+3VS	VGA thermal	82H	1000 0010 b
+3VL	Charger	12H	0001 0010 b	+3VS	APU thermal	98H	1001 1000 b

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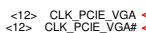


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Issued Date	2013/05/15	Deciphered Date	2015/09/27	FT3 DISP/MISC/HDT	
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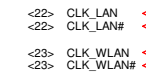
SATA HDD



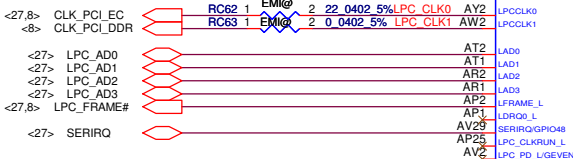
VGA



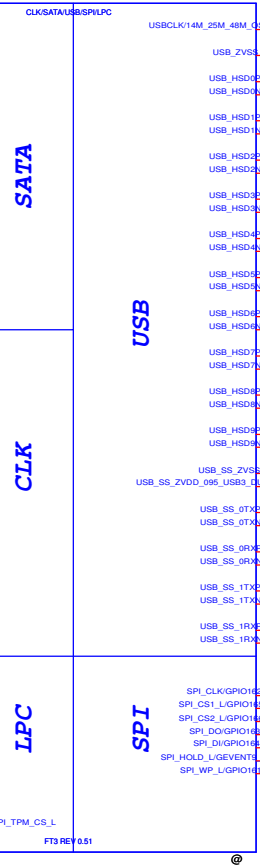
**LAN
WLAN**



EC



UC1E

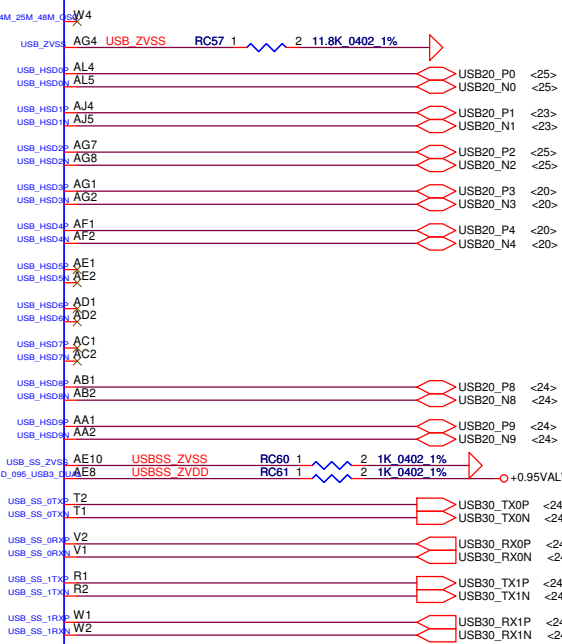


SATA

USB

CLK

SPI

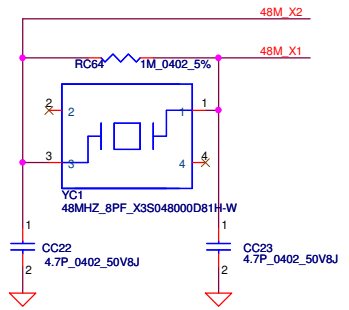


USB2.0-Left1 (Debug Port)
WLAN (BT)
Cardreader
Int. Camera
Touch Screen

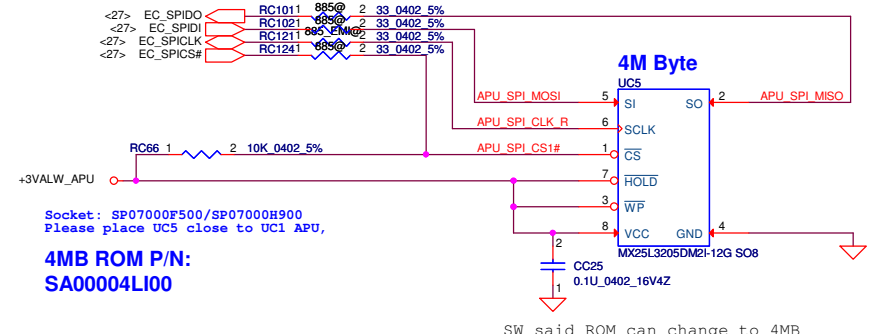
USB2.0-Right1
USB2.0-Right2

USB3.0-Right1
USB3.0-Right2

48KMHZ CRYSTAL



SPI ROM



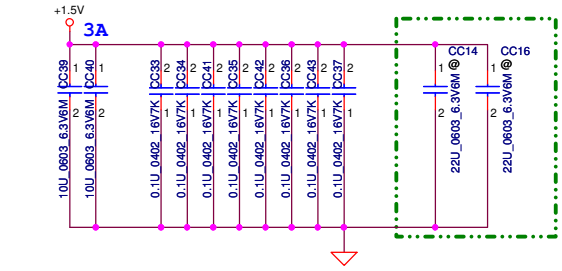
Socket: SP07000F500/SP07000H900
Please place UC5 close to UCI APU,
4MB ROM P/N:
SA00004LI00

SW said ROM can change to 4MB

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Issued Date	2013/05/15	Deciphered Date	2015/09/27	FT3-SATA/CLK/USB/SPI/LPC	
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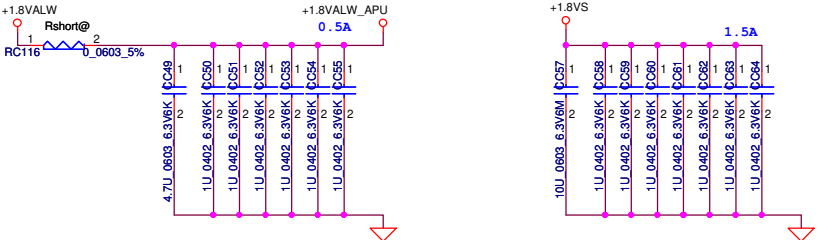
1.5V OF APU

AMD CKL v1.01	10uF	0.1uF	180pF
VDDIO_MEM_S	2	8	4

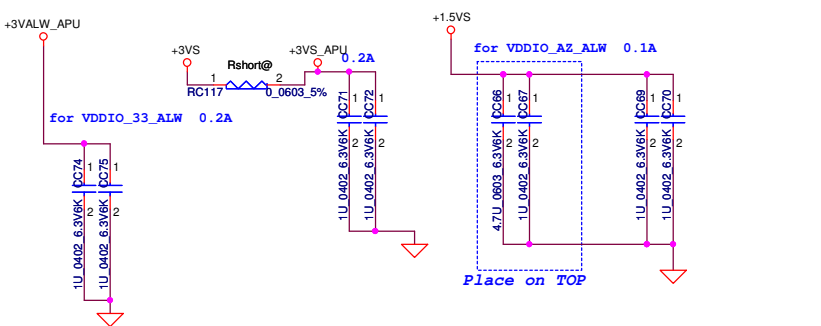


1.8VALW & 1.8VS OF APU

AMD CKL v1.01	10uF	4.7uF	1uF	180pF
VDD_18	1	7	1	
VDD_18_ALW	1	6	1	

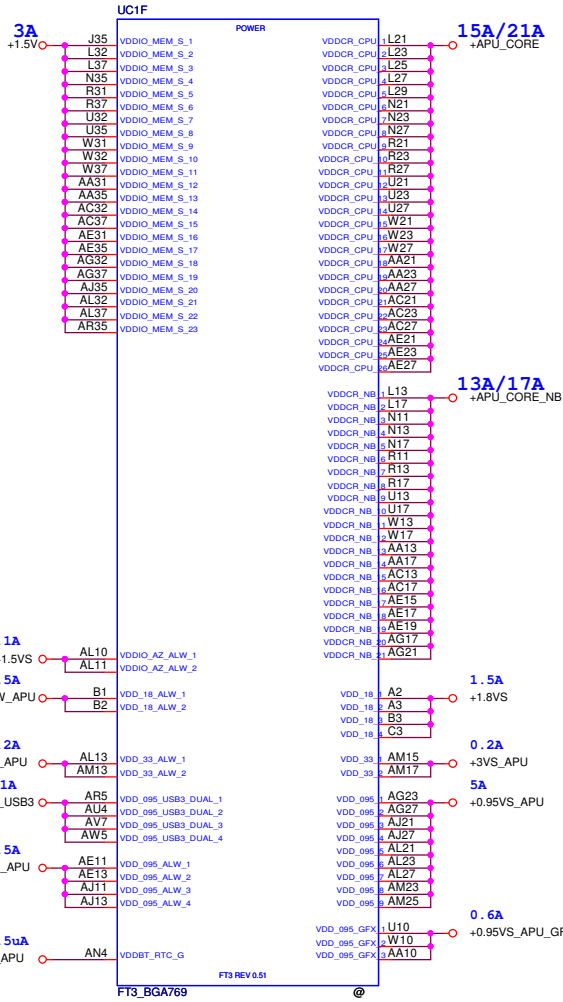
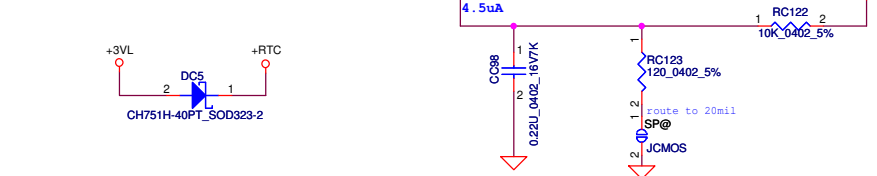


3.3VALW & 3.3VS OF APU

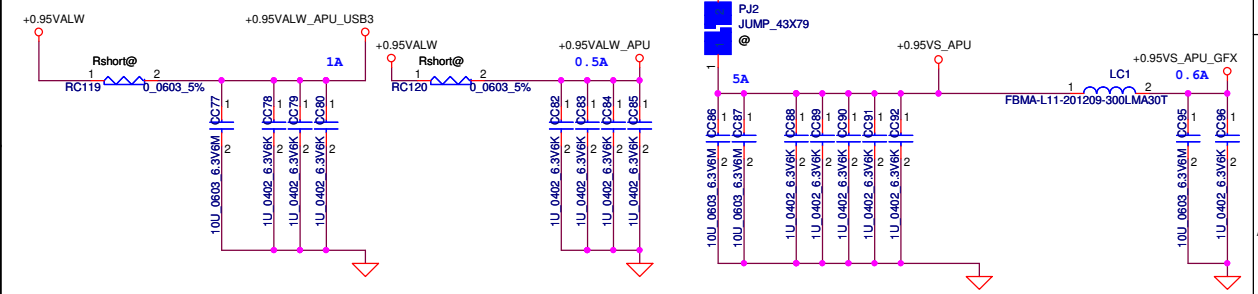


RTC OF APU

AMD CKL v1.01	4.7uF	1uF	180pF
VDDIO_AZ_ALW	1	3	1
VDDIO_33_ALW	2	2	1
VDDIO_33	2	2	1



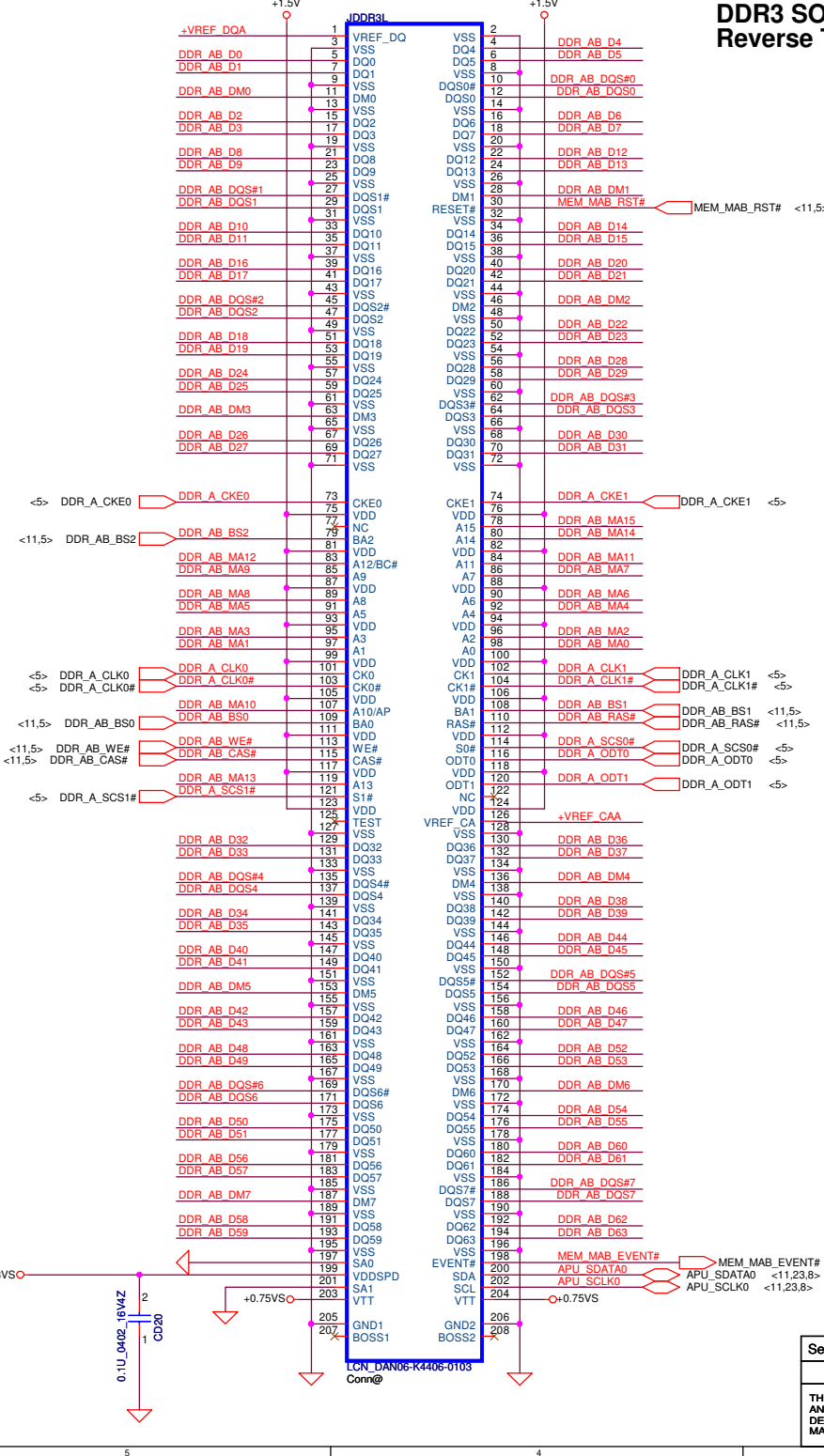
0.95VALW & 0.95VS OF APU



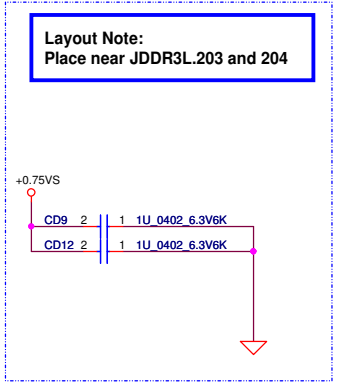
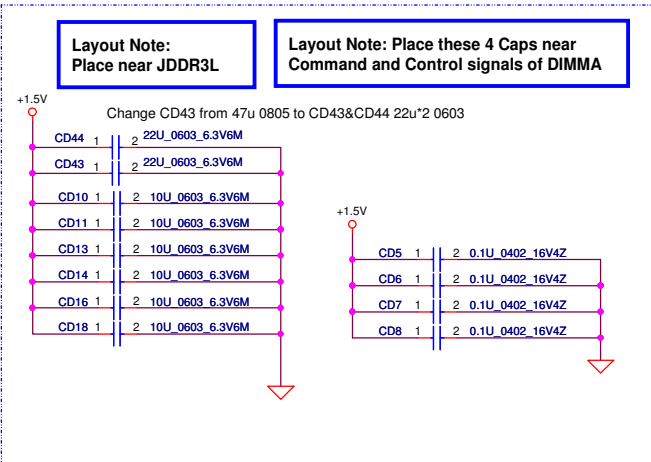
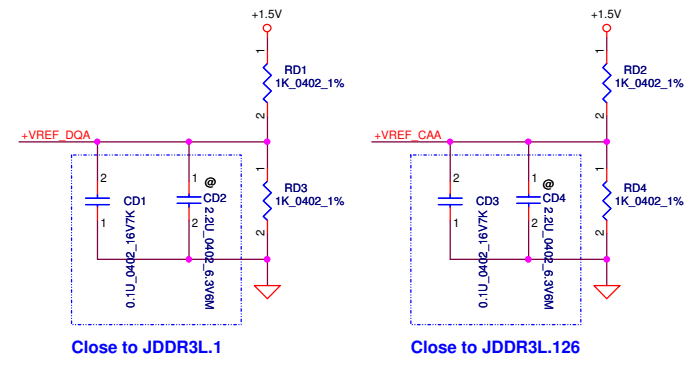
AMD CKL v1.01	10uF	1uF	180pF
VDD_095_USB3_DUAL	2	3	1
VDD_095	2	5	1
VDD_095_ALW	4	1	
VDD_095_GFX	1	1	

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DDR3 SO-DIMM A Reverse Type

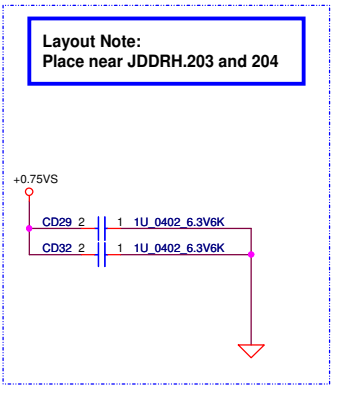
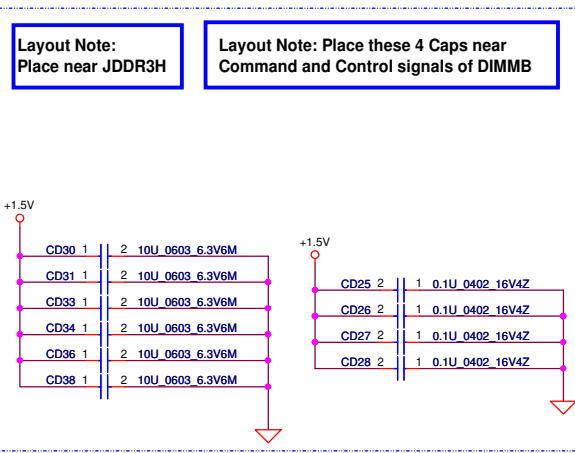
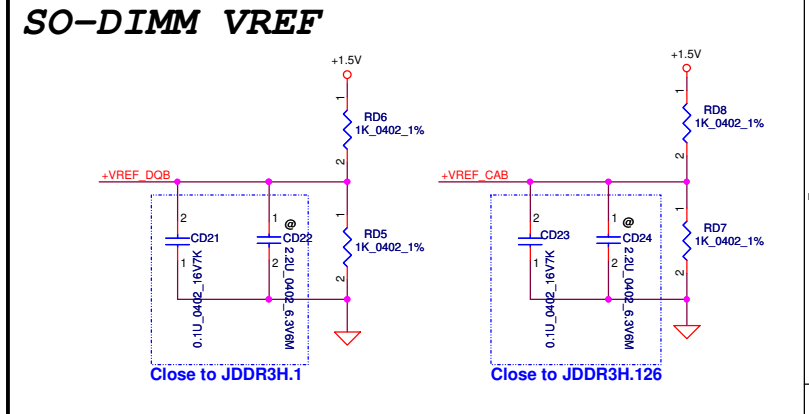
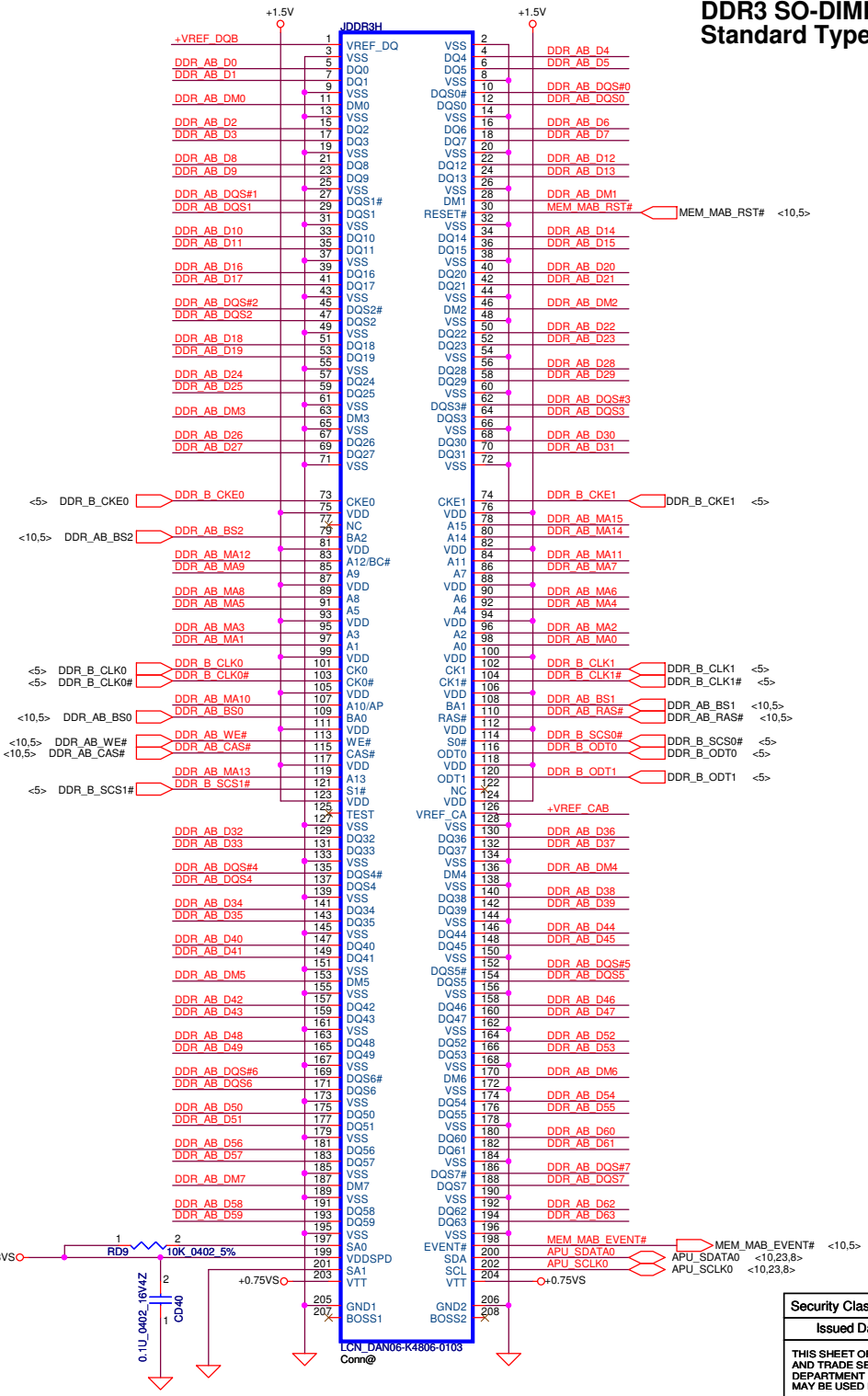


SO-DIMM VREF

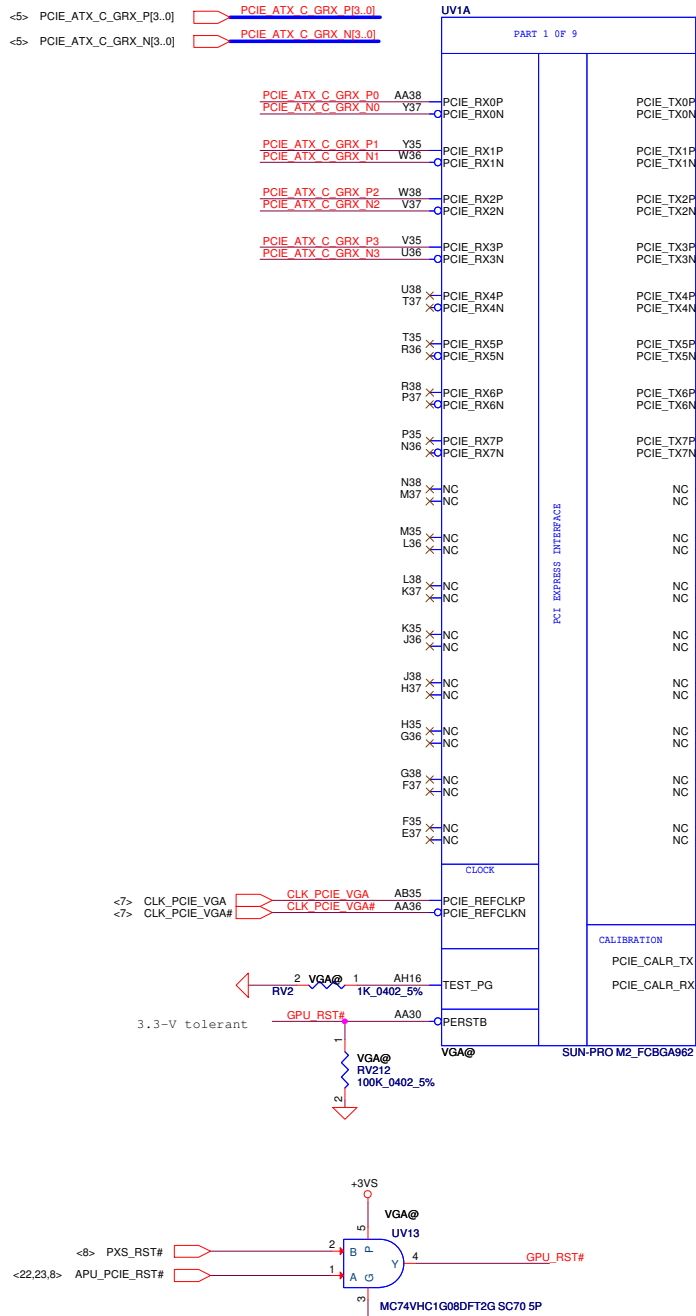


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				DDR3-SODIMMA	
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DDR3 SO-DIMM B Standard Type

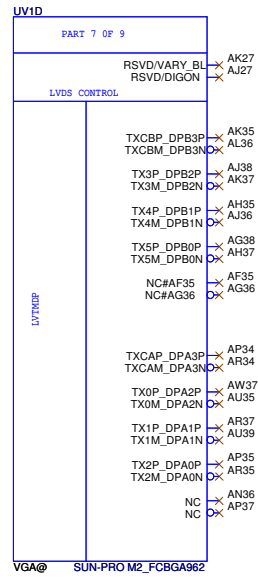


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AC Coupling Capacitor
 PCIe Gen1 and Gen2 only: Recommended value is 100 nF 10%.
 PCIe Gen3: Recommended value is 220 nF 10%.

LVDS Interface



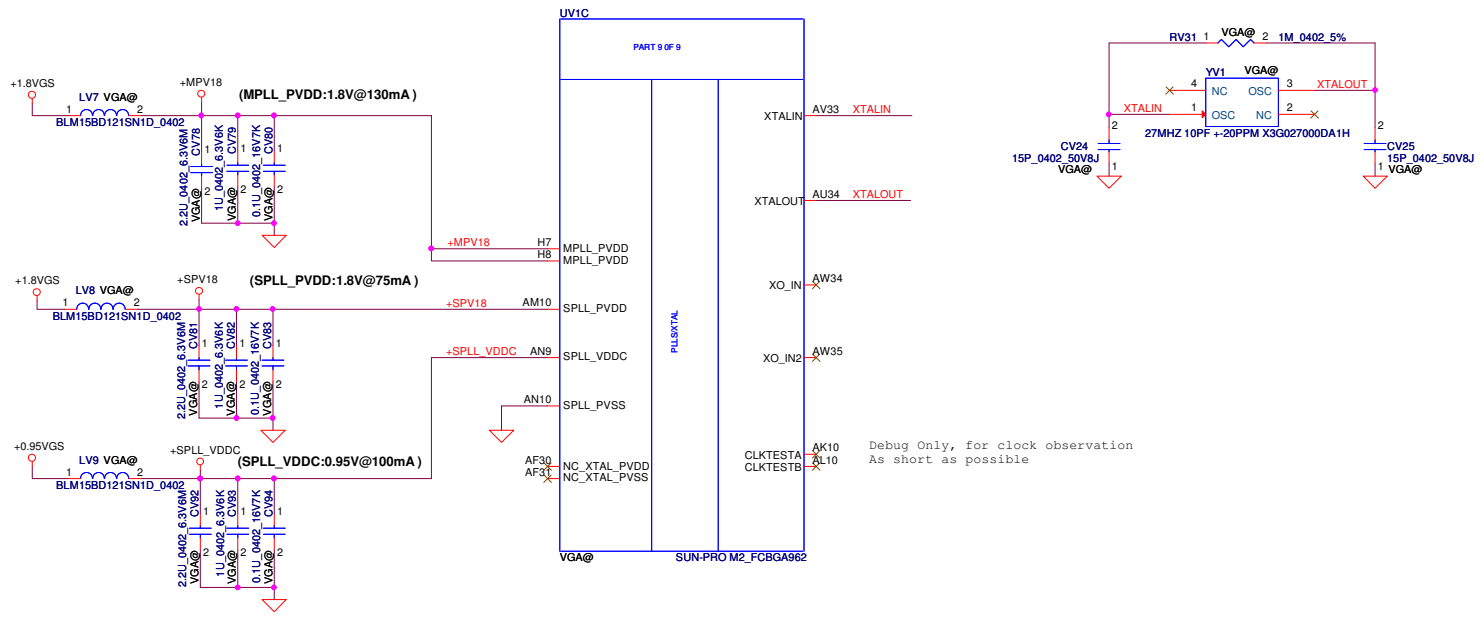
For MEMCLK 1GHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-107G:K	1.35V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-BC11	1.5V/900MHz	111	4750	NC

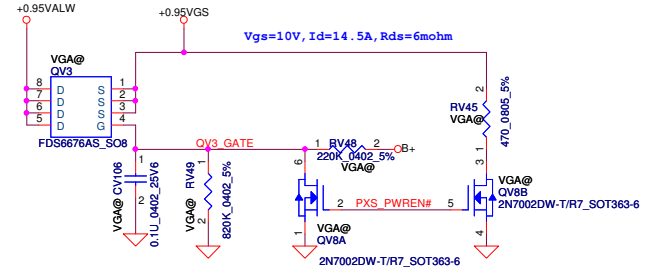
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

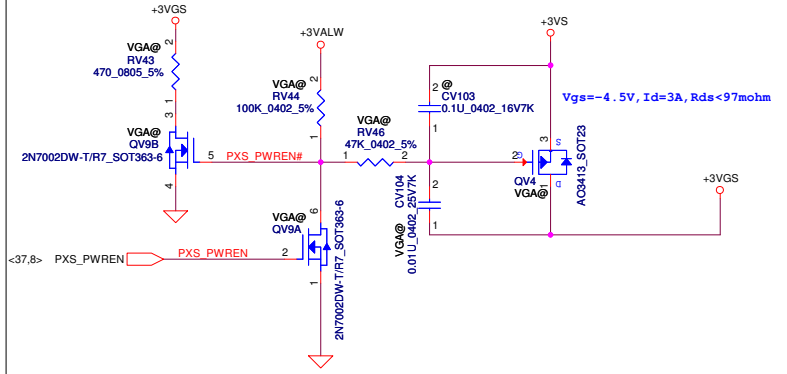
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



+0.95VS to +0.95VGS



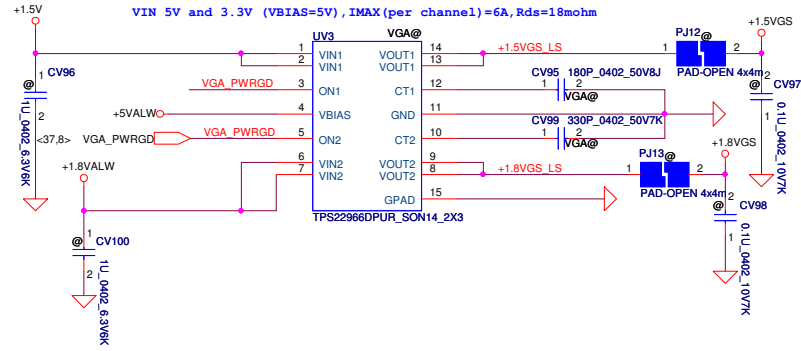
+3VS to +3VGS



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Only for Kabini

+1.8VALW to +1.8VGS
+1.5V to +1.5VGS

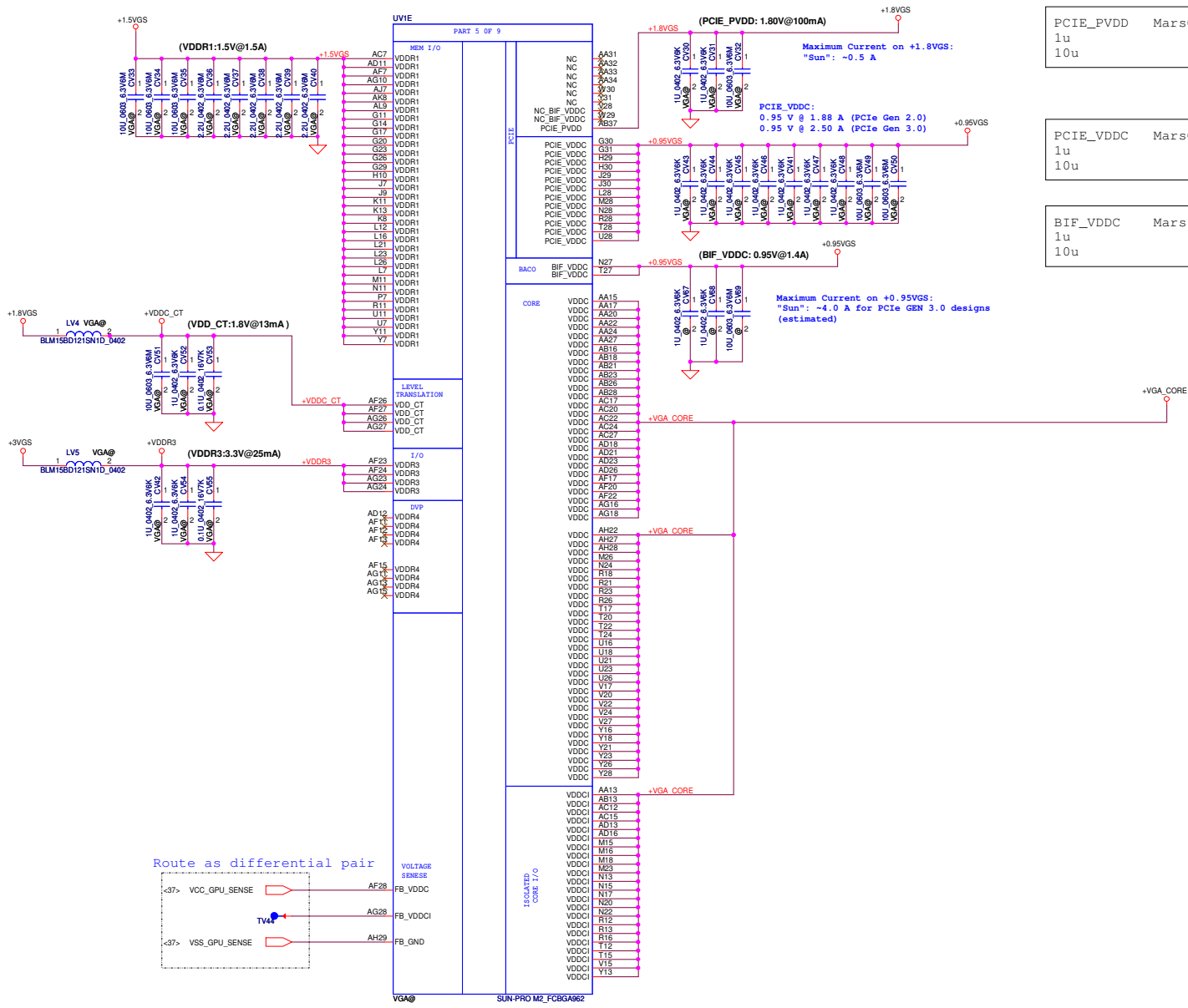


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VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	0
2.2u	5	5
10u	3	3

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDDR3	Mars	check list	Design
120ohm	1	1	1
1u	3	2	2
10u	1	0	0
0.1u	0	1	1

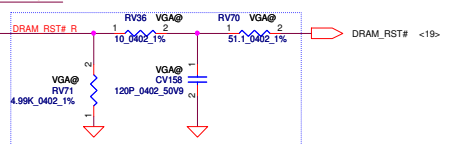
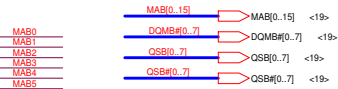
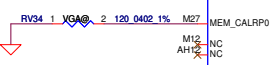
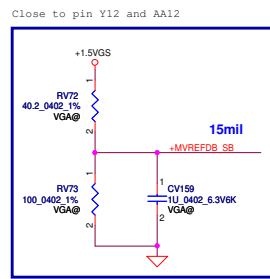
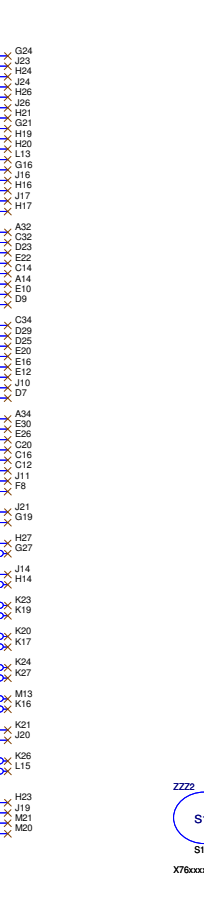
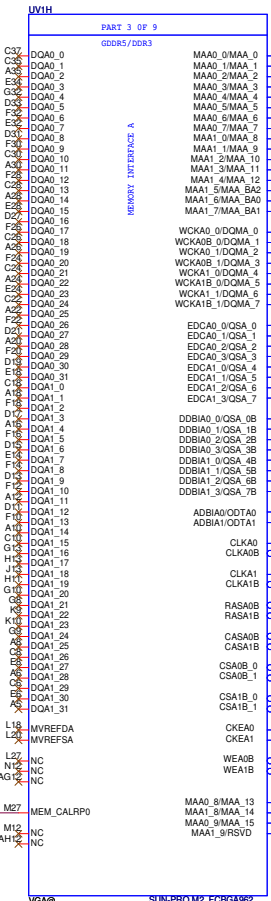


PCIE_PVDD	MarsCRB	Design
1u	2	2
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	7
10u	2	2

BIF_VDDC	Mars	check list	Design
1u	1	1	1
10u	1	1	1

Need check all power current and decoupling capacitors after got SUN databook and reference schematic.



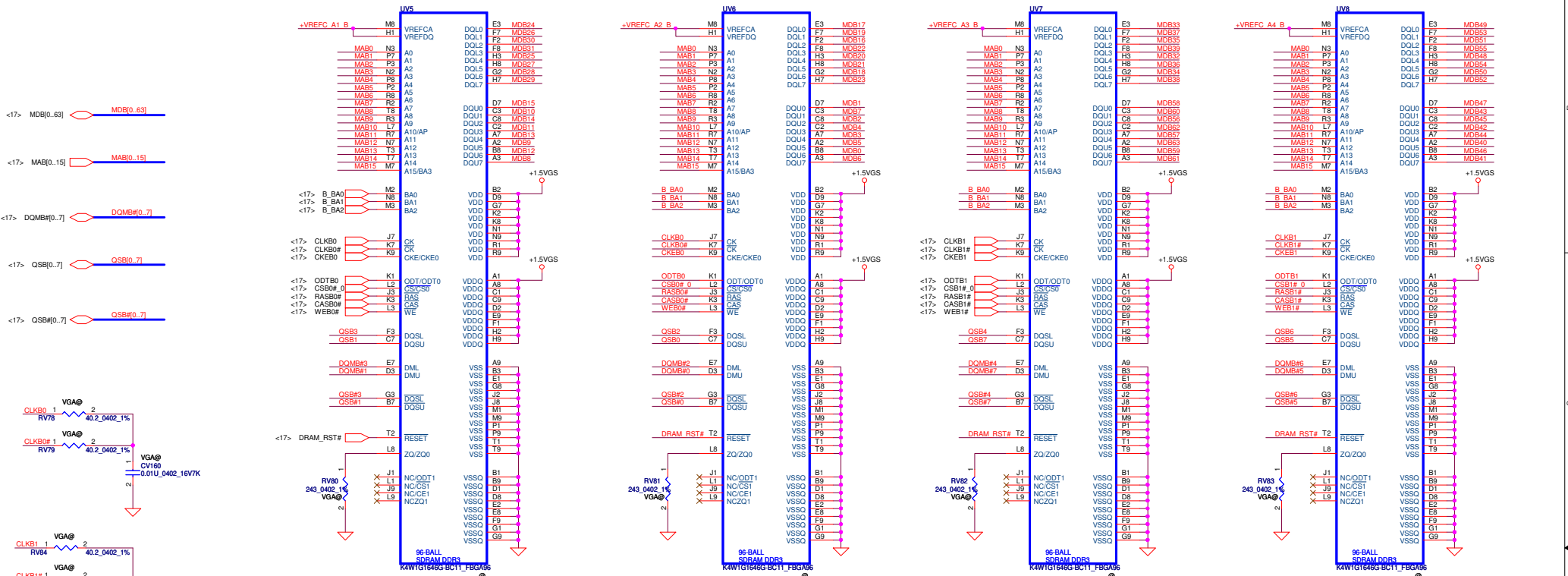
Memory clock 900MHz

R_{pu} & R_{pd} resistor:
0402 1% resistors are required.

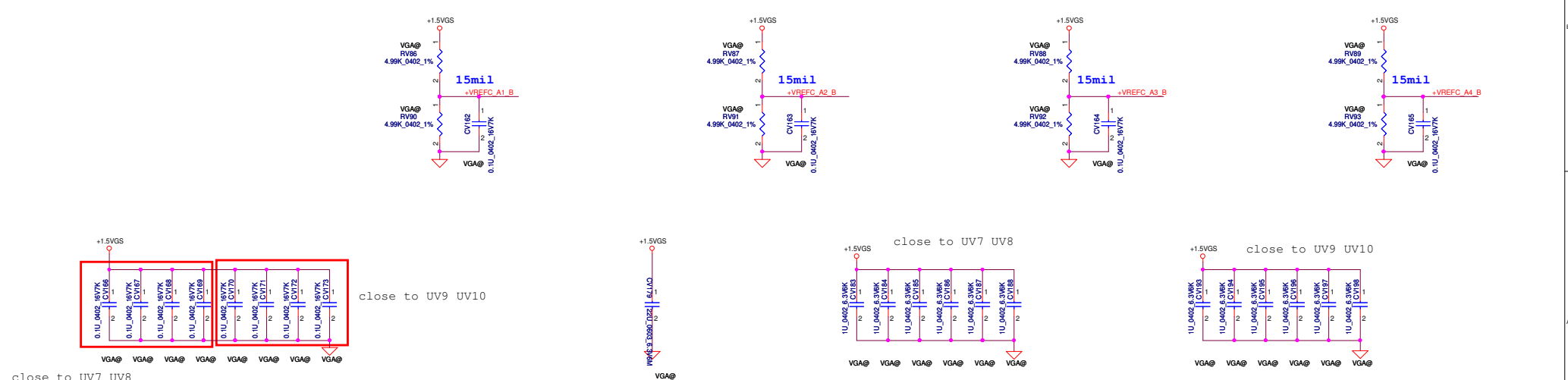
Place all these components close to GPU (Within 25mm) and keep all component close to each other

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R _{pu}	R _{pd}
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A		2Gbit	128M*16	1GB/4pcs	0	0	0	RV20	RV27
SUN PRO-M2	64bit	Micron	SA00005XB00	MT41K128M16JT-107G:K		2Gbit	128M*16	1GB/4pcs	0	0	1	RV20	RV27
SUN PRO-M2	64bit	Samsung	SA00005SH00	K4W2G1646E-BC11		2Gbit	128M*16	1GB/4pcs	0	1	0	RV20	RV27
SUN PRO-M3	64bit	Micron	SA000065D30	MT41K256M16HA-107G:E		4Gbit	128M*16	2GB/4pcs	1	1	0	RV20	RV27
SUN PRO-M4	64bit	Samsung	SA000068R20	K4W4G1646B-HC11		4Gbit	128M*16	2GB/4pcs	1	1	1	RV20	RV27

CHANNEL B: 512MB/1024MB DDR3



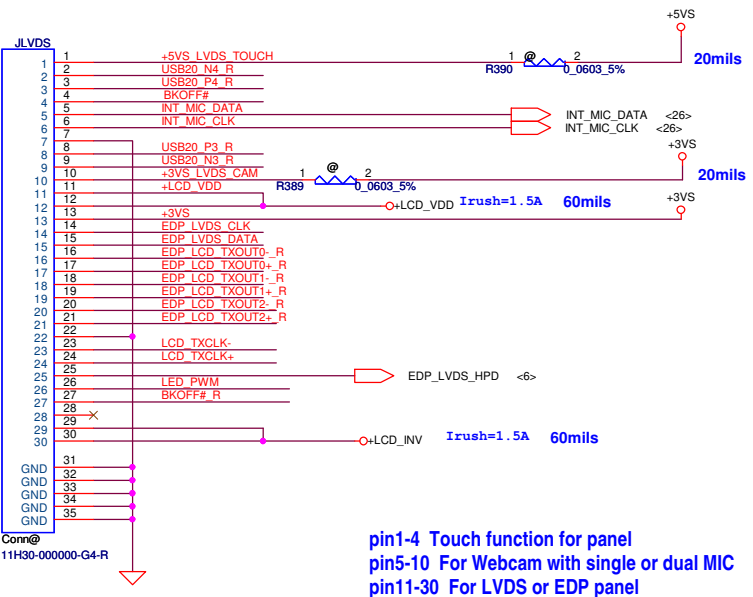
Supported Memory Configurations: Up to 4 Gbit/part for DDR3.



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Issued Date	2013/05/15	Deciphered Date	2015/09/27	VRAM Channel B	
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Size	C	Document Number	LA-A551P	Rev	1.0
Date:	Tuesday, July 16, 2013	Sheet	19	of 40	

- <6> EDP_LCD_TXOUT0+_R EDP_LCD_TXOUT0+_R
- <6> EDP_LCD_TXOUT0-_R EDP_LCD_TXOUT0-_R
- <6> EDP_LCD_TXOUT1+_R EDP_LCD_TXOUT1+_R
- <6> EDP_LCD_TXOUT1-_R EDP_LCD_TXOUT1-_R
- <6> EDP_LCD_TXOUT2+_R EDP_LCD_TXOUT2+_R
- <6> EDP_LCD_TXOUT2-_R EDP_LCD_TXOUT2-_R
- <6> LCD_TXCLK+ LCD_TXCLK+
- <6> LCD_TXCLK- LCD_TXCLK-
- <6> EDP_LVDS_CLK EDP_LVDS_CLK
- <6> EDP_LVDS_DATA EDP_LVDS_DATA

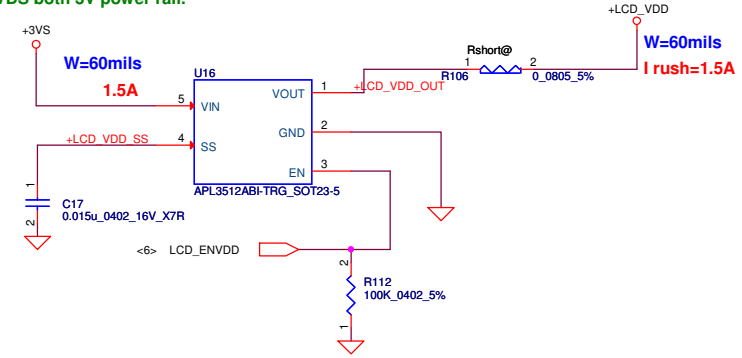
If it's EPD, they're become
 LCD_TXOUT2+_R = EDP_TX0+
 LCD_TXOUT2-_R = EDP_TX0-
 LCD_TXOUT1+_R = EDP_TX1+
 LCD_TXOUT1-_R = EDP_TX1-
 LVDS_CLK = EDP_AUXP
 LVDS_DATA = EDP_AUXN



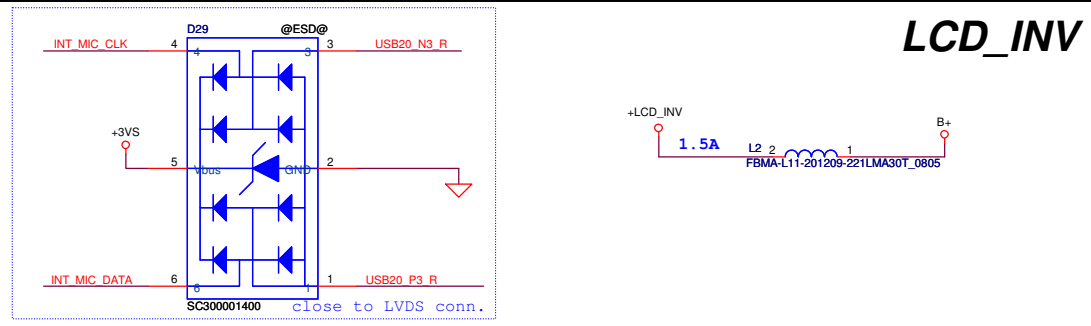
pin1-4 Touch function for panel
 pin5-10 For Webcam with single or dual MIC
 pin11-30 For LVDS or EPD panel

LCD_VDD

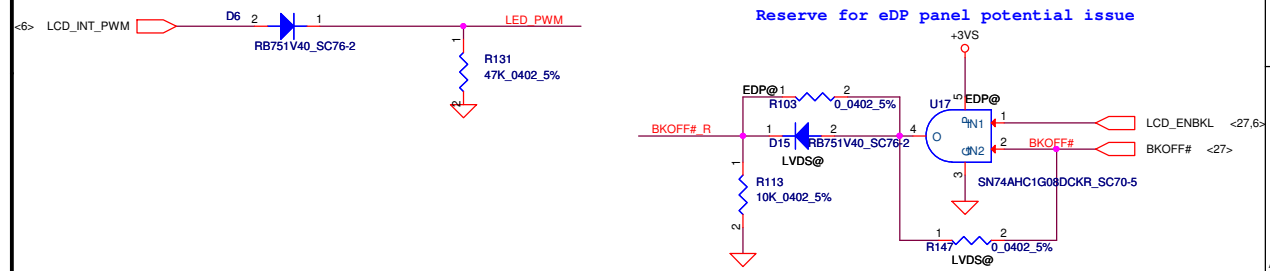
Need check eDP&LVDS both 3V power rail.



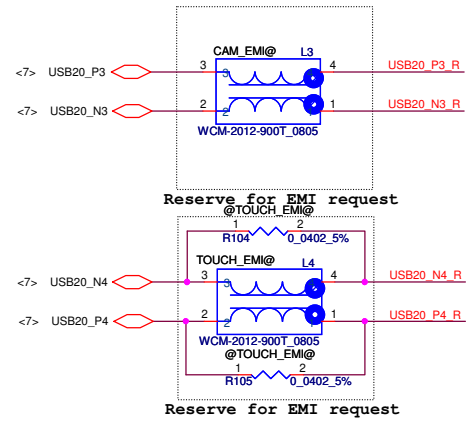
LCD_INV



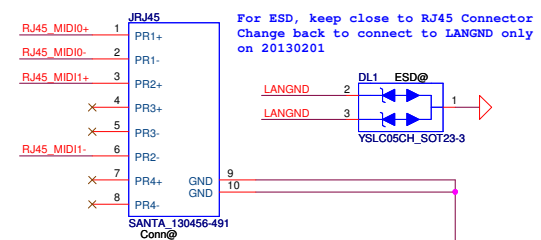
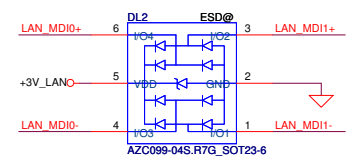
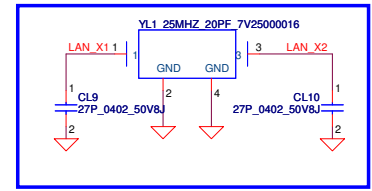
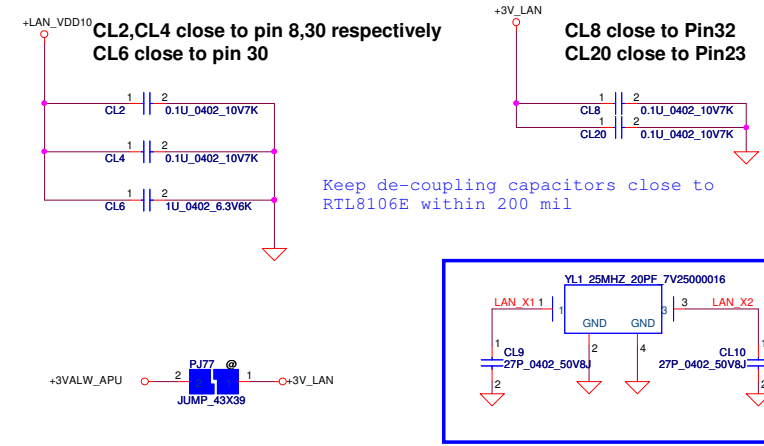
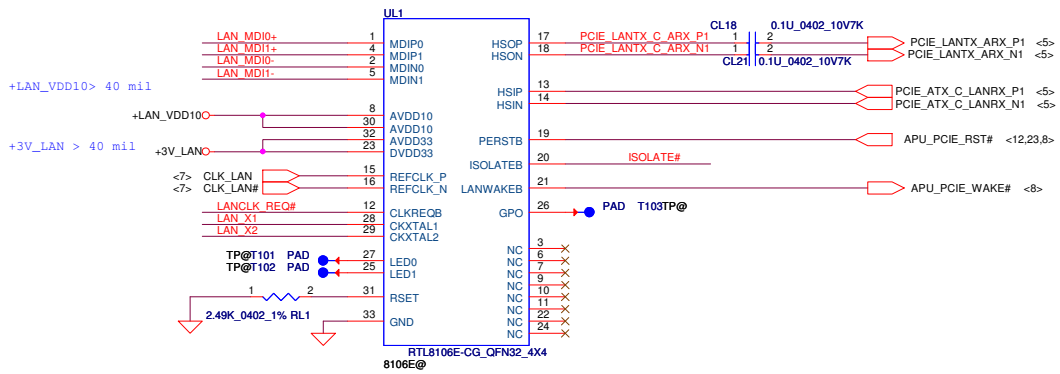
LCD Control



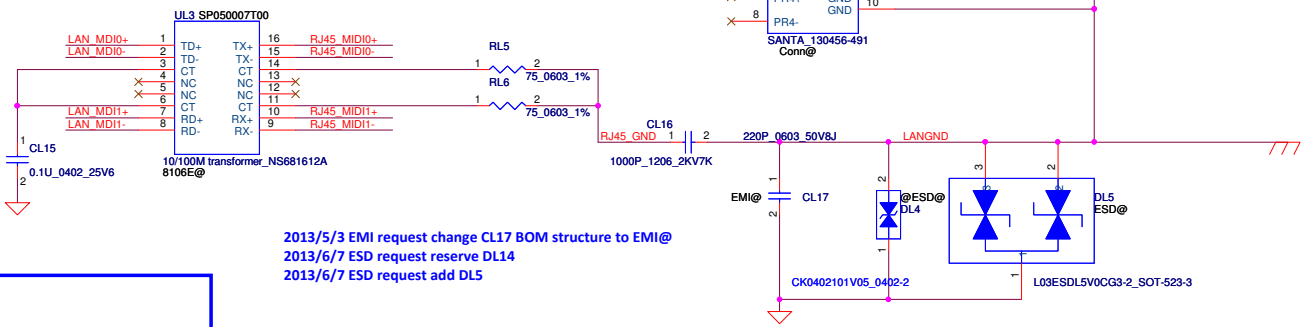
Camera & Touch Screen



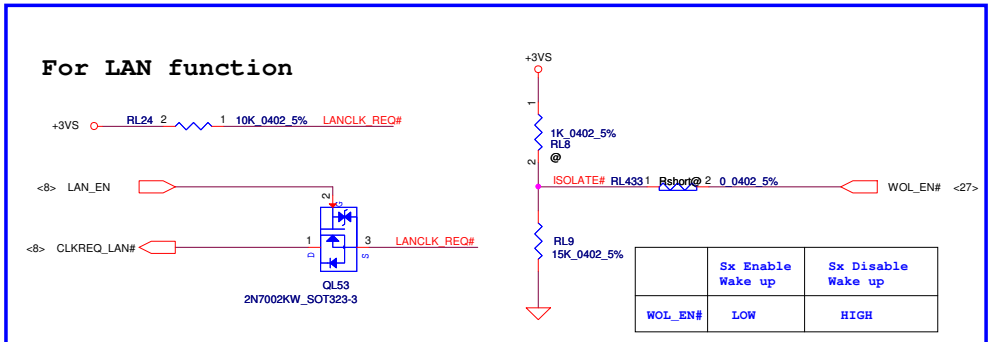
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title
				LVDS/EDP W/ CAMERA
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main: SP050007T00
 2nd: SP050007K00
 3nd: SP050006H00



2013/5/3 EMI request change CL17 BOM structure to EMI@
 2013/6/7 ESD request reserve DL14
 2013/6/7 ESD request add DL5



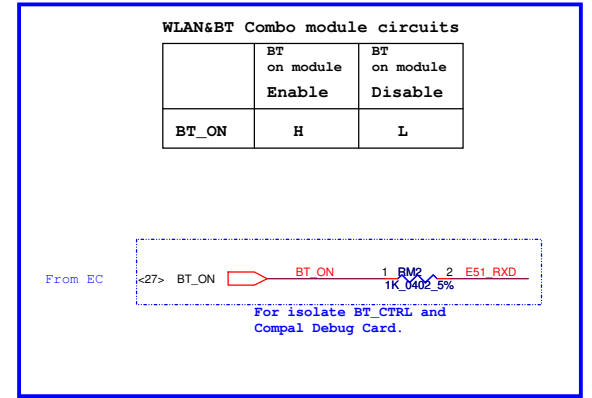
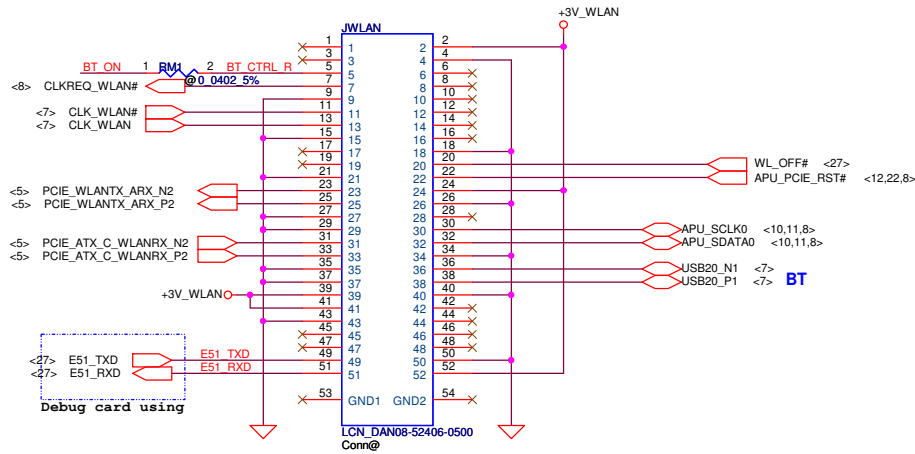
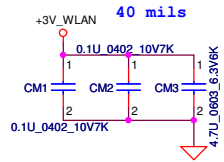
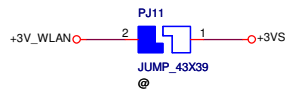
	Sx Enable	Sx Disable
WOL_EN#	LOW	HIGH

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

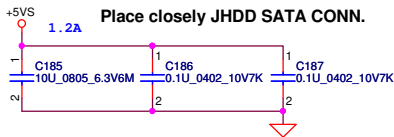
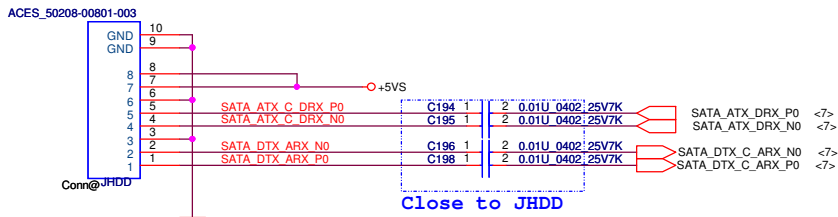
* S3: after SUSP# assert low over 100ms
 S4/S5: after SYSON assert low over 100ms

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

Slot 1 Half PCIe Mini Card-WLAN



SATA HDD Conn.



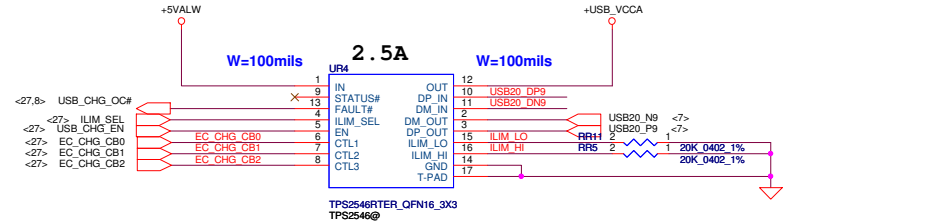
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title WLAN/SATA HDD&ODD		
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USB Sleep & Charge

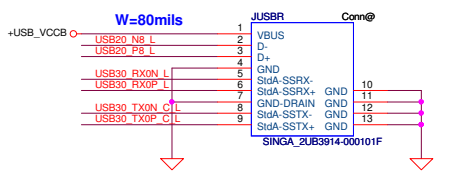
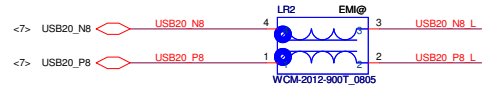
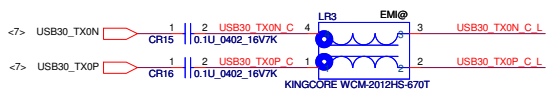
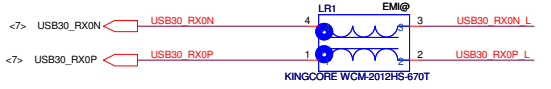
State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto/Alternate	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

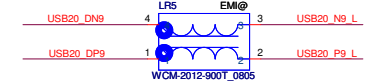
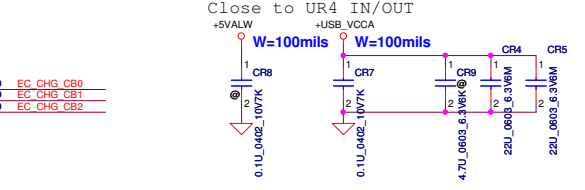
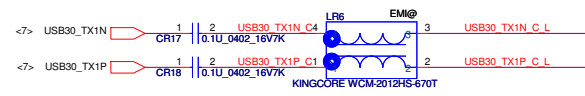
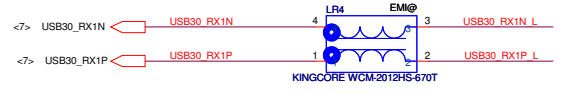
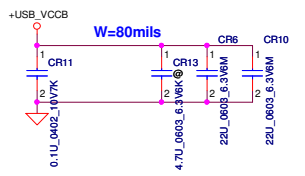
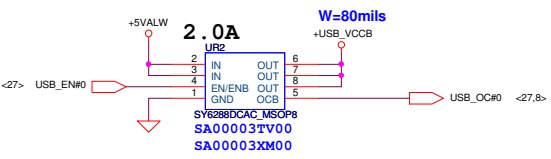
Right side USB 3.0 x 1 W/ Sleep&Charge



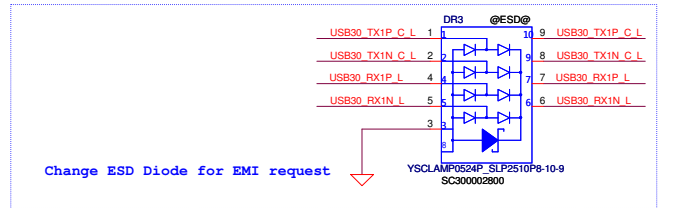
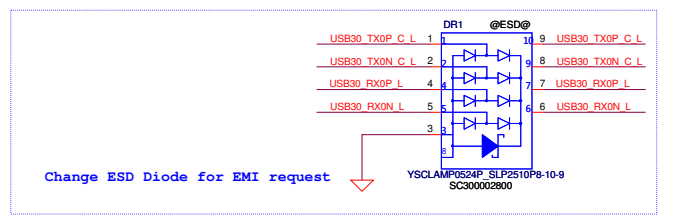
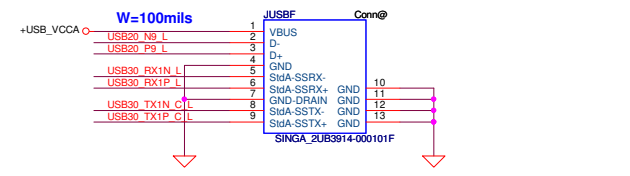
Right side USB 3.0 x 1



USB POWER SWITCH



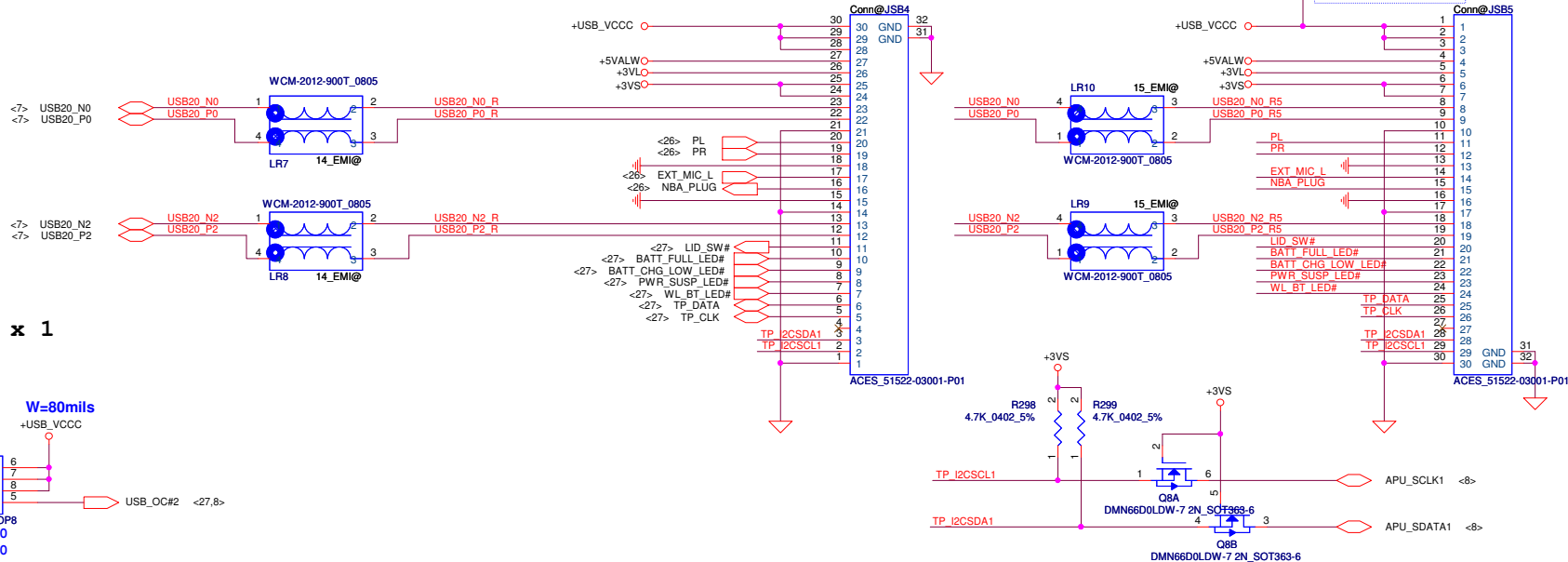
Sleep & Charge Port



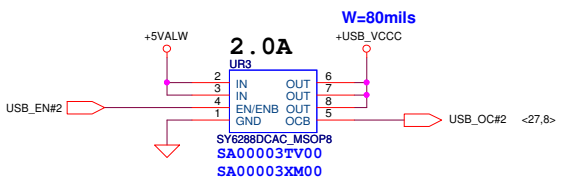
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title
				LSUB/RUSB/S&C
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Date:	Tuesday, July 16, 2013	Sheet	24	of 40

Small board Conn

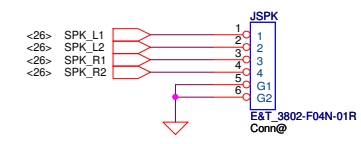
Close to JSB5



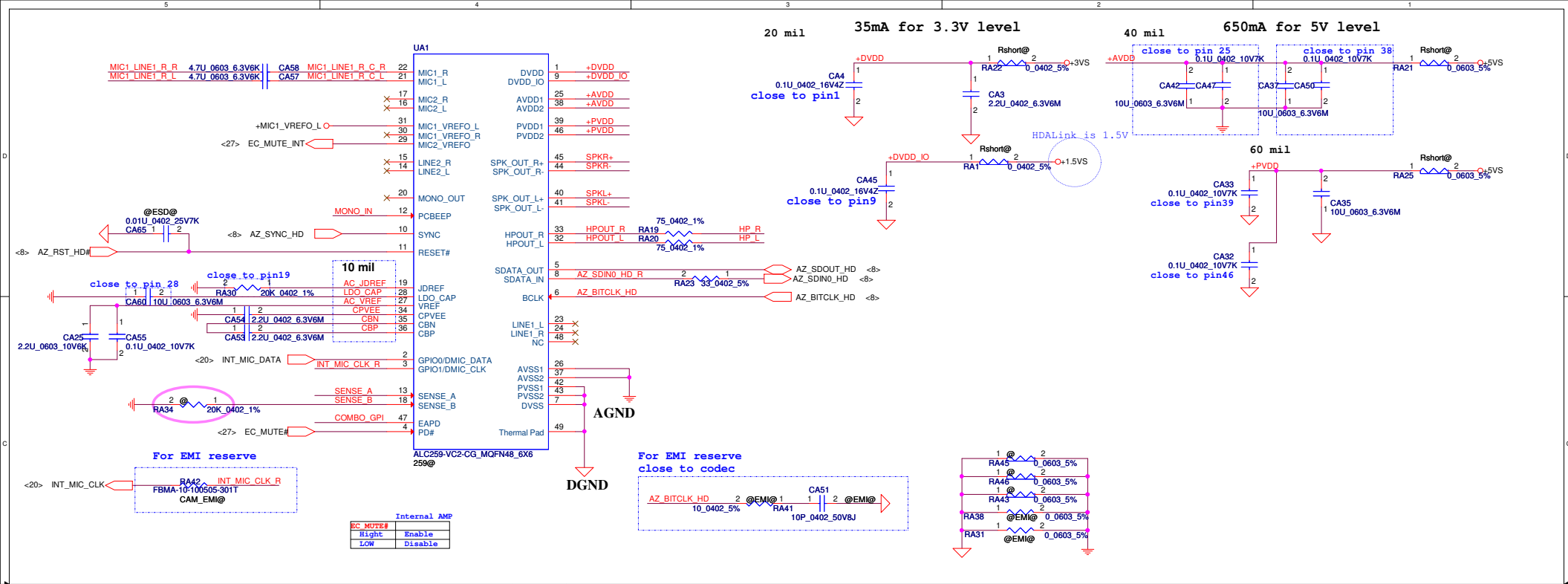
Left USB 2.0 x 1



SPK Conn.



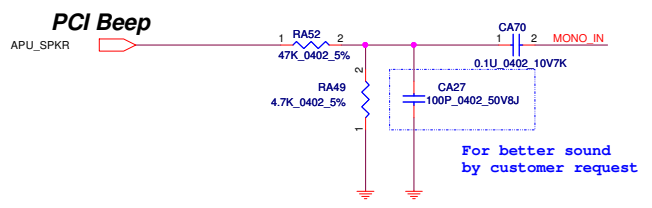
Security Classification	Compal Secret Data		Title	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Compal Electronics, Inc.
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Size	Custom	Document Number	LA-A551P	Rev
Date	Tuesday, July 16, 2013	Sheet	25	of 40



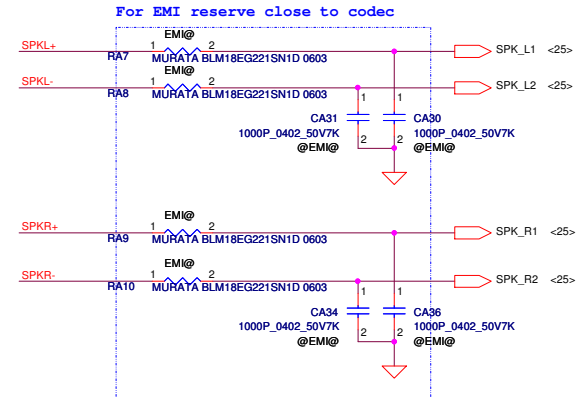
Internal AMP

EC_MUTE#	
High	Enable
Low	Disable

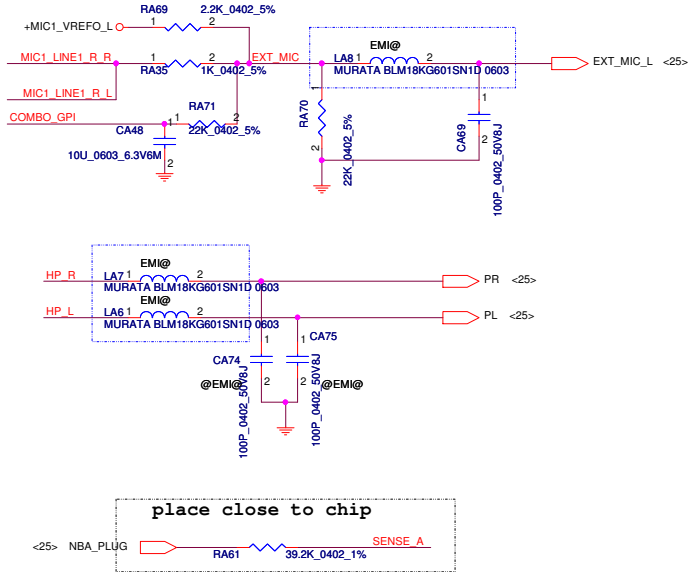
Beep sound



SPK 2W 4ohm =40mil 1W 8ohm =20mil

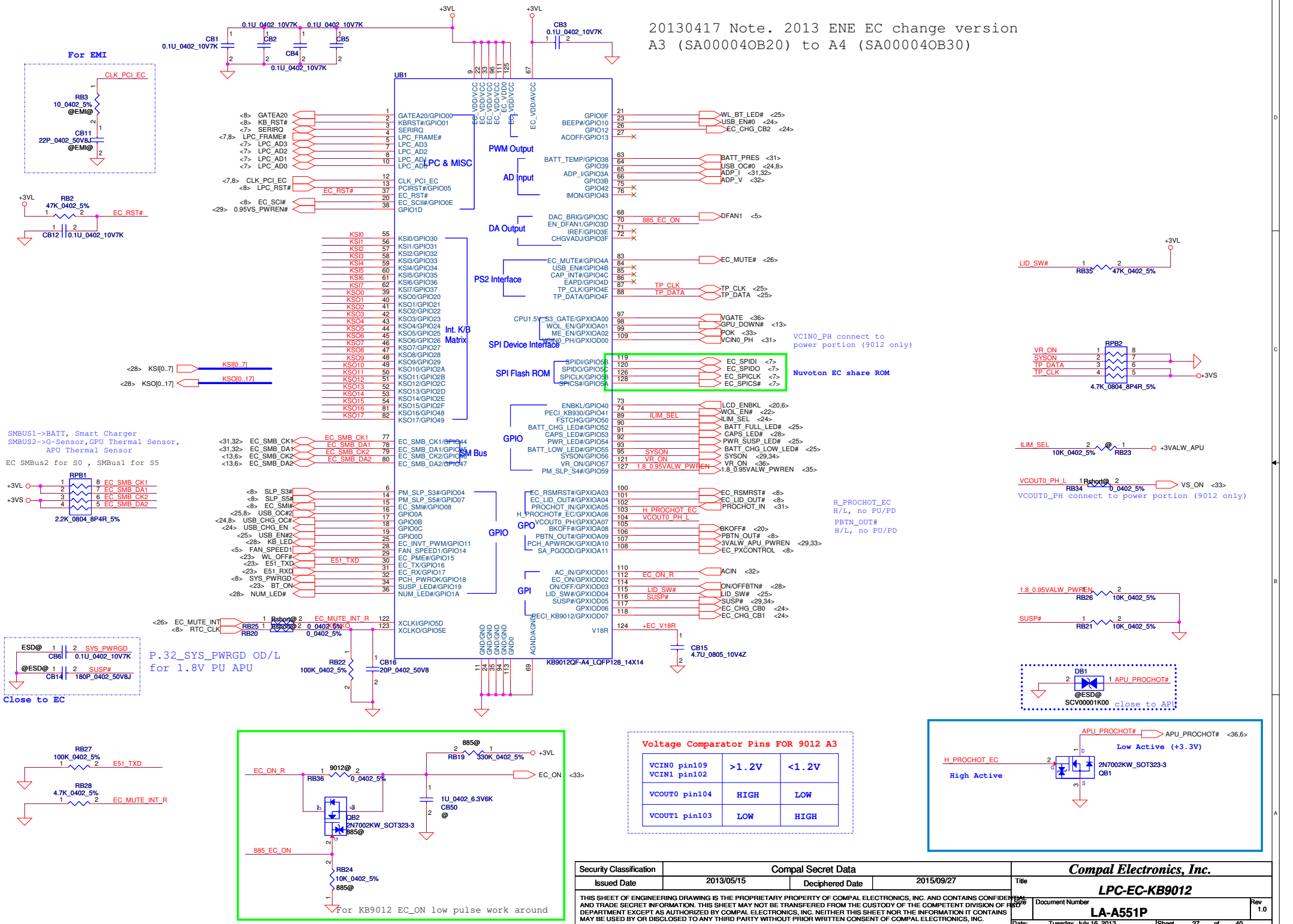


Combo Jack



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

20130417 Note. 2013 ENE EC change version A3 (SA000040B20) to A4 (SA000040B30)

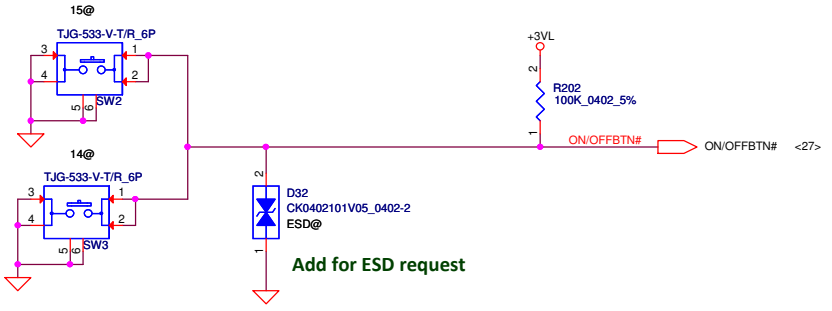


Security Classification	Compal Secret Data	
Issued Date	2013/05/15	Deciphered Date
		2015/09/27

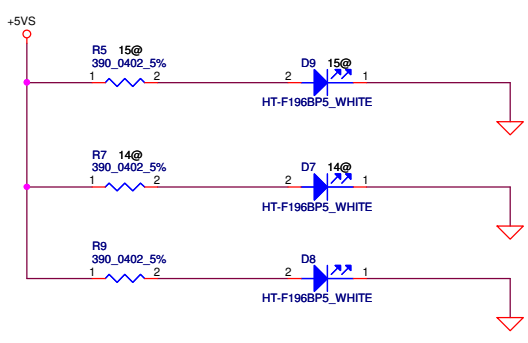
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Compal Electronics, Inc.	
LPC-EC-KB9012	
Document Number	Rev
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Date: Tuesday, July 16, 2013	Sheet 27 of 40

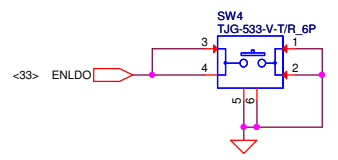
Power Button



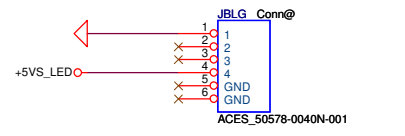
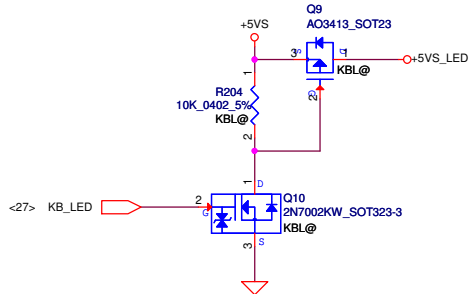
POWER LED



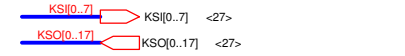
Battery Reset



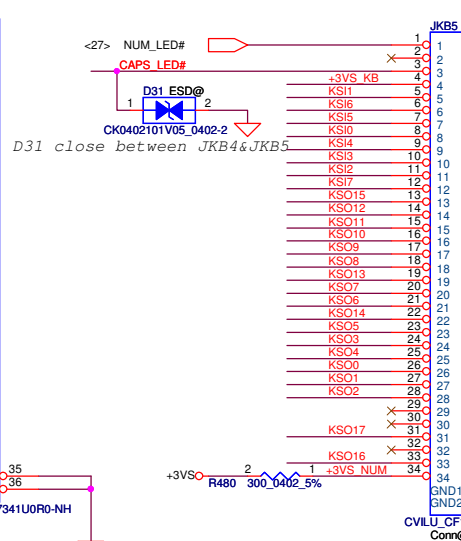
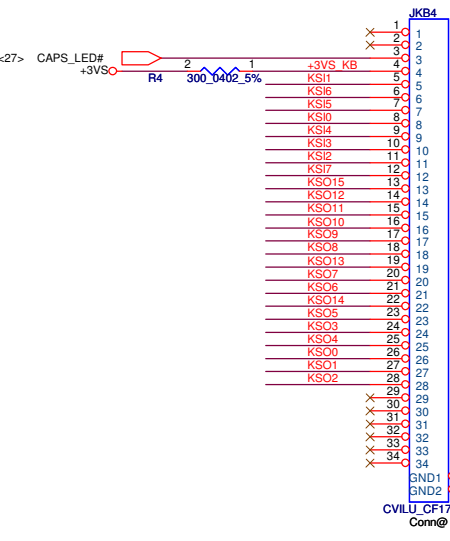
Keyboard LED



15" KEYBOARD CONN.

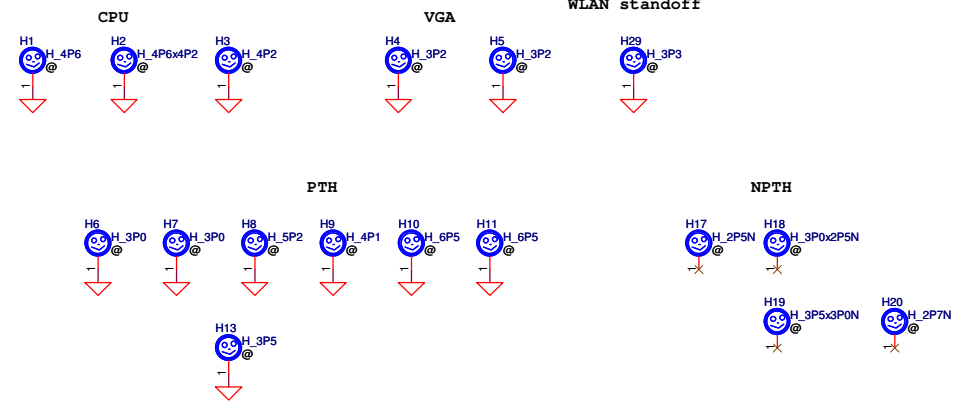


14" KEYBOARD CONN.

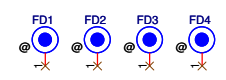


D31 close between JKB4&JKB5

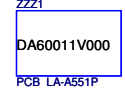
Screw Hole



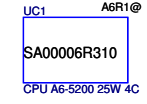
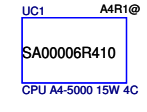
PCB Fedcal Mark PAD



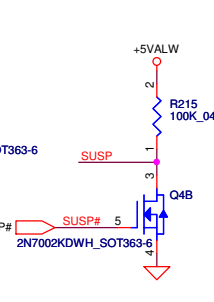
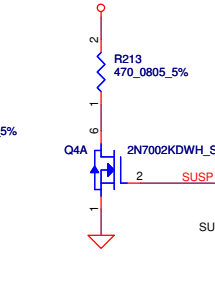
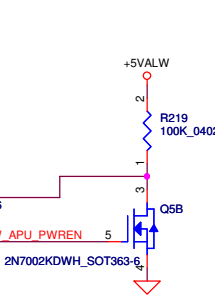
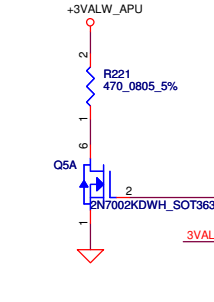
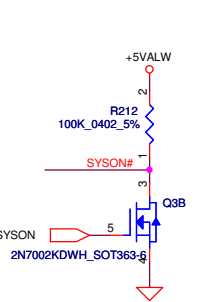
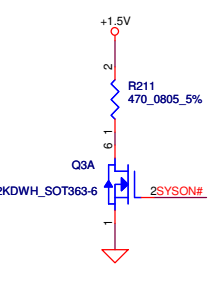
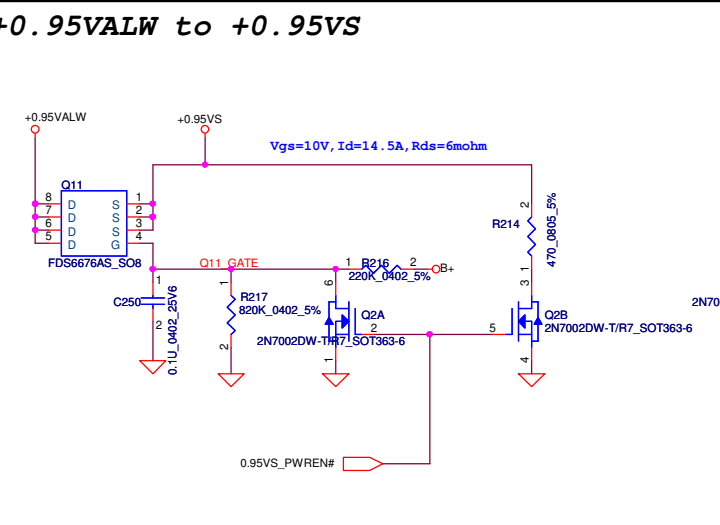
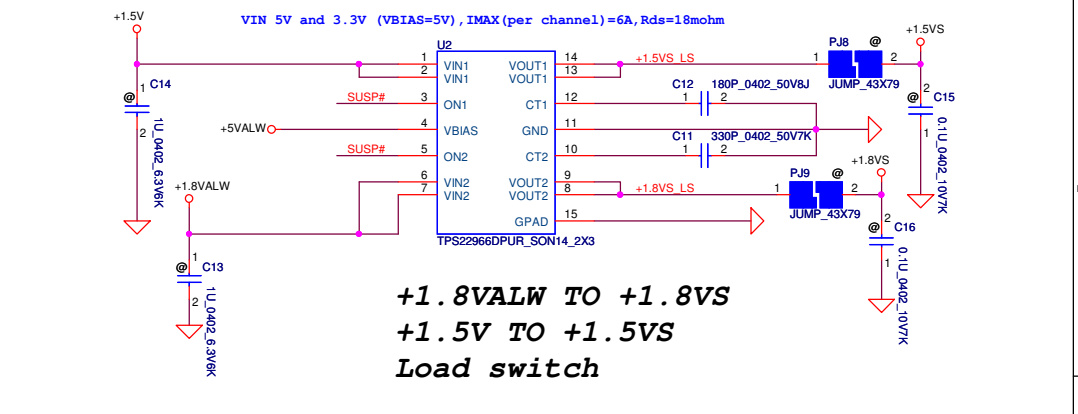
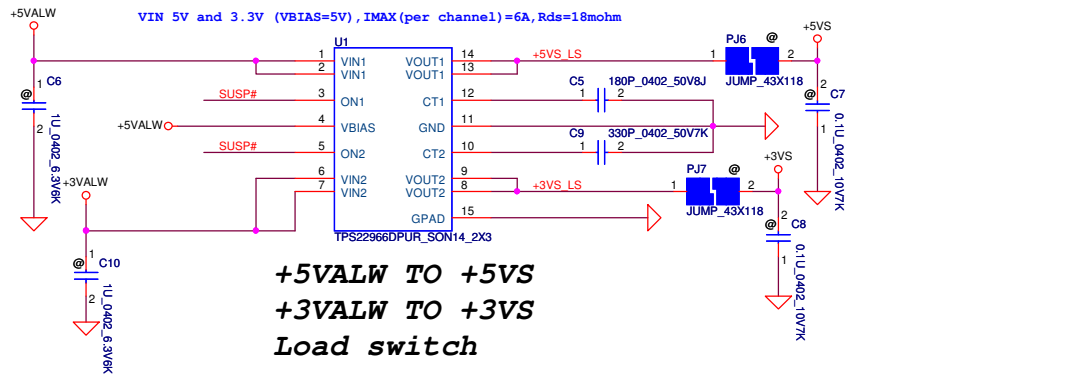
ISPD



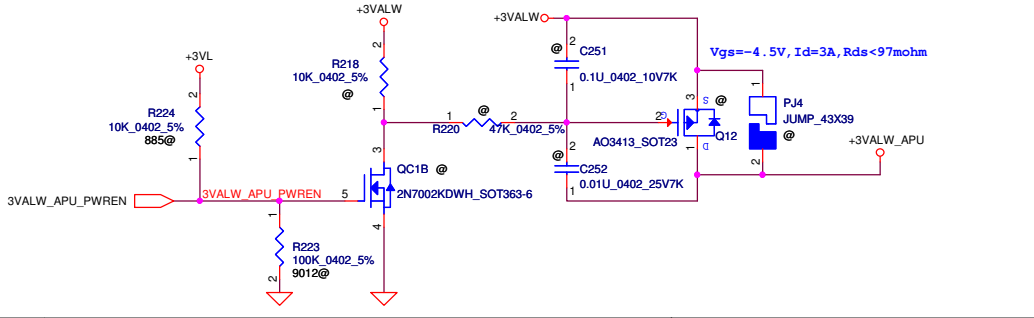
APU PR sample



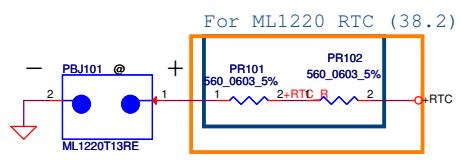
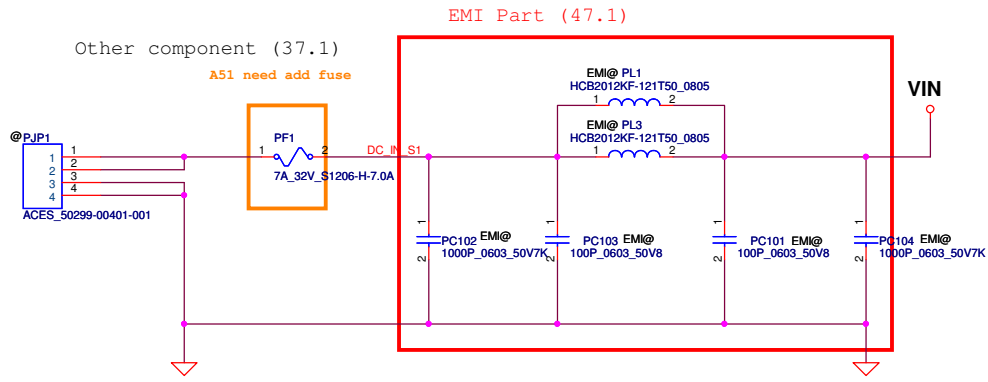
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title	
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				LA-A551P	
Date: Tuesday, July 16, 2013				Rev 1.0	
				Sheet 28 of 40	



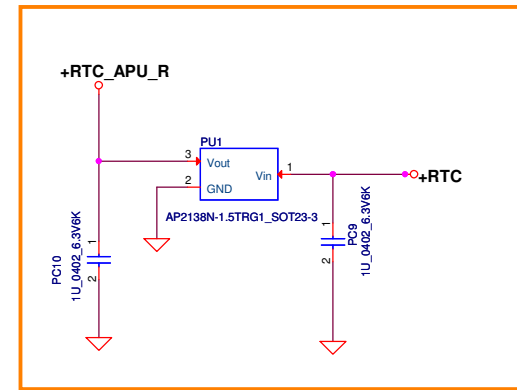
+3VALW to +3VALW_FCH



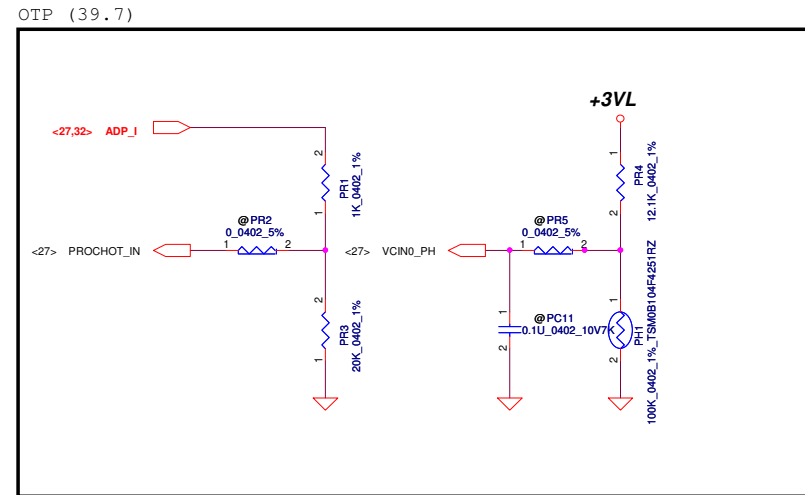
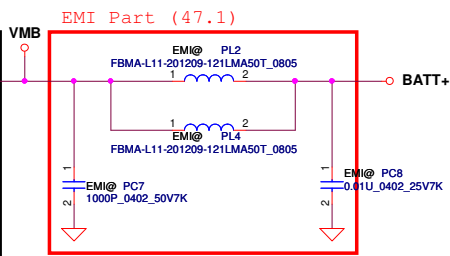
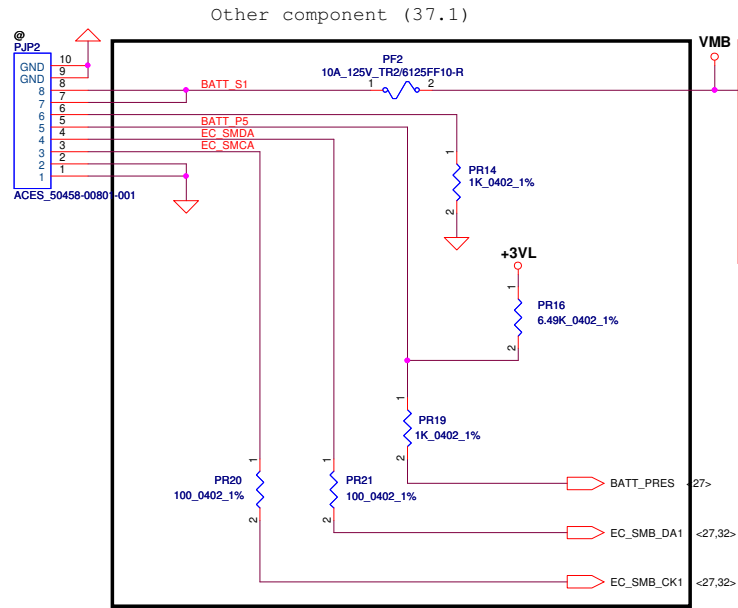
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title	DC TO DC INTERFACE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Document Number	Date		Sheet	Rev
	LA-A551P	Tuesday, July 16, 2013		29	1.0



For RTC (38.2)



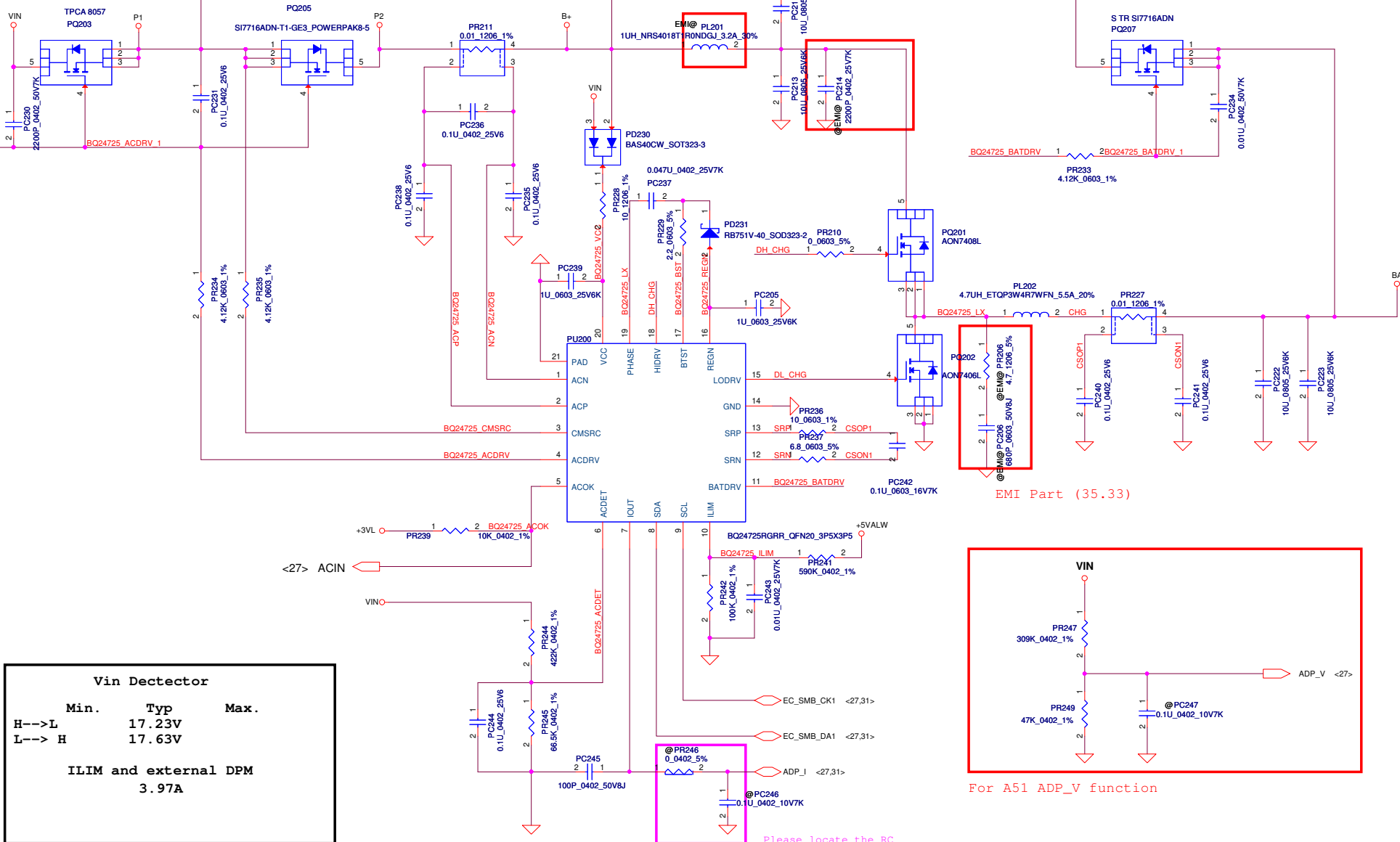
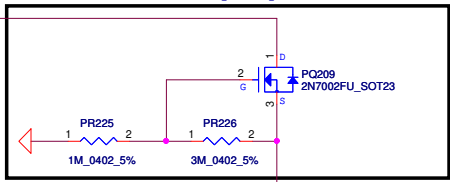
Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	DCIN/PRECHARGE
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Document Number Custom LA-A551P
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Issued Date	2012/09/27	Deciphered Date	2015/09/27	Compal Electronics, Inc.	
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				Custom	0.1
				Date:	Sheet 31 of 40
				Document Number LA-A551P	

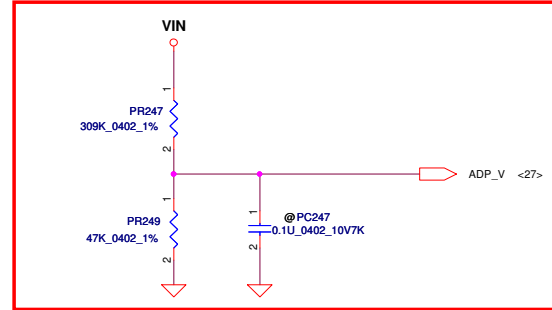
for reverse input protection

Charger controller (40.1), Support component (40.2)



Vin Dectector		
Min.	Typ	Max.
H-->L	17.23V	
L-->H	17.63V	
ILIM and external DPM		
3.97A		

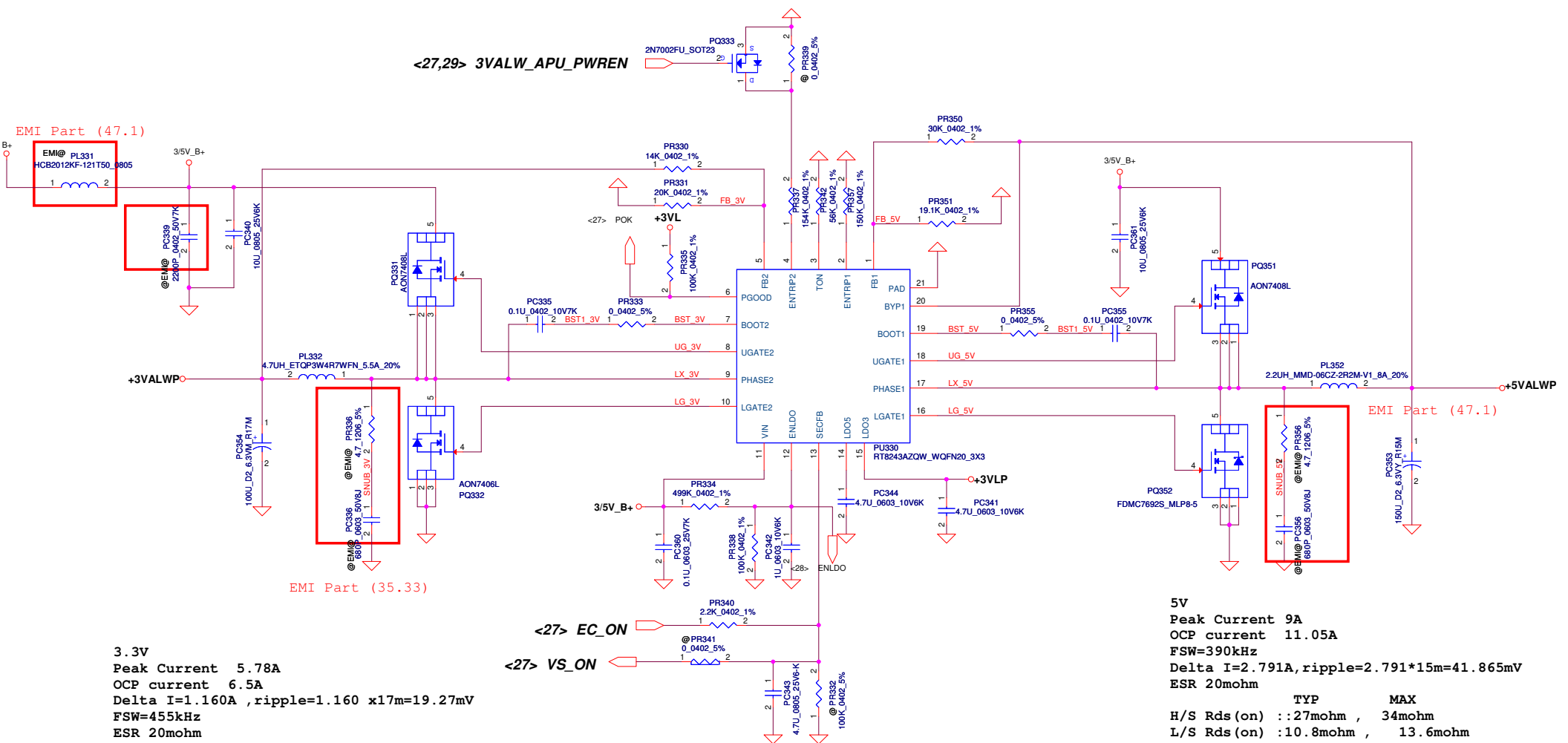
Please locate the RC Near EC chip 2011-02-22



For A51 ADP_V function

Security Classification		Compal Secret Data		Title	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	CHARGER	
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Date:				Sheet	32 of 40

<27,29> 3VALW_APU_PWREN



EMI Part (47.1)
 EMI@ FL331
 HCB2012KF-121T50_0805

EMI Part (35.33)
 EMI@ PR336
 @EM@ PR336
 @EM@ PR336
 @EM@ PR336

EMI Part (47.1)
 EMI@ PR356
 @EM@ PR356
 @EM@ PR356
 @EM@ PR356

3.3V
 Peak Current 5.78A
 OCP current 6.5A
 Delta I=1.160A , ripple=1.160 x17m=19.27mV
 FSW=455kHz
 ESR 20mohm

TYP MAX
 H/S Rds (on) : 27mohm , 34mohm
 L/S Rds (on) : 19mohm , 23.5mohm

<27> EC_ON
 <27> VS_ON

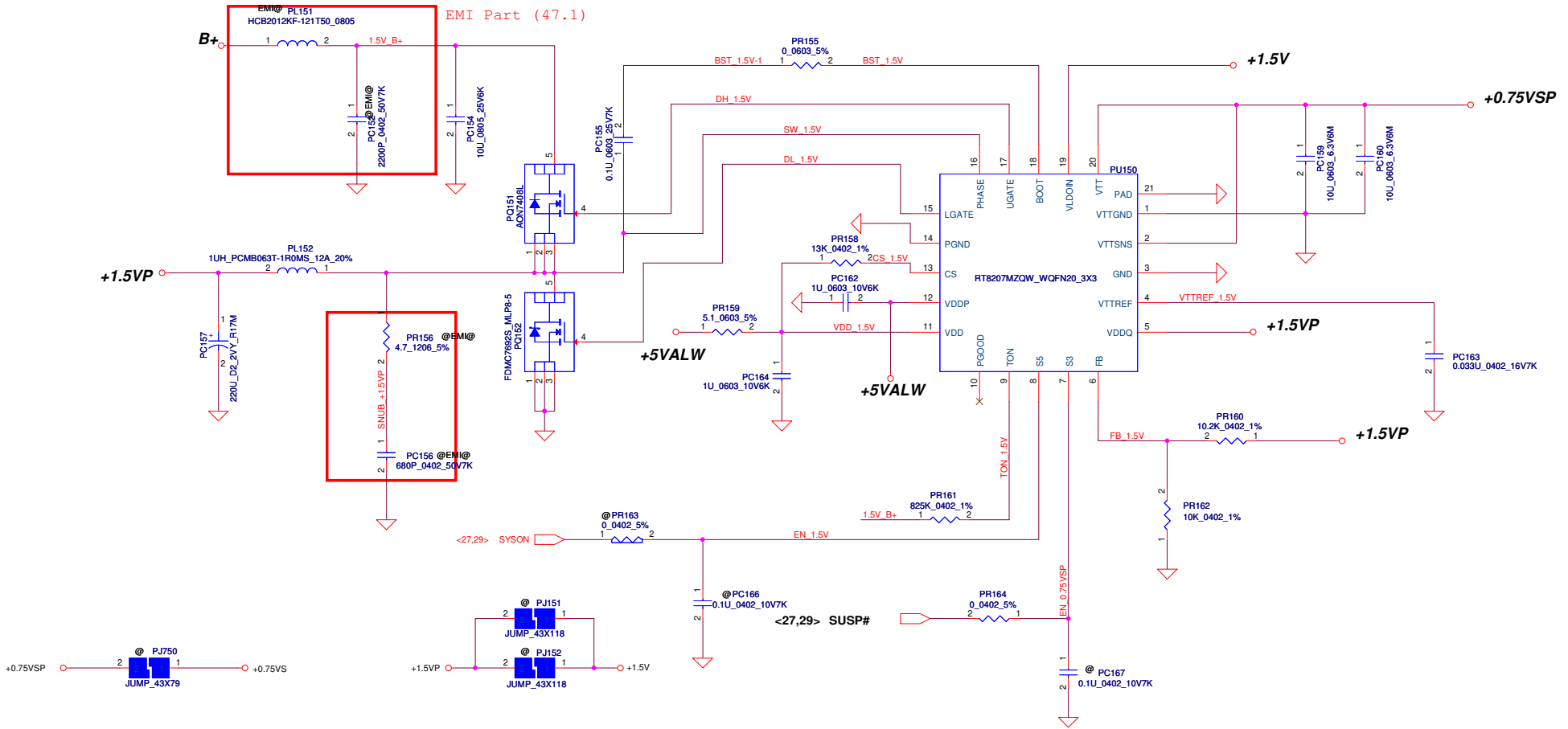
5V
 Peak Current 9A
 OCP current 11.05A
 FSW=390kHz
 Delta I=2.791A, ripple=2.791*15m=41.865mV
 ESR 20mohm

TYP MAX
 H/S Rds (on) : 27mohm , 34mohm
 L/S Rds (on) : 10.8mohm , 13.6mohm



Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	3VALW/5VALW	
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				Sheet	33 of 40

DDR controller (35.3), Support component (35.4)



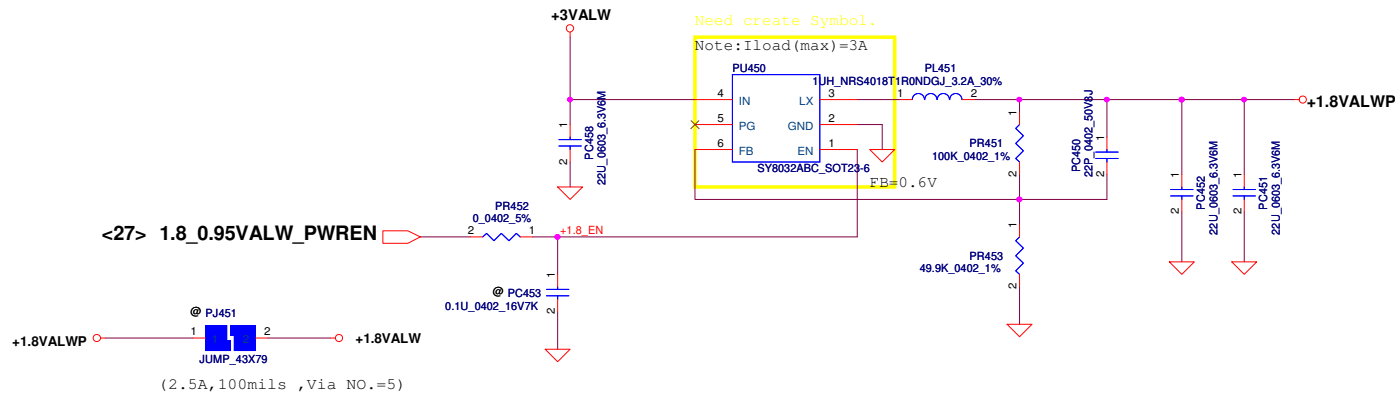
1.5V
 Peak Current 8.1A
 OCP current 9.63A
 FSW=500kHz
 DCR 8.3 ~ 10mohm
 TYP MAX
 H/S Rds (on) :27mohm , 34mohm
 L/S Rds (on) :10.8mohm , 13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Compal Electronics, Inc.	
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				Custom	LA-A551P
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				Sheet	34 of 40

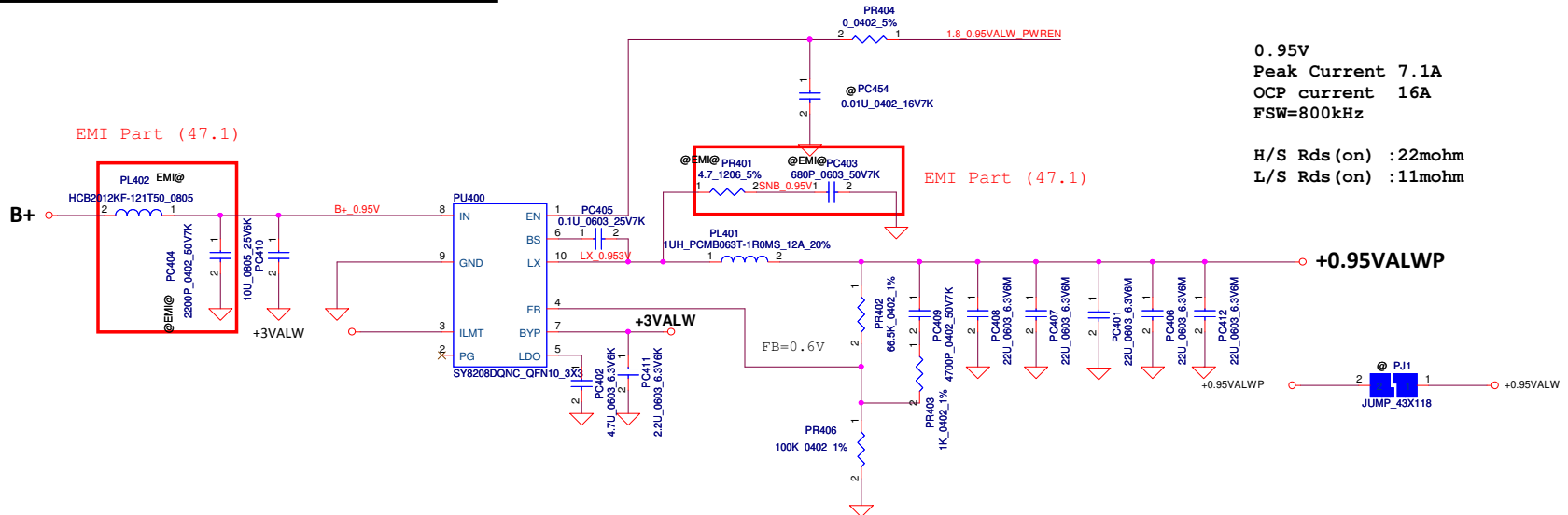
1.8V controller (35.15), Support component (35.16)



1.8V
Peak Current 2.5A
OCP current 3.5A
FSW=800kHz

H/S Rds(on) :100mohm ,
L/S Rds(on) :80mohm ,

0.95V controller (35.27), Support component (35.28)



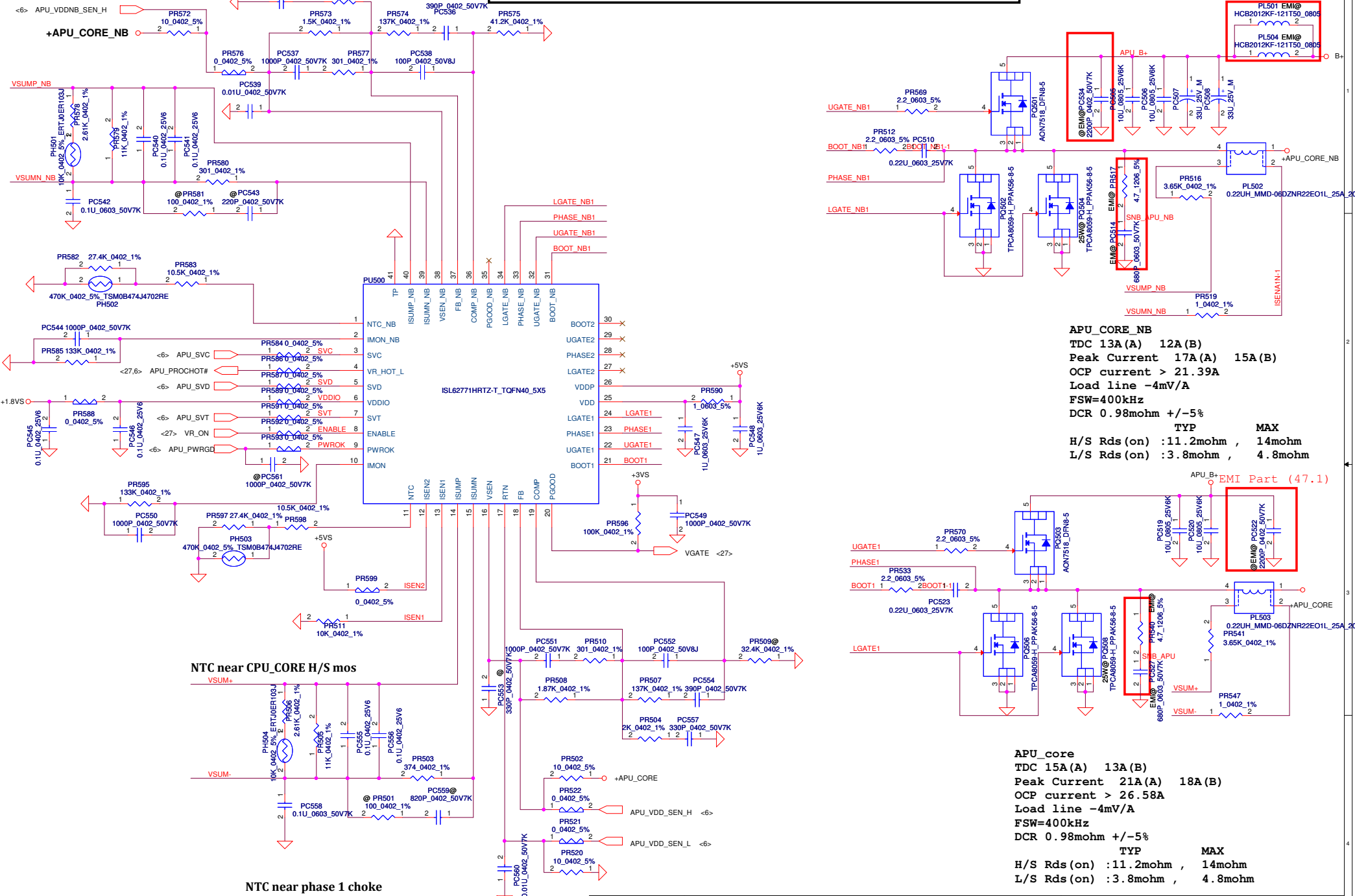
0.95V
Peak Current 7.1A
OCP current 16A
FSW=800kHz

H/S Rds(on) :22mohm
L/S Rds(on) :11mohm

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title		
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Size	Document Number	ZRM AE		Rev	0.1	
Date:	Tuesday, July 16, 2013	Sheet	35	of	40	

CPU controller (36.1), Driver (36.2) Support component (36.3)

EMI Part (47.1)



APU_CORE_NB
 TDC 13A(A) 12A(B)
 Peak Current > 17A(A) 15A(B)
 OCP current > 21.39A
 Load line -4mV/A
 FSW=400kHz
 DCR 0.98mohm +/-5%

TYP MAX
 H/S Rds(on) : 11.2mohm , 14mohm
 L/S Rds(on) : 3.8mohm , 4.8mohm

APU_core
 TDC 15A(A) 13A(B)
 Peak Current 21A(A) 18A(B)
 OCP current > 26.58A
 Load line -4mV/A
 FSW=400kHz
 DCR 0.98mohm +/-5%

TYP MAX
 H/S Rds(on) : 11.2mohm , 14mohm
 L/S Rds(on) : 3.8mohm , 4.8mohm

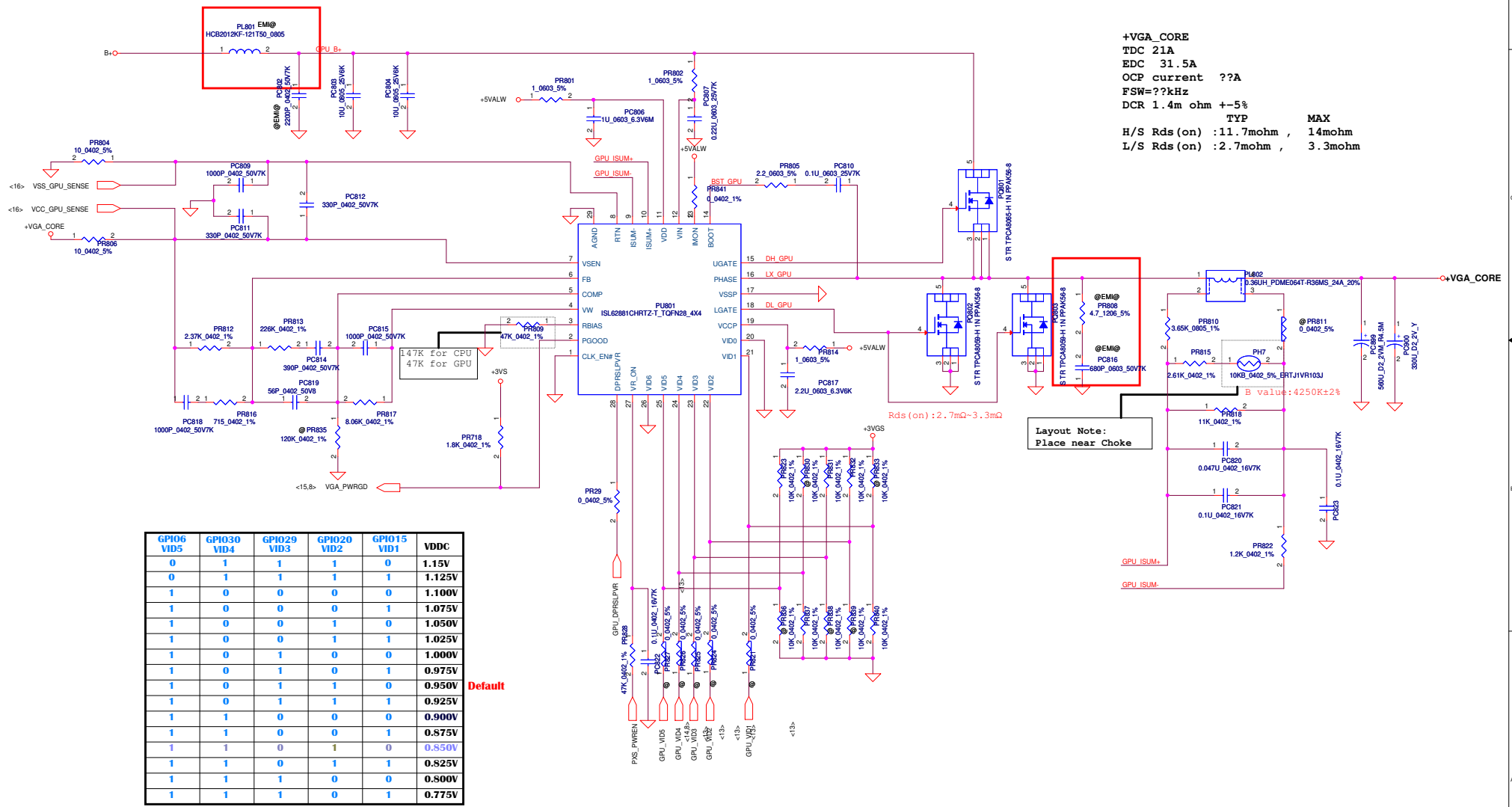
NTC near CPU_CORE H/S mos

NTC near phase 1 choke

Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/27	Deciphered Date	+CPU CORE/VDDNB	
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			Date: Tuesday, July 16, 2013	Sheet 36 of 40

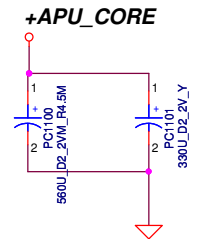
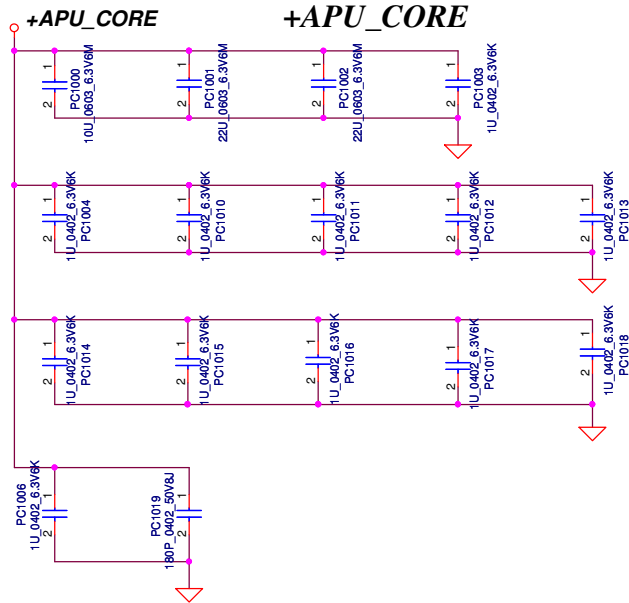
VGA controller (43.1), Driver (43.2) Support component (43.3)

EMI Part (47.1)

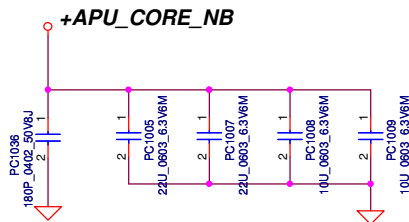


+VGA_CORE
TDC 21A
EDC 31.5A
OCP current ??A
FSW=?kHz
DCR 1.4m ohm +-5%
H/S Rds(on) :11.7mohm , 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

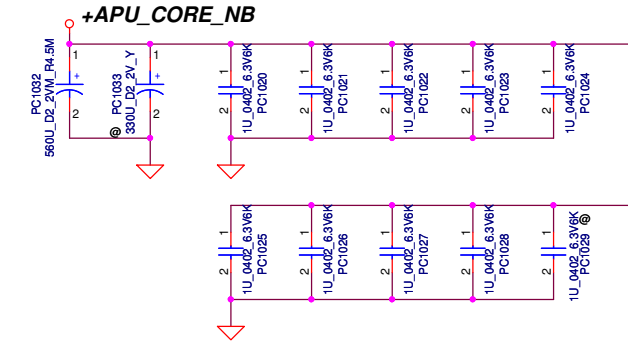
CPU_Core output CAP (Including MLCC) 36.4



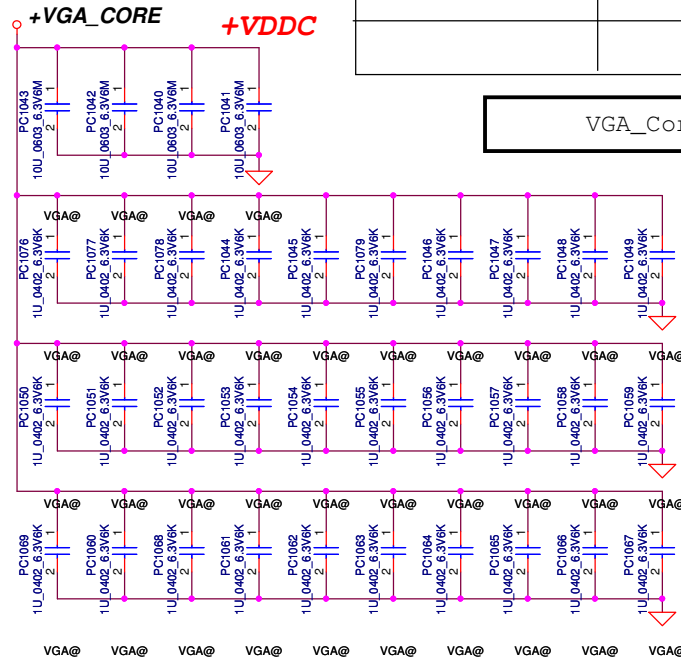
+APU_CORE_NB



GFX output CAP (Including MLCC) 36.5



+VGA_CORE



kABINI

	560uF*4.5m	330uF	22uF (0603)	10uF (0603)	1u (0402)	180P (0402)
VDD	1	1	2	1	12	1
VDD_NB	1		2	2	9	1

VGA_Core output CAP (Including MLCC 43.9)

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			Sheet 38	of 40

Item Reason for change PG# Modify List Date Phase

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	for design change
1	DVT--2013/05/03	P32-PWR-CHARGER	PR248/Remove 10K	PWR	double count for parts
2	DVT--2013/05/03	P33-PWR-3VALW/5VALW	PR337 PR357/change to 107K 150K	PWR	For 3/5 V OCP Setting
3	DVT--2013/05/03	P34-PWR+1.5VP/0.75VSP	PR158/ change to 15K	PWR	For 1.5 V OCP Setting
4	DVT--2013/05/03	P34-PWR+1.5VP/0.75VSP	PC157 / change to 220U	PWR	for design change
5	DVT--2013/05/03	P34-PWR+1.5VP/0.75VSP	PL152 / change PN	PWR	Common with PL401(1UH)
6	DVT--2013/05/03	P35-PWR +1.8VALWP/+0.95VALWP	PR405 /Remove 10K	PWR	EC pull low 10k
7	DVT--2013/05/03	P36-PWR-CPU_CORE/VDDNB	PQ504 PQ508 / Remove TPCA8059	PWR	For 15W APU
8	DVT--2013/05/07	P38-PWR-PROCESSOR DECOUPLING	PC1044,PC1045,PC1046,PC1047,PC1048, PC1049,PC1050,PC1051,PC1052,PC1053, PC1054,PC1055,PC1056,PC1057,PC1058, PC1059,PC1060,PC1061,PC1062,PC1063, PC1064,PC1065,PC1066,PC1067,PC1068, PC1069, PC1076, PC1077,PC1078,PC1079	PWR	Remove VGA MLCC
9	DVT--2013/05/07	P38-PWR-PROCESSOR DECOUPLING	PC1040,PC1041,PC1042,PC1043	PWR	Remove VGA MLCC
10	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1006/add 1U	PWR	for APU Transient test
11	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1001,PC1002/change 22U	PWR	for APU Transient test
12	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1101/change 330U	PWR	for APU Transient test
13	PVT--2013/06/10	P35-PWR +1.8VALWP/+0.95VALWP	PC412/add 22U	PWR	for 0.95v Ripple
14	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC353 / change to 150U	PWR	for 3/5V design change
15	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC354 / change to 100U	PWR	for 3/5V design change
16	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC343/ add 4.7U	PWR	for 3/5V design change
17	PVT--2013/06/10	P36-PWR-CPU_CORE/VDDNB	PC540 PC555/ change to 0.1U	PWR	for APU Transient test
18	PVT--2013/06/17	P33-PWR-3VALW/5VALW	PR337/change to 154K	PWR	for 3V OCP Setting
19	PVT--2013/06/17	P36-PWR-CPU_CORE/VDDNB	PC538,PC552/ change to SE071101J80	PWR	SE068101K80 - X1 Code
20	PreMP--2013/07/15	P38-PWR-PROCESSOR DECOUPLING	PC1005 PC1007/change 22U	PWR	for APU_NB Transient test

HW PIR (Product Improve Record)

ZEMAE LA-A551P SCHEMATIC CHANGE

LIST

REVISION CHANGE: 0.1 to 0.2

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	05/29	P24.	Delete RR2,RR3,RR7,RR6,RR12,RE7 for USB trace.	Part conut reduce
2.	05/29	P24.	Change CR13 to 0603.	HW4 Common design
3.	05/29	P24.	Delete SLP_CHG_CB0 & SLLP_CHG_CB1 from APU.	Reduce reserve
4.	05/29	P24,27,28.	EC_CHG_CB2(GPIO1A) move to GPIO12 \ ADD NUM_LED#(JKB5.1 to JUB1.36)	Design change
5.	05/30	P08.	Add QC2 and connect HDMI_HDP_N to HDMI_HDP.	For HDMI utility
6.	05/30	P08.	Delete T24,T25,T27	For RTC issue
7.	05/30	P08.	Add RC3 15K pull down and reserve RC12,RC16,RC17 pull +3VALW_APU and RC5,RC11 pull gnd.	For RTC issue
8.	06/03	P24.	Change CR3&CR2 47u 0805 to CR6&CR10 and CR4&CR5 22u 0603	For hight limit
9.	06/03	P10.	Change CD43 from 47u 0805 to CD43&CD44 22u*2 0603	For hight limit
10.	06/03	P09.	Change CC14 from 47u 0805 to CC14&CC16 22u*2 0603	For hight limit
11.	06/07	P22.	Reserve varistor DL14 for LANGND to DGND	For ESD request
12.	06/07	P22.	Add diode DL5 for LANGND to DGND	For ESD request
13.	06/07	P26.	Remove RA18 and RA24	Remove reserve 0 ohm
14.	06/07	P25.	Add C18 0.1uF 0402 on +USB_VCC close to JSB5	For EMI request
15.	06/10	P20.	Change C17 form 1500P to 0.015uF	For LCD sequence
16.	06/10	P25.	Remove 0ohm for 14 and 15 and add LR10 and LR9	For part count reduce
17.	06/11	P26.	Change LA7 and LA6 form 0402 to 0603 size	For EMI request
18.	06/11	P25.	Swap LR7/LR8 pin1&4 and pin3&2	For layout smooth
19.	06/11	P24.	Add test point for S&C IC T10&T11&T24	For NPI debug
20.	06/13	P28.	Change H4&H5 form H_3P3 to H_3P2	For ME limite
21.	06/14	P21.	Colay RY4,RY5,RY6,RY7,RY8,RY9,RY10,RY11 with HDMI chock	For EMI request

ZEMAE LA-A551P SCHEMATIC CHANGE

LIST

REVISION CHANGE: 0.2 to 1.0

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	07/05	A11	Change R2,R130,RC116,RC117,RC119,RC120,R106,RA22,RA25,RA1,RA21,LA8 to shortpad	MP Part reduce
2.	07/05	P28	Delete SW5	Remove debug part
3.	07/05	P29	Reserve QC1B	Remove non-used part
4.	07/05	P06	Add APU_CRT_R/G/B pull 75ohm to GND	For disable CRT
5.	07/05	P08	Change CC31 form 10P to 8PF	XTRAL PPM fine tune
6.	07/08	P28	Change H20 screw hole to 2.7mm from 2.8mm	ME change
7.	07/08	P08	Add RC11 15K pull GND	AMD request
8.	07/08	P26	Change LA8 shortpad form 0402 to 0603	EMI request
9.	07/11	P28	Change C24 100pF cap to D32 100p varistor	ESD request
10.	07/15	P24	Update PCB footprint	DFB request

Title		
HW PIR		
Size	Document Number	Rev
B	LA-A551P	1.0
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