

Compal Confidential

Model Name : Cheetah_CT

File Name : ZEJV4

BOM P/N:

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ZEJV4 LA-A411P Schematics Document

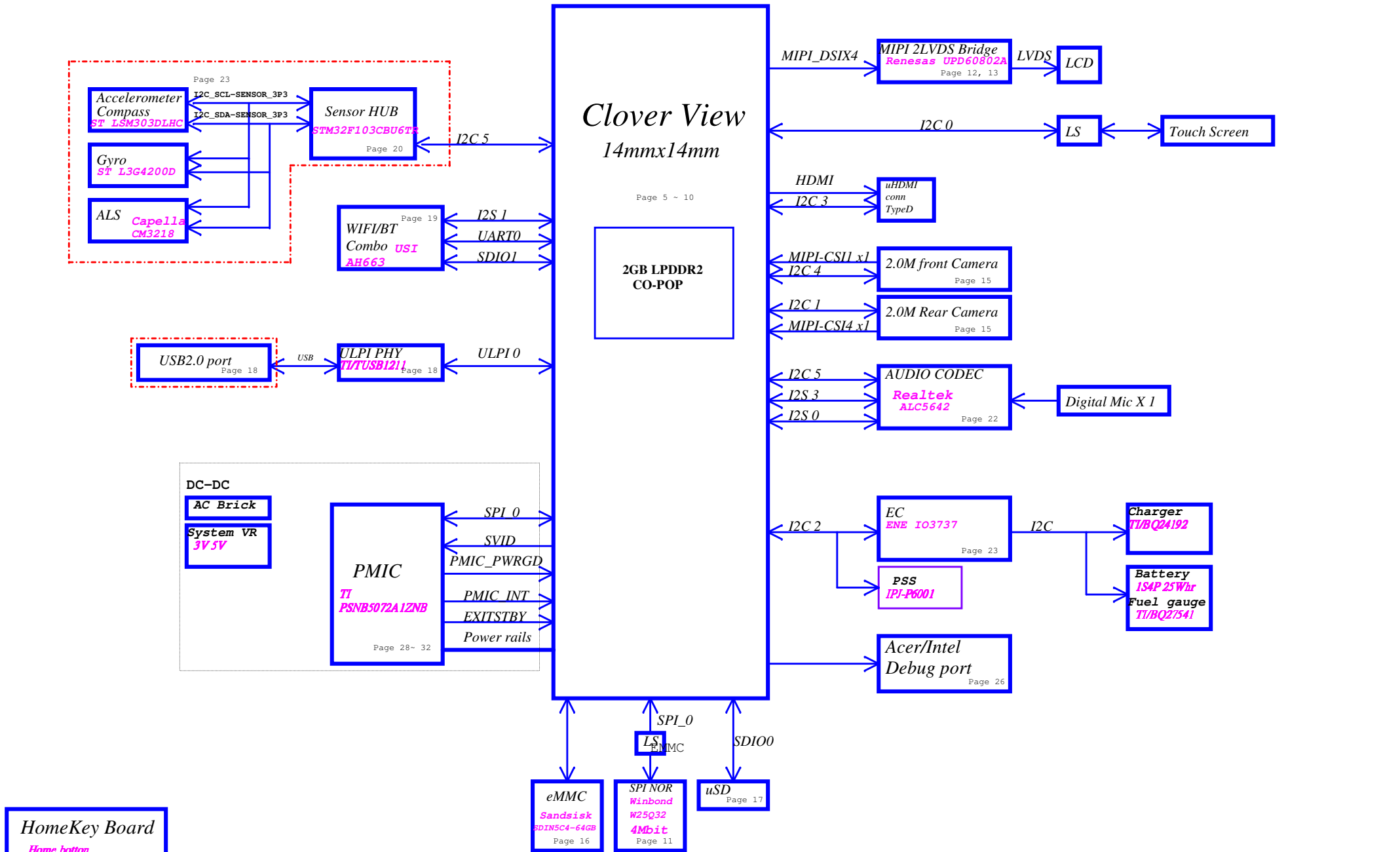
Intel Clover Trail

2013-04-15

REV: 1.0

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System Block Diagram



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Power rail

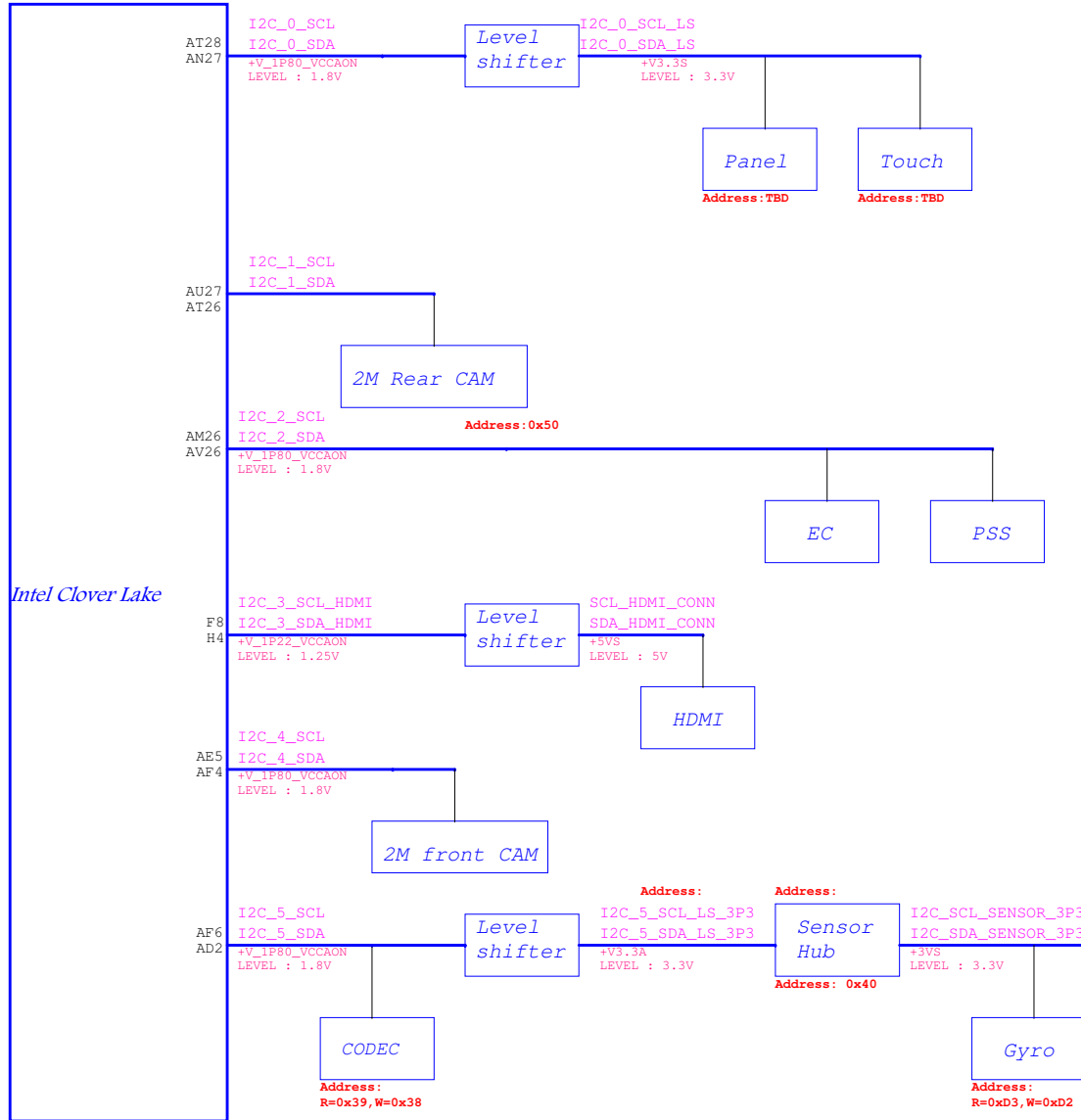
		Net name	Voltage	Comment
System		DC_IN	5V or 12V	adapter input
		+V_BATTERY	Max 4.2V	Battery input
		+VBATA	3.4V~4.2V	It's tablet's "B+"
		+V5A	5V	Should be 5VALW
		+V3_3A	3.3V	Should be 3VALW
		+V5S	5V	Should be 5VS
		+V3_3S	3.3V	Should be 3VS
PMIC	PMIC BUCK Converter	+V_VCC	0.3~1.2V	0.95V is default value
		+V_VNN	0.6~1.2V	0.95V is default value
		+V_VNNAON	0.6~1.2V	0.95V is default value
		+V_1P22_VCCAON	1.250V	1.25V is default value
		+V_1P80_AON	1.836V	1.836V is default value
		+V_1P08_VCCAON	1.08V	
		+V_1P08_VCCAS	1.08V	
		+V_1P08_VCC	1.08V	
		+V_1P00_VCCAS	1.025V	
		+V_1P00_VCCA	1.025V	
		+V_2P85_1P80_VCCSDIO	2.85V	2.85V is default value
		+V_2P80_VPROG1	1.2V	1.2V is default value
		+V_2P80_VPROG2	1.2V	1.2V is default value
		+V_2P85_EMMC1	2.85V	
		+V_2P85_EMMC2	2.85V	No routing
		+V_1P80_AON	1.8V	
		+V_1P80_VCCAON	1.8V	
		+V_1P80_VCC	1.8V	
		+V_3P30_VCC	3.3V	

IO MAP

Interface		Device
MIPI DSI		LVDS Bridger
MIPI CSI	X1	2M Camera
	X1	2M Camera
MIPI HSI		NC
LPC		NC
EMMC	0	EMMC
	1	NC
HDMI		HDMI Conn.
SDIO	0	Micro SD
	1	WIFI/BT
	2	NC
SVID		PMIC
SPI	0	FLASH ROM/PMIC/XDP
	1	XDP
	2	Test Point
	3	NC
ULPI	0	Internal USB
	1	POGO conn
UART	0	WIFI/BT
	1	NC
	2	XDP
I2S	0	Codec
	1	BT PCM
	2	NC
	3	Codec
I2C	0	LVDS / Panel / Touch screen
	1	2M rear camera
	2	Charger / Battery / PSS
	3	HDMI
	4	2M front camera
	5	Codec / Sensor Hub

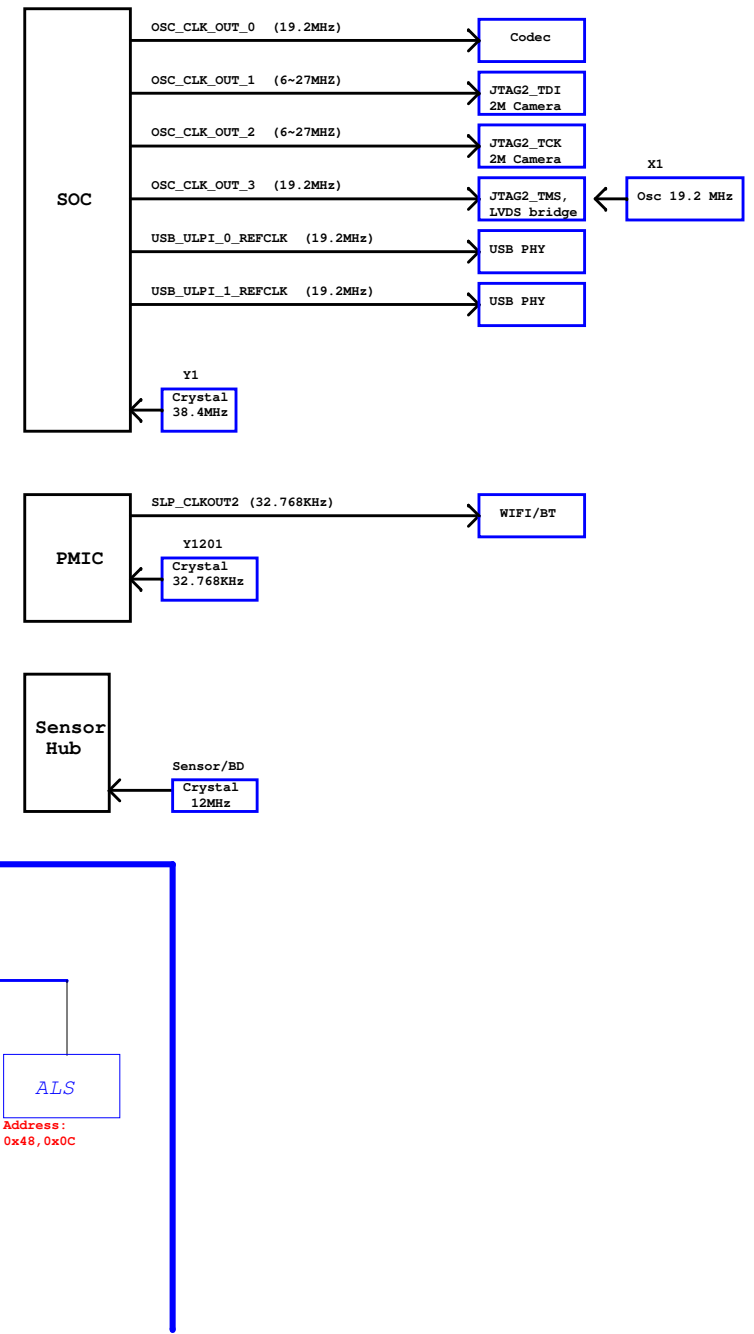
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I2C Routing



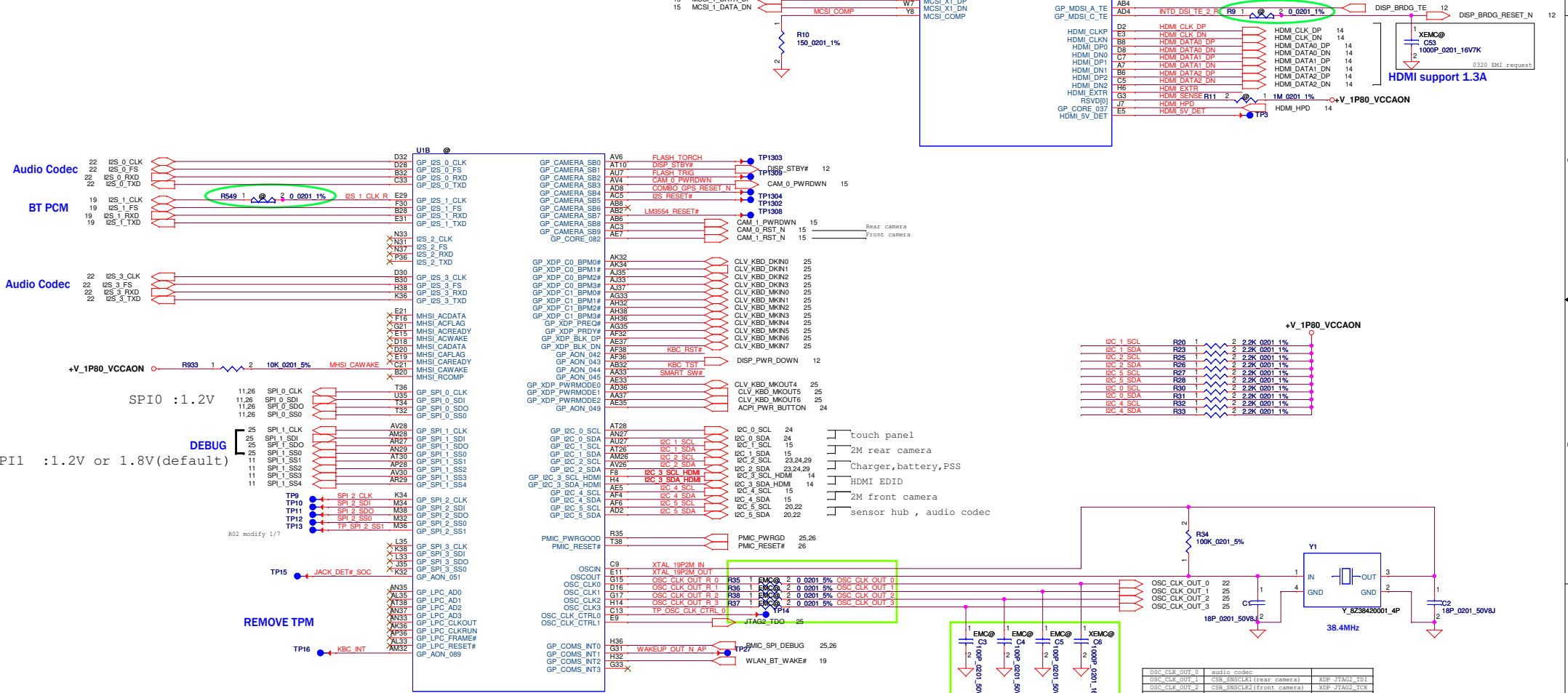
Clock Distribution

MB

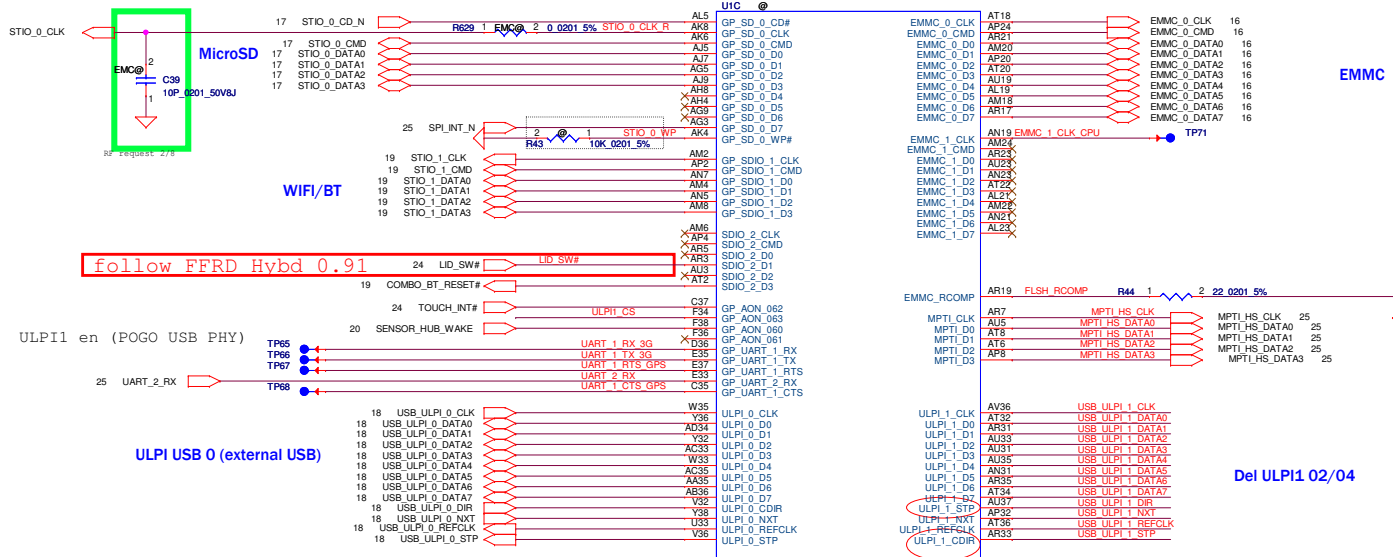


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 ZZZ PCB 10E LA-A411P REV0 M/B HDI DAA00075000	MB PCB P/N
 QC4K@ UI1 S IC A32 DG8065001202400 QC4K A0 1.5G SA00005HJ30	ES CPU P/N
 QD4T@ UI1 S IC DG8065001313500 QD4T C0 1.8G FCMB4 SA000061C60	QS CPU P/N

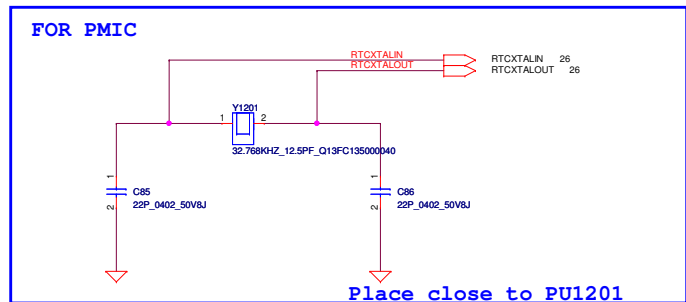


Must Disable internal pull-high for uSD interface !!

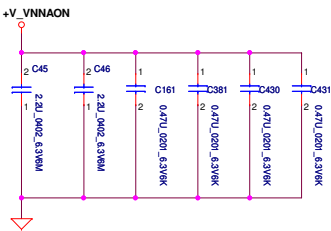
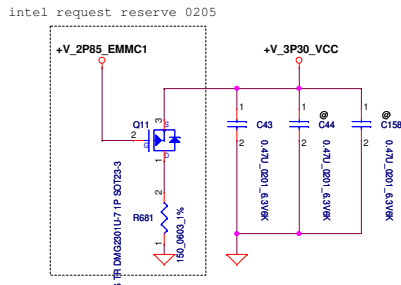
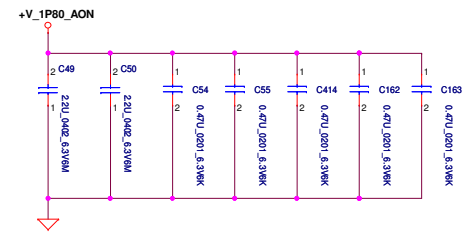
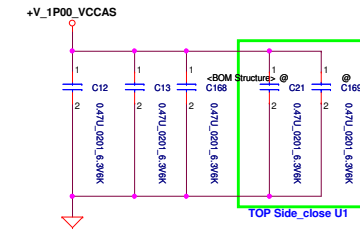
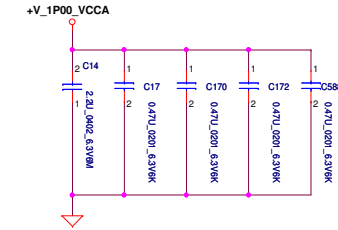
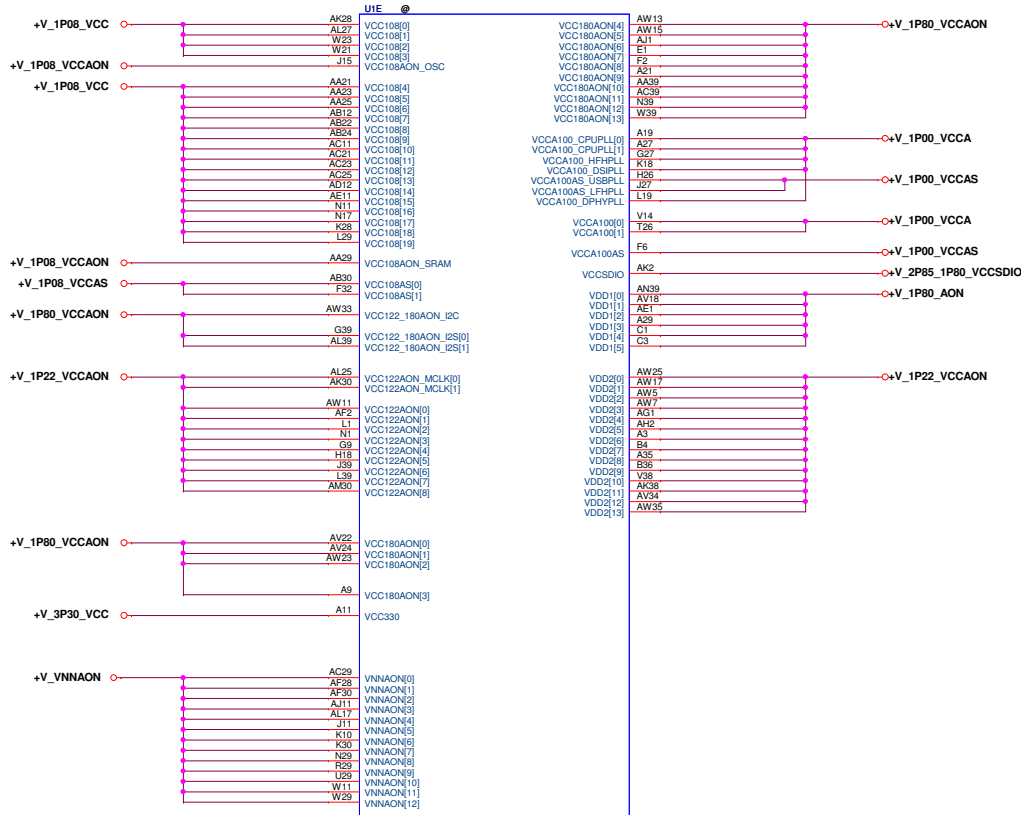
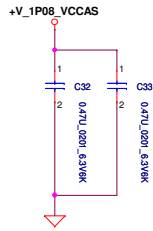
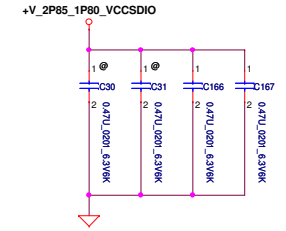
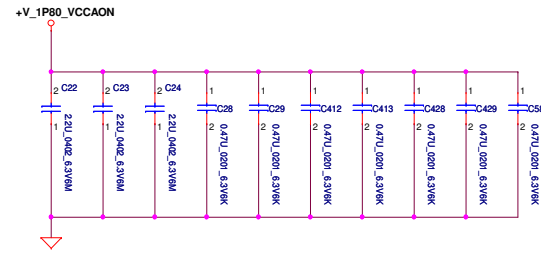
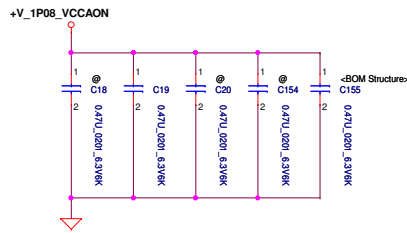
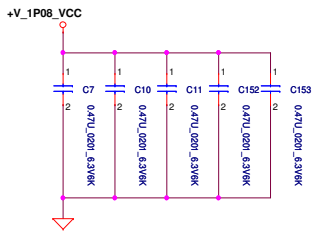


follow FFRD Hybd 0.91

Those two pins were labeled in error on the SoC and in the EDS
 The correct pinout is:
 ULPPI_1_DIR = AU37
 ULPPI_1_STP = AR33

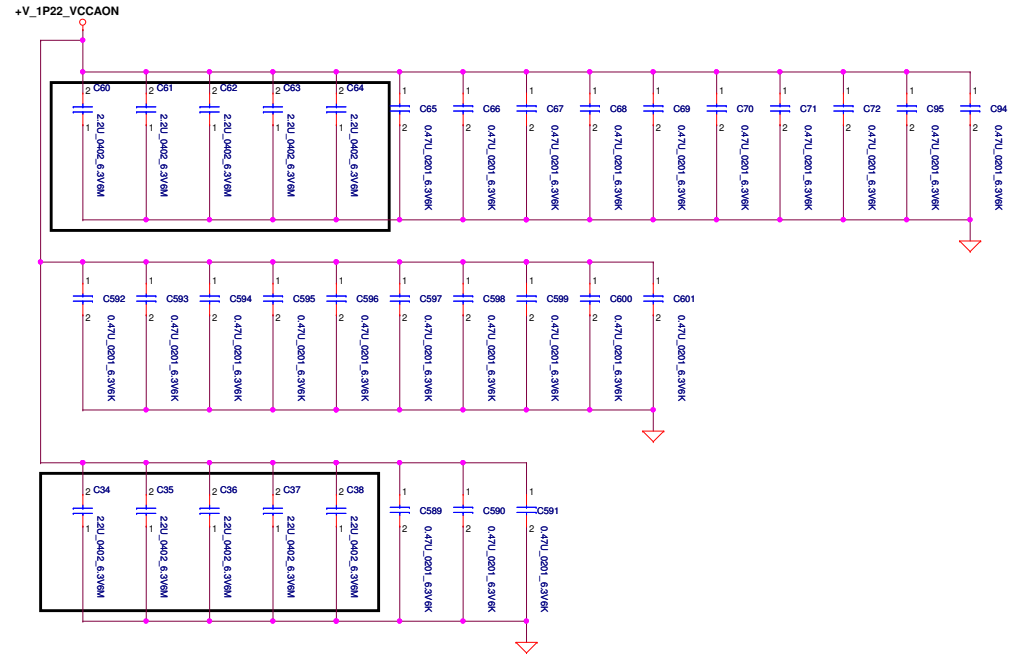
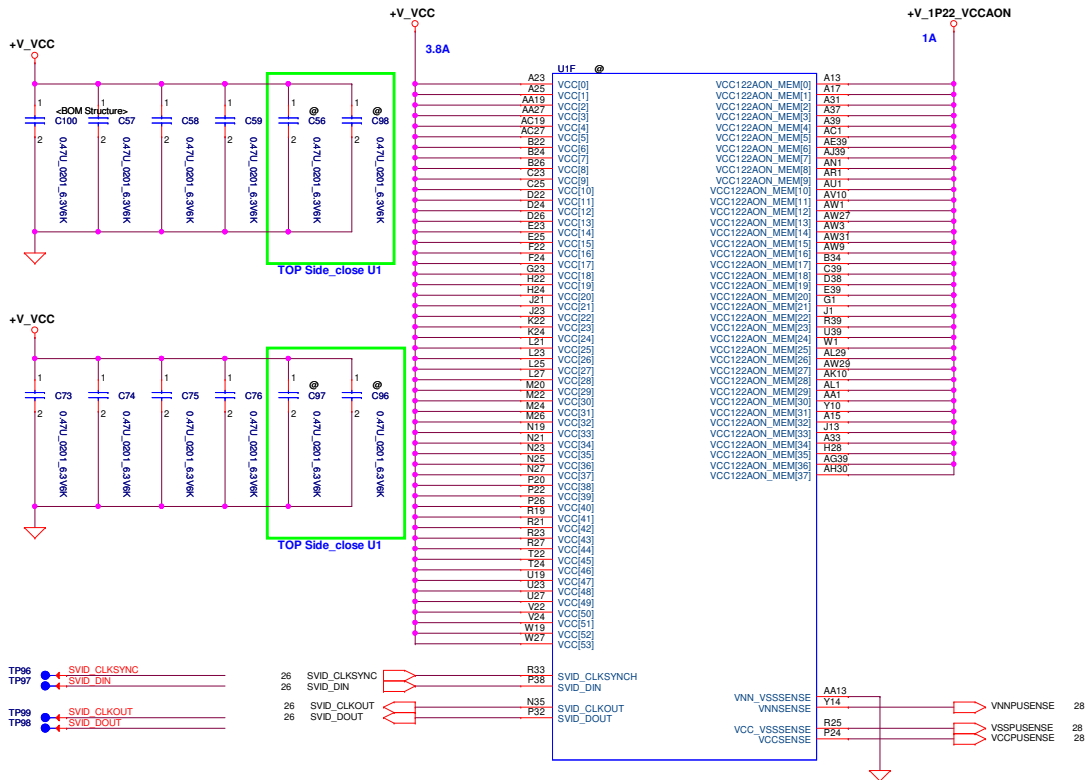


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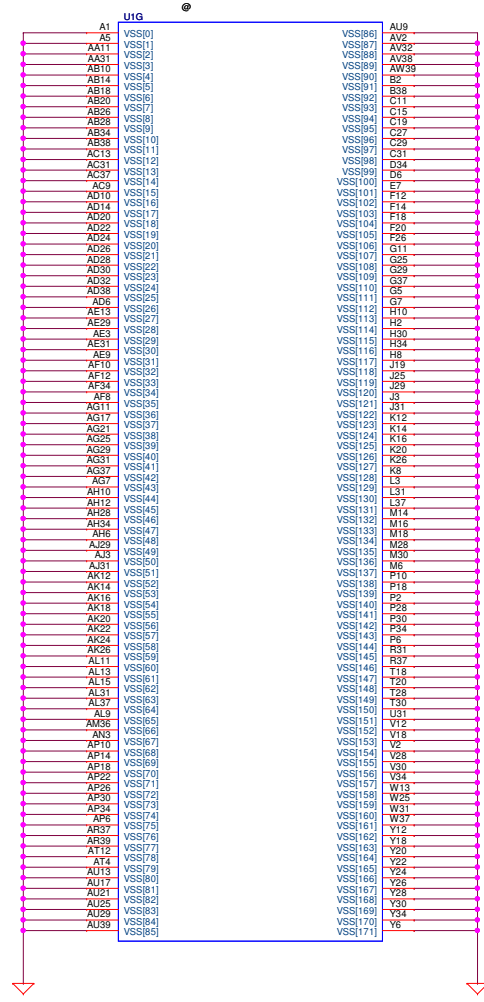
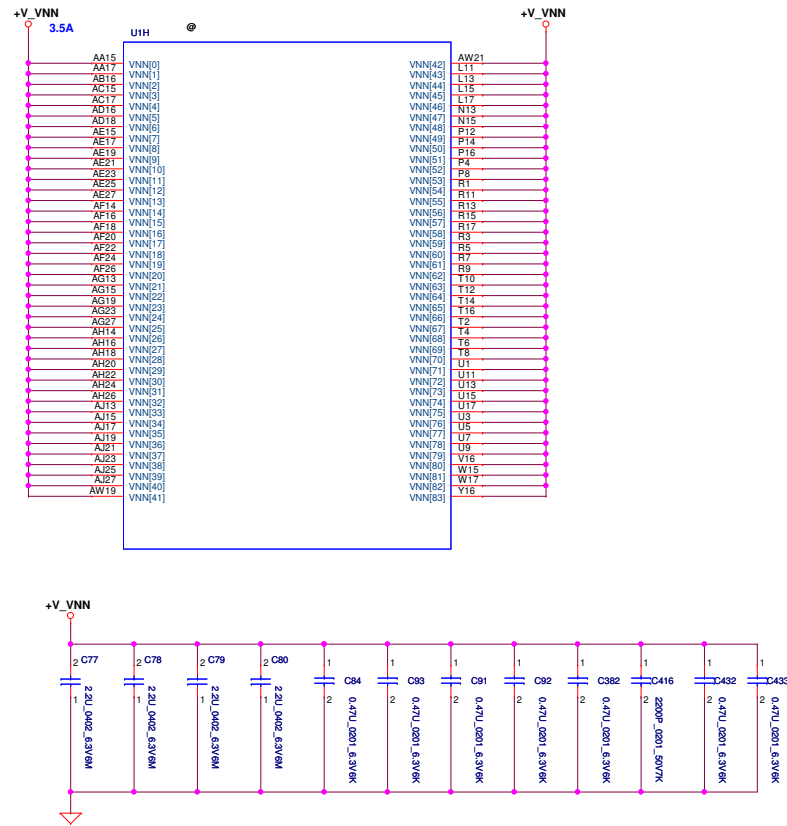
intel request reserve 0205

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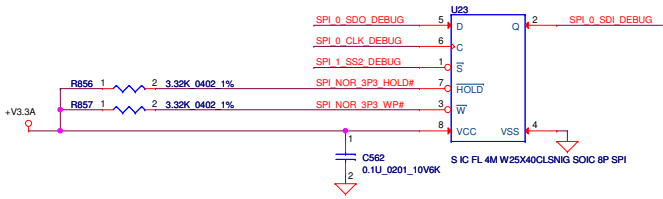
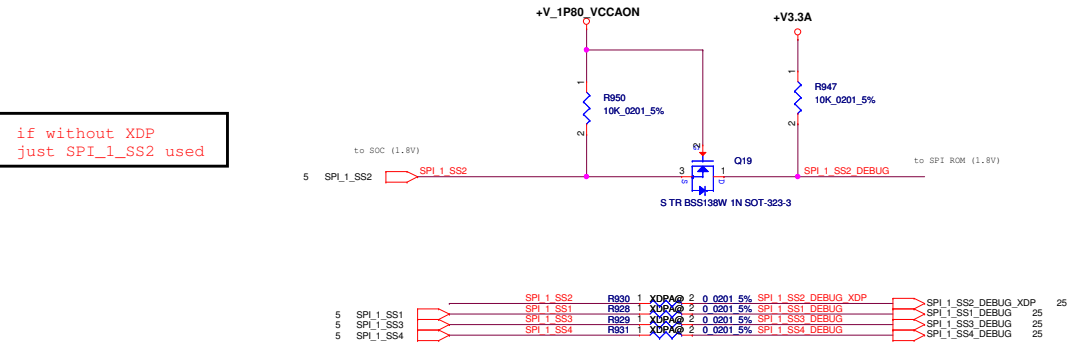
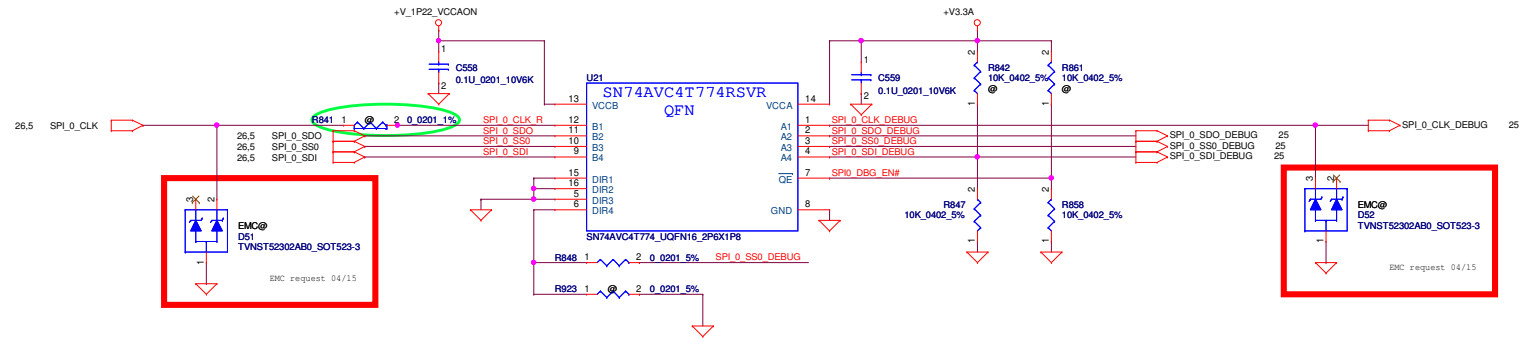


Power Rail	FFRD Hyprid 0.91	FFRD SLATE 1.1	Tangol116	Coach	Coach 1121
VNN	0.47uF x 7 (82)	0.47uF x 7 (82)	0.47uF x 16 (810)	0.47uF x 15 (81)	0.47uF x 8 / 2.2uF x 4
VNNAON	0.47uF x 5	0.47uF x 6	0.47uF x 9 (87)	0.47uF x 9 (81)	0.47uF x 4 / 2.2uF x 2
VCC	0.47uF x 11 (83)	0.47uF x 10 (82)	0.47uF x 12 (84)	0.47uF x 12 (84)	0.47uF x 12 (84)
VCC108	0.47uF x 7	0.47uF x 7	0.47uF x 7	0.47uF x 7	0.47uF x 4 / 2.2uF x 1
VCC108AS	0.47uF x 2 (81)	0.47uF x 2 (81)	0.47uF x 2	0.47uF x 2	0.47uF x 2
VCC108AON	0.47uF x 2	0.47uF x 2	0.47uF x 5 (83)	0.47uF x 5 (83)	0.47uF x 5 (83)
VCC122_180AON_I2C/I2S	0.47uF x 12	0.47uF x 13	0.47uF x 13	0.47uF x 13	0.47uF x 7 / 2.2uF x 3
VCC180AON_SRAM					
VCC122AON	0.47uF x 25	0.47uF x 25	0.47uF x 24	0.47uF x 24	0.47uF x 23 / 2.2uF x 10
VDD2	0.47uF x 9	0.47uF x 10			
VCC122AON_MEM	0.47uF x 14	0.47uF x 14	0.47uF x 24 (89)	0.47uF x 24	
VCCA100	0.47uF x 7	0.47uF x 7	0.47uF x 7	0.47uF x 7	0.47uF x 7
VCCA100AS	0.47uF x 3	0.47uF x 3	0.47uF x 5 (82)	0.47uF x 5 (82)	0.47uF x 5 (82)
VCCSDIO	0.47uF x 2	0.47uF x 2	0.47uF x 2 (82)	0.47uF x 2 (82)	0.47uF x 2 (82)
VDD1	0.47uF x 10	0.47uF x 10	0.47uF x 10	0.47uF x 10	0.47uF x 5 / 2.2uF x 2
VCC330	0.47uF x 1	0.47uF x 1	0.47uF x 3 (82)	0.47uF x 3 (82)	0.47uF x 3 (82)

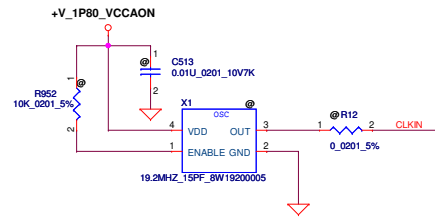
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SN74AVC4T774				OPERATION
OE#	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

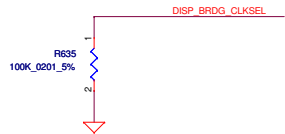


19.2 MHz OSC

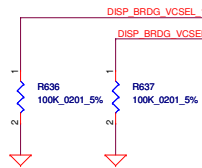


CLock selection

★ CLKSEL=0, CLKIN=19.2MHz
CLKSEL=1, CLKIN=26MHz



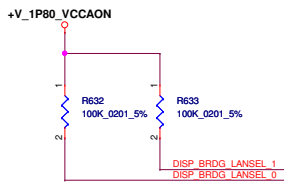
Virtual Channel Setting



Virtual Channel Setting (VCSEL[1:0])

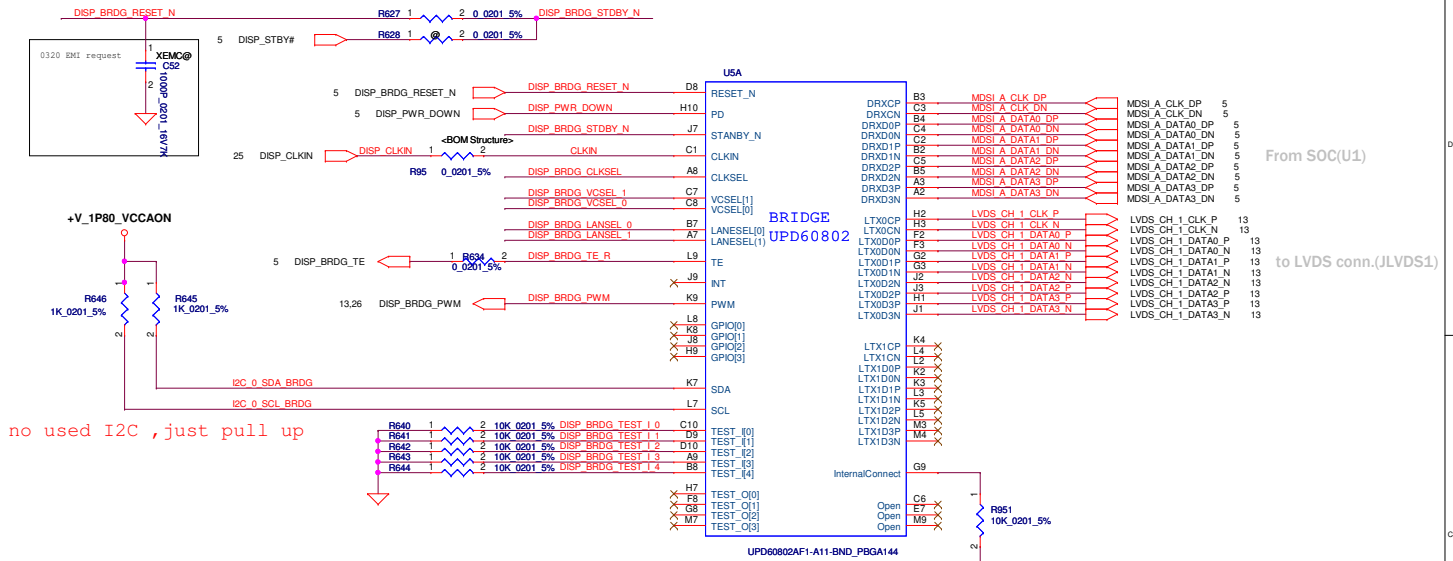
VCSEL[1:0] pin	DSI-RX Setting
★ 00	Virtual channel for Tremolo-2 sets to 0
01	Virtual channel for Tremolo-2 sets to 1
10	Virtual channel for Tremolo-2 sets to 2
11	Virtual channel for Tremolo-2 sets to 3

Data Lane Setting

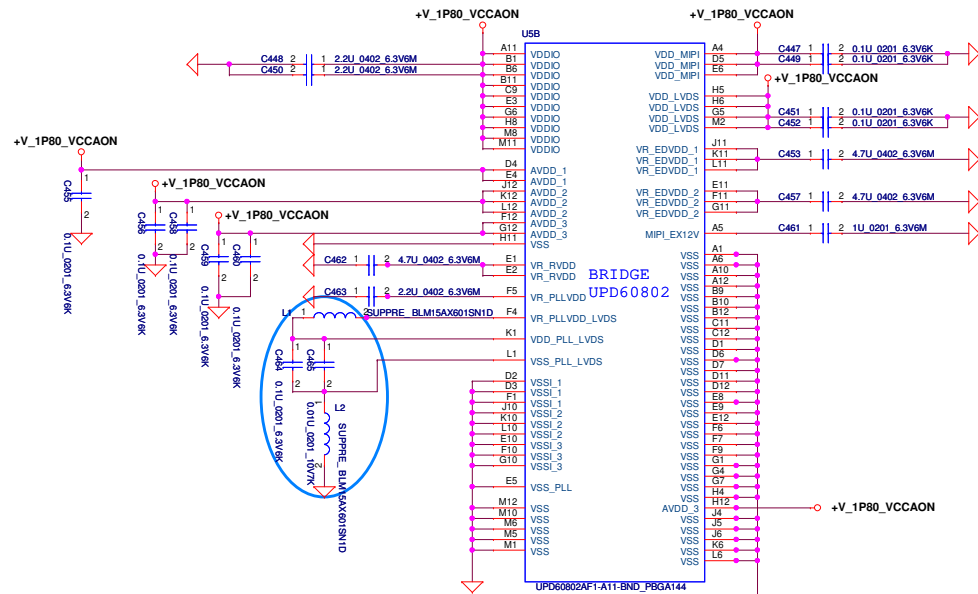


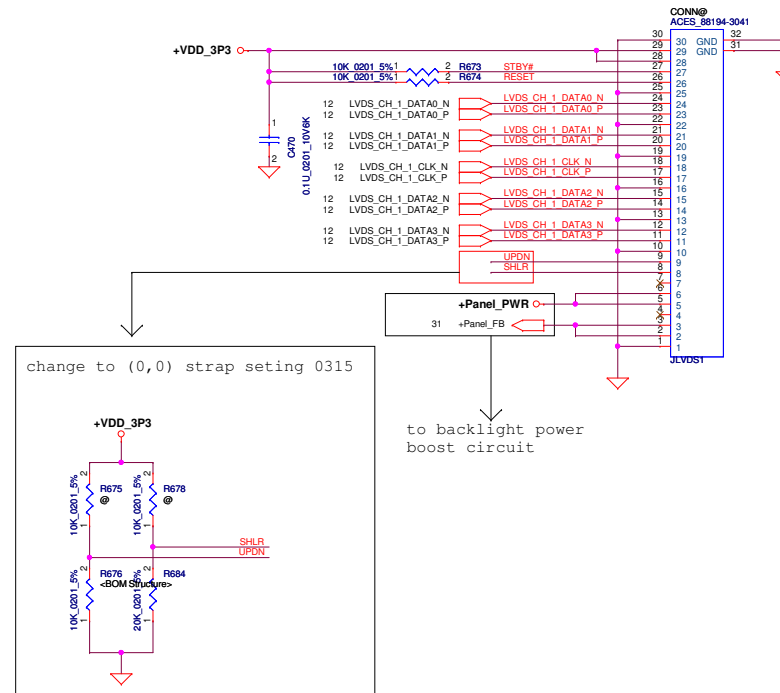
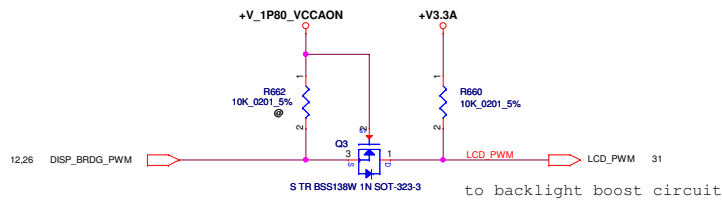
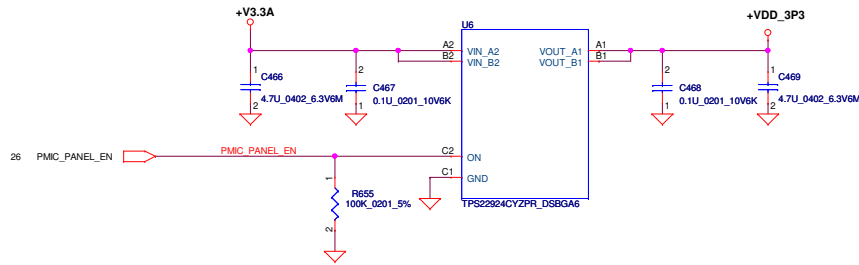
Data Lane Setting (LANSEL[1:0])

LANSEL[1:0] pin	DSI-RX Setting
00	1-Datalane: DRXCP/N, DRXD0P/N Valid DRXD1P, DRXD1N PIN should be left OPEN DRXD2P, DRXD2N PIN should be left OPEN DRXD3P, DRXD3N PIN should be left OPEN
01	2-Datalane: DRXCP/N, DRXD0P/N DRXD1P/N Valid DRXD2P, DRXD2N PIN should be left OPEN DRXD3P, DRXD3N PIN should be left OPEN
10	Reserved
★ 11	4-Datalane: DRXCP/N, DRXD0P/N, DRXD1P/N DRXD2P/N, DRXD3P/N Valid



no used I2C , just pull up





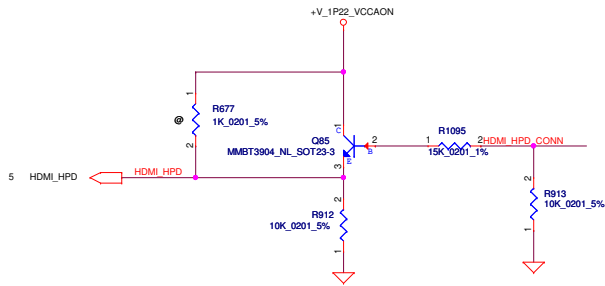
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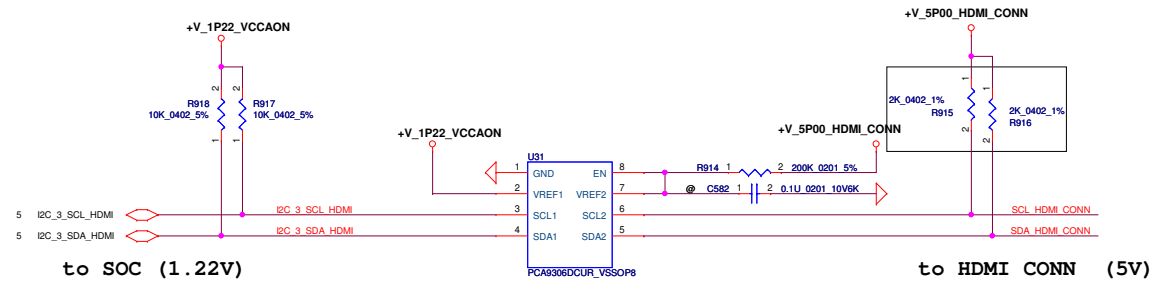
LVDS CONNECTOR

Cheetah CT LA-A411P R02

HDMI Hot plug circuit

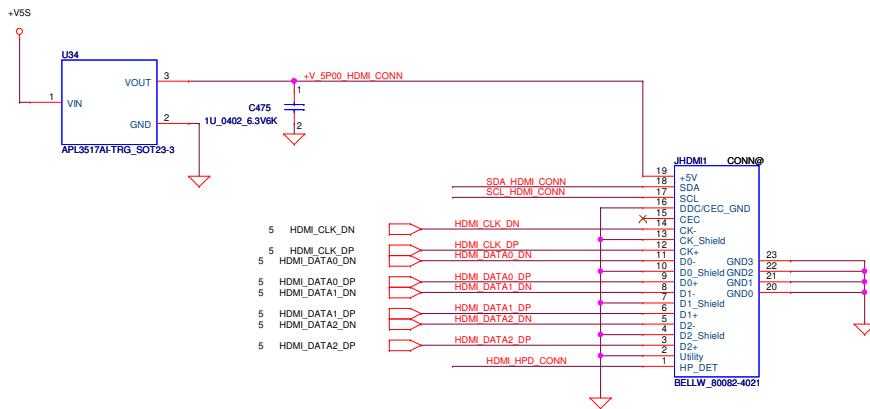


EDID I2C level shift

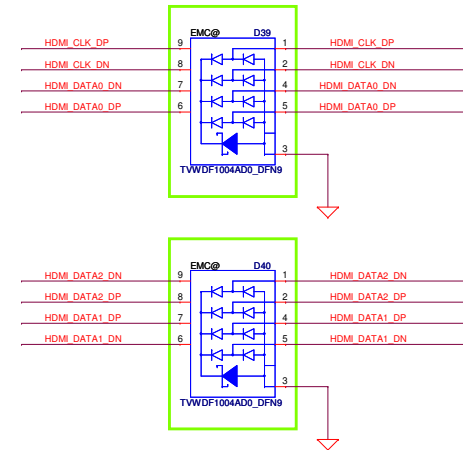


Check SMBUS pull high vaule

HDMI 5V protection and connector

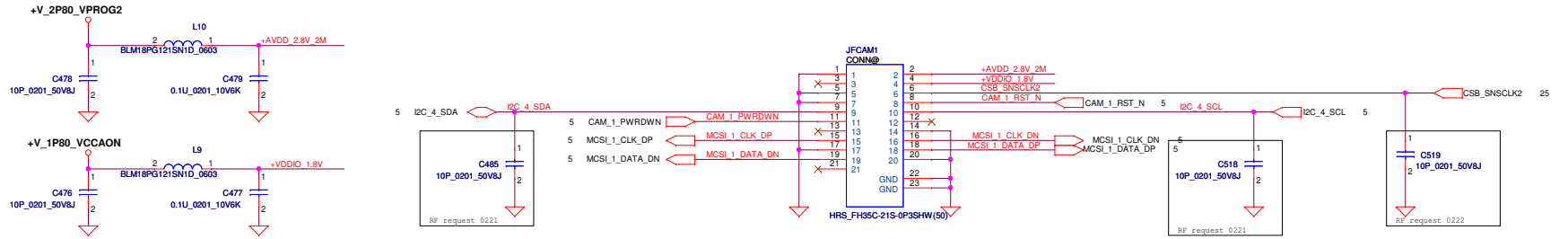


HDMI ESD protection

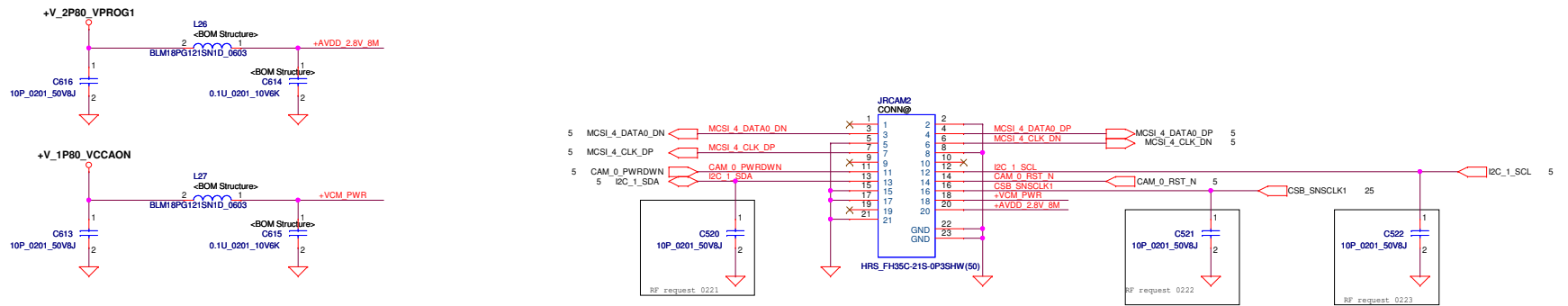


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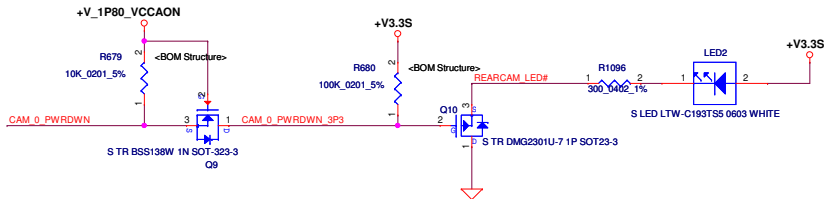
2M front Camera



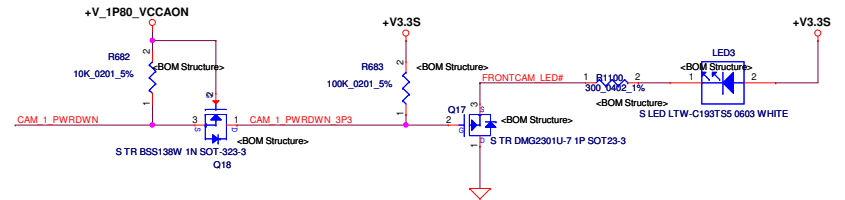
2M rear Camera



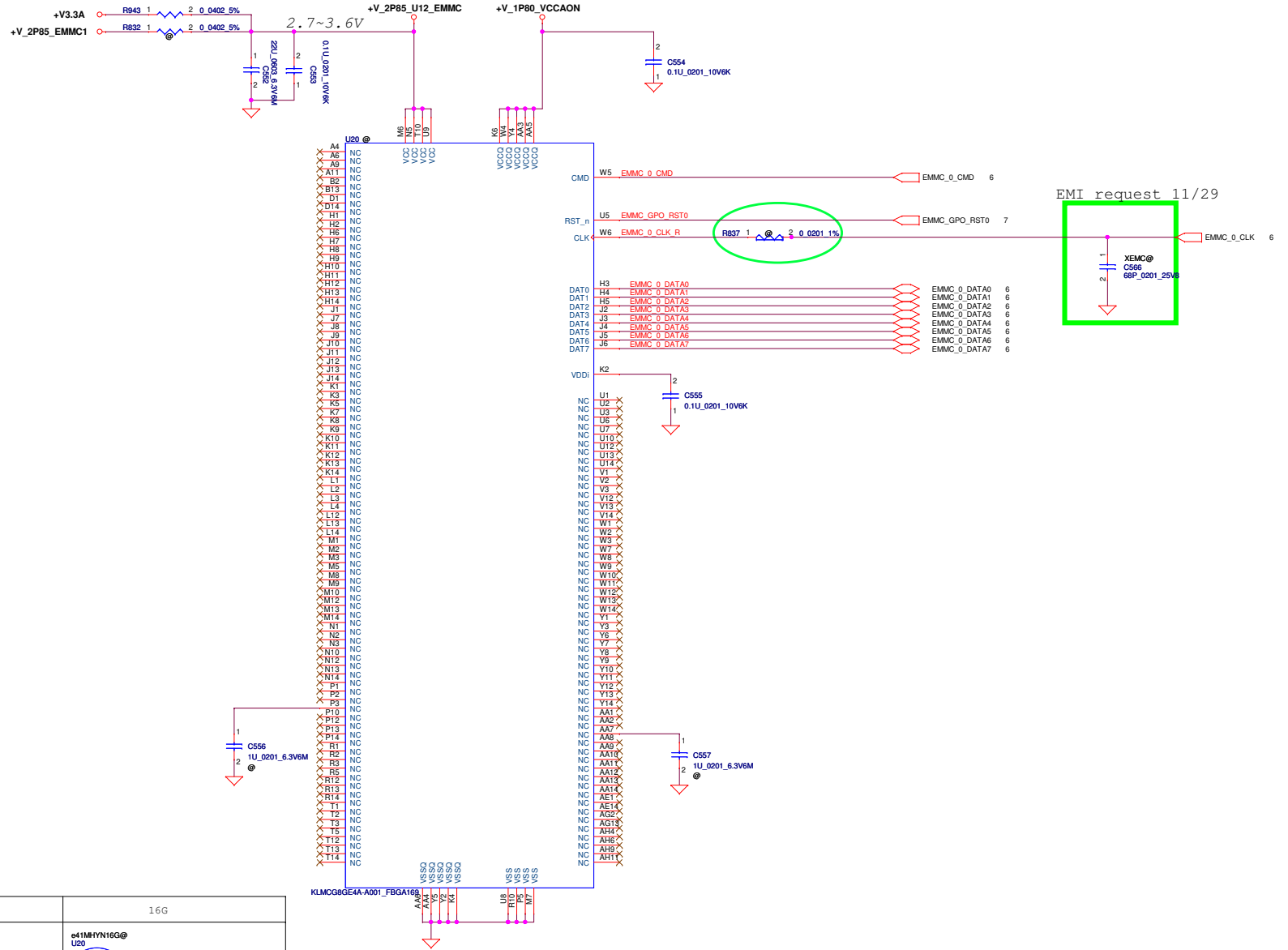
Rear Camera LED



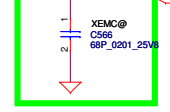
Front Camera LED



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Customer	Document Number	Rev	Cheetah CT LA-A411P R02	
Date:	Friday, April 12, 2013	Sheet	15	of 35



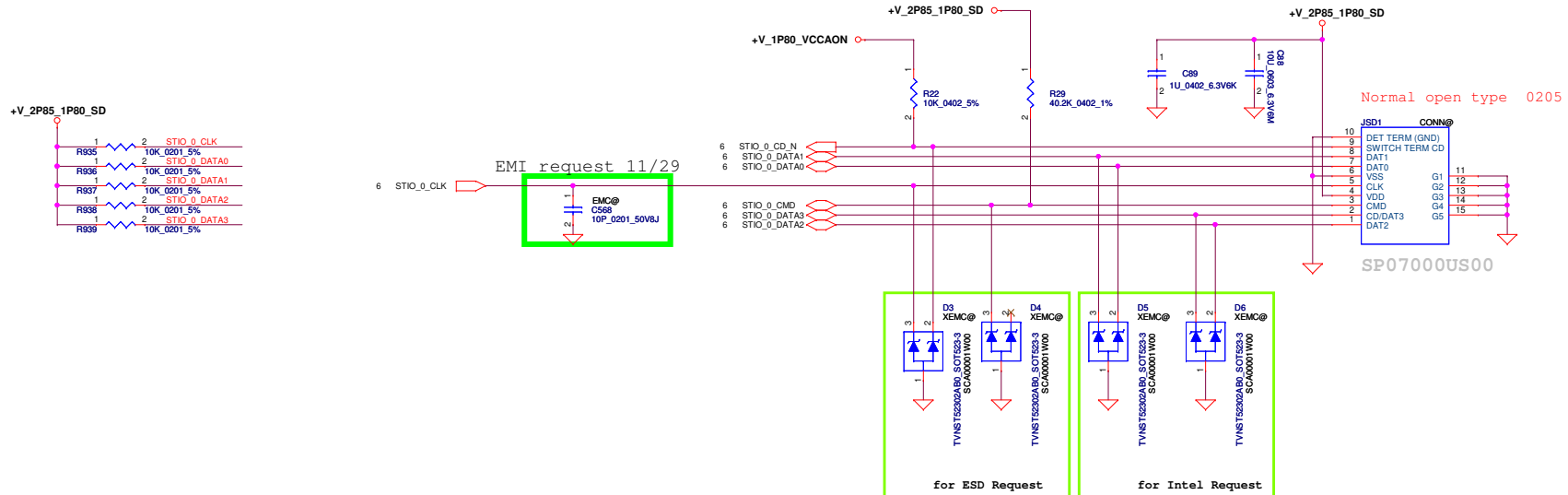
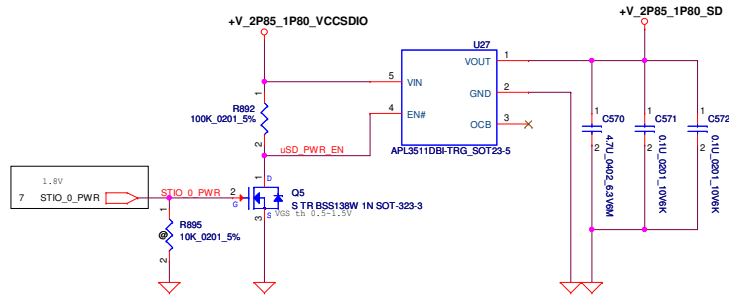
EMI request 11/29



	64G	32G	16G
V4.41	e41MSAM64G@ U20 S IC FL 64G KLMCG8GE4A-A001 FBGA169 ABO ! SA00005GT10	e41MSAM32G@ U20 S IC FL 32G KE4CN5B6A FBGA 169P ABO ! SA00006DY10	e41MHYN16G@ U20 S IC FL 16G H26M52002EQR FBGA 169P ABO ! SA00006DW10
V4.5	eMHYN64G@ U20 S IC FL 64G H26M78003BFR FBGA 169P ABO ! SA000068D20 eMSAM64G@ U20 S IC FL 64G KLMCG8GEAC-B001 FBGA153 ABO ! SA00006UU10	eMHYN32G@ U20 S IC FL 32G H26M64003DQR FBGA 169P ABO ! SA000068C20 eSAM32G@ U20 S IC FL 32G KLMBG4GEAC-B001 FBGA153 ABO ! SA00006UU10	

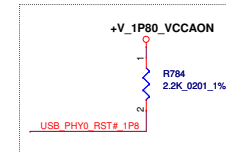
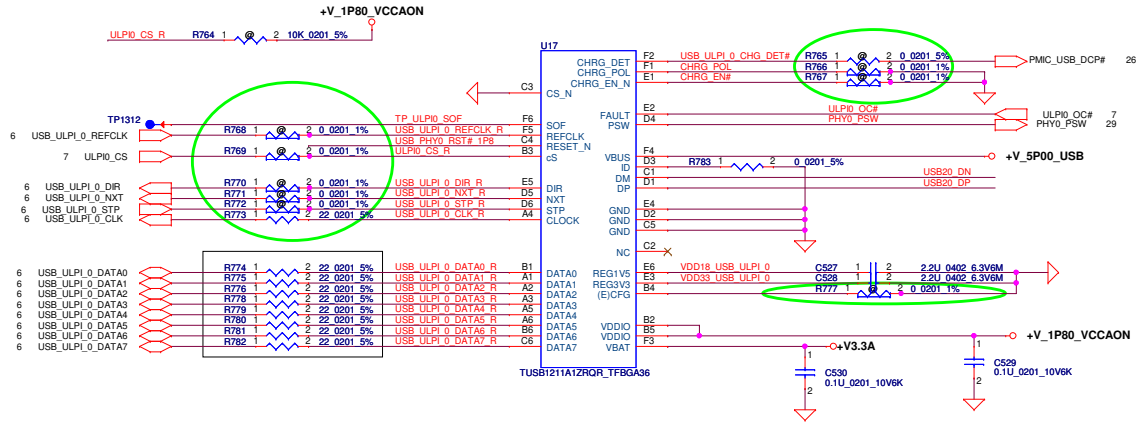
Micro SD

Micro SD power supply circuit

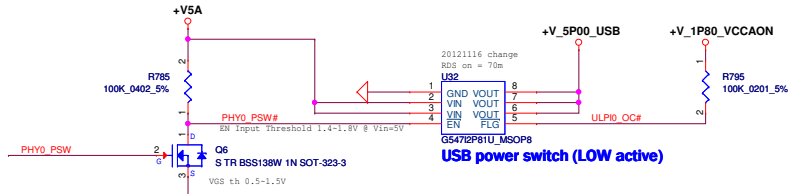


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Issued Date	2013/02/04	Deciphered Date	2014/04/01	uSD	
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			Date:	Thursday, April 11, 2013	Sheet 17 of 35

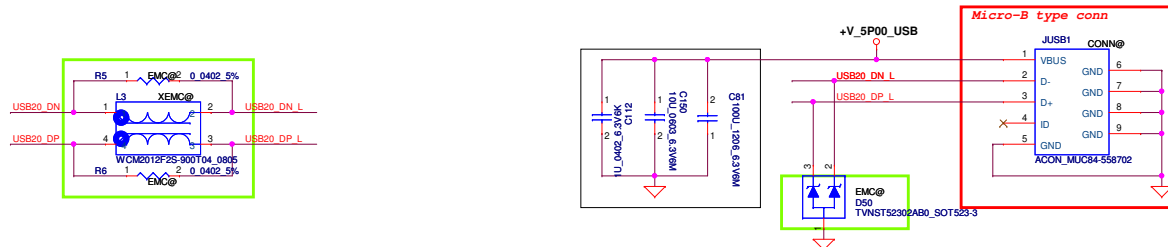
Internal USB
ULPI0_USB2.0 PHY



USB power switch



USB connector

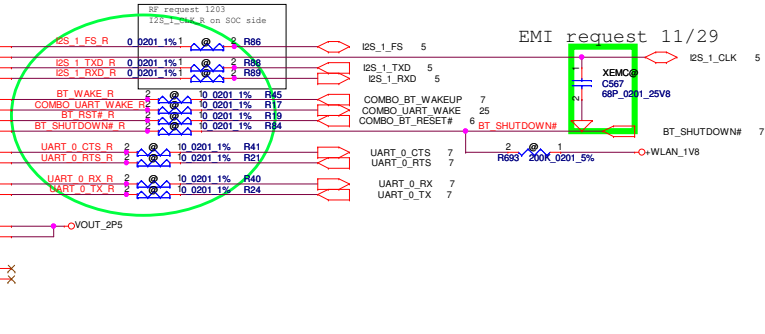
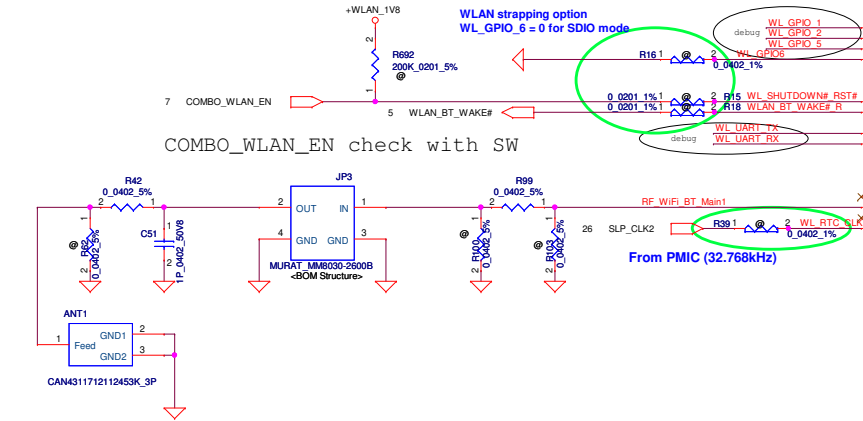
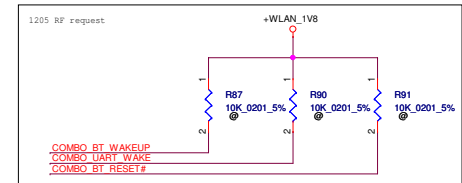
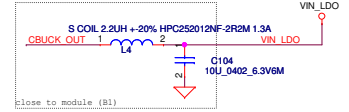
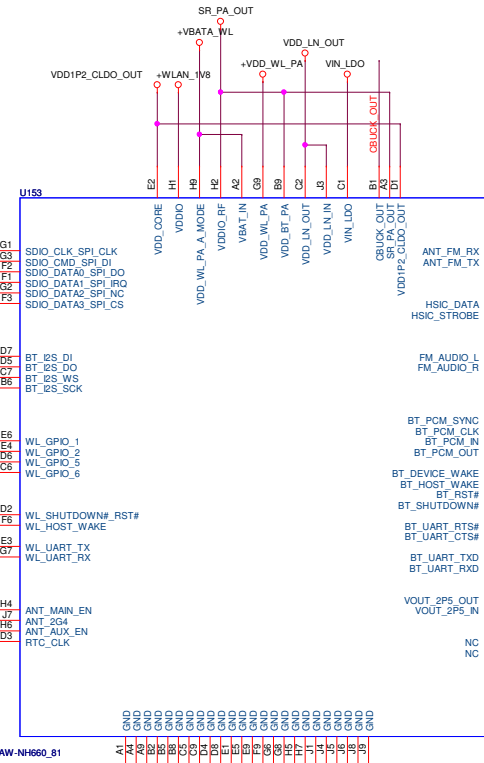
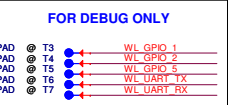
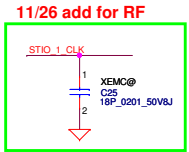
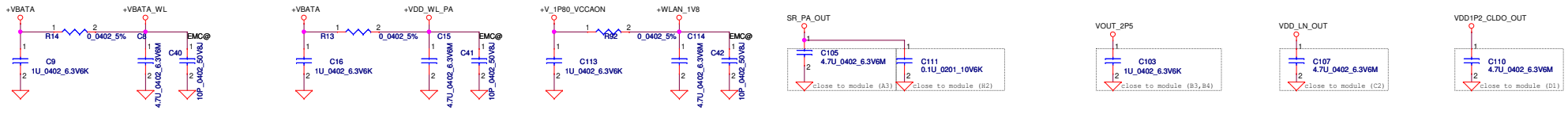


The ID pin on a Micro-A plug shall be connected to the GND pin. The ID pin on a "Micro-B" plug is not connected or is connected to ground by a resistance of greater than Rb_PLUG_ID (100k? MIN). An On-Go device is required to be able to detect whether a Micro-A or Micro-B plug is inserted by determining if the ID pin resistance to ground is less than Ra_PLUG_ID (10? MAX) or if the resistance to ground is greater than Rb_PLUG_ID. Any ID resistance less than Ra_PLUG_ID shall be treated as ID = FALSE and any resistance greater than Rb_PLUG_ID shall be treated as ID = TRUE.

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VBAT_IN	Power supply for Internal Regulators	2.3~4.8V
SR_PA_OUT	Power supply out from internal LDO	3.3V
VDD_WL_PA A MODE	Power supply for internal Power amplifier	2.3~5.5V
VDDIO_RF	I/O power supply for RF front-end	3.3V
VDD_BT_PA	Power supply for BT PA	3.3V
VDD_WL_PA	Power supply for WLAN PA driver	2.3~5.5V
CBUCK_OUT	Power supply for Internal CLDO/LDO1	1.35~2V
VOUT_2P5_IN	Power supply for FM	2.5V
VOUT_2P5_OUT	Power supply from internal LDO	2.5V
VIN_LDO	Power supply to internal Regulator	1.5V
VDD_LN_IN	Power supply for Noise Sensitive Block (AFE,PLL...)	1.14~1.26V
VDD_LN_OUT	Power supply for Noise Sensitive Block (AFE,PLL...)	1.14~1.26V
VDD1P2_CLDO_OUT	Power supply from Internal CLDO	1.14~1.26V
VDD_CORE	Power supply for Core Voltage	1.14~1.26V
VDDIO	I/O power supply for BT/FM/GPIO	1.2~2.9V

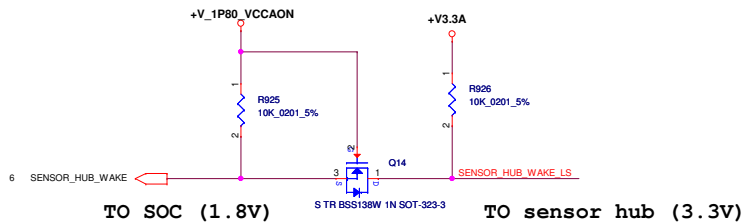
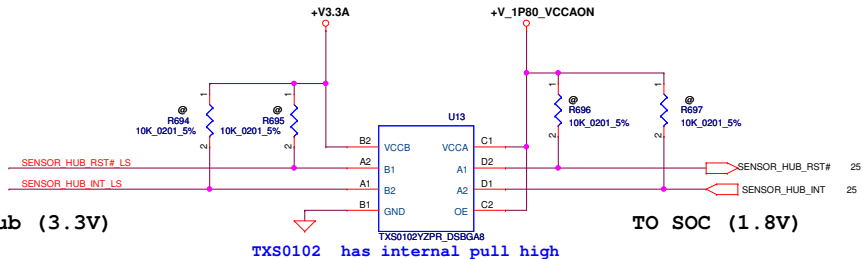
AW-NH660	WL_SHUTDOWN#_RST#	BT_SHUTDOWN#	BT_RST#
WL on/BT on	H	H	H
WL on/BT off	H	H	L
WL off/BT on	L	H	H
WL off/BT off	L	L	L



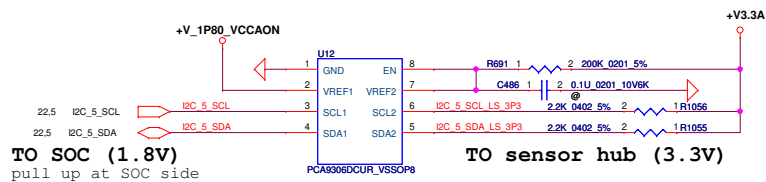
BT_WAKE : Host to Device indicating that Host requires attention.
 BT_HOST_WAKE : Device to Host indicating that BT device requires attention.
 BT_SHUTDOWN# : (OR-Gate with WL_SHUTDOWN#_RST#)
 To decide whether or not to power down int. regulator
 BT_RST# : Low Asserting Reset for Bluetooth /FM Core.

BT_SHUTDOWN# connect to SoC GP_Core, confirm with SW later

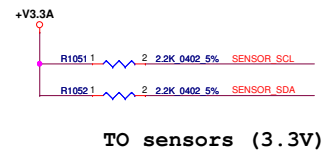
Sensor Hub GPIO level shift



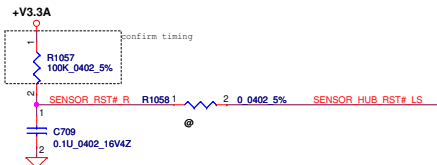
Sensor Hub I2C level shift



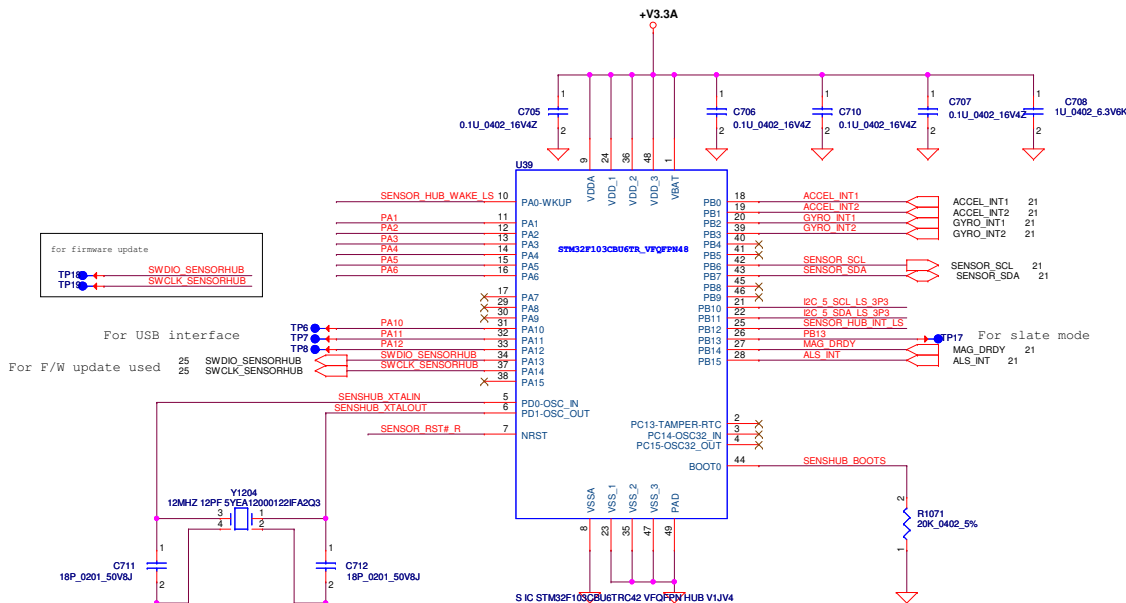
Sensor Hub I2C pull up



Sensor Hub RST circuit

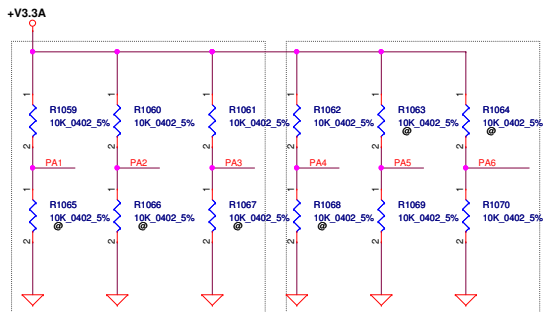


Sensor Hub circuit



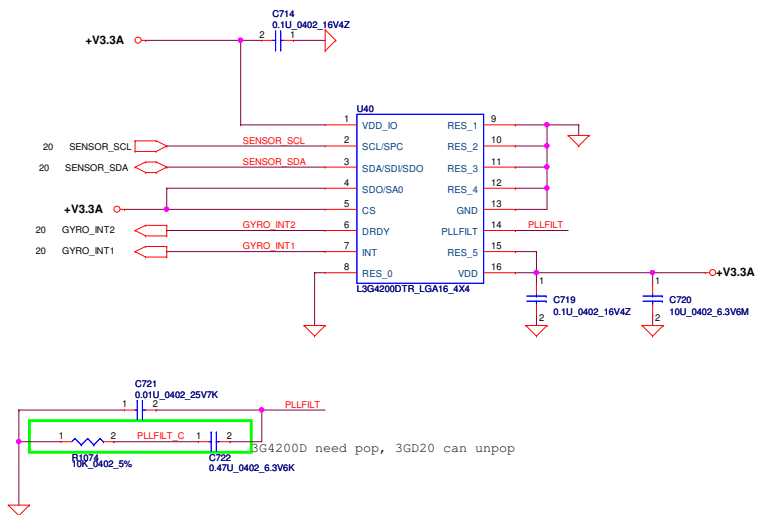
Sensor IC orientation turning

PA1	303I
PA2	303M
PA3	303N
PA4	4200I
PA5	4200M
PA6	4200N

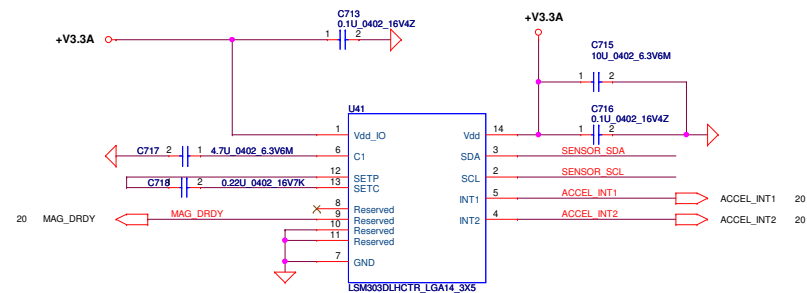


(I,M,N) about layout is (1,1,1) (I,M,N) about layout is (1,0,0)

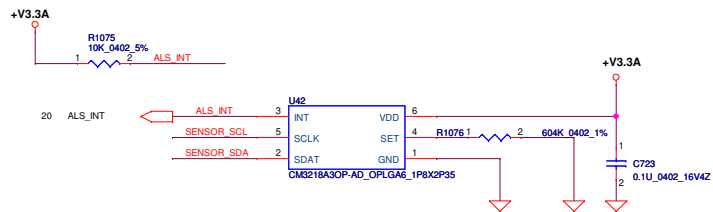
GYROSCOPE



Accelerometer & E-COMPASS

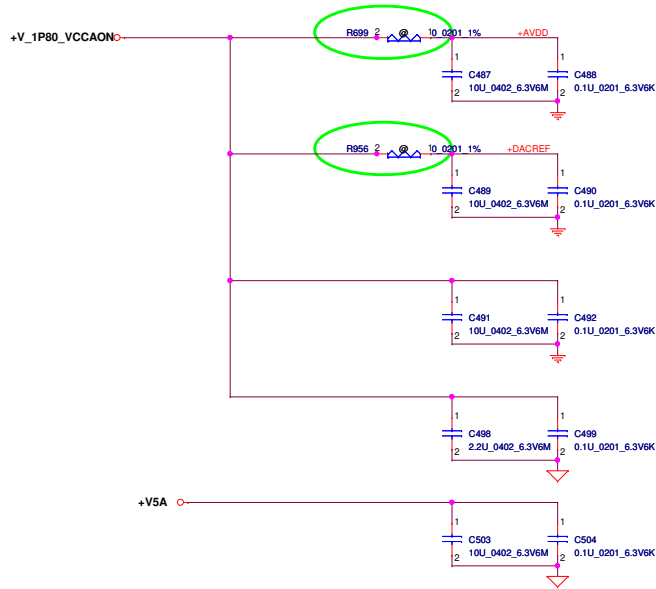


LIGHT SENSOR

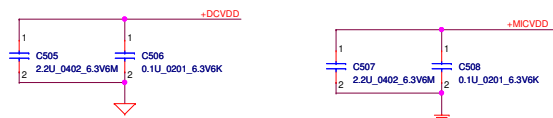


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Issued Date	2013./02/04	Deciphered Date	2014/04/01	Sensor
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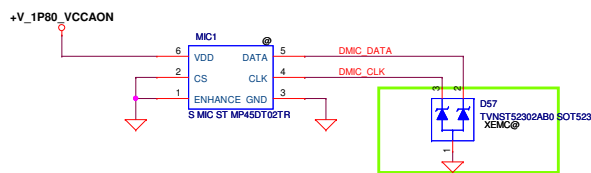
Codec input power CAP



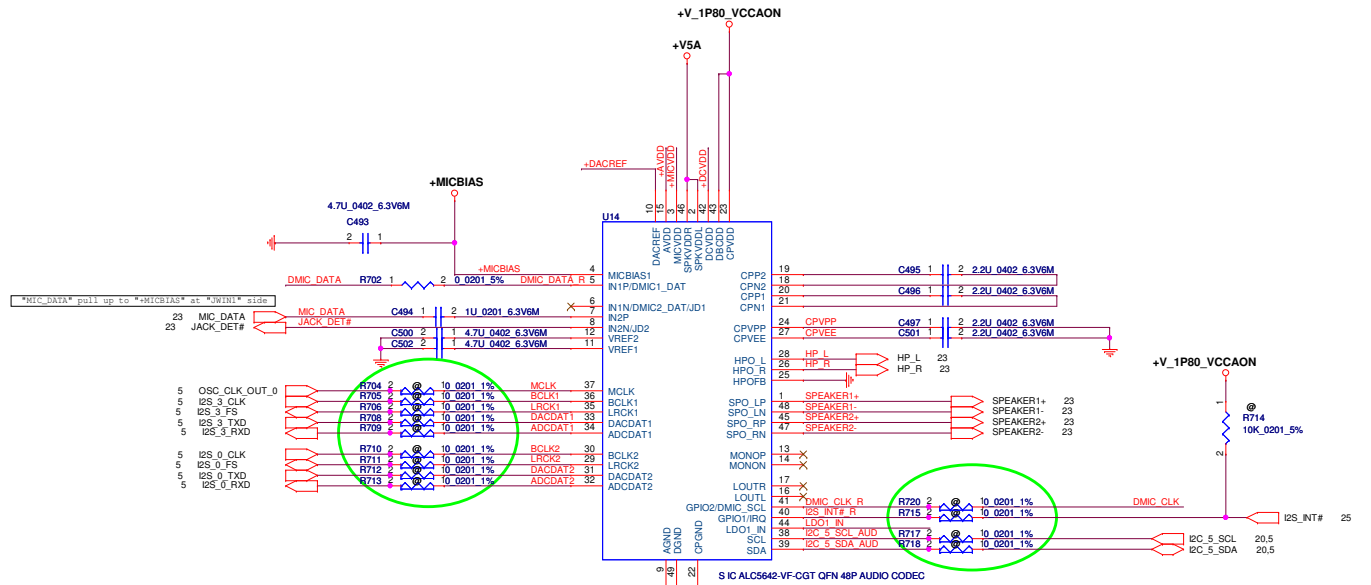
Codec output power CAP



Digital MIC Conn.

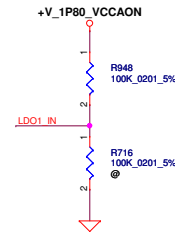


Codec



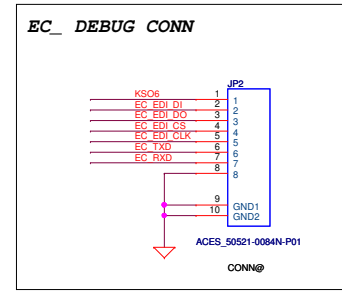
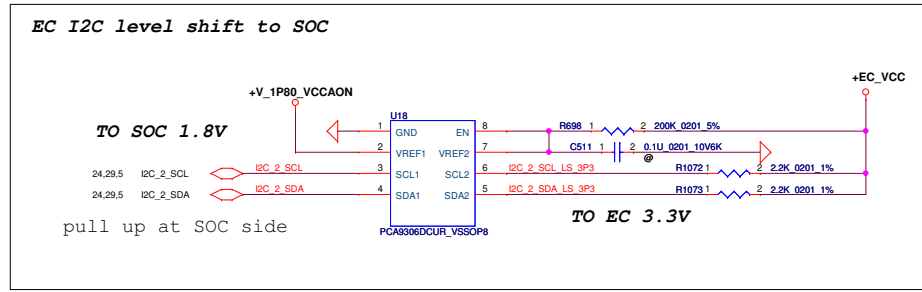
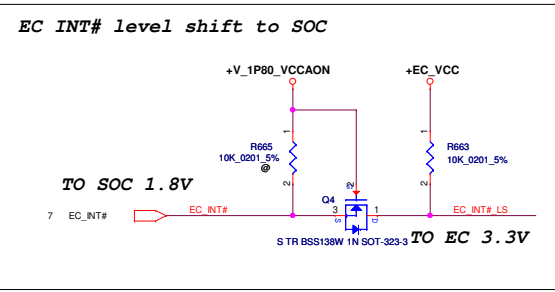
LDO1 enable control

LDO1 enable control
for digital core power DCVDD
Low: Disable
High: Enable

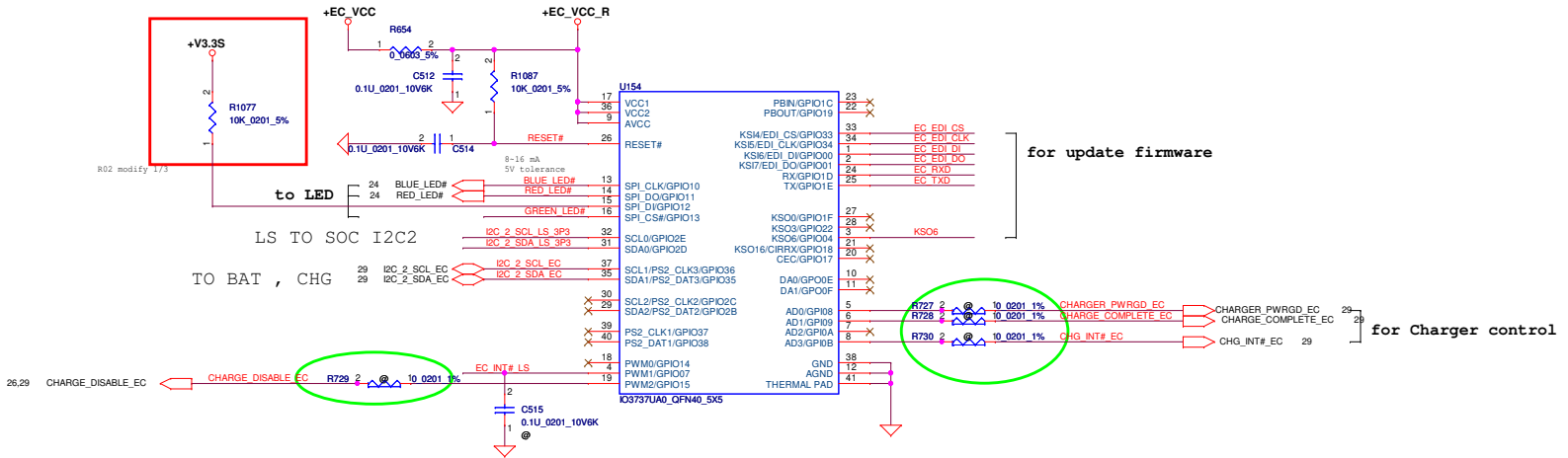


GND & GNDA bridge

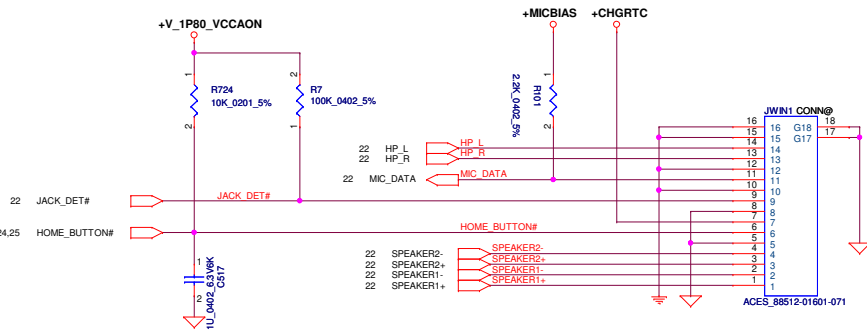




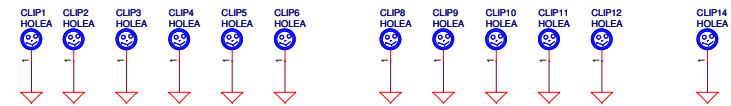
EC _ ENE IO3737



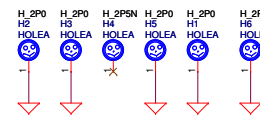
HOME Key/SPK/Jack SUB Board Conn.



Shielding Clip

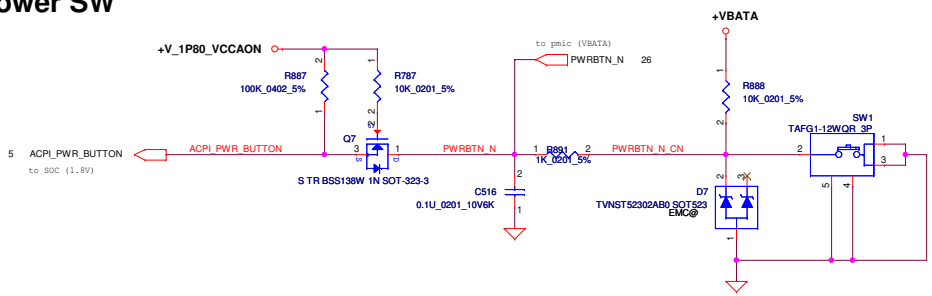


SCREW / FD

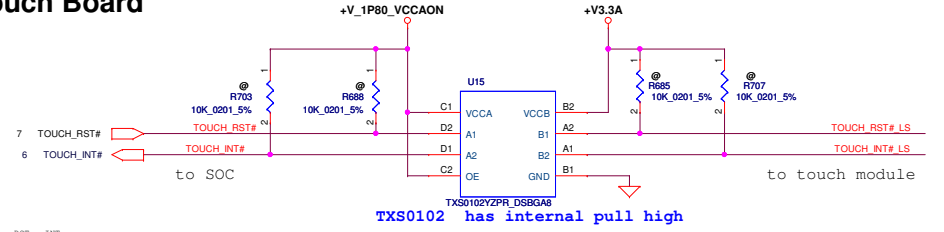


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Issued Date	2013/02/04	Deciphered Date	2014/04/01	Title	HOME CONN /SCREW/EC
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Power SW

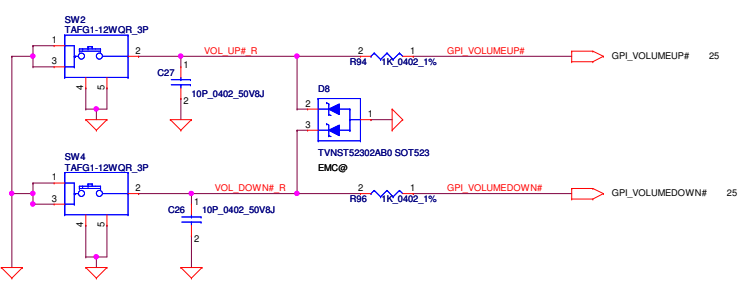


TO Touch Board

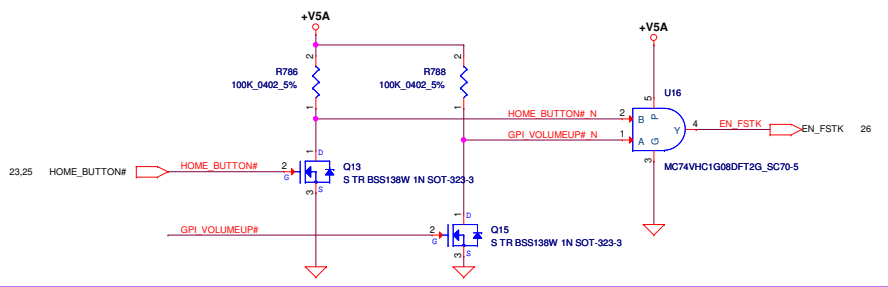


Level shift for RST , INT

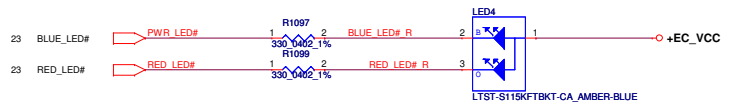
Volume button up / down



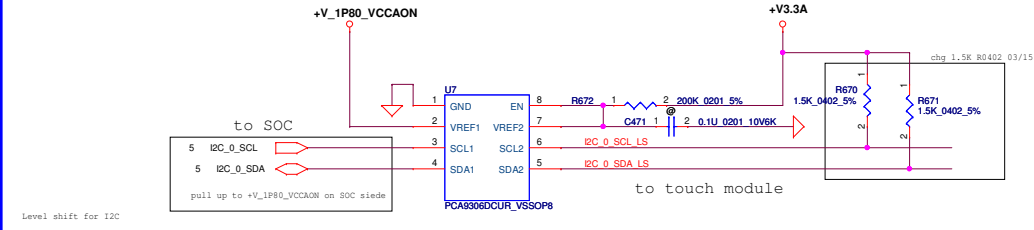
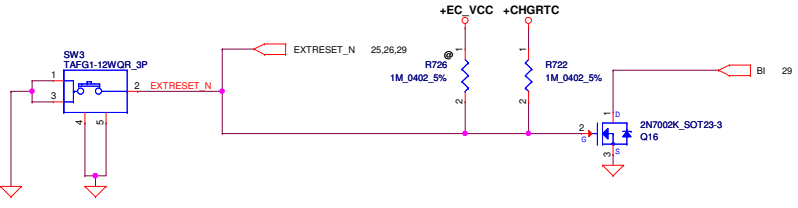
for into recovery mode



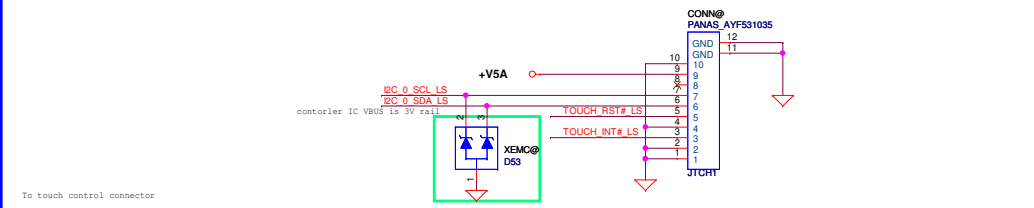
POWER LED



RST switch

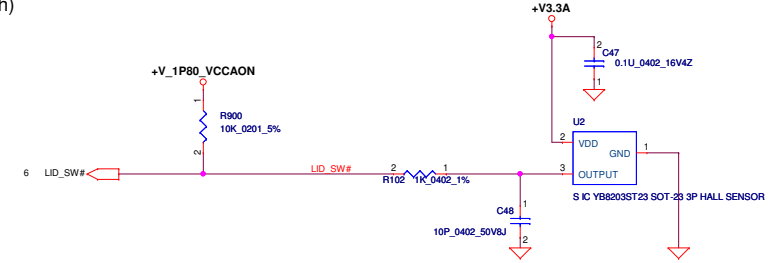


Level shift for I2C

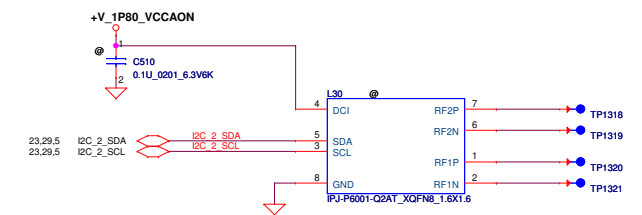


Lid Switch

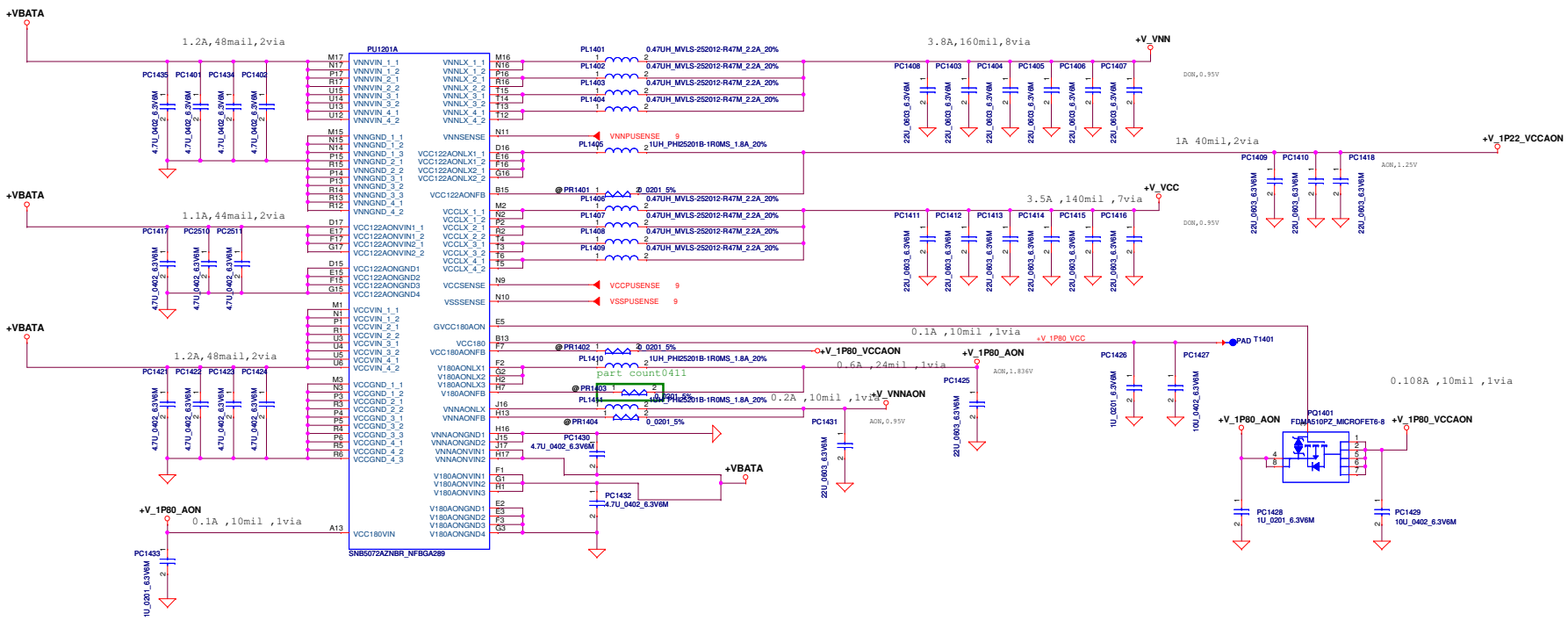
(Hall Effect Switch)



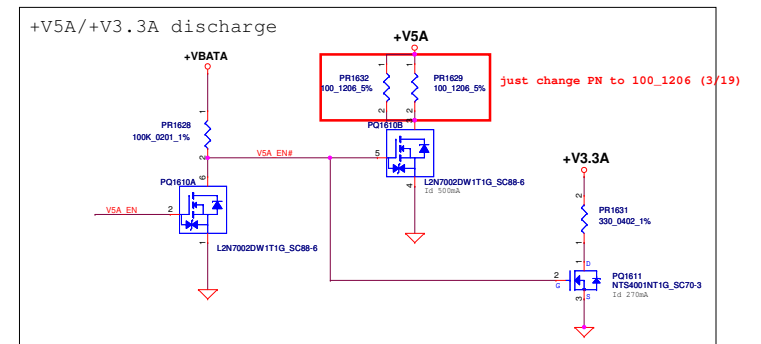
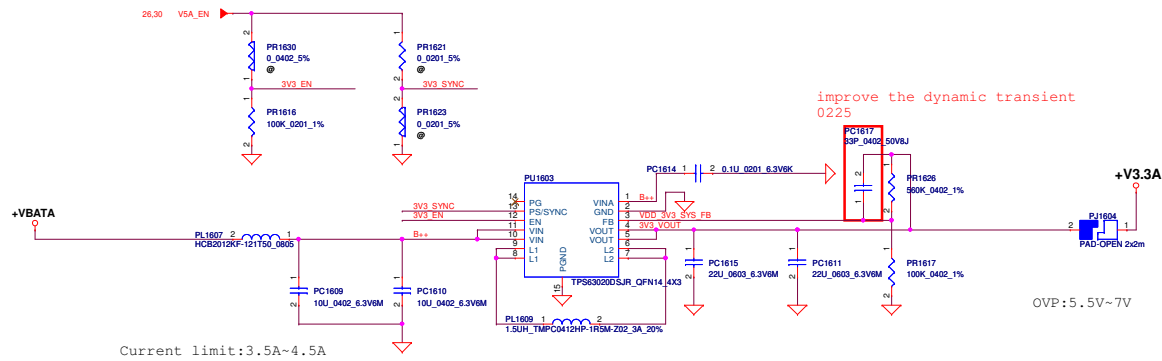
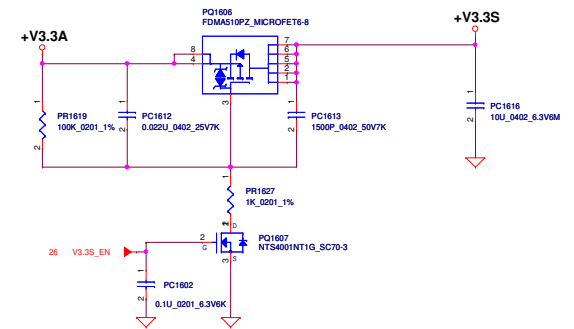
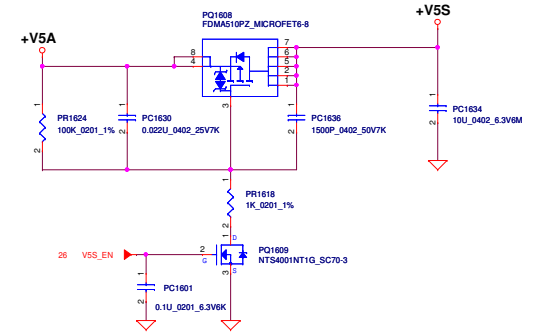
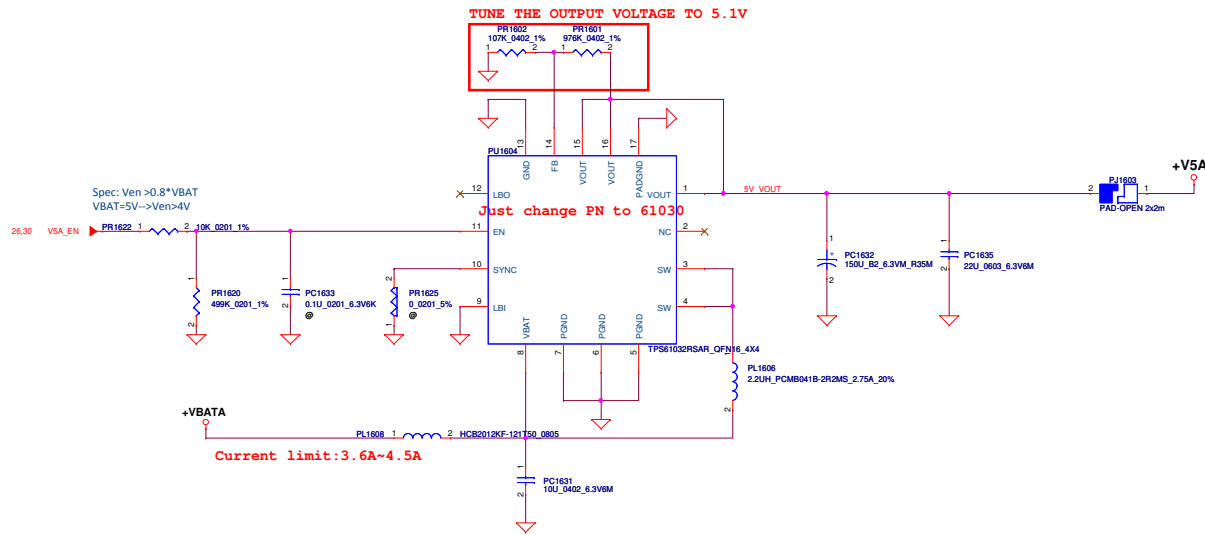
Reserve PSS



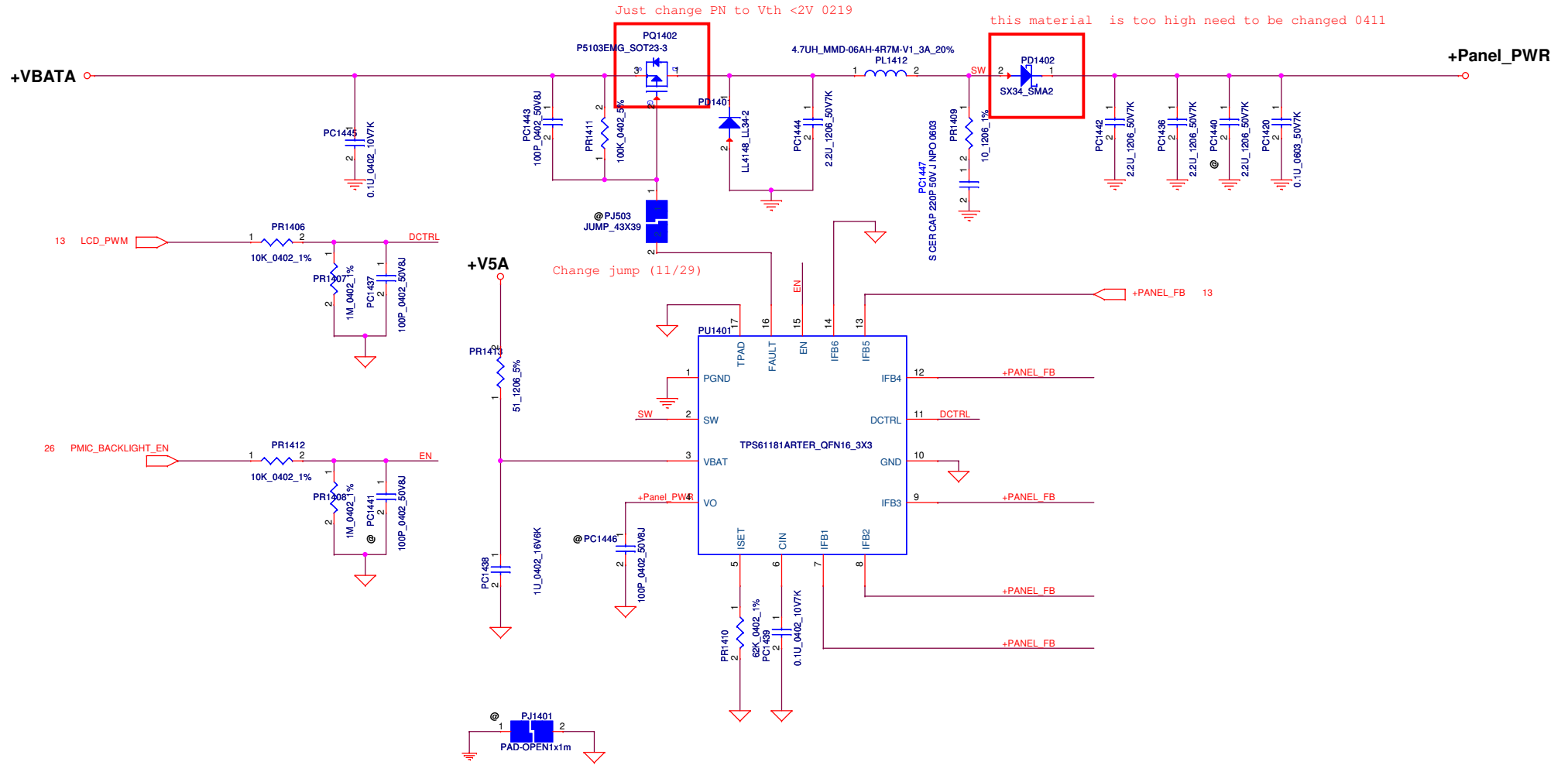
Security Classification	Compal Secret Data		Title	
Issued Date	2013/02/04	Deciphered Date	2014/04/01	BTN/LED/Touch Board
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Security Classification	Compal Secret Data		Title	
Issued Date	2013/02/04	Deciphered Date	2014/04/01	DCDC (3/5V)
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Size A2	Document Number	Rev		Raw
	Cheetah CT LA-A411P	R01		
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Issued Date	2013/02/04	Deciphered Date	2014/04/01
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Compal Electronics, Inc.	
Title Backlight LED Power	
Size A3	Document Number Cheetah CT LA-A411P_R01.2
Date: Friday, April 12, 2013	Sheet 31 of 32

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add EC to control charger	27,30	Change Net name PMIC_CHARGER_DISABLE to CHARGER_DISABLE_EC	1/3	EVT
2	Add EC to control charger	30	Add net name I2C_2_SCL_EC, I2C_2_SDA_EC, CHARGER_PWRGD_EC, CHARGE_COMPLETE_EC, CHG_INT#_EC	1/3	EVT
3	Swap battery connector pin order to follow Acer define	30	Swap PJP2801 pin order	1/3	EVT
4	Add +EC_VCC power rail	30	Add PU301, PC1527, PC1528, PC1529	1/3	EVT
5	Change DCIN connector from 4pin to 5pin	30	Change JP1 to ACES_88266-05001	1/3	EVT
6					
7	PMIC sequence issue	30	Mount PR1533	1/3	EVT
8	POWER rail V5A need to set higher change PU1604 PN to TPS61030	31	change PU1604 PN to TPS61030	1/8	EVT
9	POWER rail V5A need to set higher change PU1604 PN to TPS61030	31	mount PR1601 PR1602	1/8	EVT
10	change vender to common material		PC102, PC1511, PC1518 PC15130 PC1526	1/8	EVT
11	Follow intel schematic	30	PC1525 PC1516 PC1530	1/8	EVT
12	TI PMIC AC only bug				
13	intel request	30	PC1331	3/5	PVT
14	follow intel schematic	30	PR1629	3/5	PVT
15	PI pin pull low to GND	29	PR1535	3/6	PVT
16	change Ilim value	28	PR1520	3/25	PVT
17	change PH resistor in PVT	29	PR1511 PR1512	3/25	PVT
18	need one more resistor to sfford the current	30	PR1629 PR1632	3/25	PVT
19	change the short pad resistor to not short pad	26	PR1223	4/11	PVT
20					

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Change pwoer LED power to +EC_VCC	24		03/15	PVT
2	change panel SHLR/UPDN strap (0,0)	13	unpop R678	03/15	PVT
3	change touch I2C pull high resister	24	chg R670,R671 to 1.5K R 0402	03/15	PVT
4	touch board connector pin1 error	24	swap JTCH1	03/15	PVT
5	fine tune the crystal clock	5,20	change C1,C2 ,C711,C712 to 18P	03/15	PVT
6	add screw hole	23	add H6	03/18	PVT
7	change RF component for RF request	19	change R61 to C51 , R104 to C52 , R105 to L31	03/18	PVT
8	Reserve Rst btn pull up to +EC_VCC	24	Add R726	03/18	PVT
9	Reserve ANT2 circuit	19	remove JANT1 , R97, JANT2 , ANT2 , L31, C52 , R106 , R98	03/20	PVT
10	change JWIN1 PIN8 to DGND	23		03/20	PVT
11	change R723,R725 to R0402	22		03/20	PVT
12	net "EC_INT#_LS'' wrong pwoer rail	23	change R663 pull up to +EC_VCC	03/20	PVT
13	EMC request	5	C3,C4,C5,C6 change to 1000P and POP C3,C4,C5	03/20	PVT
14	EMC request	18	change D50 to EMC@	03/20	PVT
15	EMC request	5,12	add C52,C53 for net "DISP_BRDG_RESET_N"	03/20	PVT
16	+V_3P30_VCC discharger	8	change R681 to 0603 and pop Q11,R681	03/21	PVT
17		23	chg H4 to 2P5N	03/21	PVT
18		24	Chg hole sensor U2 to AH180WG-7_SC59-3	03/21	PVT
19	modify sensor strap setting	20	POP R1061,R1069,R1070 ; unpop R1067,R1063,R1064	03/25	PVT
20	POP RTC curcuit	24	POP R722,Q16	03/25	PVT
21	add Homekey debounce	23	add C517	04/03	Pre MP
22	change LVDS bridge to A11 version	12	change U5 PN to SA00005ER30	04/10	Pre MP
23	change JP3 to HW part and change P/N	19	change JP3 PN to SN700000100	04/11	Pre MP
24	EMC request	11	Add D51 D52 for ESD request	04/15	Pre MP

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