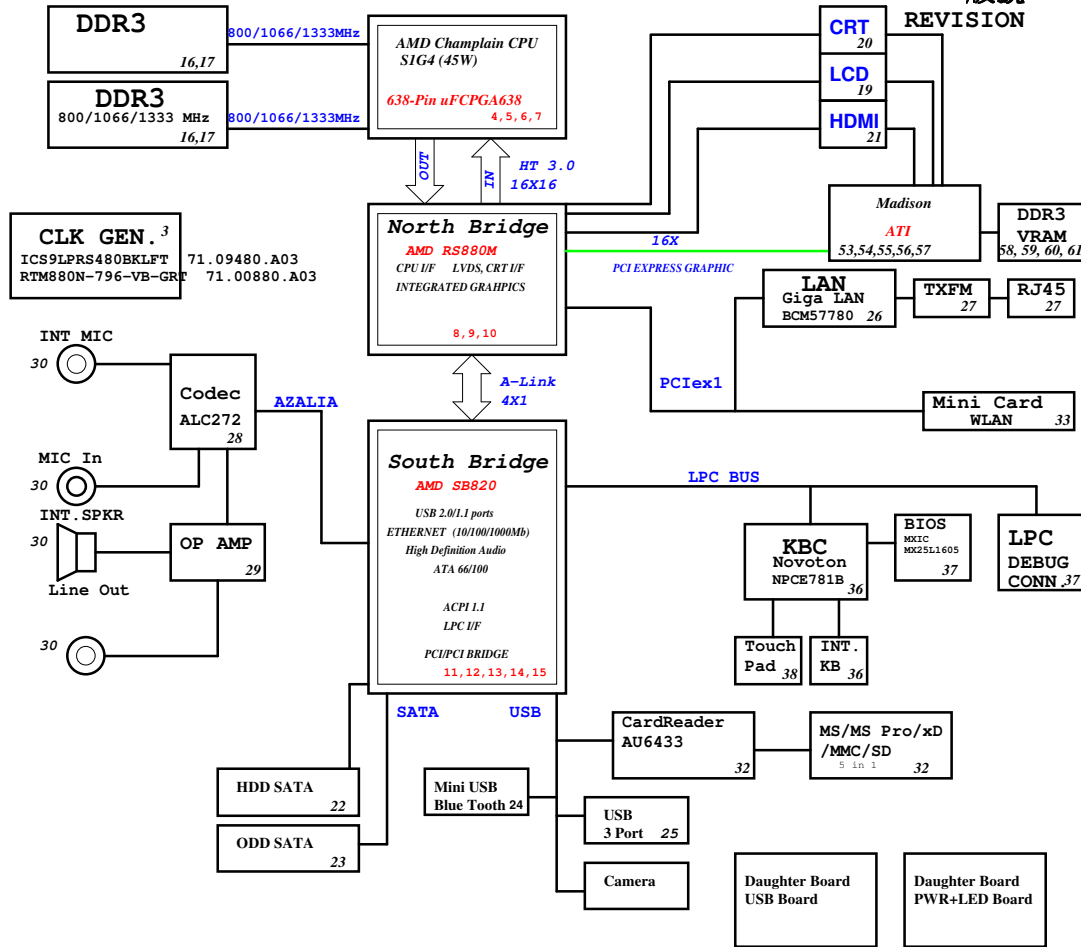


HM42-DN Block Diagram

Project code: 91.4HD01.001
 PCB P/N : 48.4GX01.0SA
 PCB 版號 : 09919 SA
 REVISION : PCB STACKUP



TOP _____
 VCC _____
 S _____
 GND _____
 BOTTOM _____

SYSTEM DC/DC	
RT8223	46
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (5.5A)
	3D3V_S5 (5A)
SYSTEM DC/DC	
RT8209E	47
5V_S5	1D5V_S3 (1.4A)
RT9026	47
5V_S5	0D75_S3 (1.2A)
SYSTEM DC/DC	
RT8209E	48
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (1.1A)
RT9025	48
3D3V_S5	1D1V_S5 (1.4A)
RT9025	49
5V_S5	1D1V_VGA
RT9161	49
3D3V_S0	2D5V_S0 (200mA)
RT9025	49
1D5V_S3	1D05V_S0 (1.4A)
CHARGER	
BQ24745	50
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	18V 6.0A
	UP+5V
	5V 100mA
CPU DC/DC	
ISL6265AHR	45
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0
	0~1.55V 18A
	VDDNB
	0~1.55V 4A

Discrete Madison Hynix

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

File: **BLOCK DIAGRAM**

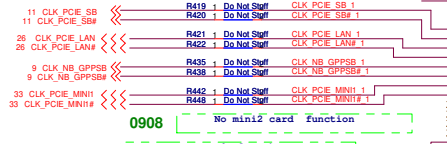
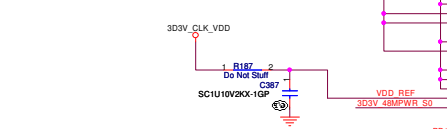
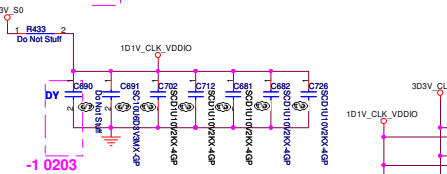
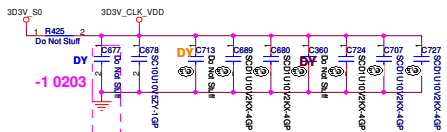
Size: A3 Document Number: JE40-DN Rev: -3

Date: Friday, March 26, 2010 Sheet: 1 of 85

Discrete Madison Hyrix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
History		
Size	Document Number	Rev
AS	JE40-DN	-3
Date:	Friday, March 26, 2010	Sheet 2 of 63

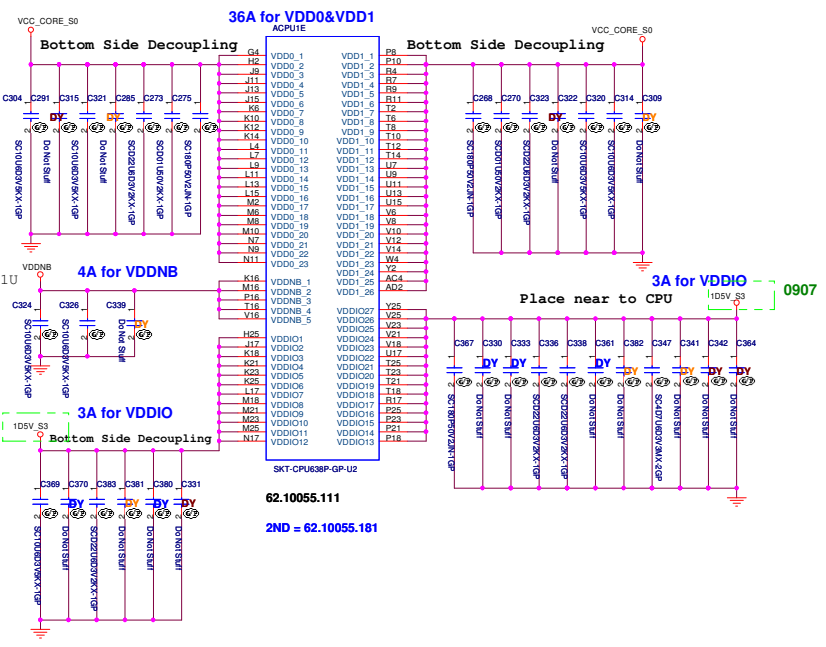


ACPUHF		
AA4	VSS1	VSS66
AA11	VSS7	J10
AA13	VSS3	J16
AA15	VSS5	J14
AA17	VSS4	VSS69
AA19	VSS6	J16
AB2	VSS7	J16
AB7	VSS8	VSS73
AB7	VSS8	VSS74
AB23	VSS9	K9
AB23	VSS9	VSS75
AB25	VSS11	VSS76
AC11	VSS12	K13
AC13	VSS13	VSS78
AC17	VSS14	VSS79
AC17	VSS15	VSS80
AC19	VSS16	L10
AC21	VSS17	K17
AD6	VSS18	VSS83
AD6	VSS18	VSS84
AD25	VSS19	L16
AE11	VSS20	L18
AE13	VSS21	M7
AE15	VSS23	M9
AE17	VSS25	AC6
AE19	VSS26	M17
AE21	VSS28	N4
AE23	VSS26	VSS92
B4	VSS28	VSS93
B8	VSS29	VSS94
B8	VSS29	VSS95
B8	VSS29	VSS96
B8	VSS29	VSS97
B11	VSS31	P7
B14	VSS32	P9
B15	VSS33	VSS98
B15	VSS34	VSS99
B17	VSS35	VSS100
B21	VSS36	R8
B21	VSS36	R10
B23	VSS37	VSS102
B26	VSS38	VSS103
B26	VSS38	VSS104
D6	VSS40	T7
D6	VSS41	VSS106
D9	VSS42	VSS107
D11	VSS43	VSS108
D13	VSS44	VSS109
D15	VSS45	VSS110
D17	VSS46	VSS111
D19	VSS47	VSS112
D21	VSS48	VSS113
D23	VSS49	VSS114
D25	VSS50	VSS115
E4	VSS51	VSS116
F2	VSS52	VSS117
F11	VSS53	VSS118
F16	VSS54	VSS119
F17	VSS55	VSS120
F21	VSS56	VSS121
F21	VSS56	VSS122
F23	VSS59	VSS123
F23	VSS59	VSS124
H7	VSS60	VSS125
H9	VSS61	VSS126
H9	VSS62	VSS127
H21	VSS63	VSS128
H23	VSS64	VSS129
J4	VSS65	VSS130

SKT-CPU638P-GP-U2

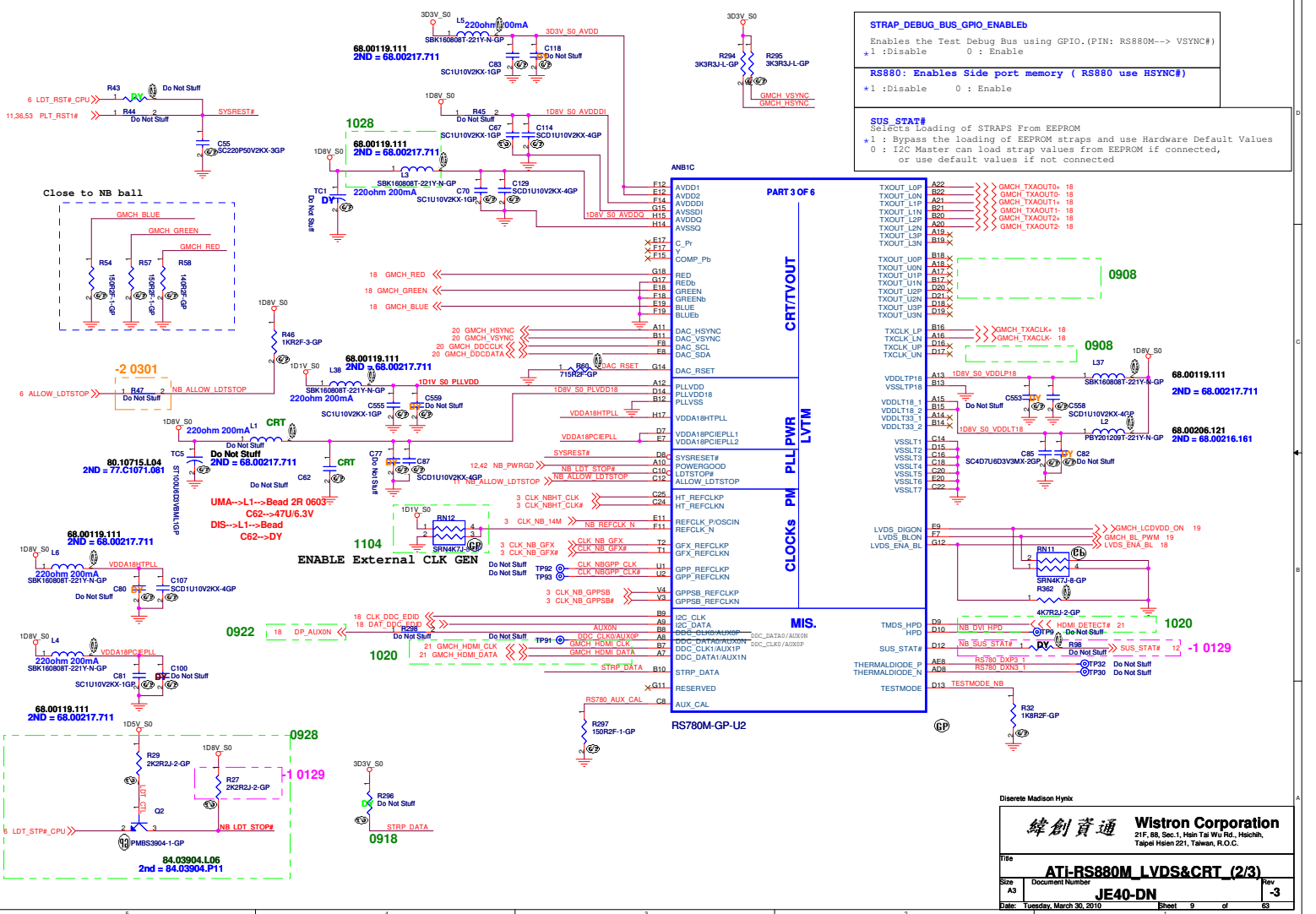
62.10055.111

2ND = 62.10055.181



Discrete Madison Hynix

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
File CPU_Power_(4/4)			
Size	Document Number	Rev	
A3	JE40-DN	-3	
Date:	Friday, March 26, 2010	Sheet	7 of 8



STRAP_DEBUG_BUS_GMIO_ENABLED
 Enables the Test Debug Bus using GPIO. (PIN: RS880M--> V5SYNC#)
 *1 : Disable 0 : Enable

RS880: Enables Side port memory (RS880 use H5SYNC#)
 *1 : Disable 0 : Enable

SUS_STAT#
 Selects Loading of STRAPS From EEPROM
 *1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected,
 or use default values if not connected

Discrete Madison Hynix

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsien 221, Taiwan, R.O.C.

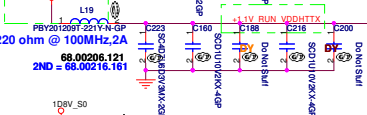
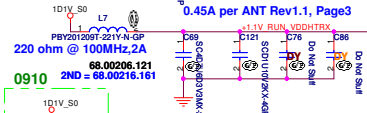
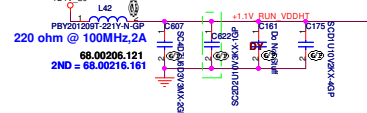
File: **ATI-RS880M LVDS&CRT (2/3)**

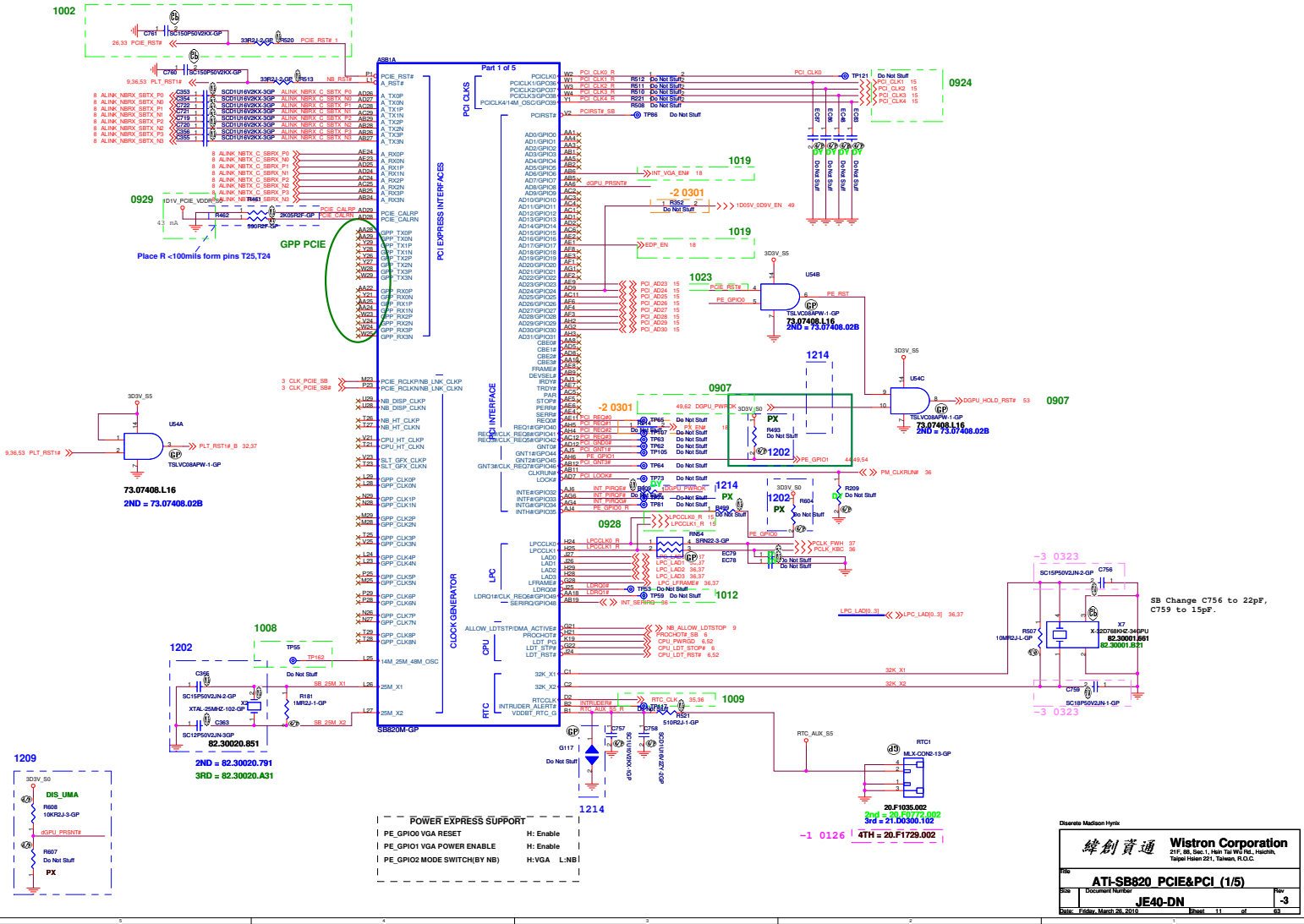
Size	Document Number	Rev
A3	JE40-DN	-3

Date: Tuesday, March 30, 2010 Sheet 9 of 95

1027 For AMD review request

0.6A per ANT Rev1.1, Page3





POWER EXPRESS SUPPORT

PE_GPI00 VGA RESET	H: Enable
PE_GPI01 VGA POWER ENABLE	H: Enable
PE_GPI02 MODE SWITCH(BY NB)	H:VGA L:NB

Discrete Madison Hynix

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Nan Tai Wu Rd., Hsinchu, Taipei Hsinchu 301, Taiwan, R.O.C.

ATI-SB820 PCIe&PCI (1/5)

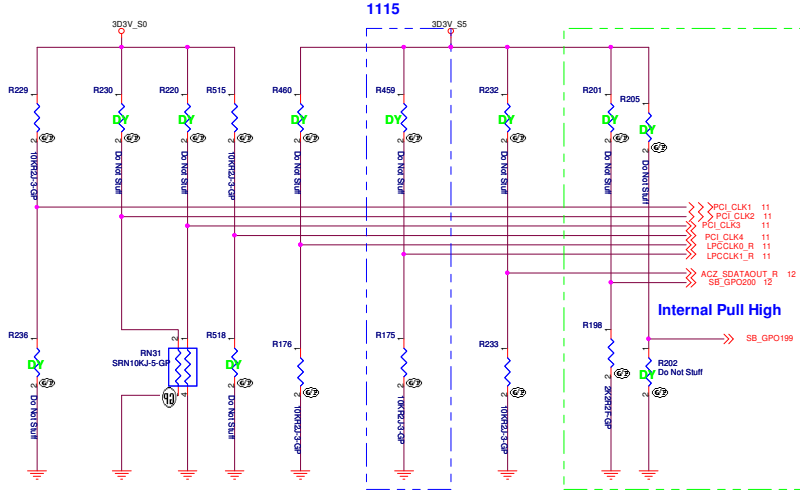
Doc. Document Number
JE40-DN

Rev. -3

Date: 11/26/2012 Issue: 11 of 53

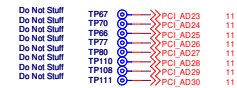
REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



1002

DEBUG STRAPS

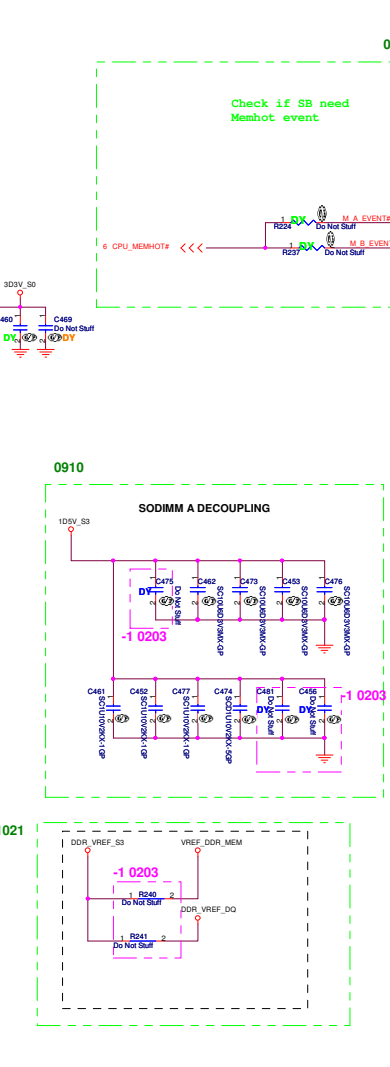
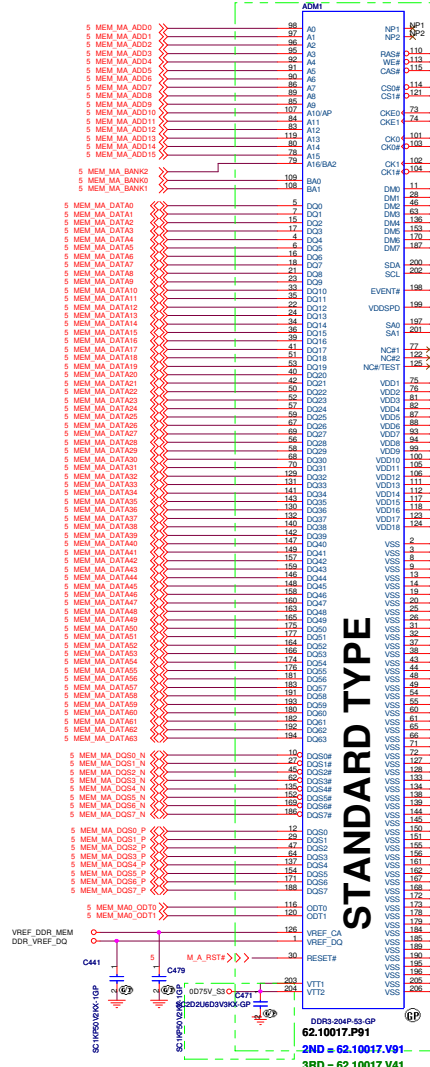


	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIe Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIe Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FW ROM	

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Discrete Madison Hynix

緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.</small>	
Title			
ATI-SB820 STRAPPING (5/5)			
Size	Document Number	Rev	
A3	JE40-DN		-3
Date:	Friday, March 26, 2010	Sheet	15 of 83



Discrete Madison Hynt:

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsinchu 301, Taiwan, R.O.C.

Rev: Custom

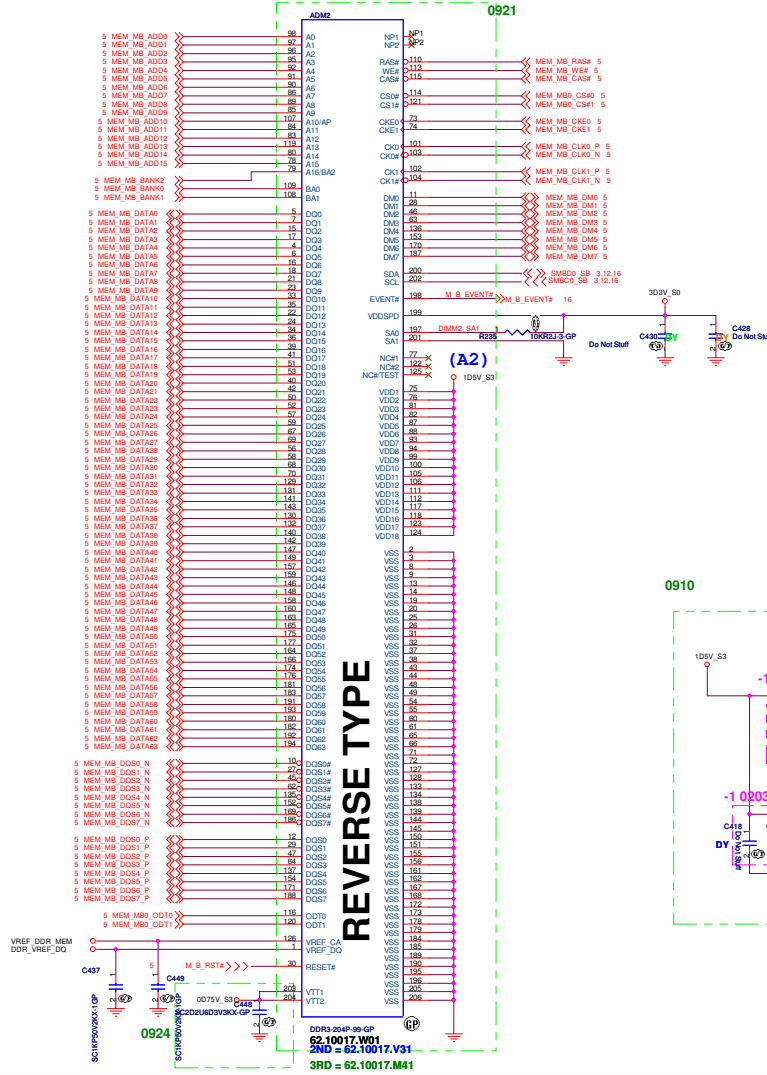
Document Number: **DDRIII SO-DIMM SKT 1**

JE40-DN

Date: Friday, March 26, 2010

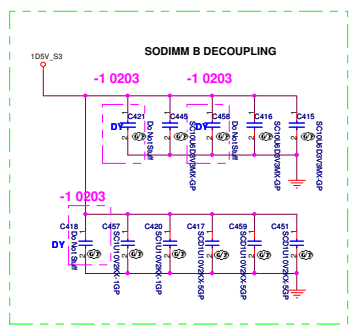
Sheet: 16 of 63

New: -3



1029

0910

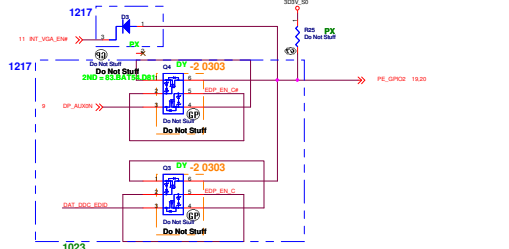
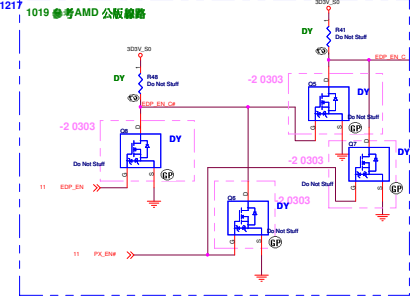


Discrete Madison Hyeix

緯創資通 **Wistron Corporation**

2/F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 301, Taiwan, R.O.C.

File	D8RIII SO-DIMM SKT_2		Rev
Doc	Document Number		-3
Case	JE40-DN		
Date	Friday, March 26, 2010	Sheet	17 of 83



LVDS Truth Table

Function	SEL
A _N to N _B 1	L
A _N to N _B 2	H

CRT Function Table

E	S	YA	YB	YC	YD	Function
H	X	H _{h-Z}	H _{h-Z}	H _{h-Z}	H _{h-Z}	Disable
L	L	IA0	IB0	IC0	ID0	S=0
L	H	IA1	IB1	IC1	ID1	S=1

EDID Function Table

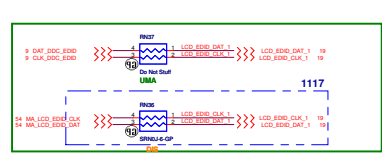
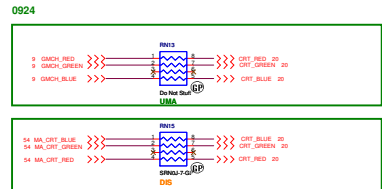
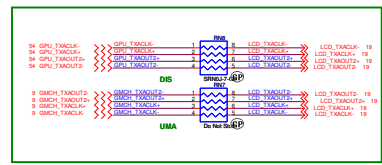
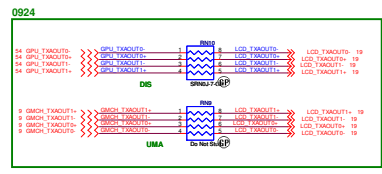
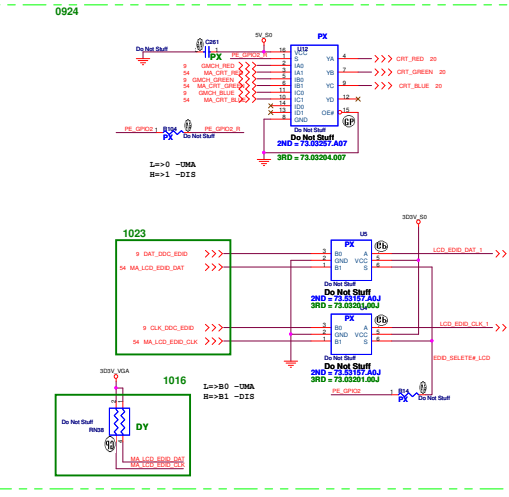
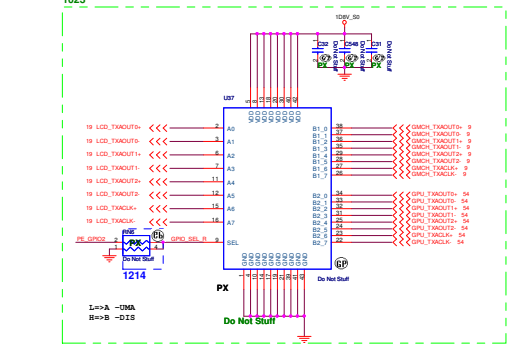
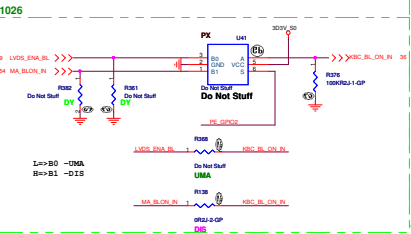
Input (B)	Function
L	B ₁ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level

BLON_IN Function Table

Input (B)	Function
L	B ₁ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level

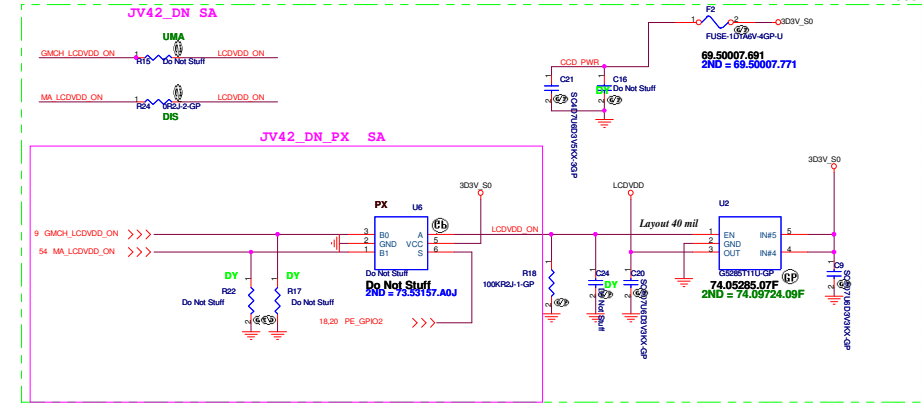
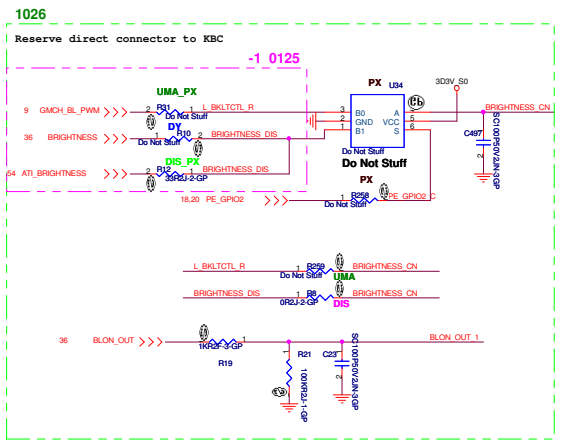
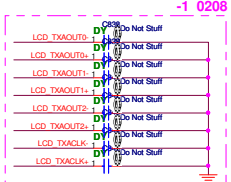
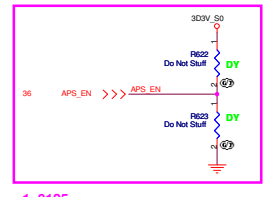
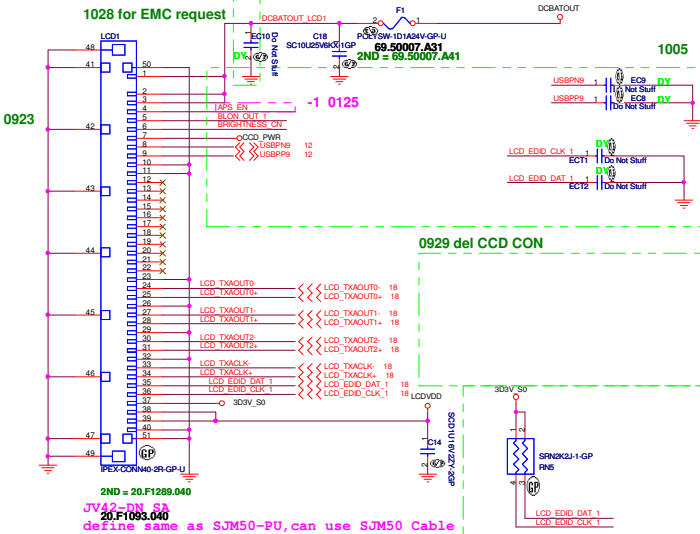


LCD/INVERTER/CCD CONN

Change PX
0922

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

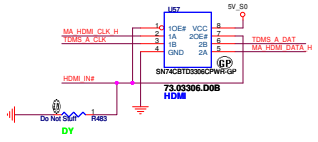
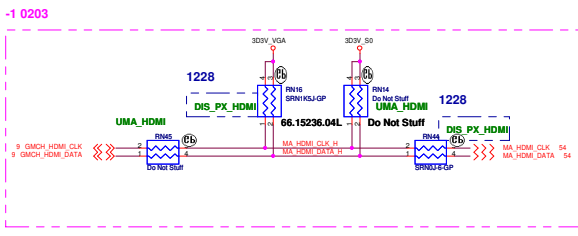
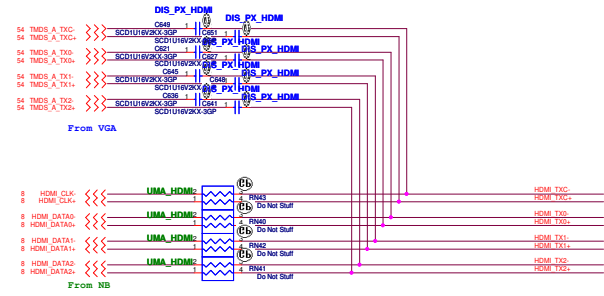
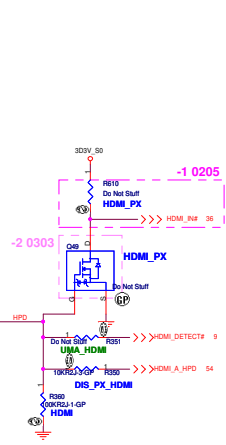
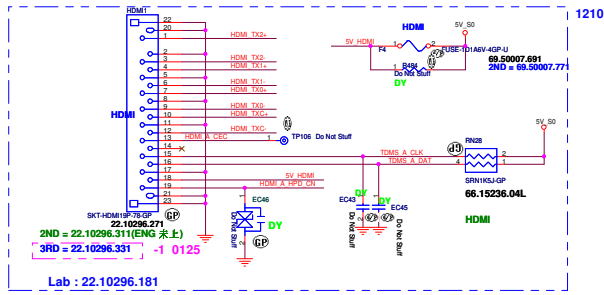
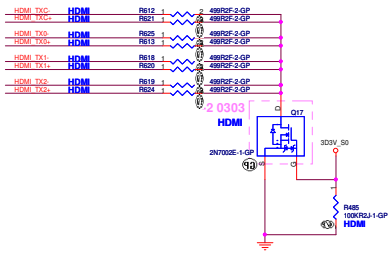
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



Discrete Medicon Hyink

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Ta Wu Rd., Hsinchu, Taipei Hsien 301, Taiwan, R.O.C.

File	LCD CONN	
Size	Document Number	Rev
Custom	JE40-DN	-3
Date:	Friday, March 26, 2010	Sheet 19 of 63



Discrete Medium Hybrid

緯創資通 Wistron Corporation

21F, 8th, Sec. 1, Hsin Tai Yeh Rd., Hsinchu, Taiwan, R.O.C.

File: **HDMI Connector**

Size: Document Number

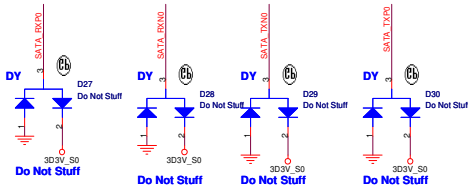
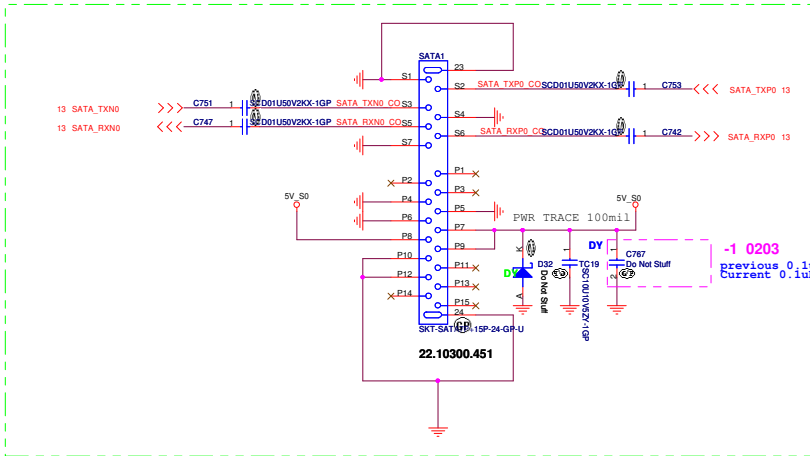
Rev: **JE40-DN**

Date: 15day March 26, 2015

Sheet: 1 of 3

SATA Connector

0923



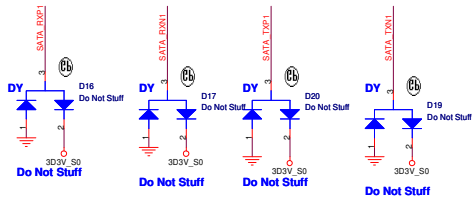
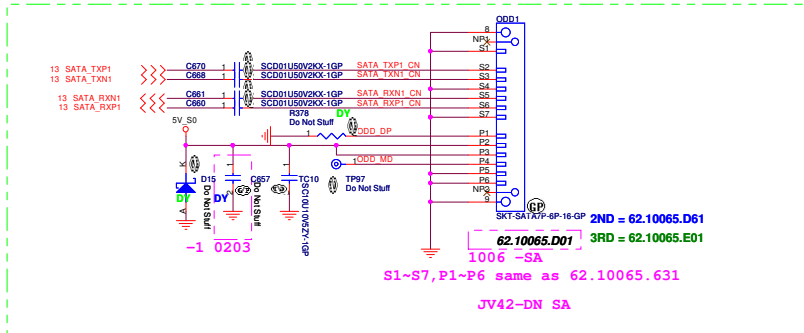
Discrete Madison Hynix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

File		HDD	
Size	Document Number	JE40-DN	
Date	Friday, March 26, 2010	Sheet	22 of 83
			Rev -3

ODD Connector

1009



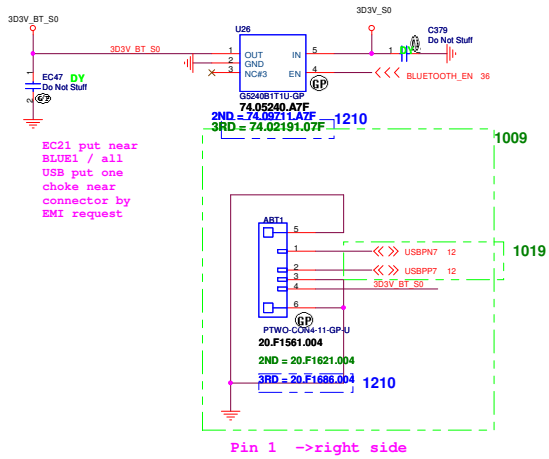
Discrete Madison Hyixix

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
 Taippei Hsien 221, Taiwan, R.O.C.

File		
ODD		
Size	Document Number	Rev
	JE40-DN	-3
Date:	Friday, March 26, 2010	Sheet 23 of 63

BLUETOOTH MODULE

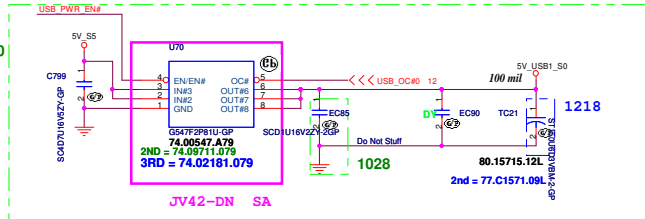
1.5A / High Active Voltage 2V



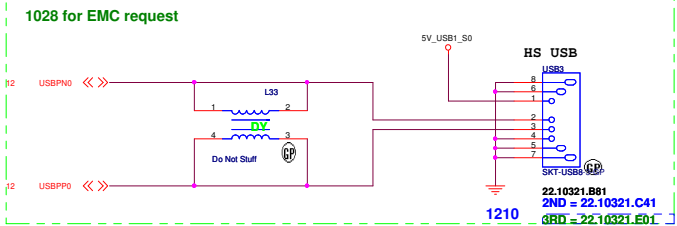
Discrete Madison Hylix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih,
Taipei Hsien 221, Taiwan, R.O.C.

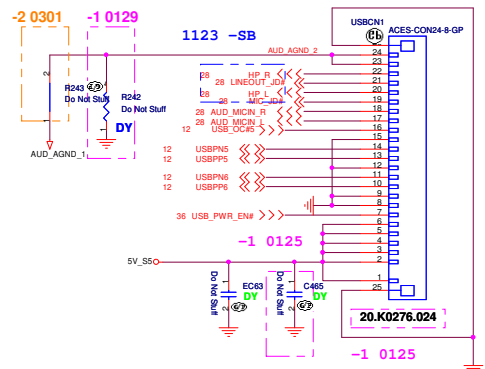
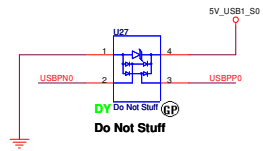
Title			BLUETOOTH
Size	Document Number	Rev	
	JE40-DN	-3	
Date: Friday, March 26, 2010	Sheet	24	of 63



0914



Pin1 -> right side
 22.10218.T51 Pin1 -> left side (JV42-DN)
 change Net sequence



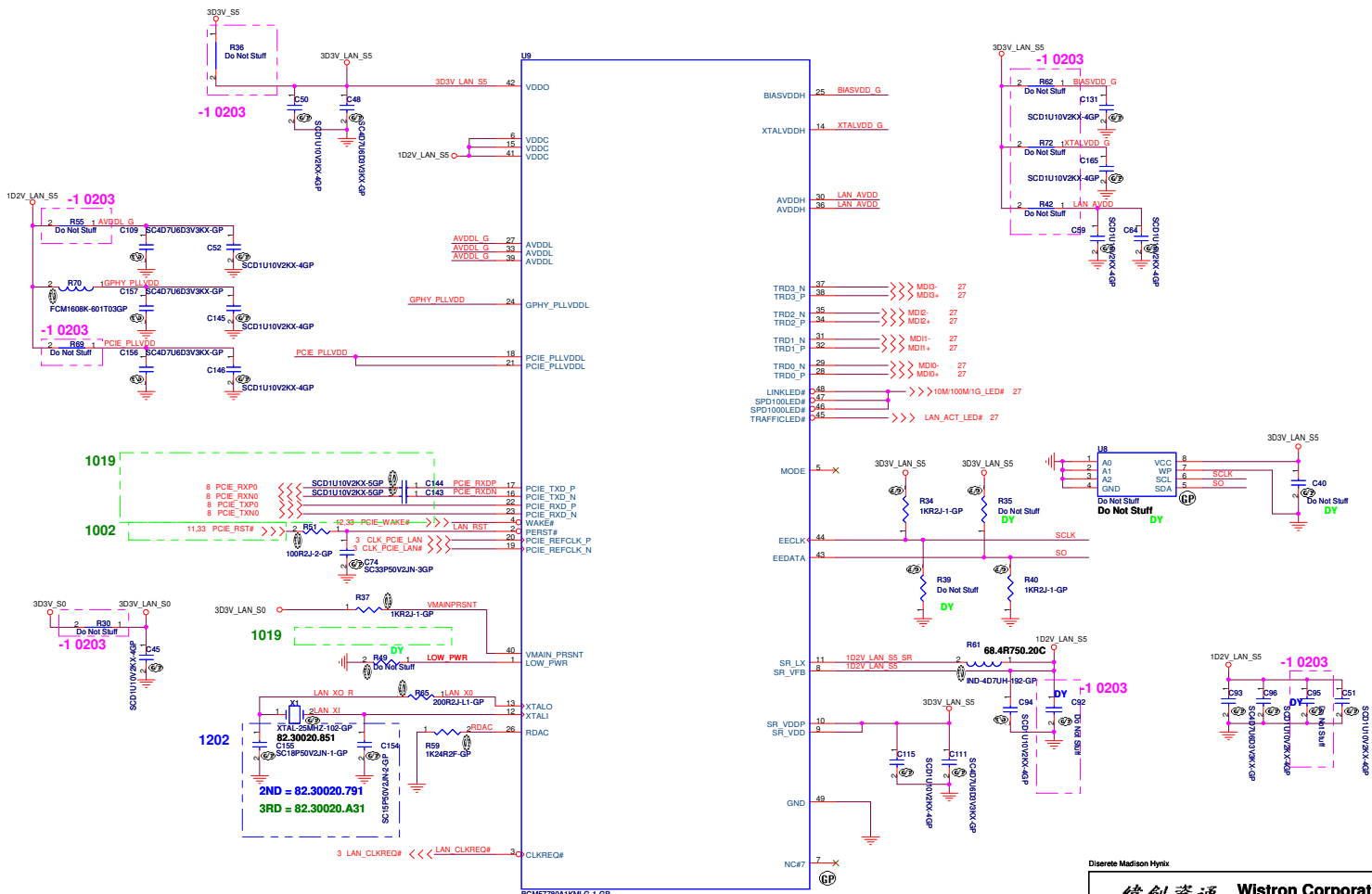
Eng stuff 20.K0216.024 Pin1 -> left side
 PD change to 20.K0276.024 Pin1 -> left side
 so do not swap net



0910

Discrete Madison Hyinx

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB			
File	Document Number		Rev
	JE40-DN		-3
Date:	Friday, March 26, 2010	Sheet	25 of 63



71.57780.M04

Discrete Madison Hyrax

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **BCM57780**

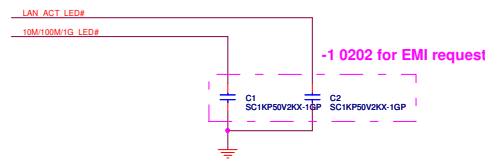
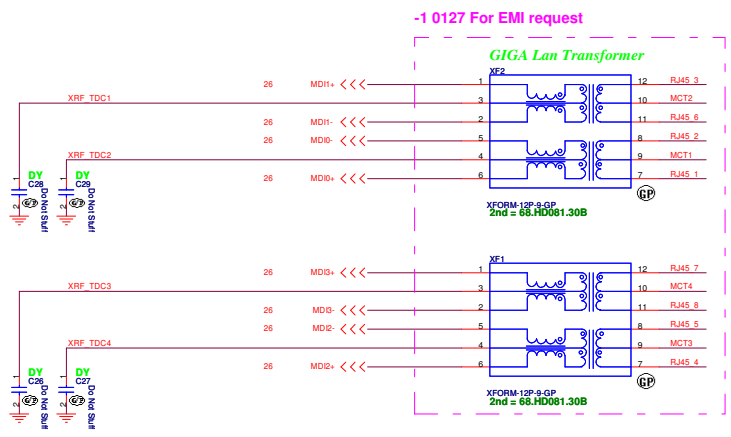
Size: **JE40-DN** Rev: **-3**

Date: Friday, March 26, 2010 Sheet 26 of 63

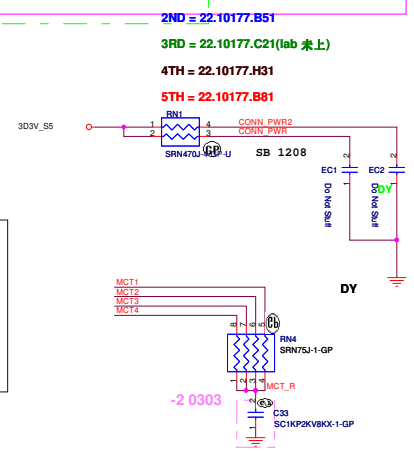
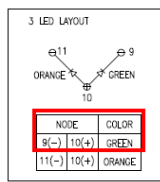
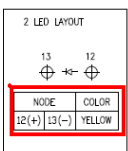
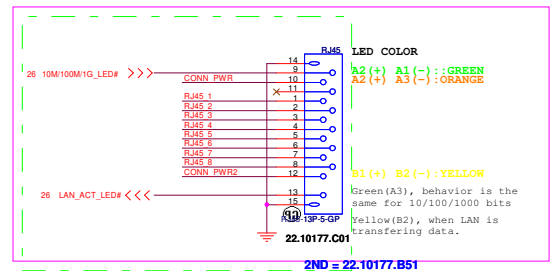
LAN Connector

LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



0923



Discrete Madison Hynix

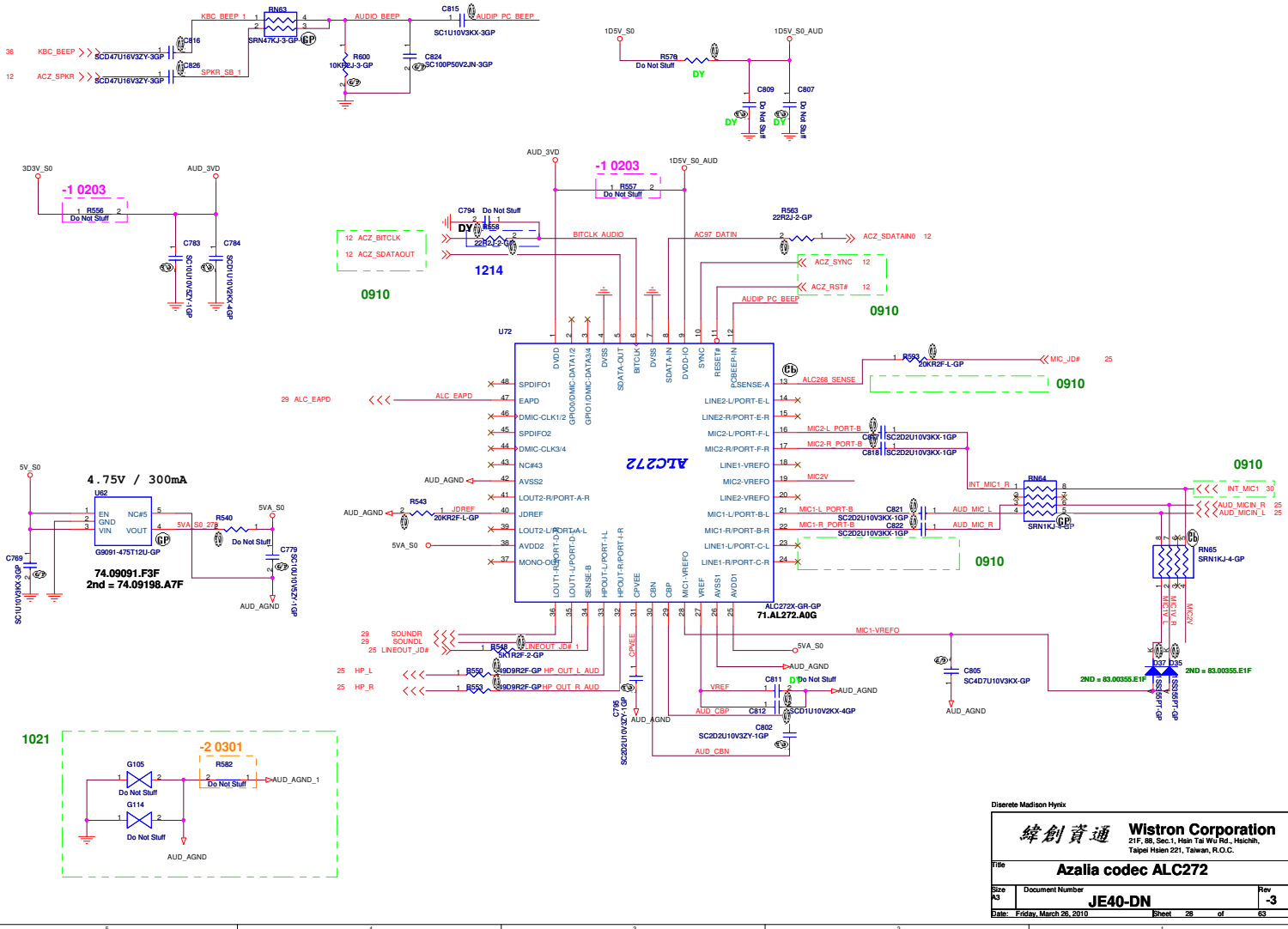
緯創資通 **Wistron Corporation**

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File **LAN CONN**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 27 of 30



Discrete Madison Hyrax

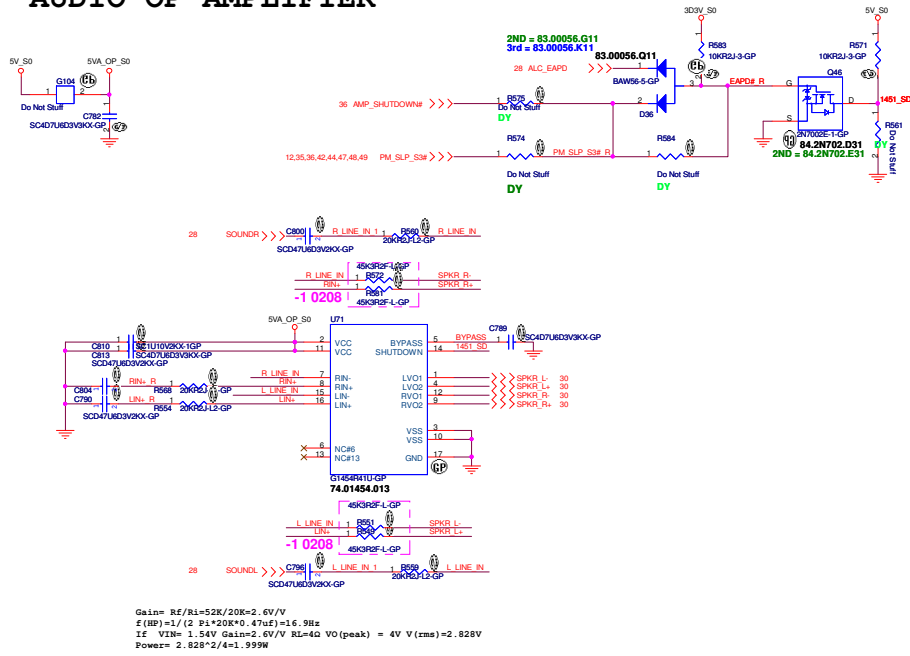
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File: **Azalia codec ALC272**

Size: A3 Document Number: **JE40-DN** Rev: **-3**

Date: Friday, March 26, 2010 Sheet: 26 of 63

AUDIO OP AMPLIFIER



Discrete Medium Hybrid

緯創資通

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Heichih,
 Taipei Hsin 221, Taiwan, R.O.C.

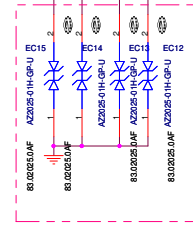
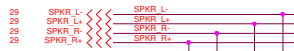
AUDIO AMP		Rev
Doc	Document Number	-3
JE40-DN		
Date:	Friday, March 26, 2010	Sheet 29 of 63

Internal Speaker

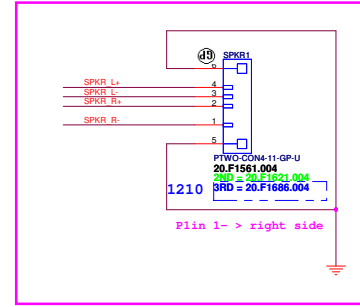
0914



0910



-1 0125 for EMI request

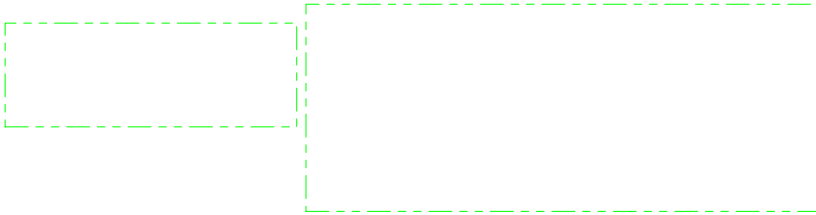


Pin 1 -> right side

JV42-DN SA

LINE OUT

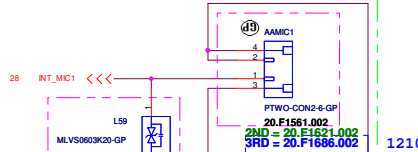
0911



0910

1016

Internal Mic



-1 0209 For MIC issue

JV42-DN PX

Pin 1 ->right side

20.F1240.002 Pin1->left side

same as JV70-CP

Discrete Madison Hyrax

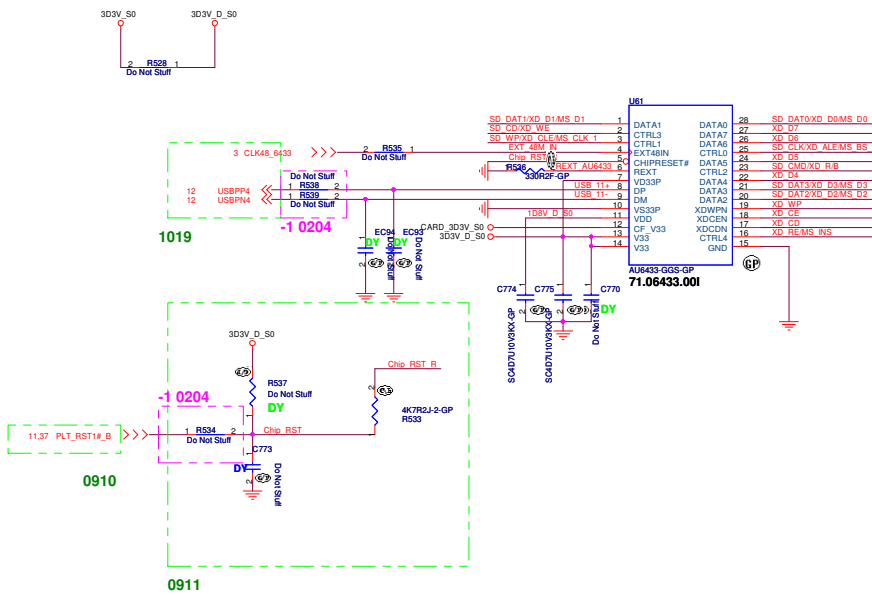
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.

File			
Size			Rev
Date: Friday, March 26, 2010			Sheet 30 of 63
AUDIO JACK JE40-DN			-3

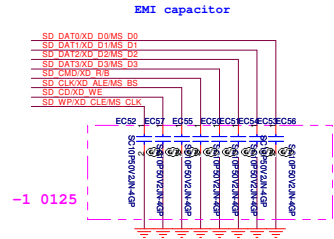
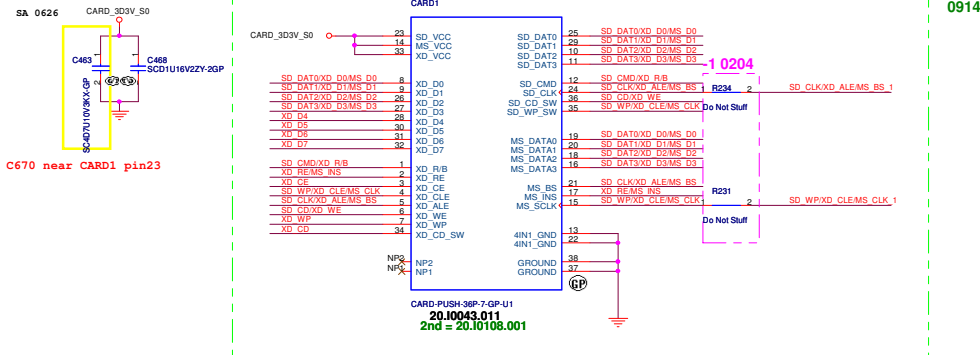
No Modem Function

Discrete Madison Hyrix

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		MDC	
Size	Document Number		Rev
	JE40-DN		-3
Date:	Friday, March 26, 2010	Sheet	31 of 63



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Discrete Madison Hybrx

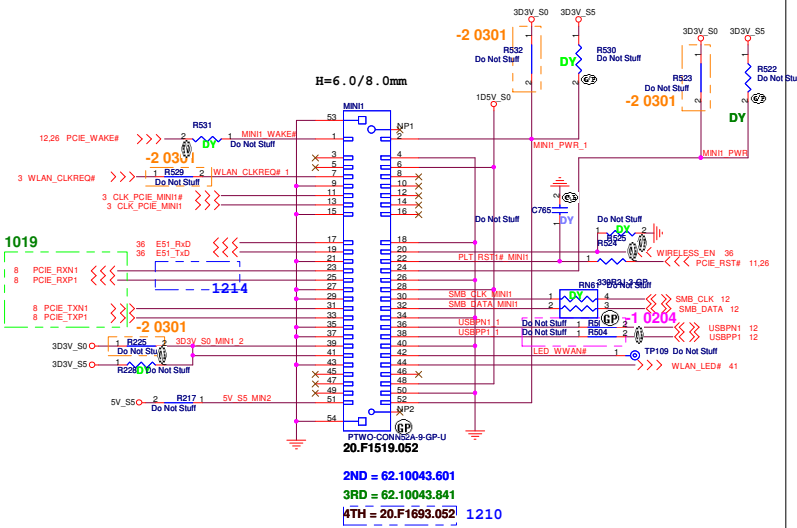
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 321, Taiwan, R.O.C.

Title: **CARDREADER**
Size: Document Number: **JE40-DN** Rev: **-3**
Date: Friday, March 26, 2010 Sheet 32 of 83

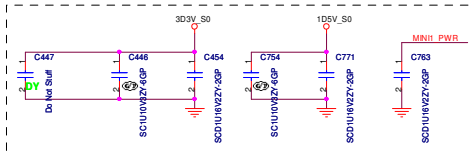
Mini Card Connector(WLAN)

No Mini Card Function (Robson2 and 3G)

0923



Place near MINI1



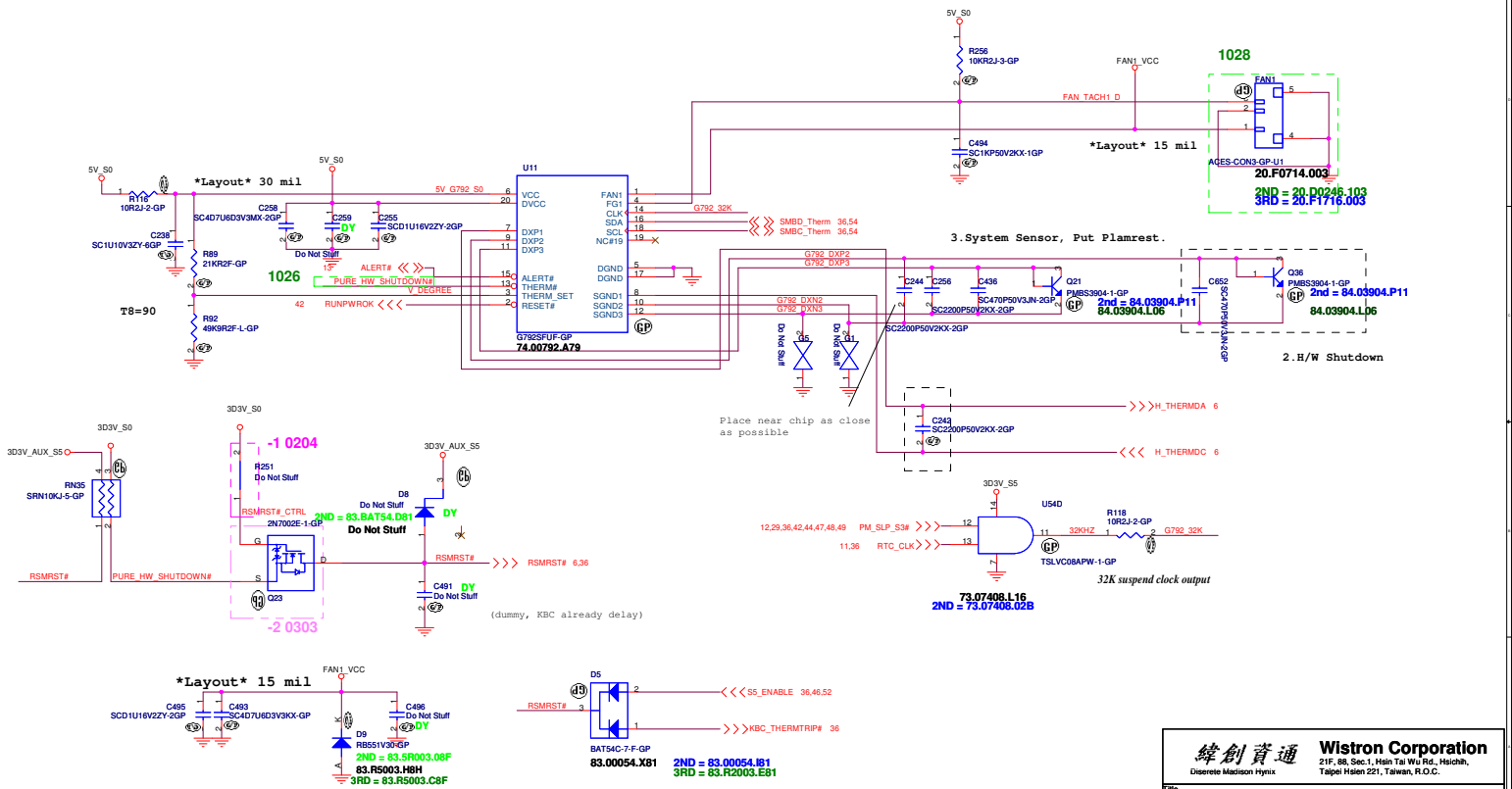
Discrete Madison Hynix

		Wistron Corporation 21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
File			
MINI CARD			
Size	Document Number	Rev	-3
JE40-DN			
Date:	Friday, March 26, 2010	Sheet	33 of 63

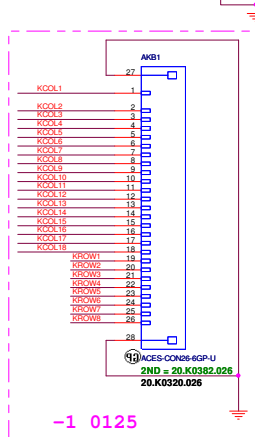
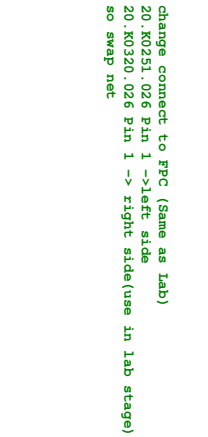
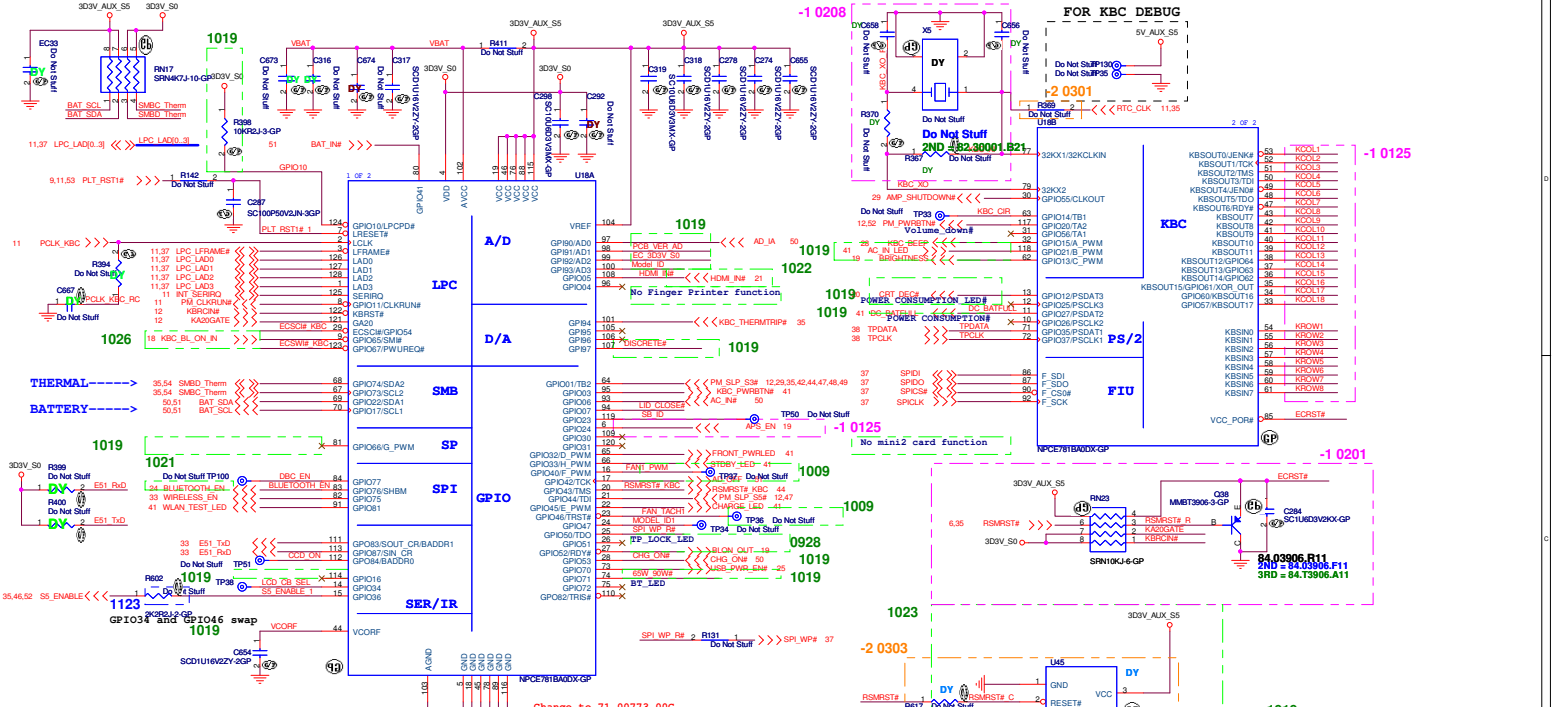
No NEWCARD Function

Discrete Madison Hynix

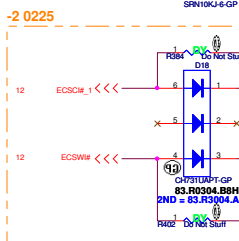
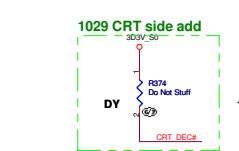
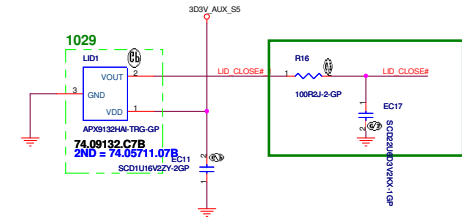
緯創資通		Wistron Corporation	
<small>21F, 88, Sec. 1, Hsin Tsai Wu Rd., Hsinchu, Taippei Hsien 321, Taiwan, R.O.C.</small>		<small>21F, 88, Sec. 1, Hsin Tsai Wu Rd., Hsinchu, Taippei Hsien 321, Taiwan, R.O.C.</small>	
NEW CARD			
Size	Document Number	Rev	
	JE40-DN	-3	
Date:	Friday, March 26, 2010	Sheet	34 of 63



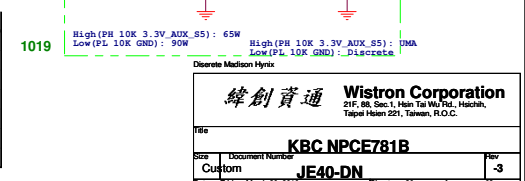
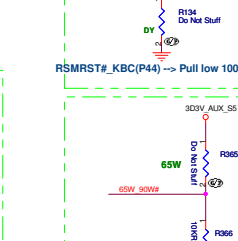
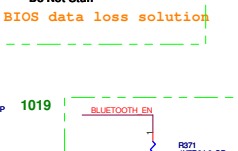
緯創資通 <small>Discrete Madison Hynix</small>		Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
File	Document Number	JE40-DN	
Site	Custom	Rev -3	
Date: Tuesday, March 30, 2010	Sheet	35	of 83



LID SWITCH



Pull-High Resistor (303V_AUX_S5)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V



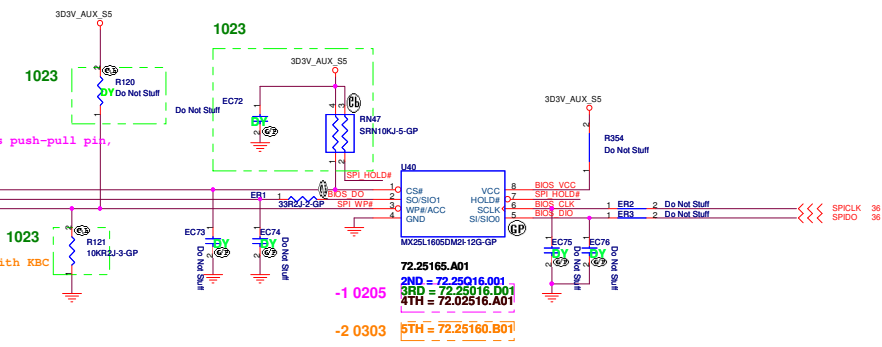
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Doc No: **KBC NPCE781B**
 Rev: **JE40-DN**

Date: Friday, March 26, 2010 Sheet: 36 of 63

for ENE FAE suggest, SPICS# is push-pull pin,
don't need to pull high

base on FAE Kevin discuss with KBC

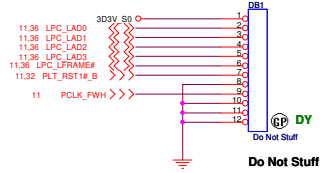


3rd 4th source LAB ENG未上

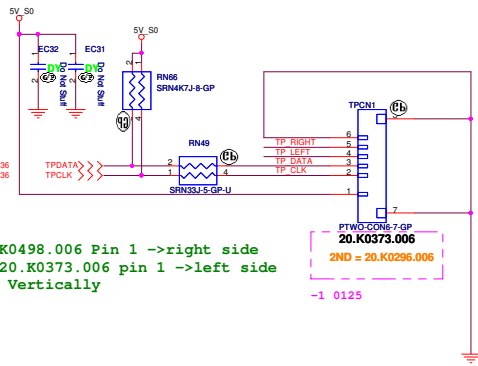
16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD

11.36 LPC_LAD[0..3] <<> LPC LAD[0..3]

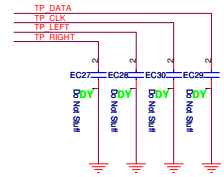


Discrete Madison Hynix		
緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.		
File		
BIOS		
Size	Document Number	Rev
A3	JE40-DN	-3
Date:	Friday, March 26, 2010	Sheet 37 of 83

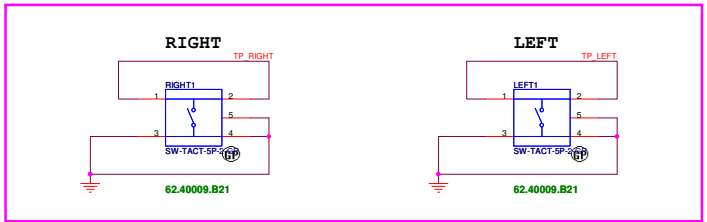


Eng stuff 20.K0498.006 Pin 1 -->right side
 PD change to 20.K0373.006 pin 1 -->left side
 so net mirror Vertically

PTWO-CON6-7-GP
 20.K0373.006
 2ND = 20.K0296.006
 -1 0125



-1 0205



No Finger printer Function

Discrete Madison Hynix

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsien 221, Taiwan, R.O.C.

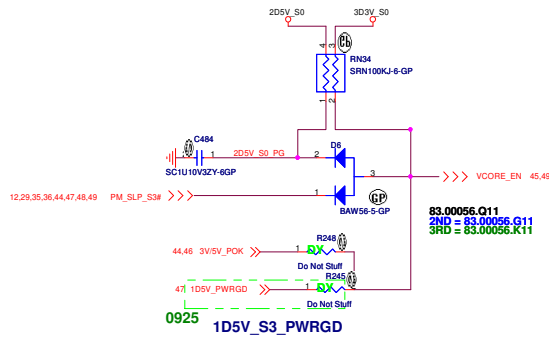
Title			Touch PAD		
Size	Document Number	Rev			
A3	JE40-DN	-3			
Date:	Friday, March 26, 2010	Sheet	38	of	63

NONE BOARD

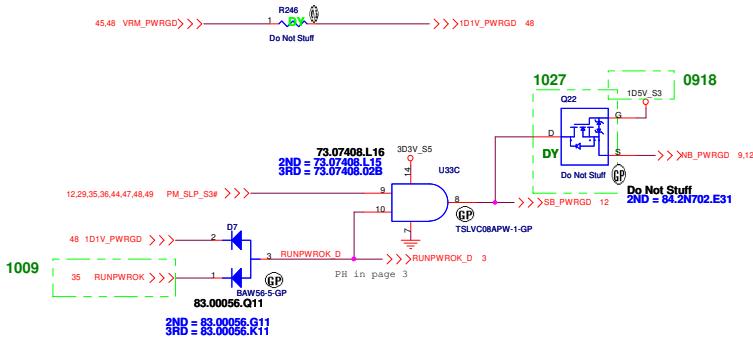
緯創資通		Wistron Corporation	
<small>21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		<small>21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
File			
NONE BOARD			
Size	Document Number	Rev	Rev
A3	JE40-DN		-3
Date	Friday, March 26, 2010	Sheet	39 of 63

緯創資通 **Wistron Corporation**
23F, 88, Sec. 1, Hsin-Tai Rd., Hsinshu,
Taichung 401, Taiwan, R.O.C.

Rev. _____
Document Number: **SWITCH** Rev. _____
A2 **JE40-DN** Rev. **-3**
Date: Friday, March 28, 2008 Sheet: 01 of 03



P/H @ 1D8V_S3 PAGE



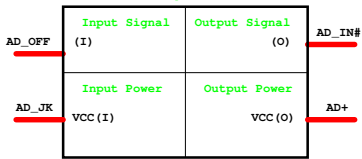
Discrete Madison Hynix

緯創資通

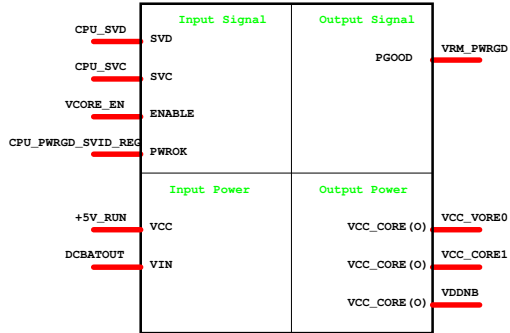
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		POWER ON LOGIC	
Size	Document Number	Rev	
A3	JE40-DN	-3	
Date:	Friday, March 26, 2010	Sheet	42 of 50

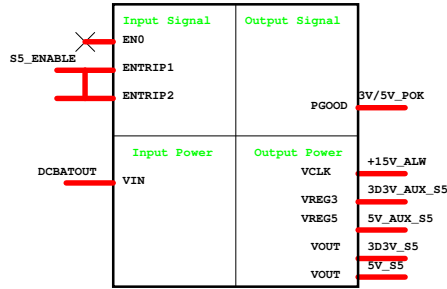
Adapter



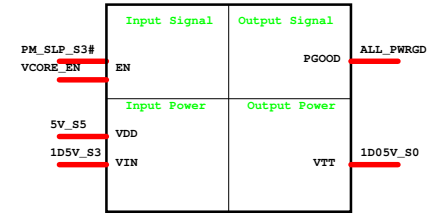
CPU_CORE ISL6265HRTZ



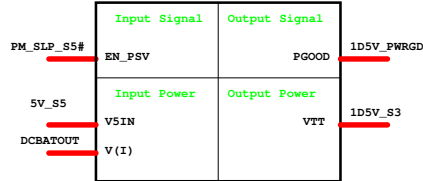
DCDC 5V/3D3V(RT8223)



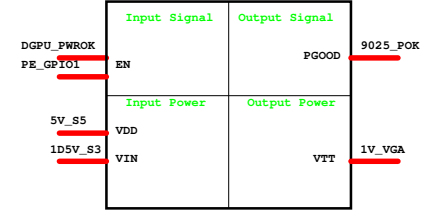
DCDC 1D05V_S0(RT9025)



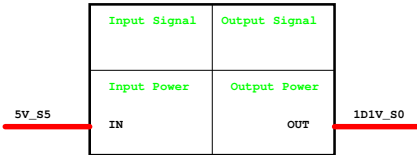
DCDC 1D5V(RT8209E)



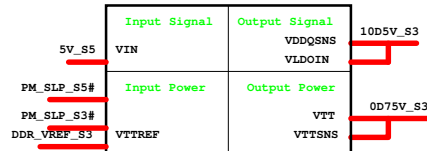
DCDC 1V_VGA(RT9025)



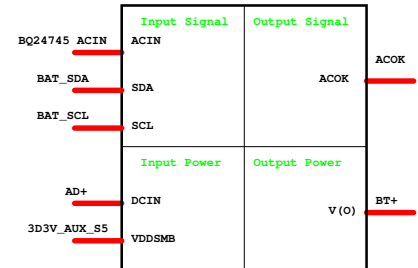
1D1V LDO RT8209E



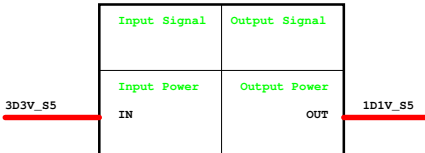
0D75V LDO RT9026



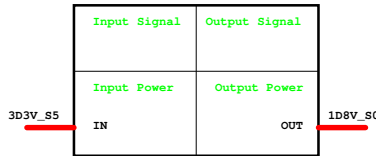
CHARGER BQ24745



1D1V LDO RT9025



1D8V LDO RT8015A



Discrete Madison Hynix

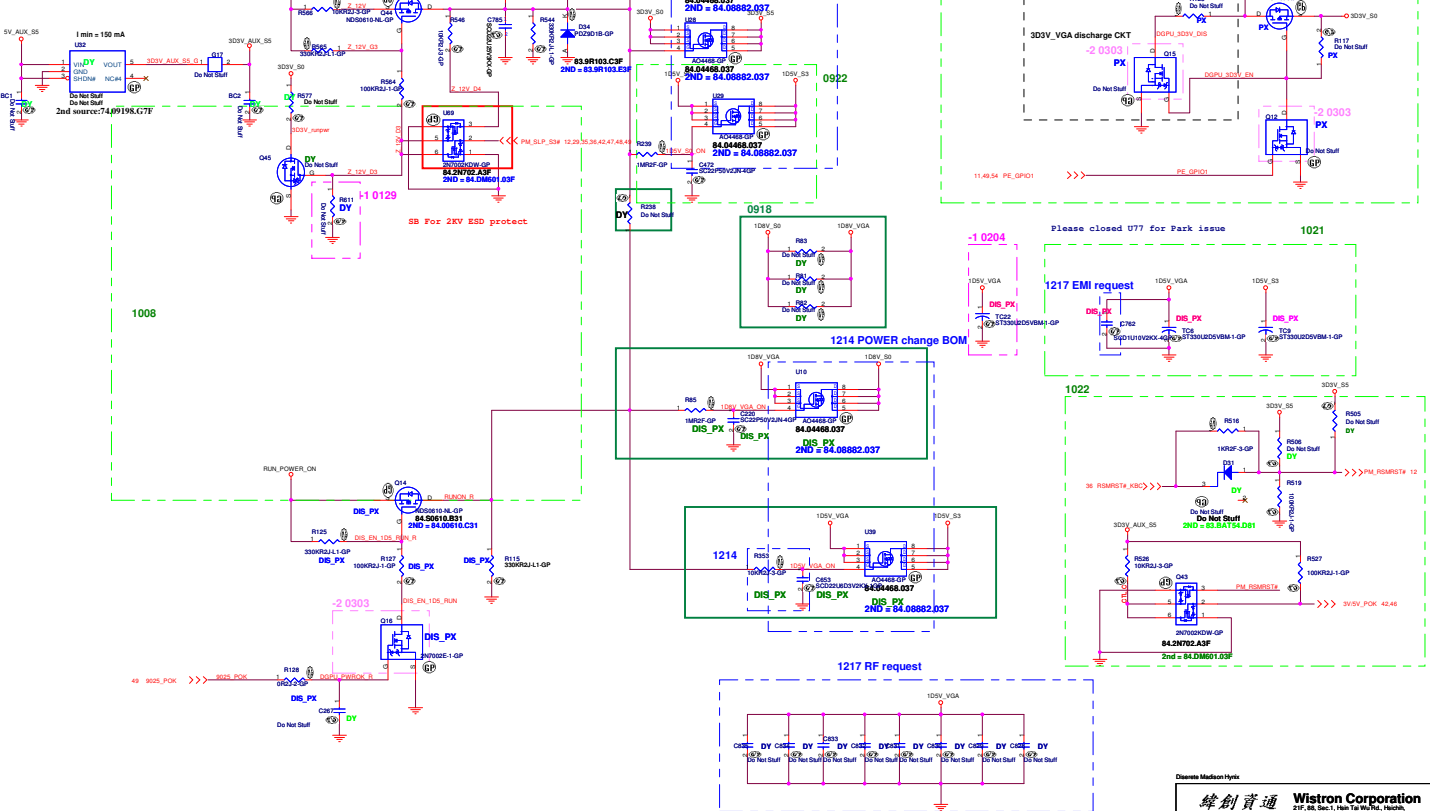
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 221, Taiwan, R.O.C.

File			Power Block Diagram		
Size	Document Number	Rev			
A3	JE40-DN	-3			
Date:	Friday, March 26, 2010	Sheet	43	of	83

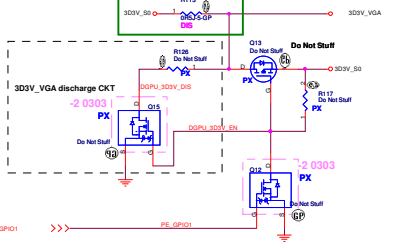
Run Power

Aux Power

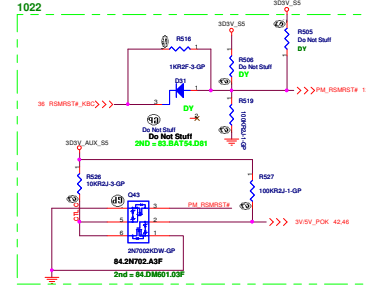
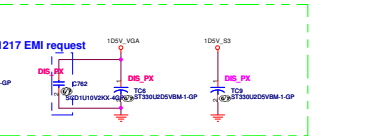
3D3V_AUX_S5



+3VS to 3.3V_DELAY Transfer



Please closed U77 for Park issue



Discrete Medium-Hybrid

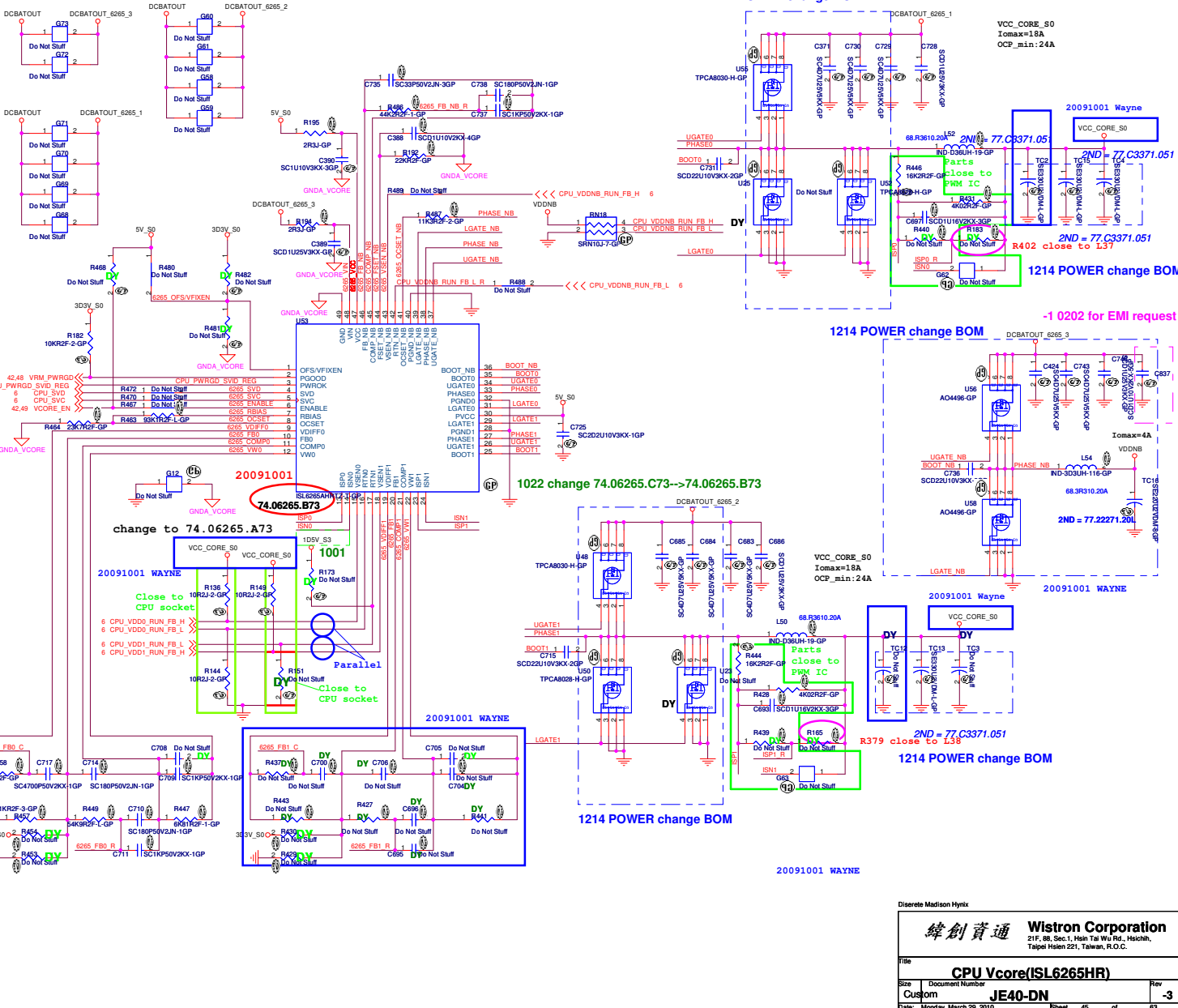
緯創資通 Wistron Corporation
235, Sec. 5, Keelung Rd., Keelung, Taiwan, R.O.C.

Doc. No. **RUN AND AUX POWER**

Rev. **Custom JE40-DN**

Doc. Format: March 28, 2012

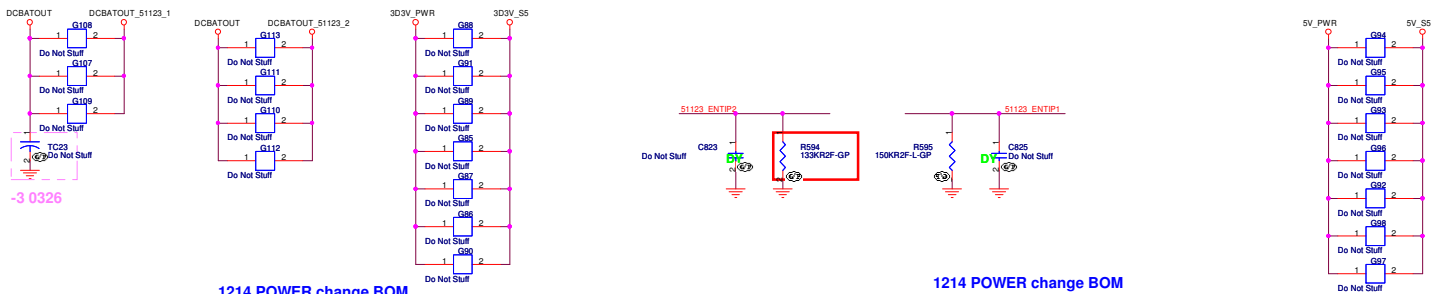
1214 POWER change BOM



Discrete Madison Hynix

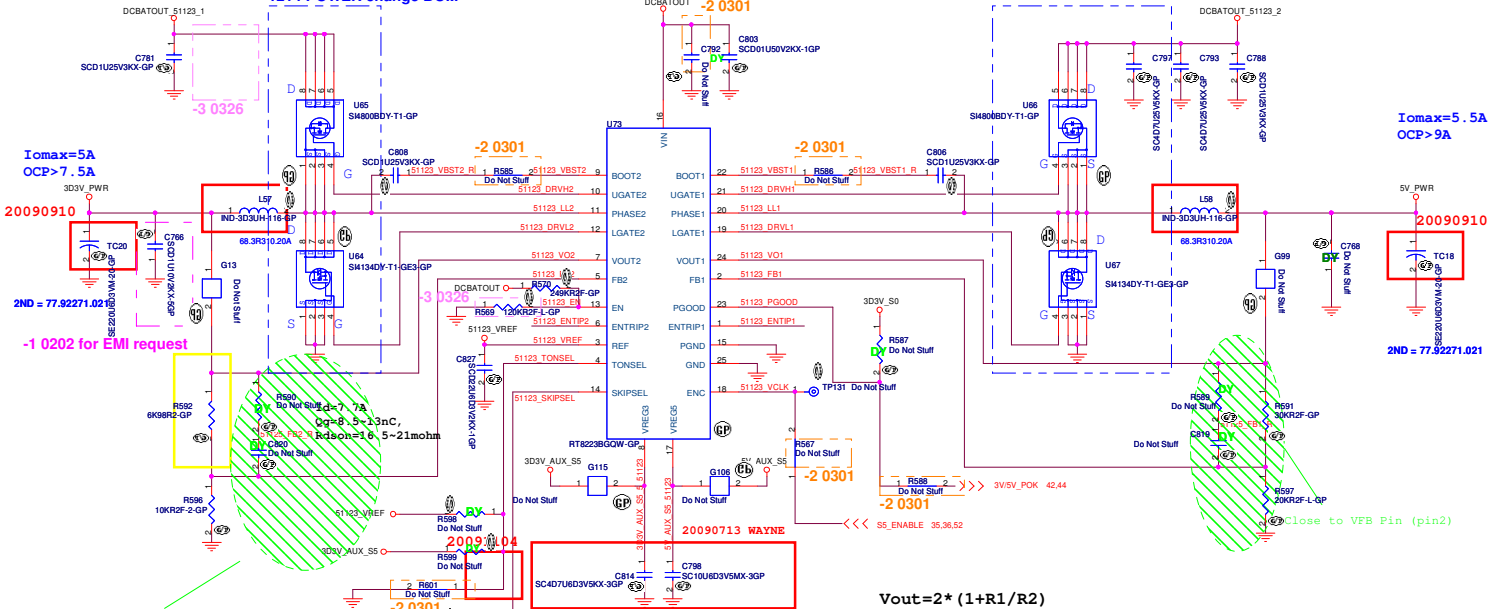
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinshih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU Vcore(ISL6265HR)	
Size	Document Number	Rev
Custom	JE40-DN	3
Date:	Monday, March 29, 2010	Sheet 45 of 53



1214 POWER change BOM

1214 POWER change BOM



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

Discrete Madison Hynix

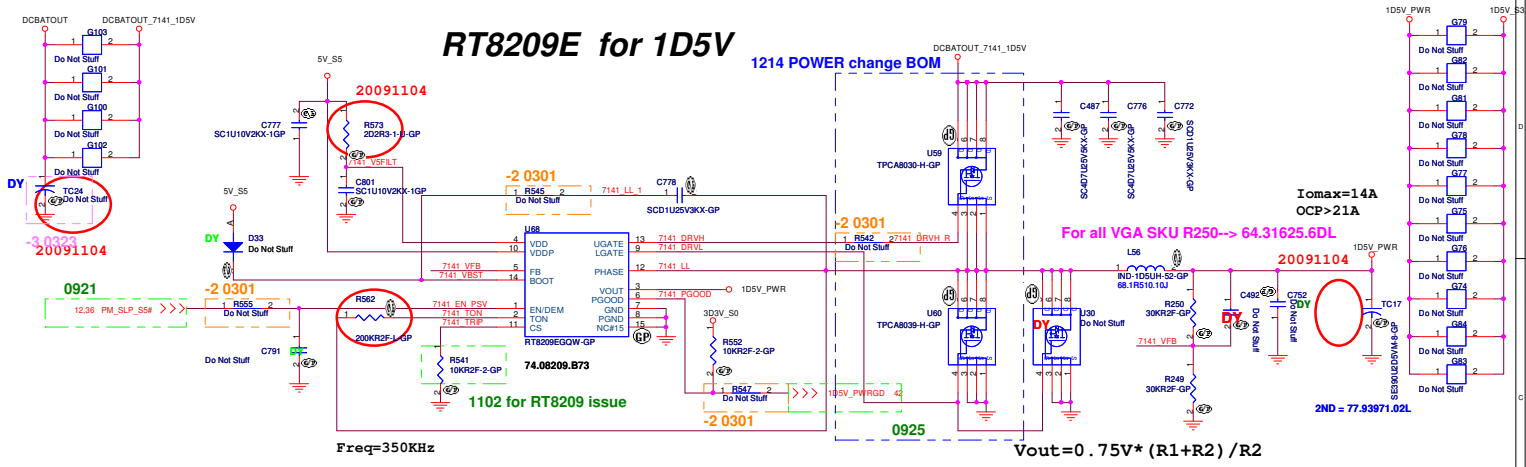
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsinchu, Taipei Hsin 321, Taiwan, R.O.C.

File: **RT8223 5V/3D3V**

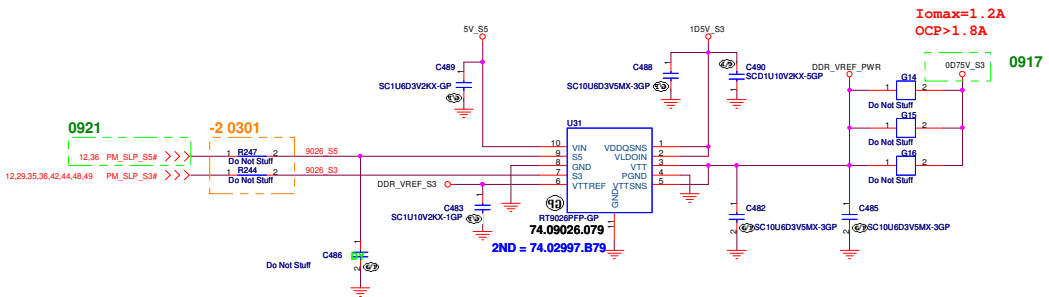
Size: Document Number **JE40-DN** Rev **-3**

Date: Monday, March 29, 2010 Sheet 46 of 63

RT8209E for 1D5V



RT9026 for 0D75V_S3



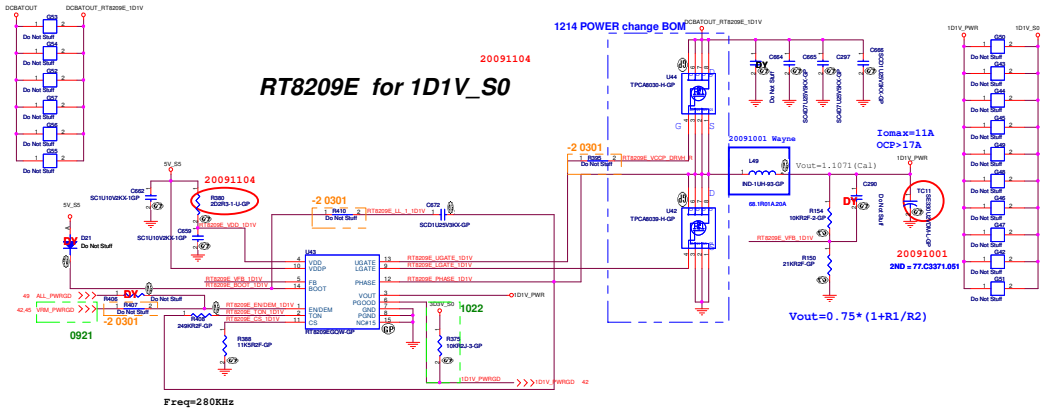
Discrete Madison Hytek

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

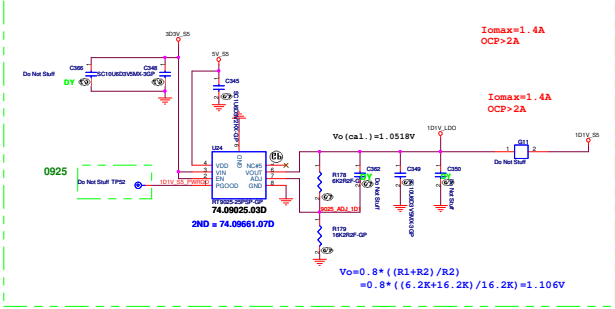
RT8209E 1D5V		
File	Document Number	Rev
	JE40-DN	-3
Date: Monday, March 29, 2010	Sheet: 47	of 63

0917

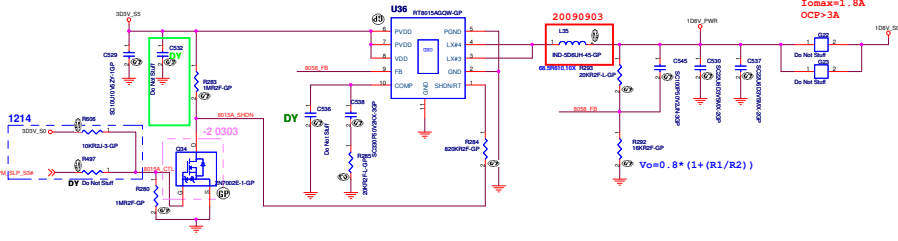
20091104 RT209E for 1D1V_S0



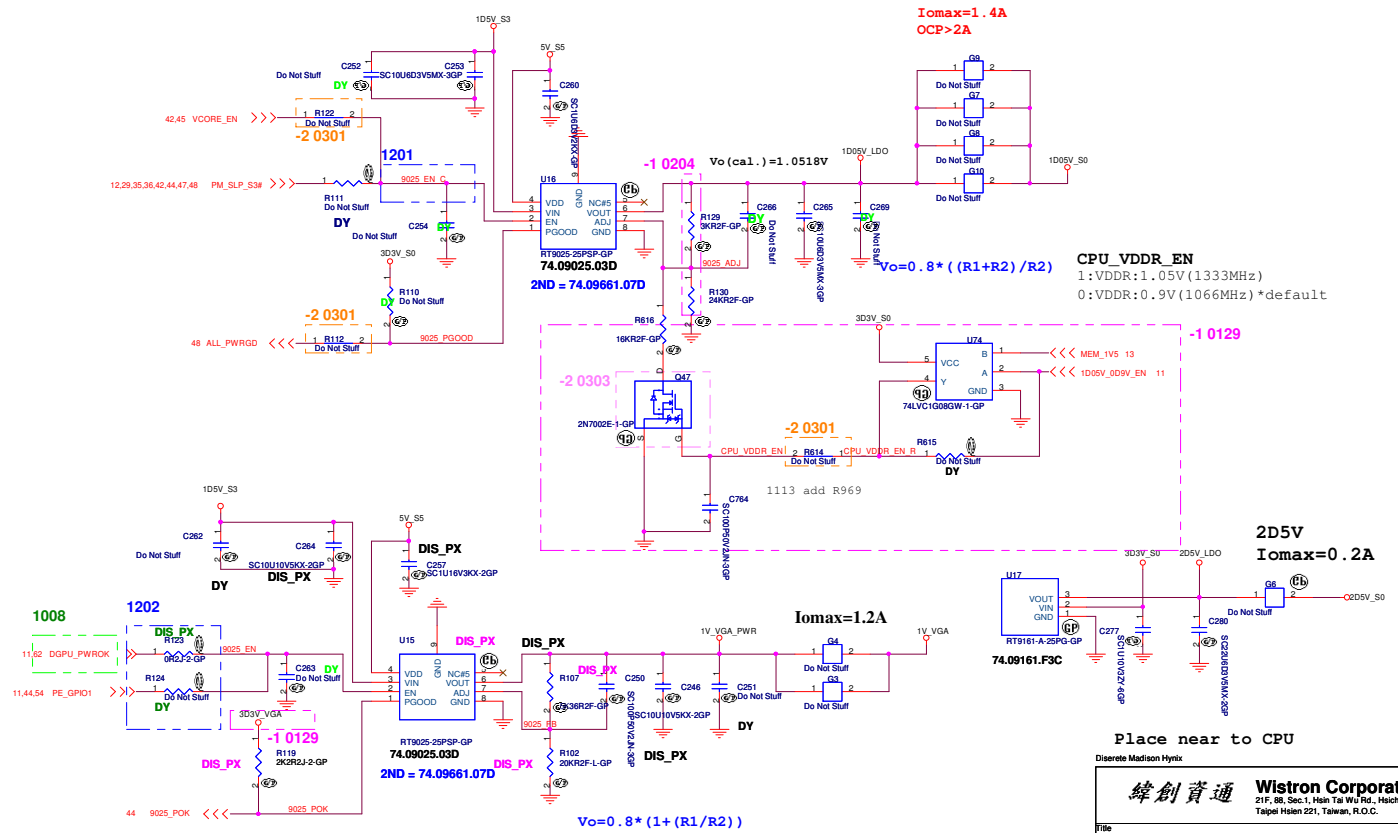
0921 RT9025 for 1D1V_S5



RT8015A for 1D8V_S0



RT9025 for 1D05V_S0

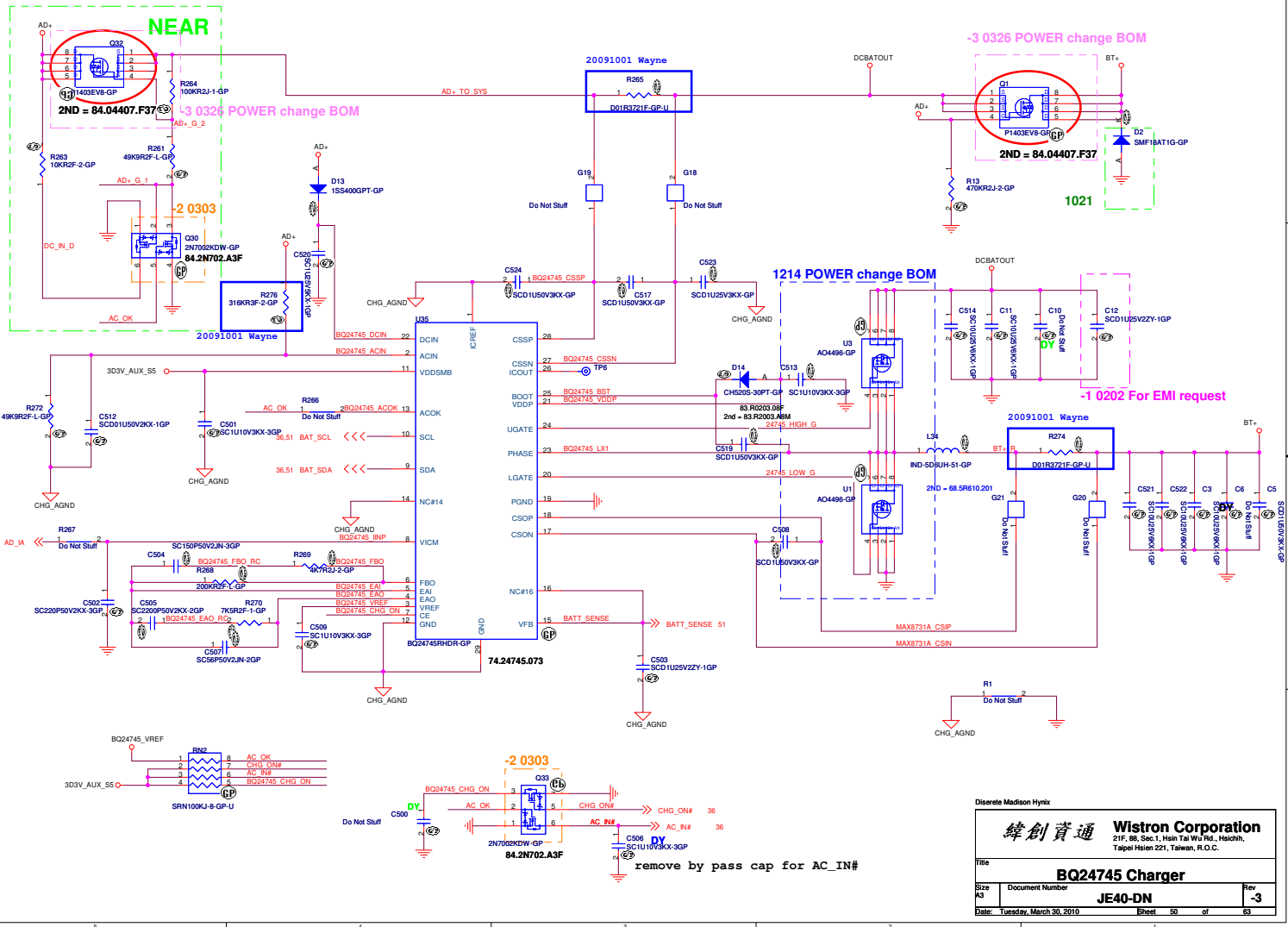


Place near to CPU

Discrete Madison Hynix

緯創資通 **Wistron Corporation**
 21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File	LDO 1D05V/2D5V/1V		Rev
Size	Document Number	JE40-DN	
A3			-3
Date:	Friday, March 26, 2010	Sheet	49 of 63



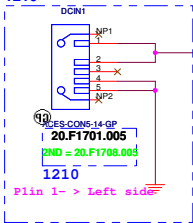
Discrete Madison Hynix

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 321, Taiwan, R.O.C.

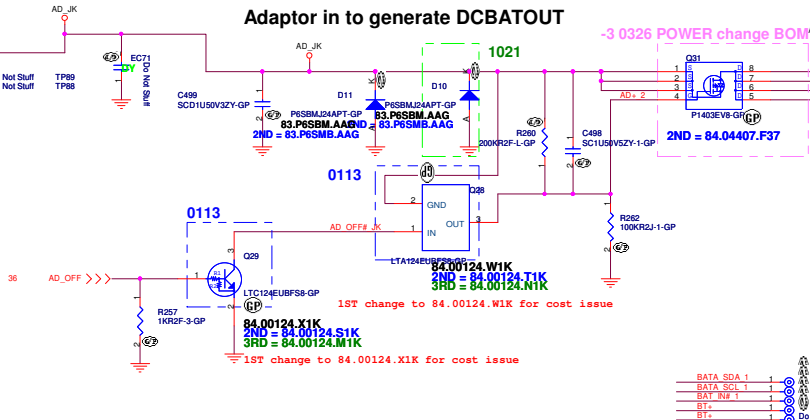
BQ24745 Charger

Title		
Size A3	Document Number	Rev -3
Date: Tuesday, March 30, 2010		Sheet 50 of 63

1210



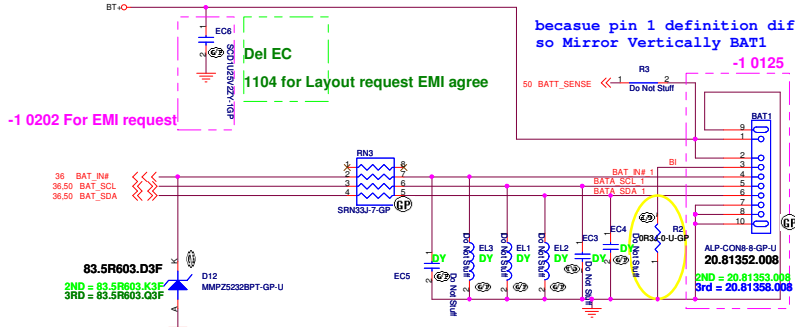
Adaptor in to generate DCBATOUT



Pin Definition

BATA_SDA_1	1	Do Not Stuff	TP2
BATA_SCL_1	1	Do Not Stuff	TP1
BAT_INF_1	1	Do Not Stuff	TP3
BI+	1	Do Not Stuff	TP5
BI-	1	Do Not Stuff	TP4

BATTERY CONNECTOR



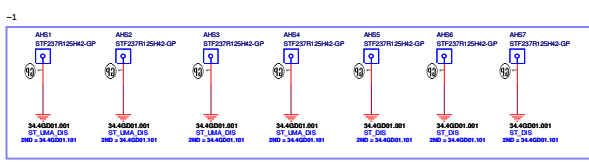
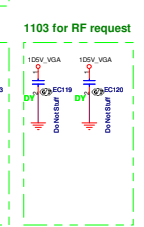
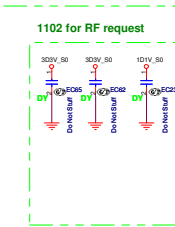
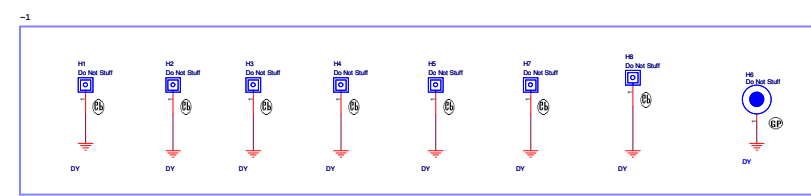
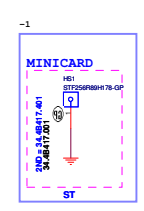
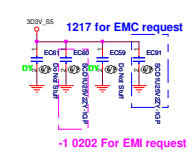
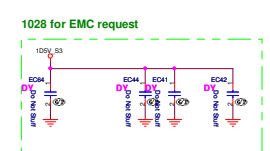
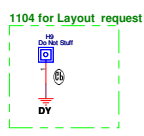
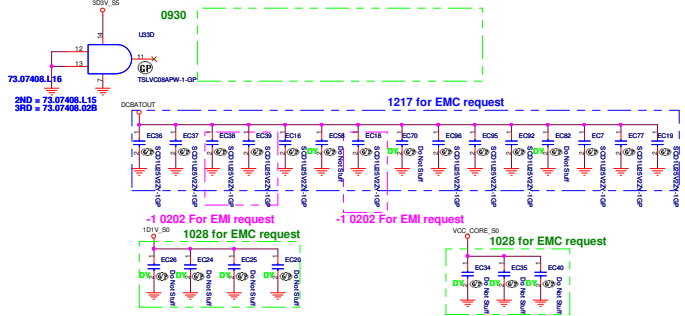
Pin Definition

1+	GND+	Batt-, Battery Negative Terminal+
2-	GND-	Batt+, Battery Negative Terminal-
3+	SMD+	SMBus data interface I/O pin+
4-	SMD-	SMBus clock interface I/O pin-
5+	TH+	Connect to Resistor to GND (10K to GND)+
6+	BI+	System present pin, low active+
7+	BATT+	Batt+, Battery Positive Terminal+
8-	BATT-	Batt-, Battery Positive Terminal-

Discrete Madison Hynix

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

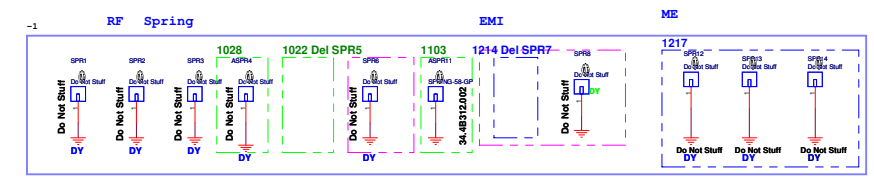
Title		
AD/BATT CONN		
Size	Document Number	Rev
	JE40-DN	-3
Date:	Friday, March 28, 2010	Sheet 51 of 63



Check test point

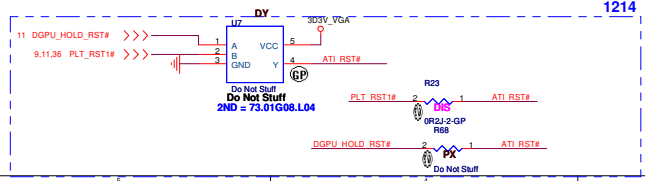
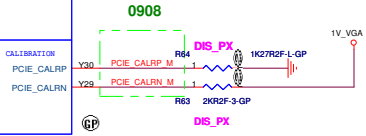
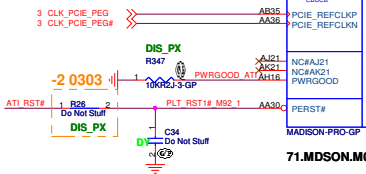
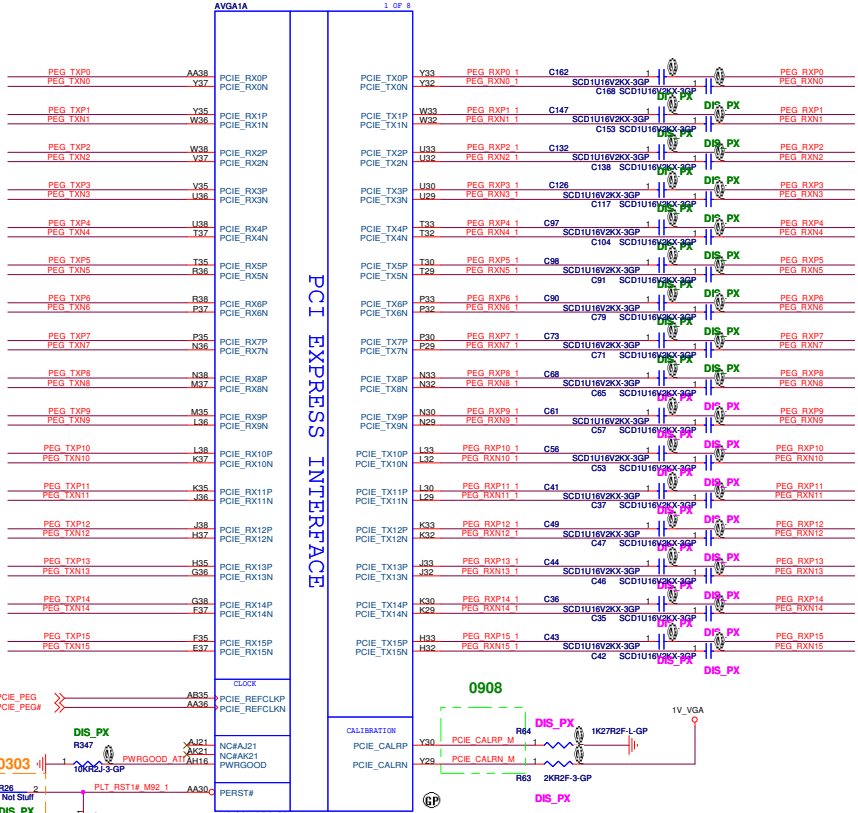
30DV_S0	TP126	Do Not Stuff
30DV_AUX_S5	TP125	Do Not Stuff
30DV_S5	TP123	Do Not Stuff
5V_S5	TP122	Do Not Stuff
12.36 PM_POWER	TP124	Do Not Stuff
4.71 CPU_POWER	TP127	Do Not Stuff
35.346 SS_ENABLE	TP128	Do Not Stuff
6.11 CPU_LED_RSTA	TP128	Do Not Stuff

Test Point放在Dimm Door打開可量測處



8 PEG_TXP[15..0] << PEG_TXP[15..0]
 8 PEG_TXN[15..0] << PEG_TXN[15..0]

8 PEG_RXP[15..0] << PEG_RXP[15..0]
 8 PEG_RXN[15..0] << PEG_RXN[15..0]



Discrete Madison Hyntx

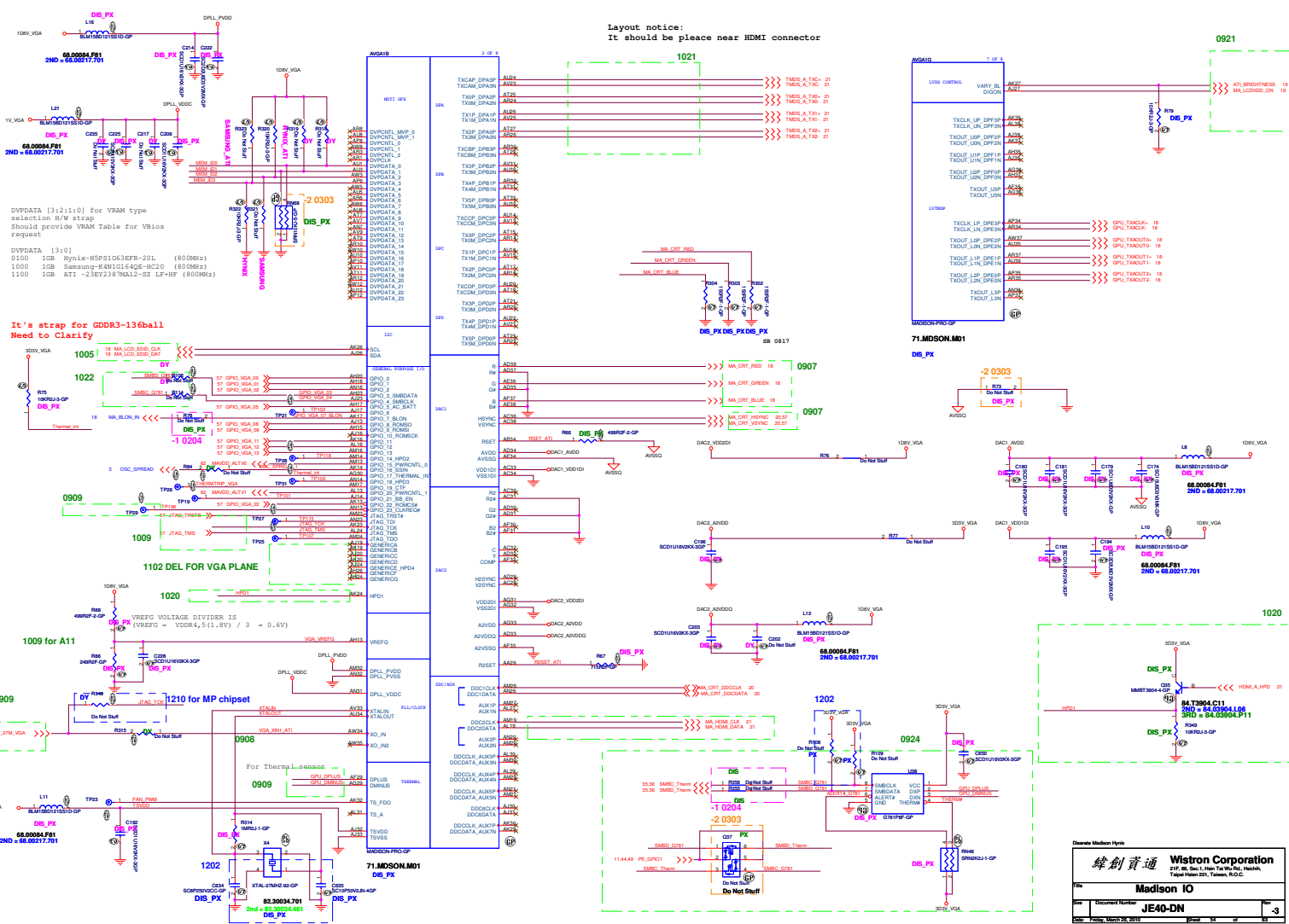
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison PCIE**


Size: Document Number **JE40-DN** Rev **-3**

Date: Friday, March 26, 2010 Sheet 53 of 53

Layout notice: please near HDMI connector
It should be placed near HDMI connector

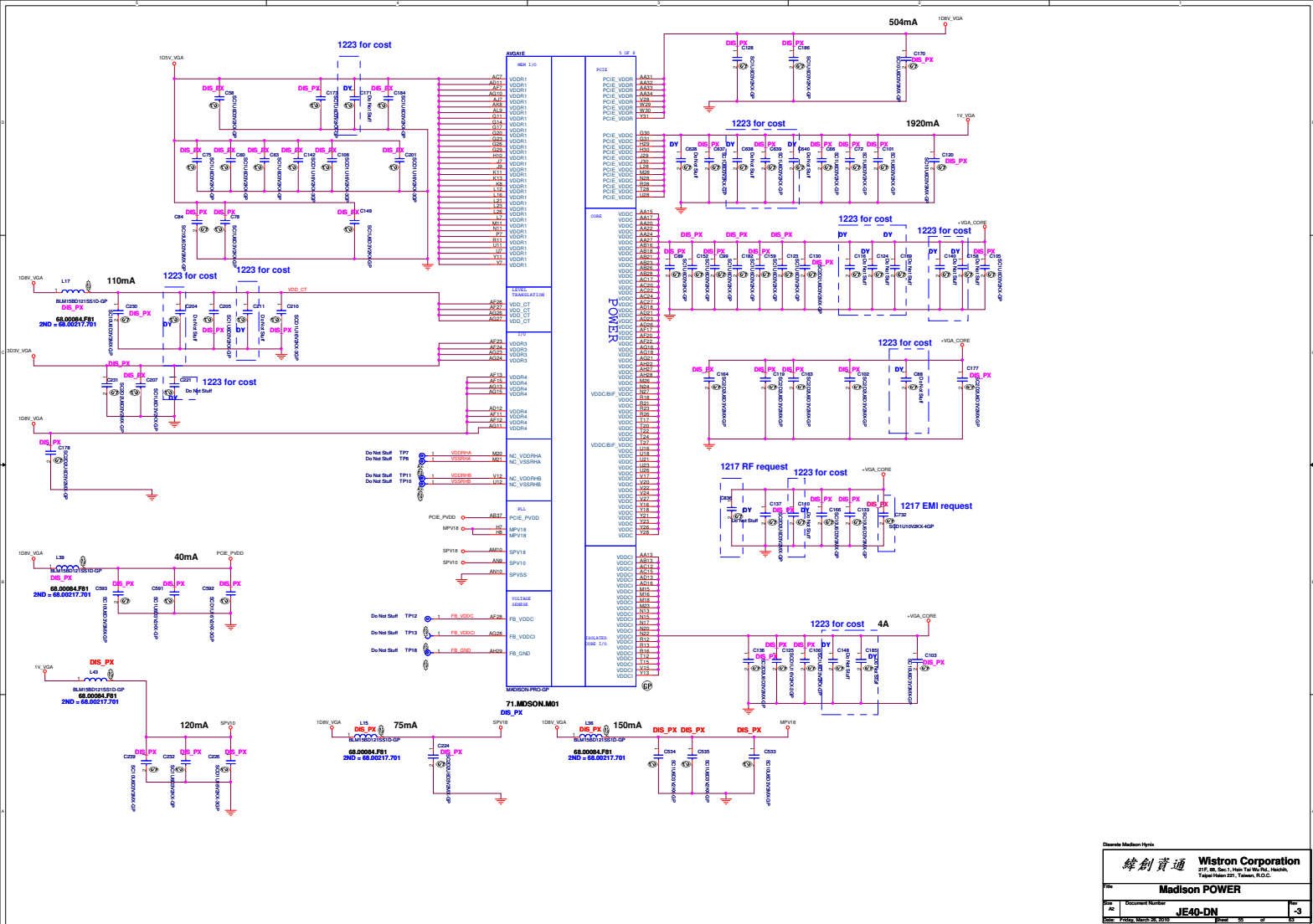


Drawn: Madison Hyeon


Wistron Corporation
 23F, 8F, 5th Fl., Hsin-Tai Rd, No. 10, Hsin-Tai, Taipei 106, Taiwan, R.O.C.

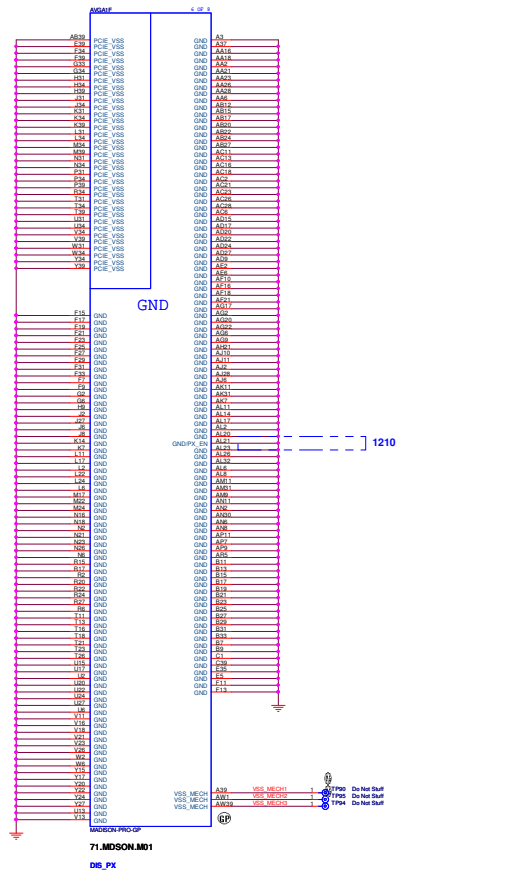
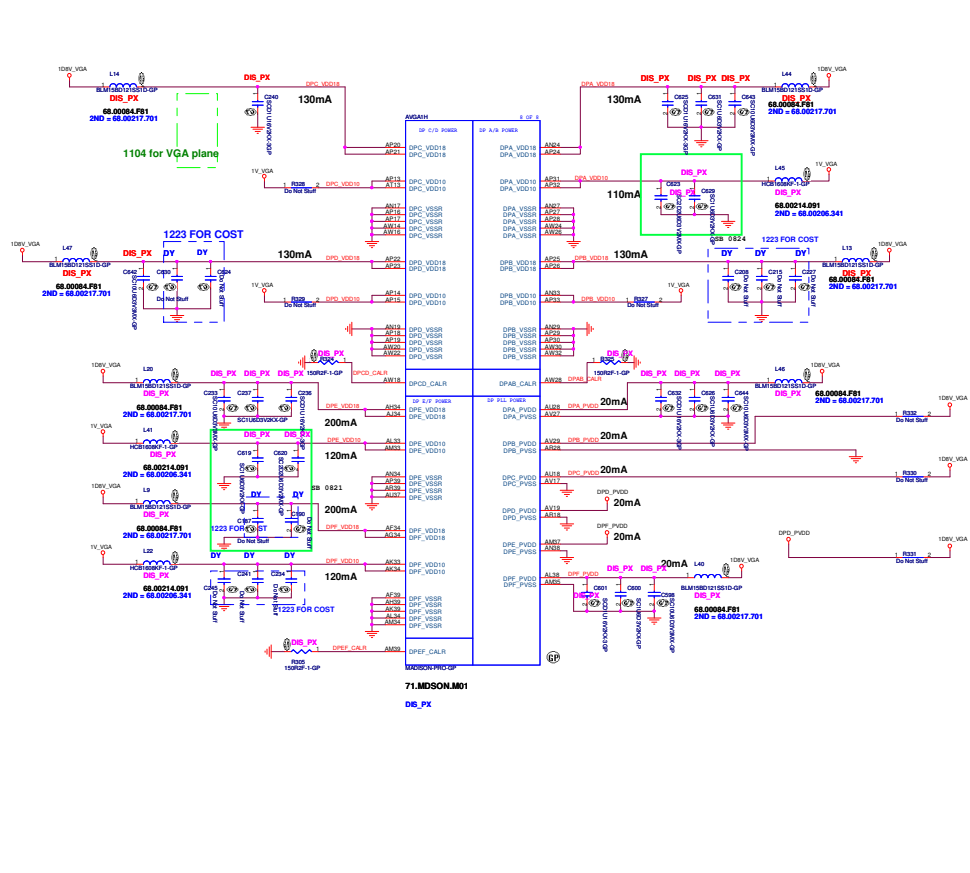
Part: **Madison IO**
 Document Number: **JE40-DN**
 2ND = 68.00217.701

Date: 2014-05-20
 Page: 3 of 3



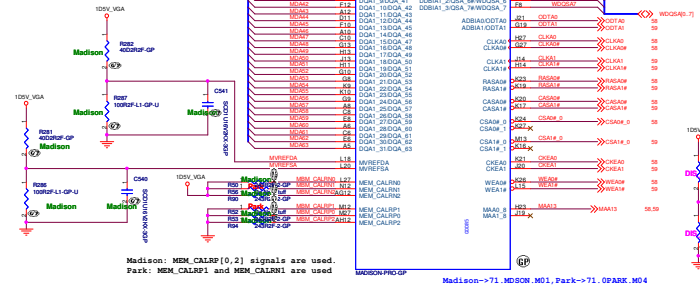
緯創資通 Wistron Corporation
 2/F, 8F, 9/F, 11/F, 12/F, 13/F, 14/F, 15/F, 16/F, 17/F, 18/F, 19/F, 20/F, 21/F, 22/F, 23/F, 24/F, 25/F, 26/F, 27/F, 28/F, 29/F, 30/F, 31/F, 32/F, 33/F, 34/F, 35/F, 36/F, 37/F, 38/F, 39/F, 40/F, 41/F, 42/F, 43/F, 44/F, 45/F, 46/F, 47/F, 48/F, 49/F, 50/F, 51/F, 52/F, 53/F, 54/F, 55/F, 56/F, 57/F, 58/F, 59/F, 60/F, 61/F, 62/F, 63/F, 64/F, 65/F, 66/F, 67/F, 68/F, 69/F, 70/F, 71/F, 72/F, 73/F, 74/F, 75/F, 76/F, 77/F, 78/F, 79/F, 80/F, 81/F, 82/F, 83/F, 84/F, 85/F, 86/F, 87/F, 88/F, 89/F, 90/F, 91/F, 92/F, 93/F, 94/F, 95/F, 96/F, 97/F, 98/F, 99/F, 100/F

8/ Madison POWER
 JE40-DN
 3



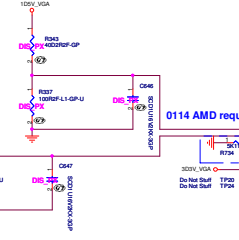
For SSTL-1.8/SSTL-2/DRI/GDR1: 0.5 * VDDR1.
For DDR3/GDR3/GDR4/GDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDR5	DOR3	DOR3
MYREF	1.5V	1.8/1.5V	1.5V
MYREF TO PWR	40.2R	10.2R	40.2R
MYREF TO GND	100R	100R	100R



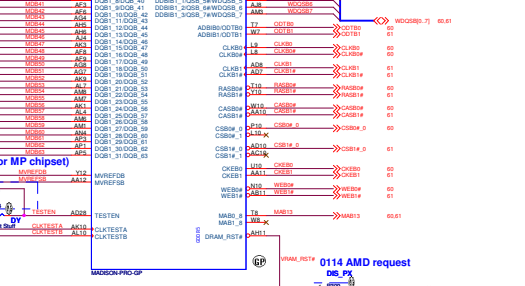
For SSTL-1.8/SSTL-2/DRI/GDR1: 0.5 * VDDR1.
For DOR3/GDR3/GDR4/GDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDR5	DOR3	DOR3
MYREF	1.5V	1.8/1.5V	1.5V
MYREF TO PWR	40.2R	10.2R	40.2R
MYREF TO GND	100R	100R	100R



For SSTL-1.8/SSTL-2/DRI/GDR1: 0.5 * VDDR1.
For DOR3/GDR3/GDR4/GDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDR5	DOR3	DOR3
MYREF	1.5V	1.8/1.5V	1.5V
MYREF TO PWR	40.2R	10.2R	40.2R
MYREF TO GND	100R	100R	100R

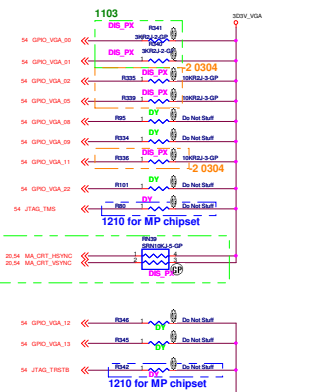


STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS (0=DO NOT RETAIL RESISTOR 1=RETAIL RESISTOR X=DESIGN DEPENDANT NA=NOT APPLICABLE)
TX_PRRS_ENB (Internal PD)	GP100	PCB FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% TX output swing 1= Full TX output swing	X
TX_DRAMP_EN (Internal PD)	GP101	Transmitter De-emphasis Enable 0= 1x de-emphasis disabled 1= 1x de-emphasis enabled	X
RESERVED	GP108	RESERVED	0
BIF_VGA_DIS	GP109	VGA ENABLED	0
RESERVED	GP1021	RESERVED	0
BIOS_ROM_EN	GP1022,ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GP01[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT If BIOS_ROM_EN=1, then Config[3:0] defines the ROM type If BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	X X X
RSV0	V2SYNC	0	0
RSV0	R2SYNC	0	0
ADD[1]	VGA_HSYNC	ADD[1:0] 0:0= audio function 0:1=audio for Displayport and HDMI	X
ADD[0] (Internal PD)	VGA_VSYNC	ADD[0] 0:1=audio for Displayport and HDMI 1:0=audio for Displayport only 1:1=Audio for both Displayport and HDMI	X

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

R2SYNC, GENERIC0, GPIO0, GPIO1

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory aperture	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	SP	M25P10A
256MB	x001		M25P10A
512MB	x010	Microelectronics	M25P20
1GB	x011		M25P40
2GB	x012		M25P80
4GB	x013	Changis (Formerly PMC)	25LV012A
			25LV010A

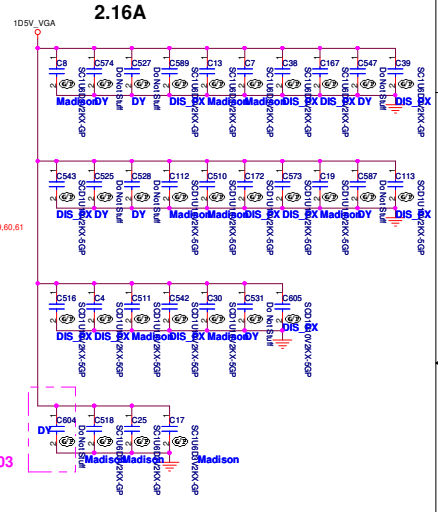
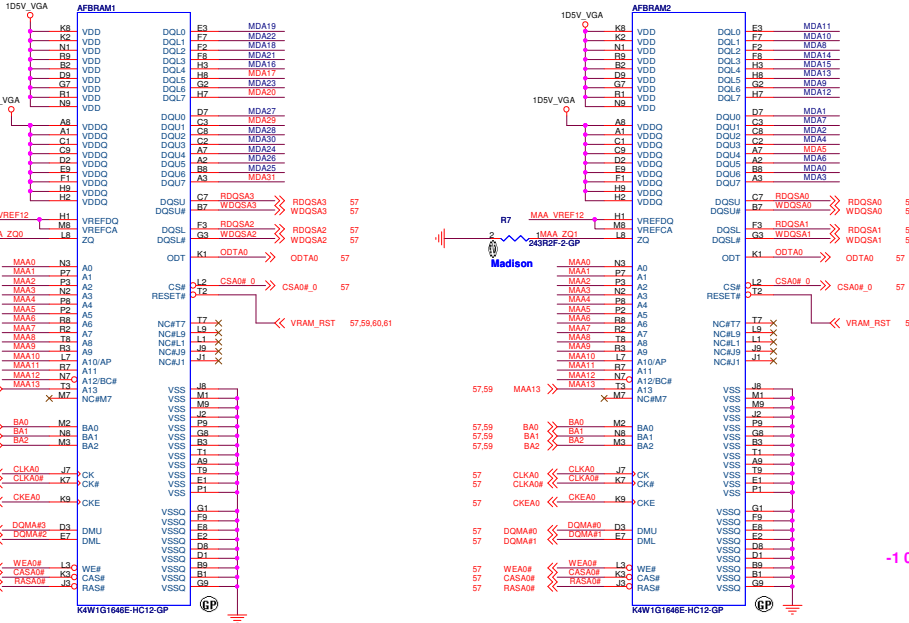


Designator	For M97-M2	For Manhattan
R_MEM_1	10K	10K
R_MEM_2	40R/Short	51R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Wistron Corporation
217, 2nd, 3rd, 4th, 5th, 6th, 7th, 8th, 9th, 10th, 11th, 12th, 13th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st, 22nd, 23rd, 24th, 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, 41st, 42nd, 43rd, 44th, 45th, 46th, 47th, 48th, 49th, 50th, 51st, 52nd, 53rd, 54th, 55th, 56th, 57th, 58th, 59th, 60th, 61st, 62nd, 63rd, 64th, 65th, 66th, 67th, 68th, 69th, 70th, 71st, 72nd, 73rd, 74th, 75th, 76th, 77th, 78th, 79th, 80th, 81st, 82nd, 83rd, 84th, 85th, 86th, 87th, 88th, 89th, 90th, 91st, 92nd, 93rd, 94th, 95th, 96th, 97th, 98th, 99th, 100th

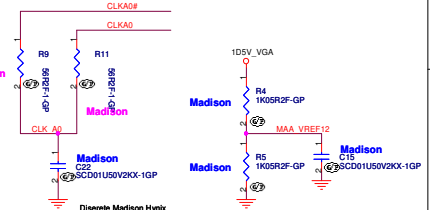
Madison Memory / Straps
JE40-DN
3

DDR3



SAMSUNG: 72.41164.HOU
 HYNIX: 72.51G63.COU

- 57.59 DQMA#(0..7) <<>
- 57.59 RDQSA(0..7) <<>
- 57.59 WDQSA(0..7) <<>
- 57.59 MAA(0..12) <<>
- 57.59 MDA(0..63) <<>

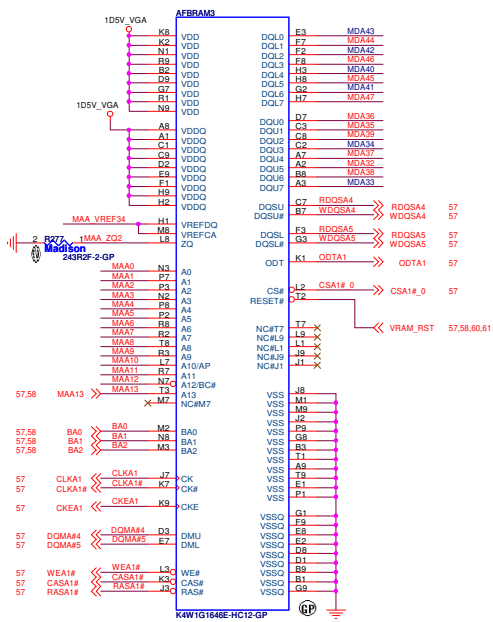


Discrete Madison Hynix

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

File	VRAM(1/4)	
Size	Document Number	Rev
A8	JE40-DN	*3
Date:	Friday, March 26, 2010	Page 58 of 60

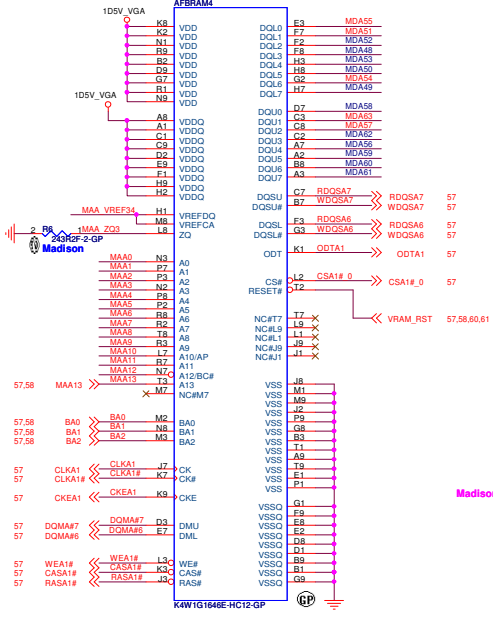
DDR3



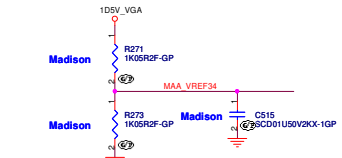
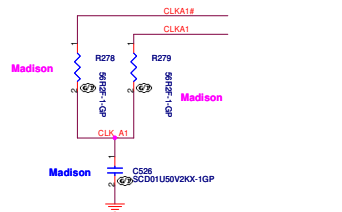
Madison
72.41164.H0U

SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

- 57.58 DQMA[0..7] <<>
- 57.58 RDQSA[0..7] <<>
- 57.58 WDQSA[0..7] <<>
- 57.58 MAA[0..12] <<>
- 57.58 MDA[0..63] <<>



Madison
72.41164.H0U

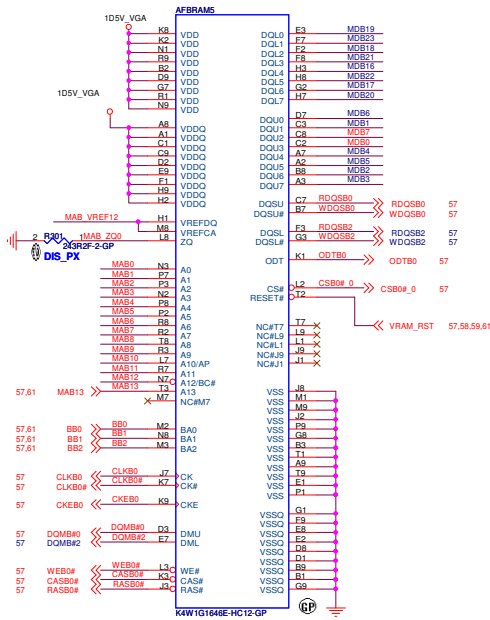


Discrete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

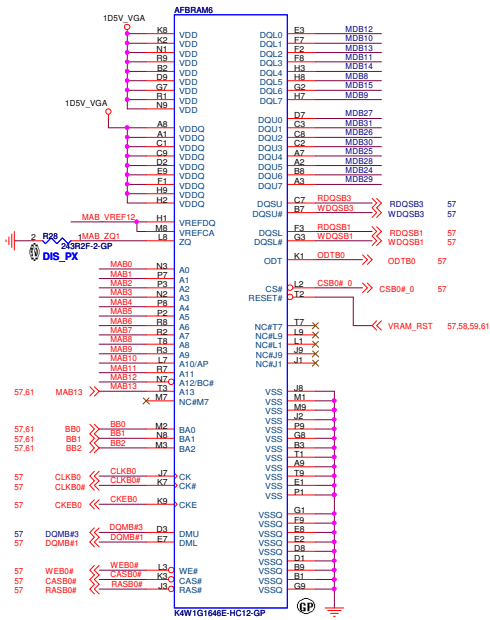
File	JE40-DN		
Size	Document Number	Rev	-3
Date:	Friday, March 26, 2010	Sheet	59 of 63

DDR3



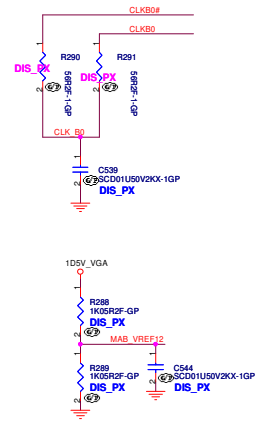
DIS_PX
72.41164.H0U

SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



DIS_PX
72.41164.H0U

- 57.61 DOMB[0..7] <<>
- 57.61 RDQS[0..7] <<>
- 57.61 WDQS[0..7] <<>
- 57.61 MAB[0..12] <<>
- 57.61 MAB[0..63] <<>



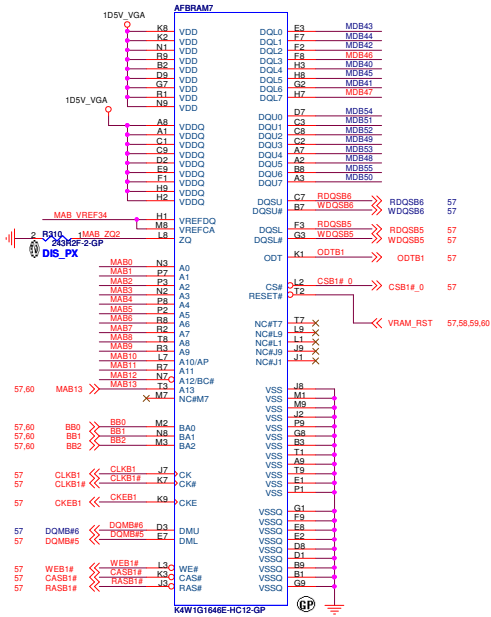
Discrete Madison Hynix

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 221, Taiwan, R.O.C.

Title			VRAM(3/4)	
Size	Document Number			Rev
A0		JE40-DN		-3
Date:	Friday, March 28, 2010	Sheet	60	of
			63	

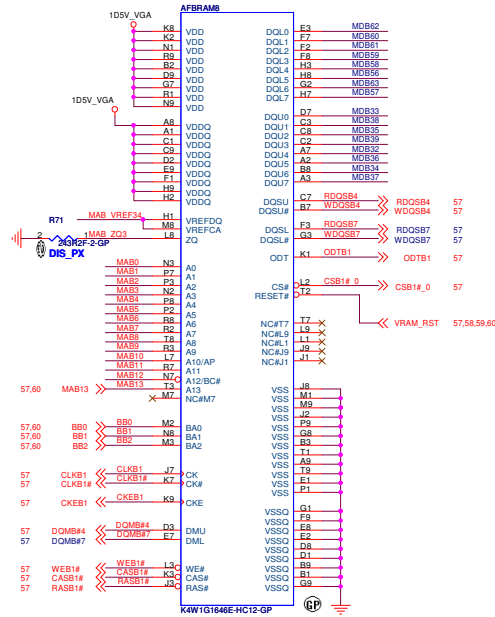
DDR3



DIS_PX
72.41164.H0U

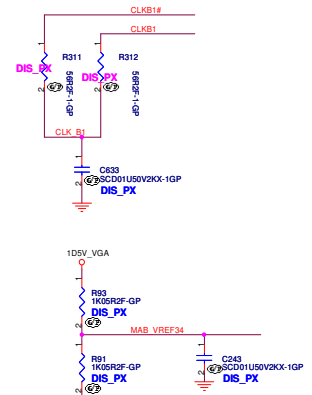
- 57.60 D0MB#0..7] <<>
- 57.60 RDQS0#0..7] <<>
- 57.60 WDSQS0#0..7] <<>
- 57.60 MAB#0..12] <<>
- 57.60 MD#0..63] <<>

SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



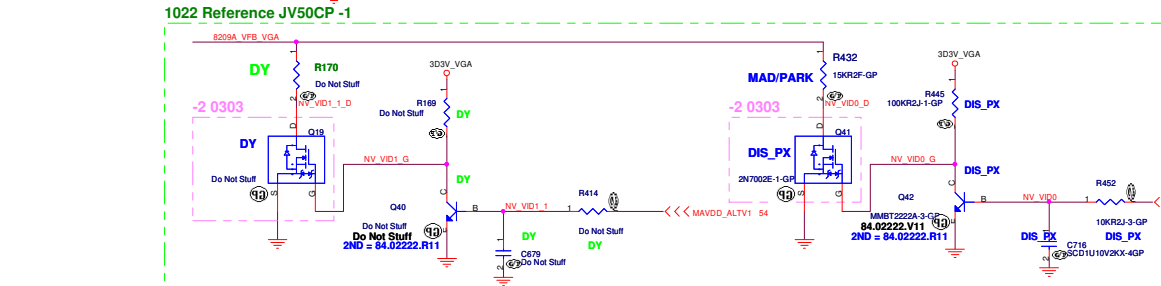
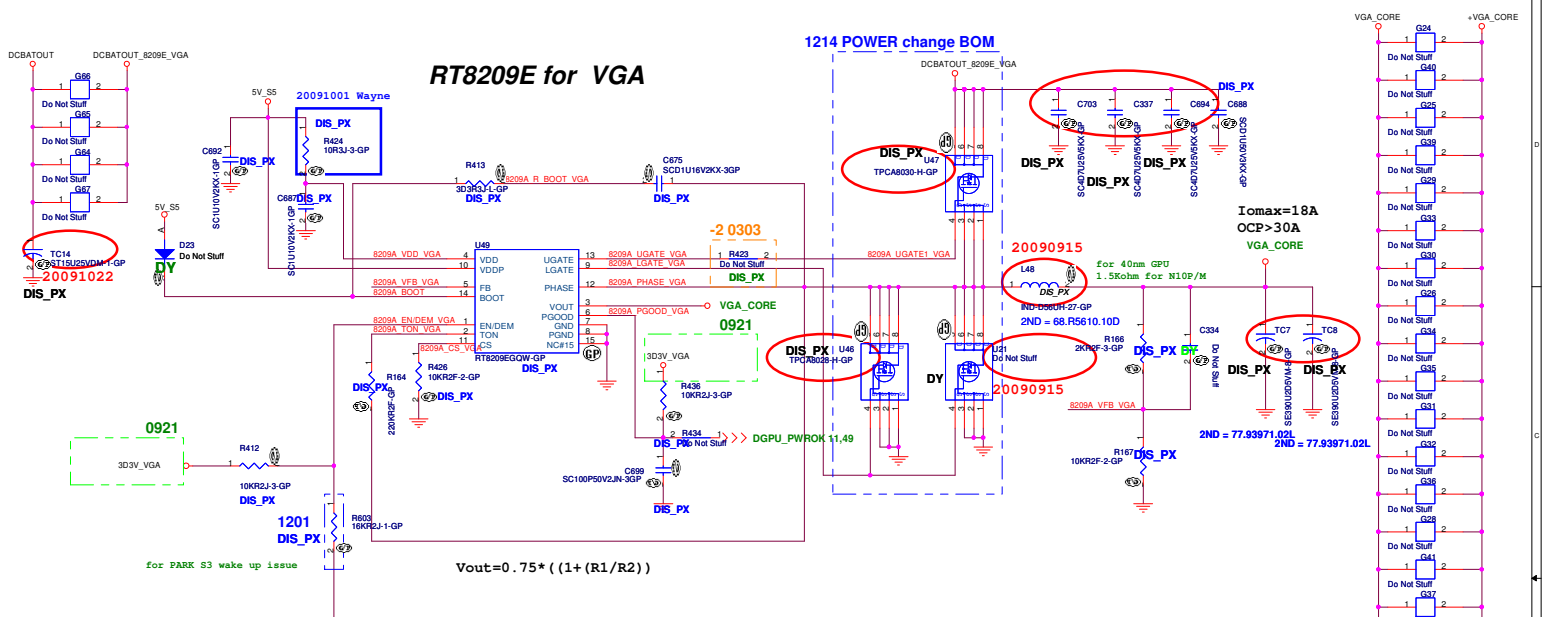
DIS_PX
72.41164.H0U

- 57.60 D0MB#0..7] <<>
- 57.60 RDQS0#0..7] <<>
- 57.60 WDSQS0#0..7] <<>
- 57.60 MAB#0..12] <<>
- 57.60 MD#0..63] <<>



Discrete Madison Hynix

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Ta Wu Rd., Hsinchu, Taipei Hsin 321, Taiwan, R.O.C.	
File	VRAM(4/4)		
Size	Document Number	JE40-DN	
		Rev	-3
Date:	Friday, March 26, 2010	Sheet	61 of 63



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDV_ALTVO	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDV_ALTVO	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

R432	15KR2F-GP
MADSION PRO	15KR2F 64.15025.6DL
PARK XT	6R81K 64.68115.6DL

Discrete Madision Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209E VGA CORE		Rev
Size	Document Number	JV42-DN	-3
Customer			
Date: Monday, March 29, 2010	Sheet: 62	of	63

NB
RS780-->RS880M
71.RS780.M02-->71.RS880.M02

BOM
1st -> All SKU

SB
SB820M-1-GP
71.SB820.00U-->71.SB820.M03

SATA_CALRP
A11: 80歐姆 1% resistor to GND
A12: TBD歐姆 1% resistor to GND

SATA_CALRN
A11:A11: 931歐姆 1% resistor to VDDAN_11_SATA
A12: TBD歐姆 1% resistor to VDDAN_11_SATA.

R250
Madison-->R250 64.32425.6DL R402H16 32K4R2F
Park -->R250 64.32425.6DL R402H16 32K4R2F
PX -->R250 64.32425.6DL R402H16 32K4R2F

VGA
Madison--> PN:71.MDSON.M01
Park--> PN:71.0PARK.M04

VRAM
Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006
Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004
ATI--> VRAM FBRAM1~8 PN: VR.1GB0T.002

CRT
UMA-->L1-->2R 0603
C62-->47U/6.3V
DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)
C62-->DY
PX--> 133 歐姆 (R58 63.10334.1DL R402H16 133R2F-GP)

R605(MAD/PARK/PX)
Madison-->R605 64.15005.6DL R402H16150R2F-L-GP
Park -->R605 64.15005.6DL R402H16150R2F-L-GP
PX -->R605 64.15005.6DL R402H16150R2F-L-GP

HDMI
UMA -->R612 R613 R618 R619 R620 R621 R624 R625 64.71505.6DL R402H16715R2F-2-GP

R432(MAD/PARK)
Madison-->15KR2F 64.15025.6DL
Park-->R432 64.68115.6DL R402H16 6.81KR2F

Discrete Madison Hynix

緯創資通		Wistron Corporation	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.</small>			
NOTE			
File	Document Number		Rev
	JV42-DN		-3
Date:	Monday, March 29, 2010	Sheet	63 of 63