

Compal Confidential

Model Name : JE50-HR/SJV50-HR

Compal Project Name : P5WE0/P5WS0

File Name : LA-6902P

Compal Confidential

JE50-HR/SJV50-HR(P5WE0/P5WS0) M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH

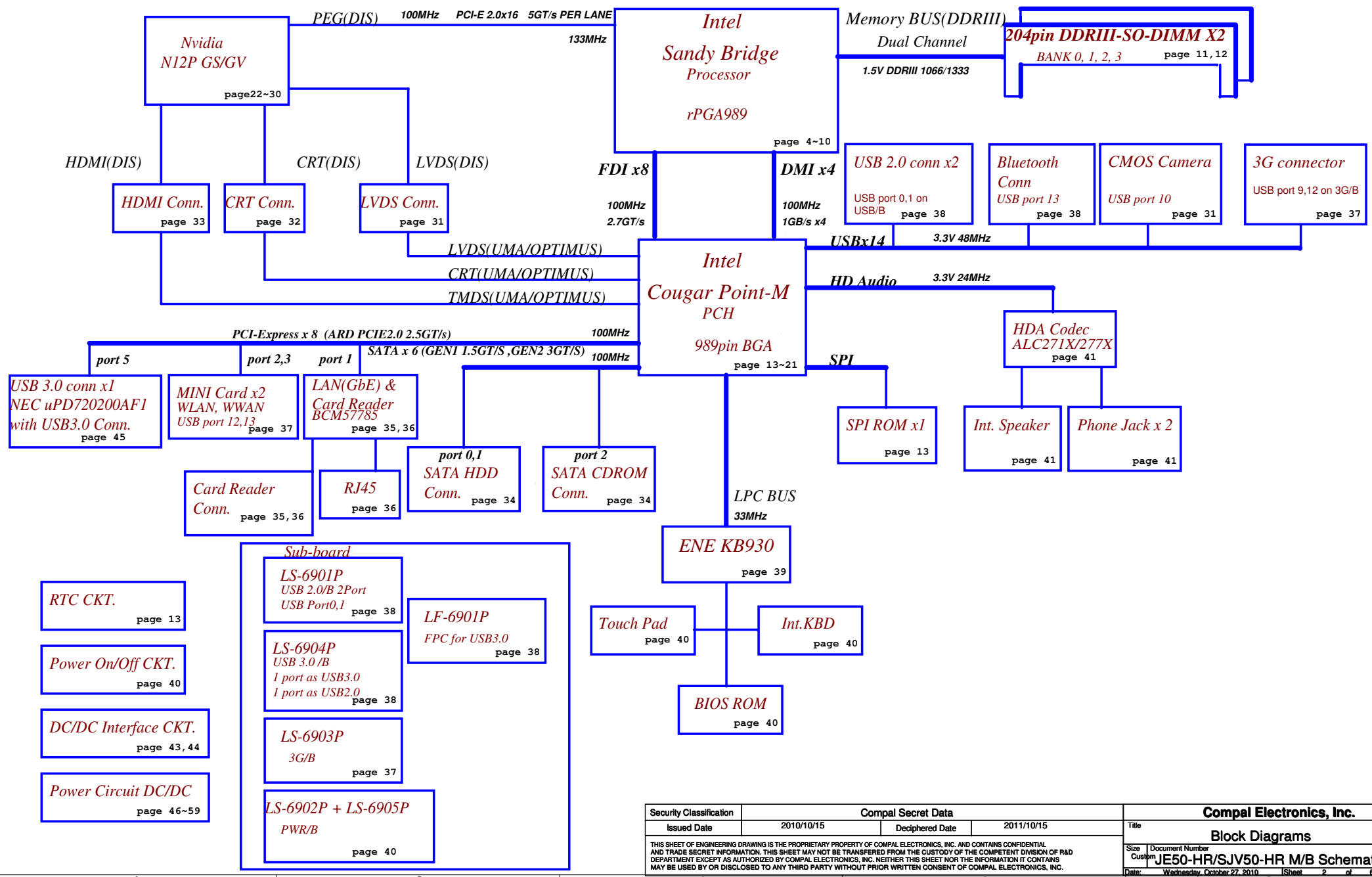
Nvidia N12P GS/GV

2010-10-19

REV : 0 . 1

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Fan Control
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
--------	---------

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ USB30 SKU: USB30@ OPTIMUS SKU: OPT@
 BT SKU: BT@ USB20 SKU: USB20@ Non-OPTIMUS SKU: NOPT@

LAN Chip A0 version: A0@ N12P-GS: GS@
 LAN chip B0 Version: B0@ N12P-GV: GV@

BOM Config

UMA Only: BT@3G@/USB30@/UMA@/UMAO@/NOPT@/A0@
 OPTIMUS (N12P-GS) : BT@3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GS@
 DIS Only (N12P-GS) : BT@3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GS@
 OPTIMUS (N12P-GV) : BT@3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GV@
 DIS Only (N12P-GV) : BT@3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GV@

VRAM P/N:
 64*16
 Samsung : SA000035700
 Hynix : SA000032400/SA0000324C0
 128*16
 Samsung : SA00003MQ40
 Hynix : SA00003VS00

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
 EVT2
 DVT
 PVT
 Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@
N12P-GS	GS@
N12P-GV	GV@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
		2	USB3.0 coloy USB2.0 Conn.
	UHCI1	3	USB/B Coloy USB3.0
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Mini Card 1(WLAN)
	UHCI3	9	3G/B(WWAN)
		10	Camera
		11	Mini Card 2(Reserved)
UHCI4	UHCI5	12	3G/B(SIM Card)
		13	BlueTooth

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DA6000KC00

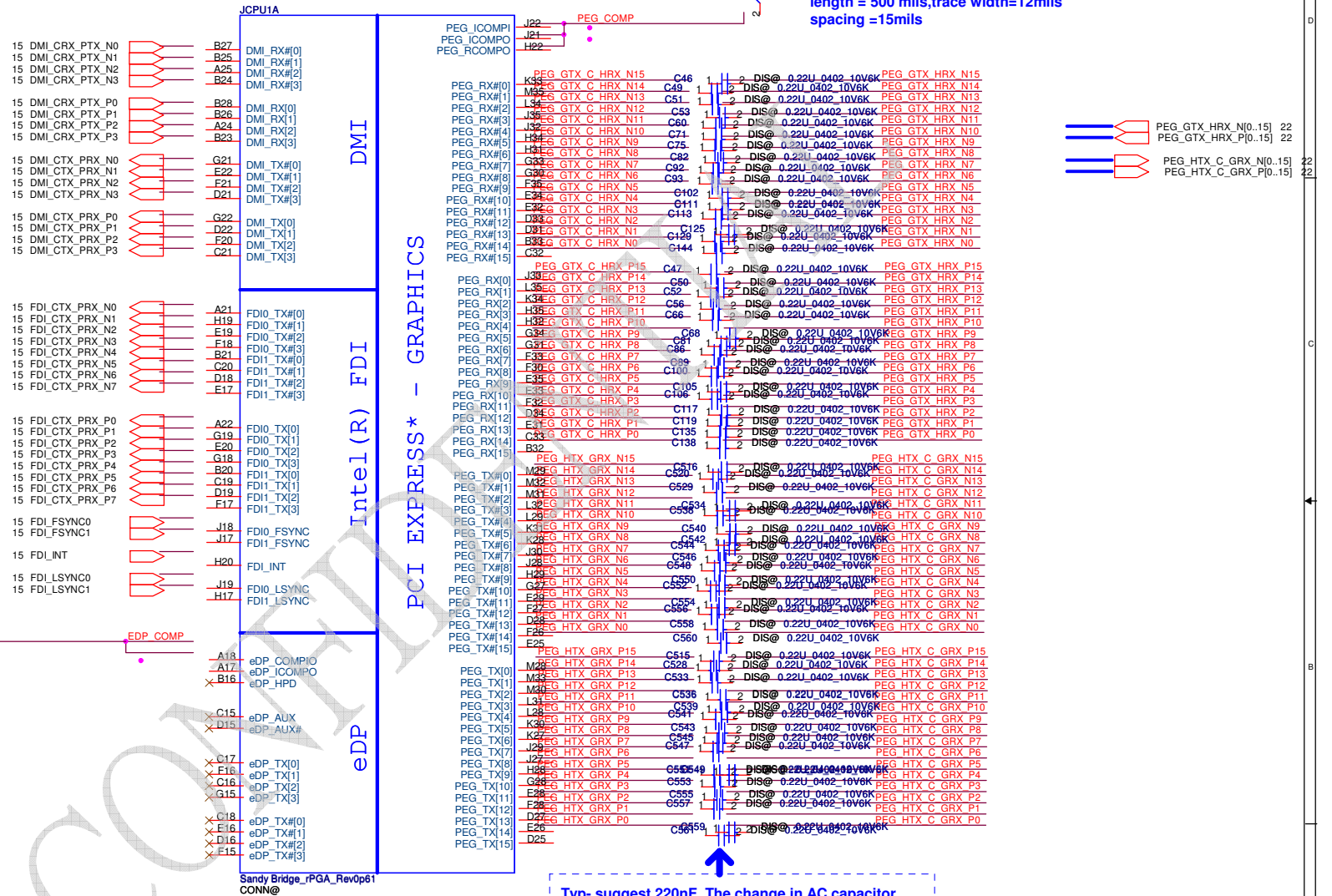


+1.05VS_VTT

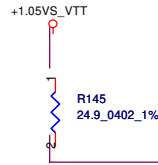
R517

24.9_0402_1%

PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed,
max length = 500 mils, trace width=4mils
PEG_ICOMPO signals should be routed with - max
length = 500 mils, trace width=12mils
spacing =15mils

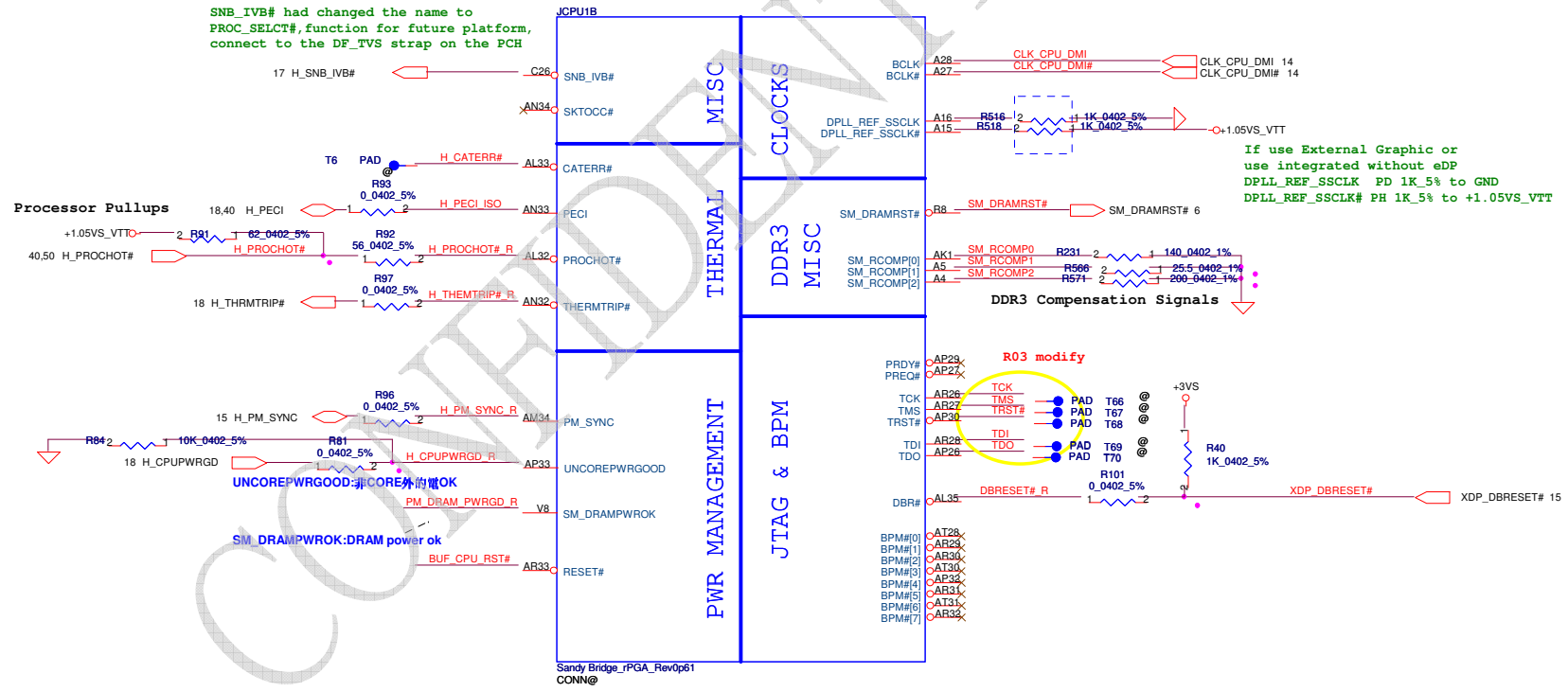
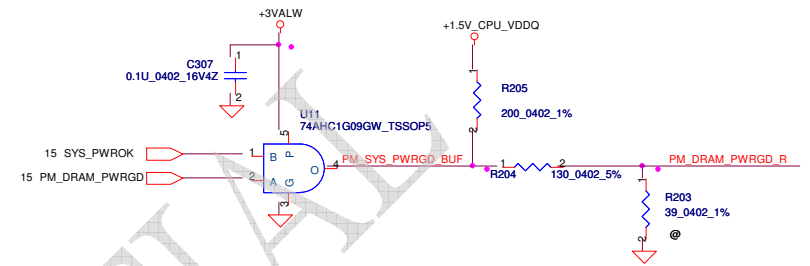
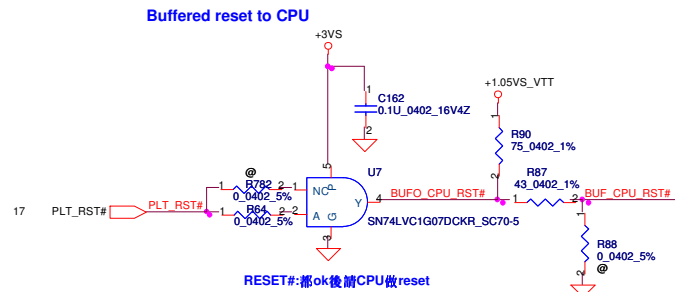


eDP_COMPIO and ICOMPO signals should be shorted near balls,
Trace Width for EDP_COMPIO=4mils,
EDP_ICOMPO=12mils,
should not be left floating
, even if disable eDP function...

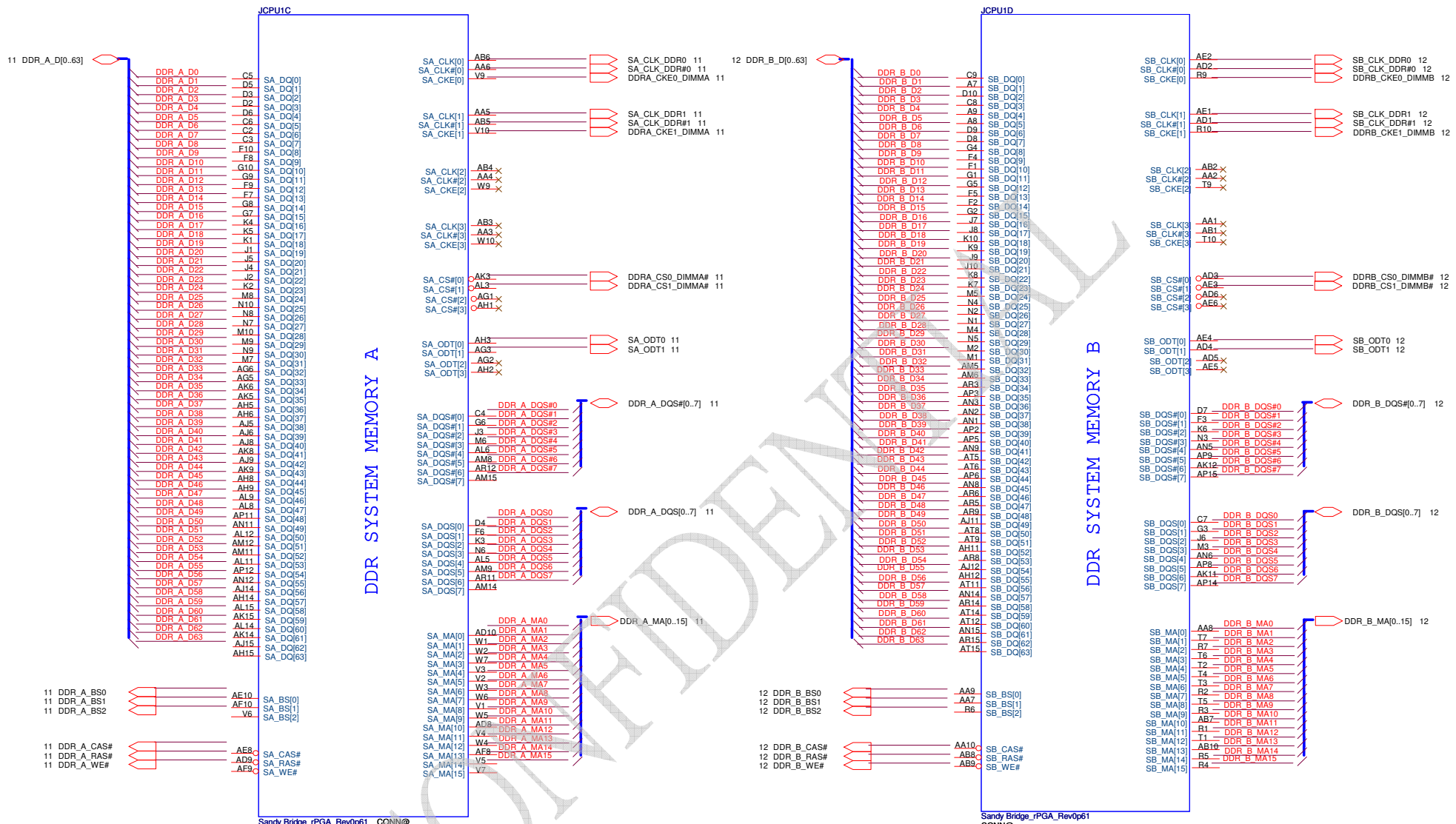


Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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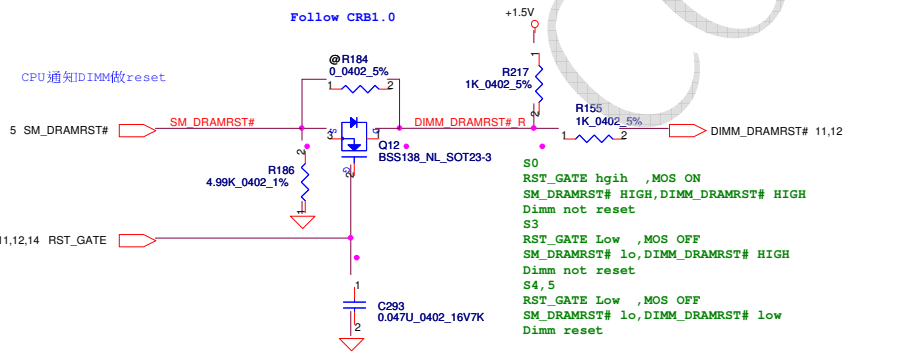


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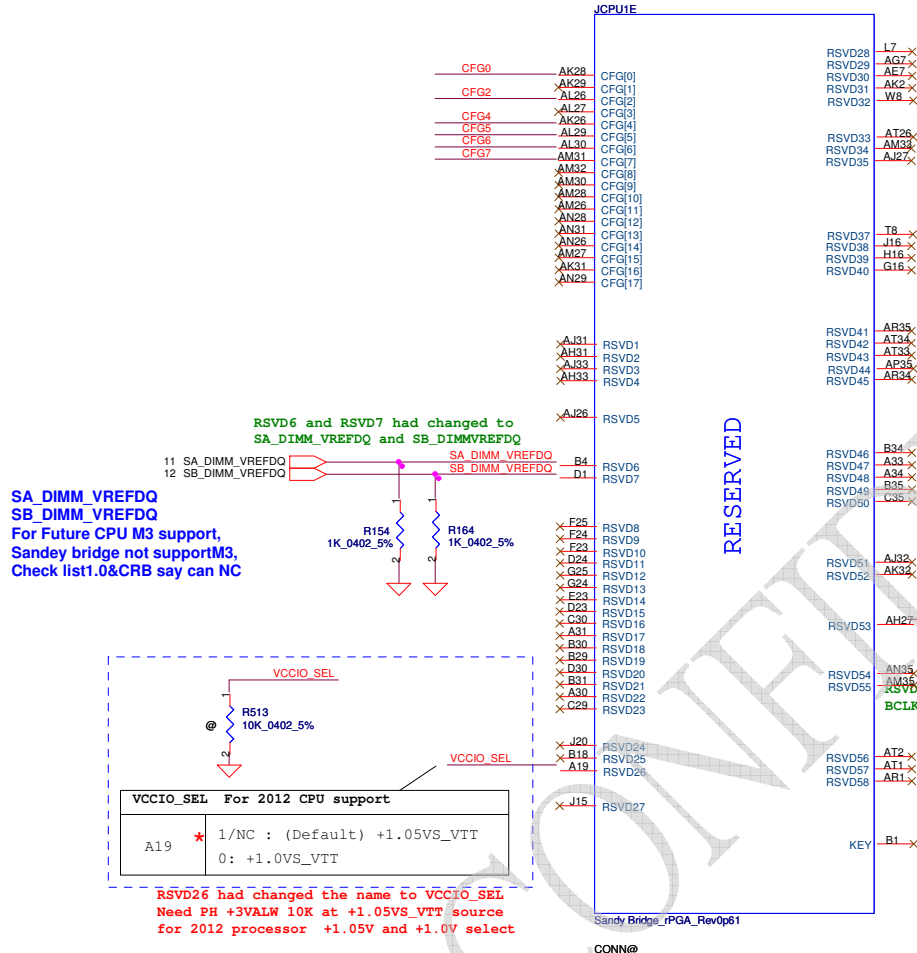
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Sandy Bridge_rPGA_Rev0p61 CONN@



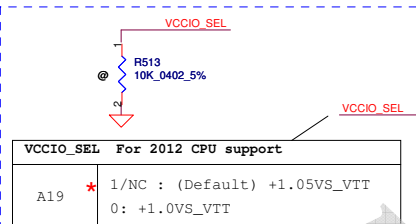
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CFG Straps for Processor



RSVD6 and RSVD7 had changed to SA_DIMM_VREFDQ and SB_DIMM_VREFDQ

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandy bridge not support M3,
Check list1.0&CRB say can NC



RSVD26 had changed the name to VCCIO_SEL.
Need PH +3VALW 10K at +1.05VS_VTT source
for 2012 processor +1.05V and +1.0V select

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

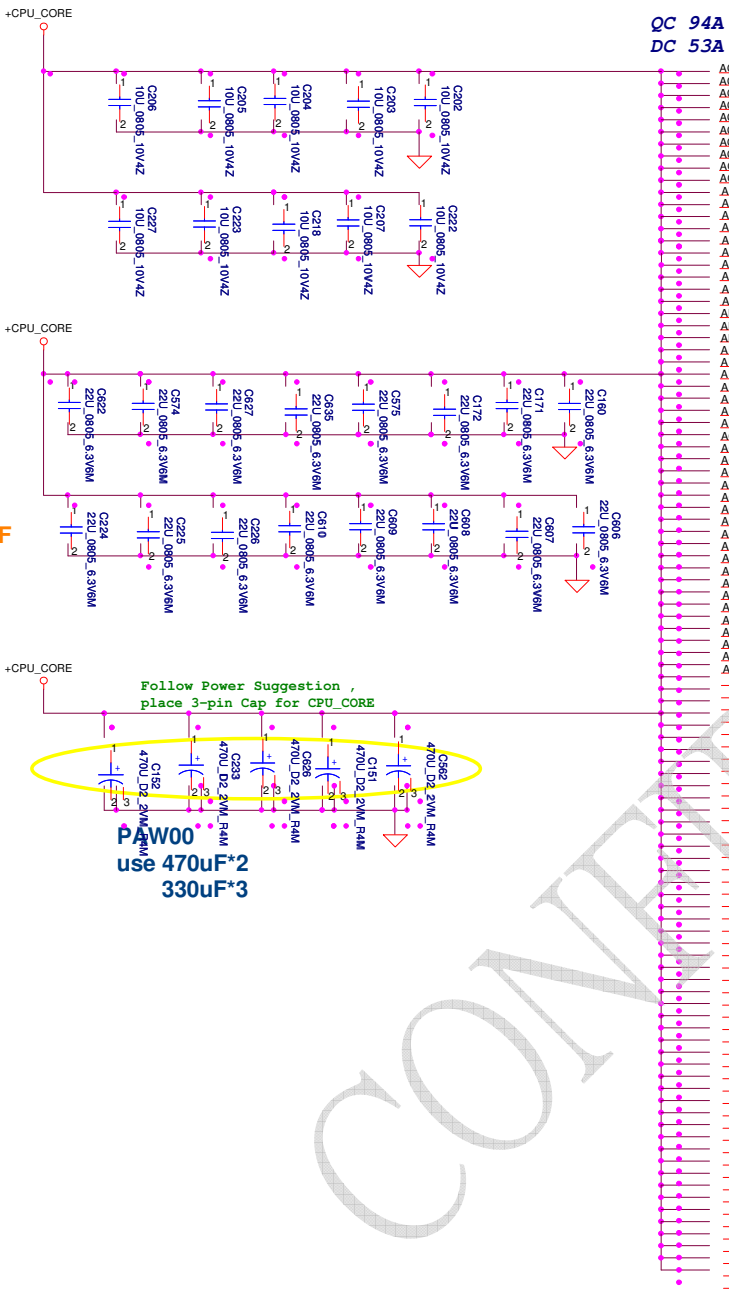
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

SV type CPU

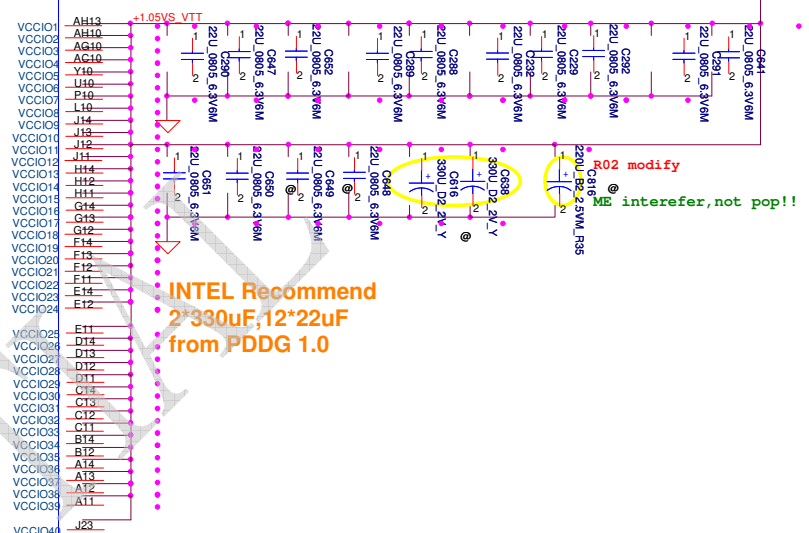
JCPU1F

POWER



- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AF35 VCC10
- AF34 VCC11
- AF33 VCC12
- AF32 VCC13
- AF31 VCC14
- AF30 VCC15
- AF29 VCC16
- AF28 VCC17
- AD35 VCC18
- AD34 VCC19
- AD33 VCC20
- AD32 VCC21
- AD31 VCC22
- AD30 VCC23
- AD29 VCC24
- AD28 VCC25
- AD27 VCC26
- AD26 VCC27
- AC35 VCC28
- AC34 VCC29
- AC33 VCC30
- AC32 VCC31
- AC31 VCC32
- AC29 VCC33
- AC28 VCC34
- AC27 VCC35
- AA35 VCC36
- AA34 VCC37
- AA33 VCC38
- AA32 VCC39
- AA31 VCC40
- AA29 VCC41
- AA28 VCC42
- AA27 VCC43
- AA26 VCC44
- AA25 VCC45
- AA24 VCC46
- AA23 VCC47
- AA22 VCC48
- AA21 VCC49
- Y35 VCC50
- Y34 VCC51
- Y33 VCC52
- Y32 VCC53
- Y31 VCC54
- Y30 VCC55
- Y29 VCC56
- Y28 VCC57
- Y27 VCC58
- Y26 VCC59
- Y25 VCC60
- V34 VCC61
- V33 VCC62
- V32 VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- V25 VCC70
- U33 VCC71
- U32 VCC72
- U31 VCC73
- U30 VCC74
- U29 VCC75
- U28 VCC76
- U27 VCC77
- U26 VCC78
- U25 VCC79
- U24 VCC80
- U23 VCC81
- U22 VCC82
- U21 VCC83
- U20 VCC84
- U19 VCC85
- U18 VCC86
- U17 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

8.5A



INTEL Recommend
2*330uF, 12*22uF
from PDDG 1.0

R02 modify
ME interfere, not pop!

INTEL Recommend
4*470uF, 16*22uF and 10*10uF
from PDDG 1.0

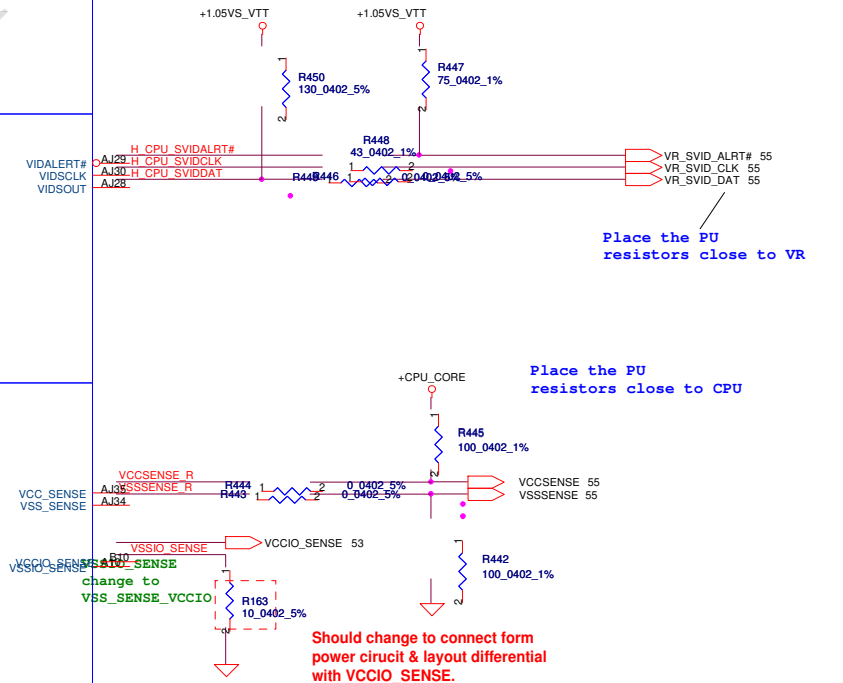
Follow Power Suggestion,
place 3-pin Cap for CPU_CORE

PAW00
use 470uF*2
330uF*3

CORE SUPPLY

SVID

SENSE LINES

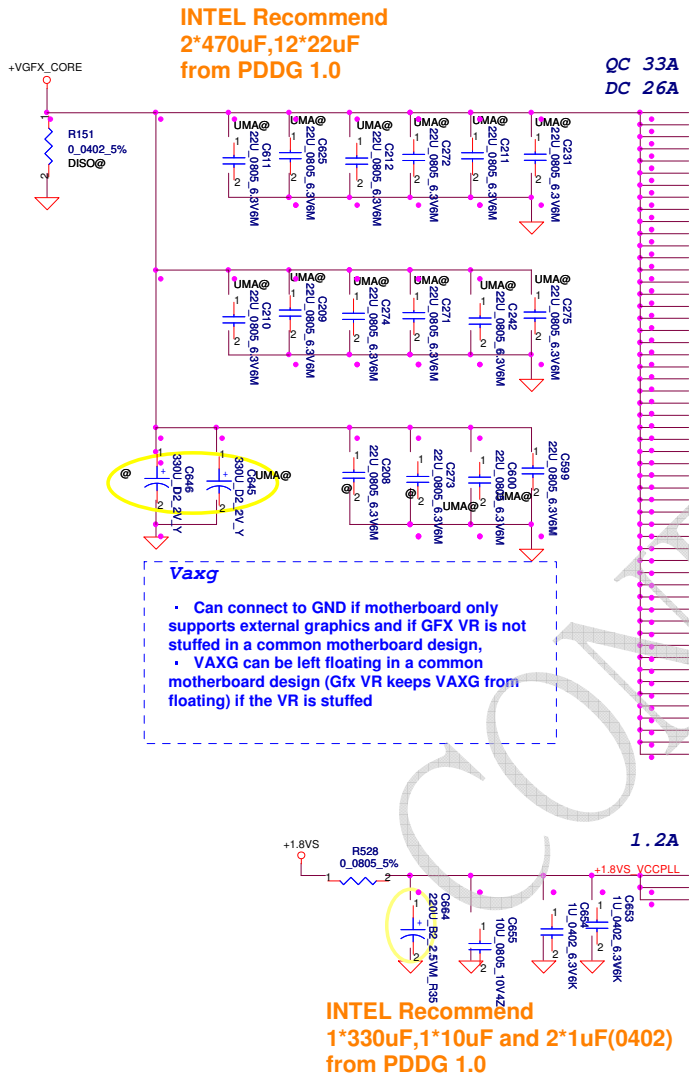


Place the PU
resistors close to VR

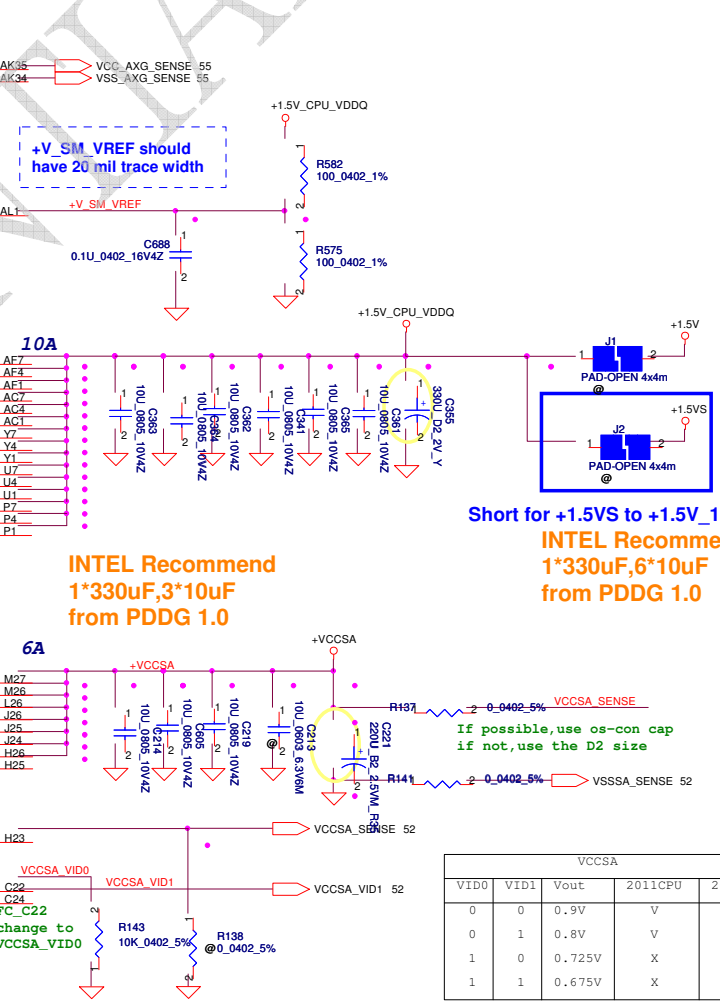
Place the PU
resistors close to CPU

Should change to connect form
power circuit & layout differential
with VCCIO_SENSE.

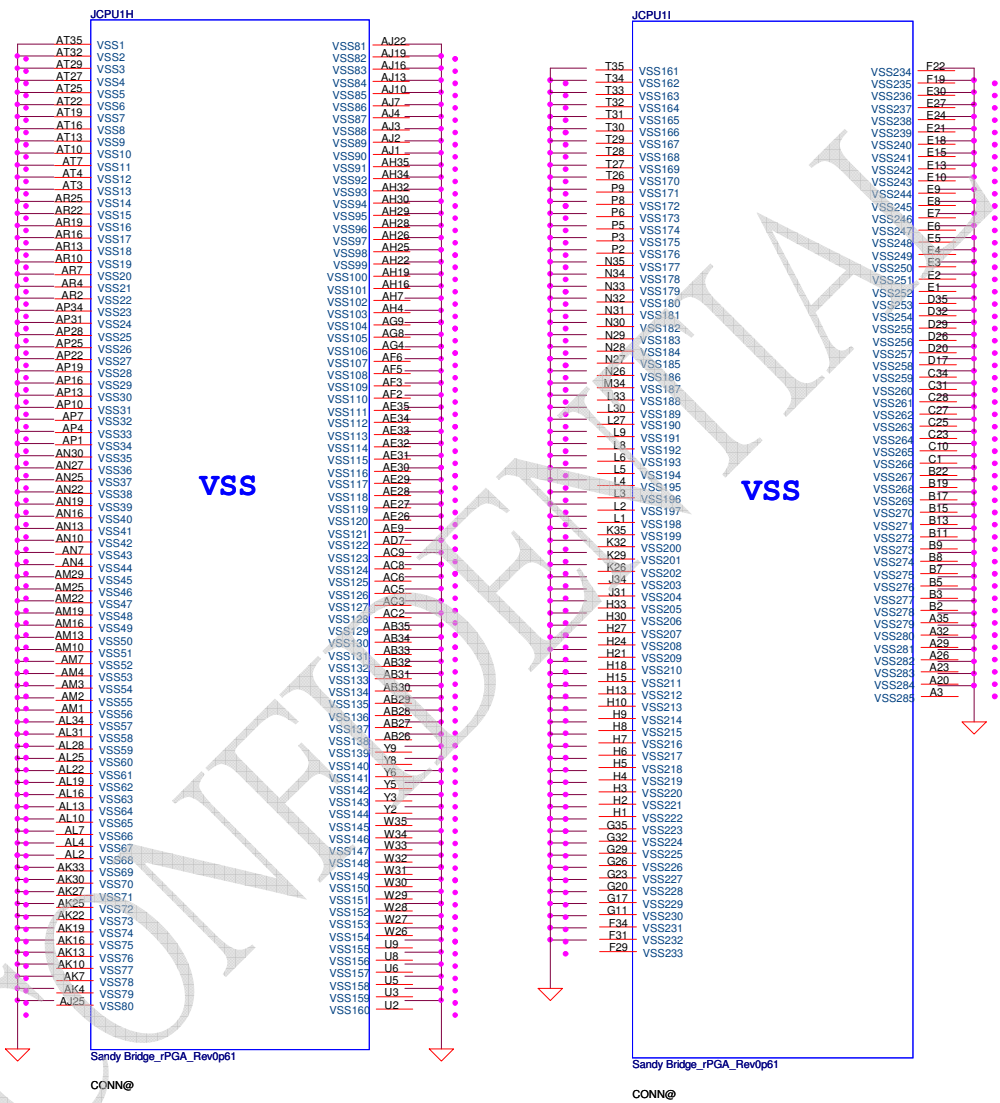
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POWER



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Sandy Bridge_rPGA_Rev0p61

Sandy Bridge_rPGA_Rev0p61

CONN@

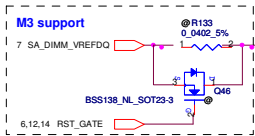
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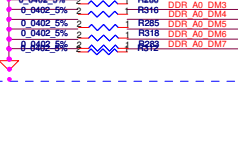
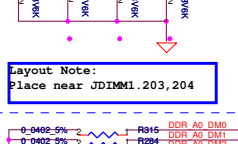
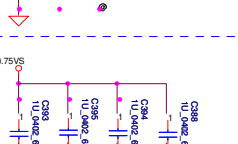
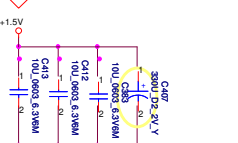
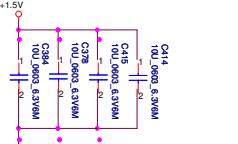
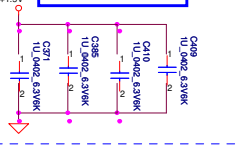
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JES0-HR/SJV50-HR M/B Schematics

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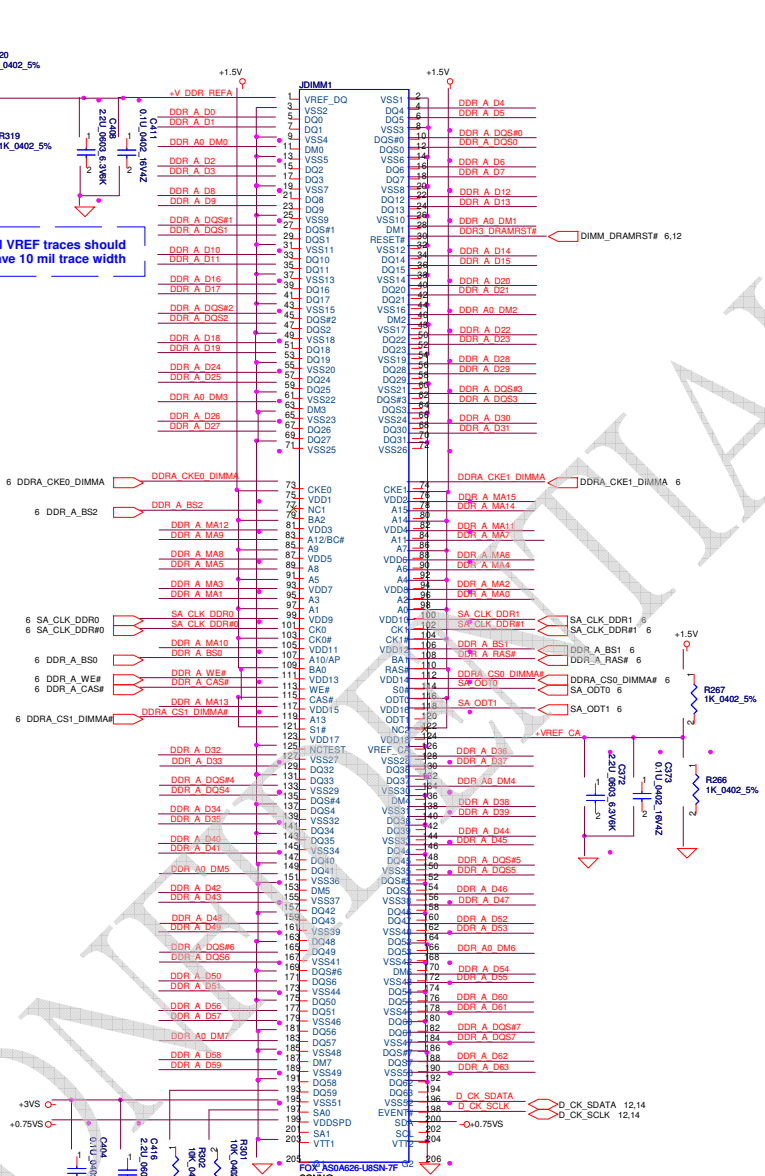


Layout Note:
Place near JDIMM1

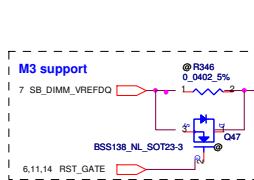


All VREF traces should have 10 mil trace width

<Address(SA1,SA0): 00>
DIMM_1 Reserve H:8mm



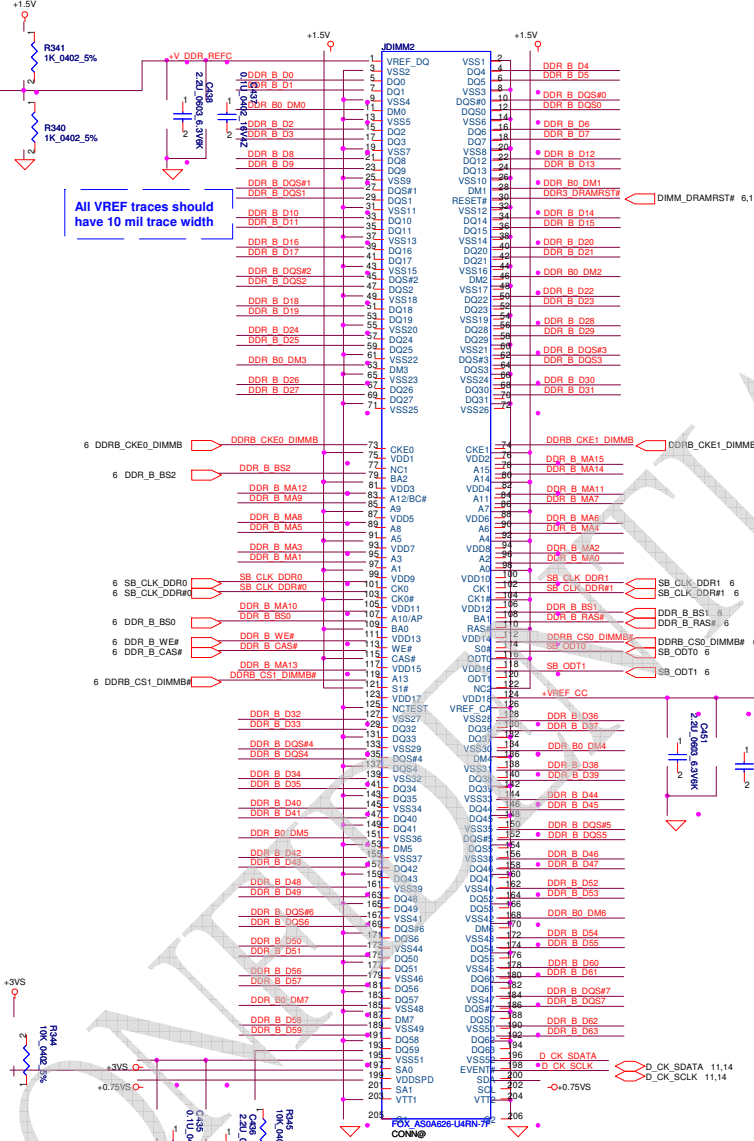
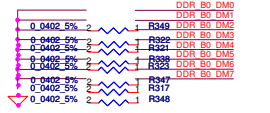
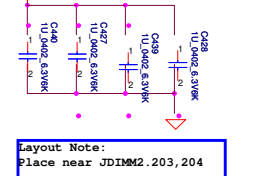
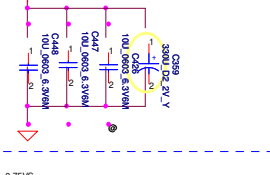
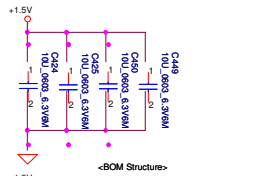
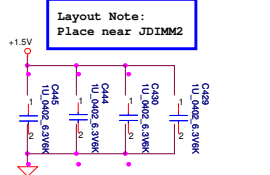
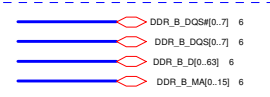
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				DDRIII DIMMA
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				JE50-HR/SJV50-HR M/B Schematics
				Date: Wednesday, October 27, 2010 11 of 61



All VREF traces should have 10 mil trace width

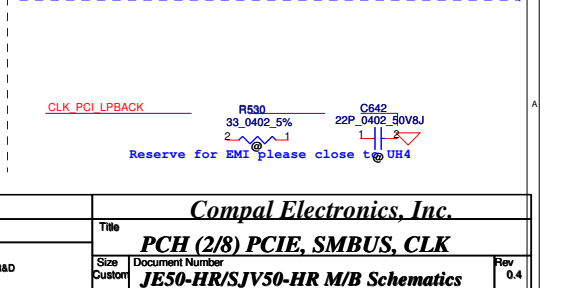
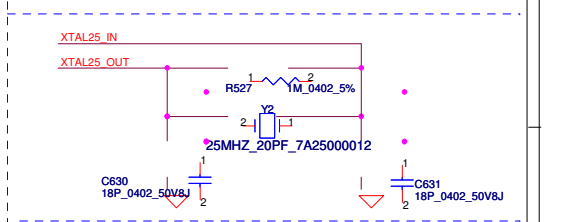
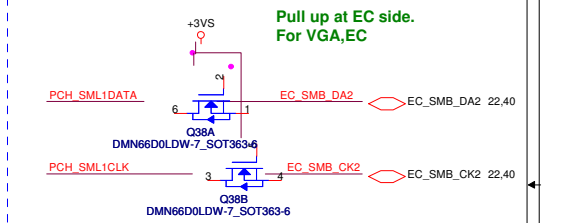
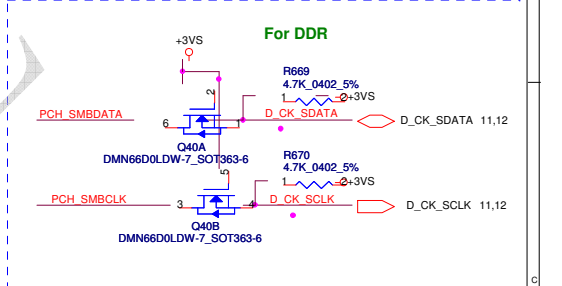
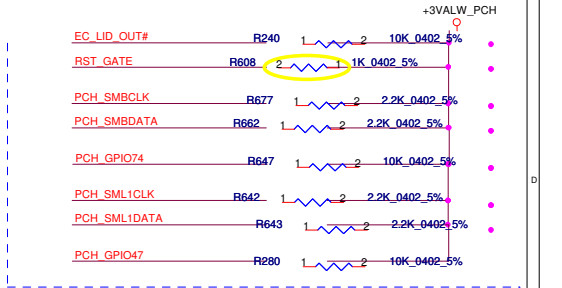
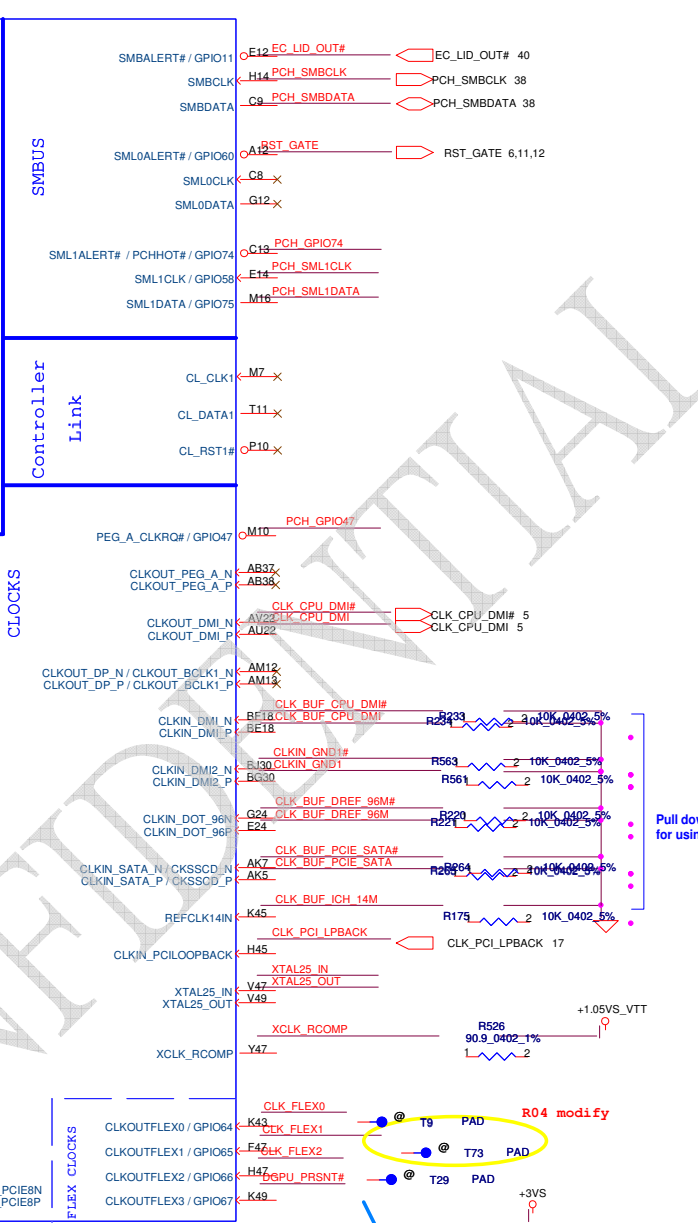
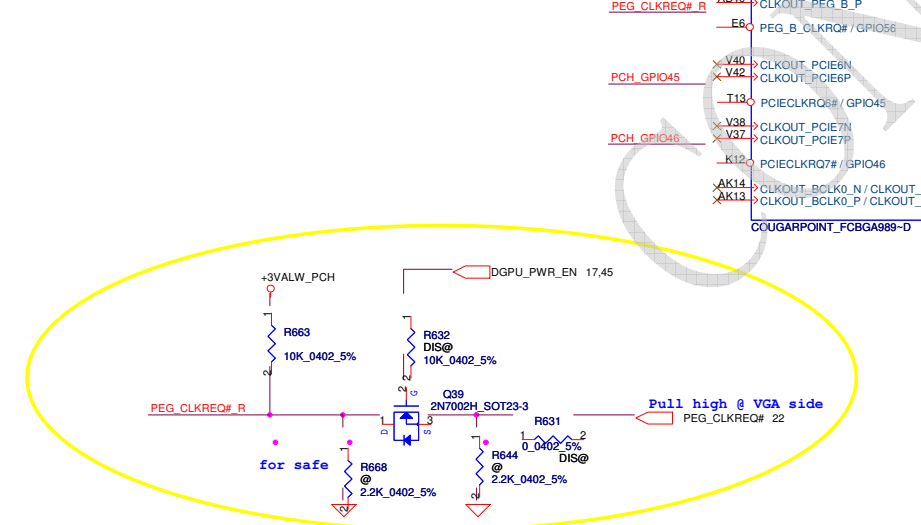
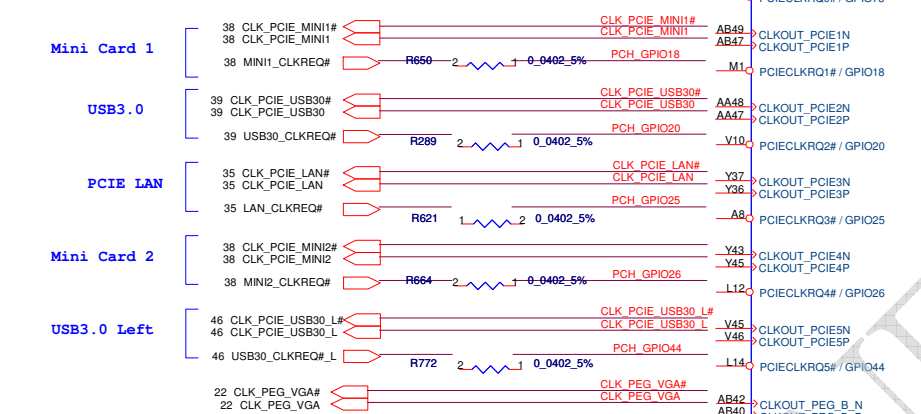
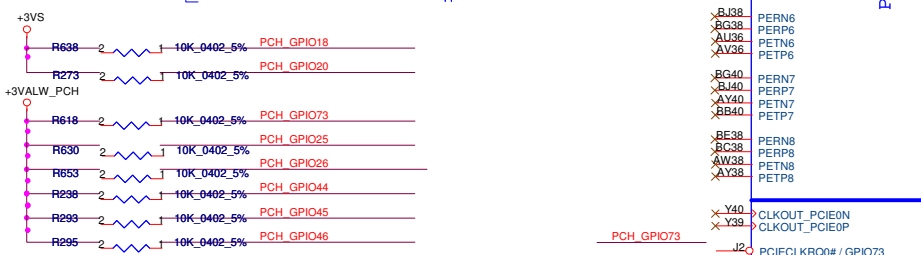
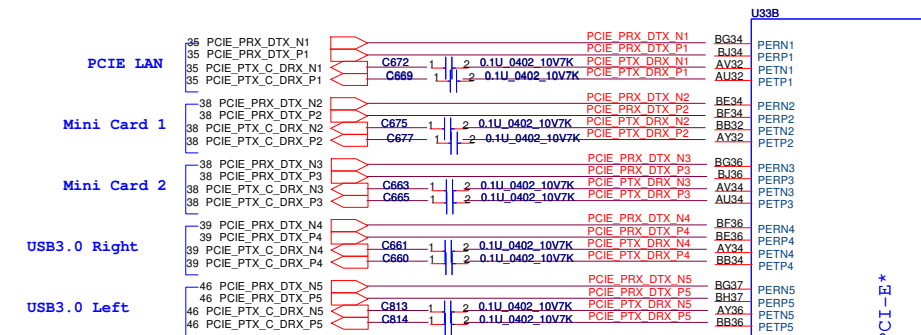
Layout Note: Place near JDIMM2

Layout Note: Place near JDIMM2. 203,204

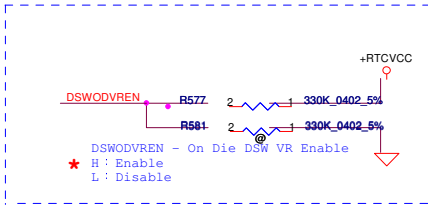
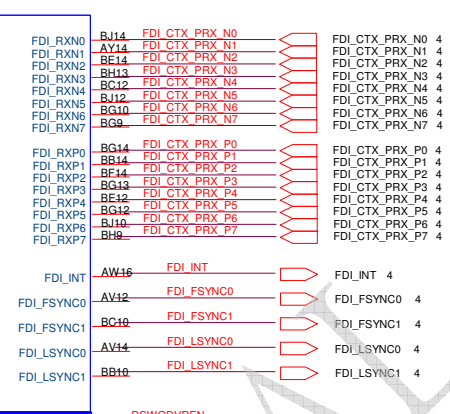
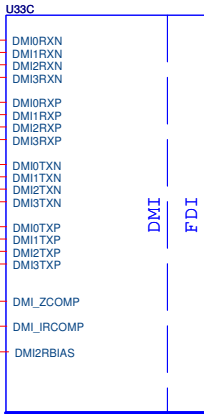
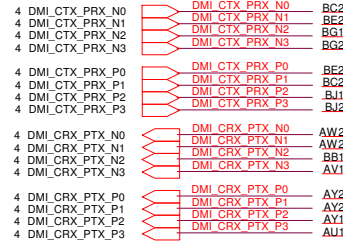
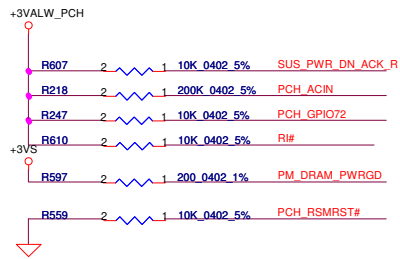


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DIMM_2 Reserve H:4mm

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GPIO67	
DGPU_PRSNT#	
DIS, OPTIMUS	0
UMA	1



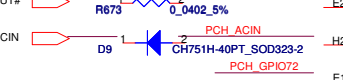
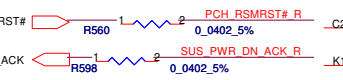
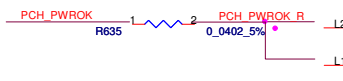
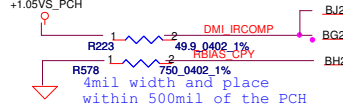
not support Deep S4,S5 mux with SUS_PWR_DN_ACK

not support Deep S4,S5 DPWROK mux with PWROK check list1.0 P.42

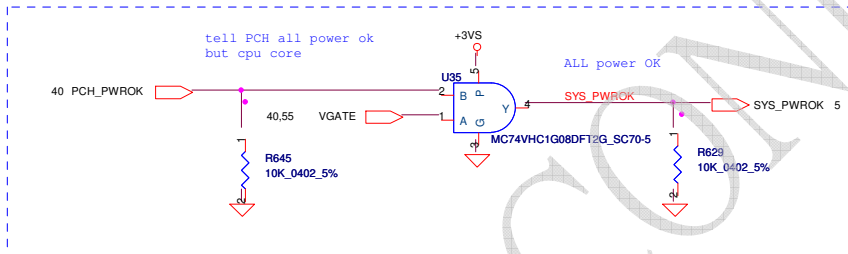
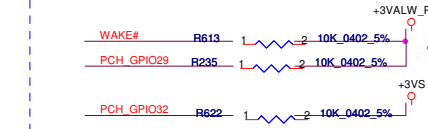
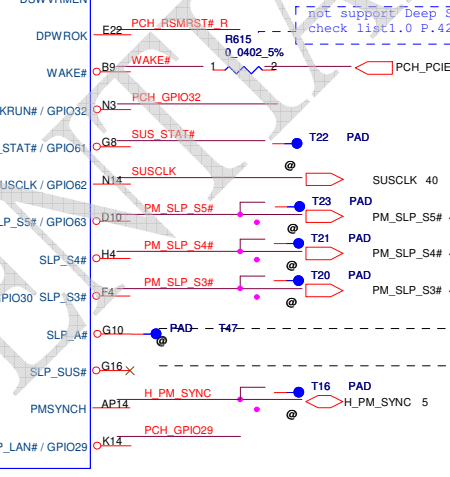
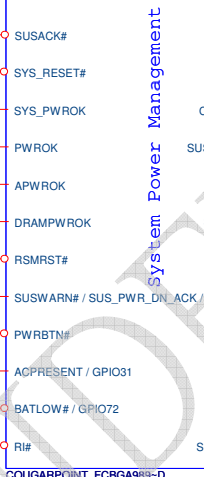
not support AMT APWROK can mux with PWROK (check list1.0 P.40)

Can be left NC when IAMT is not support on the platform

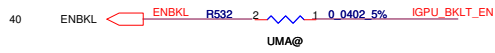
not support Deep S4,S5 can NC PCH ED0S1.2 P.74



Ring Indicator CRB1.0 PH 10K +3VALW



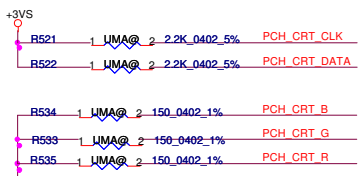
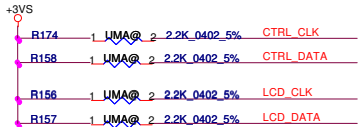
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Size	Customer	Document Number	Date	Sheet
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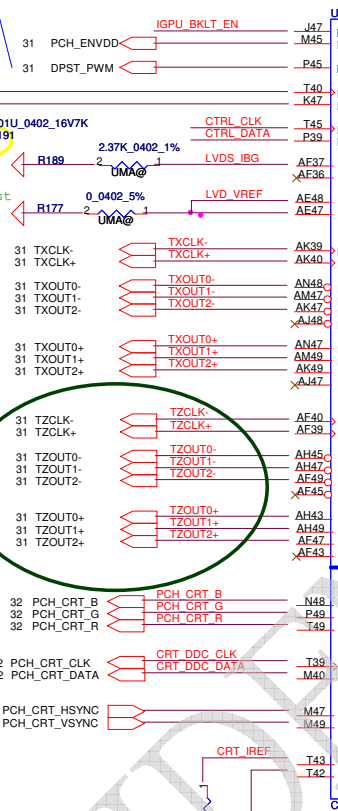
31 LCD_CLK
31 LCD_DATA



For RF request

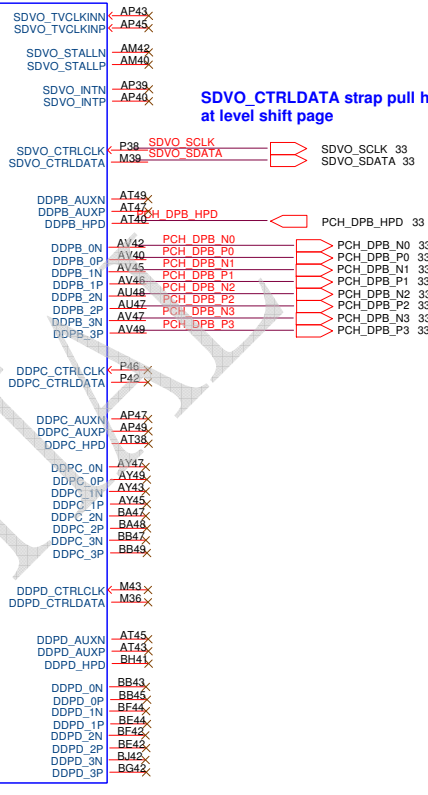


Pull high at LVDS conn side.



U38D
L_BKLTEN
L_VDD_EN
L_BKLTCTL
L_DDC_CLK
L_DDC_DATA
L_CTRL_CLK
L_CTRL_DATA
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3
LVDSB_CLK#
LVDSB_CLK
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN

Digital Display Interface

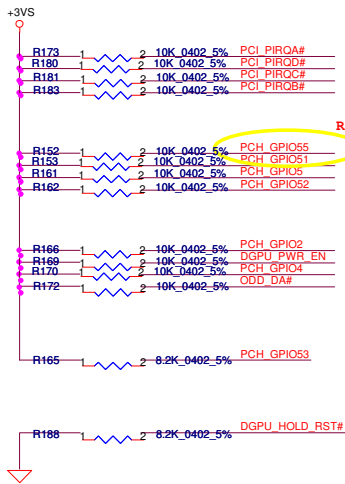


SDVO_CTRLDATA strap pull high at level shift page

HDMI D2
HDMI D1
HDMI D0
HDMI CLK

CONFIDENTIAL

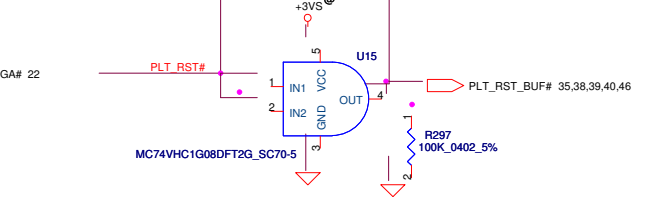
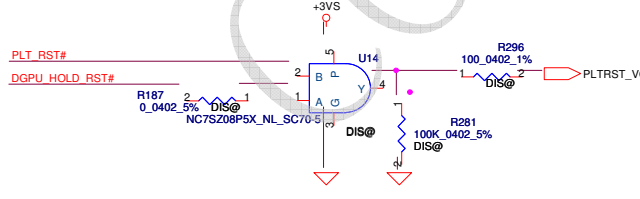
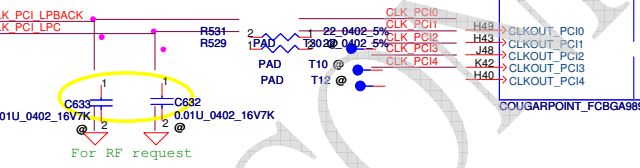
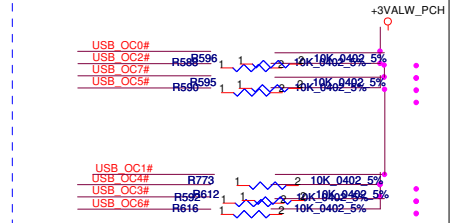
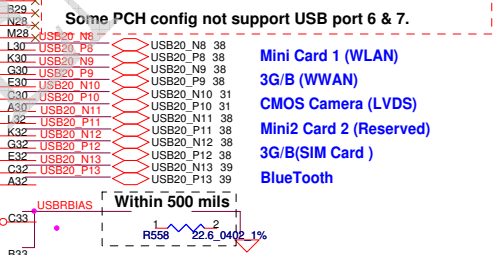
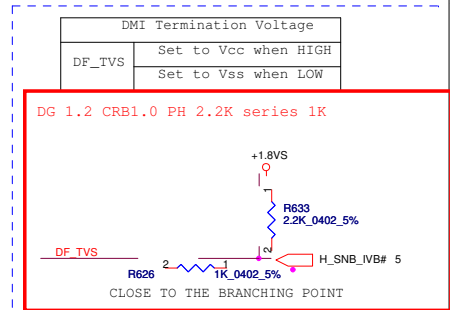
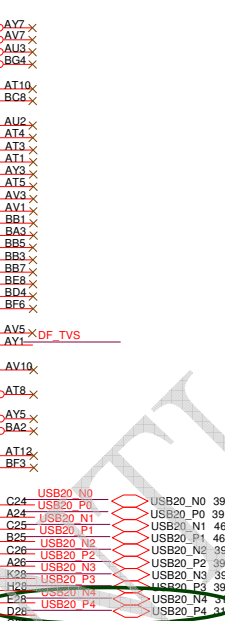
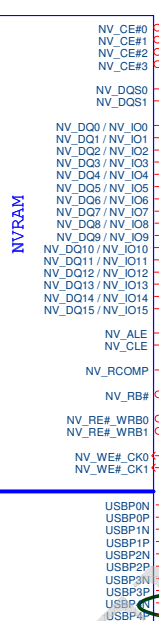
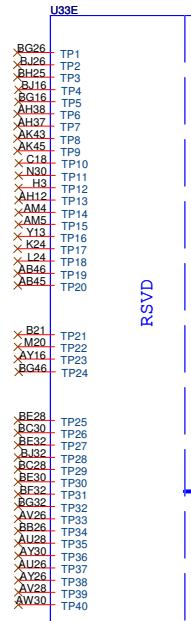
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Customer	Document Number			Rev	
	JES0-HR/SJV50-HR M/B Schematics			0.4	
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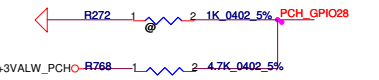
R03 modify

GPIO51 Internal pull high

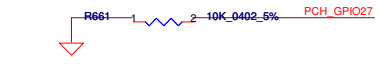
Boot BIOS Strap bit1 BBS1		Boot BIOS Destination	
Bit11	Bit10		
GNT1# / GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC



HDA_SYNC PH(PLL =+1.5VS)
 GPIO28
 On-Die PLL Voltage Regulator
 This signal has a weak internal pull up
 * H : On-Die voltage regulator enable
 L : On-Die PLL Voltage Regulator disable

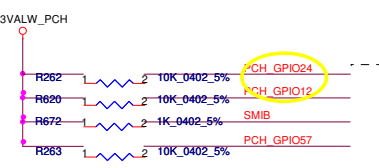
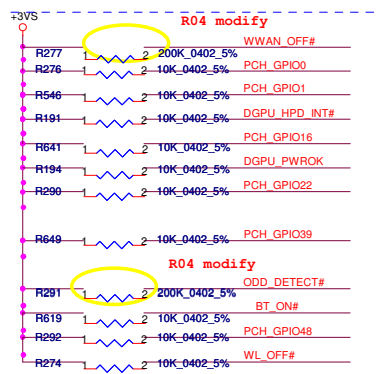


Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal
 No use PD to GND Check list1.0 P.70

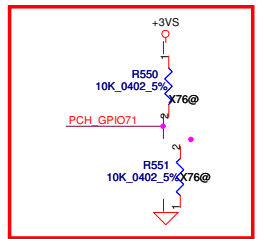
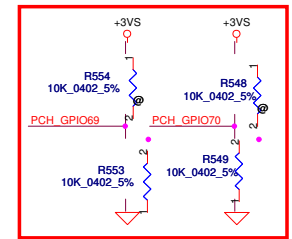
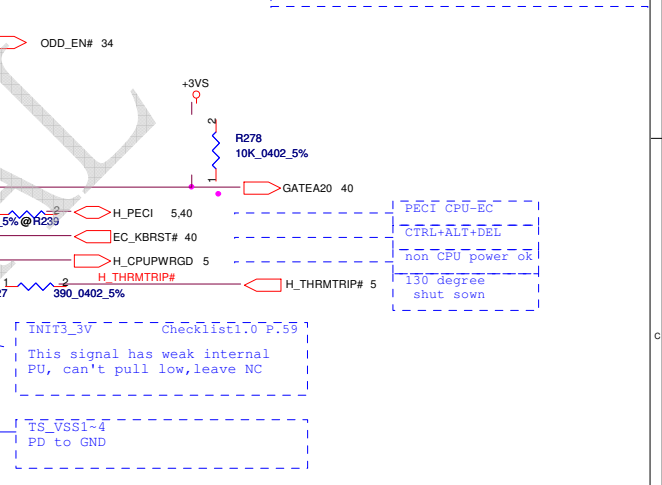
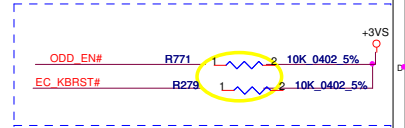
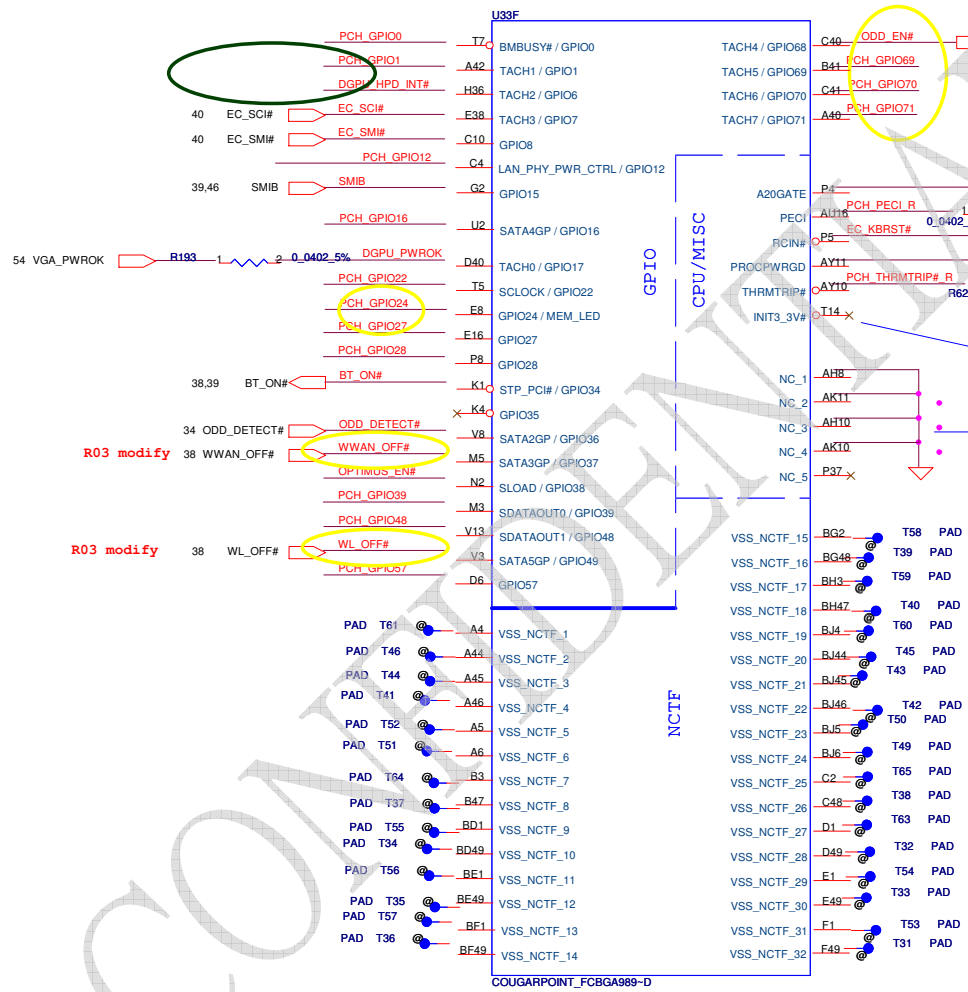


GPIO38
 OPTIMUS_EN#

OPTIMUS	0
Non-OPTIMUS	1



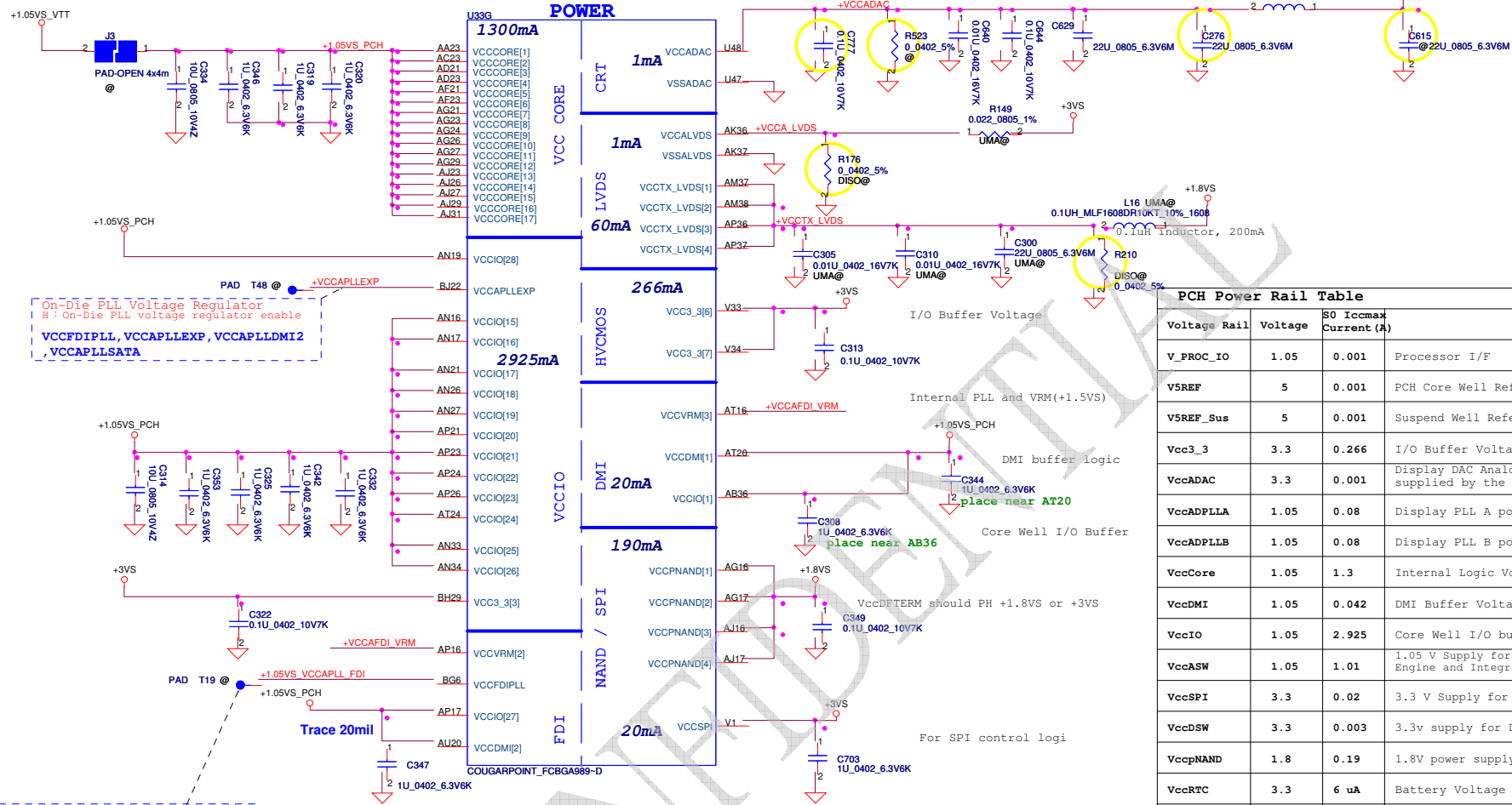
GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
 CRB1.0 PH10K to +3VALW



Project ID	GPIO69	GPIO70
* P5WE0	0	0
P7YE0	0	0
x	1	0
x	1	1

	GPIO71 PCH_GPIO71
*VRAM 800 MHz	0
VRAM 900 MHz	1

+VCCADAC should be powered up during S0 system state. Note that Thermal Sensor shares the same power supply rail with DAC

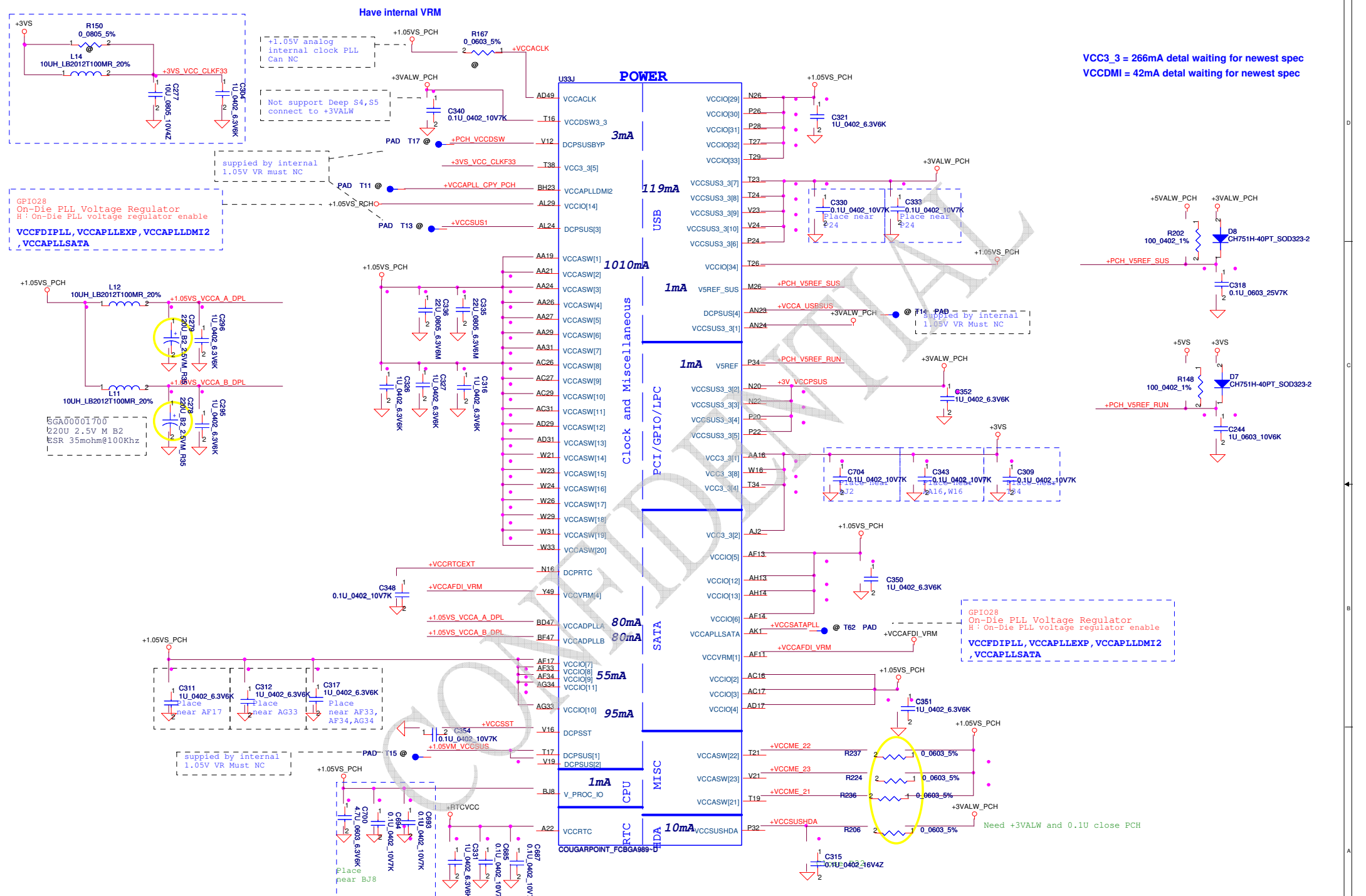


On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

GP1028
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2

+1.5VS
R257 0.0600 5%
+VCCAFDL_VRM
VCCVRM=>1.5V FOR MOBILE
VCCVRM=>1.8V FOR DESKTOP
VCCVRM = 160mA detsal waiting for newest spec
HDA_SYNC PH(PLL) = 1.5VS

PCH Power Rail Table			
Voltage Rail	Voltage	SO Iccmax Current (A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltage
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

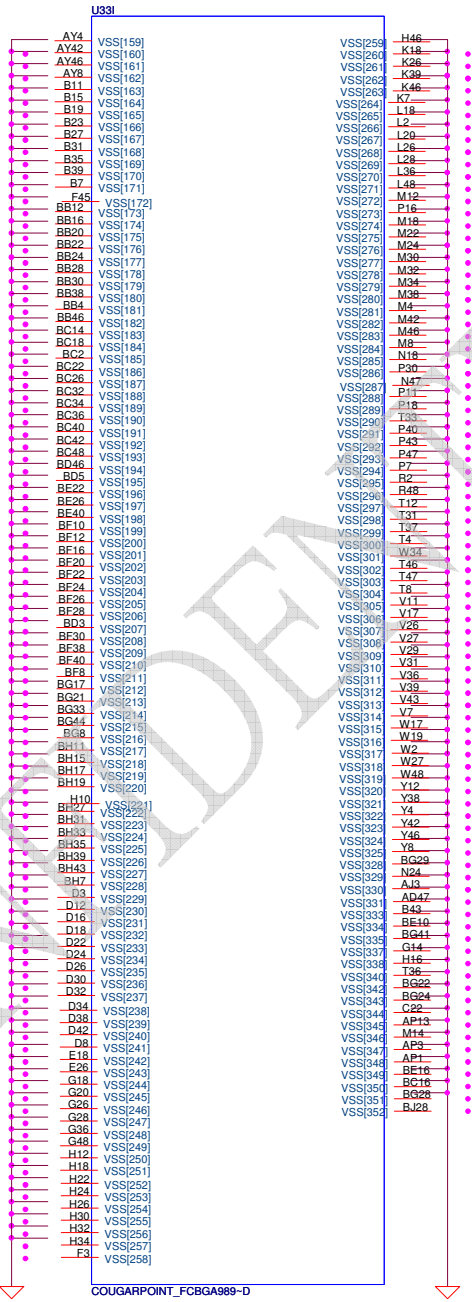
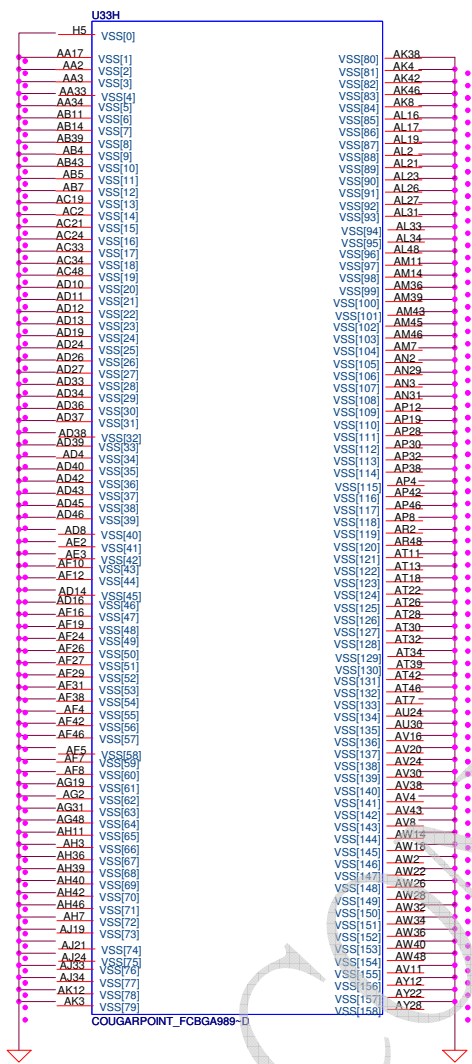


VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

GPIO28
 On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

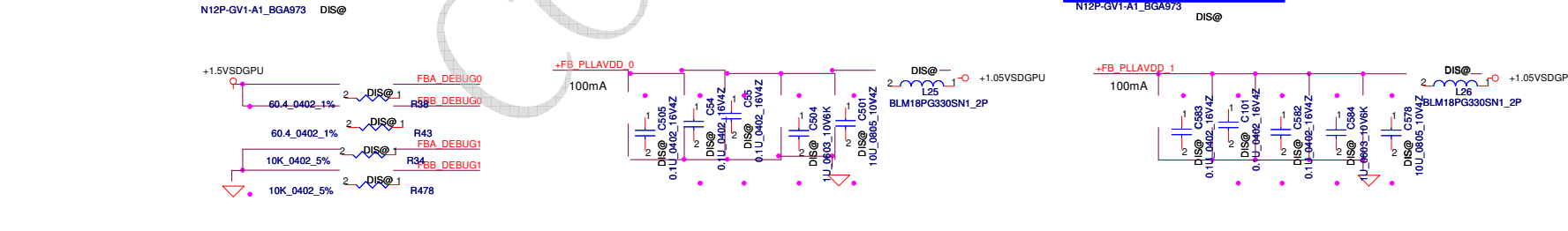
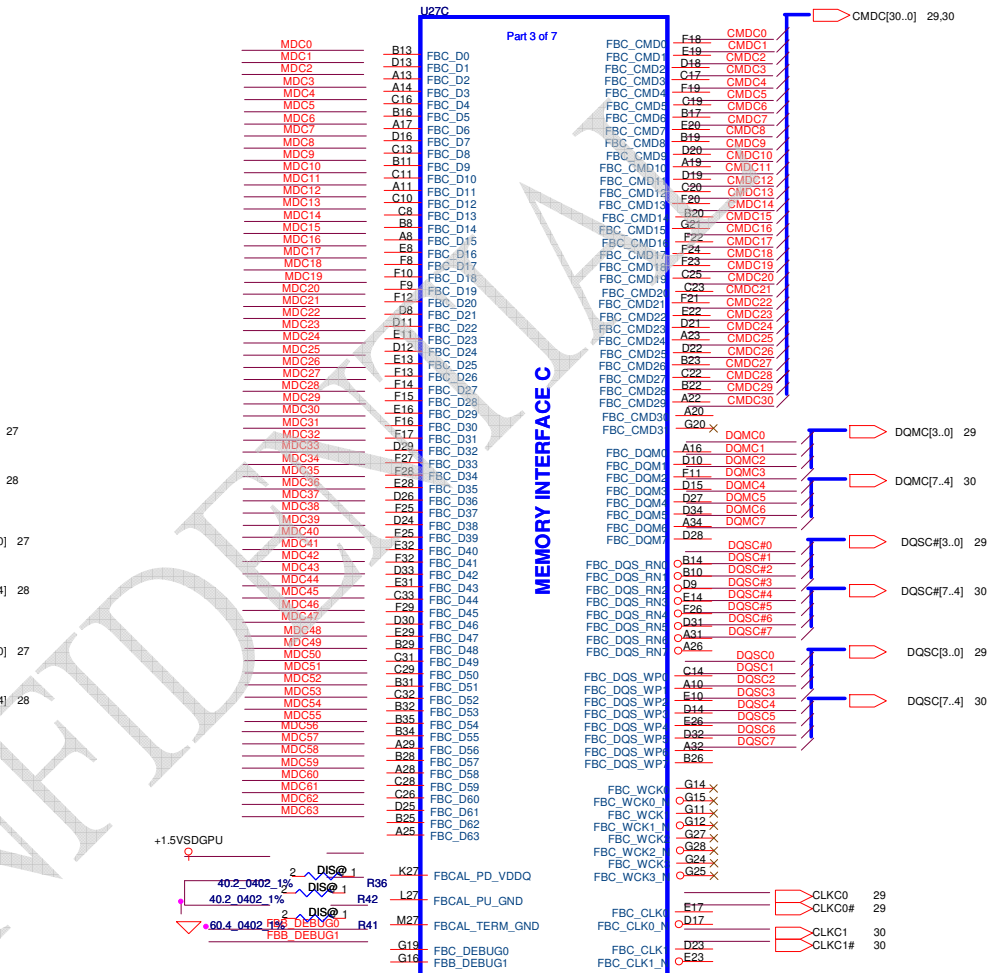
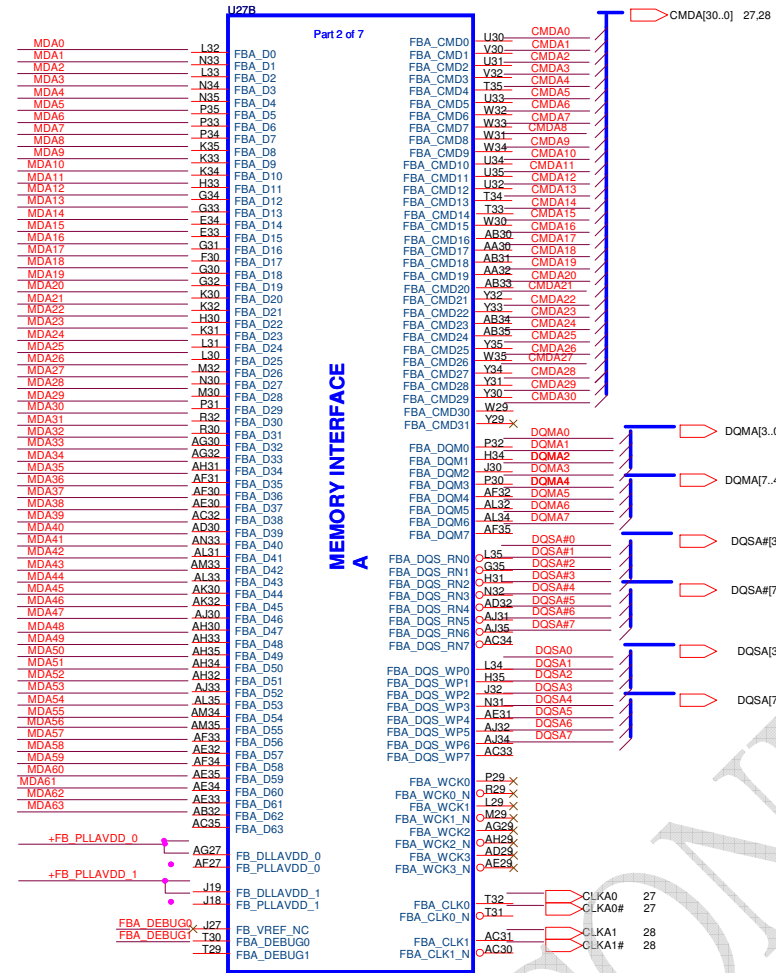
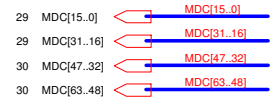
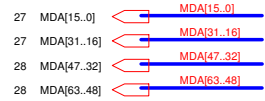
GPIO28
 On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

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VRAM Interface



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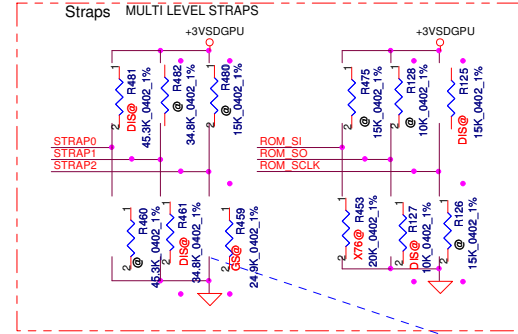
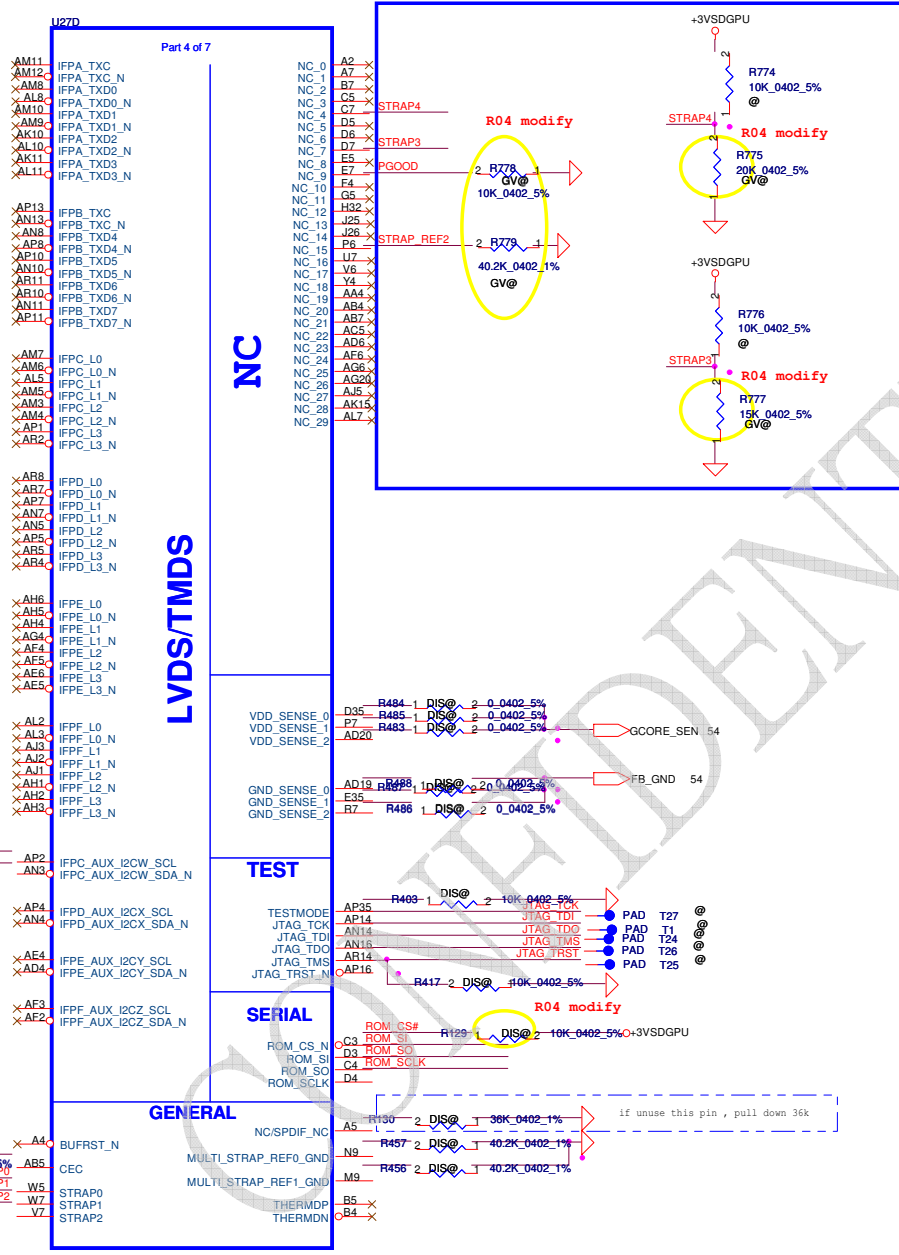
For GB2-128 & GB2b-128 colayout....

For N12P-GV ES strap table

Freq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK	strap3	strap4
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	H 45K	L 15K	H 10K	H 15K	L 15K	L 20K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	H 45K	L 15K	H 10K	H 15K	L 15K	L 20K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	H 45K	L 25K	H 10K	H 15K	L 15K	L 20K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	H 45K	L 45K	H 10K	H 15K	L 15K	L 20K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	H 45K	L 35K	H 10K	H 15K	L 15K	L 20K

For N12P-GV A1 strap table

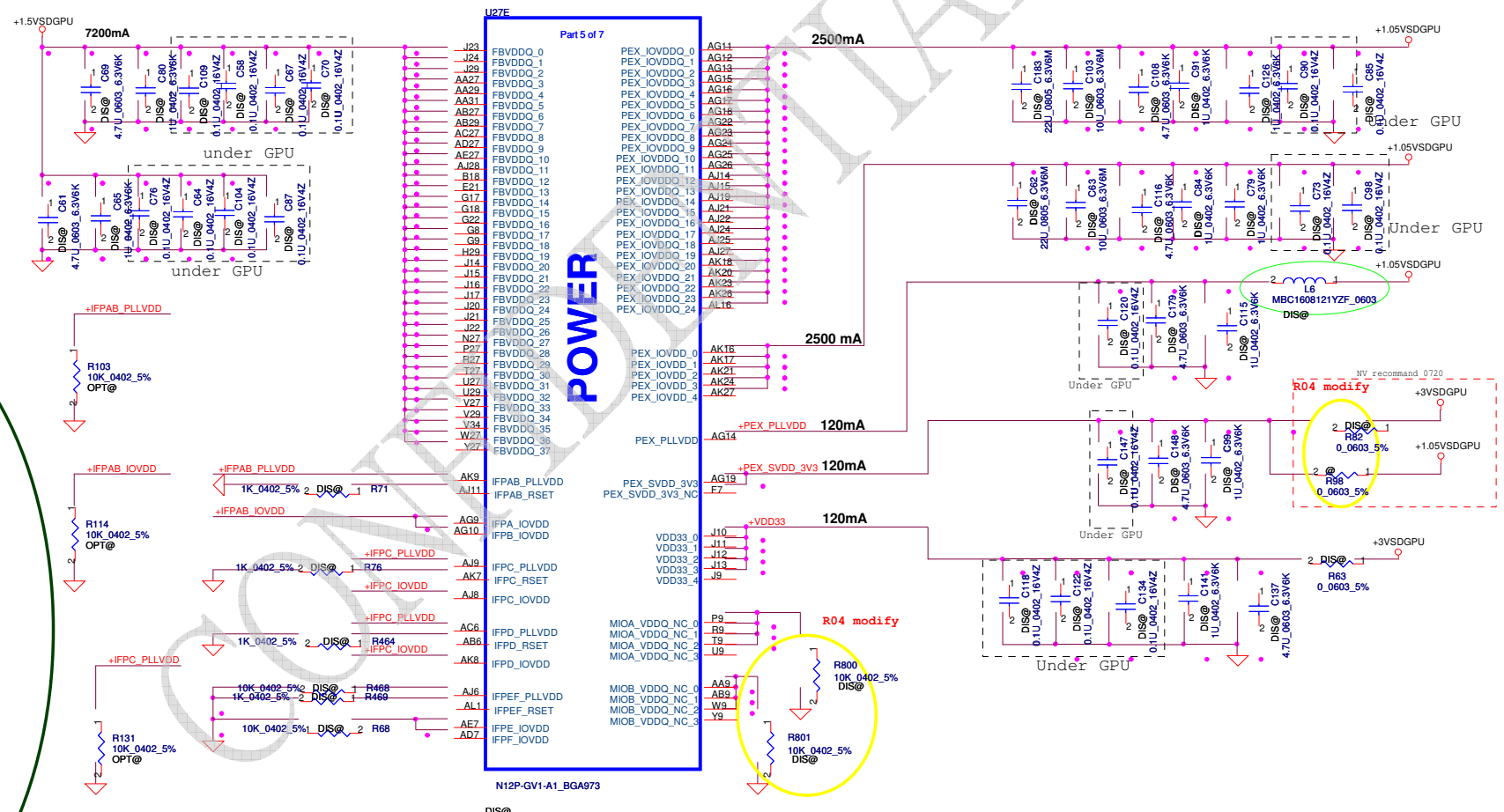
Freq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK	strap3	strap4
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	L 5K	L 15K	H 10K	H 5K	L 15K	L 20K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 5K	L 15K	H 10K	H 5K	L 15K	L 20K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 5K	L 25K	H 10K	H 5K	L 15K	L 20K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 5K	L 45K	H 10K	H 5K	L 15K	L 20K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	L 5K	L 35K	H 10K	H 5K	L 15K	L 20K



For N12P-GS strap table (strap 3 and strap4 left NC)

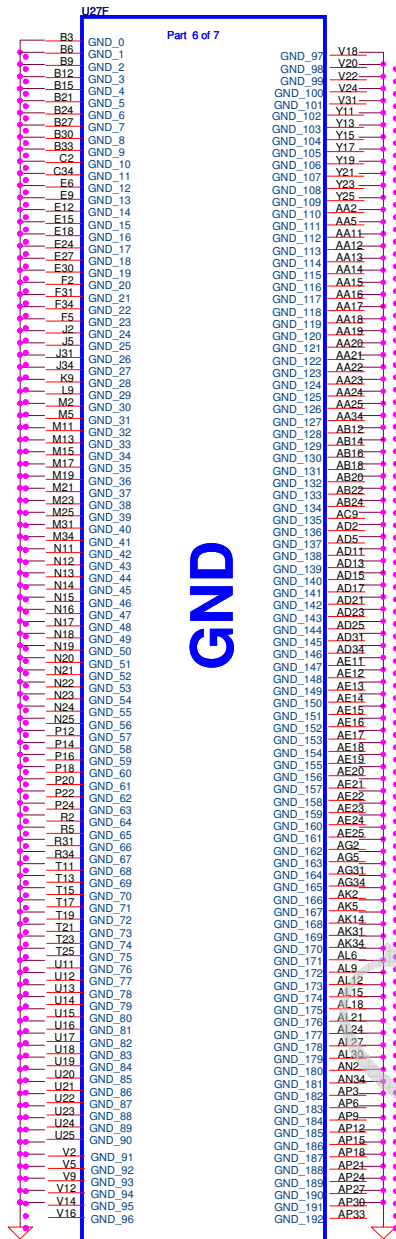
Freq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	L 25K	L 5K	L 10K	H 15K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

GV@ R459 45.3K 0402_1%
Strap 2 for GV1, Pull low 45K Ohm



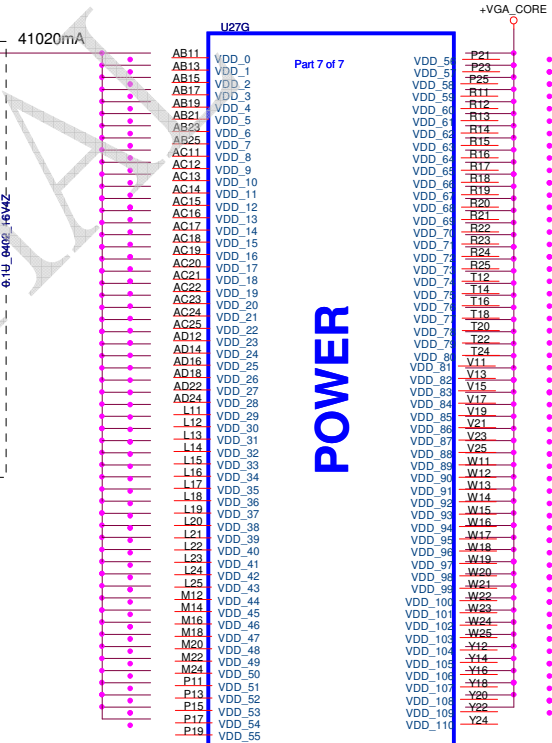
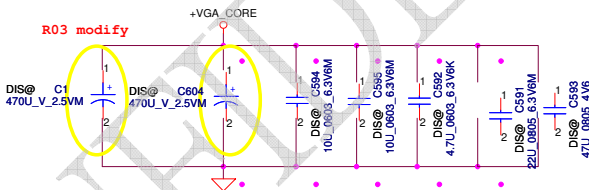
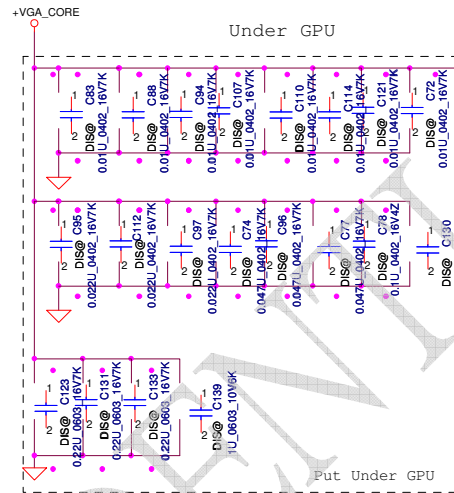
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N12P POWER & GND 4/9		
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N12P-GV1-A1_BGA973

DIS@



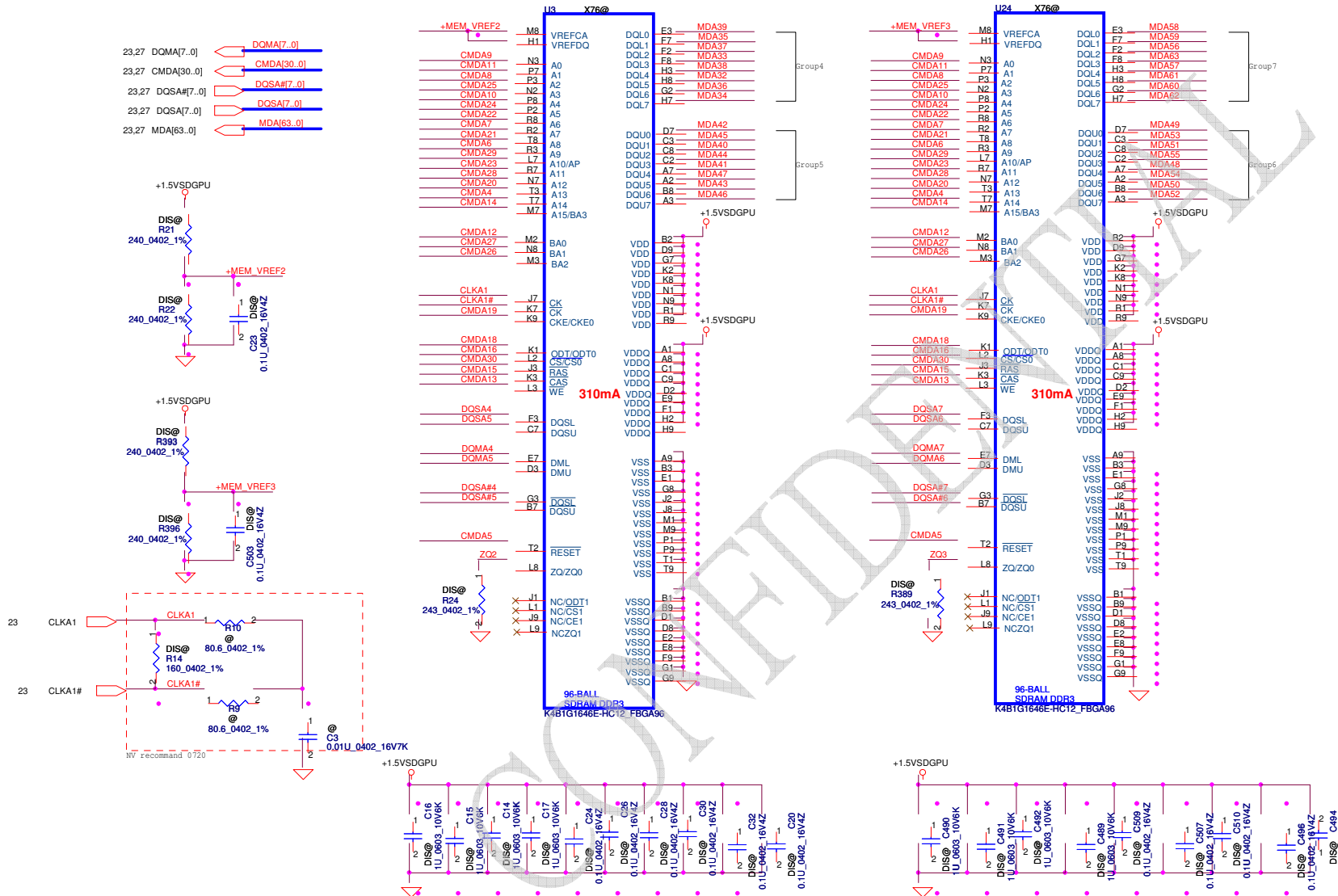
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DIS@

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VRAM DDR3 chips (1GB)

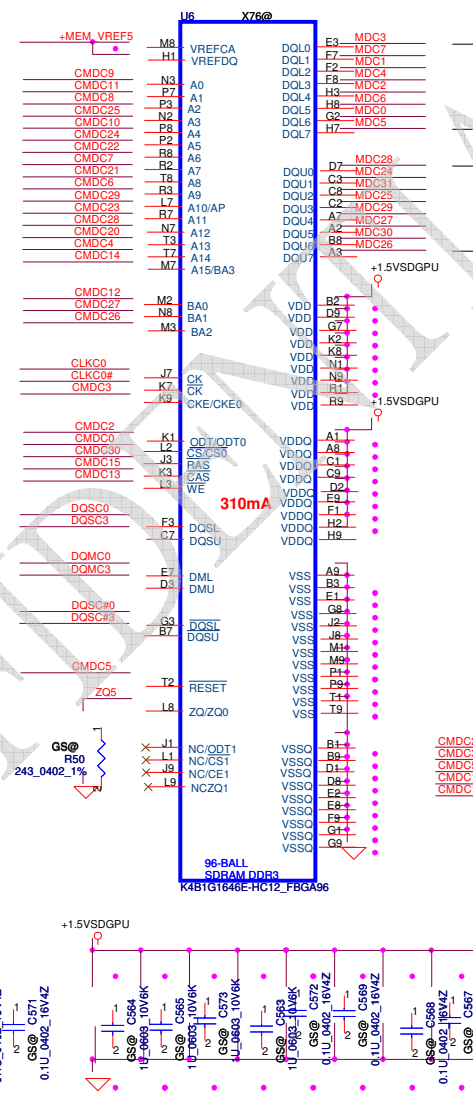
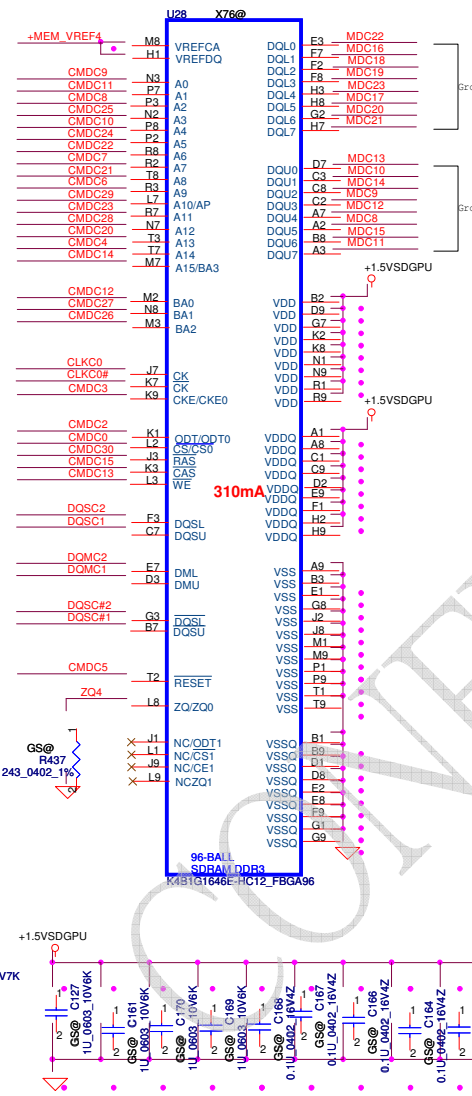
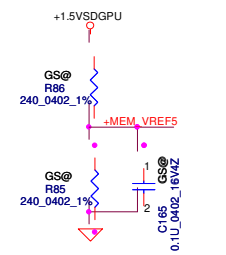
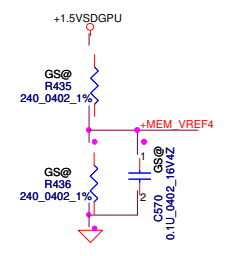
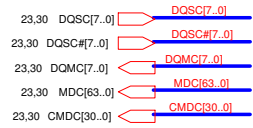
64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

VRAM DDR3 chips (1GB)

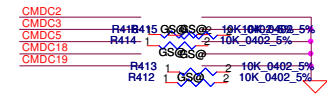
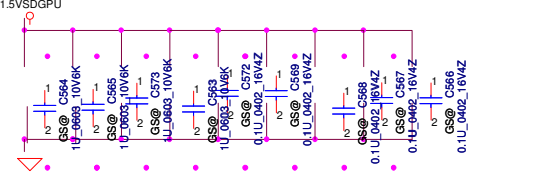
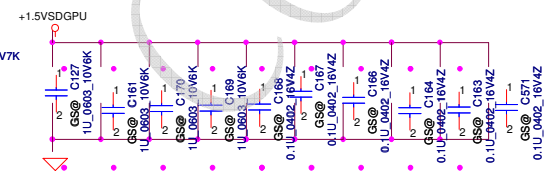
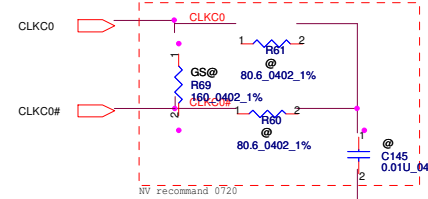
64Mx16 DDR3 *8==>1GB

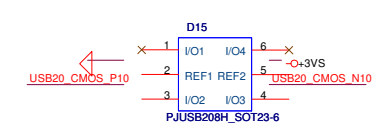
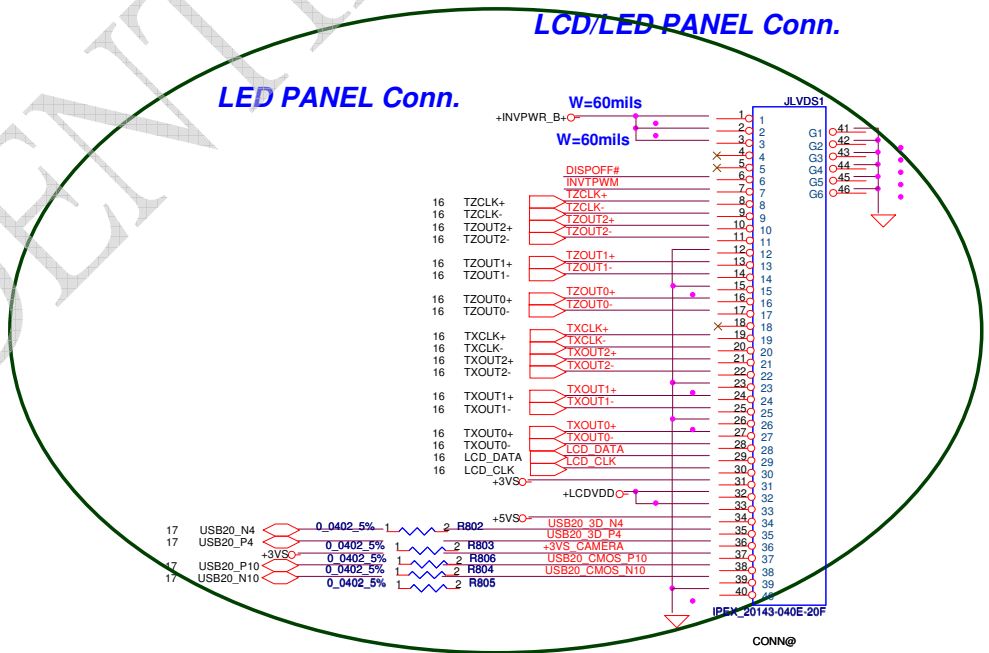
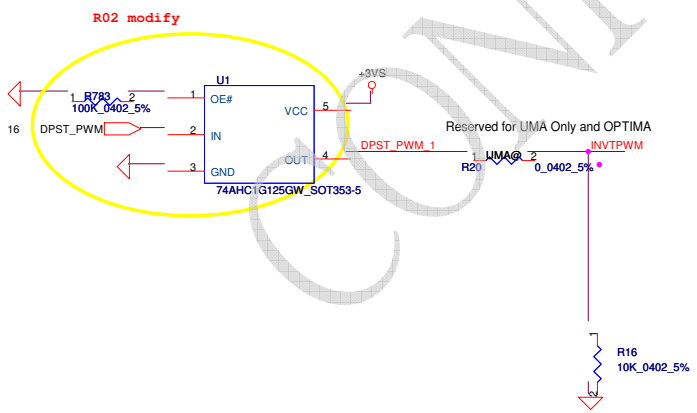
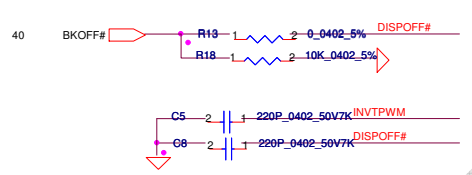
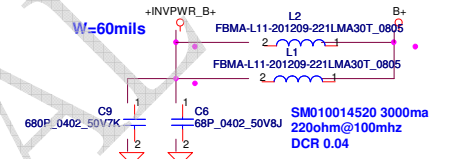
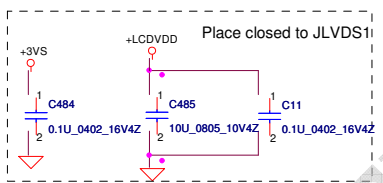
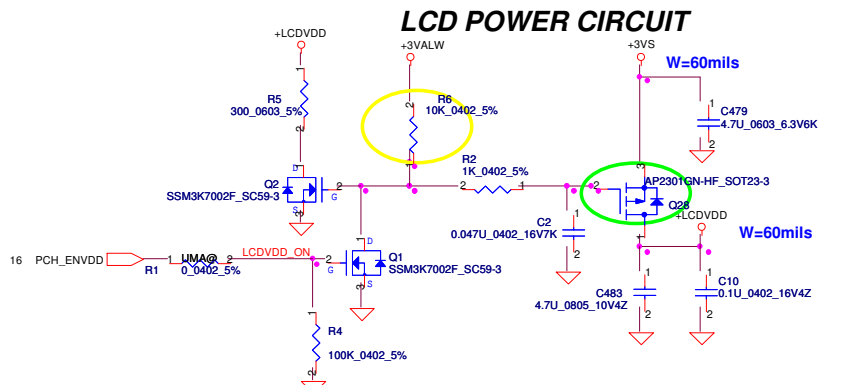


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

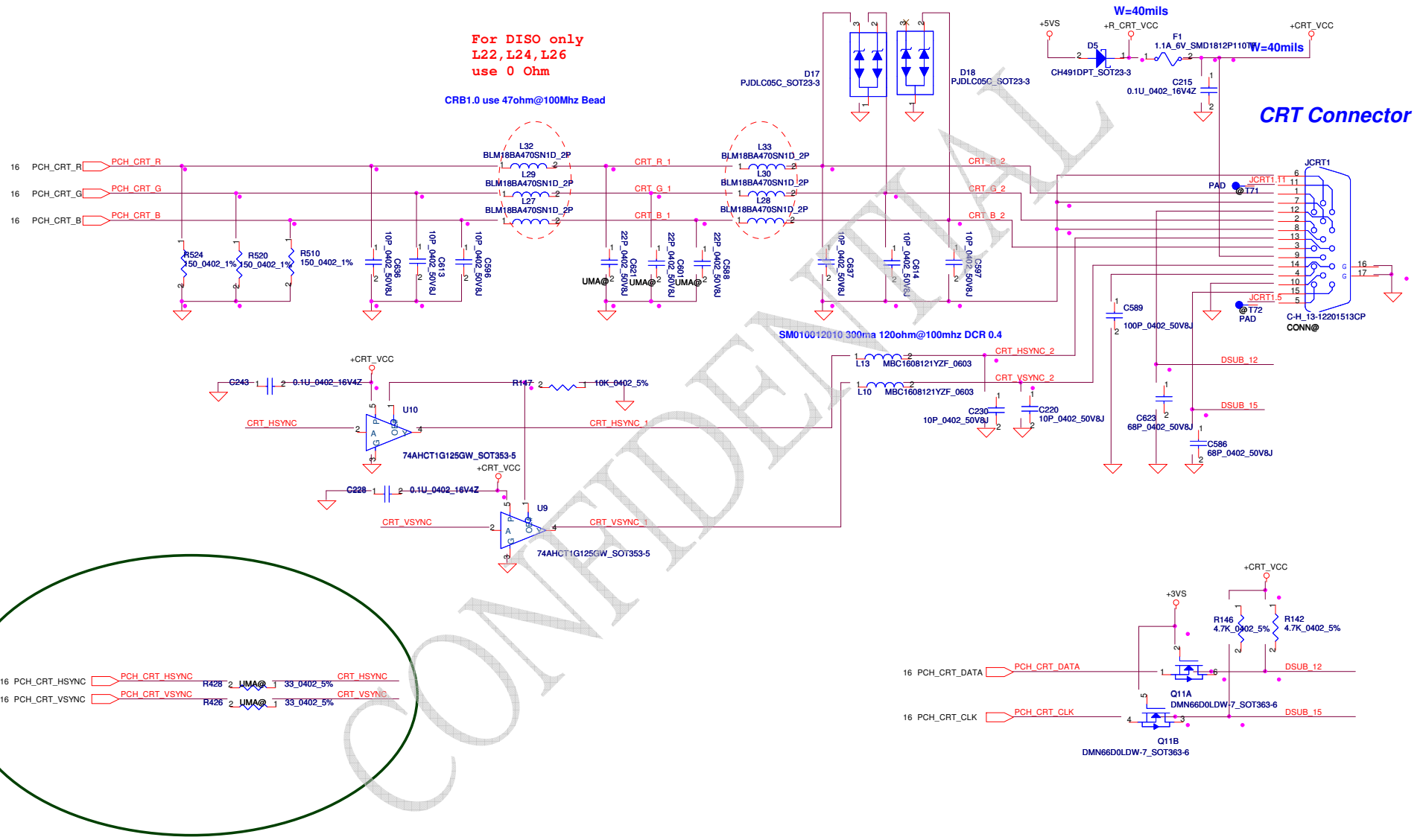
LOW HIGH

Command Bit	Default Pull-down
ODT#	10k
CKE#	10k
RST	10k
CAS*	No Termination





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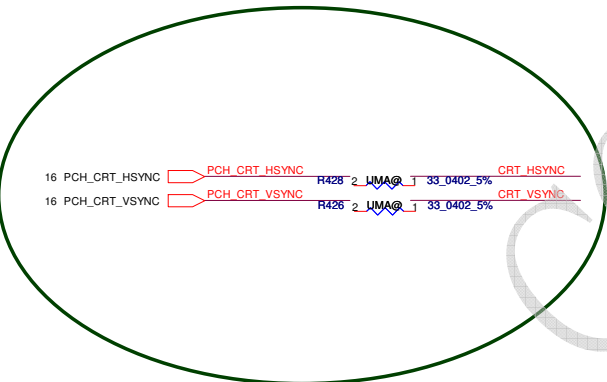


For DISO only
L22, L24, L26
use 0 Ohm

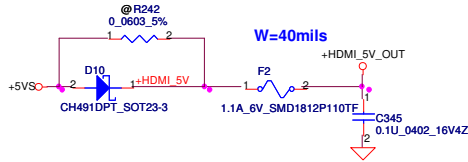
CRB1.0 use 470hm@100Mhz Bead

W=40mils

CRT Connector

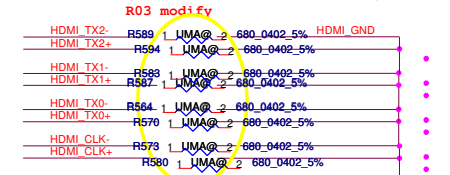
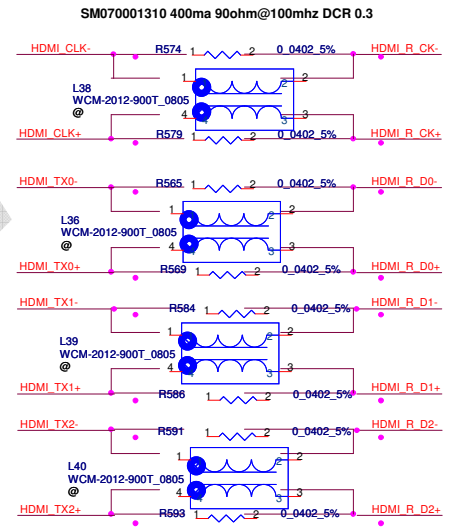
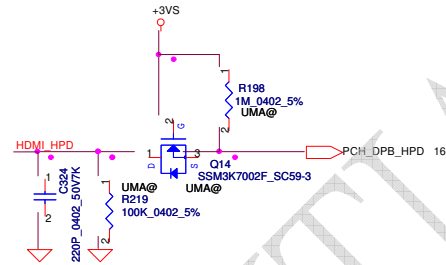


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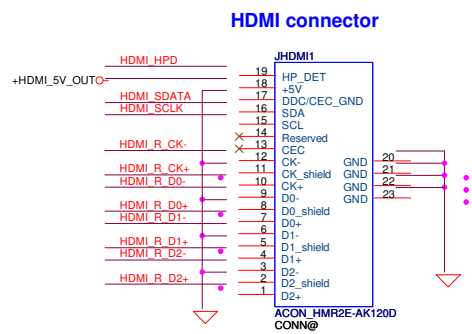
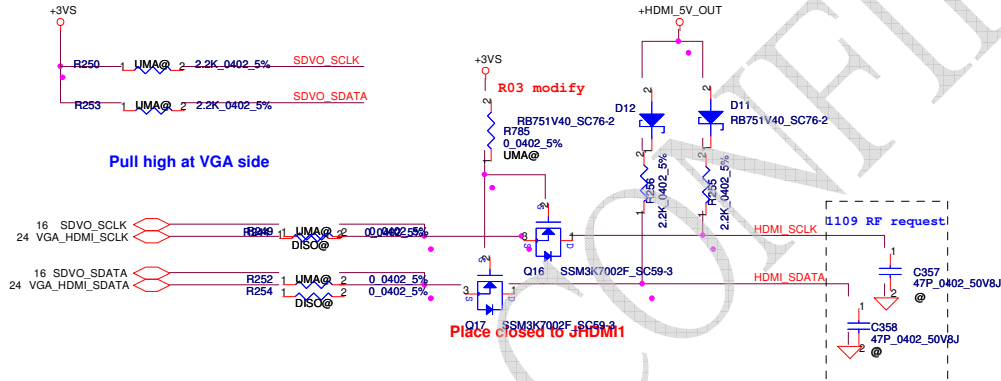
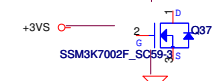
UMA

16 PCH_DPB_N0	C280	UMA@	2	0.1U_0402_10V7K	HDMI TX2-
16 PCH_DPB_P0	C281	UMA@	2	0.1U_0402_10V7K	HDMI TX2+
16 PCH_DPB_N1	C283	UMA@	2	0.1U_0402_10V7K	HDMI TX1-
16 PCH_DPB_P1	C282	UMA@	2	0.1U_0402_10V7K	HDMI TX1+
16 PCH_DPB_N2	C287	UMA@	2	0.1U_0402_10V7K	HDMI TX0-
16 PCH_DPB_P2	C286	UMA@	2	0.1U_0402_10V7K	HDMI TX0+
16 PCH_DPB_N3	C285	UMA@	2	0.1U_0402_10V7K	HDMI CLK-
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INTEL use 680 Ohm for termination in DG 1.5

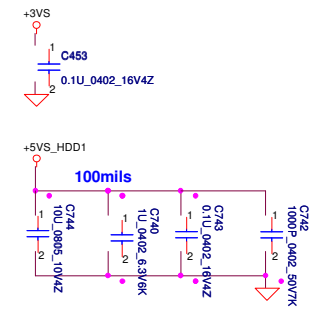
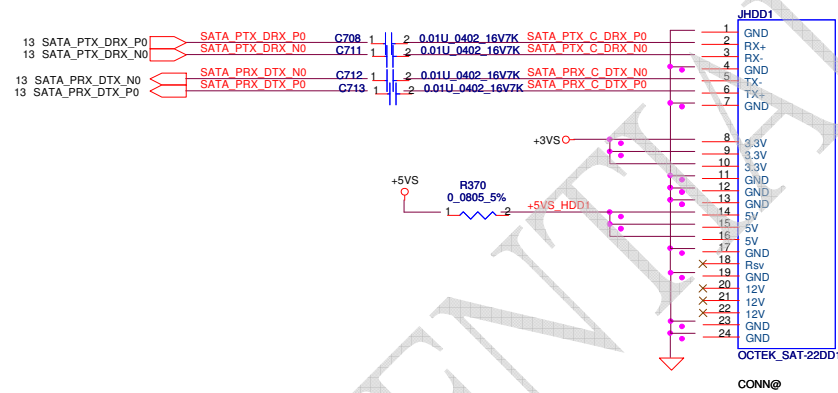
NV use 499 Ohm for termination



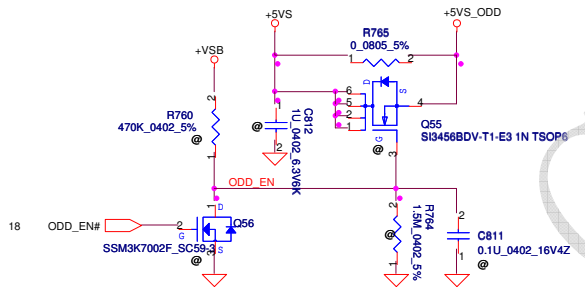
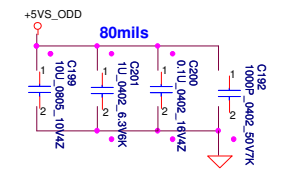
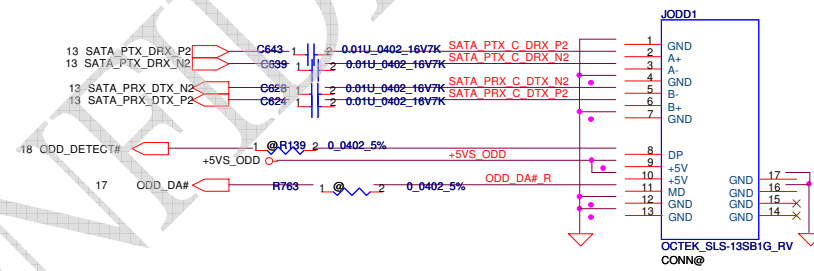
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SATA HDD1 Conn.

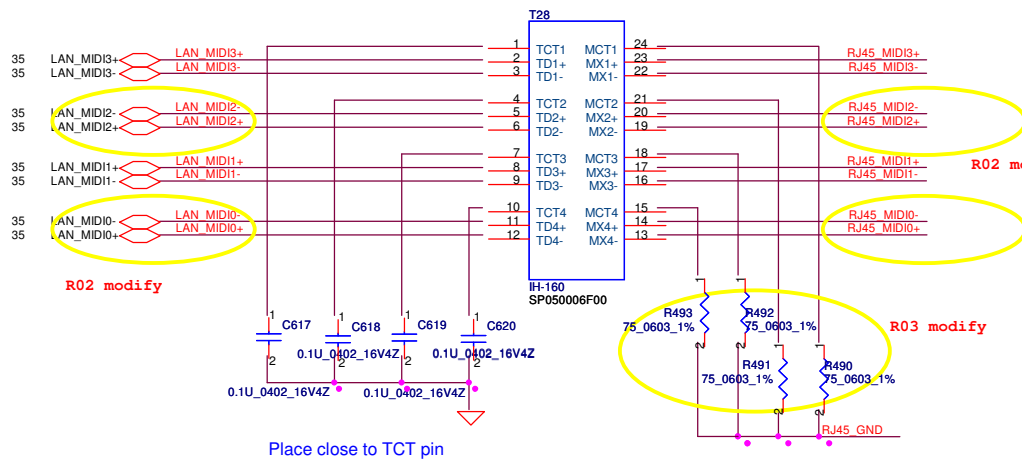
CL 4.0 mm



SATA ODD Conn.

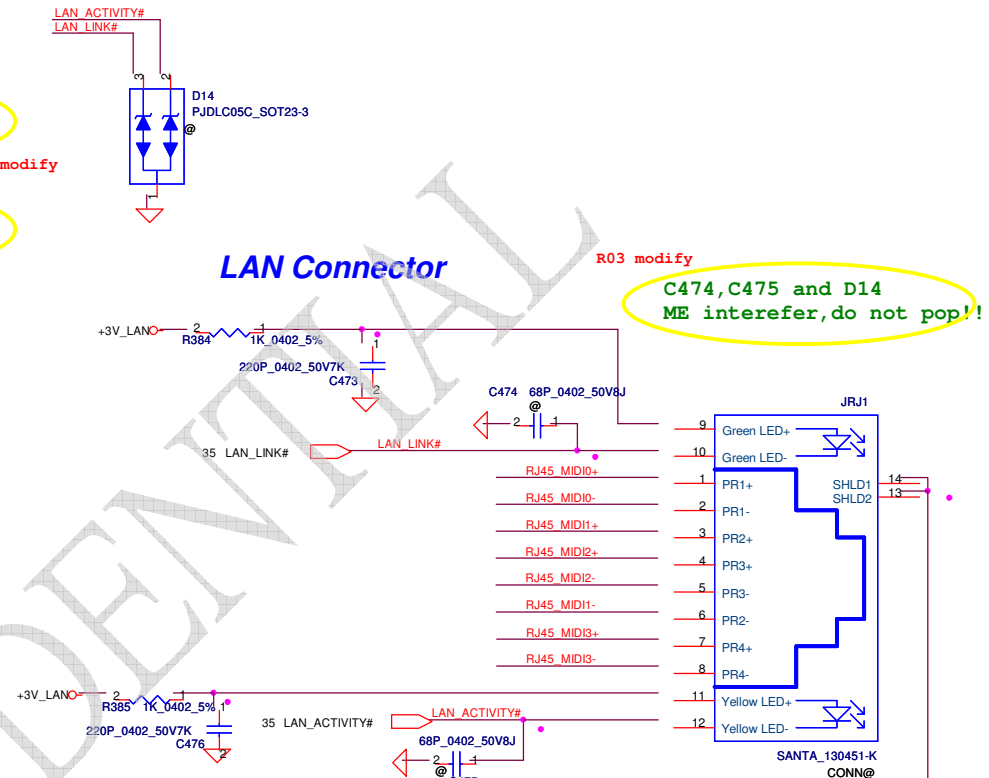


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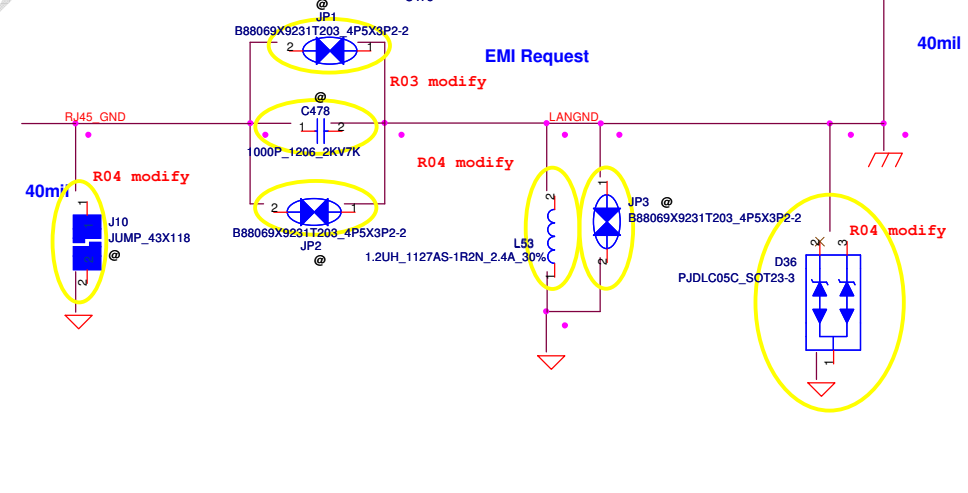
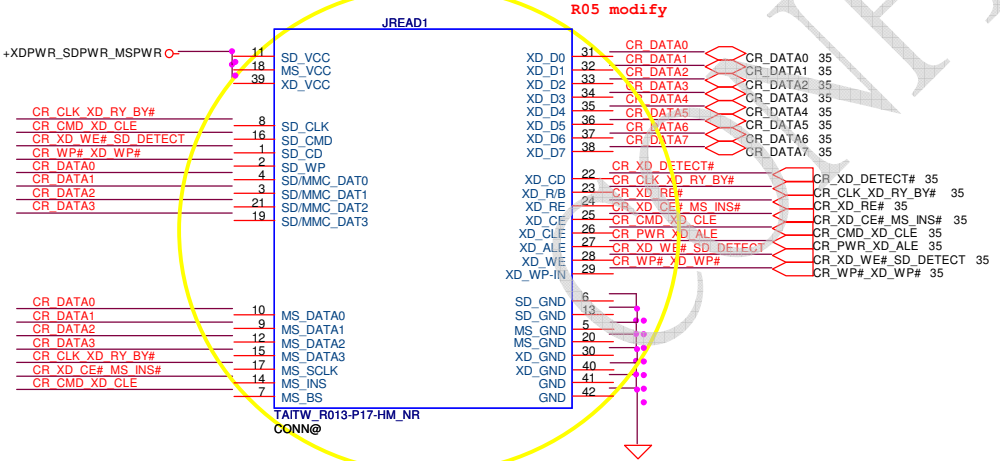


BOTHHAND: S X'FORM_GST5009-D L F LAN, SP050006B00
 TIMAG:S X'FORM_IH-160 LAN , SP050006F00

LAN Connector



Card Reader Connector

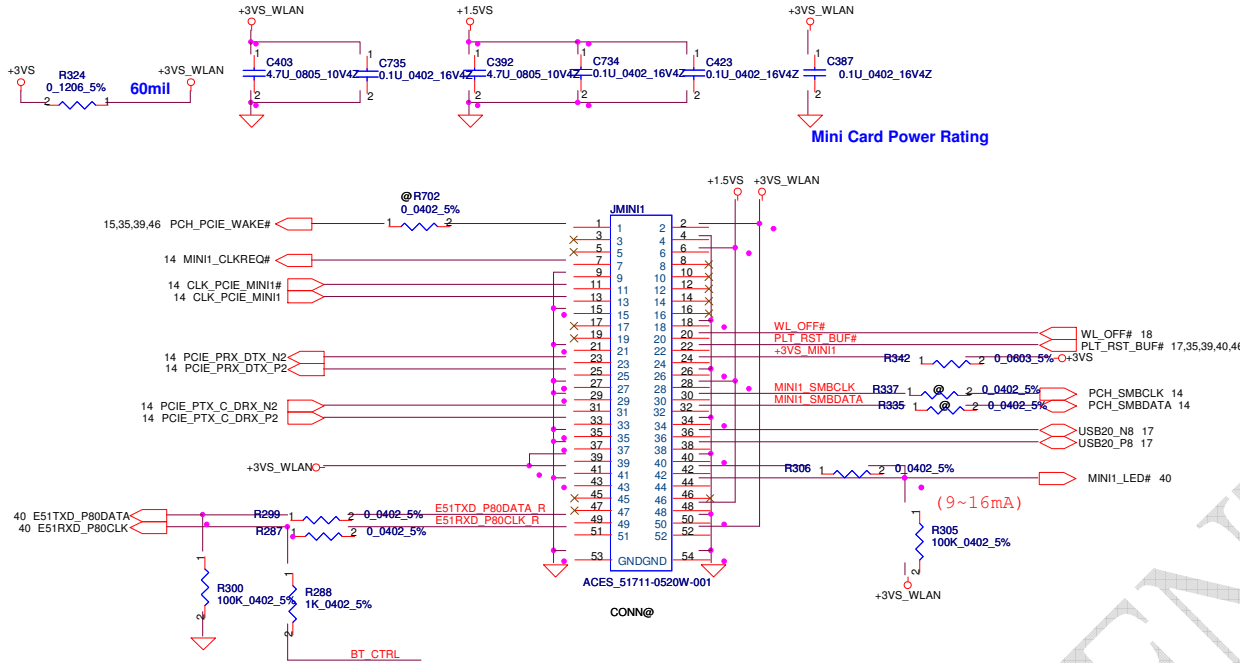


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				Custom	JE50-HR/SJV50-HR M/B Schematics
				Date:	Wednesday, October 27, 2010
				Sheet	36 of 61

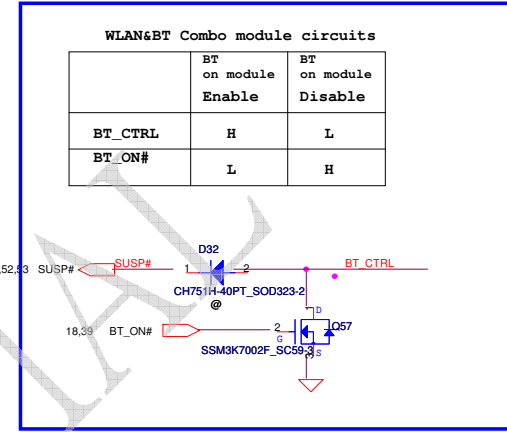
CONFIDENTIAL

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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				Custom	JE50-HR/SJV50-HR M/B Schematics	0.4
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For Wireless LAN



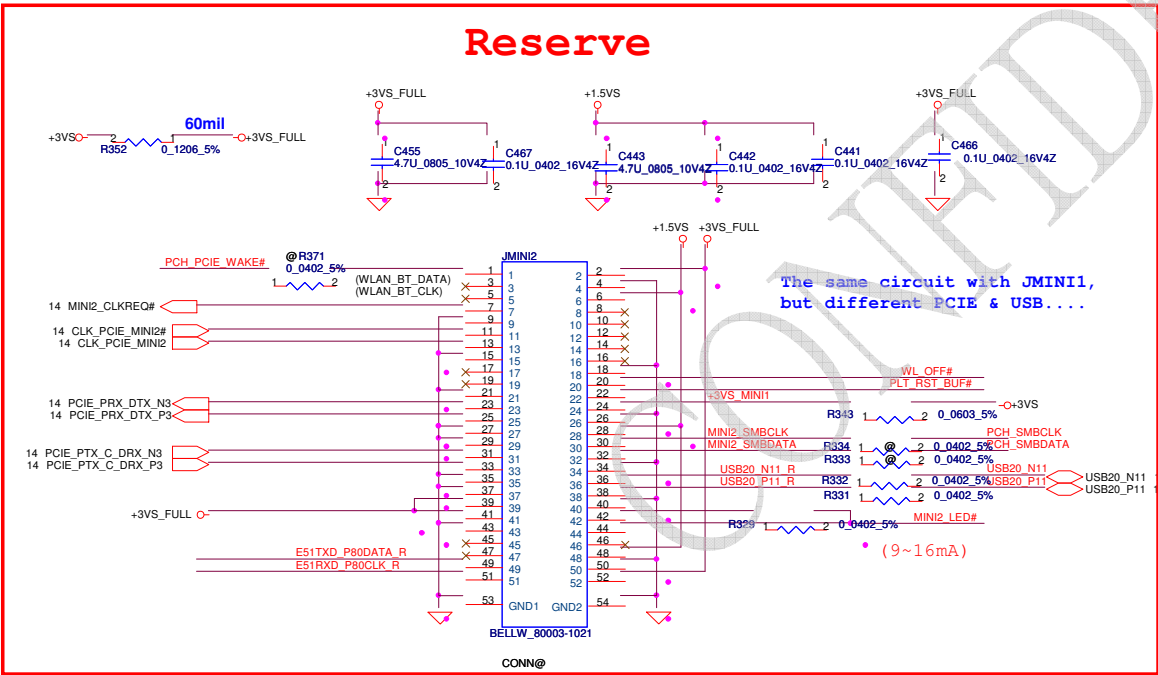
Mini Card Power Rating



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

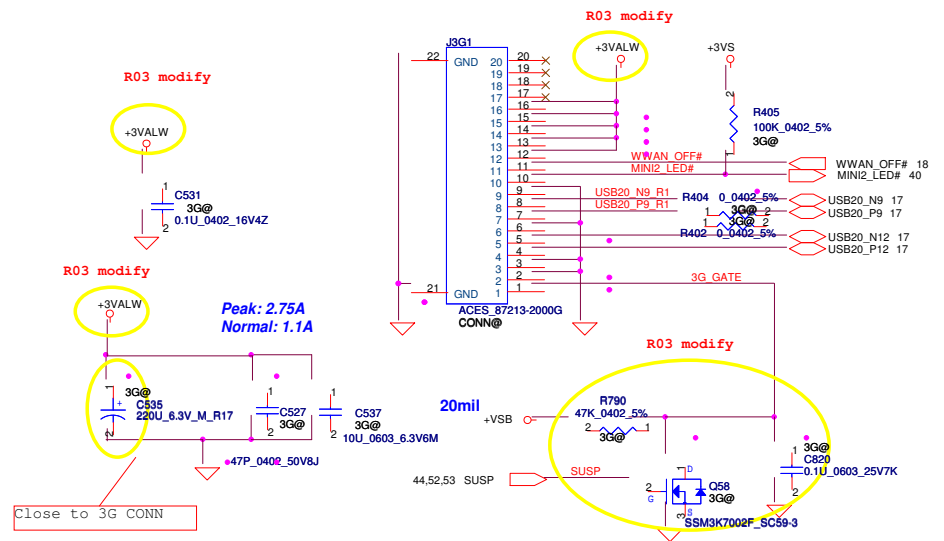
Reserve



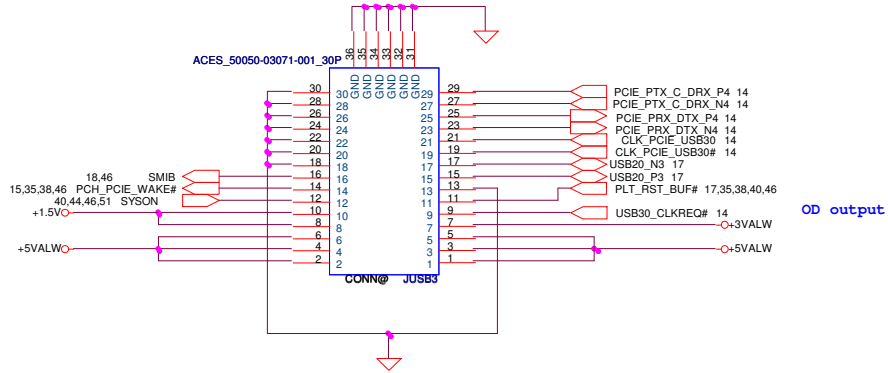
The same circuit with JMINI1, but different PCIE & USB....

For 3G / GPS

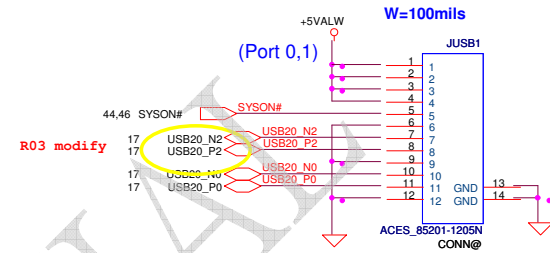
To 3G Module Connect



USB3.0 Conn.

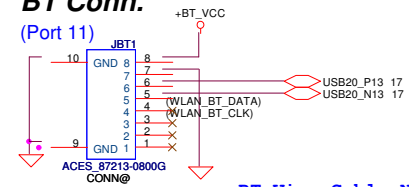


USB/B Conn.

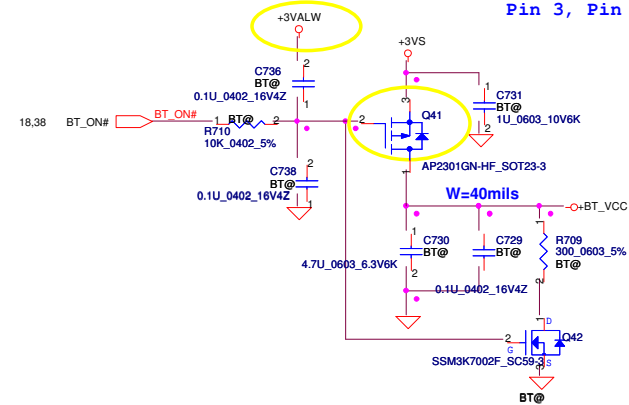


BT Conn.

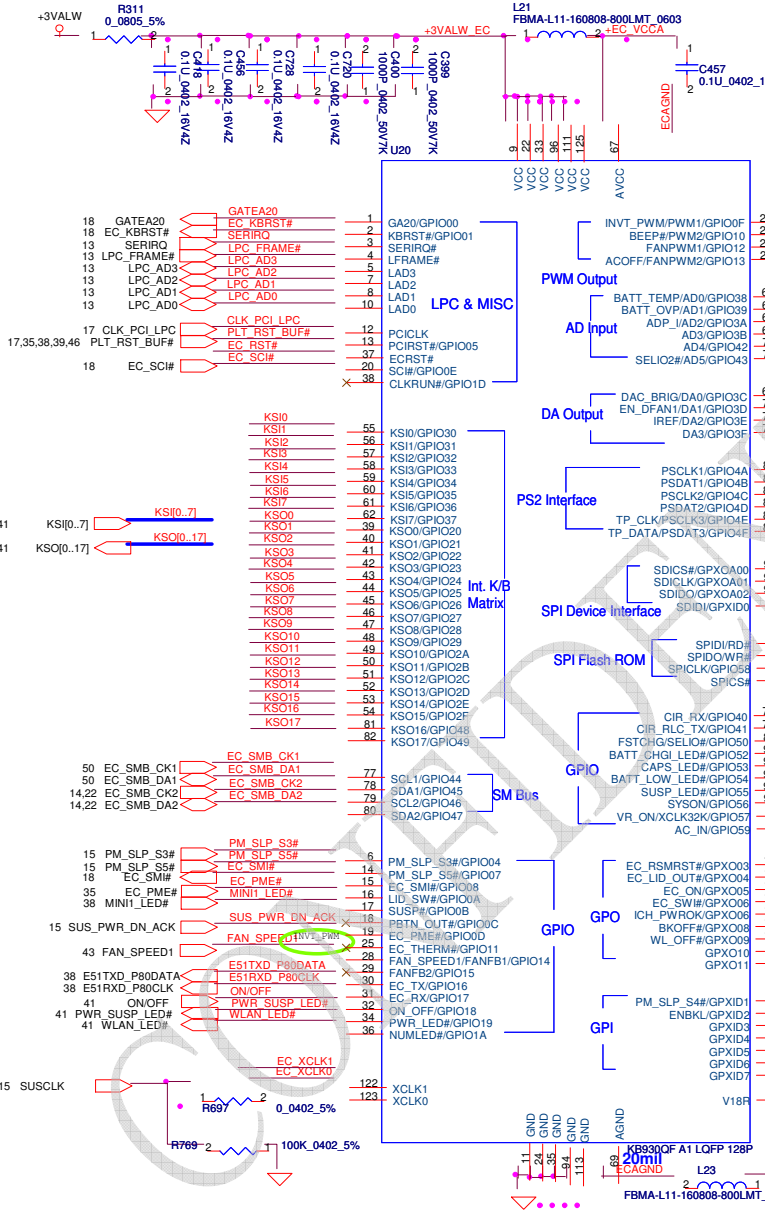
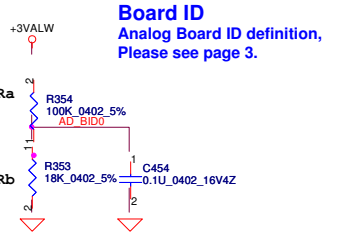
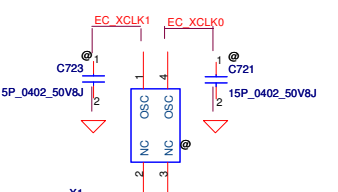
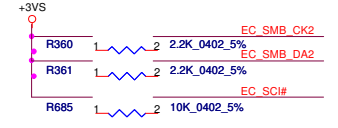
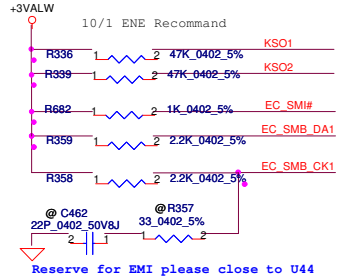
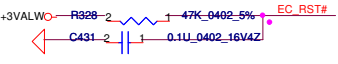
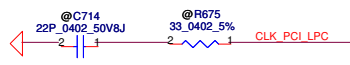
(Port 11)



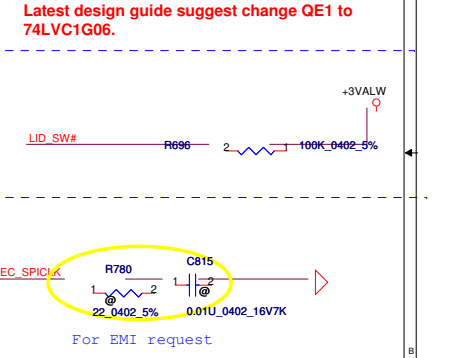
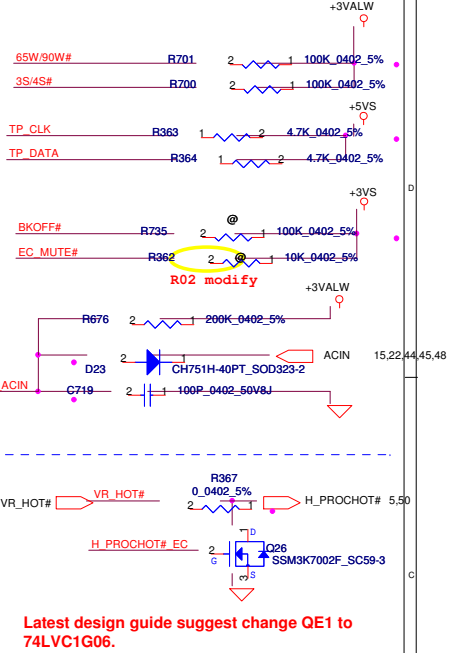
BT Wire Cable Note:
Pin 3, Pin 4 NC



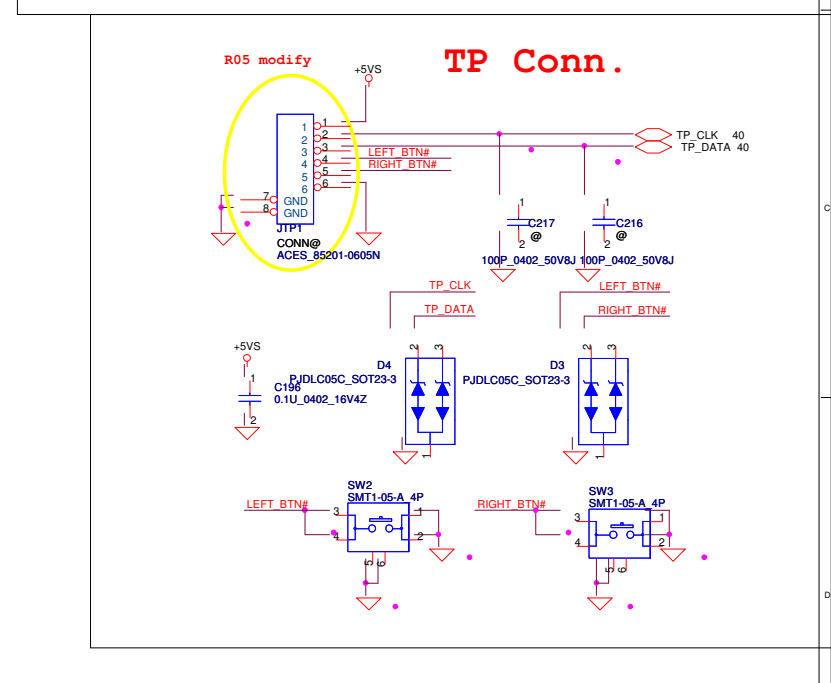
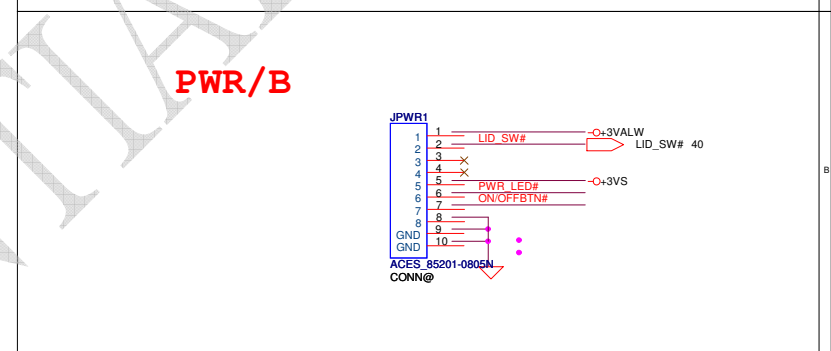
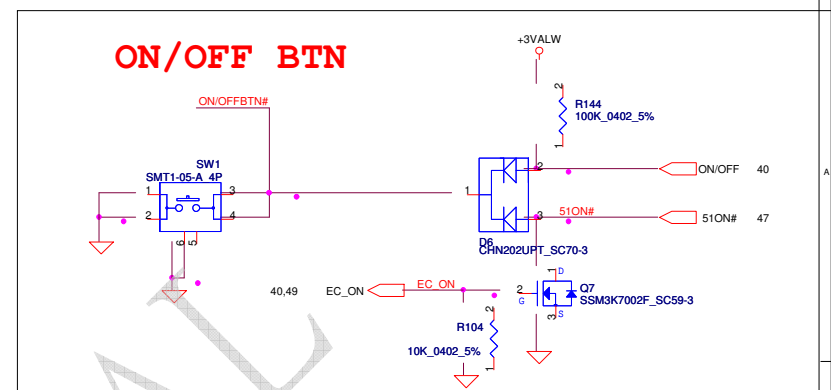
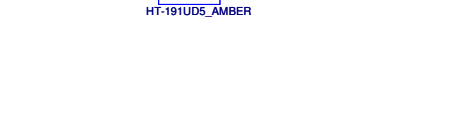
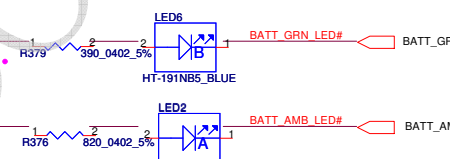
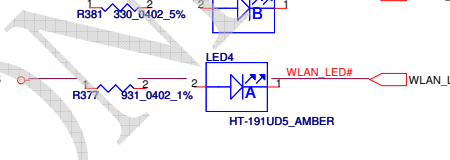
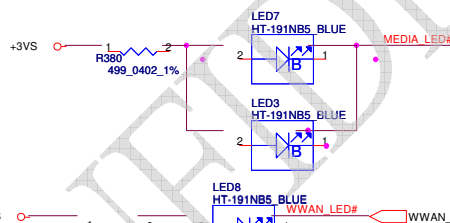
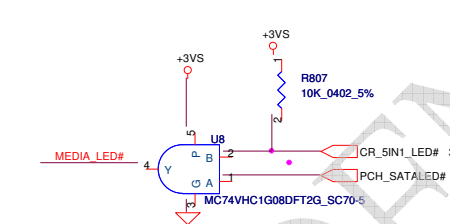
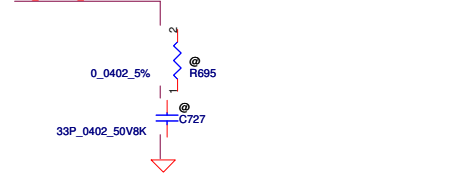
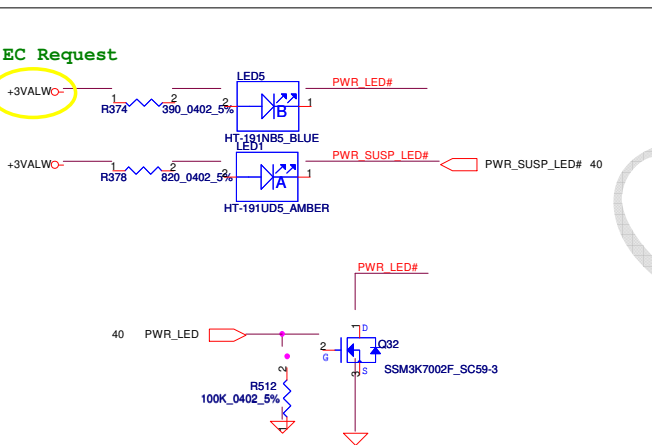
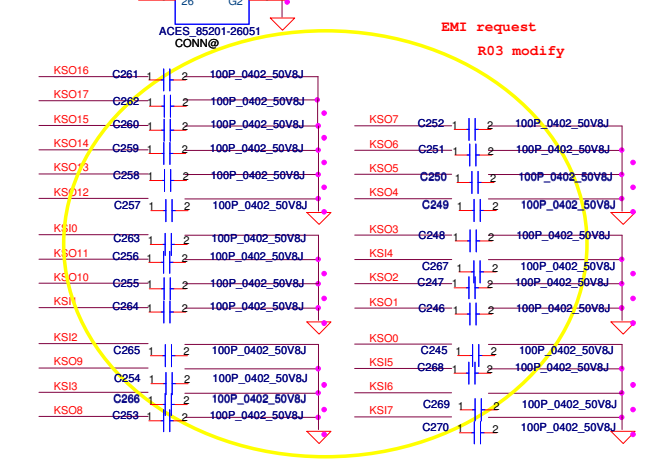
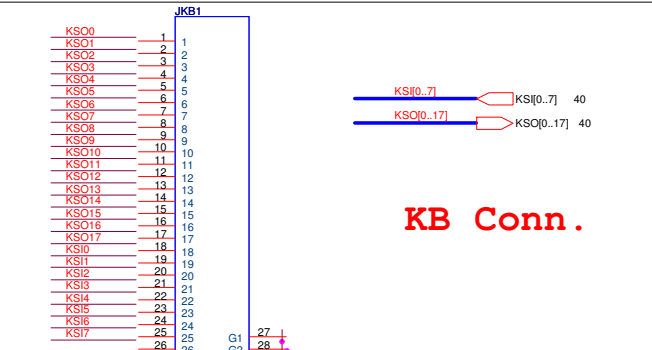
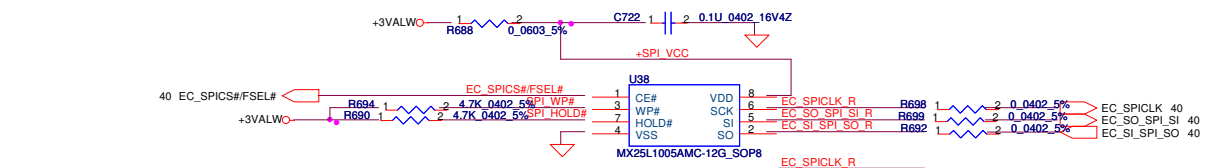
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				Custom JE50-HR/SJV50-HR M/B Schematics 0.4
				Date: Wednesday, October 27, 2010 Sheet 30 of 61



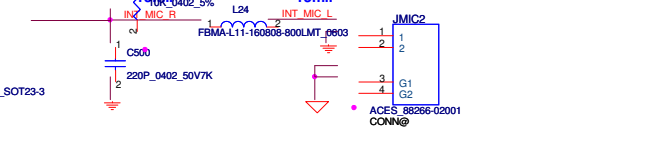
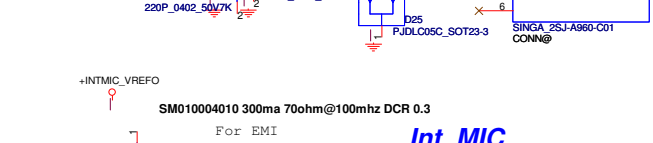
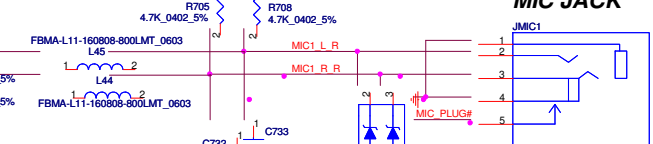
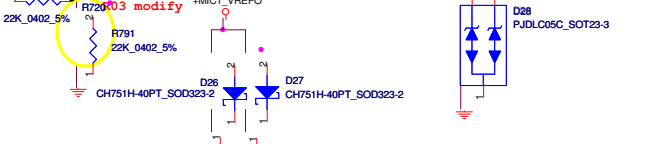
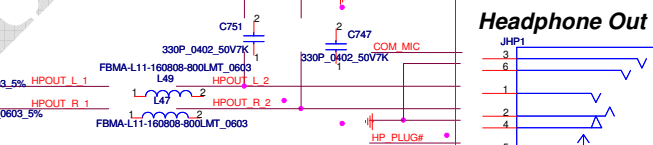
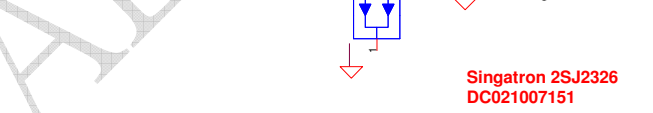
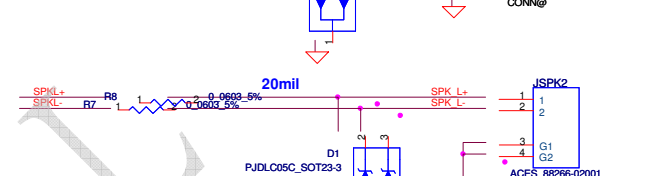
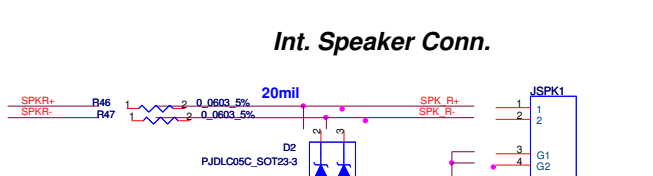
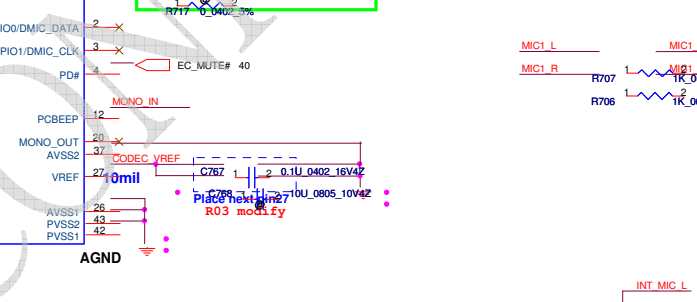
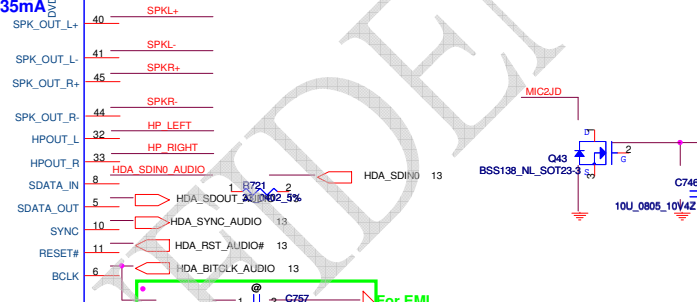
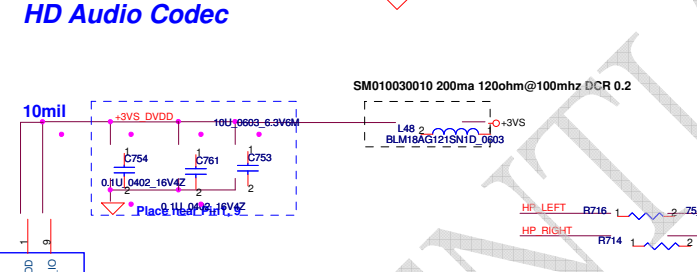
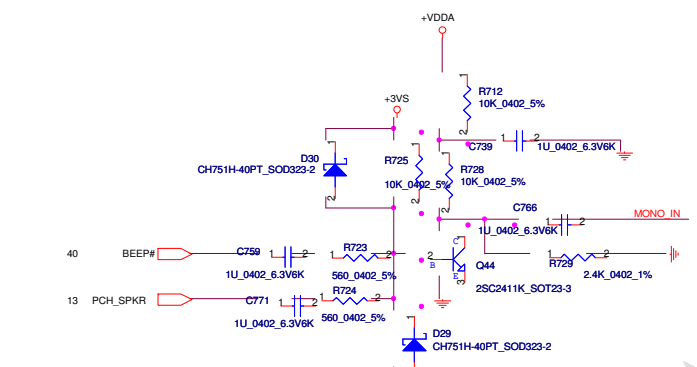
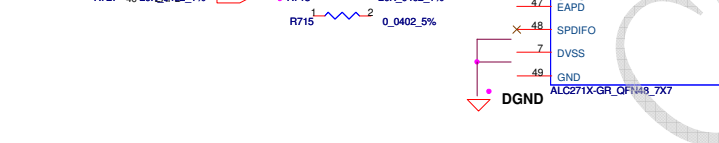
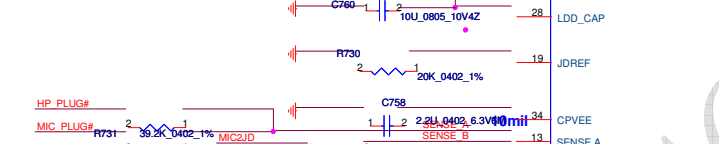
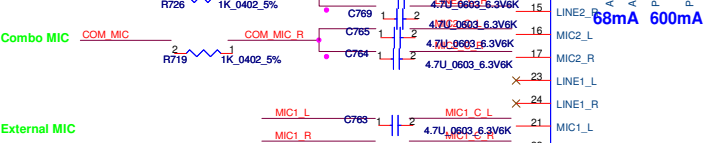
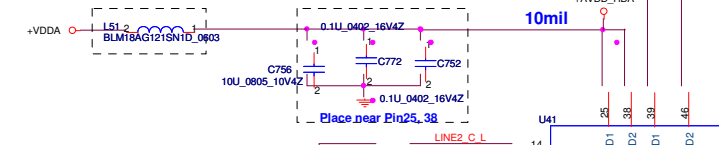
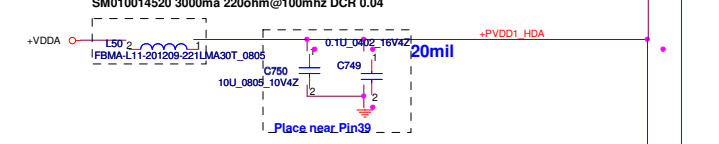
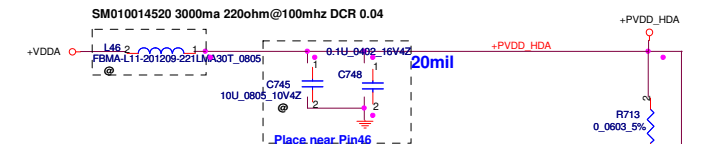
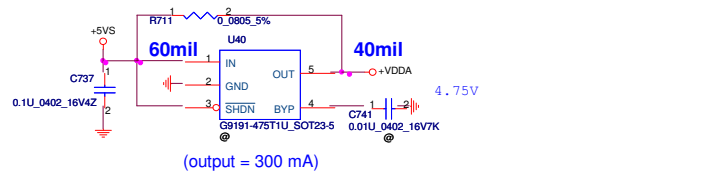
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18	EC_KBRST#		
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13	LPC_FRAME#		
13	LPC_AD3		
13	LPC_AD2		
13	LPC_AD1		
13	LPC_AD0		
17,35,38,39,46	CLK_PCL_LPC		
17,35,38,39,46	PLT_RST_BUF#		
18	EC_RST#		
18	EC_SC1#		
18	EC_SC2#		
18	EC_SC3#		
18	EC_SC4#		
18	EC_SC5#		
18	EC_SC6#		
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18	EC_SC9#		
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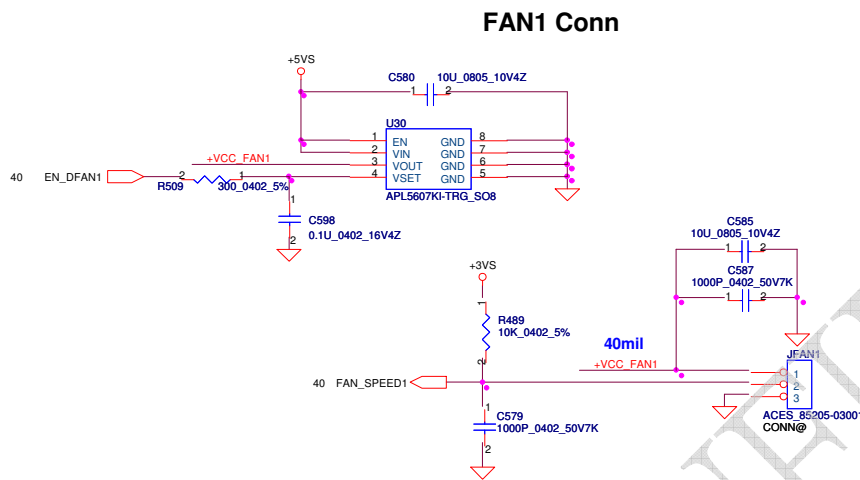
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Size	Document Number	Date		Rev	
Custom	JES0-HR/SJVS0-HR M/B Schematics	Wednesday, October 27, 2010		0,4	
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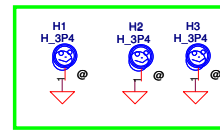
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Date: Wednesday, October 27, 2010			Sheet: 41 of 81



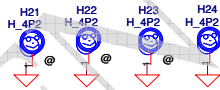
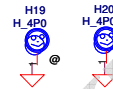
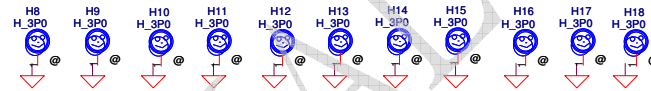
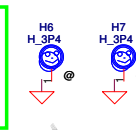
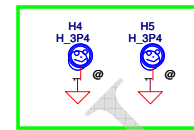
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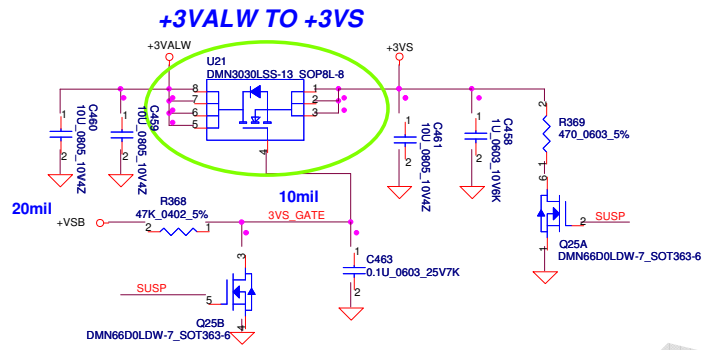
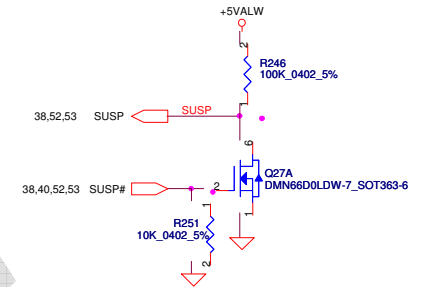
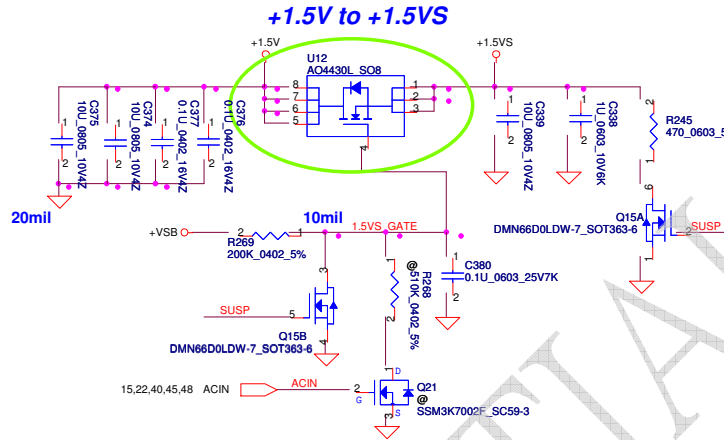
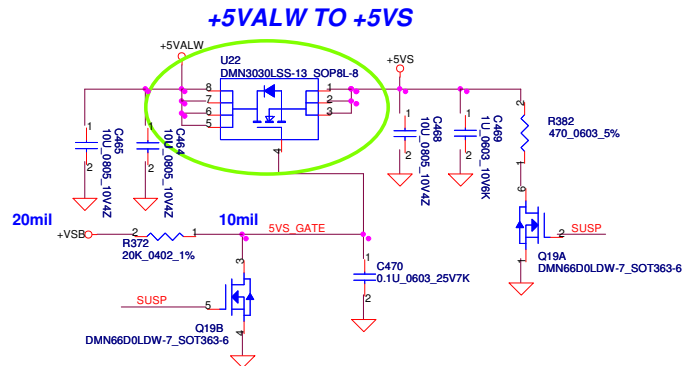
FAN Stand-Off



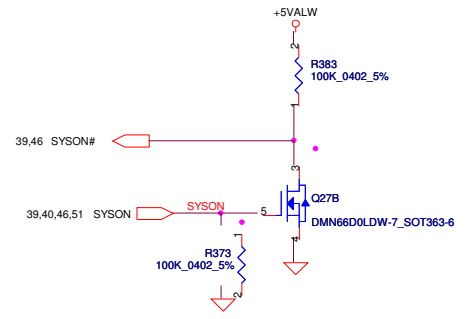
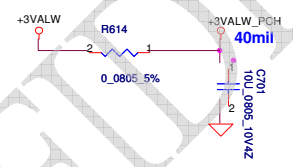
JUSB3 Stand-Off



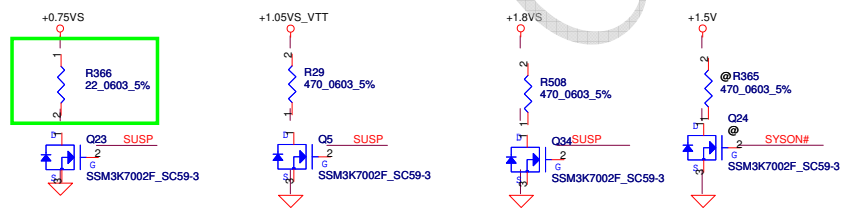
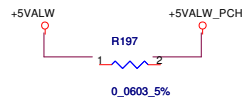
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/10/15	Deciphered Date	2011/10/15	Title FAN & Screw Hole	
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+3VALW TO +3VALW_PCH(PCH AUX Power)

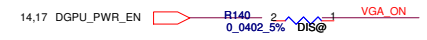
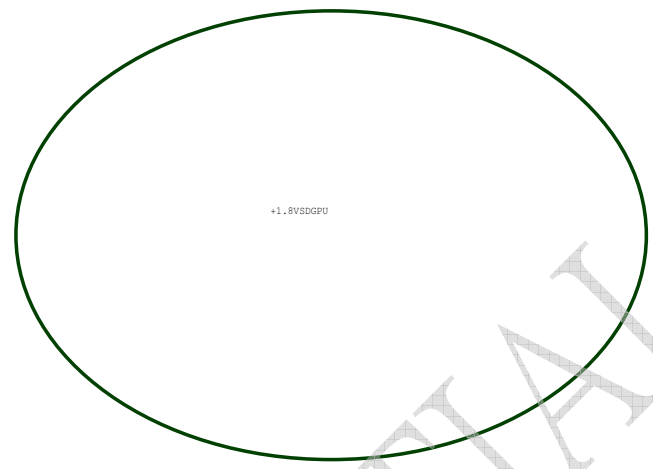
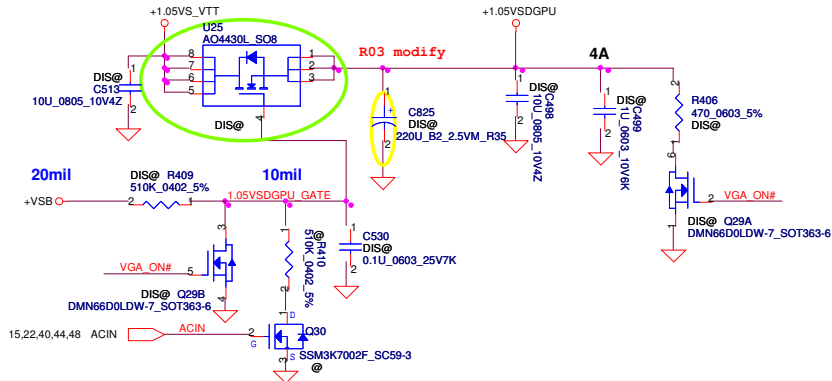


+5VALW TO +5VALW_PCH(PCH AUX Power)

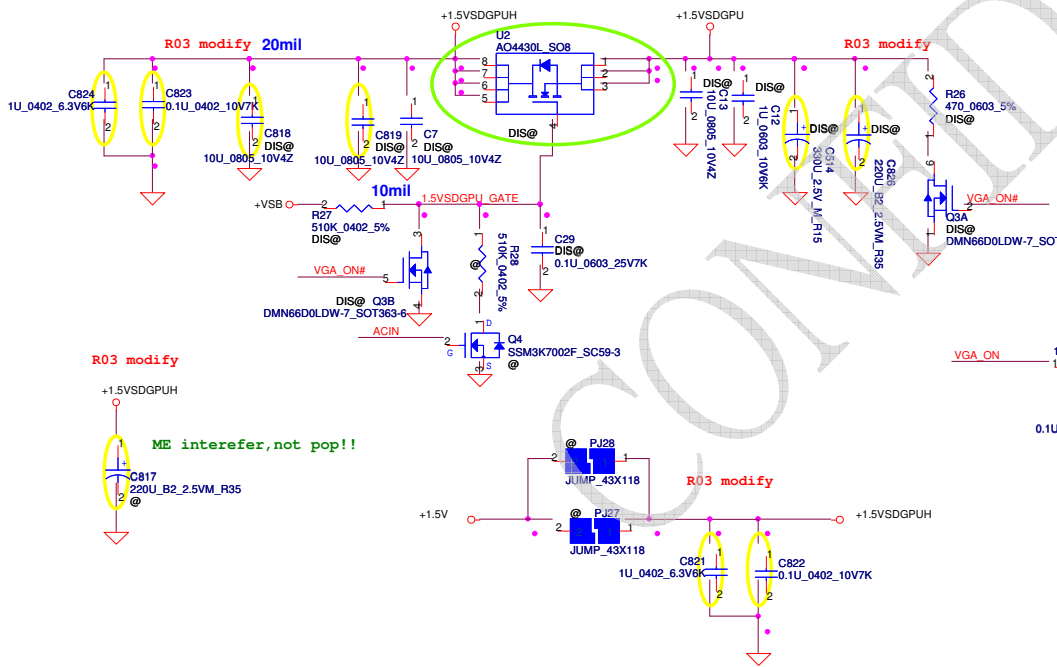


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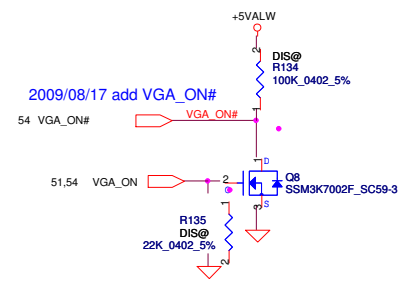
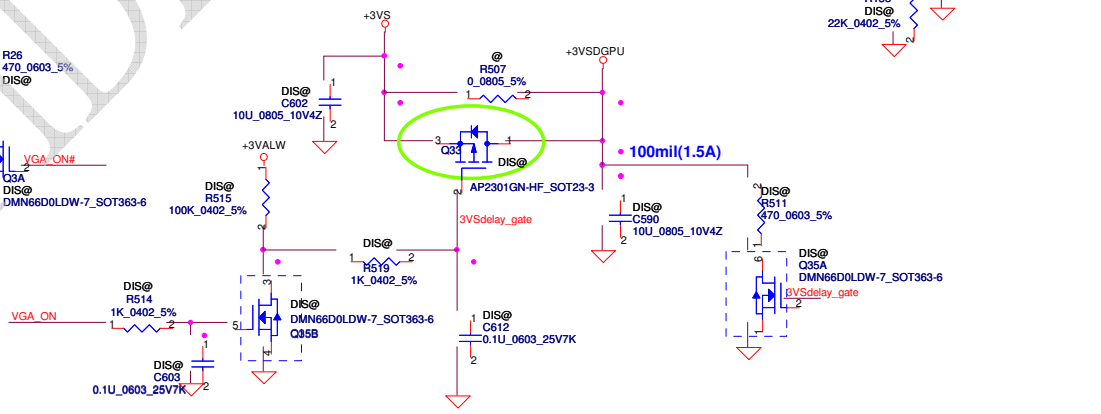
+1.05VS_VTT to +1.05VSDGPU for GPU



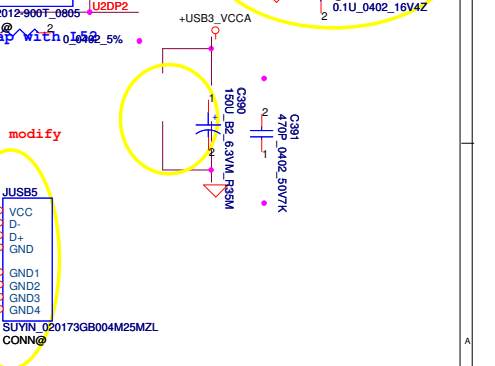
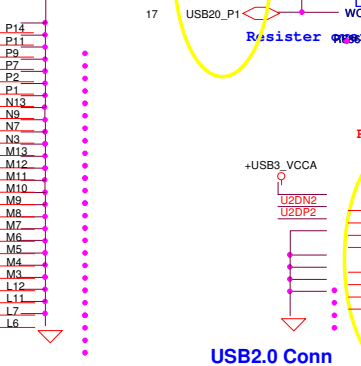
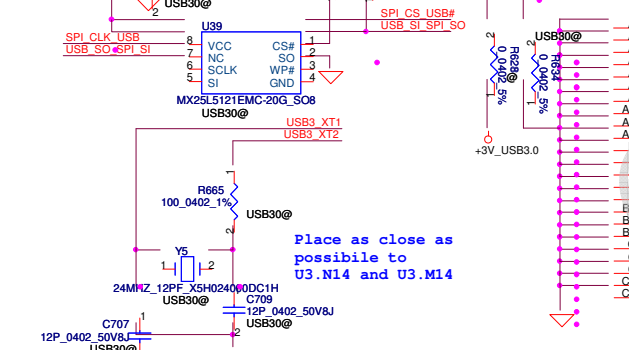
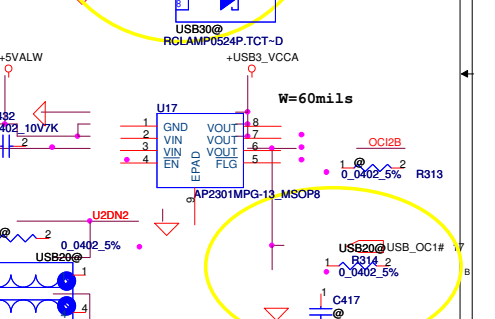
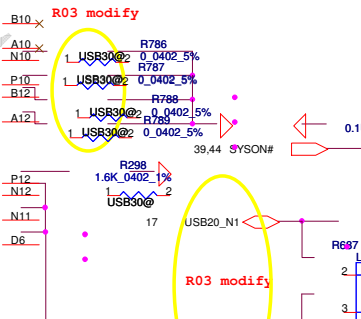
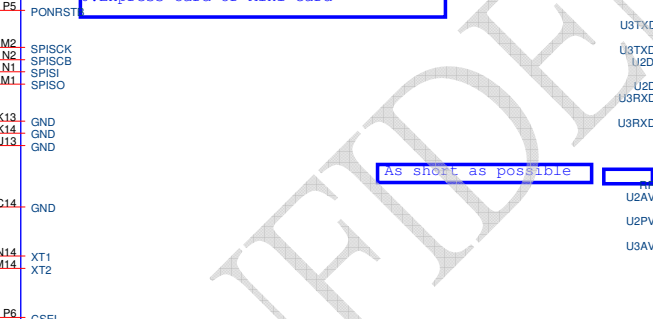
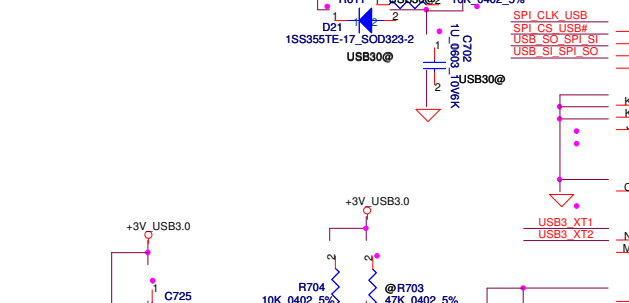
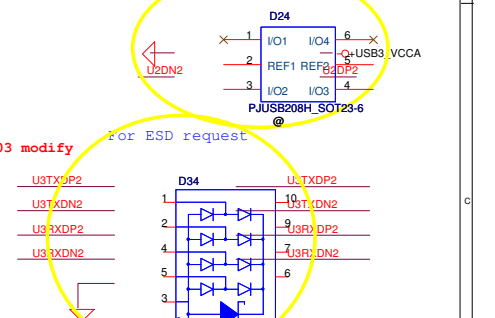
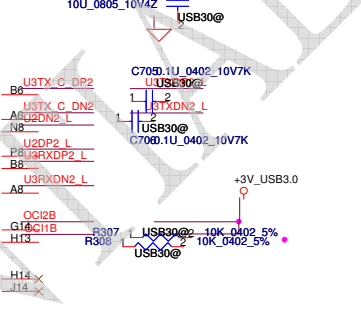
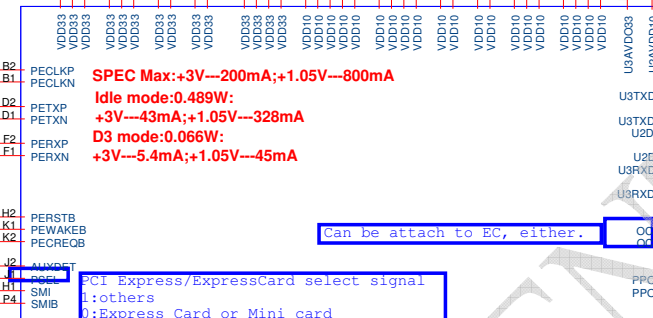
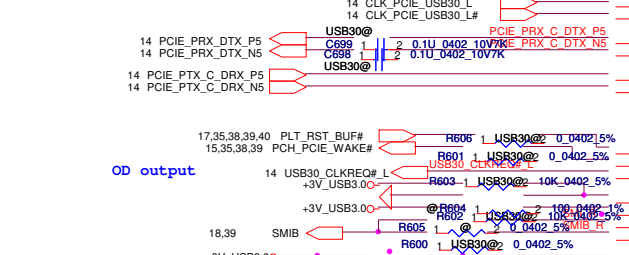
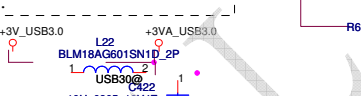
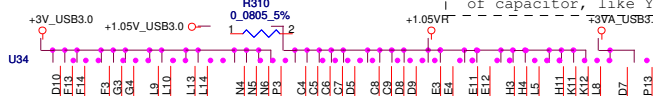
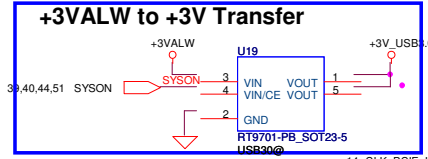
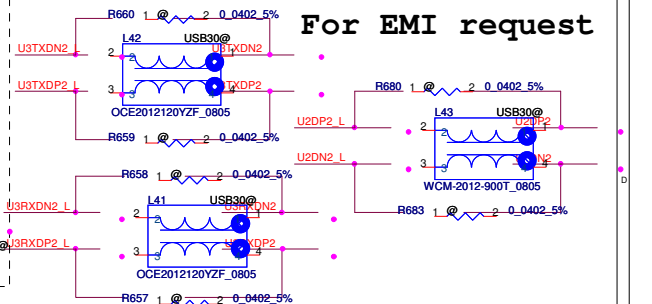
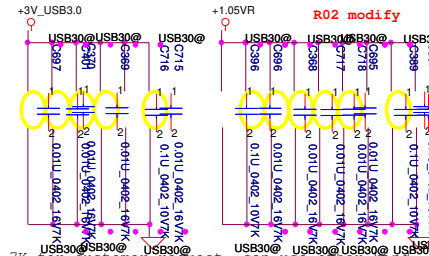
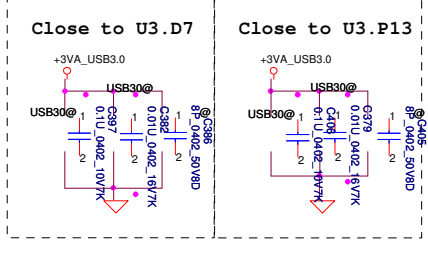
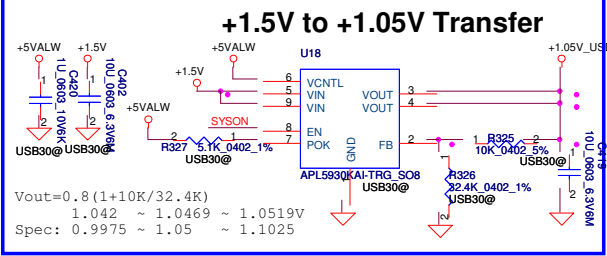
+1.5VSDGPUH to +1.5VSDGPU for GPU



+3VS to +3VSDGPU for GPU



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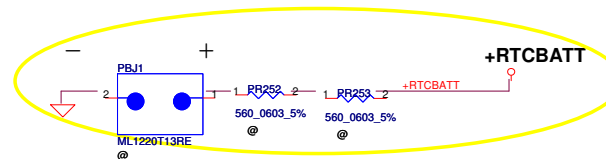
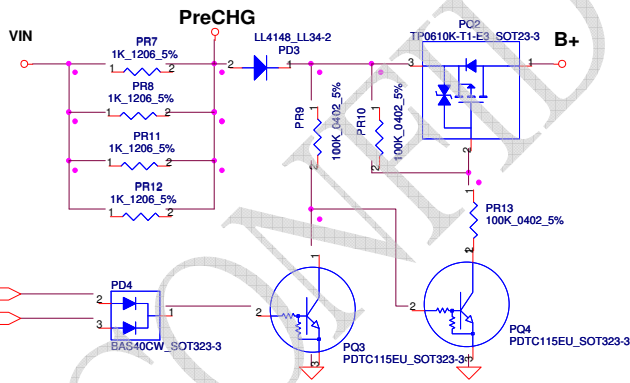
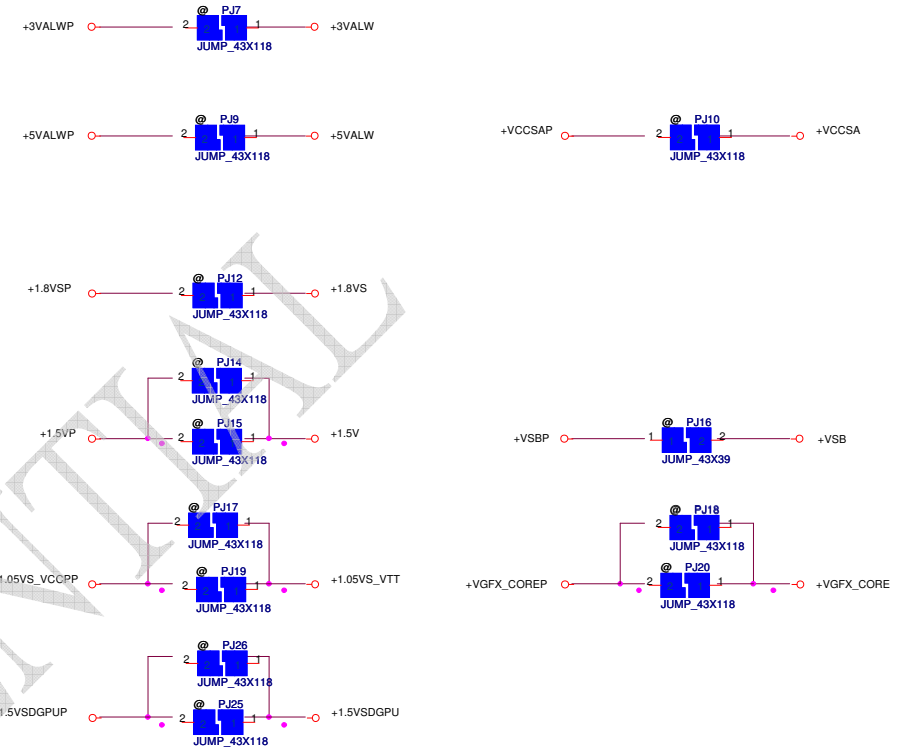
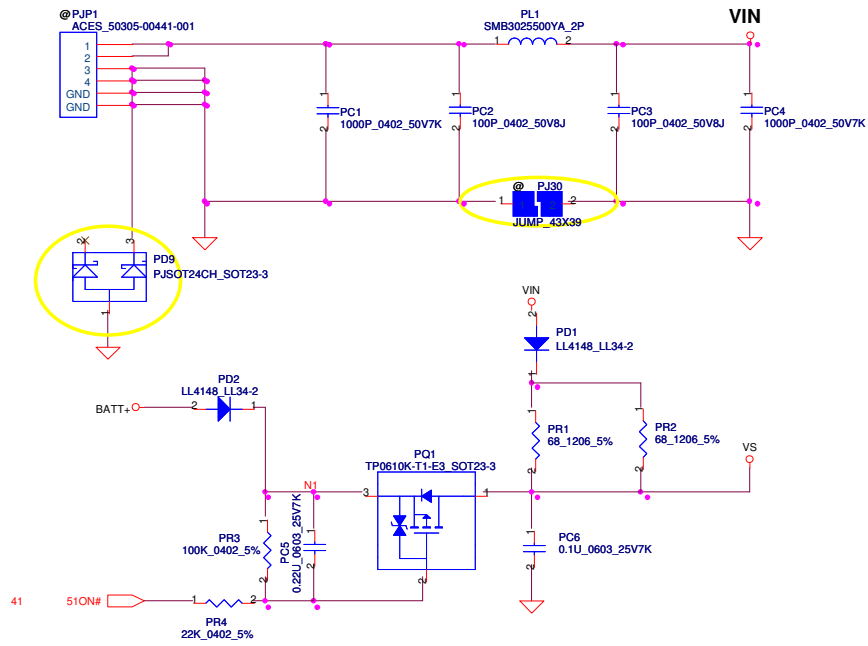
Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25



UPD72020AF1-DAP-A_FPGA176-USB30@

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		Custom	
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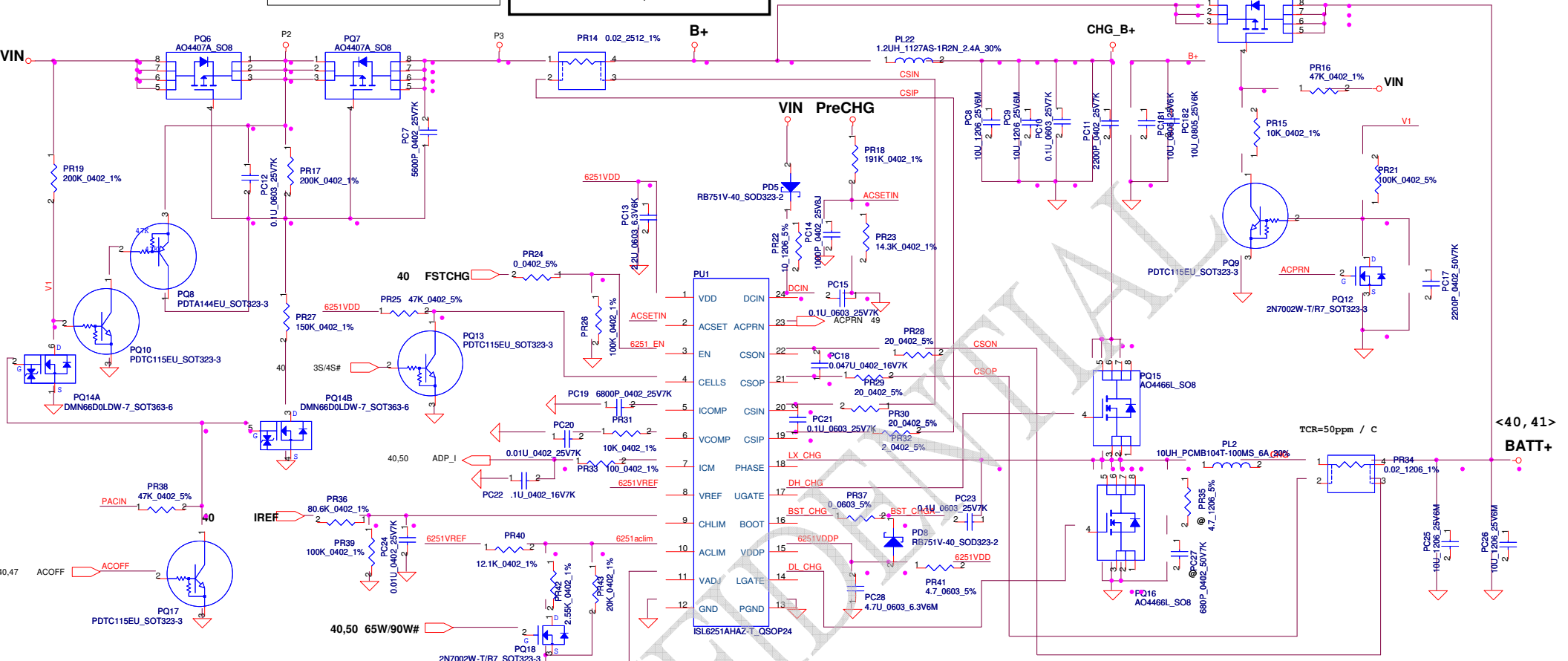
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Iada=0~4.74A (90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A

PC181 and PC182 reserve for EMI Isen solution



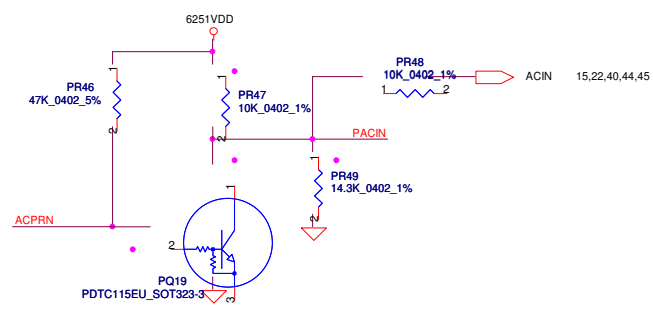
CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

Ki
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow Ki = 0.7224$

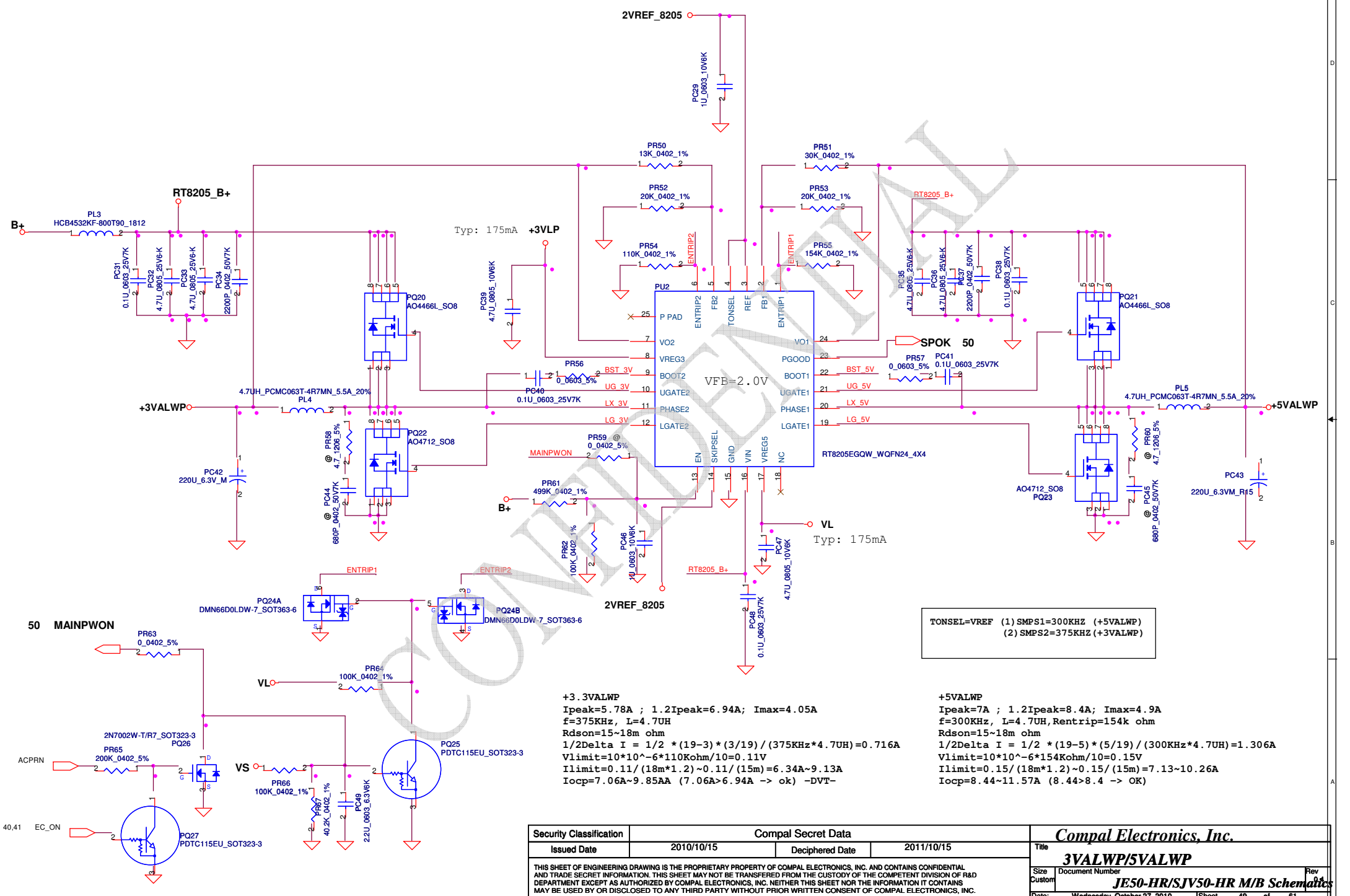
Kv
 $R_{internal} = ic = 514k$ Rec=3K R1=PR379=15.4K R2=PR381=31.6K
 $R = 514k / (31.6k / (15.4k + 3k)) = 11.372K$
 $r = 514k / 514k / (31.6k + 28.14k)$
 $V_{cell} = 0.175 * V_{adj} + 3.99v$
 $4.2V = 0.175 * V_{adj} + 3.99v \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514k)) + CALIBRATE * (r / (r + 514k))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$
 $A = V_{ref} * (R / (R + 514k)) = 0.052$
 $Kv = 9.451$



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Compal Electronics, Inc.			
Title: PWR-CHARGER			
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Typ: 175mA +3VLP

Typ: 175mA

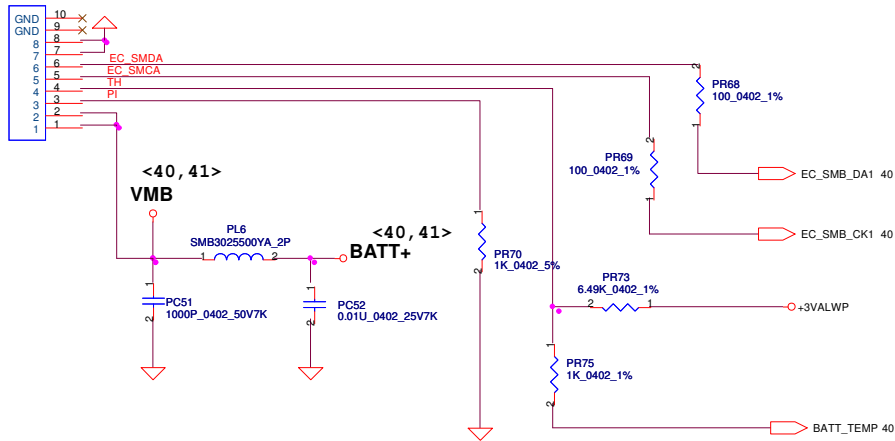
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

+3.3VALWP
 $I_{peak}=5.78A$; $1.2I_{peak}=6.94A$; $I_{max}=4.05A$
 $f=375KHz$, $L=4.7UH$
 $R_{dson}=15\sim 18m\ ohm$
 $1/2\Delta I = 1/2 * (19-3) * (3/19) / (375KHz * 4.7UH) = 0.716A$
 $V_{limit}=10 * 10^{-6} * 110Kohm / 10 = 0.11V$
 $I_{limit}=0.11 / (18m * 1.2) \sim 0.11 / (15m) = 6.34A \sim 9.13A$
 $I_{ocp}=7.06A \sim 9.85AA$ ($7.06A > 6.94A \rightarrow ok$) -DVT-

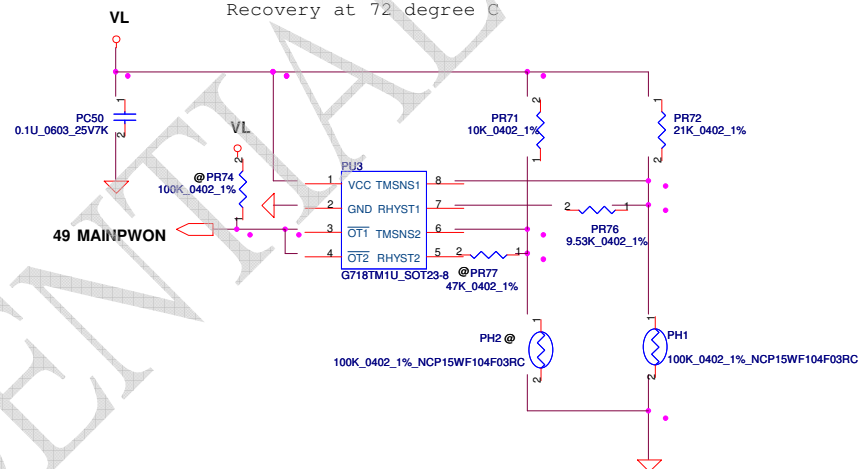
+5VALWP
 $I_{peak}=7A$; $1.2I_{peak}=8.4A$; $I_{max}=4.9A$
 $f=300KHz$, $L=4.7UH$, $R_{entrip}=154k\ ohm$
 $R_{dson}=15\sim 18m\ ohm$
 $1/2\Delta I = 1/2 * (19-5) * (5/19) / (300KHz * 4.7UH) = 1.306A$
 $V_{limit}=10 * 10^{-6} * 154Kohm / 10 = 0.15V$
 $I_{limit}=0.15 / (18m * 1.2) \sim 0.15 / (15m) = 7.13 \sim 10.26A$
 $I_{ocp}=8.44 \sim 11.57A$ ($8.44 > 8.4 \rightarrow OK$)

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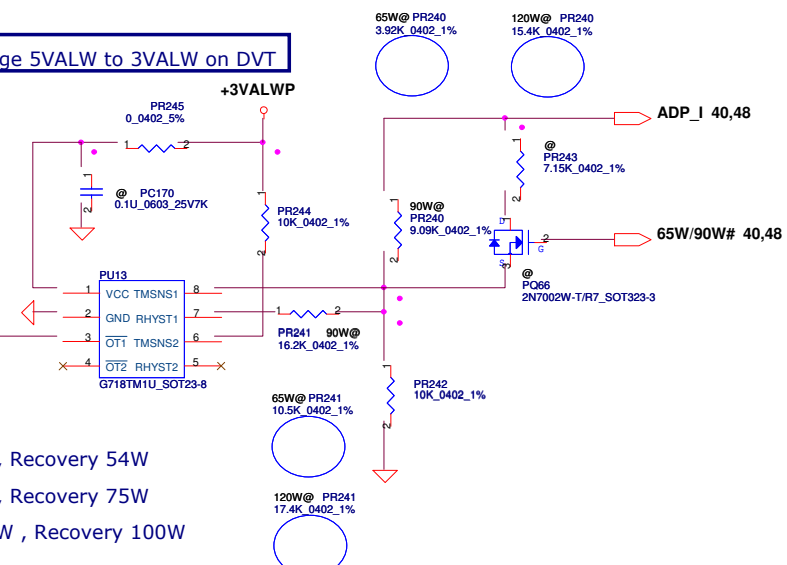
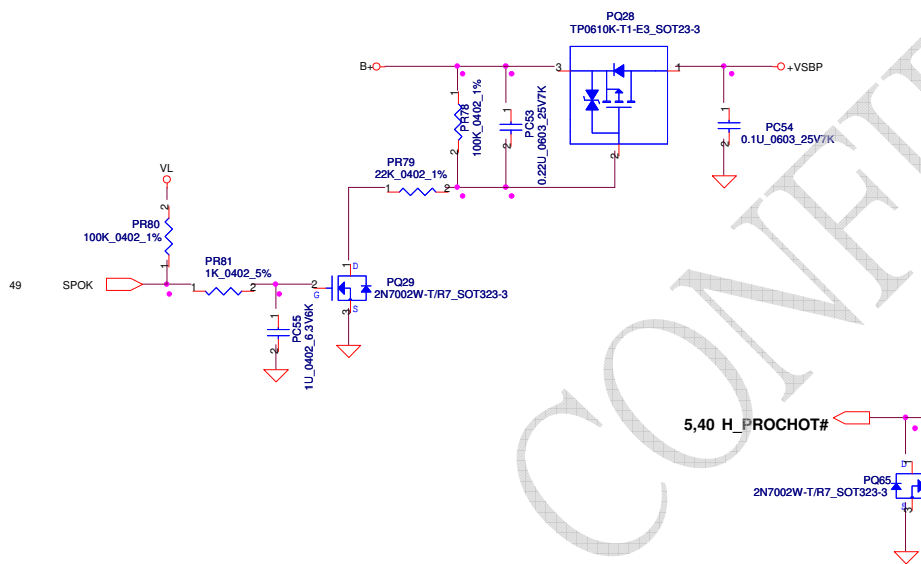
PJP2
SUYIN_200275GR008G13GZR



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



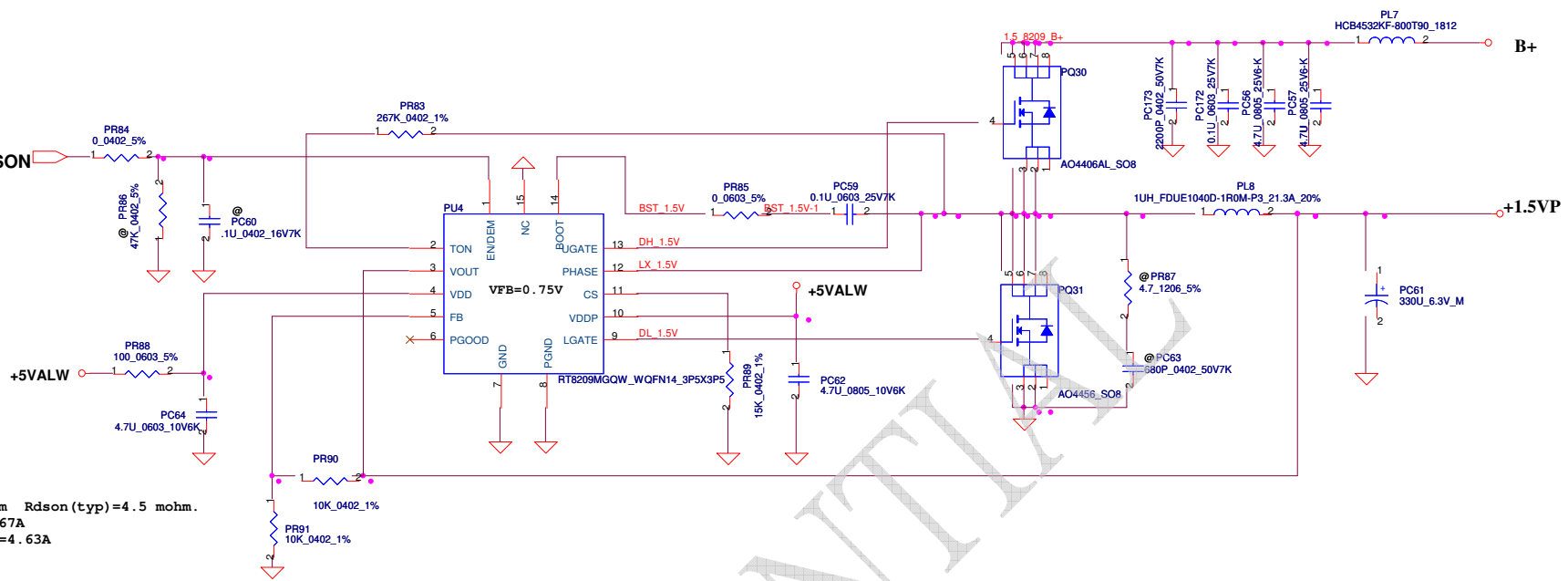
Change 5VALW to 3VALW on DVT



For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W
For 120W adapter==>action 135W , Recovery 100W

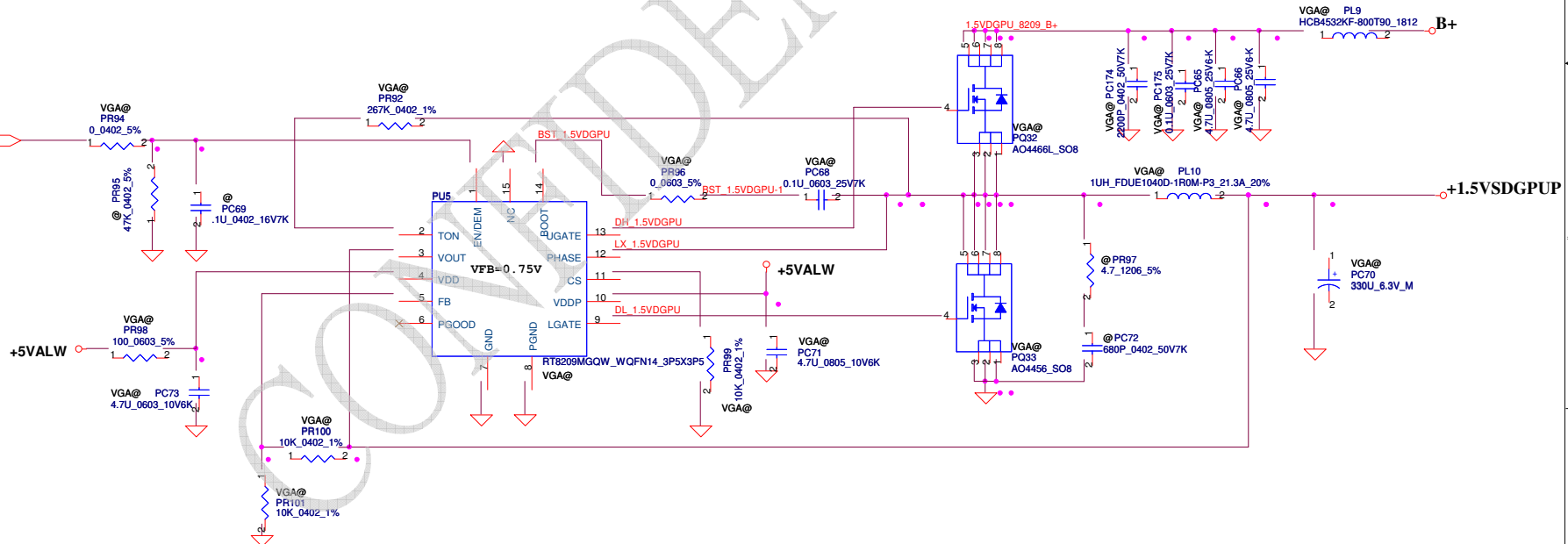
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39,40,44,46 SYSON



<Vo=1.5V> VFB=0.75V
 $V=0.75 * (1+10K/10K)=1.5V$
 $Fsw=298KHz$
 $Cout ESR=15m\ ohm\ R_{dson(max)}=5.6\ mohm\ R_{dson(typ)}=4.5\ mohm.$
 $I_{peak}=19.53A, I_{max}=23.44A, I_{ocp}=13.67A$
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Fsw) = 4.63A$
 $\Rightarrow 1/2 \Delta I = 2.315A$
 choose $R_{cs}=15K$
 $I_{ocpmax} = ((15K * 11\mu A) / 0.0045) + 2.315A = 35.65A$
 $I_{ocpmin} = ((15K * 9\mu A) / (0.0056 * 1.3)) + 2.315A = 23.06A$
 $I_{ocp}=23.06A \sim 35.65A$

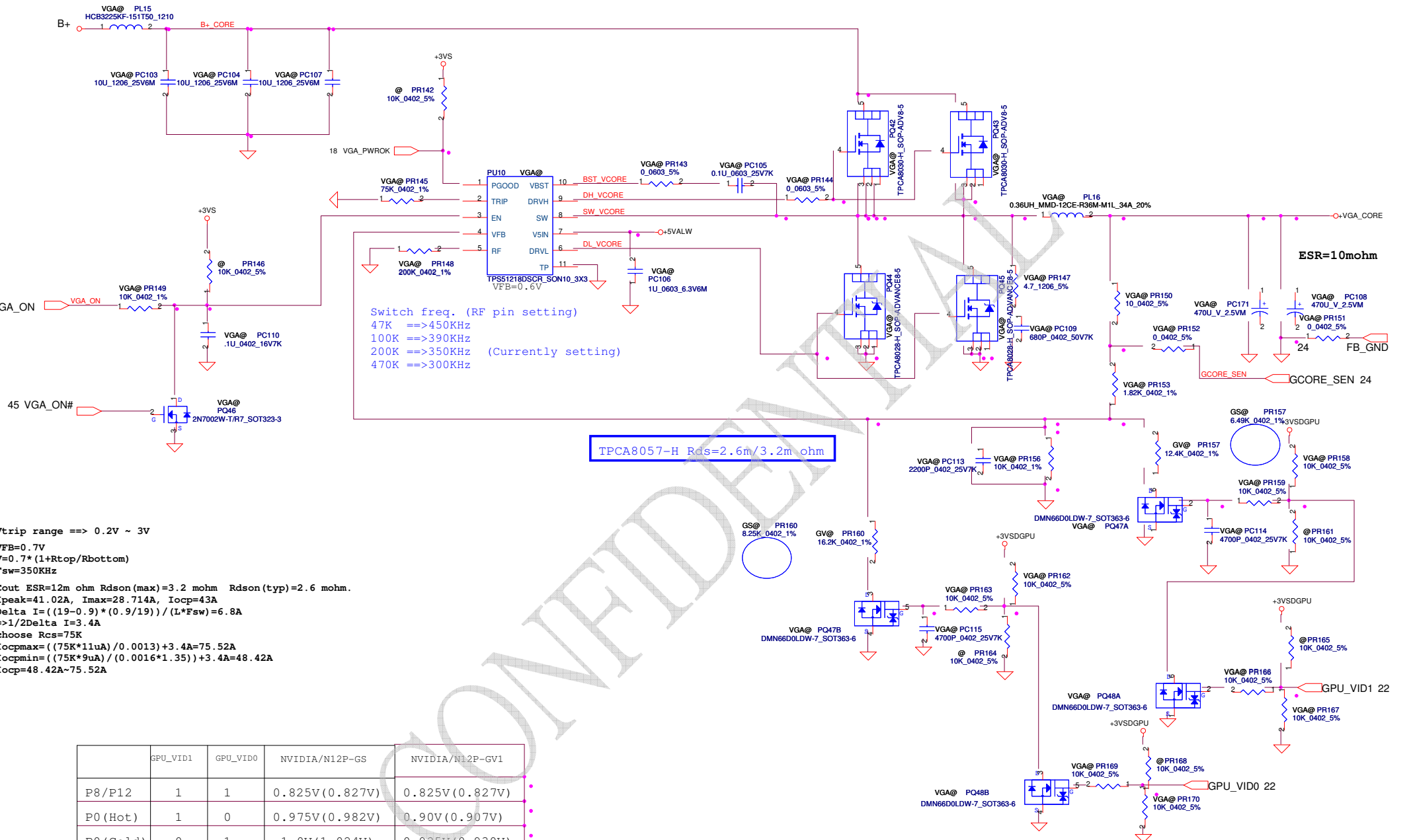
45,54 VGA_ON



<Vo=1.5V> VFB=0.75V
 $V=0.75 * (1+10K/10K)=1.5V$
 $Fsw=298KHz$
 $Cout ESR=15m\ ohm\ R_{dson(max)}=5.6\ mohm\ R_{dson(typ)}=4.5\ mohm.$
 $I_{peak}=10.4A, I_{max}=12.48A, I_{ocp}=7.28A$
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Fsw) = 4.63A$
 $\Rightarrow 1/2 \Delta I = 2.315A$
 choose $R_{cs}=10K$
 $I_{ocpmax} = ((10K * 11\mu A) / 0.0045) + 2.315A = 24.59A$
 $I_{ocpmin} = ((10K * 9\mu A) / (0.0056 * 1.3)) + 2.315A = 15.95A$
 $I_{ocp}=15.95A \sim 24.59A$

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Compal Electronics, Inc.			
Title	PWR-+1.5VP/+1.5VSDGPU		
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Switch freq. (RF pin setting)
 47K ==>450KHz
 100K ==>390KHz
 200K ==>350KHz (Currently setting)
 470K ==>300KHz

TPCA8057-H Rds=2.6m/3.2m ohm

Vtrip range ==> 0.2V ~ 3V
 VFB=0.7V
 $V=0.7 * (1+Rtop/Rbottom)$
 $Fsw=350KHz$
 $Cout ESR=12m\ ohm\ R_{dson(max)}=3.2\ mohm\ R_{dson(typ)}=2.6\ mohm.$
 $I_{peak}=41.02A, I_{max}=28.714A, I_{ocp}=43A$
 $\Delta I = ((19-0.9) * (0.9/19)) / (L * Fsw) = 6.8A$
 $\Rightarrow 1/2 \Delta I = 3.4A$
 choose Rcs=75K
 $I_{ocpmax} = (75K * 11uA) / (0.0013) + 3.4A = 75.52A$
 $I_{ocpmin} = (75K * 9uA) / (0.0016 * 1.35) + 3.4A = 48.42A$
 $I_{ocp} = 48.42A \sim 75.52A$

	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P8/P12	1	1	0.825V(0.827V)	0.825V(0.827V)
P0(Hot)	1	0	0.975V(0.982V)	0.90V(0.907V)
P0(Cold)	0	1	1.0V(1.024V)	0.925V(0.930V)
	0	0	----	----

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Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
1	Shut down for PWM3 pin floating	IF the PWM3 no used, please pull high it for +5VS and not floating	0.1	P.55	(1)Add PR638(0_0603_5%) between PWM3 and +5VS (2)connect the ISNG to +5VS	2010-03-29	DVT
2	OVP problem with PWR and HW side	If the HW side is 0V, through the jumper will cause the sense pin to over the votage setting and it may happen OVP problem.	0.1	P.55	Change the +VGFX_CORE to +VGFX_COREP	2010-03-29	DVT
3							

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Title		<Title> PIR POWER1
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A	PAW00 (LA-6361P)	0.1
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.18	PCH_GPIO71	09/01	SW	For identify VRAM 900 or 800 MHz		0.2
2	P.31	DPST buffer	09/03	HW	Change U1 from NOT gate to Buffer		0.2
3	P.39	EC_MUTE# pull high	09/03	HW	Change EC_MUTE# Pull high from +3VALW to +3VS		0.2
4	P.40	TP Conn. Reverse	09/03	HW	TP Mudule change,so reverse TP pin		0.2
5	P.13	R624 pop @	09/03	HW	Already pull high R655~		0.2
6	P.45	Change Cap from 0.1u to 0.01u	09/03	HW	C696,C368,C717,C718,C695,C366,C697,C401,C370,C369,C715 change to 0.01U Follow Vendor Suggest ..		0.2
7	P.35	Change 0 Ohm to 47 Ohm	09/04	Broadcom	R199,R207,R211,R215,R168,R171,R179,R182,R195,R216,R192 change to 47 Ohm Follow Vendor Suggest ..		0.2
8	P.5		09/17	HW	CPU XDP socket take off		0.2
9	P.40		09/17	HW	TP pin reverse		0.2
10	P.13		09/17	HW	R624 change to 4.7K		0.2
11	P.45		09/17	HW	OCI2B(R313) place @ for BOM		0.2
12	P.33		09/17	HW	HDMI output from PCH (by UMA)		0.2
13	P.35		09/17	HW	switch the LAN MIDI0 and MIDI2 pin		0.2
14	P.17,35,37,38,39,45		09/17	HW	Change IO port PLT_RST# to PLT_RST_BUE#		0.2
15	P.18		09/17	HW	OPTIMUS_EN# pull high, pull low resistor value both change to 10K		0.2
16	P.24		09/20	HW	modify the VRAM strap pin ROM_SI pull low resistor for implement VRAM 900MHz		0.3
17	P.33		09/23	HW	Add R784 and R785 for DDC pull high...		0.3
18	P.44		09/23	HW	Add C818 and C819 for coupling noise from other spare trace...		0.3
19	P.45		09/23	HW	Add R786,R787,R788 and R789 pull down from vendor's suggestion..		0.3
20	P.37		09/23	HW	Add C820,R790 and Q58 for 3G/B and change source voltage from +3VS to +3VALW..		0.3
21	P.45		09/23	HW	Add C821,C822,C823,C824 for +1.5V... and move the PJ26 & PJ27 between 1.5V to 1.5VSDGPHH		0.3
22	P.46		09/24	HW	Change JUSB5 to USB2.0 Conn. Add D34 as ESD Diode for USB3.0		0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	P.41		09/24	HW	Add R791 pull down 22k Ohm to ground Vendor's request...		0.3
24	P.22		09/24	HW	Add D31 to connect to ACIN Vendor's request...		0.3
25	P.36		09/29	HW	Add JP1,JP2 and JP3 for 家電下鄉 ESD protection		0.3
26	P.36		09/29	ME	Update the JREAD1 symbol		0.3
27	P.13		09/29	HW	Add R792 follow DGI.5		0.3
28	P.33		09/29	HW	Change HDMI termination R to 680 Ohm		0.3
29	P.44		09/29	HW	Add C825 fro +1.05VSDGPU		0.3
30	P.17,38,45		09/30	HW	Change the M/B to USB port to port 1 Sub/B to port 0 and port 2		0.3
31	P.5		10/04	HW	Add test point for TCK,TMS, TRST#,TDO,TDI		0.3
32	P.17,18		10/04	HW	WWAN_OFF# from GPIO51 to GPIO37 WL_OFF# from GPIO55 to GPIO49		0.3
33	P.17,45		10/04	HW	M/B USB port from port 2 change to port1		0.3
34	P.26		10/04	HW	C1 and C604 chaneg to 470uF		0.3
35	P.36		10/04	HW	Add C827 as DGND and RJ45_GND bridge		0.3
36	P.36		10/04	HW	Change R490,R491,R492 and R493 to 0603 package		0.3
37	P.35		10/04	HW	Chaneg R214 to 0603 package		0.3
38	P.35		10/04	HW	Chaneg R192,R195,R199,R207,R211, R215,R168,R171,R179,R182 to 0 Ohm		0.3
39	P.40		10/04	HW	follow broadcom suggestion,add R496		0.3
40	P.40		10/04	HW	Add keyboard cap for EMI		0.3
41	P.44		10/04	HW	Add C826 for +1.5VSDGPU		0.3
42	P.37		10/05	HW	Add RTS5138 circuit		0.4
43	P.13		10/12	HW	Add D35 ,R799 and C838 for changing the RTC to samll size... and can be charged!!		0.4
44	P.14		10/12	HW	Add CLK_SD_48M for Card Reader 5138		0.4
45	P.24		10/12	HW	Pop R129 follow NV suggestion		0.4
46	P.25		10/12	HW	Pop R82 and De-pop R92 follow NV suggestion		0.4
47	P.25		10/12	HW	Add R800 and R801 10K Ohm pull down follow NV suggestion		0.4
48	P.24		10/12	HW	Change R775,R777,R778 and R779 to GV@		0.4

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