

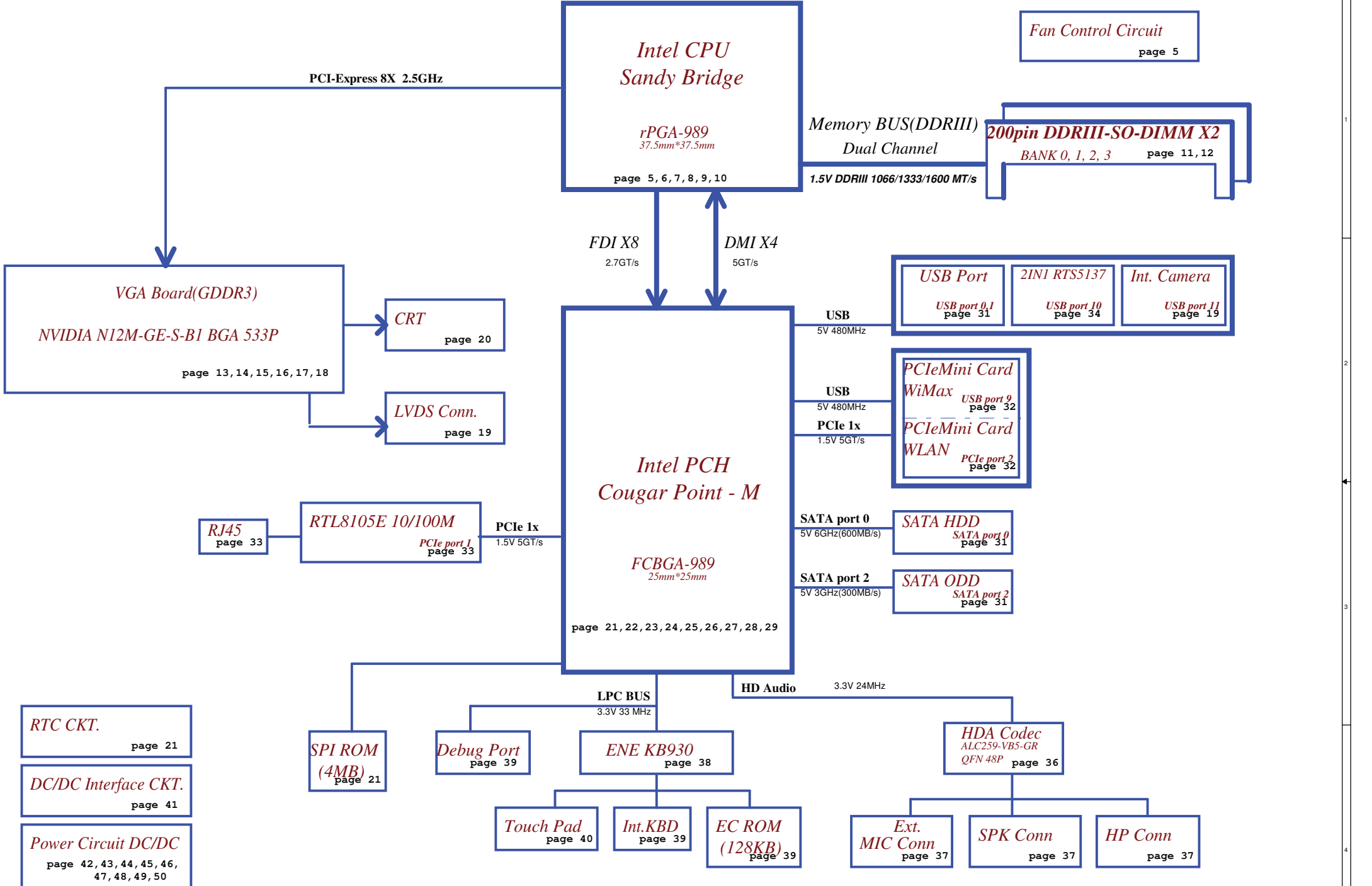
PWWHA

Delhi 10RG

LA-7201P REV 1.0 Schematic

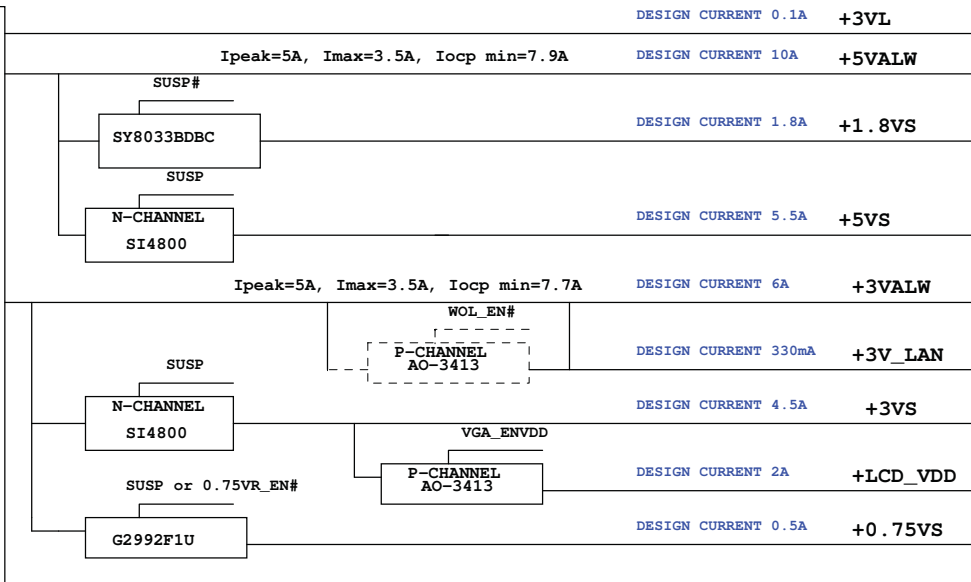
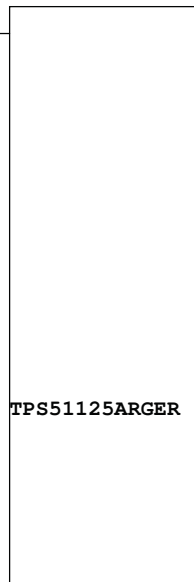
Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2011-01-31 Rev 1.0

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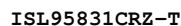


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B+

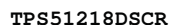


VR_ON



Ipeak=53A, I_{max}=36A, I_{ocp min}=70A DESIGN CURRENT 53A +CPU_CORE

SUSP#



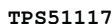
Ipeak=20A, I_{max}=14A, I_{ocp min}=26A DESIGN CURRENT 21A +VGA_CORE

SUSP#



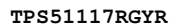
Ipeak=12.5A, I_{max}=8.75A, I_{ocp min}=21.4A DESIGN CURRENT 17A +1.05VS_VCCP

VCCPPWRGD



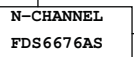
Ipeak=6A, I_{max}=4.2A, I_{ocp min}=7.76A DESIGN CURRENT 6A +VCCSA

SYSON



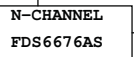
Ipeak=16.5A, I_{max}=11.55A, I_{ocp min}=21.03A DESIGN CURRENT 20A +1.5V

SUSP



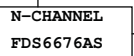
DESIGN CURRENT 2A +1.5V_CPU

SUSP



DESIGN CURRENT 0.7A +1.5VS

VGA_PWROK#



DESIGN CURRENT 3A +1.5V_MEM_GFX

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b

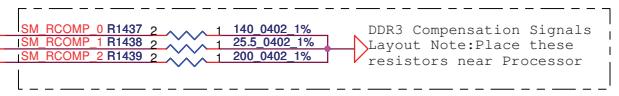
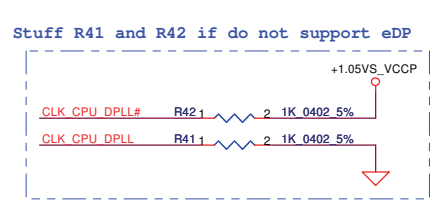
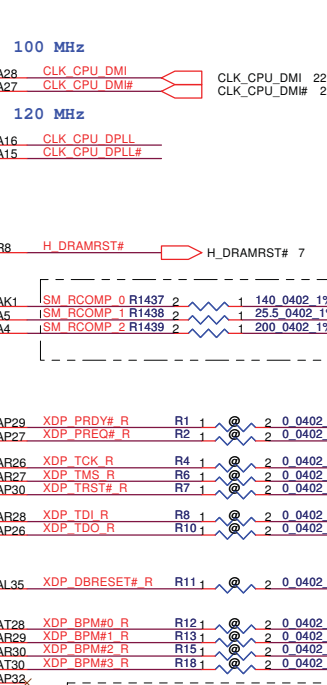
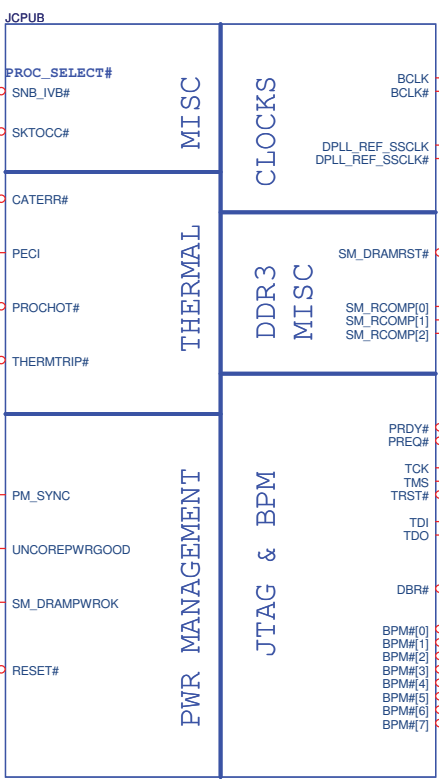
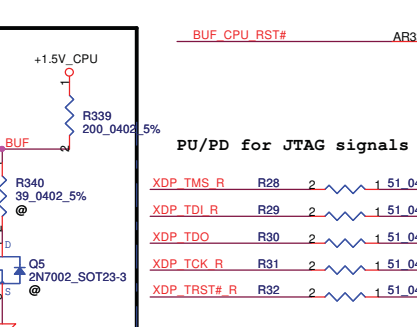
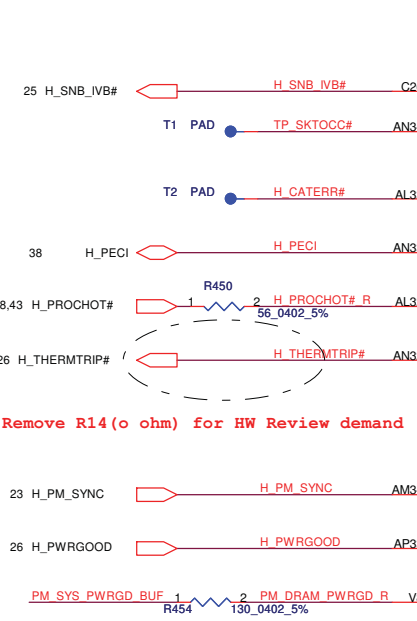
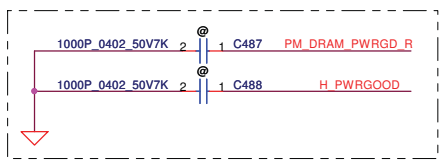
BTO Option Table

Function	DIS only	MINI PCI-E SLOT	LAN			Camera & Mic
description		SLOT1	LAN			Camera & Mic
explain		WIMAX	10/100M	Giga		Camera & Mic
BTO	DIS@	WIMAX@	8105ELDO@	8105ESWR@	8111E@	CAM@

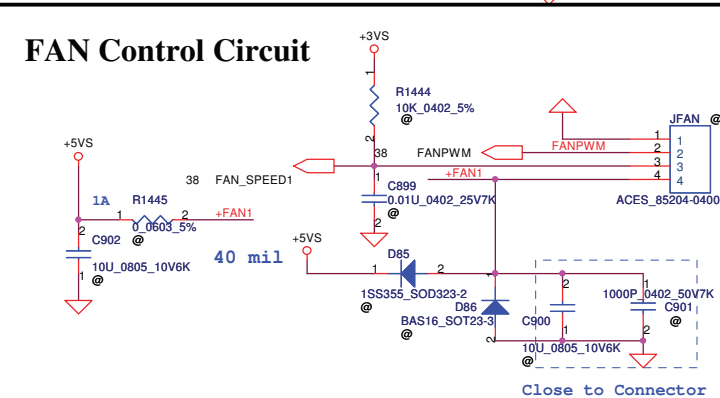
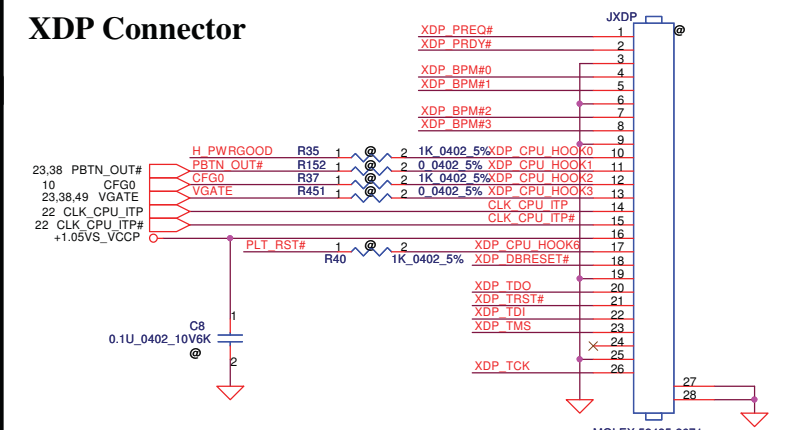
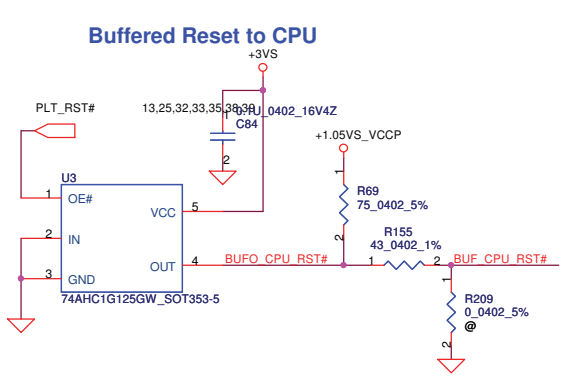
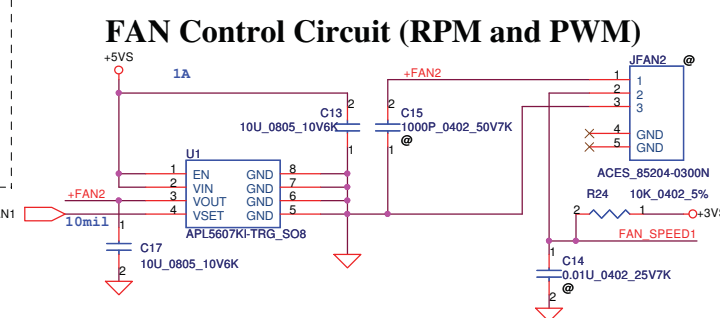
Function	PCH	HDMI/Non-HDMI	EC Chip			Zero ODD
description			930 or 9012			
explain			930	Complete	Simple	
BTO	Q65R3@	HDMI@/NHDMI@	930@	9012@	S9012@	ZODD@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

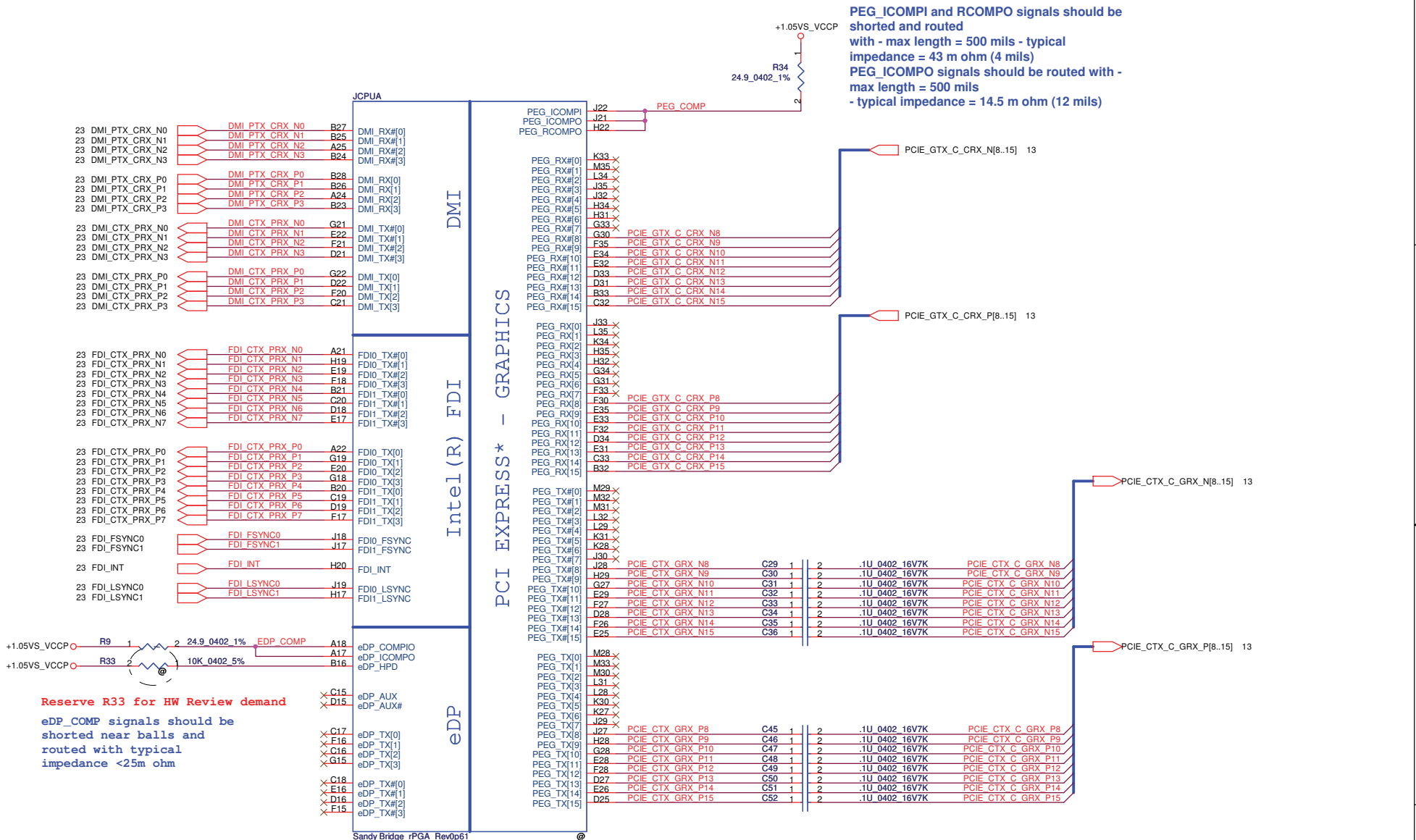
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Routed as a single daisy chain



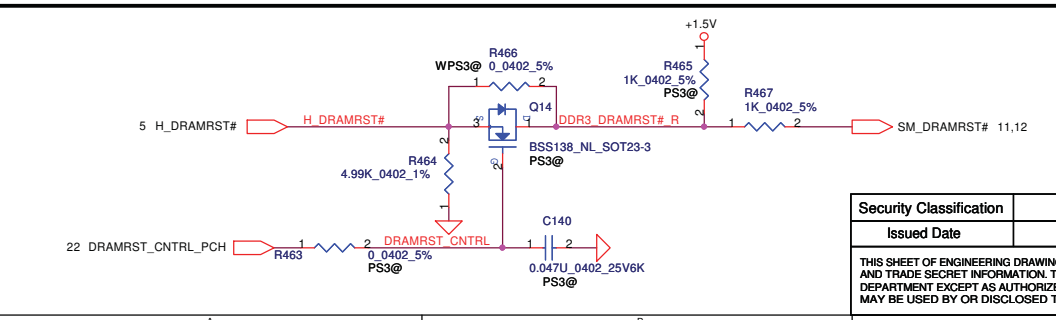
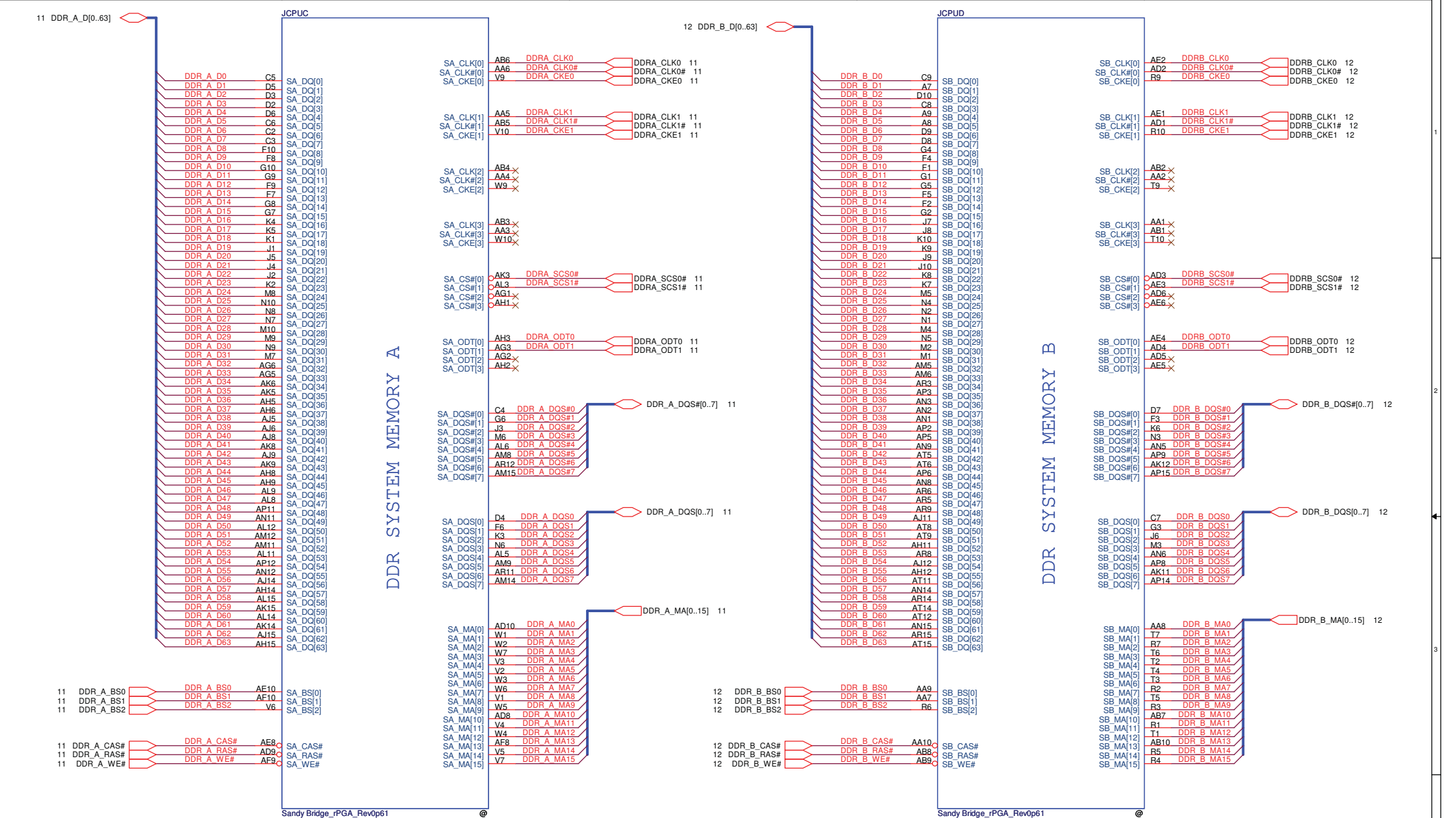
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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

Reserve R33 for HW Review demand
 eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

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- +CPU_CORE
- JCPUFP
- 53A (SV 35W)
- 8.5A
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD29 VCC26
- AD28 VCC27
- AD27 VCC28
- AD26 VCC29
- AC35 VCC30
- AC34 VCC31
- AC33 VCC32
- AC32 VCC33
- AC31 VCC34
- AC30 VCC35
- AC29 VCC36
- AC28 VCC37
- AC27 VCC38
- AC26 VCC39
- AA35 VCC40
- AA34 VCC41
- AA33 VCC42
- AA32 VCC43
- AA31 VCC44
- AA30 VCC45
- AA29 VCC46
- AA28 VCC47
- AA27 VCC48
- AA26 VCC49
- Y35 VCC50
- Y34 VCC51
- Y33 VCC52
- Y32 VCC53
- Y31 VCC54
- Y30 VCC55
- Y29 VCC56
- Y28 VCC57
- Y27 VCC58
- Y26 VCC59
- Y25 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- U35 VCC70
- U34 VCC71
- U33 VCC72
- U32 VCC73
- U31 VCC74
- U30 VCC75
- U29 VCC76
- U28 VCC77
- U27 VCC78
- U26 VCC79
- R35 VCC80
- R34 VCC81
- R33 VCC82
- R32 VCC83
- R31 VCC84
- R30 VCC85
- R29 VCC86
- R28 VCC87
- R27 VCC88
- R26 VCC89
- P35 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- P26 VCC99
- VCC100

POWER

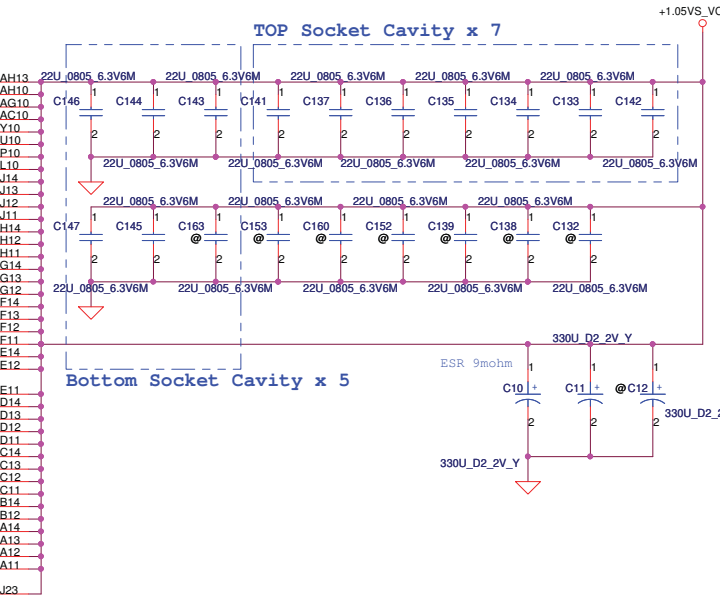
CORE SUPPLY

SENSE LINES

PEG AND DDR

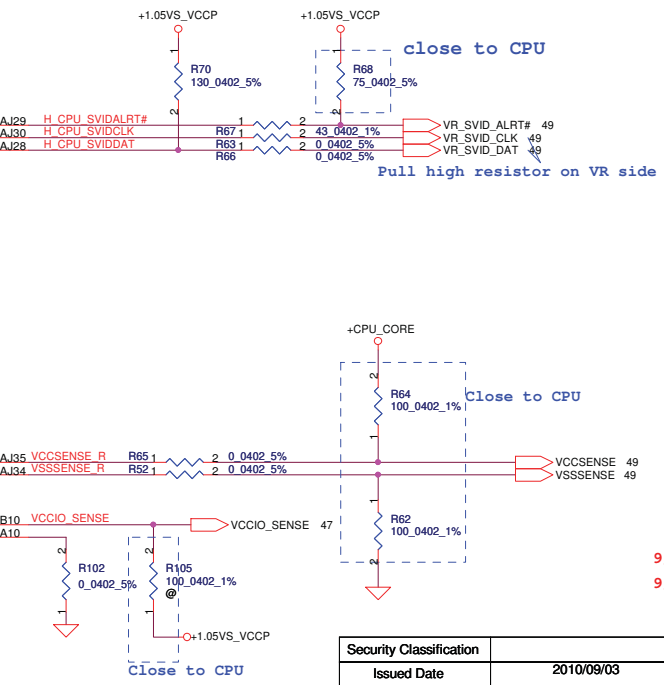
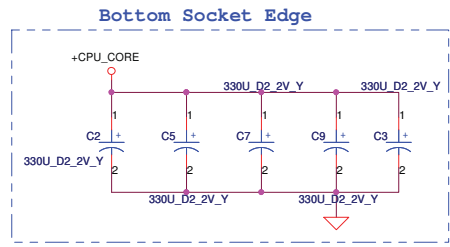
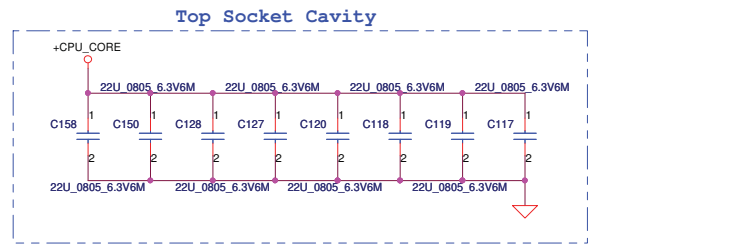
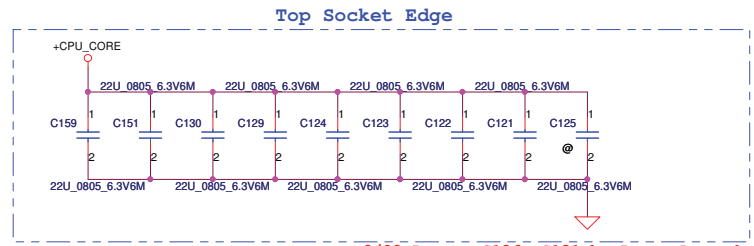
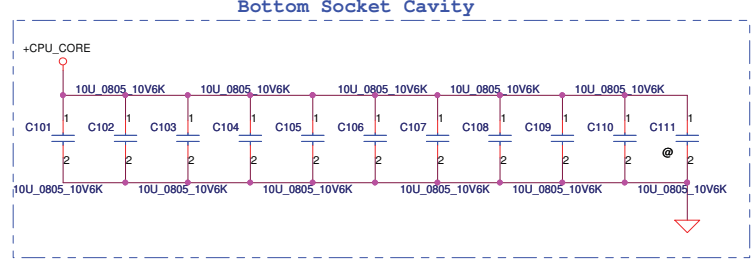
- VCCIO1 AH13
- VCCIO2 AH10
- VCCIO3 AG10
- VCCIO4 AC10
- VCCIO5 Y10
- VCCIO6 P10
- VCCIO7 L10
- VCCIO8 J14
- VCCIO9 J13
- VCCIO10 J12
- VCCIO11 J11
- VCCIO12 H11
- VCCIO13 H12
- VCCIO14 H11
- VCCIO15 G14
- VCCIO16 G13
- VCCIO17 G12
- VCCIO18 F14
- VCCIO19 F13
- VCCIO20 F12
- VCCIO21 E11
- VCCIO22 E14
- VCCIO23 E12
- VCCIO24 E11
- VCCIO25 D14
- VCCIO26 D13
- VCCIO27 D12
- VCCIO28 D11
- VCCIO29 D14
- VCCIO30 C13
- VCCIO31 C12
- VCCIO32 C11
- VCCIO33 B14
- VCCIO34 B12
- VCCIO35 A14
- VCCIO36 A13
- VCCIO37 A12
- VCCIO38 A11
- VCCIO39 J23
- VCCIO40

- VIDALERT# AJ29
- VIDSCLK AJ30
- VIDSOUT AJ28
- VCC Sense A J35
- VSS Sense A J34
- VCCIO Sense B10
- VSSIO Sense A10



+1.05VS_VCCP
+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

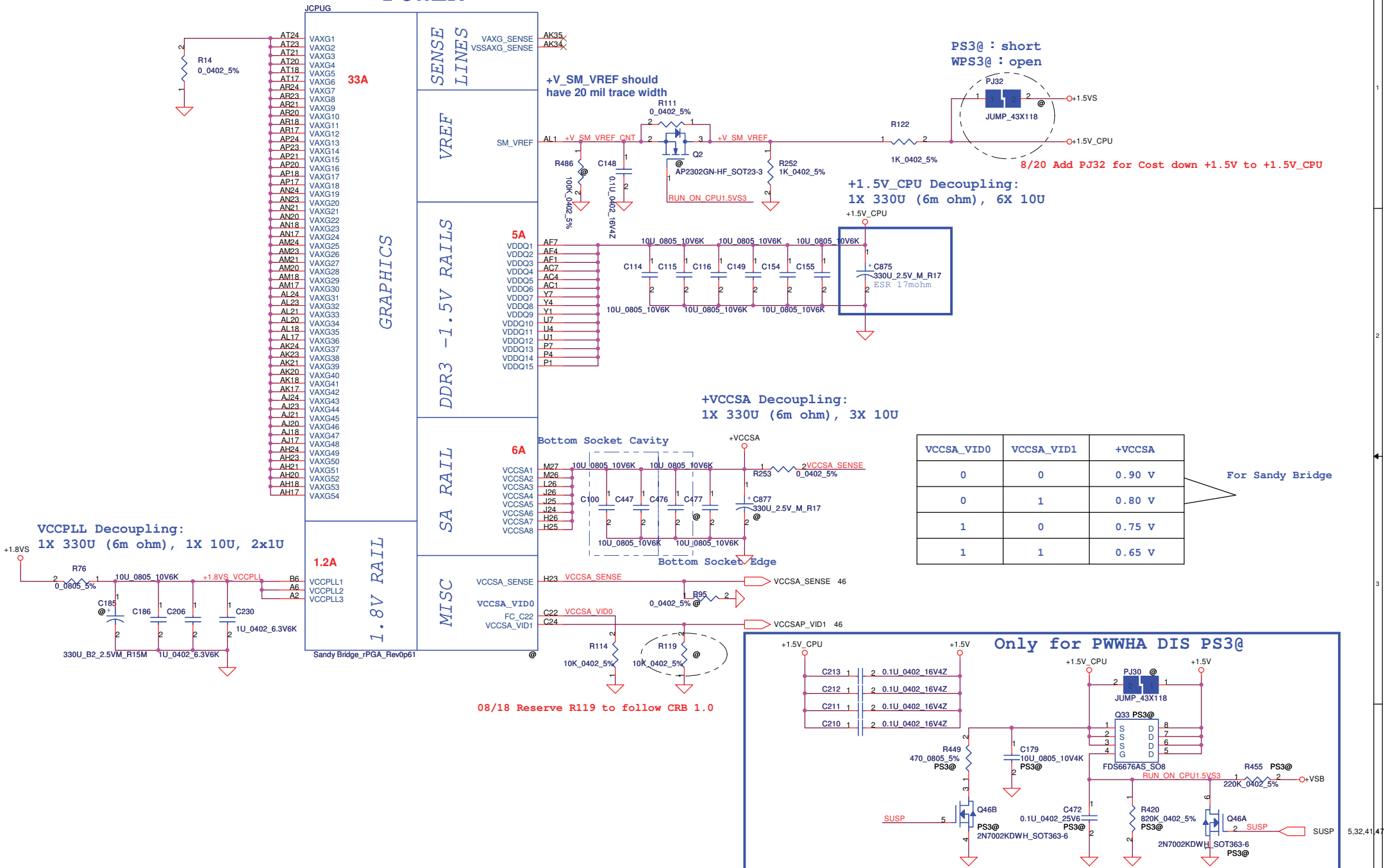
+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U



9/02 Add C898 3Pin Bulk Cap by Power Demand
9/02 Change C890, C891, C894 from SGA00005R00 to SGA00004X80 for Power demand

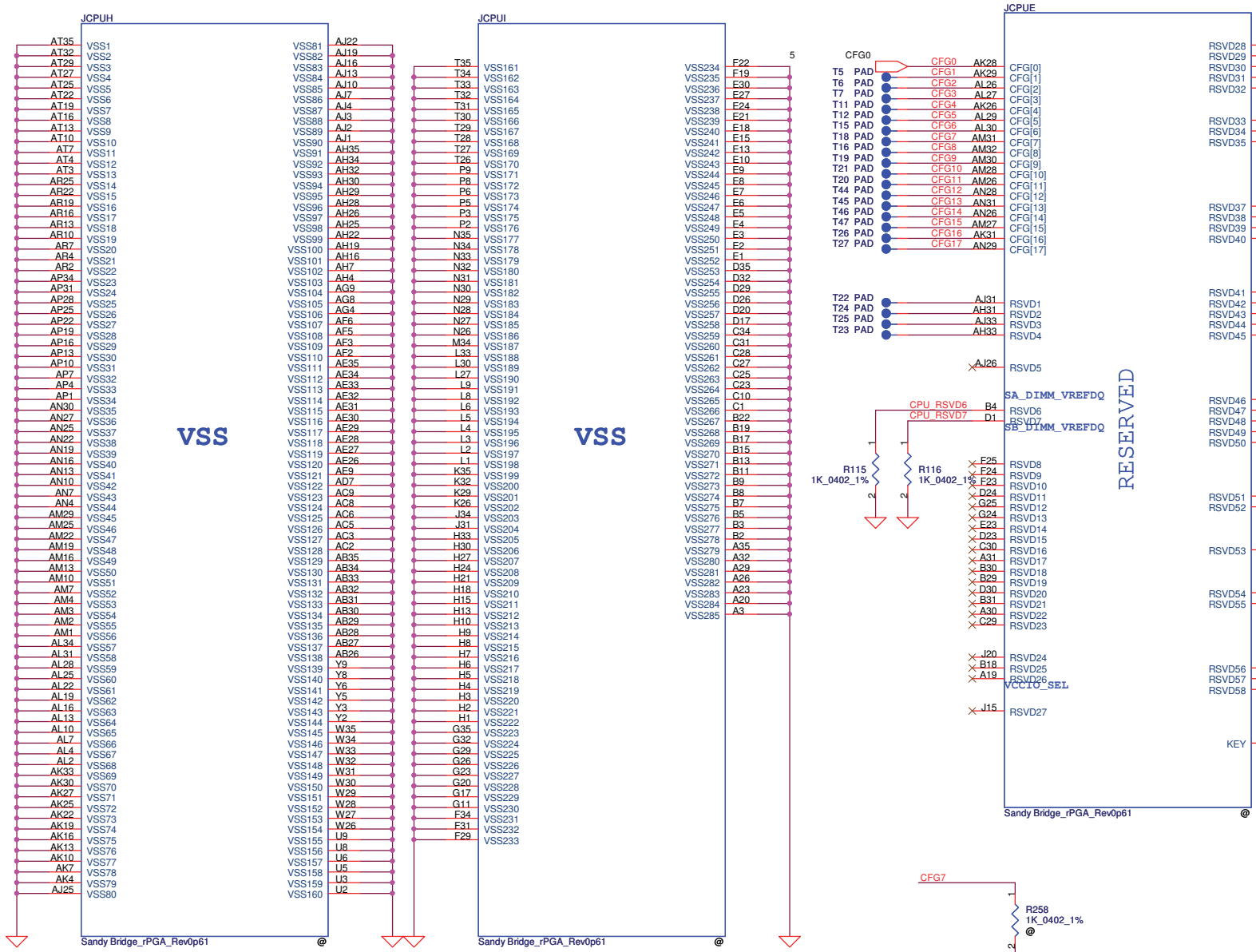
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POWER



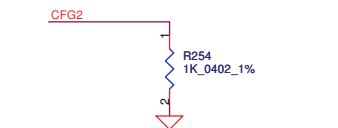
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge



CFG Straps for Processor

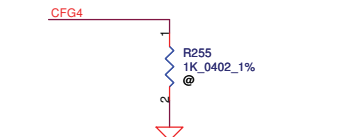
(CFG[17:0] internal pull high to VCCIO)



PEG Static Lane Reversal
- CFG2 is for the 16x

CFG2

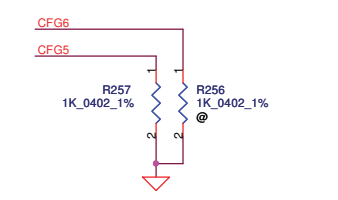
- 1: Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed



Embedded Display Port Presence Strap

CFG4

- 1: Disabled; No Physical Display Port attached to mbedded Display Port
- 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps

CFG [6:5]

- 11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
- 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

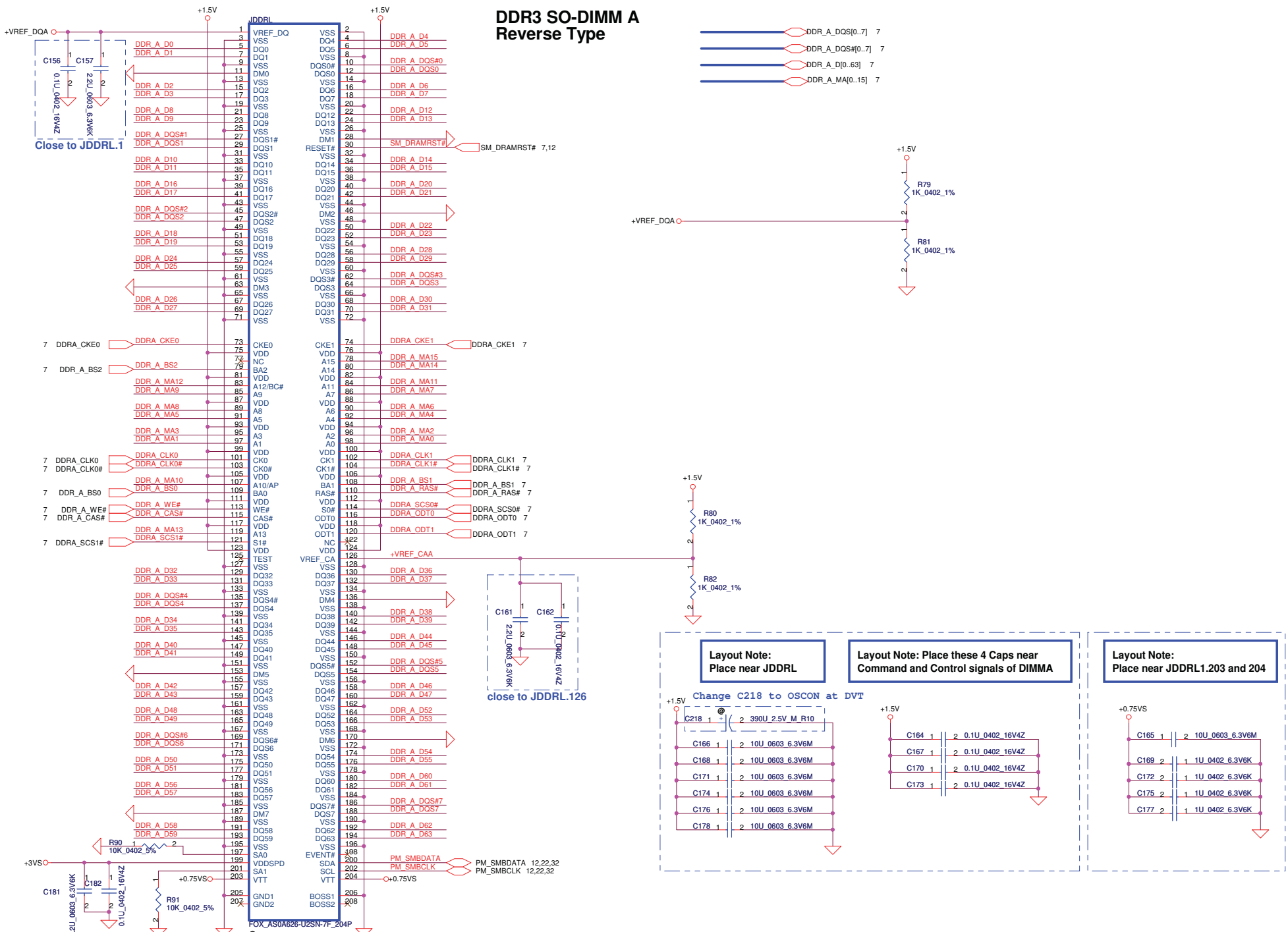
PEG DEFER TRAINING

CFG7

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS for training

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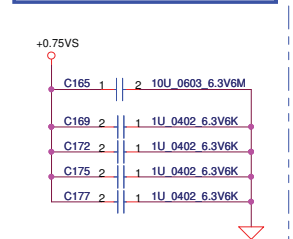
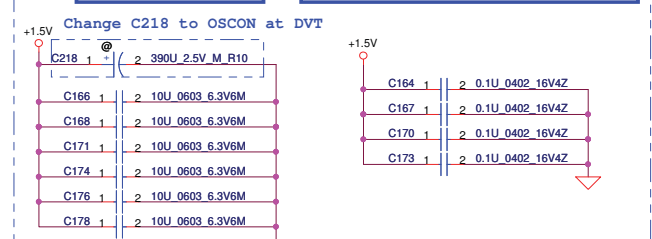
DDR3 SO-DIMM A Reverse Type



Layout Note:
Place near JDDRL

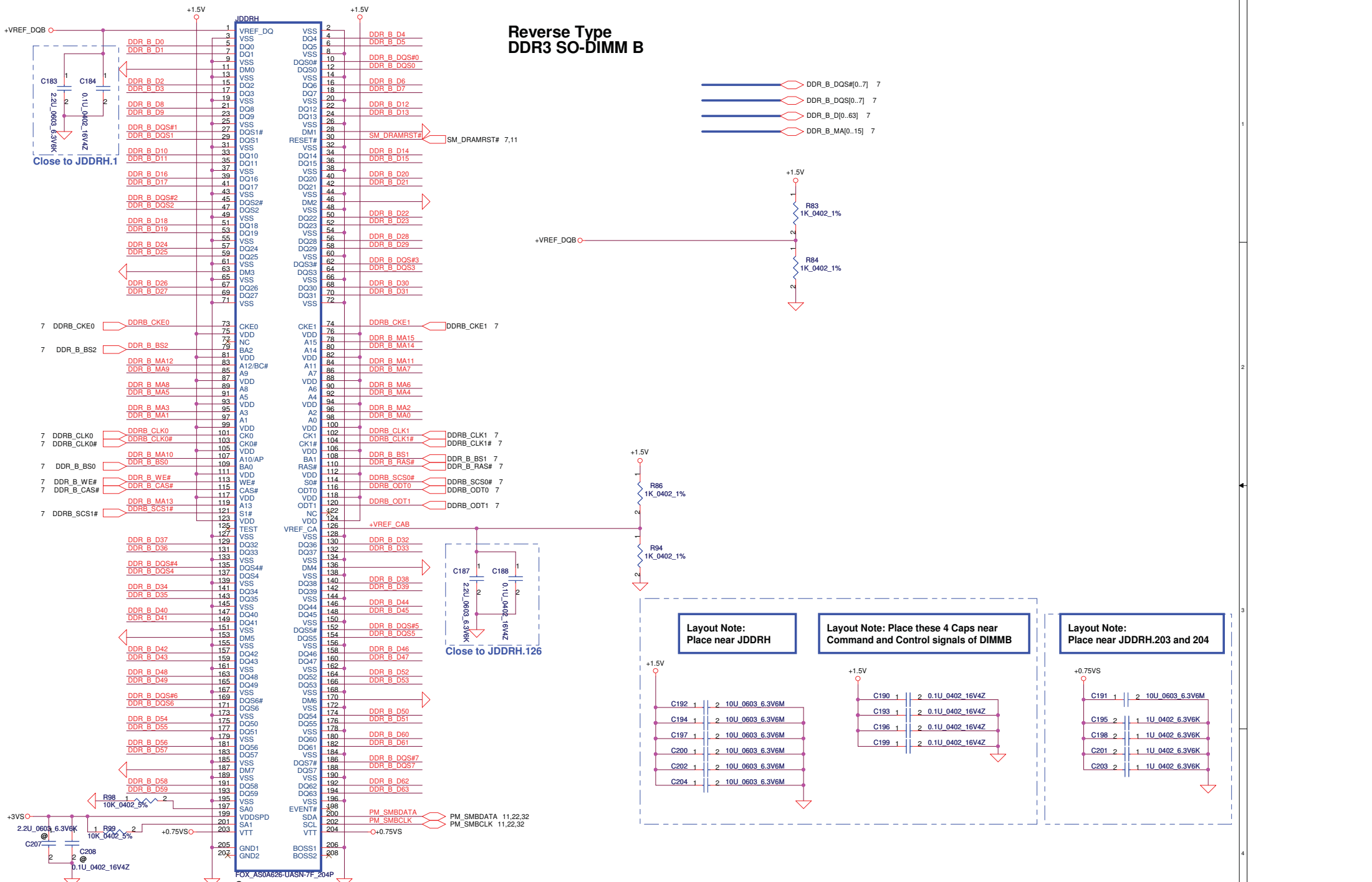
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMA

Layout Note:
Place near JDDRL1.203 and 204

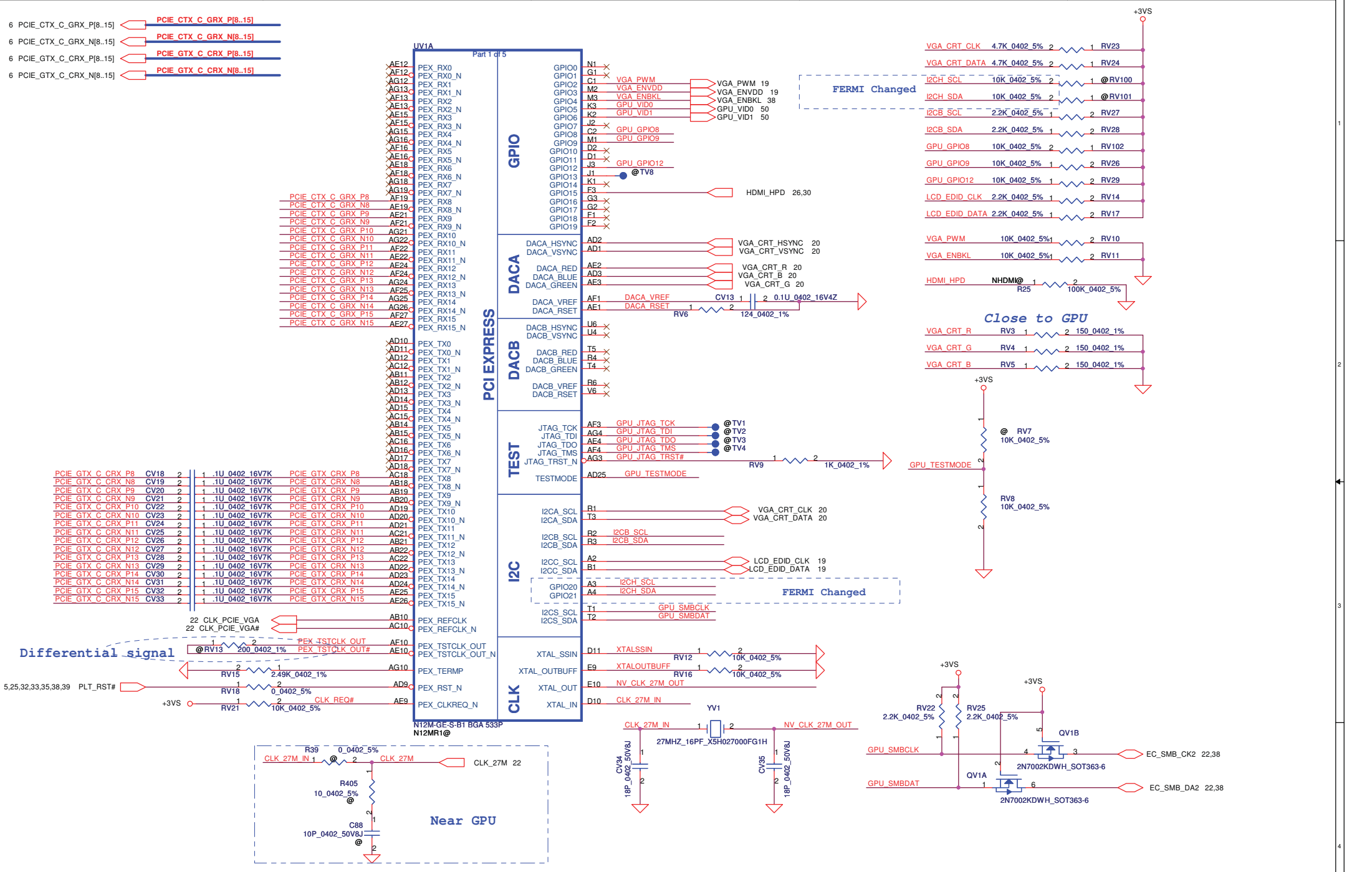


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Title	DDR3III-SODIMMO			
Size	Document Number	PWWHA LA-7201P M/B		Rev 1.0
Date:	Friday, March 04, 2011	Sheet	11	of 53

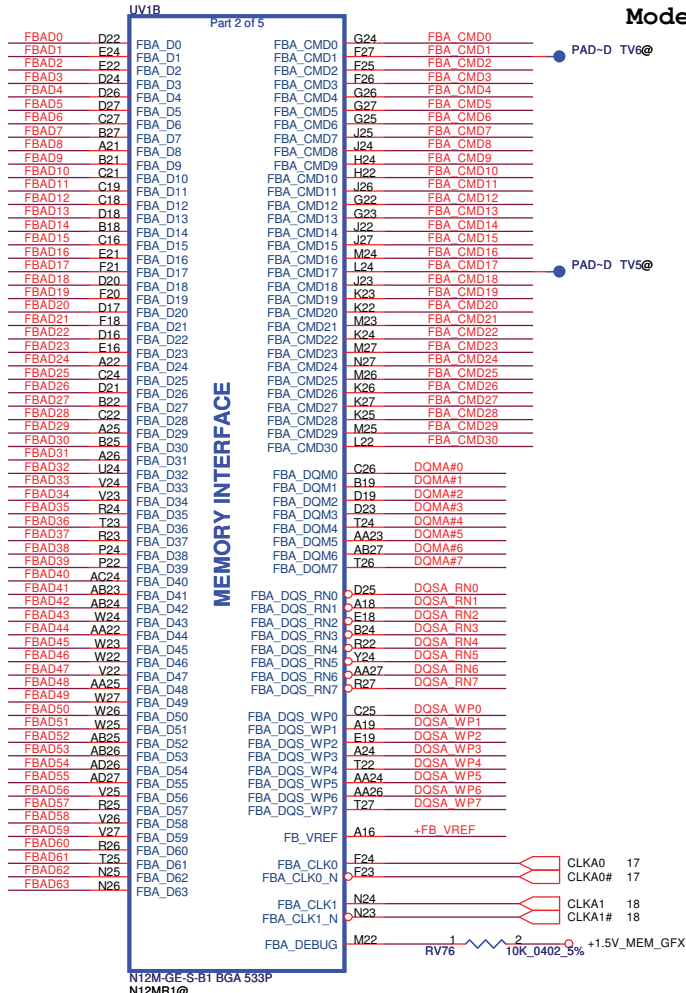
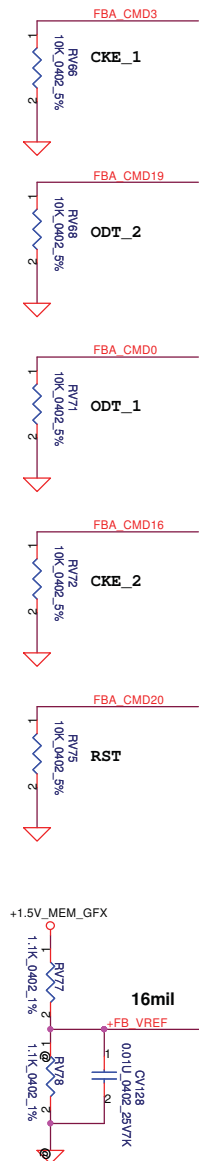
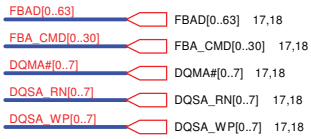
Reverse Type DDR3 SO-DIMM B



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Title	DDR3II-SODIMM1			
Size	Document Number	PWWHA LA-7201P M/B		Rev 1.0
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				PWWHA LA-7201P M/B	
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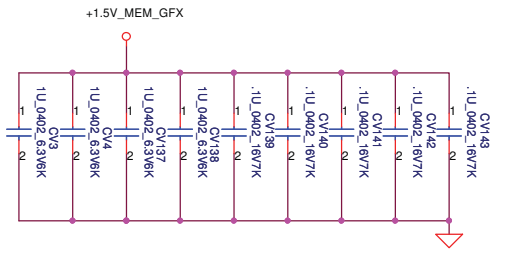
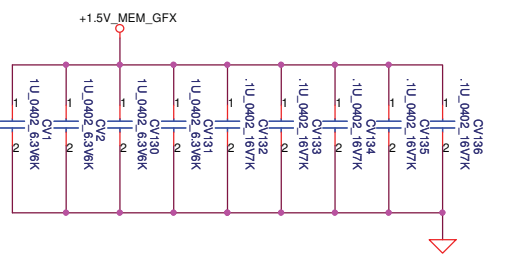
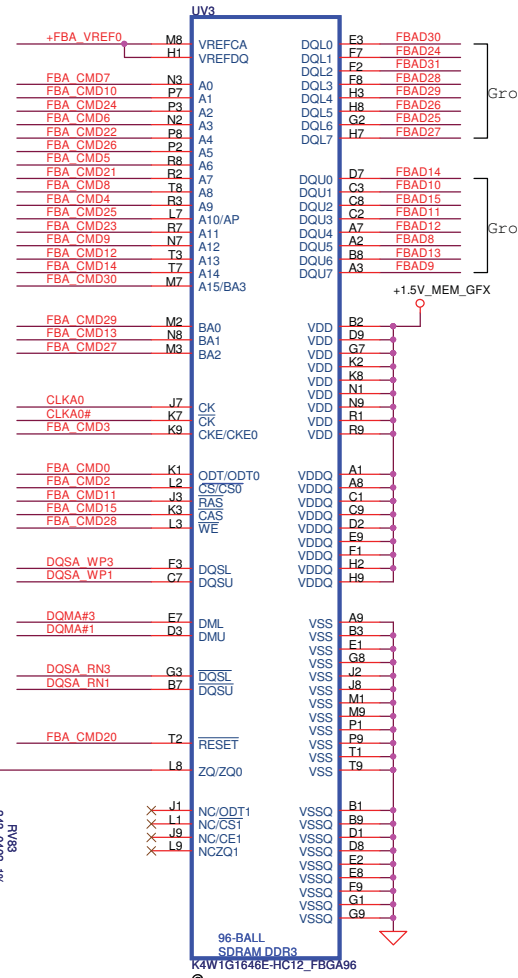
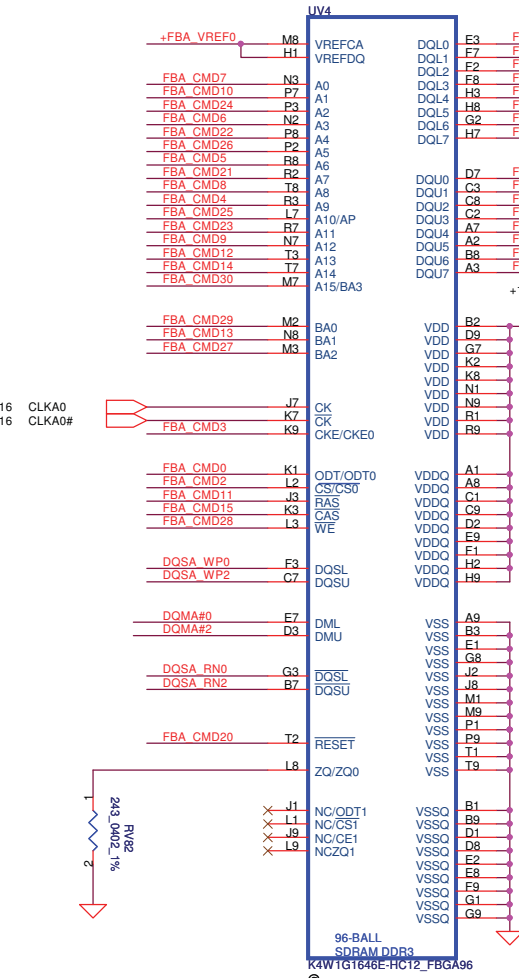
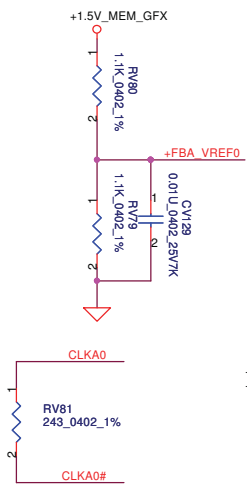
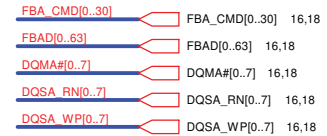
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

Memory Partition A - Lower 32 bits

16mil

16mil



Mode E - Mirror Mode Mapping

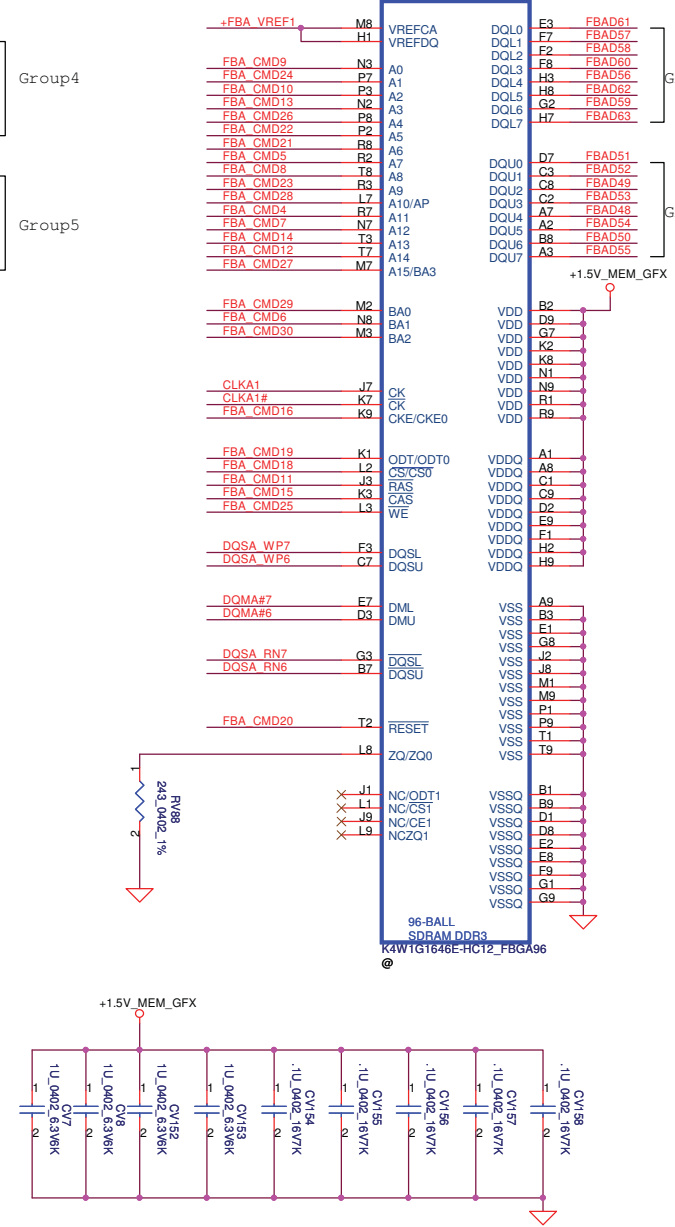
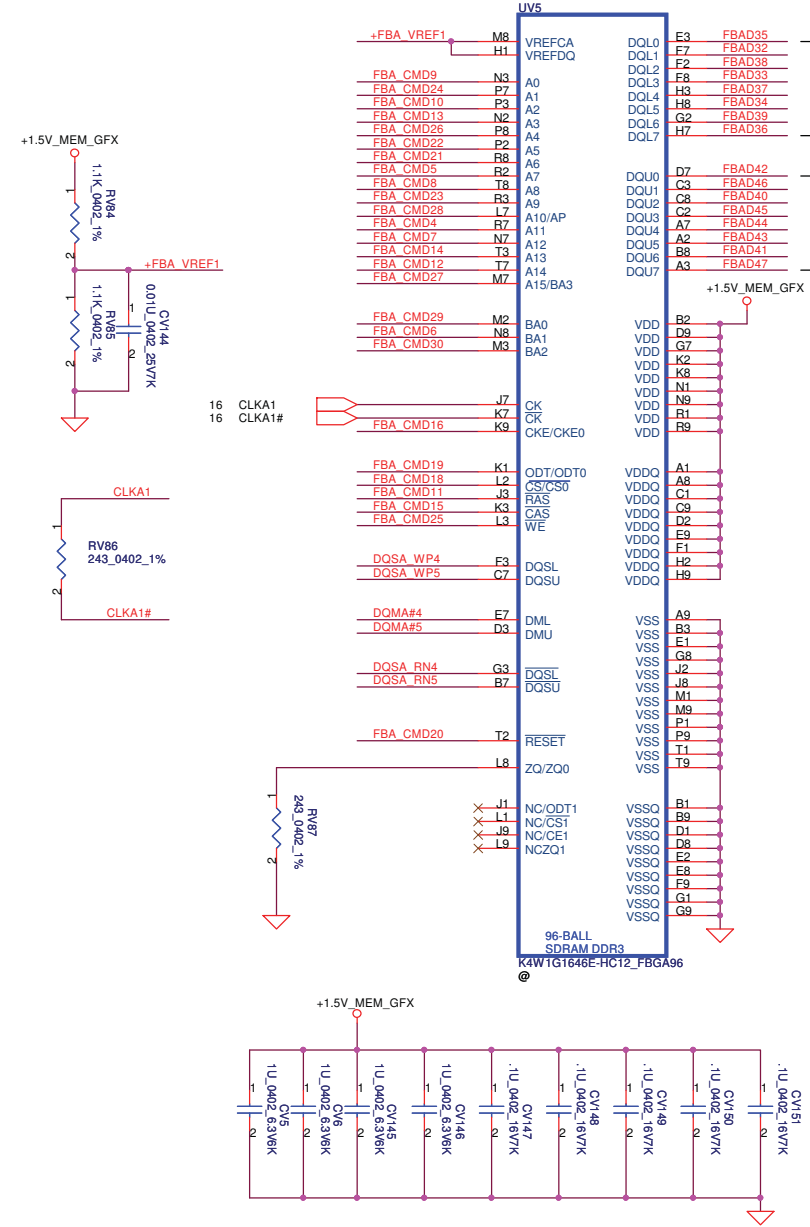
Address	DATA Bus	
	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

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				Custom	PWWHA LA-7201P M/B
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Memory Partition A - Upper 32 bits

16mi1

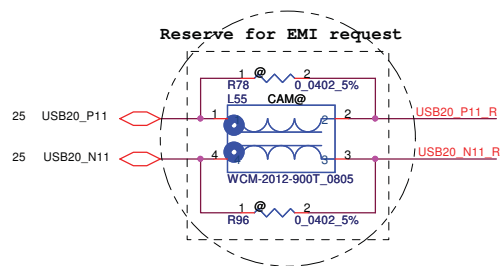
16mi1



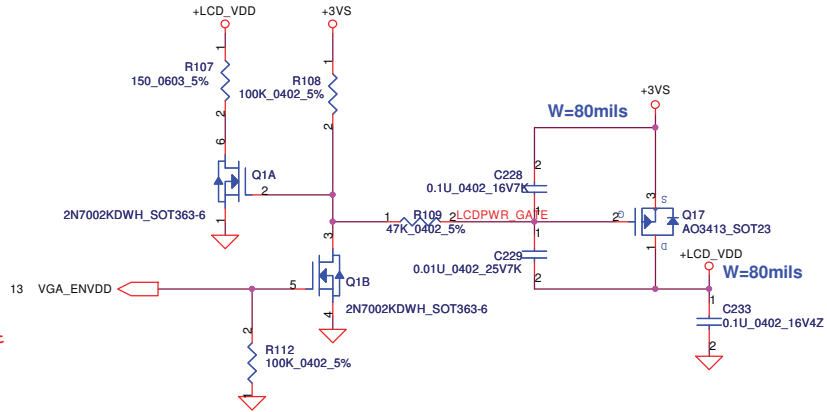
- FBAD[0..63] FBAD[0..63] 16,17
- FBA_CMD[0..30] FBA_CMD[0..30] 16,17
- DQMA#[0..7] DQMA#[0..7] 16,17
- DQSA_RN[0..7] DQSA_RN[0..7] 16,17
- DQSA_WP[0..7] DQSA_WP[0..7] 16,17

Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

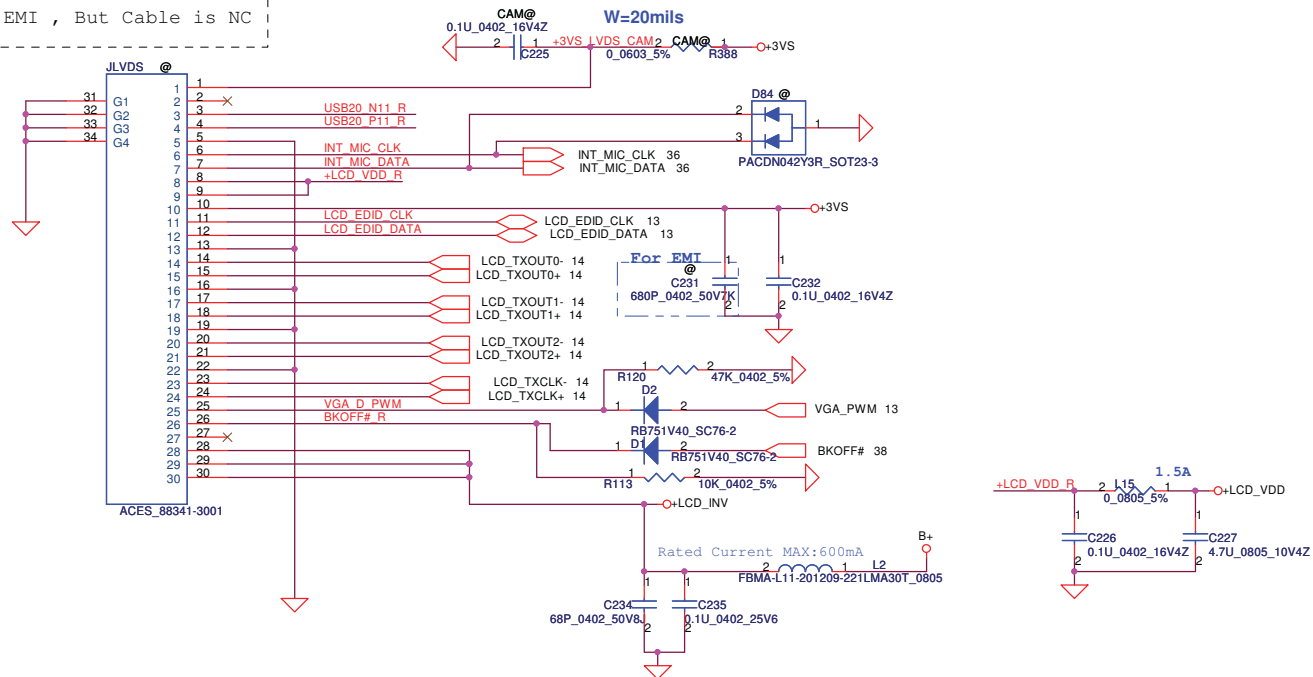


8/20 Swap USB20_P11 and USB20_N11 for layout request



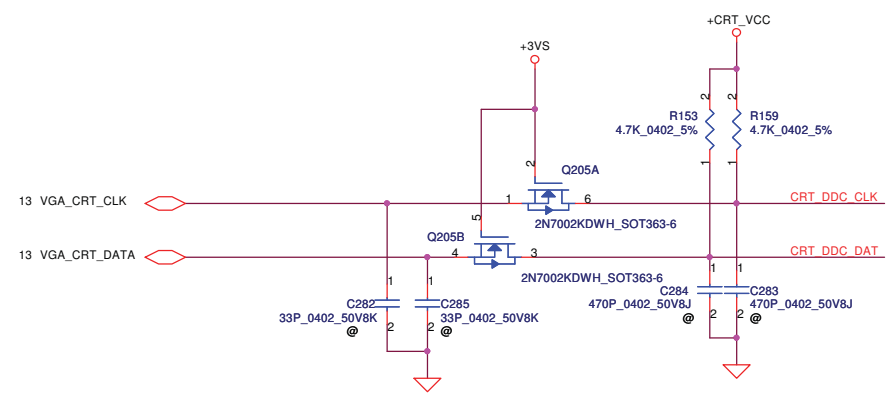
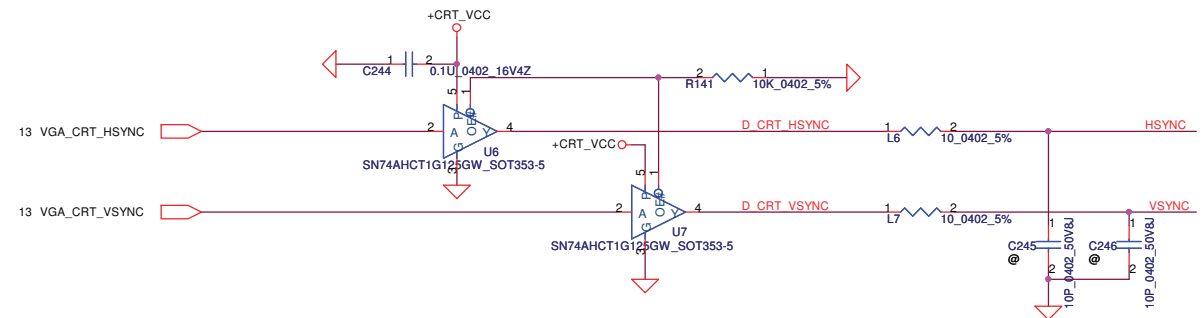
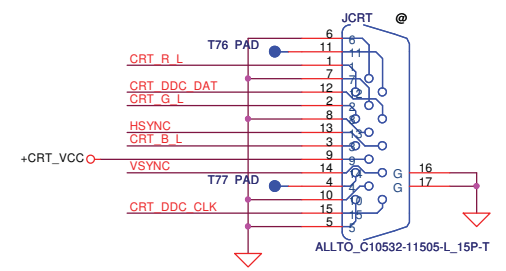
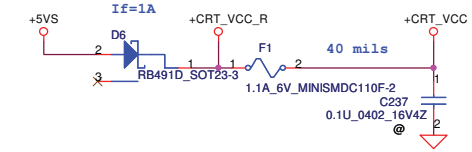
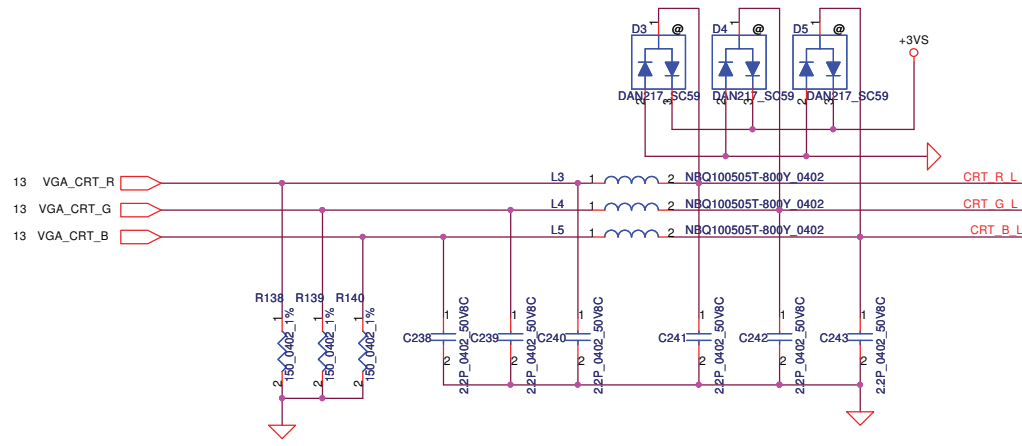
LCD/PANEL BD. Conn.

Pin13 GND for EMI , But Cable is NC

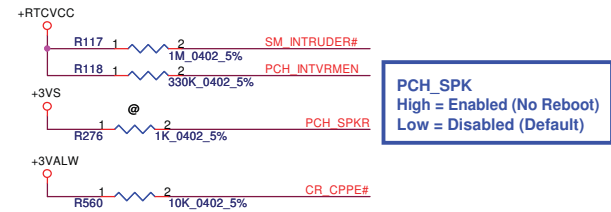
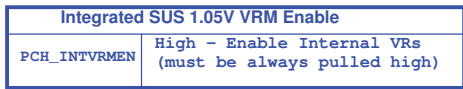
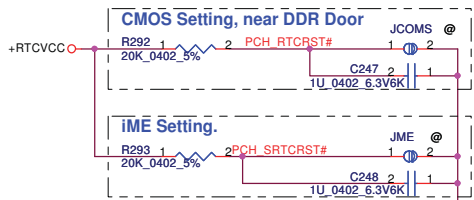


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				LVDS/eDP	
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				Document Number	
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CRT CONNECTOR

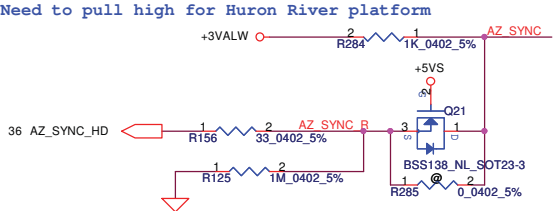


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Size	Document Number	Rev		1.0	
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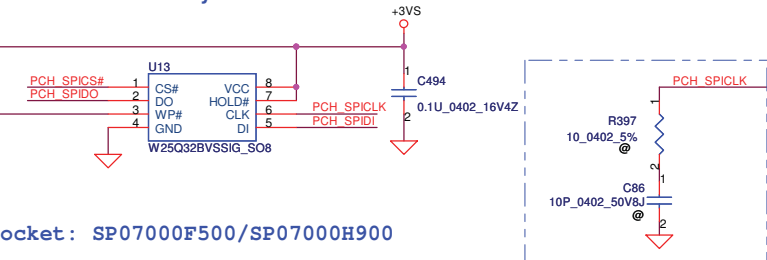


HDA_SDO
ME debug mode, this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

HDA_SYNC
★This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform



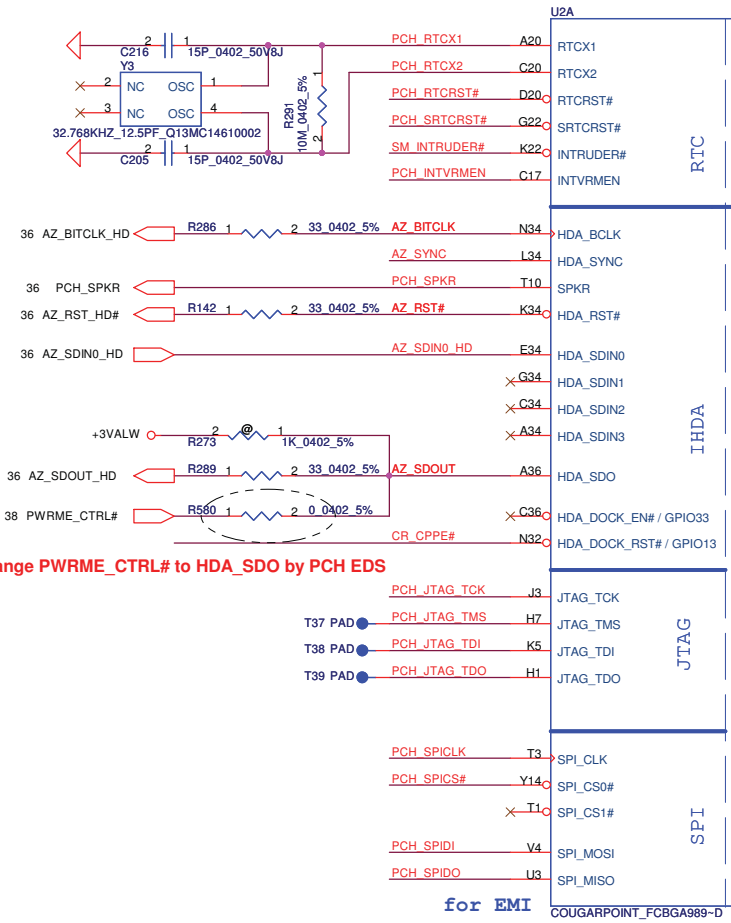
4M Byte



Socket: SP07000F500/SP07000H900

Please close to U2 PCH

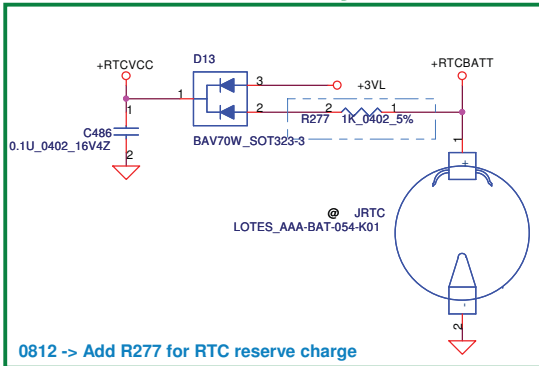
8/30 Change U13 from SA000021A00 to SA000031N00 due to EOL of SA000021A00



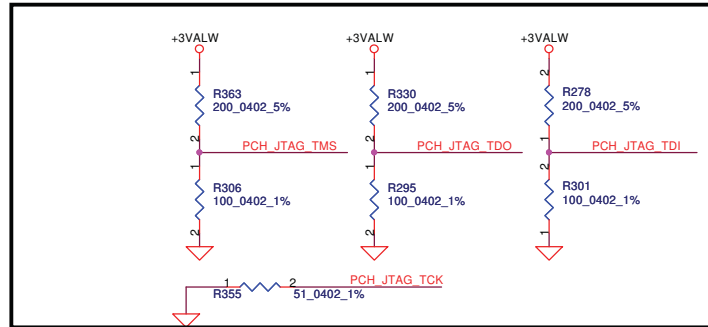
8/30 Change PWRME_CTRL# to HDA_SDO by PCH EDS

for EMI
PCH_JTAG_TCK J3
T37 PAD PCH_JTAG_TMS H7
T38 PAD PCH_JTAG_TDI K5
T39 PAD PCH_JTAG_TDO H1
PCH_SPICLK T3
PCH_SPICS# Y14
T1 C SPI_CS1#
PCH_SPIDI V4
PCH_SPIDO U3

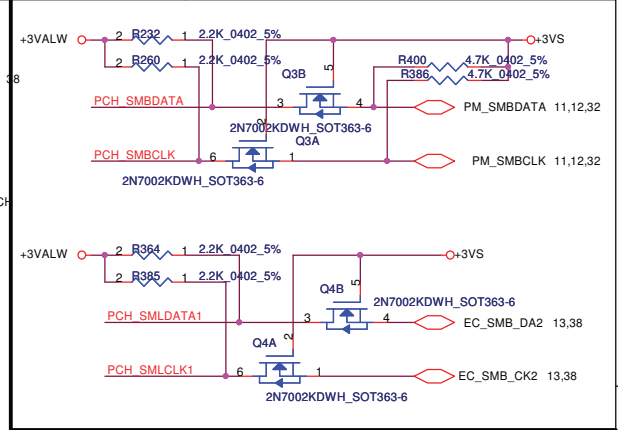
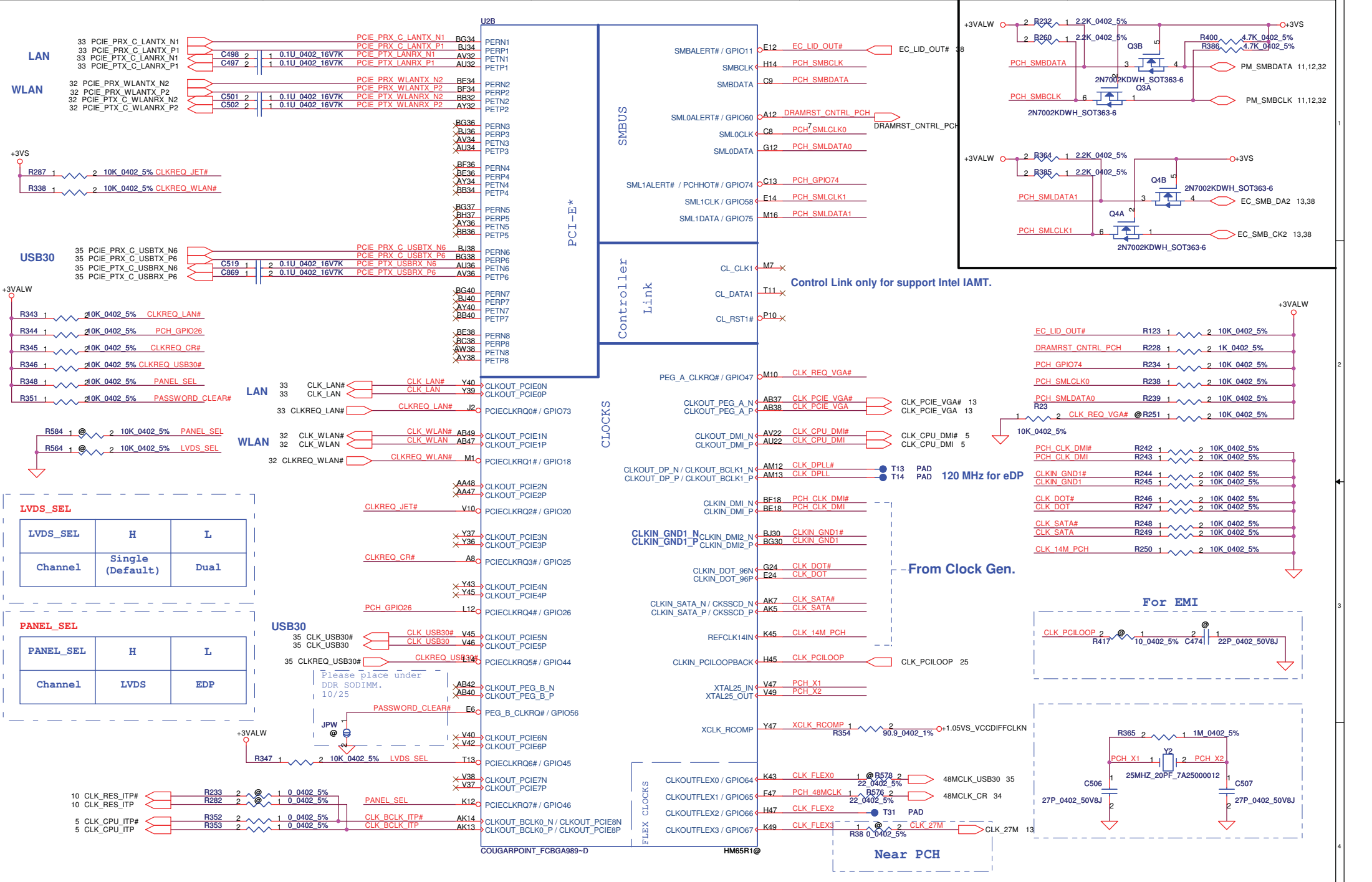
RTC schematic for non-chargeable



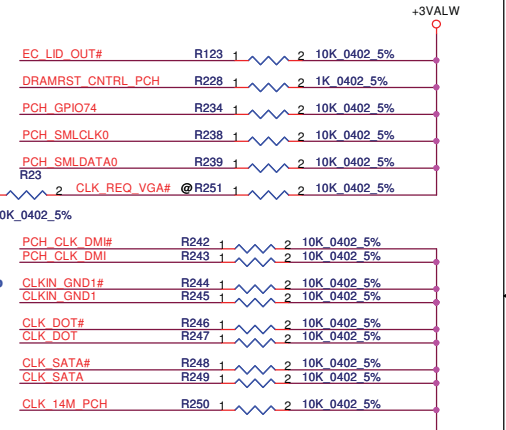
0812 -> Add R277 for RTC reserve charge



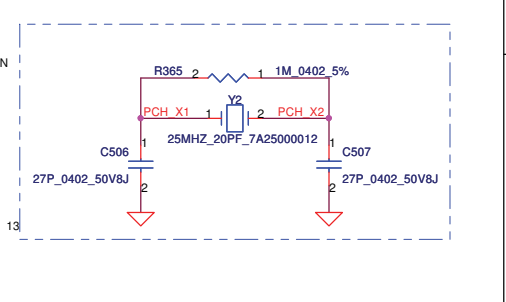
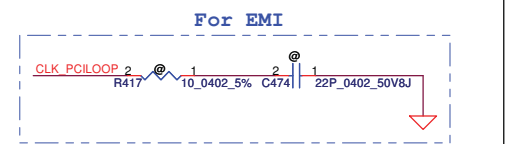
Security Classification		Compal Secret Data		Title	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	PCH_HDA/JTAG/SATA/SPI/LPC	
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Control Link only for support Intel IAMT.

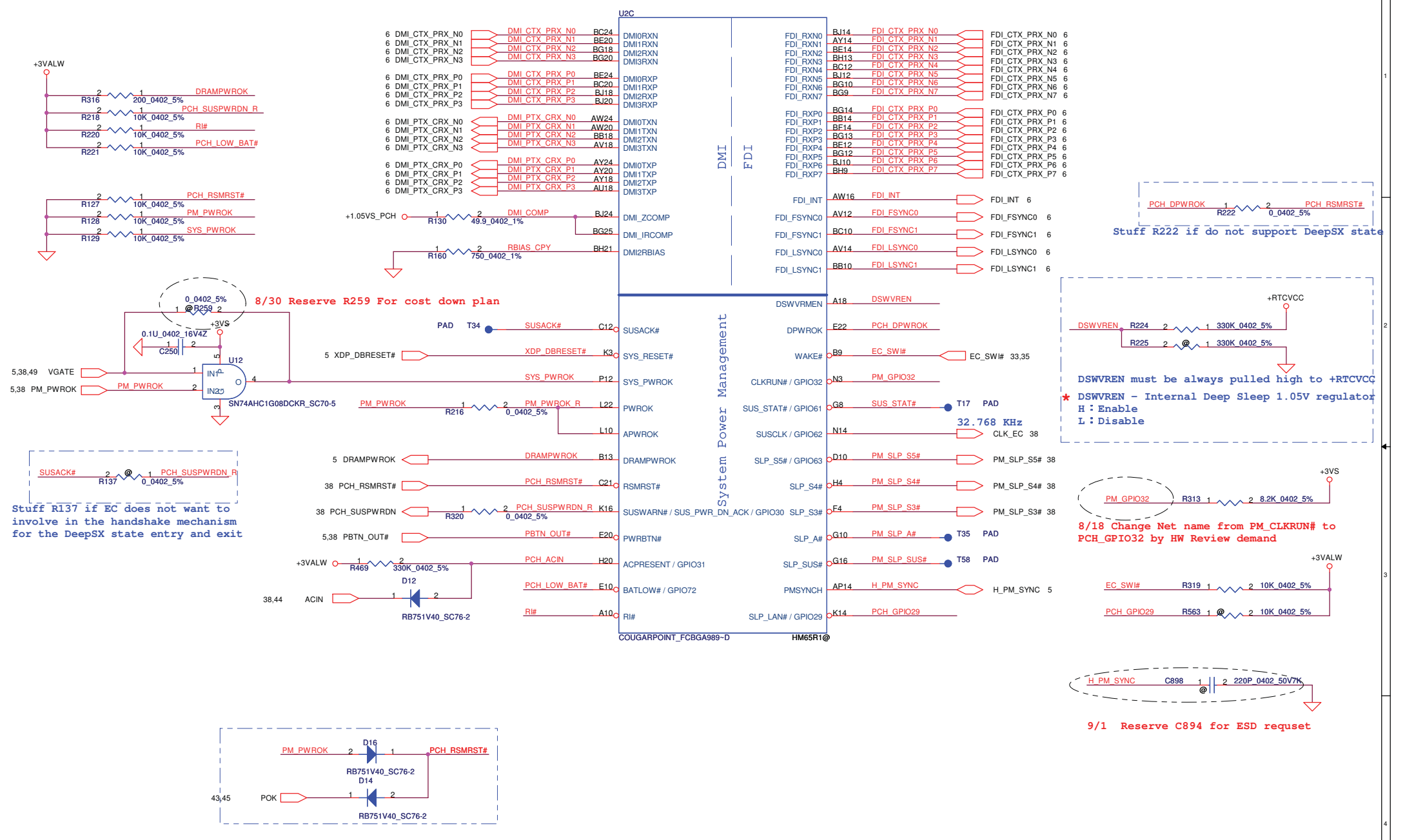


From Clock Gen.

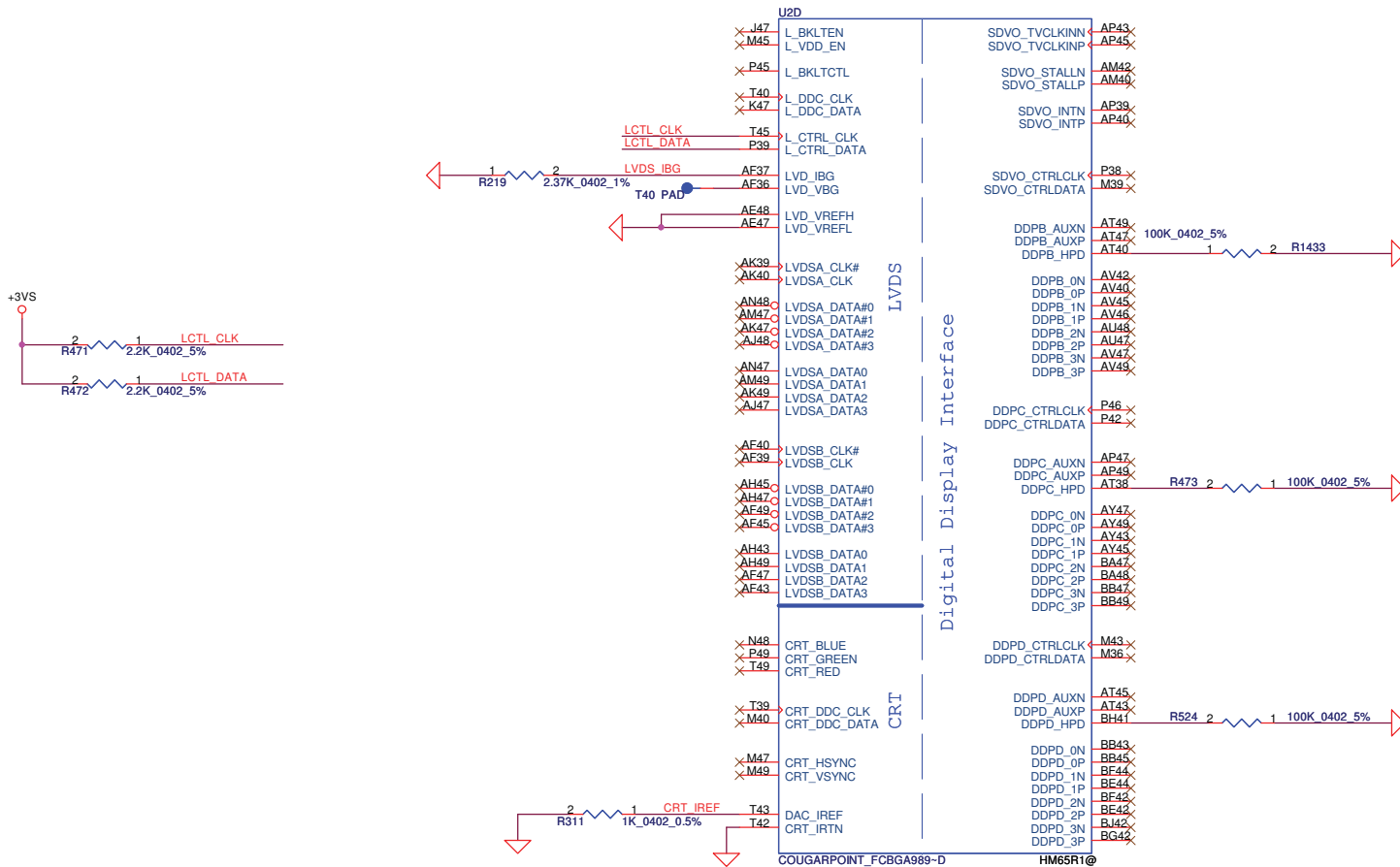


Near PCH

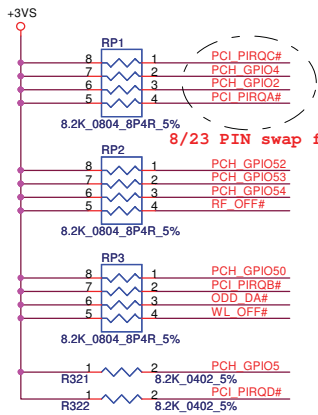
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				PCH_DMI/FDI/PM	
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Size	Custom	Document Number	PWWHA LA-7201P M/B		Rev
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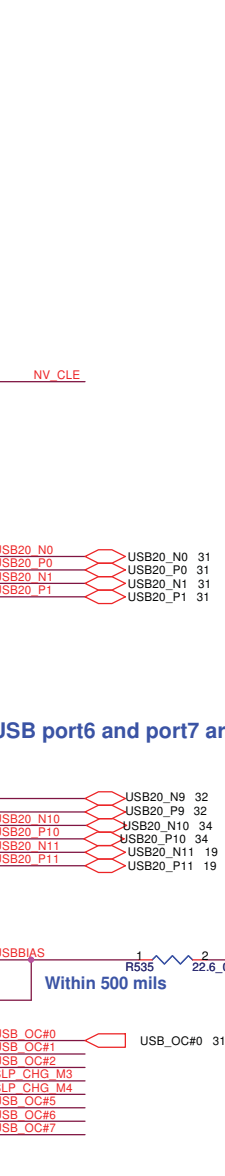
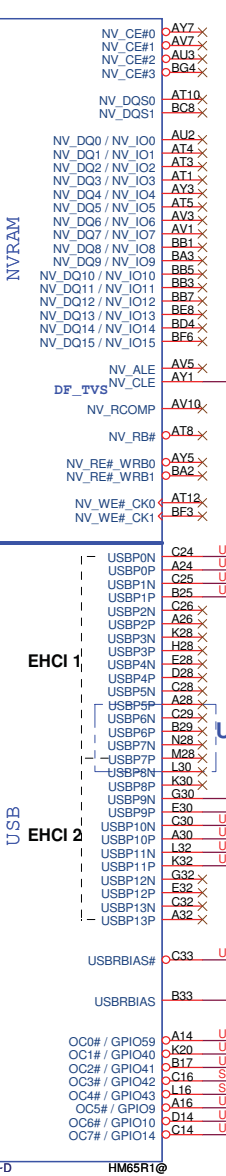
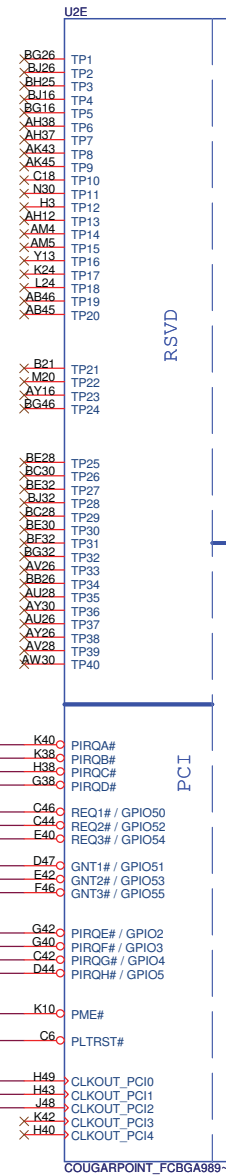
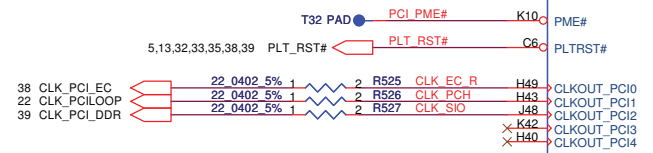
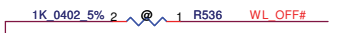


8/23 PIN swap for layout request

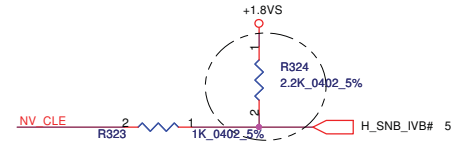
Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *



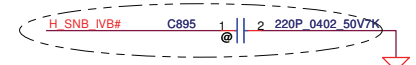
A16 Swap Override Strap	
WL_OFF#	Low= A16 swap override Enable * High= A16 swap override Disable
32	WL_OFF#
31	ODD_DA#



DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW



8/18 Change R324 From 1K to 2.2K by Intel check list demand

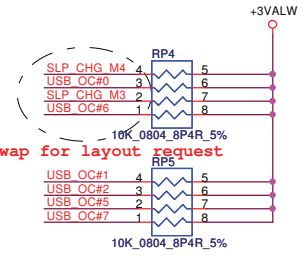


9/1 Reserve C895 for ESD request

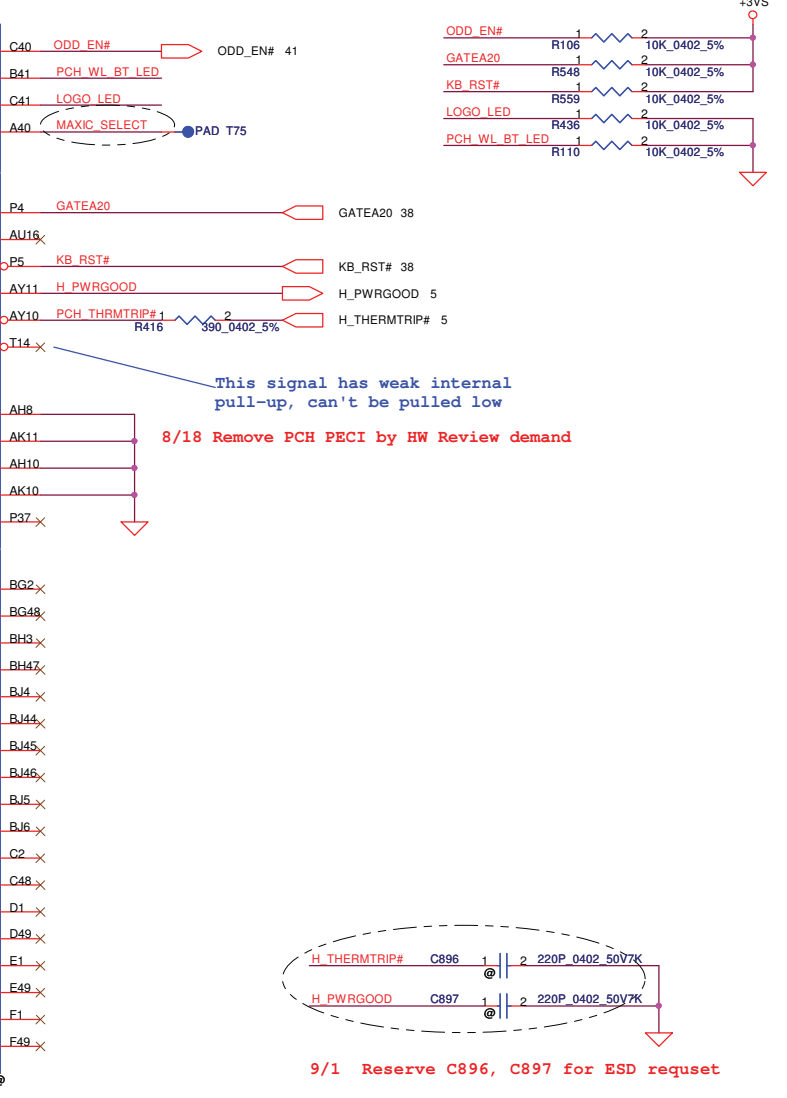
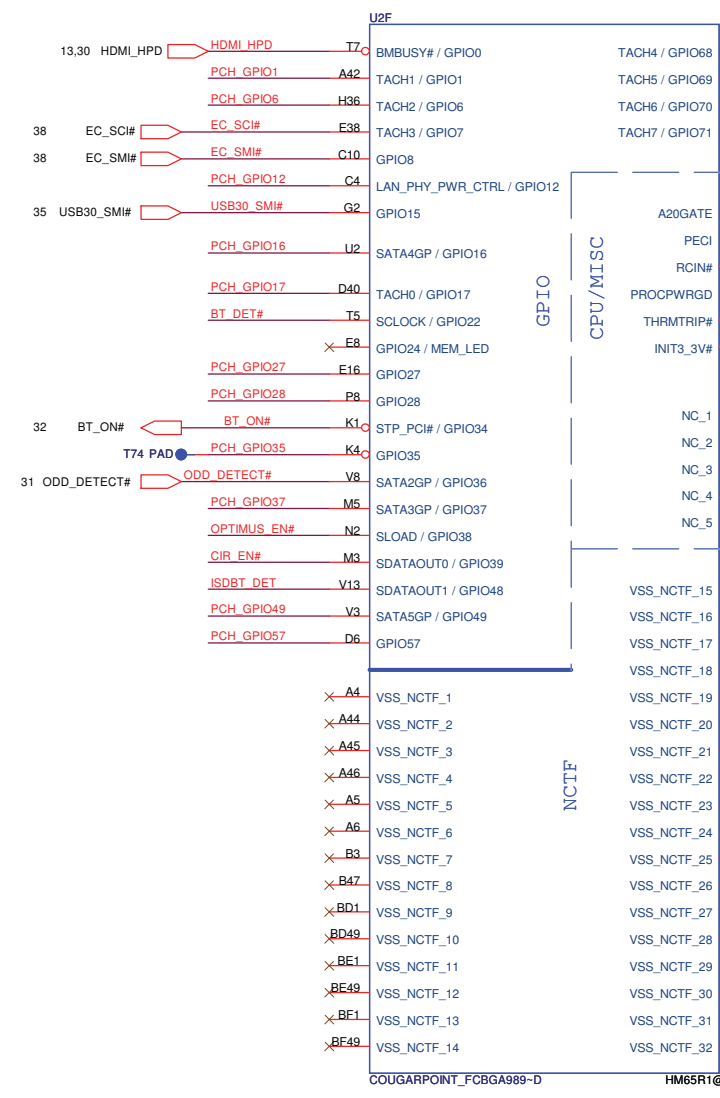
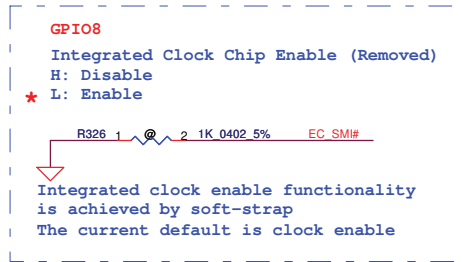
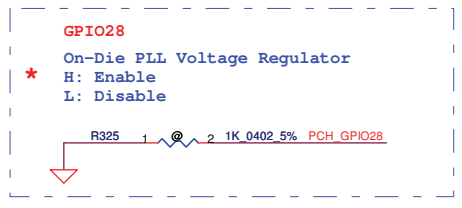
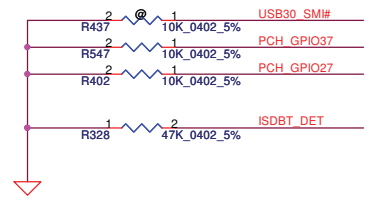
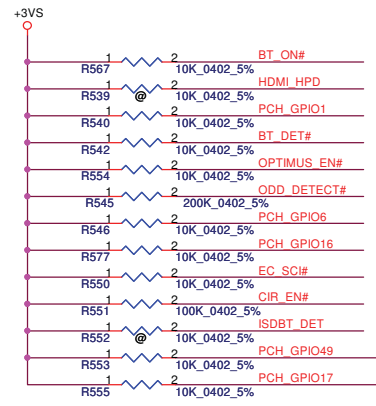
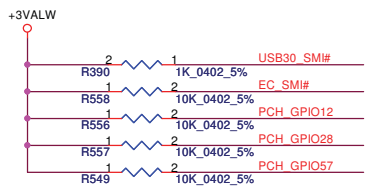
USB-LEFT1
USB-LEFT2

USB port6 and port7 are disabled on HM65

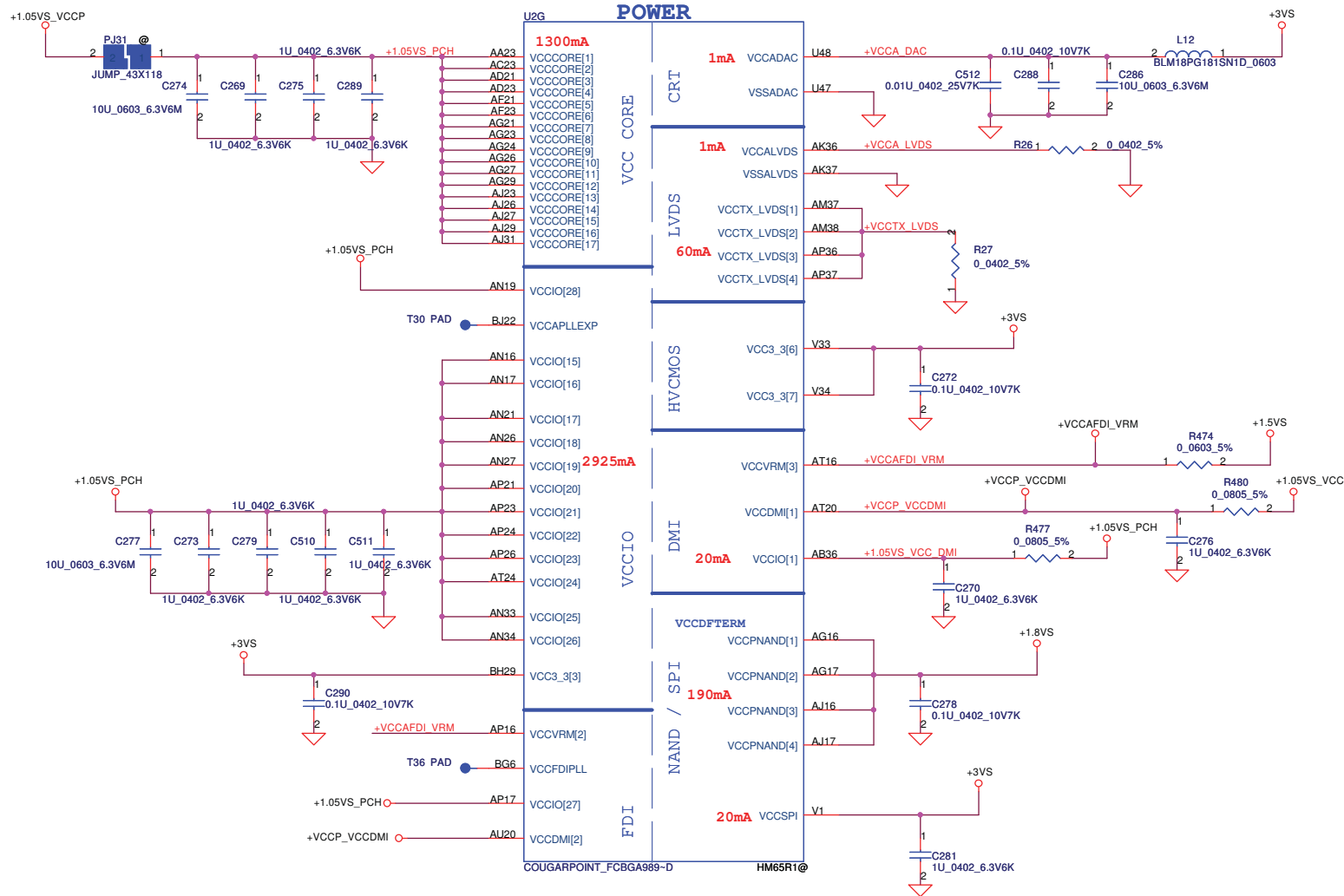
WiMax
Card Reader
Int. Camera



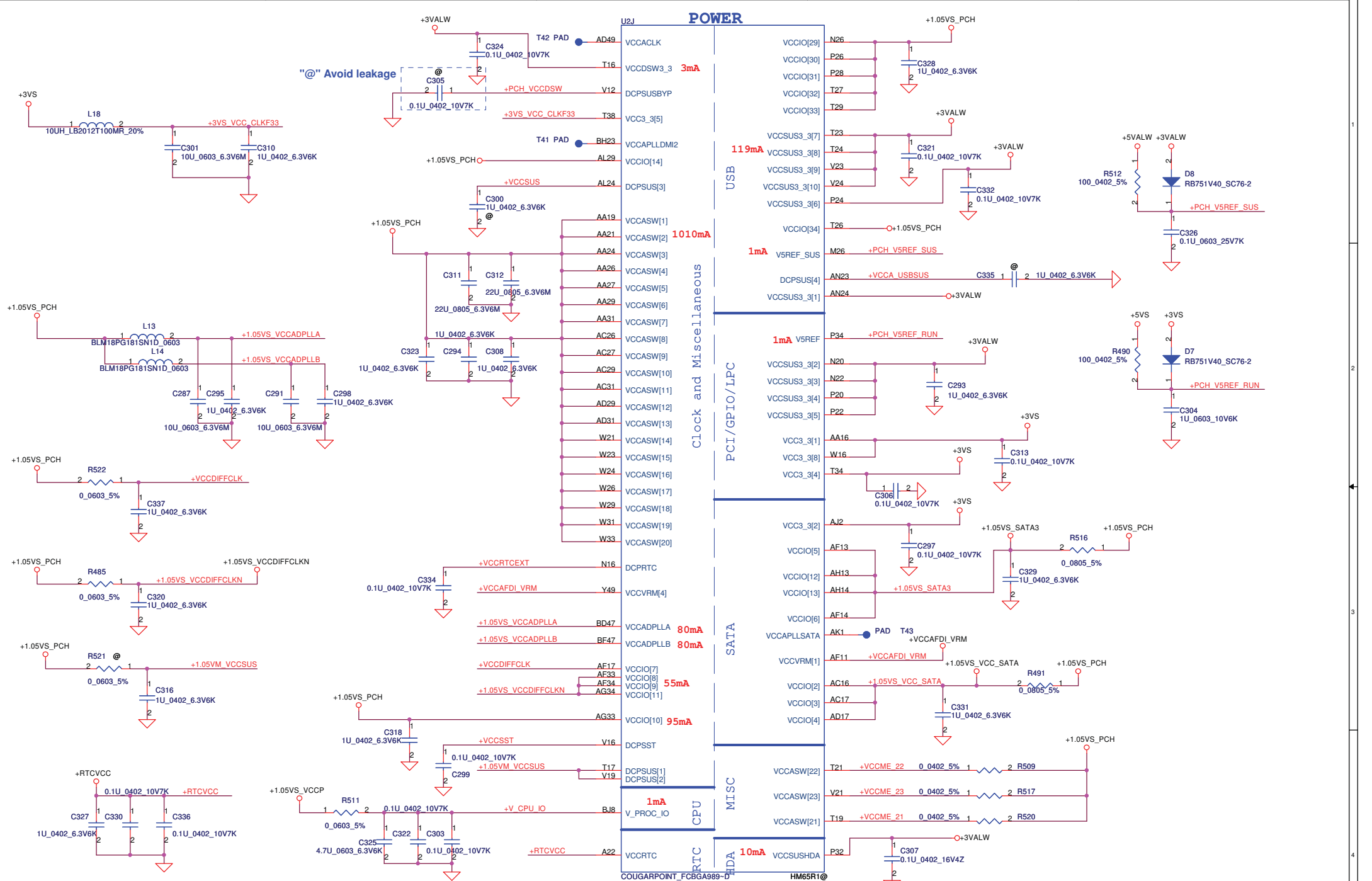
8/23 PIN swap for layout request



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Date: Friday, March 04, 2011		Sheet 26 of 53		Compal Electronics, Inc.	
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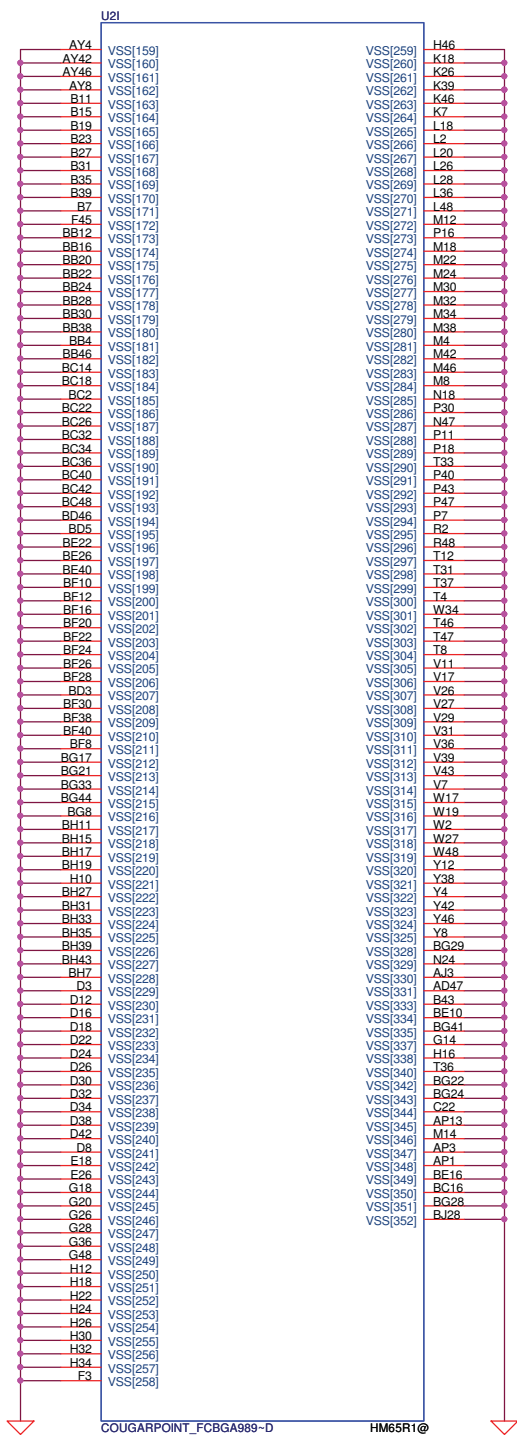


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



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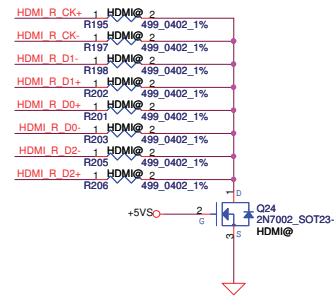
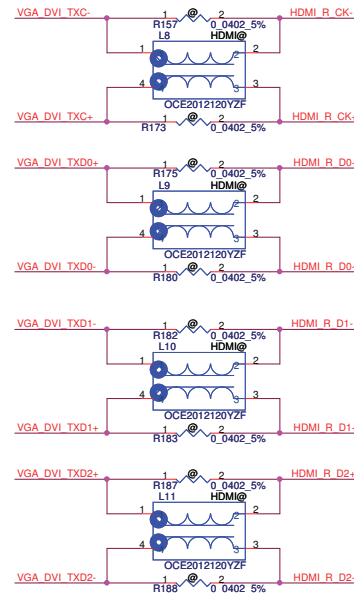
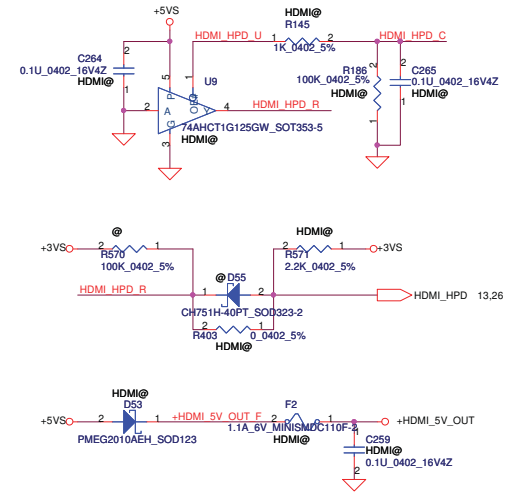
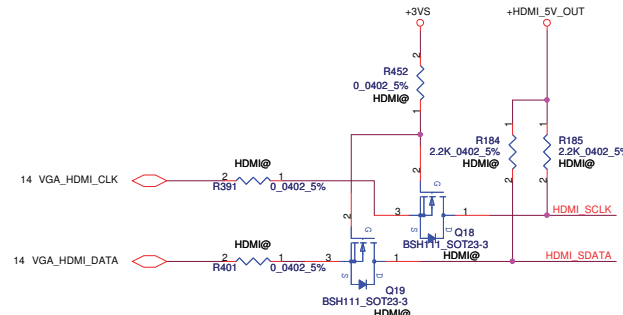
PCH_POWER-2
PWWHA LA-7201P M/B



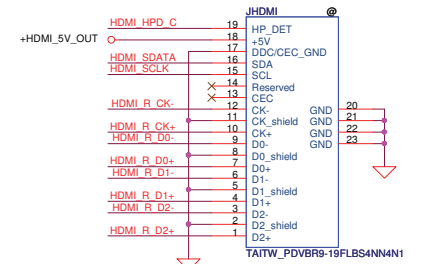
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For DISCRETE

14	VGA_HDMI_CLK-	CV296	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXC+
14	VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXC-
14	VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD0+
14	VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD0-
14	VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD1+
14	VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD1-
14	VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K	HDMI@	VGA_DVI_TXD2+
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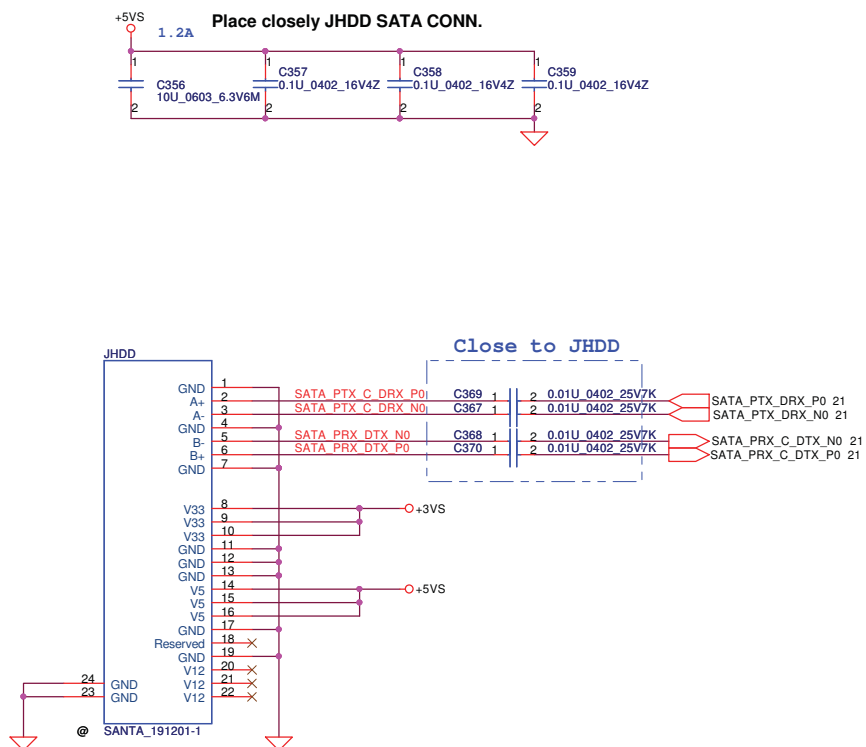


HDMI Connector

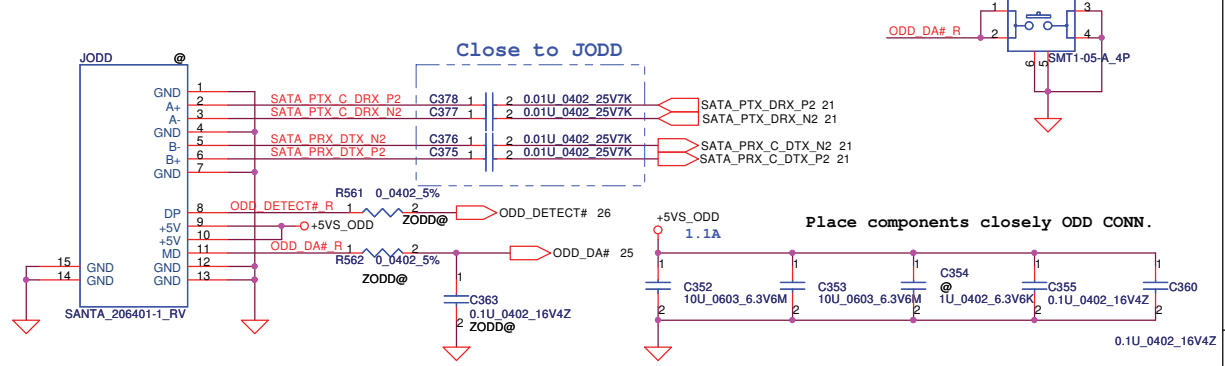


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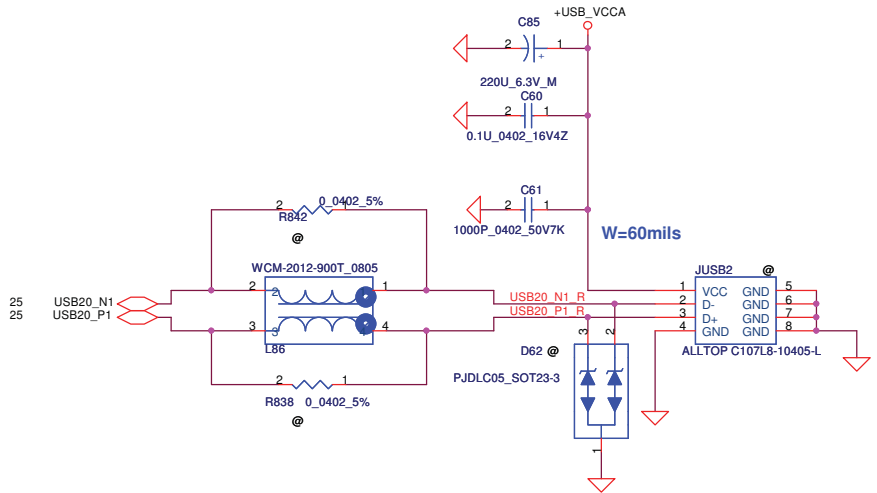
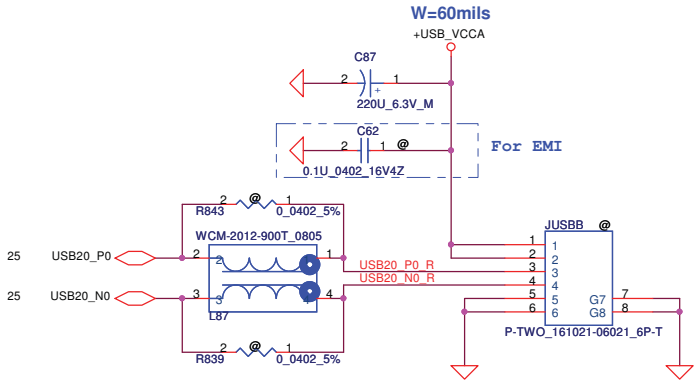
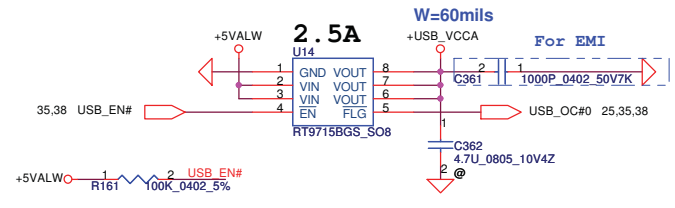
SATA HDD Conn



SATA ODD Conn



USB Conn



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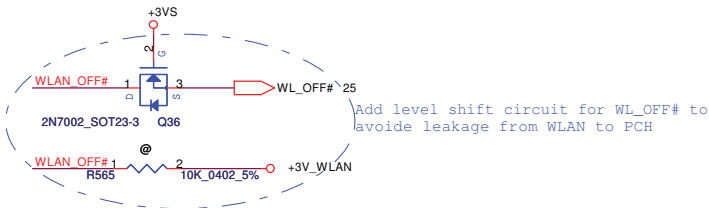
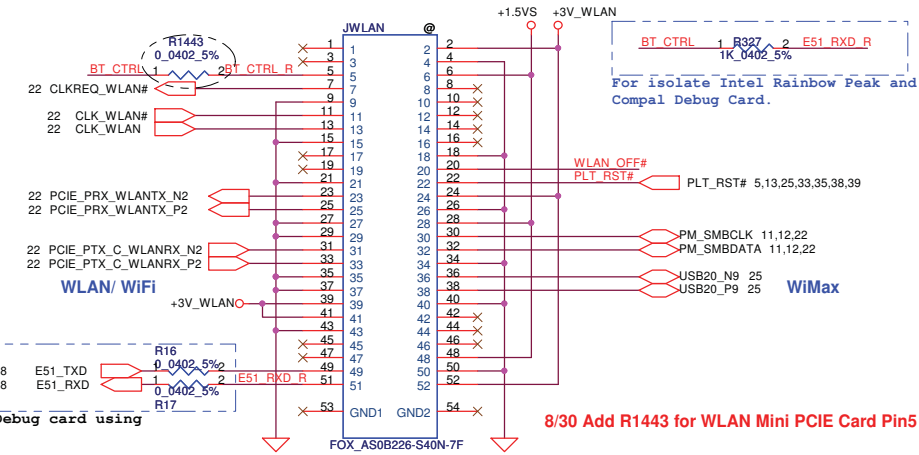
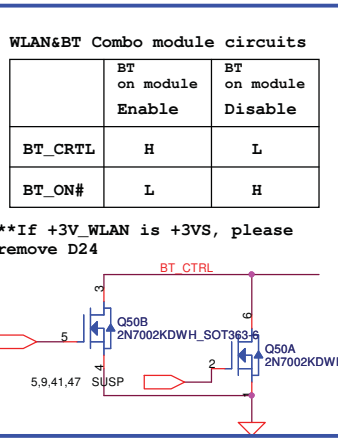
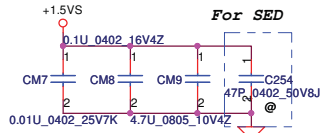
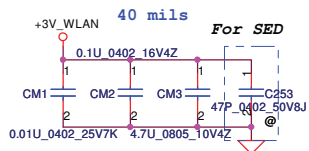
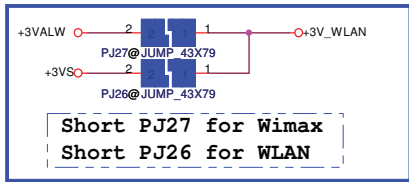
Compal Electronics, Inc.

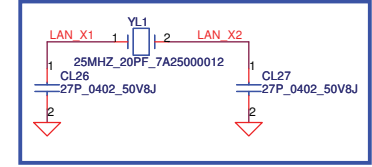
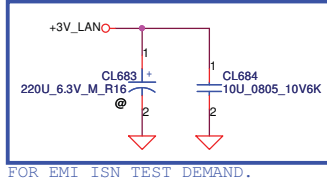
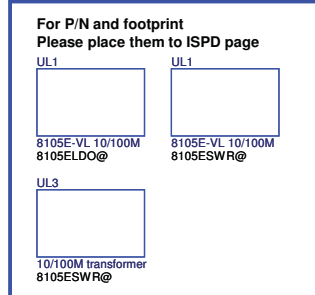
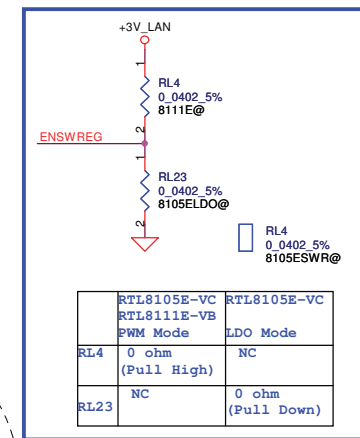
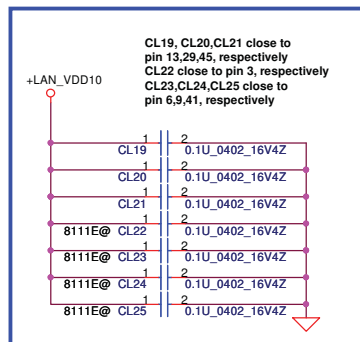
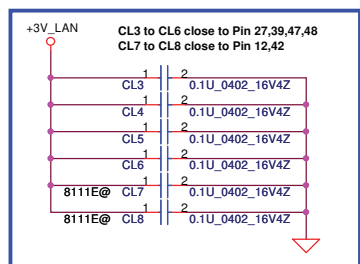
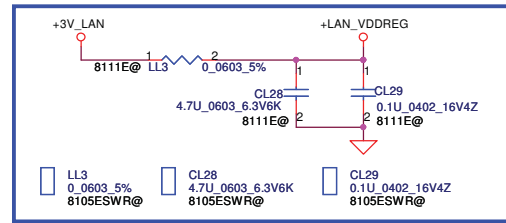
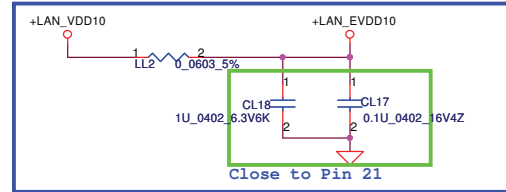
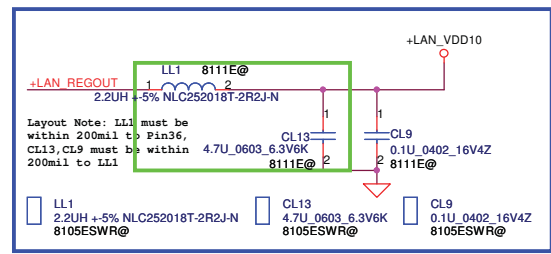
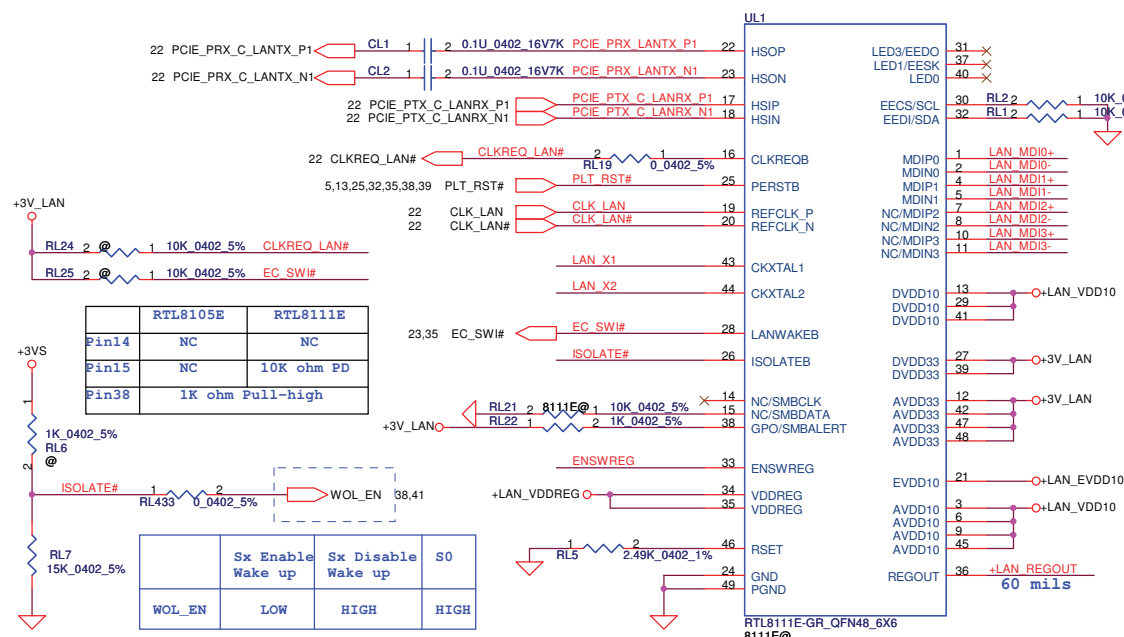
SATA-HDD/ODD/USB

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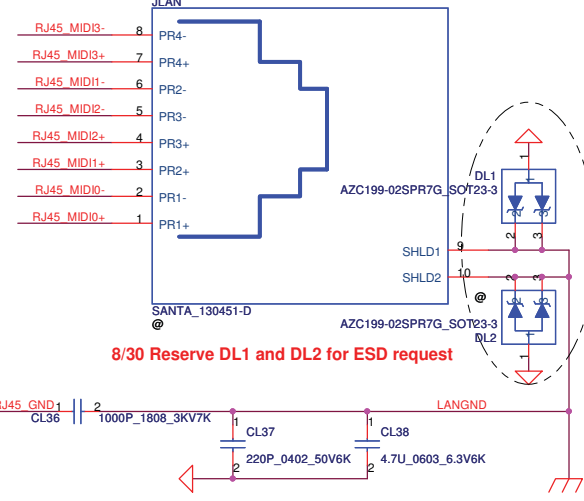
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Half PCIe Mini Card-WLAN/ WiMax





LAN Conn.

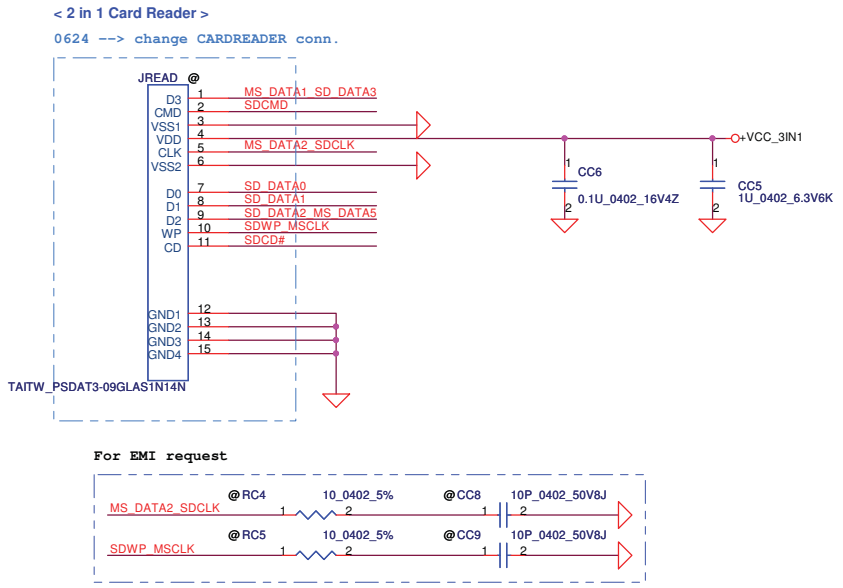
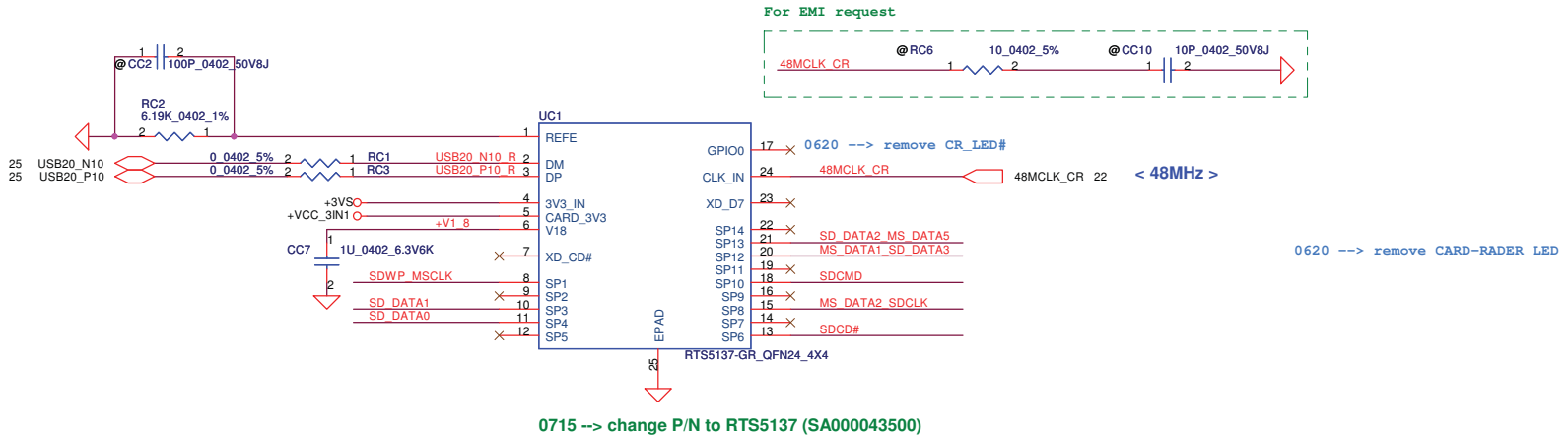


FOR EMI ISN TEST DEMAND.

8/30 Add UL3 at DVT

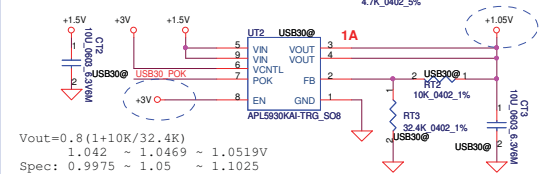
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Title PCIe-LAN-RTL8105E/8111E			
Size Custom	Document Number PWWHA LA-7201P M/B	Rev 1.0	
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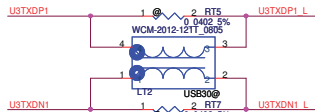
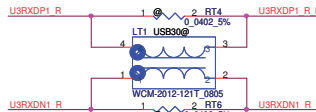
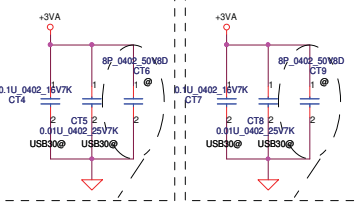


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				PWWHA LA-7201P M/B	
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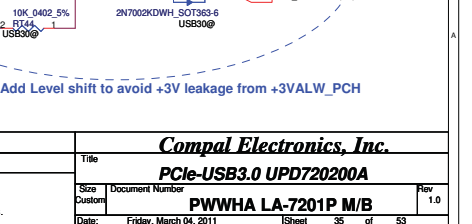
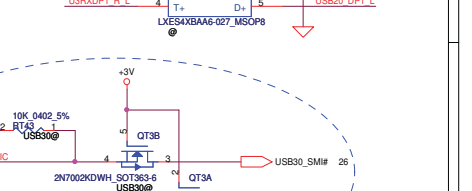
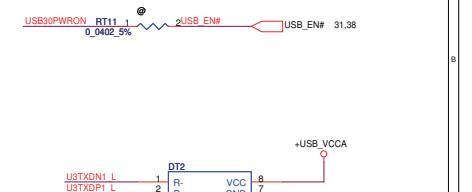
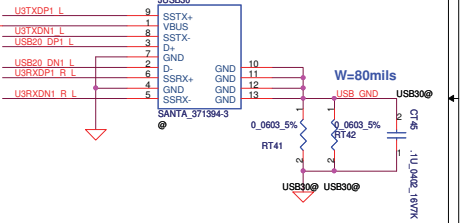
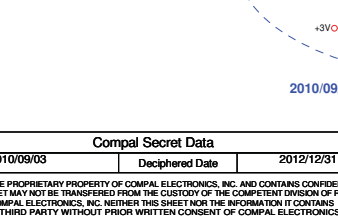
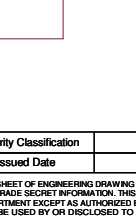
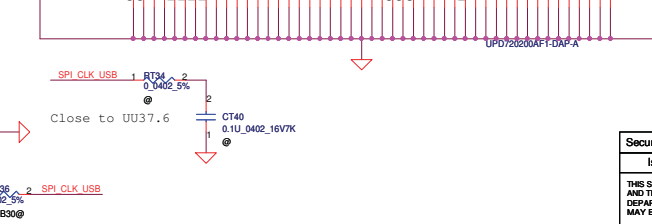
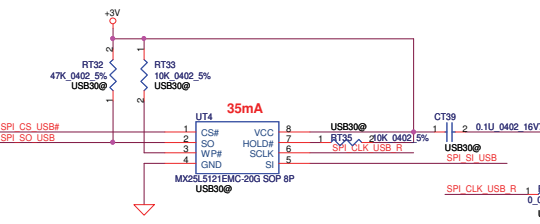
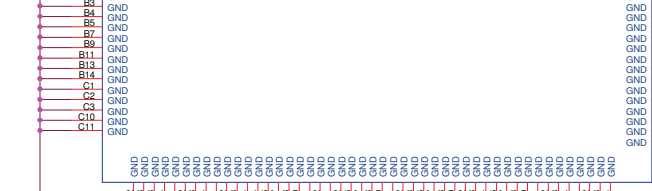
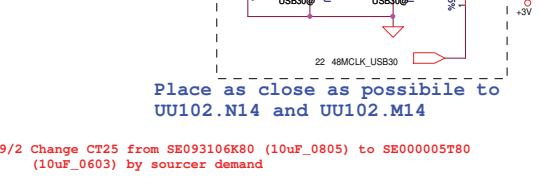
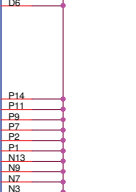
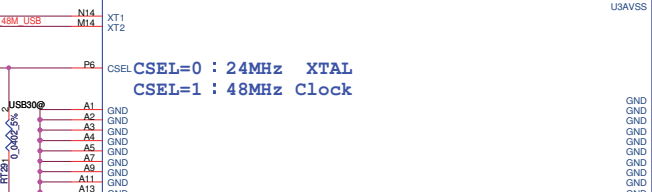
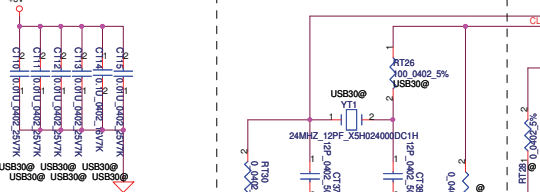
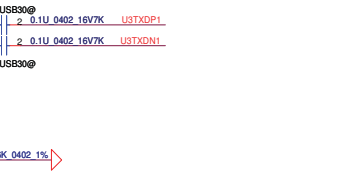
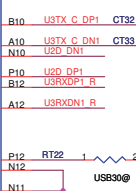
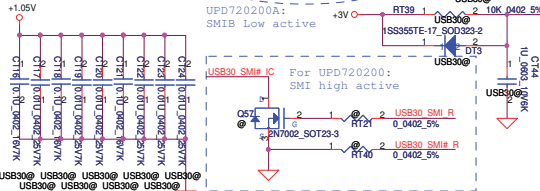
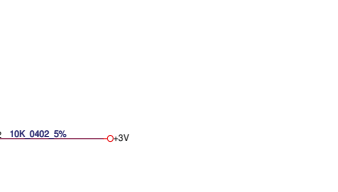
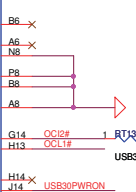
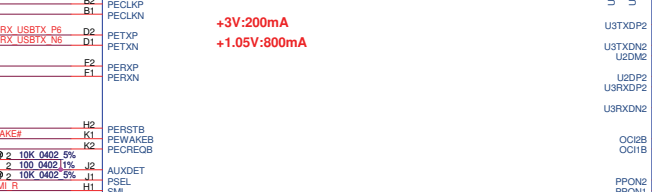
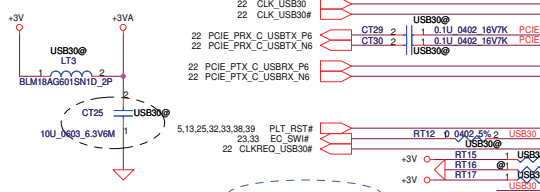
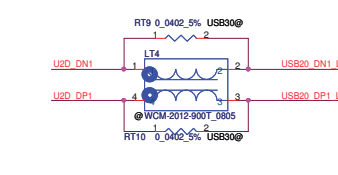
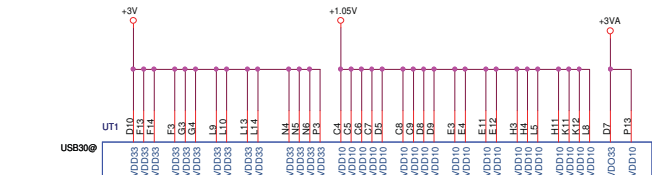
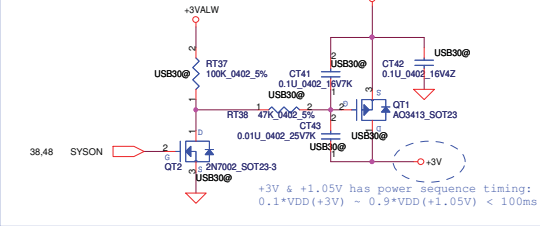
+1.5V to +1.05V Transfer



Close to U102.D7 Close to U102.P13



+3VALW to +3V Transfer

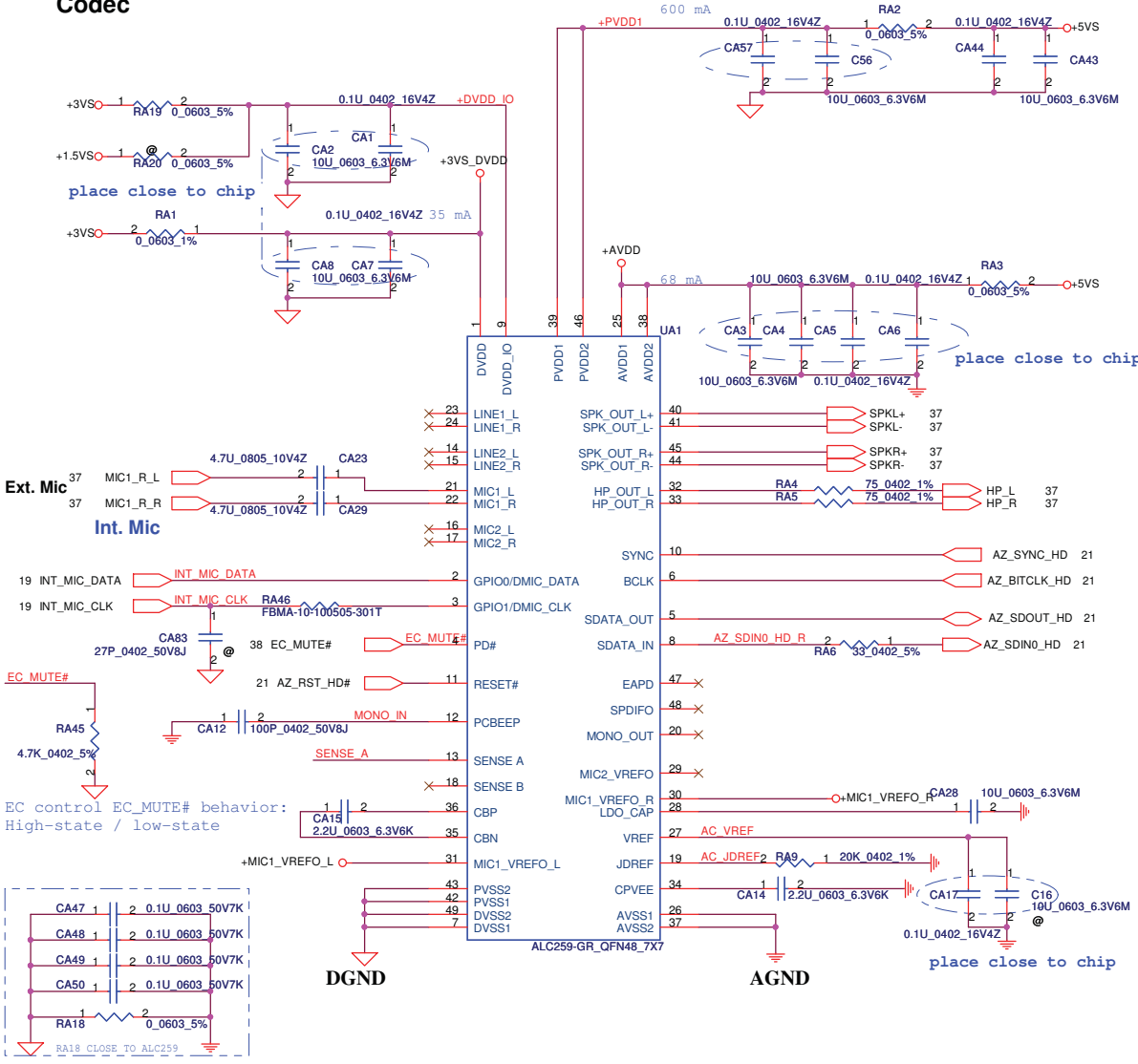


2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

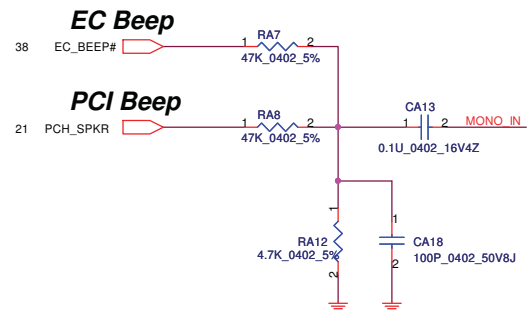
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Document Number	
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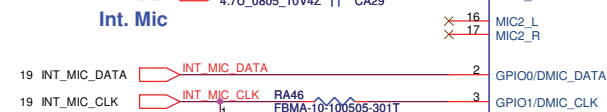
Codec



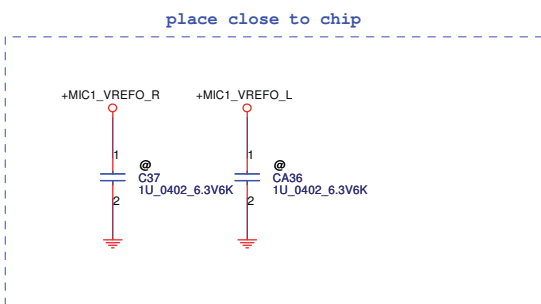
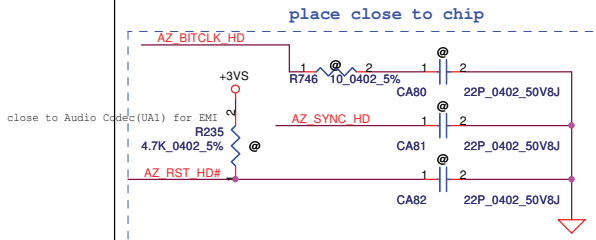
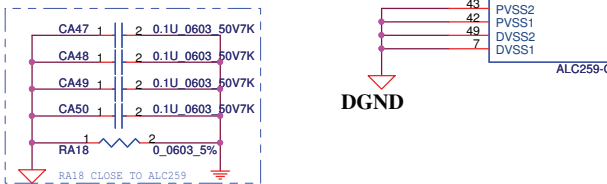
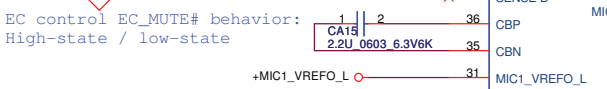
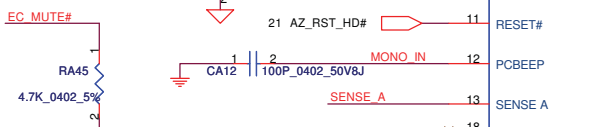
Beep sound



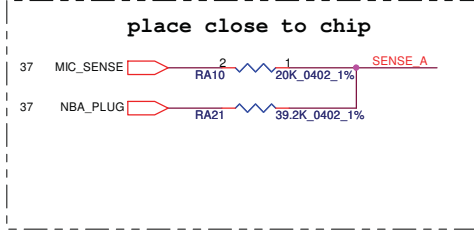
Ext. Mic



Int. Mic



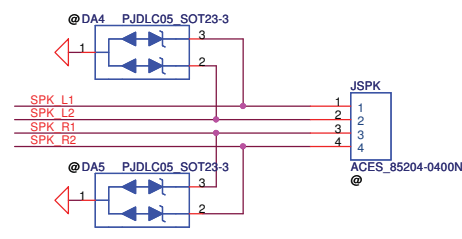
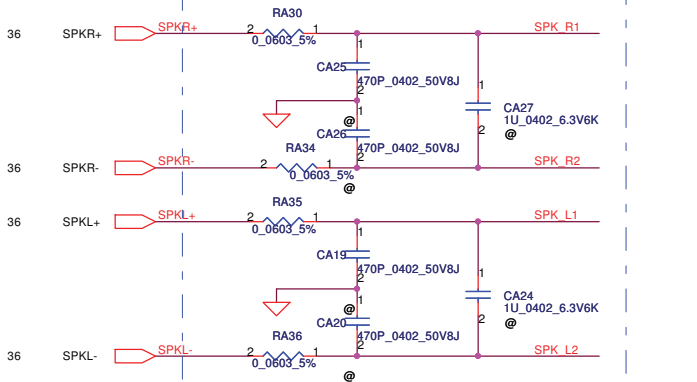
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	



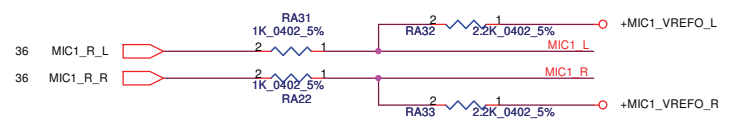
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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Speaker Connector

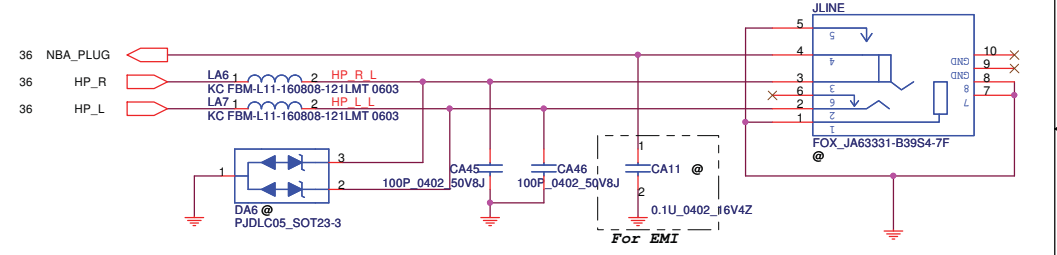
placement near Audio Codec UA1



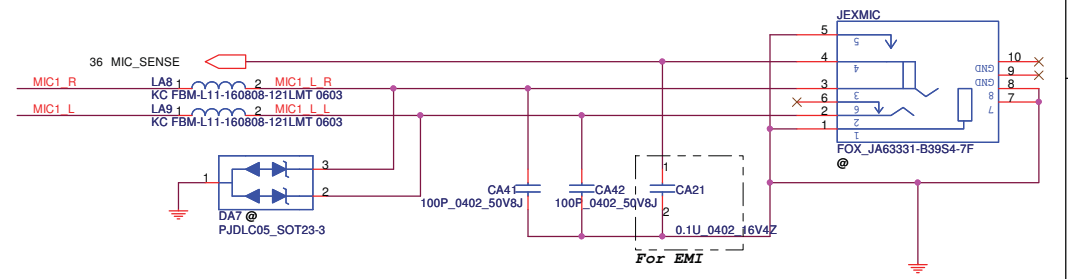
Ext. Mic



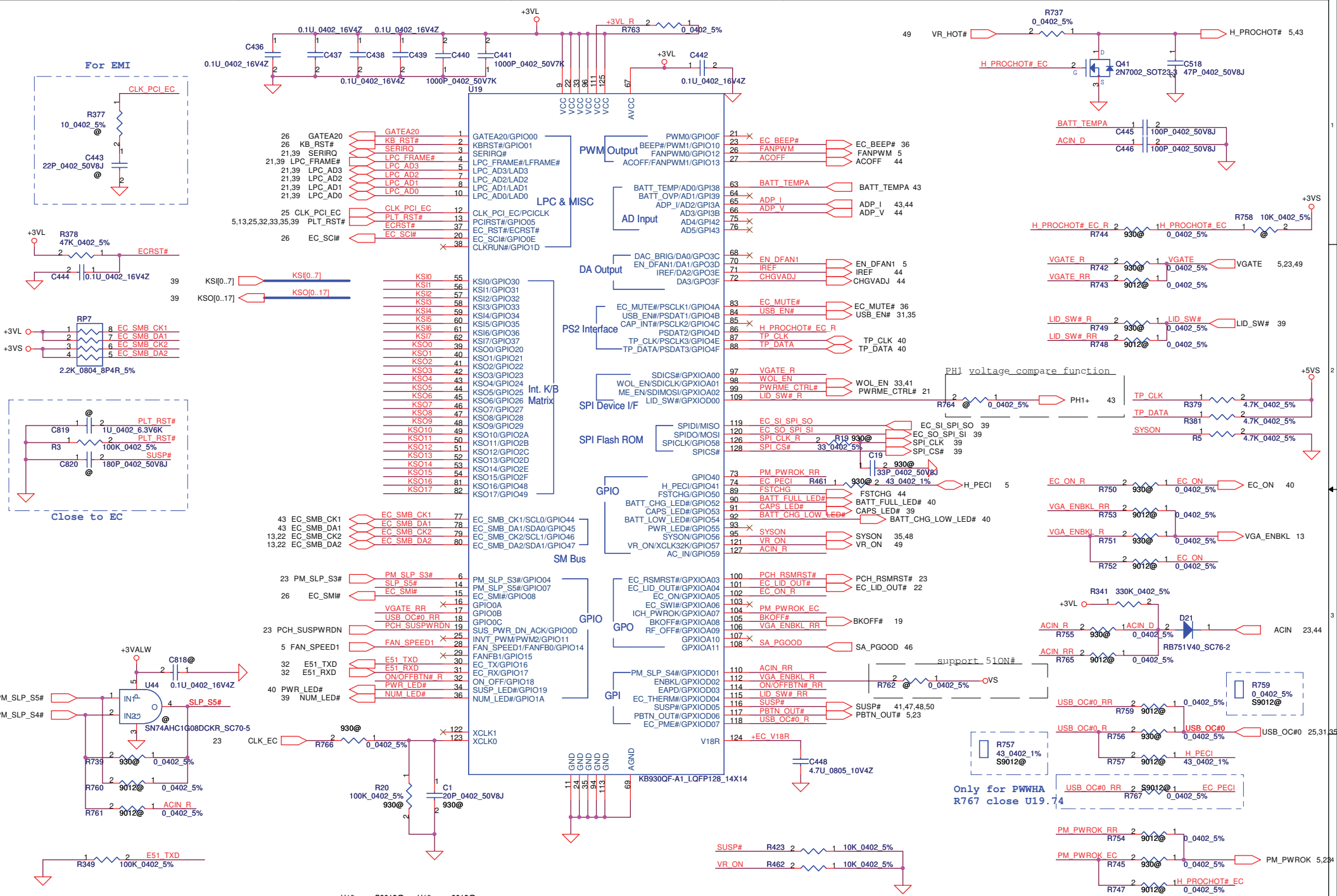
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



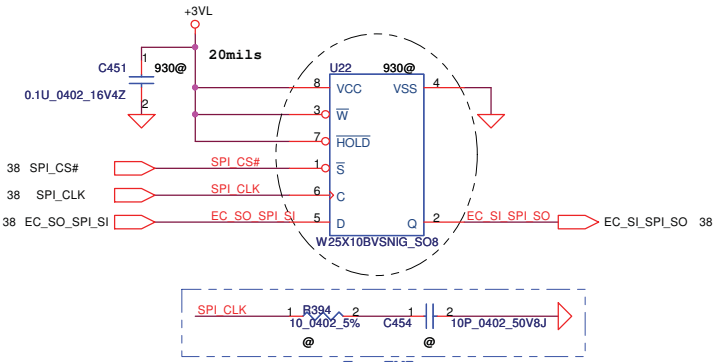
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	AUDIO AMP/MIC/SPK/VR	
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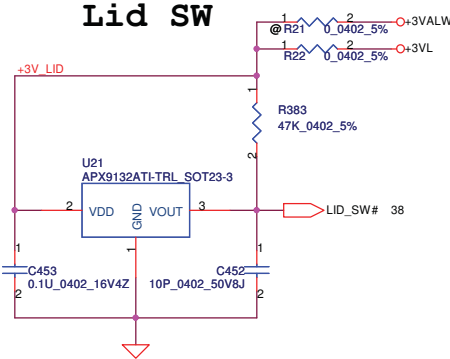
Compal Electronics, Inc.			
LPC-EC-KB930			
PWWHA LA-7201P M/B			
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SPI Flash (256KB)



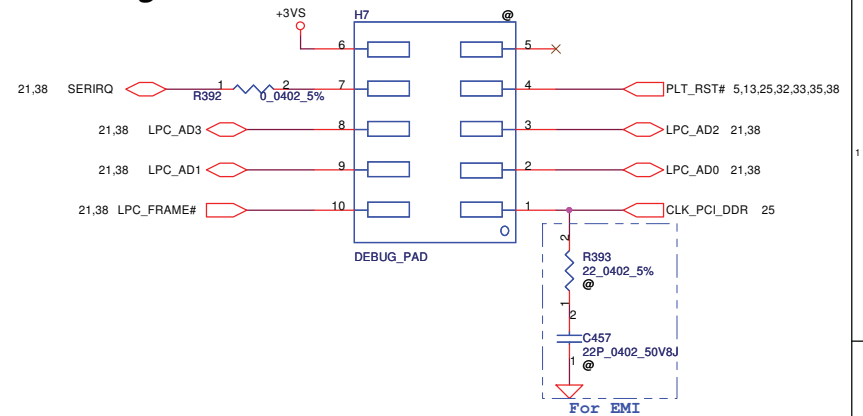
8/30 Change U22 From SA00003GK00 to SA00003GM10 due to EOL of SA00003GK00
 9/03 Change U22 change to SA00003FL10

Lid SW



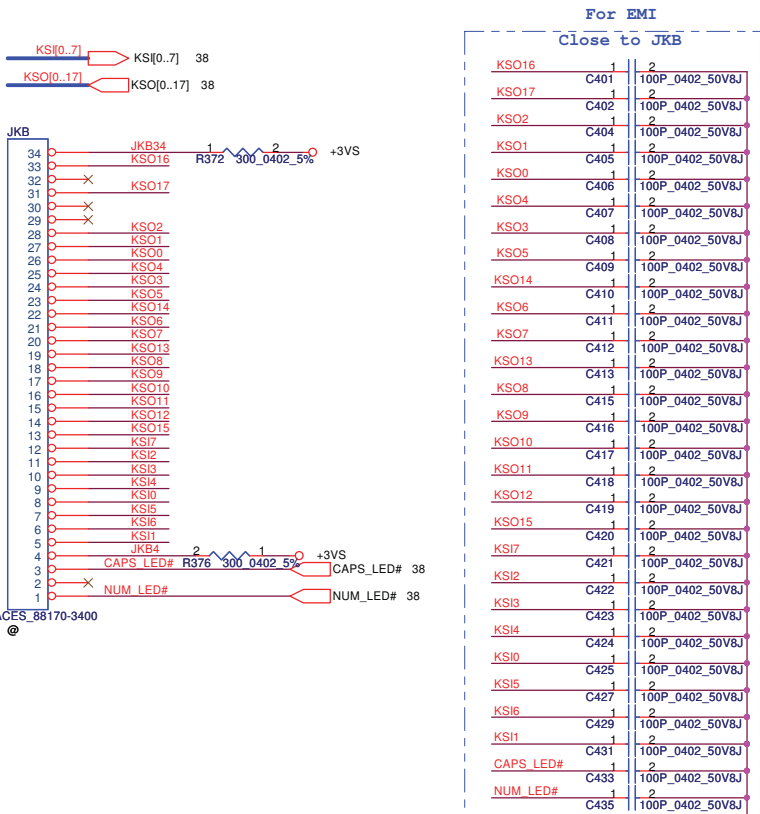
LPC Debug Port

Place the PAD under DDR DIMM.



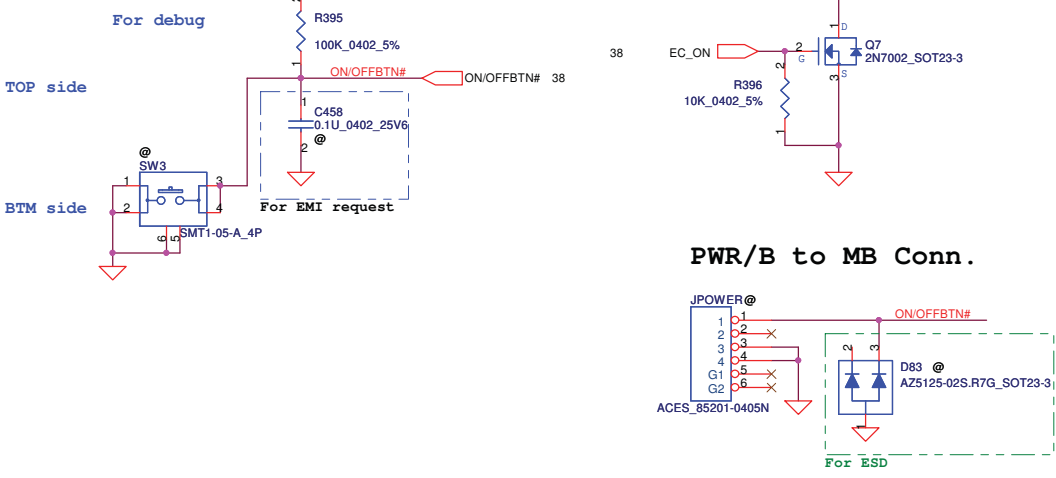
KEYBOARD CONN.

Noticed: KB Connector Pin Definition
 Reversed with KB Membrane Pin Definition

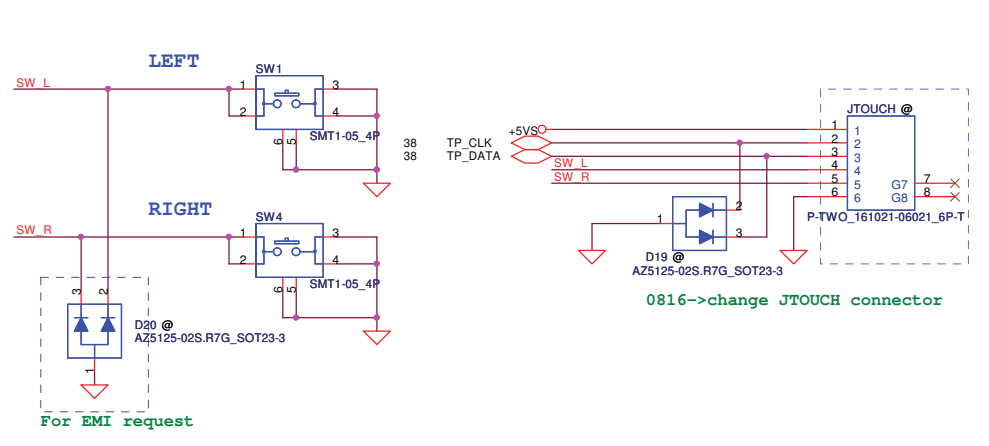


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				SPI ROM/LID/Debug/KB	
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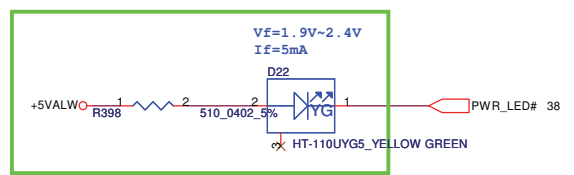
Power Button



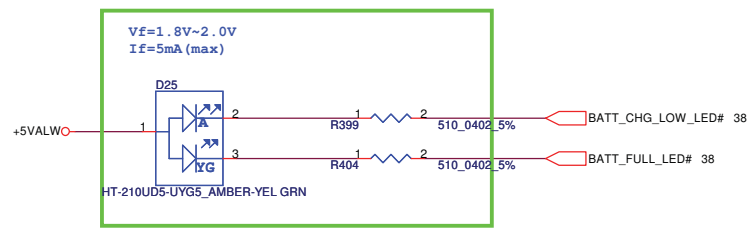
TP Button/Conn.



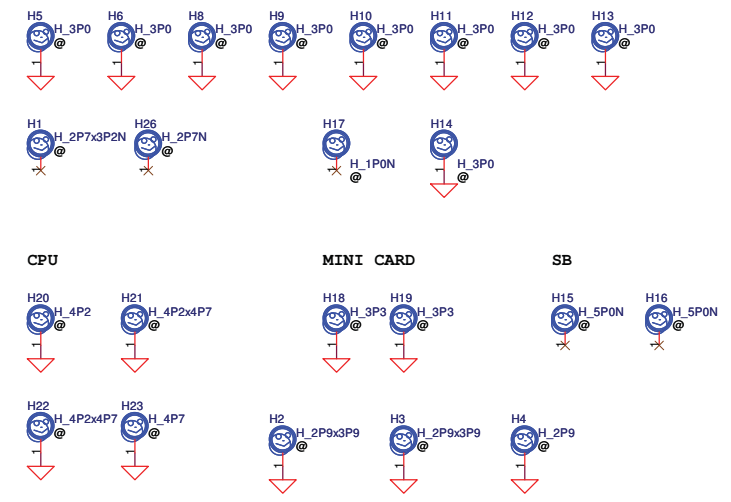
POWER/SUSPEND LED



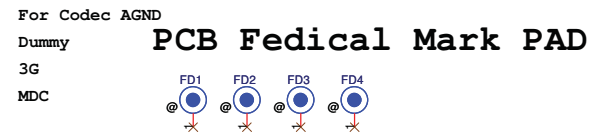
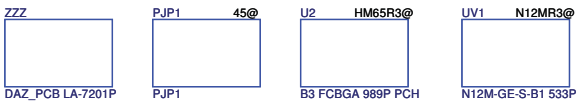
BATT CHARGE/FULL LED



Screw Hole



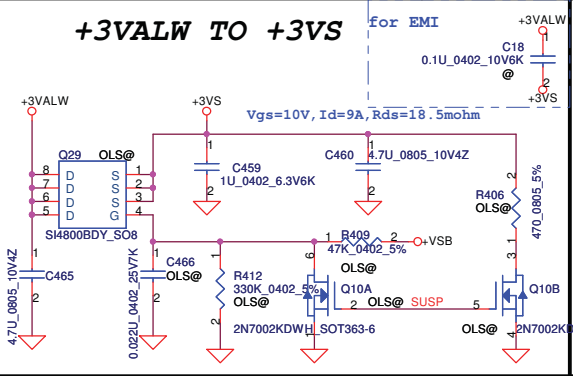
ISPD



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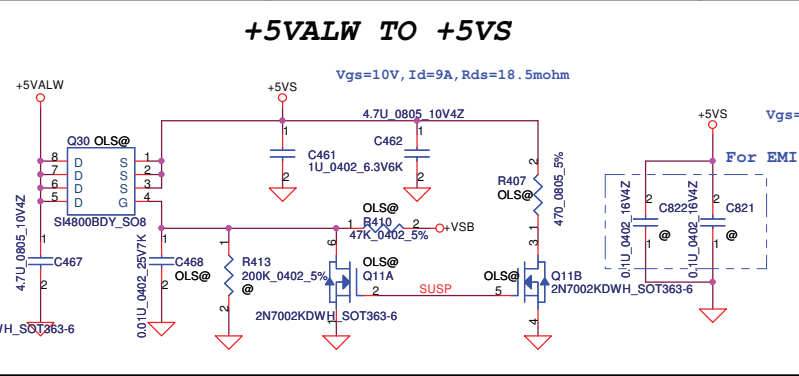
+3VALW TO +3VS

for EMI



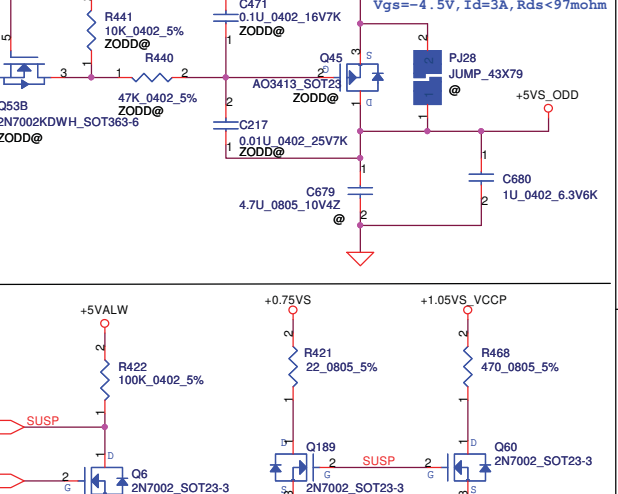
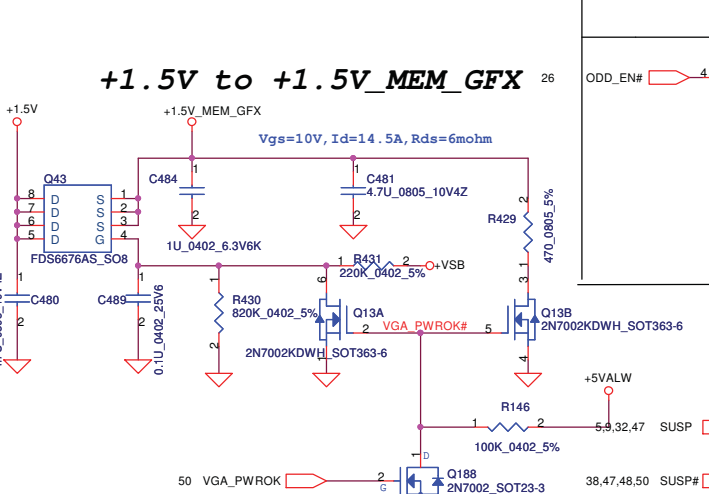
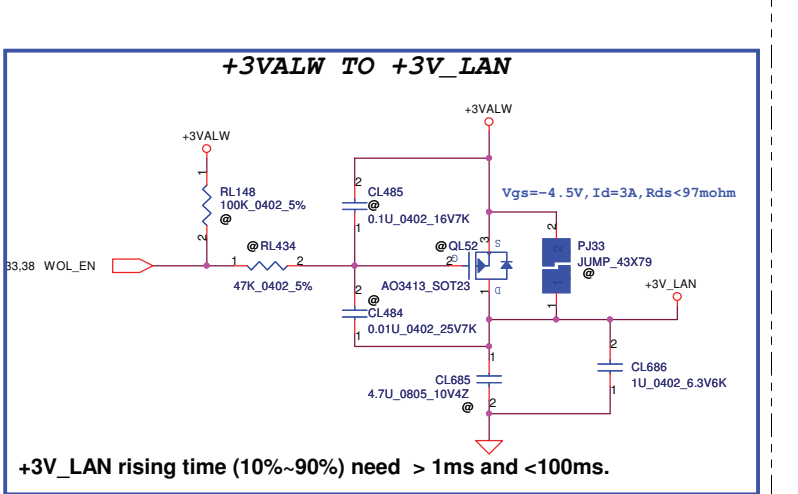
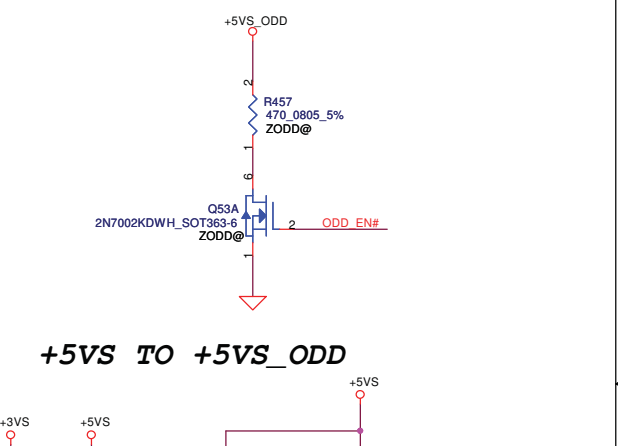
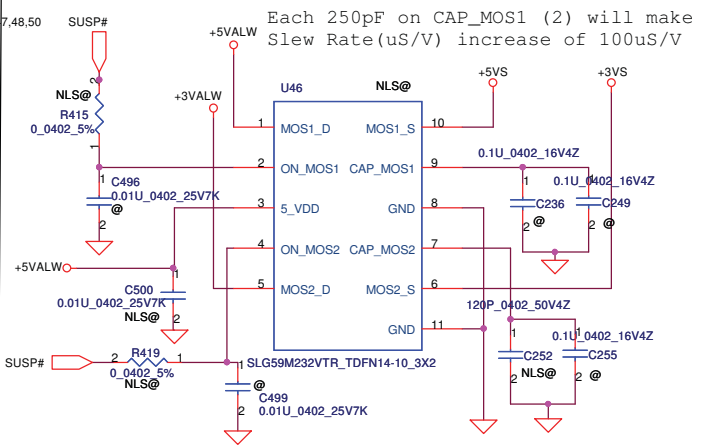
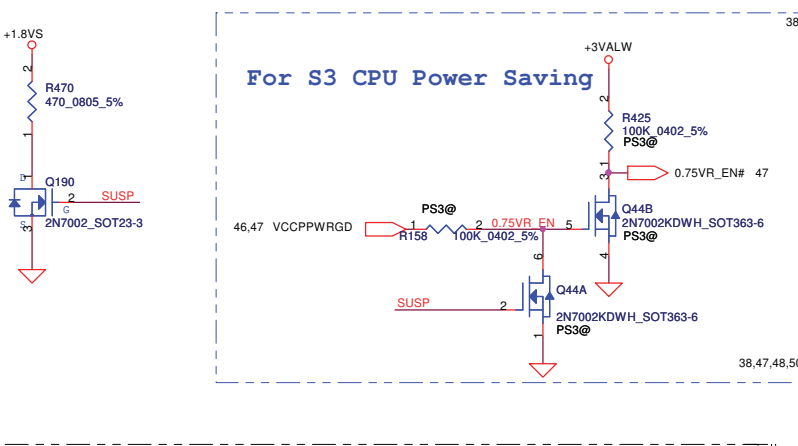
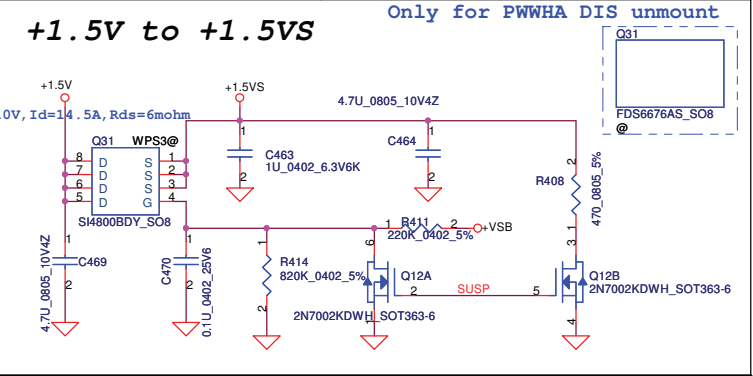
+5VALW TO +5VS

Vgs=10V, Id=9A, Rds=18.5mohm

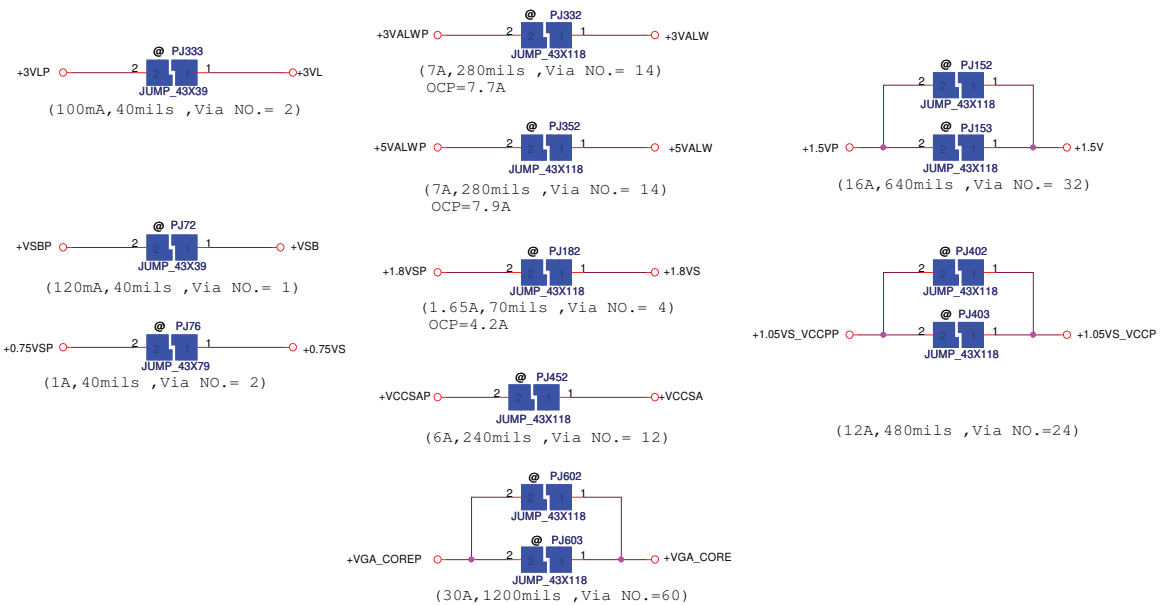
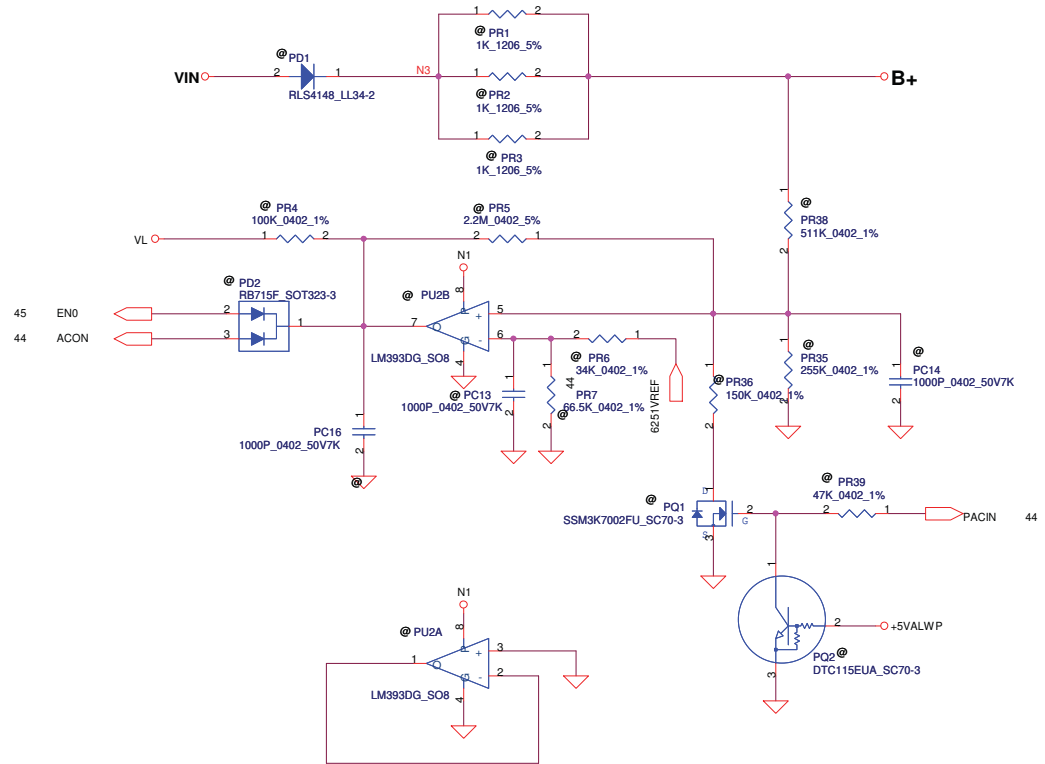
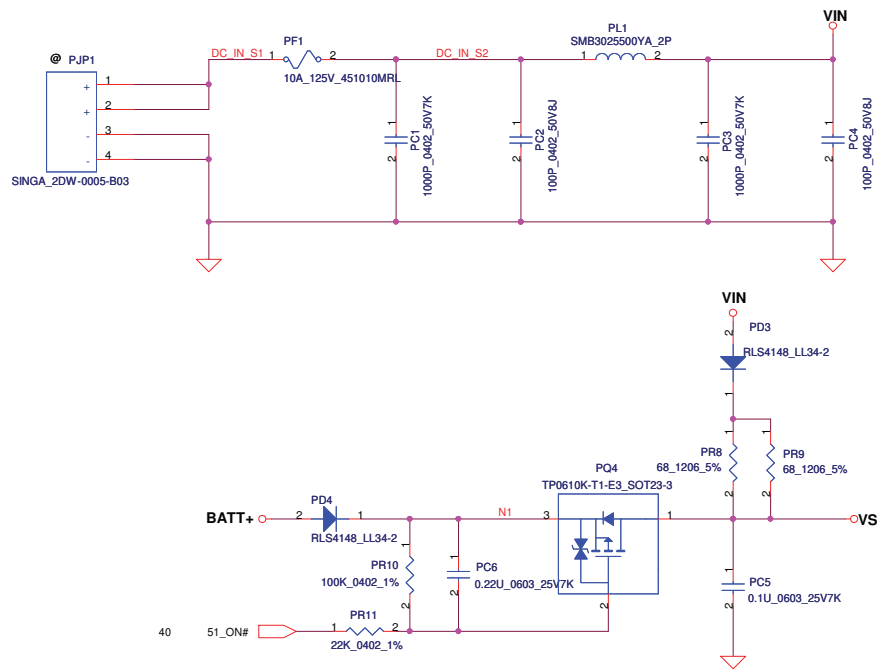


+1.5V to +1.5VS

Only for PWWHA DIS unmount

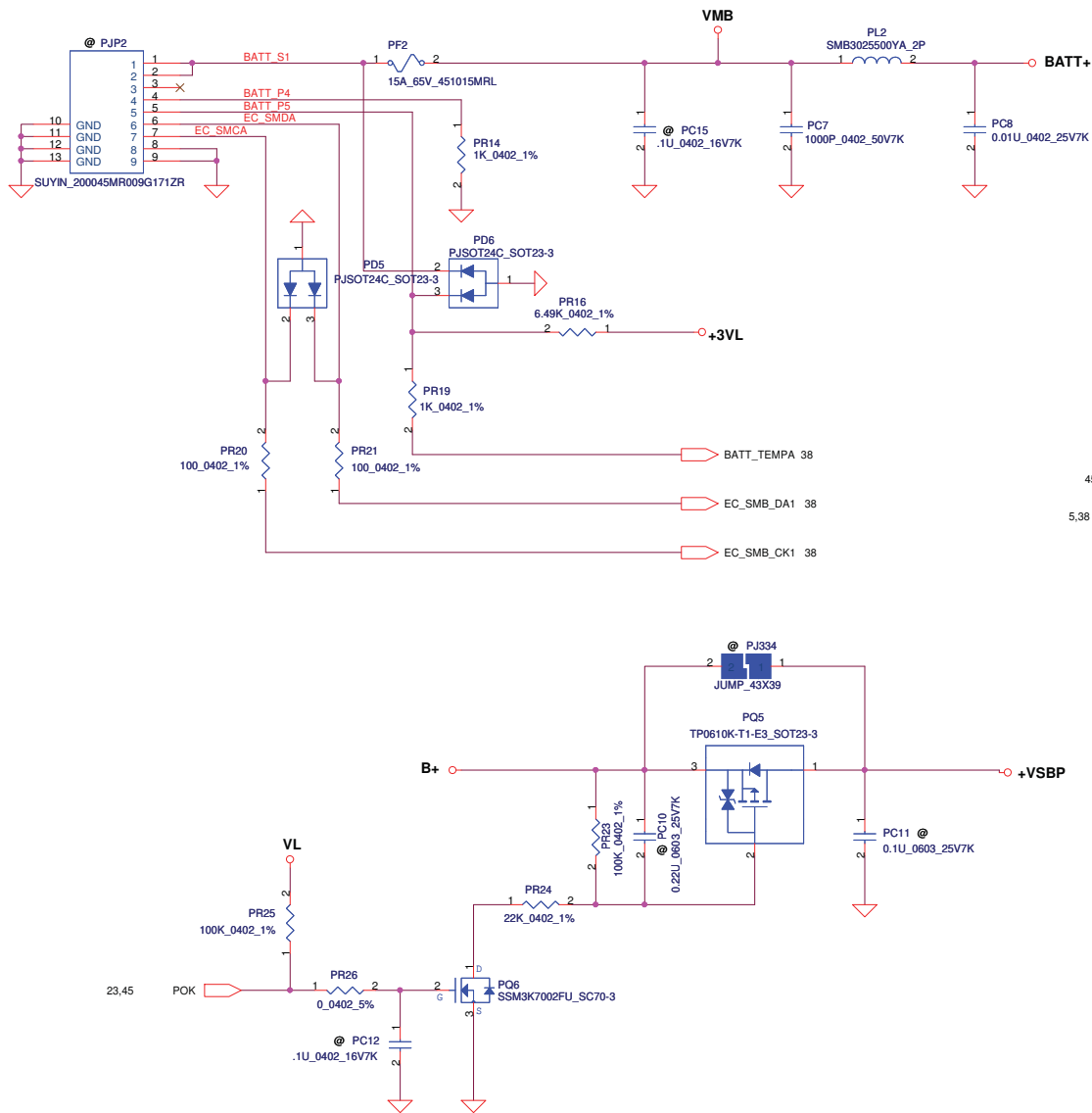


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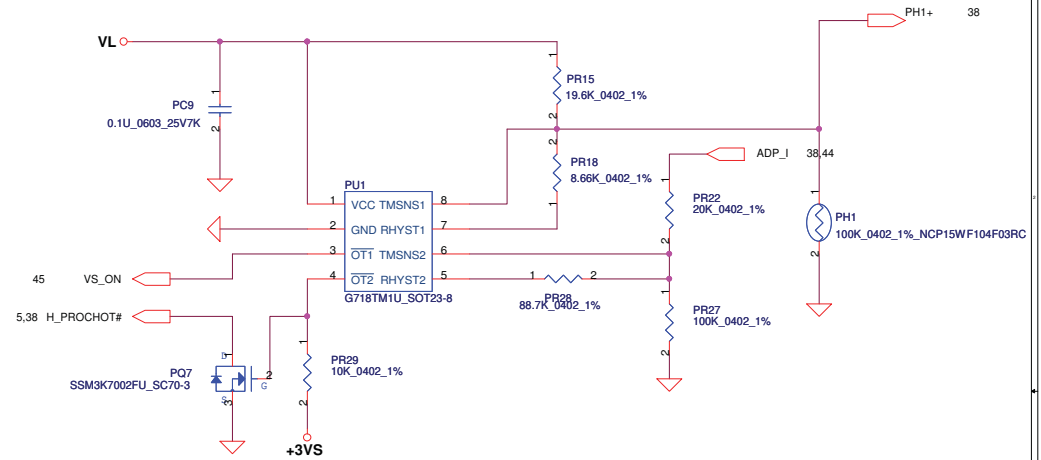


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.42V	14.74V	15.23V
L->H	15.39V	15.88V	16.39V

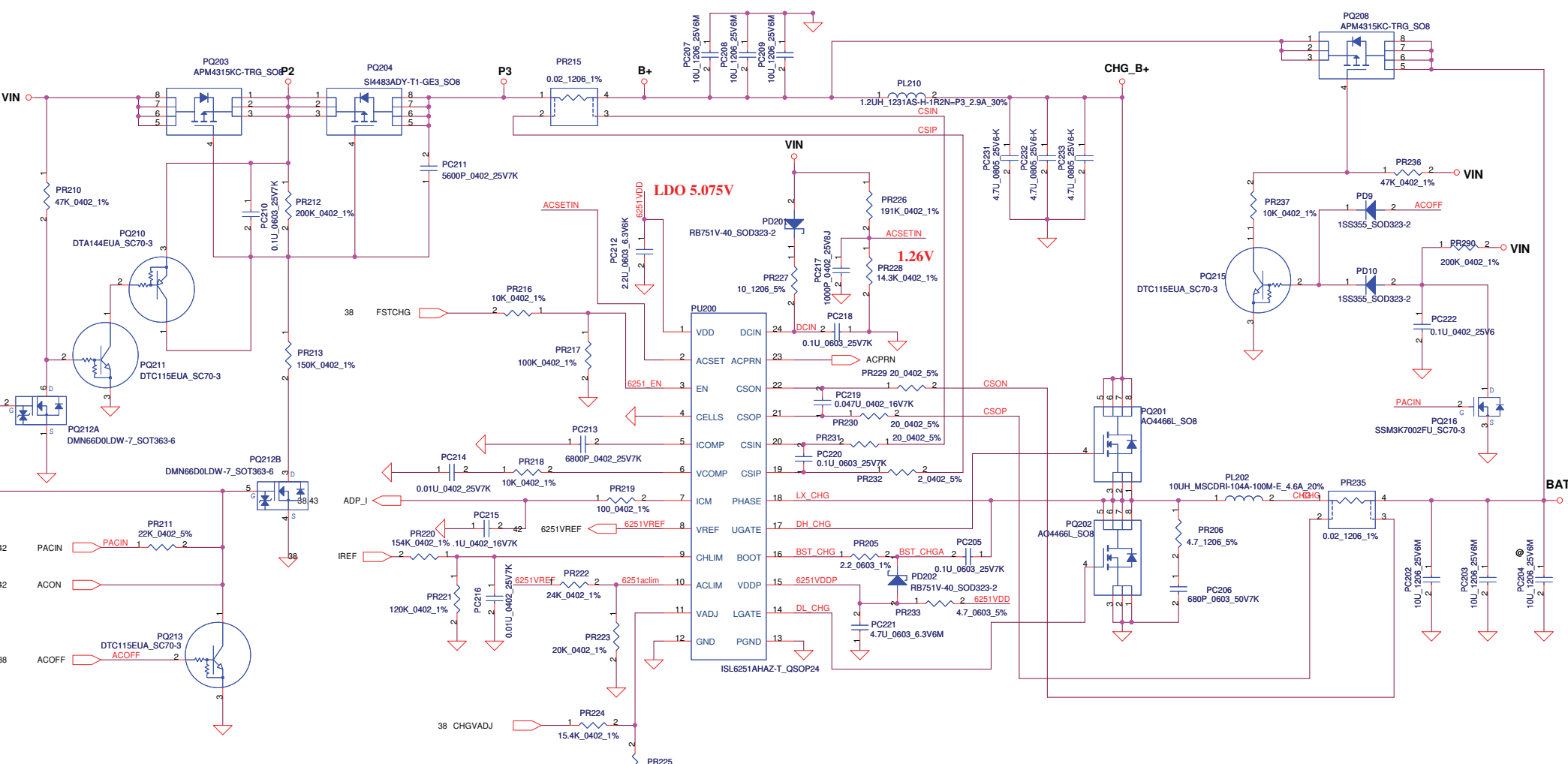
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PH1 under CPU bottom side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C



Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V



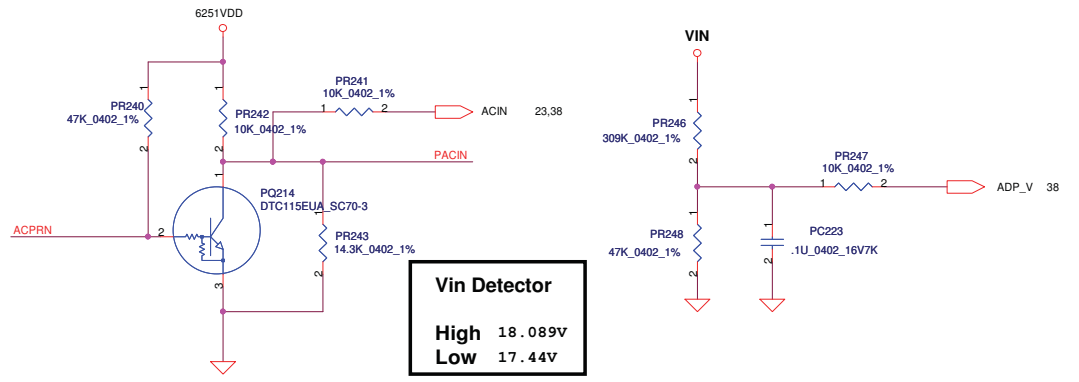
CC=0.25A~3A
 IREF=1.016*Icharge
 IREF=0.254V~3.048V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode

Iada=0~3.42A (65W)	CP= 92%*Iada; CP=3.147A
Vaclim=1.08V (65W)	PR222=75k PR223=20k PR215=0.02
Iada=0~3.947A (75W)	CP= 92%*Iada; CP=3.63A
Vaclim=0.736V (75W)	PR222=24k PR223=20k PR215=0.02

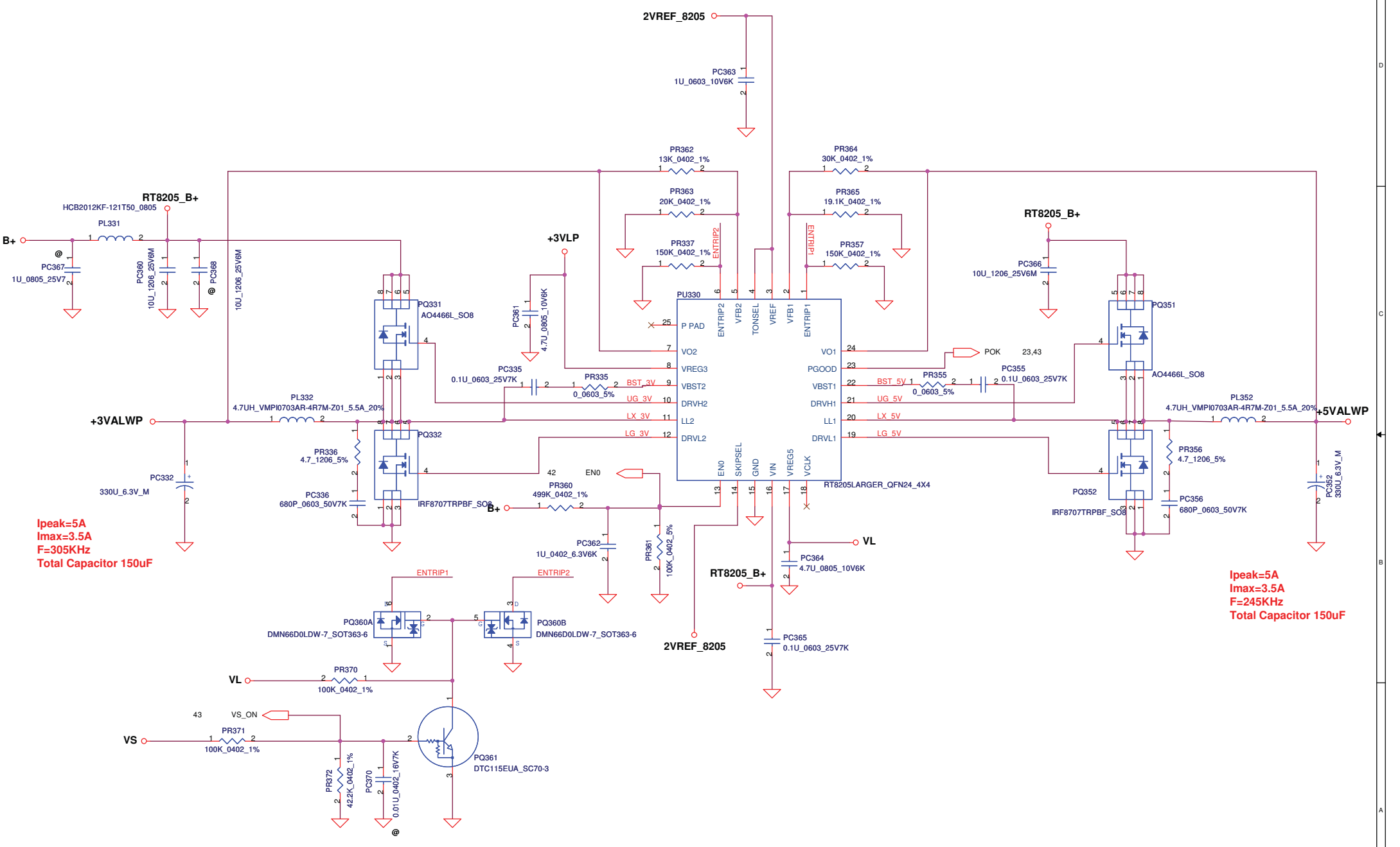


Vin Detector
 High 18.089V
 Low 17.44V

$1.26 / 14.3 * 205.3 = 18.089V$

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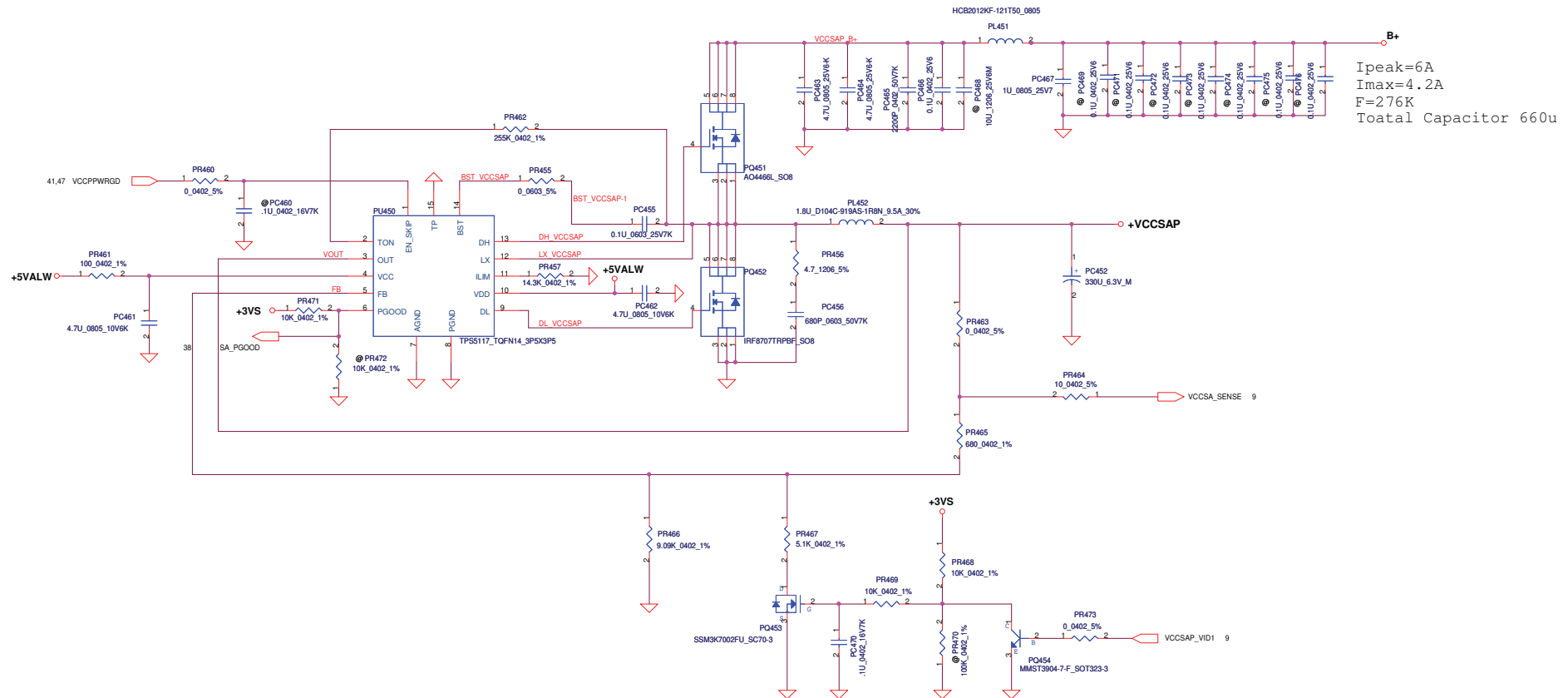
Compal Electronics, Inc.			
Title CHARGER			
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I_{peak}=5A
I_{max}=3.5A
F=305KHz
Total Capacitor 150uF

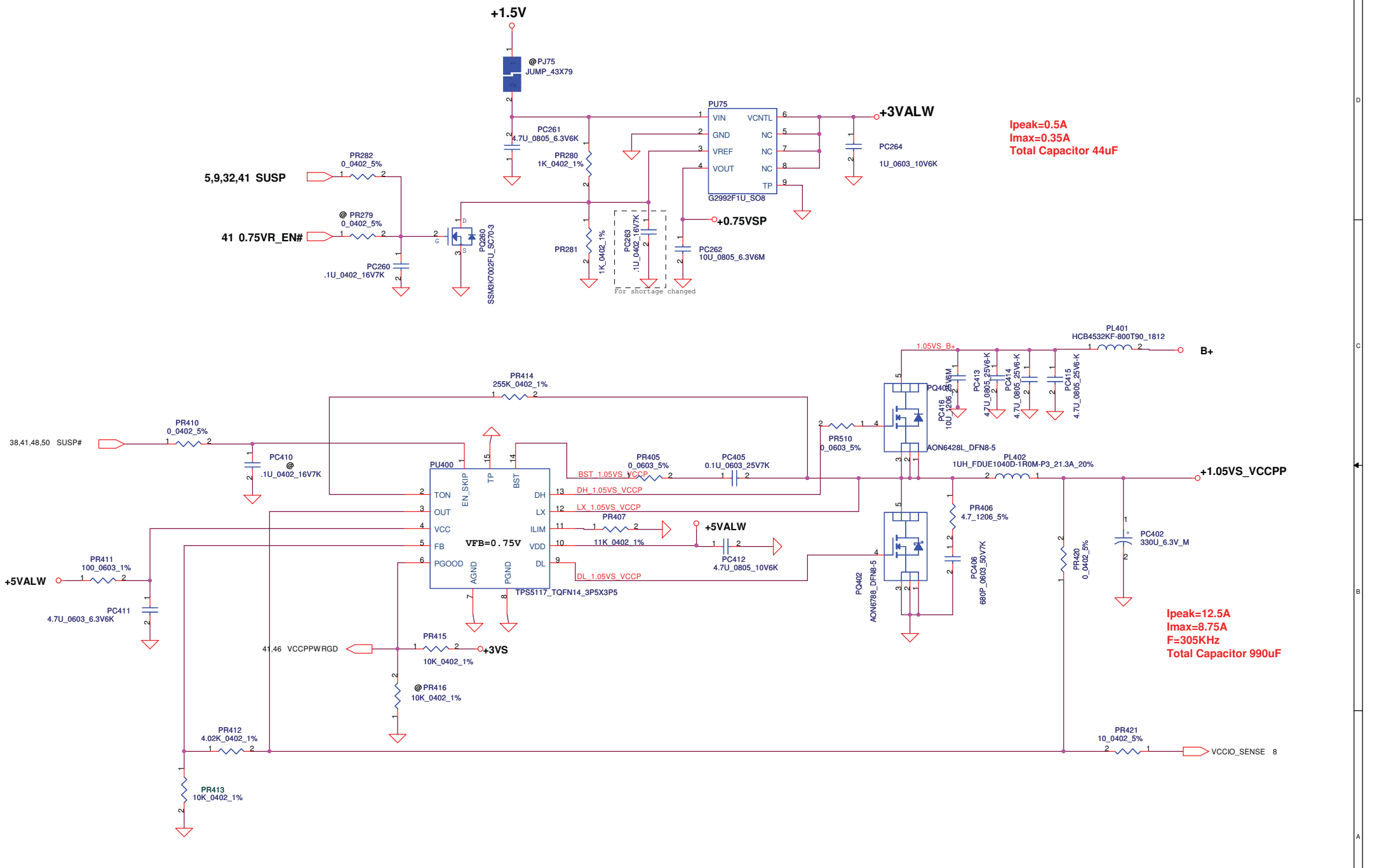
I_{peak}=5A
I_{max}=3.5A
F=245KHz
Total Capacitor 150uF

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I_{peak}=6A
 I_{max}=4.2A
 F=276K
 Total Capacitor 660u

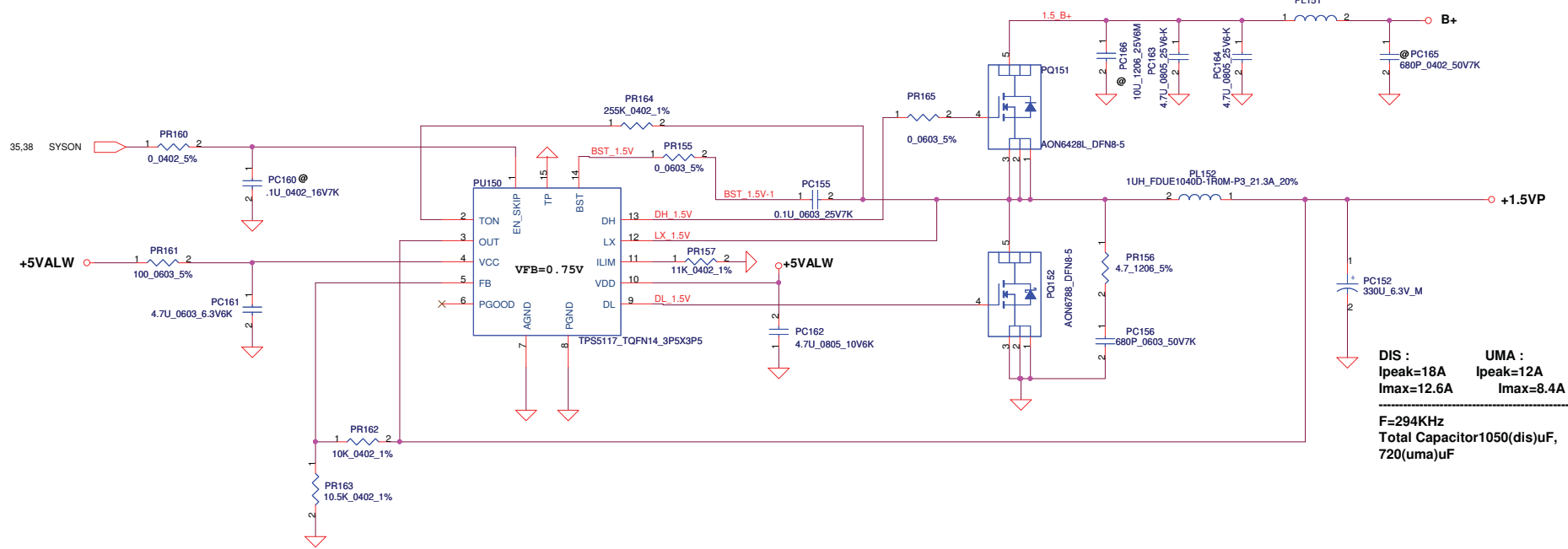
VID1	+VCCSAP
1	0.8V
0	0.9V



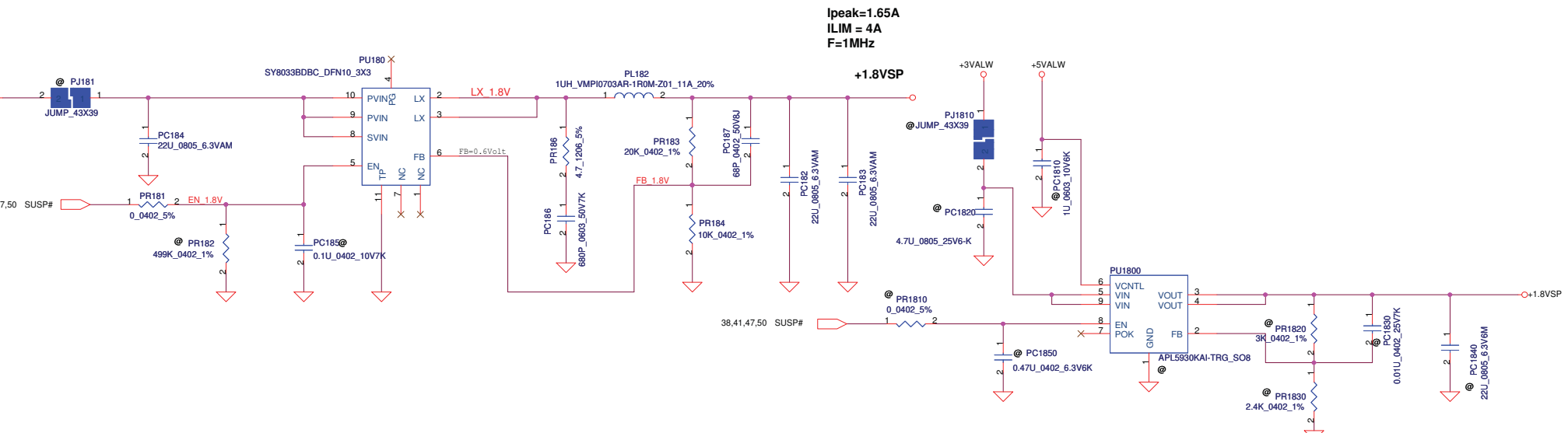
I_{peak}=0.5A
 I_{max}=0.35A
 Total Capacitor 44uF

I_{peak}=12.5A
 I_{max}=8.75A
 F=305KHz
 Total Capacitor 990uF

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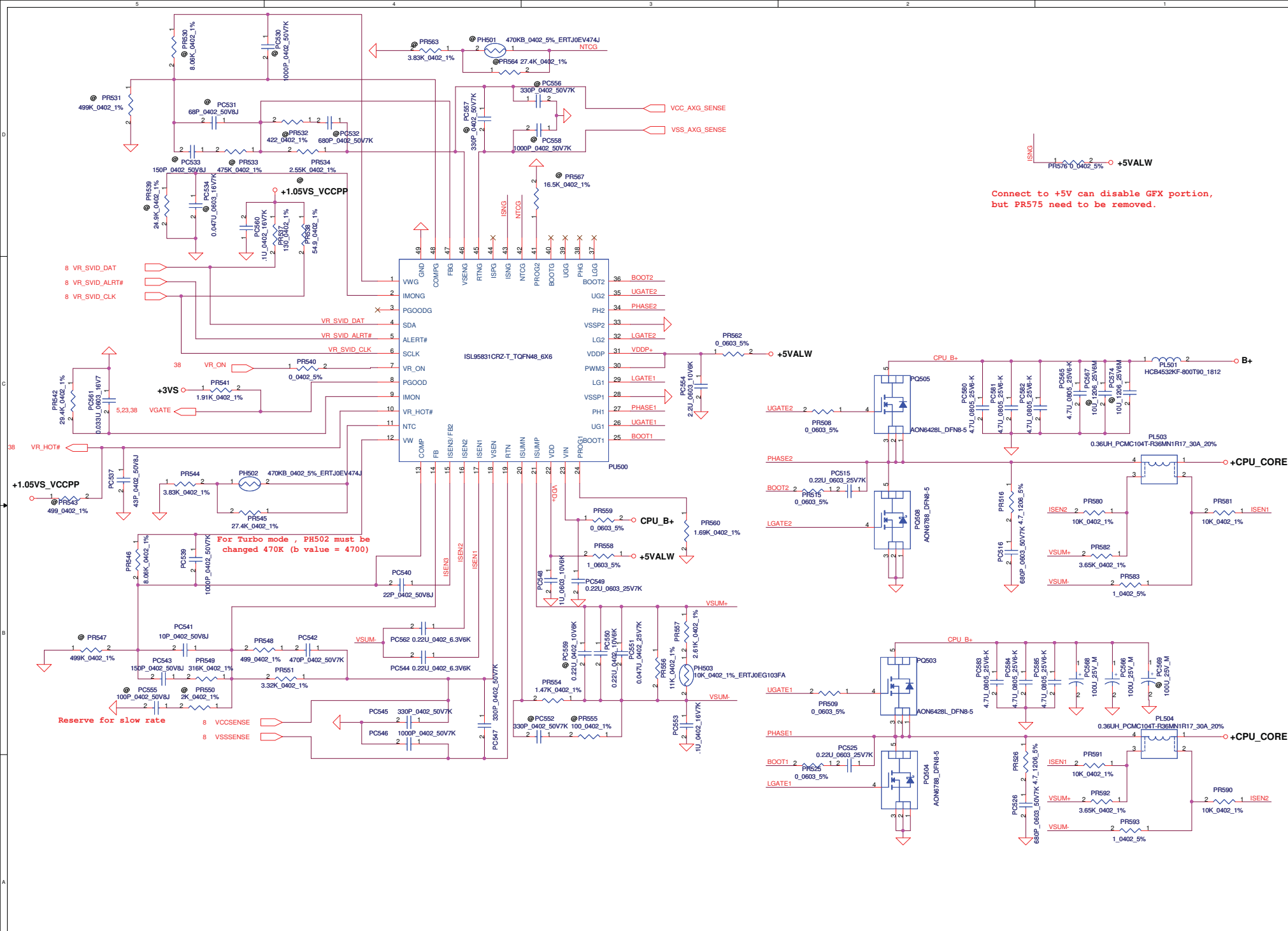


DIS : Ipeak=18A
UMA : Ipeak=12A
 Imax=12.6A Imax=8.4A
 F=294KHz
 Total Capacitor 1050(dis)uF,
 720(uma)uF



Ipeak=1.65A
ILIM = 4A
F=1MHz

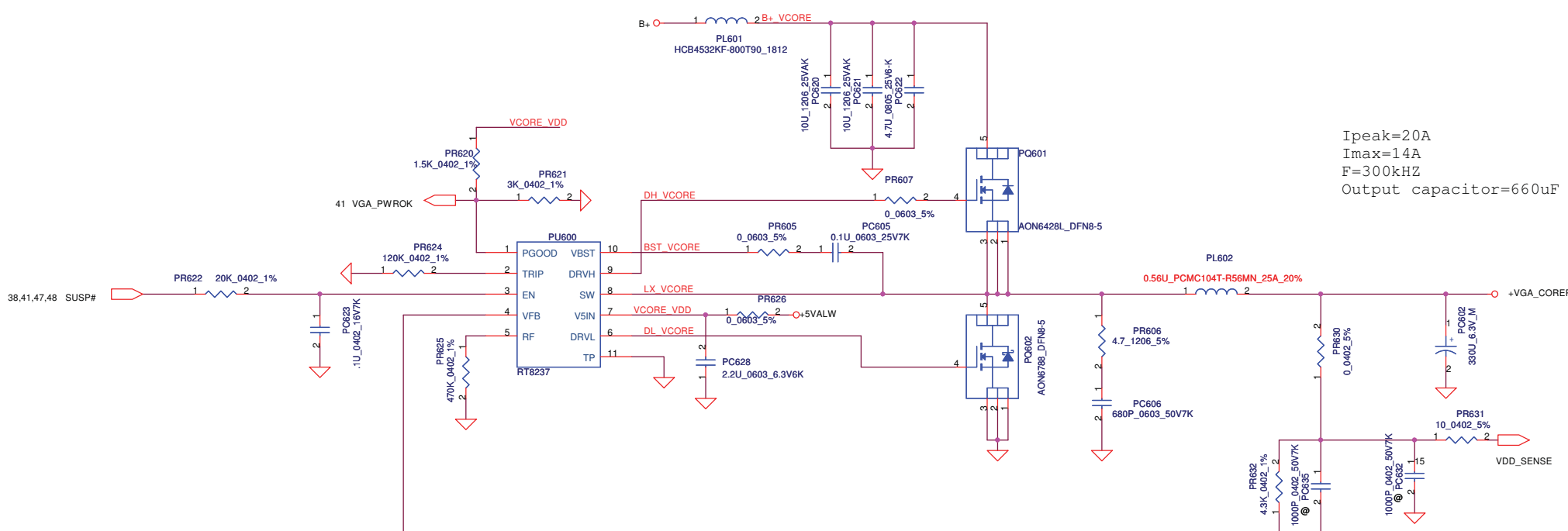
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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Connect to +5V can disable GFX portion, but PR575 need to be removed.

For Turbo mode , PH502 must be changed 470K (b value = 4700)

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Ipeak=20A
 Imax=14A
 F=300kHz
 Output capacitor=660uF

PR625 = 470Kohm => FSW = 300KHZ
 PR625 = 200Kohm => FSW = 350KHZ
 PR625 = 100Kohm => FSW = 390KHZ
 PR625 = 47Kohm => FSW = 400KHZ

$VFB(0.7) = V_{out} \cdot R_{bottom} / (R_{top} + R_{bottom})$

Pstate	GPU_VID0	GPU_VID1	N12M-GE	
P8/P12	0	x	0.85V	
P0	1	x	1V	
	0	x		
P0 (cold)	1	x	1V	
			PR632=4.3K PR633=20K PR641=20K	

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DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/12/31 (PVT)	P36	Charger add snubber PR206,PC206	EMI command
2010/12/31 (PVT)	P36	Charger change boost to 2.2 ohm PR205	EMI command
2010/12/31 (PVT)	P35	+3VALW/+5VALW add snubber PR336,PC336,PR356,PC336	EMI command
2010/12/31 (PVT)	P37	+1.5VP/+1.8VSP Change PR155,PR165 to 0 ohm	EMI command
2010/12/31 (PVT)	P37	+1.5VP/+1.8VSP Change PQ151 to POK 5*6	EMI command
2010/12/31 (PVT)	P37	+1.5VP/+1.8VSP Reserve snubber PR156,PC156	EMI command
2010/12/31 (PVT)	P37	+1.5VP/+1.8VSP add PC165 for MEI	EMI command
2010/12/31 (PVT)	P37	+VCCSA add snubber PR456,PC456	EMI command
2010/12/31 (PVT)	P38	+1.05VS/+0.75 change PRQ401 to POK 5x6	EMI command
2010/12/31 (PVT)	P38	+1.05VS/+0.75 change PR405,PR510 to 0 ohm	EMI command
2010/12/31 (PVT)	P38	+1.05VS/+0.75 change 0.75V enable PR279 tp PR282	HW command
2010/12/31 (PVT)	P39	+CPU_CORE change PC549,PC515,PC525 to correct rating	design change
2010/12/31 (PVT)	P39	+CPU_CORE change PL503,PL504 to DCR 5%	design change
2010/12/31 (PVT)	P39	+CPU_CORE change PC568 PC 566 to 5.8mmm capacitor	design change
2010/12/31 (PVT)	P39	+CPU_CORE change PC551 for load line adjust	design change
2010/12/31 (PVT)	P39	+CPU_CORE change PR560 for program temperture	design change
2010/12/31 (PVT)	P39	+CPU_CORE change PC505,PQ503 change to POK5X6	design change
2010/12/31 (PVT)	P40	+VGA_CORE change PU600 to RT8237	design change
2010/12/31 (PVT)	P40	+VGA_CORE change PR605,PR607 to 0ohm	design change
2010/12/31 (PVT)	P40	+VGA_CORE change PR601 to POK 5X6	EMI command
2010/12/31 (PVT)	P40	+VGA_CORE change VID0 and VID1 compont chage	design change

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				Power PIR		
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HW PIR (Product Improve Record)

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2010/10/29

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	10/29	17	SWAP FBA_CMD2 and FBA_CMD11	Schematic error
2	10/29	18	SWAP FBA_CMD18 and FBA_CMD11	Schematic error
3	10/29	21	Chane +3V_SPI to +3VS	Schematic error
4	10/29	22	Add R23 for CLK_REQ_VGA#	Reserve pull down for clock request

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2010/11/11

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	11/03	25,31	Add USB20_N9 & USB20_P9	Support Wimax
2	11/03	32	Co-Lay Giga LAN	Giga LAN support
3	11/22	22	Add R584 & R564 for Panel select	For HW common design
4	11/22	5	change D86 (SC100001M00)	For HW common design
5	11/22	5	cancel D85 @	For HW common design
6	11/24	32	LAN 8105E-VC update to 8105E-VL	For HW common design

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.4 TO 0.6

GERBER-OUT DATE: 2011/01/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	01/15	14	Change RV48 BOM structure from @ to HDMI@.	For HDMI function
2	01/15	15	Add net name +IFPE_IOVDD & +IFPE_PLLVDD	For HDMI function
3	01/15	15	Add LV12, CV160, CV169, CV170, CV173, LV8, CV178, CV159, CV176, CV182, CV215	For HDMI function
4	01/15	38	Add U19 BOM symbol for 9012	For EC 9012
5	01/15	19	Change R120 from 10Kohm to 47Kohm.	For backlight PWM issue
6	01/15	35	Change UT2.6 & RT1 connector from +5VALW to +3V and del CT1.	For LDO leakage issue
7	01/15	41	Add Q31 BOM symbol and add BOM structure PS3@.	For power saving function
8	01/16	13	Change R25 BOM structure from @ to NHDMI@.	For HDMI function
9	01/16	38	Delete U19.123 CLK_EC_R net name	Due to duplicate net name
10	01/16	38	Change U19.104 & R745.2 & R747.2 net name from PM_PWROK_R to PM_PWROK_EC.	Due to duplicate net name
11	01/18	38	Add R757 & R759 & U19 BOM symbol and add BOM structure S9012@	For EC9012 solution
12	01/18	38	Add R767 and BOM structure S9012@	For EC9012 solution
13	01/19	21~29	Change U2 P/N from SA00003P440 to SA00004EE80.	For PCH P/N update
14	01/19	21~29	Change U2 BOM structure from Q65R3@ to HM65R1@.	For BOM structure update
15	01/19	40	Add U2 BOM symbol and BOM structure HM65R3@.	For BOM structure update
16	01/19	33	Change UL3 to SP050006E00	For EMI
17	01/20	5, 7, 9	Change C93, R312, U10, Q14, R465, R463, C140 BOM structure to PS3@	For BOM structure update
18	01/20	41	Change Q31 BOM symbol structure from PS3@ to @	Only for PWWHA DIS unmount
19	01/20	9	Change Q46, R449, C179, C472, R420, R455, Q33 BOM structure from @ to PS3@	Only for PWWHA DIS PS3@

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.6 TO 0.7

GERBER-OUT DATE: 2011/02/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	01/31	5	Change JFAN2.2 connect FAN_SPEED1, JFAN2.3 connect GND	For FAN pin define modification
2	02/09	5,38	Change Q5, Q41 from SB570020110 to SB570020020	For common material

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HW PIR (Product Improve Record)

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.6 TO 1.0

GERBER-OUT DATE: 2011/02/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	01/31	5	Change JFAN2.2 connect FAN_SPEED1, JFAN2.3 connect GND	For FAN pin define modification
2	02/09	5,38	Change Q5,Q41 from SB570020110 to SB570020020	For common material
3	02/17	5	Change C902,R1445,D85,D86,C900,C901,R1444 from mount to @.	For unused PWM FAN
4	02/17	5	Change R24 from @ to mount.	For use RPM FAN
5	02/17	40	Change R396,Q7 from 930@ to mount.	For EC9012 function
6	02/17	31	Add C363	For solving ODD issue
7	02/17	31	Change SW3 from mount to @	For MP phase
8	02/17	41	Change C496,C499,C236,C249,C255 from NLS@ to @	For low cost power switch
9	02/17	41	Change R415,R419 from 47Kohm to 0ohm	For low cost power switch
10	02/17	40	Change ZZZ P/N from DA60000L700 to DAZ0II00101	For MP phase
11	02/17	41	Change C252 from SE070104Z80 to SE071121J80	For low cost power switch
12	02/17	31	Change R561,R562,R457,Q53,R441,R440,C471,C217,Q45 from mount to ZODD@	For zero ODD function
13	02/18	21~29	Change U2 P/N from SA00004EE80 to SA00004EES0	For PCH B3 version
14	02/18	40	Change U2 P/N from SA00004EEA0 to SA00004EET0	For PCH B3 version
15	02/22	40	ADD UV1 BOM symbol and BOM structure N12MR3@.	For N12M R3 P/N
16	02/22	13~16	ADD UV1 BOM structure N12MR1@.	For N12M R1 P/N
17	02/23	32,35,41	Change Q50,Q53,QT3 from SB00000EO00 to SB00000EO10	For common material
18	02/23	41	Change C465,C467 BOM structure from OLS@ to always mount	For low cost power switch

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