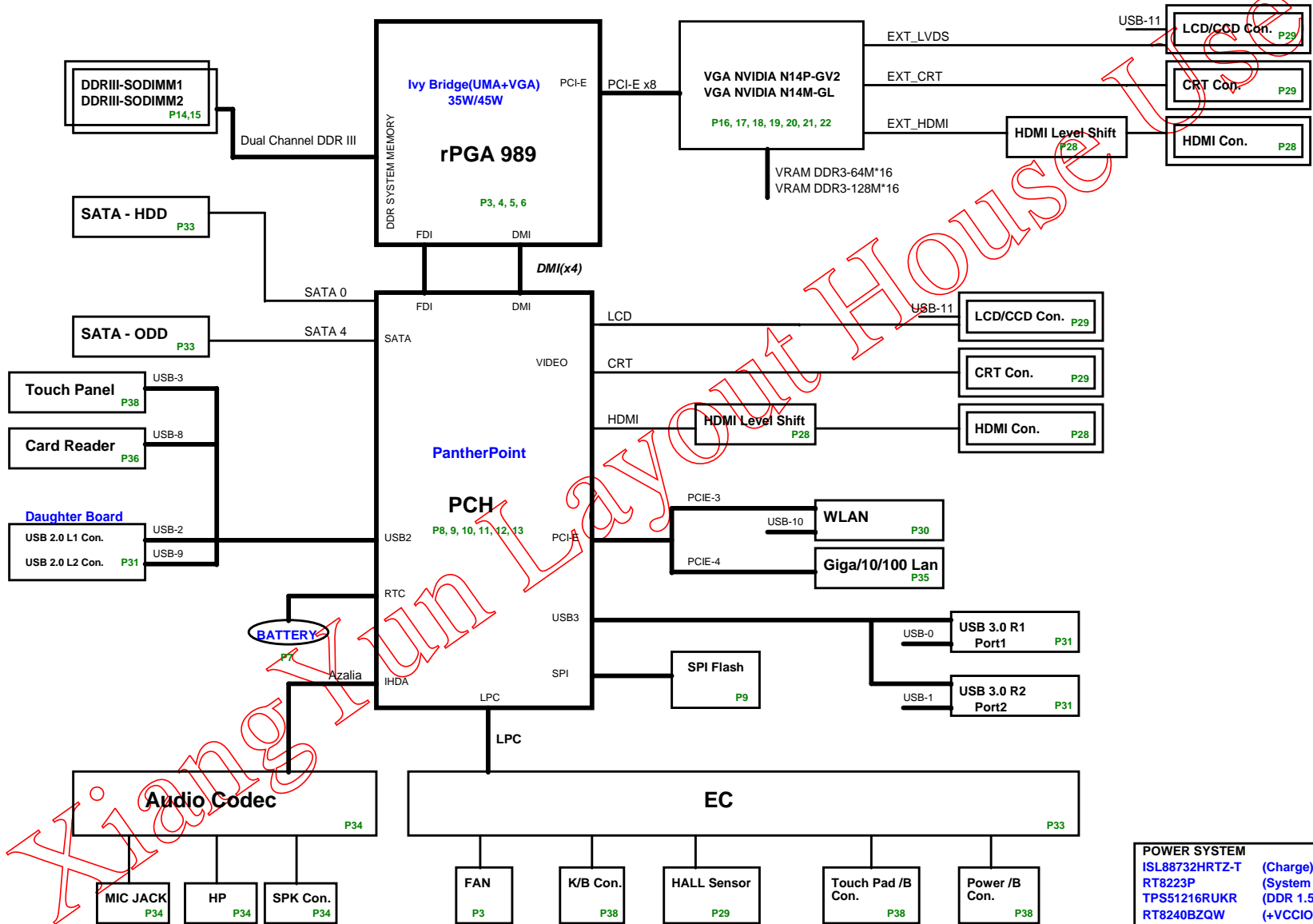


BD5 Block Diagram



POWER SYSTEM		
ISL88732HRTZ-T	(Charge)	P40
RT8223P	(System 5V/3V)	P41
TPS51216RUKR	(DDR 1.5V)	P42
RT8240BZQW	(+VCCIO)	P43
TPS51462RGER	(+VCCSA)	P44
ISL95836HRZ-T	(+VCC_CORE)	P45
G9661-25ADJF12U	(+1.8V)	P46
RT8812A	(NV_GPU_CORE)	P47
	(other GPU)	P48

Quanta Computer Inc.
PROJECT : BD5

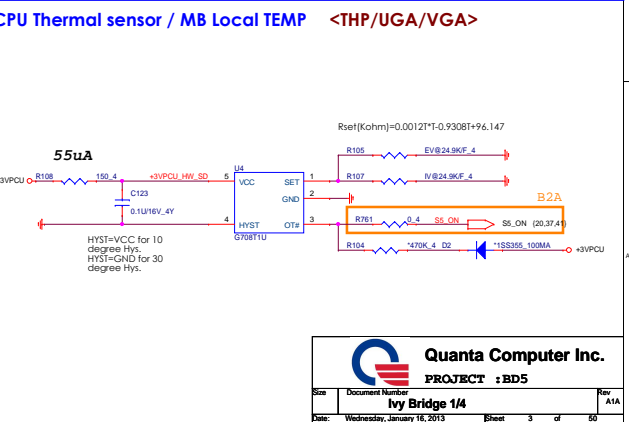
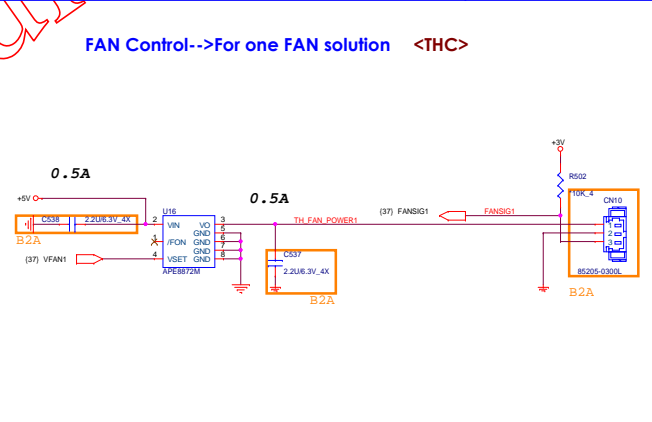
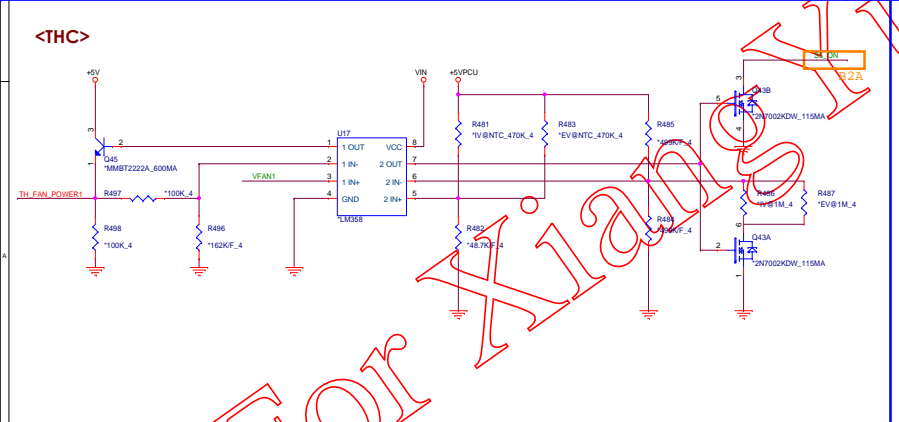
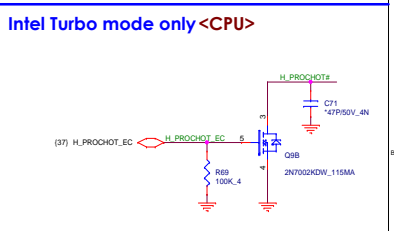
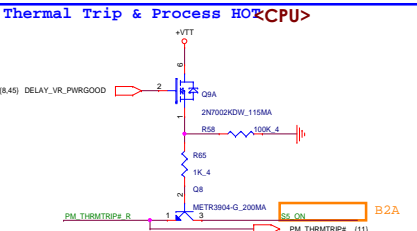
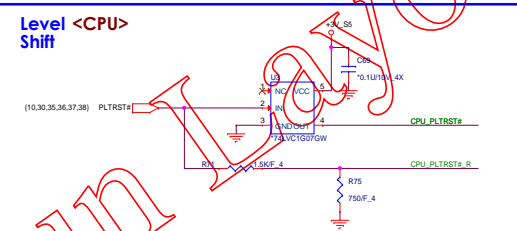
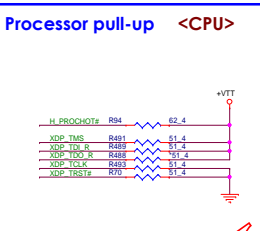
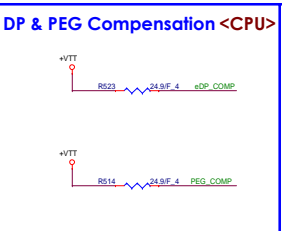
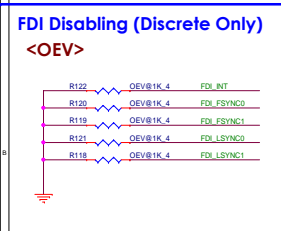
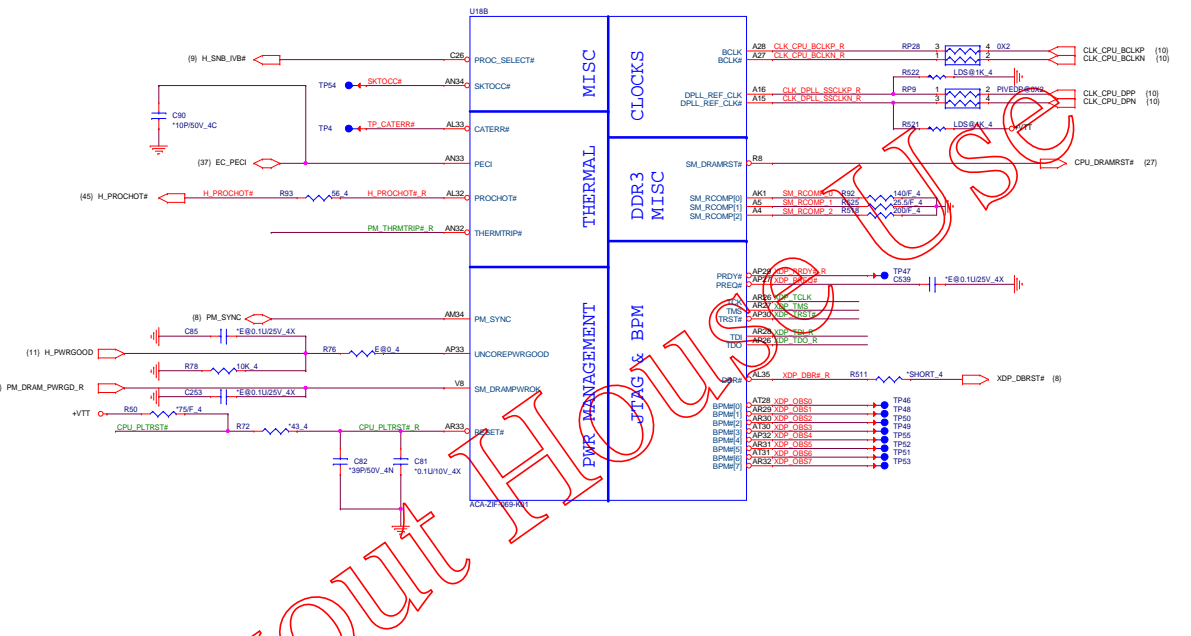
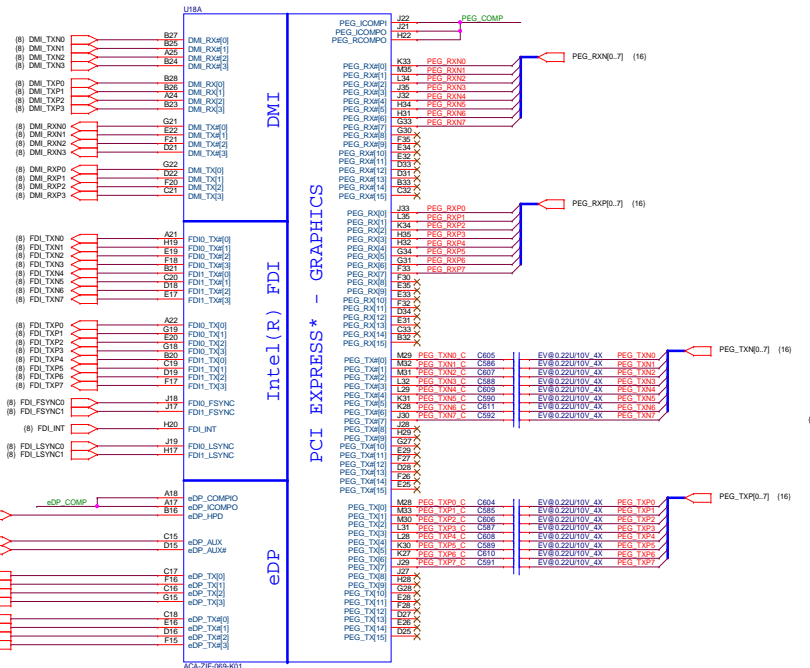
Table of Contents

PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3 - 6	Processor	CPU
8 - 13	PCH	CLG
14 - 15	DDRIII SO-DIMM	DDR
16 - 22	N14P-GV2/N14M-GL	VGA
23 - 24	VRAM - DDR3	VGA
28	HDMI comm part	HDM
29	VGA Connector	VGA
	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
30	MINI Card (Wi-Fi & WIMAX)	MNW
31	USB Connector	USB
	USB Sleep Charger	SLC
33	HDD	HDD
	ODD	ODD
34	Audio Codec	ADO
35	Atheros LAN	LAN
36	Card reader	MMC
37	EC	KBC
38	KeyBoard	KBC
	TP&FP board	TPD,FPD
	Power SW	PSW
39	LED	LED
40	Charger	PWM
41	System 5V/3V	PWM
42	DDR 1.5V	PWM
43	+VCCIO	PWM
44	+VCCSA	PWM
45	+V CORE+VGFX	PWM
46	+1.8V / Discharge	PWM
47	GPU_CORE	PWM
48	other GPU	PWM

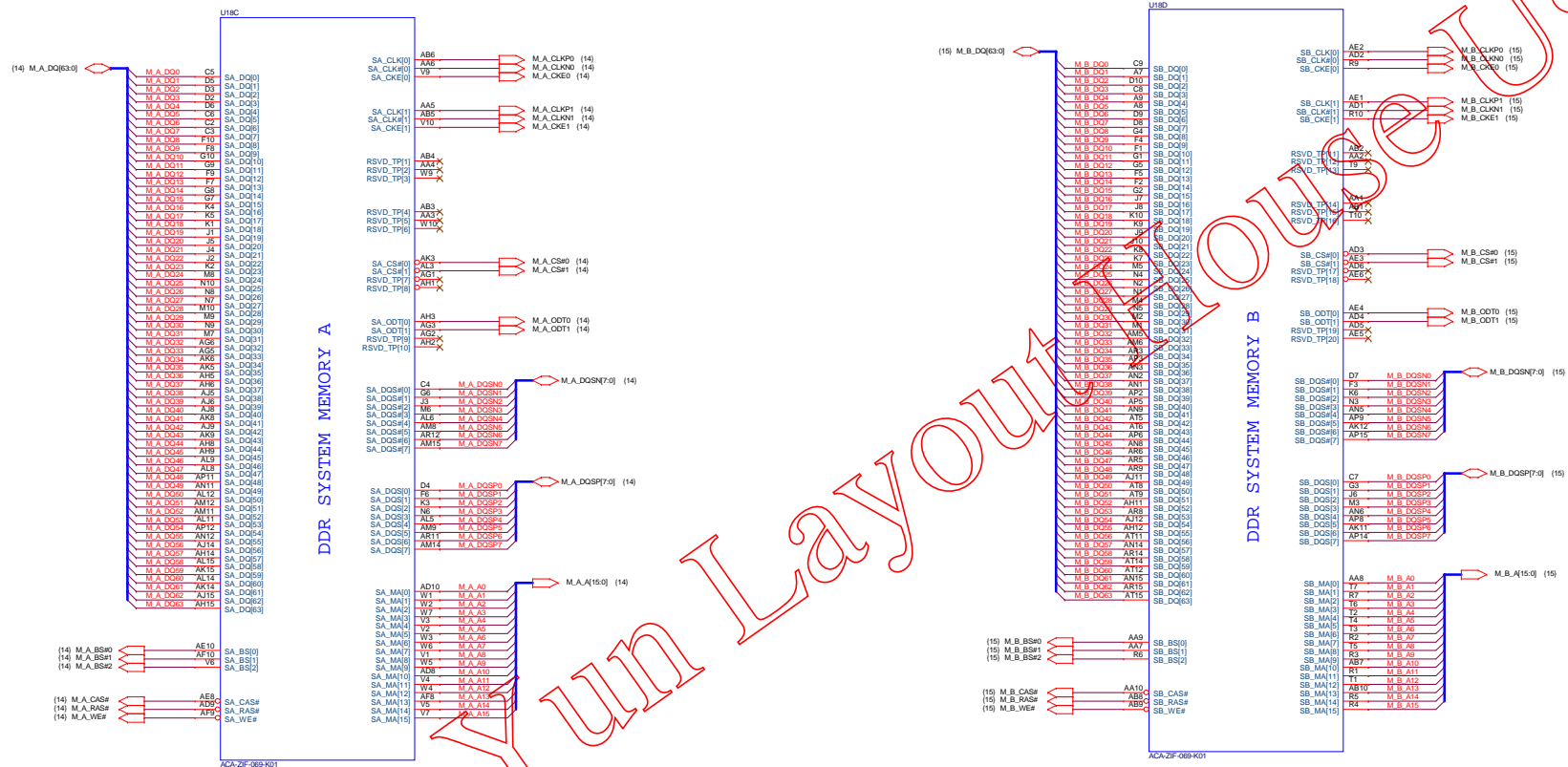
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
+VIN	10V~+19V		S0-S5
+3V_RTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3VPCU	+3.3V	AC/DC Insert enable	S0-S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
+1.5VSUS	+1.5V	S5_ON	S0-S3
+1.5V	+1.5V	MAIN_ON	S0
+VCCIO	+1.05V	MAIN_ON	S0
+VCCSA	-	HWPG_VCCIO	S0
+V CORE+VGFX	-	MPWROK	S0
+3V_GPU	+3.3V	DGPU_PWR_EN_R	S0
+V GPU_CORE	-	DGPU_PWR_EN_RC	S0
+1.5V_GPU	+1.5V	GPU_PWR_GD	S0
+1.05V_GPU	+1.05V	GPU_PWR_GD	S0

GND PLANE	PAGE
↓ GND_SIGNAL	32
↓ 8769GND	37
≡ GND	ALL
↓ ADOGND	34

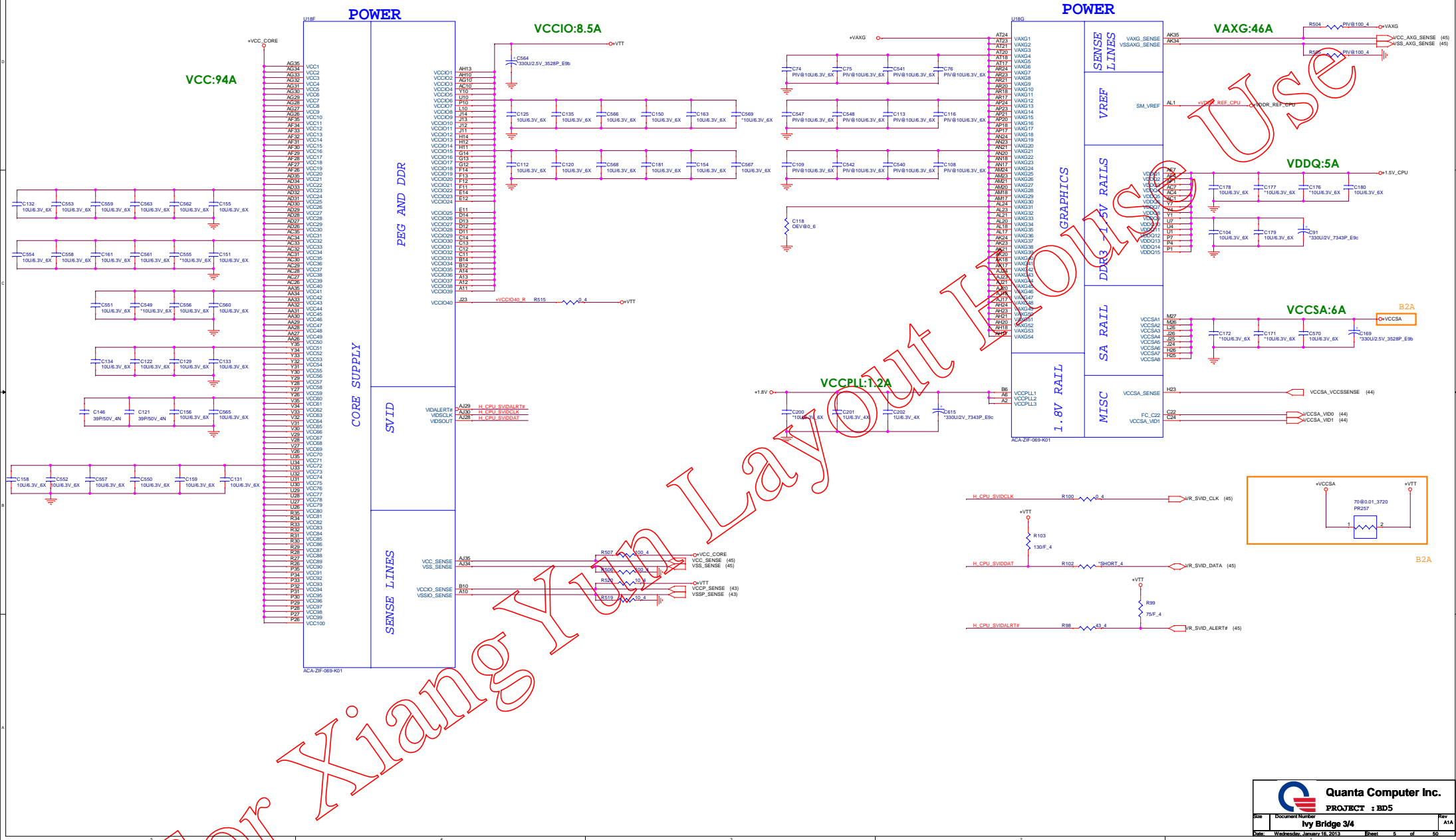
For Xiangyun Layout House Use



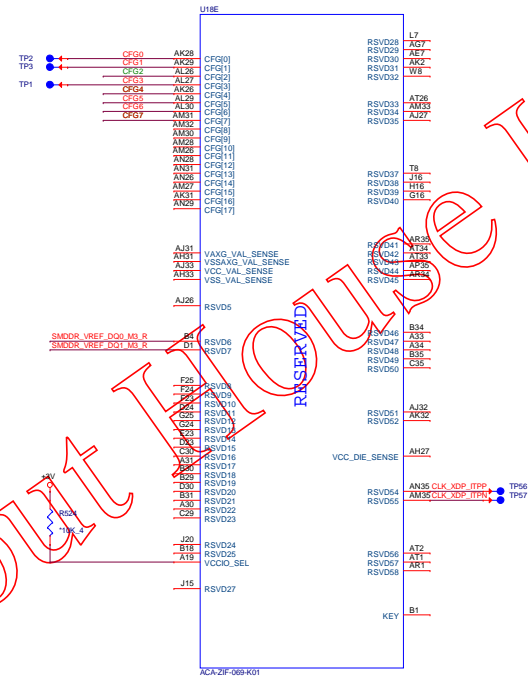
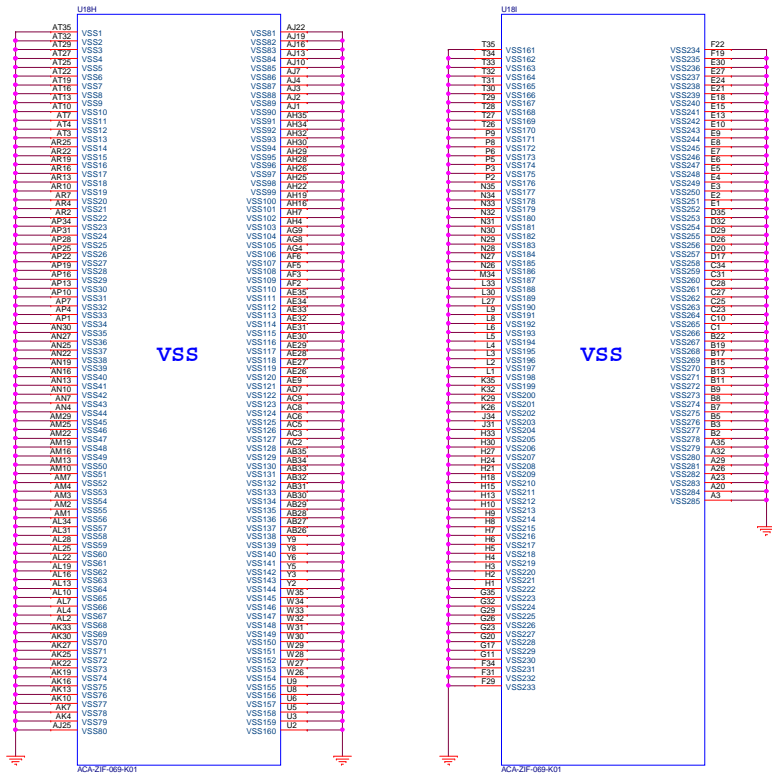
Ivy Bridge Processor (DDR3) <CPU>



For Xiang Yun Layout House Use



For Xiang Yu Layout Holders Use

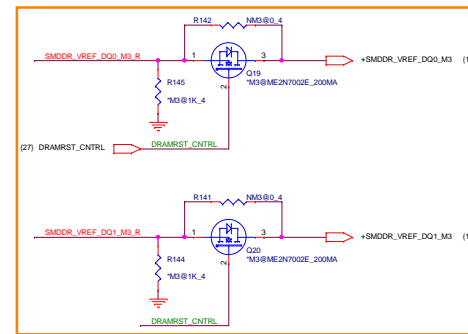


Processor Strapping CPU/VGA

The CFG signals have a default value of '1' if not terminated on the board.

Pin Name	Configuration
CFG2 (PEG Static Lane Reversal --> 16 Lane)	1=Normal Operation 0=Lane Reversed
CFG3 (Reserved)	
CFG4 (DP Presence Strap)	1=Disable; No physical DP attached to eDP 0=Enable; An ext DP device is connected to eDP
CFG5 CFG6 (PCIe Biturion)	00=x8,x4,x4 - Device 1 function 1 and 2 enable 01=Reserved - (Device 1 function 1 disable; function 2 enable) 10=x8,x8 - Device 1 function 1 enable; function 2 enable 11=(Default)x16 - Device 1 function 1 and 2 disable
CFG7 (PEG Defer Training)	1=PEG train immediately following xRES#B de assertion 0=PEG wait for BIOS training

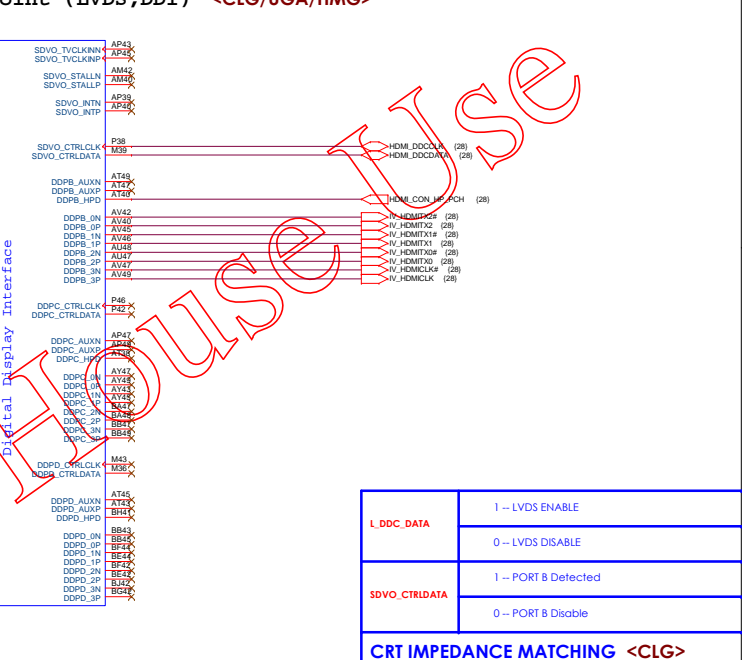
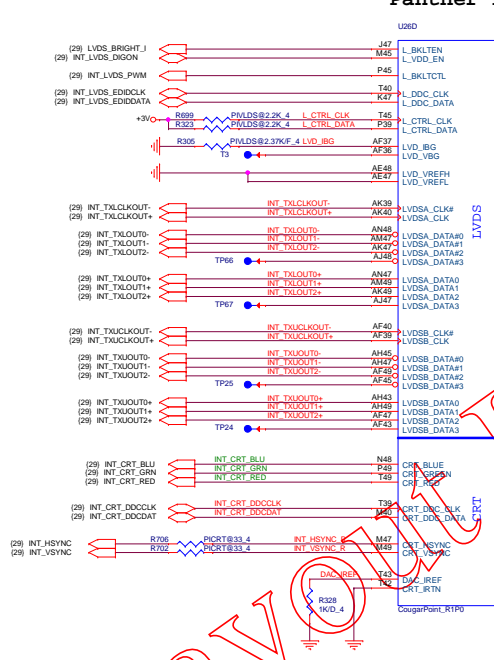
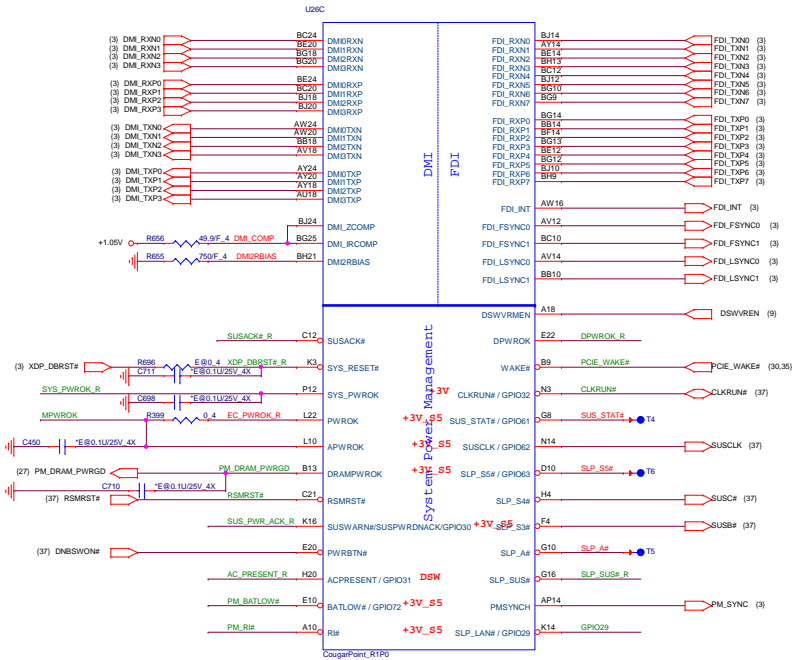
DDR3 VREF DQ (M3) S3P



For Xiang Yun Layout House Use

Panther Point (DMI, FDI, PM) <CLG>

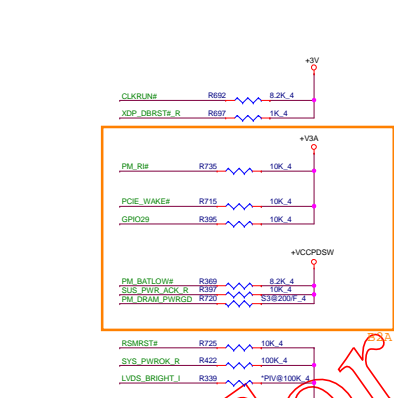
Panther Point (LVDS, DDI) <CLG/UGA/HMG>



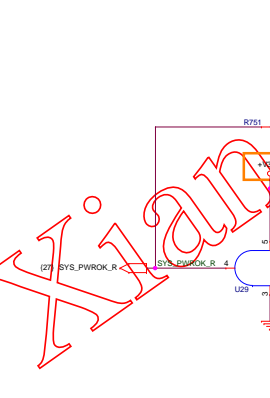
L_DDC_DATA	1 -- LVDS ENABLE
	0 -- LVDS DISABLE
SDVO_CTRLDATA	1 -- PORT B Detected
	0 -- PORT B Disable

CRT IMPEDANCE MATCHING <CLG>

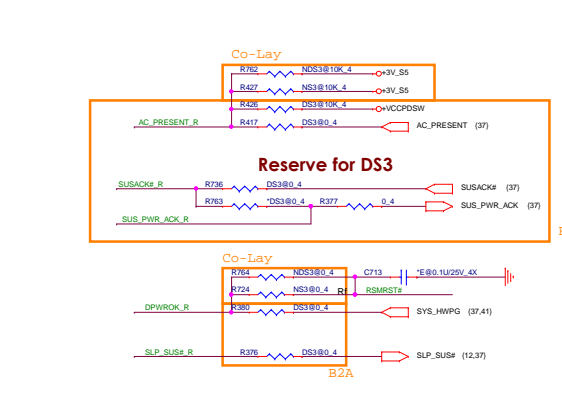
PCH Pull-high/low <CLG>



System PWR_OK <CLG>

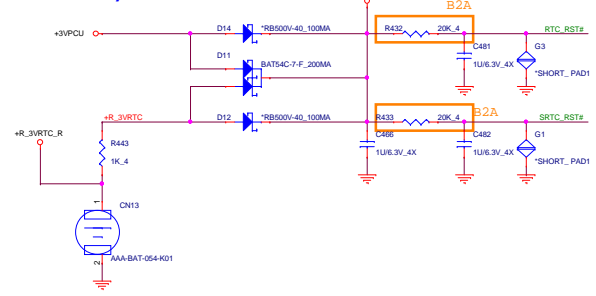


Deep Sx <CLG>

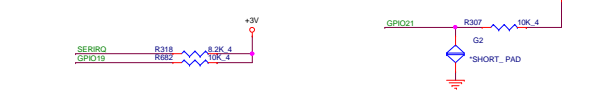


Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	V	NA
SUS_PWR_ACK	V	NA
SUSACK#_R	V	V
DPWROK	V	NA
SLP_SUS	V	NA

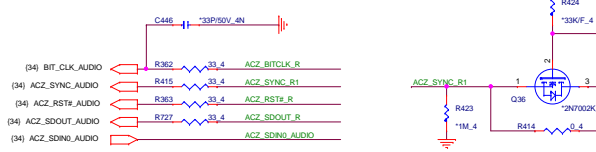
RTC Circuitry <RTC>



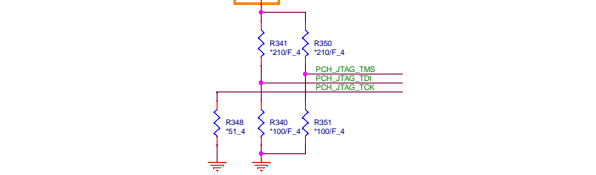
PU & Password Clear <CLG>



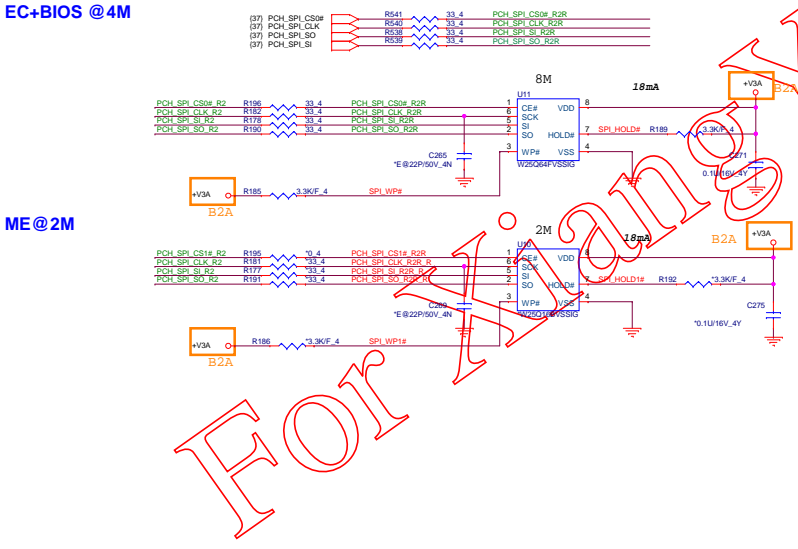
HDA Bus <CLG>



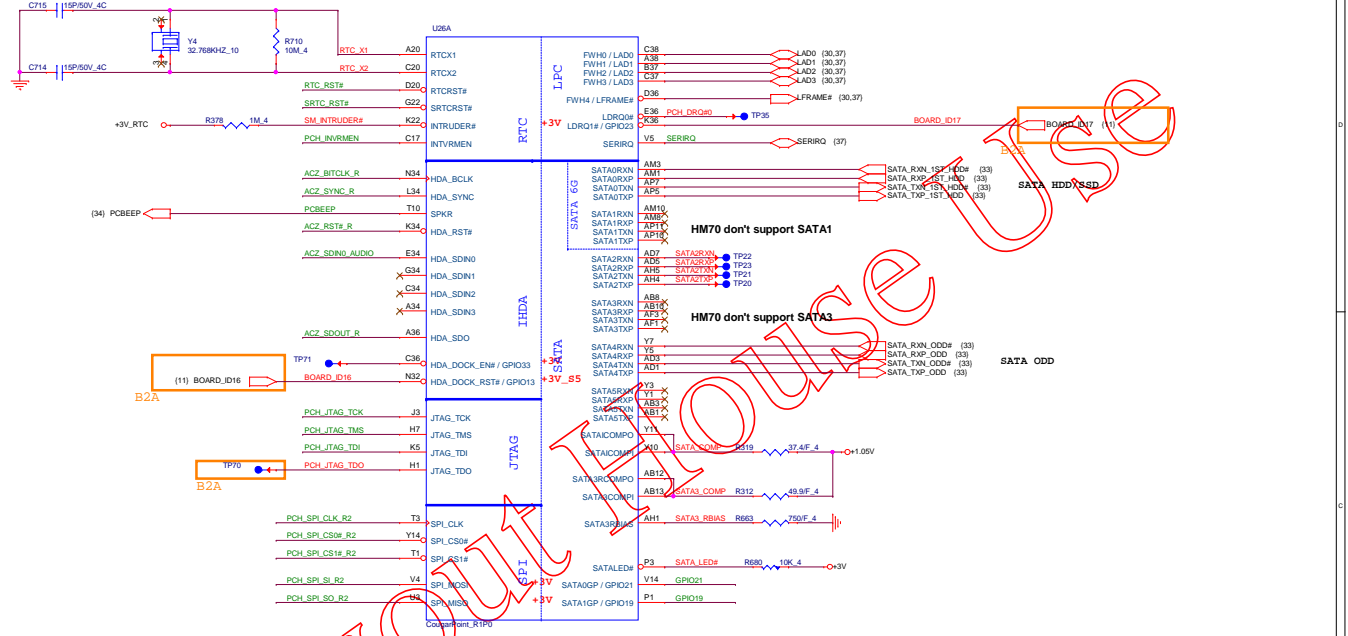
PCH JTAG Debug <CLG>



PCH Dual SPI <CLG>



Panther Point (HDA, JTAG, SATA) <CLG>



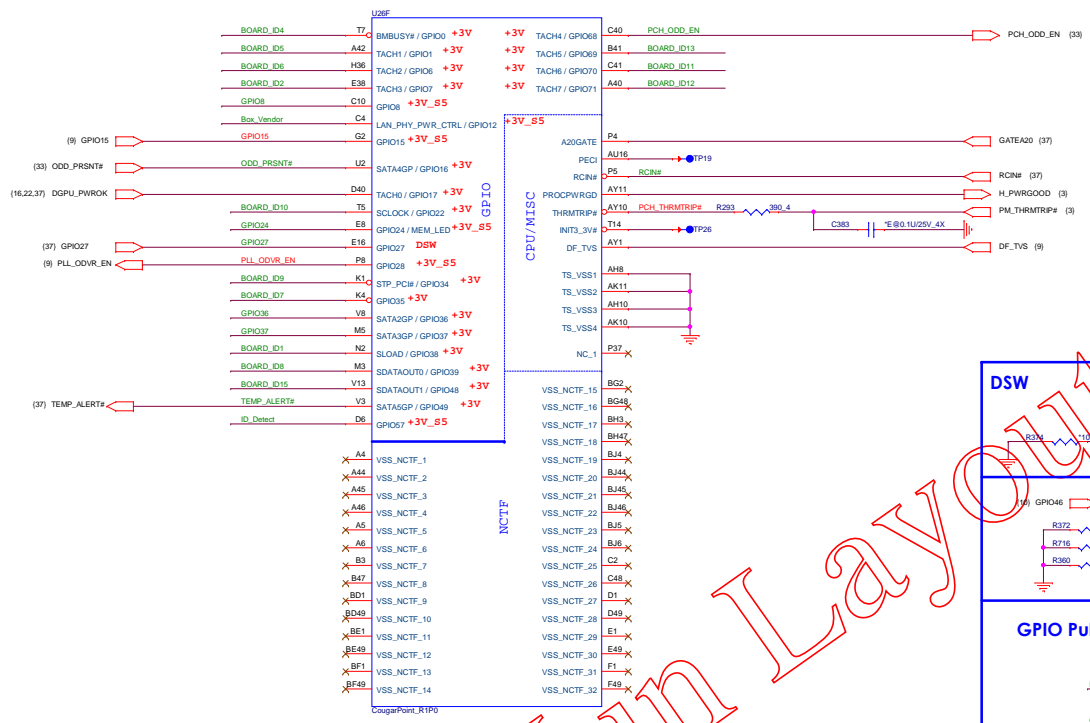
PCH Strap Table

Table with columns: Pin Name, Strap description, Sampled, Configuration, and connections. Rows include SPKR, GNT3# / GPIO55, INTVRMEN, GNT1# / GPIO51, GPIO19, HDA_SDO, DF_TV5, GPIO28, HDA_SYNC, INIT3_3V#, GNT2# / GPIO53, GPIO15, L_DDC_DATA, SDVO_CTRLDATA, DDPC_CTRLDATA, DDPD_CTRLDATA, SATA3GP / GPIO37, SATA2GP / GPIO36, and DSWVRMEN.

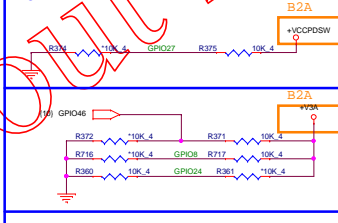
BOARD ID SETTING <CLG>

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14	ID15	ID16	ID17
HM70 HM76	H L														
UMA SKU VGA SKU		H L													
VRAM-1000MHz VRAM-900MHz			H L												
Standard ULV				H L											
17" 14"					H L										
GV2 GL						H L									
W/ 4K2K W/O 4K2K							H L								
W/ HDMI W/O HDMI								H L							
W/ CRT W/O CRT									H L						
Only VGA Optimus										H L					
WIN7 WIN8											H L				
HM75_76 NM70												H L			
EDP LVDS													H L		
Celestron 2775A, 2777														H L	
45W 35W															H L

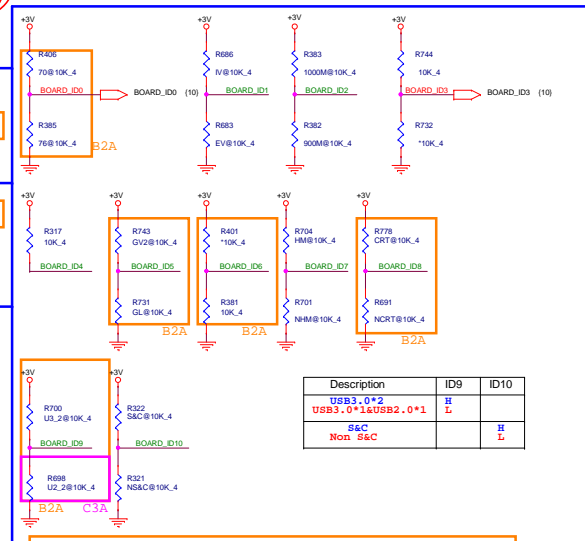
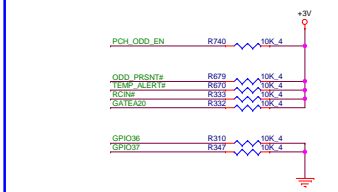
Panther Point (GPIO,VSS_NCTF,RSVD) <CLG>



DSW



GPIO Pull-up/Pull-down <CLG>



Description	ID9	ID10
USB3.0*2	H	L
USB3.0*1&USB2.0*1	L	L
S&C		H
Non S&C		L

Box Vendor	Board_ID11
GPIO12	GPIO70
L	L
ONKYO	H
Harman-Kardon	L
Non-brand	H

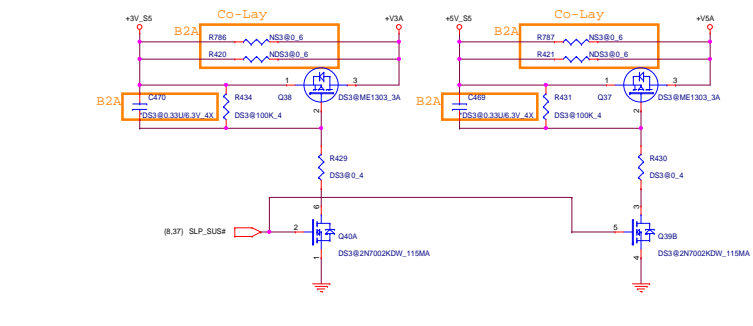
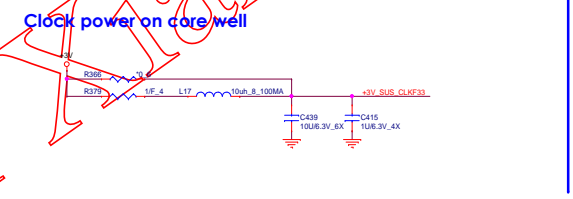
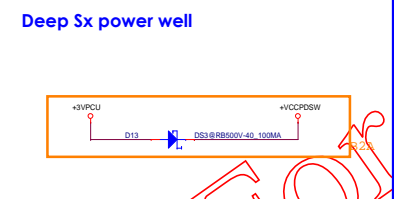
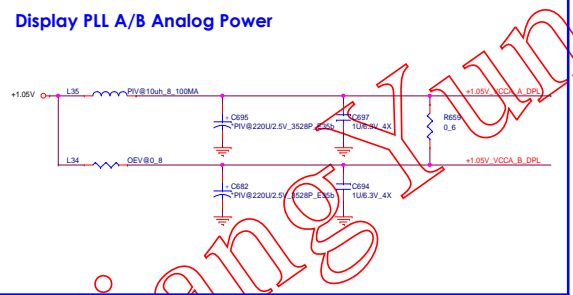
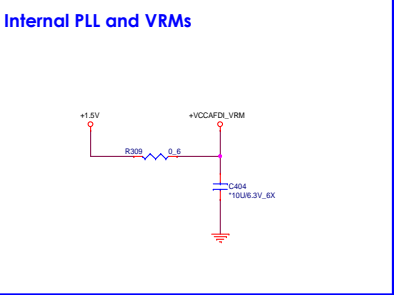
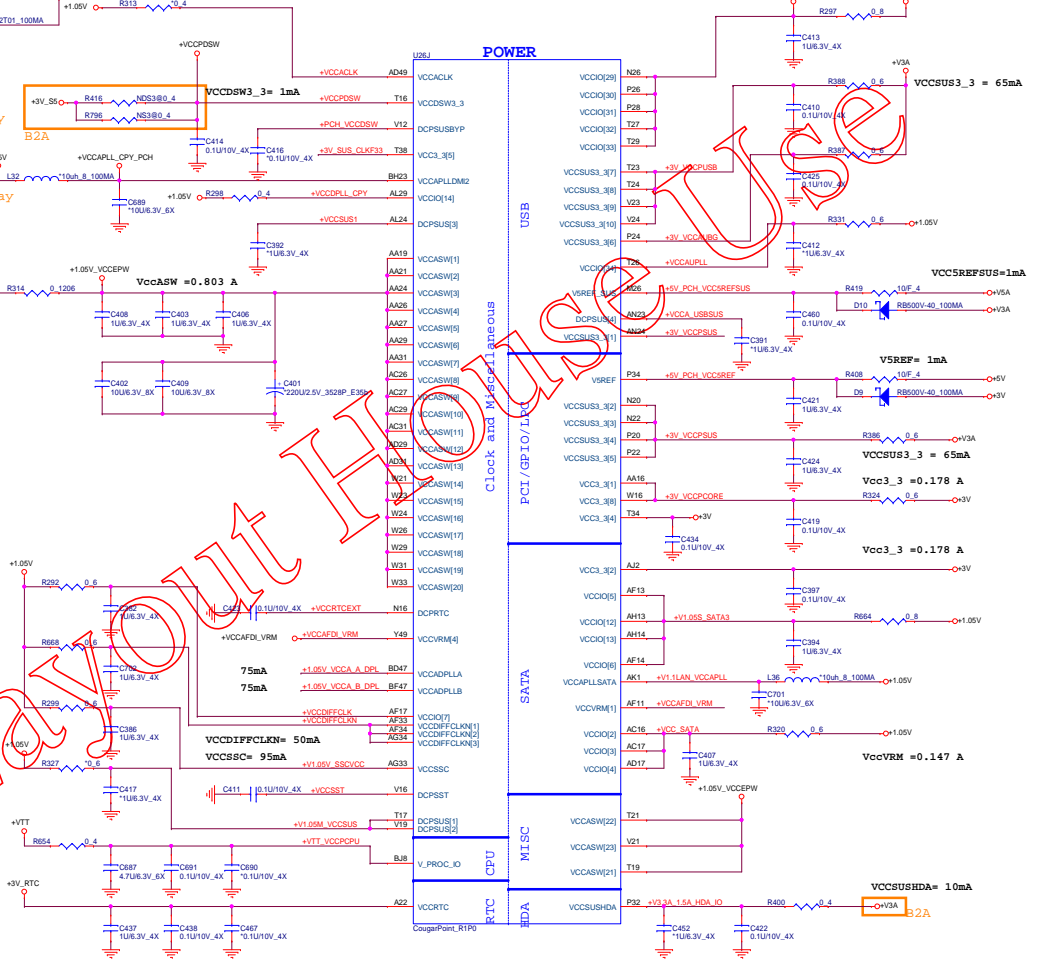
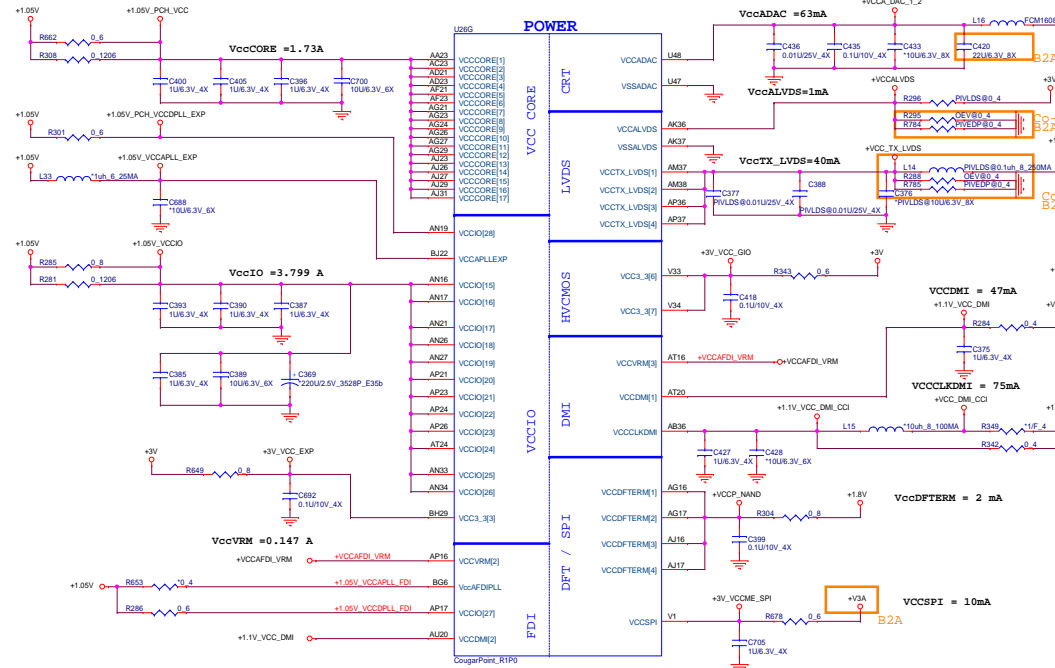
GPIO52	
W/O KB Backlight	H
W KB Backlight	L

GPIO57			
ID_Detect	Speaker	Touch Pad	KB Backlight
H	Metal/IMR	Box	3.3V Metal(Y)
L	TEXTURE	Boxless	5V(NMTP) X

For Xiang Yun Layout

Panther POINT (POWER) <CLG>

Panther Point-M (POWER) <CLG>



Panther Point-M (GND) <CLG>

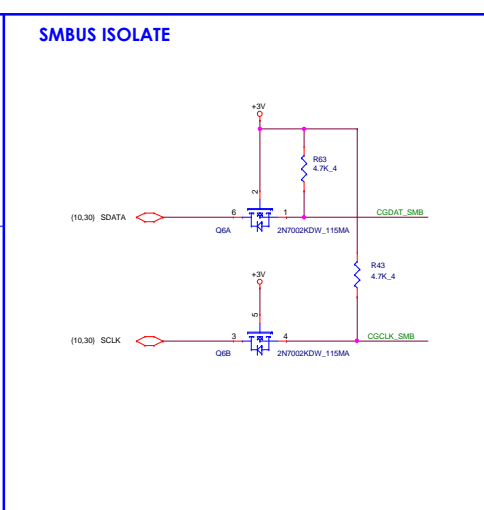
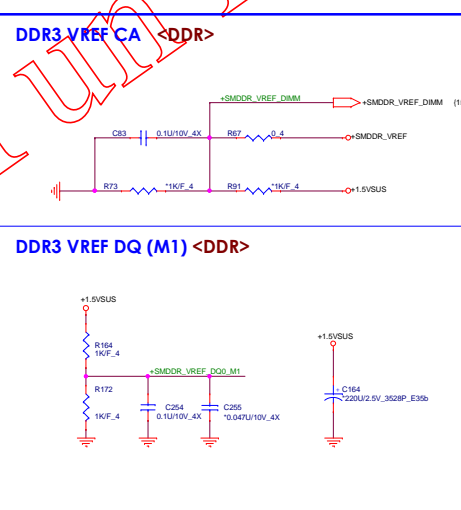
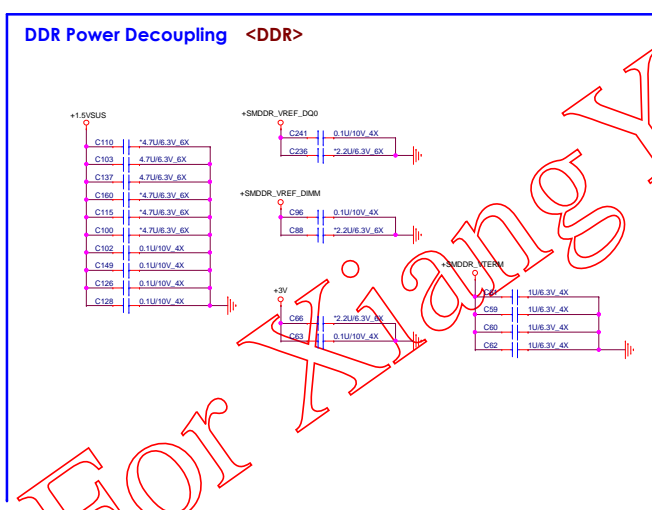
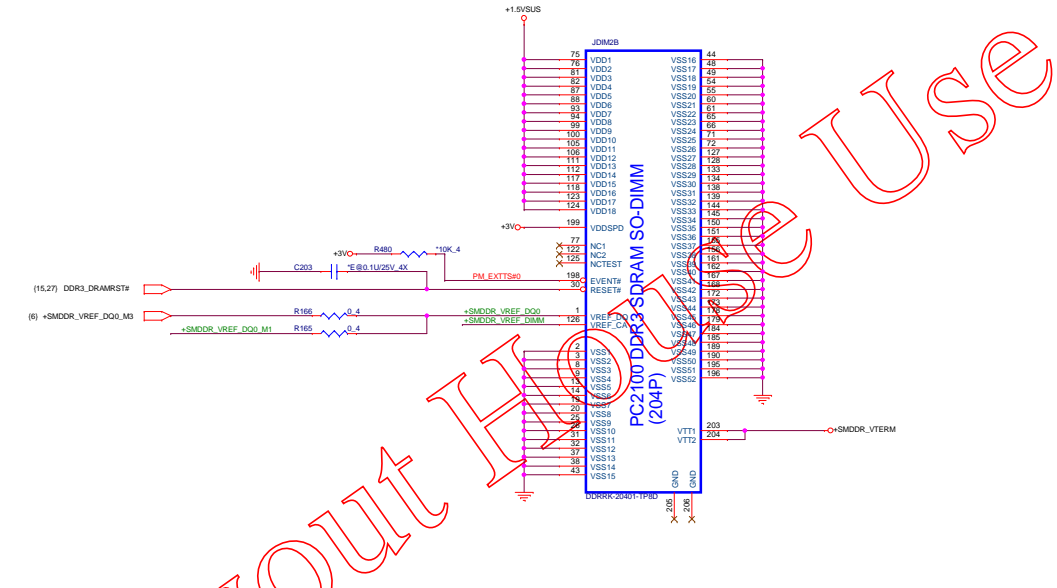
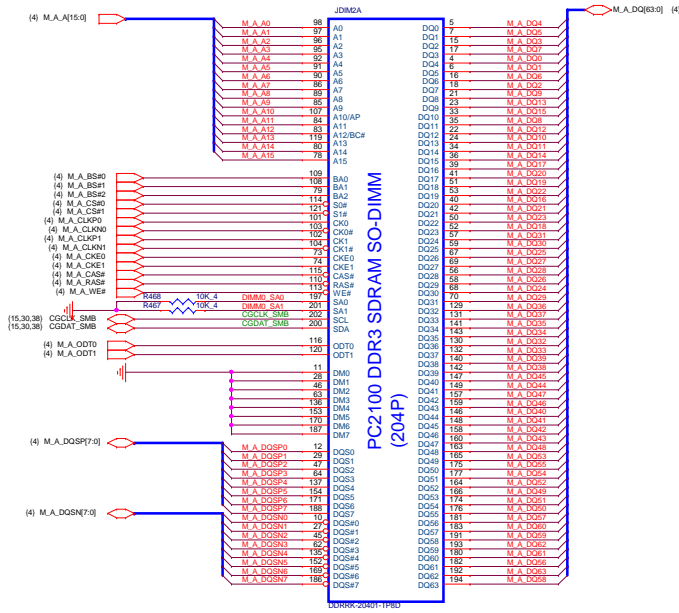
HS	U26H		
VSS00			
AA17	VSS01	AK38	
AA3	VSS02	AK39	
AA33	VSS03	AK40	
AA34	VSS04	AK41	
AA35	VSS05	AK42	
AB11	VSS06	AK43	
AB14	VSS07	AK44	
AB35	VSS08	AK45	
AB4	VSS09	AK46	
AB43	VSS10	AK47	
AB5	VSS11	AK48	
AC18	VSS12	AK49	
AC2	VSS13	AK50	
AC14	VSS14	AK51	
AC21	VSS15	AK52	
AC29	VSS16	AK53	
AC31	VSS17	AK54	
AC35	VSS18	AK55	
AC4	VSS19	AK56	
AD12	VSS20	AK57	
AD13	VSS21	AK58	
AD15	VSS22	AK59	
AD22	VSS23	AK60	
AD24	VSS24	AK61	
AD26	VSS25	AK62	
AD27	VSS26	AK63	
AD33	VSS27	AK64	
AD34	VSS28	AK65	
AD38	VSS29	AK66	
AD39	VSS30	AK67	
AD39	VSS31	AK68	
AD39	VSS32	AK69	
AD39	VSS33	AK70	
AD39	VSS34	AK71	
AD40	VSS35	AK72	
AD42	VSS36	AK73	
AD43	VSS37	AK74	
AD46	VSS38	AK75	
AD46	VSS39	AK76	
AE1	VSS40	AK77	
AE2	VSS41	AK78	
AE3	VSS42	AK79	
AF12	VSS43	AK80	
AF14	VSS44	AK81	
AD18	VSS45	AK82	
AF16	VSS46	AK83	
AF18	VSS47	AK84	
AF2	VSS48	AK85	
AF28	VSS49	AK86	
AF28	VSS50	AK87	
AF27	VSS51	AK88	
AF31	VSS52	AK89	
AF38	VSS53	AK90	
AF4	VSS54	AK91	
AF46	VSS55	AK92	
AF46	VSS56	AK93	
AF5	VSS57	AK94	
AF5	VSS58	AK95	
AF5	VSS59	AK96	
AF5	VSS60	AK97	
AG2	VSS61	AK98	
AG11	VSS62	AK99	
AG4	VSS63	AK100	
AG4	VSS64	AK101	
AH5	VSS65	AK102	
AH8	VSS66	AK103	
AH8	VSS67	AK104	
AH8	VSS68	AK105	
AH40	VSS69	AK106	
AH46	VSS70	AK107	
AH5	VSS71	AK108	
AI18	VSS72	AK109	
AI24	VSS73	AK110	
AI24	VSS74	AK111	
AI24	VSS75	AK112	
AI24	VSS76	AK113	
AI24	VSS77	AK114	
AK12	VSS78	AK115	
AK3	VSS79	AK116	

U26H			
AY4	VSS159	H46	VSS259
AY4	VSS160	K26	VSS260
AY4	VSS161	K28	VSS261
AY4	VSS162	K30	VSS262
AY4	VSS163	K32	VSS263
AY4	VSS164	K34	VSS264
AY4	VSS165	K36	VSS265
AY4	VSS166	K38	VSS266
AY4	VSS167	K40	VSS267
AY4	VSS168	K42	VSS268
AY4	VSS169	K44	VSS269
AY4	VSS170	K46	VSS270
AY4	VSS171	K48	VSS271
AY4	VSS172	K50	VSS272
AY4	VSS173	K52	VSS273
AY4	VSS174	K54	VSS274
AY4	VSS175	K56	VSS275
AY4	VSS176	K58	VSS276
AY4	VSS177	K60	VSS277
AY4	VSS178	K62	VSS278
AY4	VSS179	K64	VSS279
AY4	VSS180	K66	VSS280
AY4	VSS181	K68	VSS281
AY4	VSS182	K70	VSS282
AY4	VSS183	K72	VSS283
AY4	VSS184	K74	VSS284
AY4	VSS185	K76	VSS285
AY4	VSS186	K78	VSS286
AY4	VSS187	K80	VSS287
AY4	VSS188	K82	VSS288
AY4	VSS189	K84	VSS289
AY4	VSS190	K86	VSS290
AY4	VSS191	K88	VSS291
AY4	VSS192	K90	VSS292
AY4	VSS193	K92	VSS293
AY4	VSS194	K94	VSS294
AY4	VSS195	K96	VSS295
AY4	VSS196	K98	VSS296
AY4	VSS197	K100	VSS297
AY4	VSS198	K102	VSS298
AY4	VSS199	K104	VSS299
AY4	VSS200	K106	VSS300
AY4	VSS201	K108	VSS301
AY4	VSS202	K110	VSS302
AY4	VSS203	K112	VSS303
AY4	VSS204	K114	VSS304
AY4	VSS205	K116	VSS305
AY4	VSS206	K118	VSS306
AY4	VSS207	K120	VSS307
AY4	VSS208	K122	VSS308
AY4	VSS209	K124	VSS309
AY4	VSS210	K126	VSS310
AY4	VSS211	K128	VSS311
AY4	VSS212	K130	VSS312
AY4	VSS213	K132	VSS313
AY4	VSS214	K134	VSS314
AY4	VSS215	K136	VSS315
AY4	VSS216	K138	VSS316
AY4	VSS217	K140	VSS317
AY4	VSS218	K142	VSS318
AY4	VSS219	K144	VSS319
AY4	VSS220	K146	VSS320
AY4	VSS221	K148	VSS321
AY4	VSS222	K150	VSS322
AY4	VSS223	K152	VSS323
AY4	VSS224	K154	VSS324
AY4	VSS225	K156	VSS325
AY4	VSS226	K158	VSS326
AY4	VSS227	K160	VSS327
AY4	VSS228	K162	VSS328
AY4	VSS229	K164	VSS329
AY4	VSS230	K166	VSS330
AY4	VSS231	K168	VSS331
AY4	VSS232	K170	VSS332
AY4	VSS233	K172	VSS333
AY4	VSS234	K174	VSS334
AY4	VSS235	K176	VSS335
AY4	VSS236	K178	VSS336
AY4	VSS237	K180	VSS337
AY4	VSS238	K182	VSS338
AY4	VSS239	K184	VSS339
AY4	VSS240	K186	VSS340
AY4	VSS241	K188	VSS341
AY4	VSS242	K190	VSS342
AY4	VSS243	K192	VSS343
AY4	VSS244	K194	VSS344
AY4	VSS245	K196	VSS345
AY4	VSS246	K198	VSS346
AY4	VSS247	K200	VSS347
AY4	VSS248	K202	VSS348
AY4	VSS249	K204	VSS349
AY4	VSS250	K206	VSS350
AY4	VSS251	K208	VSS351
AY4	VSS252	K210	VSS352
AY4	VSS253	K212	VSS353
AY4	VSS254	K214	VSS354
AY4	VSS255	K216	VSS355
AY4	VSS256	K218	VSS356
AY4	VSS257	K220	VSS357
AY4	VSS258	K222	VSS358

For Xiangjun Latout House Use

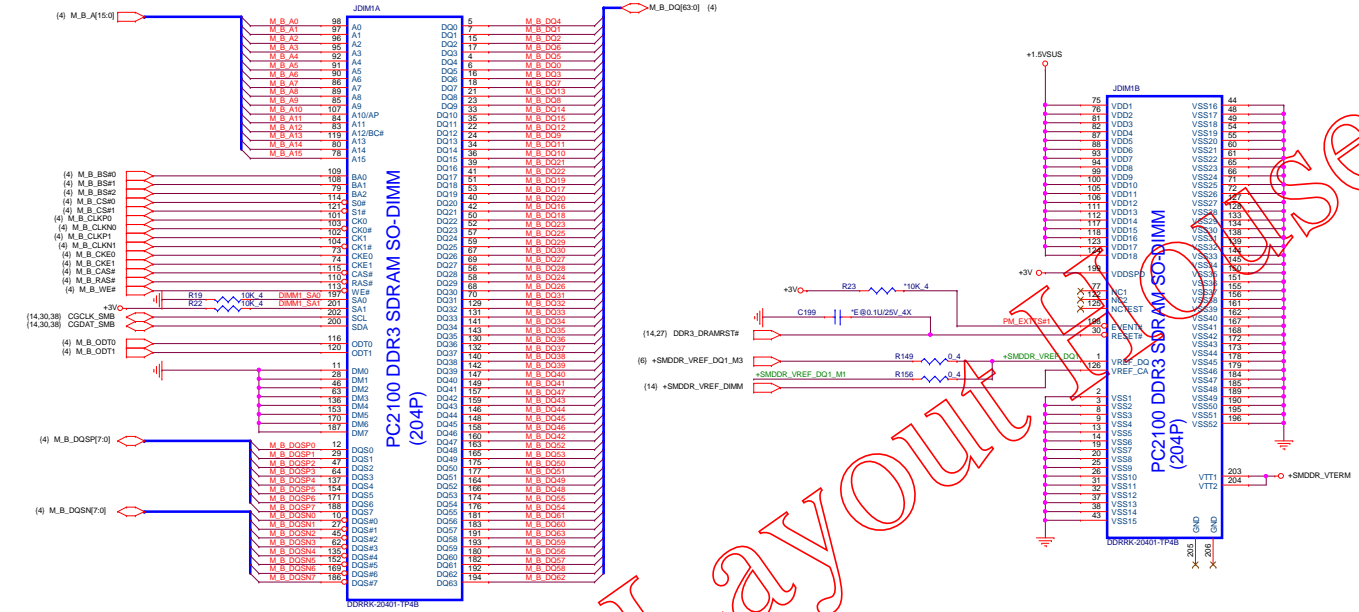
<DDR>

H=8 (Rev)

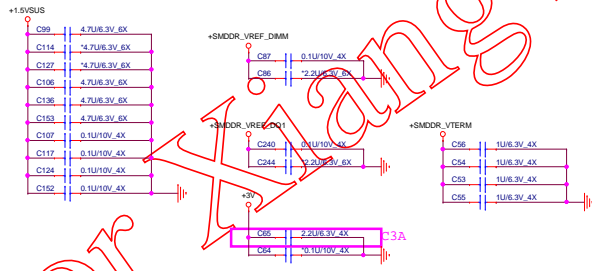


<DDR>

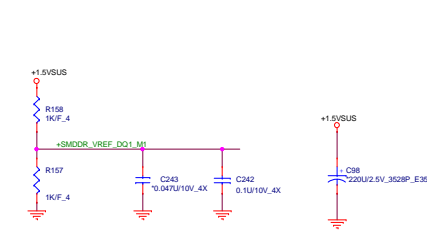
H=4 (Rev)

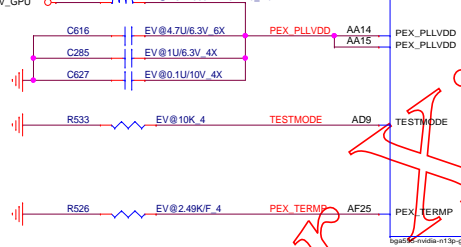
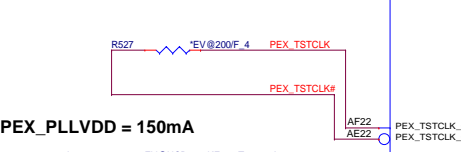
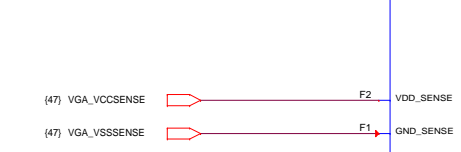
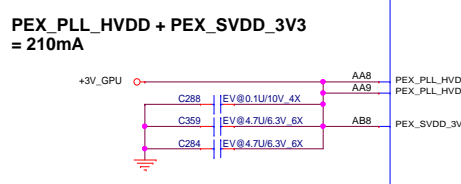
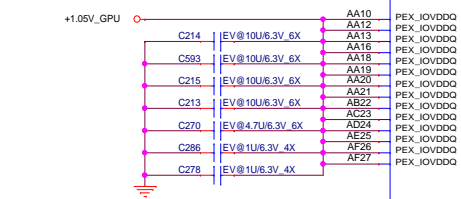
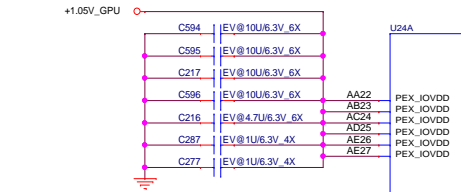


<DDR> DDR Power Decoupling



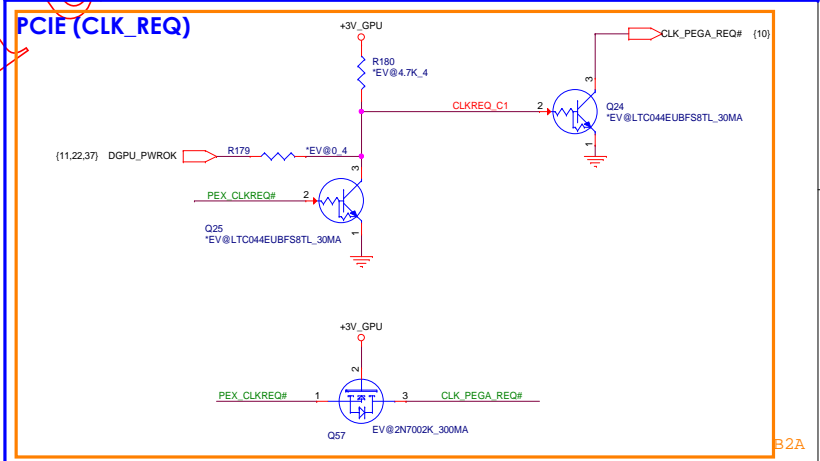
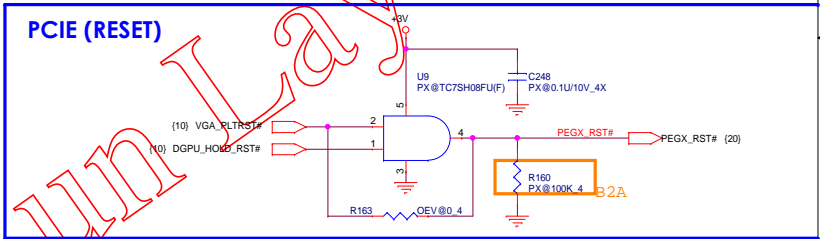
DDR3 VREF DQ (M1) <DDR>





PCI_EXPRESS

NC	PEX_WAKEX
NC	PEX_RST#
NC	PEX_CLKREQ#
NC	PEX_REFCLK#
NC	PEX_TX0
NC	PEX_RX0
NC	PEX_TX1
NC	PEX_RX1
NC	PEX_TX2
NC	PEX_RX2
NC	PEX_TX3
NC	PEX_RX3
NC	PEX_TX4
NC	PEX_RX4
NC	PEX_TX5
NC	PEX_RX5
NC	PEX_TX6
NC	PEX_RX6
NC	PEX_TX7
NC	PEX_RX7
NC	PEX_TX8
NC	PEX_RX8
NC	PEX_TX9
NC	PEX_RX9
NC	PEX_TX10
NC	PEX_RX10
NC	PEX_TX11
NC	PEX_RX11
NC	PEX_TX12
NC	PEX_RX12
NC	PEX_TX13
NC	PEX_RX13
NC	PEX_TX14
NC	PEX_RX14
NC	PEX_TX15
NC	PEX_RX15
NC	PEX_TX16
NC	PEX_RX16
NC	PEX_TX17
NC	PEX_RX17
NC	PEX_TX18
NC	PEX_RX18
NC	PEX_TX19
NC	PEX_RX19
NC	PEX_TX20
NC	PEX_RX20
NC	PEX_TX21
NC	PEX_RX21
NC	PEX_TX22
NC	PEX_RX22
NC	PEX_TX23
NC	PEX_RX23
NC	PEX_TX24
NC	PEX_RX24
NC	PEX_TX25
NC	PEX_RX25
NC	PEX_TX26
NC	PEX_RX26
NC	PEX_TX27
NC	PEX_RX27
NC	PEX_TX28
NC	PEX_RX28
NC	PEX_TX29
NC	PEX_RX29
NC	PEX_TX30
NC	PEX_RX30
NC	PEX_TX31
NC	PEX_RX31
NC	PEX_TX32
NC	PEX_RX32
NC	PEX_TX33
NC	PEX_RX33
NC	PEX_TX34
NC	PEX_RX34
NC	PEX_TX35
NC	PEX_RX35
NC	PEX_TX36
NC	PEX_RX36
NC	PEX_TX37
NC	PEX_RX37
NC	PEX_TX38
NC	PEX_RX38
NC	PEX_TX39
NC	PEX_RX39
NC	PEX_TX40
NC	PEX_RX40
NC	PEX_TX41
NC	PEX_RX41
NC	PEX_TX42
NC	PEX_RX42
NC	PEX_TX43
NC	PEX_RX43
NC	PEX_TX44
NC	PEX_RX44
NC	PEX_TX45
NC	PEX_RX45
NC	PEX_TX46
NC	PEX_RX46
NC	PEX_TX47
NC	PEX_RX47
NC	PEX_TX48
NC	PEX_RX48
NC	PEX_TX49
NC	PEX_RX49
NC	PEX_TX50
NC	PEX_RX50
NC	PEX_TX51
NC	PEX_RX51
NC	PEX_TX52
NC	PEX_RX52
NC	PEX_TX53
NC	PEX_RX53
NC	PEX_TX54
NC	PEX_RX54
NC	PEX_TX55
NC	PEX_RX55
NC	PEX_TX56
NC	PEX_RX56
NC	PEX_TX57
NC	PEX_RX57
NC	PEX_TX58
NC	PEX_RX58
NC	PEX_TX59
NC	PEX_RX59
NC	PEX_TX60
NC	PEX_RX60
NC	PEX_TX61
NC	PEX_RX61
NC	PEX_TX62
NC	PEX_RX62
NC	PEX_TX63
NC	PEX_RX63
NC	PEX_TX64
NC	PEX_RX64
NC	PEX_TX65
NC	PEX_RX65
NC	PEX_TX66
NC	PEX_RX66
NC	PEX_TX67
NC	PEX_RX67
NC	PEX_TX68
NC	PEX_RX68
NC	PEX_TX69
NC	PEX_RX69
NC	PEX_TX70
NC	PEX_RX70
NC	PEX_TX71
NC	PEX_RX71
NC	PEX_TX72
NC	PEX_RX72
NC	PEX_TX73
NC	PEX_RX73
NC	PEX_TX74
NC	PEX_RX74
NC	PEX_TX75
NC	PEX_RX75
NC	PEX_TX76
NC	PEX_RX76
NC	PEX_TX77
NC	PEX_RX77
NC	PEX_TX78
NC	PEX_RX78
NC	PEX_TX79
NC	PEX_RX79
NC	PEX_TX80
NC	PEX_RX80
NC	PEX_TX81
NC	PEX_RX81
NC	PEX_TX82
NC	PEX_RX82
NC	PEX_TX83
NC	PEX_RX83
NC	PEX_TX84
NC	PEX_RX84
NC	PEX_TX85
NC	PEX_RX85
NC	PEX_TX86
NC	PEX_RX86
NC	PEX_TX87
NC	PEX_RX87
NC	PEX_TX88
NC	PEX_RX88
NC	PEX_TX89
NC	PEX_RX89
NC	PEX_TX90
NC	PEX_RX90
NC	PEX_TX91
NC	PEX_RX91
NC	PEX_TX92
NC	PEX_RX92
NC	PEX_TX93
NC	PEX_RX93
NC	PEX_TX94
NC	PEX_RX94
NC	PEX_TX95
NC	PEX_RX95
NC	PEX_TX96
NC	PEX_RX96
NC	PEX_TX97
NC	PEX_RX97
NC	PEX_TX98
NC	PEX_RX98
NC	PEX_TX99
NC	PEX_RX99
NC	PEX_TX100
NC	PEX_RX100

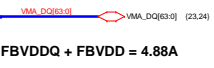


FOR HUMAN LAYOUT HOUSE USE



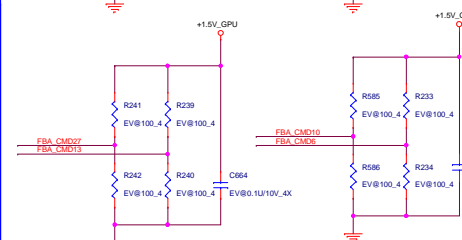
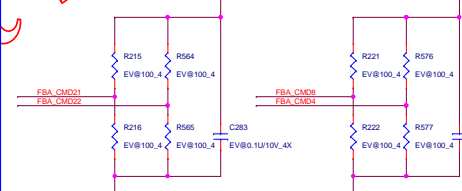
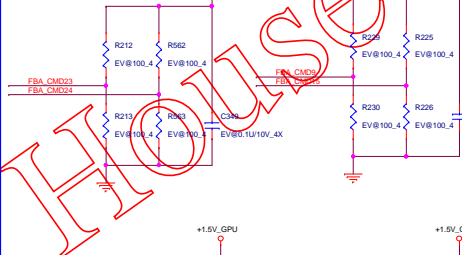
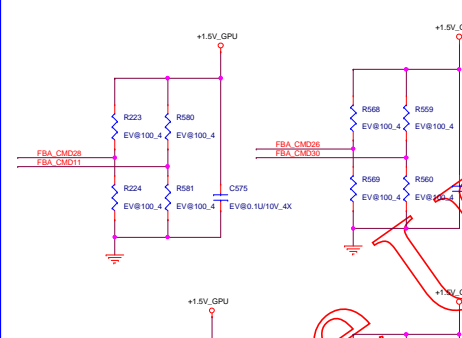
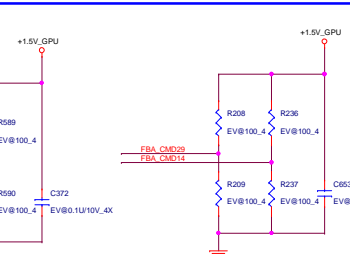
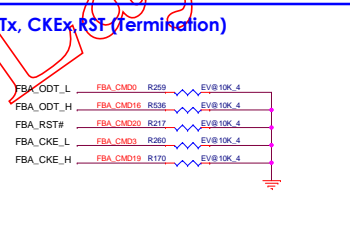
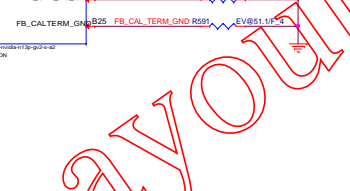
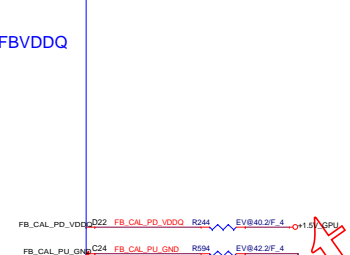
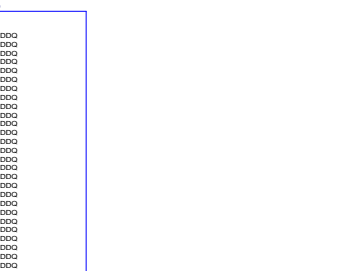
U24B

FBA_D0	E18	VMA_D00
FBA_D1	E16	VMA_D01
FBA_D2	E16	VMA_D02
FBA_D3	E20	VMA_D03
FBA_D4	D20	VMA_D04
FBA_D5	D21	VMA_D05
FBA_D6	F20	VMA_D06
FBA_D7	E21	VMA_D07
FBA_D8	E15	VMA_D08
FBA_D9	D15	VMA_D09
FBA_D10	F13	VMA_D10
FBA_D11	C13	VMA_D11
FBA_D12	E13	VMA_D12
FBA_D13	B13	VMA_D13
FBA_D14	E13	VMA_D14
FBA_D15	D13	VMA_D15
FBA_D16	B15	VMA_D16
FBA_D17	A15	VMA_D17
FBA_D18	A13	VMA_D18
FBA_D19	A15	VMA_D19
FBA_D20	B18	VMA_D20
FBA_D21	A18	VMA_D21
FBA_D22	A18	VMA_D22
FBA_D23	C19	VMA_D23
FBA_D24	B24	VMA_D24
FBA_D25	C23	VMA_D25
FBA_D26	A25	VMA_D26
FBA_D27	A24	VMA_D27
FBA_D28	A24	VMA_D28
FBA_D29	B21	VMA_D29
FBA_D30	C20	VMA_D30
FBA_D31	C21	VMA_D31
FBA_D32	R22	VMA_D32
FBA_D33	R24	VMA_D33
FBA_D34	T22	VMA_D34
FBA_D35	K25	VMA_D35
FBA_D36	N26	VMA_D36
FBA_D37	O25	VMA_D37
FBA_D38	O23	VMA_D38
FBA_D39	N24	VMA_D39
FBA_D40	Y23	VMA_D40
FBA_D41	Y22	VMA_D41
FBA_D42	Y23	VMA_D42
FBA_D43	U22	VMA_D43
FBA_D44	Y22	VMA_D44
FBA_D45	A24	VMA_D45
FBA_D46	A23	VMA_D46
FBA_D47	A27	VMA_D47
FBA_D48	A26	VMA_D48
FBA_D49	A26	VMA_D49
FBA_D50	A26	VMA_D50
FBA_D51	A26	VMA_D51
FBA_D52	A27	VMA_D52
FBA_D53	W26	VMA_D53
FBA_D54	T25	VMA_D54
FBA_D55	C25	VMA_D55
FBA_D56	T25	VMA_D56
FBA_D57	T25	VMA_D57
FBA_D58	T27	VMA_D58
FBA_D59	Z27	VMA_D59
FBA_D60	Y28	VMA_D60
FBA_D61	Z27	VMA_D61
FBA_D62	Y27	VMA_D62
FBA_D63	W25	VMA_D63

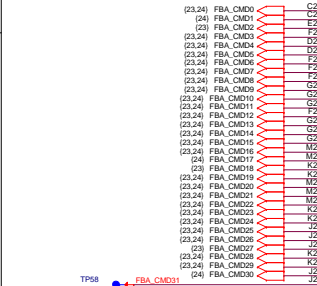


U24D

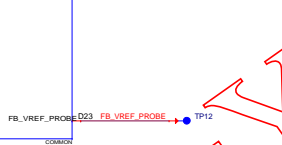
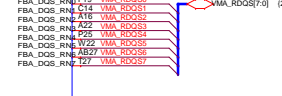
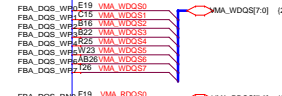
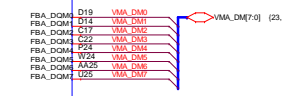
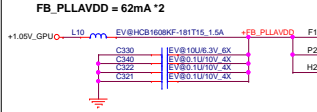
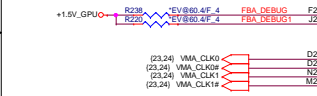
FBA_D0	E18	VMA_D00
FBA_D1	E16	VMA_D01
FBA_D2	E16	VMA_D02
FBA_D3	E20	VMA_D03
FBA_D4	D20	VMA_D04
FBA_D5	D21	VMA_D05
FBA_D6	F20	VMA_D06
FBA_D7	E21	VMA_D07
FBA_D8	E15	VMA_D08
FBA_D9	D15	VMA_D09
FBA_D10	F13	VMA_D10
FBA_D11	C13	VMA_D11
FBA_D12	E13	VMA_D12
FBA_D13	B13	VMA_D13
FBA_D14	E13	VMA_D14
FBA_D15	D13	VMA_D15
FBA_D16	B15	VMA_D16
FBA_D17	A15	VMA_D17
FBA_D18	A13	VMA_D18
FBA_D19	A15	VMA_D19
FBA_D20	B18	VMA_D20
FBA_D21	A18	VMA_D21
FBA_D22	A18	VMA_D22
FBA_D23	C19	VMA_D23
FBA_D24	B24	VMA_D24
FBA_D25	C23	VMA_D25
FBA_D26	A25	VMA_D26
FBA_D27	A24	VMA_D27
FBA_D28	A24	VMA_D28
FBA_D29	B21	VMA_D29
FBA_D30	C20	VMA_D30
FBA_D31	C21	VMA_D31
FBA_D32	R22	VMA_D32
FBA_D33	R24	VMA_D33
FBA_D34	T22	VMA_D34
FBA_D35	K25	VMA_D35
FBA_D36	N26	VMA_D36
FBA_D37	O25	VMA_D37
FBA_D38	O23	VMA_D38
FBA_D39	N24	VMA_D39
FBA_D40	Y23	VMA_D40
FBA_D41	Y22	VMA_D41
FBA_D42	Y23	VMA_D42
FBA_D43	U22	VMA_D43
FBA_D44	Y22	VMA_D44
FBA_D45	A24	VMA_D45
FBA_D46	A23	VMA_D46
FBA_D47	A27	VMA_D47
FBA_D48	A26	VMA_D48
FBA_D49	A26	VMA_D49
FBA_D50	A26	VMA_D50
FBA_D51	A26	VMA_D51
FBA_D52	A27	VMA_D52
FBA_D53	W26	VMA_D53
FBA_D54	T25	VMA_D54
FBA_D55	C25	VMA_D55
FBA_D56	T25	VMA_D56
FBA_D57	T25	VMA_D57
FBA_D58	T27	VMA_D58
FBA_D59	Z27	VMA_D59
FBA_D60	Y28	VMA_D60
FBA_D61	Z27	VMA_D61
FBA_D62	Y27	VMA_D62
FBA_D63	W25	VMA_D63



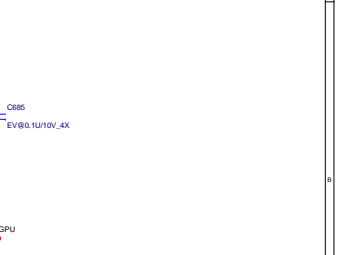
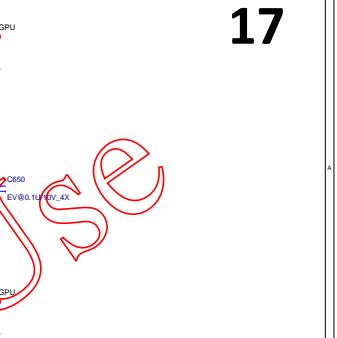
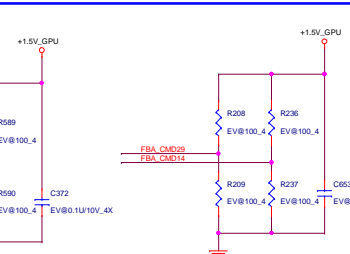
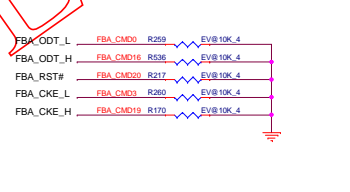
DUAL RANK (Mode E)

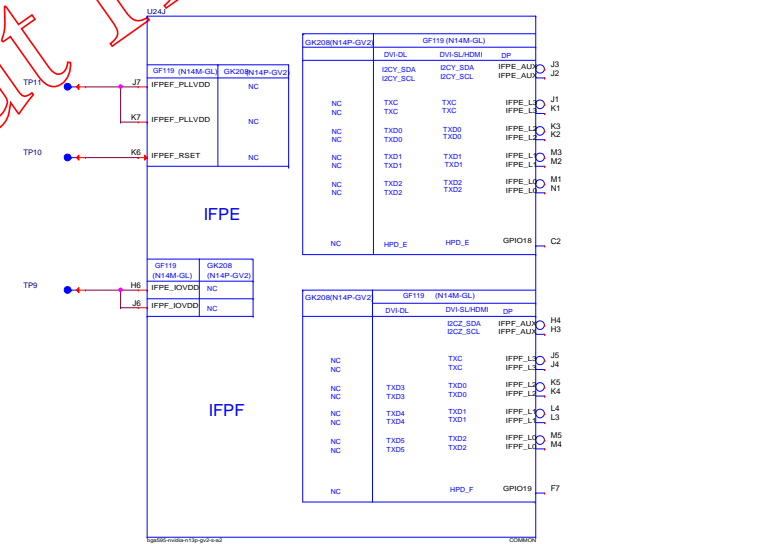
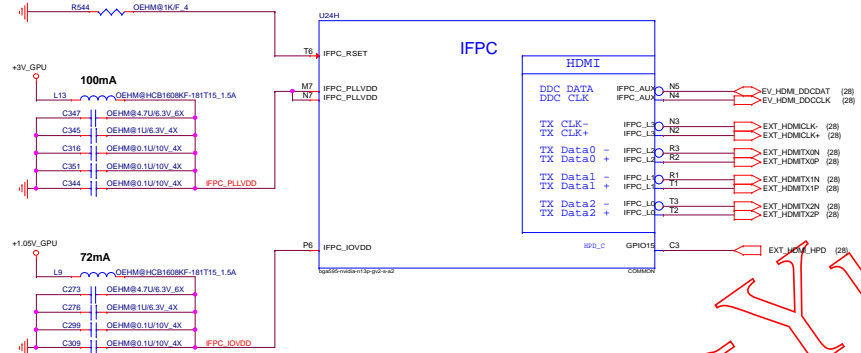
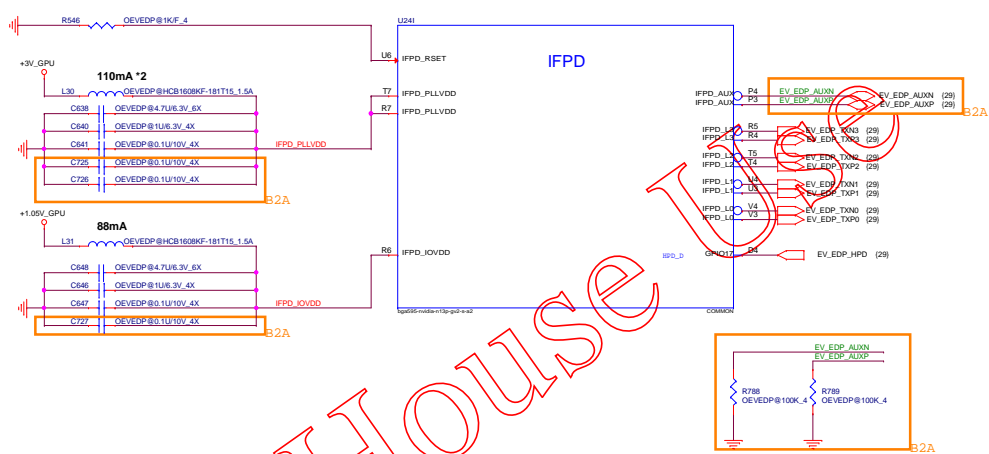
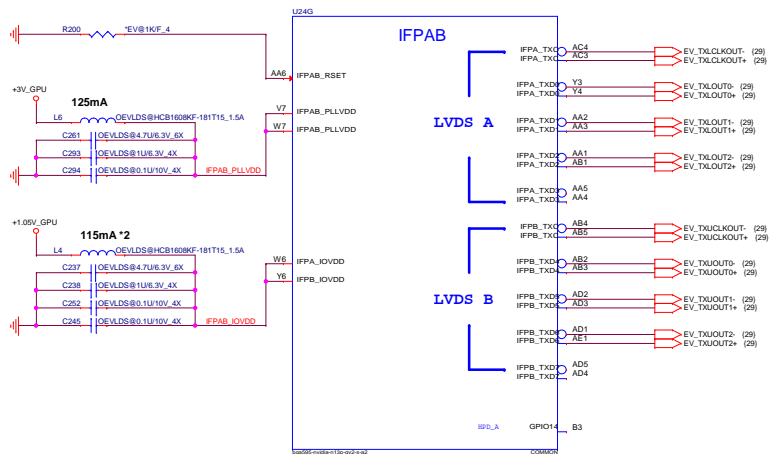


(23.24) FBA_CMD0	C27	FBA_CMD0	Rank 0/1 [31:0] CS19
(24) FBA_CMD1	C28	FBA_CMD1	Rank1 [31:0] CS19
(23) FBA_CMD2	F24	FBA_CMD2	Rank 0/1 [31:0] CS2
(23.24) FBA_CMD3	E24	FBA_CMD3	Rank0/ [31:0] CS29
(23.24) FBA_CMD4	D26	FBA_CMD4	[Rank0:18] [Rank1:14]
(23.24) FBA_CMD5	D26	FBA_CMD5	[Rank0:18] [Rank1:14]
(23.24) FBA_CMD6	F25	FBA_CMD6	[Rank0:15] [Rank1:18]
(23.24) FBA_CMD7	G25	FBA_CMD7	[Rank0:18] [Rank1:15]
(23.24) FBA_CMD8	F23	FBA_CMD8	[Rank0:18] [Rank1:18]
(23.24) FBA_CMD9	G25	FBA_CMD9	[Rank0:18] [Rank1:18]
(23.24) FBA_CMD10	G23	FBA_CMD10	[Rank0:14] [Rank1:12]
(23.24) FBA_CMD11	G24	FBA_CMD11	[Rank0:18] [Rank1:18]
(23.24) FBA_CMD12	F27	FBA_CMD12	[Rank0:11] [Rank1:14]
(23.24) FBA_CMD13	G25	FBA_CMD13	[Rank0:18] [Rank1:18]
(23.24) FBA_CMD14	G27	FBA_CMD14	[Rank0:14] [Rank1:13]
(23.24) FBA_CMD15	G26	FBA_CMD15	[Rank0:18] [Rank1:18]
(23.24) FBA_CMD16	M24	FBA_CMD16	[Rank0:18] [Rank1:18]
(24) FBA_CMD17	M23	FBA_CMD17	Rank1 [18:12] CS19
(23) FBA_CMD18	K24	FBA_CMD18	Rank0 [18:12] CS29
(23.24) FBA_CMD19	K23	FBA_CMD19	Rank 0/1 [18:12] CS2
(23.24) FBA_CMD20	M27	FBA_CMD20	[Rank0:17] [Rank1:16]
(23.24) FBA_CMD21	M25	FBA_CMD21	[Rank0:14] [Rank1:15]
(23.24) FBA_CMD22	K26	FBA_CMD22	[Rank0:11] [Rank1:18]
(23.24) FBA_CMD23	K22	FBA_CMD23	[Rank0:12] [Rank1:11]
(23.24) FBA_CMD24	L24	FBA_CMD24	[Rank0:12] [Rank1:18]
(23.24) FBA_CMD25	L24	FBA_CMD25	[Rank0:15] [Rank1:16]
(23.24) FBA_CMD26	J25	FBA_CMD26	[Rank0:18] [Rank1:16]
(23) FBA_CMD27	J24	FBA_CMD27	Rank0:18
(23.24) FBA_CMD28	K27	FBA_CMD28	[Rank0:18] [Rank1:15]
(23.24) FBA_CMD29	K25	FBA_CMD29	[Rank0:18] [Rank1:18]
(24) FBA_CMD30	J27	FBA_CMD30	Rank1:18
(24) FBA_CMD31	J26	FBA_CMD31	N/A

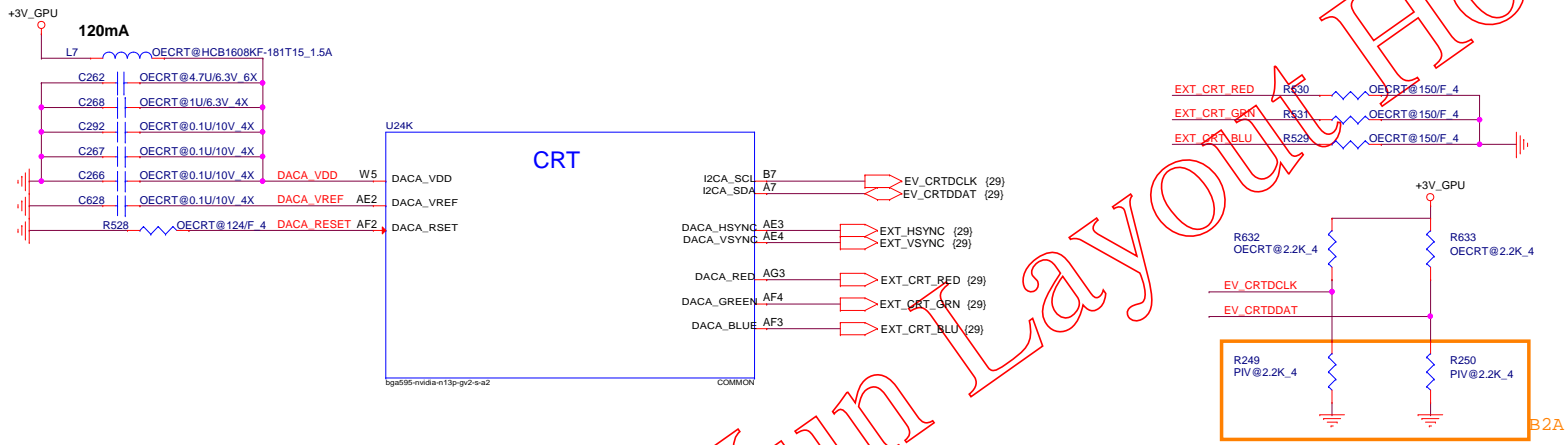
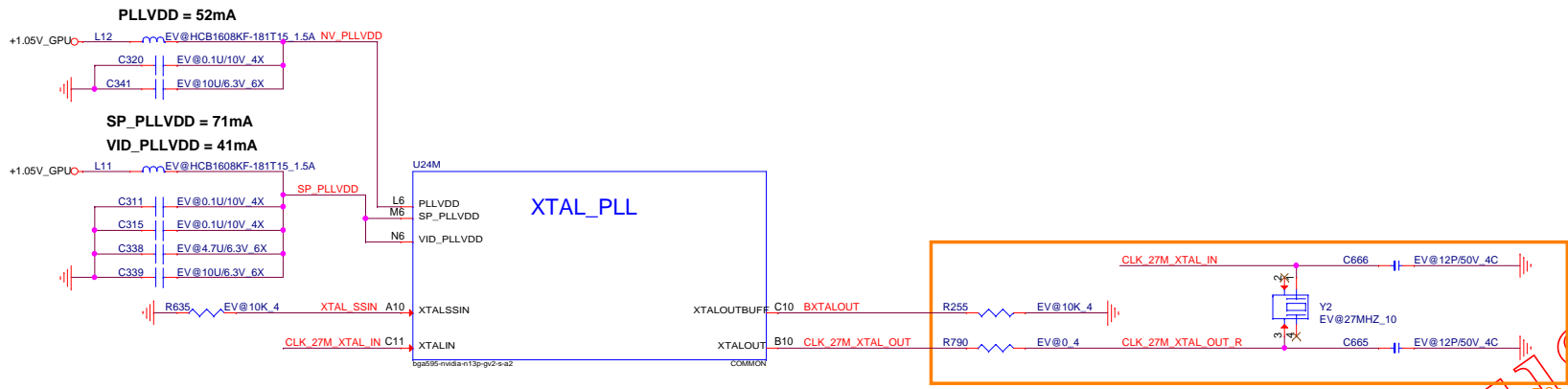


ODT_x, CKEx, RST (Termination)

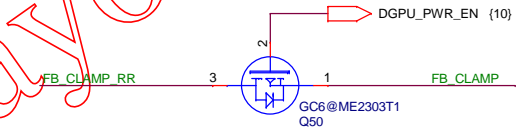
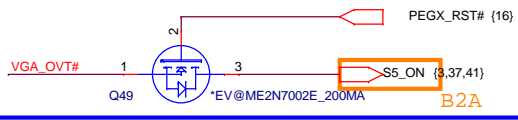
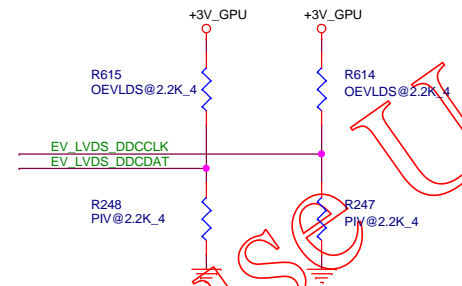
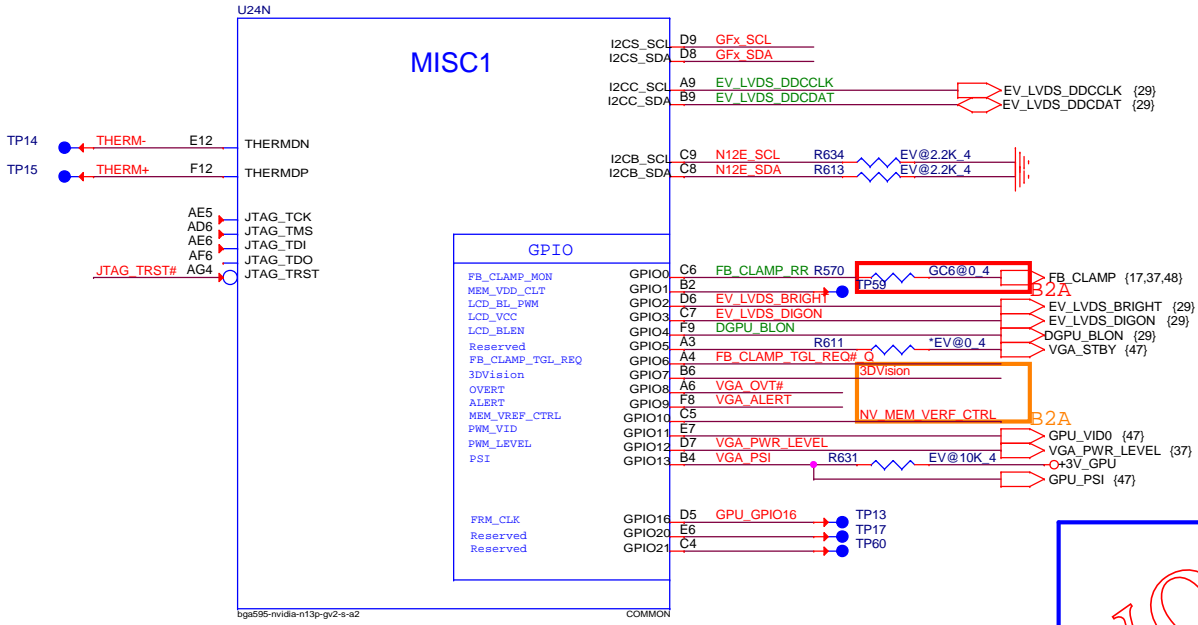




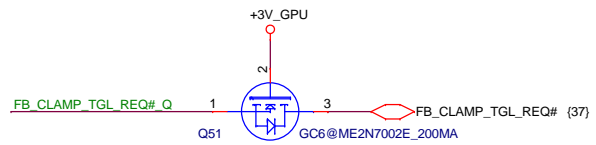
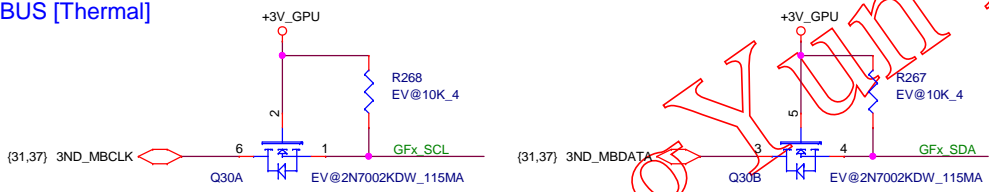
For Xiang Yun Layout House



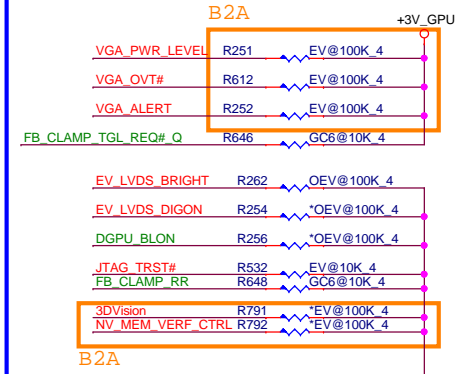
For Xiang Yun Layout House Use



SMBUS [Thermal]



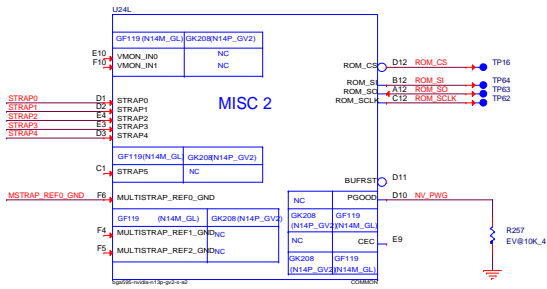
GPIO PU/PD



Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	N14x (GPIO)	A1A
Date:	Wednesday, January 16, 2013	Sheet 20 of 50

For Xiang Yun Layout



MULT STRIP [N14P_GV2]			
PCI_DEVICE STRAP	PCI DEVICE ID 0x1292 ->GS 0x12AD ->ES	DP_PLL_VDD33	1 [Default]
RAM_CFG	RAM_CFG[3:0] for memory configuration	PEX_PLL_EN_TERM	PCIE PLL termination 0:Disable [Default]; 1:Enable
SUB_VENDOR	0:No NVBIOS ROM; 1 BIOS ROM [Default]	3GIO_PADCFG	[0000] -> Gen3 support
FB[1:0]	[1:0] -> 256MB	PCIE_MAX_SPEED	[1] -> Allow boot to PCIE Gen3
VGA_DEVICE	0:3D Device; 1:VGA Device	PCIE_SPEED_CHANG_GEN3	[1] -> Enable Gen3
ICSS_Slave Address	0:9E [Default]; 1:9C	SORx_EXPOSED	SOR0_EXPOSED; SOR1_EXP=1 [BFA:BLVDS]; [BFC:HDM]
USER STRAP	Panel EDID Support		

Strap Pin name	Strapping Bits 3	Strapping Bits 2	Strapping Bits 1	Strapping Bits 0	SETTING	NOTE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM		
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]		
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE		
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]		
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		
STRAP4	RESERVED	PCI_SPEED_CHAN CE_GEN4	PCI_MAX_SPEED	DP_PLL_VDD33V		
4.99K	1000	0000	24.9K	1100	0100	
10K	1001	0001	30.1K	1101	0101	
16K	1010	0010	34.8K	1110	0110	
20K	1011	0011	45.3K	1111	0111	
Resistor Value	VDD33	GND	Resistor Value	VDD33	GND	

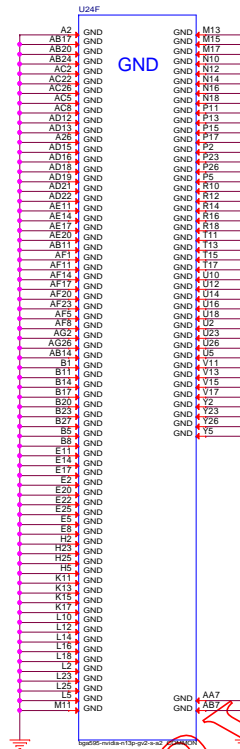
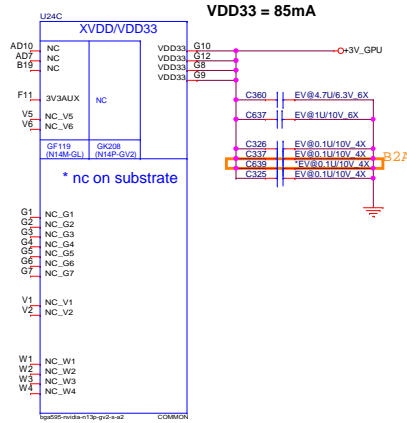
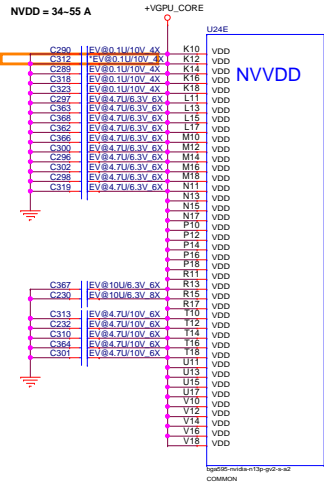
N14P_GV2	H1/H2	S1/S2	M1/M2	S3	M3
ROM_SI	33.8K	45.3K	30.1K	20K	10K
ROM_SCLK	CS33482FB22	CS34532FB18	CS33012FB18	CS32002FB29	CS31002FB26

Binary Strap [N14M_GL]			
Strap Pin name	Strap Mapping	Polarity	SETTING
ROM_SCLK	SMB_ALT_ADDR	Pull-down to GND	
ROM_SI	SUB_VENDOR	Pull-up to 3V3 if BIOS ROM exists Pull-down to GND if no VBIOS ROM	
ROM_SO	VGA_DEVICE	Pull-down to GND (no display)	
STRAP0	RAMCFG[0]	USER defined	
STRAP1	RAMCFG[1]	USER defined	
STRAP2	RAMCFG[2]	USER defined	
STRAP3	RAMCFG[3]	USER defined	
STRAP4	PCI_MAX_SPEED	Pull-down to GND	

N14M_GL	Strap3	Strap2	Strap1	Strap0
H1	D0	C1	B1	A0
H2	D0	C1	B1	A0
H3	D0	C0	B1	A1
H4	D0	C1	B0	A0
S1	D0	C1	B0	A1
S2	D0	C1	B0	A1
S3	D1	C0	B1	A1
M1	D0	C0	B0	A1
M2	D0	C0	B0	A1
M3	D1	C1	B0	A1

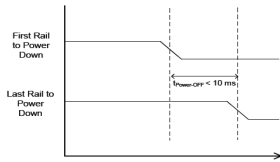
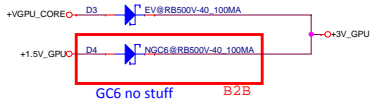
		Vendor P/N	STN B/S P/N	Size	Strap	Note	
128M (2G bit)	Hynix H2	H5TQ2G63DFR-N0C (128M*16) GL/GV2		x4+1GB	GL:0x06 0110	GV2:0x06 0110	1000MHz
				x8+2GB		GV2:0x06 0110	1000MHz
		H5TQ2G63DFR-11C (128M*16) GL/GV2		x4+1GB	GL:0x06 0110	GV2:0x06 0110	900MHz
			x8+2GB		GV2:0x06 0110	900MHz	
	Samsung S2	K4W2G1646E-BC1A (128M*16) GL/GV2		x4+1GB	GL:0x05 0101	GV2:0x07 0111	1000MHz
				x8+2GB		GV2:0x07 0111	1000MHz
Micron M2	MT41J128M16JT-107G:K (128M*16) GL/GV2		x4+1GB	GL:0x01 0001	GV2:0x05 0101	900MHz	
			x8+2GB		GV2:0x05 0101	900MHz	
	MT41J128M16JT-093G:K (128M*16) GL/GV2		x4+1GB	GL:0x01 0001	GV2:0x05 0101	1000MHz	
			x8+2GB		GV2:0x05 0101	1000MHz	
256M (4Gbit)	Micron M3	MT41K256M16HA-107D:E (256M*16) GL/GV2		x4+2GB	GL:0x0D 1101	GV2:0x01 0001	900MHz
				x8+4GB		GV2:0x01 0001	900MHz
	Samsung S3	K4W4G1646B-HC11 (256M*16) GL/GV2		x4+2GB	GL:0x0B 1011	GV2:0x03 0011	900MHz
				x8+4GB		GV2:0x03 0011	900MHz
Hynix H4	H5TQ4G63MFR-11C (256M*16) GL		x4+2GB	GL:0x04 0110	GV2:0x03 0110	900MHz	
			x4+2GB		GV2:0x03 0110	900MHz	
				N/A			
				N/A			

FOR HANDBOOK

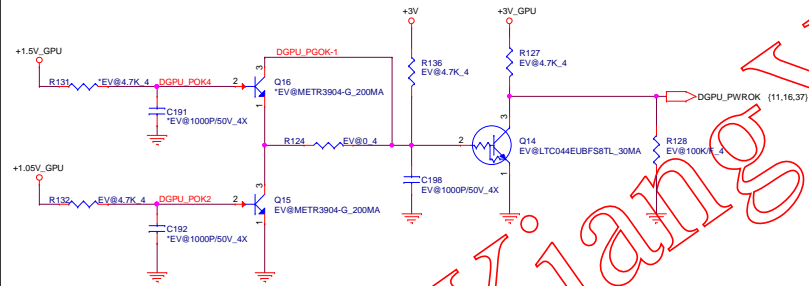
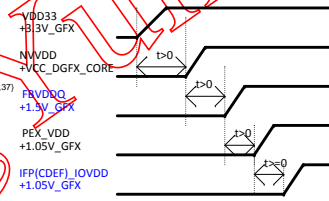


Power down sequence

for meet Power down sequence for +3V_GFX



Power up sequence



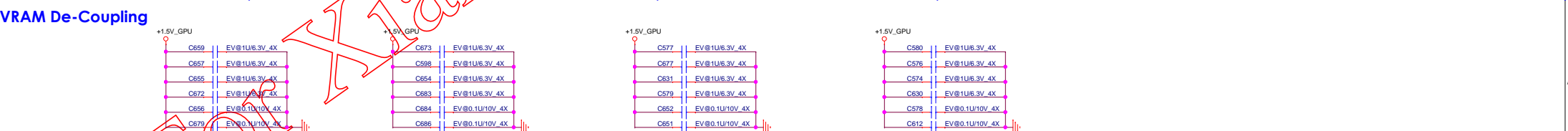
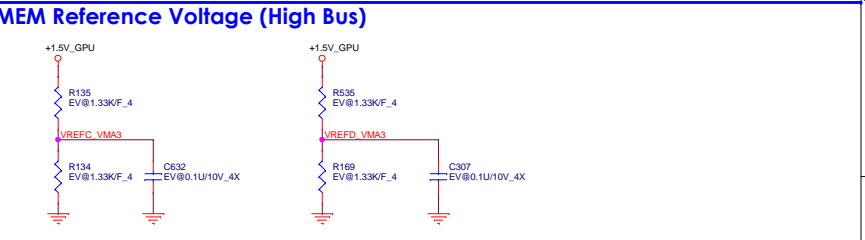
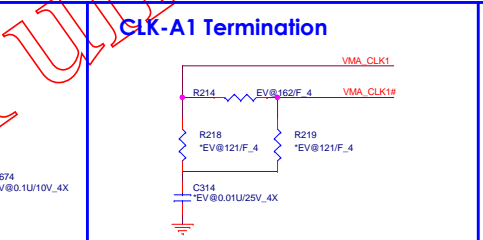
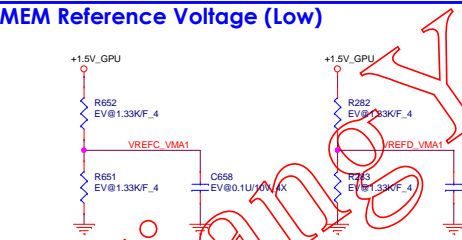
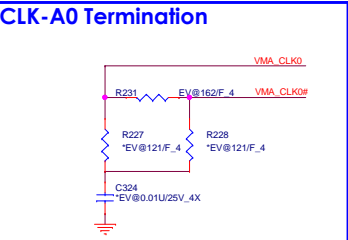
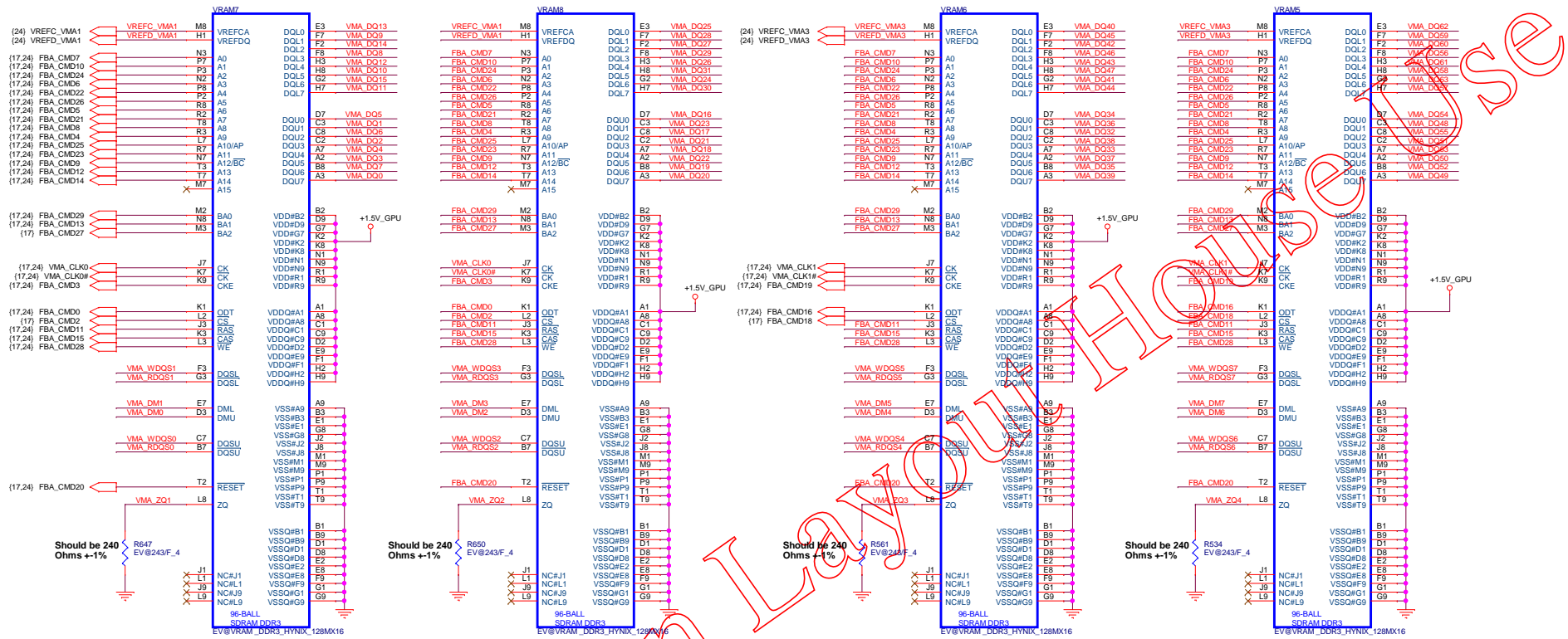
For Xiang Jun Layout House Use

RANK0: 256MB/512MB DDR3

(17.24) VMA_DM[6:3..0]
(17.24) VMA_DM7..0
(17.24) VMA_WDQS[7..0]
(17.24) VMA_WDQS7..0

DataBus [0:31]

DataBus [64:32]



Quanta Computer Inc.
PROJECT : Chief River

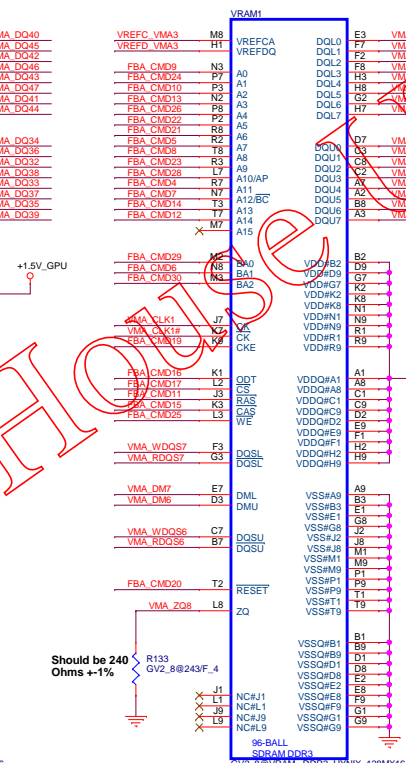
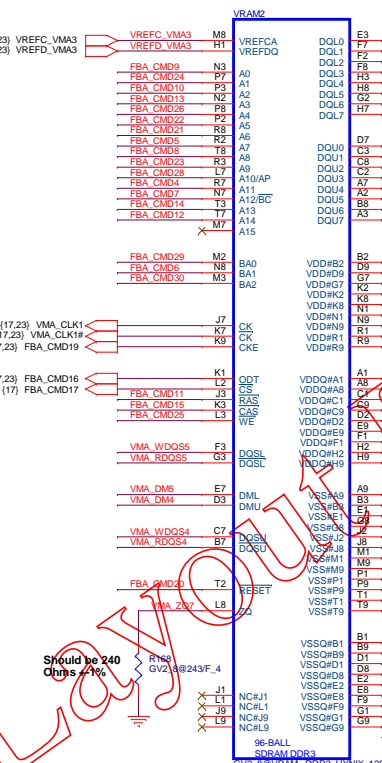
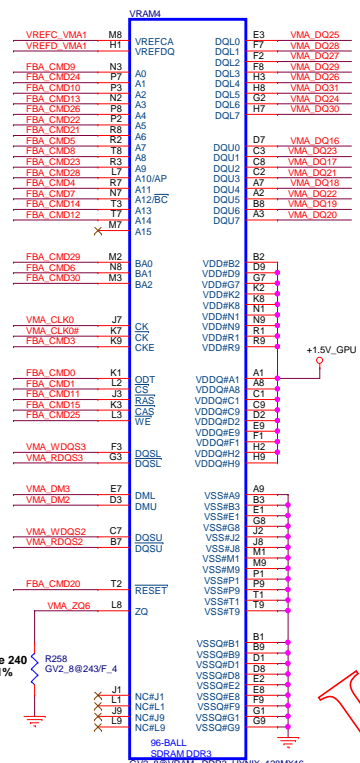
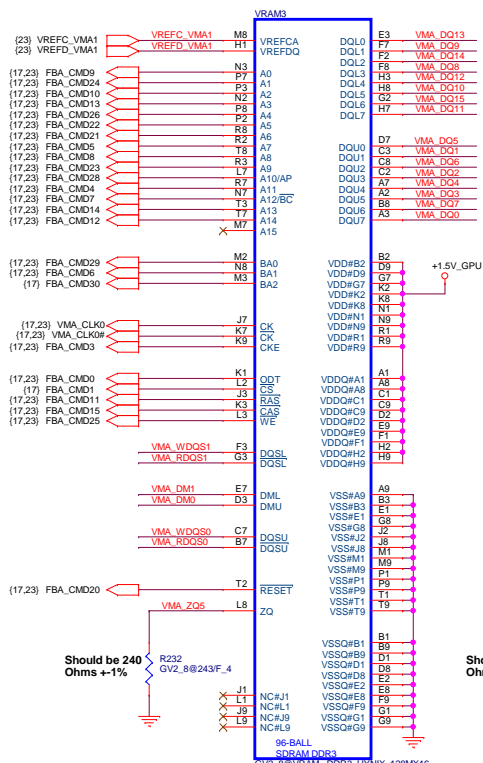
Size	Document Number	Rev
	N14x (DDR/Rank0)	A1A
Date:	Wednesday, January 16, 2013	Sheet 23 of 50

(17.23) VMA_DM7[3..0]
(17.23) VMA_DM7[3..0]
(17.23) VMA_DM7[3..0]
(17.23) VMA_DM7[3..0]

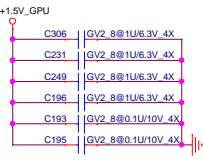
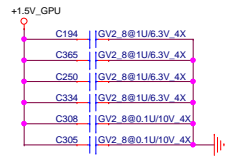
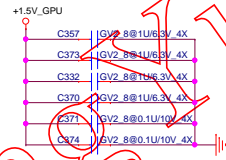
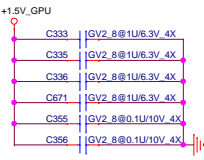
RANK1: 256MB/512MB DDR3

DataBus [0:31]

DataBus [64:32]




VRAM De-Coupling



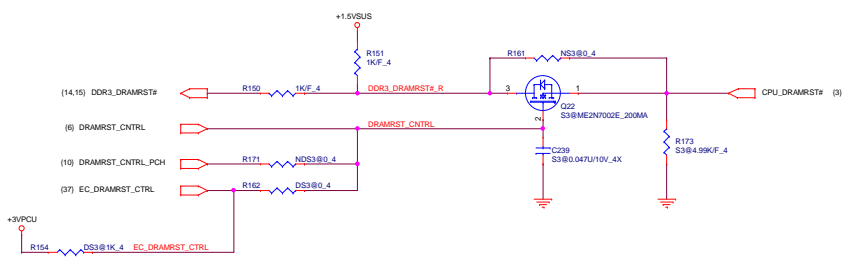
For Xiang's Fun Layout

For Xiang Yun Layout House Use

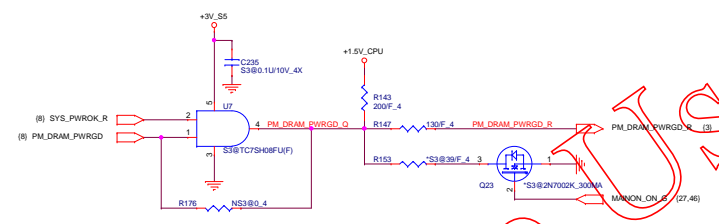
For Xiang Yun Layout House Use

		Quanta Computer Inc.
		PROJECT : Chief River
Size	Document Number	Rev
	VRAM A: DDR3*4PCS	A1A
Date: Wednesday, January 16, 2013		Sheet 26 of 50

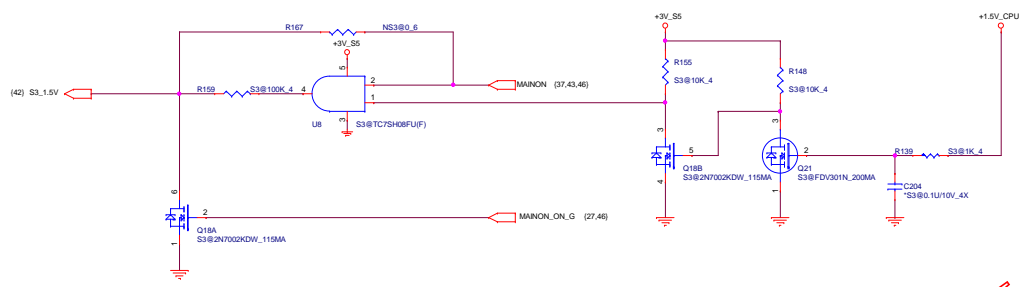
S3 power Reduction (SM_DRAMRST#) <S3P>



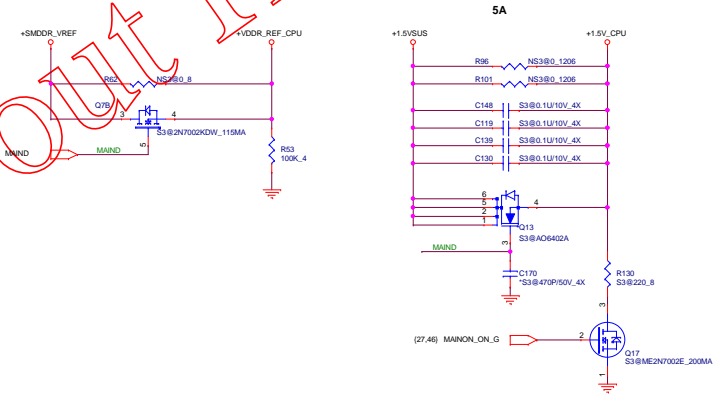
S3 power Reduction (SM_DRAMPWROK) <S3P>



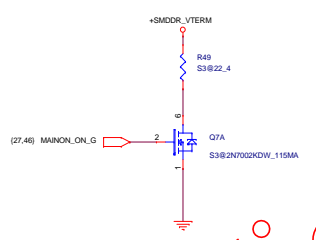
For S3 power Reduction Sequence <S3P>



S3 power Reduction (CPU Power) <S3P>

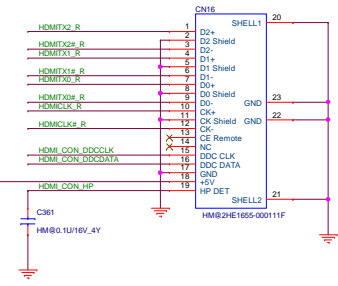
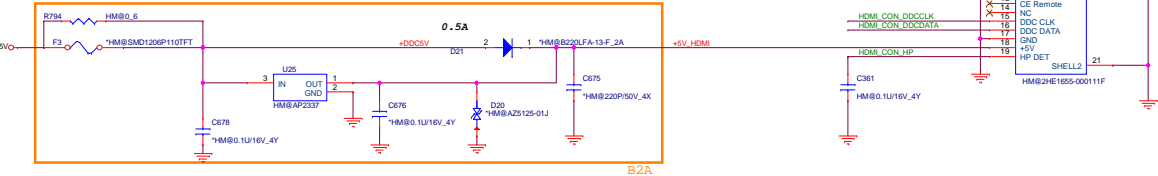
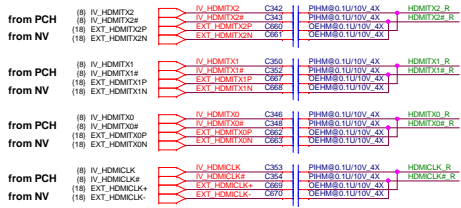


For S3 power Reduction VTT discharge <S3P>

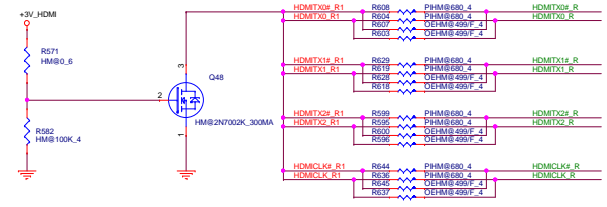


For Xiang Yun Layout House Use

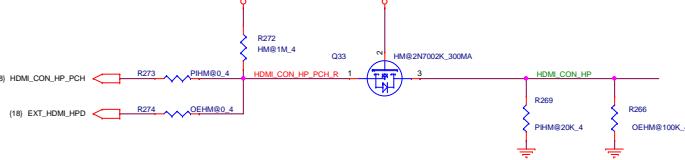
HDMI Conn <HDM>



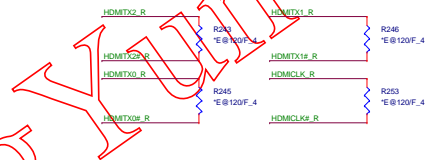
HDMI-passive level shift <HMP/HMG>



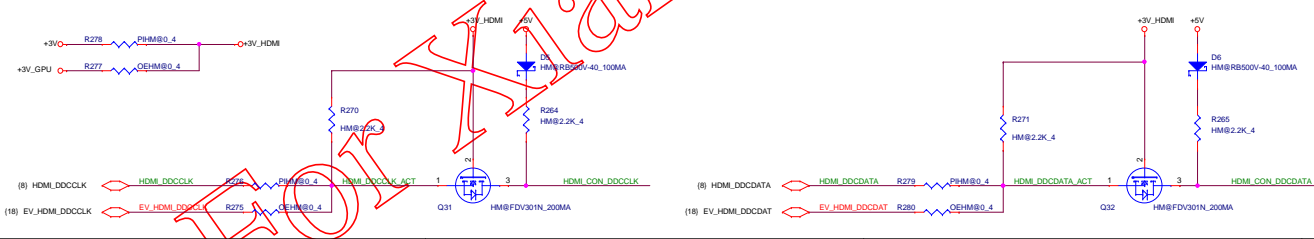
HDMI-HPD <HMP/HMG>



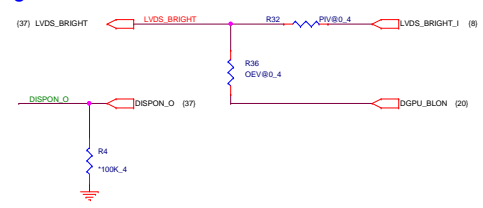
FOR EMI <EMC>



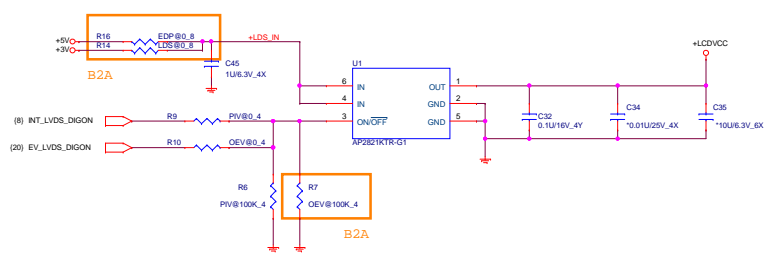
HDMI-SMBus <HDM>



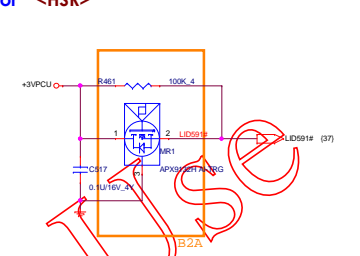
Panel backlight control <LDS>



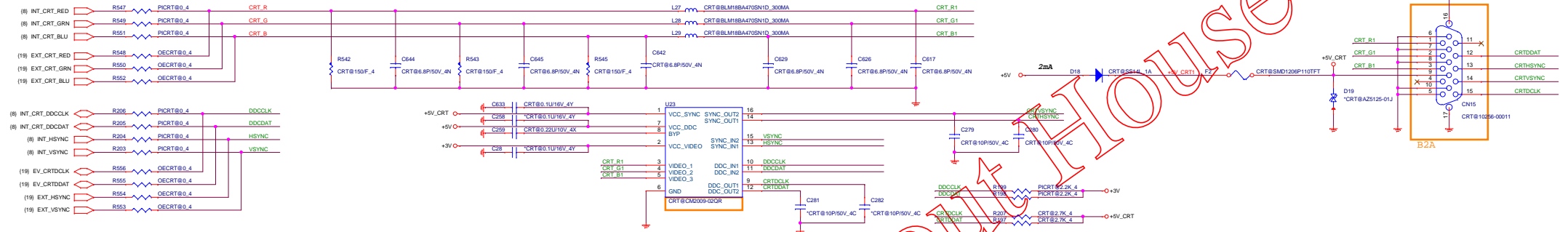
LCD POWER SWITCH <LDS>



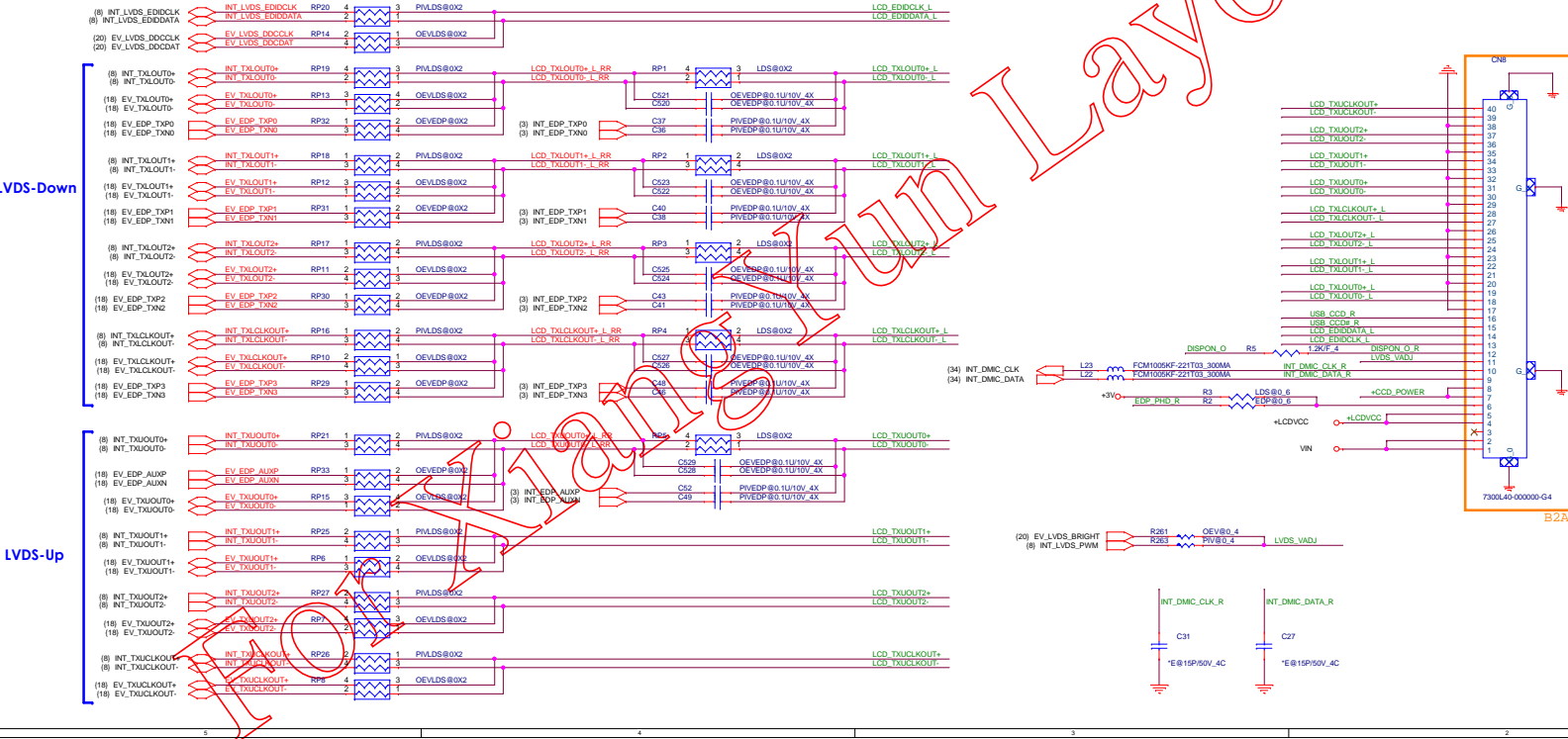
HALL Sensor <HSR>



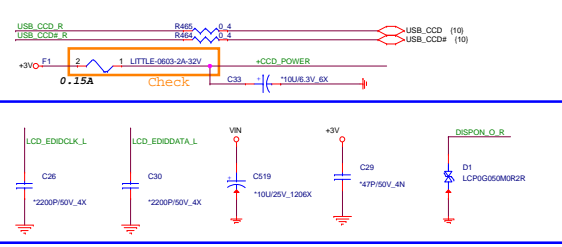
CRT <CRT>



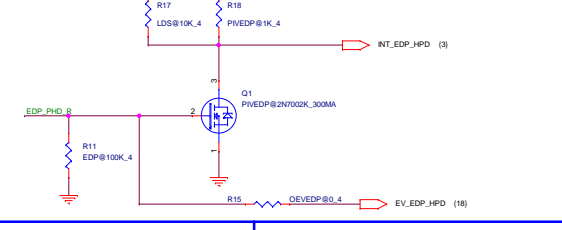
LCD Panel Module <LDS>



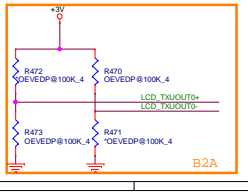
CCD <CCD>



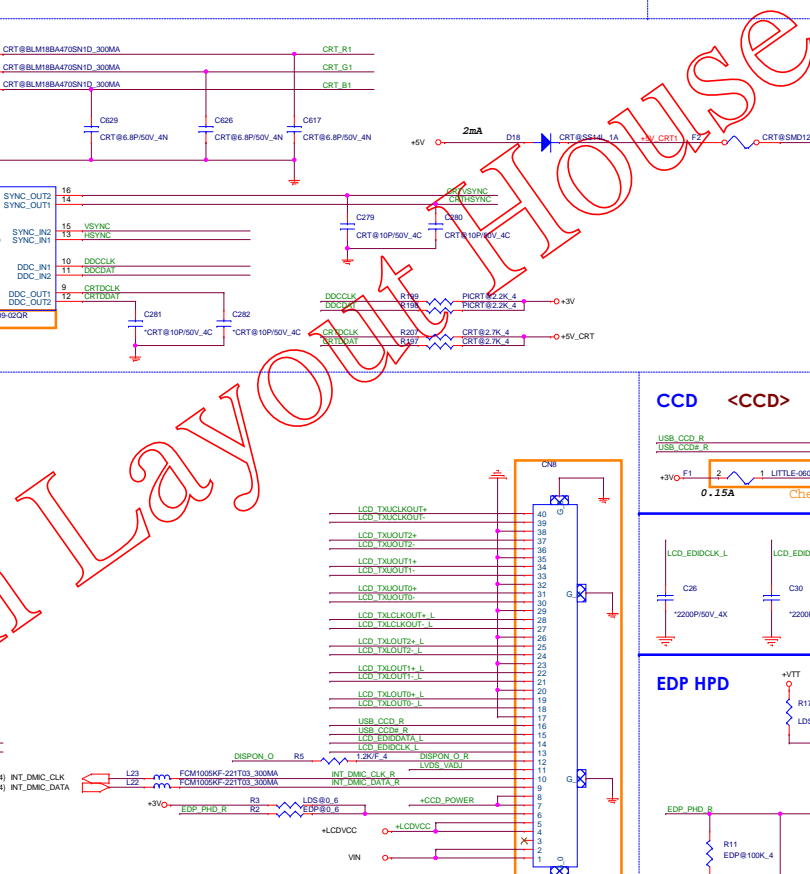
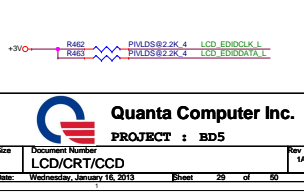
EDP HPD

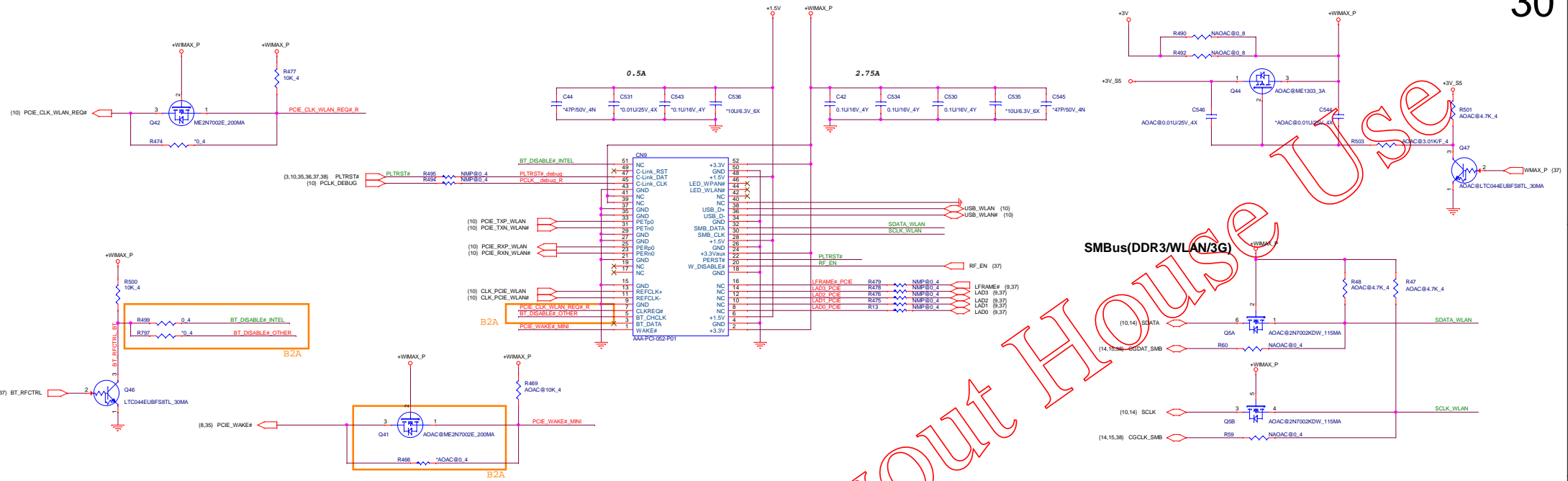


EDP PU/PD

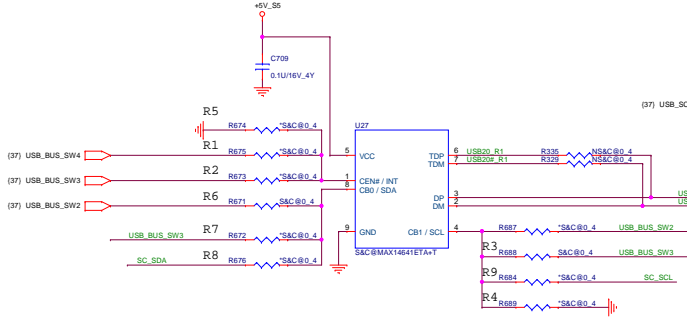
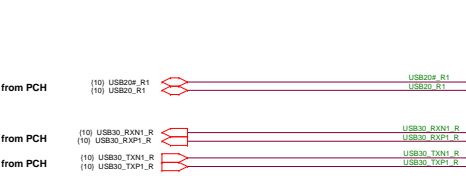


SMBus





USB CONNECT RIGHT1 <U3B> <USB>



	R1	R2	R3	R4	R5	R6	R7	R8	R9
14566		V	V	V					
14600		V	V	V	V				
14617 (with CB2)	V	V	V	V					
14617 (no CB2)				V	V	V			
14641/14642/14644			V	V		V	V		
14640							V	V	

SW2	SW3	14600	Status
0	0	0	Auto mode
0	1	0	Force dedicated charger mode
1	0	0	Pass-Through(USB) mode
1	1	0	pass-through(USB) with CDP Emulation

Charger, AM
Charger, FM
USB, PM
USB, CM

SW2	SW3	14644	Status
0	0	0	2A Auto mode for Apple device
0	1	0	Force dedicated charger mode
1	0	1	Pass-Through(USB) mode
1	1	1	pass-through(USB) with CDP Emulation

Charger, AM2
Charger, FM2
USB, PM
USB, CM

SW2	SW3	14641	Status
0	0	0	2A Auto mode for Apple device
0	1	0	Force 1A for Apple device
1	0	1	Pass-Through(USB) mode
1	1	1	pass-through(USB) with CDP Emulation

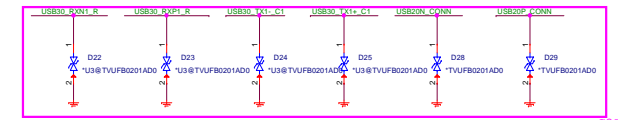
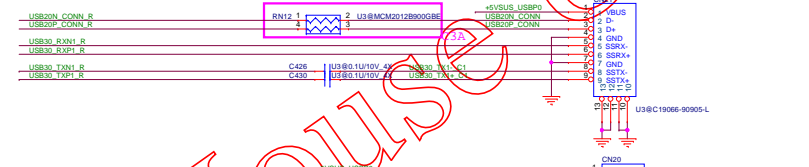
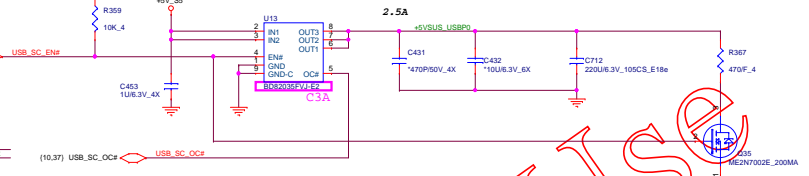
Charger, AM2
Charger, AP1
USB, PM
USB, CM

SW2	SW3	14642	Status
0	0	0	2A Auto mode for Apple device
X	0	1	Pass-through(USB) mode
1	1	1	pass-through(USB) with CDP Emulation

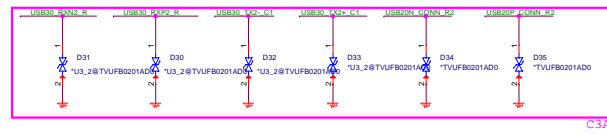
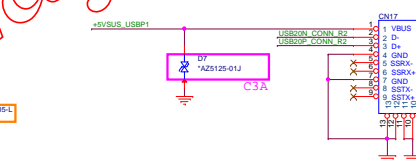
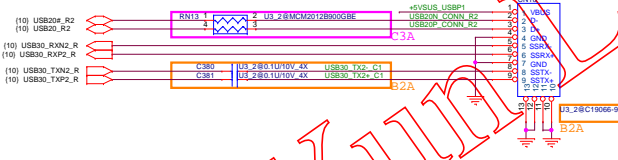
Charger, AM2
USB, PM
USB, CM

2012 Chief River/Brazos

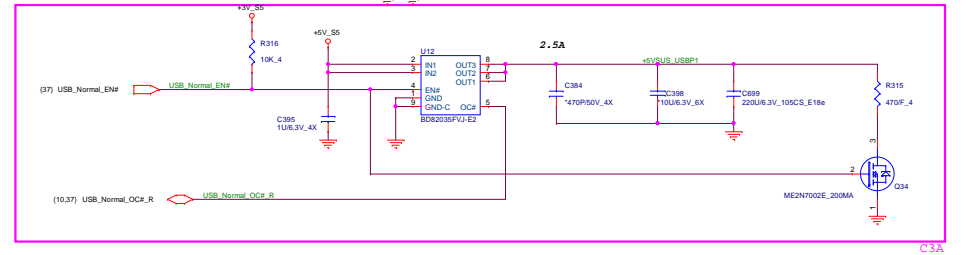
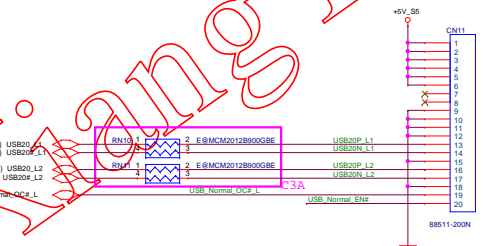
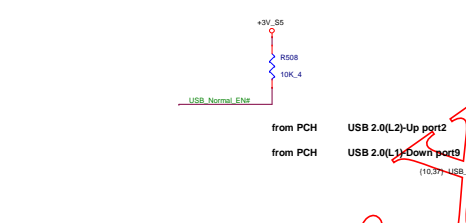
2013 Shark bay / Kabini



USB CONNECT Right2 <U3B>

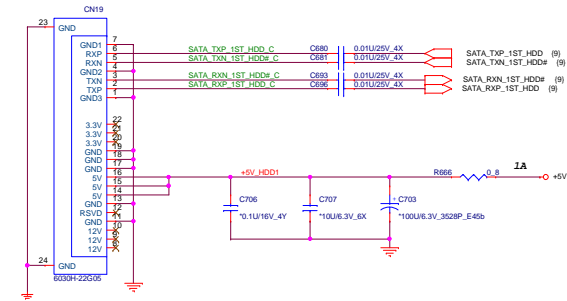


USB CONNECT Left1/Left2 <U2B>

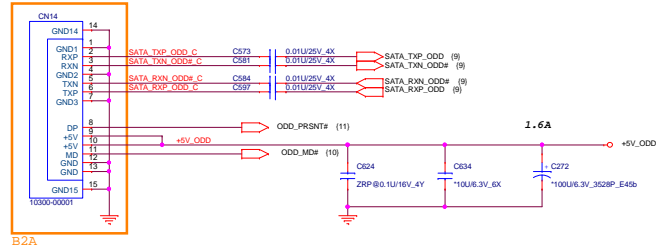


For Xiang Yun Layout House Use

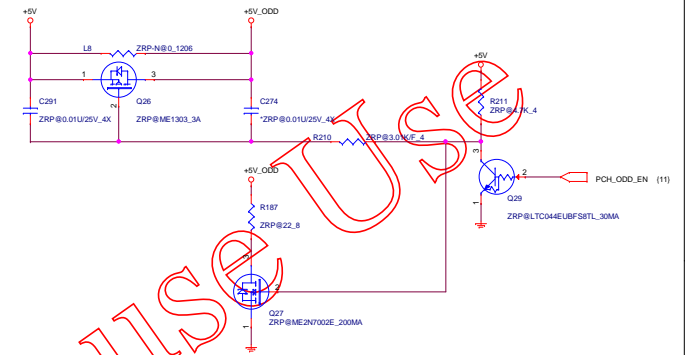
SATA HDD <HDD>



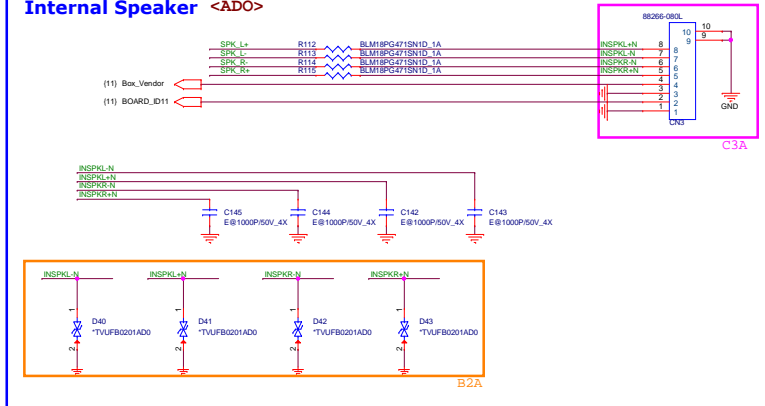
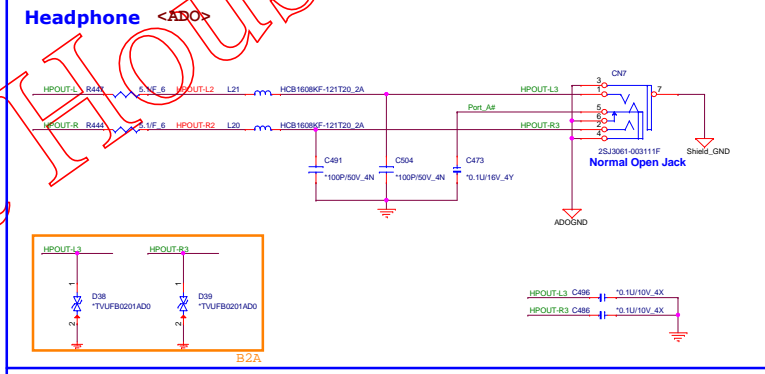
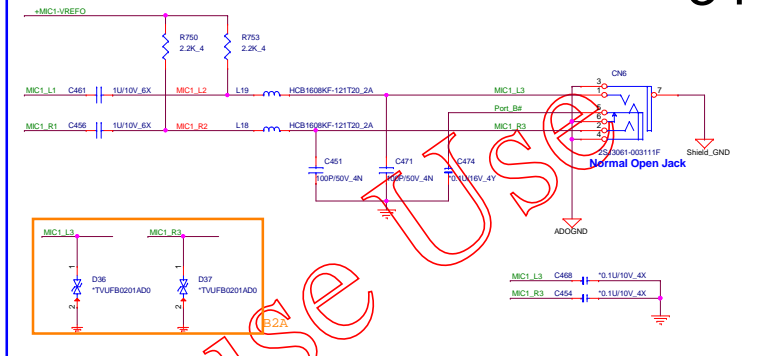
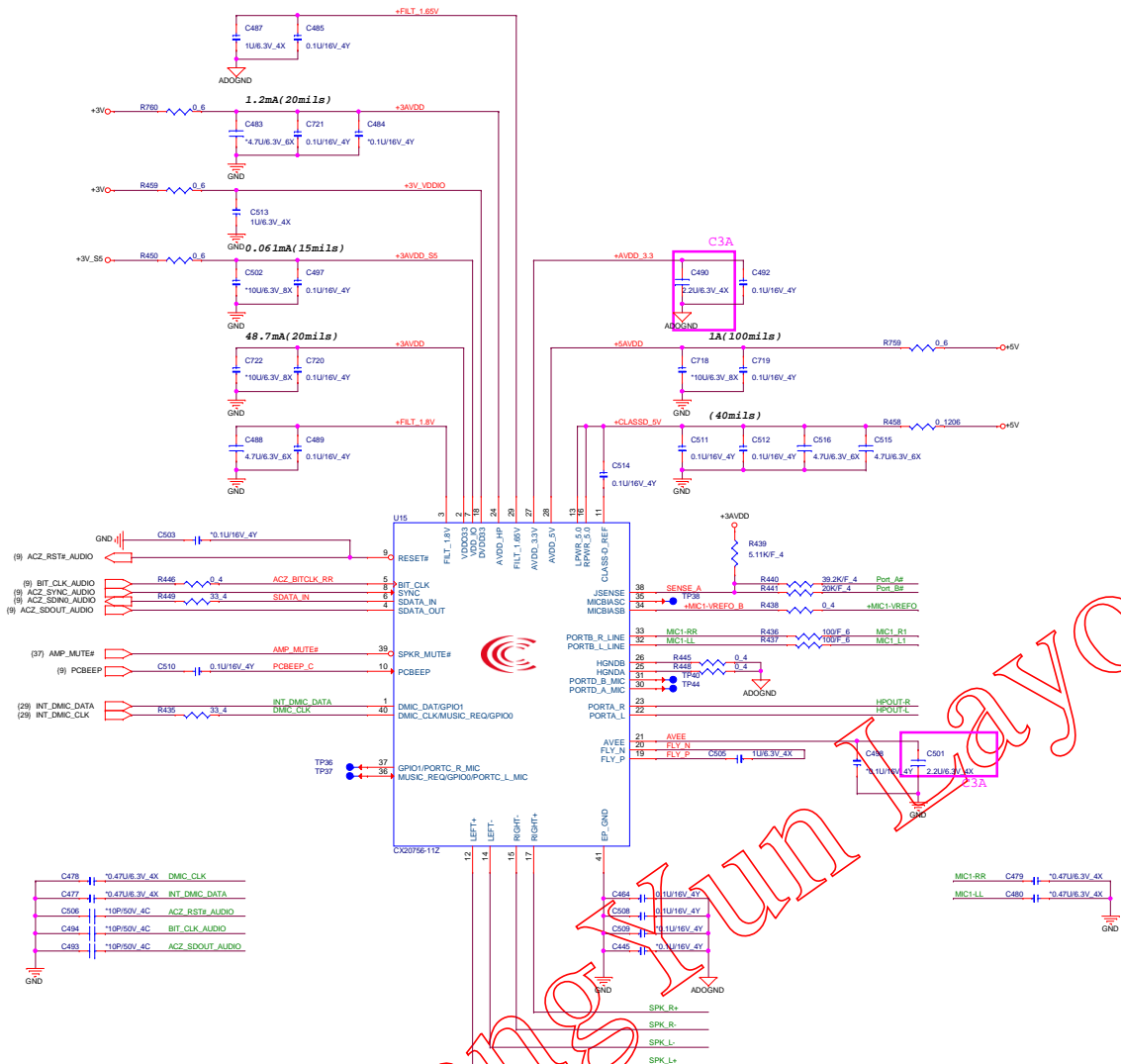
SATA ODD <ODD>



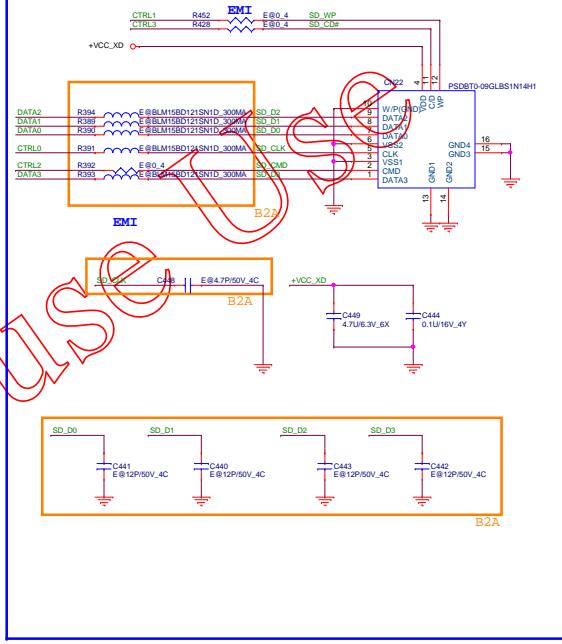
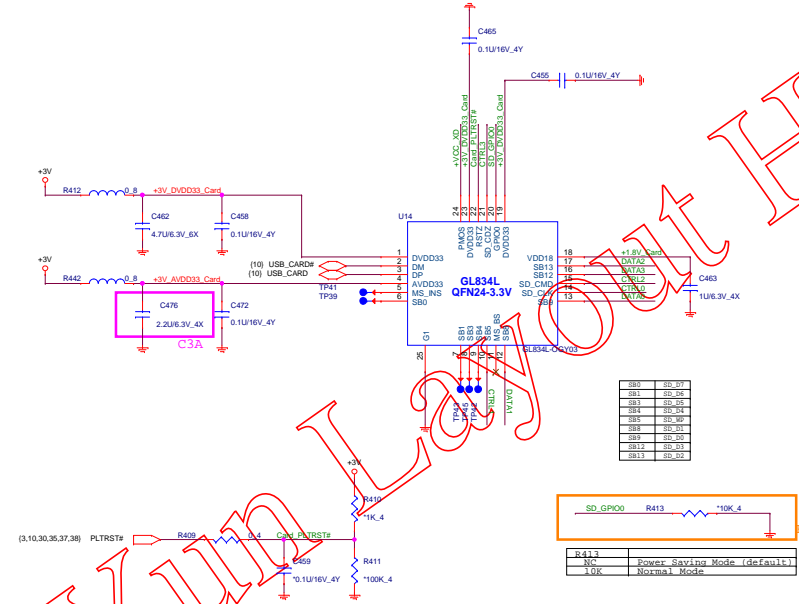
Odd Zero power . (Only for Intel) <OZP>



For Xiang Yun Layout House Use

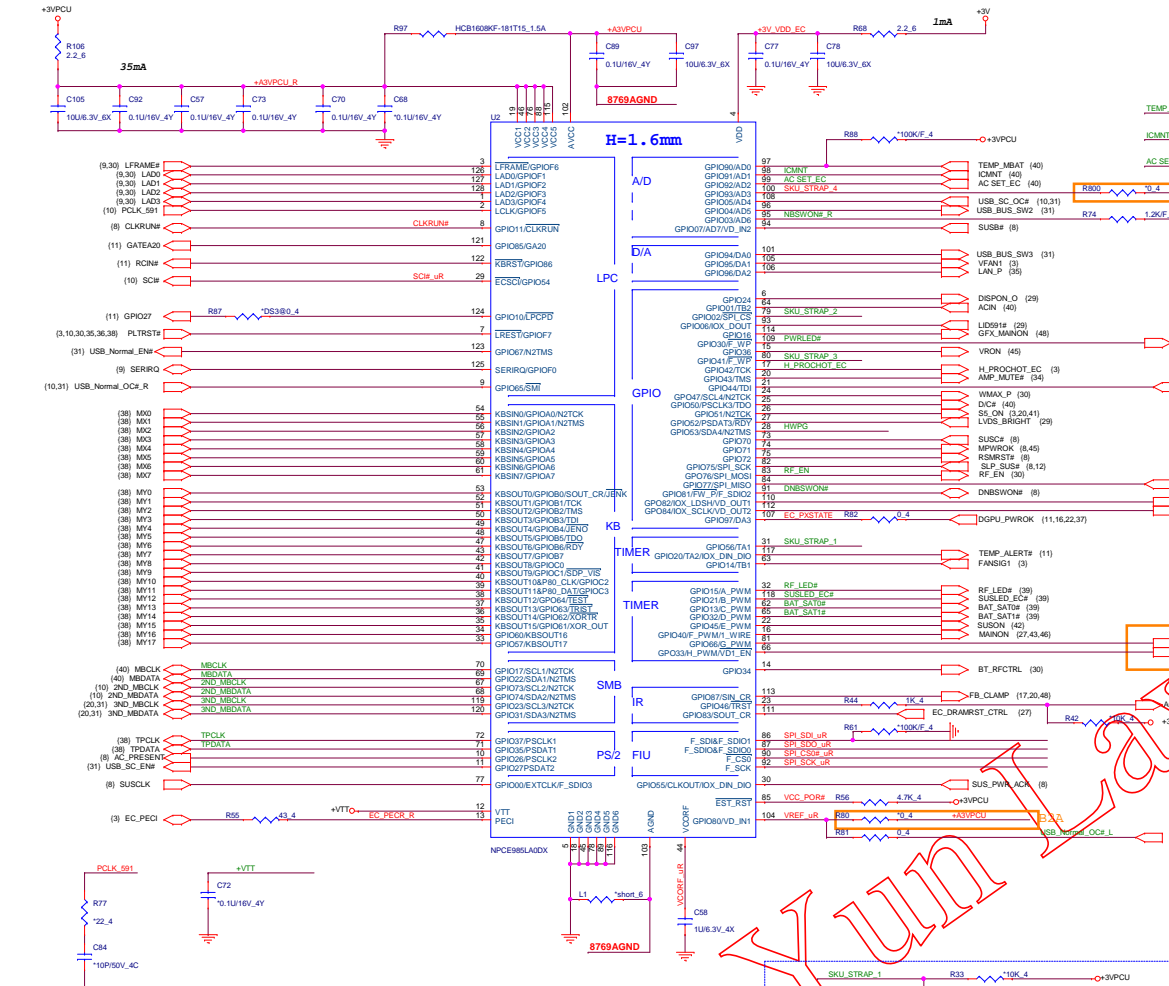


Card Reader (GL834L) <MMC>

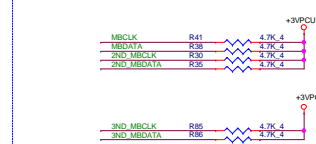


For Xiang Yun Layout House

EC <KBC>

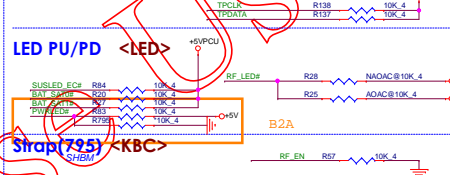


SM BUS PU/Address <KBC>



SMBUS Devices	Address
1 Battery(A)	
2 PCH(S)	
G-sensort(S0)	
IDROM(A)	
VGA Thermal(S0)	
CEC(A)	

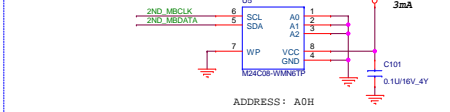
TP <KBC>



INTERNAL KEYBOARD STRIP SET <KBC>



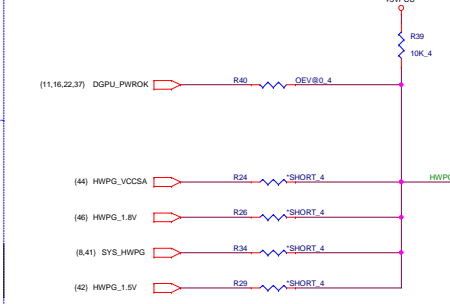
ID EEPROM <KBC>



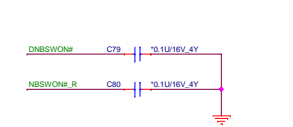
SPI FLASH <KBC>



HWPG circuit <KBC>

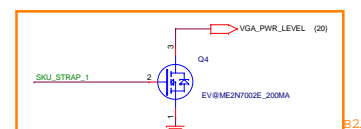


Power Button <KBC>



MS Strap	SKU_STRAP_2	SKU_STRAP_3
14" Capetown UMA	1	0
14" Capetown DIS	1	1
17" Aswan UMA	0	0
17" Aswan DIS	0	1

SKU_STRAP_4
H Shark Bay
L Chief River



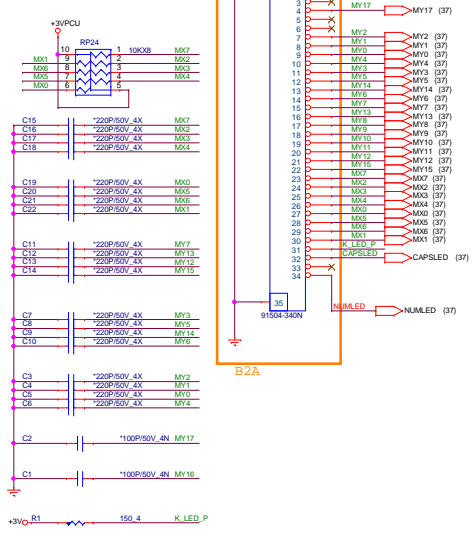
FOR Xiangyun Layout House

Quanta Computer Inc.
PROJECT : BD5

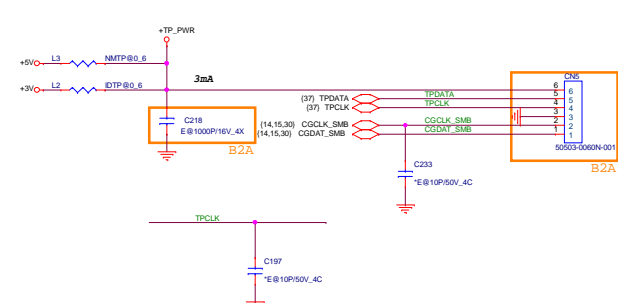
Doc: _____ Document Number
EC-NPCE795L

Date: Wednesday, January 16, 2013 Sheet 37 of 60

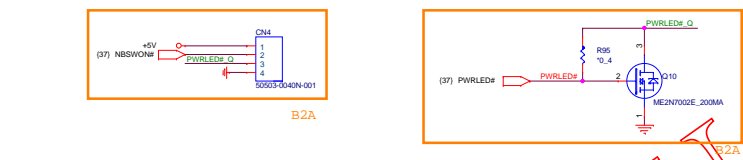
INT Keyboard <KBC>



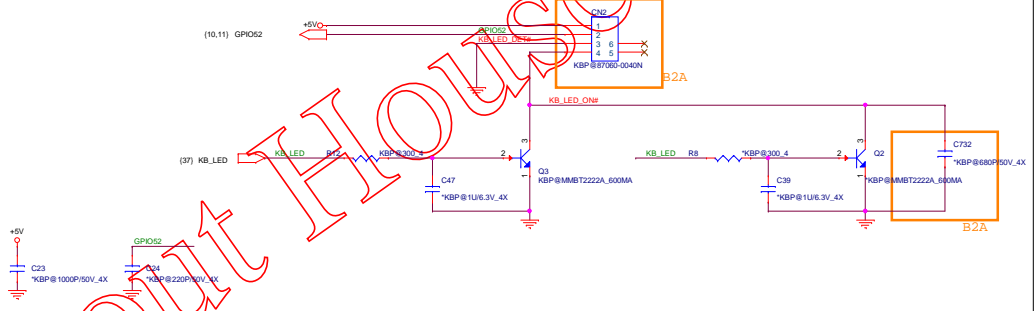
TP board <TPD>



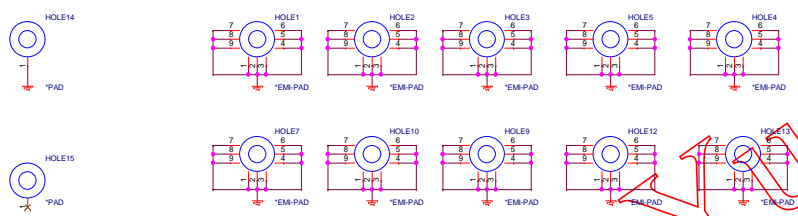
Power board w LED <PSW>



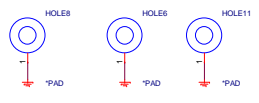
K/B LED power <KBP>



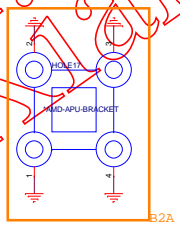
HOLE



VGA HOLE



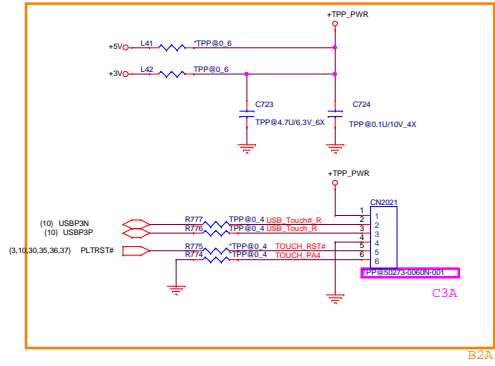
CPU HOLE



MINI Card NUT

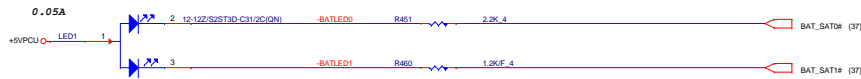


TOUCH PANEL <TPP>

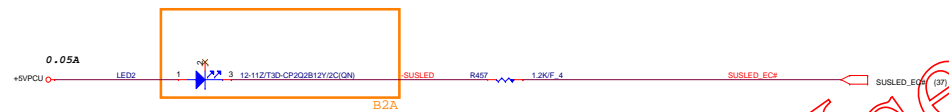


FOR HANG FUN Layout House USE

LED-Battery <LED><W+A>



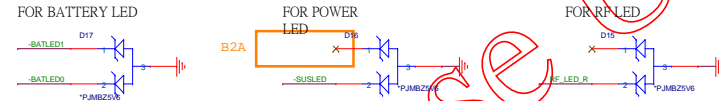
LED-Power <LED><W+A>



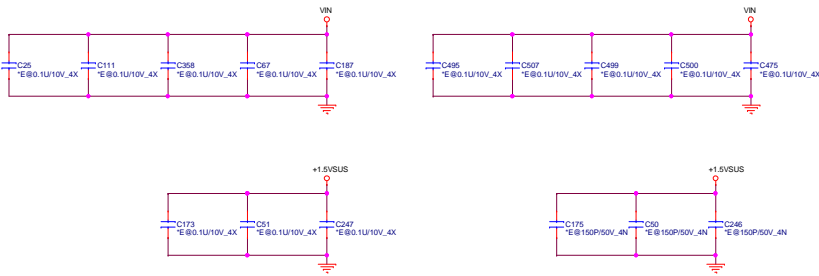
LED-Wifi <LED>



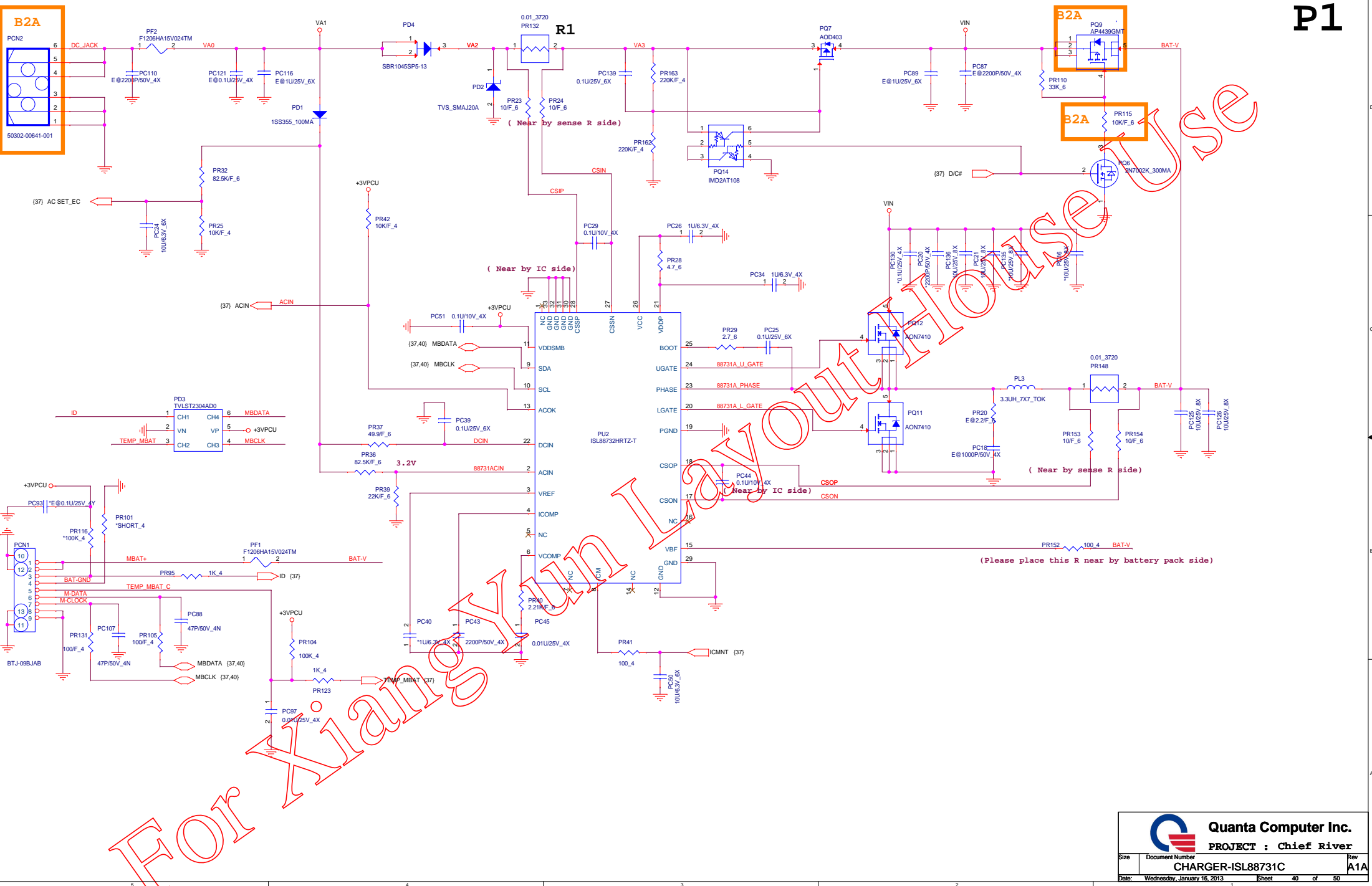
ESD Protect <EMC>



EMI

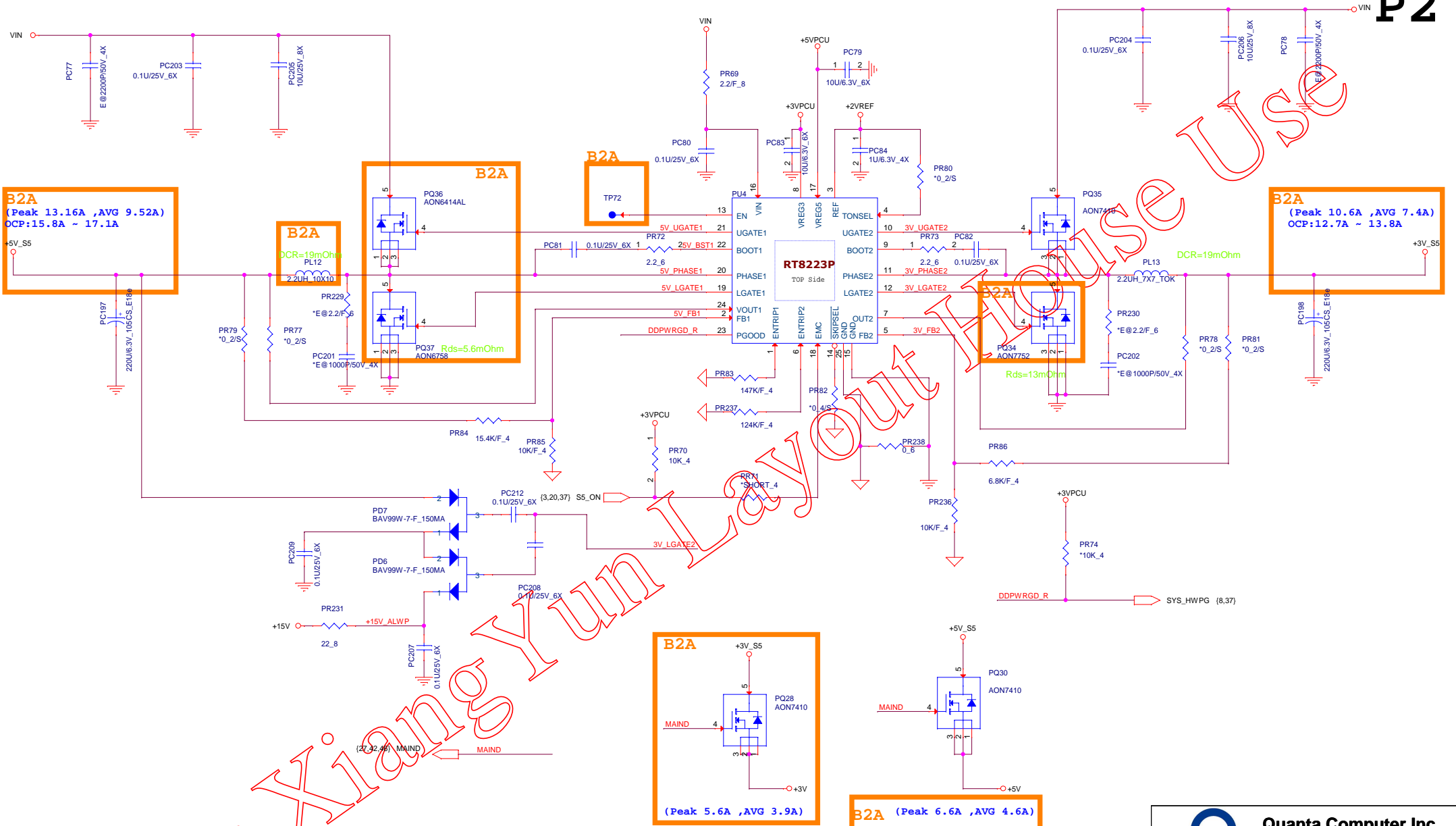


For Xiang Yun Layout House Use




FOR Xiangyun

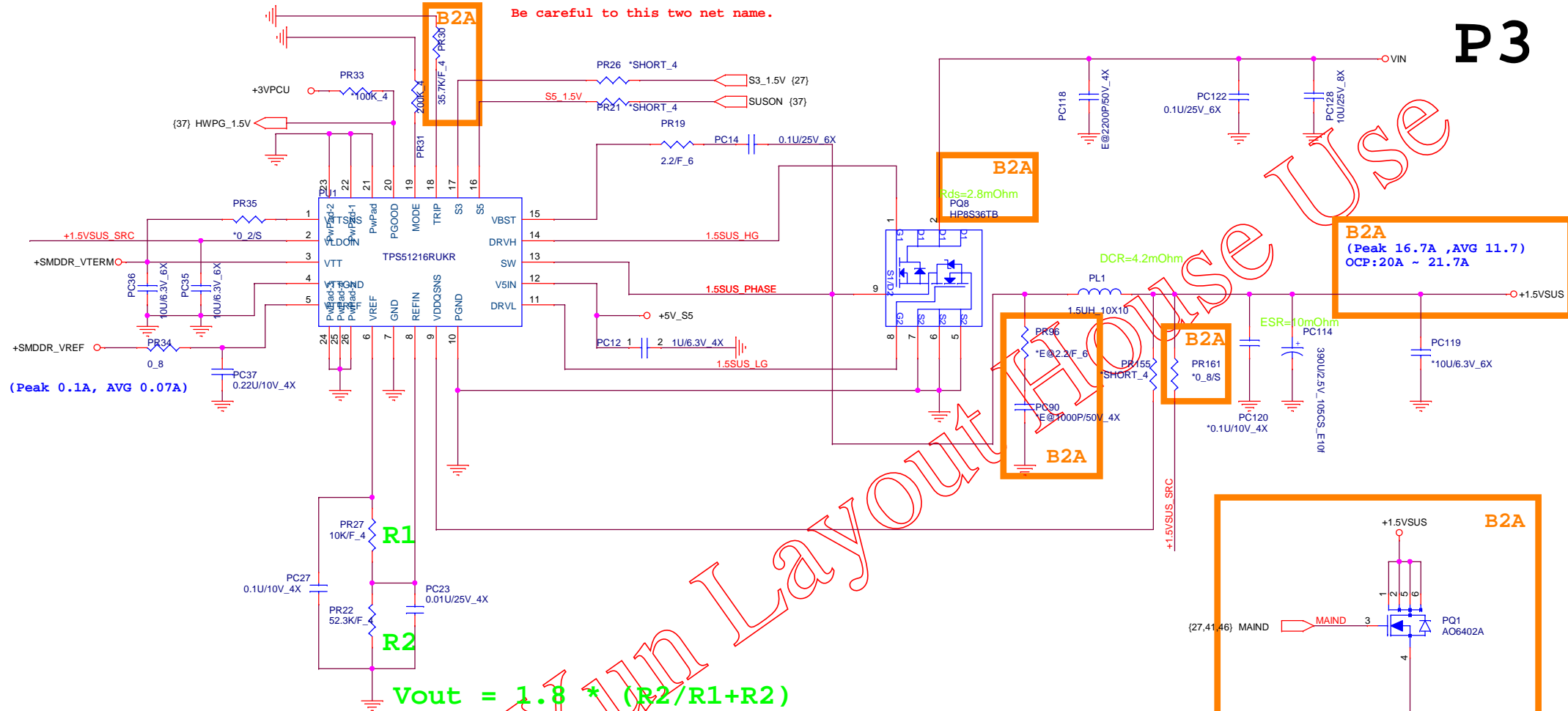
For Xiangyun



For Xiang Yun Layout House USE

 Quanta Computer Inc. PROJECT : Chief River		
Size	Document Number	Rev
	System 3V/5V(TPS51123A)	A1A
Date:	Wednesday, January 16, 2013	Sheet 41 of 50

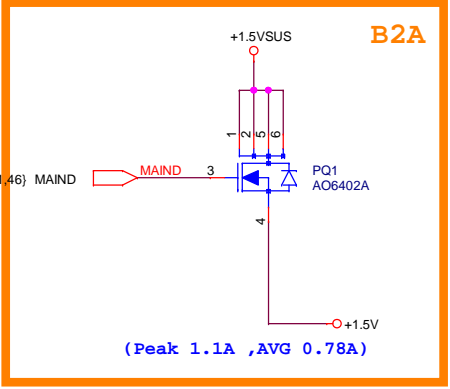
Be careful to this two net name.



(Peak 0.1A, AVG 0.07A)

$$V_{out} = 1.8 * (R2/R1+R2)$$

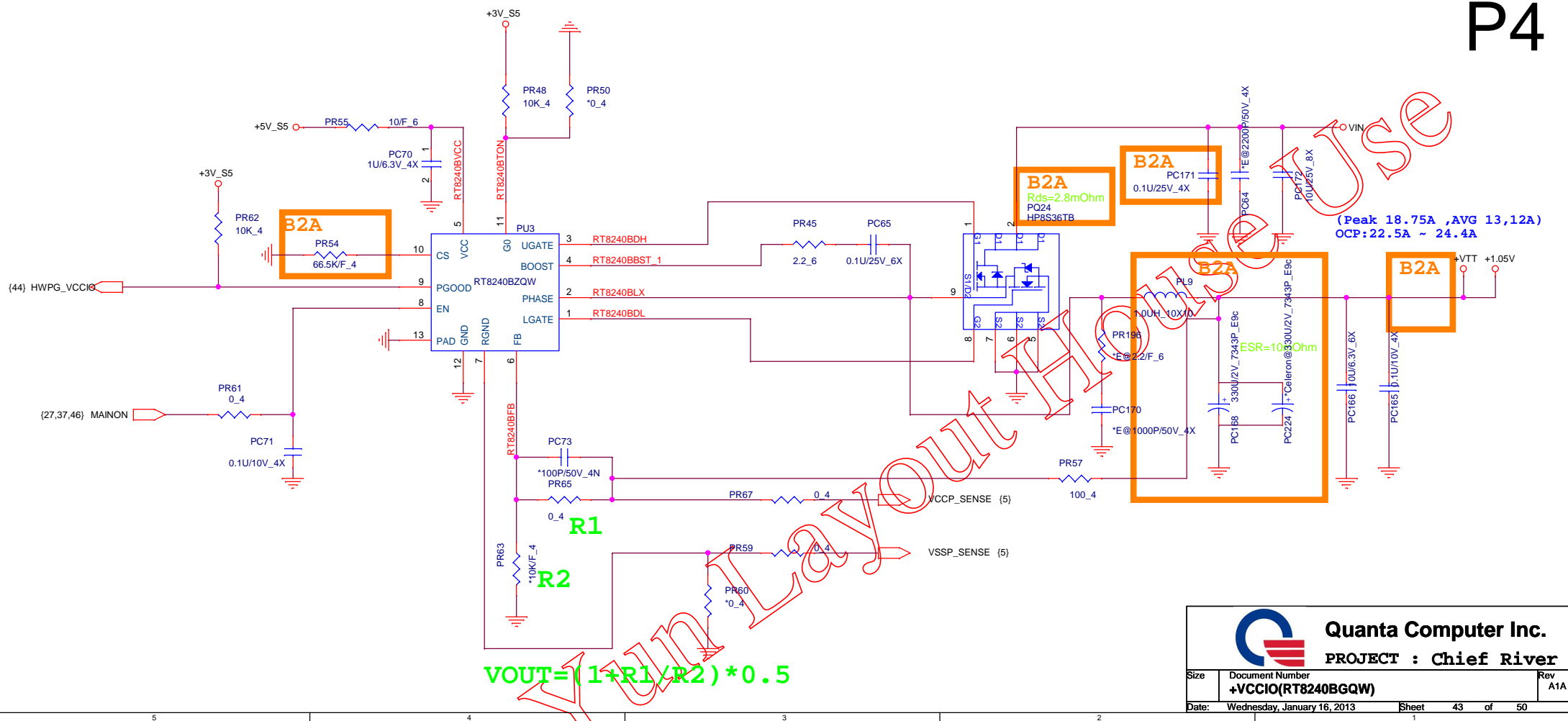
B2A
 (Peak 16.7A ,AVG 11.7)
 OCP:20A ~ 21.7A



Quanta Computer Inc.
 PROJECT : Chief River

Size	Document Number	Rev
	DDR1.5V	A1A
Date:	Wednesday, January 16, 2013	Sheet 42 of 50

For Xiang Yun Layout

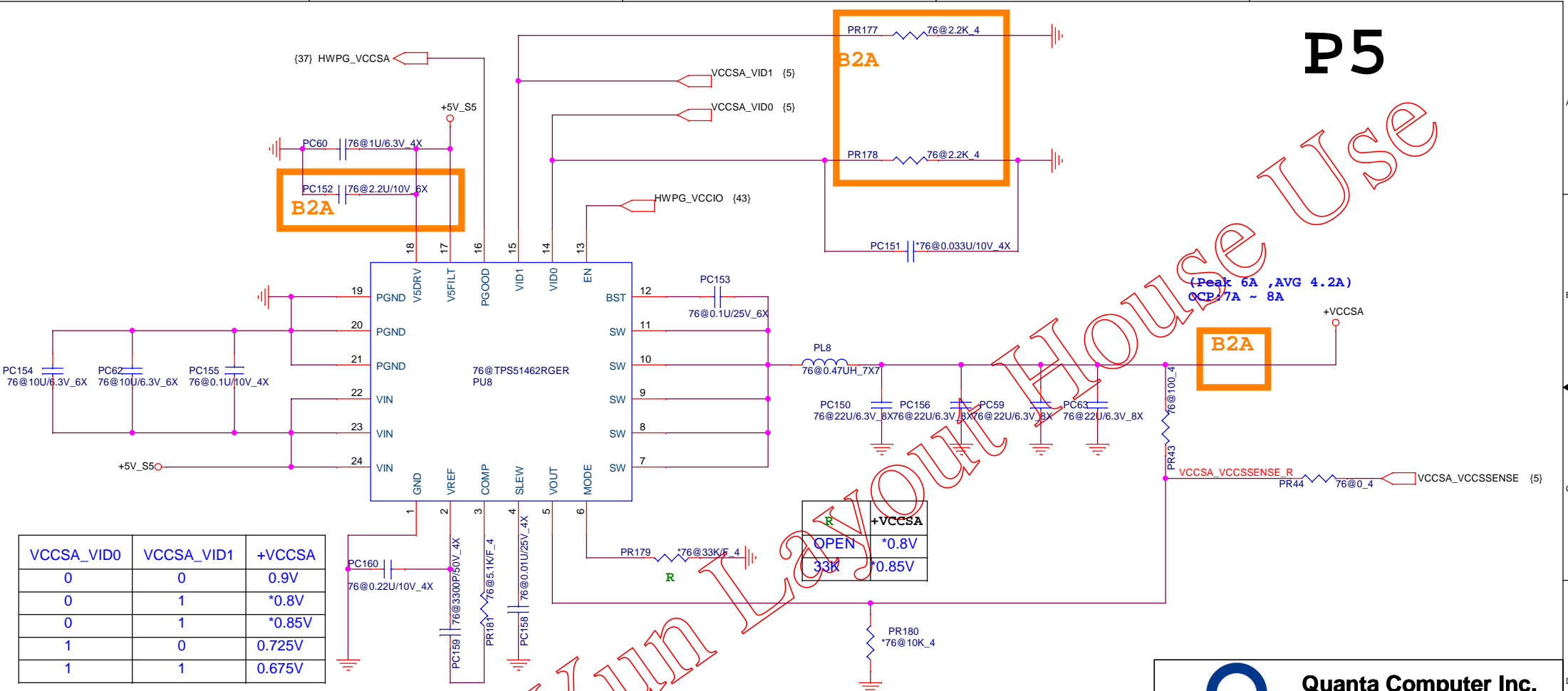


$$V_{OUT} = (1 + R1/R2) * 0.5$$

Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	+VCCIO(RT8240BGQW)	A1A
Date:	Wednesday, January 16, 2013	Sheet 43 of 50

For Xiang Yun Layout



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	*0.8V
0	1	*0.85V
1	0	0.725V
1	1	0.675V

*0.8V FOR SV TYPE
 *0.85V FOR LV/ULV TYPE

R	+VCCSA
OPEN	*0.8V
33K	*0.85V

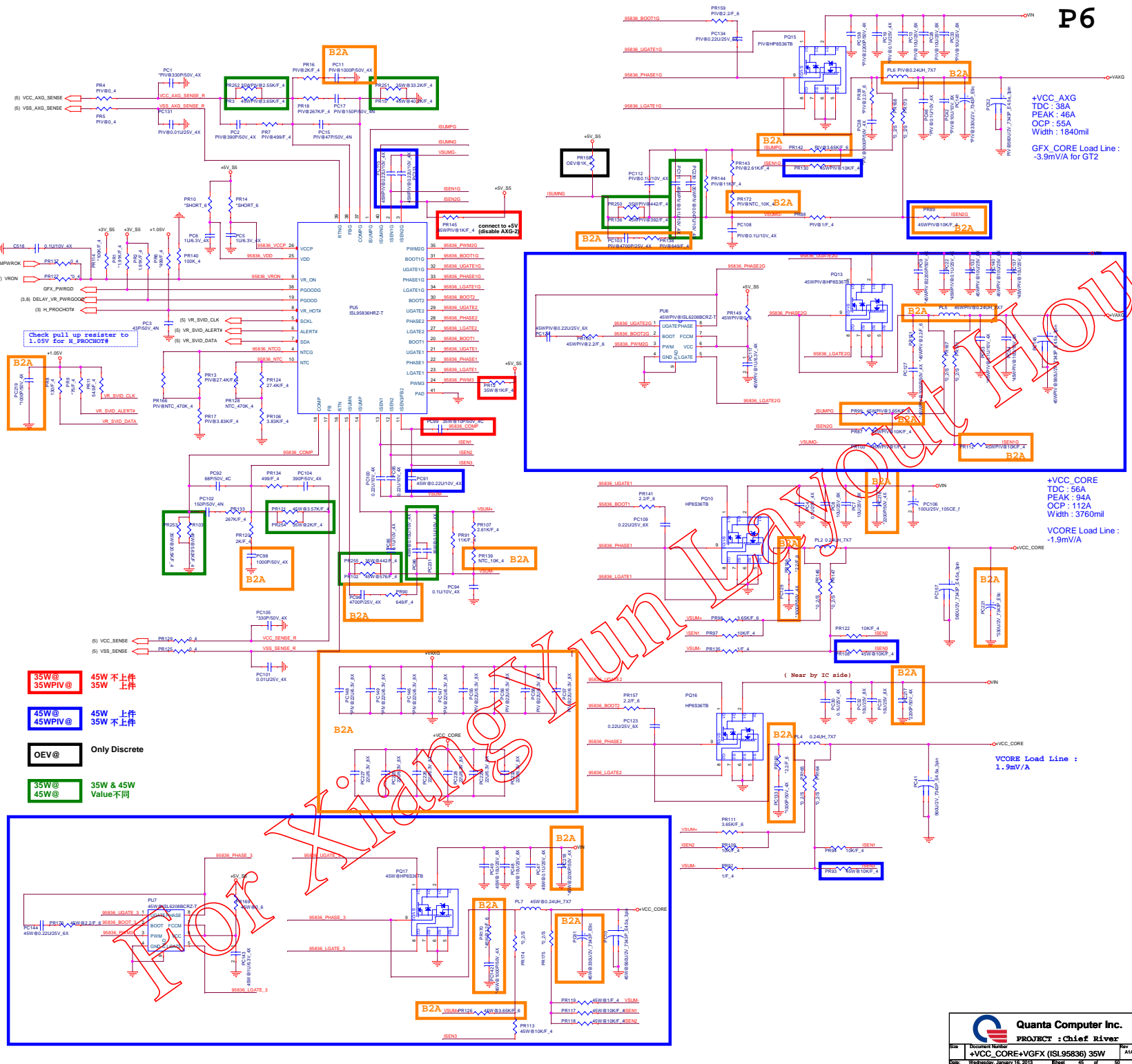
(Peak 6A ,AVG 4.2A)
 OCP 7A ~ 8A

Quanta Computer Inc.

PROJECT : Chief River

Size	Document Number +VCCSA(TI51461)	Rev A1A
Date:	Wednesday, January 16, 2013	Sheet 44 of 50

For Xiang Yun Layout House Use



House Use

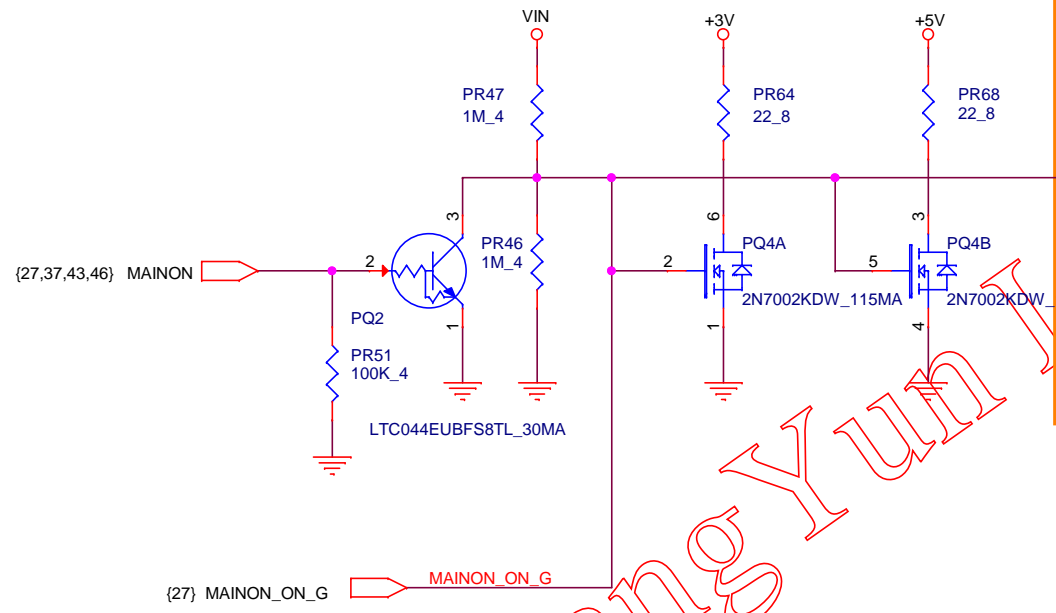
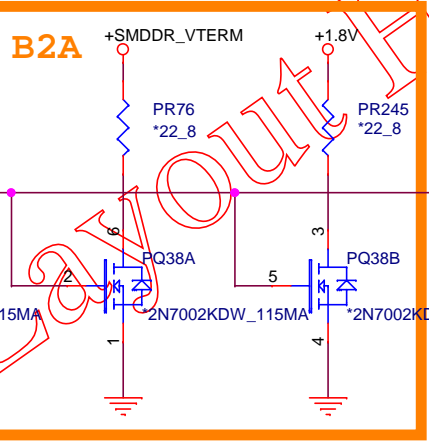
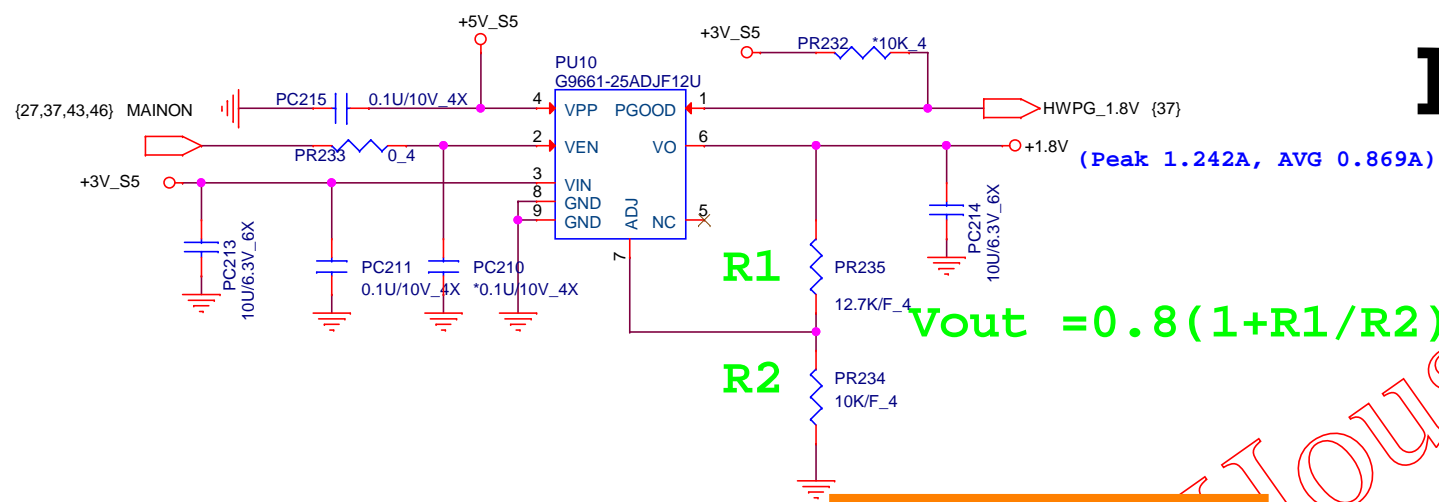
+VCC_AXG
TDC : 38A
PEAK : 46A
OCP : 55A
Width : 1840mil
GFX_CORE Load Line :
-3.9mV/A for GT2

+VCC_CORE
TDC : 56A
PEAK : 94A
OCP : 112A
Width : 3760mil
VCORE Load Line :
-1.9mV/A

VCORE Load Line :
1.9mV/A

- 35W@ 45W 不上件
- 45WPV@ 35W 不上件
- OEV@ Only Discrete
- 35W@ 35W & 45W Value不同

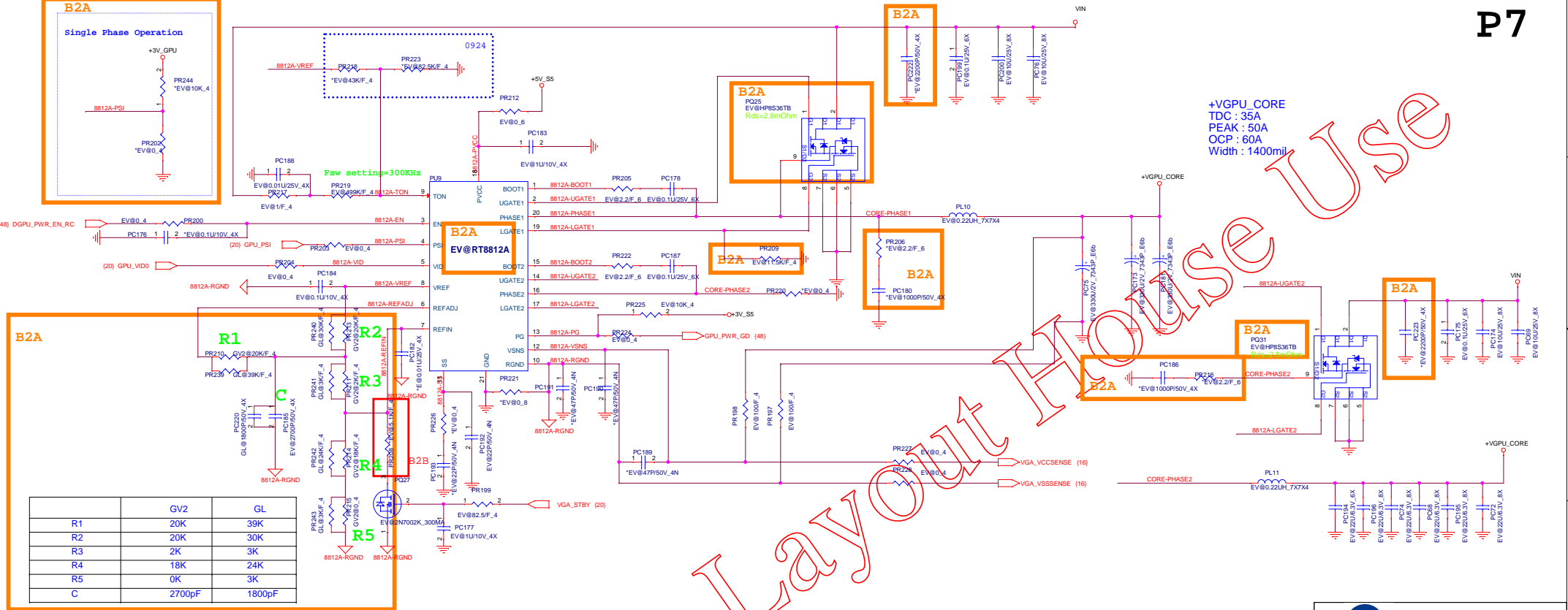
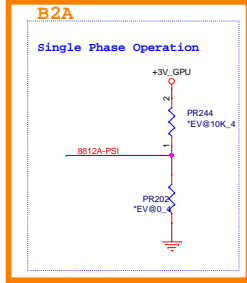
P7



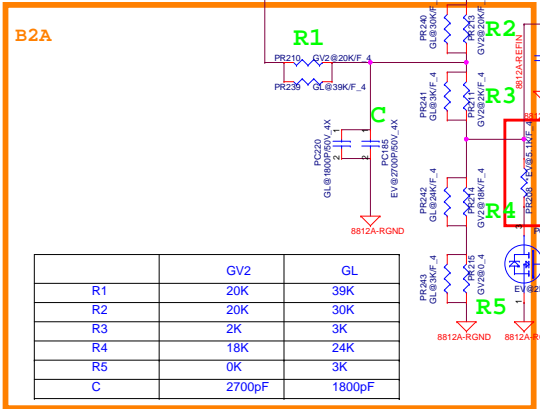
For Xiang Yun

House Use

		Quanta Computer Inc.
		PROJECT : Chief River
Size	Document Number	Rev
	+1.8V/Discharge	A1A
Date:	Wednesday, January 16, 2013	Sheet 46 of 50



+VGPU_CORE
TDC : 35A
PEAK : 50A
OCP : 60A
Width : 1400mil



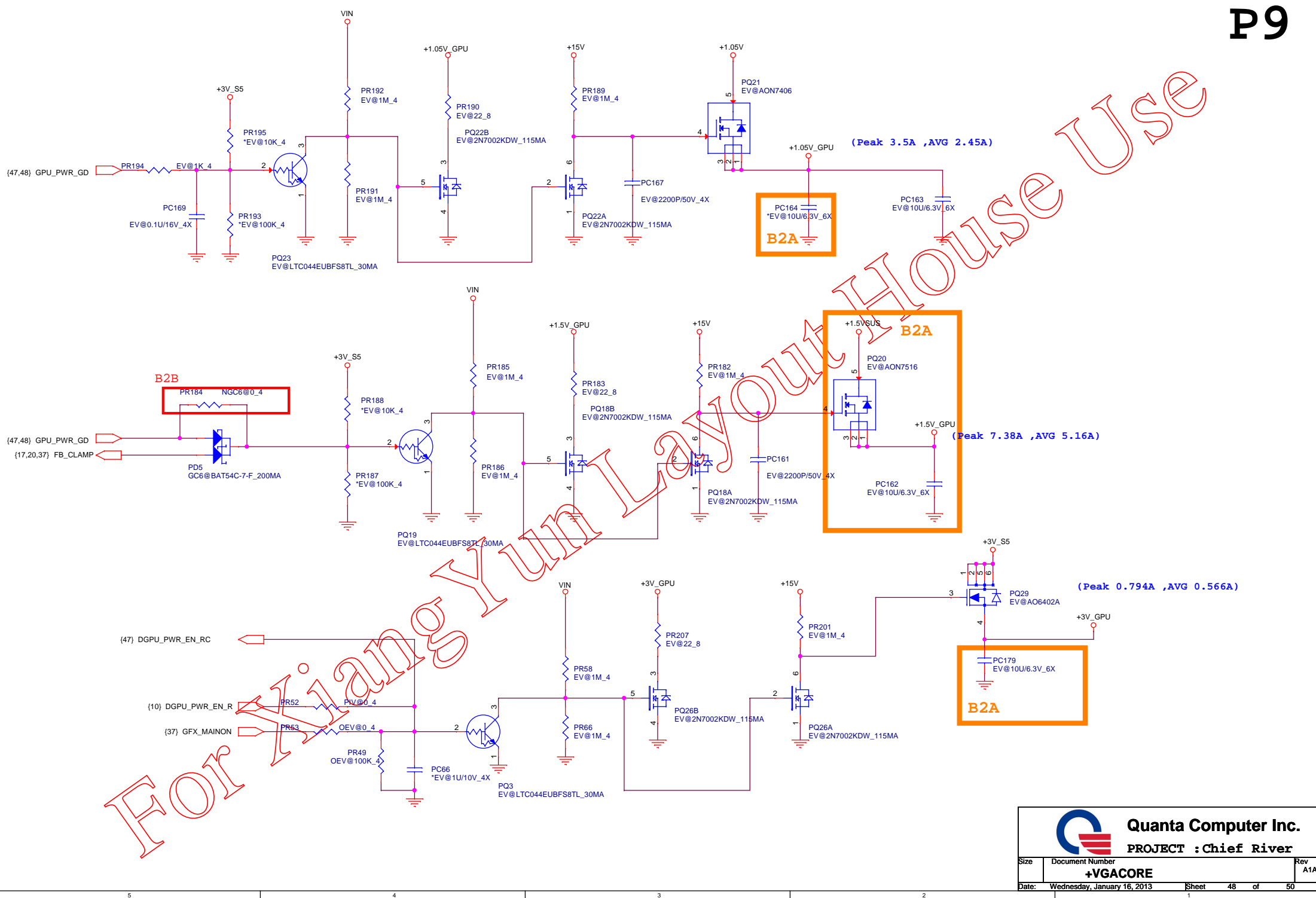
Quanta Computer Inc.
PROJECT : 2013 PROJECT

Size	Document Number	Rev
	GPU Core (RT8812A)	A1A

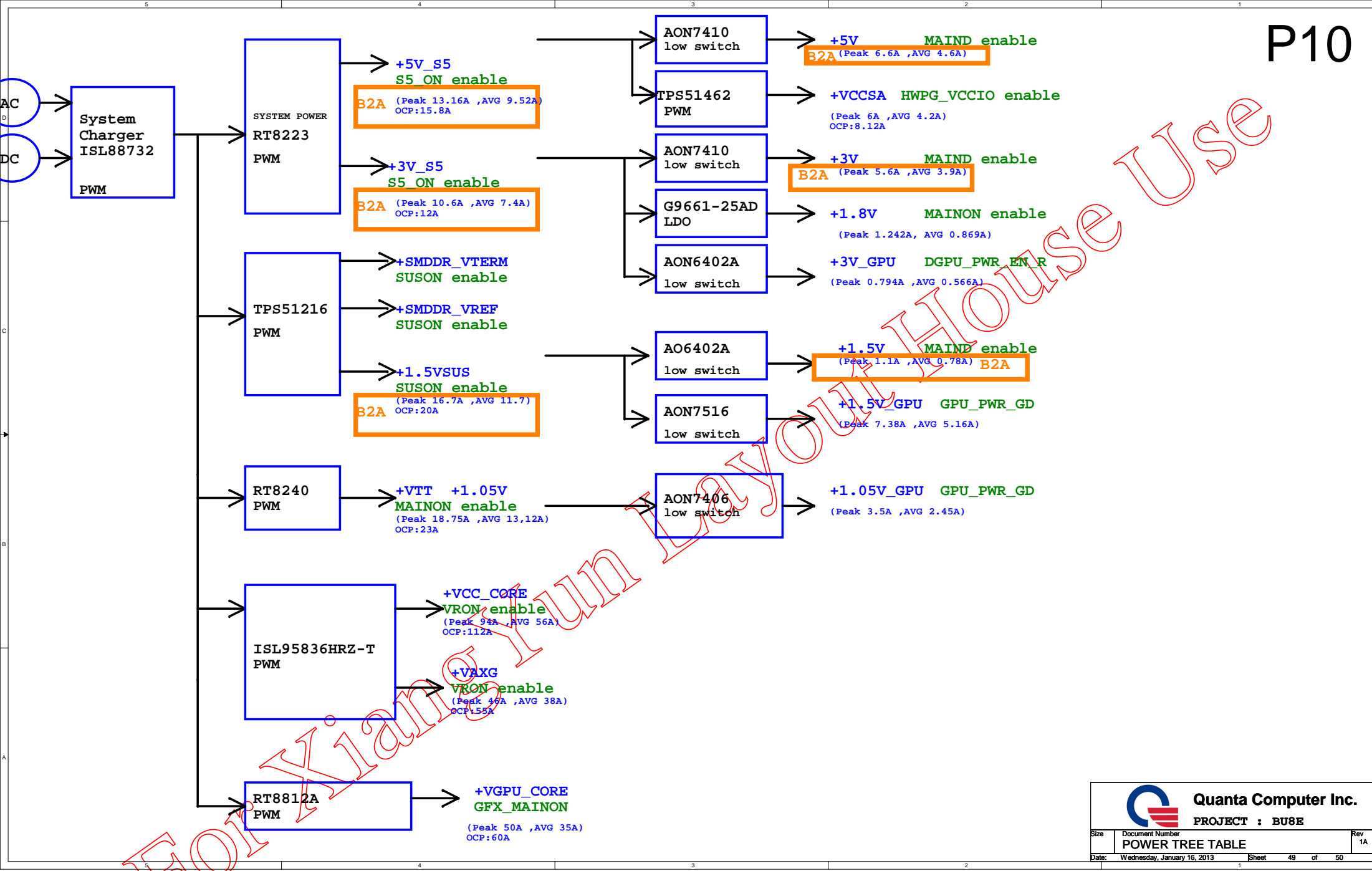
Date: Wednesday, January 16, 2013 Sheet 47 of 50

For Xiang Yun Layout House Use

1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.




For Liang Yun's House Use



For Kiano's Run Layout House Use

Model	REV	CHANGE LIST	MODEL		
			PAGE	FROM	To
BD5 MB	A1A	First Release	1		
	B2A	PAGE 3: Change C537,C538 size and stuff R761	2		
		PAGE 5: add PR257	3		
		PAGE 6: modify R142,Q19,R145,R141,Q20,R144 value for DDR3 VREF DQ (M3).	4		
		PAGE 8: modify R735,R715,R395,R369,R397,R720 value to S3	5		
		PAGE 9: change GPIO13 to BOARD_ID16,GPIO23 to BOARD_ID17	6		
		PAGE 10: add USB port3 for Touch Panel function,add R766,R768,R755,R769,R770,R772,R767,R773,Q55,Q56 for S3,change C704,C708 to 12PF	7		
		PAGE 11: change R406,R385,R743,R731,R401,R381,R778,R691,R700,R698,R306,R779,R780,R781,R405,R384 for BOARD_ID select	8		
		PAGE 12: change C420,R295,R784,L14,R288,R785,R416,R796 value and change R786,R420,C470,R787,R421,C469 value for S3	9		
		PAGE 16: change R180,R179,Q25,Q24,Q57 value for CLK PEG	10		
		PAGE 18: change C725,C726,C727 value,and add R788,R789 for EDP PD	11		
		PAGE 19: add R790 for XTAL,and change R249,R250 value	12		
		PAGE 20: change R251,R612,R252,R791,R792 value	13		
		PAGE 21: add R793 for co-lay	14		
		PAGE 22: change C312,C639 value	15		
		PAGE 28: change R794,F3,U25,D21 value for HDMI	16		
		PAGE 29: change R14,R16,R7,MR1,CN15,CN8,F1,R472,R470,R473,R471 value	17		
		PAGE 30: change R499,R797,Q41,R466 value for AOAC	18		
		PAGE 31: add D7,D22,D23,D24,D25,D28,D29,D31,D30,D32,D33,D34,D35 for ESD,change C380,C381,CN18,CN17,R316,R395,U12,C384,C398,C699,R315,Q34 value	19		
		PAGE 33: change CN14 value	20		
		PAGE 34: add D36,D37,D38,D39,D40,D41,D42,D43 for ESD	21		
		PAGE 35: change C234,C221,C190,C184,C174,C168 value,and add C730,C728,C729,C731 for EMI,add D44,D45,D46,D47 for ESD	22		
		PAGE 36: change R413,R394,R389,R390,R391,R392,R393,C448,C441,C440,C442,C443 value	23		
		PAGE 37: change R80,Q4 value,add R799,R798 for STRAP select	24		
		PAGE 38: change CN1,CN2,CN5,CN4,R95,Q10 value and change C218 value for EMI,and add L41,L42,C723,C724,CN2021,R777,R776,R775,R774 for Touch PAD Panel function	25		
		PAGE 39: change LED2 symbol	26		
		B2B PAGE 20: change R570 value	27		
		PAGE 22: change D4 value	28		
		C3A PAGE 15: change C65 size to 0402	29		
		PAGE 31: change RN10,RN11,RN12,RN13 pin define	30		
		PAGE 34: change C490,C501 size to 0402	31		
		PAGE 36: change C476 size to 0402	32		
			33		
			34		
			35		
			36		
			37		
			38		
			39		
			40		
			41		
			42		
			43		

For Xiang Yun Layout House Use

DOC NO. 204	PROJECT MODEL :	BD5	APPROVED BY:	Kent Su	DATE:	2012/12/14	 Quanta Computer Inc. PROJECT : BD5
	PART NUMBER:		DRAWING BY:	Kent Su	REVISION:		