

Compal confidential

Schematics Document

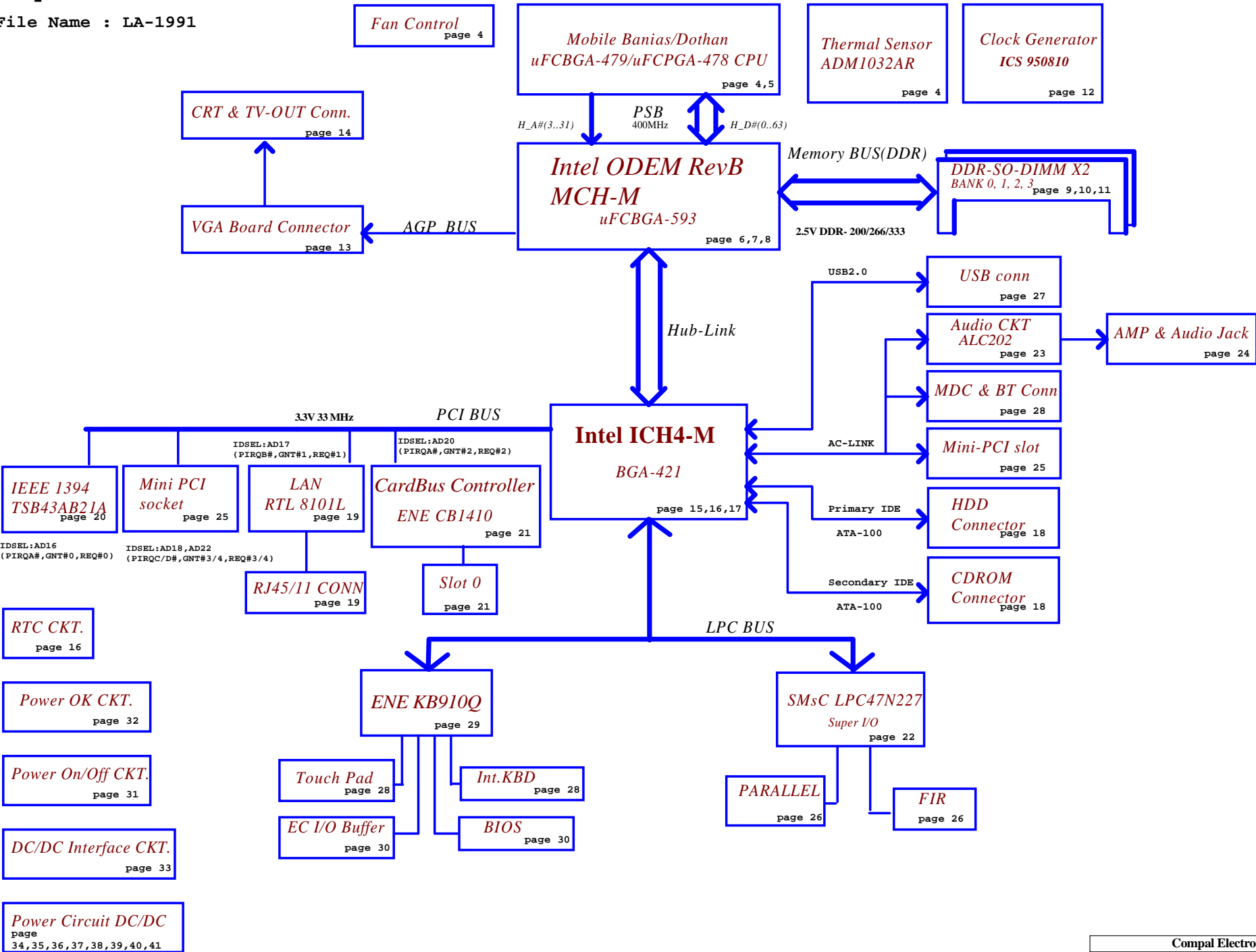
Mobile Baniyas/Dothan uFCBGA/uFCPGA
with Intel ODEM_MCH RevB+ICH4-M
core logic

2003-09-01

REV:1.0

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RTC CKT.
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Power OK CKT.
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Power On/Off CKT.
page 31

DC/DC Interface CKT.
page 33

Power Circuit DC/DC
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.2VS	1.2V switched power rail for MCH core power	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail for AGP interface	ON	OFF	OFF
+1.8VS	1.8V switched power rail for CPU PLL & Hub-Link	ON	OFF	OFF
+2.5V	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12Vswitched power rail on power rail	ON	OFF	OFF
RTCVC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol note:

↓ :means digital ground.

↓ :means analog ground.

@ :means reserved.

Internal PCI Devices

DEVICE	PCI Device ID
HUB	D30
USB	D29
AC97 MODEM	D31
AC97	D31
ATA 100	D31
ETHERNET	D8 (AD24)
LPC I/F	D31
SMBUS	D31

External PCI Devices

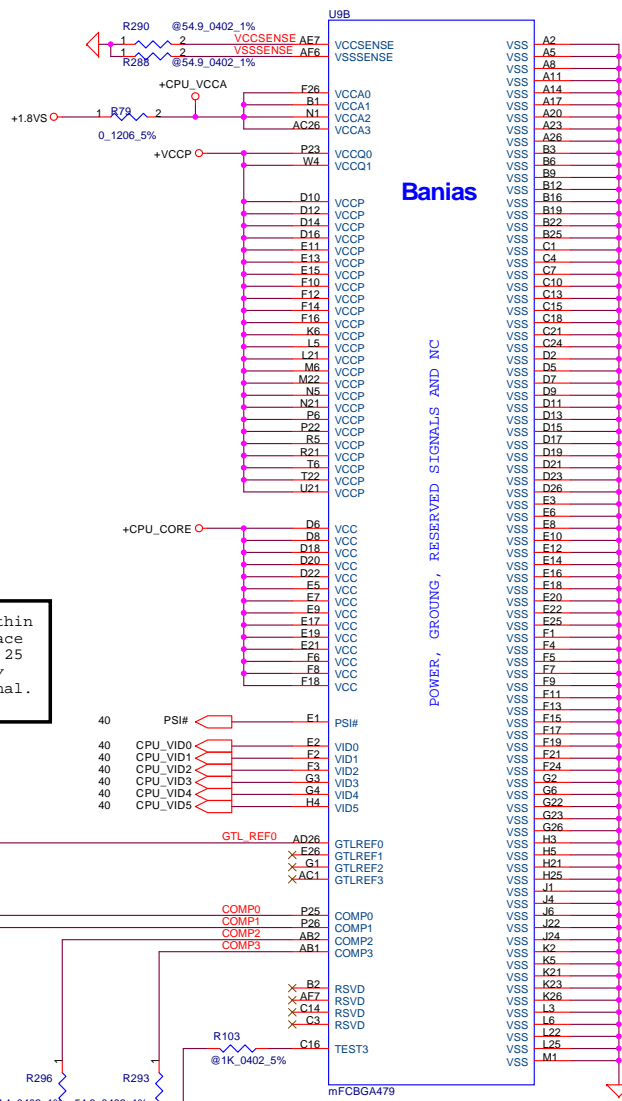
DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD16	0	A
LAN	D1	AD17	1	B
CARD BUS	D4	AD20	2	C
Wireless LAN	D2	AD18	3	D
Mini-PCI	D6	AD22	4	D
AGP BUS	N/A	AGP_DEVSEL#	N/A	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 X

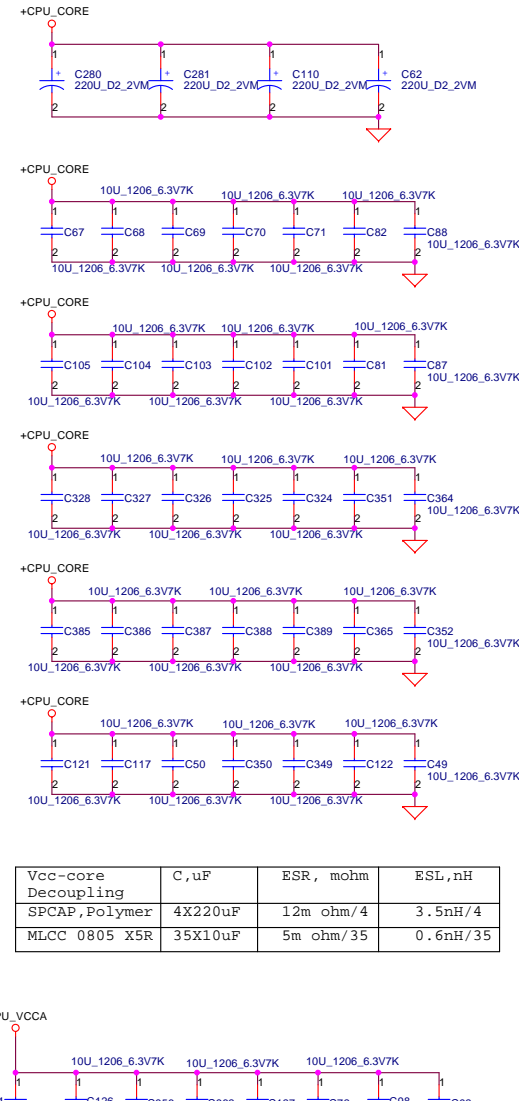
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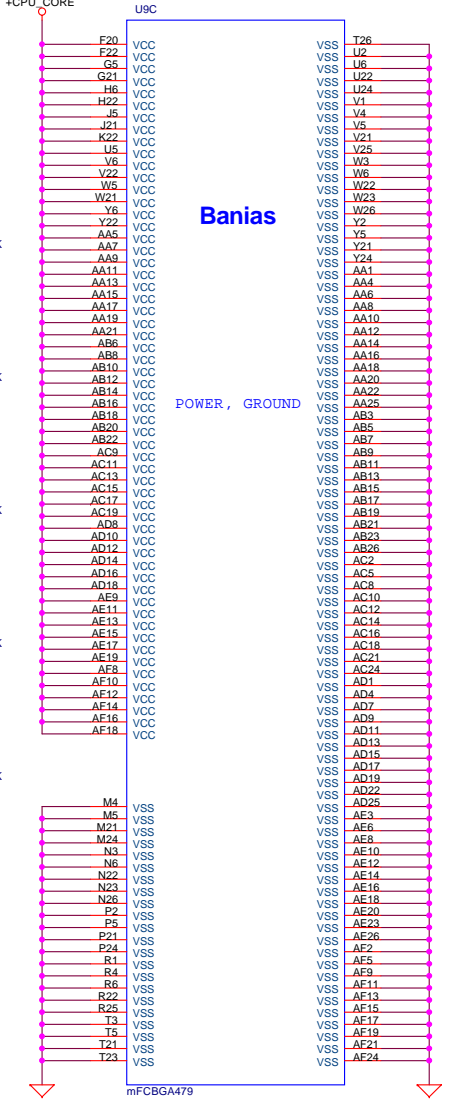


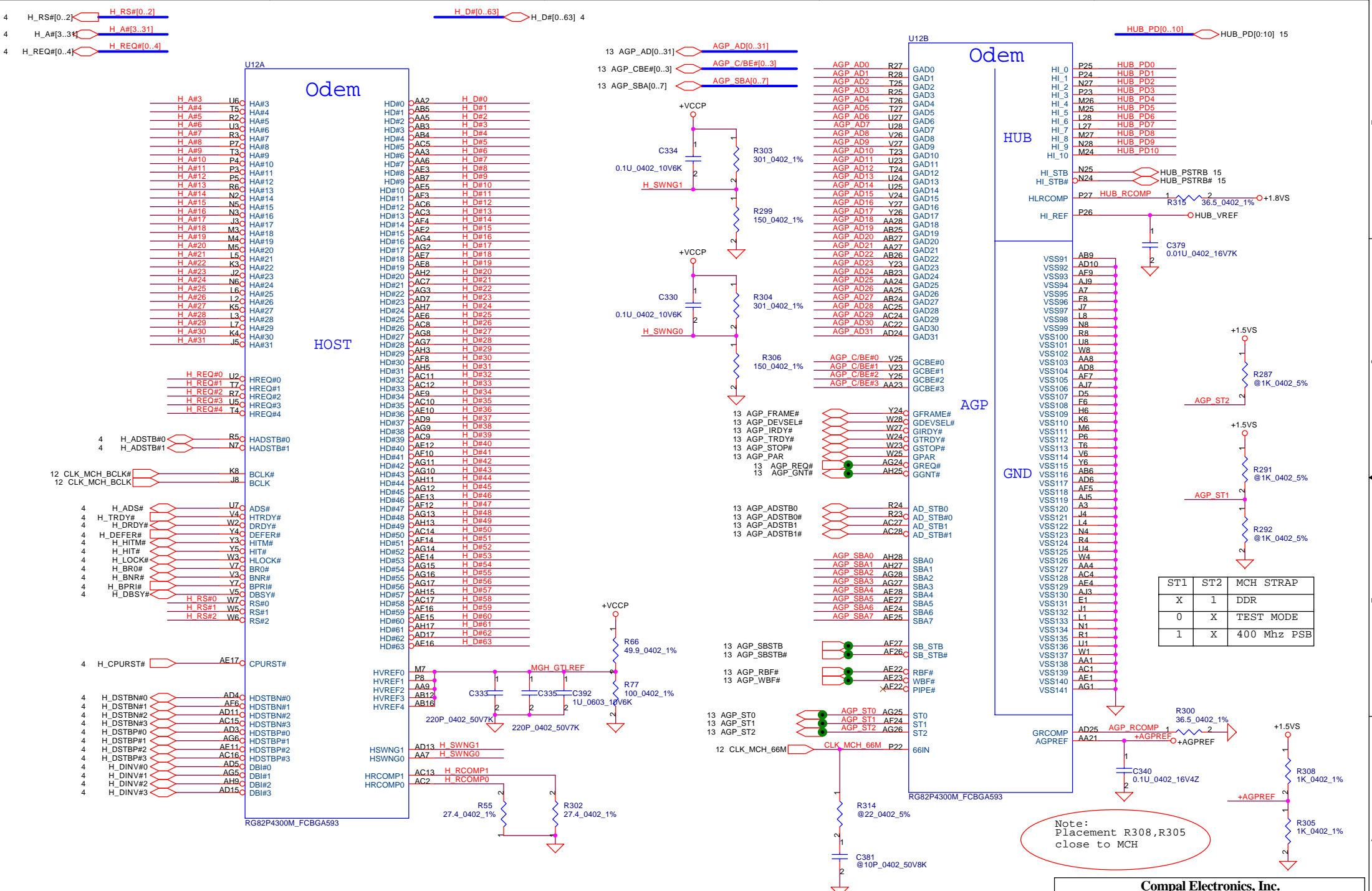
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35





Note: Placement R308, R305 close to MCH

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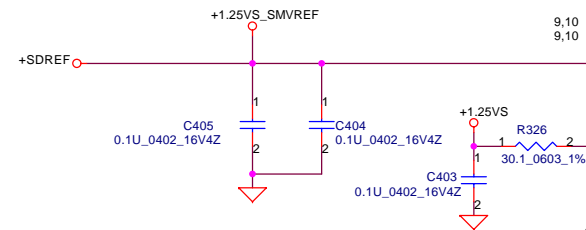
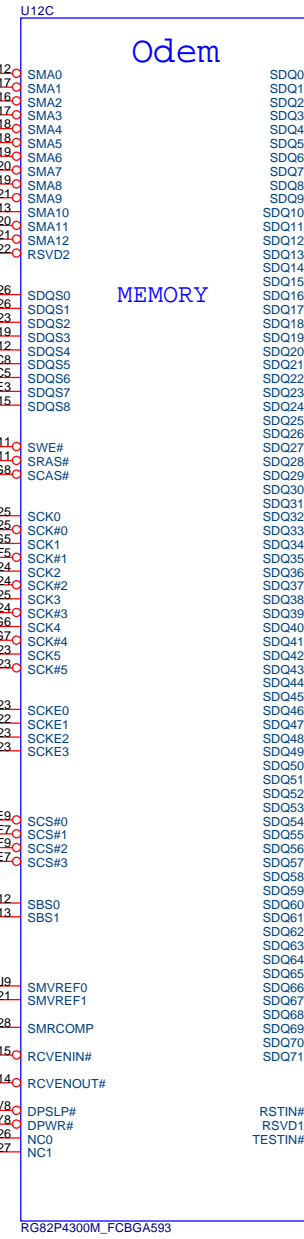
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- 9,10 DDR_MMA[0..12] \rightarrow DDR_MMA[0..12]
- 9 DDR_SDQ[0..63] \rightarrow DDR_SDQ[0..63]
- 9 DDR_SDQS[0..8] \rightarrow DDR_SDQS[0..8]
- 9 DDR_CB[0..7] \rightarrow DDR_CB[0..7]

- DDR_MMA0 E12
- DDR_MMA1 F17
- DDR_MMA2 E16
- DDR_MMA3 G17
- DDR_MMA4 G18
- DDR_MMA5 F18
- DDR_MMA6 F19
- DDR_MMA7 G20
- DDR_MMA8 G19
- DDR_MMA9 F21
- DDR_MMA10 F13
- DDR_MMA11 E20
- DDR_MMA12 G21
- ~~G22~~
- DDR_SDQS0 F26
- DDR_SDQS1 C26
- DDR_SDQS2 C23
- DDR_SDQS3 B19
- DDR_SDQS4 D12
- DDR_SDQS5 C8
- DDR_SDQS6 C6
- DDR_SDQS7 E3
- DDR_SDQS8 F15

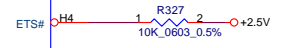
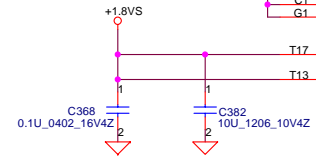
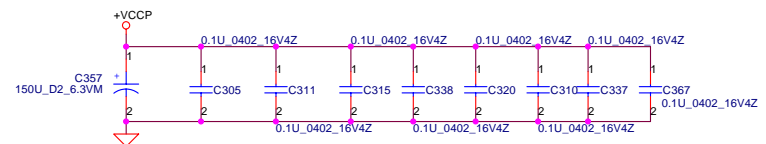
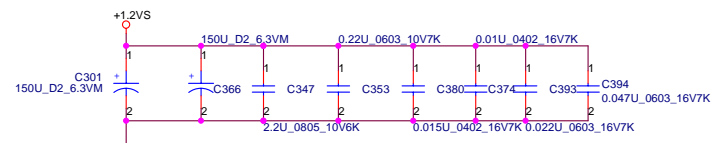
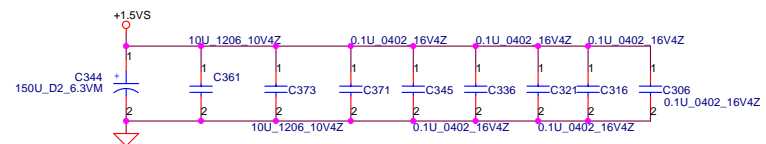
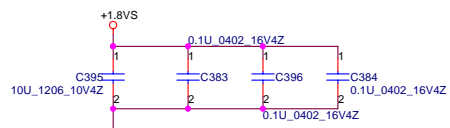
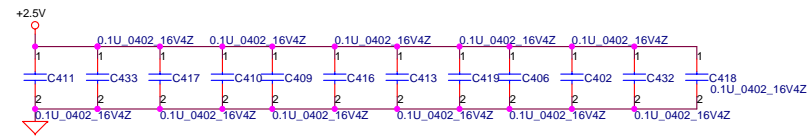
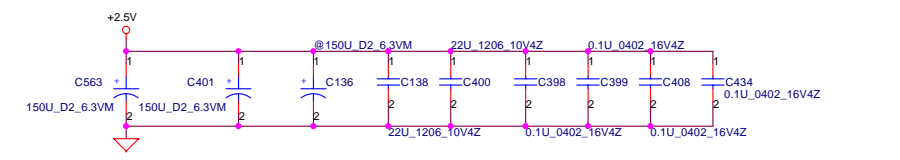
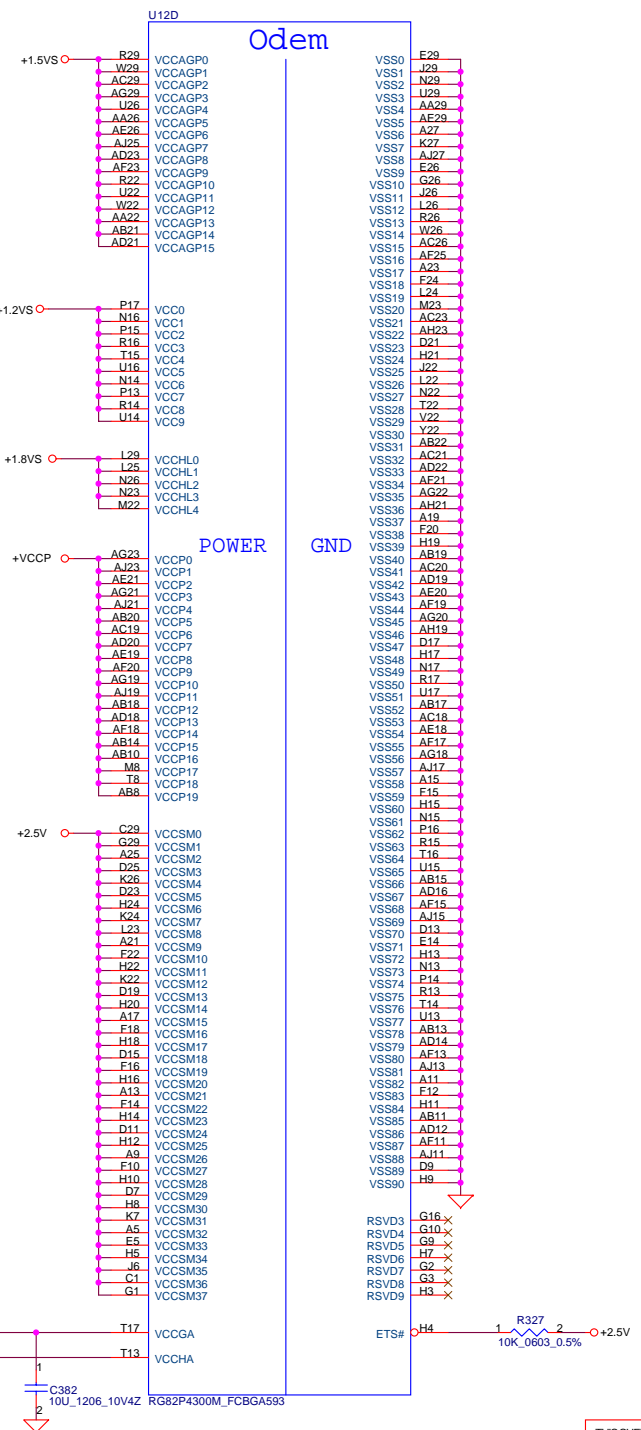
- 9,10 DDR_SWE# \rightarrow G11
- 9,10 DDR_SRAS# \rightarrow F11
- 9,10 DDR_SCAS# \rightarrow G8
- 9 DDR_CLK0 \rightarrow J25
- 9 DDR_CLK0# \rightarrow K25
- 9 DDR_CLK1 \rightarrow G5
- 9 DDR_CLK1# \rightarrow F5
- 9 DDR_CLK2 \rightarrow G24
- 9 DDR_CLK2# \rightarrow E24
- 10 DDR_CLK3 \rightarrow J24
- 10 DDR_CLK3# \rightarrow G6
- 10 DDR_CLK4 \rightarrow G7
- 10 DDR_CLK4# \rightarrow K23
- 10 DDR_CLK5 \rightarrow J23
- 9,10 DDR_CKE0 \rightarrow G23
- 9,10 DDR_CKE1 \rightarrow E22
- 10 DDR_CKE2 \rightarrow H23
- 10 DDR_CKE3 \rightarrow F23
- 9,10 DDR_SCS#0 \rightarrow E9
- 9,10 DDR_SCS#1 \rightarrow F7
- 10 DDR_SCS#2 \rightarrow F9
- 10 DDR_SCS#3 \rightarrow E7
- 9,10 DDR_SBS0 \rightarrow G12
- 9,10 DDR_SBS1 \rightarrow G13



NOTE: 1.M_RCV# max 2Via
 2.G15 to Via max=40mils
 3.G14 to Via max=40mils
 4.Via to Via must = 100mils +-5mils

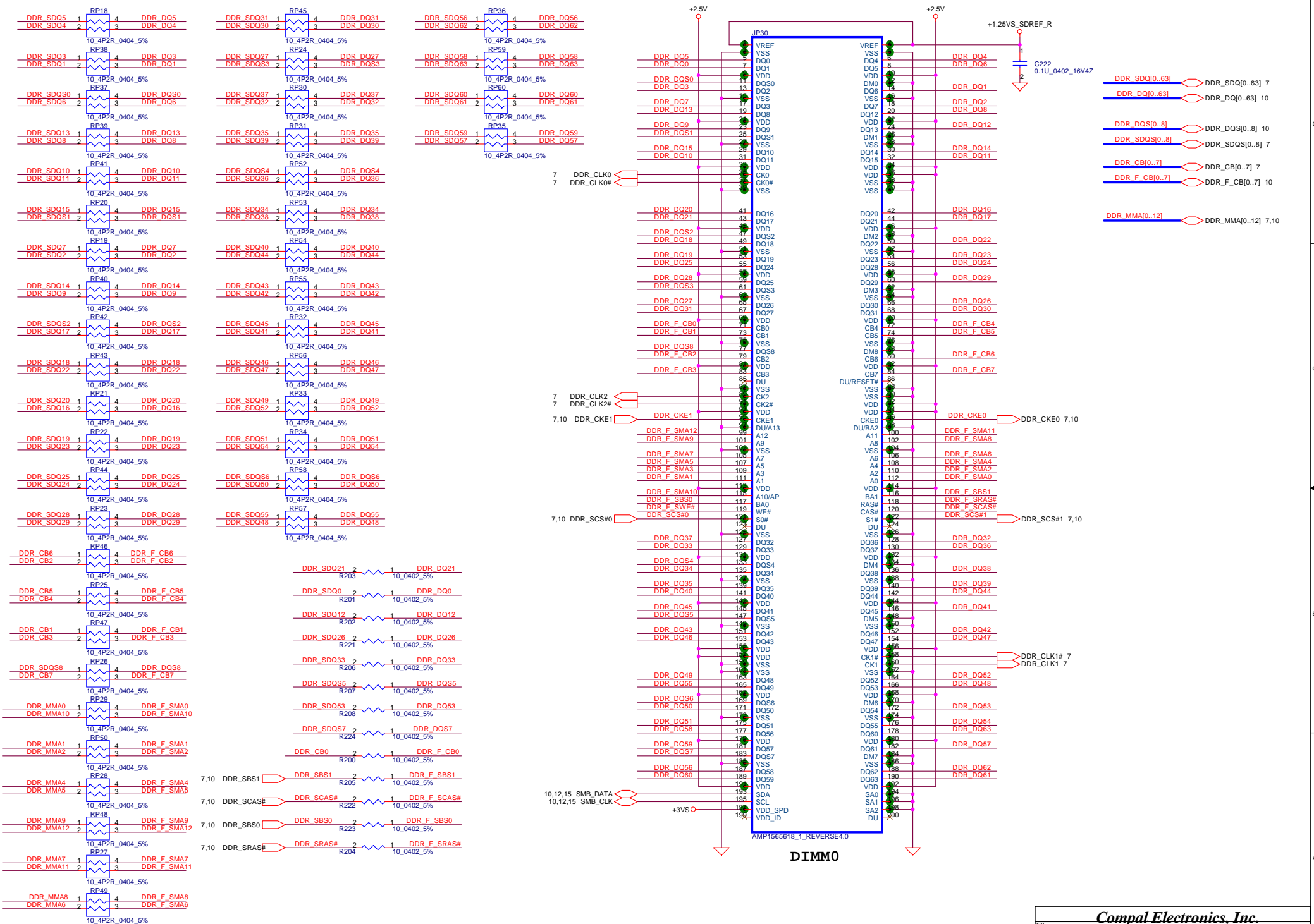
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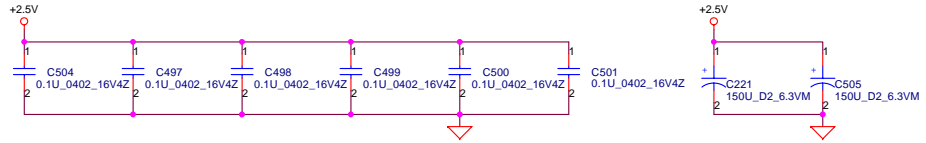
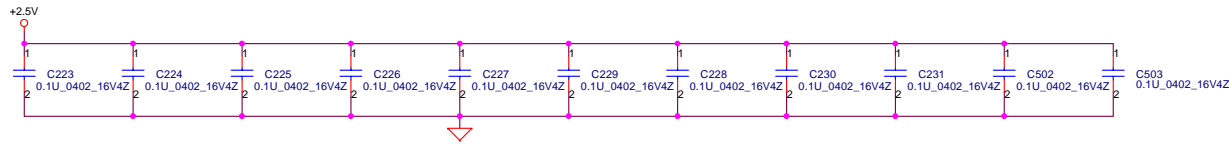
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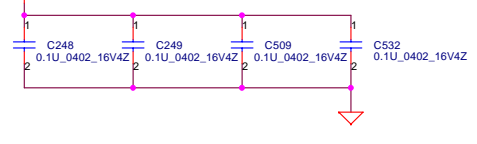
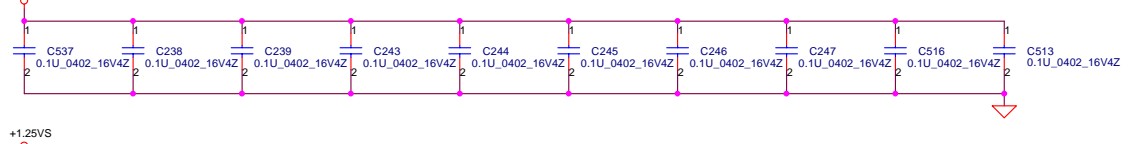
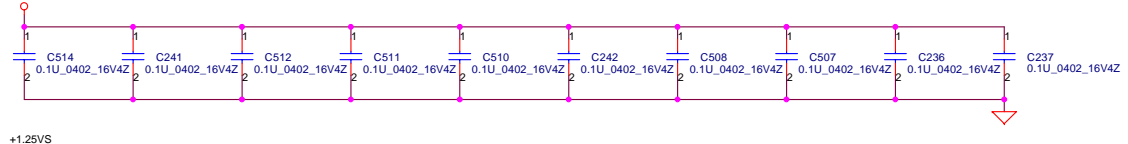
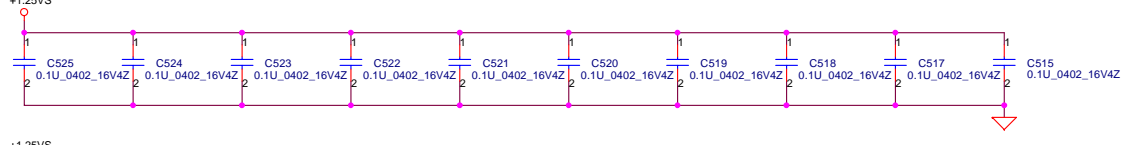
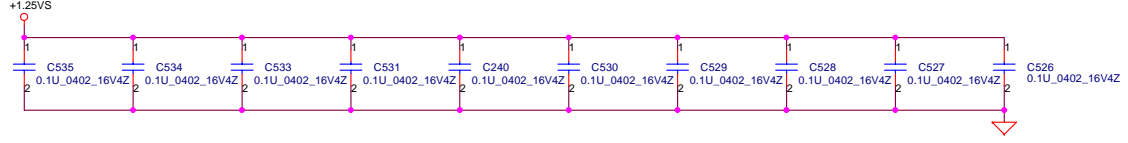
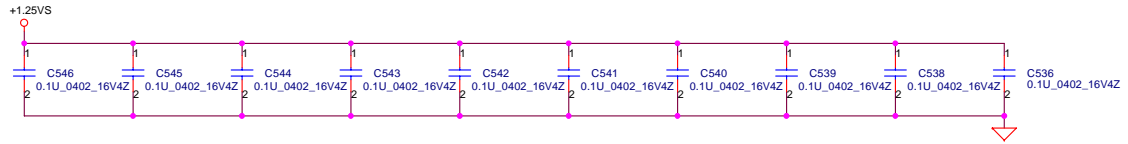
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Layout note :
Distribute as close as possible to DDR-SODIMM.



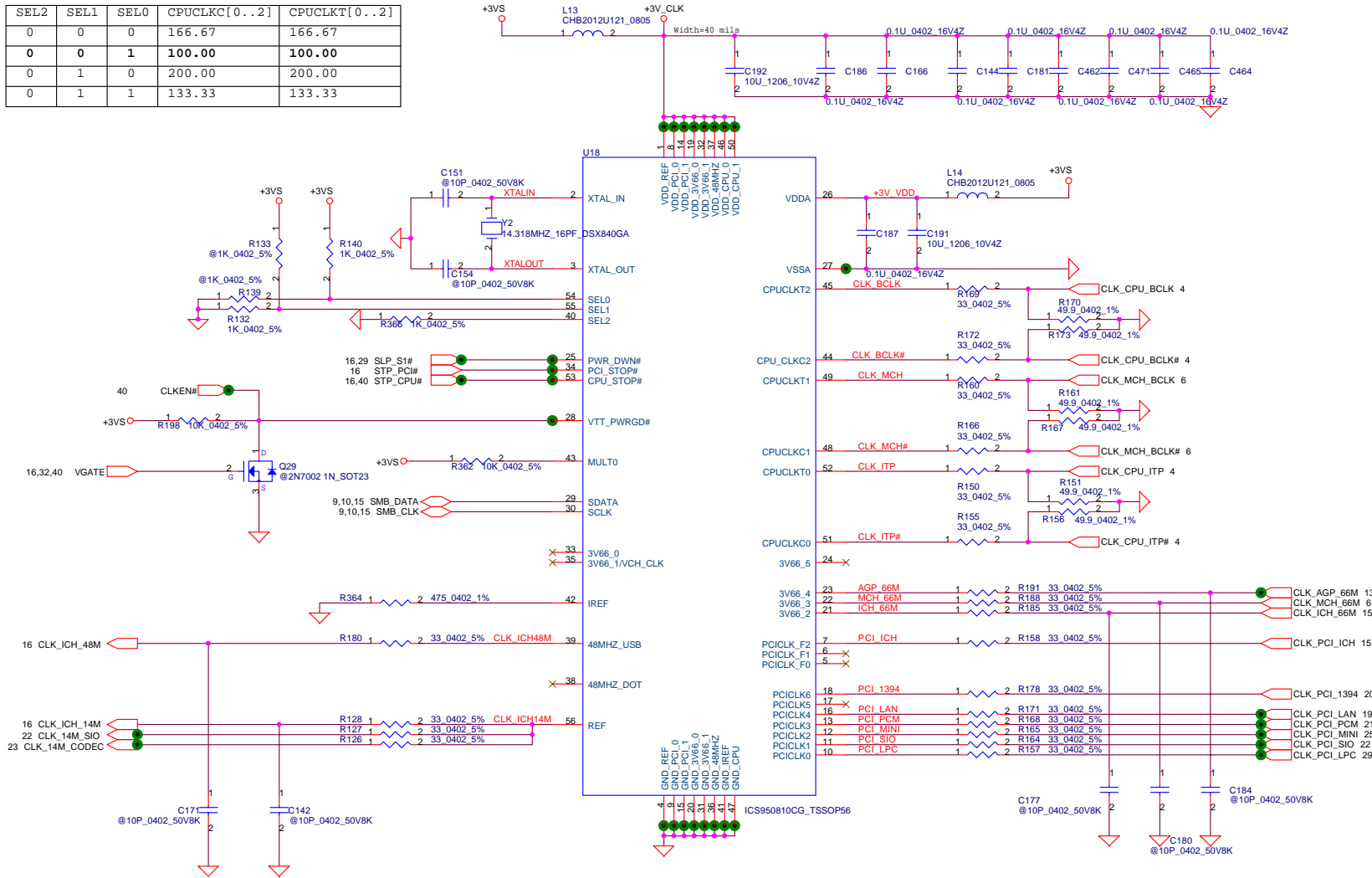
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



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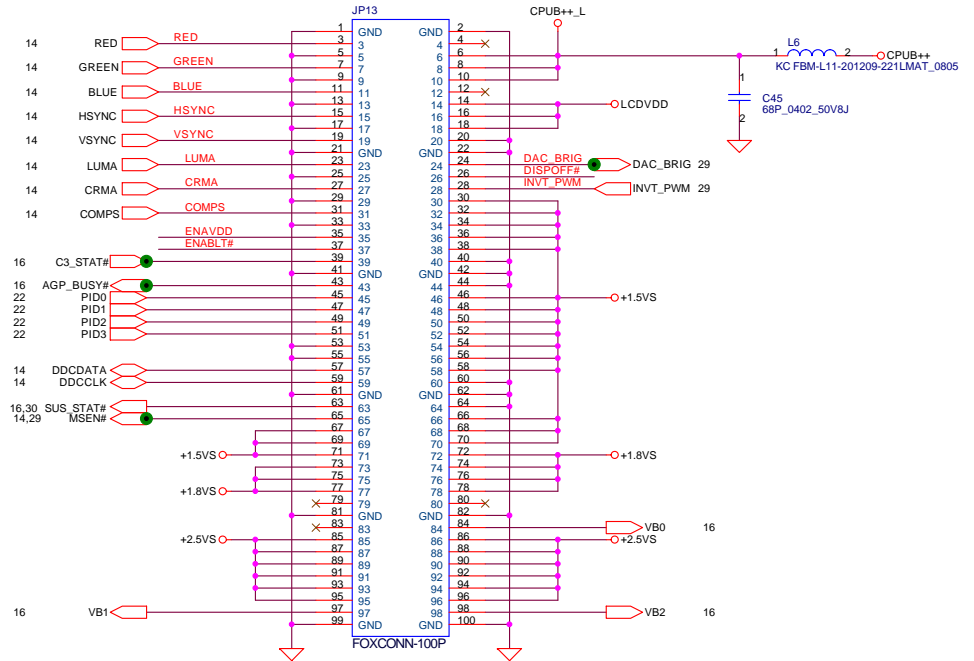
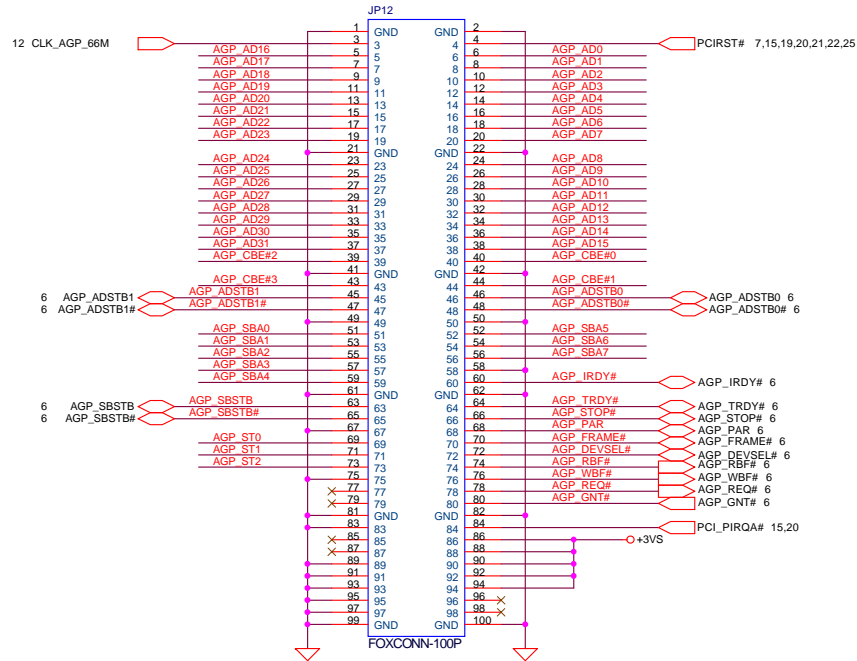
SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



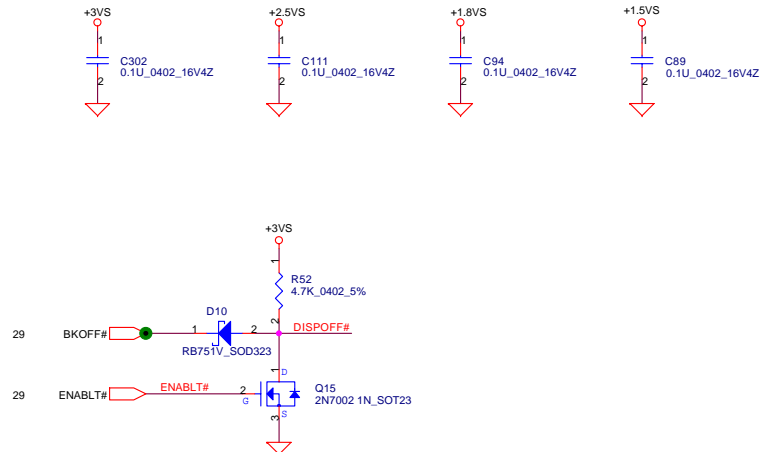
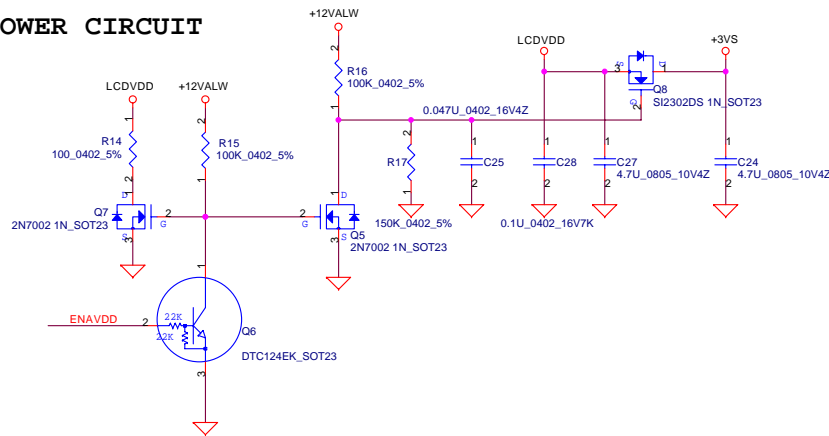
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AGP CONN



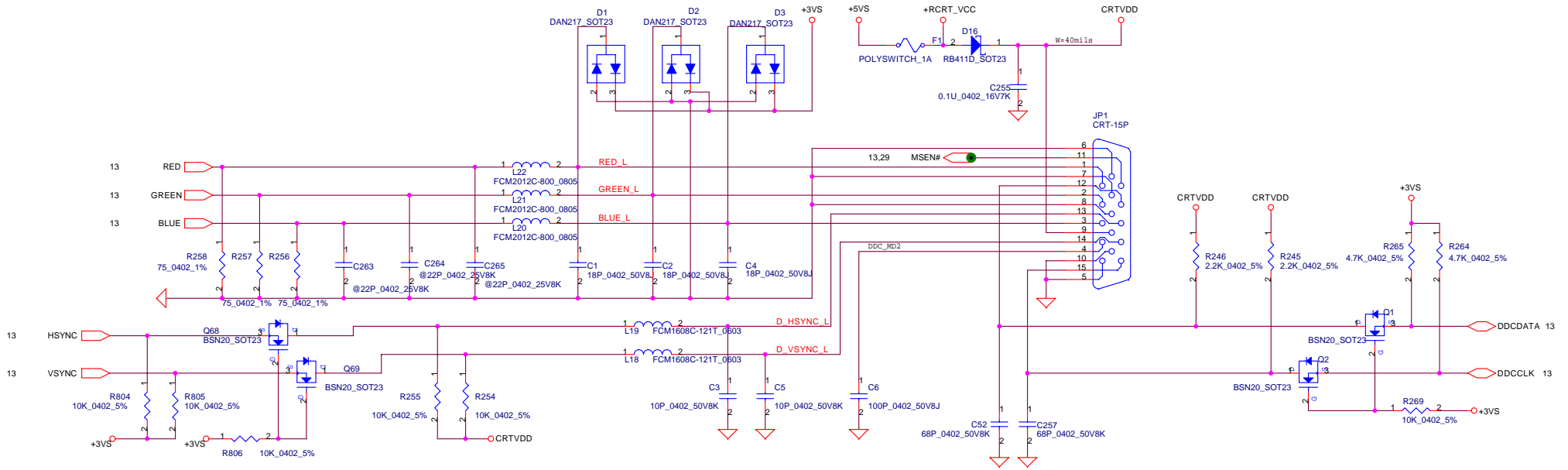
LCD POWER CIRCUIT



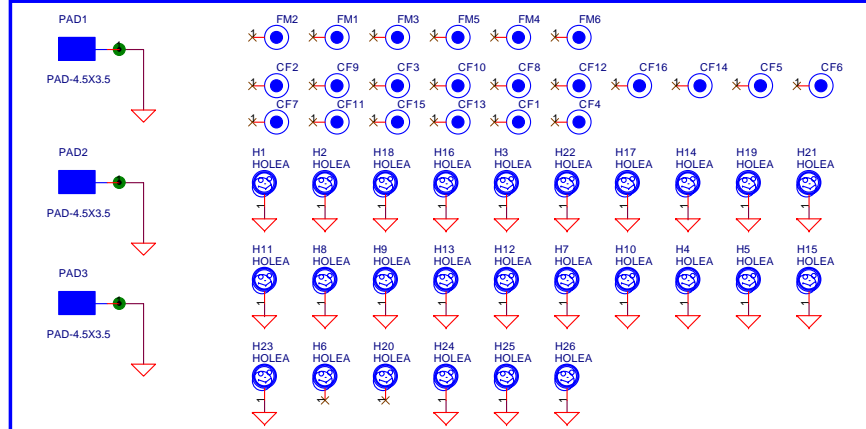
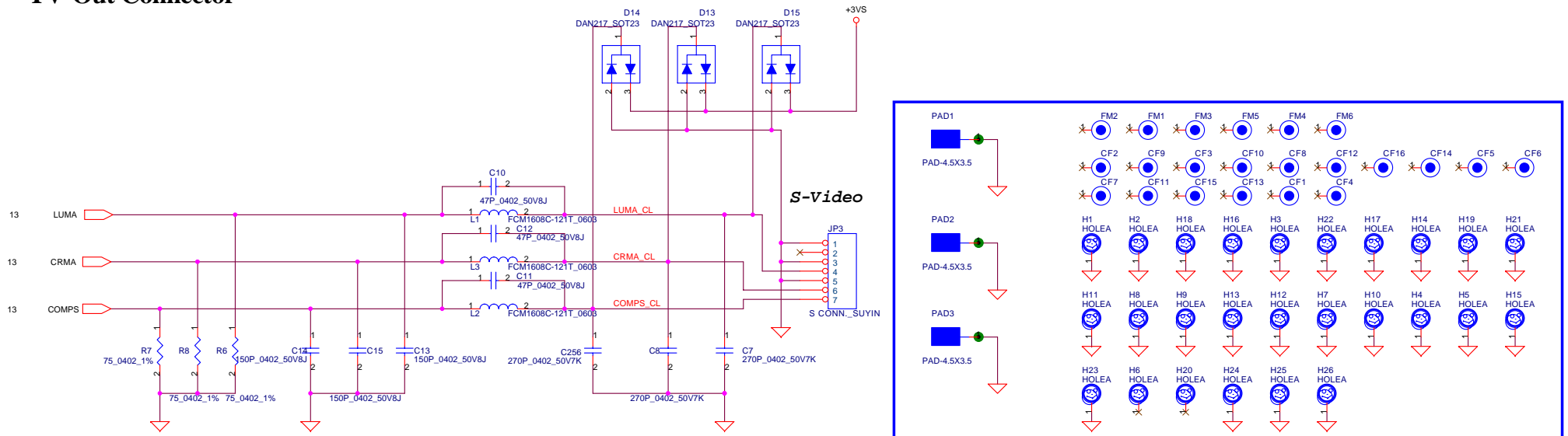
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CRT Connector

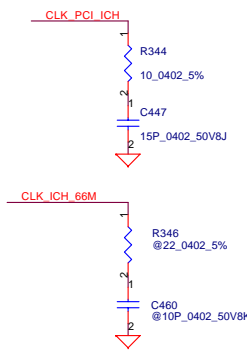


TV-Out Connector

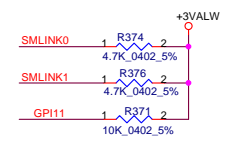
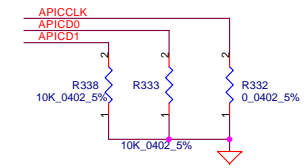
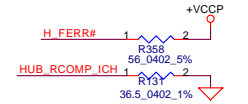
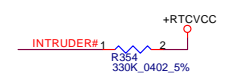
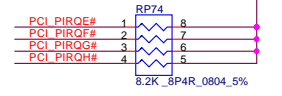
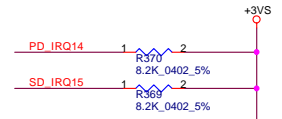
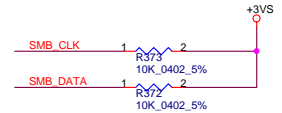
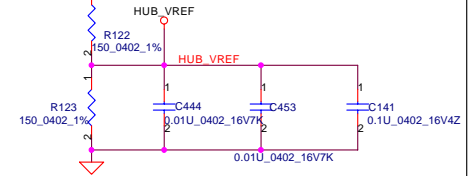
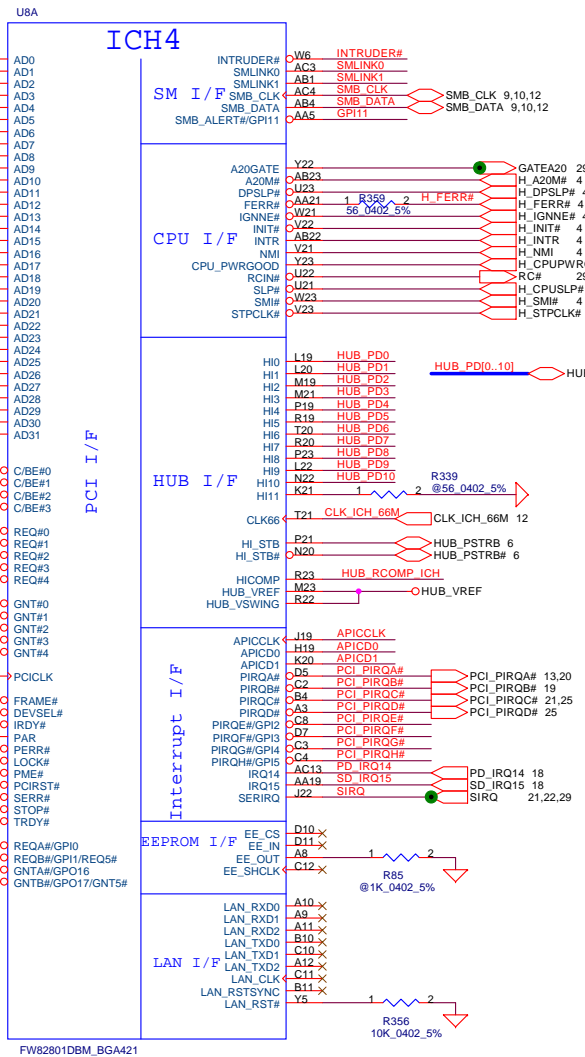
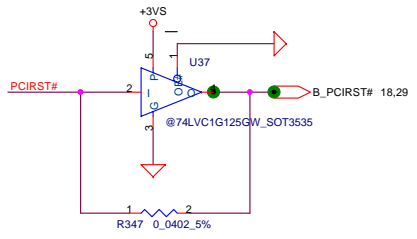
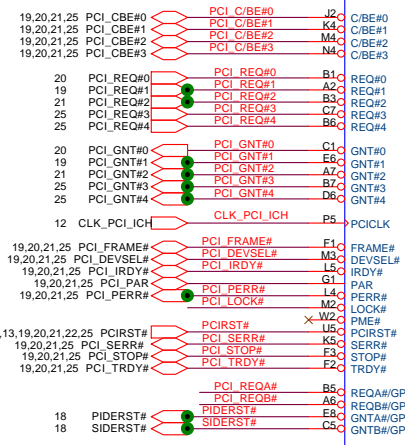
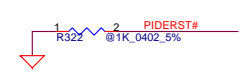
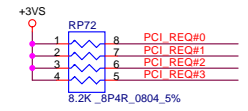
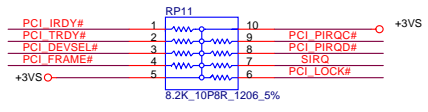
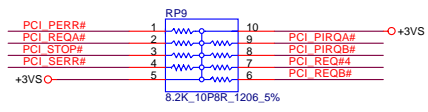


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	星期五, 九月 05, 2003	14	45

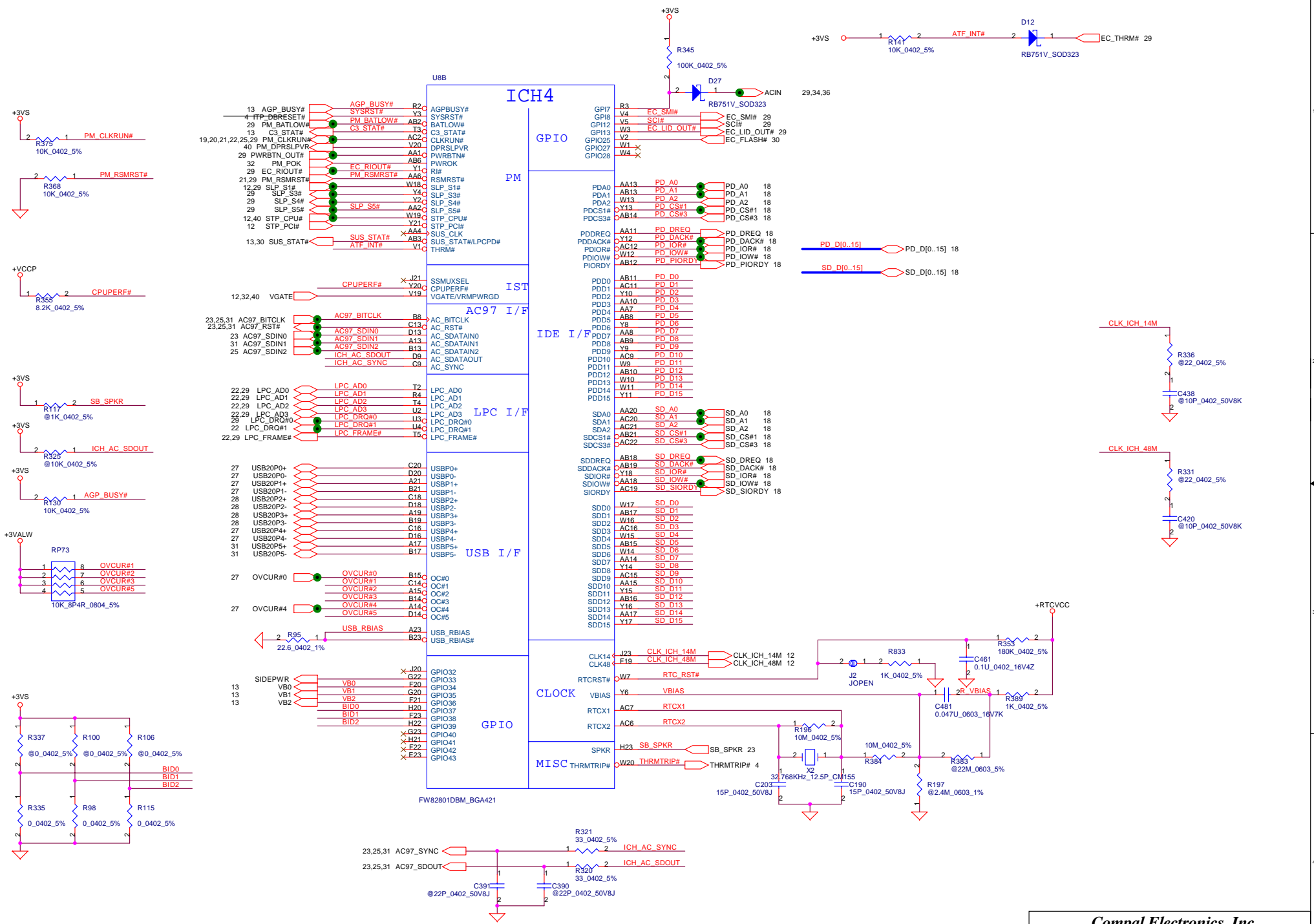


PCI Pullups



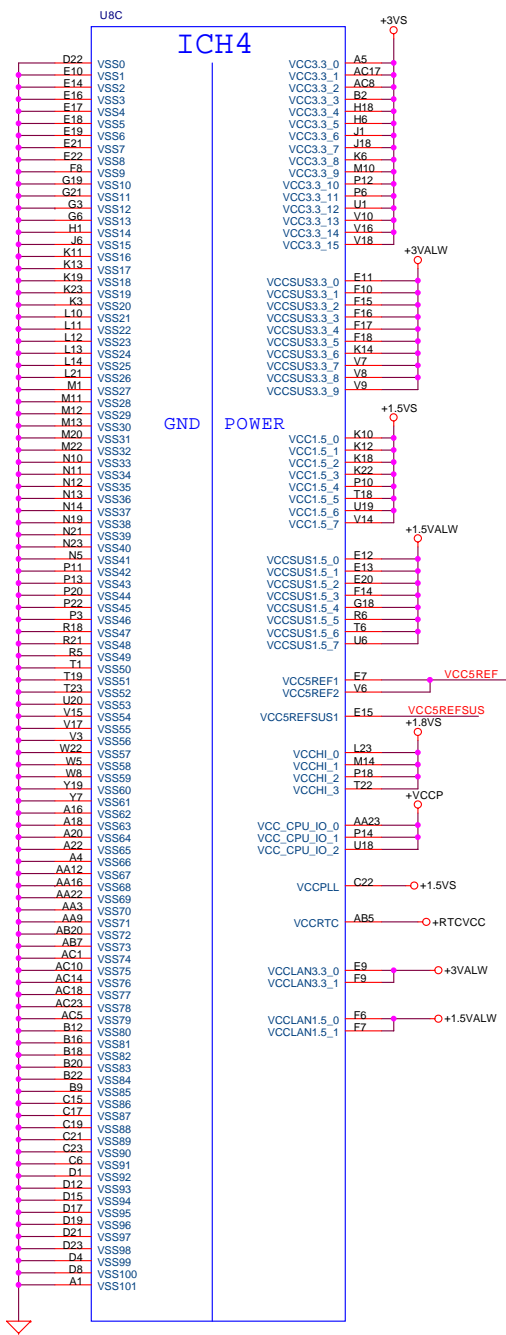
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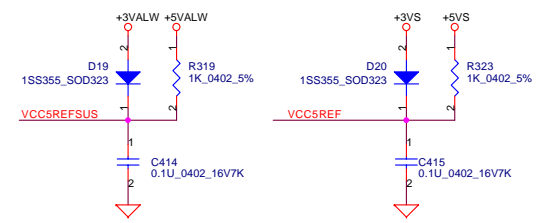
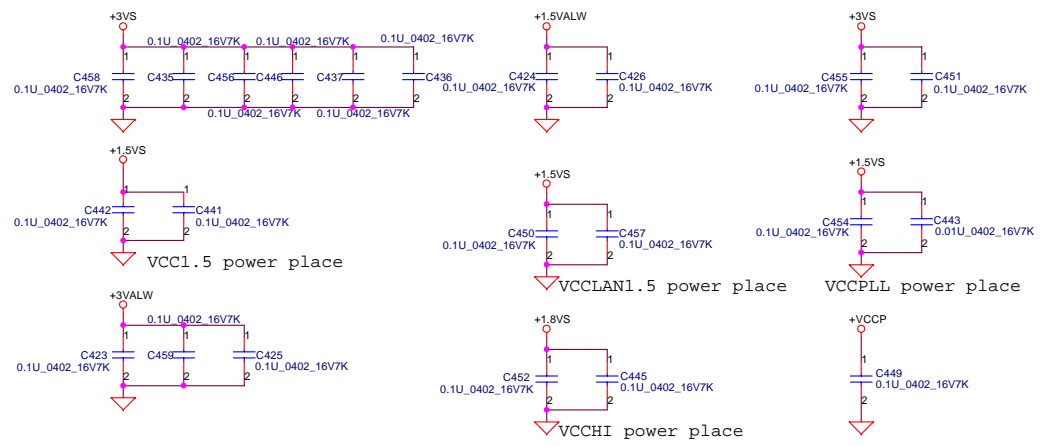


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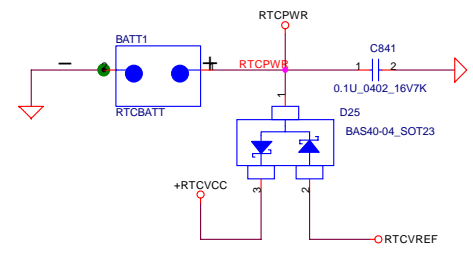
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FW82801DBM_BGA421



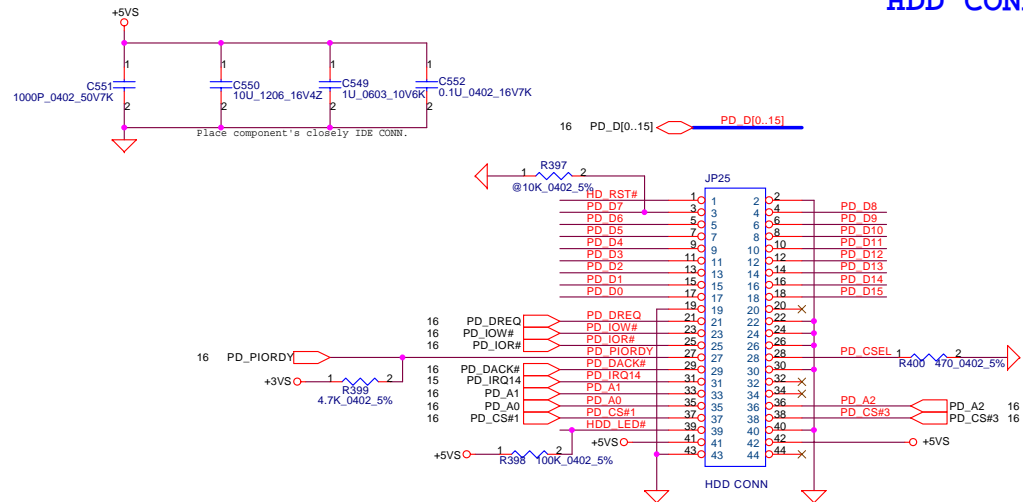
RTC Battery



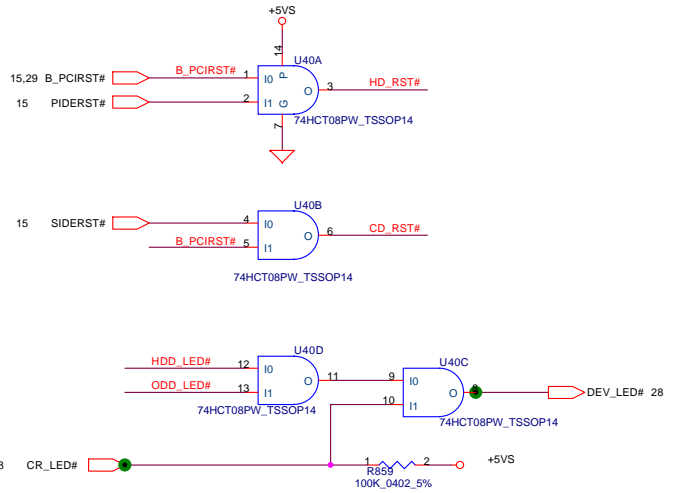
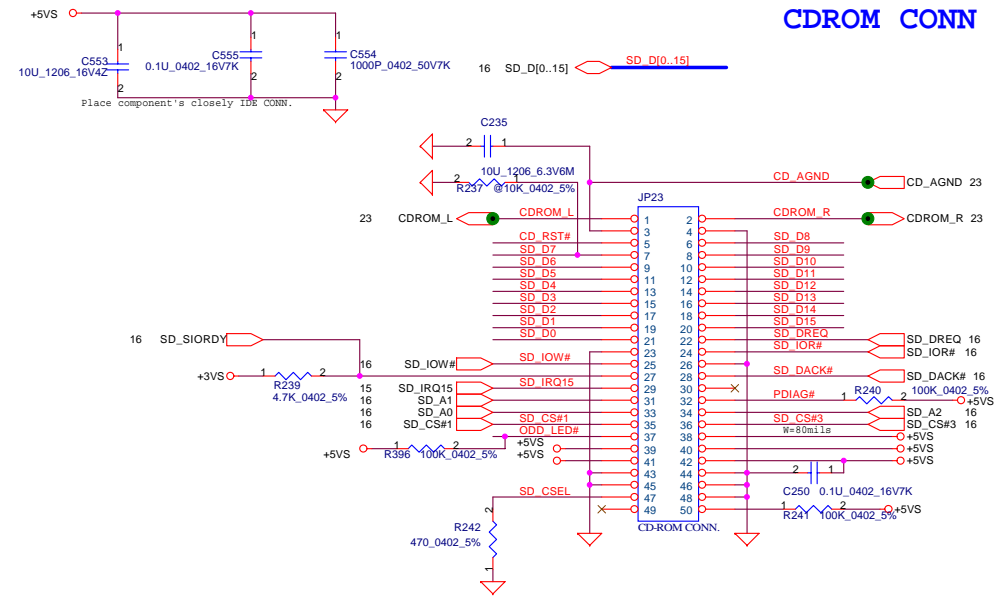
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HDD CONN

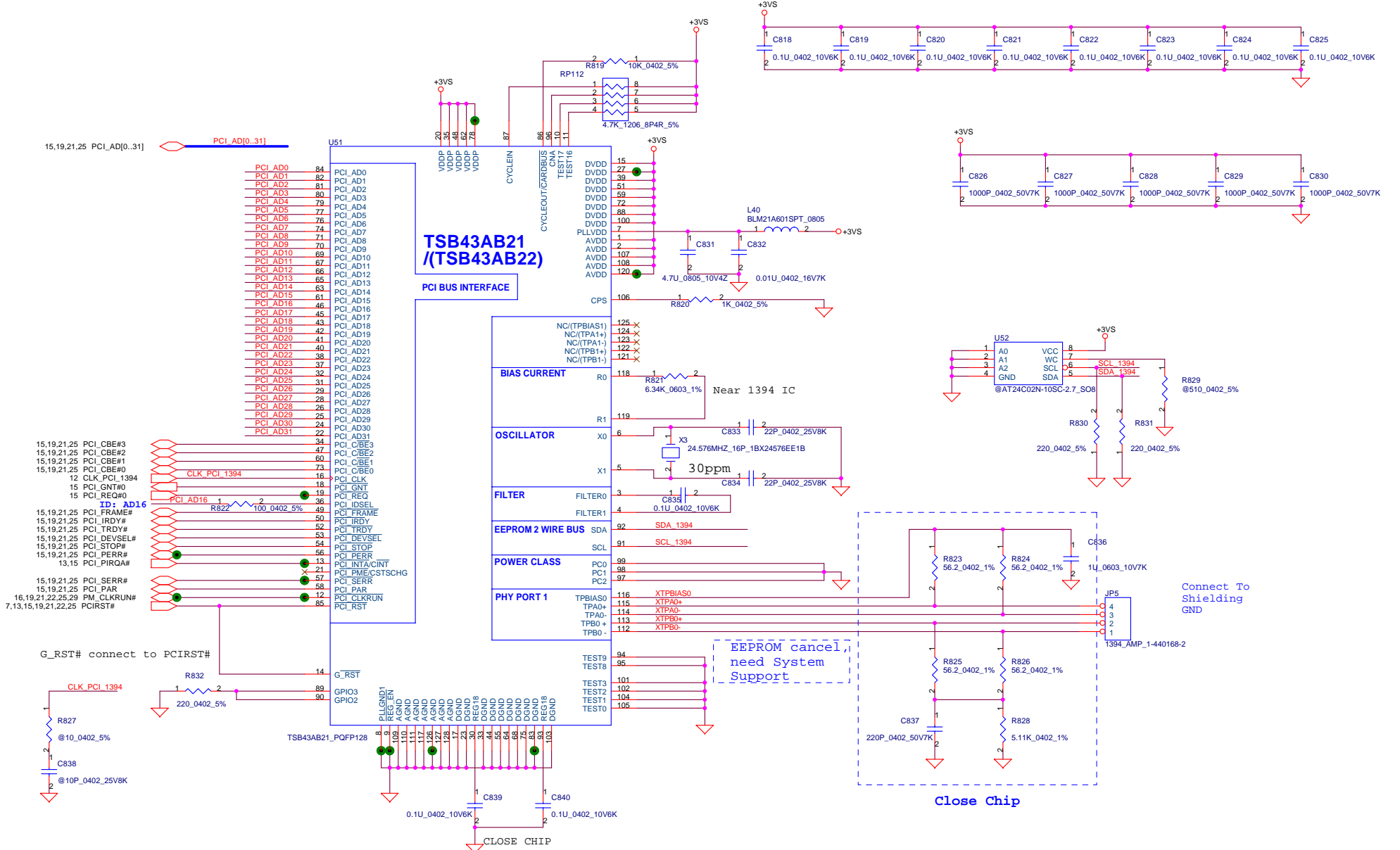


CDROM CONN



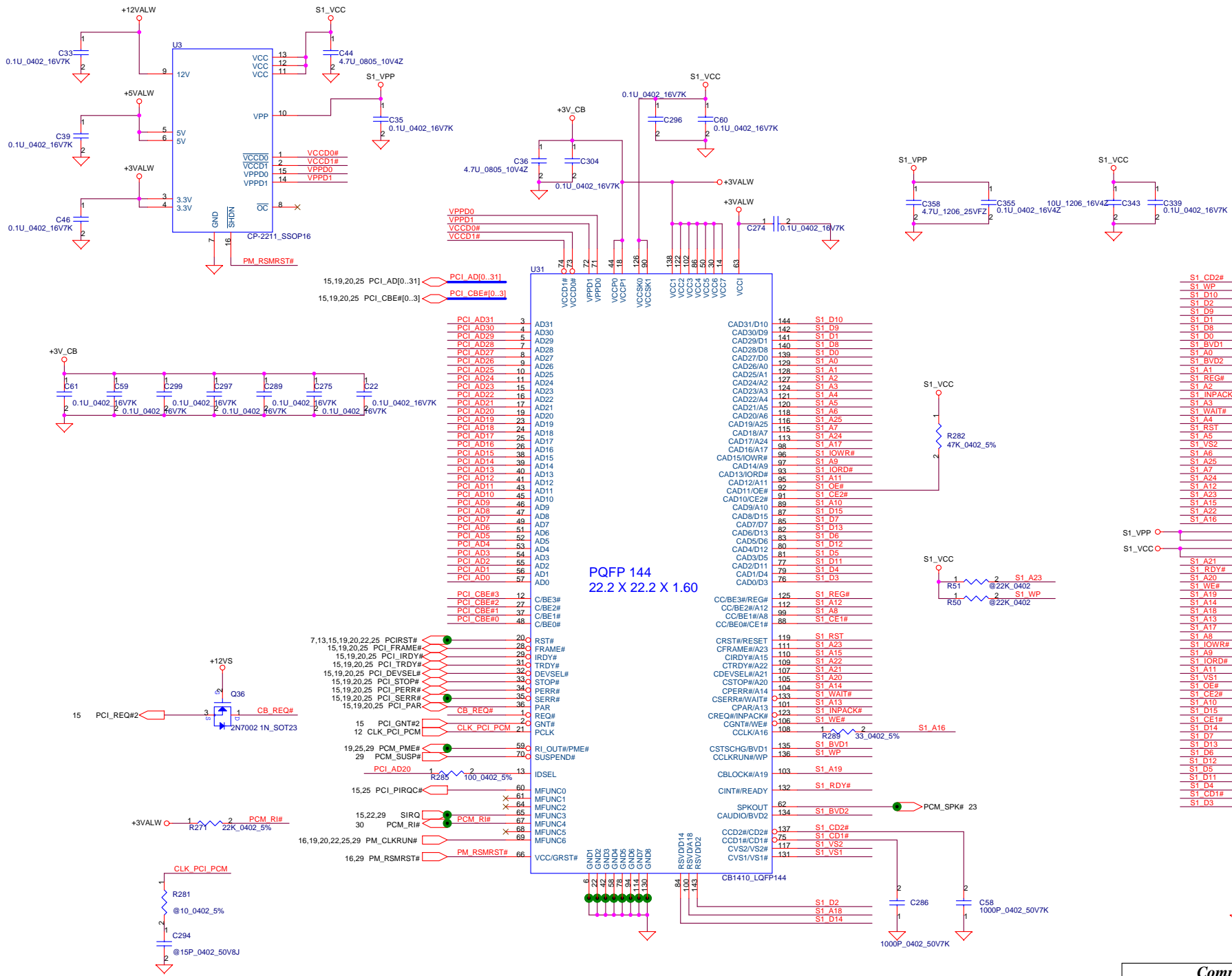
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** GPIO2 and GPIO3 defaults as an input and if it is not implemented, it is recommended that it be pulled low to ground with a 220 ohm resistor.

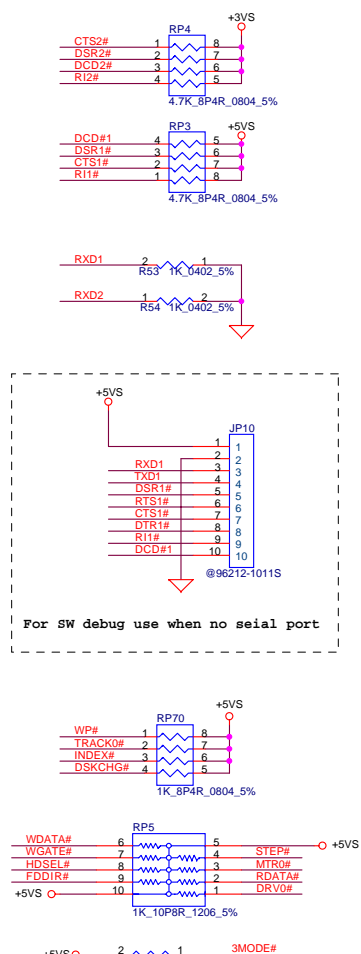
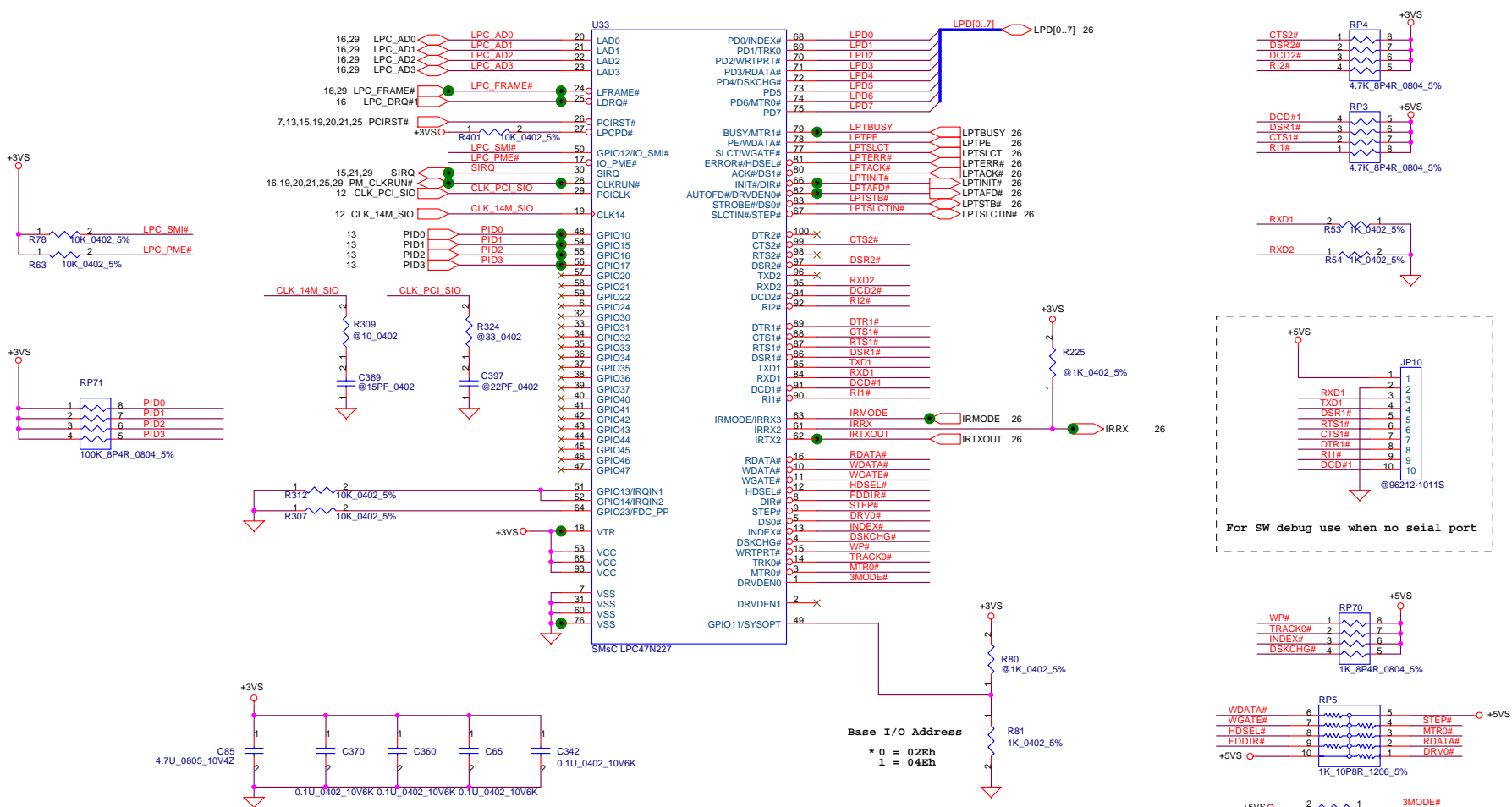
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PQFP 144
22.2 X 22.2 X 1.60

15,19,20,25	PCI_AD[0..31]	PCI AD0..31	AD0..31	144	S1 D10	S1 D10
15,19,20,25	PCI_CBE#[0..3]	PCI CBE#0..3	C/BE#0..3	142	S1 D9	S1 D9
3	PCI_AD31	AD31	AD31	141	S1 D8	S1 D8
4	PCI_AD30	AD30	AD30	140	S1 D8	S1 D8
5	PCI_AD29	AD29	AD29	139	S1 D0	S1 A0
7	PCI_AD28	AD28	AD28	129	S1 A0	S1 BVD1
8	PCI_AD27	AD27	AD27	128	S1 A1	S1 A0
10	PCI_AD26	AD26	AD26	127	S1 A2	S1 BVD2
11	PCI_AD25	AD25	AD25	124	S1 A3	S1 A1
15	PCI_AD24	AD24	AD24	121	S1 A4	S1 REG#
16	PCI_AD23	AD23	AD23	120	S1 A5	S1 A2
17	PCI_AD22	AD22	AD22	118	S1 A6	S1 A2
18	PCI_AD21	AD21	AD21	116	S1 A25	S1 INPACK#
19	PCI_AD20	AD20	AD20	115	S1 A7	S1 A2
20	PCI_AD19	AD19	AD19	114	S1 A7	S1 A2
21	PCI_AD18	AD18	AD18	113	S1 A7	S1 A2
22	PCI_AD17	AD17	AD17	98	S1 A17	S1 A2
25	PCI_AD16	AD16	AD16	96	S1 IOWR#	S1 A6
26	PCI_AD15	AD15	AD15	97	S1 A9	S1 A25
38	PCI_AD14	AD14	AD14	83	S1 IORD#	S1 A7
39	PCI_AD13	AD13	AD13	95	S1 A11	S1 A24
40	PCI_AD12	AD12	AD12	92	S1 OE#	S1 A24
41	PCI_AD11	AD11	AD11	81	S1 CE2#	S1 A12
43	PCI_AD10	AD10	AD10	89	S1 A10	S1 A23
45	PCI_AD9	AD9	AD9	87	S1 D15	S1 A15
46	PCI_AD8	AD8	AD8	85	S1 D7	S1 A22
47	PCI_AD7	AD7	AD7	82	S1 D13	S1 A19
48	PCI_AD6	AD6	AD6	83	S1 D6	S1 A18
52	PCI_AD5	AD5	AD5	81	S1 D5	S1 A21
53	PCI_AD4	AD4	AD4	77	S1 D11	S1 A20
54	PCI_AD3	AD3	AD3	79	S1 D4	S1 A15
55	PCI_AD2	AD2	AD2	76	S1 D3	S1 A16
56	PCI_AD1	AD1	AD1	125	S1 REG#	S1 A21
57	PCI_AD0	AD0	AD0	112	S1 A12	S1 RDY#
12	PCI_CBE#3	C/BE#3	C/BE#3	99	S1 A3	S1 A20
27	PCI_CBE#2	C/BE#2	C/BE#2	88	S1 CE1#	S1 WE#
37	PCI_CBE#1	C/BE#1	C/BE#1	119	S1 RST	S1 A19
48	PCI_CBE#0	C/BE#0	C/BE#0	111	S1 A23	S1 A14
20	RST#	RST#	RST#	110	S1 A15	S1 A18
28	FRAME#	FRAME#	FRAME#	109	S1 A22	S1 A13
29	CI RDY#	CI RDY#	CI RDY#	107	S1 A21	S1 A17
31	TRDY#	TRDY#	TRDY#	106	S1 A20	S1 A8
32	DEVSEL#	DEVSEL#	DEVSEL#	104	S1 A14	S1 D15
33	STOP#	STOP#	STOP#	101	S1 A13	S1 D14
34	PERR#	PERR#	PERR#	108	S1 WE#	S1 D7
35	SERR#	SERR#	SERR#	135	S1 BVD1	S1 D13
36	PAR#	PAR#	PAR#	136	S1 WP	S1 D6
1	REQ#	REQ#	REQ#	103	S1 A19	S1 D12
2	GNT#	GNT#	GNT#	132	S1 RDY#	S1 D5
1	CLK PCI_PCM	CLK PCI_PCM	CLK PCI_PCM	62	S1 SPKOUT	S1 D11
12	CLK_PCI_PCM	CLK_PCI_PCM	CLK_PCI_PCM	134	S1 BVD2	S1 D4
59	RI_OUT#/PME#	RI_OUT#/PME#	RI_OUT#/PME#	137	S1 CD2#	S1 D3
70	SUSPEND#	SUSPEND#	SUSPEND#	75	S1 CD1#	S1 D2
13	IDSEL	IDSEL	IDSEL	117	S1 VS2	S1 A18
60	MFUNC0	MFUNC0	MFUNC0	131	S1 VS1	S1 D14
61	MFUNC1	MFUNC1	MFUNC1	84	RSV/DD14	S1 D2
64	MFUNC2	MFUNC2	MFUNC2	100	RSV/DD2	S1 A18
65	MFUNC3	MFUNC3	MFUNC3	143	RSV/DD2	S1 D14
67	MFUNC4	MFUNC4	MFUNC4	2	C286	1000P_0402_50V7K
68	MFUNC5	MFUNC5	MFUNC5	1	C58	1000P_0402_50V7K
69	MFUNC6	MFUNC6	MFUNC6	2	C286	1000P_0402_50V7K
16,19,20,22,25,29	PM_CLKRUN#	PM_CLKRUN#	PM_CLKRUN#	84	RSV/DD14	S1 D2
16,29	PM_RSMRST#	PM_RSMRST#	PM_RSMRST#	100	RSV/DD2	S1 A18
13	PM_RSMRST#	PM_RSMRST#	PM_RSMRST#	143	RSV/DD2	S1 D14

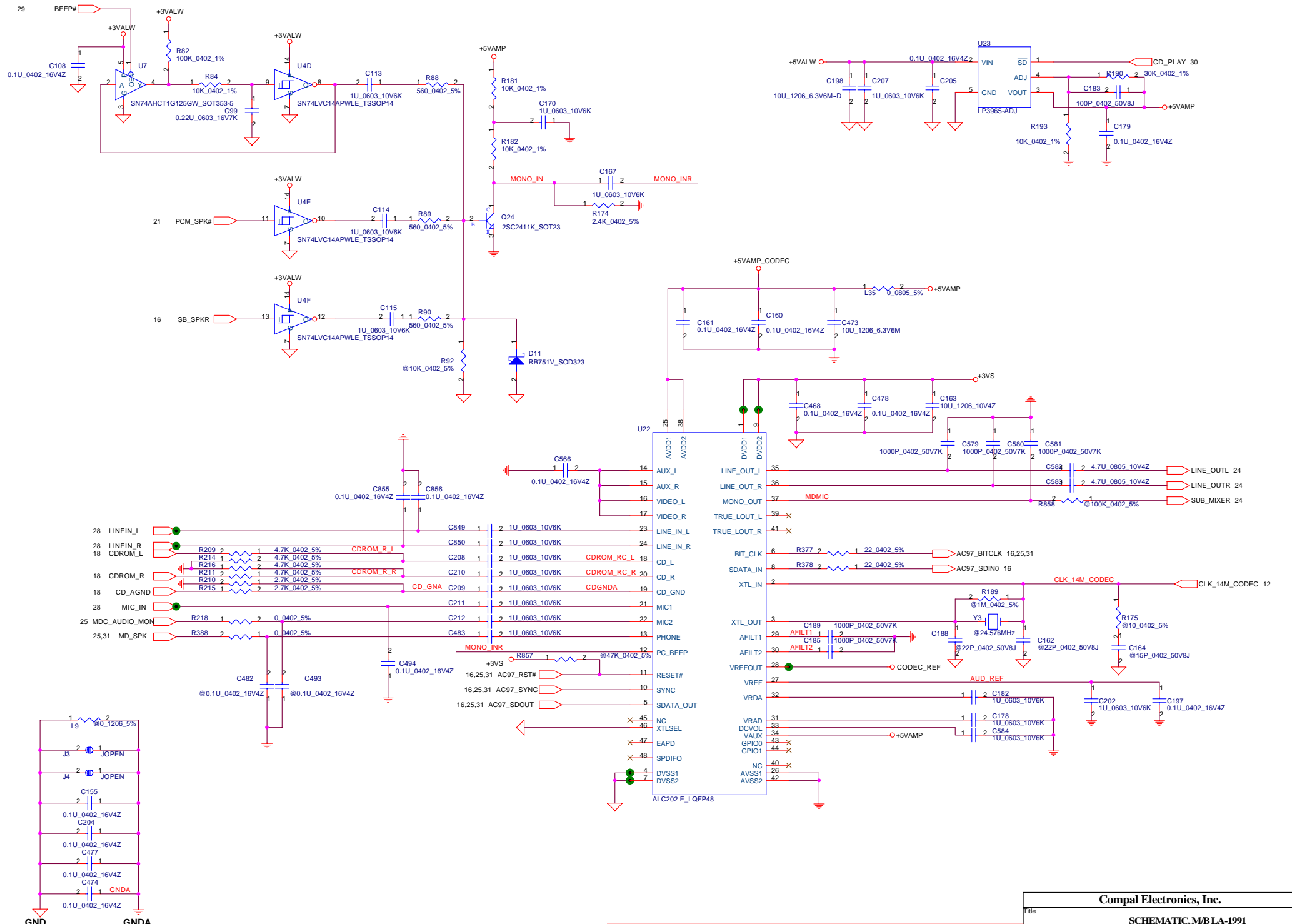
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For SW debug use when no serial port

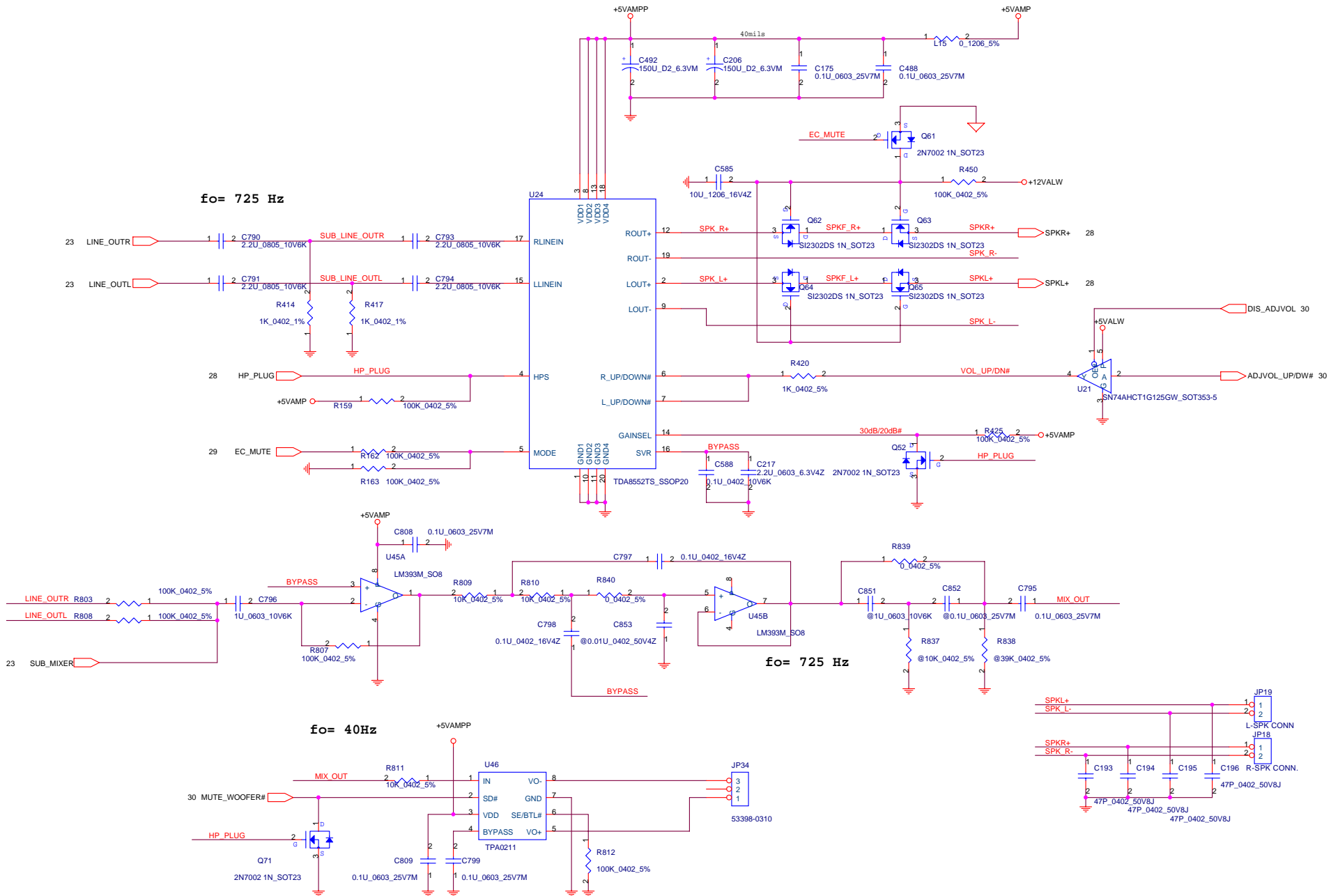
Base I/O Address
 * 0 = 02Eh
 1 = 04Eh

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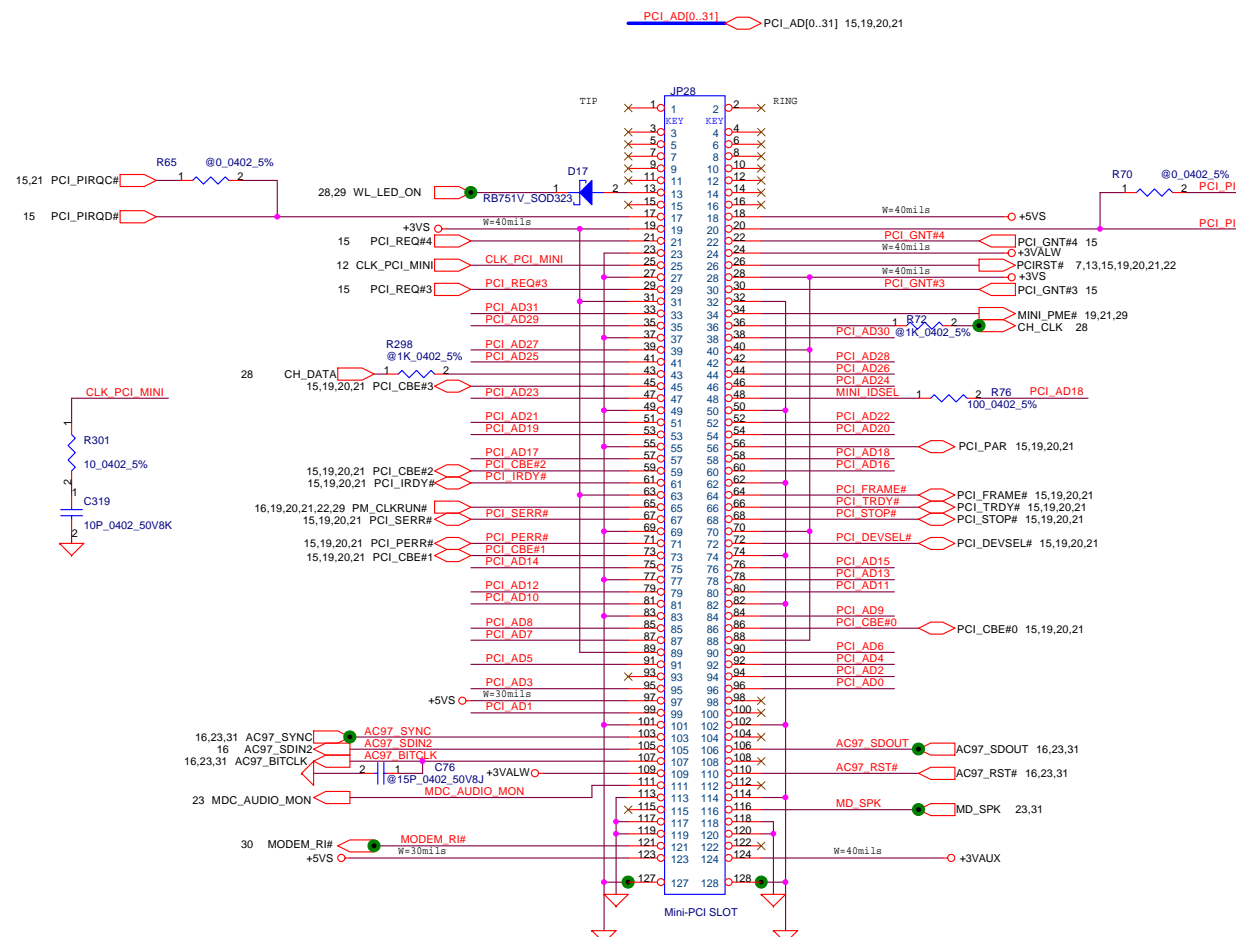
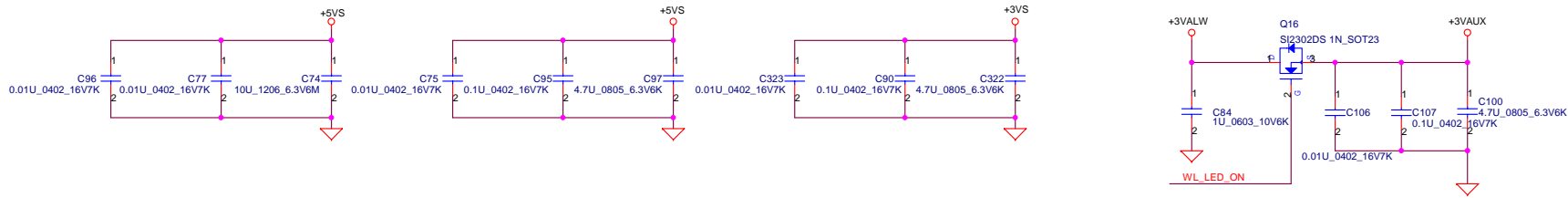
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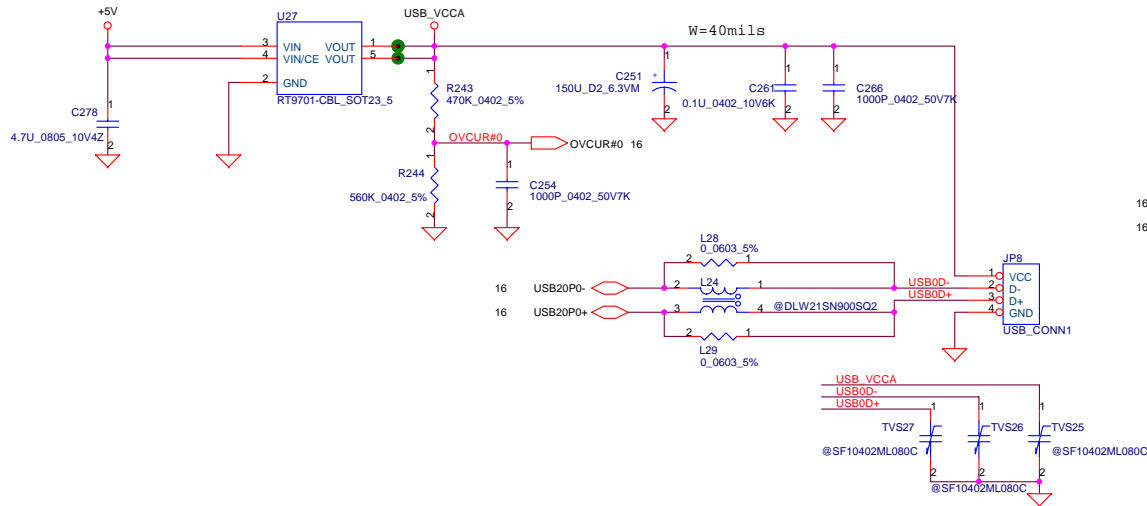
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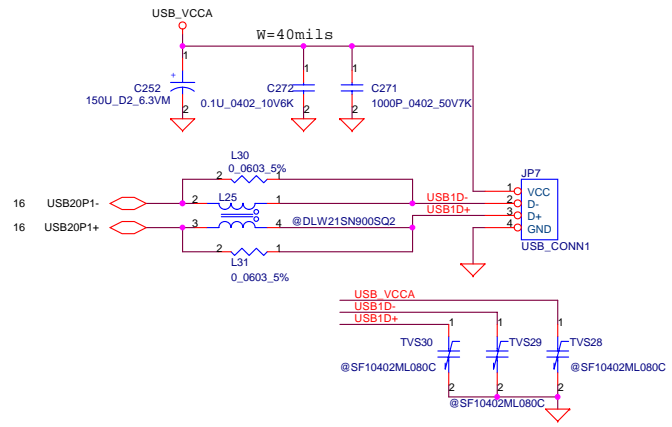
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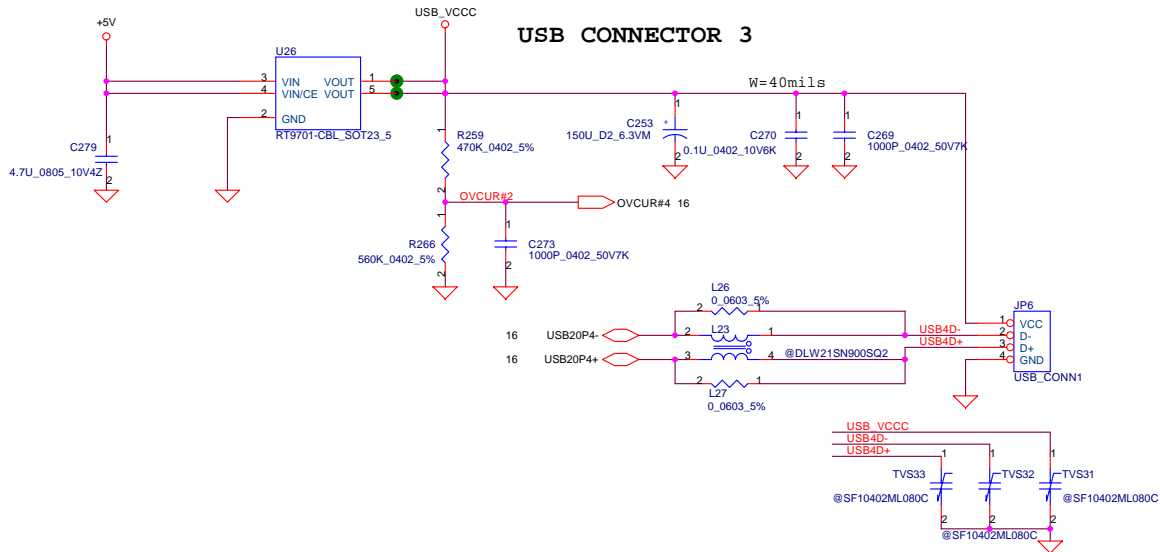
USB CONNECTOR 1



USB CONNECTOR 2



USB CONNECTOR 3



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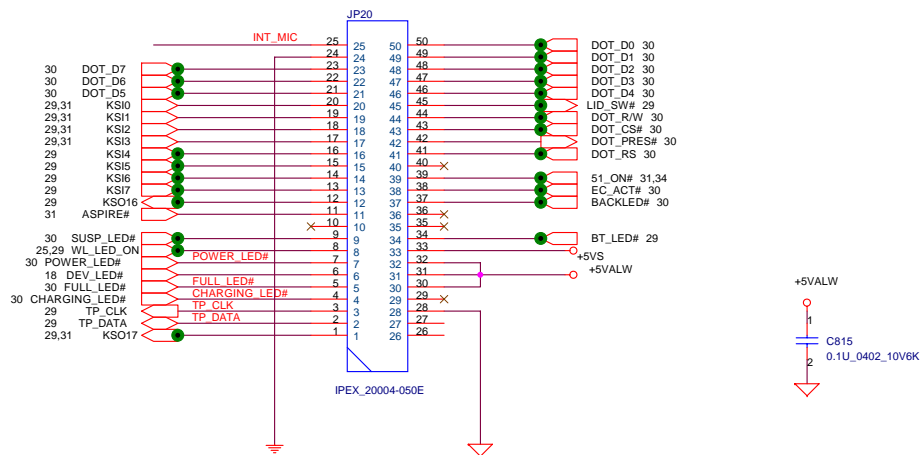
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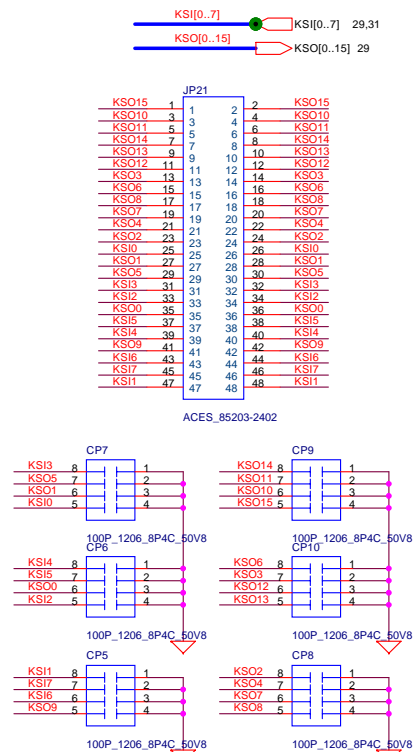
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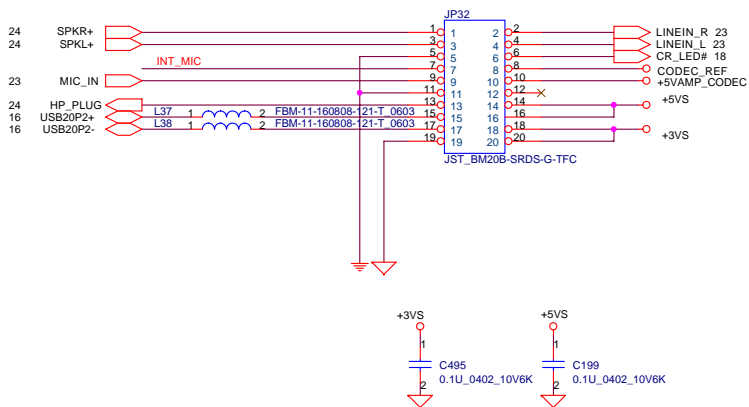
T/P & LED CONN.



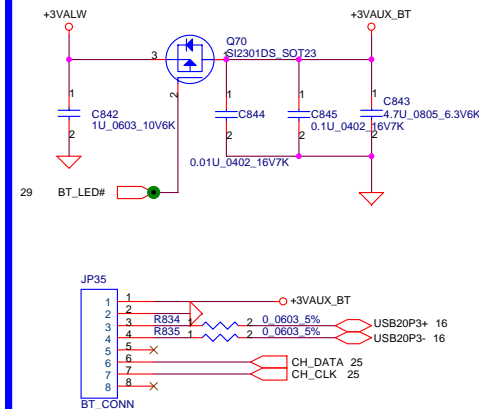
INT_KBD CONN.



CardReader CONN.



BT_CONN



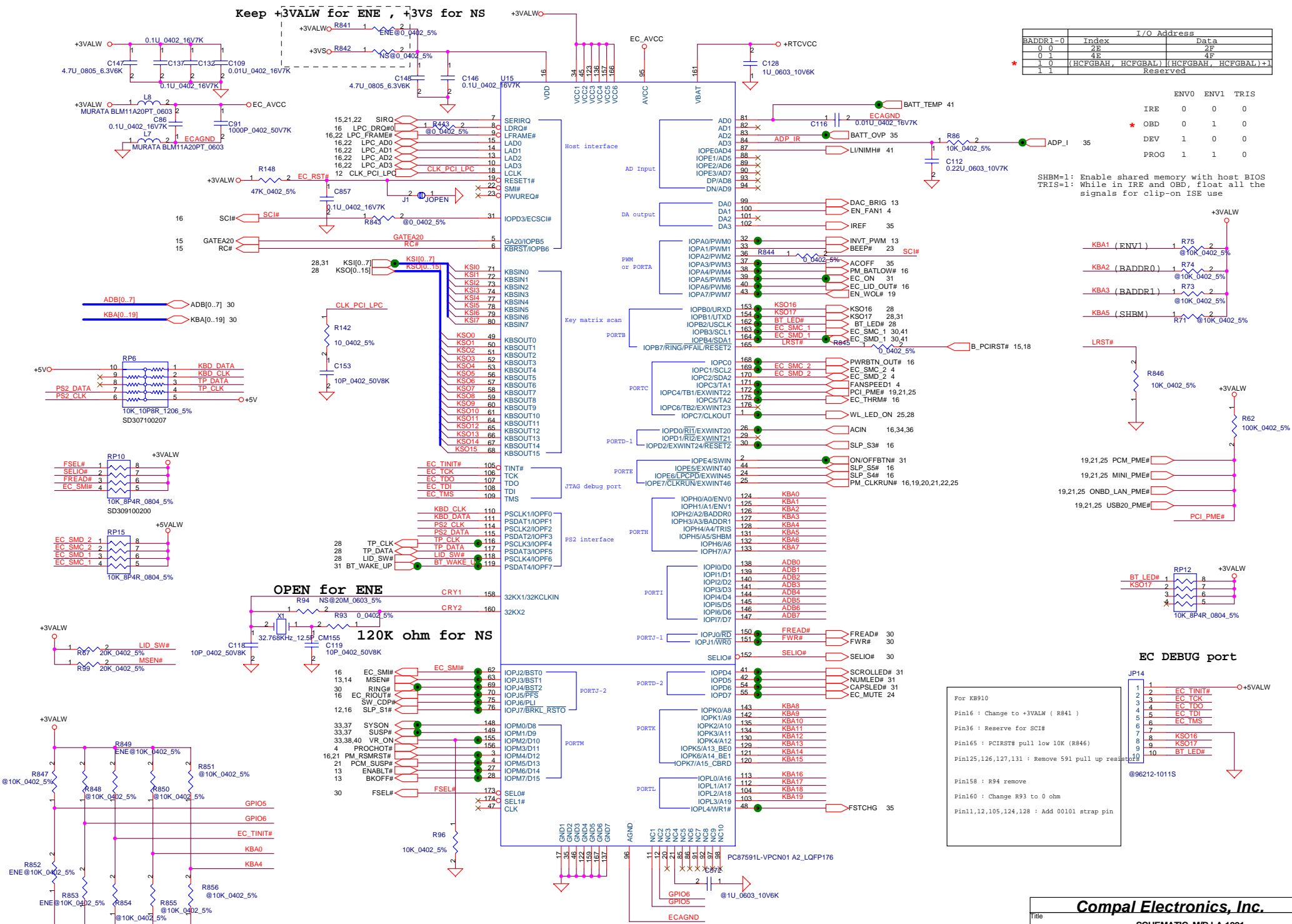
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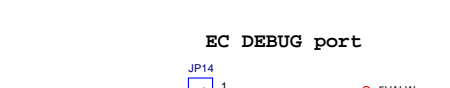
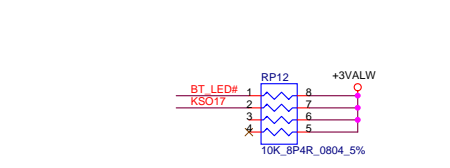
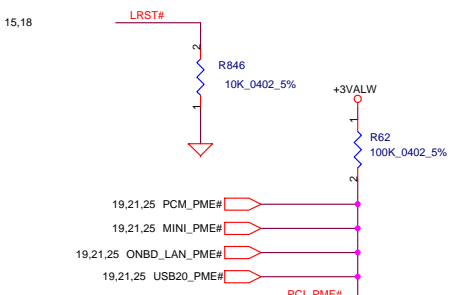
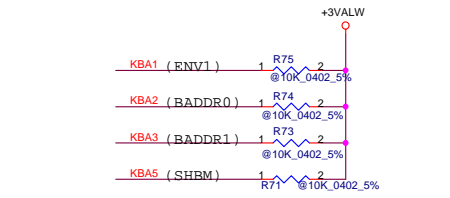
Keep +3VALW for ENE, +3VS for NS

BADDR1-0	Index	I/O Address	Data
0 0	2E		2F
0 1	4E		4F
1 0		{HCFGBAH, HCFGBAL HCFGBAH, HCFGBAL}+1	
1 1		Reserved	



ENVO	ENVI	TRIS
IRE	0	0
OBD	0	1
DEV	1	0
PROG	1	1

SHBM=1: Enable shared memory with host BIOS
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



For KB910
 Pin16 : Change to +3VALW (R841)
 Pin36 : Reserve for SCI#
 Pin165 : PCIRST# pull low 10K (R846)
 Pin125,126,127,131 : Remove 591 pull up resistor
 Pin158 : R94 remove
 Pin160 : Change R93 to 0 ohm
 Pin11,12,105,124,128 : Add 00101 strap pin

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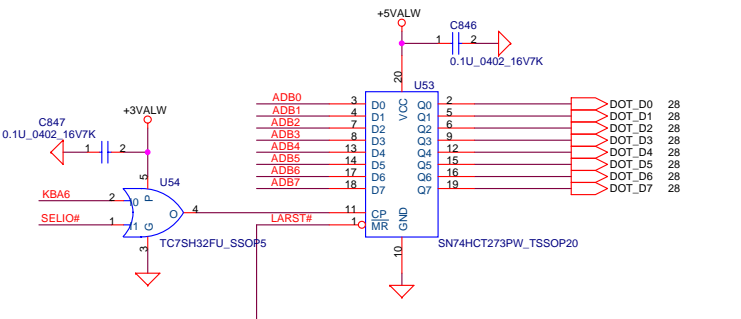
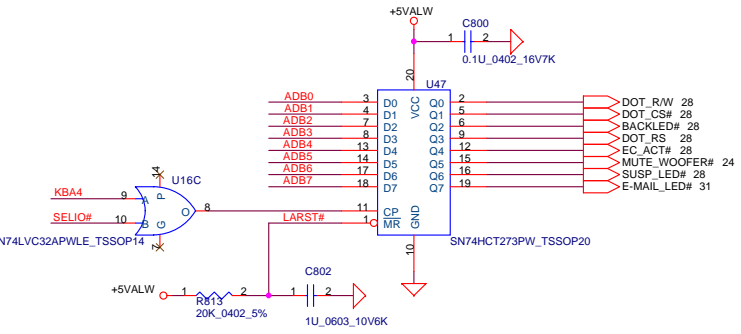
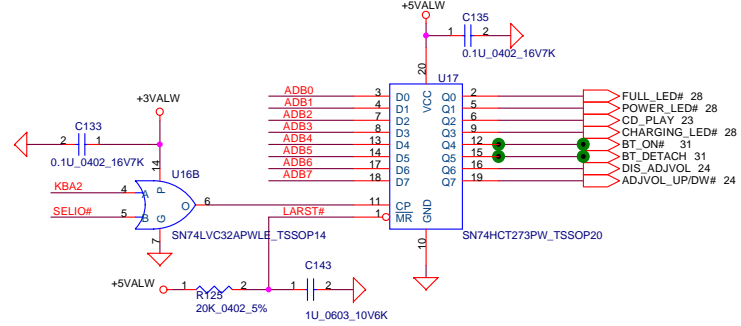
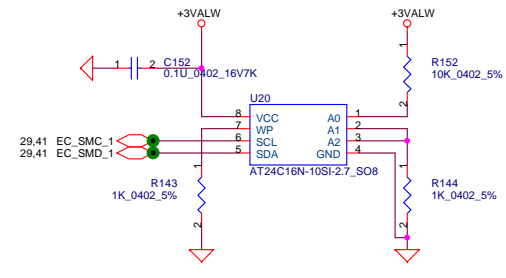
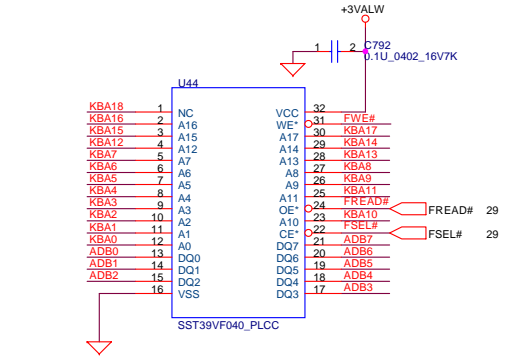
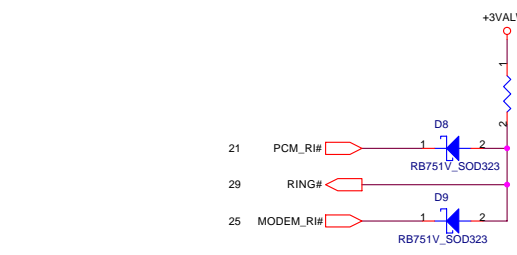
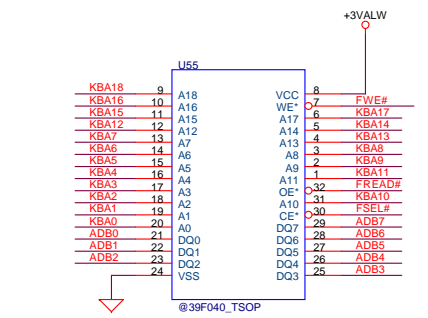
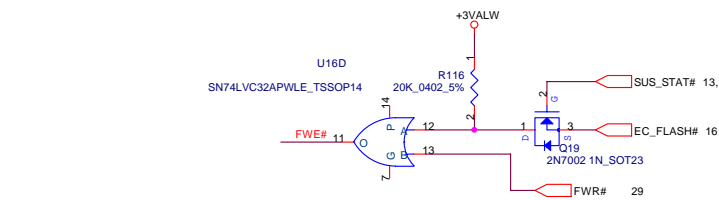
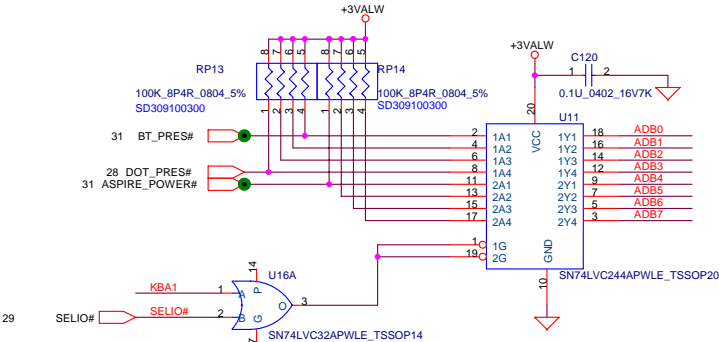
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INPUT

29 KBA[0..19]
29 ADB[0..7]

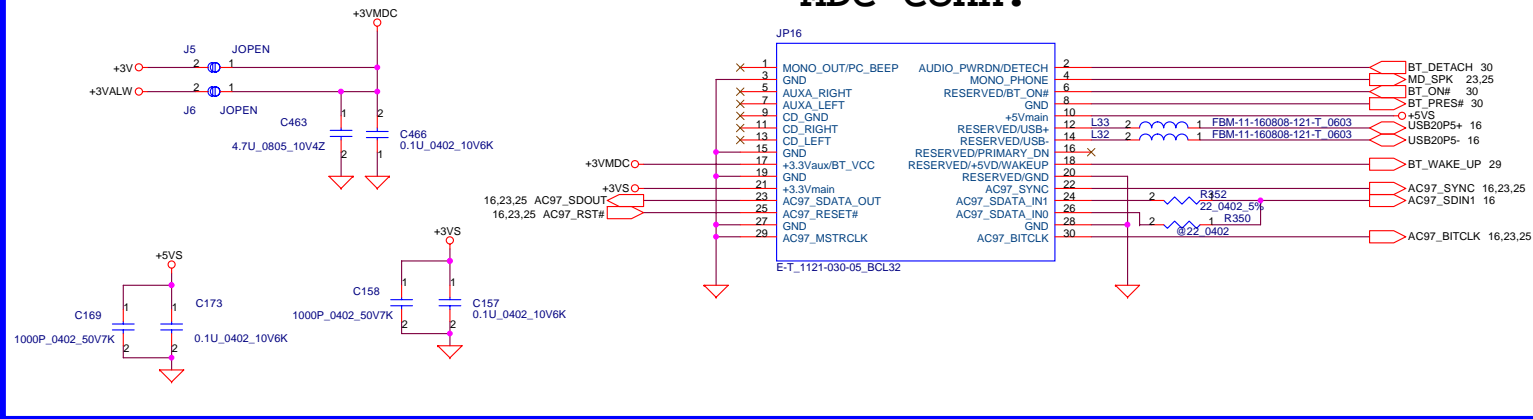
OUTPUT



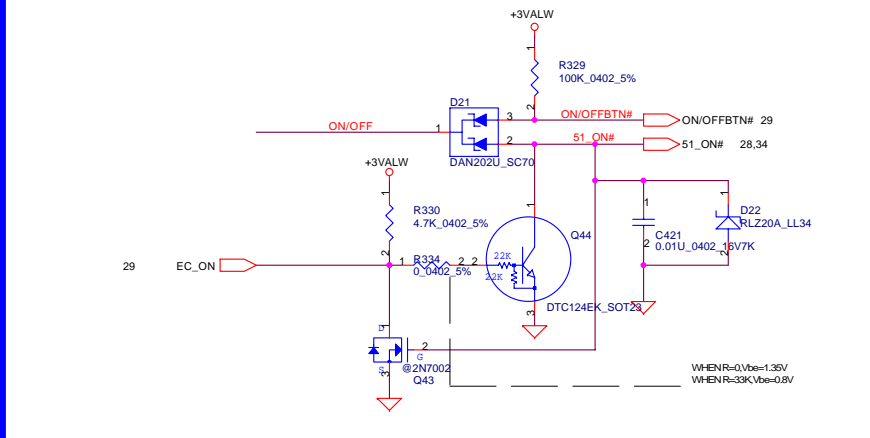
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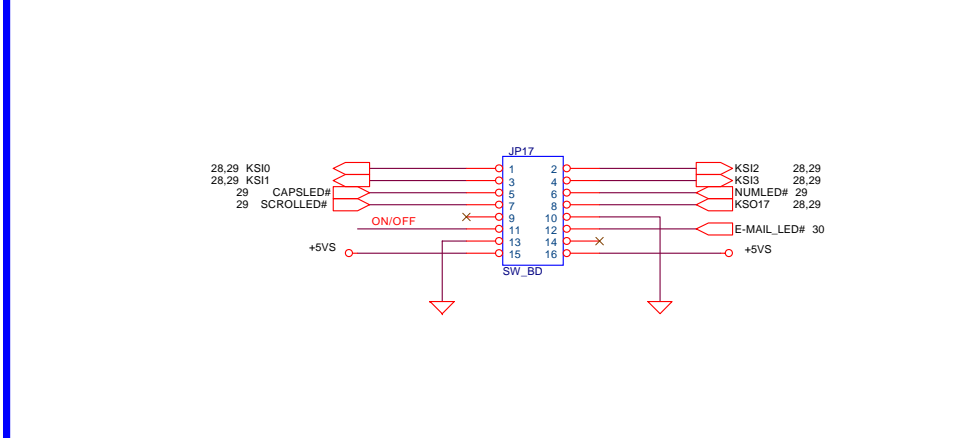
MDC Conn.



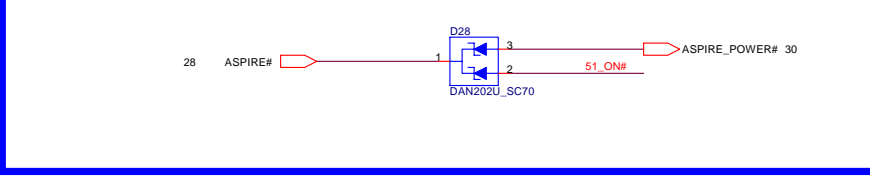
ON/OFF BUTTON



SWITCH CONN

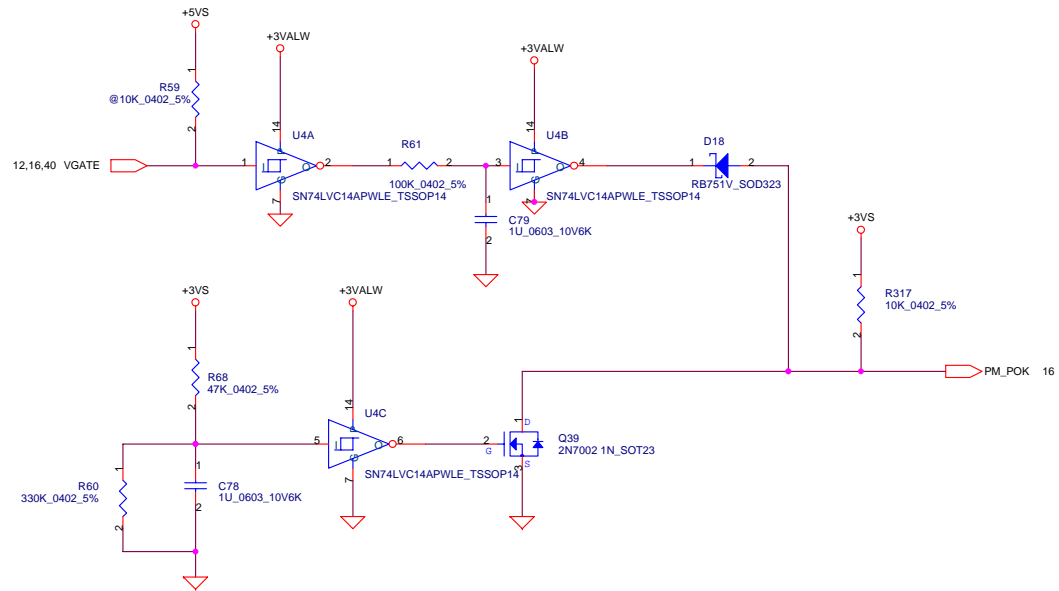


ASPIRE POWER



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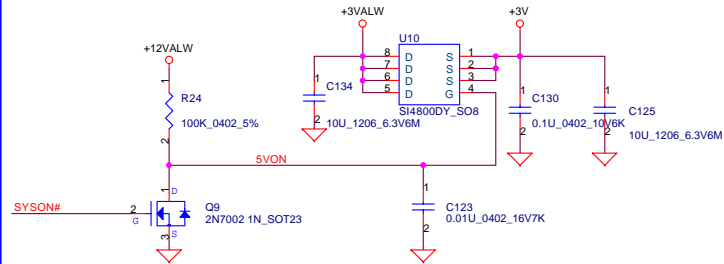
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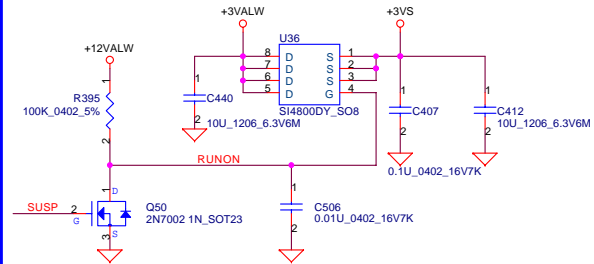
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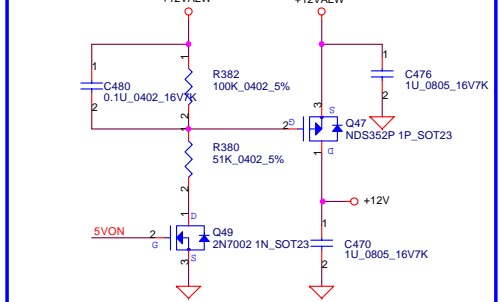
+3VALW to +3V Transfer



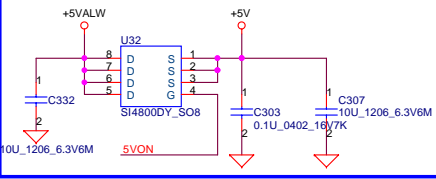
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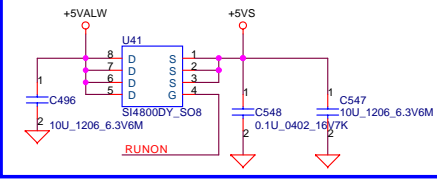
+12VALW TO +12V Transfer

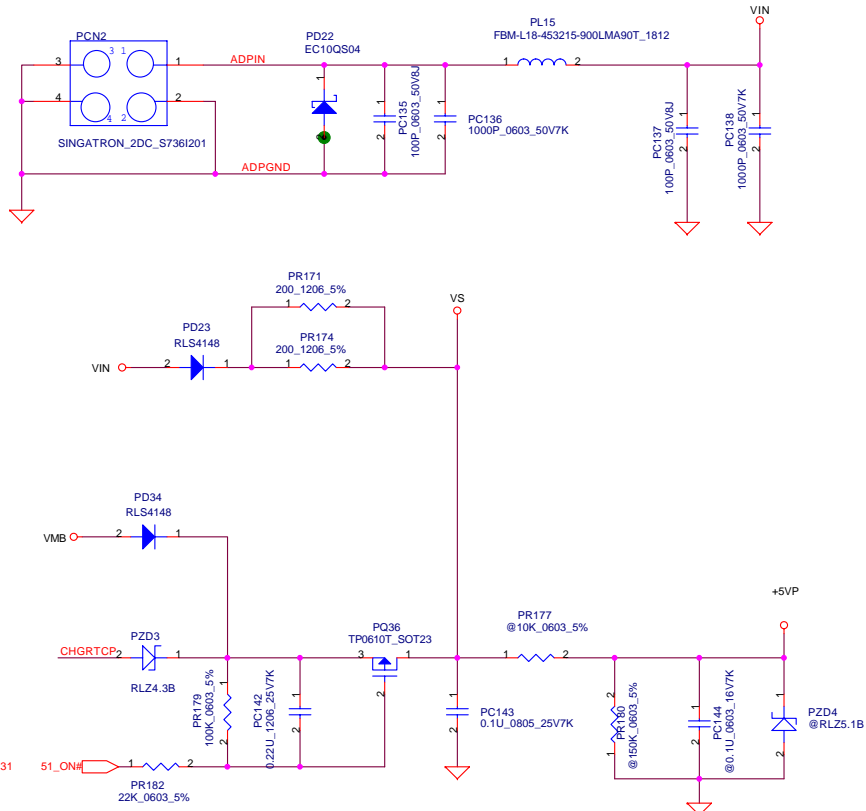


+5VALW to +5V Transfer

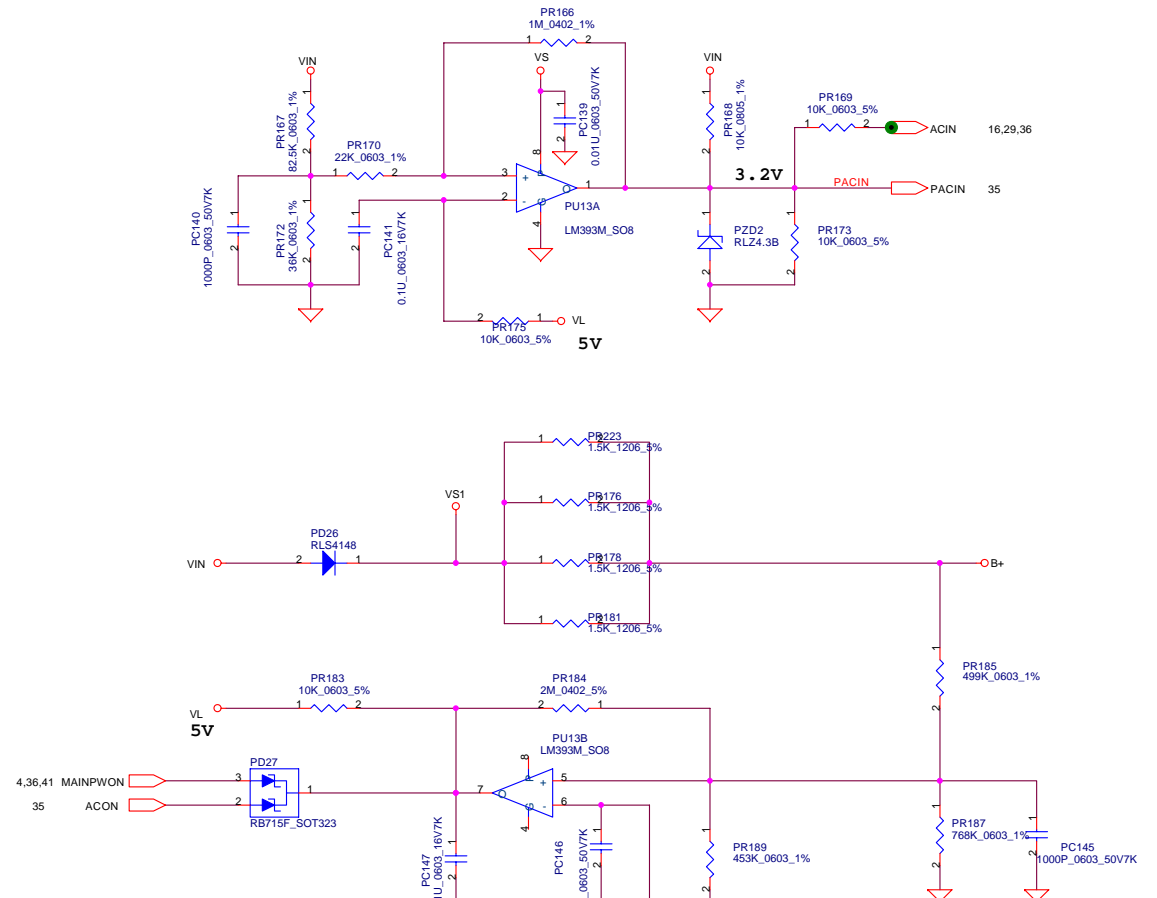


+5VALW to +5VS Transfer



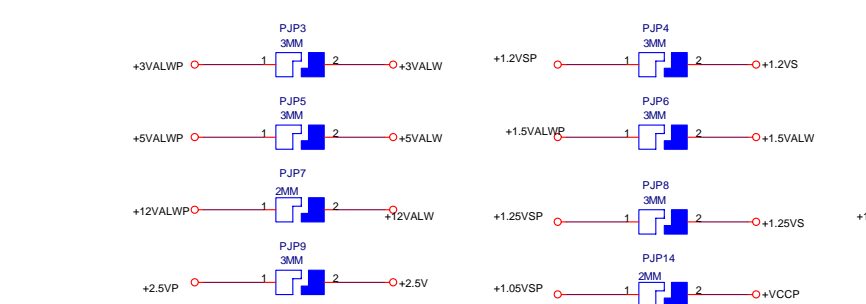
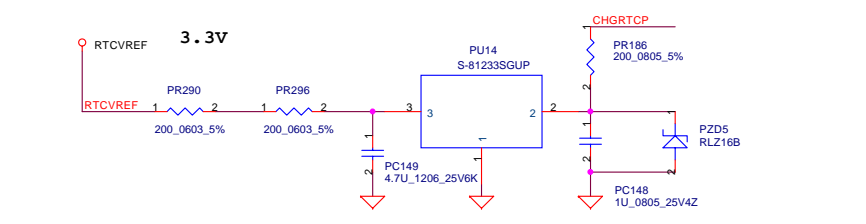


VIN detector		
17.905	17.233	16.587
17.391	16.737	16.073



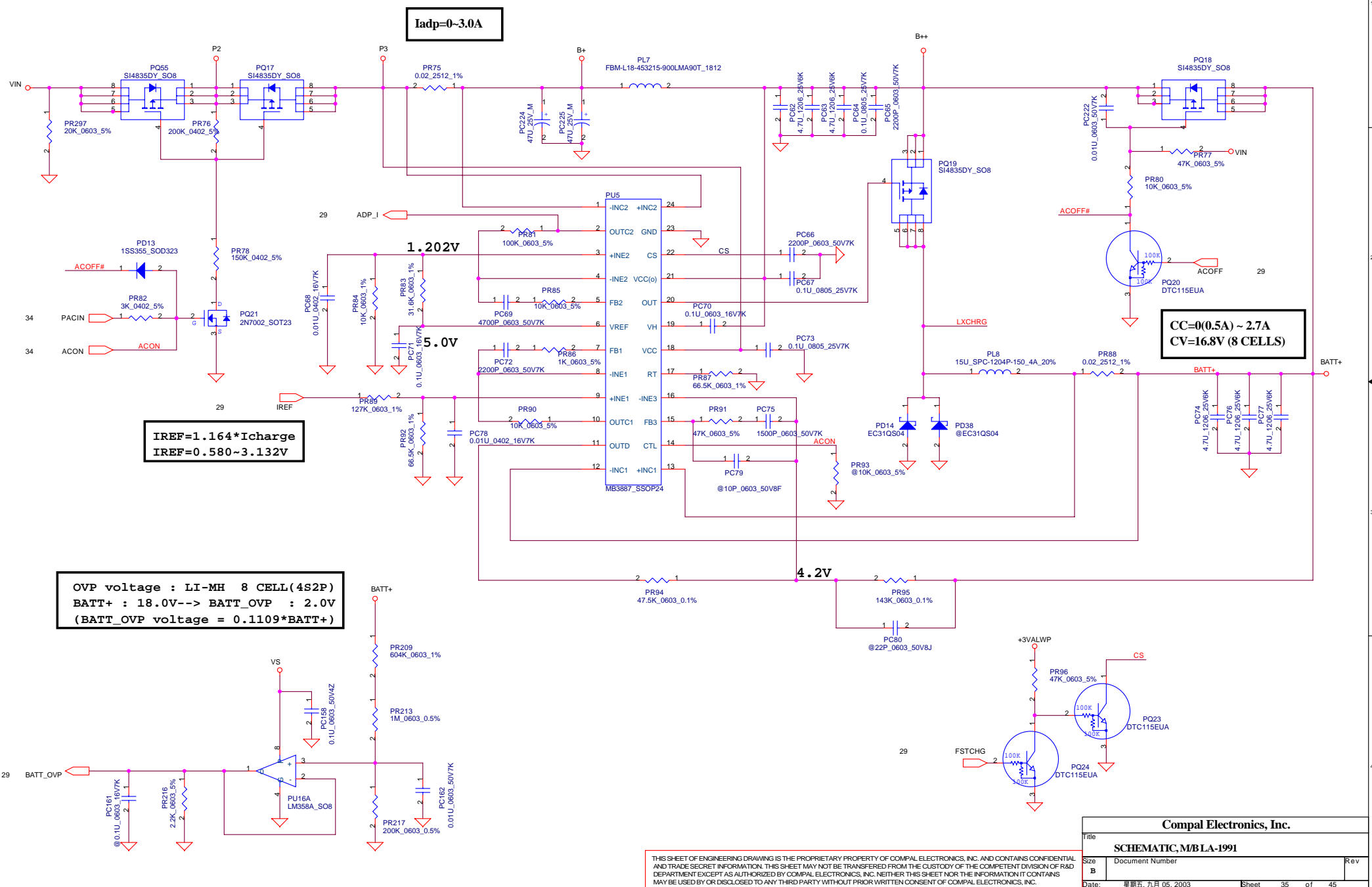
ACIN		
Precharge detector		
15.571	15.004	14.450
14.235	13.756	13.165

BAT ONLY		
Precharge detector		
9.817	9.496	9.181
8.481	8.249	7.896



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I_{adp}=0~3.0A

I_{REF}=1.164*I_{charge}
I_{REF}=0.580~3.132V

1.202V

5.0V

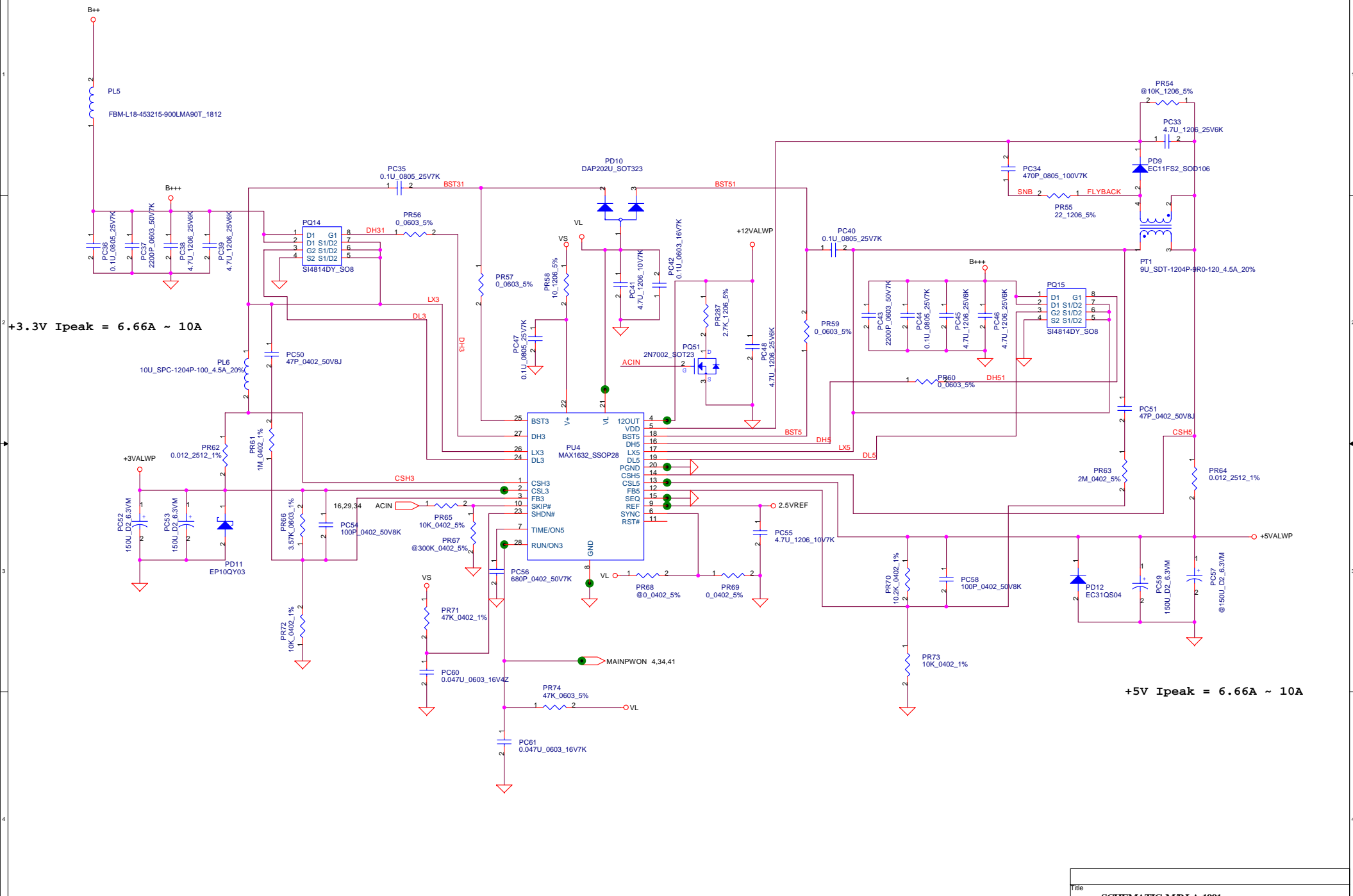
4.2V

CC=0(0.5A) ~ 2.7A
CV=16.8V (8 CELLS)

OVP voltage : LI-MH 8 CELL(4S2P)
BATT+ : 18.0V--> BATT_OVP : 2.0V
(BATT_OVP voltage = 0.1109*BATT+)

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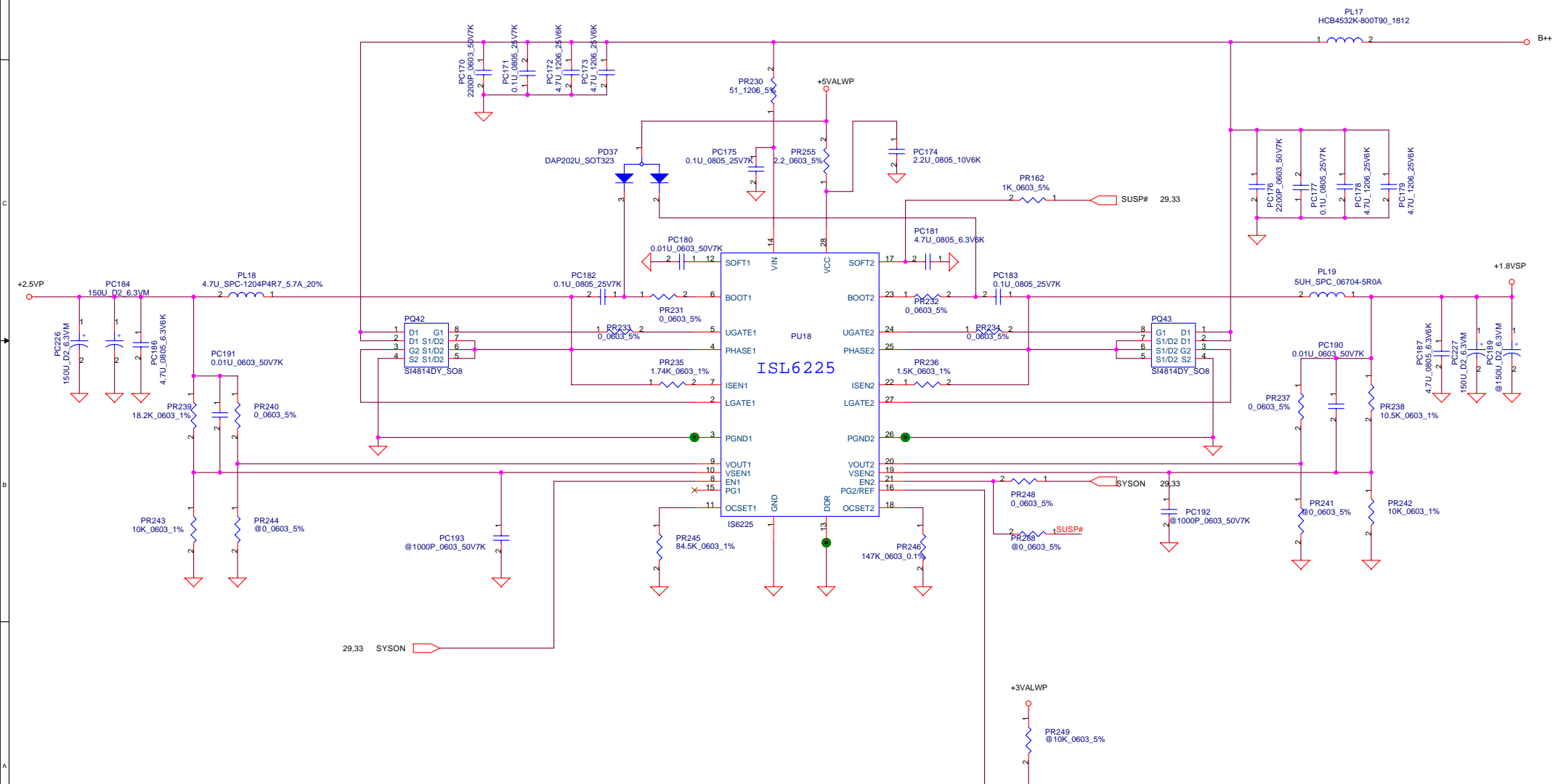
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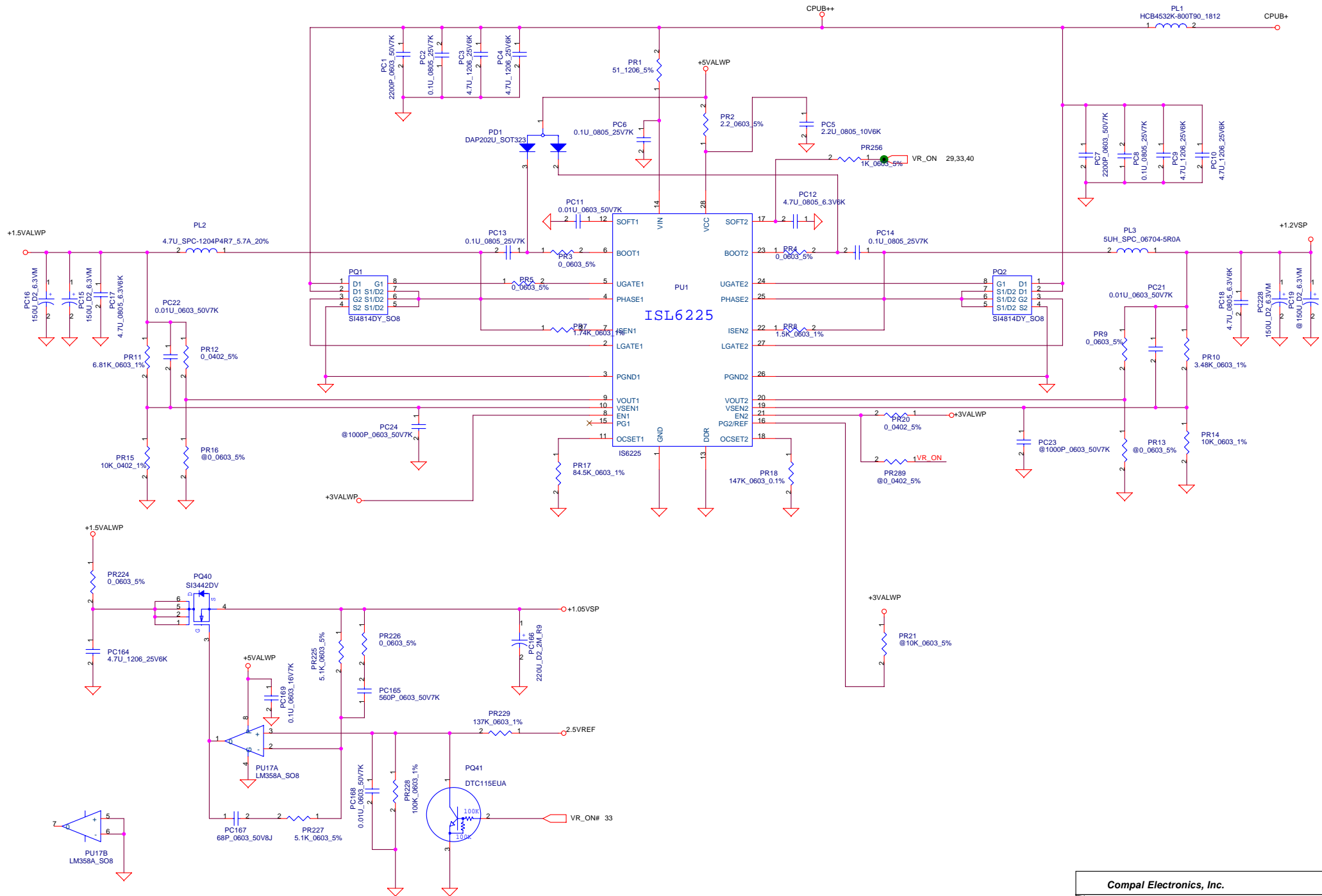
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+2.5VP/+1.8VSP



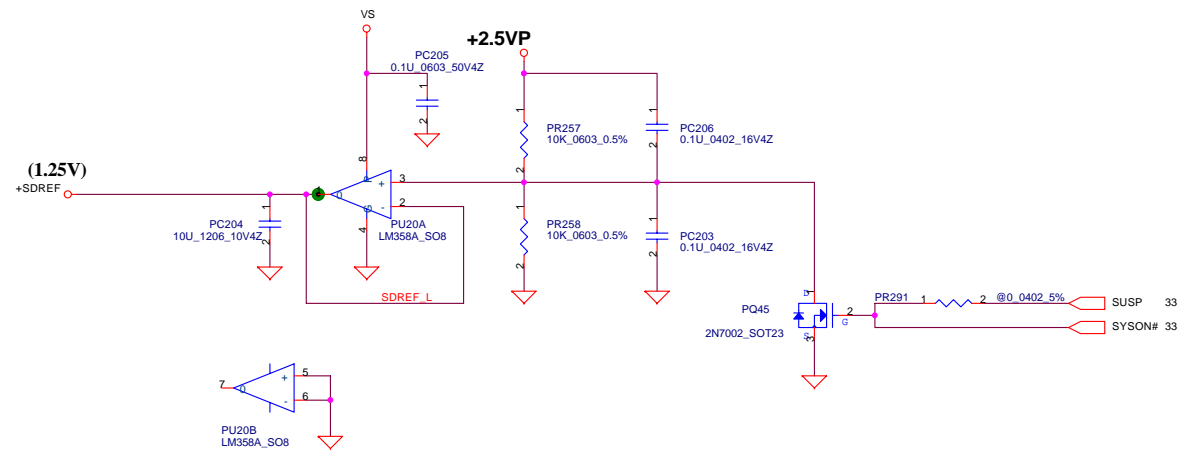
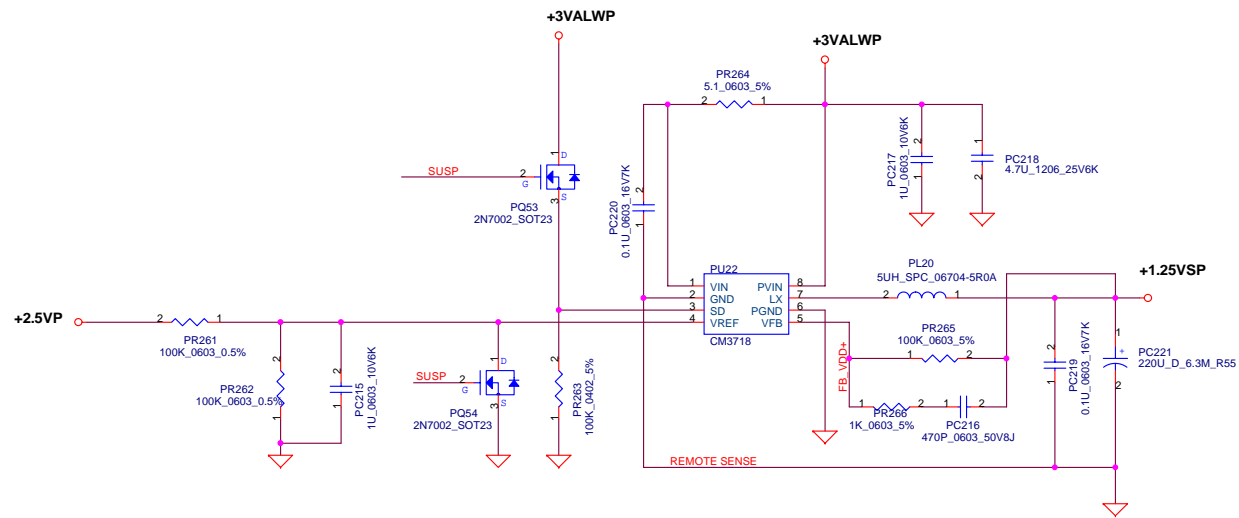
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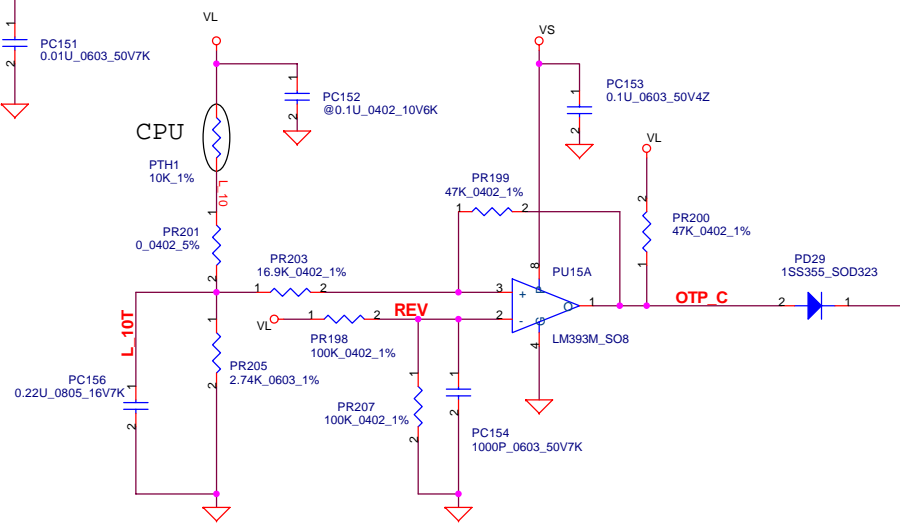
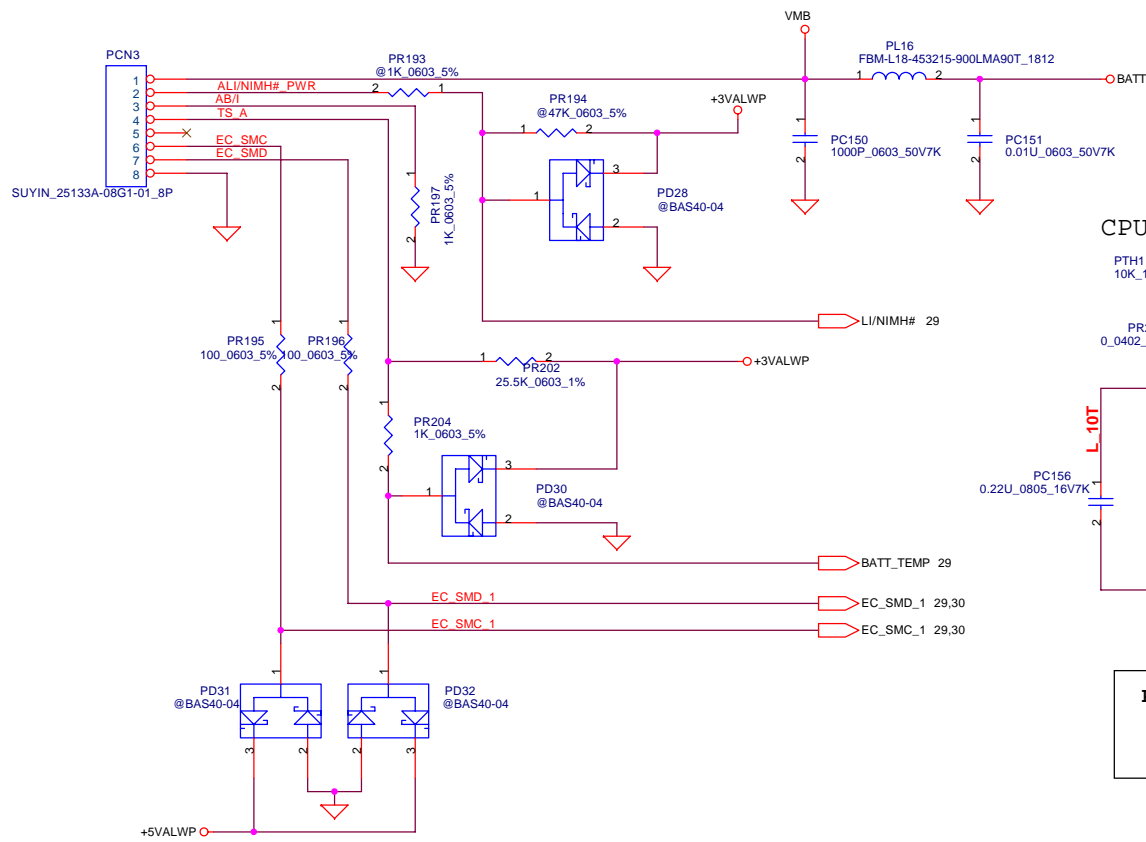
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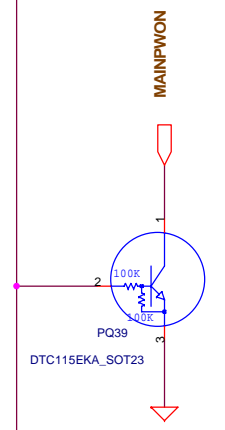
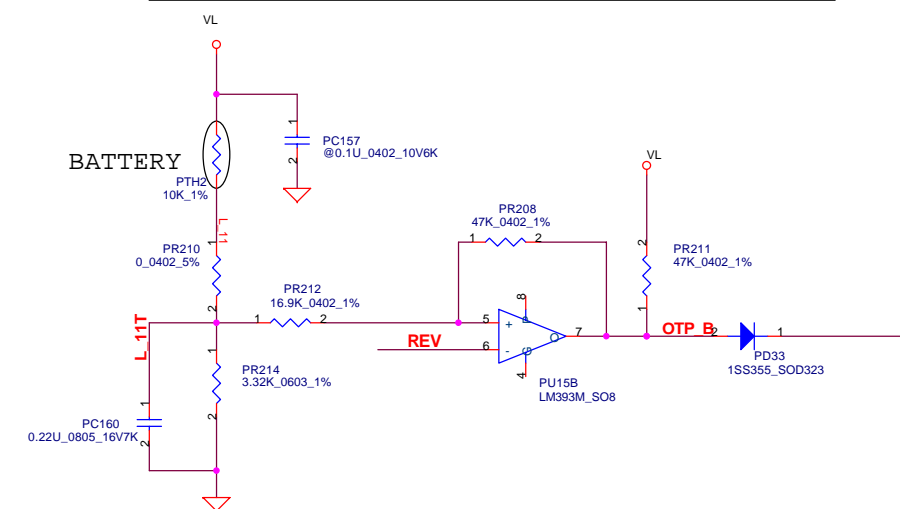
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PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 84 +/-3 degree C
 Recovery at 45 +/-3 degree C



4.34.36

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A1-TEST 2003/05/28

1. P18 : Add C854 1U_0603
2. P23 : Add C849,C850 1U_0603 for LINEIN
3. P24 :
 1. Add Q71 2N7002 for mute sub woofer
 2. Add R839 0_0402 for pass through
 3. C795 change to 0.1U_0603
 4. R809, R810 change to 10K_0402
 5. Add R840,C853,C851,C852,R838 for reserve
4. P25 : Q16 change to SI2302_N for high active signal
5. P29 : Change from NS87591L to KB910
 - A. Add R841,R843,R845 0_0402
 - B. Add R846,R852,R853,R849,R855,R851 10K_0402
 - C. Delete R94 ,R93, R71,R73,R75

A2-TEST 2003/05/28

1. P29 : Remove R841 , Add R71
2. P23 : Add C855,C856= 0.1U_0402

B-regression TEST 2003/09/02

1. P29 : Add C857
2. P31: Add D28

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4

3

2

1

D

D

C

C

B

B

A

A

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4

3

2

1

REV: 0.2D

1. To change the mute circuitry for SI build.
 - a. Connect EAPD (pin U22:47) to JP24.2 and reserve a 0_0402_5% (R431) resistor for testing.
 - b. Install R162 (0_0402_5%) and no install R163.
 - c. Add R432 (100K_0402_5%) and Q51 (2N7002) to invert EAPD signal for amplifier and mute LED.

REV: 0.2E

1. For EMI requirement.
Add C204 0.1U_0402_16V4Z
2. To exchange TP and PS2 signals for EC requirement.
3. For cost down plan.
To exchange the capacitor of C83,C136 from 150U_D2_6.3VM to 100U_6.3V_M.

REV: 0.2F

1. For cost down plan.
Move audio line-out BLOCK capacitor from TP to MB. To add C565,C566 100U_6.3V_M.
2. For solving audio noise when IR active. (A2C039)
 - a. Del C206.
 - b. To change C492 from 150U_D2_6.3VM to 10U_1206_6.3V7K.
3. For EMI requirement.
Add R435~R440 0_0402_5%.

REV: 0.2G

1. For solving power LED signal wrong on PR/APR side.
 - a. Add R441 1K_0402_5%.
 - b. Q52 2N7002.
2. For solving power button must be pressed twice issue.
 1. Add D27 RB751V.
 2. Add R330 4.7K_0402_5%.
 3. Change R345 from 10K_0402_5% to 100K_0402_5%.
3. Per HPQ requirement to change audio component.
To change C174 and C201 to 0.022U_0603_25V7K.

REV: 0.2H (For SI gerber)

1. Per HPQ requirement to change audio component.
To change R427 from 20K_0402_5% to 39.2K_0402_1%.

REV: 0.3 (For SI SMT)

1. Per HPQ requirement to change LED color from BLUE to GREEN.
 - a. Change D5,D6,D7,D26 from HSMB-C172_BLUE_0805 to HSMG-C170_GRN_0805.
 - b. Change R9,R10,R11,R421 from 140_0402_1% to 330_0402_5%.
2. To improve RTC crystal accuracy.
Change C190,C203 from 12P_0402_50V8J to 15P_0402_50V8J.

REV: 0.3A (For PV Build)

1. Per HPQ requirement to add FET to shut off power to the Bluethumb module.
 - a. Add Q53 SI2301DS.
 - b. Add C568 1U_0603_10V6K.
 - c. Add C570 0.01U_0402_16V7K.
 - d. Add C571 0.1U_0402_16V7K.
 - e. Add C569 4.7U_0805_6.3V6K.
 - f. Add Q54 2N7002.
 - g. Add R442 100K_0402_5%.
 - h. Del R424.
 - i. Change Q16.2 signal source from Wireless_OFF# to Wireless_OFF.
2. For supporting WLAN and BT devices exist in the same system.
 - a. Connect Mini-PCI JP28-36 to Bluethumb JP32-7 using a series resistor of 1K_0402_5% (R72).
 - b. Connect Mini-PCI JP28-43 to Bluethumb JP32-6 using a series resistor of 1K_0402_5% (R298).

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Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	ME add a limit area, layout place not enough	38	delete PR6 change PR12 from 0_0603_5% to 0_0402_5% change PR15 from 10K_0603_1% to 10K_0402_1%	2003.06.18	
2	Customer request change adapter. The Vin voltage changed to 18V(minimum). So, we need to change Vin detector and Pre-charge detector	34	change PR170 from 100K_0603_1% to 73.2K_0603_1% change PR172 from 39K_0603_1% to 40.2K_0603_1% change PR187 from 732K_0603_1% to 768K_0603_1% change PR189 from 402K_0603_1% to 453K_0603_1%	2003.06.23	
3	For common parts design		change PR166 from 1M_0603_1% to 1M_0402_1% change PR184 from 2M_0603_5% to 2N_0402_5% change capacitor from 4.7U_1210_25V to 4.7U_1206_25V of all location (PC62,PC63,PC74,PC76,PC77,PC38,PC39, PC45,PC46,PC172,PC173,PC178,PC179,PC3,PC4,PC9, PC10,PC86,PC87,PC88,PC101,PC102,PC103,PC48,PC33, PC218) change PC164 and PC149 from SE035475Z07 to SE142475K00	2003.07.16	
4	delete unnecessary 0ohm resister		delete PR247,PR19,PR109,PR113,PR115,PR116,PR117,PR118, PR107,PR125,PR127,PR132,PR135,PR137,PR254,PR79, PR260,PR292,PR119	2003.07.16	
5	adjust Vin detector	34	change PR170 from 73.2K_0603_1% to 22K_0603_1% change PR172 from 40.2K_0603_1% to 36K_0603_1% change PR167 from 84.5K_0603_1% to 82.5K_0603_1%	2003.07.21	
6	adjust PACIN voltage from 3.3V to 3.2V	34	change PR168 from 8.2K_0805_5% to 10K_0805_1%	2003.9.01	
7	EMI test failure	40	change PR105 and PR140 from 0_0603_5% to 2.2_0603_5%	2003.9.01	

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