

Compal Confidential

QLA01 LA7811P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

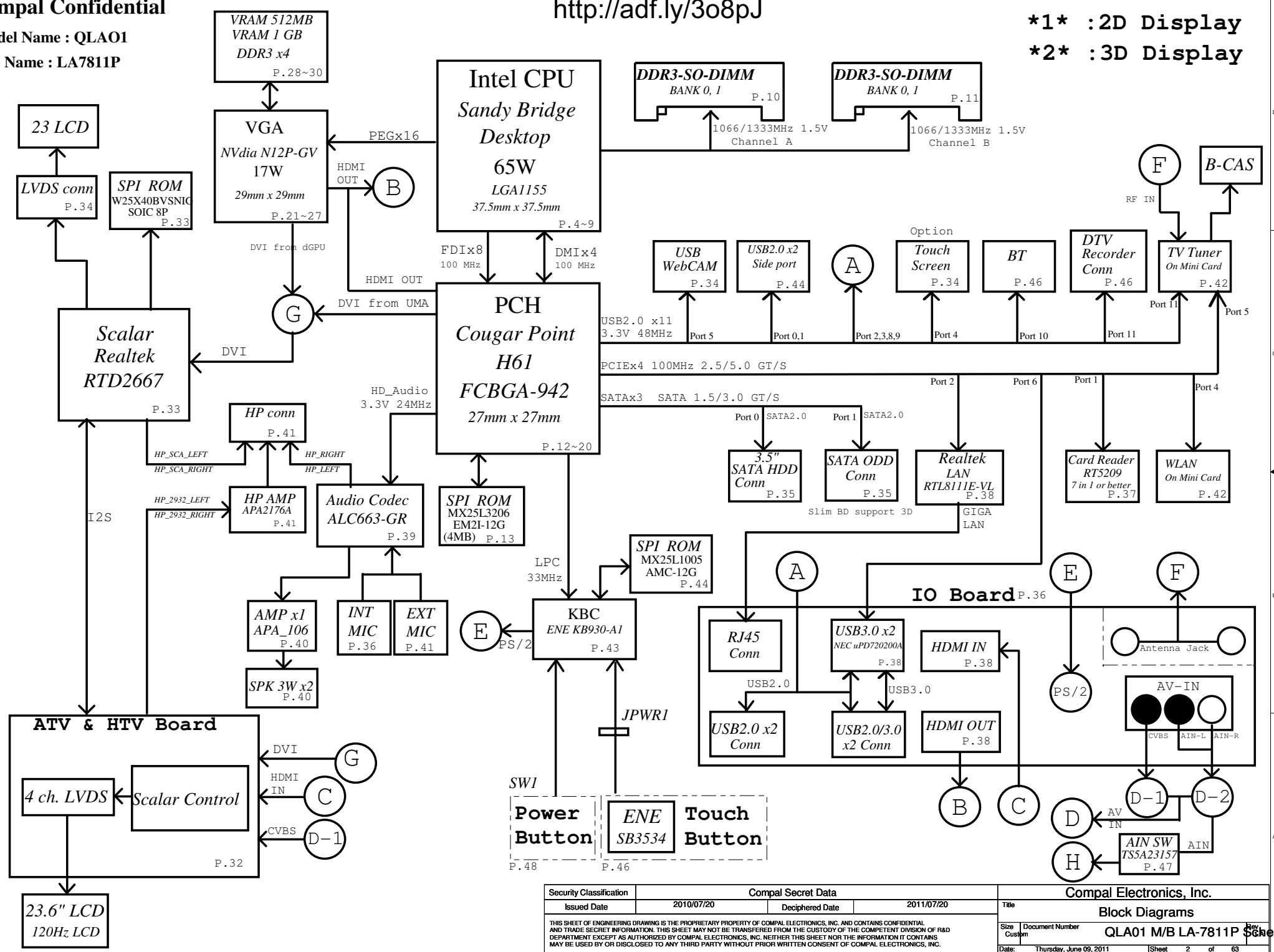
2011-06-02

REV: 0.1

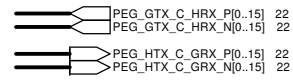
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	Cover Page
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				Custom	QLA01 M/B LA-7811P Schematic 1.A
				Date	Thursday, June 09, 2011
				Sheet	1 of 63

***1* : 2D Display**
***2* : 3D Display**

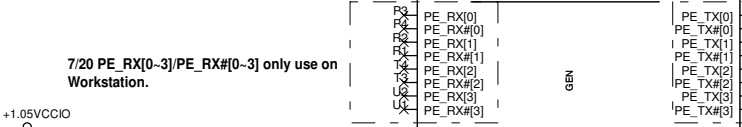
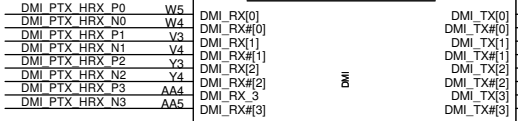
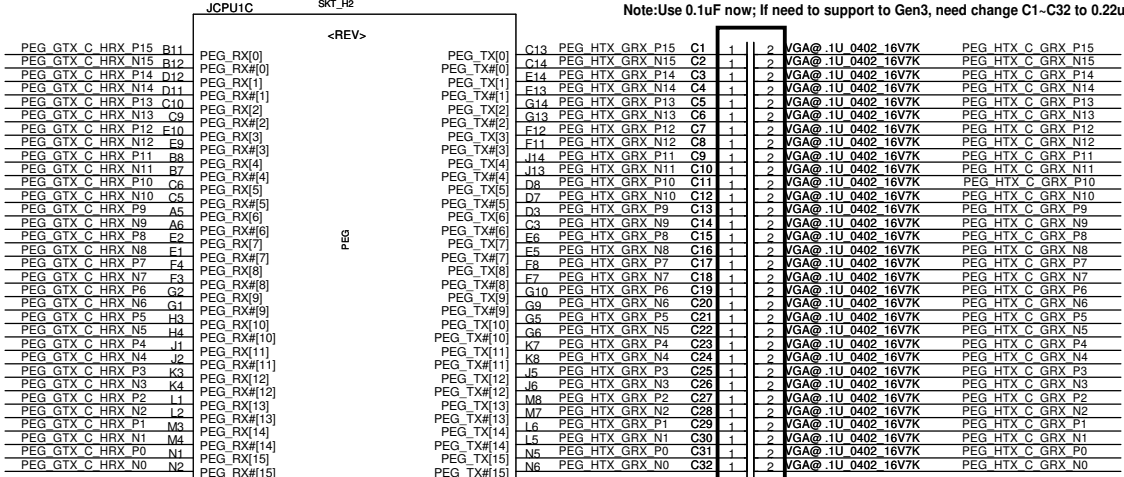
Model Name : QLA01
File Name : LA7811P



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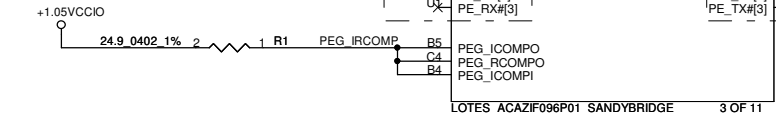


Note: Use 0.1uF now; if need to support to Gen3, need change C1-C32 to 0.22uF.

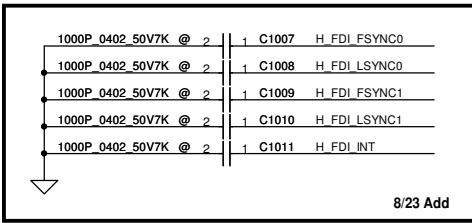
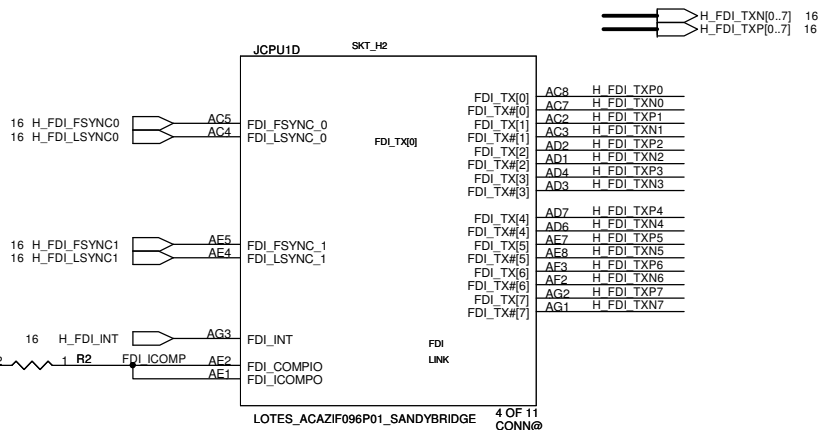


7/20 PE_RX[0-3]/PE_RX#0-3 only use on Workstation.

7/20 PE_TX[0-3]/PE_TX#0-3 only use on Workstation.

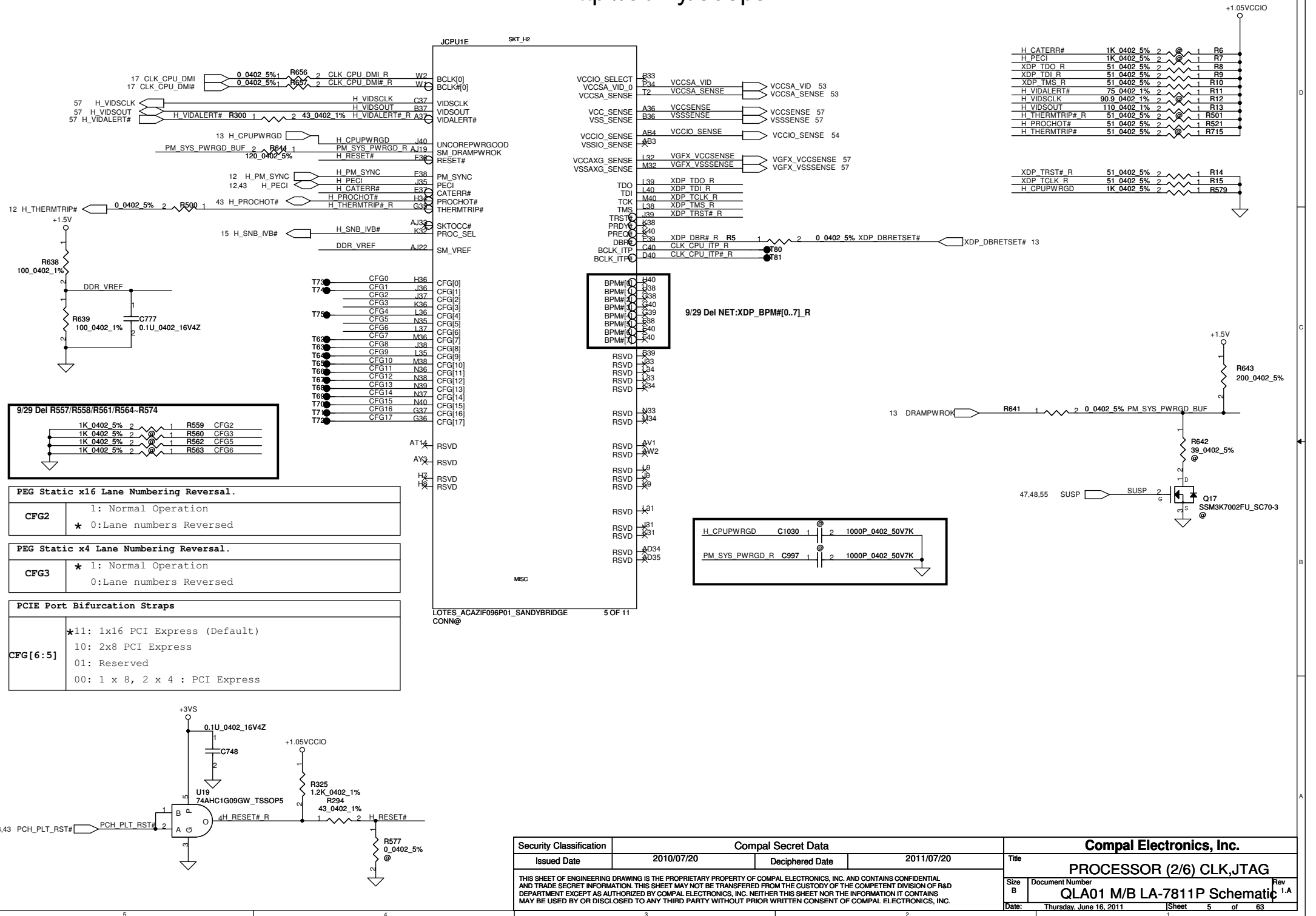


PEG_IROMPO and RCOMP signals should be shorted and routed with - max length = 500 mils - ;Width/Space= (4 mils/15mils) PEG_IROMPO signals should be routed with - max length = 500 mils - Width/Space (12 mils/15mils)



8/23 Add

Table with 4 columns: Security Classification (Compal Secret Data), Issued Date (2010/07/20), Deciphered Date (2011/07/20), Title (PROCESSOR (1/6) DMI,FDI,PEG), and other metadata like Date (Thursday, June 16, 2011) and Sheet (4 of 63).



9/29 Del R557/R558/R561/R564-R574

1K 0402 5% 2	R559	CFG2
1K 0402 5% 2	R560	CFG3
1K 0402 5% 2	R562	CFG5
1K 0402 5% 2	R563	CFG6

PEG Static x16 Lane Numbering Reversal.

CFG2	1: Normal Operation
	* 0: Lane numbers Reversed

PEG Static x4 Lane Numbering Reversal.

CFG3	* 1: Normal Operation
	0: Lane numbers Reversed

PCIe Port Bifurcation Straps

CFG[6:5]	*11: 1x16 PCI Express (Default)
	10: 2x8 PCI Express
	01: Reserved
	00: 1 x 8, 2 x 4 : PCI Express

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Title		PROCESSOR (2/6) CLK,JTAG
Size B	Document Number	QLA01 M/B LA-7811P Schematic
Date:	Thursday, June 16, 2011	Sheet 5 of 63

10 DDR_A_D[0..63]
10 DDR_A_DQS[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_MA[0..15]

11 DDR_B_DQS[0..7]
11 DDR_B_DQS[0..7]
11 DDR_B_MA[0..15]

JCPU1A SKT_H2
DDR_A_MA0 AV27 SA_MA[0]
DDR_A_MA1 AV24 SA_MA[1]
DDR_A_MA2 AW24 SA_MA[2]
DDR_A_MA3 AW23 SA_MA[3]
DDR_A_MA4 AV23 SA_MA[4]
DDR_A_MA5 AT24 SA_MA[5]
DDR_A_MA6 AT23 SA_MA[6]
DDR_A_MA7 AU22 SA_MA[7]
DDR_A_MA8 AV22 SA_MA[8]
DDR_A_MA9 AT22 SA_MA[9]
DDR_A_MA10 AV28 SA_MA[10]
DDR_A_MA11 AU21 SA_MA[11]
DDR_A_MA12 AT21 SA_MA[12]
DDR_A_MA13 AW32 SA_MA[13]
DDR_A_MA14 AU20 SA_MA[14]
DDR_A_MA15 AT20 SA_MA[15]

AJ3 DDR_A_D0
AJ4 DDR_A_D1
AJ5 DDR_A_D2
AJ6 DDR_A_D3
AJ7 DDR_A_D4
AJ8 DDR_A_D5
AJ9 DDR_A_D6
AJ10 DDR_A_D7
AJ11 DDR_A_D8
AJ12 DDR_A_D9
AJ13 DDR_A_D10
AJ14 DDR_A_D11
AJ15 DDR_A_D12
AJ16 DDR_A_D13
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AJ61 DDR_A_D58
AJ62 DDR_A_D59
AJ63 DDR_A_D60
AJ64 DDR_A_D61
AJ65 DDR_A_D62
AJ66 DDR_A_D63

JCPU1B SKT_H2
DDR_B_MA0 AK24 SB_MA[0]
DDR_B_MA1 AM20 SB_MA[1]
DDR_B_MA2 AM19 SB_MA[2]
DDR_B_MA3 AK18 SB_MA[3]
DDR_B_MA4 AP19 SB_MA[4]
DDR_B_MA5 AP18 SB_MA[5]
DDR_B_MA6 AM18 SB_MA[6]
DDR_B_MA7 AL18 SB_MA[7]
DDR_B_MA8 AN18 SB_MA[8]
DDR_B_MA9 AY17 SB_MA[9]
DDR_B_MA10 AN23 SB_MA[10]
DDR_B_MA11 AU17 SB_MA[11]
DDR_B_MA12 AT18 SB_MA[12]
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DDR_B_MA15 AV16 SB_MA[15]

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AG6 DDR B_D5
AJ6 DDR B_D6
AJ7 DDR B_D7
AJ7 DDR B_D8
AM7 DDR B_D9
AM7 DDR B_D10
AL10 DDR B_D11
AL6 DDR B_D12
AM6 DDR B_D13
AL9 DDR B_D14
AM9 DDR B_D15
AP7 DDR B_D16
AP7 DDR B_D17
AP10 DDR B_D18
AP10 DDR B_D19
AP6 DDR B_D20
AG6 DDR B_D21
AP9 DDR B_D22
AR9 DDR B_D23
AM12 DDR B_D25
AM13 DDR B_D25
AR13 DDR B_D26
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AR31 DDR B_D45
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AM35 DDR B_D54
AL34 DDR B_D55
AH35 DDR B_D56
AH34 DDR B_D57
AE34 DDR B_D58
AE35 DDR B_D59
AJ35 DDR B_D60
AJ34 DDR B_D61
AE33 DDR B_D62
AF35 DDR B_D63

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AG9 DDR B_D2
AJ8 DDR B_D3
AG6 DDR B_D5
AJ6 DDR B_D6
AJ7 DDR B_D7
AJ7 DDR B_D8
AM7 DDR B_D9
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AJ35 DDR B_D60
AJ34 DDR B_D61
AE33 DDR B_D62
AF35 DDR B_D63
AH7 DDR B_DQS0
AM8 DDR B_DQS1
AR8 DDR B_DQS2
AN13 DDR B_DQS3
AN29 DDR B_DQS4
AP33 DDR B_DQS5
AL33 DDR B_DQS6
AG35 DDR B_DQS7
AH6 DDR B_DQS#0
AL8 DDR B_DQS#1
AP6 DDR B_DQS#2
AN12 DDR B_DQS#3
AN28 DDR B_DQS#4
AR33 DDR B_DQS#5
AM33 DDR B_DQS#6
AG34 DDR B_DQS#7

DDR_A_WE# AV29 SA_WE#
DDR_A_CAS# AV30 SA_CAS#
DDR_A_RAS# AU20 SA_RAS#

AK3 DDR_A_DQS0
AP3 DDR_A_DQS1
AW4 DDR_A_DQS2
AV8 DDR_A_DQS3
AV37 DDR_A_DQS4
AP28 DDR_A_DQS5
AK38 DDR_A_DQS6
AF38 DDR_A_DQS7
AK2 DDR_A_DQS#0
AP2 DDR_A_DQS#1
AV4 DDR_A_DQS#2
AW8 DDR_A_DQS#3
AV36 DDR_A_DQS#4
AP39 DDR_A_DQS#5
AK39 DDR_A_DQS#6
AF39 DDR_A_DQS#7

DDR_B_WE# AR26 SB_WE#
DDR_B_CAS# AK20 SB_CAS#
DDR_B_RAS# AP20 SB_RAS#

DDR_B_BS0 AP23 SB_BS[0]
DDR_B_BS1 AM24 SB_BS[1]
DDR_B_BS2 AW17 SB_BS[2]

DDR_B_CS0# AN25 SB_CS#0
DDR_B_CS1# AT20 SB_CS#1
AL3 SB_CS#2
AT2 SB_CS#3

DDR_B_CKE0 AU16 SB_CKE[0]
DDR_B_CKE1 AU15 SB_CKE[1]
AW15 SB_CKE[2]
AV15 SB_CKE[3]

DDR_B_ODT0 AL26 SB_ODT[0]
DDR_B_ODT1 AL26 SB_ODT[1]
AP26 SB_ODT[2]
AK26 SB_ODT[3]

DDR_B_CLK0# AL22 SB_CLK#0
DDR_B_CLK1 AL20 SB_CLK#1
AK20 SB_CLK#1
AL3 SB_CLK#2
AM3 SB_CLK#2
AP3 SB_CLK#3
AN3 SB_CLK#3

AN16 SB_DQS[8]
AN10 SB_DQS#8
AL16 SB_ECC_CB[0]
AM16 SB_ECC_CB[1]
AP16 SB_ECC_CB[2]
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AM15 SB_ECC_CB[4]
AR15 SB_ECC_CB[6]
AP15 SB_ECC_CB[7]

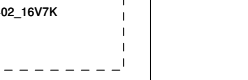
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DDR_A_BS2 AV20 SA_BS[2]

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DDR_A_CS1# AV30 SA_CS#1
AV30 SA_CS#2
AU30 SA_CS#3

DDR_A_CKE0 AV19 SA_CKE[0]
DDR_A_CKE1 AT19 SA_CKE[1]
AU18 SA_CKE[2]
AV18 SA_CKE[3]

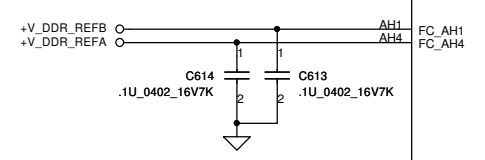
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AU30 SA_ODT[2]
AW33 SA_ODT[3]

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DDR_A_CLK1# AU20 SA_CLK#1
AU20 SA_CLK#1
AW20 SA_CLK#2
AV20 SA_CLK#2
AV20 SA_CLK#3
AW20 SA_CLK#3



AV13 SA_DQS[8]
AV13 SA_DQS#8
AU12 SA_ECC_CB[0]
AU12 SA_ECC_CB[1]
AW12 SA_ECC_CB[2]
AY12 SA_ECC_CB[3]
AU12 SA_ECC_CB[4]
AY12 SA_ECC_CB[5]
AY12 SA_ECC_CB[6]
AW12 SA_ECC_CB[7]

DDR_A
LOTES_ACAZIF096P01_SANDYBRIDGE
1 OF 11
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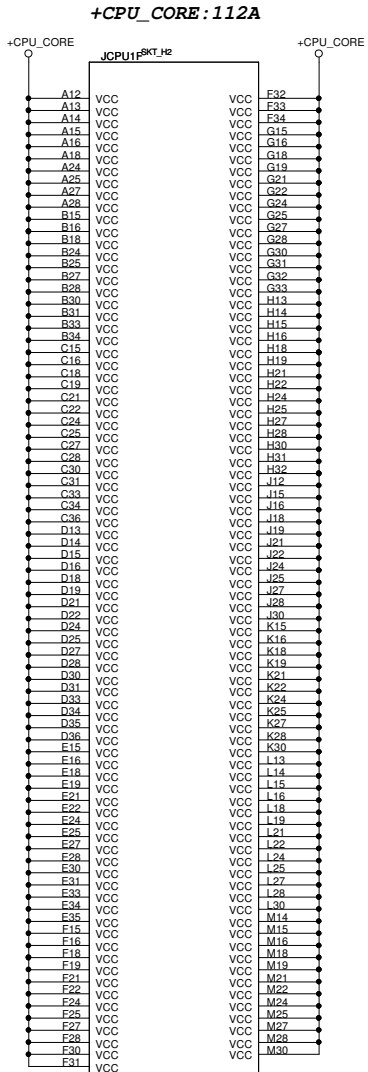


sb_CK[0]

FC_AH4
FC_AH4

DDR_B
2 OF 11

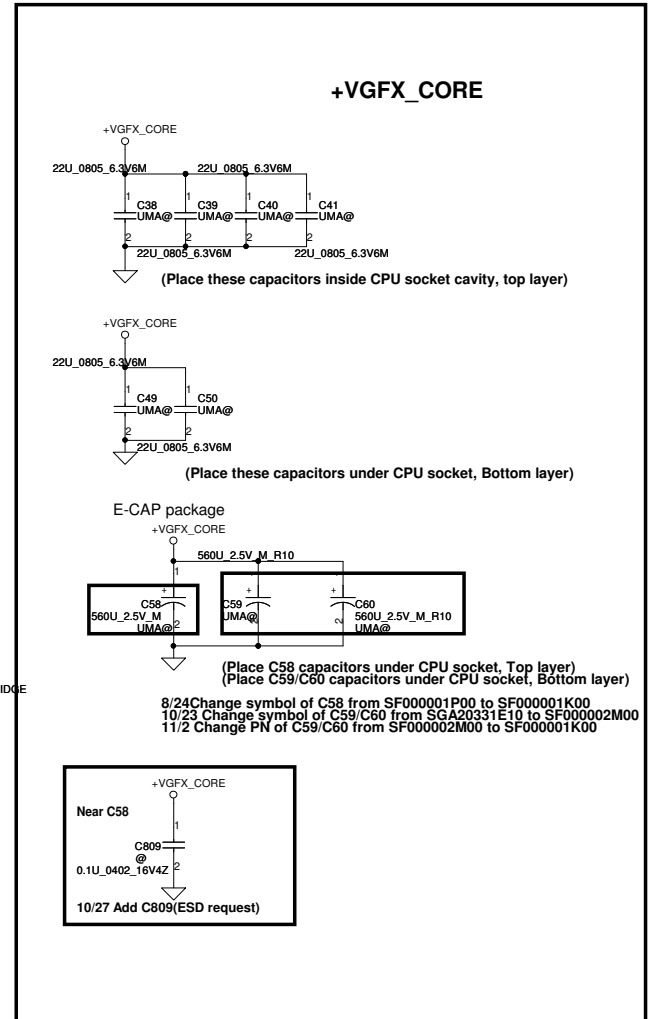
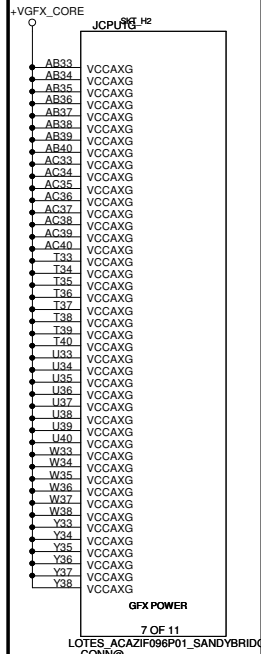
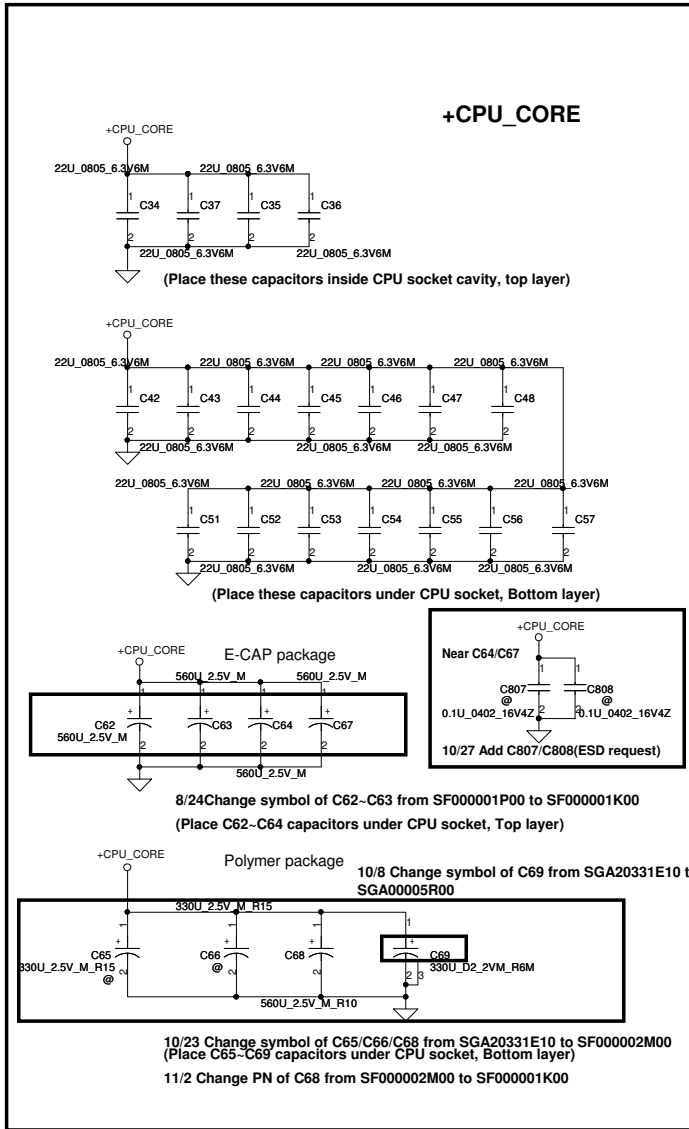
Table with 4 columns: Security Classification (Compal Secret Data), Issued Date (2010/07/20), Deciphered Date (2011/07/20), Title (PROCESSOR (3/6) DDRIII). Includes a footer with document number QLA01 M/B LA-7811P Schematic and date Thursday, June 16, 2011.



+CPU_CORE: 112A

+VGFX_CORE: 35A

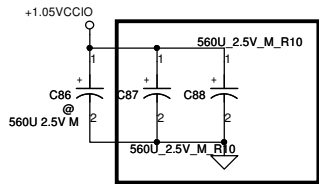
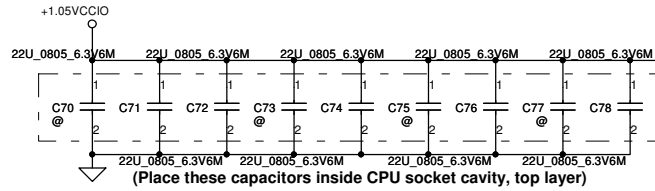
+VGFX_CORE



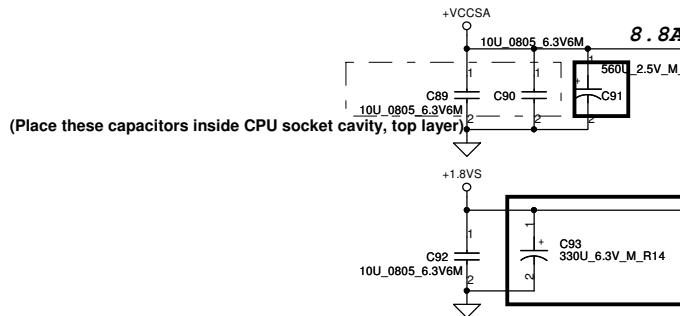
CPU POWER
6 OF 11
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@

GFX POWER
7 OF 11
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@

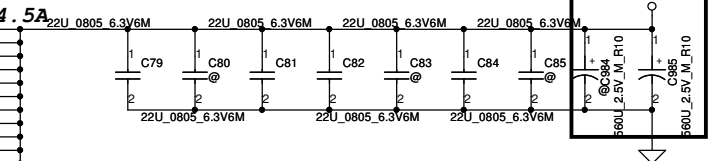
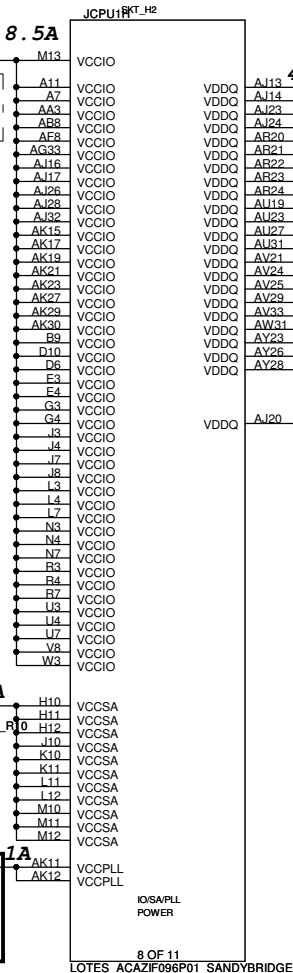
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
				PROCESSOR (4/6) PWR,Bypass	
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11/4 Change PN of C91 from SF000001P00 to SF000001K00

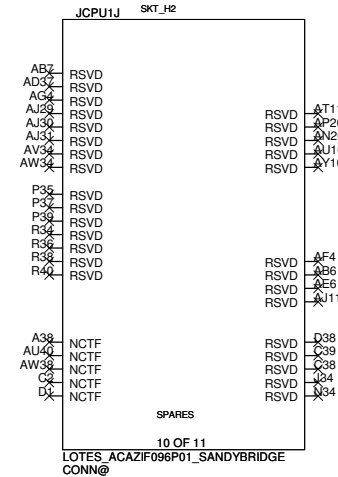
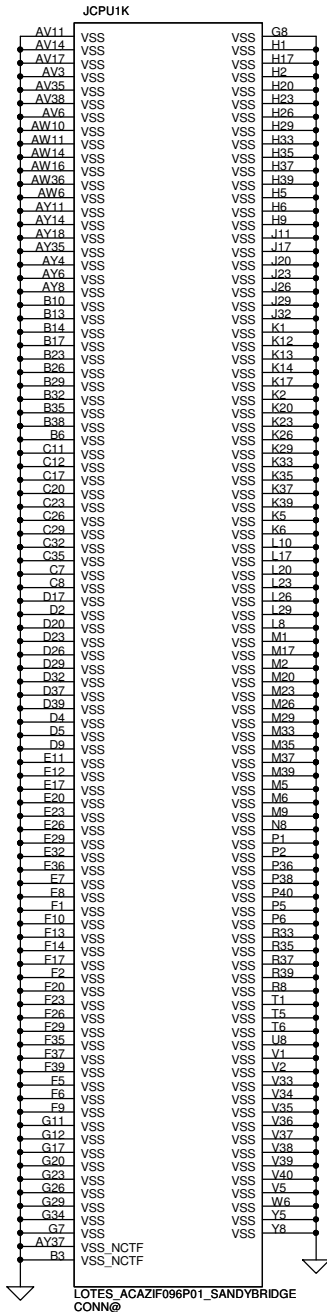
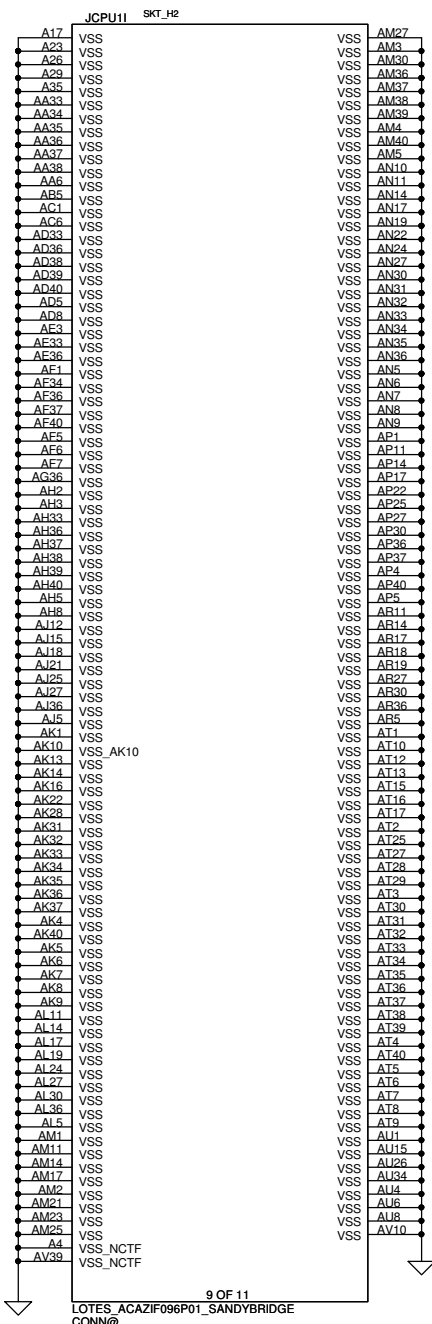


10/23 Change symbol of C93 from SGA00000Y80 to SF000002N00
11/4 Change PN of C93 from SF000002N00 to SF000001G00



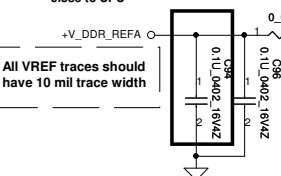
11/2 Change PN of C984/C985 from SF000002000 to SF000001K00

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Size	Custom	Document Number	QLA01 M/B LA-7811P Schematic		Rev
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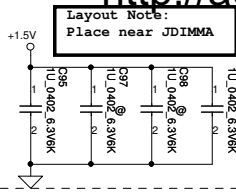
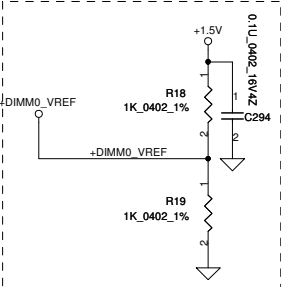


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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size	Document Number	Rev		1.A	
Custom	QLA01 M/B LA-7811P Schematic				
Date:	Thursday, June 09, 2011	Sheet	9	of	63

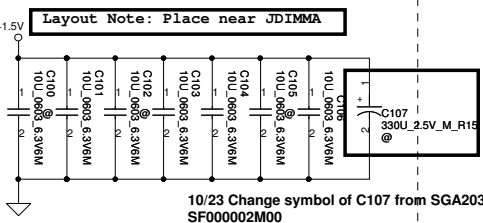
Layout Note: Place C94 on Bottom Layer at DIMM close to CPU



All VREF traces should have 10 mil trace width

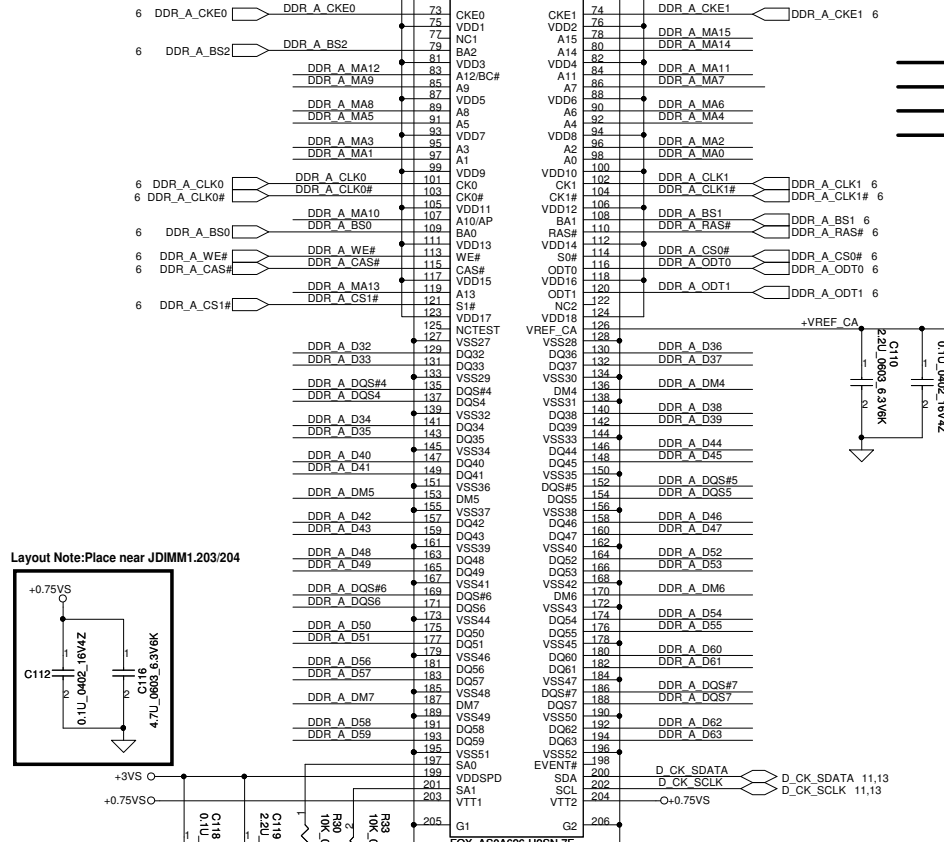


Layout Note: Place near JDIMMA

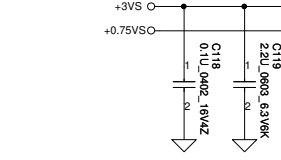
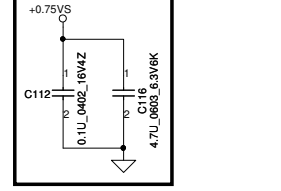


Layout Note: Place near JDIMMA

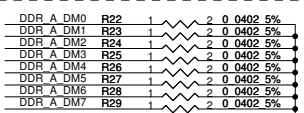
10/23 Change symbol of C107 from SGA20331E10 to SF000021M00



Layout Note: Place near JDIMM1.203/204



STANDARD: 5.2mm



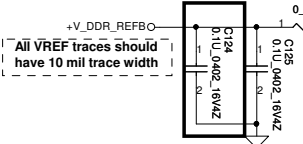
Security Classification	Compal Secret Data	
Issued Date	2010/07/20	Deciphered Date
		2011/07/20

Compal Electronics, Inc.
DDRIII CHANNELA

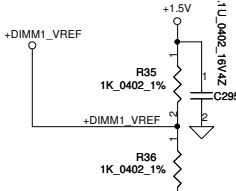
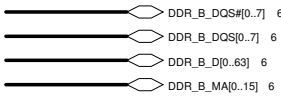
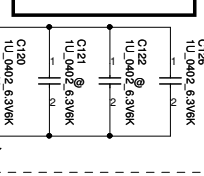
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Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1.A
Date:	Thursday, June 16, 2011	Sheet 10 of 63

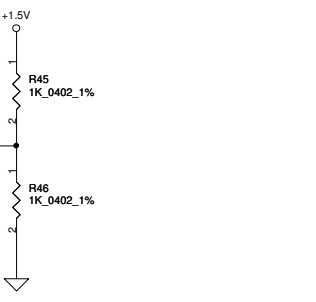
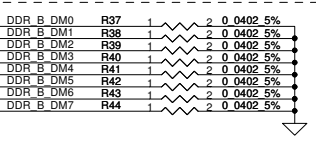
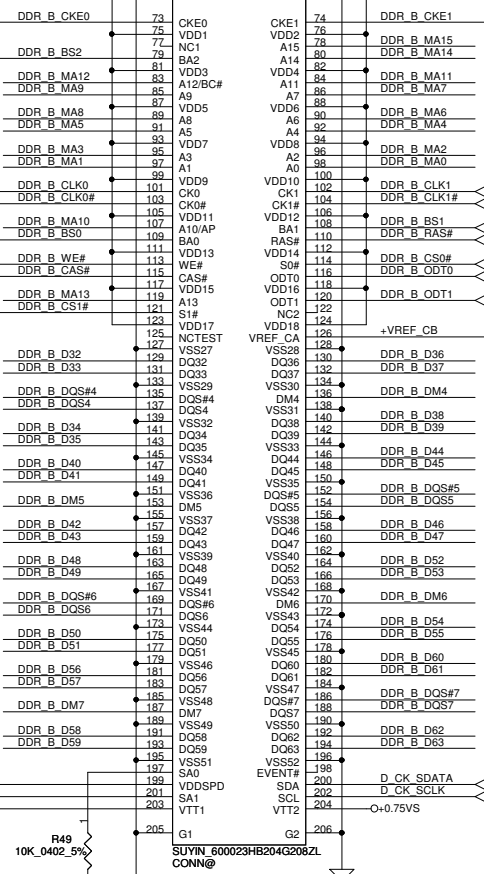
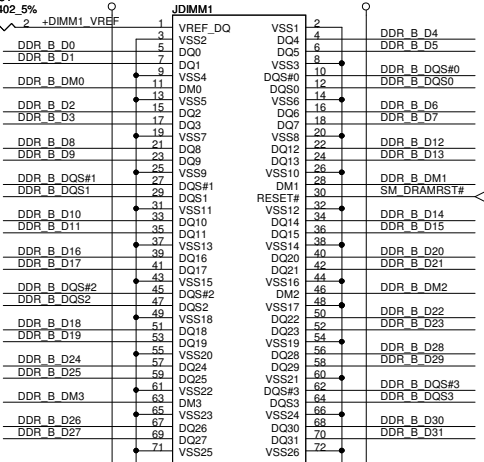
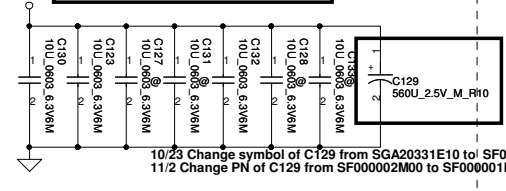
Layout Note: Place C124 on Bottom Layer at DIMM close to CPU



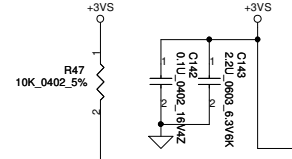
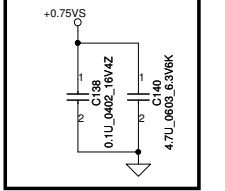
http://adf.ly/3o8pJ



Layout Note: Place near JDIMM



Layout Note: Place near JDIMM4.203/204

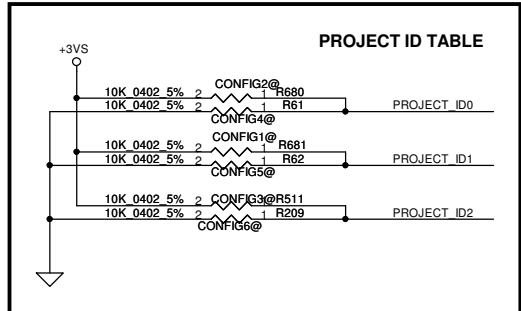
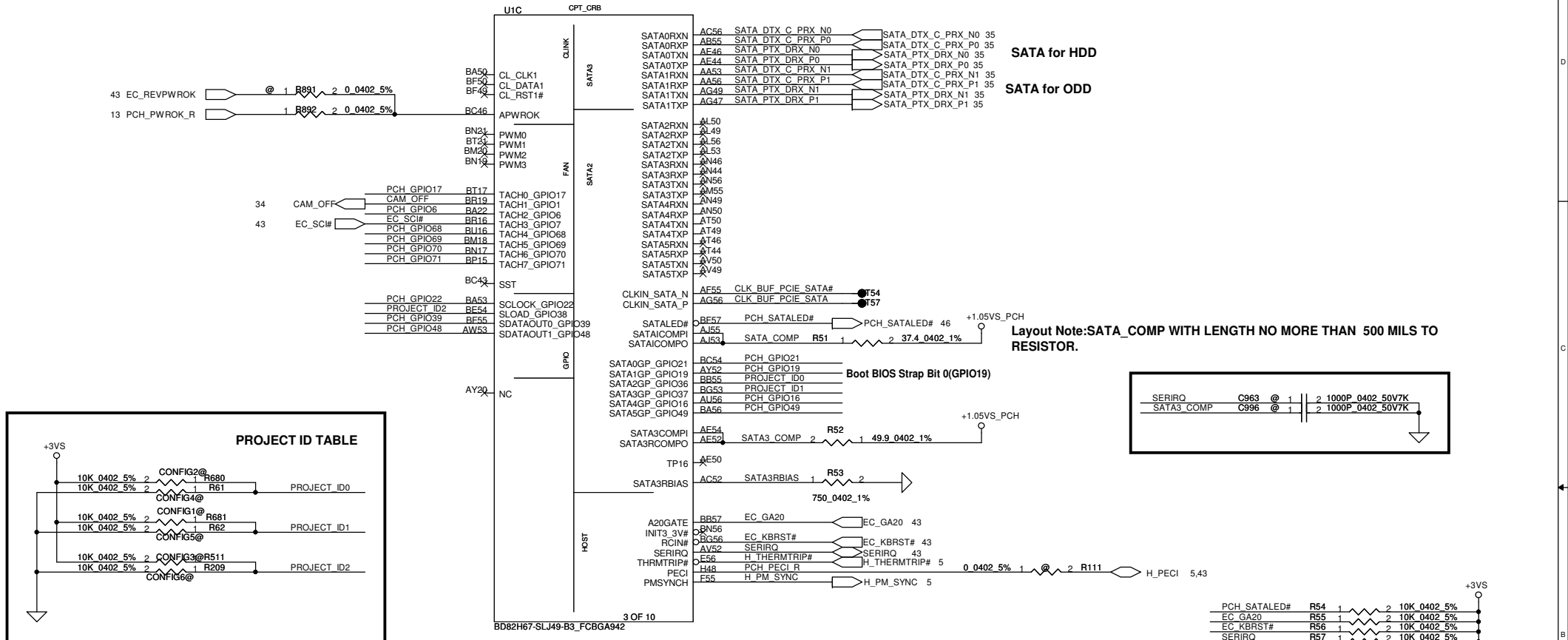


<Address: 01>

STANDARD: 9.2mm

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		2011/07/20
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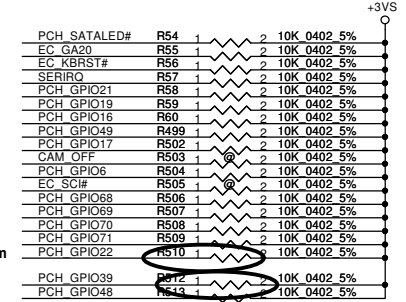
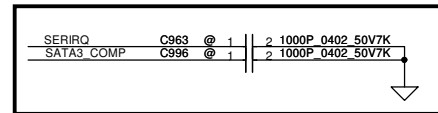
Title			Compal Electronics, Inc.	
			DDRIII CHANNELB	
Size	Document Number		Rev	
Custom	QA01 M/B LA-7811P Schematic		1.A	
Date:	Thursday, June 16, 2011	Sheet	11	of 63



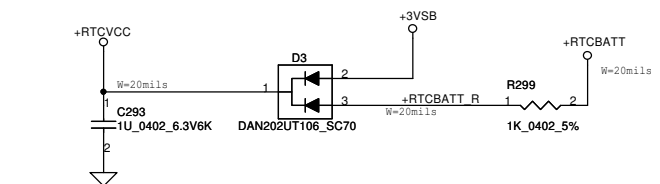
SATA for HDD

SATA for ODD

Layout Note: SATA_COMP WITH LENGTH NO MORE THAN 500 MILS TO RESISTOR.

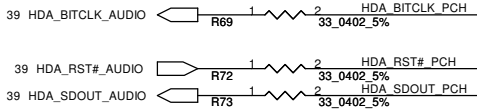


7/30 R510--- CRB:1K ohm;EDS:10K ohm
7/30 R512--- CRB:10K ohm PD to GND;EDS:10K ohm PU to +3VS



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				PCH (1/9) SATA,FAN	
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HDA for AUDIO



HDA SDO
ME debug mode, this signal has a weak internal pull down
Low = Disable (default)
High = Enable (flash descriptor security override)

HDA SYNC
This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform

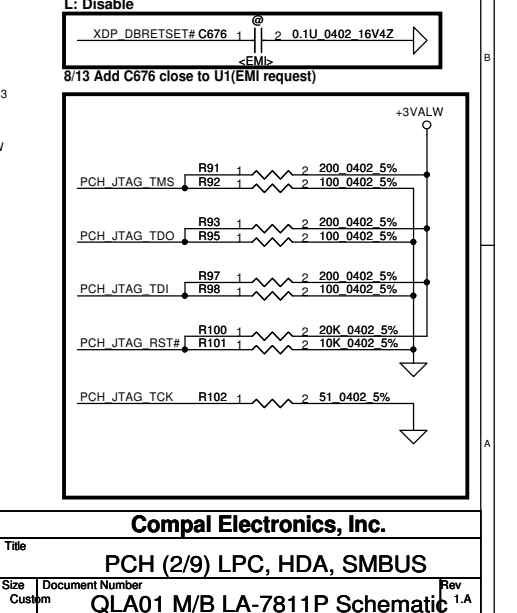
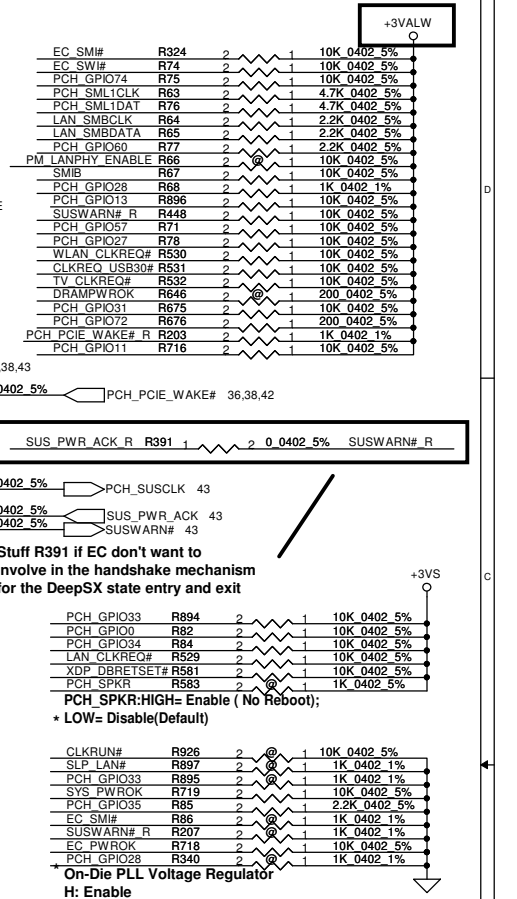
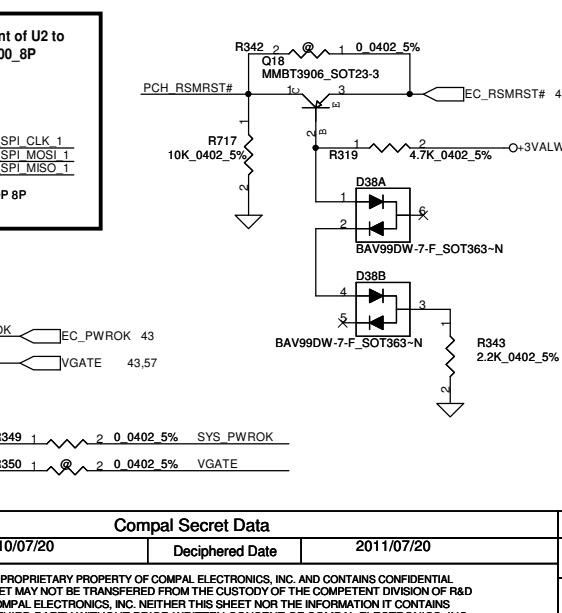
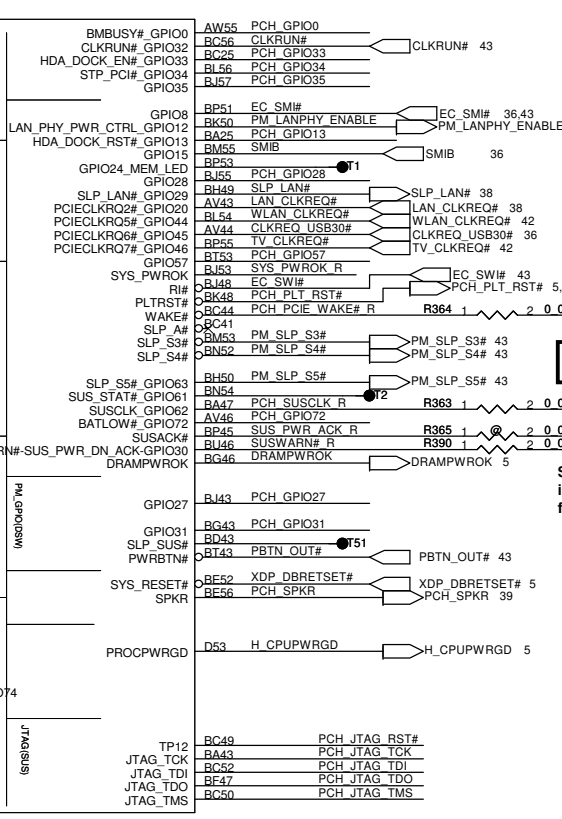
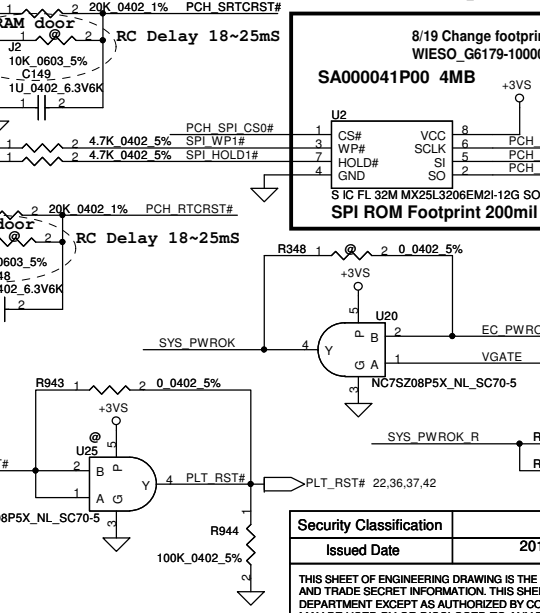
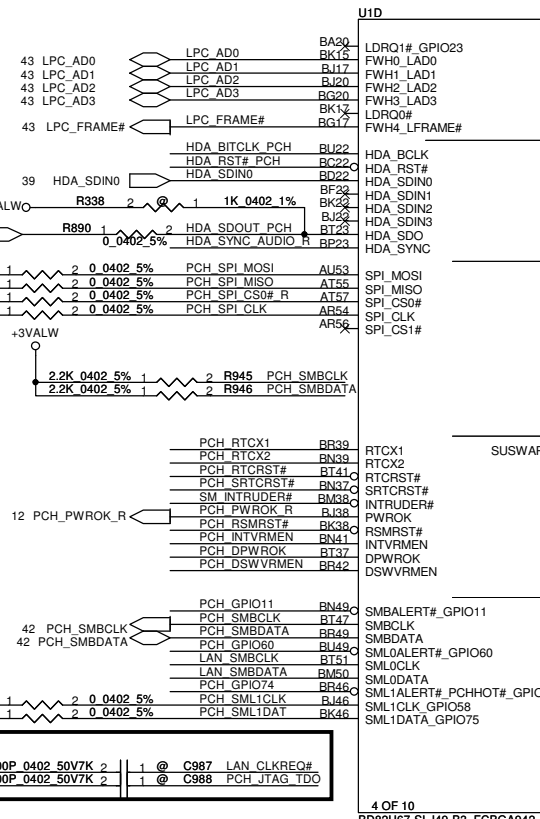
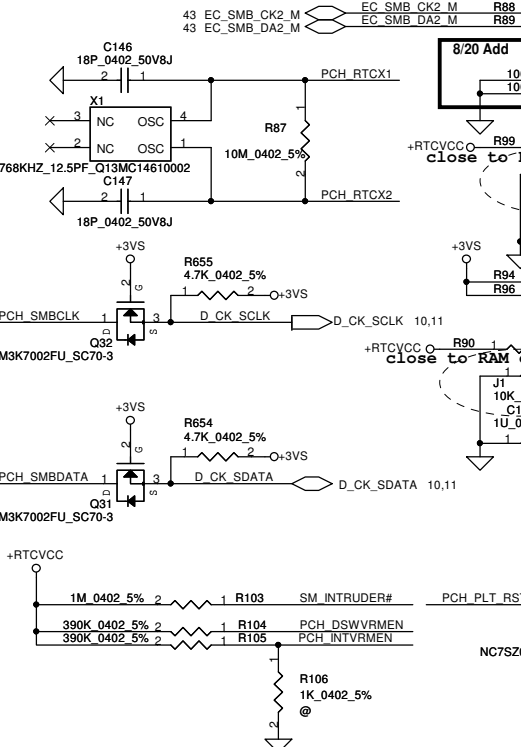
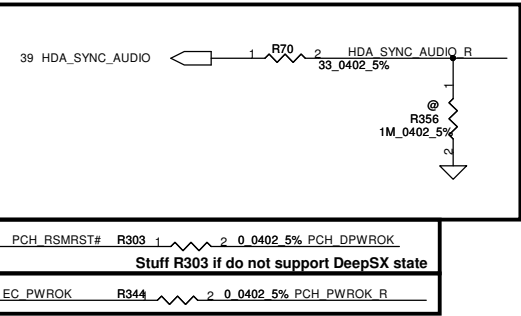
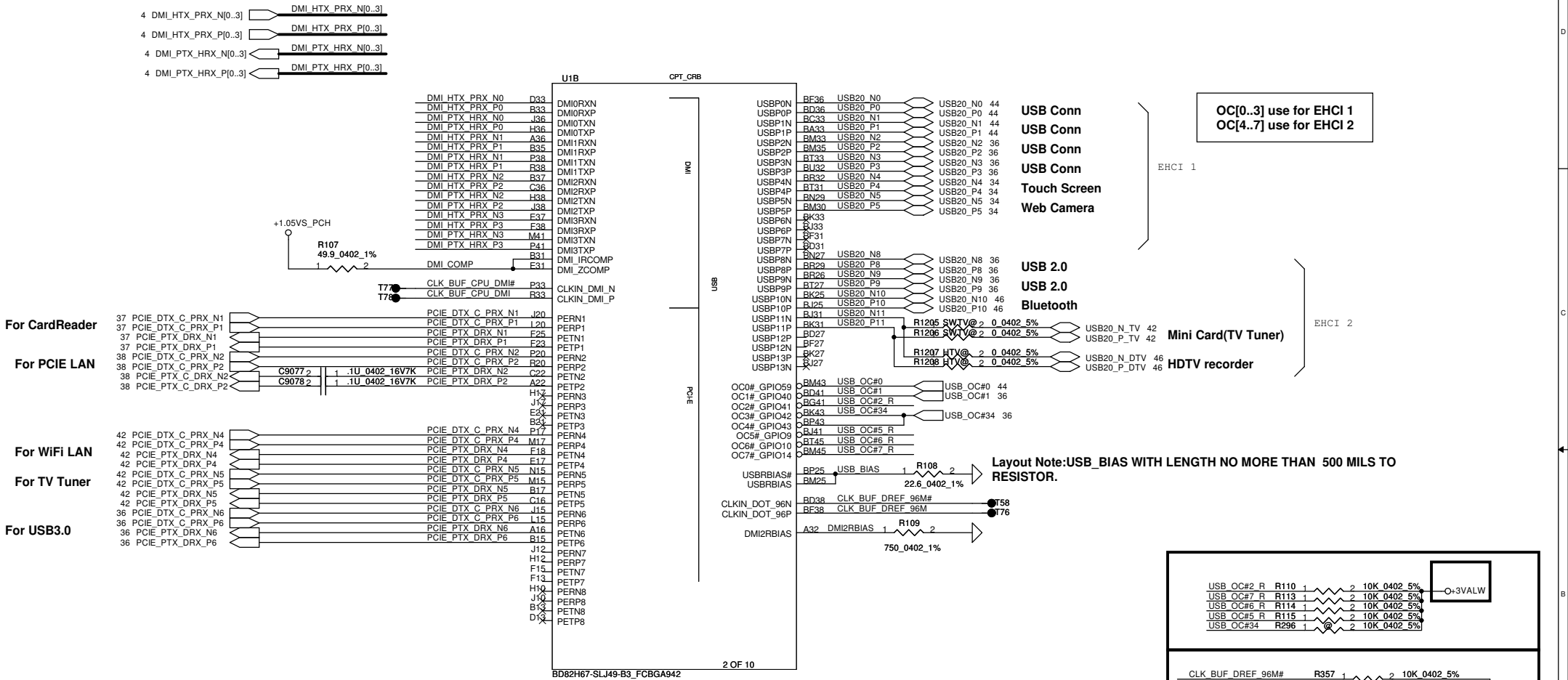


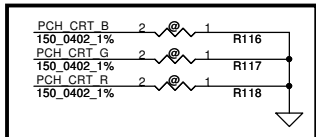
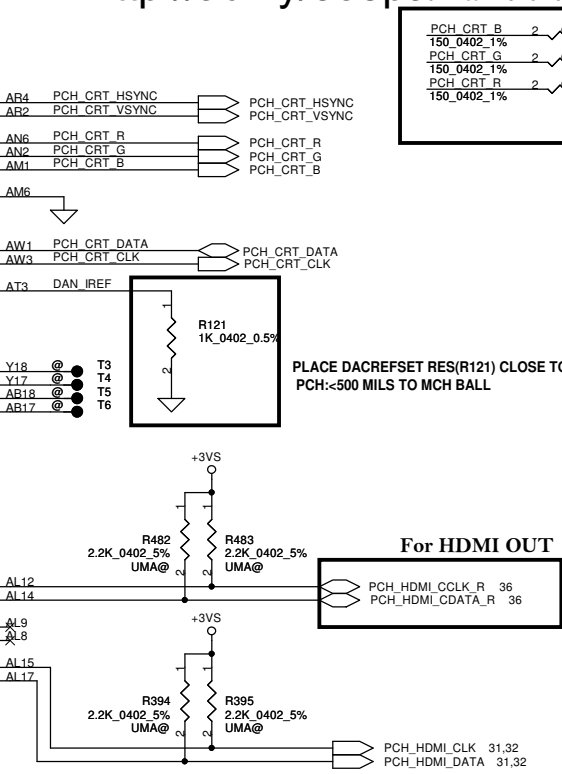
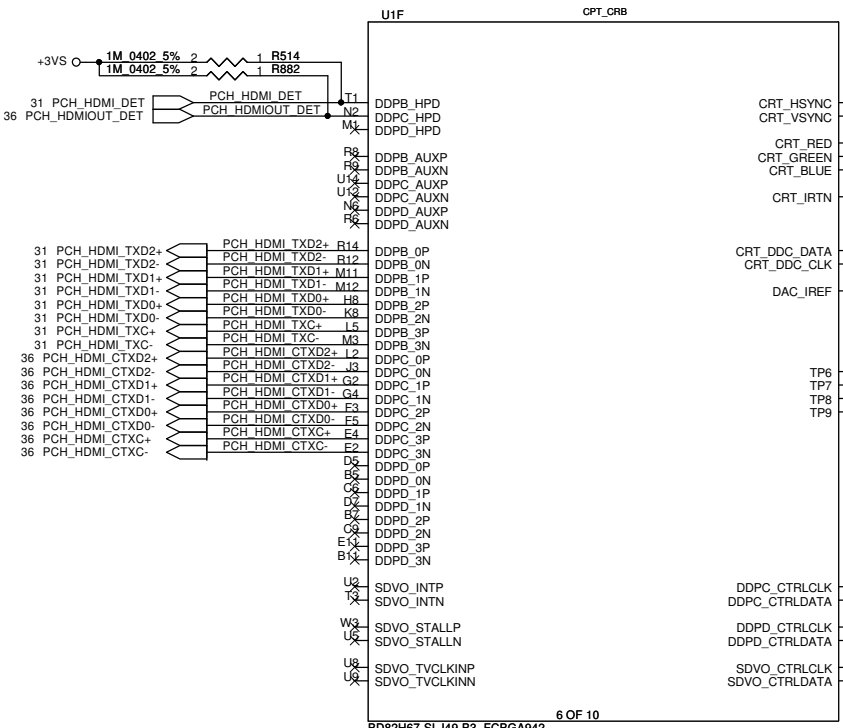
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Compal Electronics, Inc. PCH (2/9) LPC, HDA, SMBUS. QLA01 M/B LA-7811P Schematic. Rev 1.A. Date: Thursday, June 16, 2011. Sheet 13 of 63.



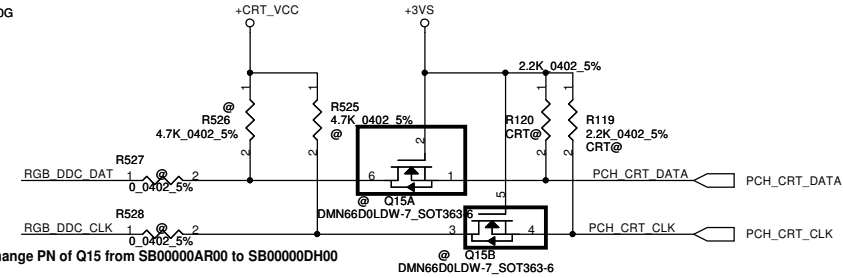
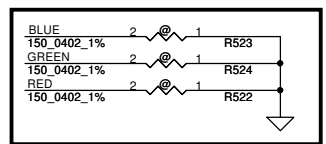
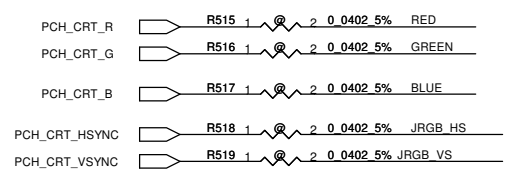
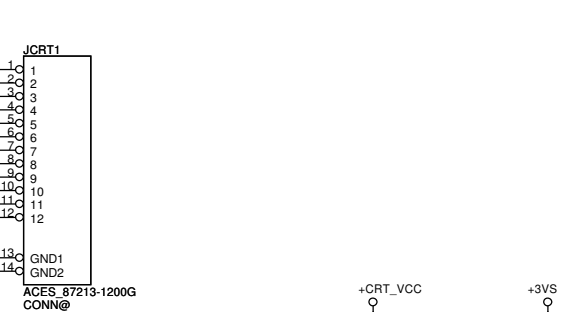
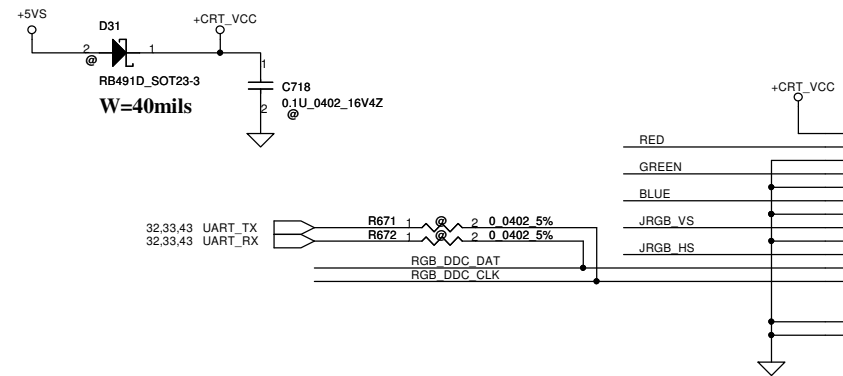
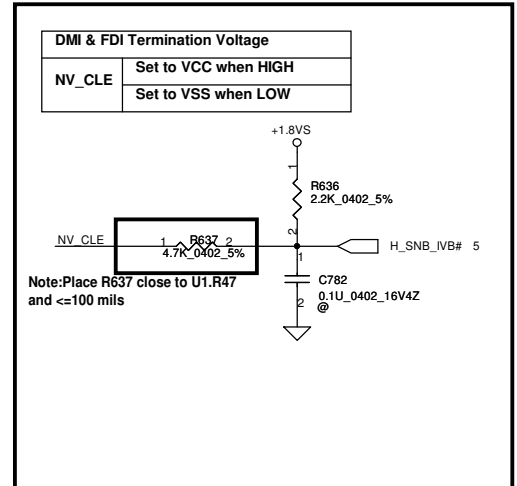
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
				PCH (3/9) DMI, USB, PCIE	
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Date:	Thursday, June 16, 2011	Sheet	14	of	63

http://adf.ly/3o8p3 PLACE RGB RESISTORS CLOSE TO MCH BALL

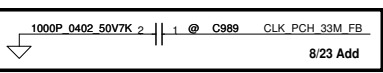
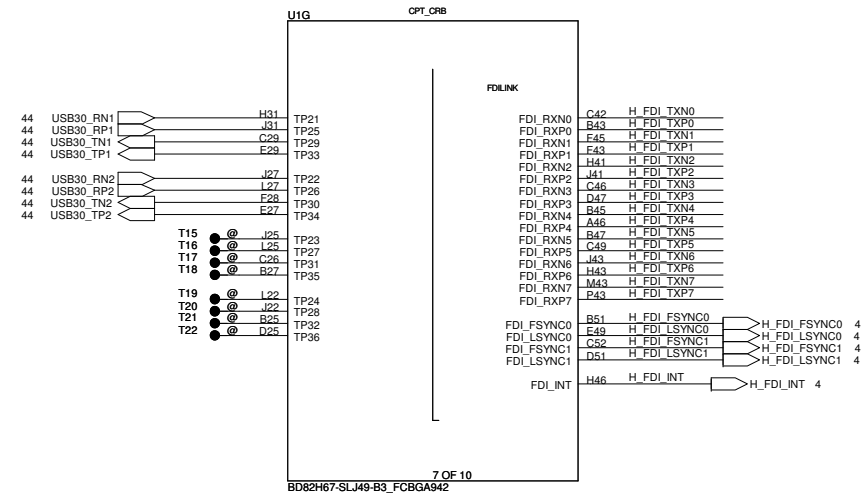
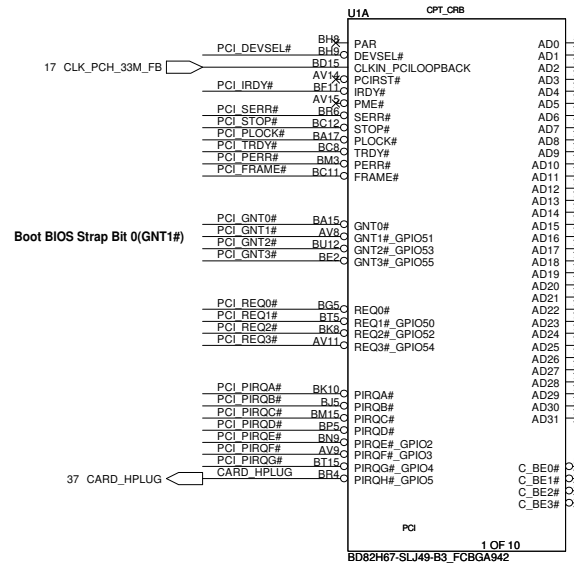
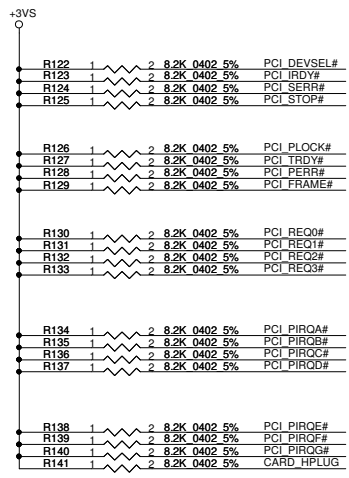


NV_CLE	U1E	CPT_CRB
M48	RESERVED_29	RESERVED_22
R47	DF_TV5	RESERVED_21
Y4L	RESERVED_6	RESERVED_14
M50	RESERVED_4	RESERVED_13
M49	RESERVED_3	RESERVED_12
U43	RESERVED_2	RESERVED_11
J52	RESERVED_1	RESERVED_10
		RESERVED_9
		RESERVED_8
		RESERVED_7
		RESERVED_20
		RESERVED_19
		RESERVED_18
		RESERVED_17
		RESERVED_16
		RESERVED_15
		RESERVED_28
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		RESERVED_5
		RESERVED_5

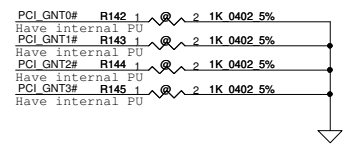
NVRAM 5 OF 10
BD82H67-SLJ49-B3_FCBGA942

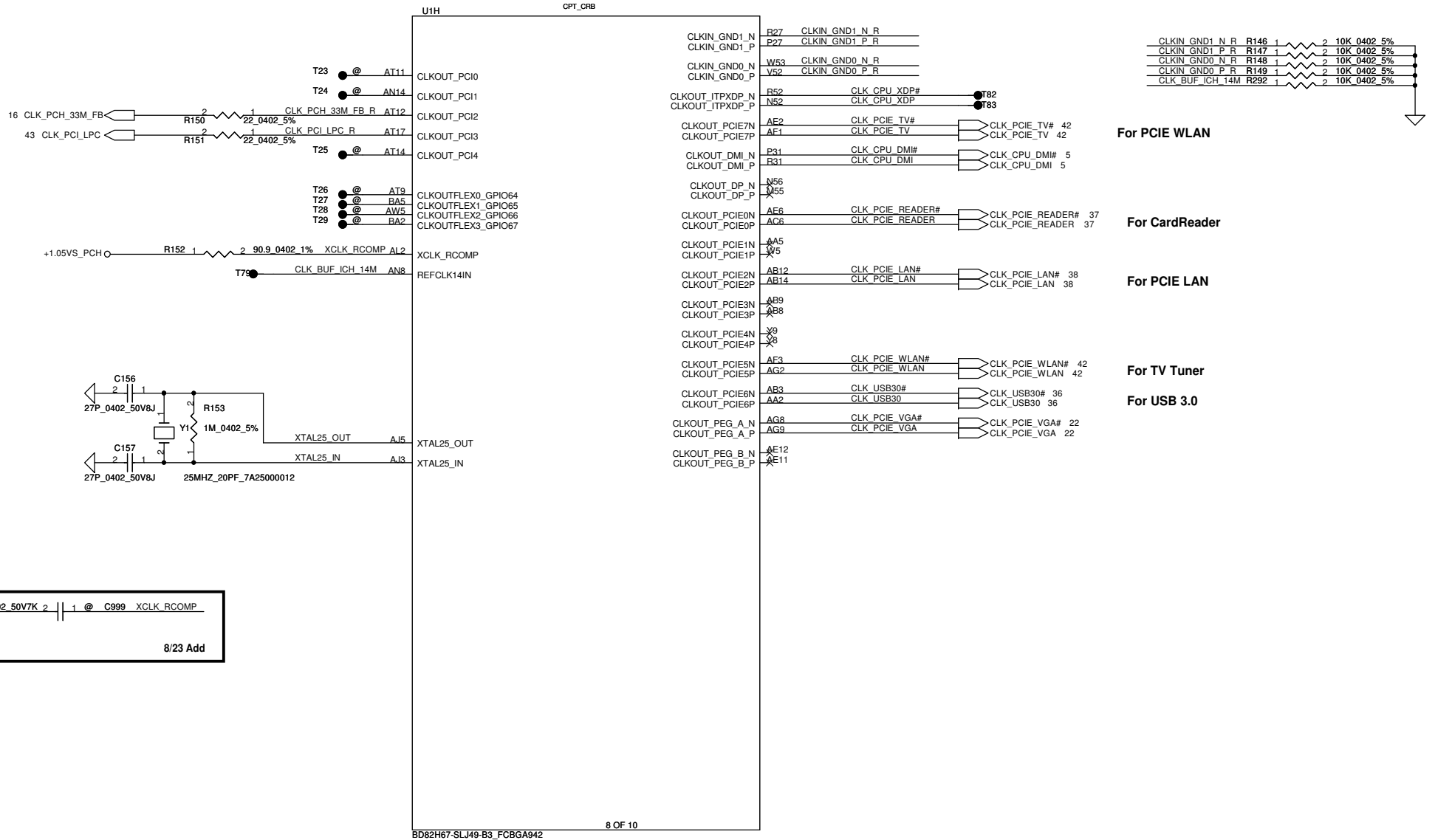


Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	PCH (4/9) CRT, DPI, VRAM	
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Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

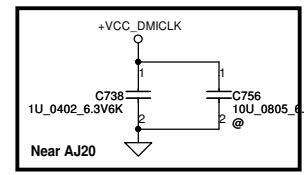
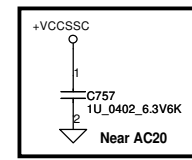
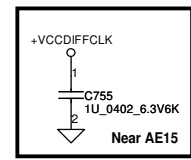
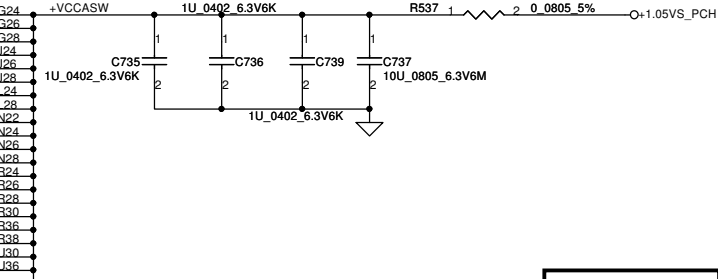
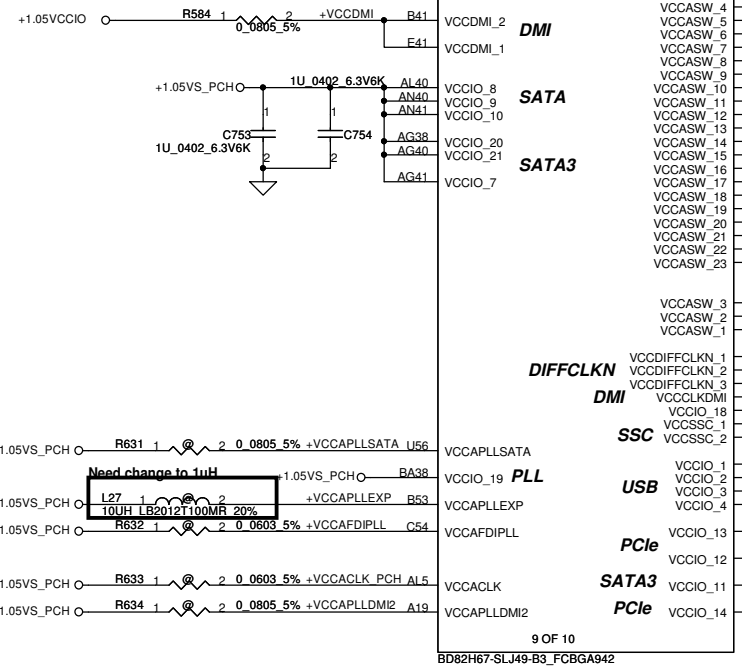
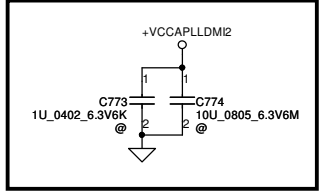
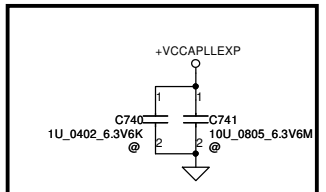
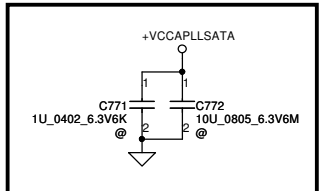
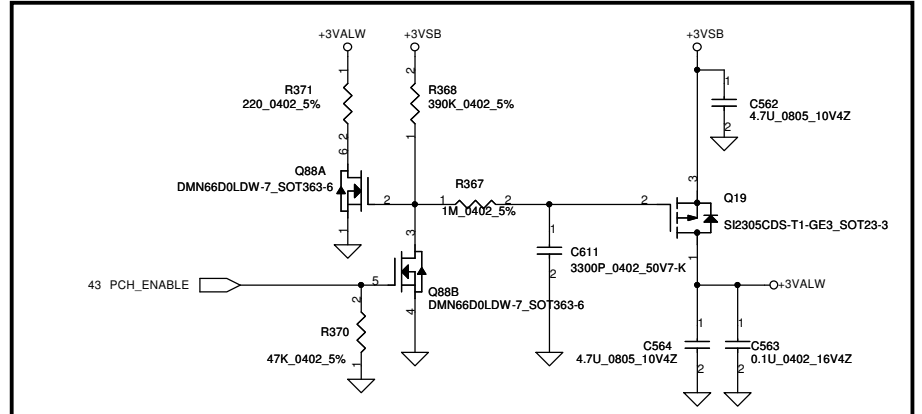
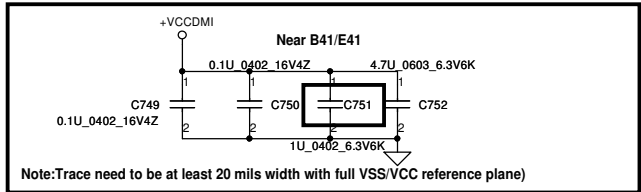
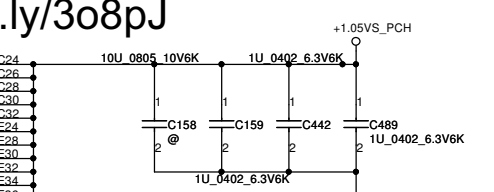
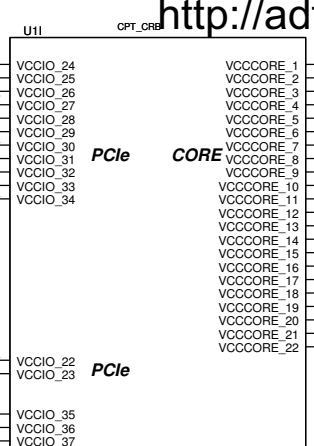
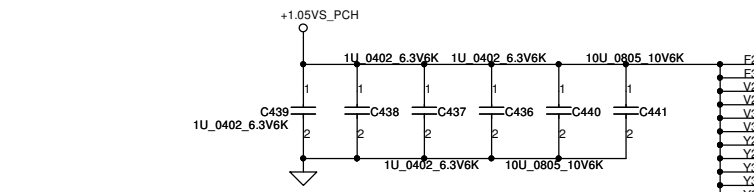




1000P_0402_50V7K 2 || 1 @ C999 XCLK RCOMP

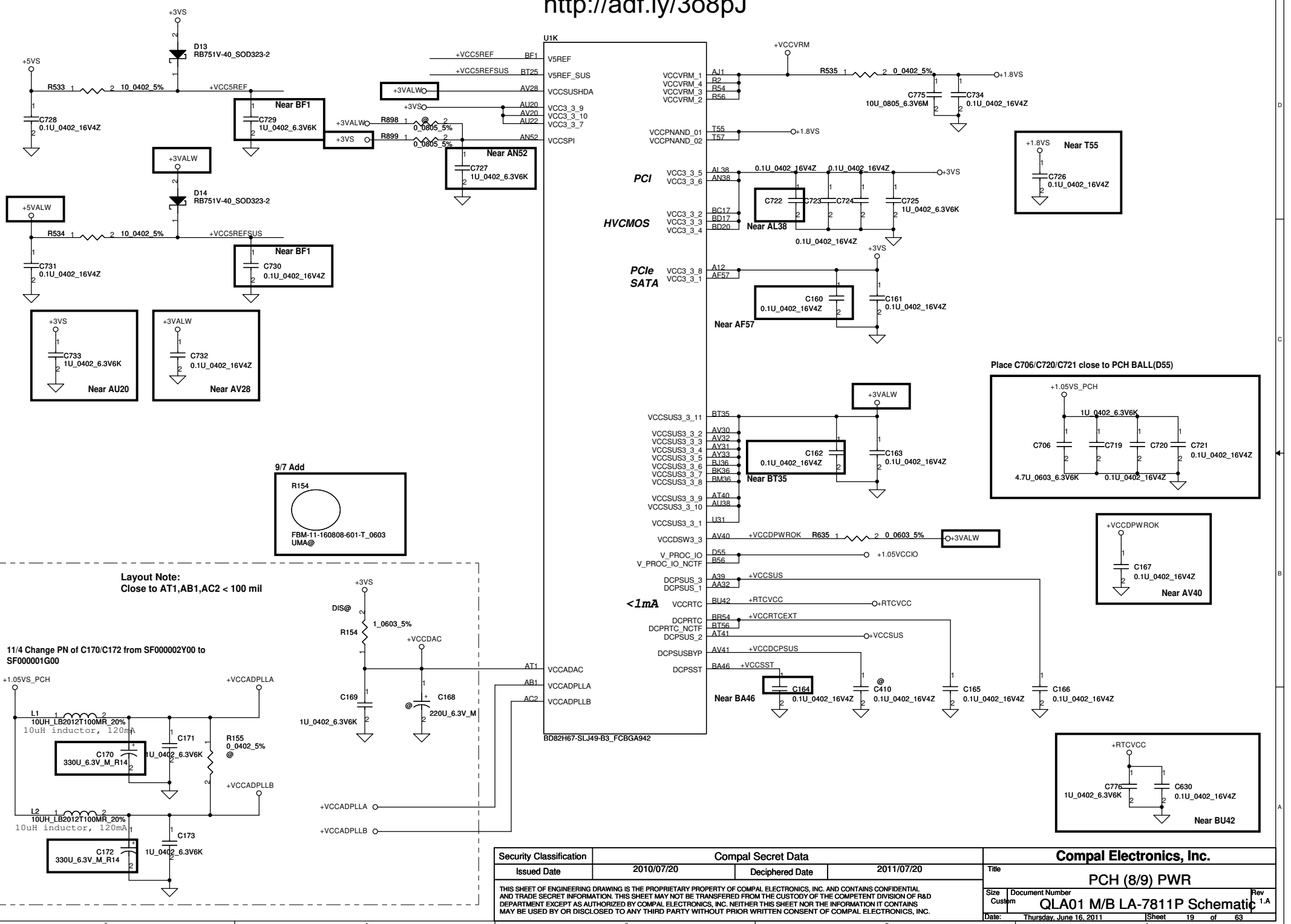
8/23 Add

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				Customer	1.A
				Date:	Thursday, June 16, 2011
				Sheet	17 of 63
				PCH (6/9) CLOCK	
				QLA01 M/B LA-7811P Schematic	

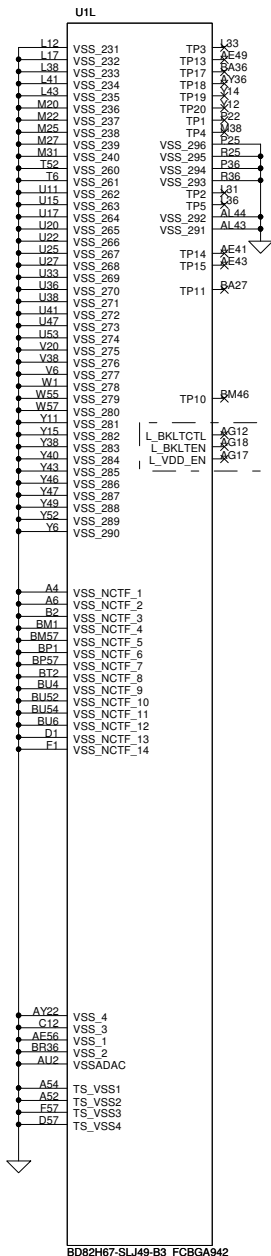


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BD82H67-SLJ49-B3_FCBGA942

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Size	Document Number	Rev		1.A	
Custom	QLA01 M/B LA-7811P Schematic	Date		Thursday, June 16, 2011	
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U1J		OPT.09E	
BC15	VSS_125	VSS_5	A29
BC20	VSS_126	VSS_6	A42
BC27	VSS_127	VSS_7	A49
BC31	VSS_128	VSS_8	A9
BC36	VSS_129	VSS_9	AA20
BC38	VSS_130	VSS_10	AA22
BC47	VSS_131	VSS_11	AA24
BC9	VSS_132	VSS_12	AA26
BD25	VSS_133	VSS_13	AA28
BD33	VSS_134	VSS_14	AA30
BF12	VSS_135	VSS_15	AA38
BF20	VSS_136	VSS_16	AB11
BF25	VSS_137	VSS_17	AB15
BF33	VSS_138	VSS_18	AB40
BF41	VSS_139	VSS_19	AB41
BF43	VSS_140	VSS_20	AB43
BF46	VSS_141	VSS_21	AB47
BF52	VSS_142	VSS_22	AB52
BF6	VSS_143	VSS_23	AB57
BG22	VSS_144	VSS_24	AB6
BG25	VSS_145	VSS_25	AC22
BG27	VSS_146	VSS_26	AC34
BG31	VSS_147	VSS_27	AC36
BG33	VSS_148	VSS_28	AC38
BG36	VSS_149	VSS_29	AC4
BG38	VSS_150	VSS_30	AC4
BG38	VSS_150	VSS_30	AC4
BH2	VSS_151	VSS_31	AE14
BH6	VSS_152	VSS_32	AE18
RJ1	VSS_153	VSS_33	AE22
RJ15	VSS_154	VSS_34	AE22
RK20	VSS_155	VSS_35	AE38
RK41	VSS_156	VSS_36	AE4
RK52	VSS_157	VSS_37	AE47
BK6	VSS_158	VSS_38	AE9
BM10	VSS_159	VSS_39	AF52
BM12	VSS_160	VSS_40	AF6
BM16	VSS_161	VSS_41	AG11
BM22	VSS_162	VSS_42	AG14
BM23	VSS_163	VSS_43	AG20
BM26	VSS_164	VSS_44	AG22
BM28	VSS_165	VSS_45	AG30
BM32	VSS_166	VSS_46	AG36
BM40	VSS_167	VSS_47	AG43
BM42	VSS_168	VSS_48	AG44
BM48	VSS_169	VSS_49	AG46
BM5	VSS_170	VSS_50	AG5
BN1	VSS_171	VSS_51	AG50
BN17	VSS_172	VSS_52	AH52
BN6	VSS_173	VSS_53	AH6
BP3	VSS_174	VSS_54	AJ22
BP33	VSS_175	VSS_55	AJ30
BP35	VSS_176	VSS_56	AJ57
BR22	VSS_177	VSS_57	AK52
BR52	VSS_178	VSS_58	AK6
BU19	VSS_179	VSS_59	AL11
BU26	VSS_180	VSS_60	AL18
BU29	VSS_181	VSS_61	AL22
BU36	VSS_182	VSS_62	AL26
BU39	VSS_183	VSS_63	AL30
C19	VSS_184	VSS_64	AL36
C32	VSS_185	VSS_65	AL41
C39	VSS_186	VSS_66	AL46
C4	VSS_187	VSS_67	AL47
D15	VSS_188	VSS_68	AM52
D23	VSS_189	VSS_69	AM5
D3	VSS_190	VSS_70	AM57
D35	VSS_191	VSS_71	AN11
D43	VSS_192	VSS_72	AN12
D45	VSS_193	VSS_73	AN15
E19	VSS_194	VSS_74	AN17
E39	VSS_195	VSS_75	AN18
E54	VSS_196	VSS_76	AN20
E6	VSS_197	VSS_77	AN30
E9	VSS_198	VSS_78	AN36
F10	VSS_199	VSS_79	AN4
F12	VSS_200	VSS_80	AN43
F16	VSS_201	VSS_81	AN47
F22	VSS_202	VSS_82	AN54
F26	VSS_203	VSS_83	AN9
F32	VSS_204	VSS_84	AR20
F33	VSS_205	VSS_85	AR22
F35	VSS_206	VSS_86	AR52
F36	VSS_207	VSS_87	AR6
F40	VSS_208	VSS_88	AT15
F42	VSS_209	VSS_89	AT18
F46	VSS_210	VSS_90	AT43
F48	VSS_211	VSS_91	AT47
F50	VSS_212	VSS_92	AT52
F8	VSS_213	VSS_93	AT6
AV18	VSS_104	VSS_94	AT8
AV22	VSS_105	VSS_95	AU24
AV34	VSS_106	VSS_96	AU26
AV38	VSS_107	VSS_97	AU28
AV47	VSS_108	VSS_98	AU5
AV6	VSS_109	VSS_99	AV12
AW57	VSS_110	VSS_100	BA49
AY38	VSS_111	VSS_101	BB1
AV6	VSS_112	VSS_102	BB2
B23	VSS_113	VSS_103	BB52
BA11	VSS_114	VSS_104	BB6
BA12	VSS_115	VSS_105	BC14
BA31	VSS_116	VSS_106	BM33
BA41	VSS_117	VSS_107	BM36
BA44	VSS_118	VSS_108	BM46
G54	VSS_214	VSS_124	IM33
H15	VSS_215	VSS_241	IM36
H20	VSS_216	VSS_242	IM46
H22	VSS_217	VSS_243	IM52
H25	VSS_218	VSS_244	IM57
H27	VSS_219	VSS_245	IM6
H33	VSS_220	VSS_246	IM8
H6	VSS_221	VSS_247	IM9
J1	VSS_222	VSS_248	IM4
J33	VSS_223	VSS_249	IM54
J46	VSS_224	VSS_250	R11
J48	VSS_225	VSS_251	R15
J5	VSS_226	VSS_252	R17
J53	VSS_227	VSS_253	R22
K52	VSS_228	VSS_254	R4
K6	VSS_229	VSS_255	R41
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		VSS_257	R46
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		VSS_259	

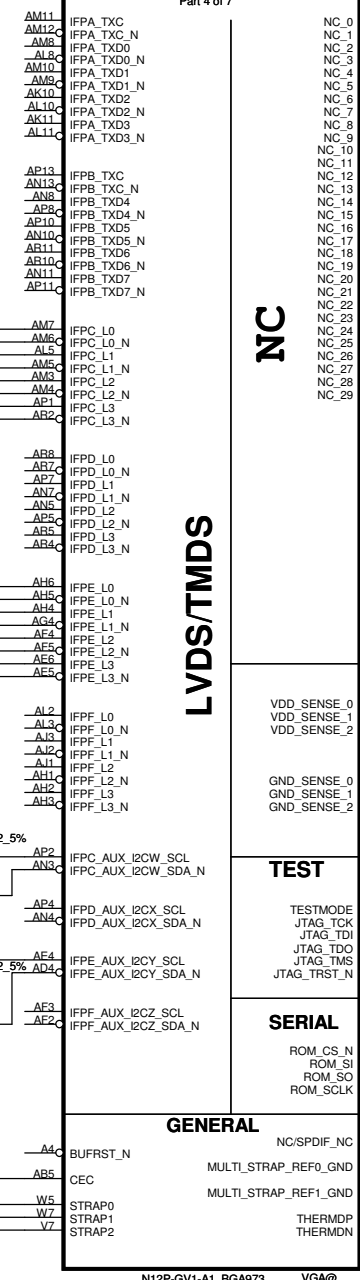


NOTE: PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

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Title	PCH(9/9)VSS			
Size	Document Number	Rev		
Custom	QLA01 M/B LA-7811P Schematic	1.A		
Date:	Thursday, June 16, 2011	Sheet	20	of 63

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NC

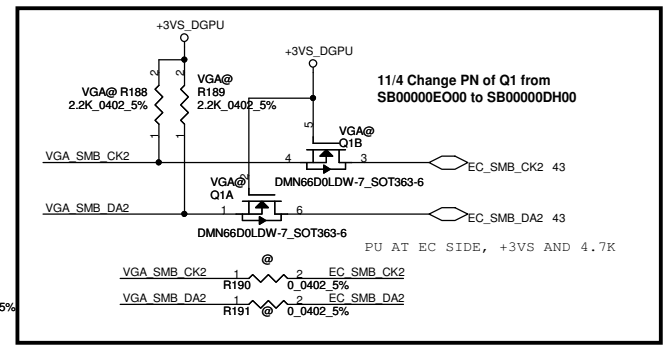
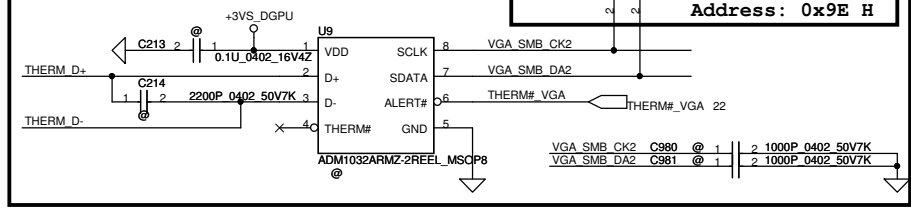
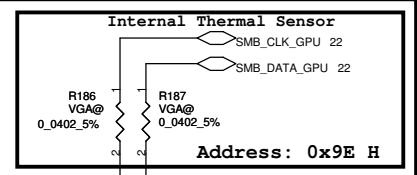
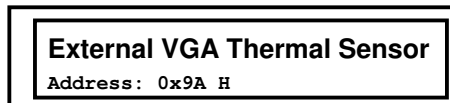
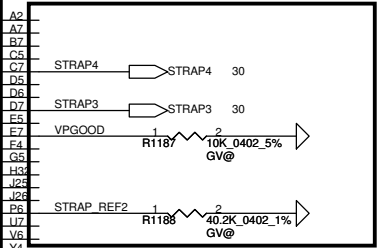
LVDS/TMDS

TEST

SERIAL

GENERAL

N12P-GV1-A1_BGA973



To HDMI-out

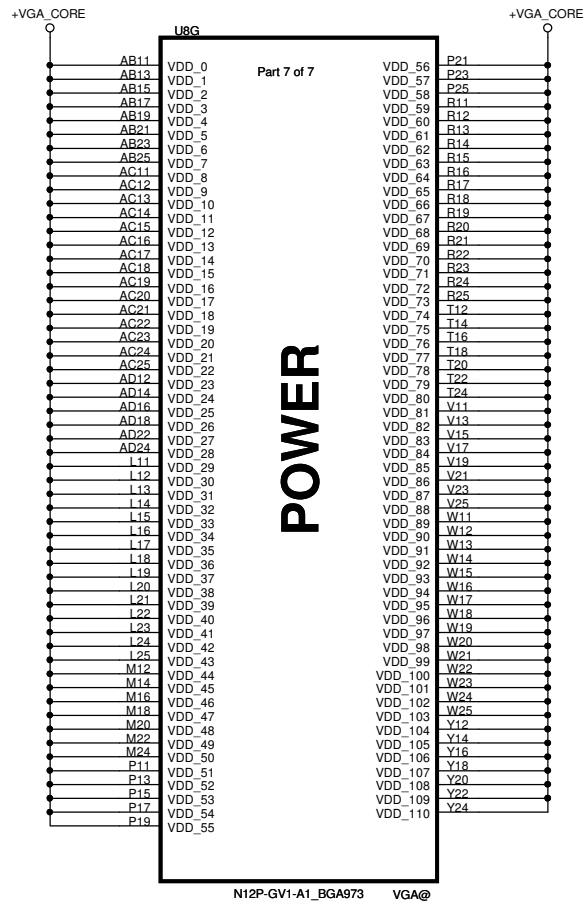
To 2D/3D Vision

HDMI-OUT

Scalar

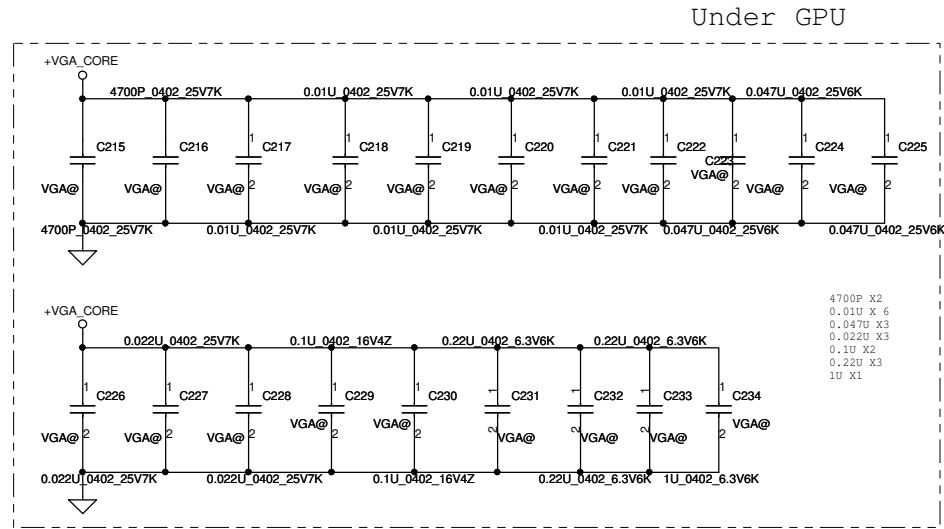
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Title		Compal Electronics, Inc.	
		VGA(1/12)-LVDS/HDMI/DP/THM	
Size	Document Number	Rev	
	QLA01 M/B LA-7811P Schematic	1.A	
Date:	Thursday, June 16, 2011	Sheet	21 of 63

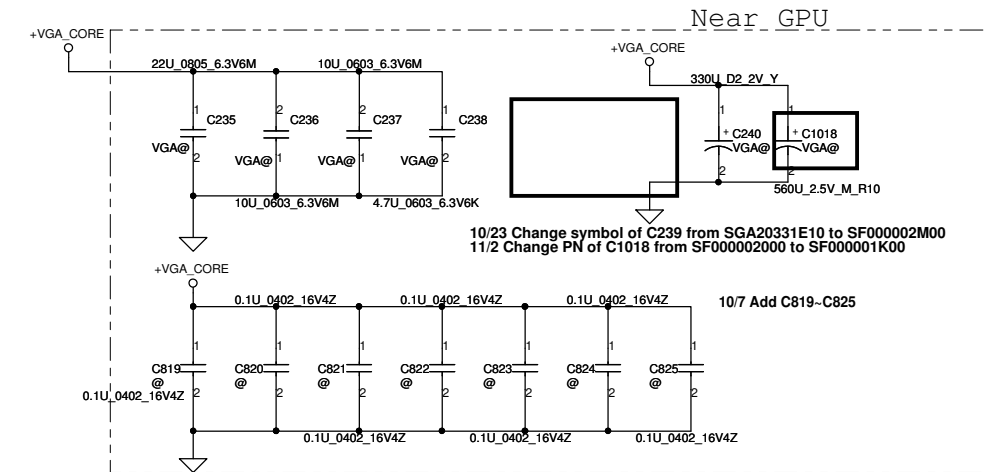


N12P-GV1-A1_BGA973

VGA@



4700P X2
0.01U X6
0.047U X3
0.022U X3
0.1U X2
0.22U X3
1U X1

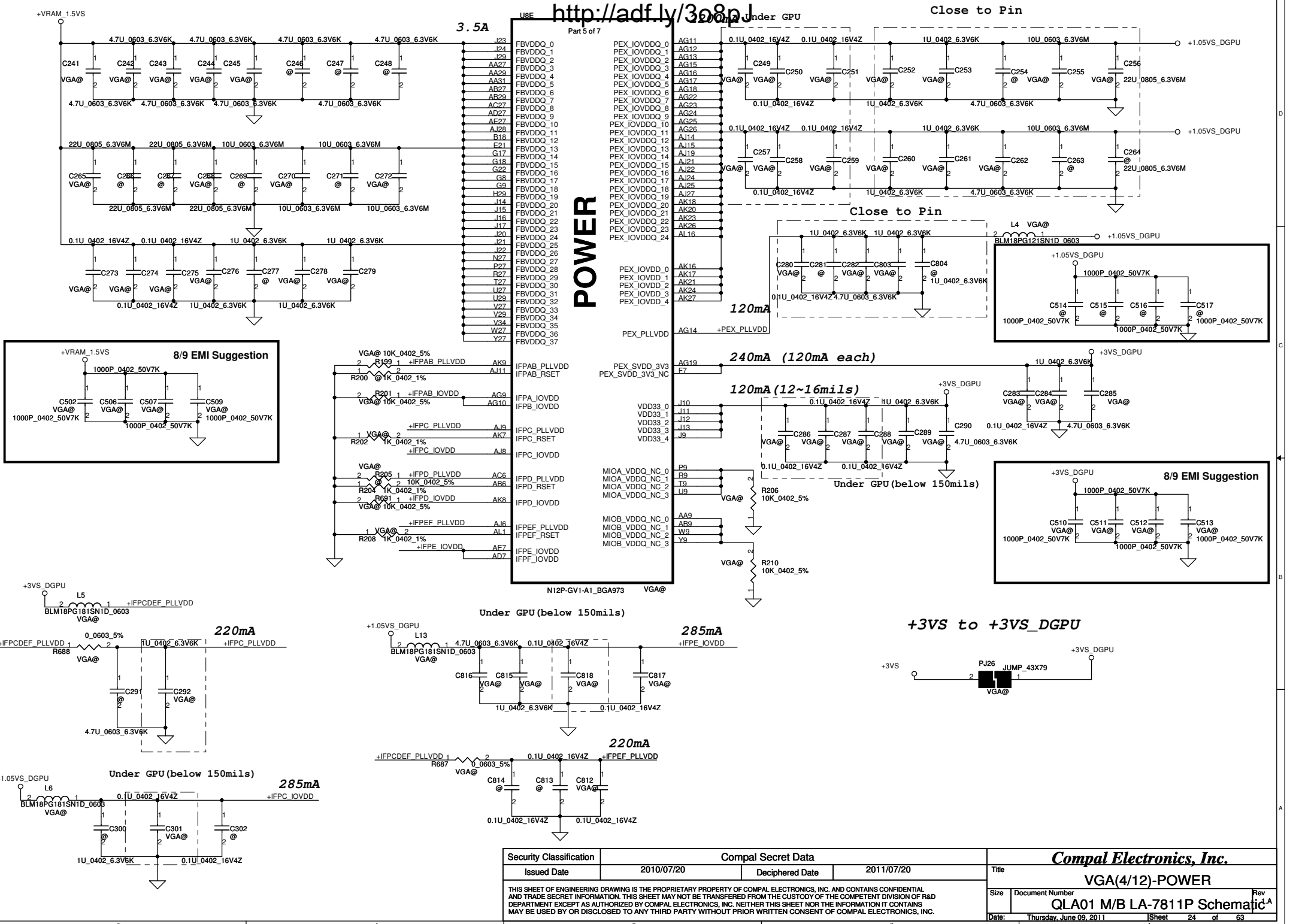


10/23 Change symbol of C239 from SGA20331E10 to SF000002M00
11/2 Change PN of C1018 from SF000002000 to SF000001K00

10/7 Add C819-C825

Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	VGA(3/12)-VGA CORE	
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<http://adf.ly/368pJ>



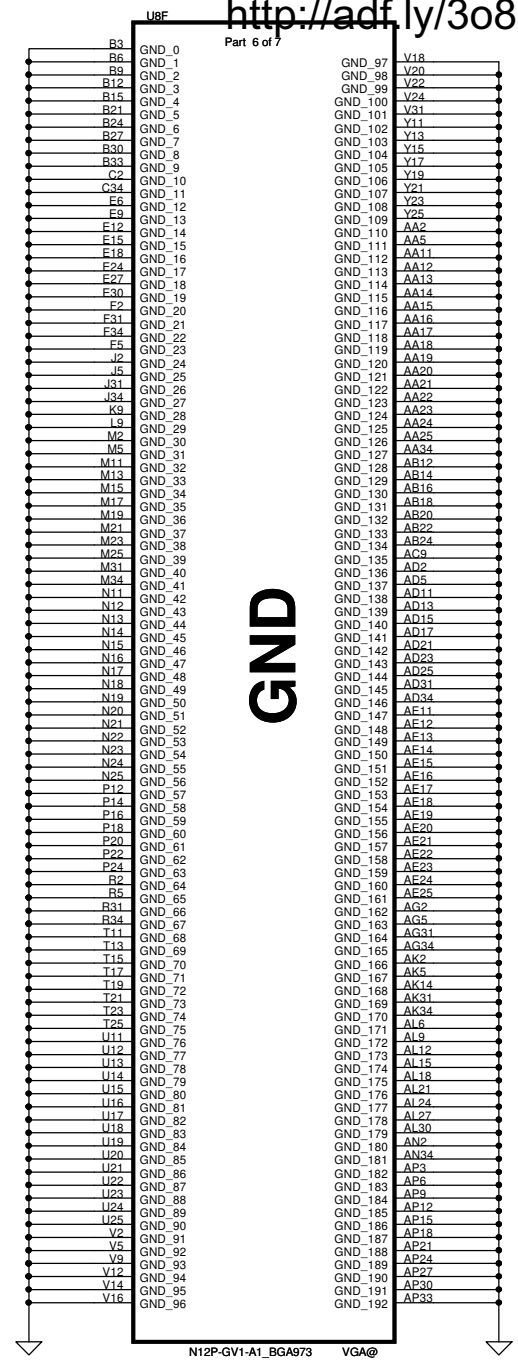
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	VGA(4/12)-POWER	
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Size	Document Number	Rev		Date	
	QLA01 M/B LA-7811P Schematic	A		Thursday, June 09, 2011	
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VGA(4/12)-POWER

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Title VGA(5/12)-GND	
Size	Document Number QLA01 M/B LA-7811P Schematic
Date:	Thursday, June 09, 2011
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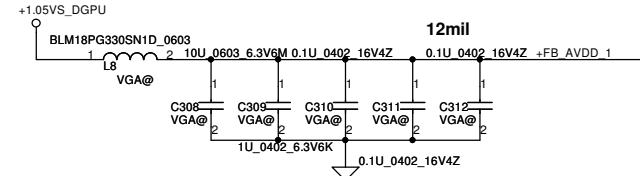
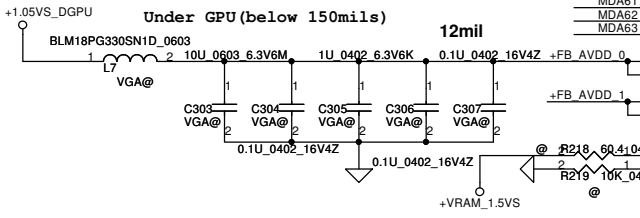
28.29 MDA[0..63] ← MDA[0..63]

Part 2 of 7

MDA0	L32	FBA_D0
MDA1	N33	FBA_D1
MDA2	L33	FBA_D2
MDA3	N34	FBA_D3
MDA4	N35	FBA_D4
MDA5	P35	FBA_D5
MDA6	P33	FBA_D6
MDA7	P34	FBA_D7
MDA8	K35	FBA_D8
MDA9	K33	FBA_D9
MDA10	K34	FBA_D10
MDA11	H33	FBA_D11
MDA12	G34	FBA_D12
MDA13	G33	FBA_D13
MDA14	F34	FBA_D14
MDA15	F33	FBA_D15
MDA16	G31	FBA_D16
MDA17	F30	FBA_D17
MDA18	G30	FBA_D18
MDA19	G32	FBA_D19
MDA20	K30	FBA_D20
MDA21	K32	FBA_D21
MDA22	H30	FBA_D22
MDA23	K31	FBA_D23
MDA24	L31	FBA_D24
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MDA28	N30	FBA_D28
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MDA30	R32	FBA_D30
MDA31	R30	FBA_D31
MDA32	AG30	FBA_D32
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MDA34	AH31	FBA_D34
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MDA60	AE34	FBA_D60
MDA61	AE33	FBA_D61
MDA62	AB32	FBA_D62
MDA63	AC35	FBA_D63

MEMORY INTERFACE

FBA_CMD0	U30	CMDA0	CMDA0	28
FBA_CMD1	V30	CMDA2	CMDA2	28
FBA_CMD2	U31	CMDA3	CMDA3	28
FBA_CMD3	T35	CMDA4	CMDA4	28,29
FBA_CMD4	U33	CMDA5	CMDA5	28,29
FBA_CMD5	W32	CMDA6	CMDA6	28,29
FBA_CMD6	W32	CMDA7	CMDA7	28,29
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FBA_CMD14	T33	CMDA15	CMDA15	28,29
FBA_CMD15	U30	CMDA16	CMDA16	29
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FBA_WCK2	L29	WCK2	WCK2	28
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FBA_WCK4	AG24	WCK4	WCK4	28
FBA_WCK5	AH24	WCK5	WCK5	28
FBA_WCK6	AD24	WCK6	WCK6	28
FBA_WCK7	AE24	WCK7	WCK7	28
FBA_CLK0	T32	CLKA0	CLKA0	28
FBA_CLK1	T31	CLKA0#	CLKA0#	28
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FBA_CLK1#	AC30	CLKA1#	CLKA1#	29

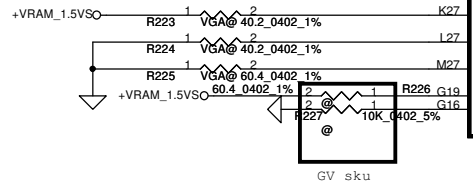


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Date:	Thursday, June 16, 2011	Sheet:	26	of 63	

U8C
Part 3 of 7

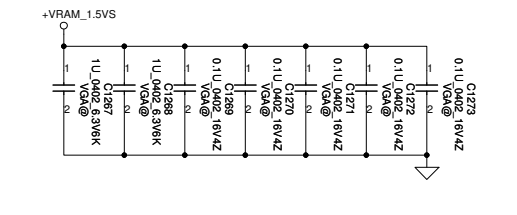
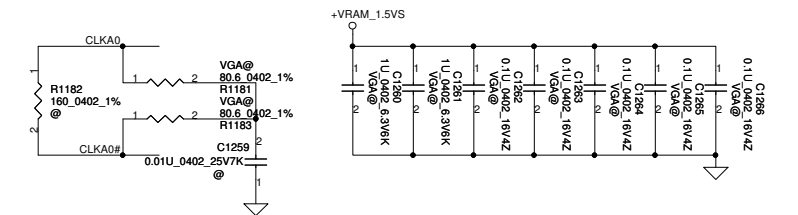
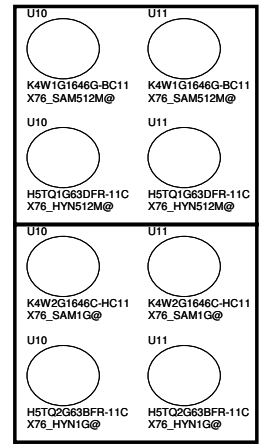
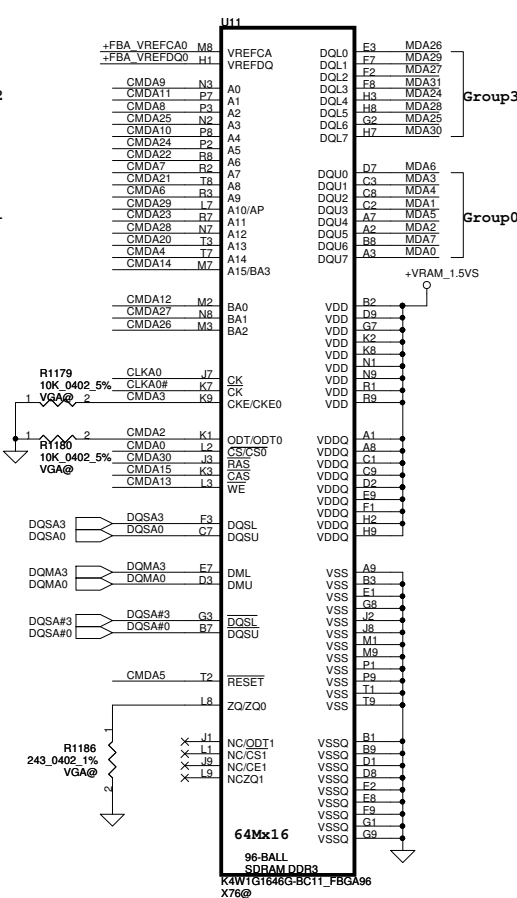
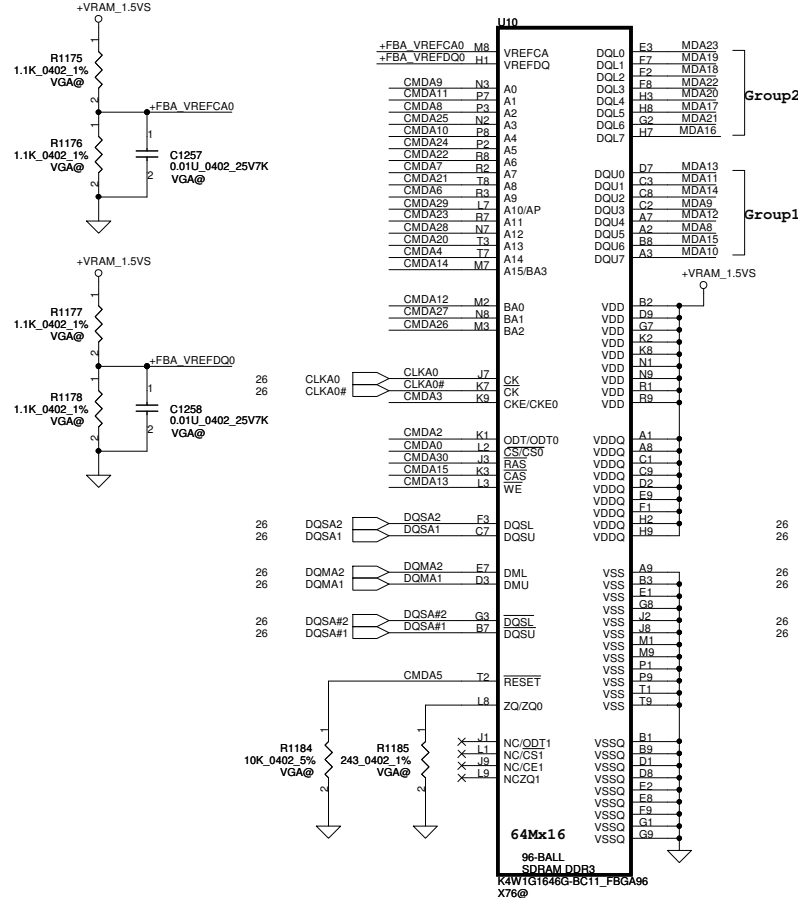
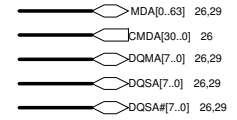
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FBC_D3	FBC_CMD3	G17
FBC_D4	FBC_CMD4	E19
FBC_D5	FBC_CMD5	C19
FBC_D6	FBC_CMD6	B17
FBC_D7	FBC_CMD7	E20
FBC_D8	FBC_CMD8	B19
FBC_D9	FBC_CMD9	D20
FBC_D10	FBC_CMD10	A19
FBC_D11	FBC_CMD11	D19
FBC_D12	FBC_CMD12	C20
FBC_D13	FBC_CMD13	E20
FBC_D14	FBC_CMD14	B20
FBC_D15	FBC_CMD15	G21
FBC_D16	FBC_CMD16	E22
FBC_D17	FBC_CMD17	E24
FBC_D18	FBC_CMD18	E23
FBC_D19	FBC_CMD19	C25
FBC_D20	FBC_CMD20	C23
FBC_D21	FBC_CMD21	F21
FBC_D22	FBC_CMD22	E22
FBC_D23	FBC_CMD23	D21
FBC_D24	FBC_CMD24	A23
FBC_D25	FBC_CMD25	D22
FBC_D26	FBC_CMD26	B23
FBC_D27	FBC_CMD27	C22
FBC_D28	FBC_CMD28	B22
FBC_D29	FBC_CMD29	A22
FBC_D30	FBC_CMD30	A20
FBC_D31	FBC_CMD31	G20
FBC_D32	FBC_DOM0	A16
FBC_D33	FBC_DOM1	D10
FBC_D34	FBC_DOM2	F11
FBC_D35	FBC_DOM3	D15
FBC_D36	FBC_DOM4	D27
FBC_D37	FBC_DOM5	D34
FBC_D38	FBC_DOM6	A34
FBC_D39	FBC_DOM7	D28
FBC_D40		
FBC_D41	FBC_DQS_RN0	B14
FBC_D42	FBC_DQS_RN1	B10
FBC_D43	FBC_DQS_RN2	G9
FBC_D44	FBC_DQS_RN3	E14
FBC_D45	FBC_DQS_RN4	E26
FBC_D46	FBC_DQS_RN5	C31
FBC_D47	FBC_DQS_RN6	A31
FBC_D48	FBC_DQS_RN7	A26
FBC_D49		
FBC_D50	FBC_DQS_WP0	C14
FBC_D51	FBC_DQS_WP1	A10
FBC_D52	FBC_DQS_WP2	E10
FBC_D53	FBC_DQS_WP3	D14
FBC_D54	FBC_DQS_WP4	E28
FBC_D55	FBC_DQS_WP5	D32
FBC_D56	FBC_DQS_WP6	A32
FBC_D57	FBC_DQS_WP7	B26
FBC_D58		
FBC_D59	FBC_WCK0	G14
FBC_D60	FBC_WCK0_N	G15
FBC_D61	FBC_WCK1	G11
FBC_D62	FBC_WCK1_N	G12
FBC_D63	FBC_WCK2	G27
	FBC_WCK2_N	G28
	FBC_WCK3	G24
	FBC_WCK3_N	G25
	FBC_CLK0	E17
	FBC_CLK0_N	D17
	FBC_CLK1	D23
	FBC_CLK1_N	E23

MEMORY INTERFACE C



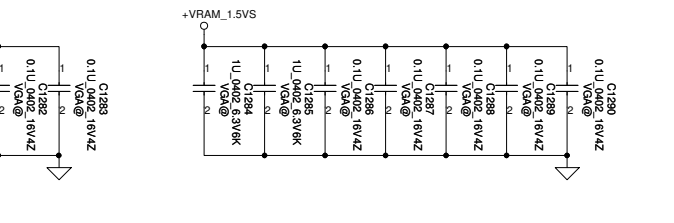
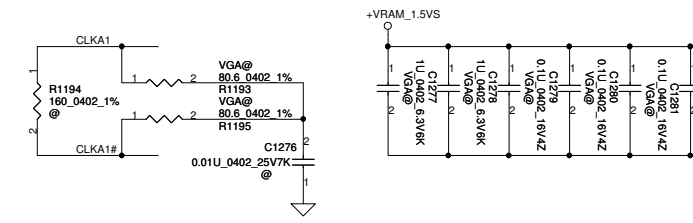
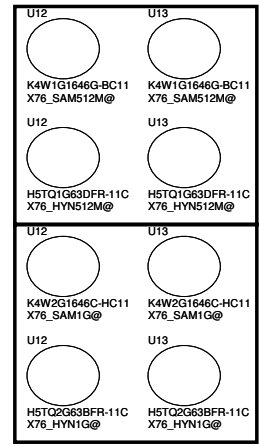
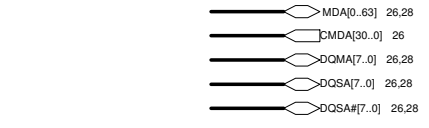
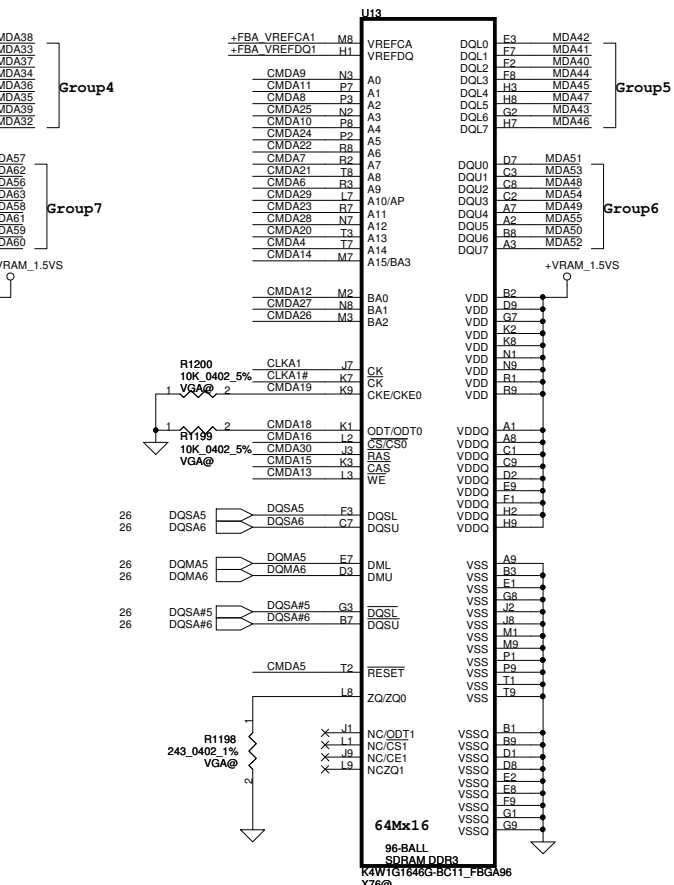
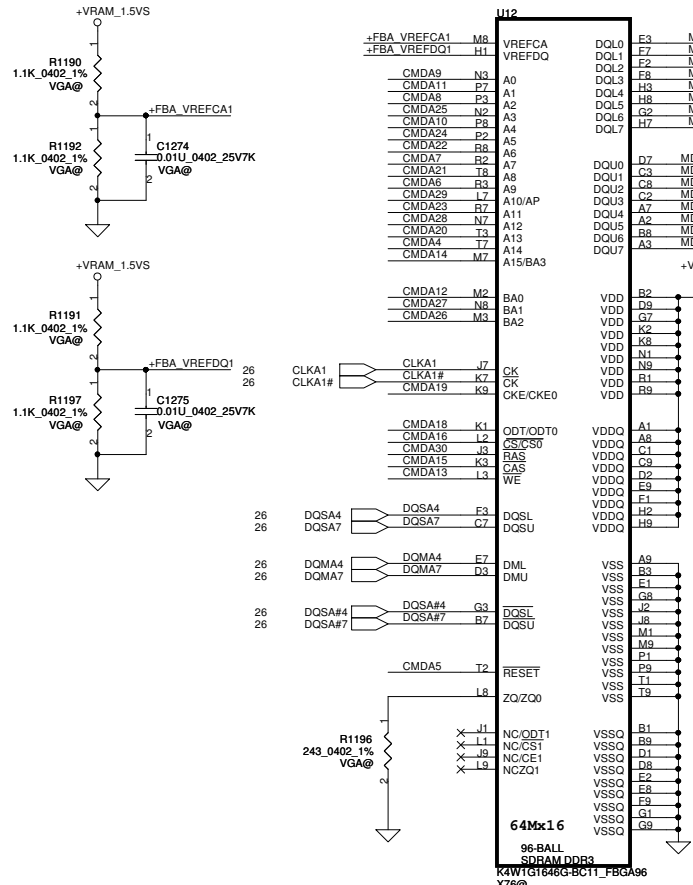
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Memory Partition A - Lower 32 bits

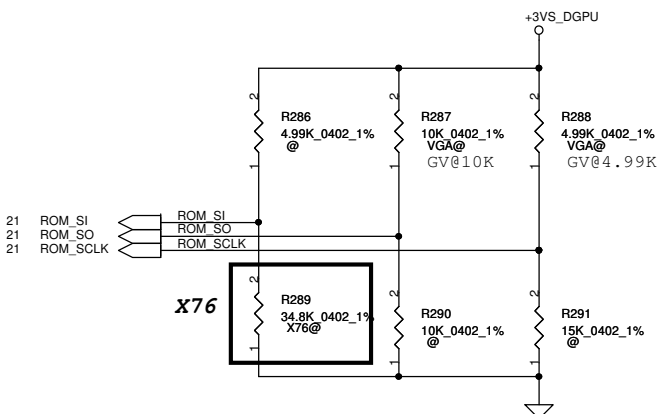
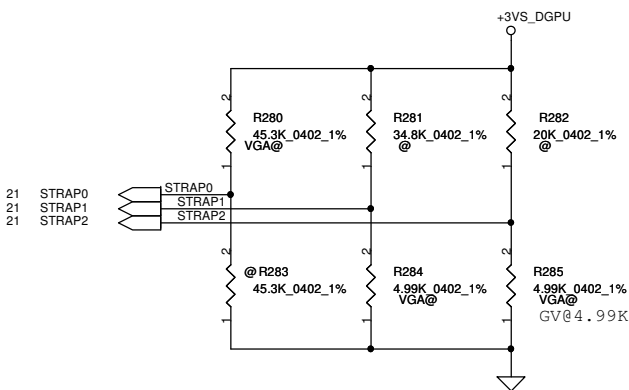


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				Size Custom	Document Number
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Memory Partition A - Upper 32 bits

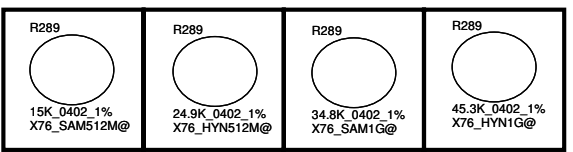
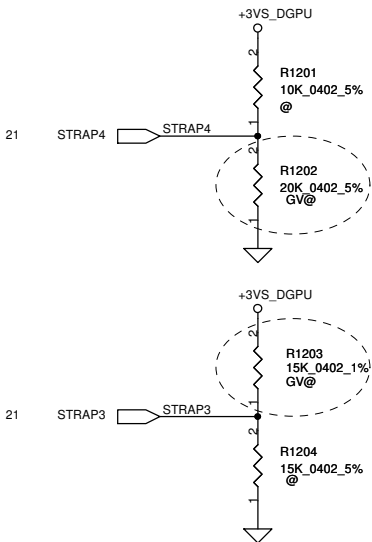


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Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	GS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
	GV	FB[1]	FB[0]		
ROM_SCLK	GS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
	GV			PCI_DEVID[5]	
ROM_SI	+3VGS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VGS	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VGS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VGS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VGS	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

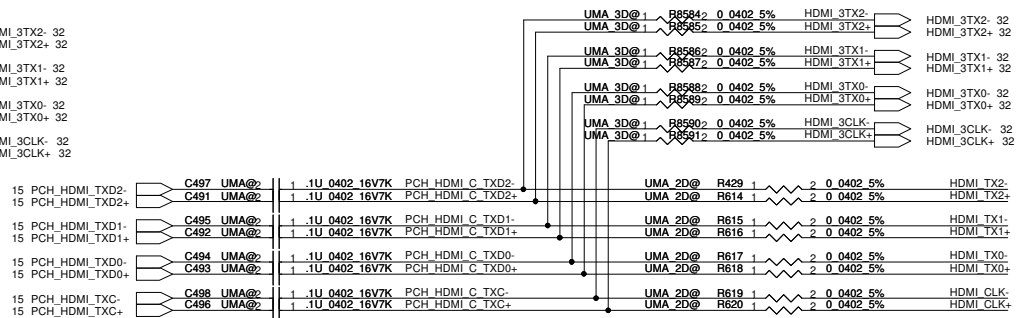
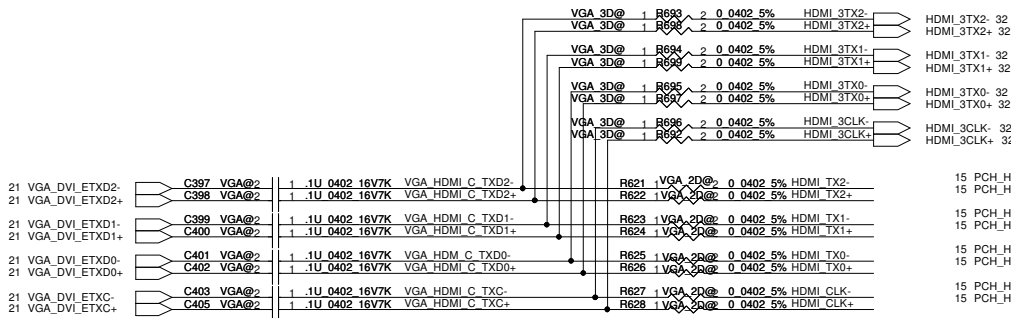


GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV	900 MHz	64M* 16* 4 512MB	K4W1G1646G-BC11 SA00004GS00	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0010 R289 PD 15K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	64M* 16* 4 512MB	H5TQ1G63DFR-11C SA000041S20	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0100 R289 PD 25K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	128M* 16* 4 1GB	K4W2G1646C-HC11 SA000047Q00	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0110 R289 PD 35K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	128M* 16* 4 1GB	H5TQ2G63BFR-11C SA00003Y030	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0111 R289 PD 45K	1001 R1228 PU 10K	1000 R1229 PU 5K

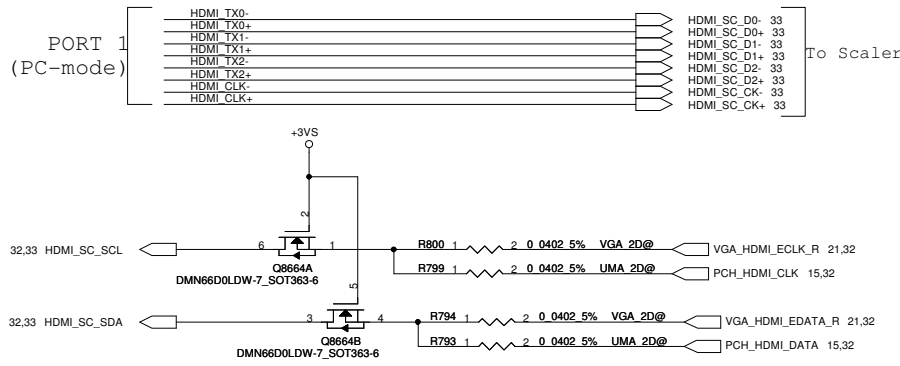
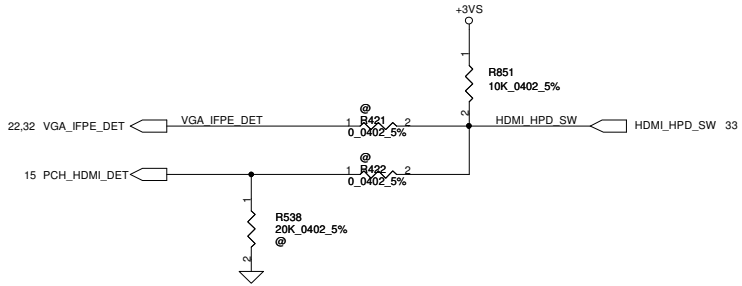
SUB_VENDOR		XCLK_417	
0	No VBIOS ROM (Default)	0	277MHz (Default)
1	BIOS ROM is present	1	Reserved
FB_0_BAR_SIZE		User [3:0]	
0	256MB (Default)	1111	EDID is used 1920x1080
1	Reserved	1000-1100	Customer defined
3GIO_PADCFG[3:0]		PEX_PLL_EN_TERM	
0000	RESERVED	0	Disable (Default)
0110	Notebook Default	1	Enable
SLOT_CLOCK_CFG			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)
PCIE_MAX_SPEED		DP_PLL_VDD33V	
1	Default	0	Default
GPU	Package	DeviceID	PCI_DEVID[5..0]
N12P-GS	GB2-128	0x0DF4	(. .1111 0100)
N12P-GV-B	GB2b-128	0x1050	(. .0101 0000)

0804 Vendor suggest close to Cap.

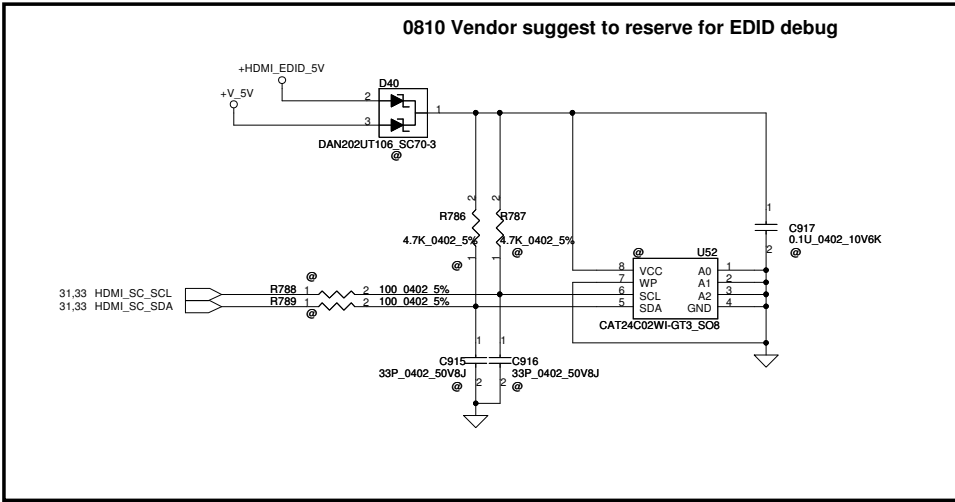
0804 Vendor suggest close to Cap.



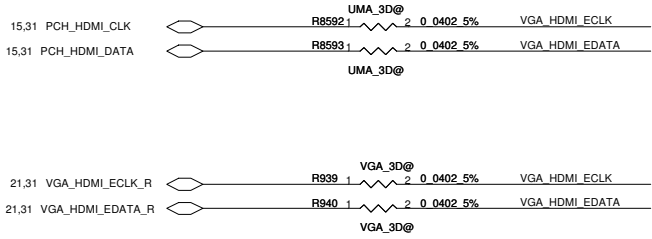
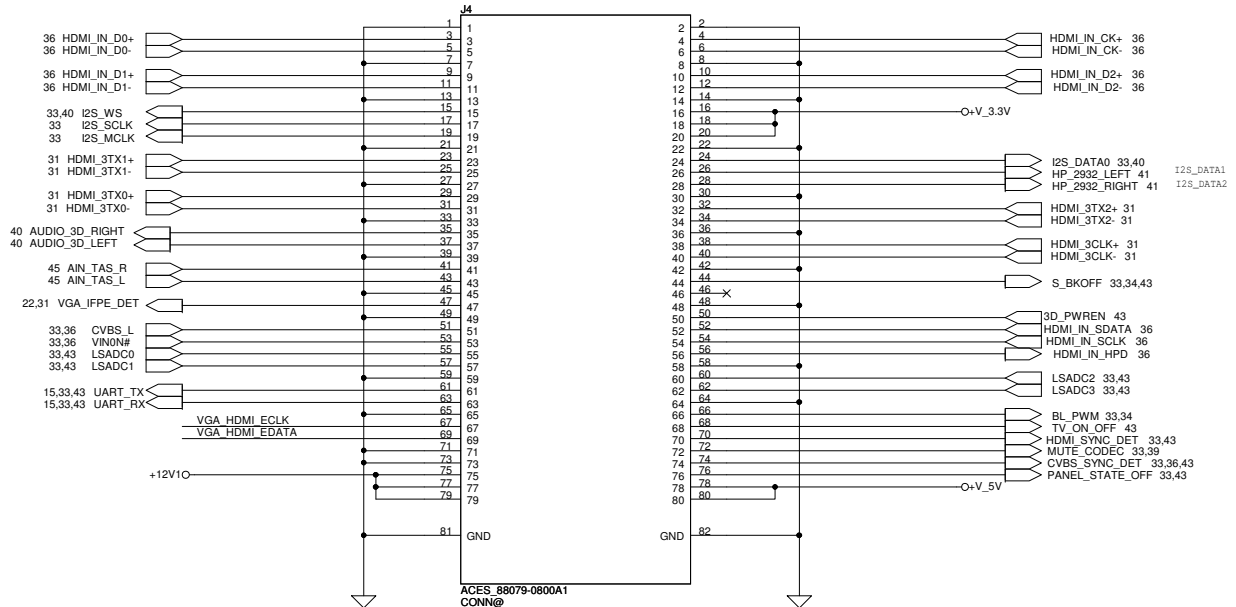
S2 (pin33)	S1 (pin32)	TMDS/DDC output
H	H	PORT1/SCL1, SDA1
H	L	PORT2/SCL2, SDA2
L	H	All disconnected



0810 Vendor suggest to reserve for EDID debug



12/11 3D Scaler Pin define update

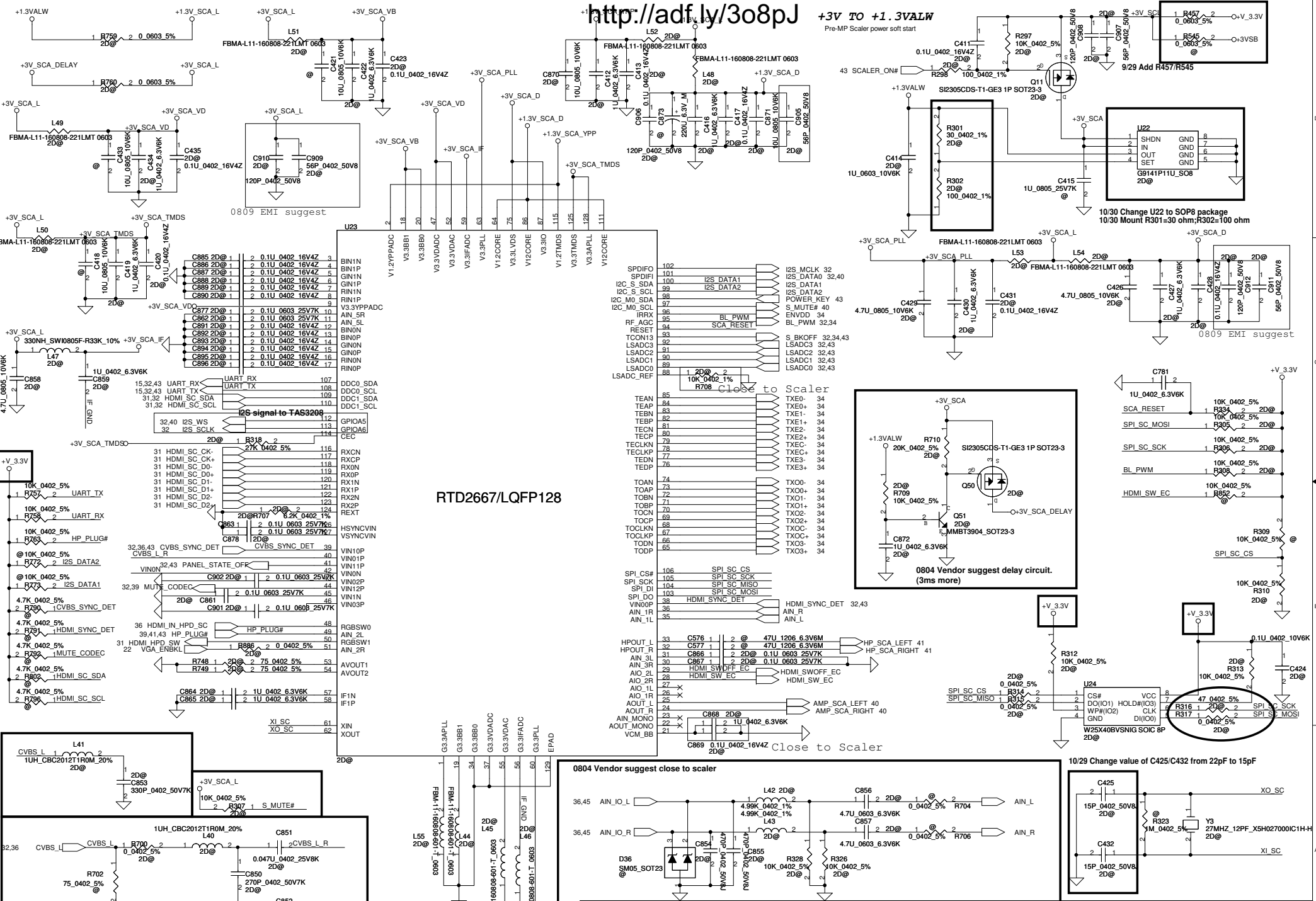


12/6 Change symbol of J4 from LTCX002TM00 to SP010011B00(60pin to 80pin)

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<http://adf.ly/3o8pJ>

+3V TO +1.3VALW
Pre-MP Scaler power soft start



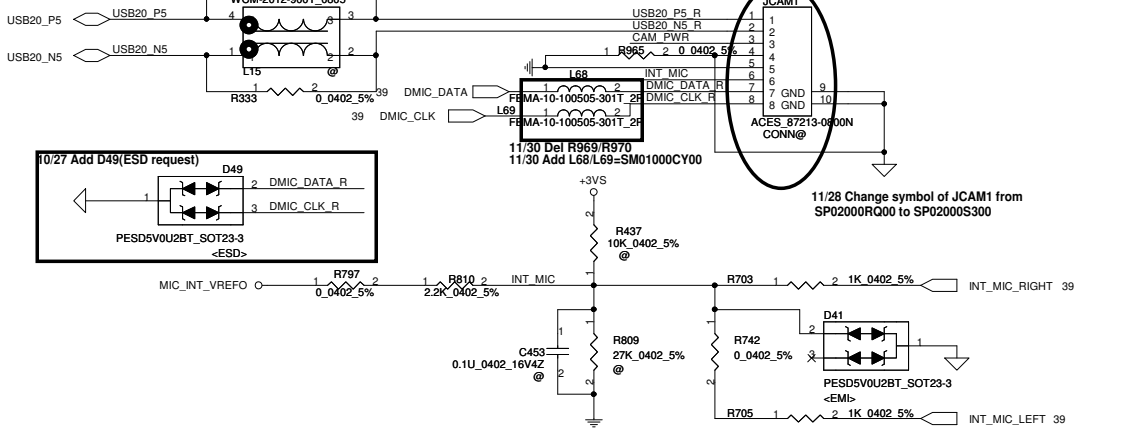
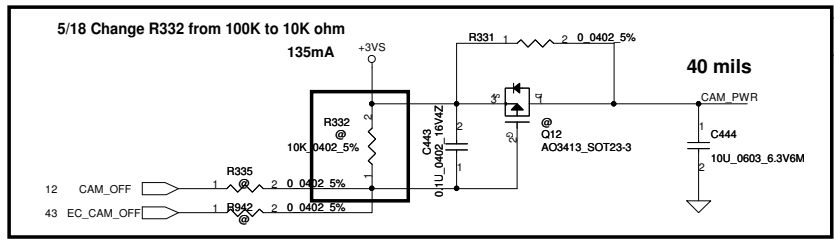
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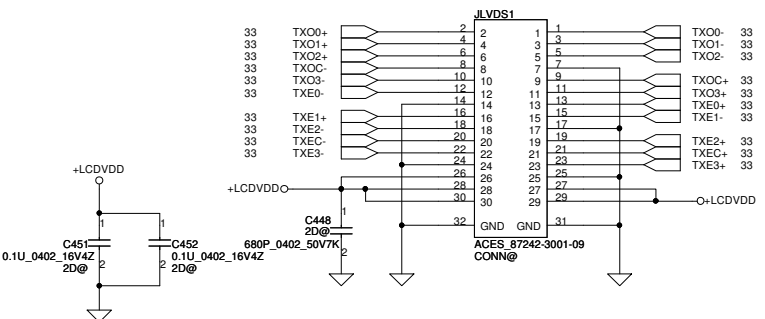
Compal Electronics, Inc.		
Scalar		
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WebCam+Digital Mic

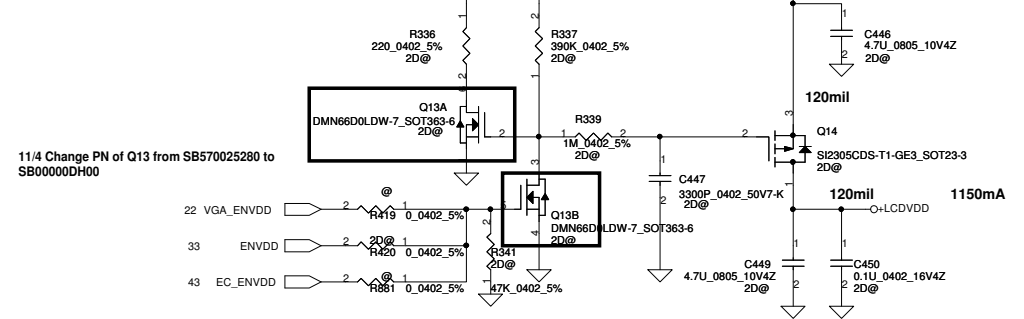
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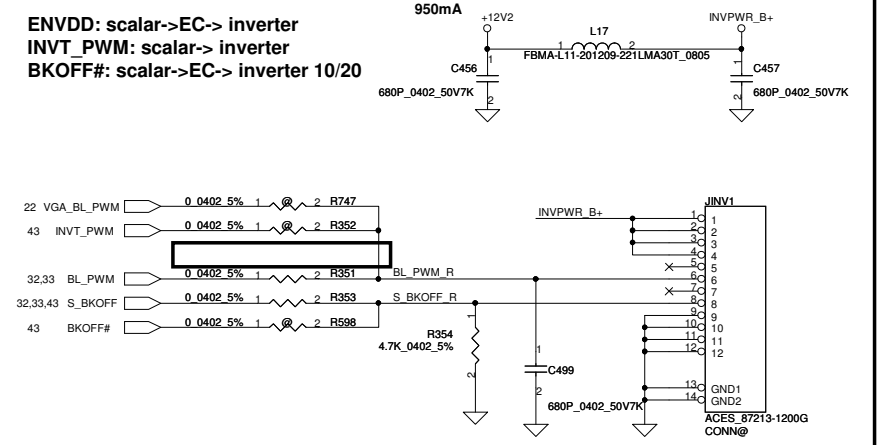
LVDS CONN



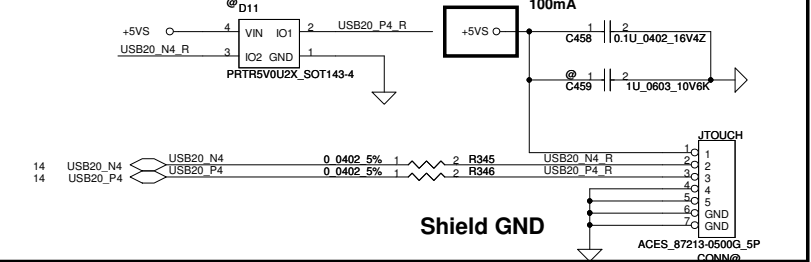
LVDS POWER



INVERTER

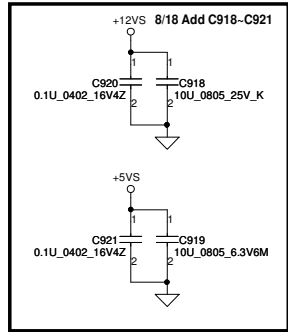


Touch Panel



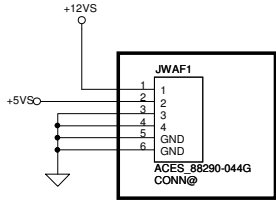
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HDD POWER Conn



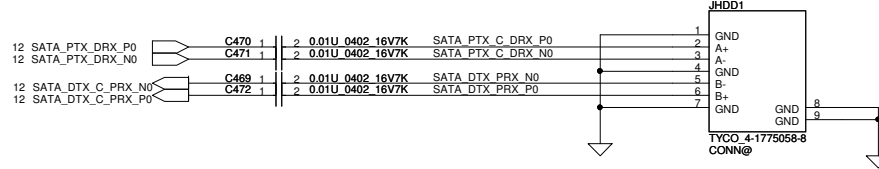
Layout Note: Place C918/C919/C920/C921 close to JWAFER1

HDD

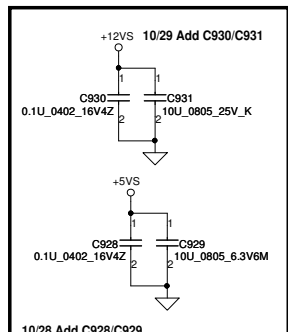


12/6 Change footprint of JWAF1 from SP02000A000 to SP02000EB00

SATA HDD Conn.



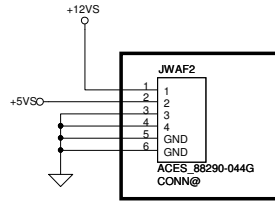
ODD POWER Conn



10/28 Add C928/C929

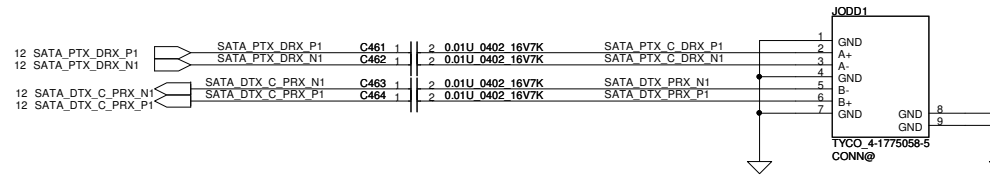
Layout Note: Place C928/C929 close to JWAFER2

ODD



12/6 Change footprint of JWAF1 from SP02000A000 to SP02000EB00

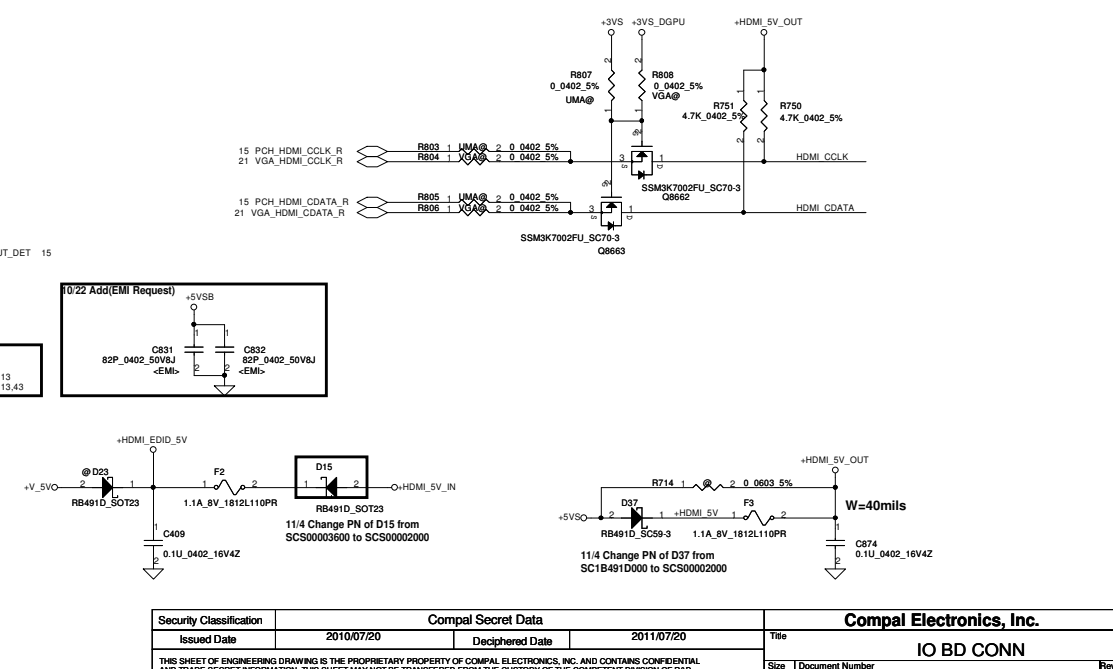
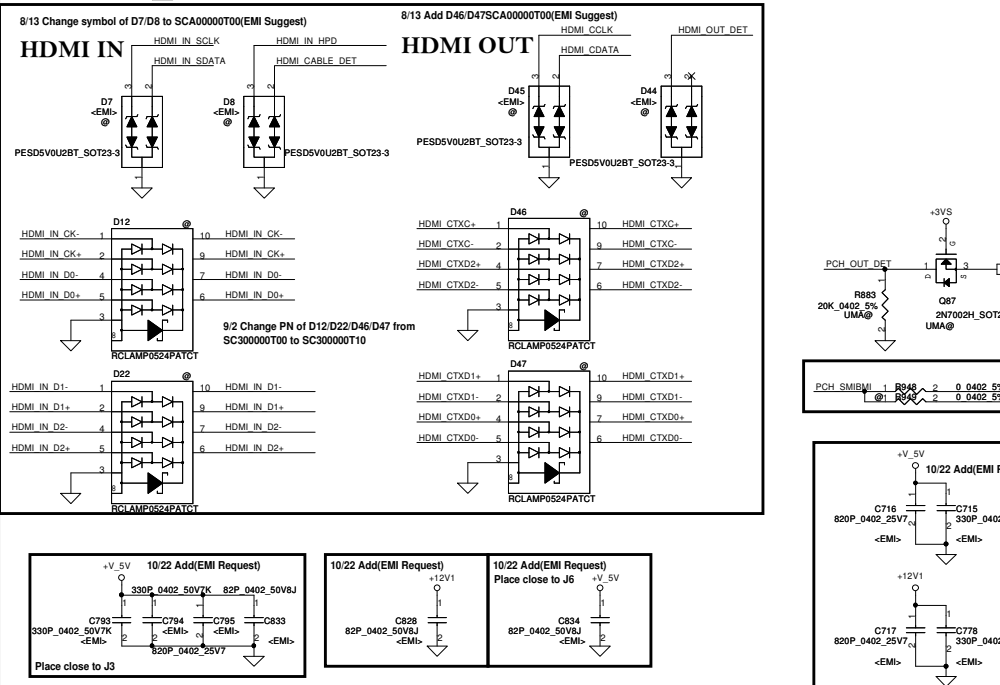
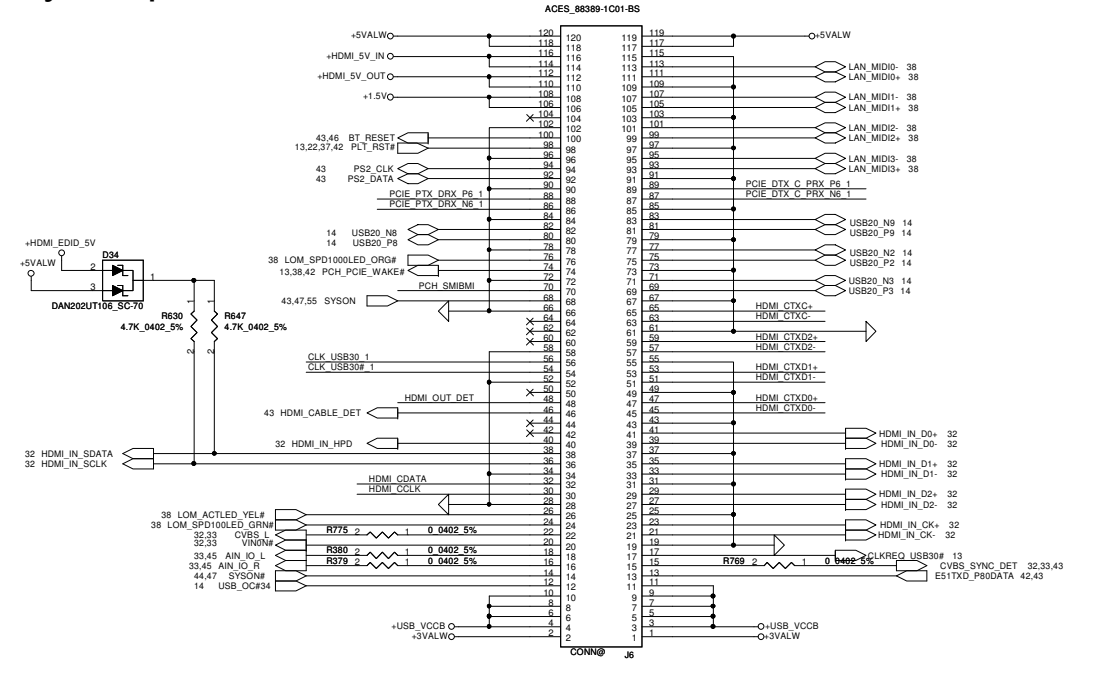
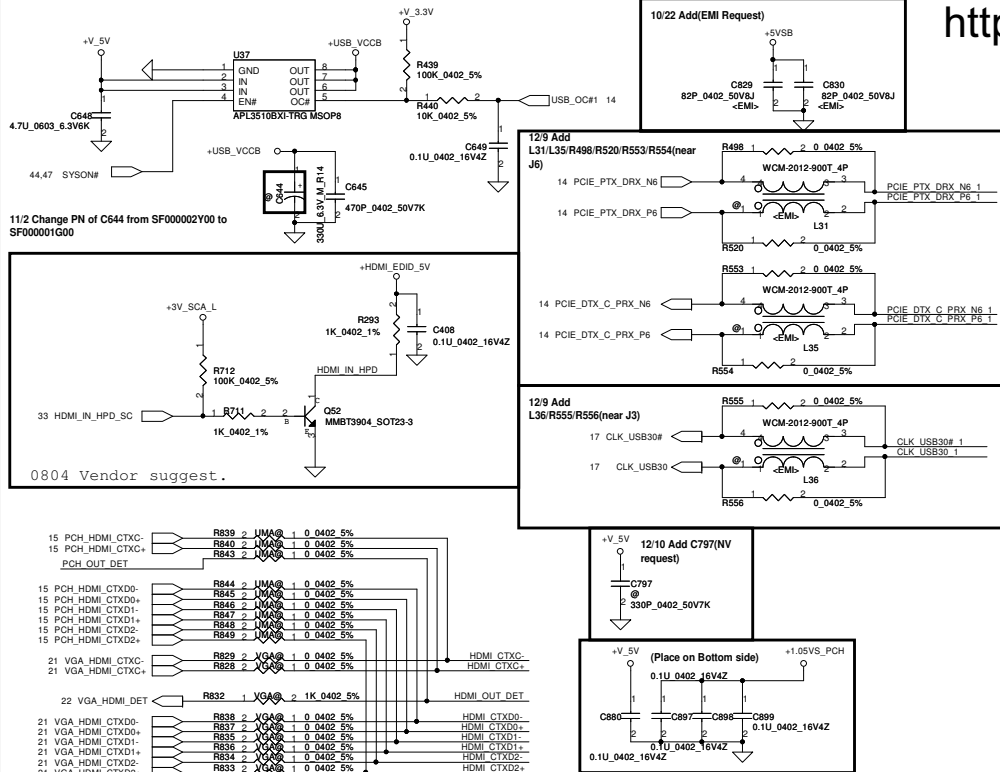
SATA ODD Conn.



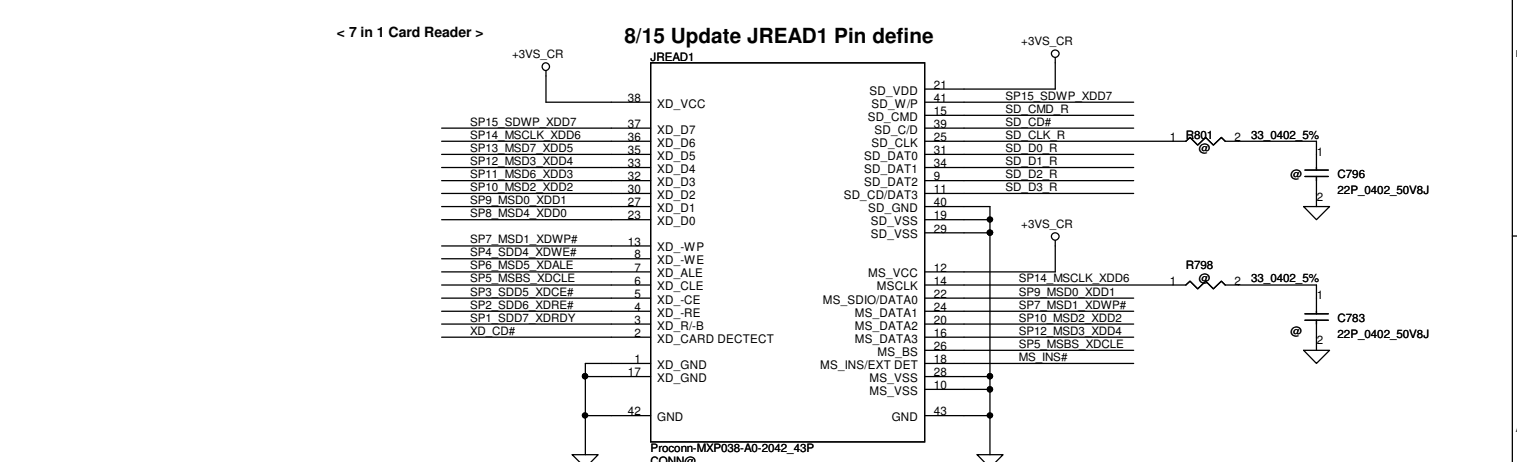
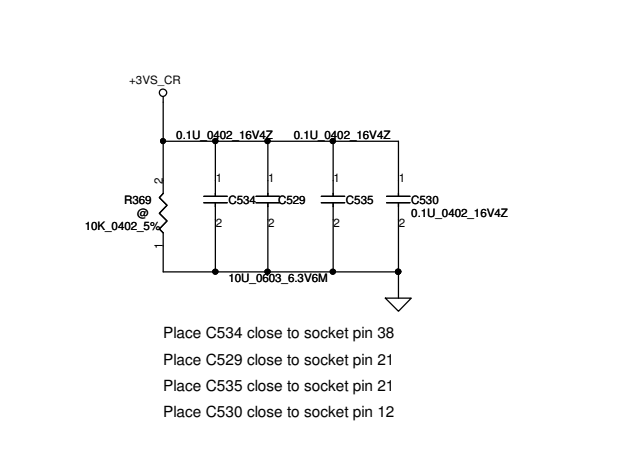
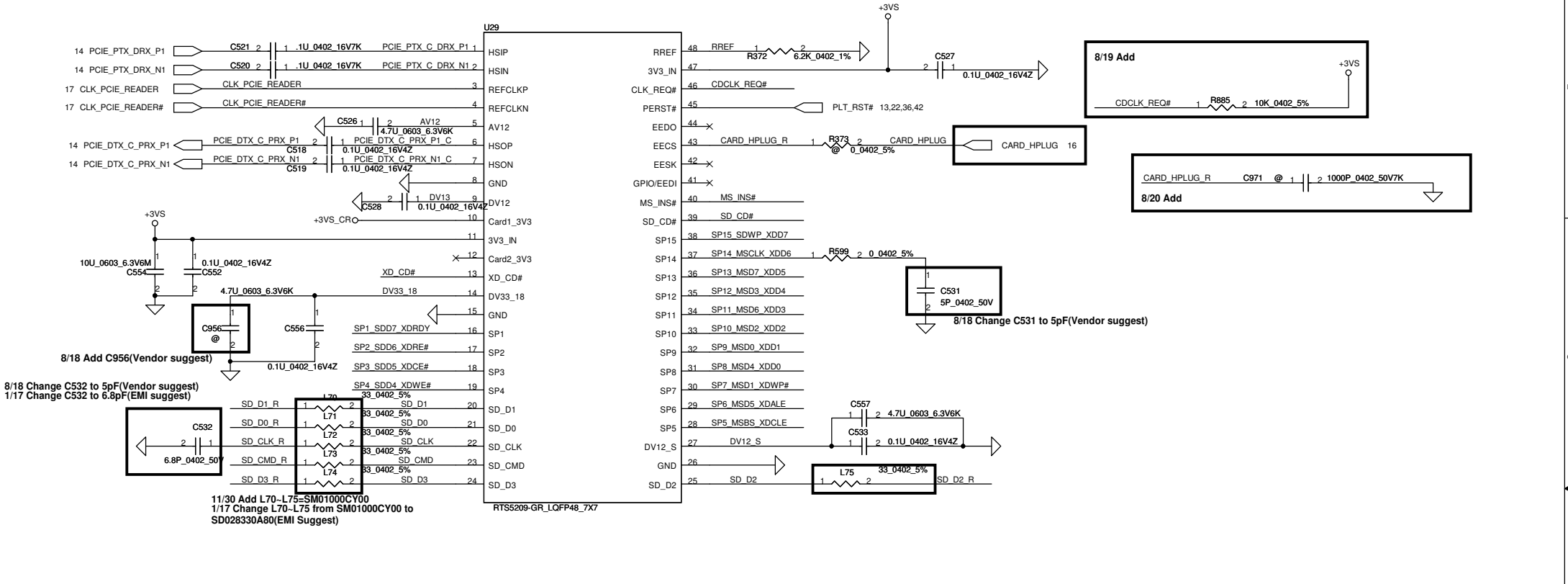
SSD

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				HDD & ODD & SSD Connector	
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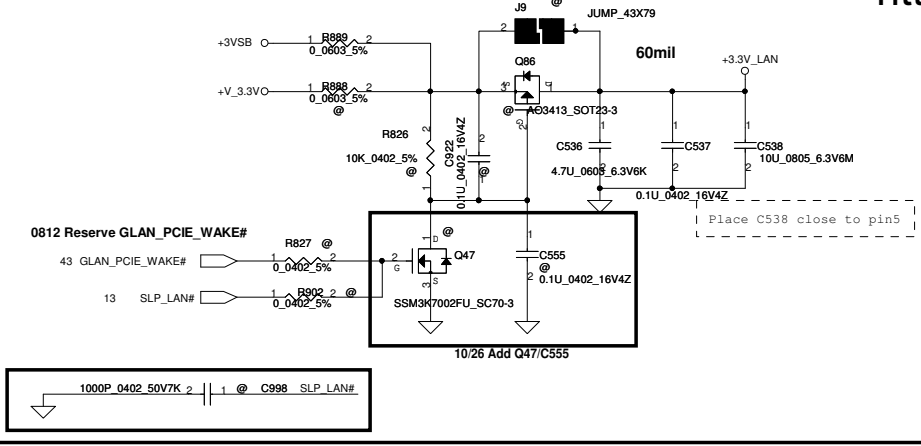
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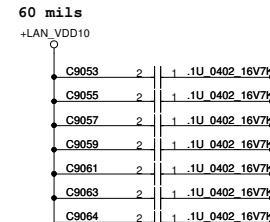
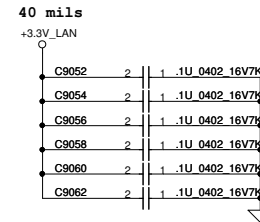
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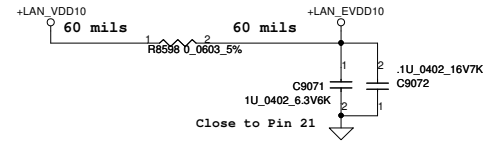
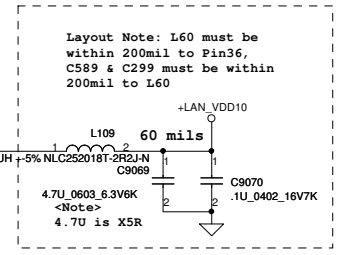
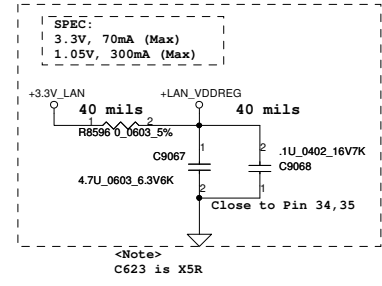
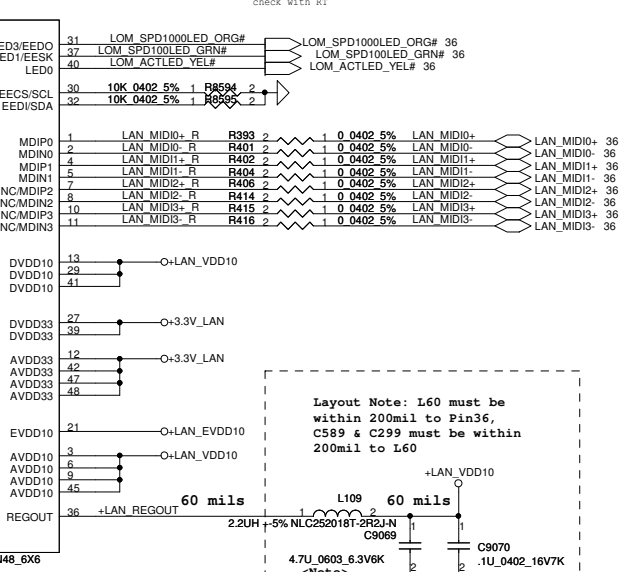
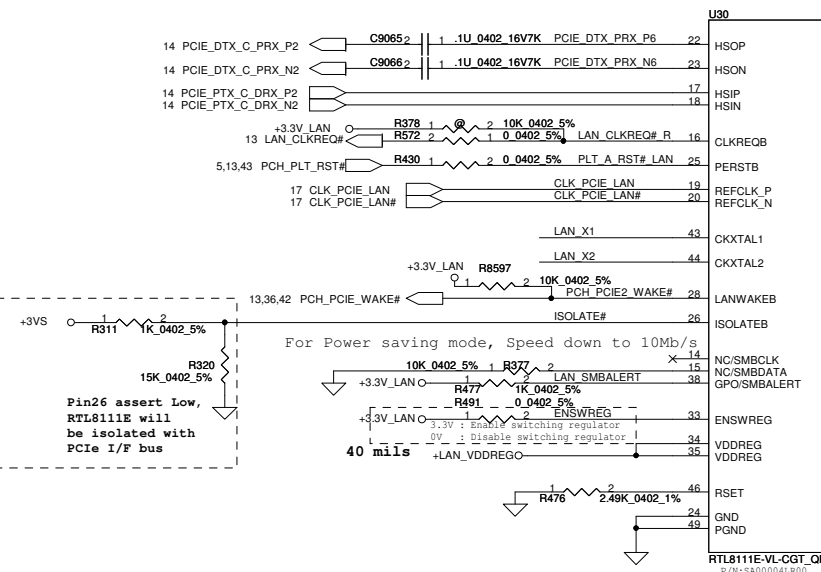


Power (Decoupling Cap.)

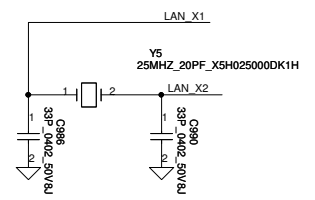


C625, C610, C617, C626, C621, C604 close to Pin 12,27,39,42,47,48, respectively

C615, C614, C622, C620, C616, C611, C624 close to pin 3,6,9,13,29,41,45, respectively



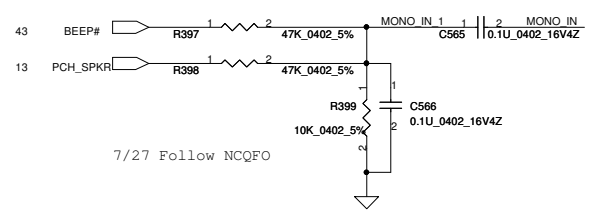
Crystal



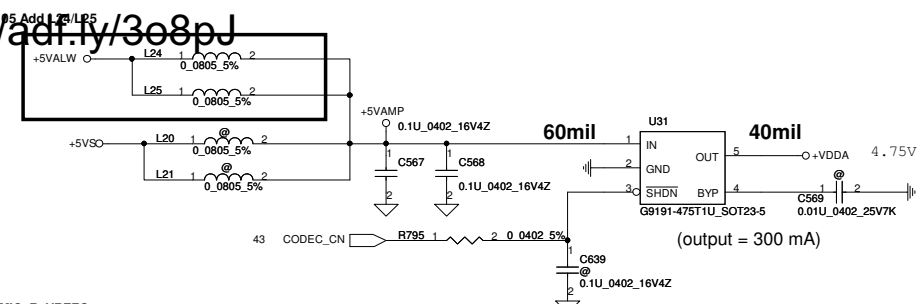
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Issued Date	2010/07/20	Deciphered Date	2011/07/20
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Intel LAN-82579			
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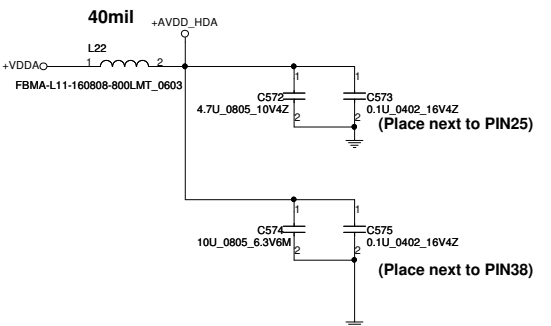
<http://ad.ly/3o8pJ>



7/27 Follow NCQFO

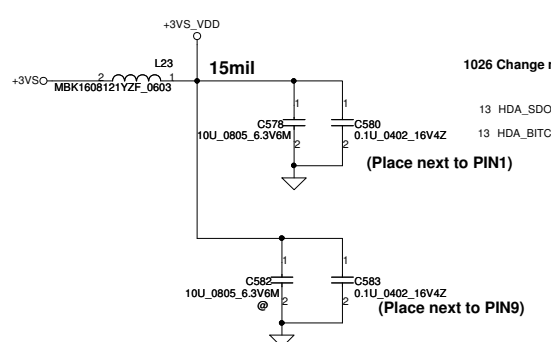


(output = 300 mA)



(Place next to PIN25)

(Place next to PIN38)

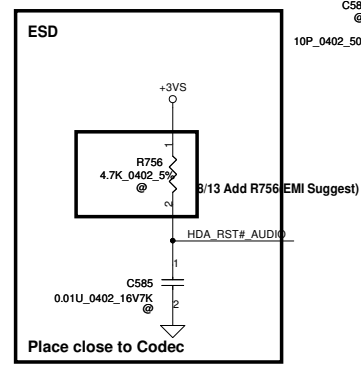


(Place next to PIN1)

(Place next to PIN9)

1026 Change mute_codec to GPIO1

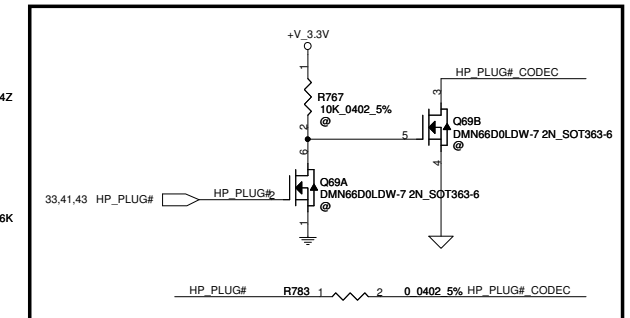
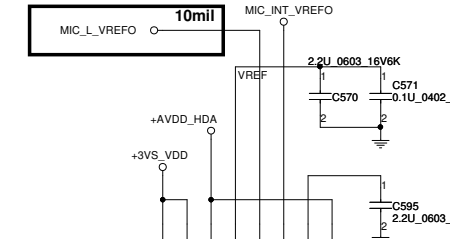
1026 Add digital-MIC for reserve



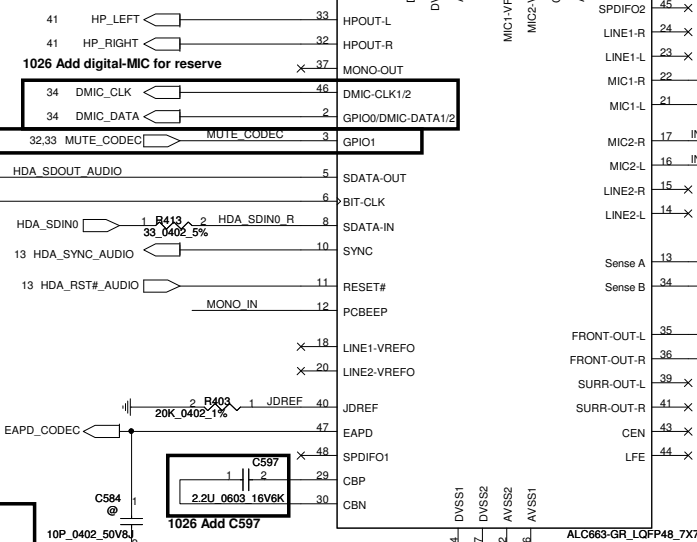
ESD

Place close to Codec

1026 DEL MIC_R_VREF0

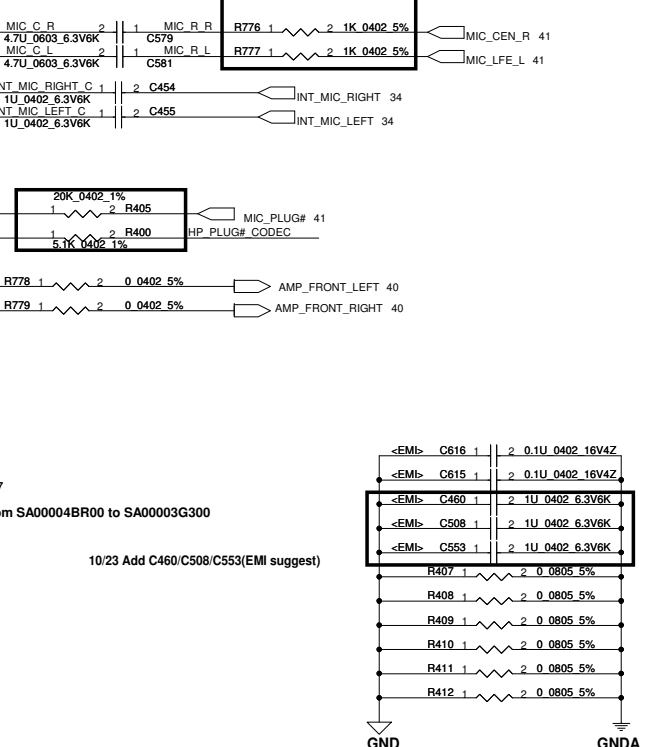


0810 vendor suggest



1026 Change U32 from SA00004BR00 to SA00003G300

10/23 Add C460/C508/C553(EMI suggest)

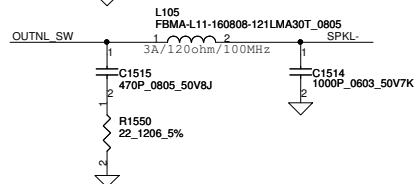
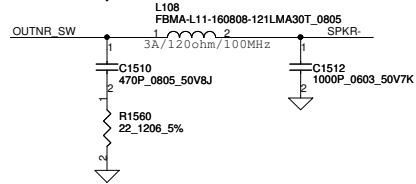
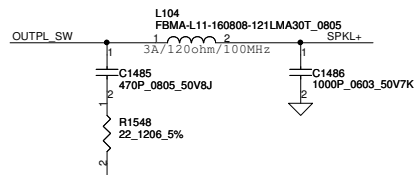
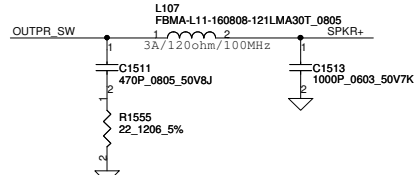
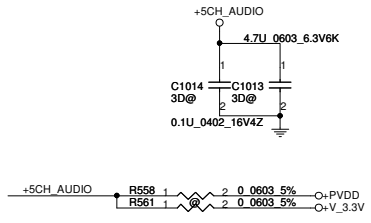
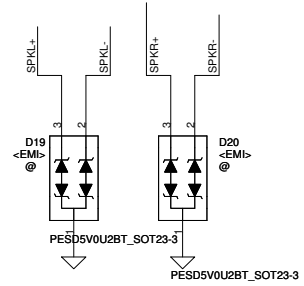
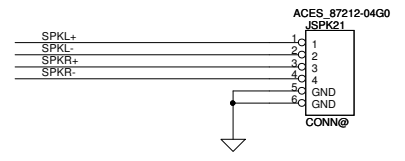
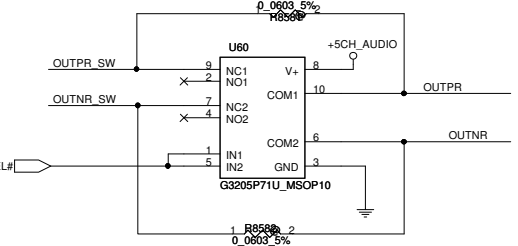
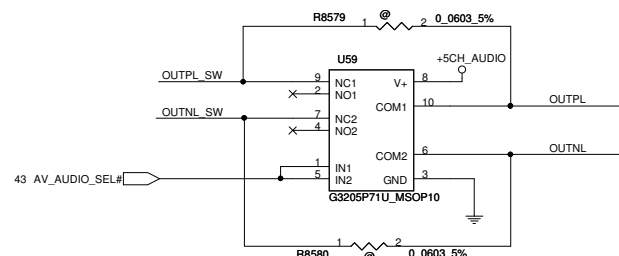
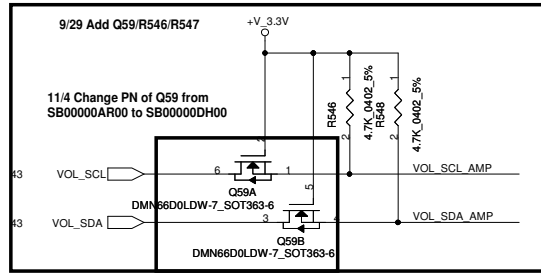
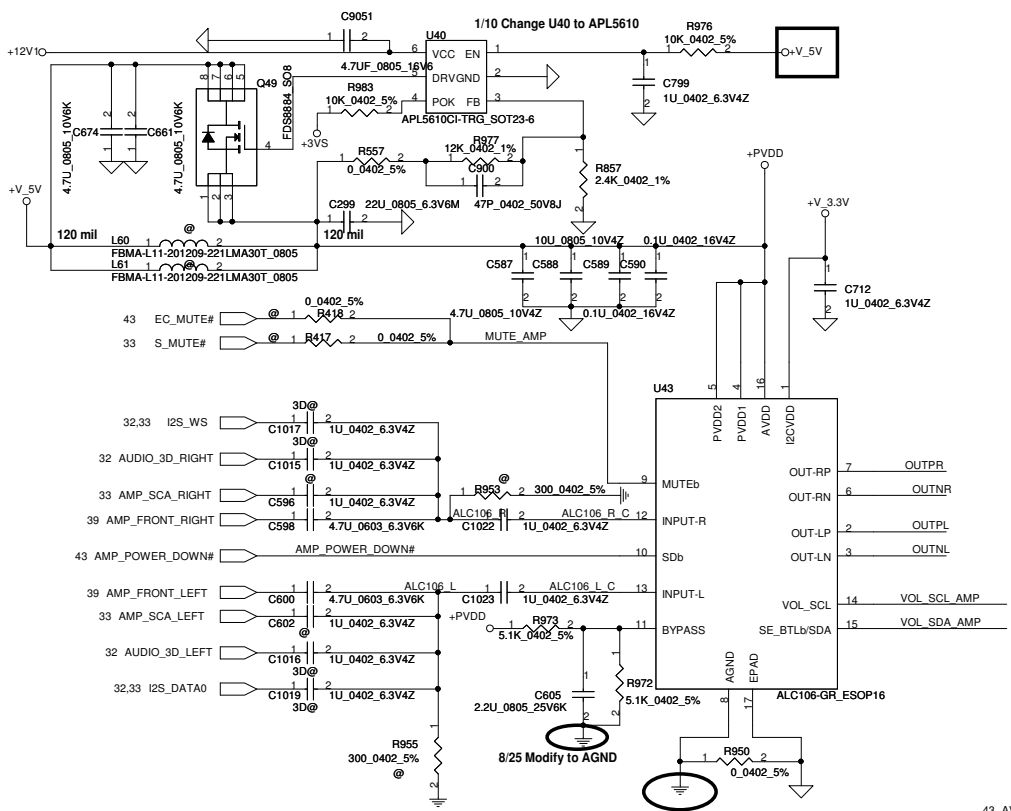


Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

Security Classification	Compal Secret Data	
Issued Date	2010/07/20	Deciphered Date
		2011/07/20

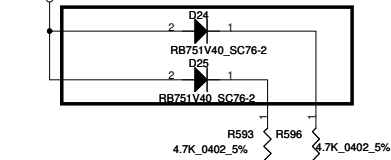
Compal Electronics, Inc.		
HD Audio Codec ALC663		
Size B	Document Number	Rev
	QLA01 M/B LA-7811P Schematic	1.A

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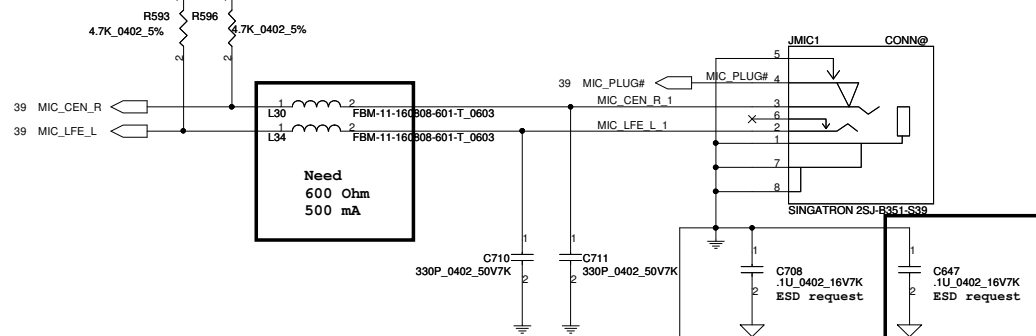


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Issued Date	2010/07/20	Deciphered Date	2011/07/20	AMP	
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			Custort	QLA01 M/B LA-7811P Schematic	A
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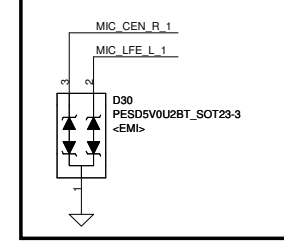
1026 Add Diode for MIC L VREFO
12/10 Change symbol of D24/D25 from SC1H751H010 to SCS00002G00



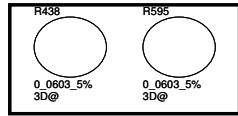
EXT MIC IN



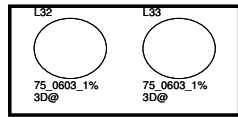
8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)



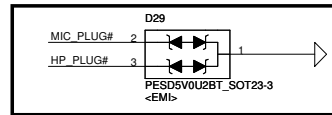
2/18 Add



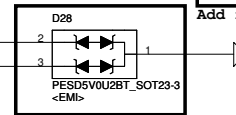
2/24 Add



8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)

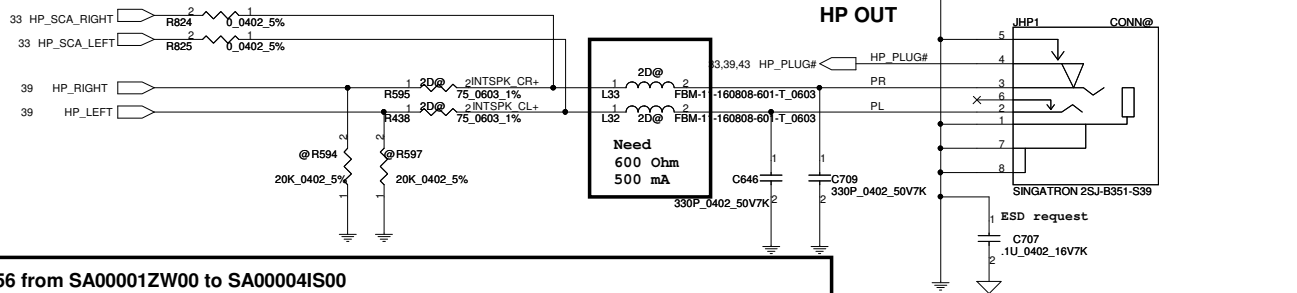


Add for EMC suggest

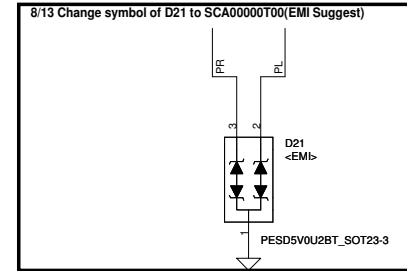


8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)

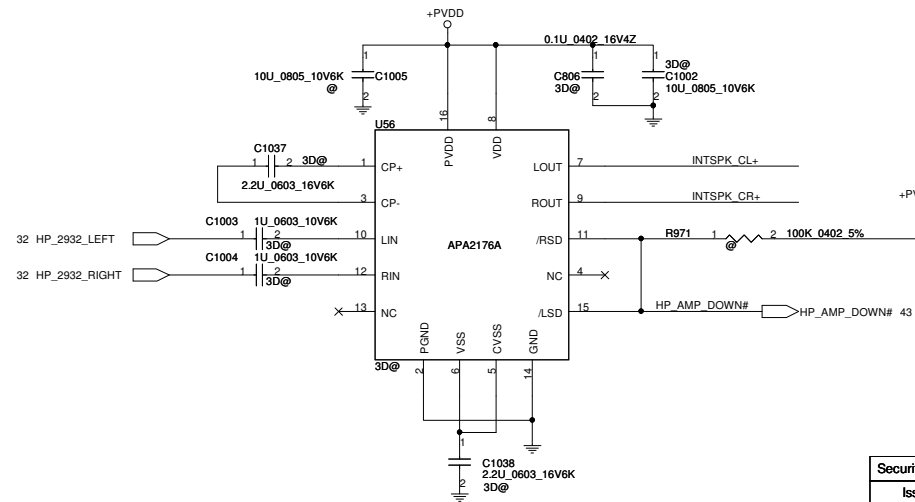
HP OUT



8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)



10/22 Change U56 from SA00001ZW00 to SA00004IS00



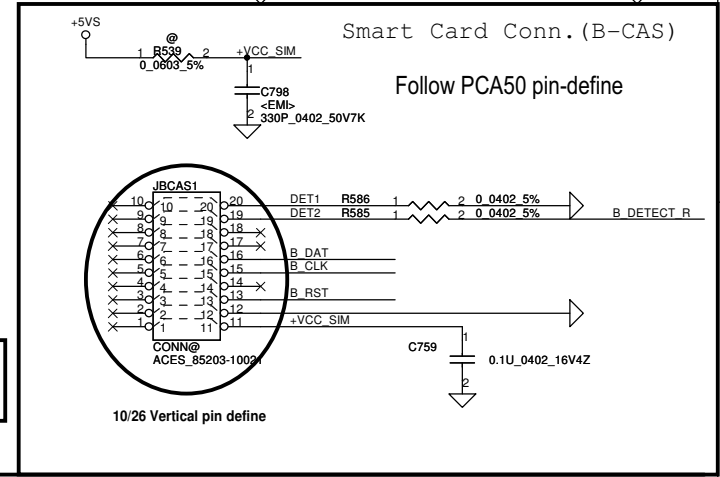
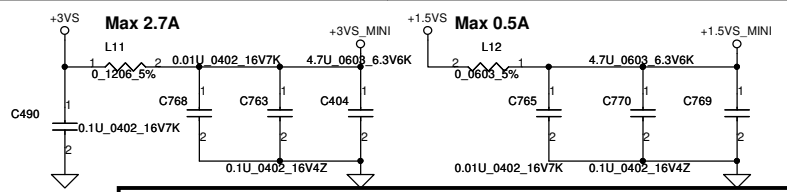
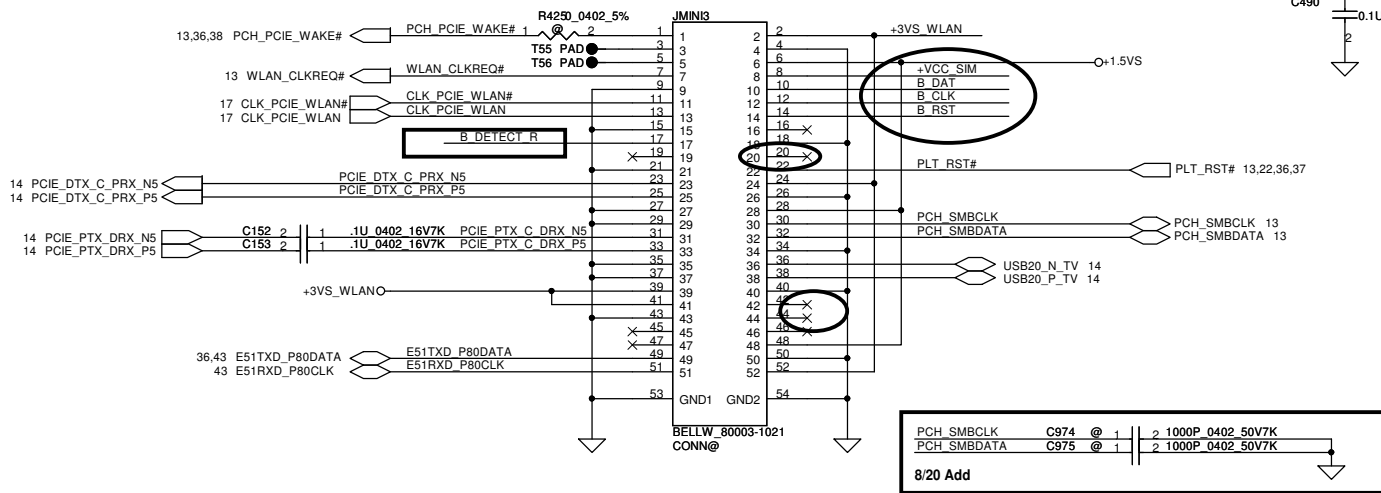
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Audio Jack	
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MINI (TV)

Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA

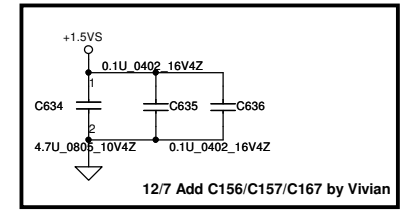
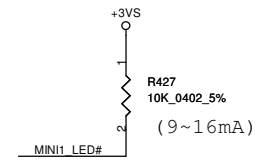
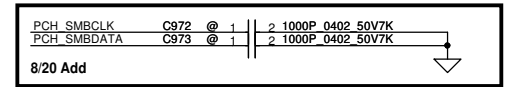
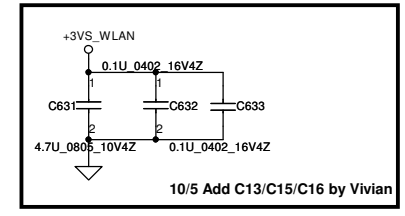
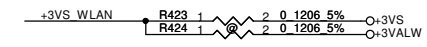
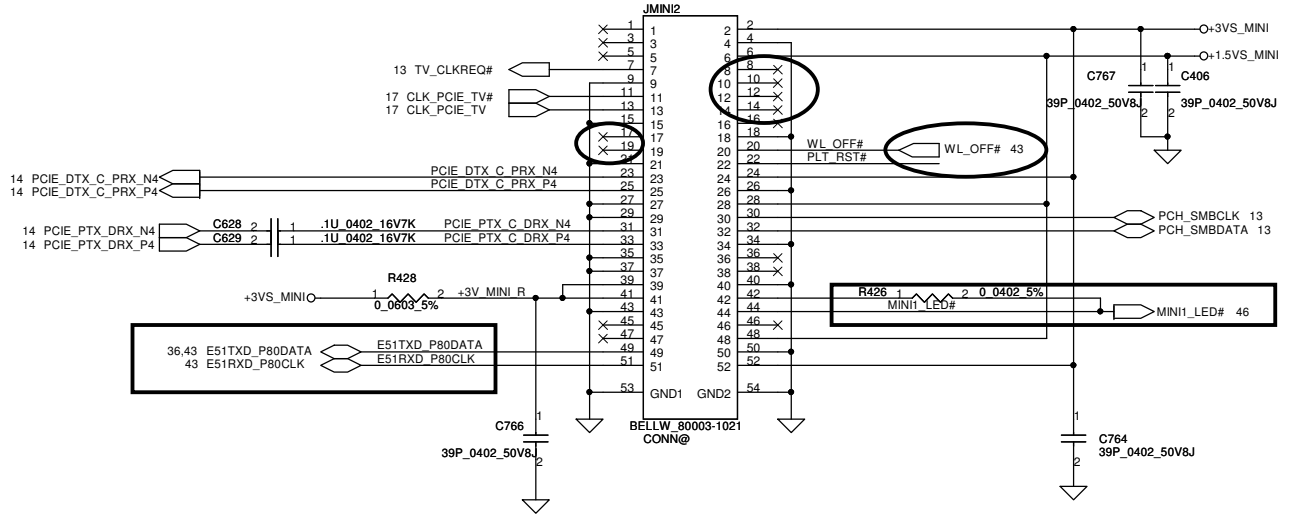
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H=9mm

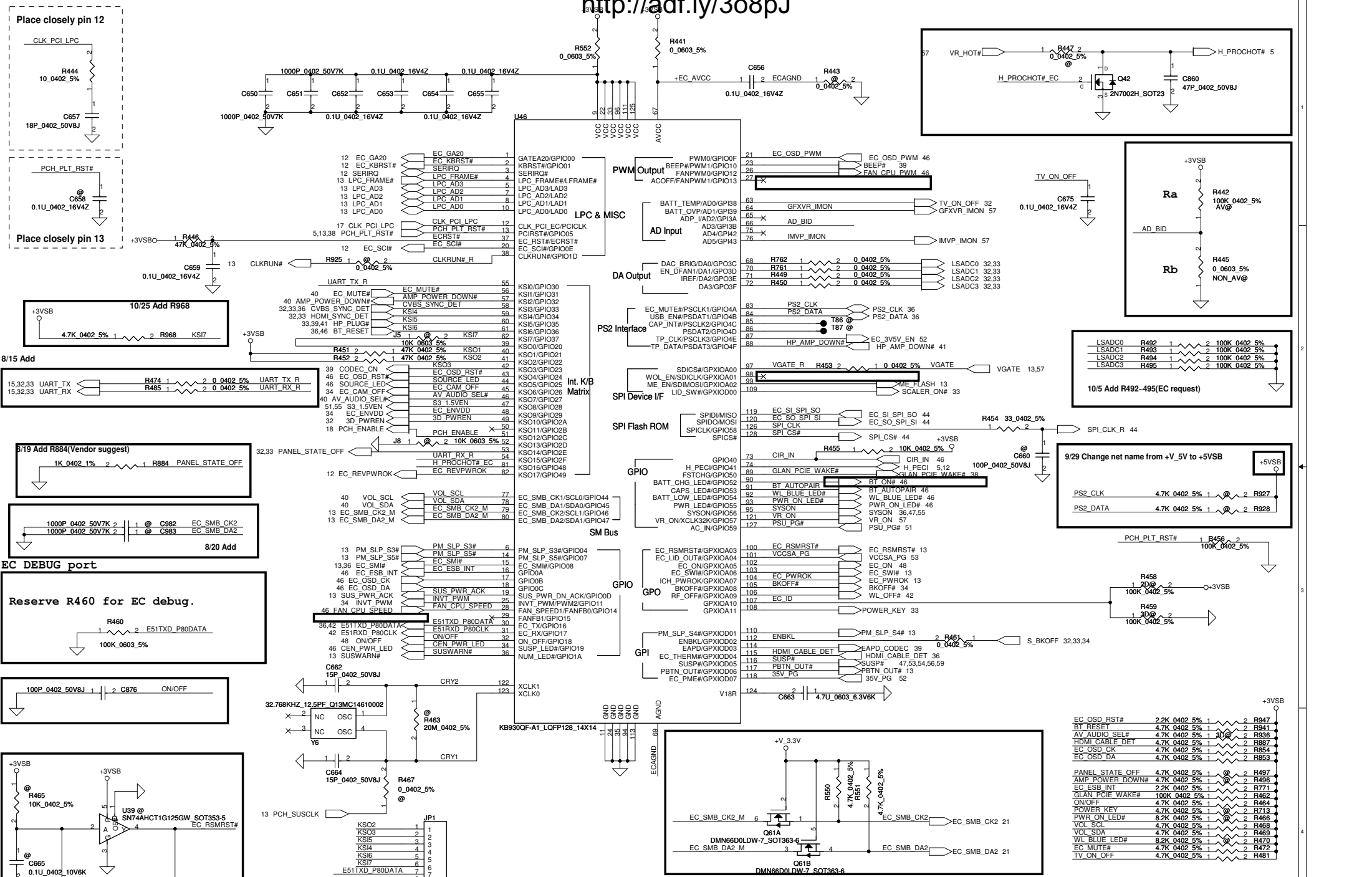


WLAN

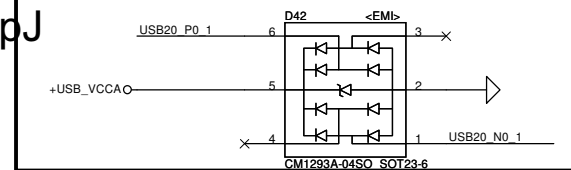
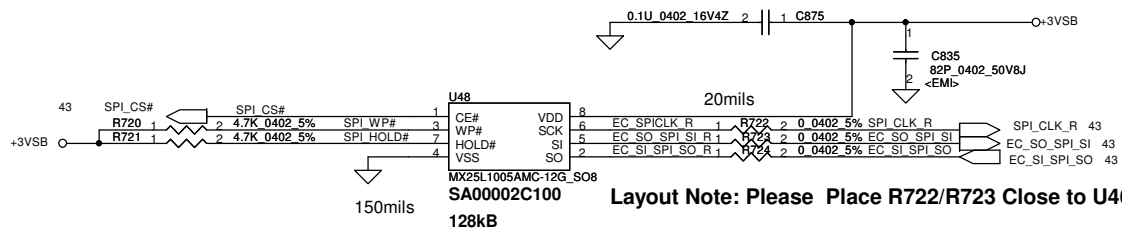
H=4mm



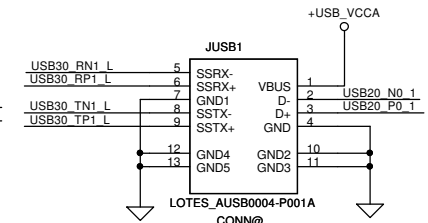
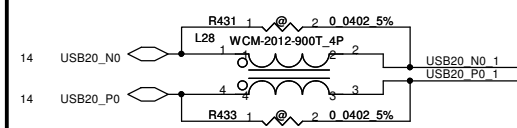
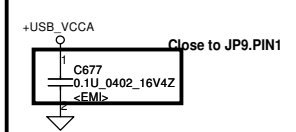
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size Custom	Document Number	Rev		1.A	
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				QLA01 M/B LA-7811P Schematic	



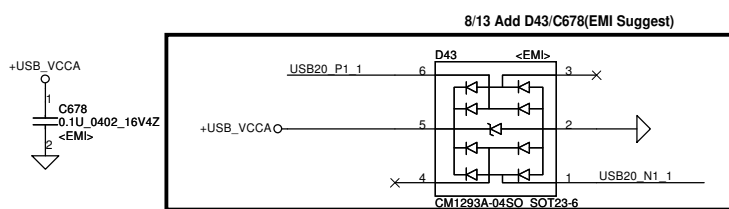
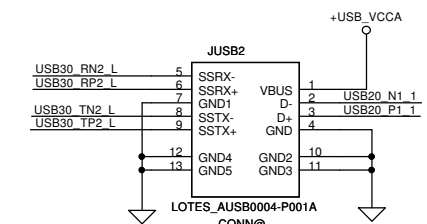
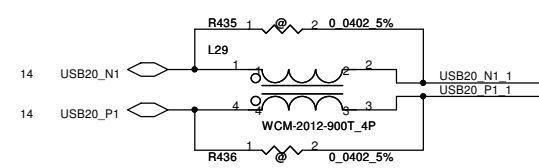
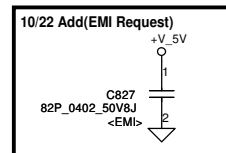
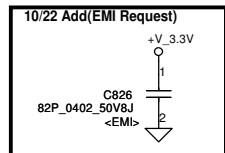
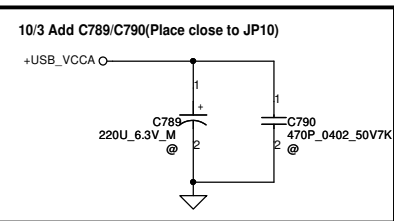
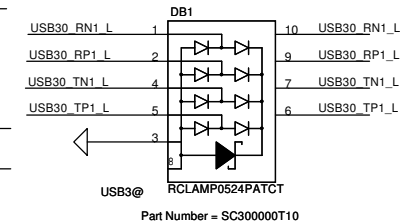
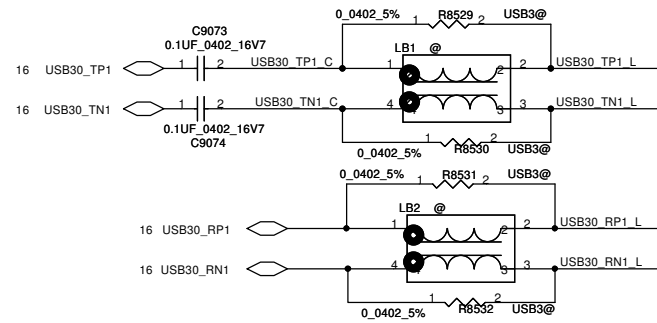
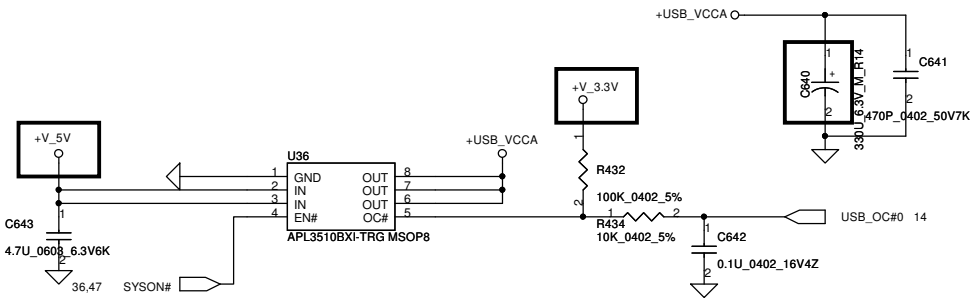
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Custort	QLA01 M/B LA-7811P Schematic			



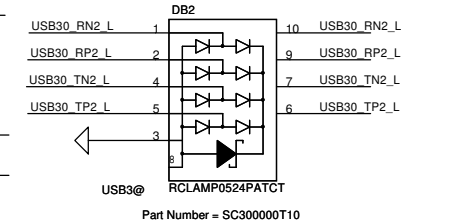
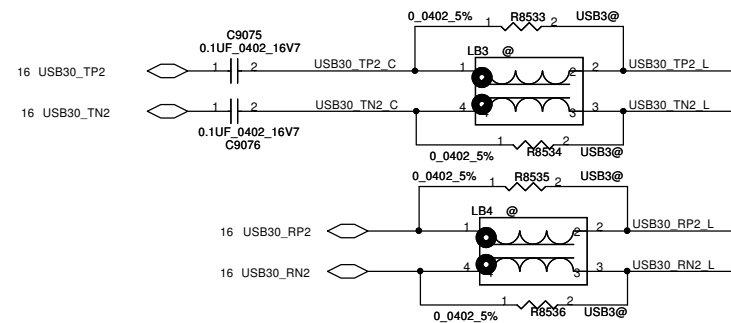
10/25 Change symbol and footprint of D42 from SC300000100 to SC300000000(ESD request)



11/2 Change PN of C640 from SF000002Y00 to SF000001G00

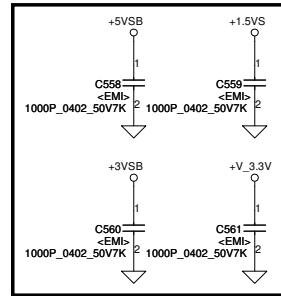


10/25 Change symbol and footprint of D43 from SC300000100 to SC300000000(ESD request)



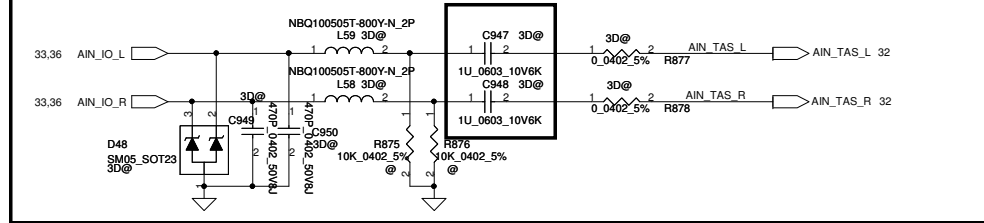
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size	Document Number	Rev		1.A	
Custom	QLA01 M/B LA-7811P Schematic	Date:		Thursday, June 16, 2011	
Date:		Sheet		44 of 63	

10/27 Add C558-C561(EMI request)



0818 Vendor suggest(Close to U42.Pin43/Pin44)

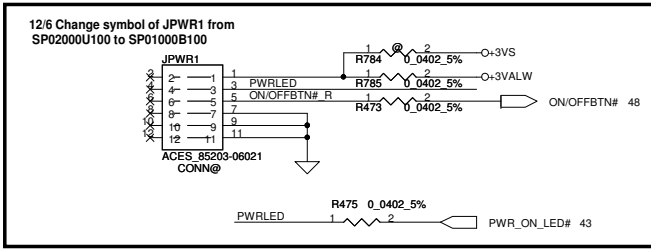
12/6 Change C947/C948 from 4.7uF to 1uF



De-Emphasis Control

DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

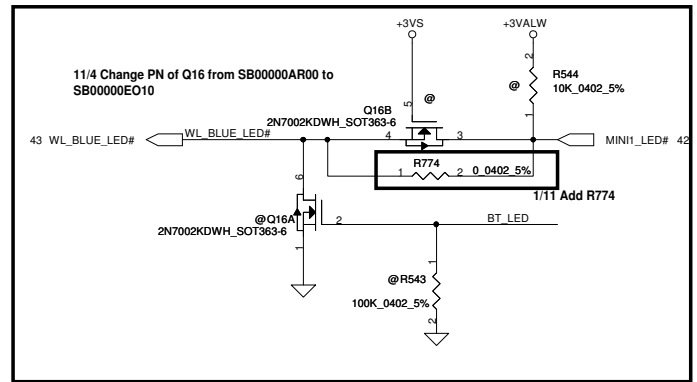
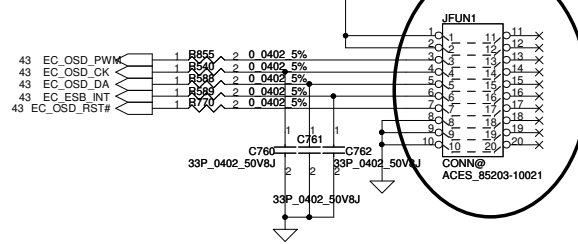
Power switch board



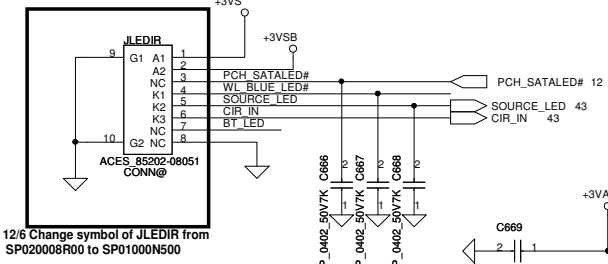
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SENSOR BOTTOM

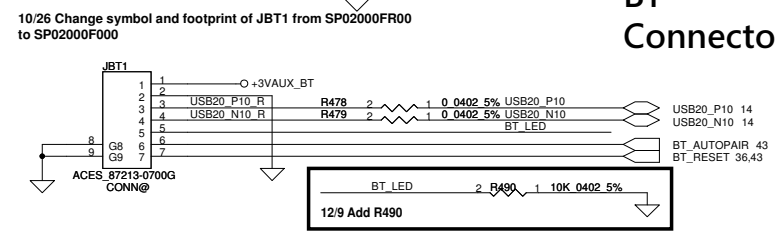
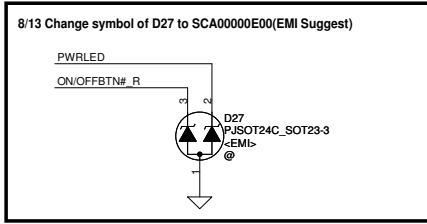
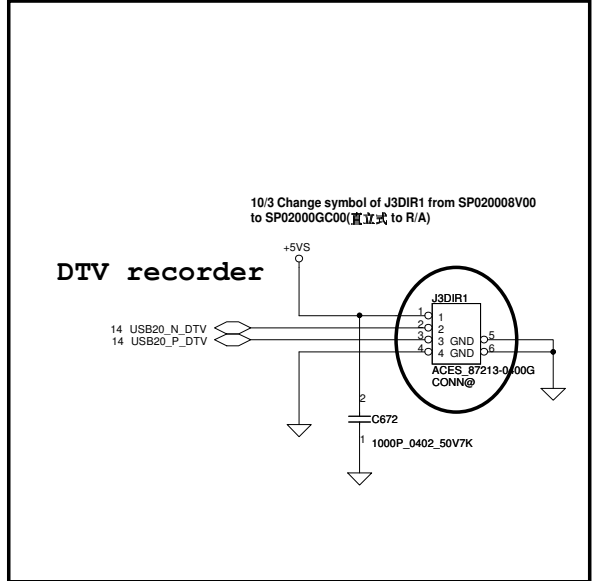
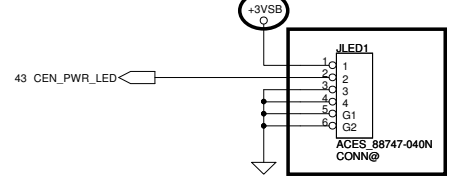
Follow NCQD0



LED board conn.

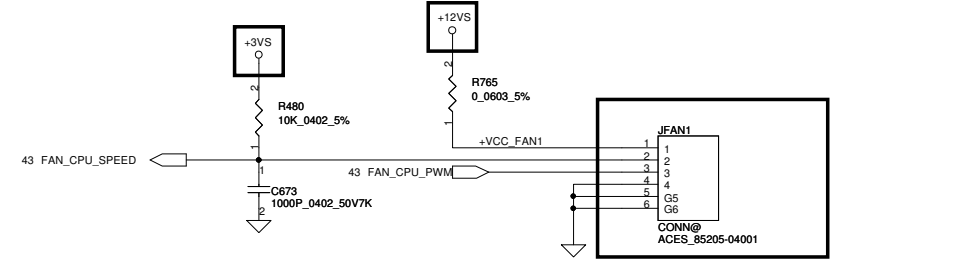


DECO LED board conn.



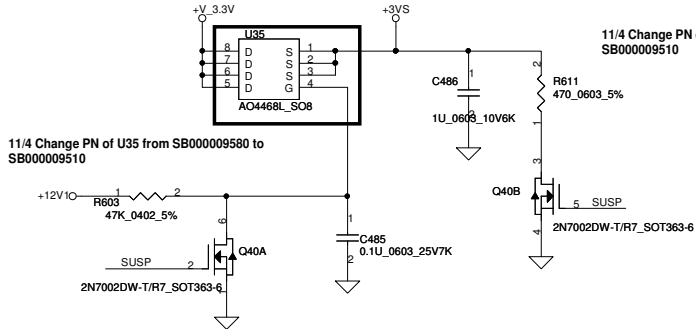
BT Connector

Fan Control circuit

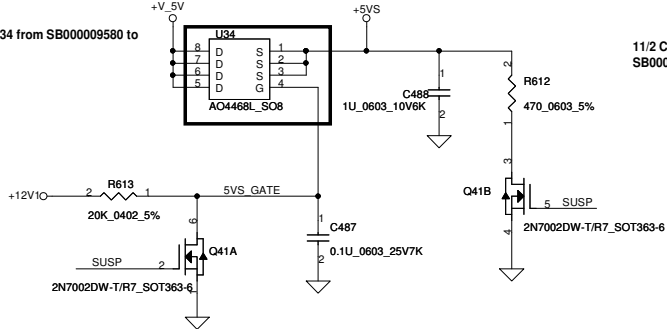


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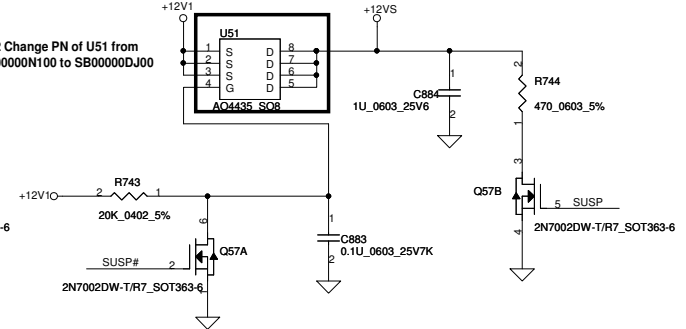
+V_3.3V TO +3VS



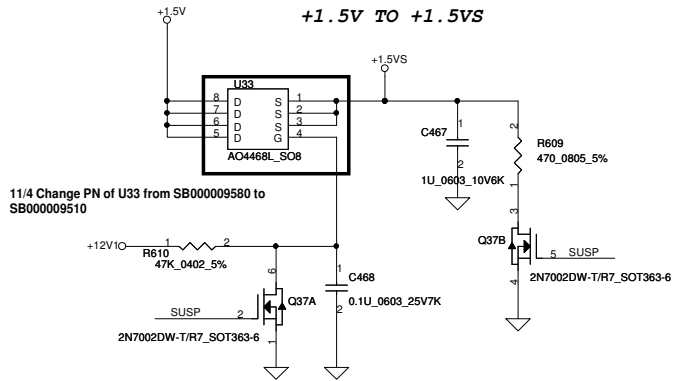
+V_5V TO +5VS



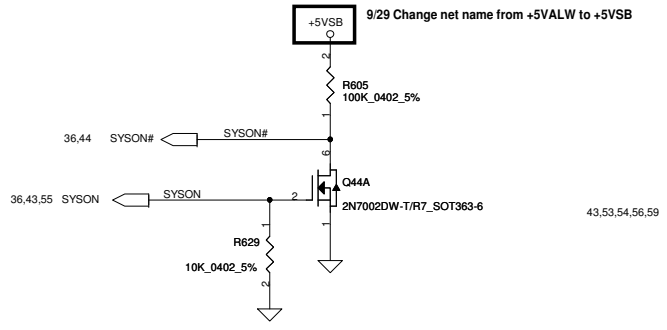
+12V1 TO +12VS



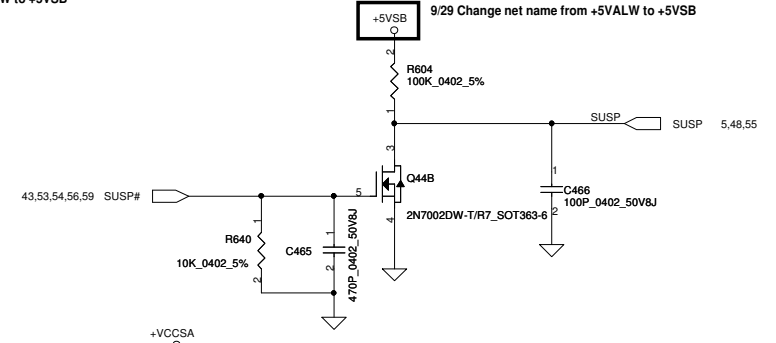
+1.5V TO +1.5VS



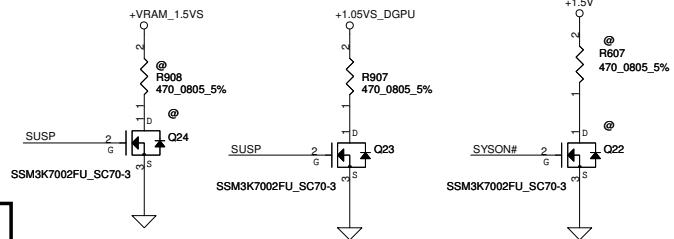
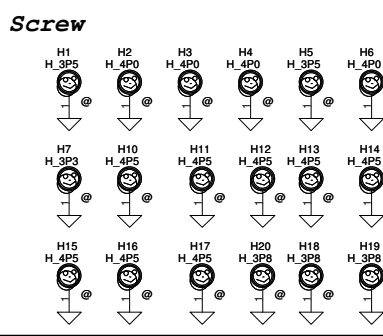
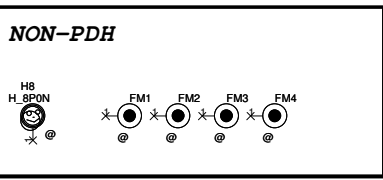
+5VSB 9/29 Change net name from +5VALW to +5VSB



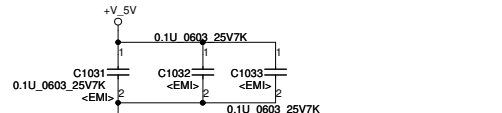
+5VSB 9/29 Change net name from +5VALW to +5VSB



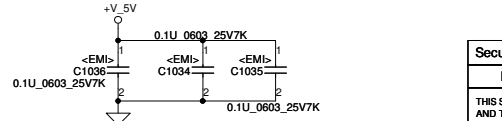
Discharge circuit



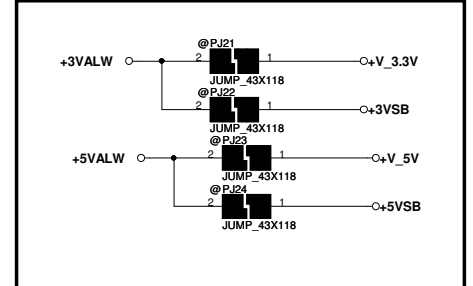
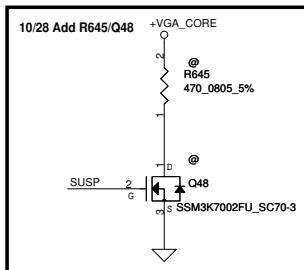
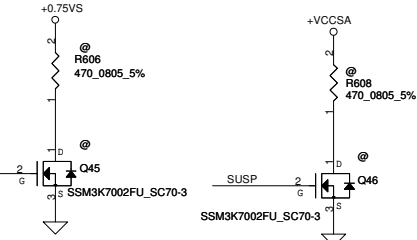
8/24 Add C1031-C1036



8/24 Place C1031/C1032/C1033 close to H4/H5/H7(EMI request)

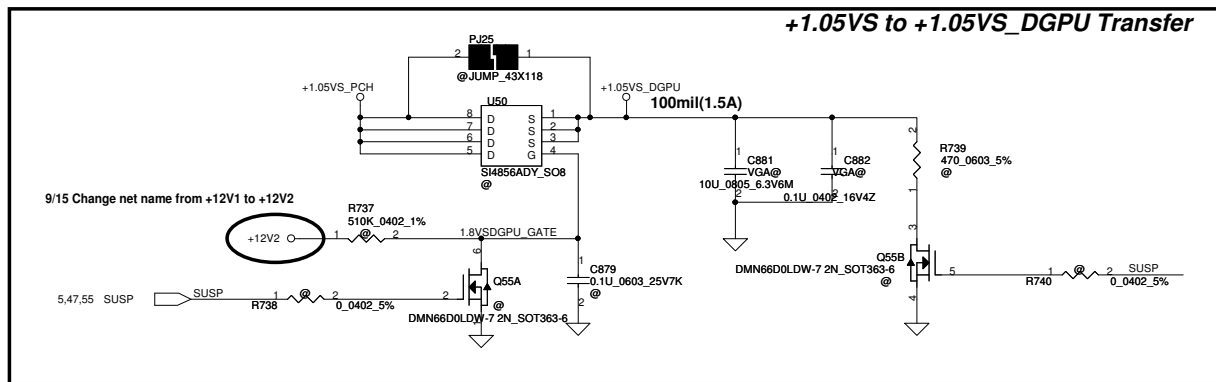
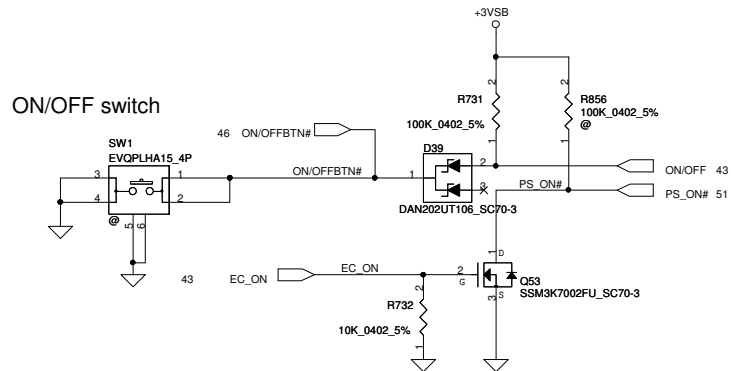


8/24 Place C1034/C1035/C1036 close to H1/H2/H6(EMI request)



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				DC Interface/Screw	
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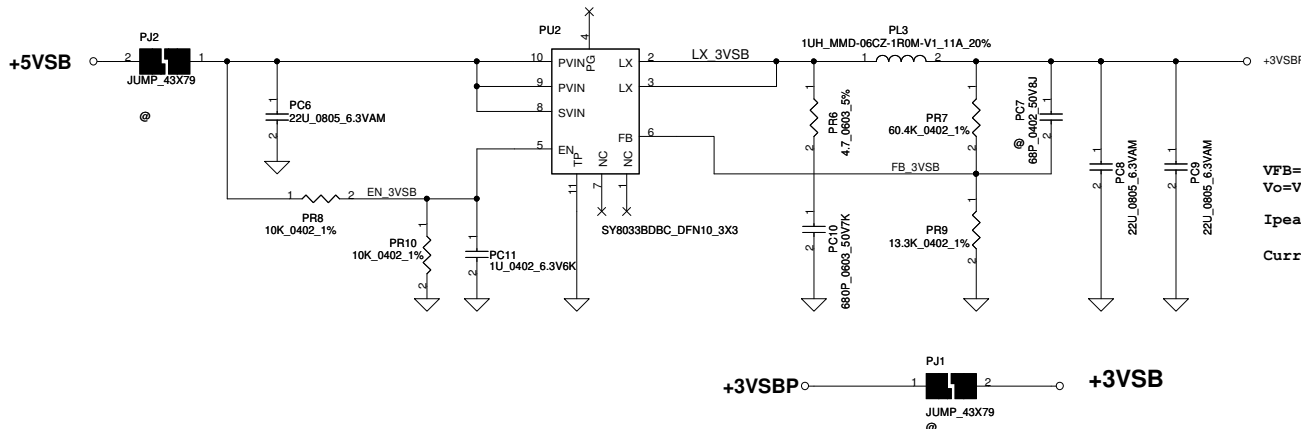
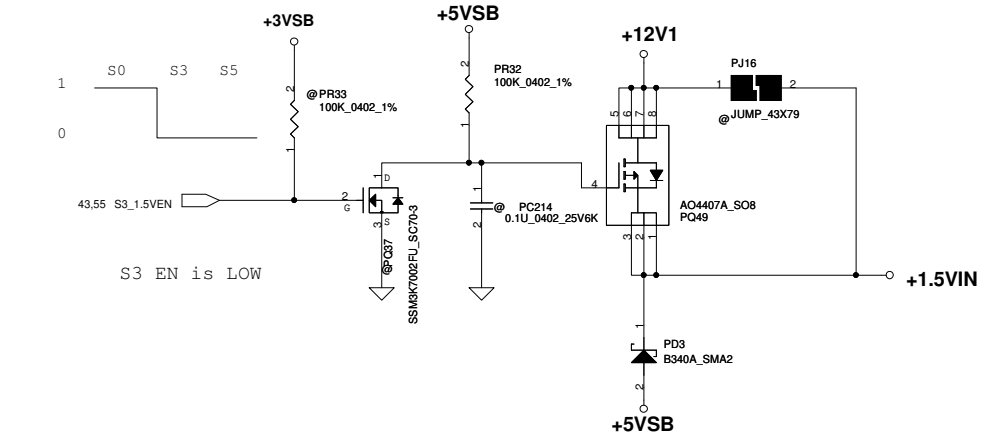
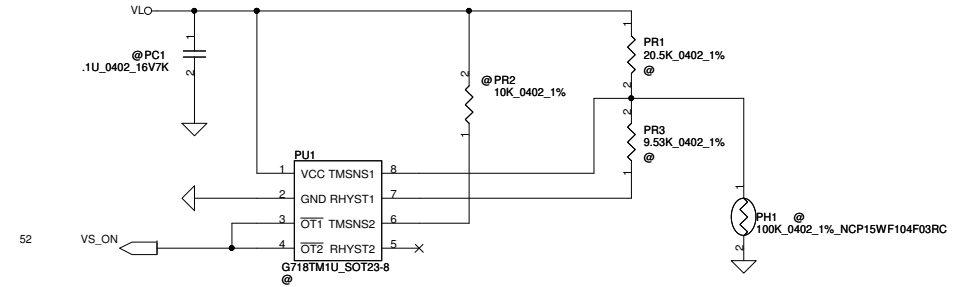
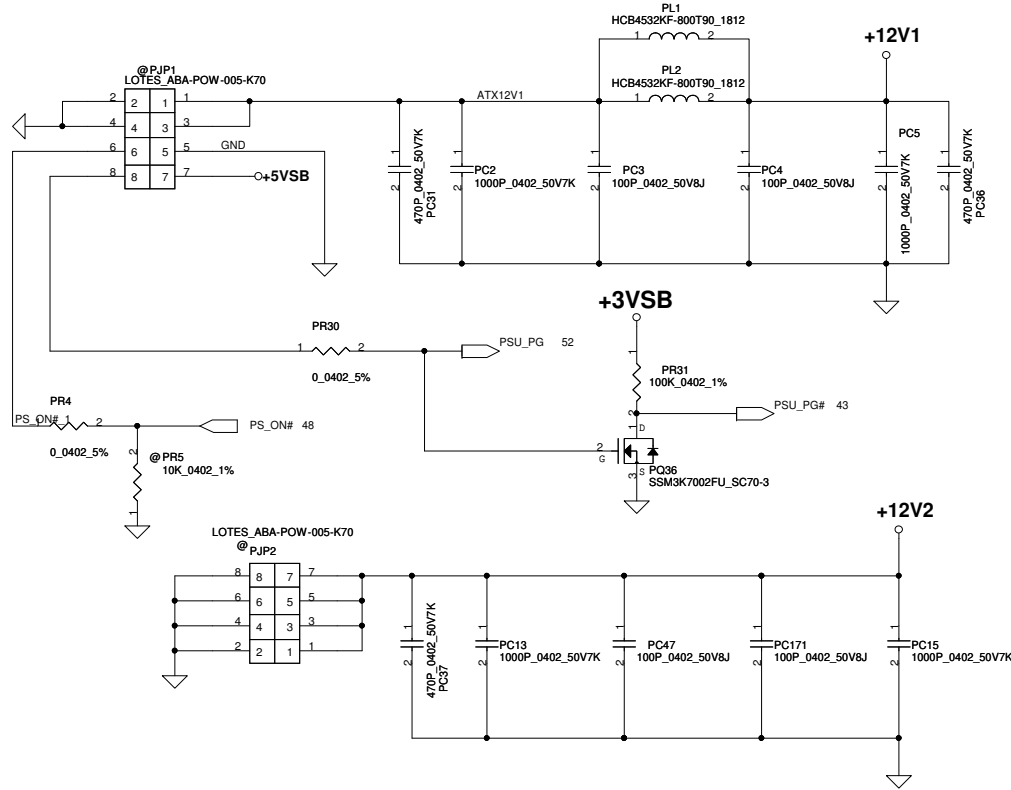
Power Button



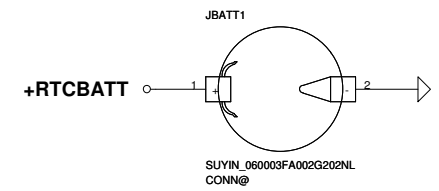
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PH1 under CPU botten side :

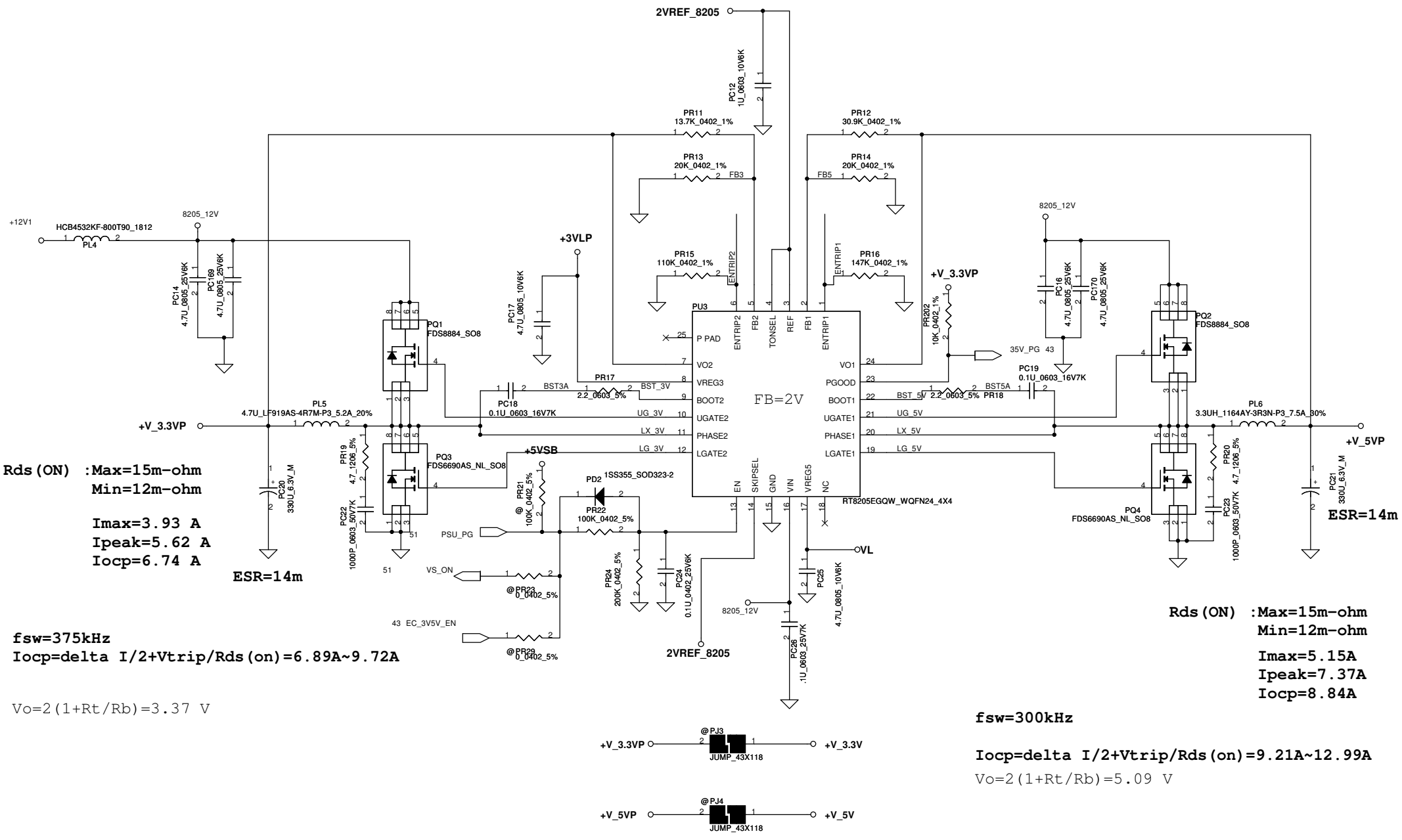
CPU thermal protection at 92 degree C
Recovery at 57 degree C



FOR EC suspend
 $V_{FB}=0.6V$
 $V_o=V_{FB} \cdot (1+PR7/PR9)=3.318V$
 $I_{peak}=0.062A, I_{max}=0.045A$
 Current limit $\geq 4A$



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**Rds (ON) : Max=15m-ohm
Min=12m-ohm**

**I_{max}=3.93 A
I_{peak}=5.62 A
I_{ocp}=6.74 A**

ESR=14m

f_{sw}=375kHz

I_{ocp}=delta I/2+V_{trip}/Rds (on)=6.89A~9.72A

$V_o = 2(1 + R_t/R_b) = 3.37 V$

**Rds (ON) : Max=15m-ohm
Min=12m-ohm**

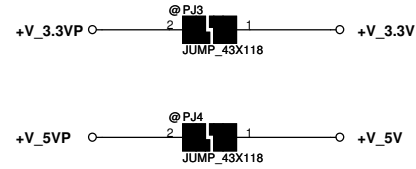
**I_{max}=5.15A
I_{peak}=7.37A
I_{ocp}=8.84A**

ESR=14m

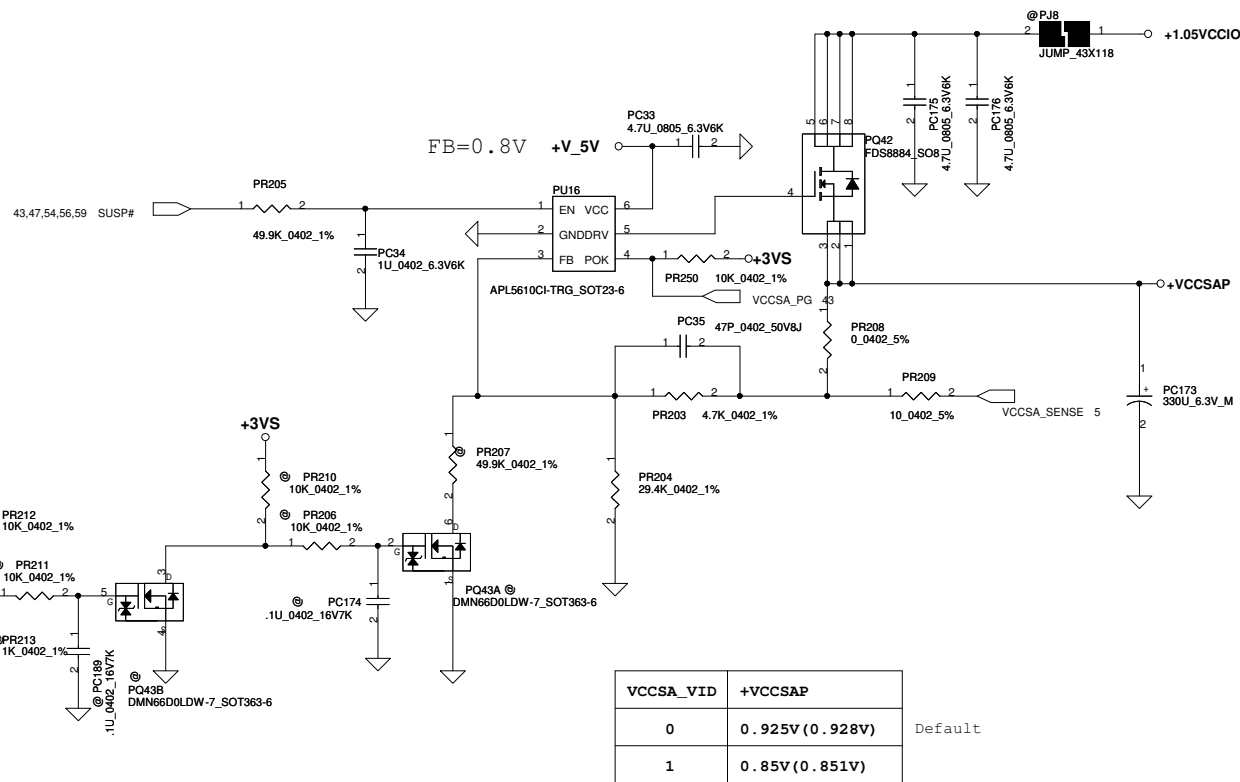
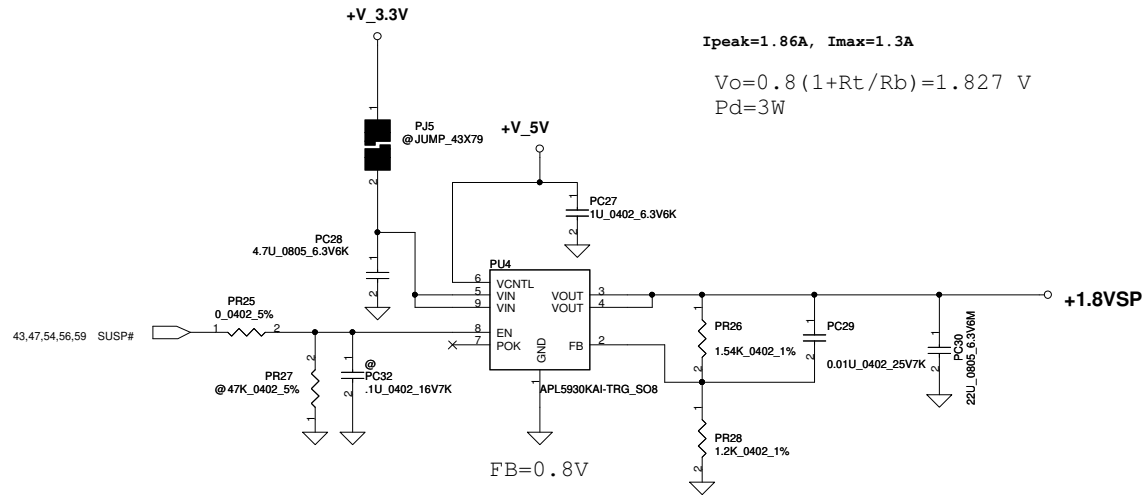
f_{sw}=300kHz

I_{ocp}=delta I/2+V_{trip}/Rds (on)=9.21A~12.99A

$V_o = 2(1 + R_t/R_b) = 5.09 V$

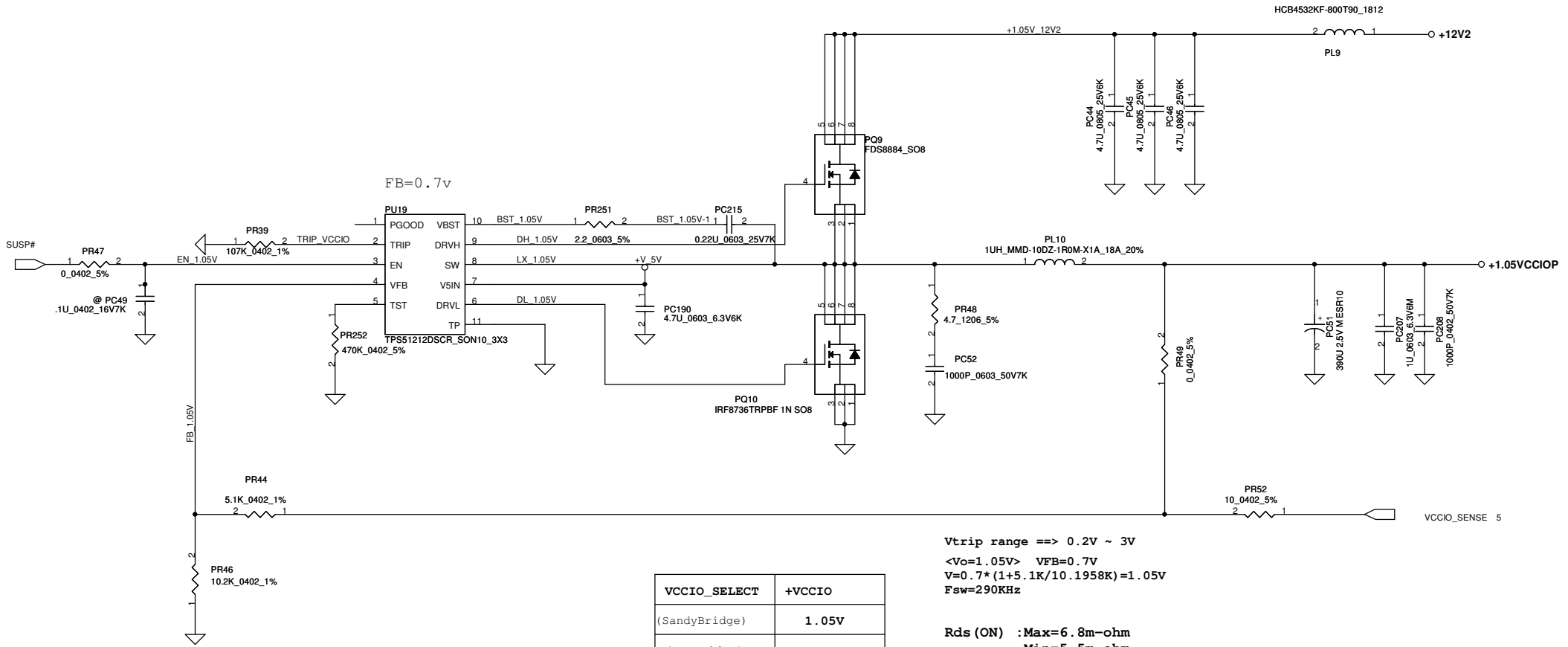


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$I_{max}=6.2A$
 $I_{peak}=8.8A$
 $ESR=14\text{ mohm}$
 $V_o=0.8(1+R_t/R_b)=0.928V$
 $P_d=2.5W$



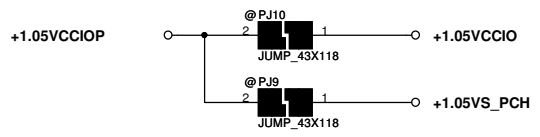


VCCIO_SELECT	+VCCIO
(SandyBridge)	1.05V
(IvyBridge)	1.05V

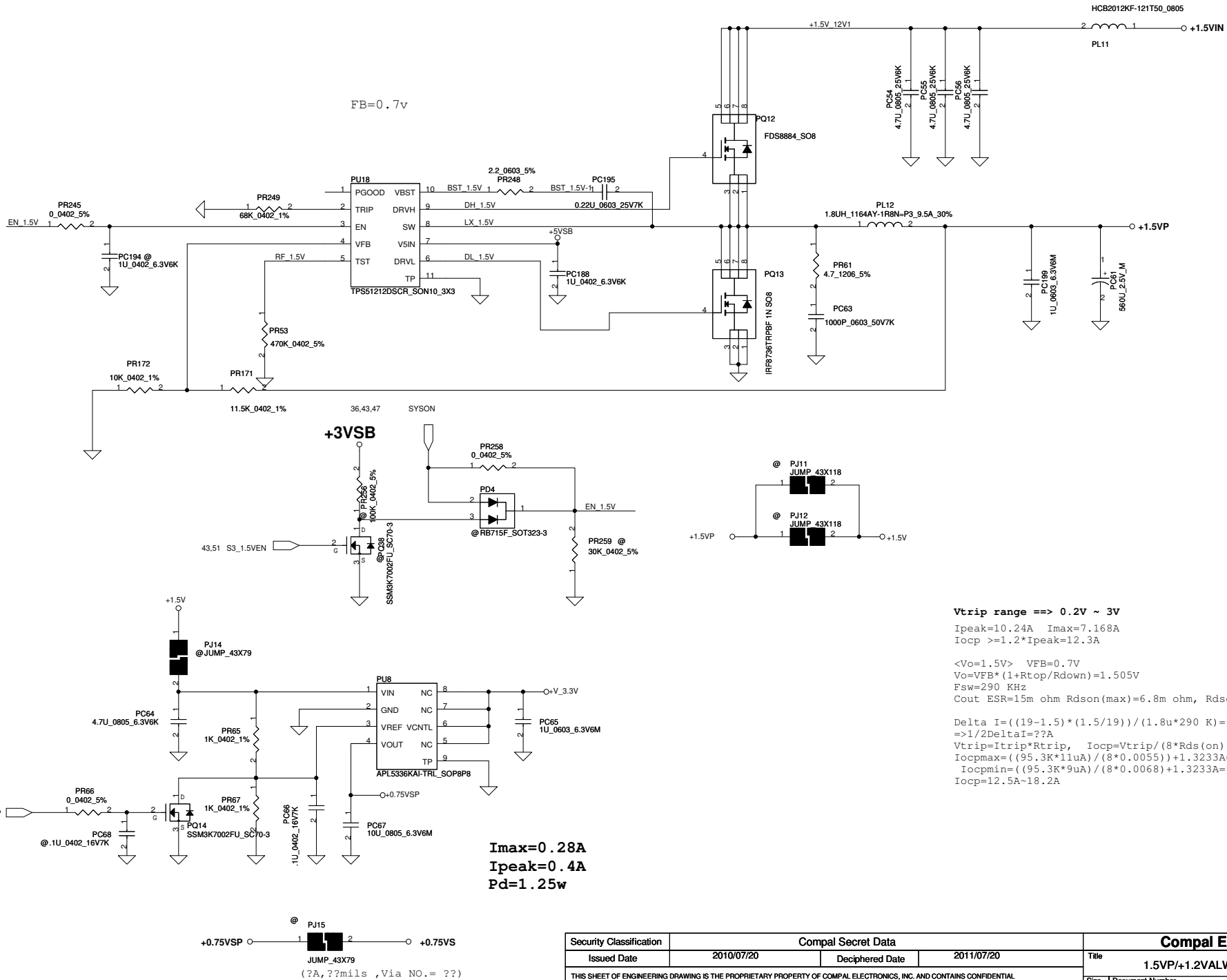
Vtrip range ==> 0.2V ~ 3V
 <Vo=1.05V> VFB=0.7V
 $V=0.7 * (1+5.1K/10.1958K)=1.05V$
 Fsw=290KHz

Rds (ON) :Max=6.8m-ohm
 Min=5.5m-ohm
 Imax=11.17 A
 Ipeak=15.96 A
 Iocp= 19.15A

1.05V, Iocp=delta I/2+Vtrip/Rds(on)=19.35A~28.4A



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				+1.05VSP	
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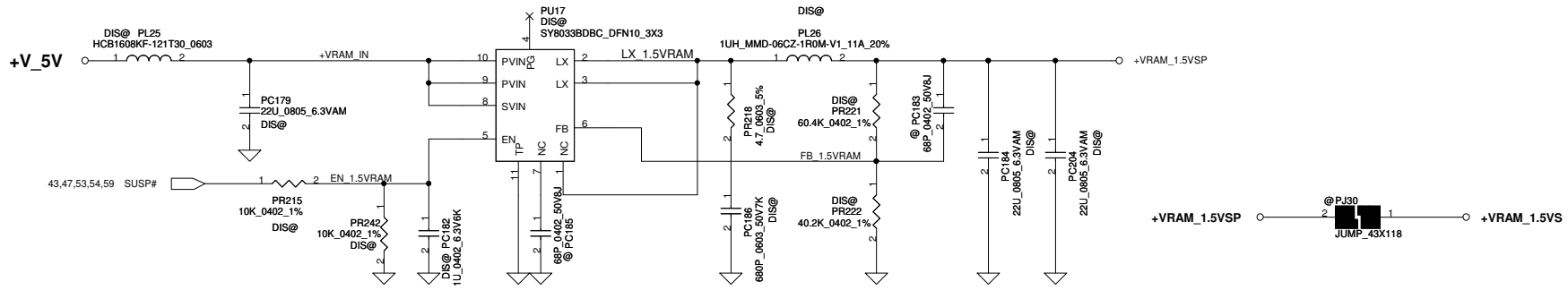
Vtrip range ==> 0.2V ~ 3V
 Ipeak=10.24A Imax=7.168A
 Iocp >=1.2*Ipeak=12.3A

<Vo=1.5V> VFB=0.7V
 Vo=VFB*(1+Rtop/Rdown)=1.505V
 Fsw=290 KHz
 Cout ESR=15m ohm Rds(on)=6.8m ohm, Rds(on)(typ)=5.5 mohm

Delta I=((19-1.5)*(1.5/19))/(1.8u*290 K)=?? A
 =>1/2DeltaI=??A
 Vtrip=Itrip*Rtrip, Iocp=Vtrip/(8*Rds(on))
 Iocpmax=(95.3k*11uA)/(8*0.0055)+1.3233A=??A
 Iocpmin=(95.3K*9uA)/(8*0.0068)+1.3233A=??A
 Iocp=12.5A~18.2A

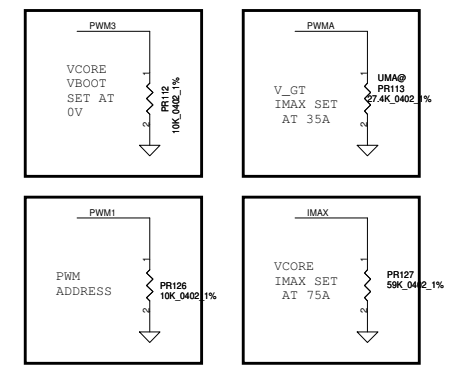
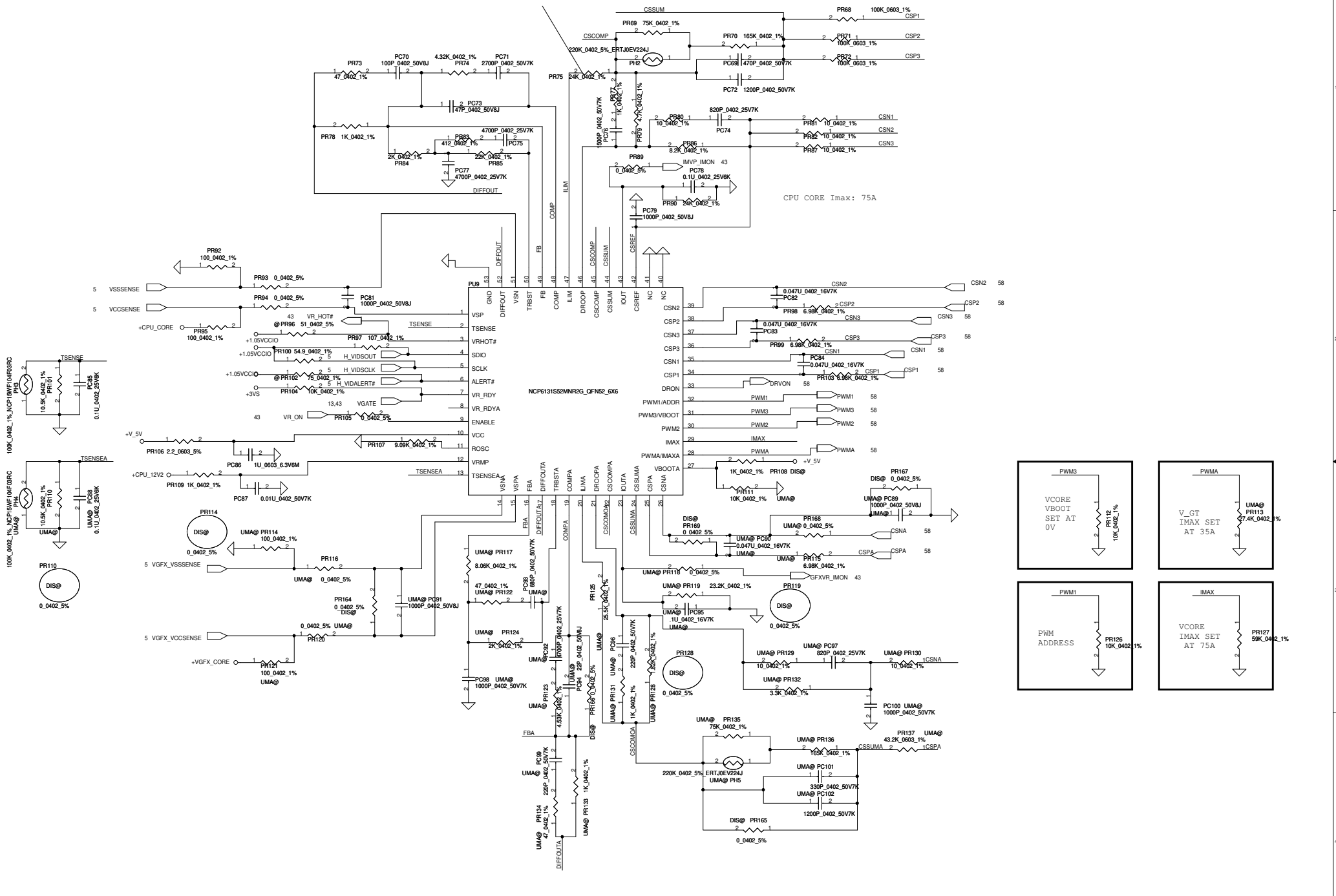
Imax=0.28A
Ipeak=0.4A
Pd=1.25w

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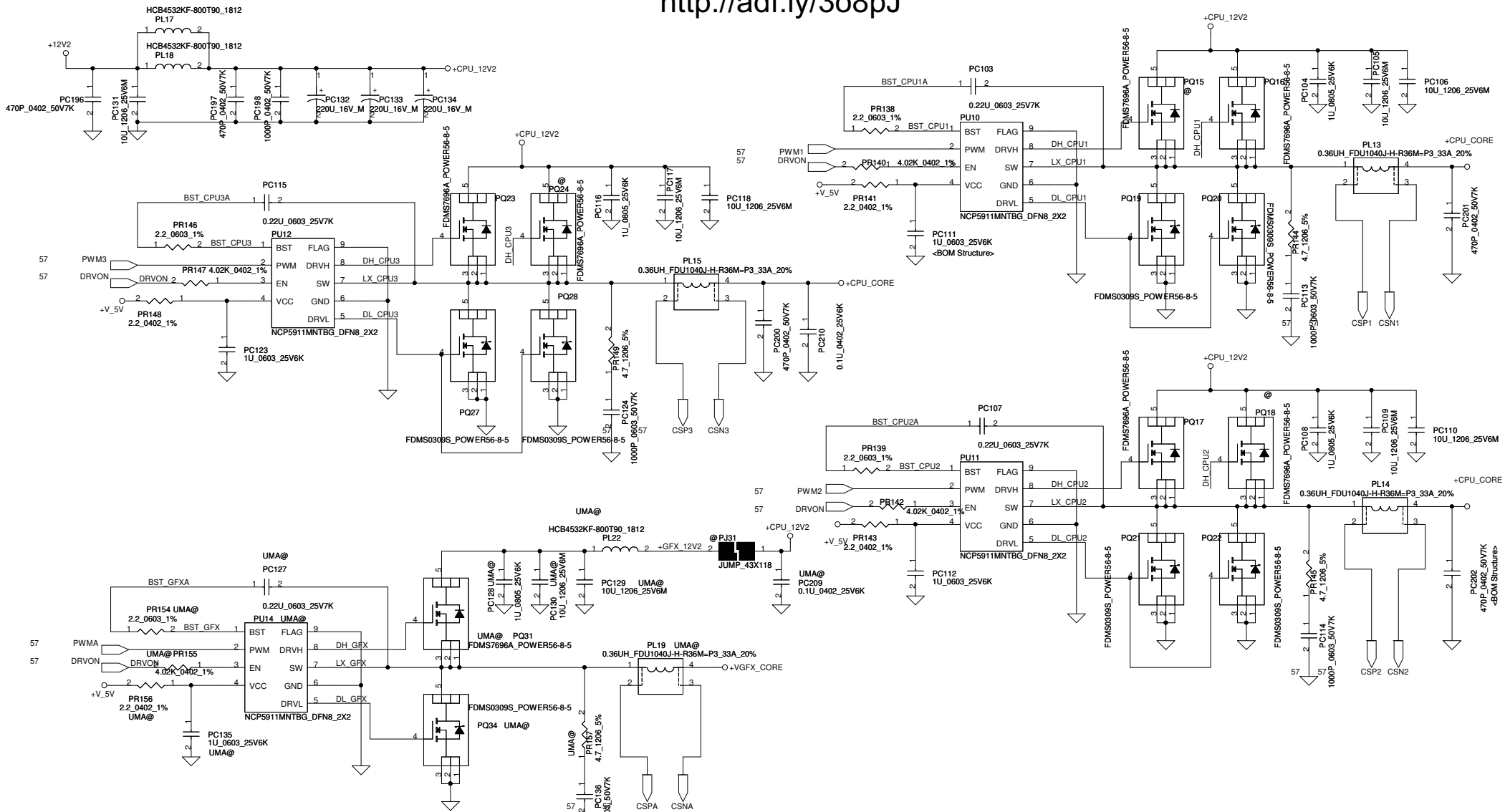


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CPU CORE OCP: 90A-----65W



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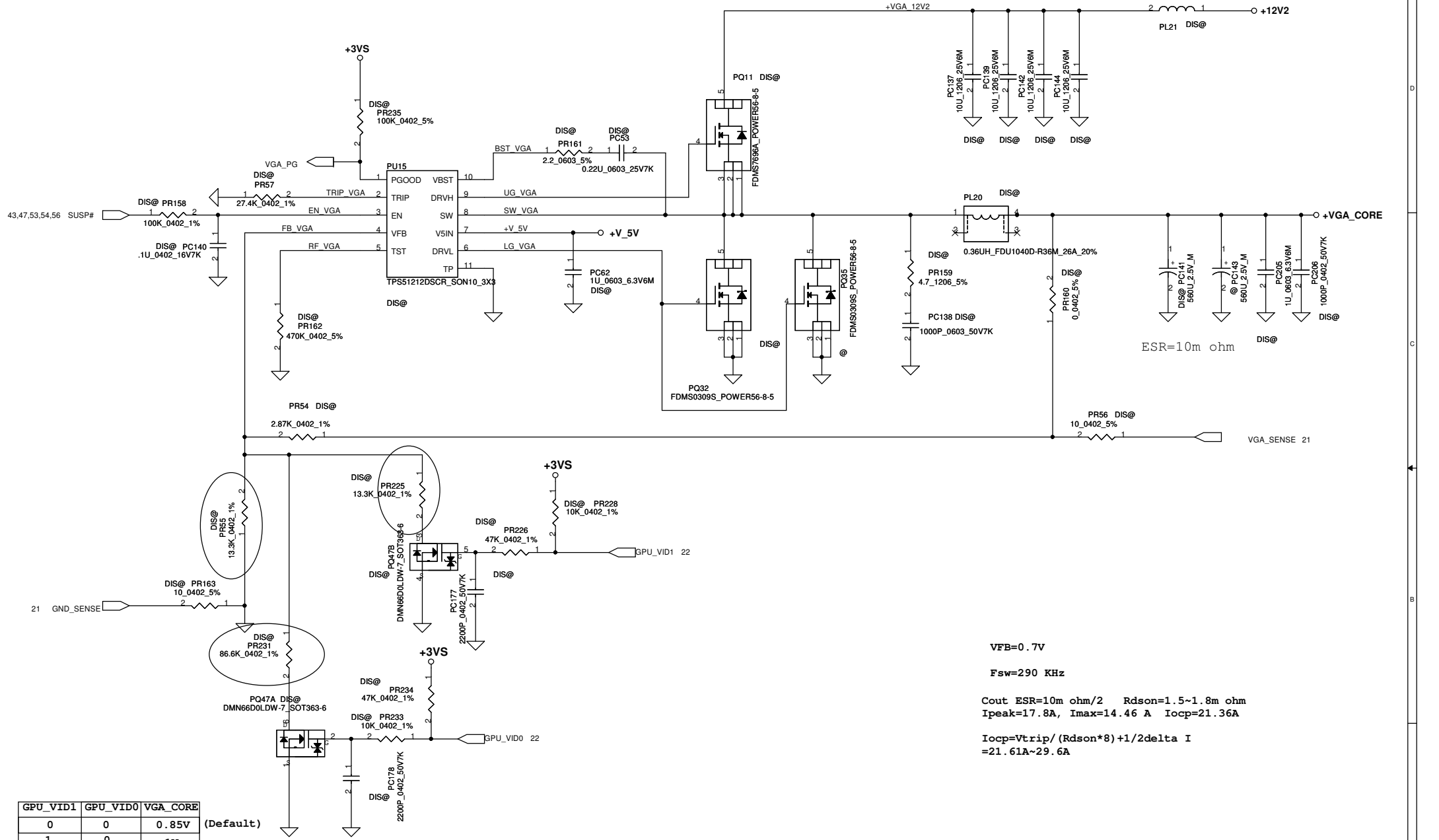
VGFX:
 Cout=220*18+ 390u 10m*4+560u 10m*3 +330u 9m*3 +560u 15m*2
 Rds=3~3.6m
 Ipeak=35 A, Imax=25 A
 Delta I=7A

OCP= 40 A

CPU_CORE:
 Cout=220*18+ 390u 10m*4+560u 10m*3 +330u 9m*3 +560u 15m*2
 Rds=3~3.6m
 Ipeak= A, Imax=85 A
 F=338k hz
 Delta I=

OCP= 135 A

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VFB=0.7V
 Fsw=290 KHz
 Cout ESR=10m ohm/2 Rdsn=1.5~1.8m ohm
 Ipeak=17.8A, Imax=14.46 A Iocp=21.36A
 $I_{ocp} = V_{trip} / (R_{dsn} * 8) + 1/2 \Delta I$
 =21.61A~29.6A

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V
1	0	1V
1	1	1.025V

(Default)

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