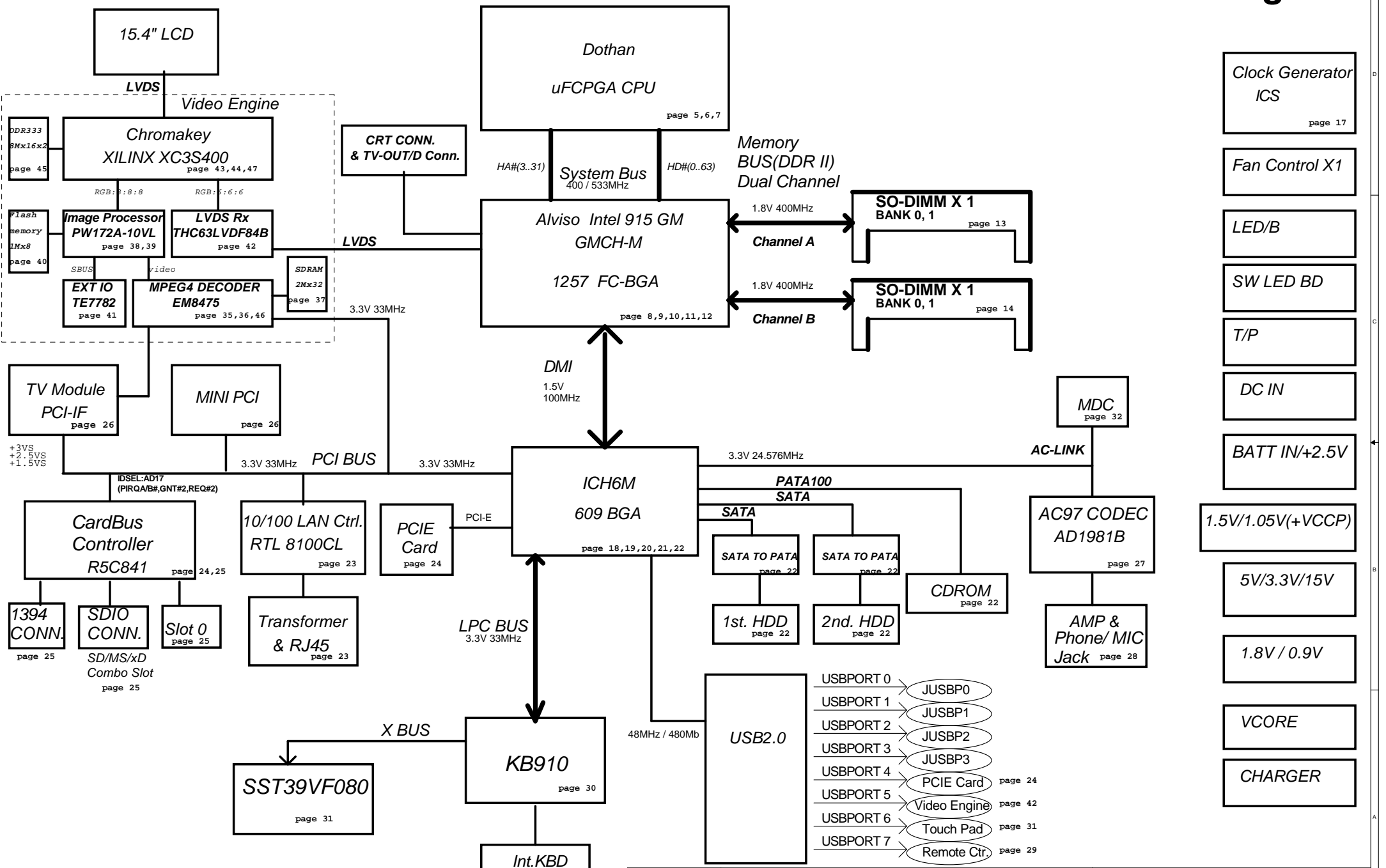


# WT2

# HAR00 LA-2831 Schematic

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# I2C / SMBUS ADDRESSING

## External PCI Devices

DEVICE	IDSEL	REQ/GNT #	PIRO
LAN	#D17	0	F
CARD BUS	AD20	1	A
Cardreader			B
1394	AD16	2	E
Wireless LAN(MINI PCI)	AD18	3	G,H

Power Management table

Signal	+12VALW +3VALW +5VALW	+2.5V +3V +5V +12V	+CPU_CORE +VCCP +5VS +3VS +2.5VS +1.8VS +1.25VS +1.5VS
State			
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	PCB Rev	Data
Bringup-Build ES-Build	0.1	
PP-Build		
MP1-Build		
MP-Build		

SCHEMATICS VERSION LIST

VERSION	ISSUE DATE	REMARK
0.0A		First Release

Ceramic Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+/-0.05PF	+/-0.1PF	+/-0.25PF	+/-0.5PF	+/-1PF	+/-2%	+/-3%	+/-5%

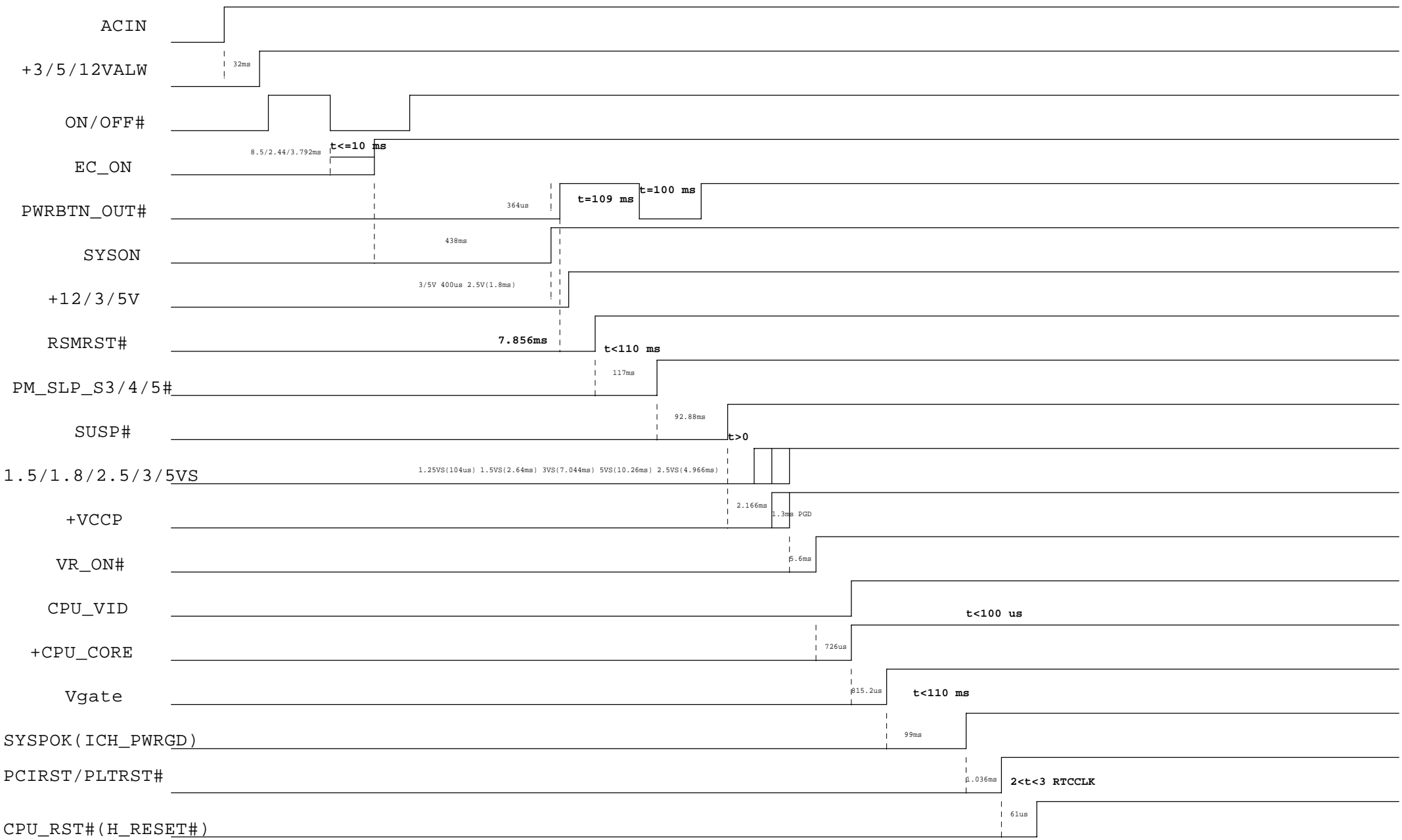
K	M	N	P	Q	V	X	Z	
+/-10%	+/-20%	+/-30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

SMBUS Control Table

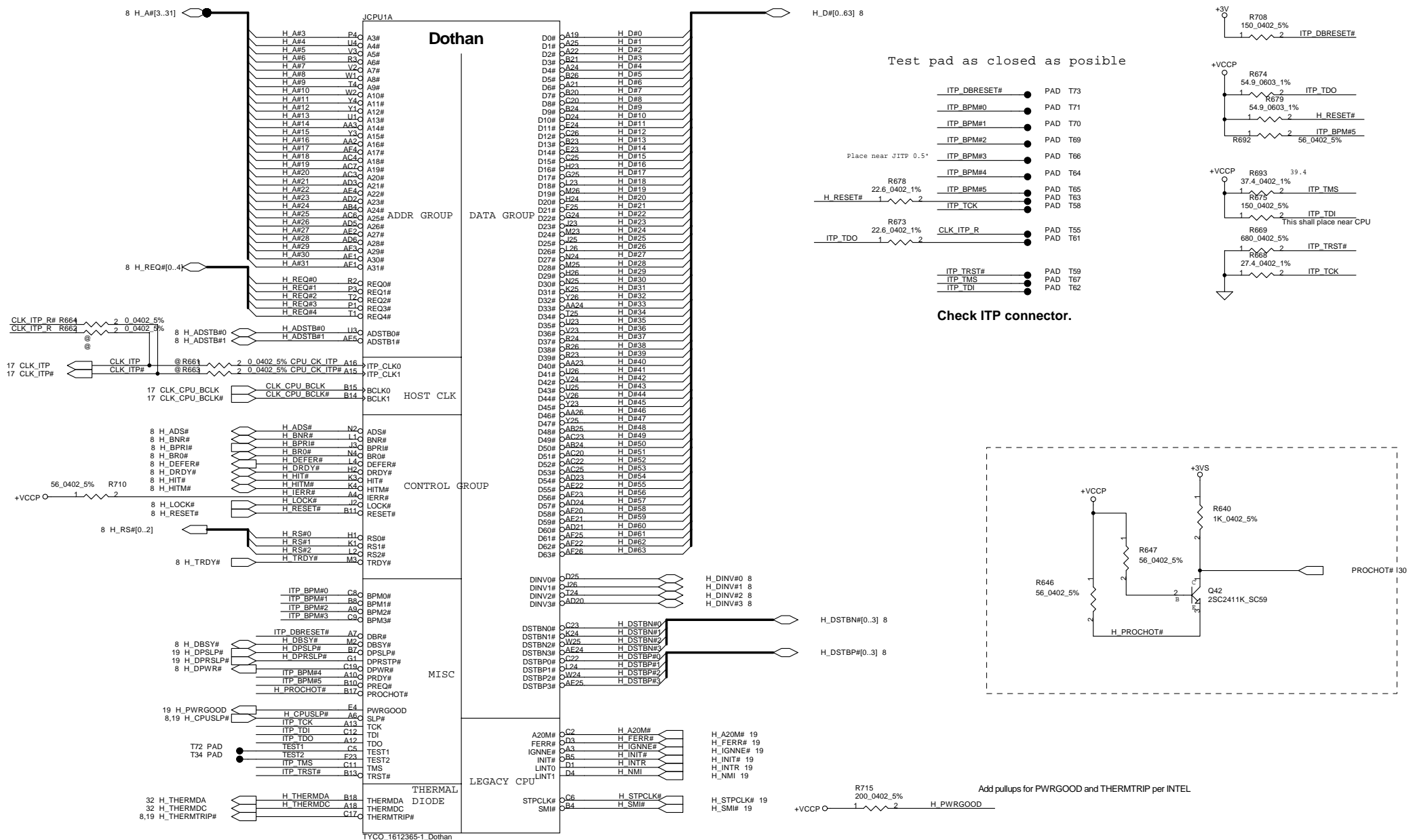
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	THERMAL SENSOR (LM75)	SODIMM	CLK CHIP	MINI PCI	LCD	VGA Thermal ADM1032
SMB_EC_CK1 SMB_EC_DA1	PC87591L	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	PC87591L	✗	✗	✗	✓	✓	✗	✗	✗	✗	✓
ICH_SMBCLK ICH_SMBDATA	ICH6-M	✗	✗	✗	✗	✗	✓	✓	✗	✗	✗
LCD_DDCCLK LCD_DDCDATA	Alviso GM-GP	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗

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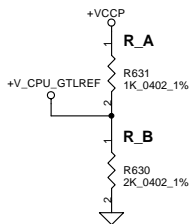
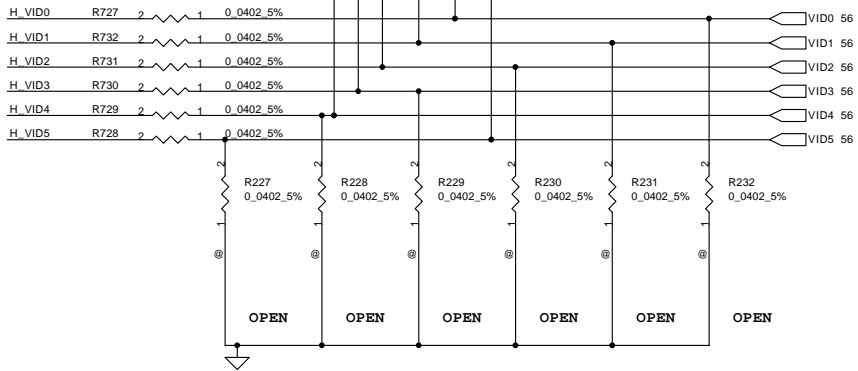


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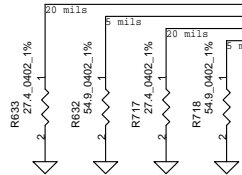
For test only ,Cmos output

CPU Voltage ID

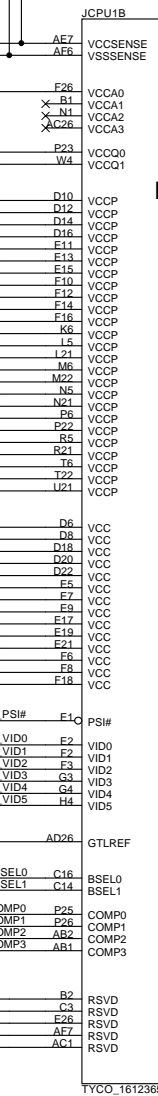
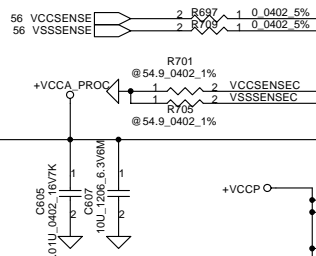


Layout close CPU

Layout Note:  
500 mil max length



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



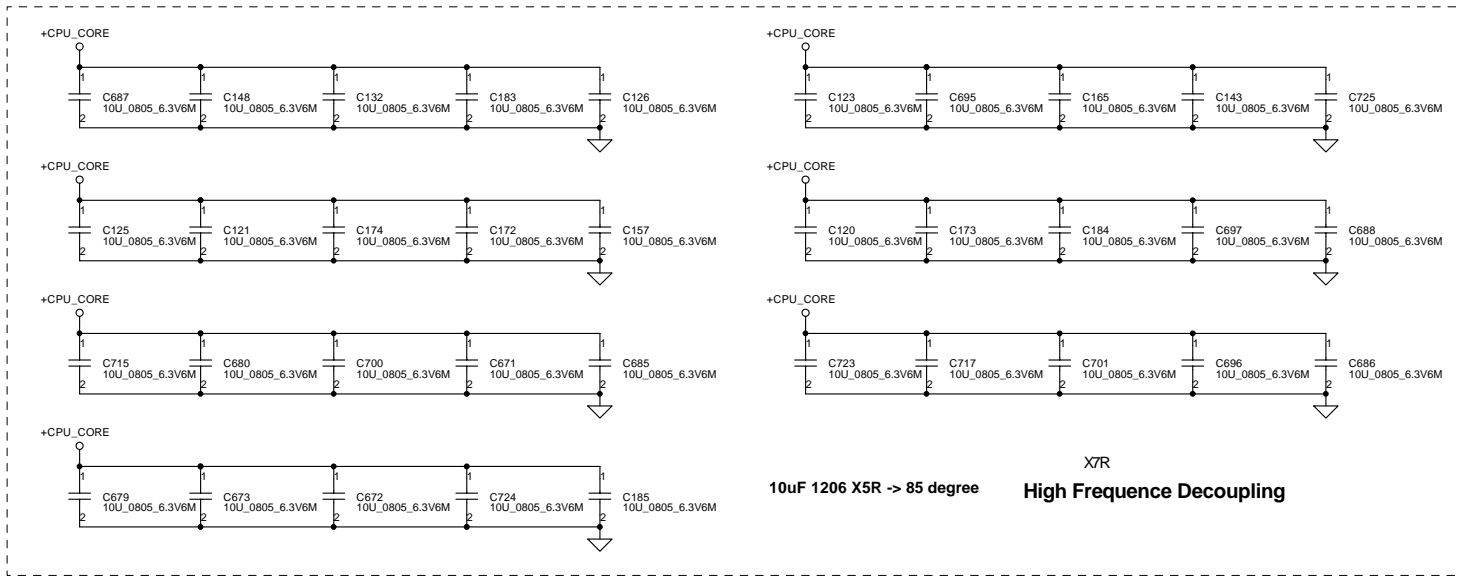
Dothan

Dothan

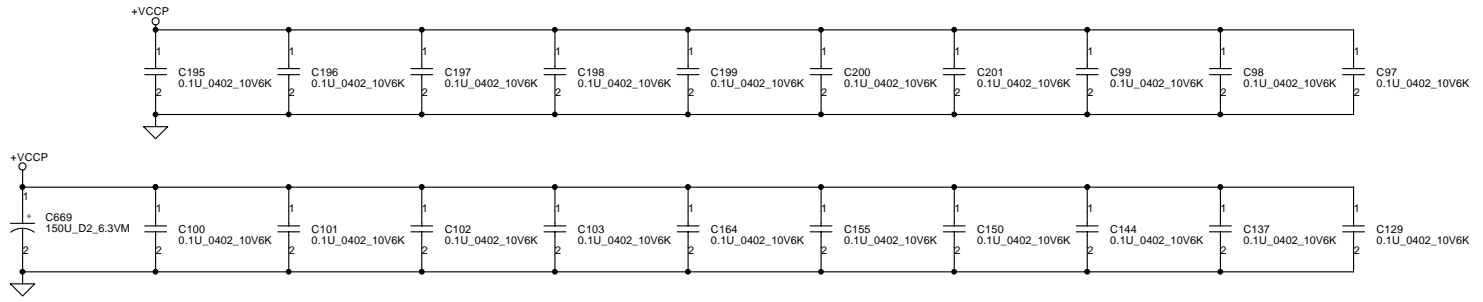
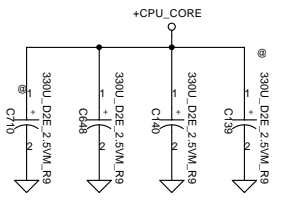
POWER, GROUND, RESERVED SIGNALS AND NC

POWER, GROUND

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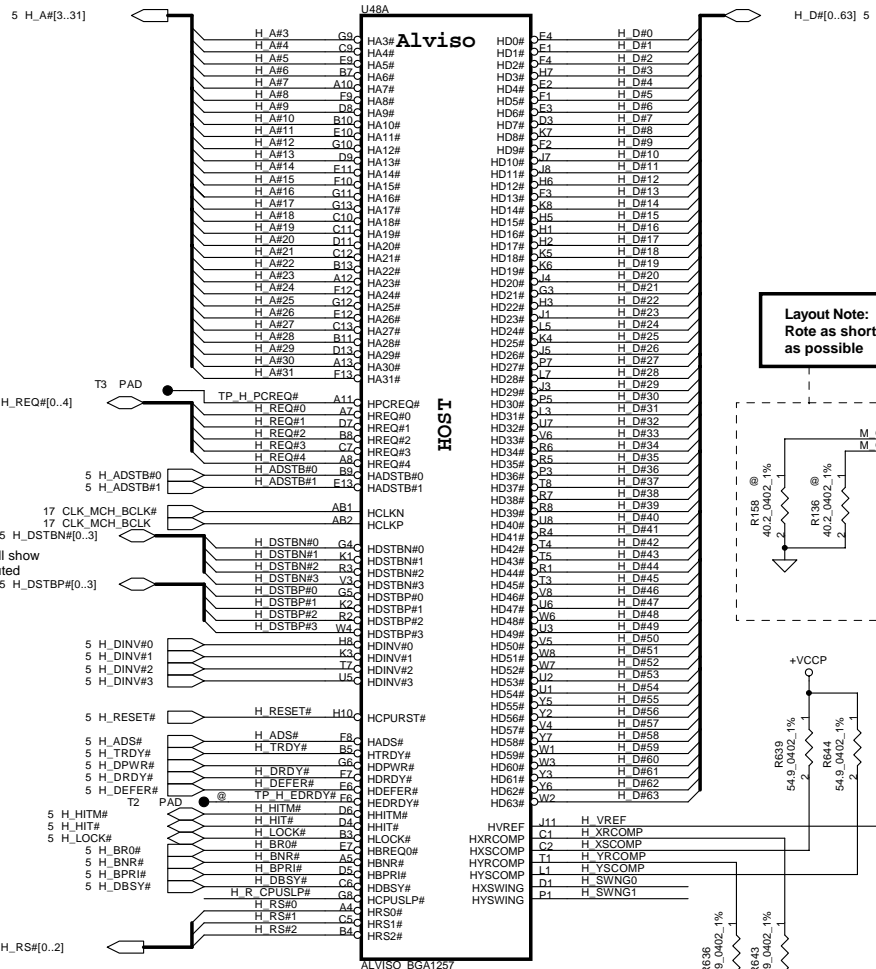
Near VCORE regulator.



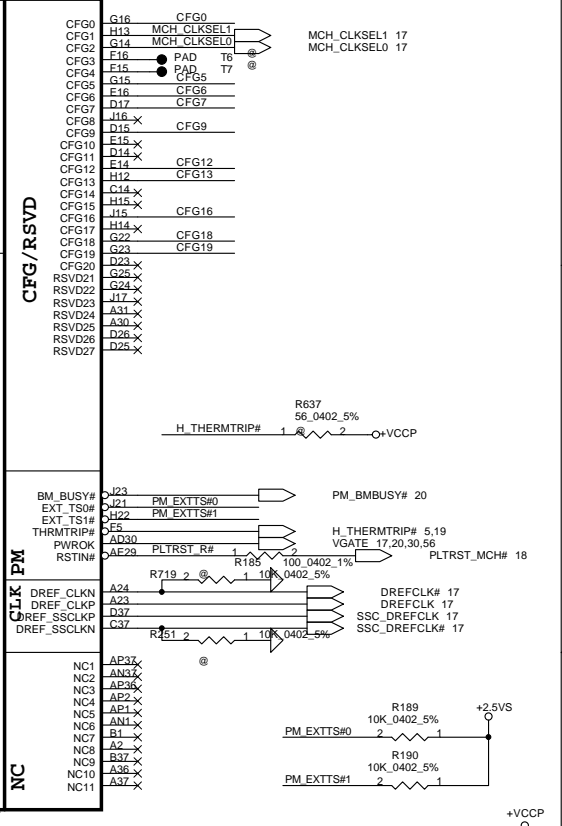
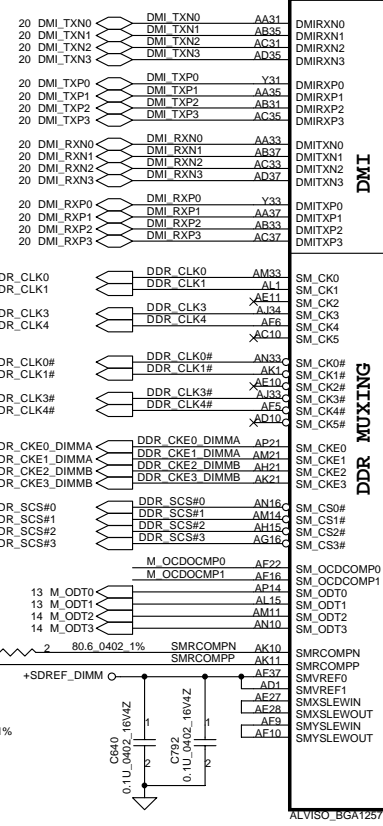
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Layout Guide will show these signals routed differentially.

Alviso CFG[17:3] has internal pull-up



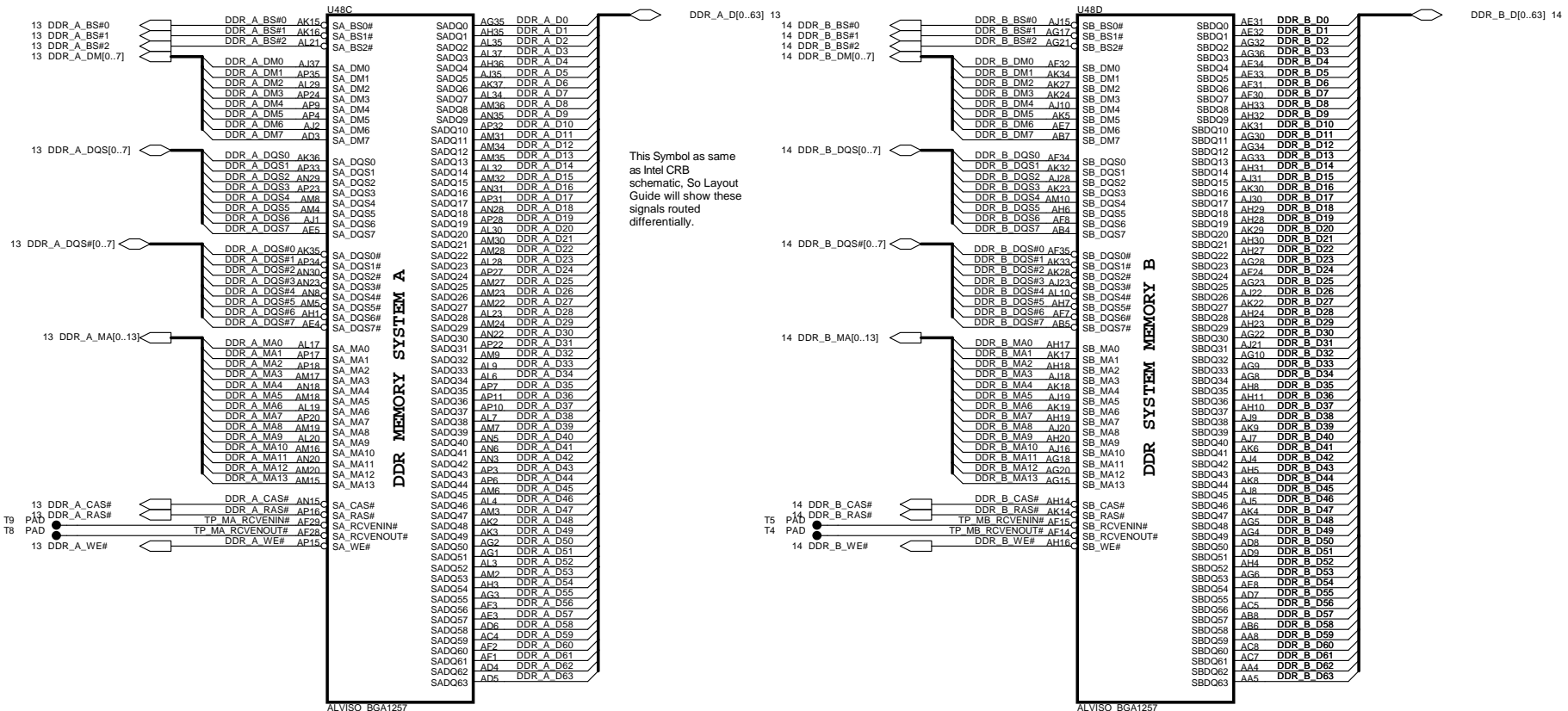
Layout Note:  
Rote as short as possible



CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

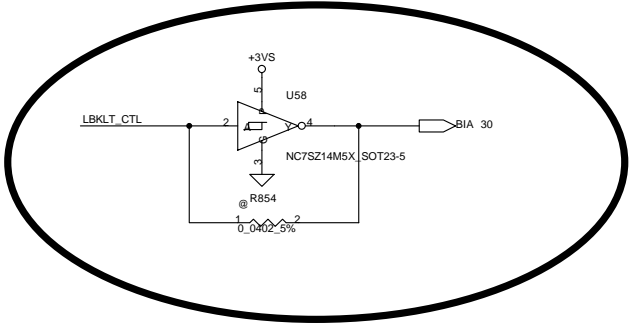
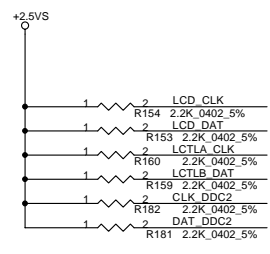
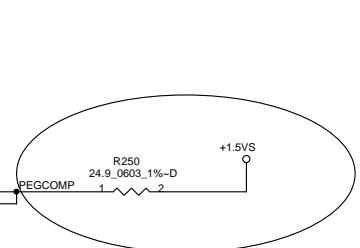
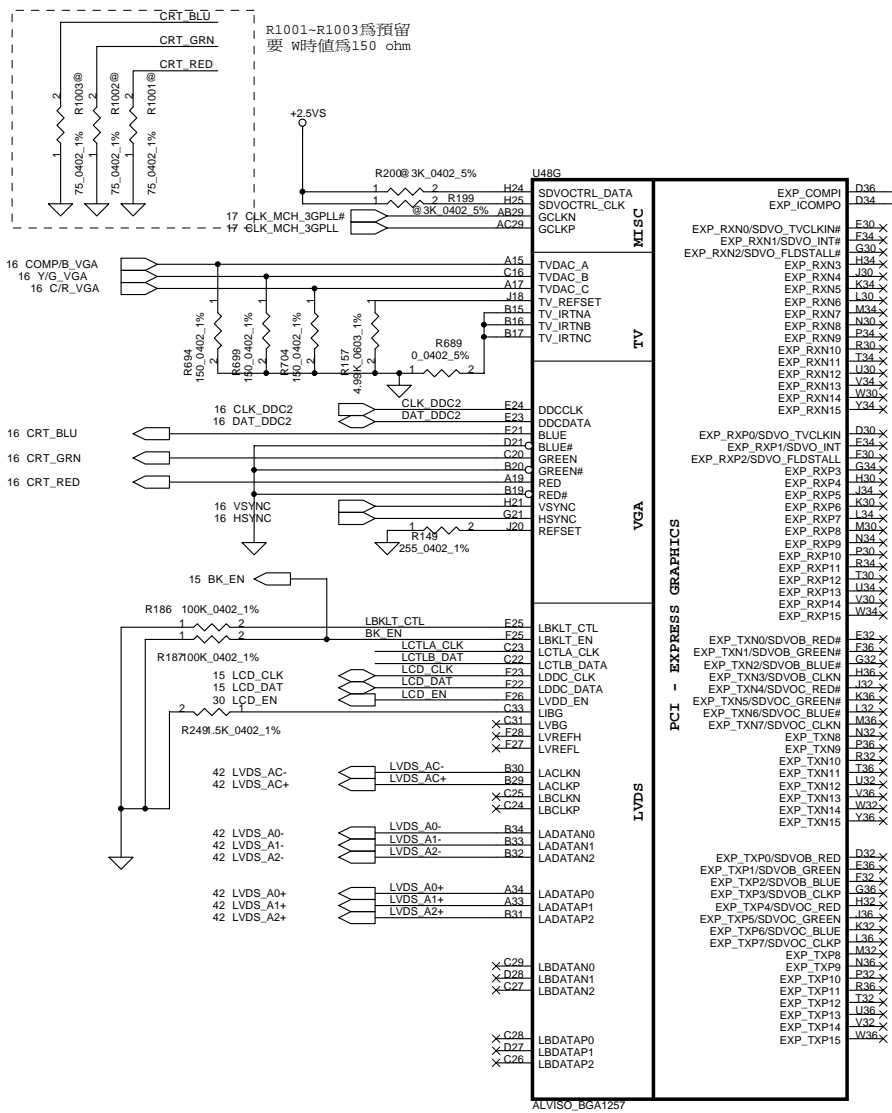
Note:  
"Do not install R for Dothan-A,  
Install R97 for Dothan-B"





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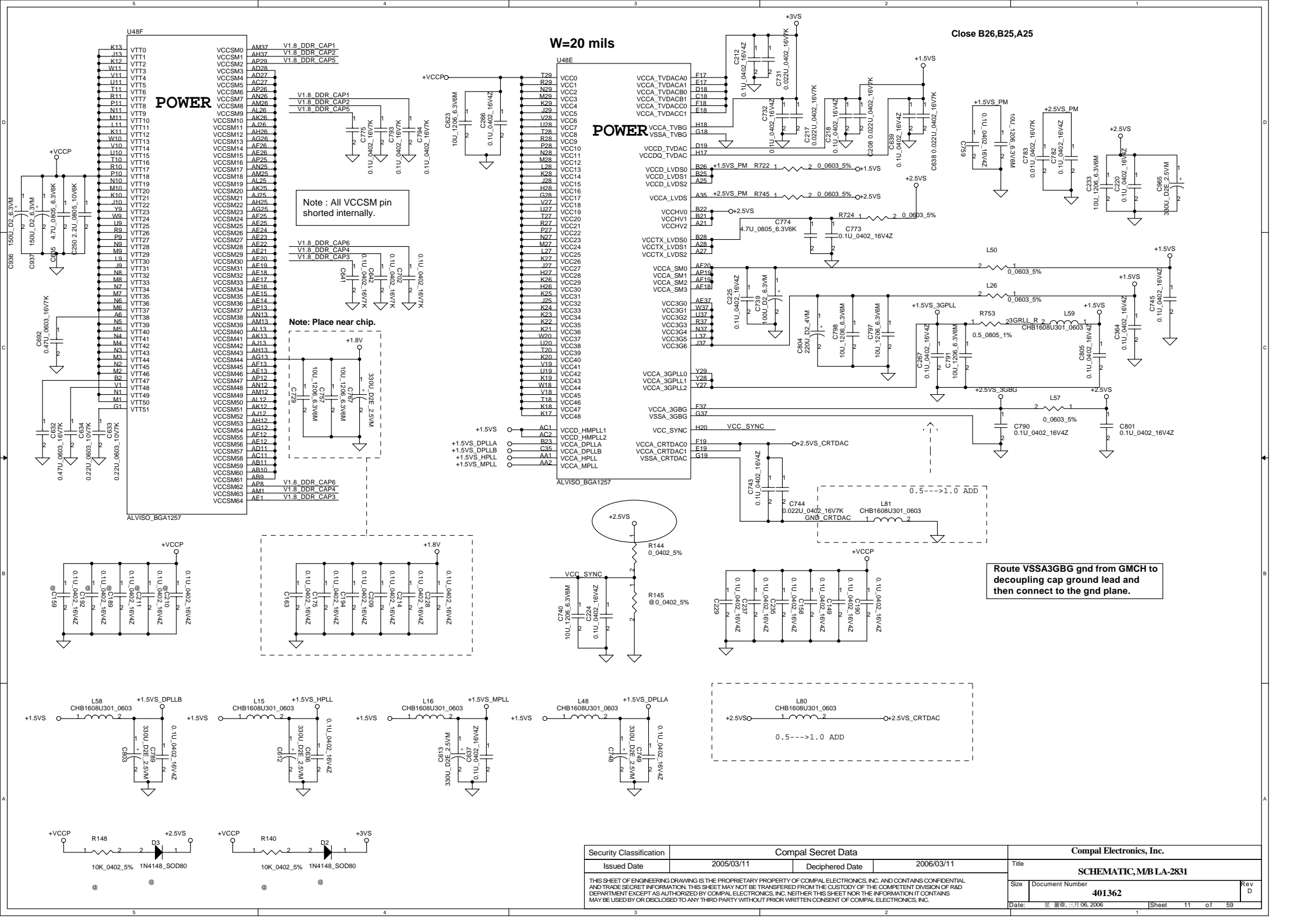


U48G

SDVOCTRL_DATA	H24	EXP_COMP1	D36
SDVOCTRL_CLK	H25	EXP_ICOMPO	D34
GCLKN	AB23	EXP_RXN0/SDVO_TVCLKIN#	F30
GCLKP	AC29	EXP_RXN1/SDVO_INT#	F34
		EXP_RXN2/SDVO_FLDSTALL#	G30
		EXP_RXN3	H34
		EXP_RXN4	I30
		EXP_RXN5	J34
		EXP_RXN6	L30
		EXP_RXN7	M34
		EXP_RXN8	N30
		EXP_RXN9	P34
		EXP_RXN10	R30
		EXP_RXN11	T34
		EXP_RXN12	U30
		EXP_RXN13	V34
		EXP_RXN14	W30
		EXP_RXN15	X34
		EXP_RXP0/SDVO_TVCLKIN	D30
		EXP_RXP1/SDVO_INT#	E34
		EXP_RXP2/SDVO_FLDSTALL	F30
		EXP_RXP3	G34
		EXP_RXP4	H30
		EXP_RXP5	I34
		EXP_RXP6	J30
		EXP_RXP7	K34
		EXP_RXP8	L30
		EXP_RXP9	M34
		EXP_RXP10	N30
		EXP_RXP11	P34
		EXP_RXP12	Q30
		EXP_RXP13	R34
		EXP_RXP14	S30
		EXP_RXP15	T34
		EXP_TXN0/SDVOB_RED#	F32
		EXP_TXN1/SDVOB_GREEN#	F36
		EXP_TXN2/SDVOB_BLUE#	G32
		EXP_TXN3/SDVOB_CLKN	H36
		EXP_TXN4/SDVOC_RED#	I32
		EXP_TXN5/SDVOC_GREEN#	J36
		EXP_TXN6/SDVOC_BLUE#	K32
		EXP_TXN7/SDVOC_CLKN	M36
		EXP_TXN8	N32
		EXP_TXN9	P36
		EXP_TXN10	R32
		EXP_TXN11	T36
		EXP_TXN12	U32
		EXP_TXN13	V36
		EXP_TXN14	W32
		EXP_TXN15	X36
		EXP_TXP0/SDVOB_RED	D32
		EXP_TXP1/SDVOB_GREEN	E36
		EXP_TXP2/SDVOB_BLUE	F32
		EXP_TXP3/SDVOB_CLKP	G36
		EXP_TXP4/SDVOC_RED	H32
		EXP_TXP5/SDVOC_GREEN	I36
		EXP_TXP6/SDVOC_BLUE	K32
		EXP_TXP7/SDVOC_CLKP	L36
		EXP_TXP8	M32
		EXP_TXP9	N36
		EXP_TXP10	P32
		EXP_TXP11	Q36
		EXP_TXP12	R32
		EXP_TXP13	S36
		EXP_TXP14	T32
		EXP_TXP15	U36

ALVISO\_BGA1257

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**POWER**

W=20 mils

**POWER**

Close B26,B25,A25

Note : All VCCSM pin shorted internally.

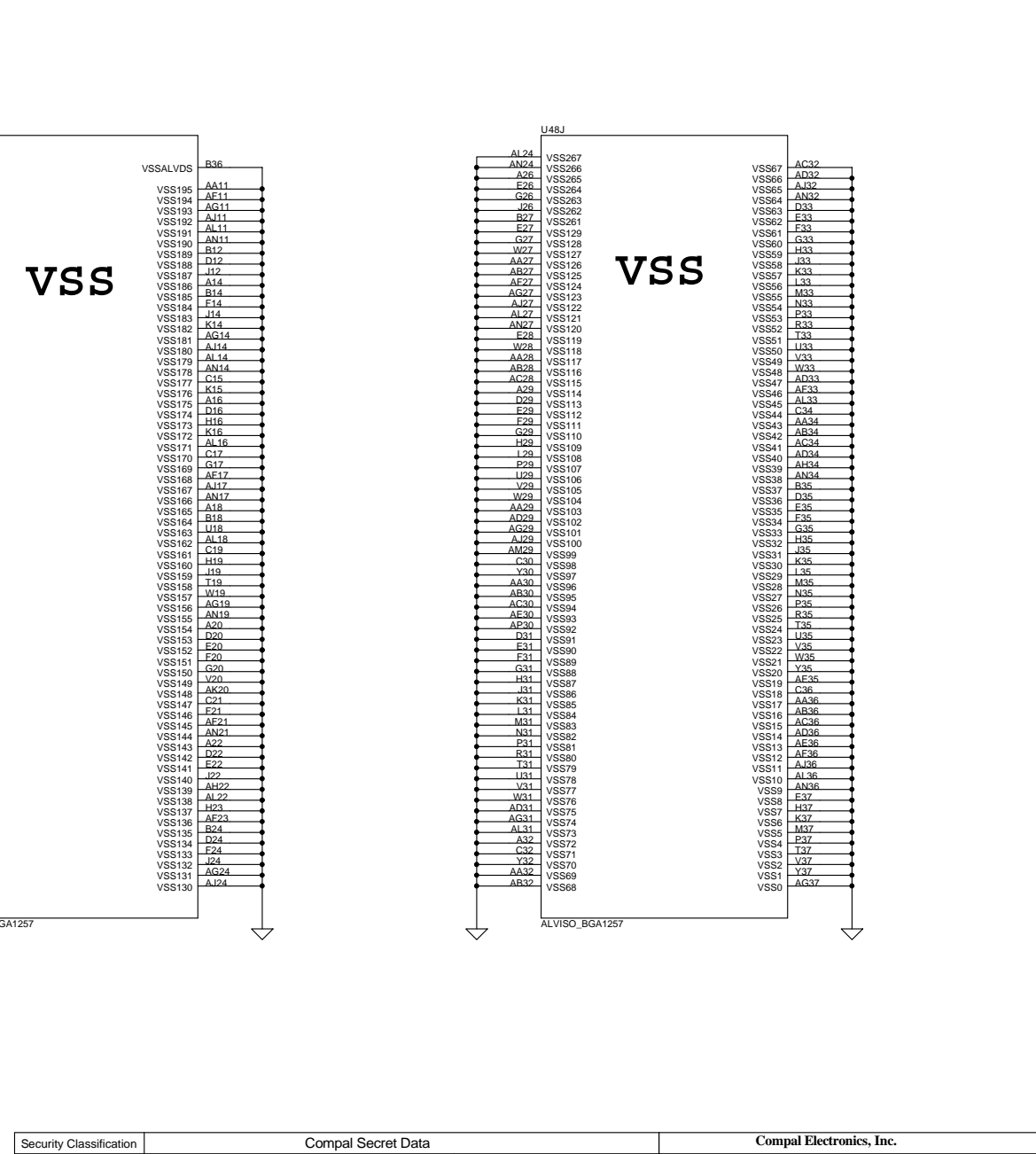
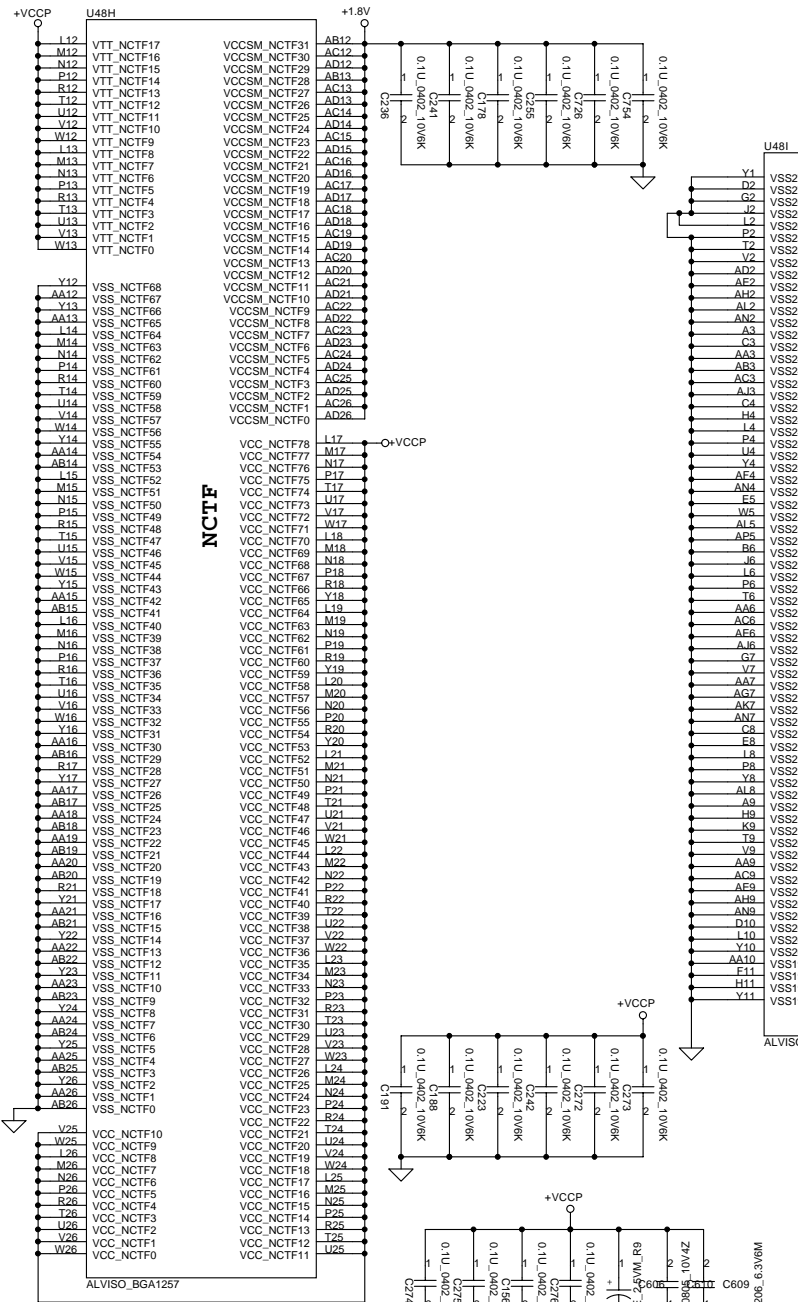
Note: Place near chip.

Route VSSA3GBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

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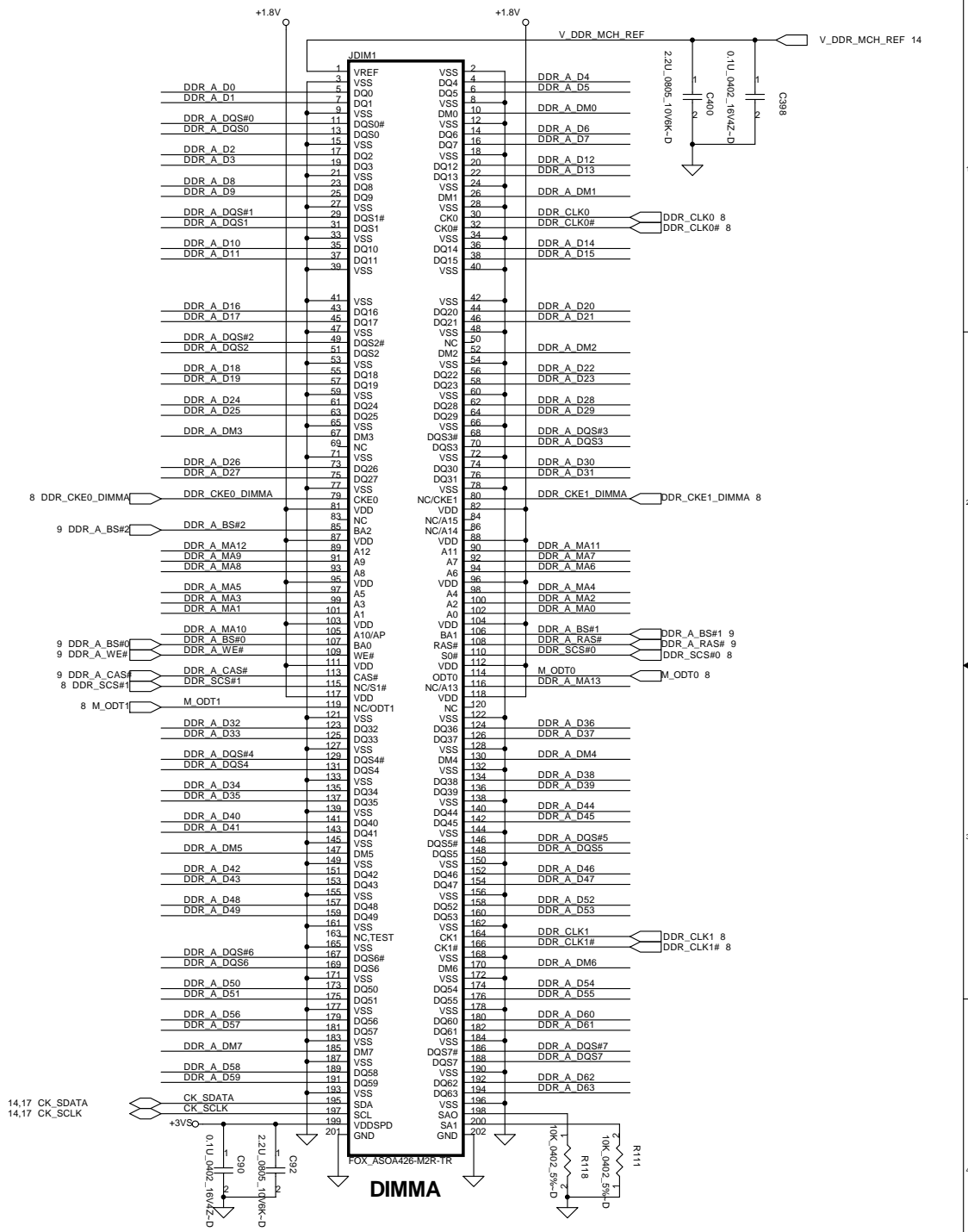
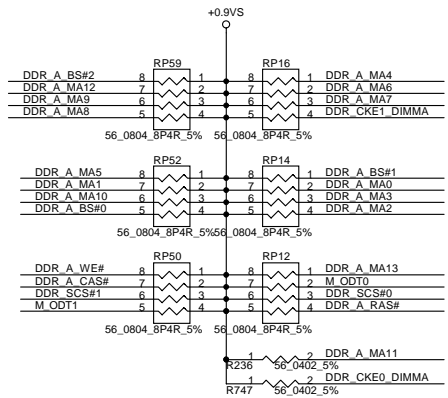
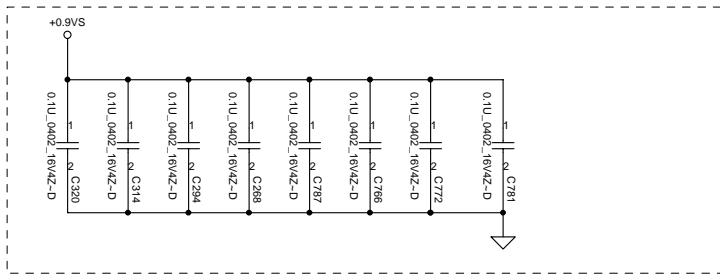
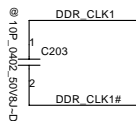
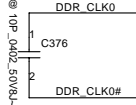
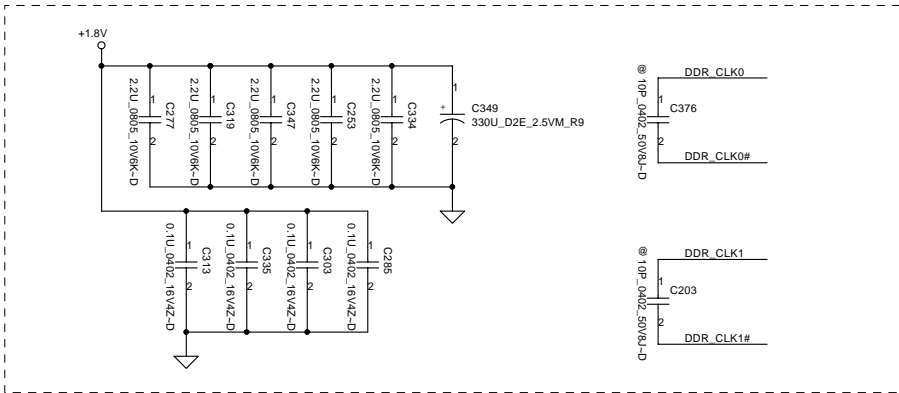
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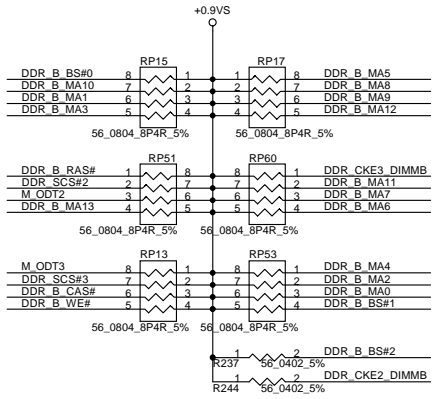
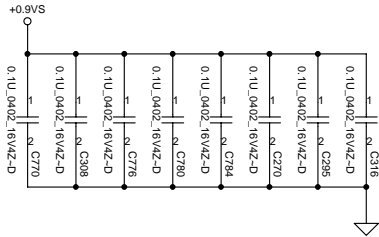
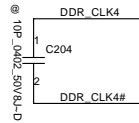
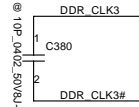
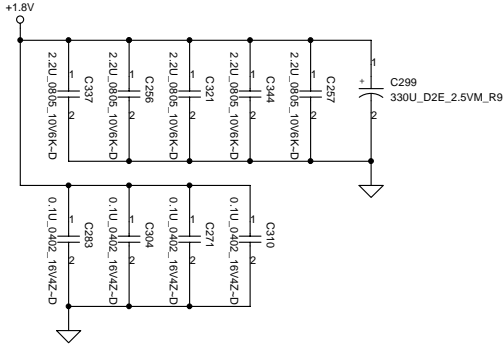
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- 9 DDR\_A\_D[0..63] DDR\_A\_D[0..63]
- 9 DDR\_A\_DM[0..7] DDR\_A\_DM[0..7]
- 9 DDR\_A\_DQS[0..7] DDR\_A\_DQS[0..7]
- 9 DDR\_A\_MA[0..13] DDR\_A\_MA[0..13]
- 9 DDR\_A\_DQS#[0..7] DDR\_A\_DQS#[0..7]



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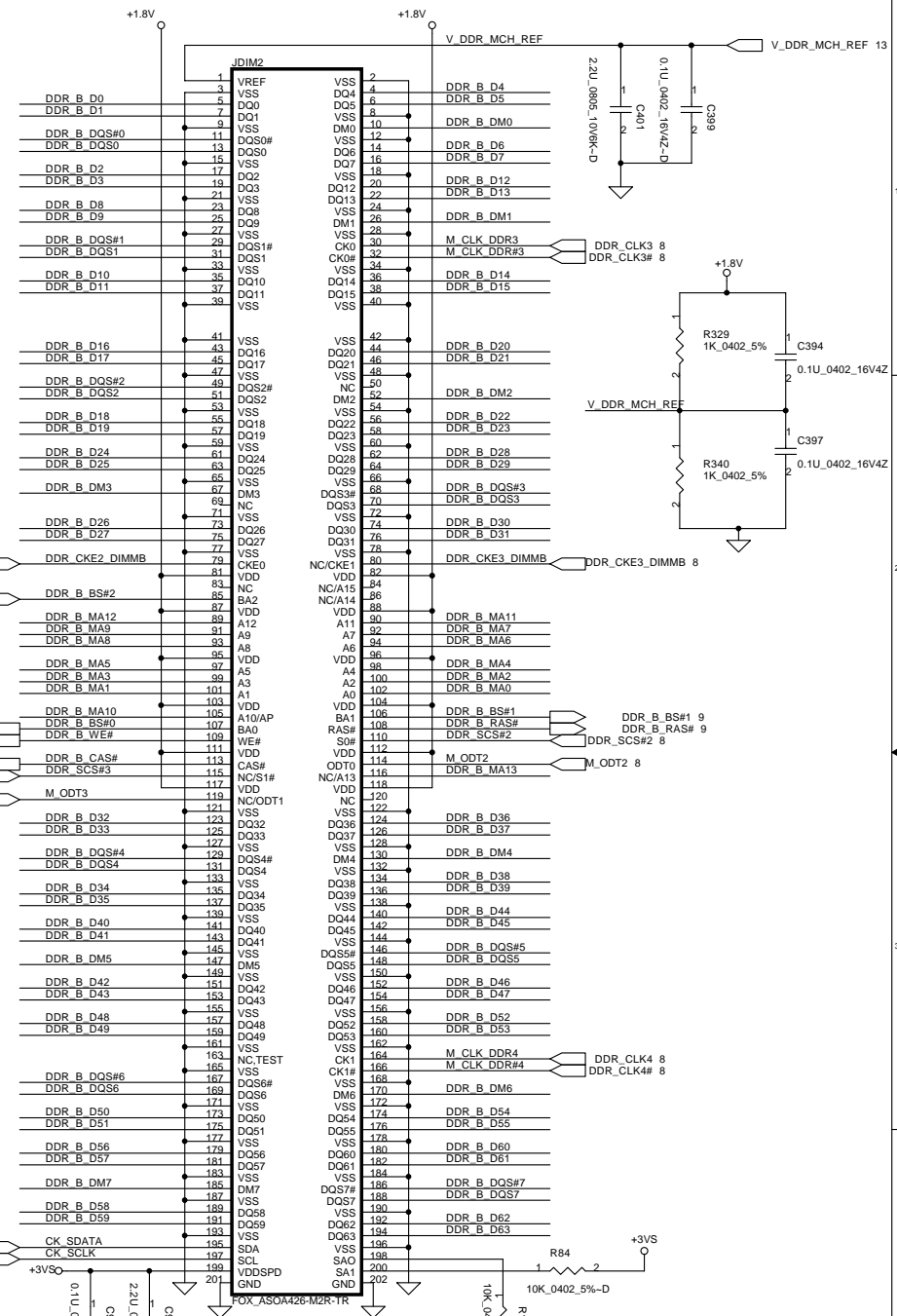
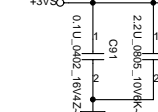
- 9 DDR\_B\_D[0..63]  $\Rightarrow$  DDR B D[0..63]
- 9 DDR\_B\_DM[0..7]  $\Rightarrow$  DDR B DM[0..7]
- 9 DDR\_B\_DQS[0..7]  $\Rightarrow$  DDR B DQS[0..7]
- 9 DDR\_B\_MA[0..13]  $\Rightarrow$  DDR B MA[0..13]
- 9 DDR\_B\_DQS#[0..7]  $\Rightarrow$  DDR B DQS#[0..7]



**Layout Note:**  
Place these resistor closely JDIM1, all trace length < 750 mil

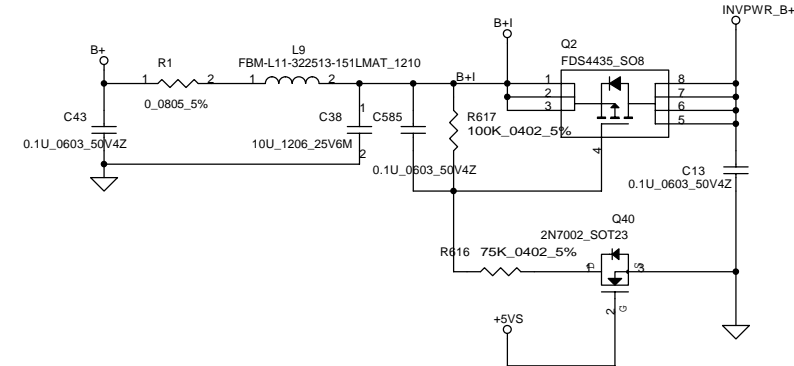
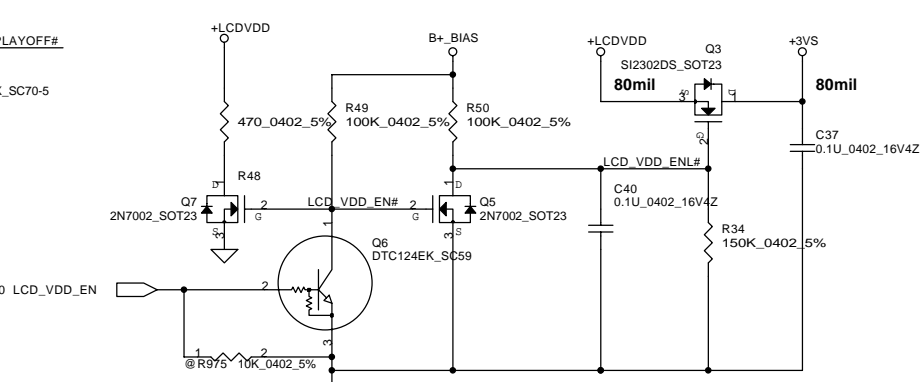
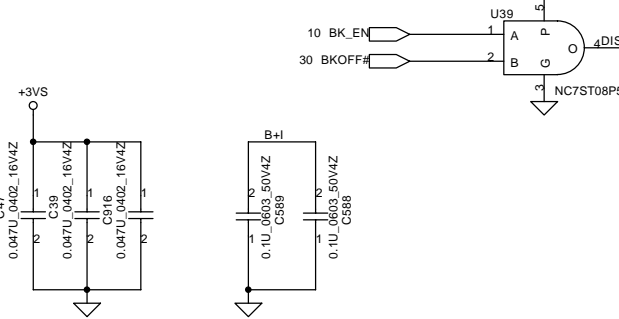
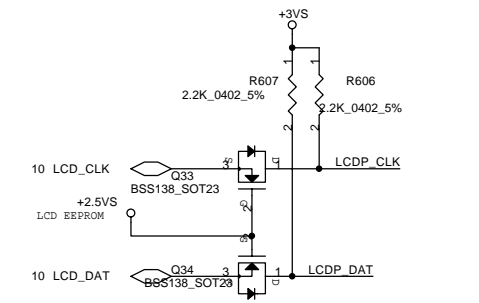
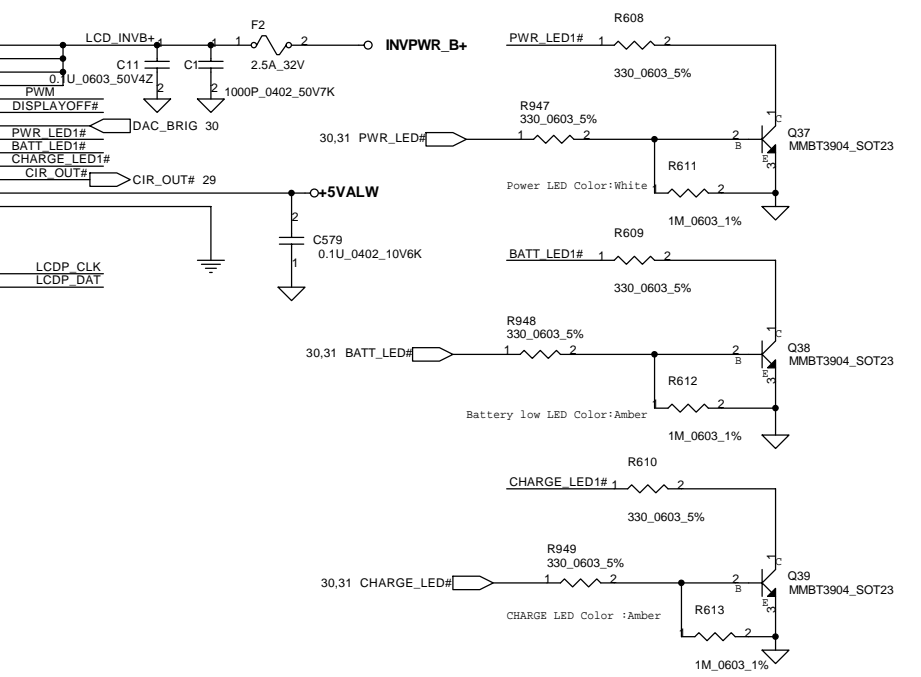
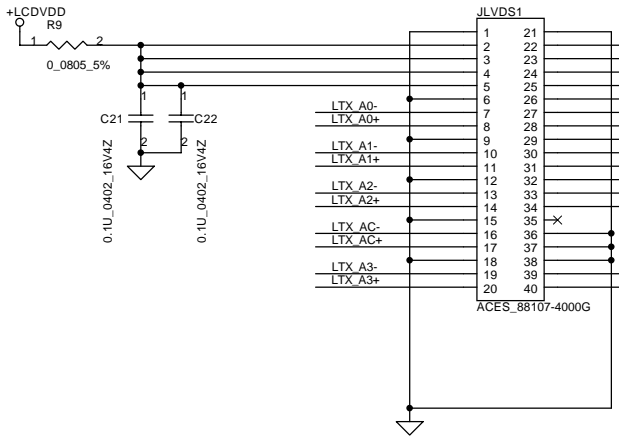
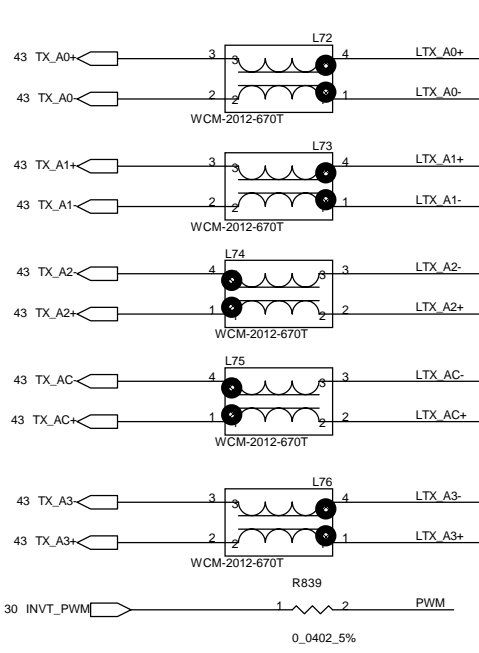
**Layout Note:**  
Place these resistor closely JDIM1, all trace length Max=1.3"

13,17 CK\_SDATA  
13,17 CK\_SCLK

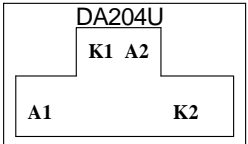
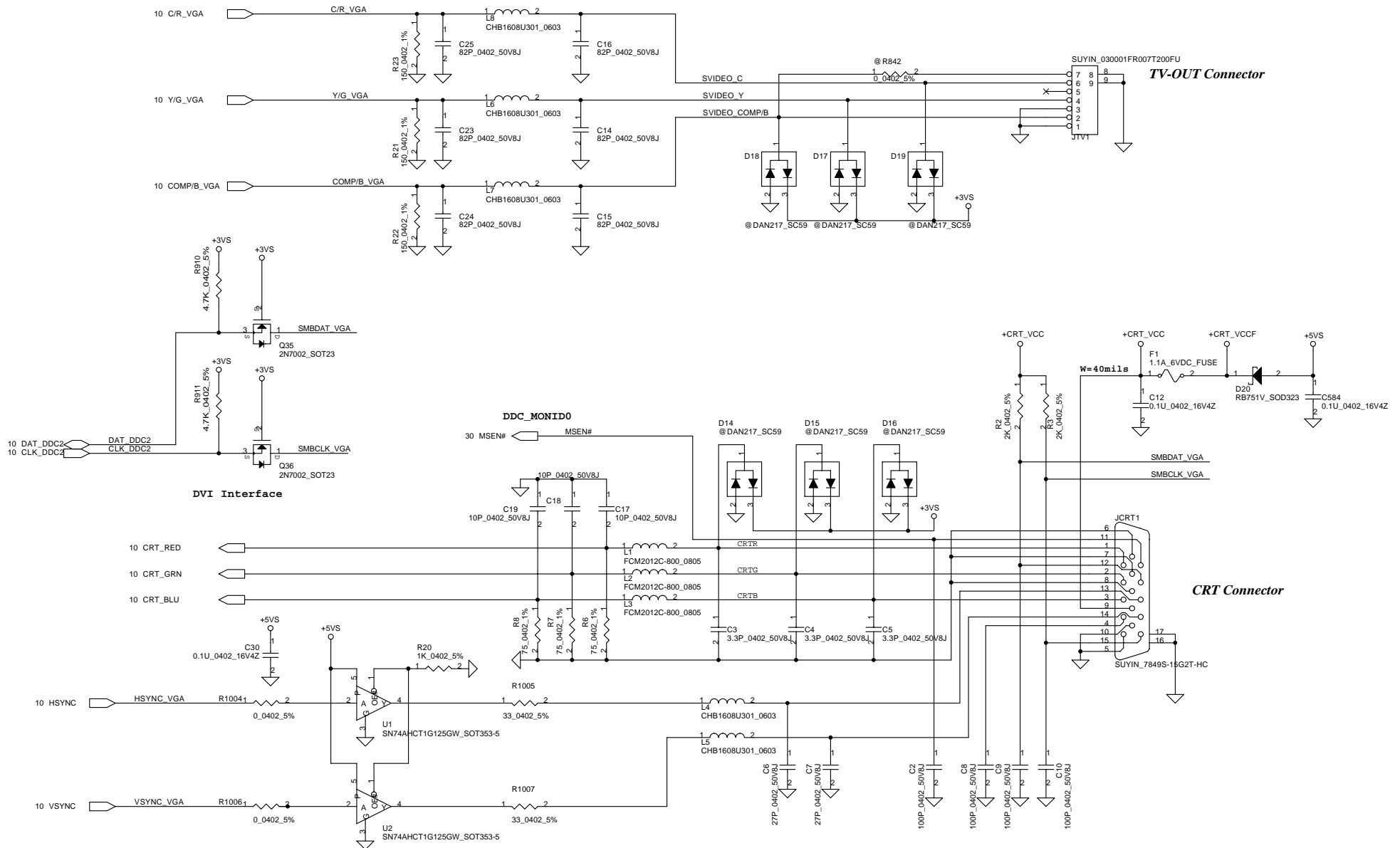


**DIMM STANDARD**

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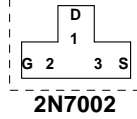
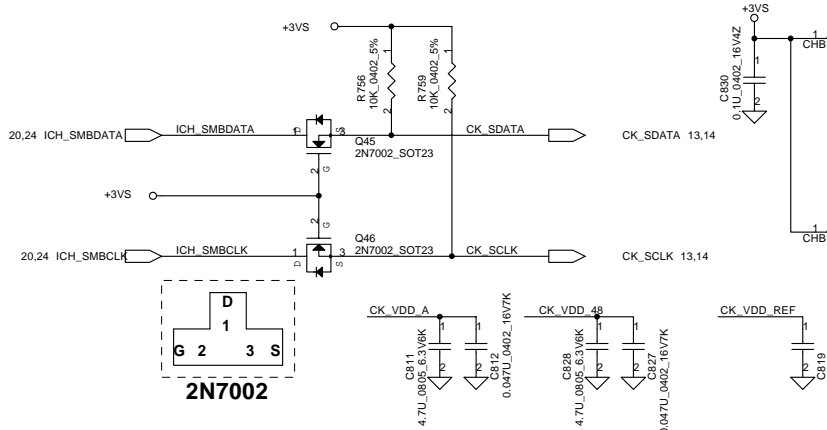
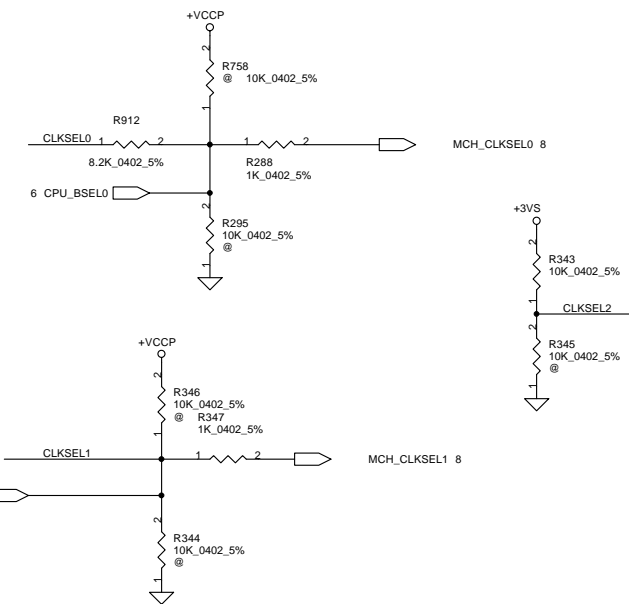
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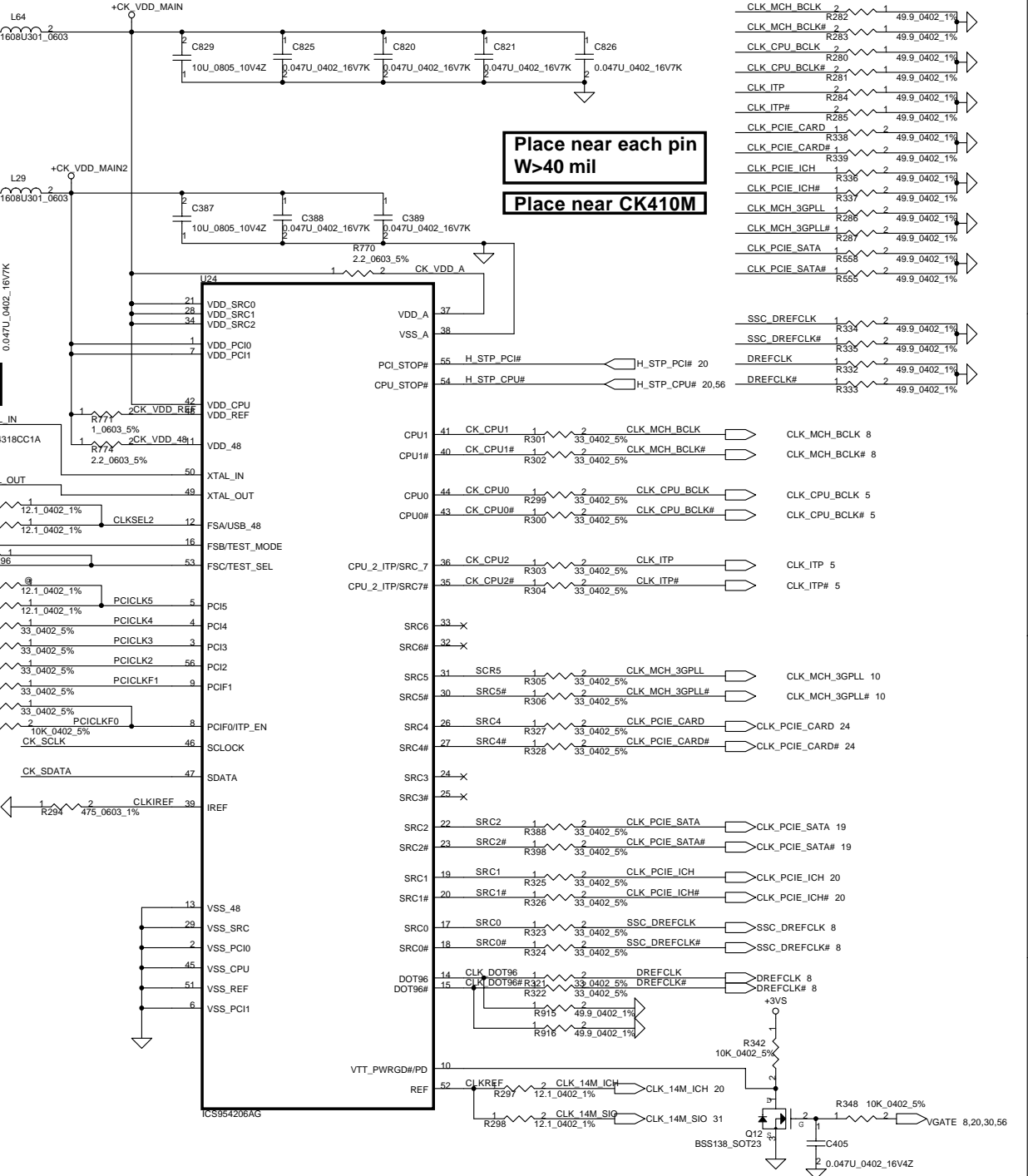
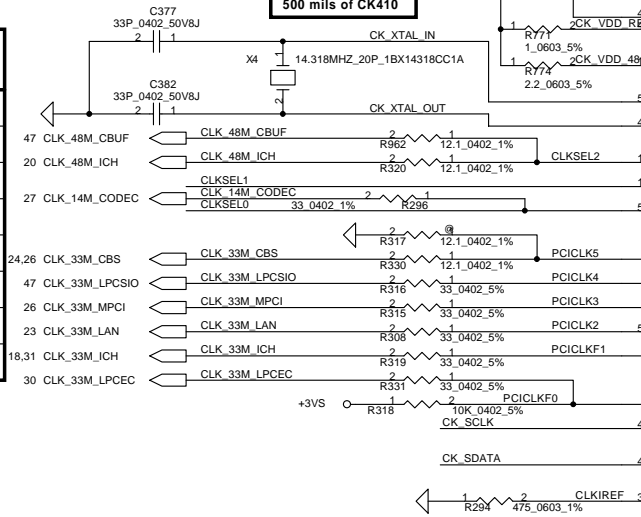
0 0 1 for Dothan-A 533Mhz  
1 0 1 for Dothan-A 400Mhz

FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	0	RESERVED		

Table : ICS 954201 / Cypress CY28411

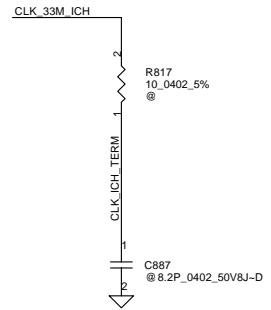
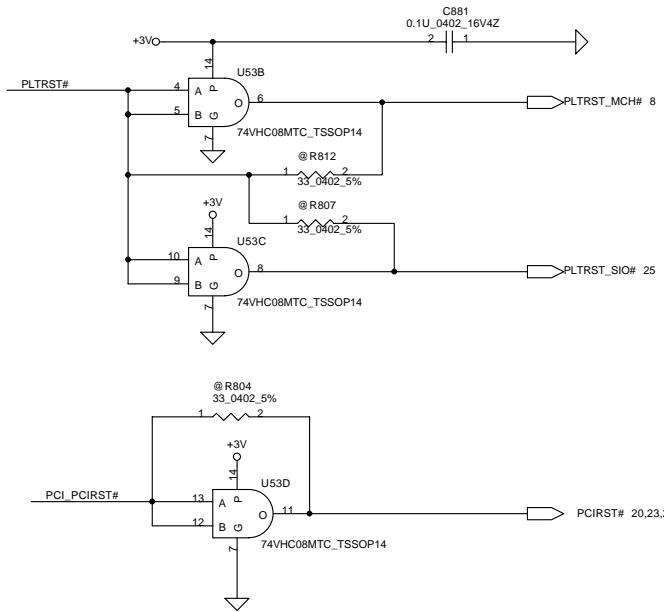
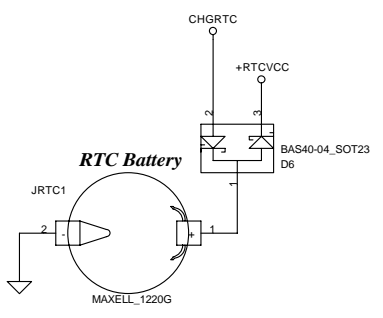
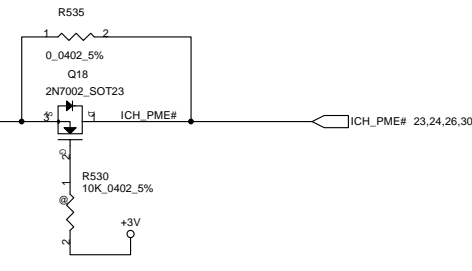
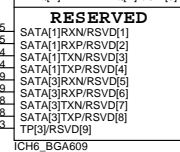
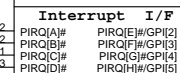
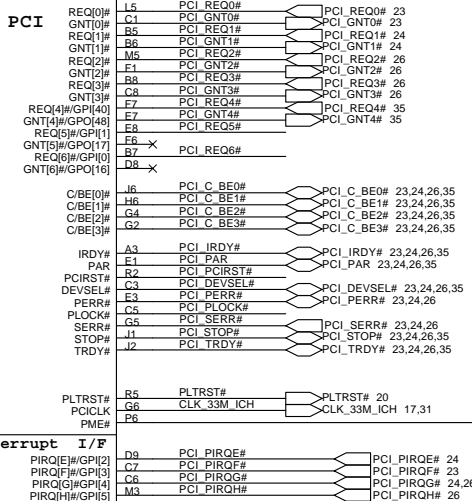
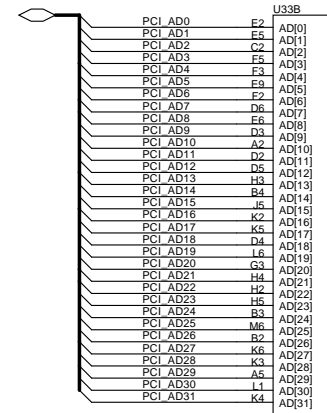
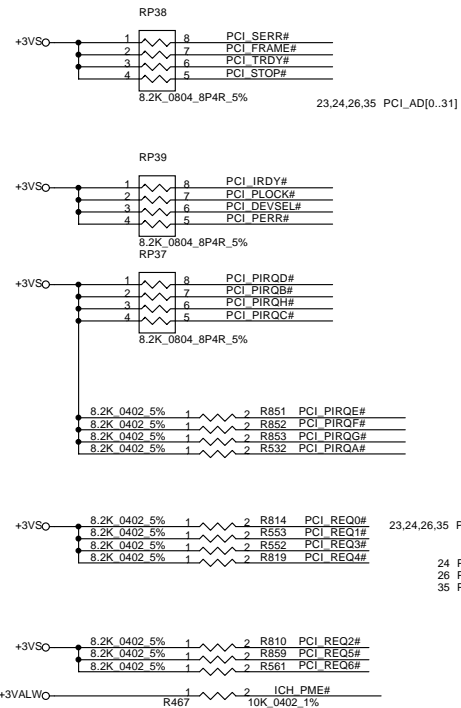


Place crystal within 500 mils of CK410

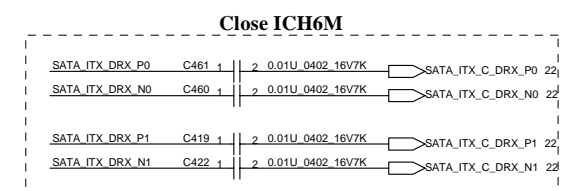
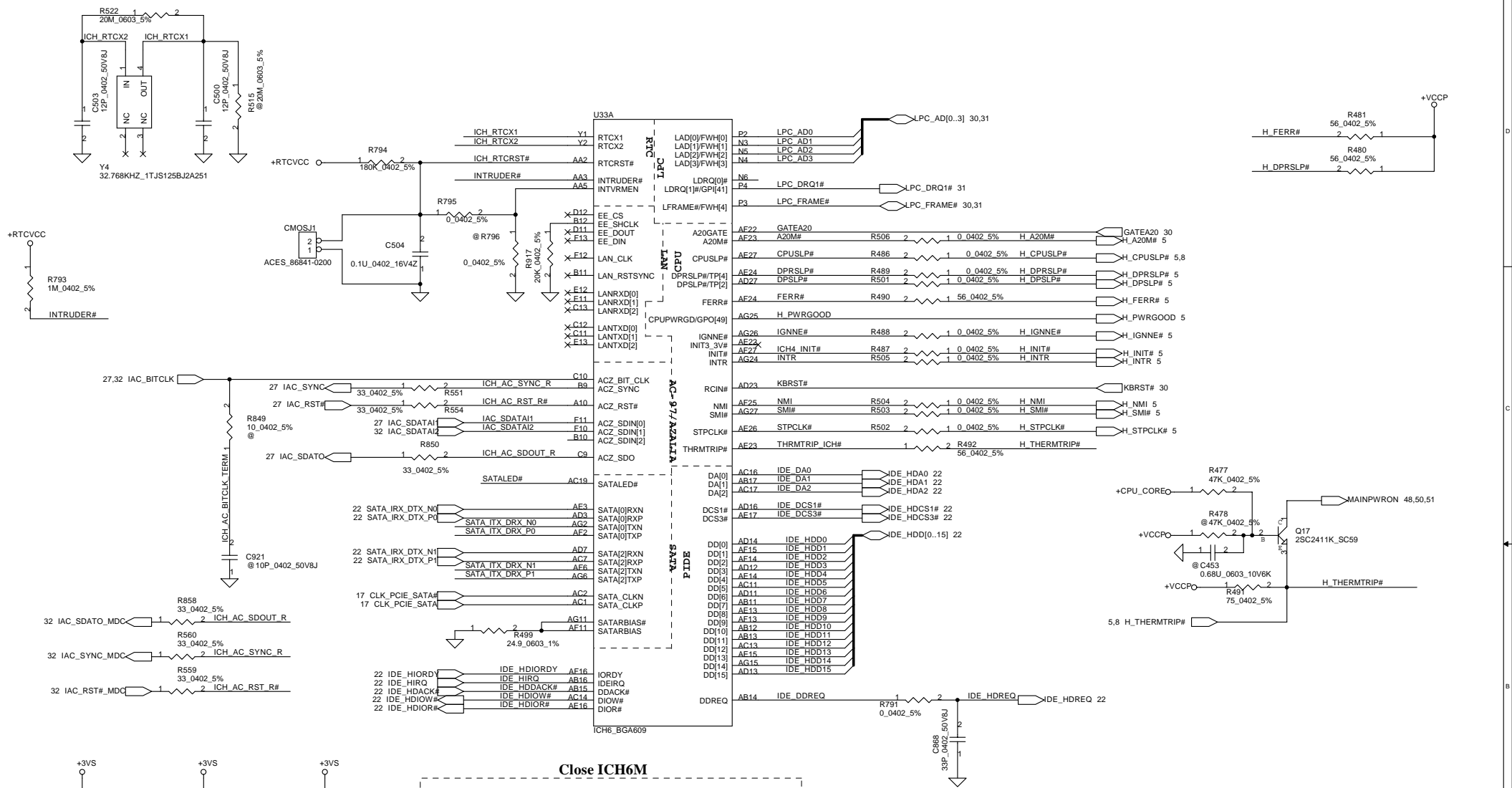


Place near each pin  
W>40 mil  
Place near CK410M

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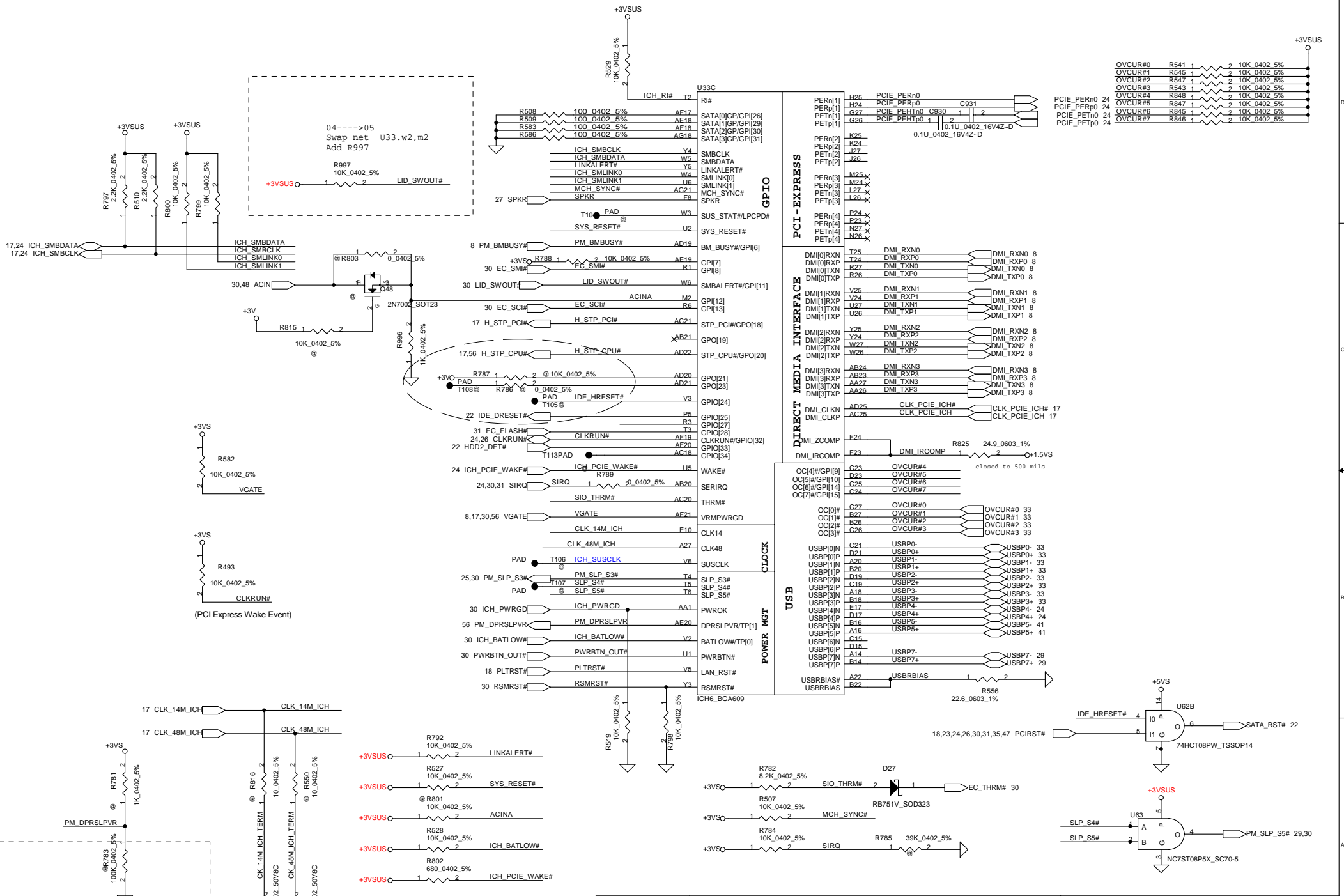


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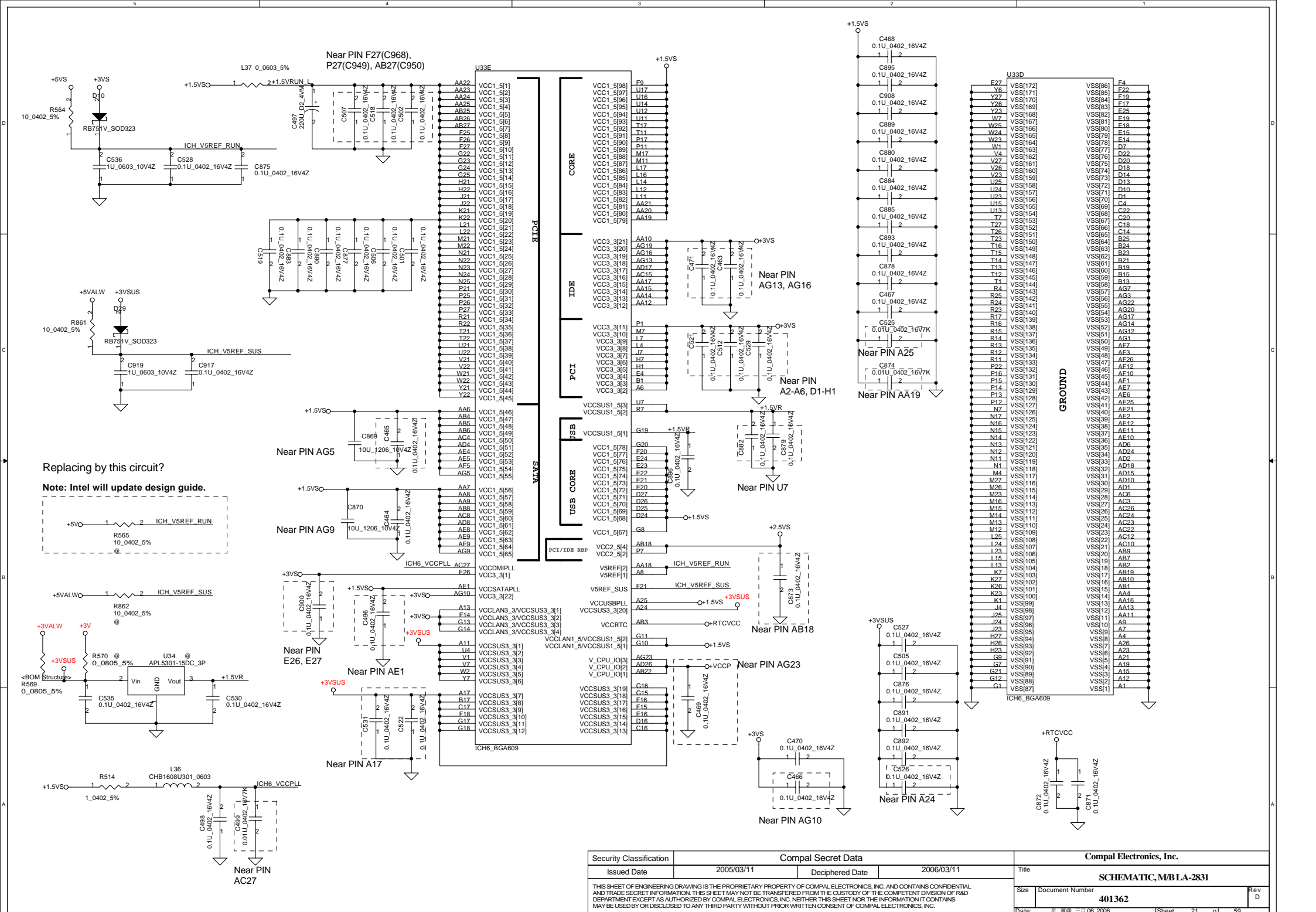
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May need pulldown for DPRSLPVR in case the ICH6m does not set this value in time for boot.

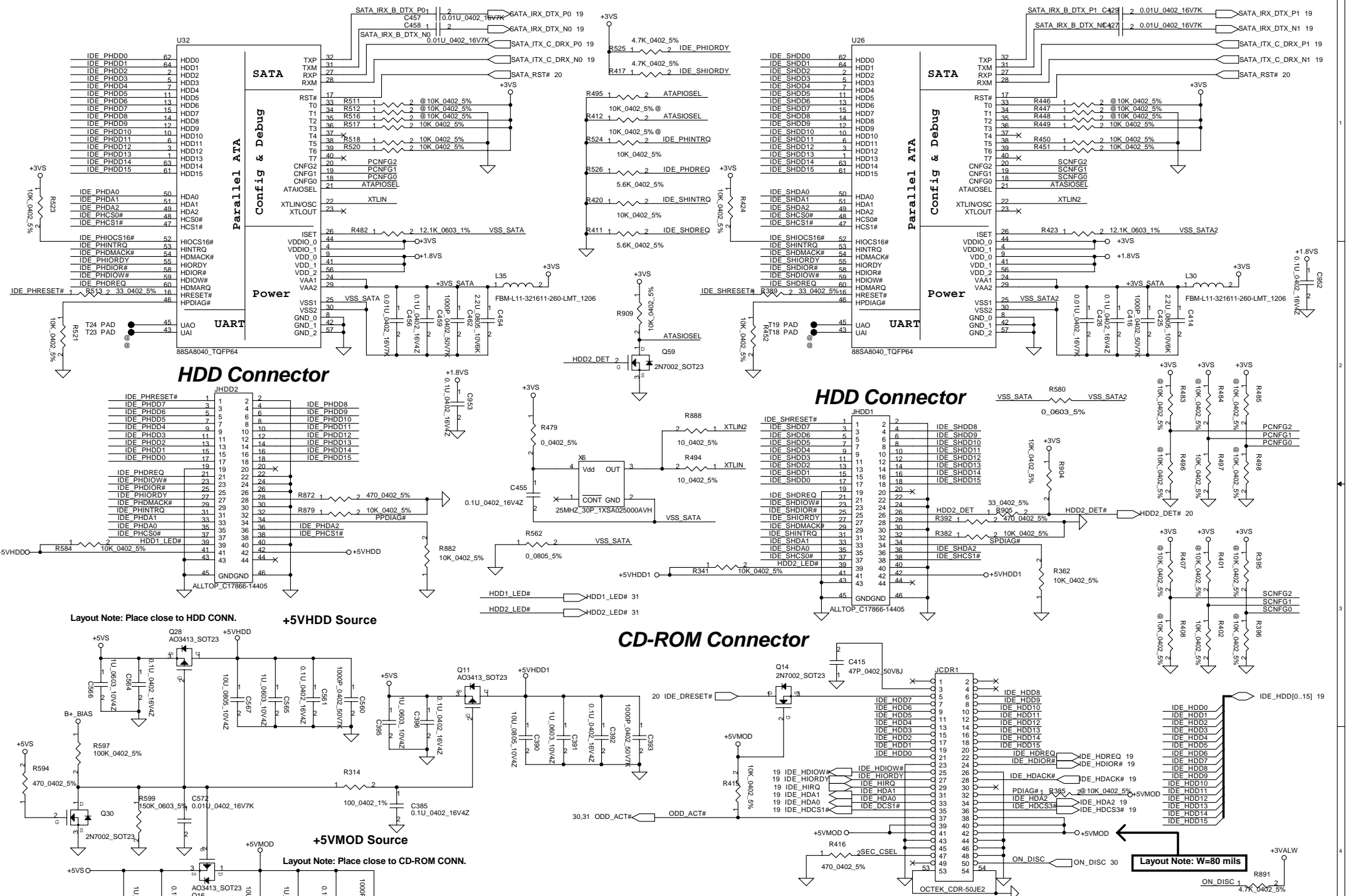
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Replacing by this circuit?

Note: Intel will update design guide.

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### HDD Connector

### HDD Connector

### CD-ROM Connector

Layout Note: Place close to HDD CONN.

**+5VHDD Source**

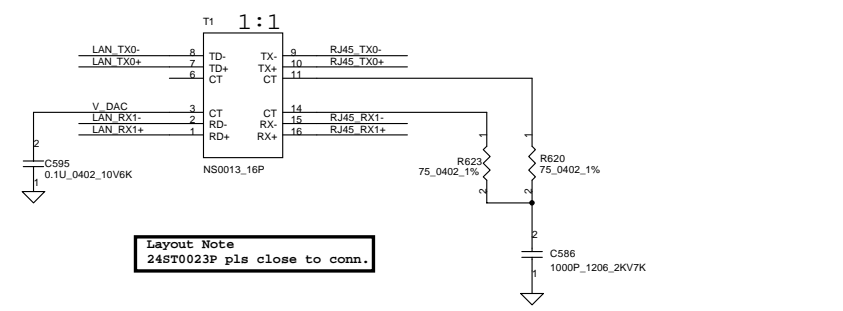
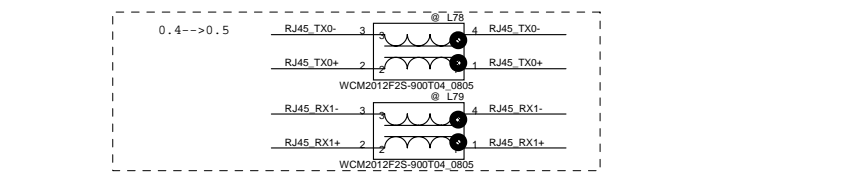
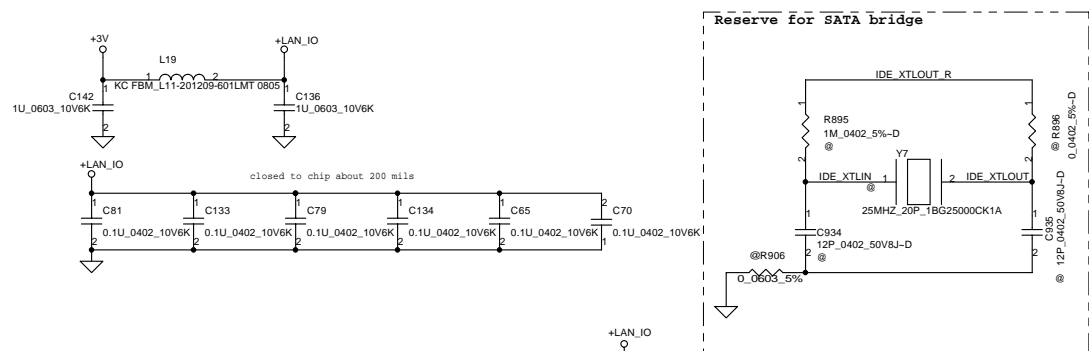
**+5VMOD Source**

Layout Note: Place close to CD-ROM CONN.

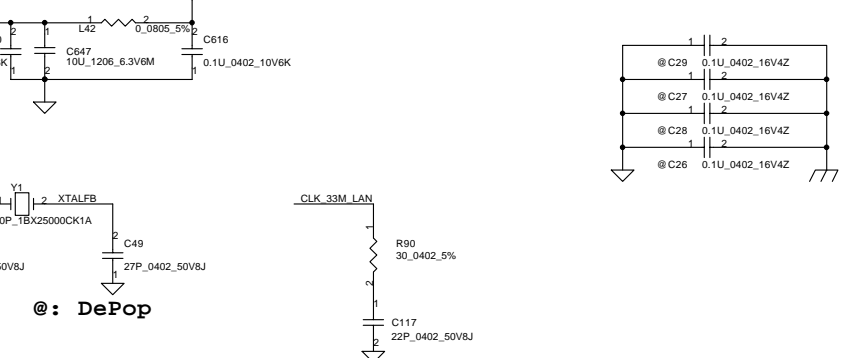
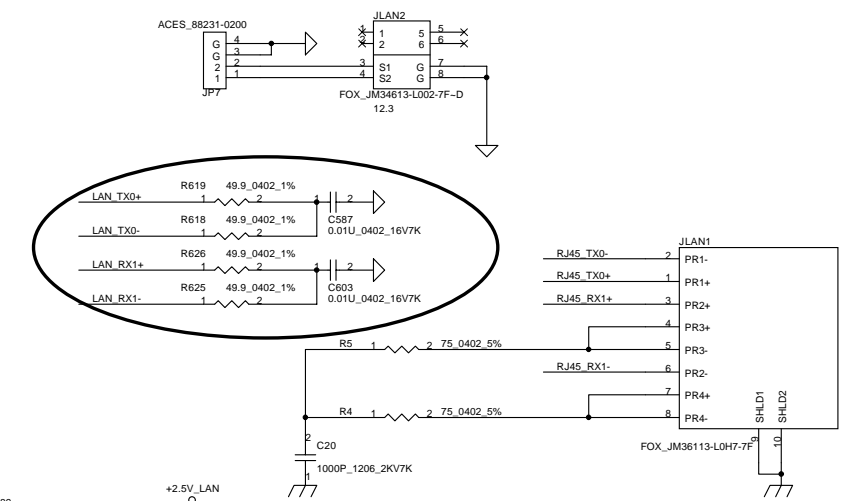
Layout Note: W=80 mils

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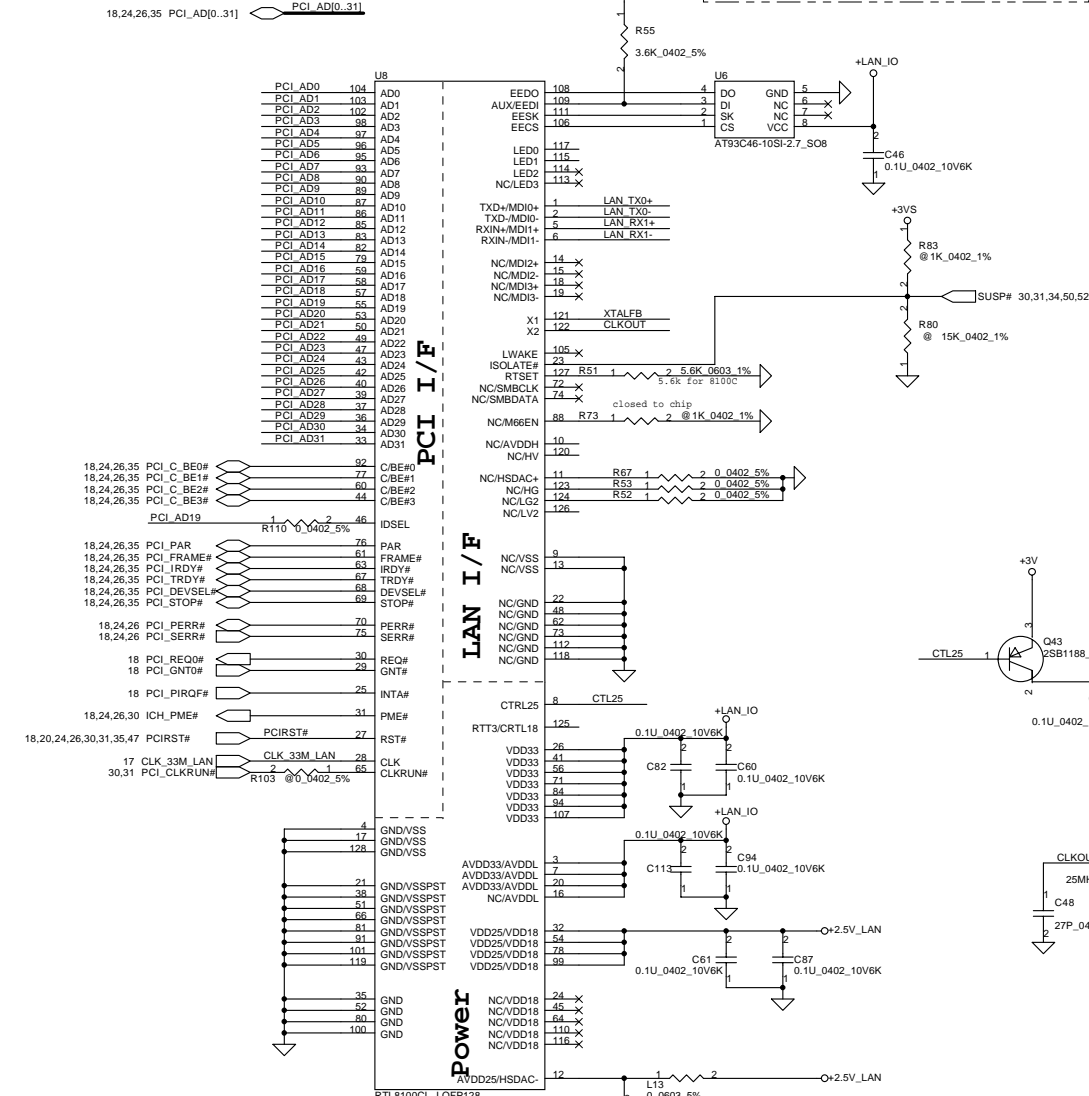
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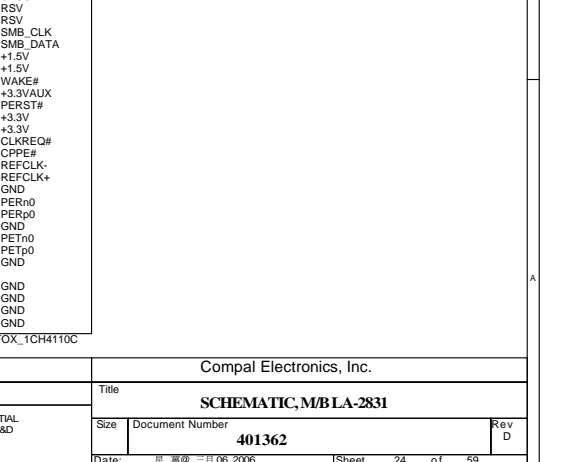
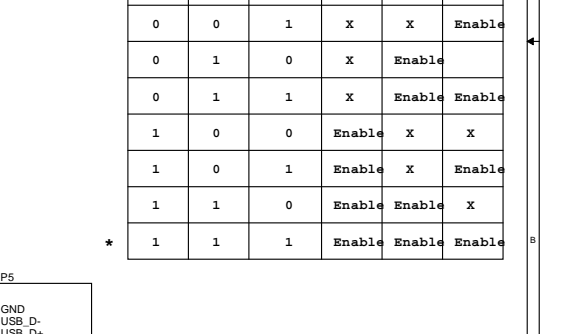
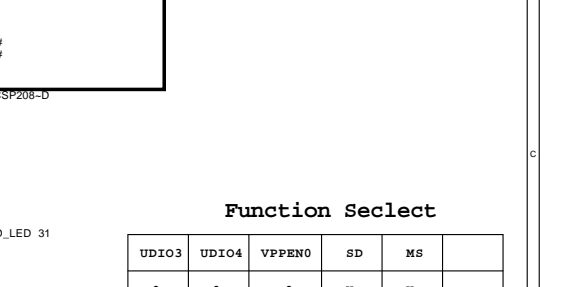
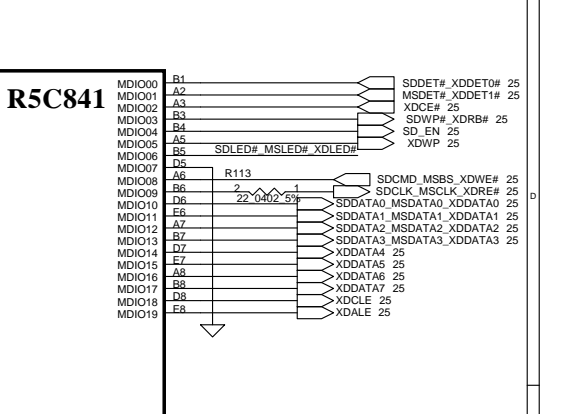
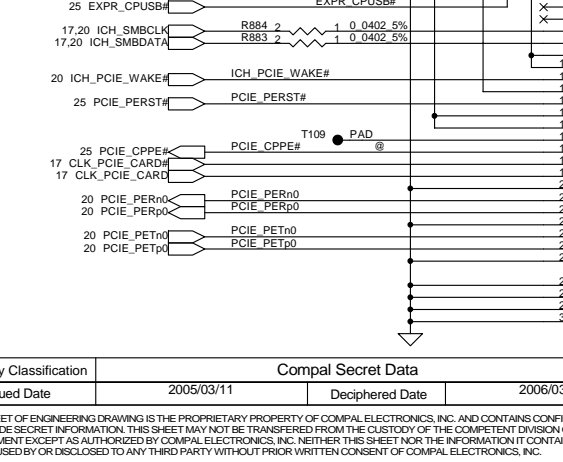
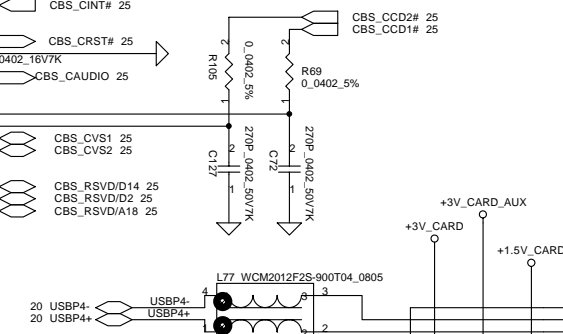
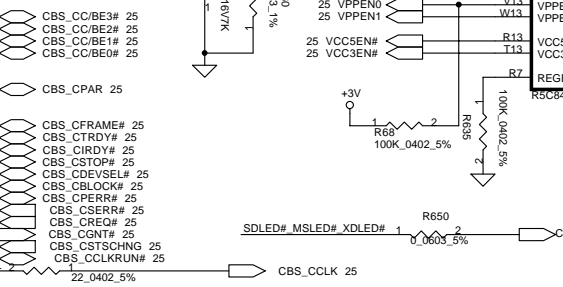
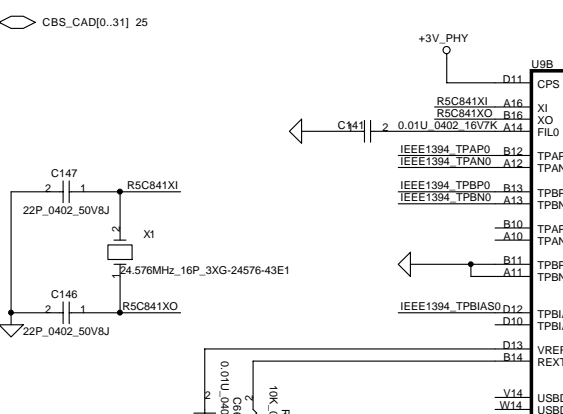
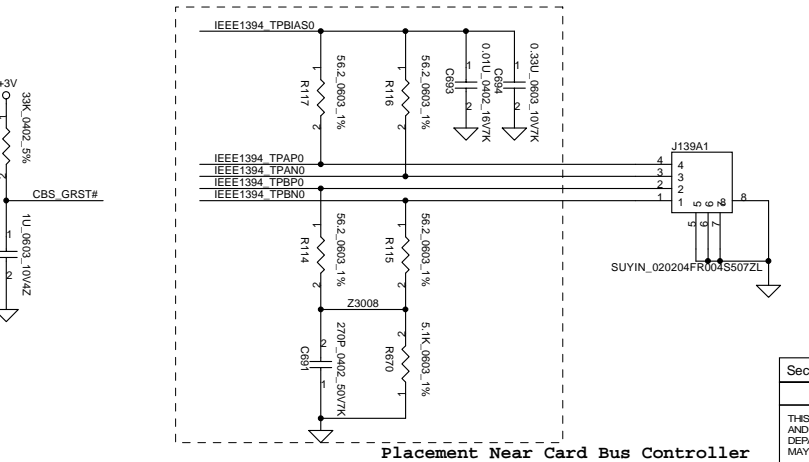
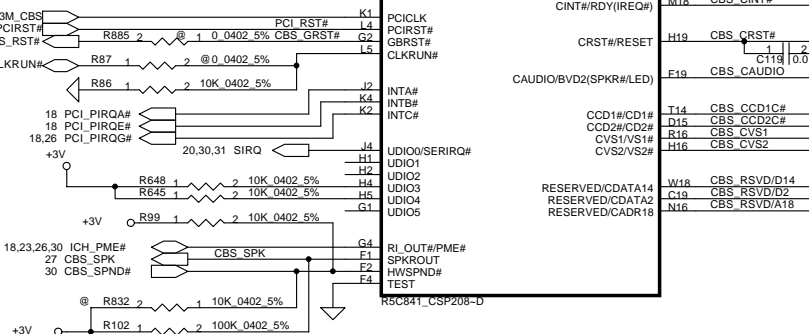
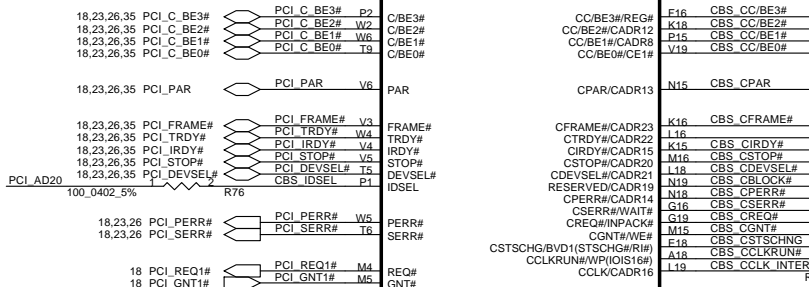
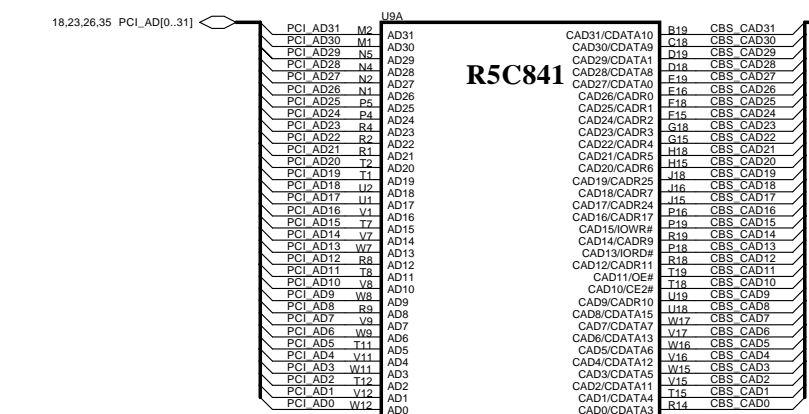
Layout Note  
245R0023P pls close to conn.



@: DePop



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**Function Select**

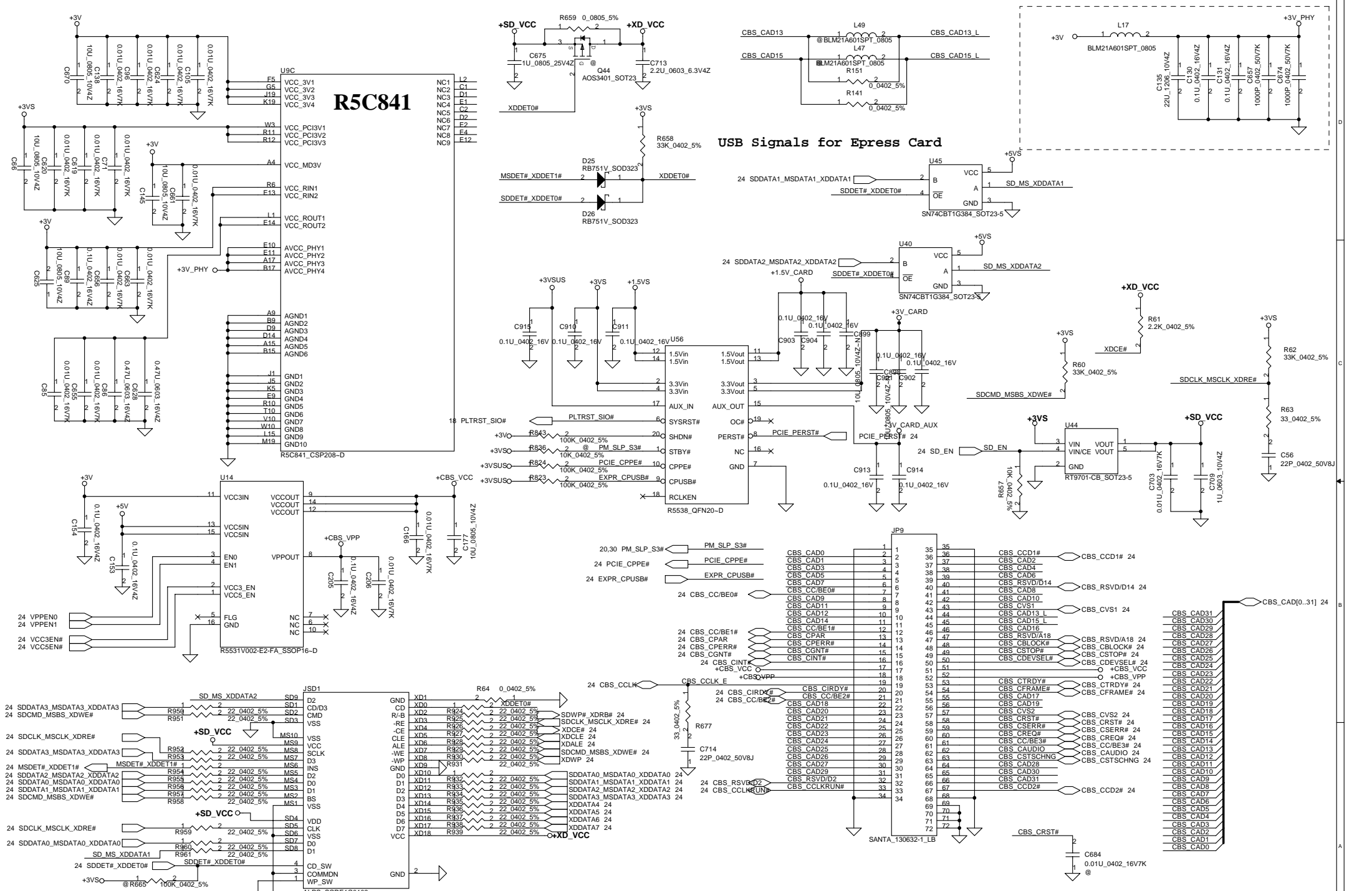
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0	0	1	X	X
0	1	0	X	Enable
0	1	1	X	Enable
1	0	0	Enable	X
1	0	1	Enable	X
1	1	0	Enable	Enable
1	1	1	Enable	Enable

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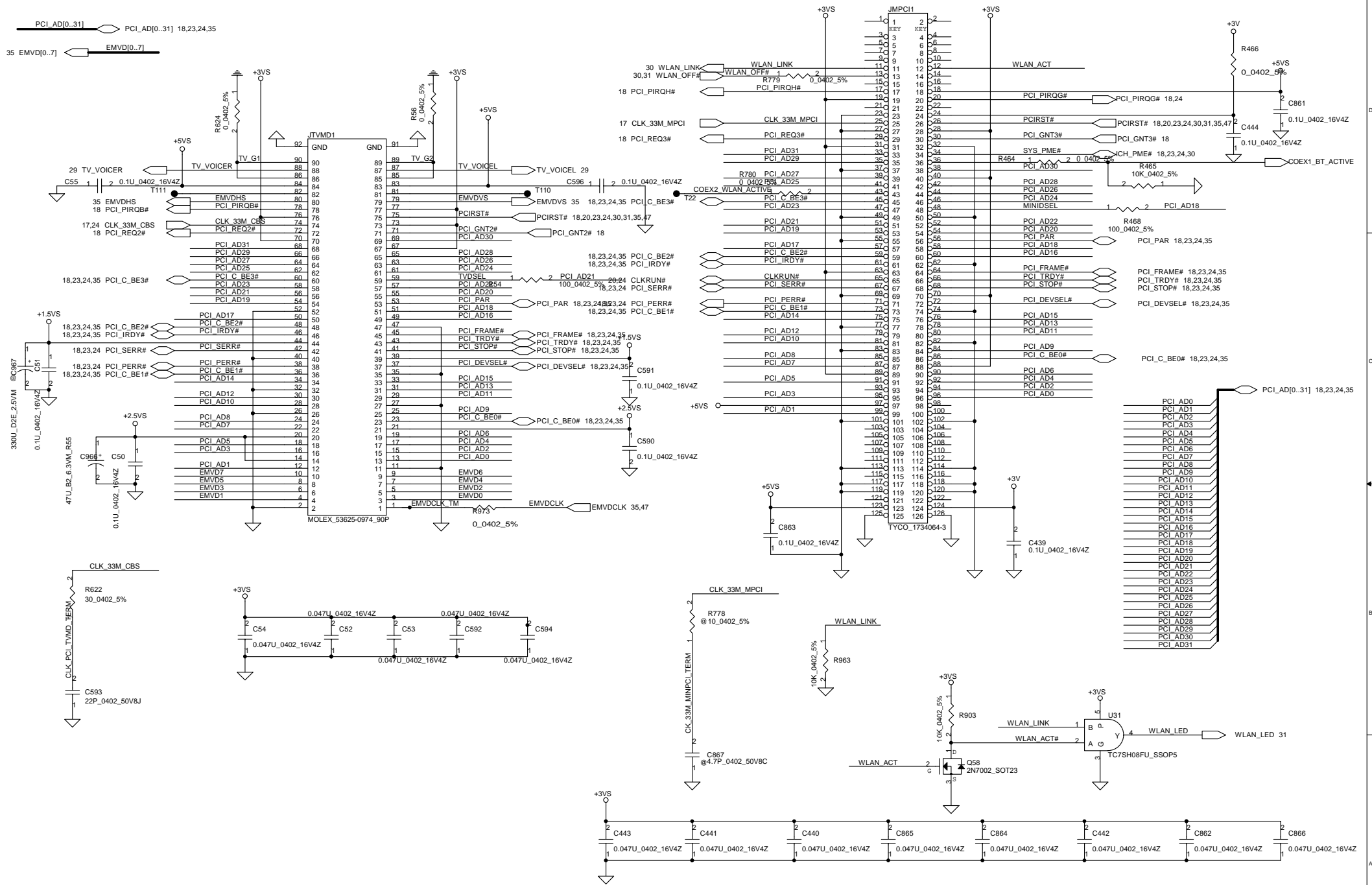




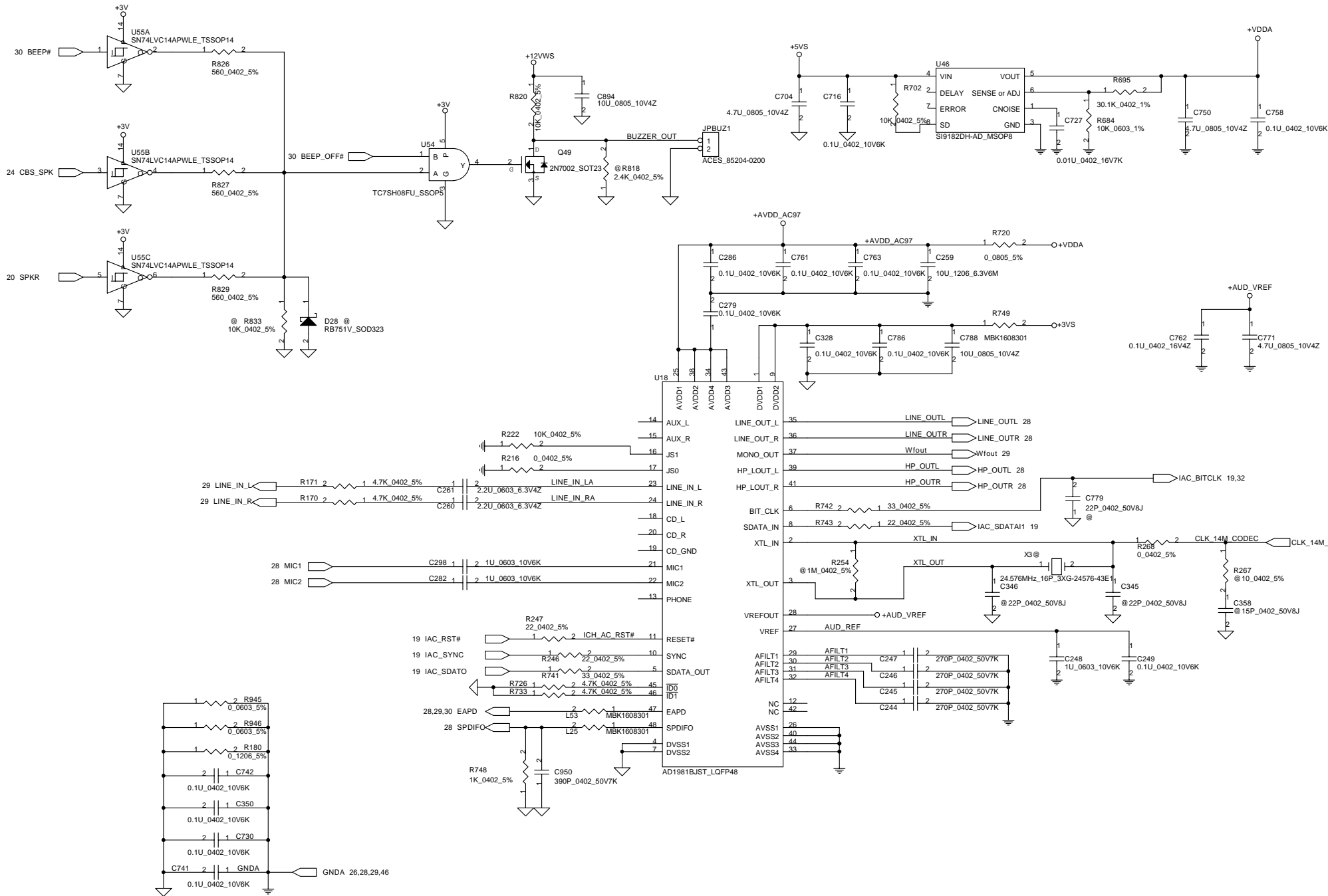
# R5C841

## USB Signals for Express Card

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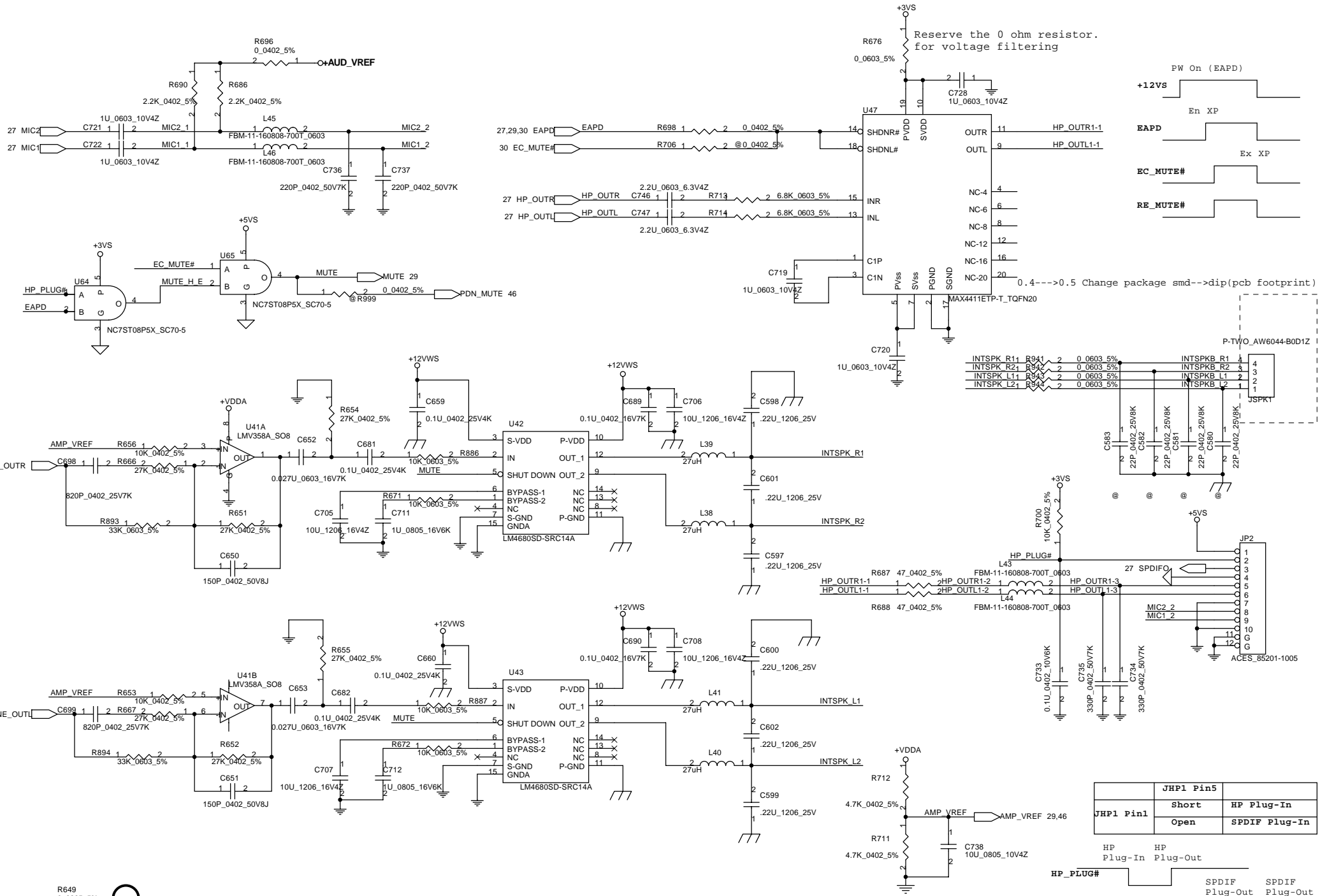


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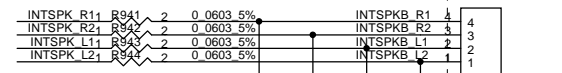
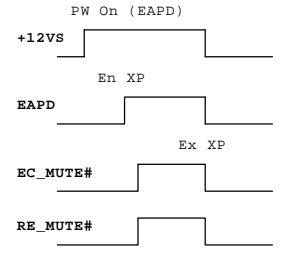


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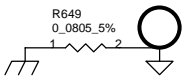
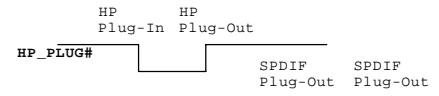
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Reserve the 0 ohm resistor.  
for voltage filtering



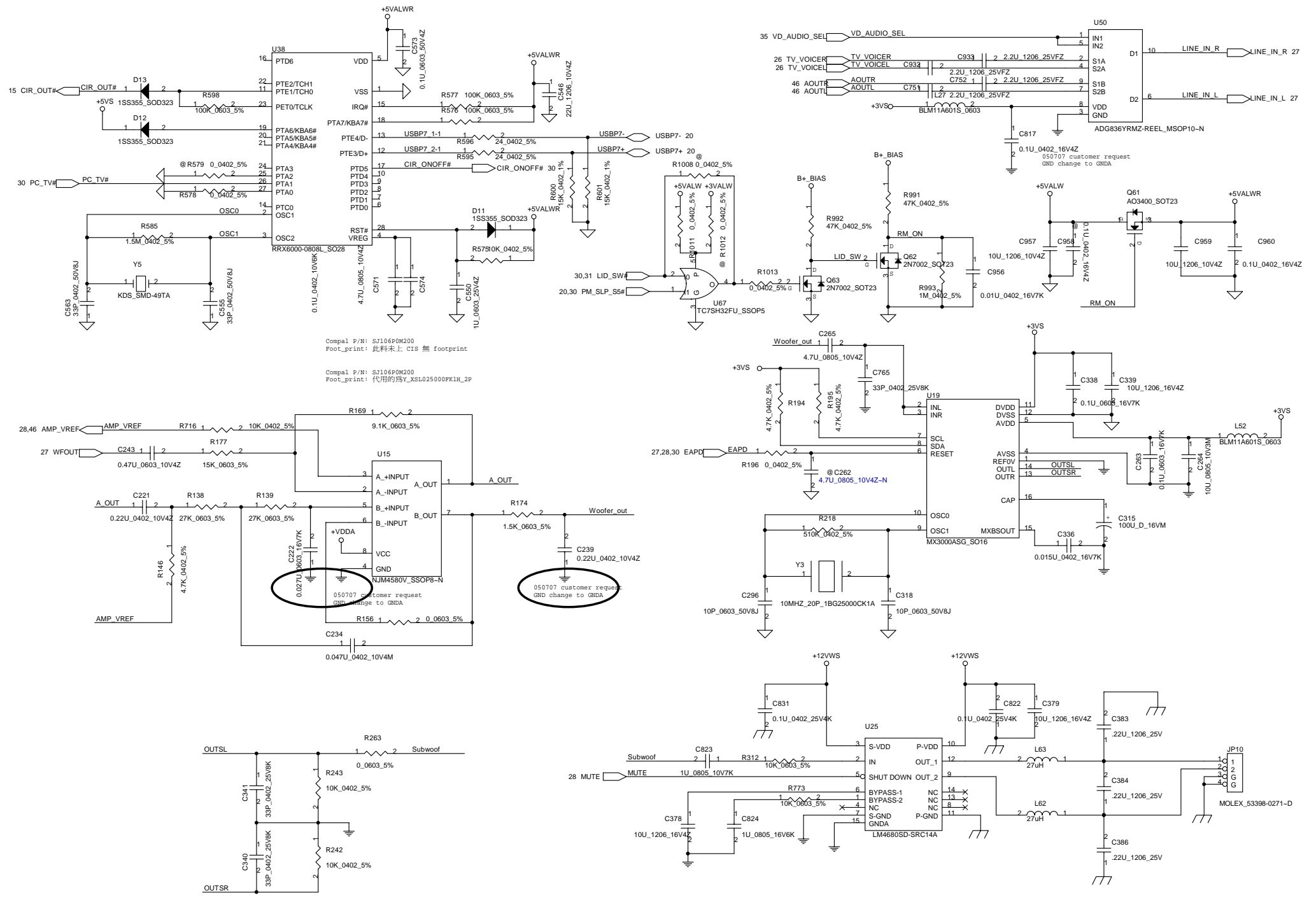
JHP1 Pin5	Short	HP Plug-In
JHP1 Pin1	Open	SPDIF Plug-In



Connect AMP\_GND to GND  
via one single point to  
HOLE close to Amplifier

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Compal P/N: SJ106PM200  
Foot\_print: 此料未上 CIS 無 footprint

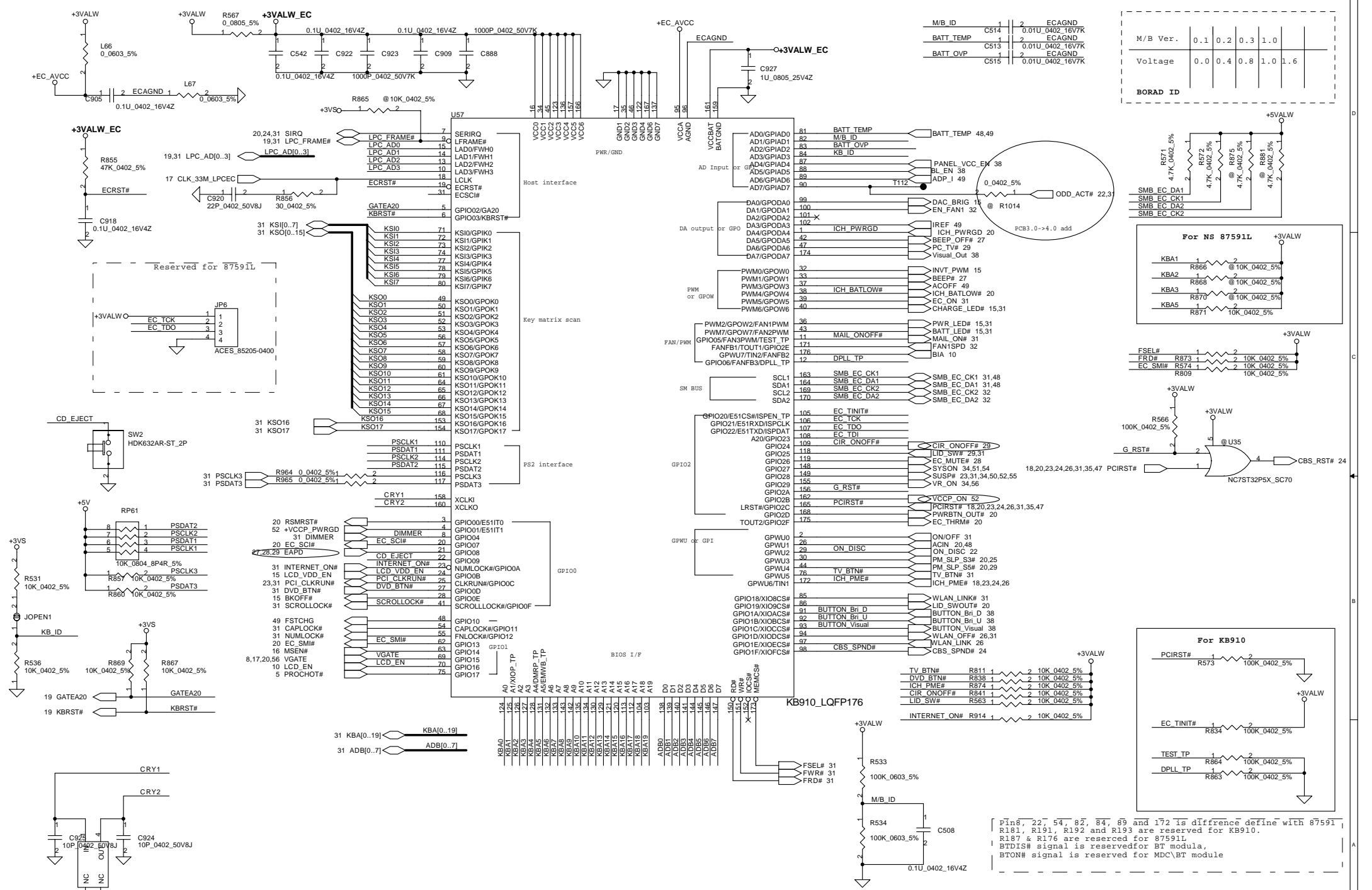
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050707 customer request  
GND change to GND4

050707 customer request  
GND change to GND4

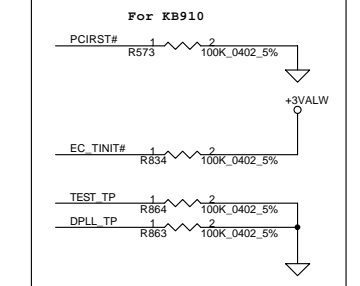
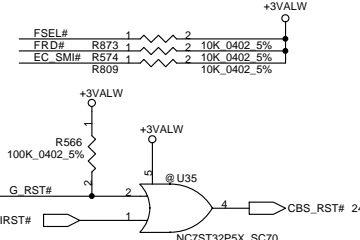
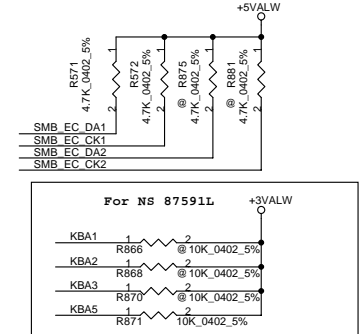
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M/B ID	C514	1	2	ECAGND
BATT_TEMP	C514	1	2	0.01U_0402_18V7K
BATT_OVP	C513	1	2	0.01U_0402_16V7K
	C515	1	2	0.01U_0402_16V7K

M/B Ver.	0.1	0.2	0.3	1.0	
Voltage	0.0	0.4	0.8	1.0	1.6
<b>BORAD ID</b>					



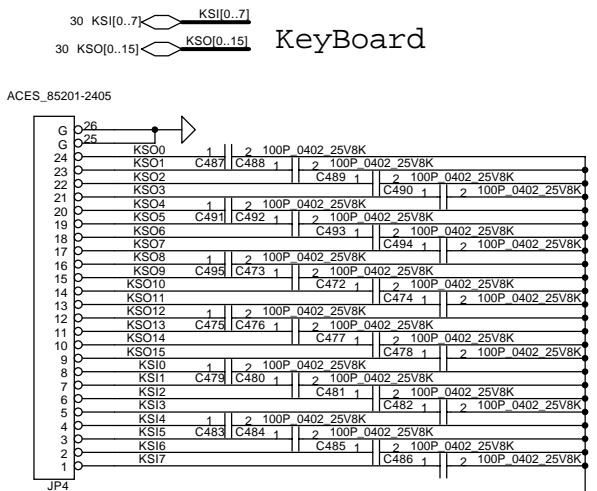
Pin8, 22, 54, 82, 84, 89 and 172 is difference define with 87591L  
 R181, R191, R192 and R193 are reserved for KB910.  
 R187 & R176 are reserved for 87591L  
 BTDIS# signal is reserved for BT module,  
 BTON# signal is reserved for MDC\BT module

Y6  
 32.768KHZ\_1TJS125BJA251

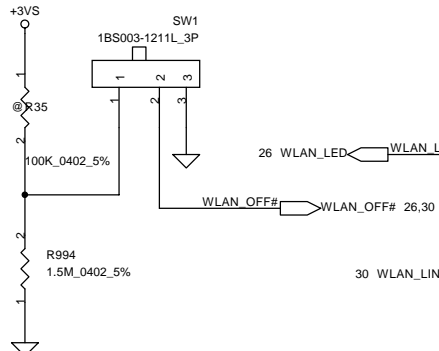
Close to RTC pad

JOPEN2 close to DDR-SODIMM

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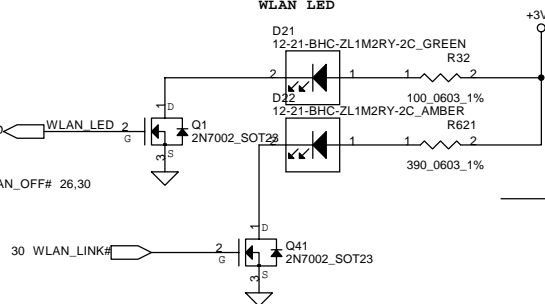


### Killer switch

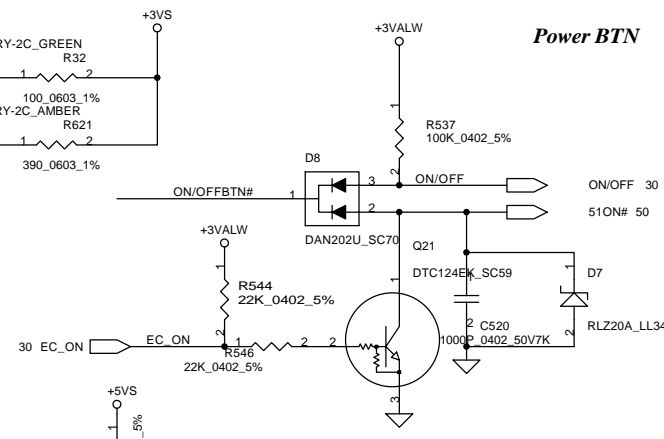


### D1 Pin3 Open PAST & MASK layer

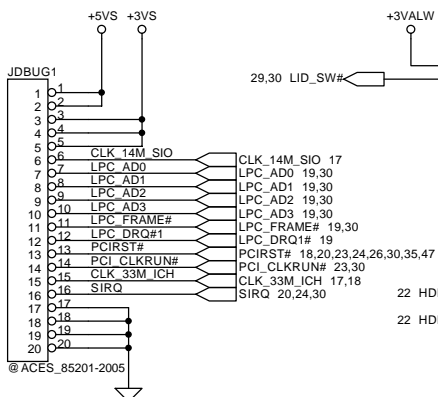
#### WLAN LED



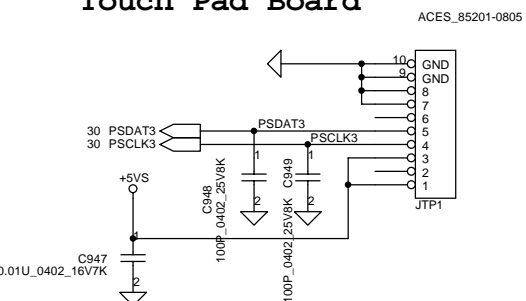
### Power BTN



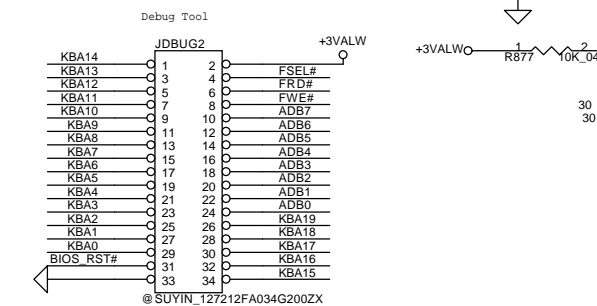
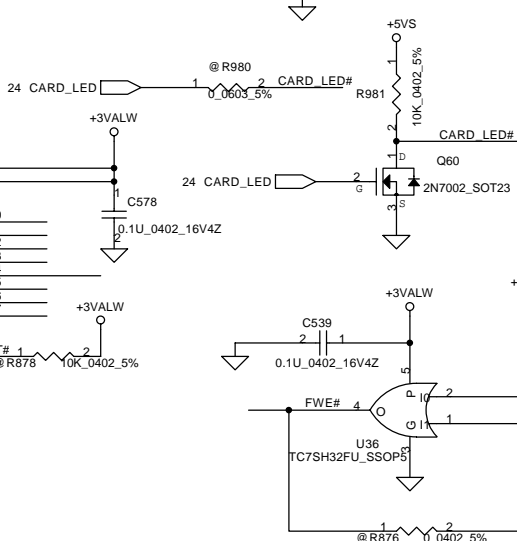
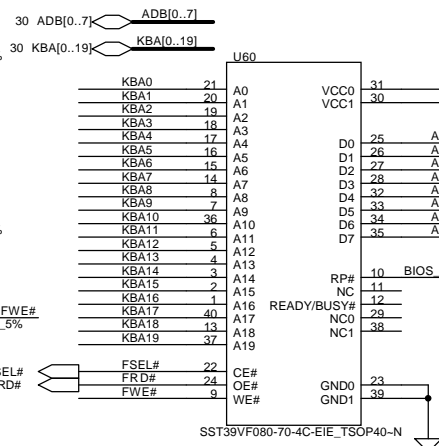
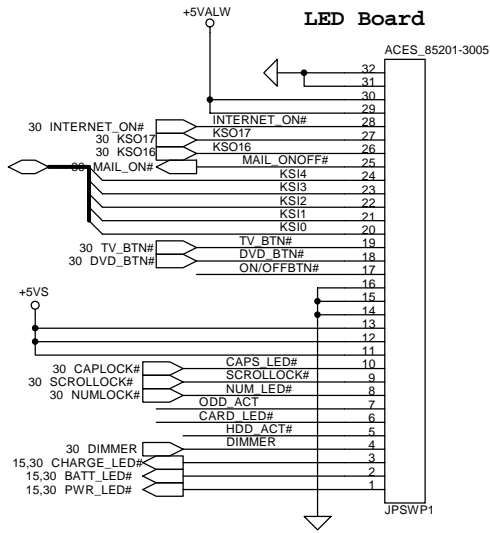
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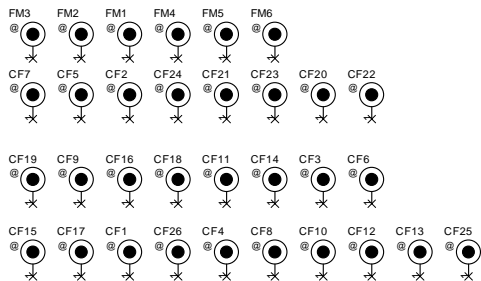
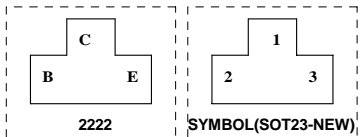
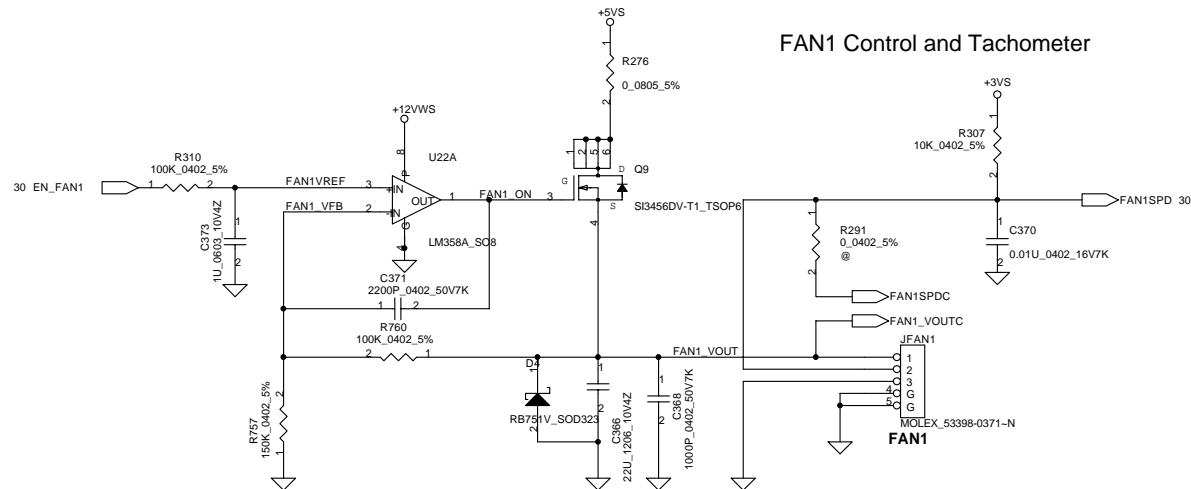
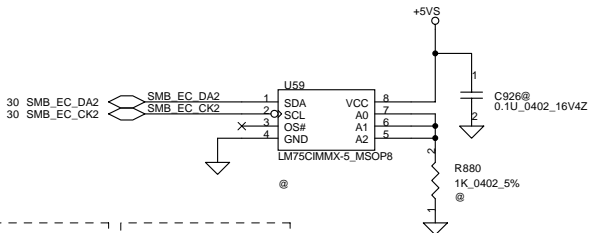
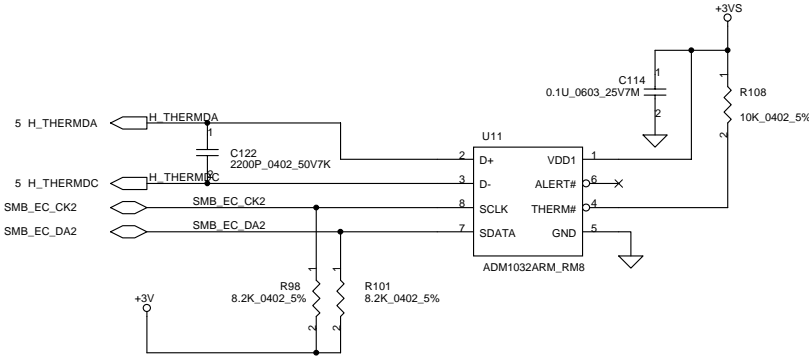
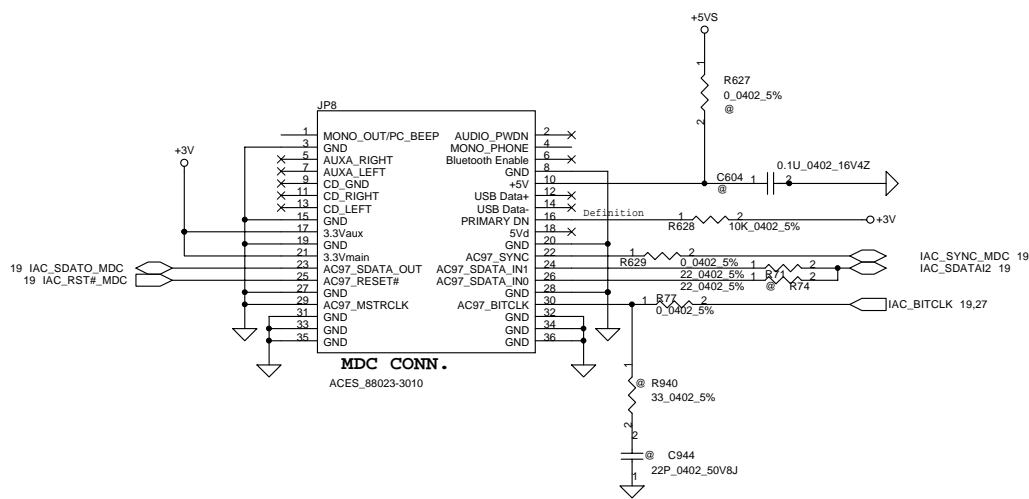
### Touch Pad Board



### LED Board

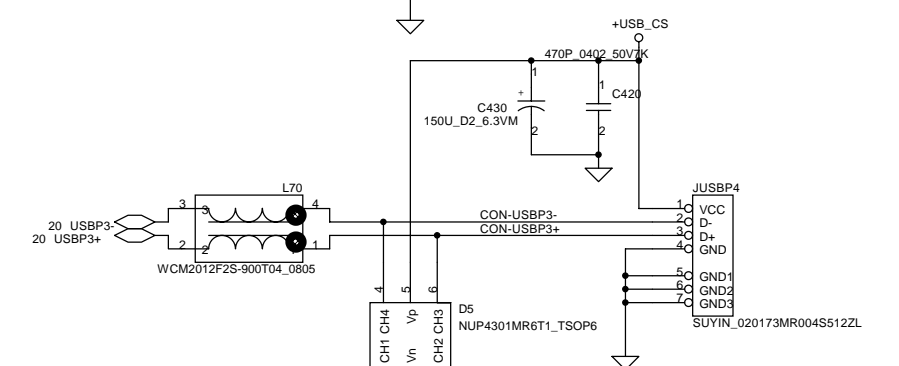
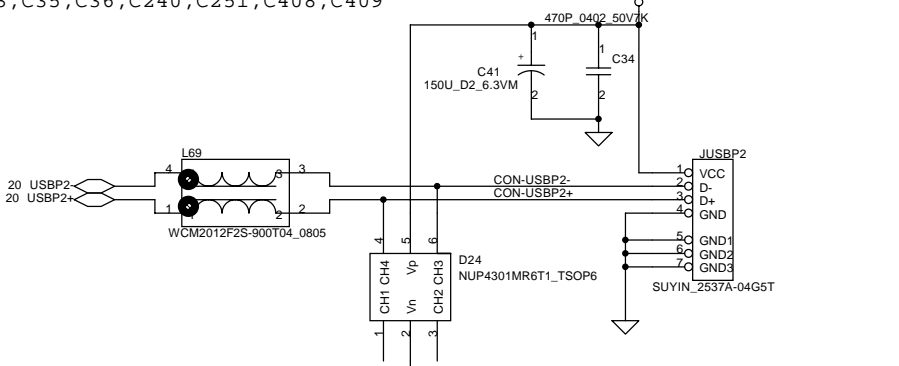
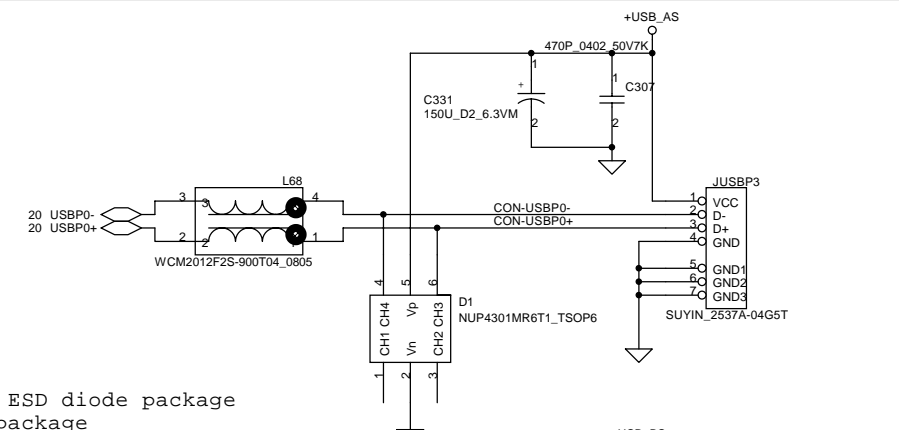
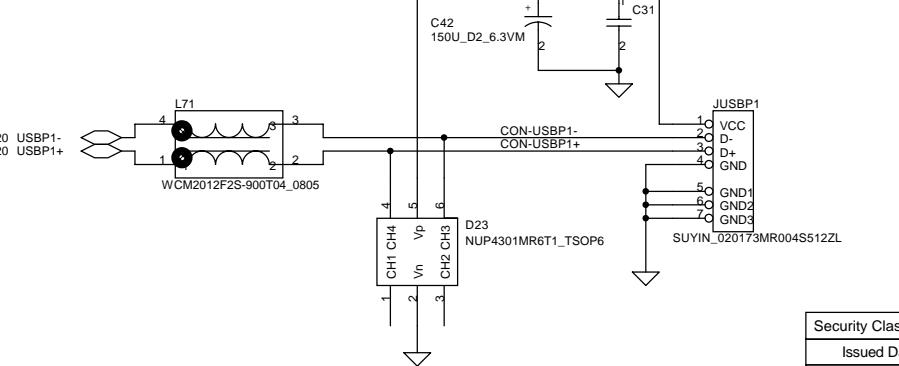
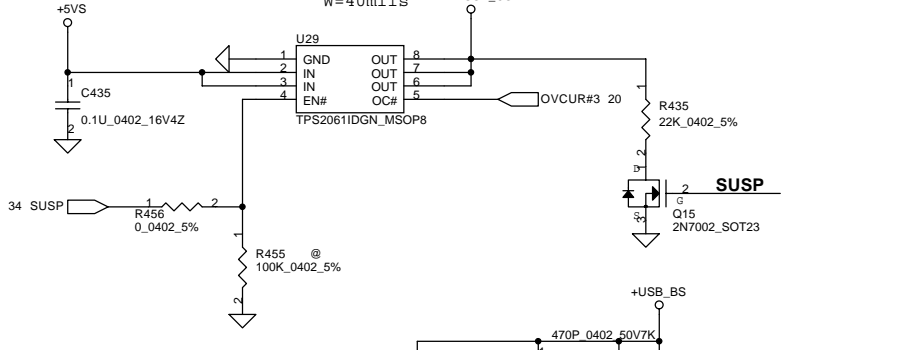
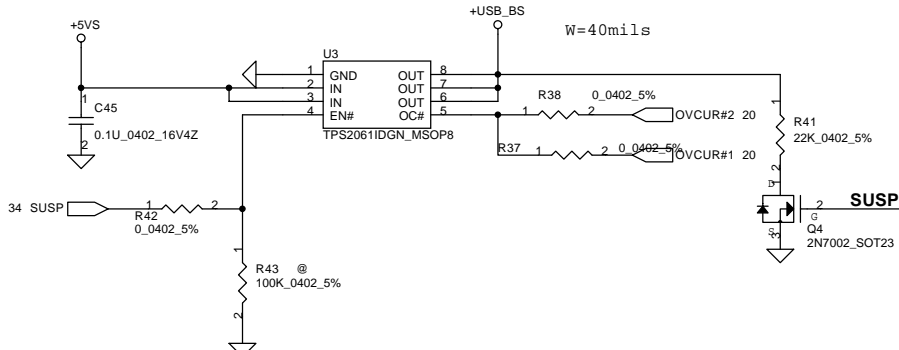
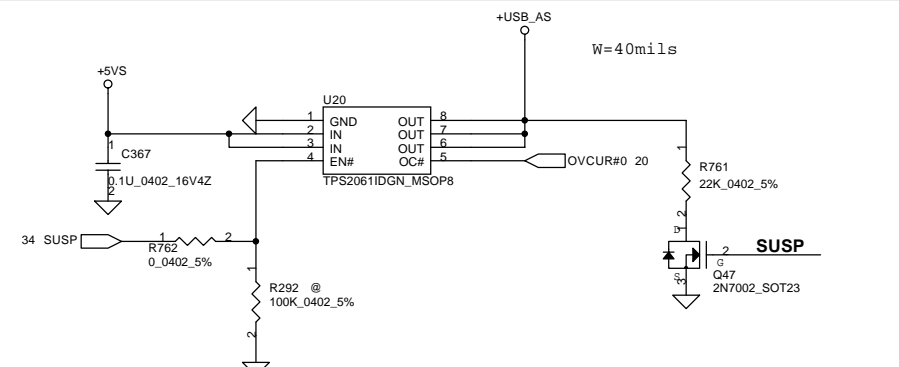


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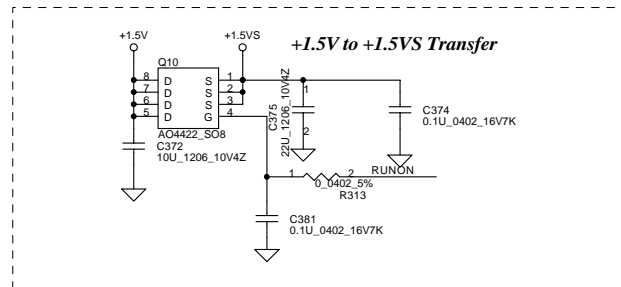
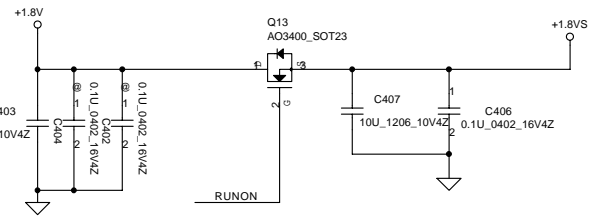
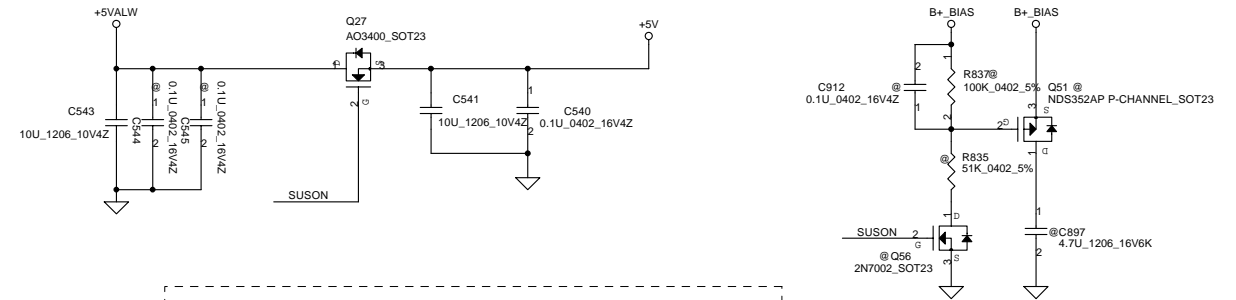
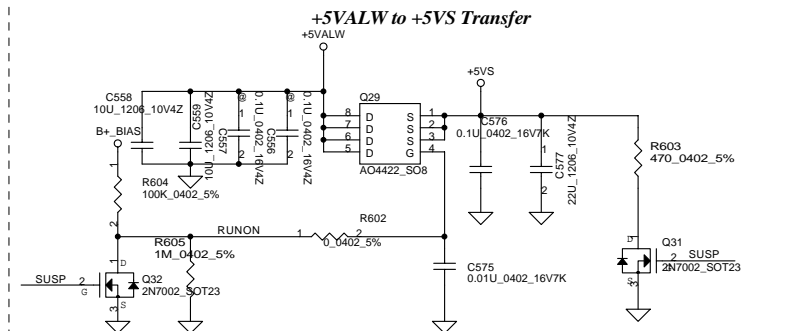
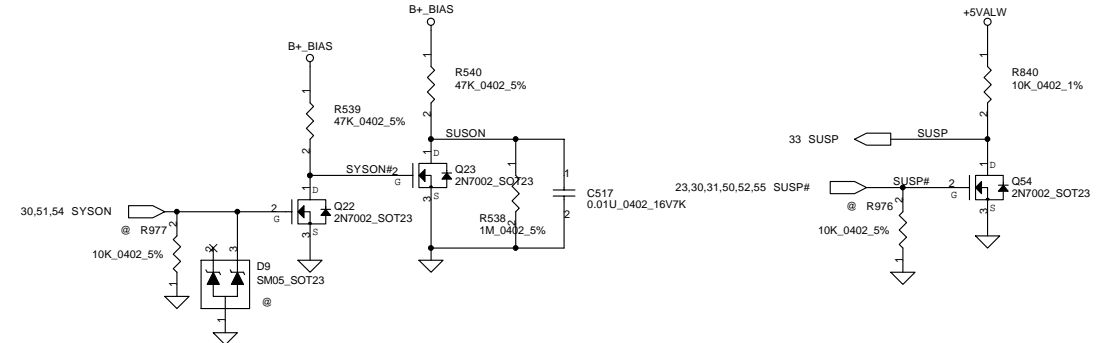
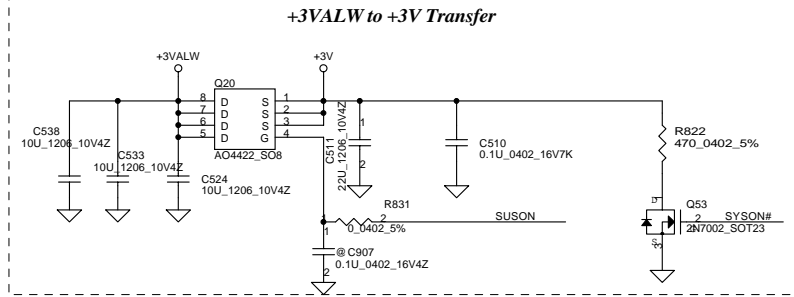
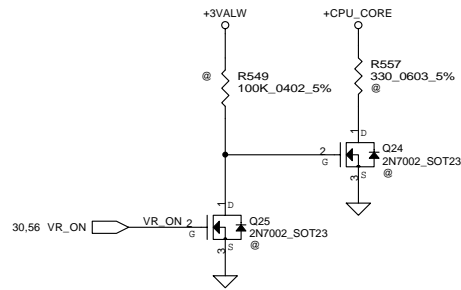
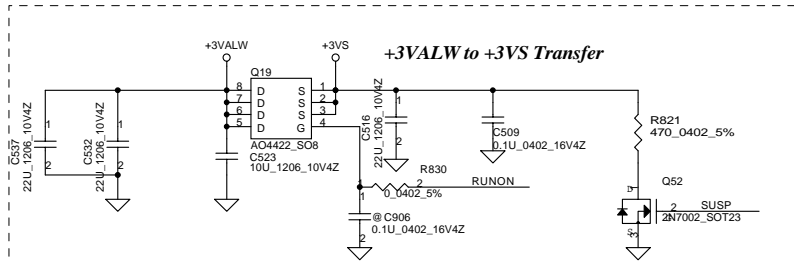
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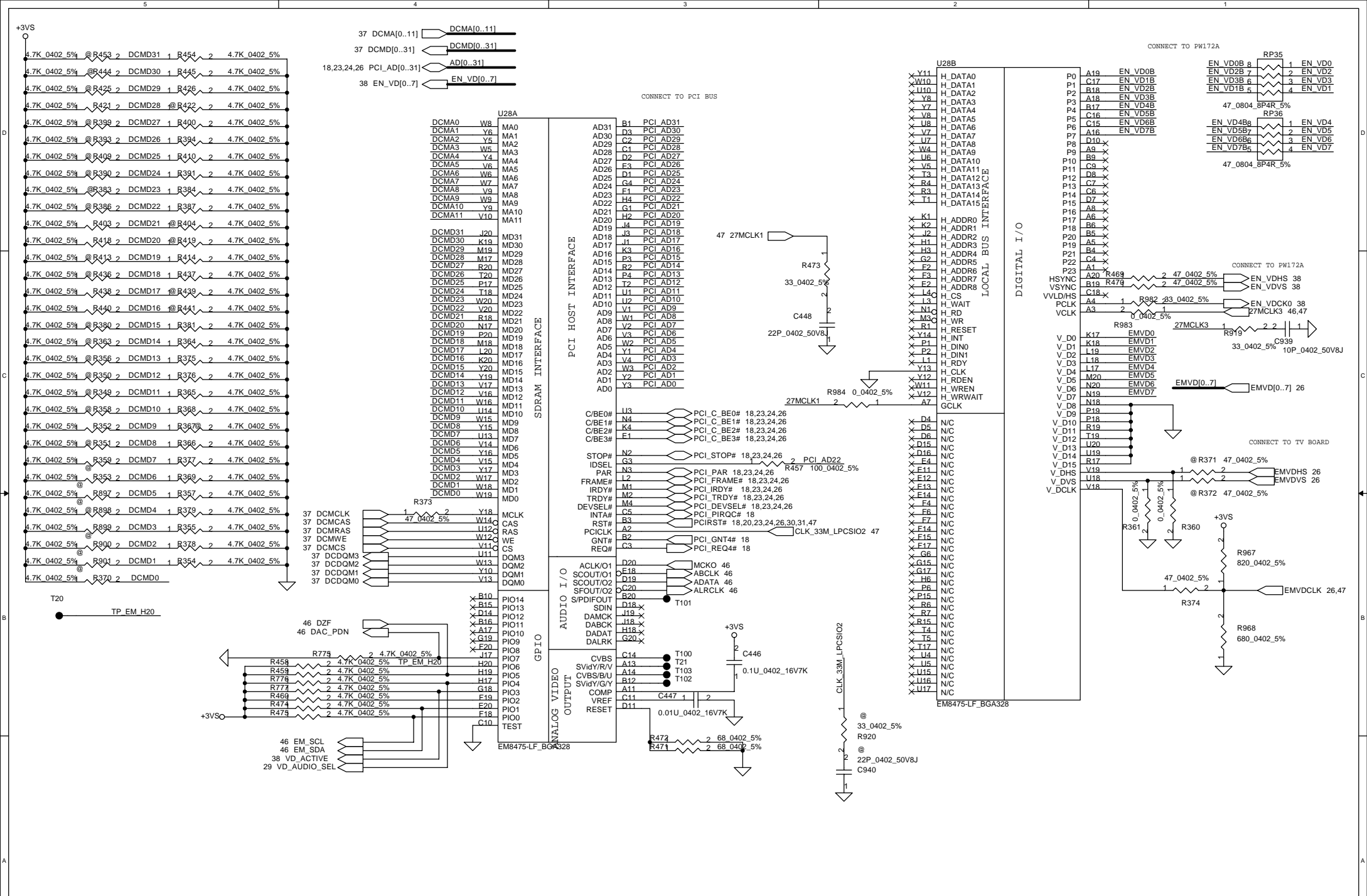
0.4--->0.5 Change USB ESD diode package  
 Change D1,D5,D23,D24 package  
 Remove 10P-NI C32,C33,C35,C36,C240,C251,C408,C409

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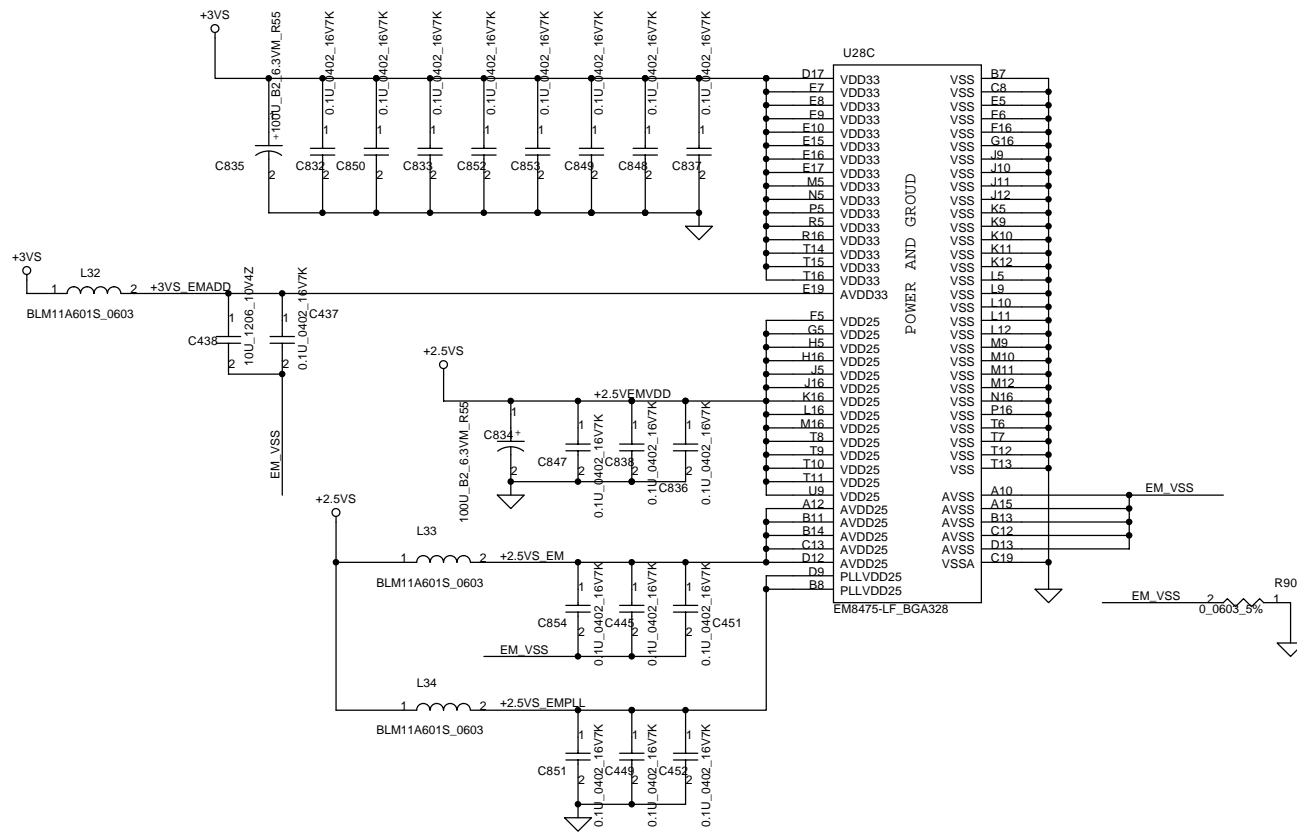


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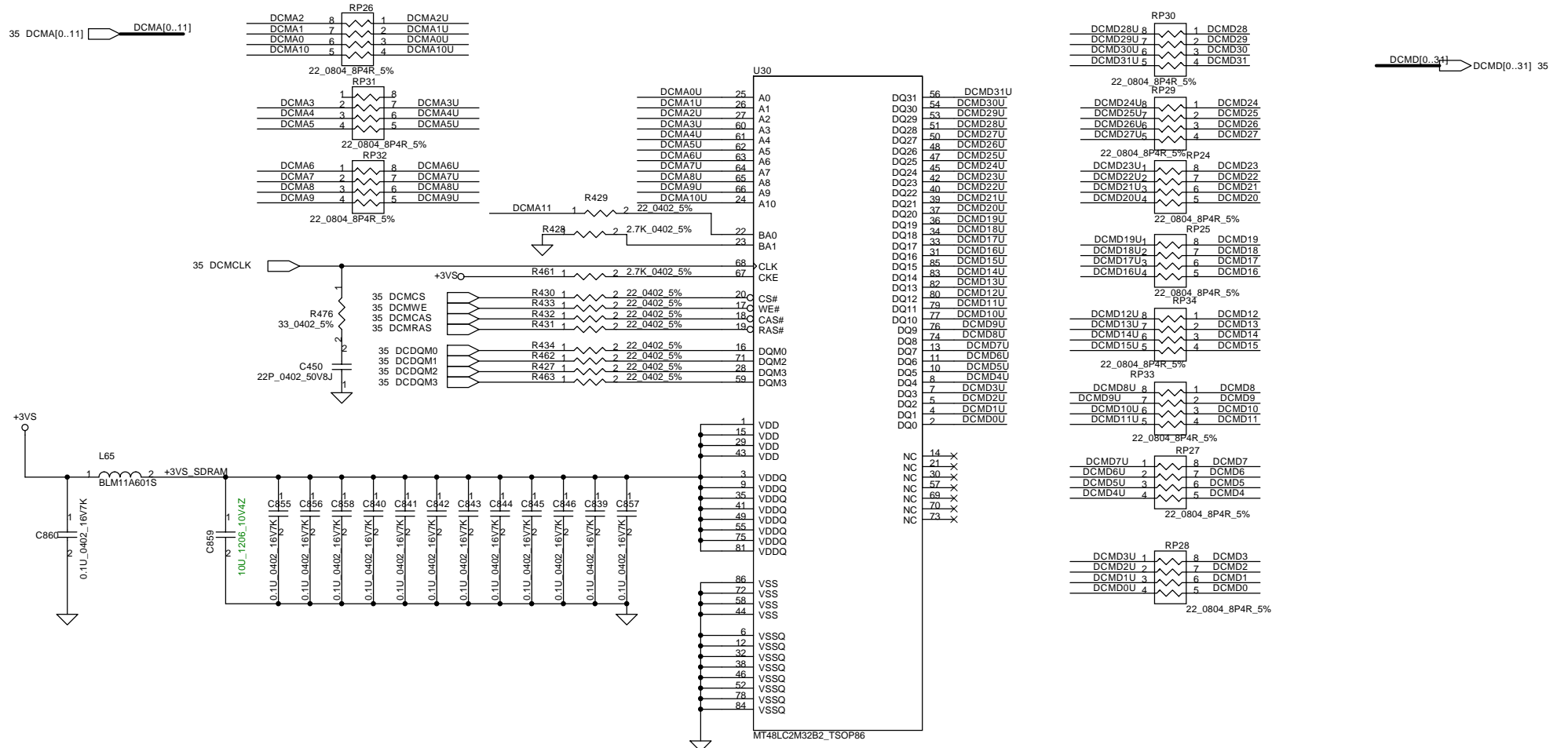
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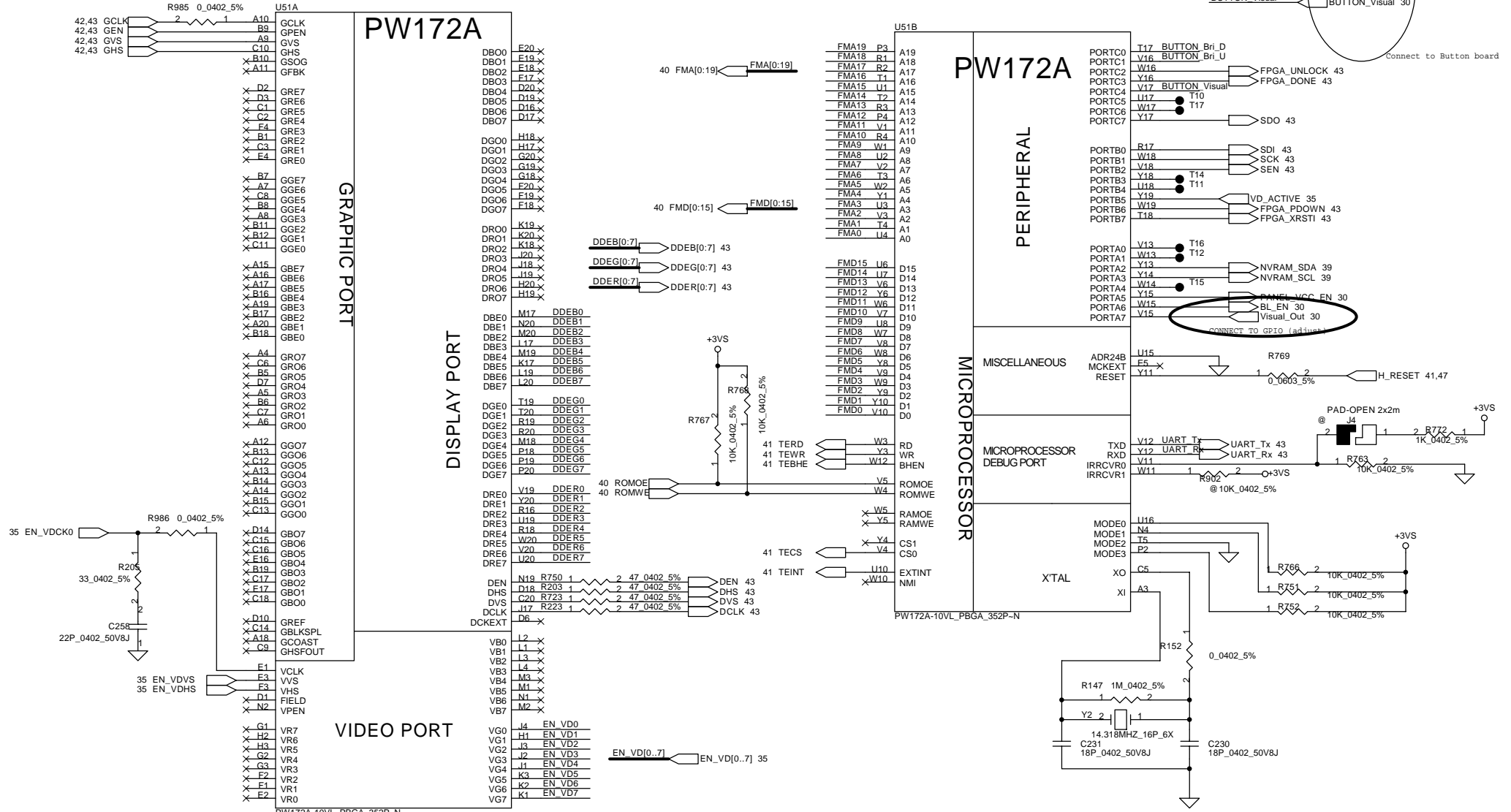
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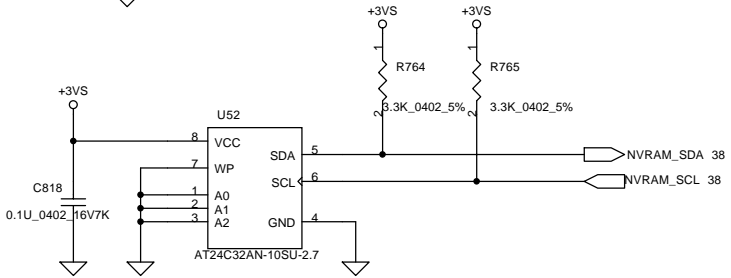
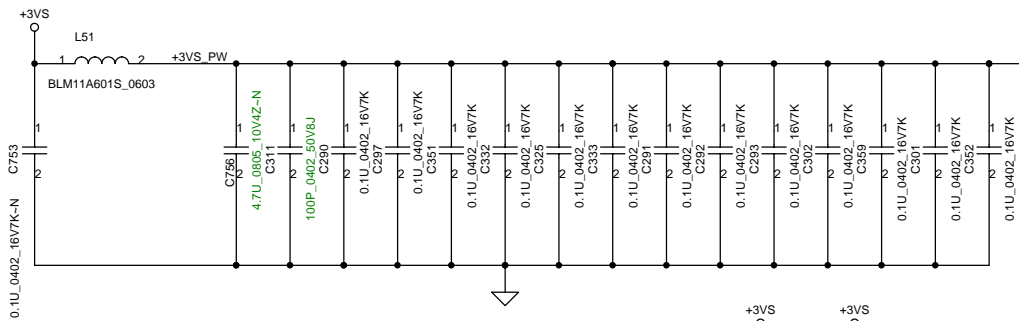
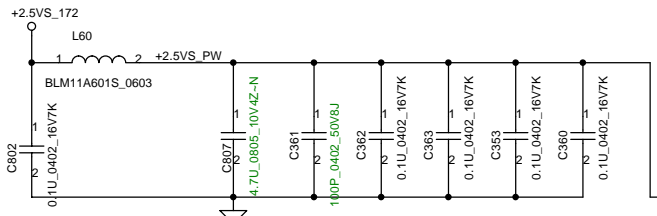
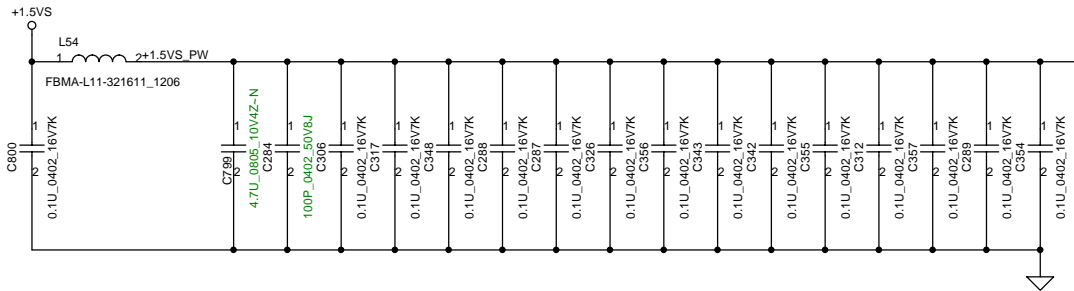
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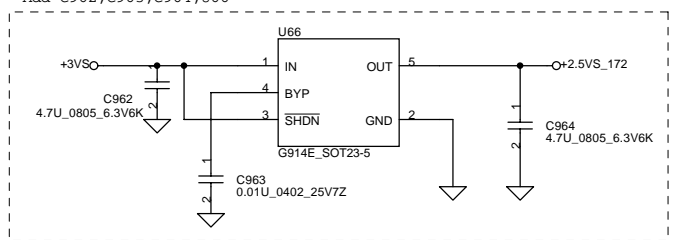
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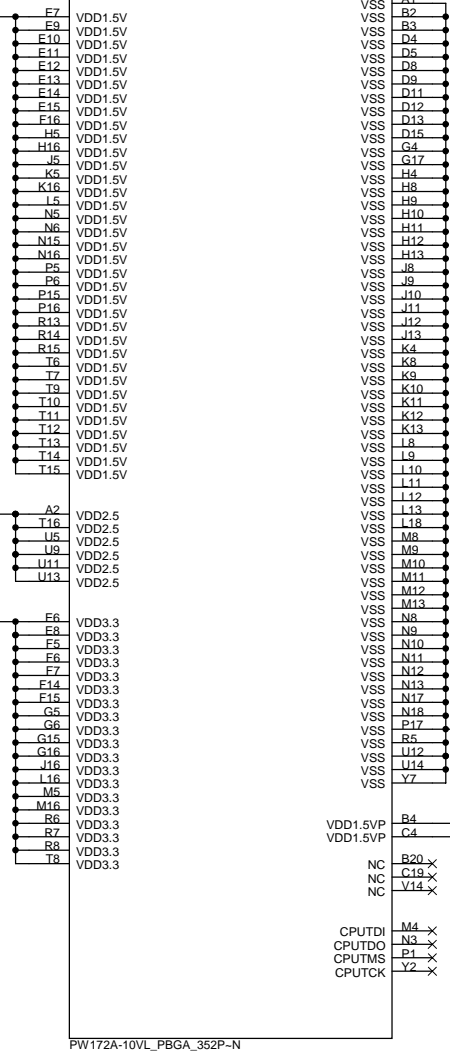
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0.4---->0.5 Improve power sequence  
Add C962, C963, C964, U66



# PW172A



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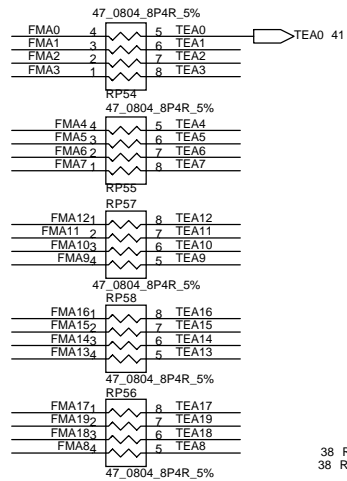
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38 FMA[0..19]

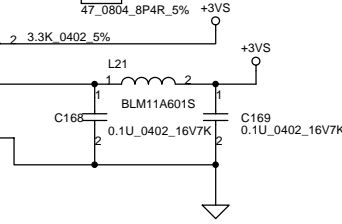
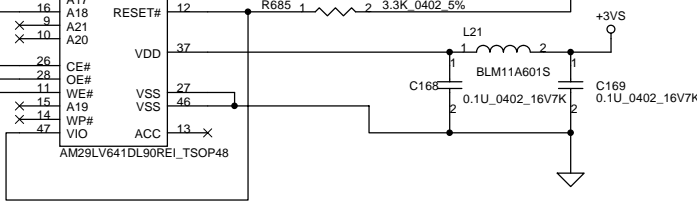
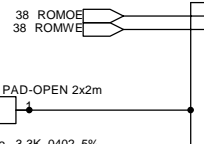
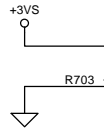
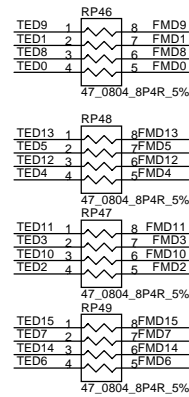
TEA[1..7]

TED[0..15]

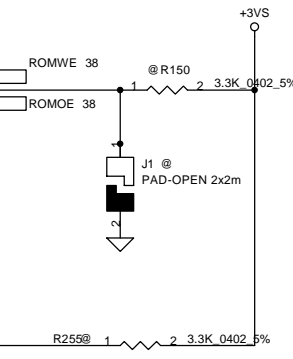
FMD[0..15]



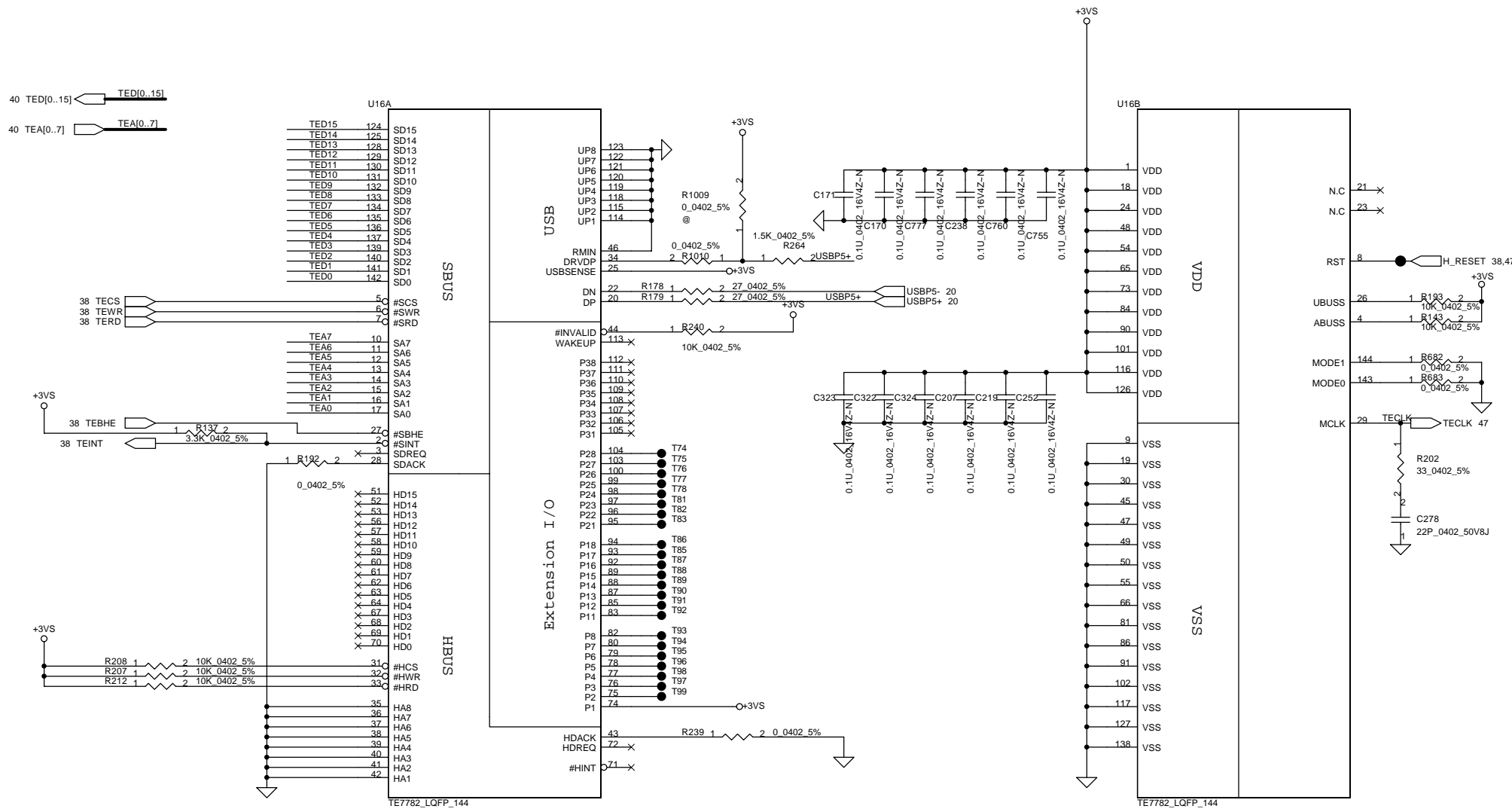
U49			
TEA1	25	A0	DQ0
TEA2	24	A1	DQ1
TEA3	23	A2	DQ2
TEA4	22	A3	DQ3
TEA5	21	A4	DQ4
TEA6	20	A5	DQ5
TEA7	19	A6	DQ6
TEA8	18	A7	DQ7
TEA9	8	A8	DQ8
TEA10	7	A9	DQ9
TEA11	6	A10	DQ10
TEA12	5	A11	DQ11
TEA13	4	A12	DQ12
TEA14	3	A13	DQ13
TEA15	2	A14	DQ14
TEA16	1	A15	DQ15/A-1
TEA17	17	A16	
TEA18	16	A17	
TEA19	15	A18	
	9	A19	
	10	A20	



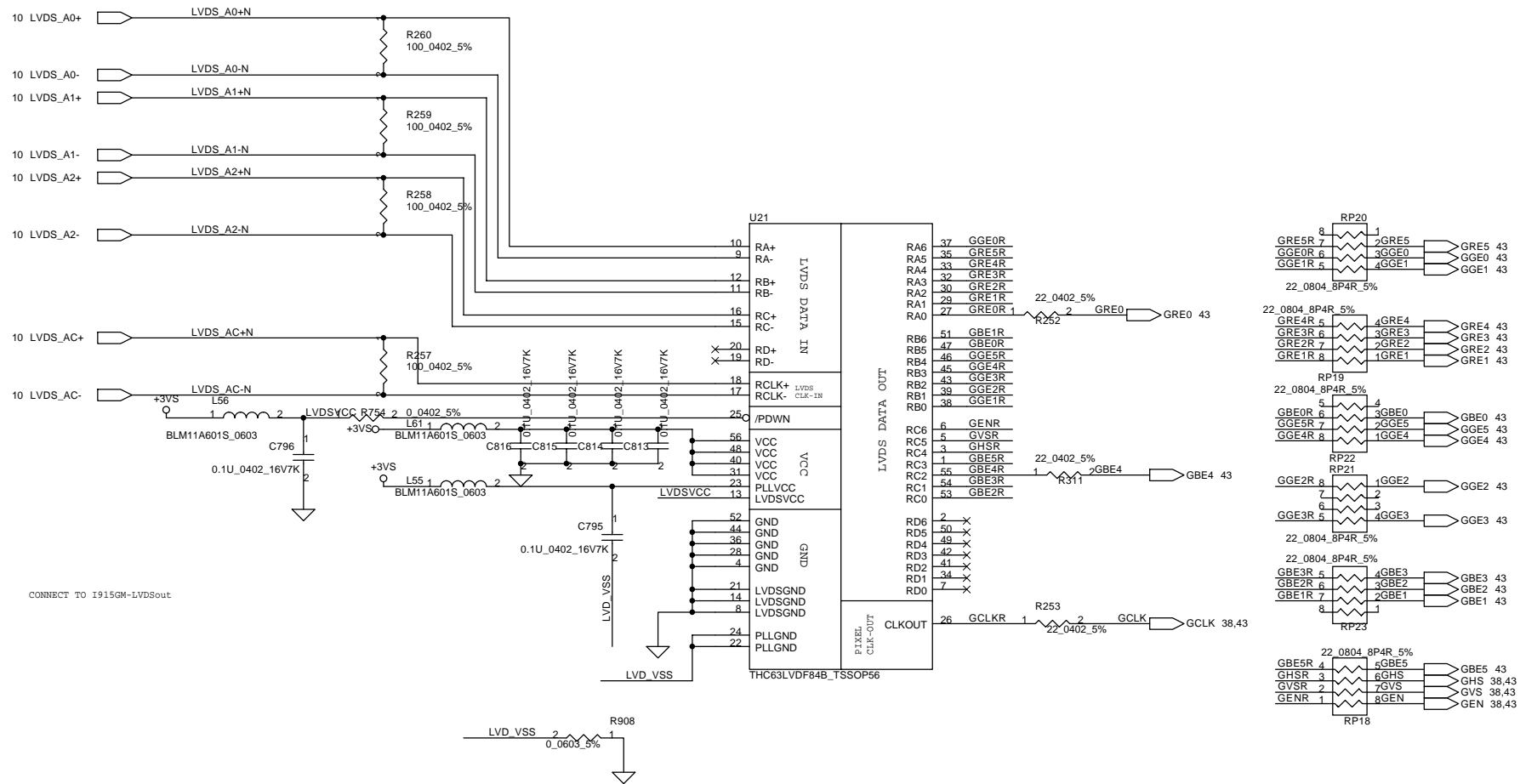
ROMWE		ROMOE	
38	ROMWE	38	ROMOE
1	@ R163	22	0402 5%
2	@ R164	22	0402 5%
3	@ R165	22	0402 5%
4	@ R166	22	0402 5%
5	@ R167	22	0402 5%
6	@ R168	22	0402 5%
7	@ R169	22	0402 5%
8	@ R170	22	0402 5%
9	@ R171	22	0402 5%
10	@ R172	22	0402 5%
11	@ R173	22	0402 5%
12	@ R174	22	0402 5%
13	@ R175	22	0402 5%
14	@ R176	22	0402 5%
15	@ R177	22	0402 5%
16	@ R178	22	0402 5%
17	@ R179	22	0402 5%
18	@ R180	22	0402 5%
19	@ R181	22	0402 5%
20	@ R182	22	0402 5%
21	@ R183	22	0402 5%
22	@ R184	22	0402 5%
23	@ R185	22	0402 5%
24	@ R186	22	0402 5%
25	@ R187	22	0402 5%
26	@ R188	22	0402 5%
27	@ R189	22	0402 5%
28	@ R190	22	0402 5%
29	@ R191	22	0402 5%
30	@ R192	22	0402 5%
31	@ R193	22	0402 5%
32	@ R194	22	0402 5%
33	@ R195	22	0402 5%
34	@ R196	22	0402 5%
35	@ R197	22	0402 5%
36	@ R198	22	0402 5%
37	@ R199	22	0402 5%
38	@ R200	22	0402 5%
39	@ R201	22	0402 5%
40	@ R202	22	0402 5%
41	@ R203	22	0402 5%
42	@ R204	22	0402 5%
43	@ R205	22	0402 5%
44	@ R206	22	0402 5%
45	@ R207	22	0402 5%
46	@ R208	22	0402 5%
47	@ R209	22	0402 5%
48	@ R210	22	0402 5%
49	@ R211	22	0402 5%
50	@ R212	22	0402 5%



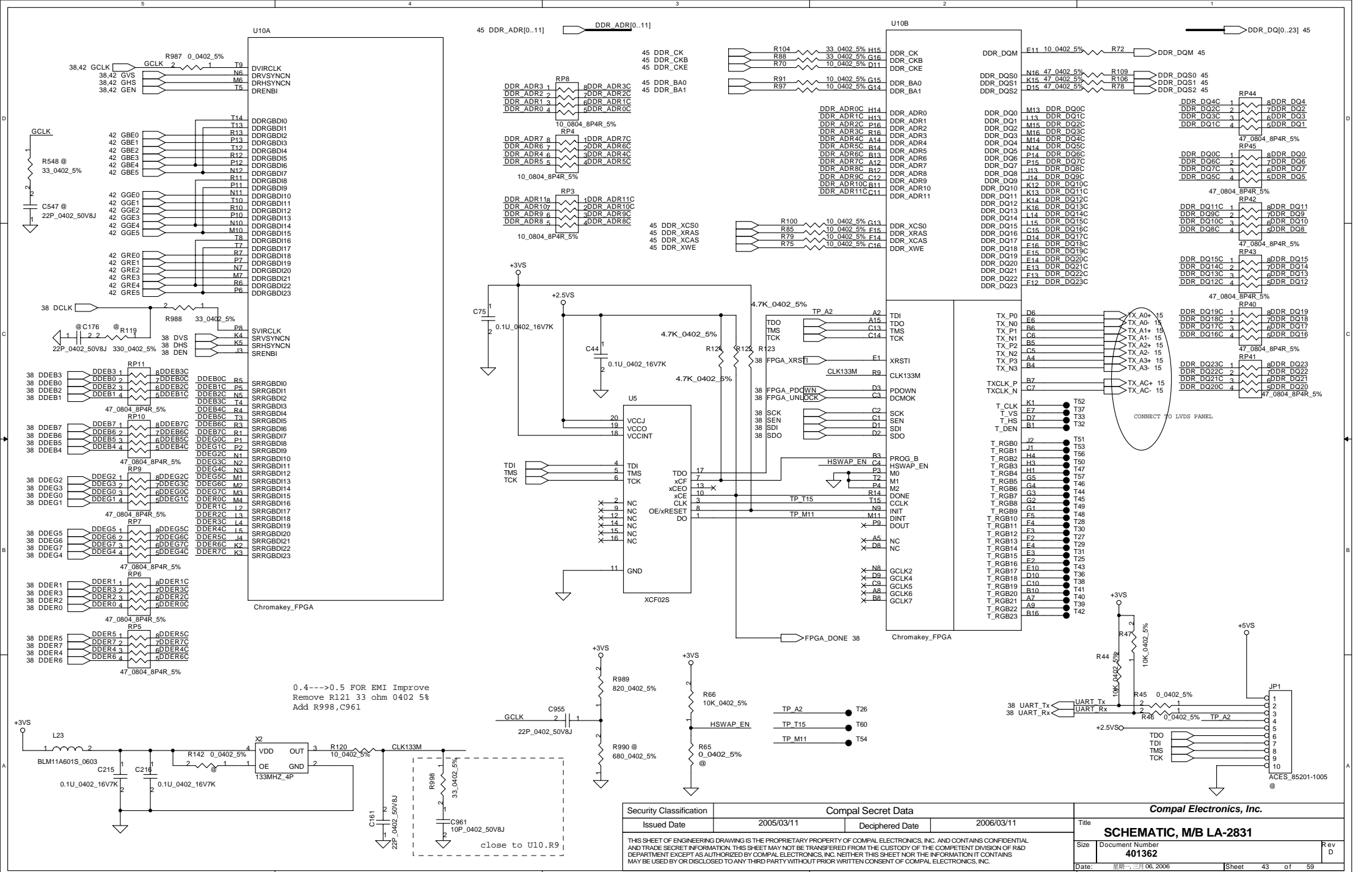




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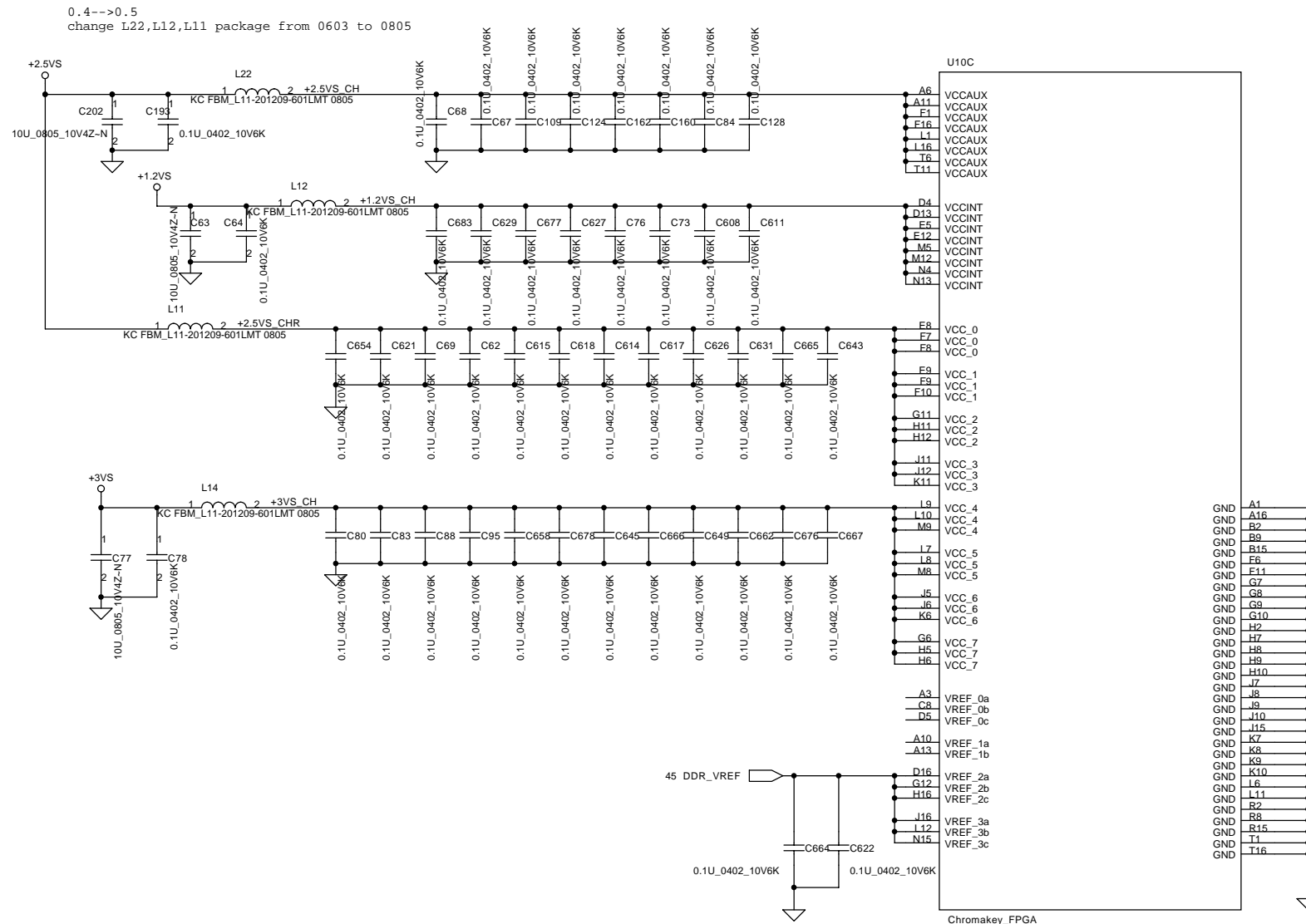
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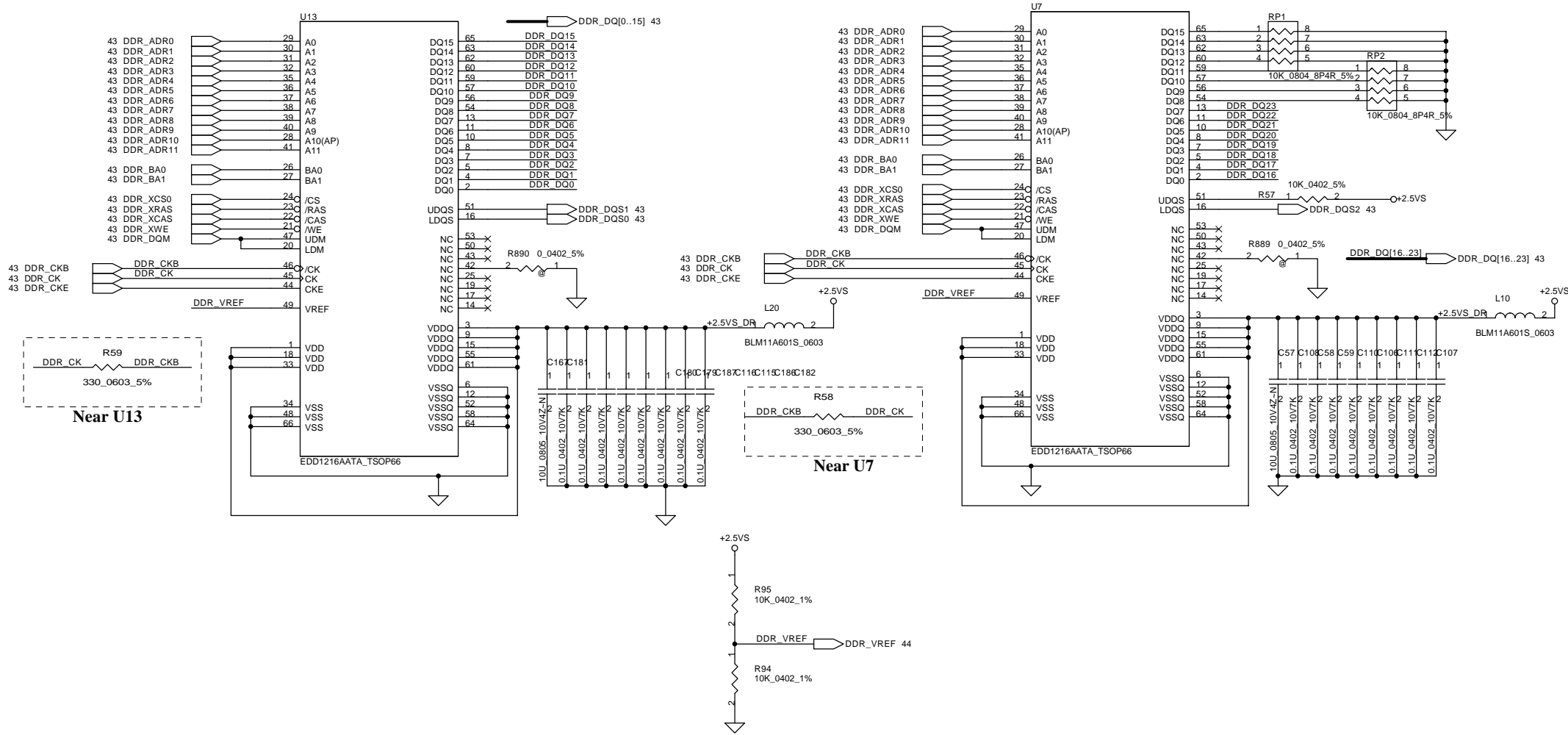
0.4--->0.5 FOR EMI Improve  
Remove R121 33 ohm 0402 5%  
Add R998,C961

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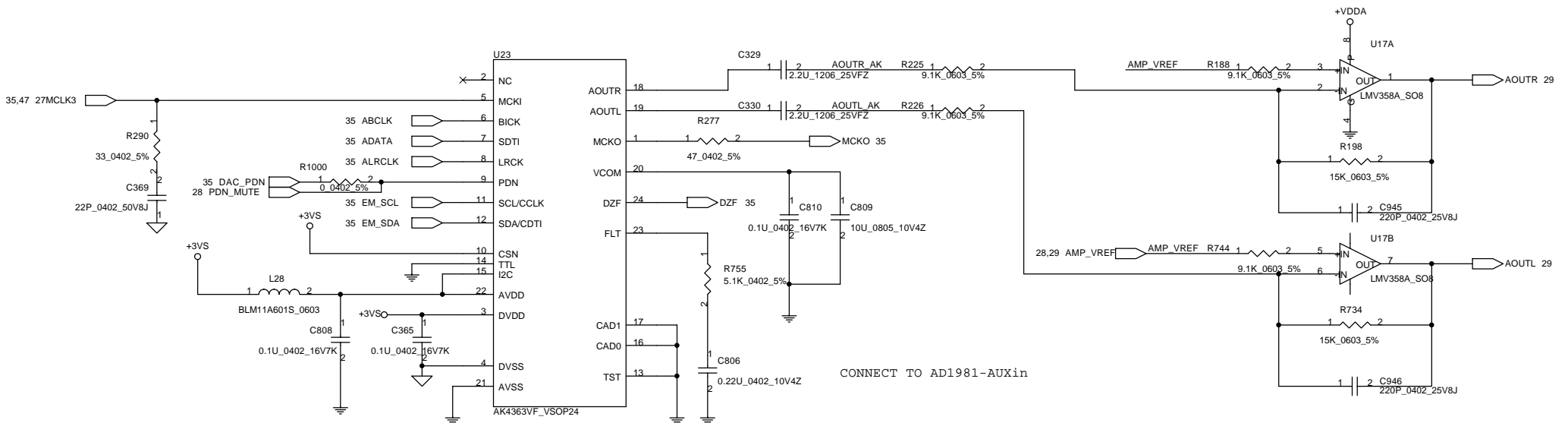
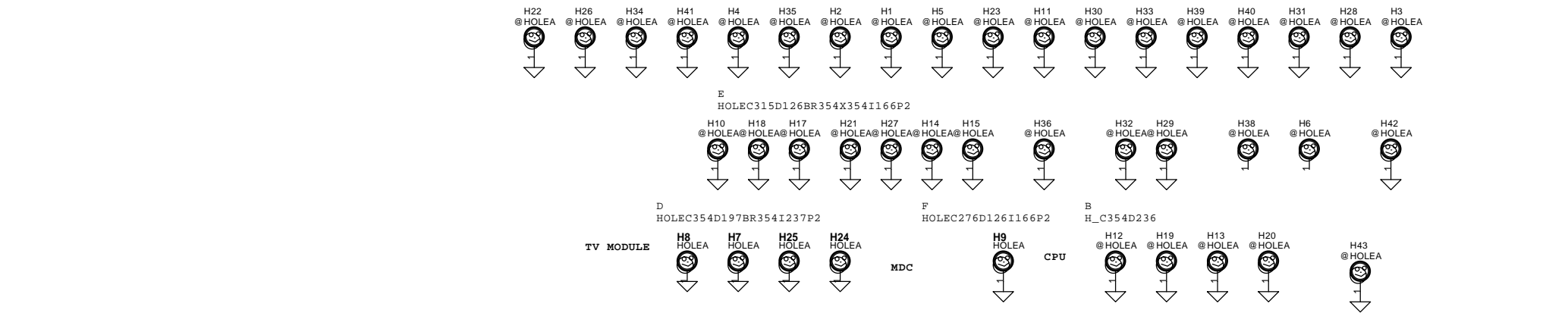
Compal Electronics, Inc.		
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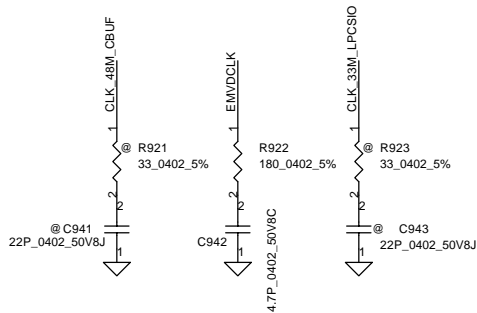
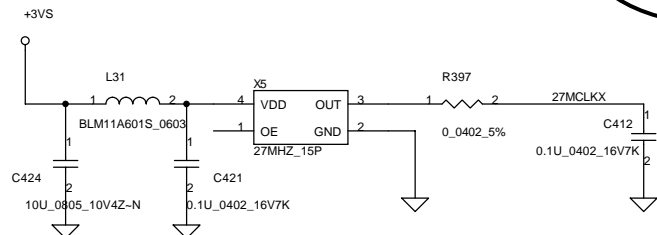
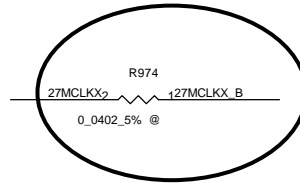
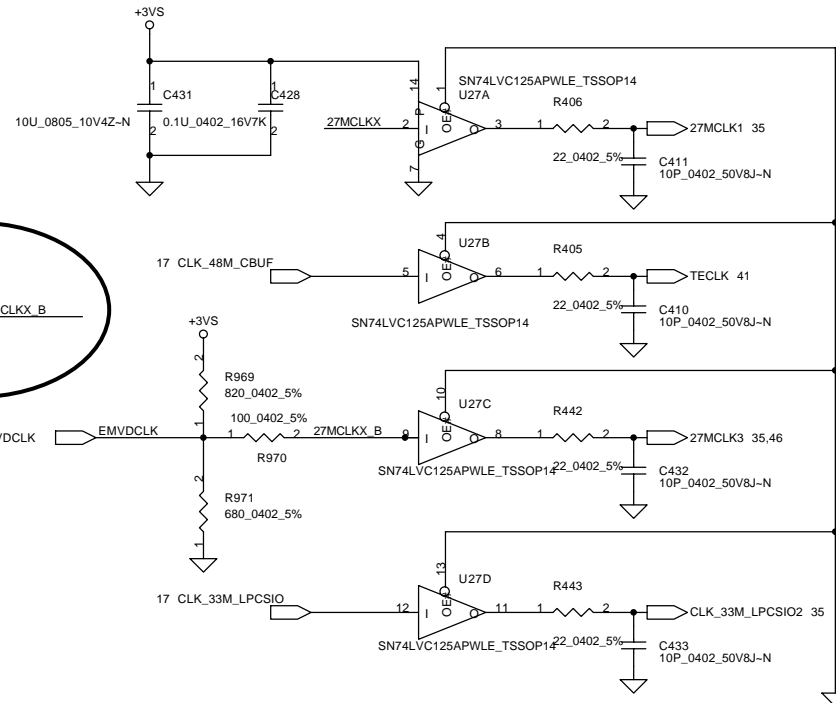
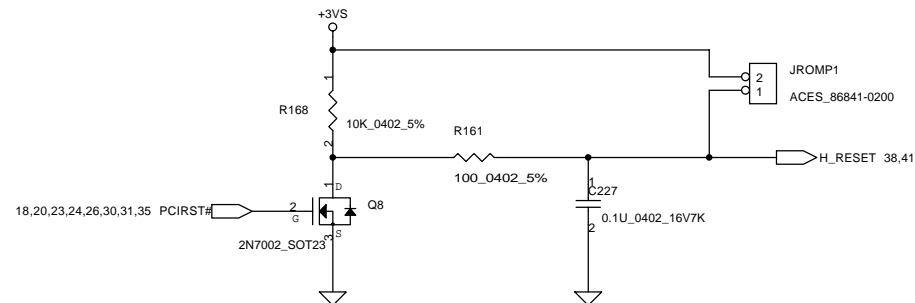
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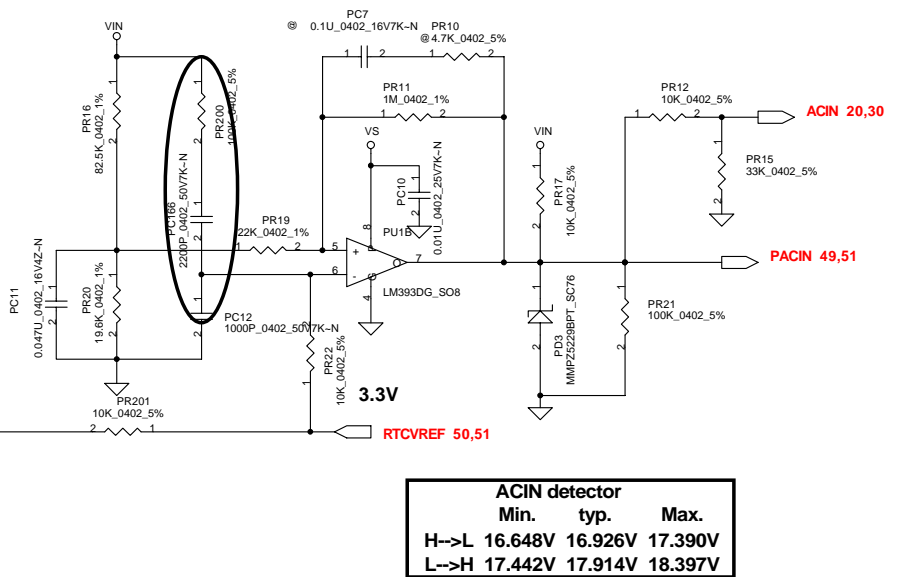
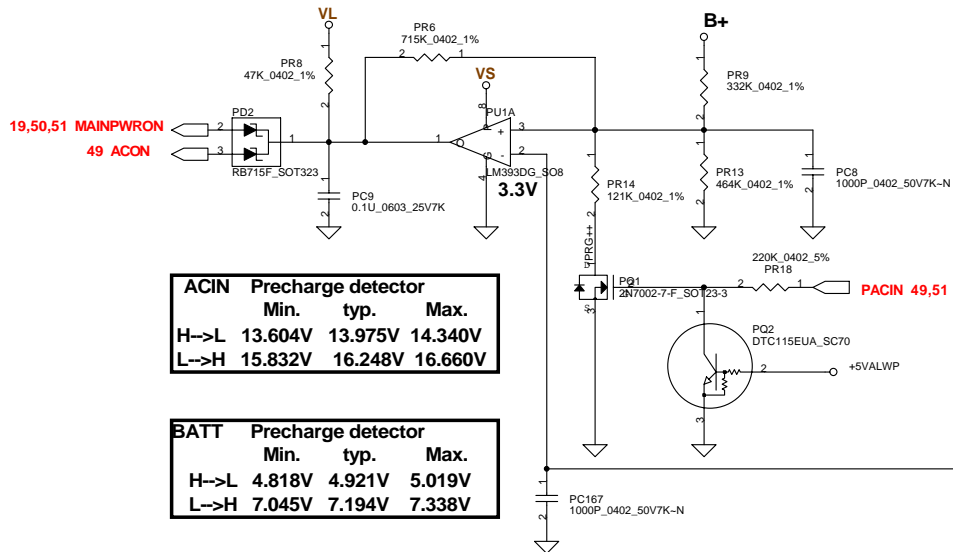
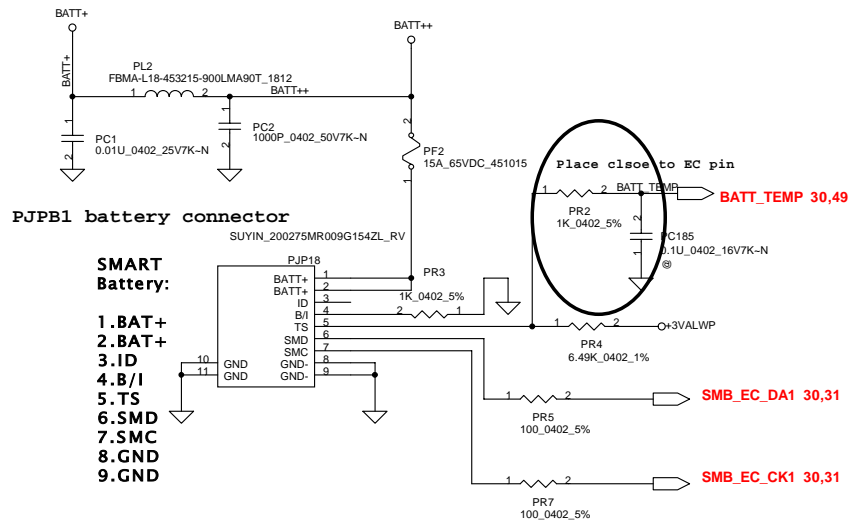
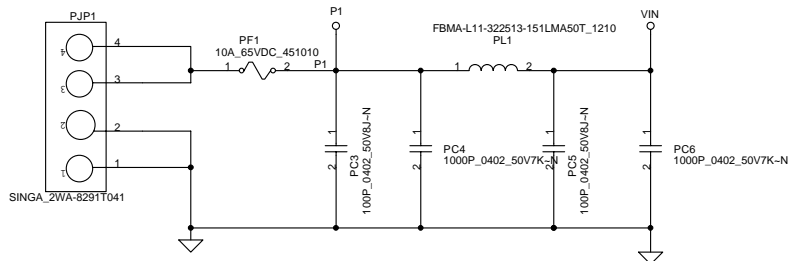
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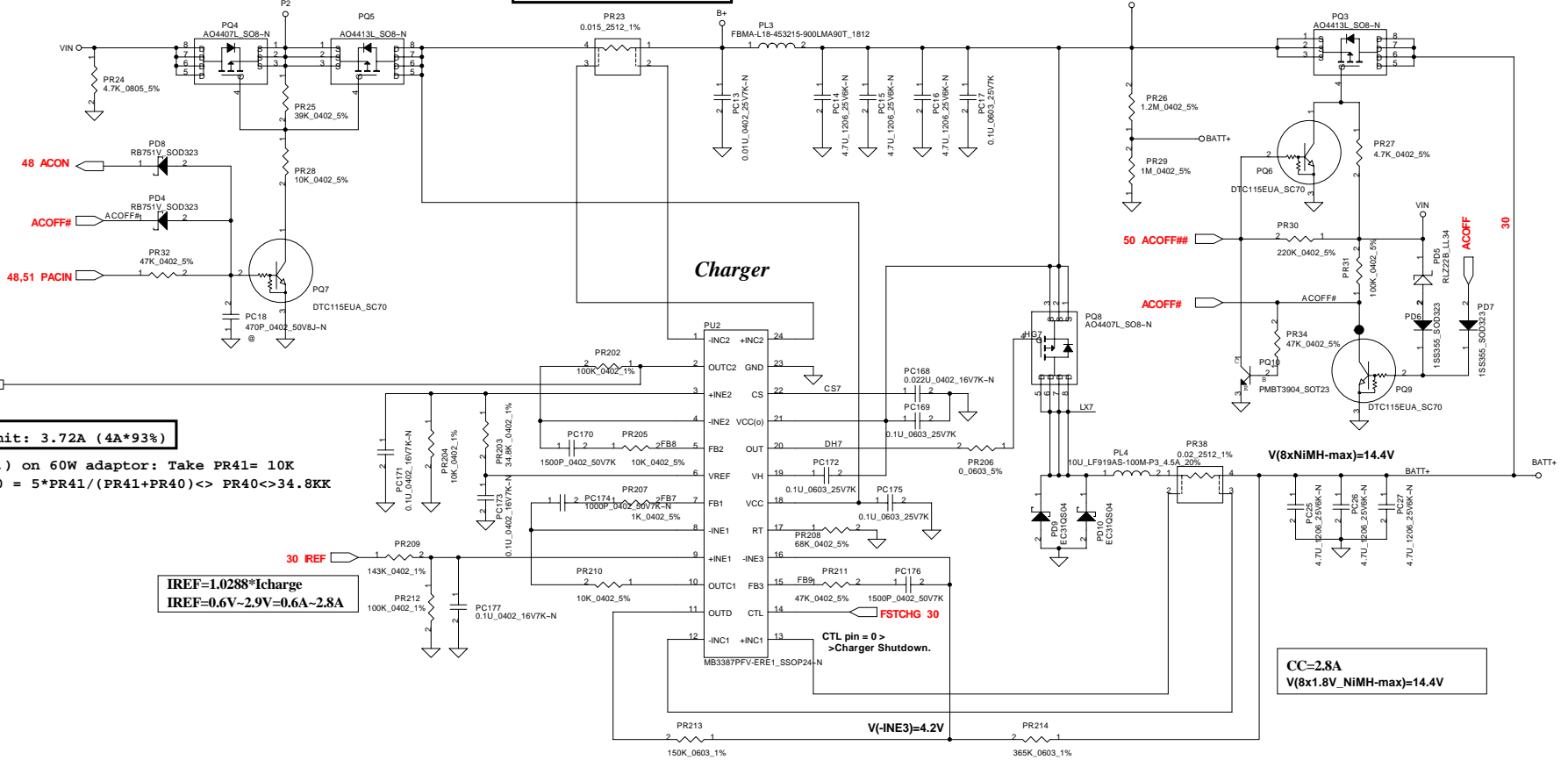
ACIN Precharge detector			
	Min.	typ.	Max.
H->L	13.604V	13.975V	14.340V
L->H	15.832V	16.248V	16.660V

BATT Precharge detector			
	Min.	typ.	Max.
H->L	4.818V	4.921V	5.019V
L->H	7.045V	7.194V	7.338V

ACIN detector			
	Min.	typ.	Max.
H->L	16.648V	16.926V	17.390V
L->H	17.442V	17.914V	18.397V



**I<sub>adp</sub>=0-4A (75W @19V)**



**Adaptor I limit: 3.72A (4A\*93%)**

D.A.C.A. (C.P.) on 60W adaptor: Take PR41= 10K  
 $3.72A \cdot 0.015 \cdot 20 = 5 \cdot PR41 / (PR41 + PR40) <> PR40 <> 34.8K$

**IREF=1.0288 \* Icharge  
 IREF=0.6V-2.9V=0.6A-2.8A**

**Charger**

**V(8xNiMH-max)=14.4V**

**CC=2.8A  
 V(8x1.8V\_NiMH-max)=14.4V**

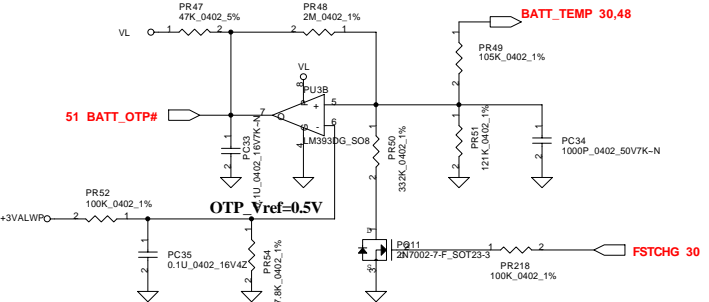
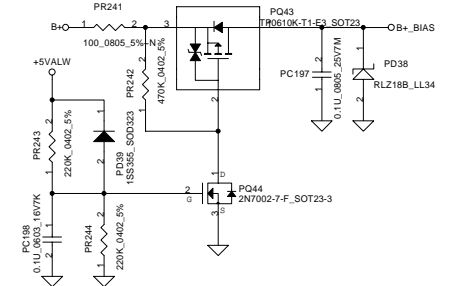
**CTL pin = 0 >  
 >Charger Shutdown.**

**V(-INE3)=4.2V**

**Batt\_OTP = 0.2V at the following conditions:**

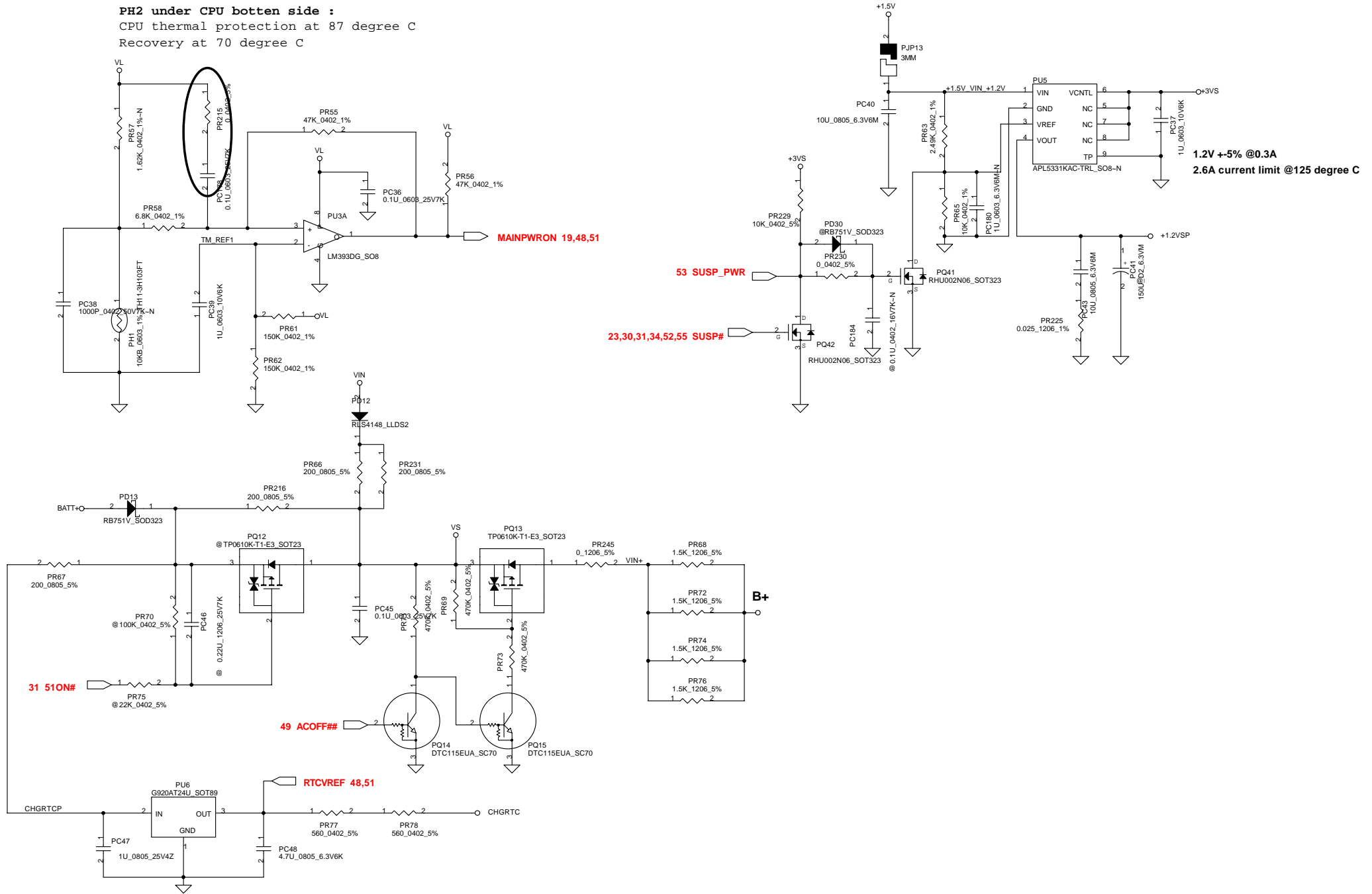
**Charge\_OTP = 0.8702V @68 degreeC.**

**Discharge\_OTP = 0.7056V @78 degreeC**



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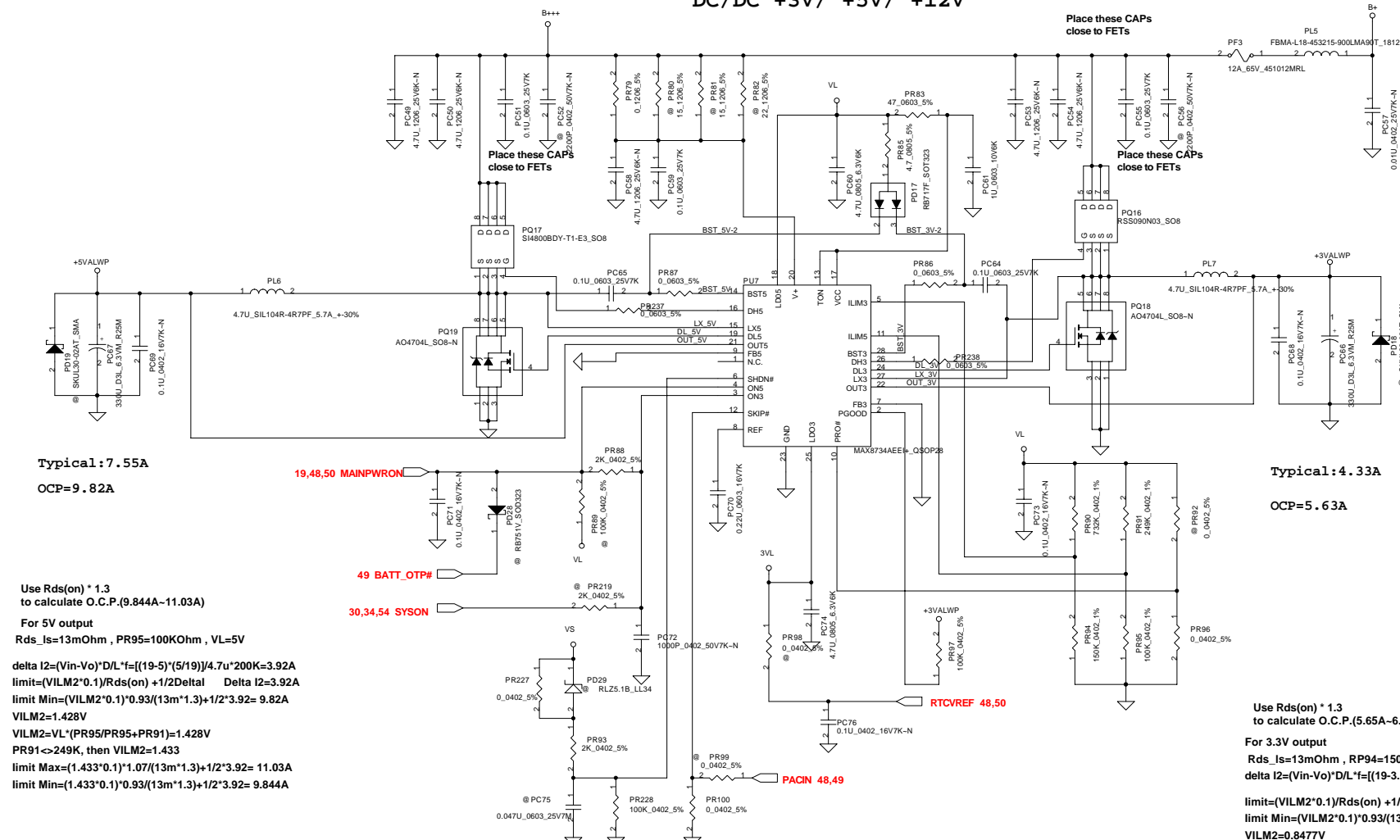
PH2 under CPU bottom side :  
 CPU thermal protection at 87 degree C  
 Recovery at 70 degree C



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# DC/DC +3V/ +5V/ +12V



Typical: 7.55A  
OCP=9.82A

19,48,50 MAINPWON

49 BATT\_OTP#

30,34,54 SYSON

Use  $R_{ds(on)} * 1.3$   
to calculate O.C.P.(9.844A-11.03A)  
For 5V output  
 $R_{ds\_ls}=13m\Omega$ ,  $PR_{95}=100K\Omega$ ,  $V_L=5V$

$\Delta I_2 = (V_{in} - V_o) * D / L * f = [(19.5V) * (5/19)] / 4.7\mu * 200K = 3.92A$   
 $limit = (V_{ILM2} * 0.1) / R_{ds(on)} + 1/2 \Delta I_2$   $\Delta I_2 = 3.92A$   
 $limit\ Min = (V_{ILM2} * 0.1) * 0.93 / (13m * 1.3) + 1/2 * 3.92 = 9.82A$   
 $V_{ILM2} = 1.428V$   
 $V_{ILM2} = V_L * (PR_{95} / PR_{95} + PR_{91}) = 1.428V$   
 $PR_{91} \rightarrow 249K$ , then  $V_{ILM2} = 1.433$   
 $limit\ Max = (1.433 * 0.1) * 1.07 / (13m * 1.3) + 1/2 * 3.92 = 11.03A$   
 $limit\ Min = (1.433 * 0.1) * 0.93 / (13m * 1.3) + 1/2 * 3.92 = 9.844A$

RTCVREF 48.50

PACIN 48.49

Typical: 4.33A  
OCP=5.63A

Use  $R_{ds(on)} * 1.3$   
to calculate O.C.P.(5.65A-6.35A)

For 3.3V output  
 $R_{ds\_ls}=13m\Omega$ ,  $RP_{94}=150K\Omega$ ,  $V_L=5V$   
 $\Delta I_2 = (V_{in} - V_o) * D / L * f = [(19.3V) * (3.3/19)] / 4.7\mu * 300K = 1.93A$   
 $limit = (V_{ILM2} * 0.1) / R_{ds(on)} + 1/2 \Delta I_2$   $\Delta I_2 = 1.93A$   
 $limit\ Min = (V_{ILM2} * 0.1) * 0.93 / (13m * 1.3) + 1/2 * 1.93 = 5.63A$   
 $V_{ILM2} = 0.8477V$   
 $V_{ILM2} = V_L * (PR_{94} / PR_{94} + PR_{90}) = 0.8477V$   
 $PR_{90} \rightarrow 732K$ , then  $V_{ILM2} = 0.85$   
 $limit\ Max = (0.85 * 0.1) * 1.07 / (13m * 1.3) + 1/2 * 1.93 = 6.35A$   
 $limit\ Min = (0.85 * 0.1) * 0.93 / (13m * 1.3) + 1/2 * 1.93 = 5.65A$

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Low\_side MOS Rds(on) typ=17mOhm, Max=24mOhm  
 To use L-side Rds(on)\*1.5 to calculate OCP  
 Set OCP=4.55A, Risen=PR106=2.05K  
 (Iocp\*Rds(on)\*1.5)/PR106+104=76.045uA  
 Rocset=PR117=10.3V/(76.045uA+8uA)=122K, Set PR117=121K

Typical: 3.5A  
 OCP: 4.55A

Low\_side MOS Rds(on) typ=17mOhm, Max=24mOhm  
 To use L-side Rds(on)\*1.5 to calculate OCP  
 Set OCP=8.45A, Risen=PR107=2.05K  
 (Iocp\*Rds(on)\*1.5)/PR107+104=141.226uA  
 Rocset=PR117=10.3V/(141.226uA+8uA)=69K, Set PR118=69.8K  
 Typical: 6.5A  
 OCP: 8.45A

$$V_{out} = 0.9V * (1 + PR109/PR114) = 0.9V * (1 + 18.2K/10K) = 2.538V$$

$$V_{out} = 0.9V * (1 + PR110/PR113) = 0.9V * (1 + 1.74K/10K) = 1.0566V$$

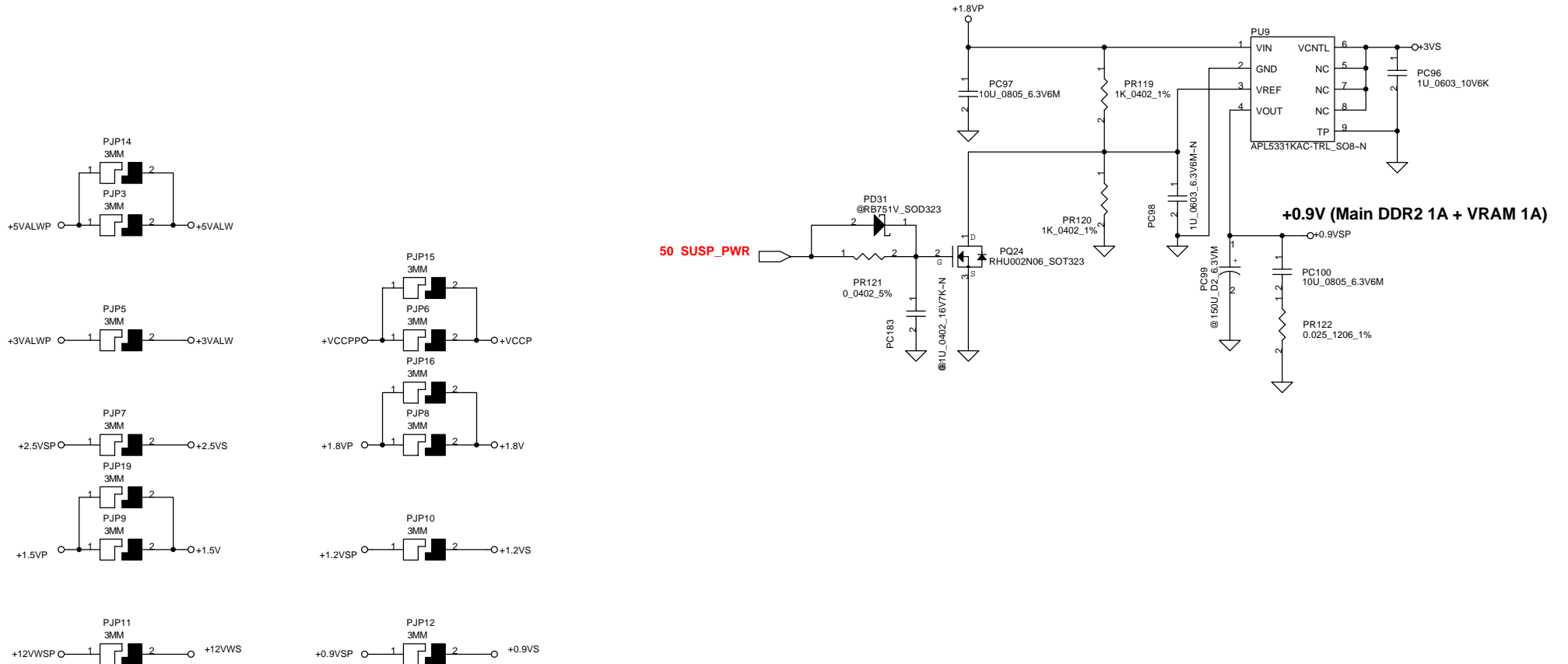
23,30,31,34,50,55 SUSP#

SUSP# 23,30,31,34,50,55

VCCP\_ON 30

+VCCP\_PWRGD 30

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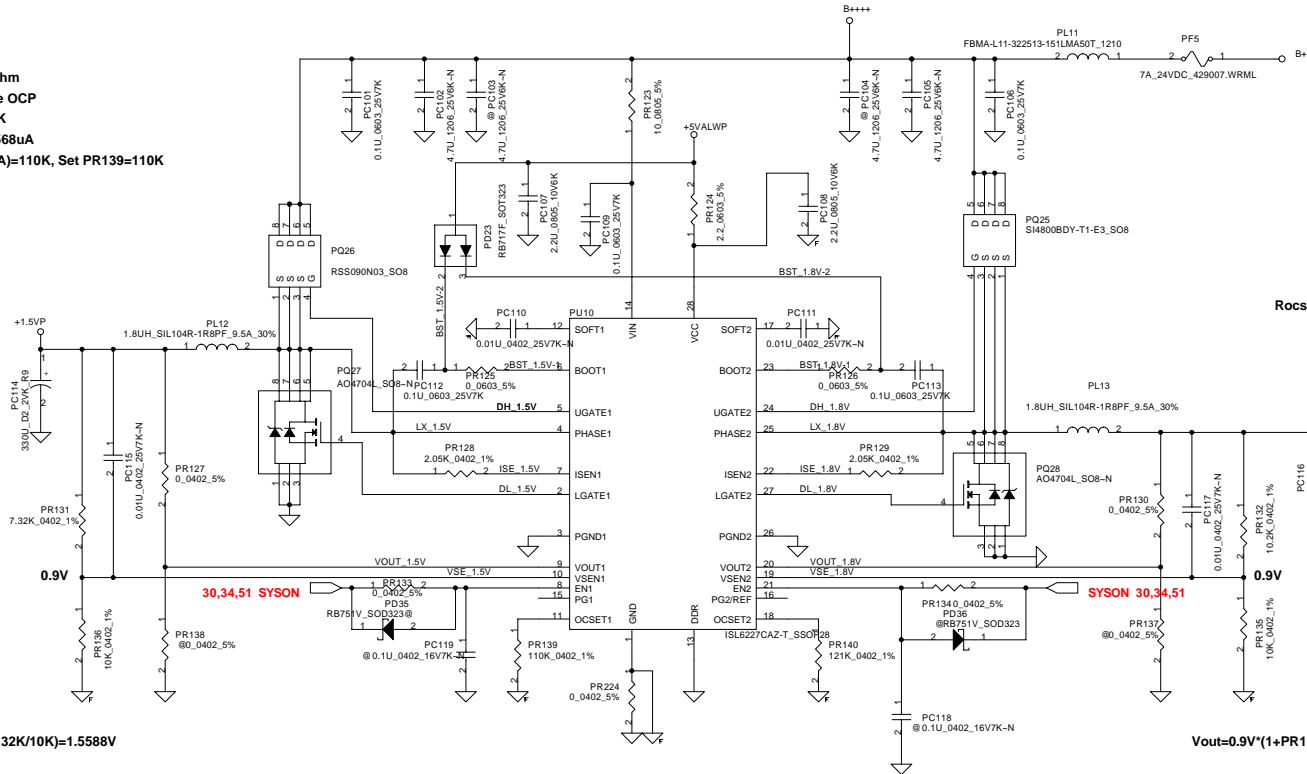


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Low\_side MOS Rds(on) Max=13mOhm  
 To use L-side Rds(on)\*1.5 to calculate OCP  
 Set OCP=9.61A, Risen=PR128=2.05K  
 (Iocp\*Rds(on)\*1.5)/(PR128+140)=85.568uA  
 Rocset=PR139=10.3V/(85.568uA+8uA)=110K, Set PR139=110K

Typical: 7.39A

OCP: 9.61A



Low\_side MOS Rds(on) typ=13.3mOhm, Max=16.5mOhm  
 To use L-side Rds(on)\*1.5 to calculate OCP  
 Set OCP=8.67A, Risen=PR129=2.05K  
 (Iocp\*Rds(on)\*1.5)/(PR129+104)=78.634uA  
 Rocset=PR140=10.3V/(200.557uA+8uA)=118.89K, Set PR140=121K

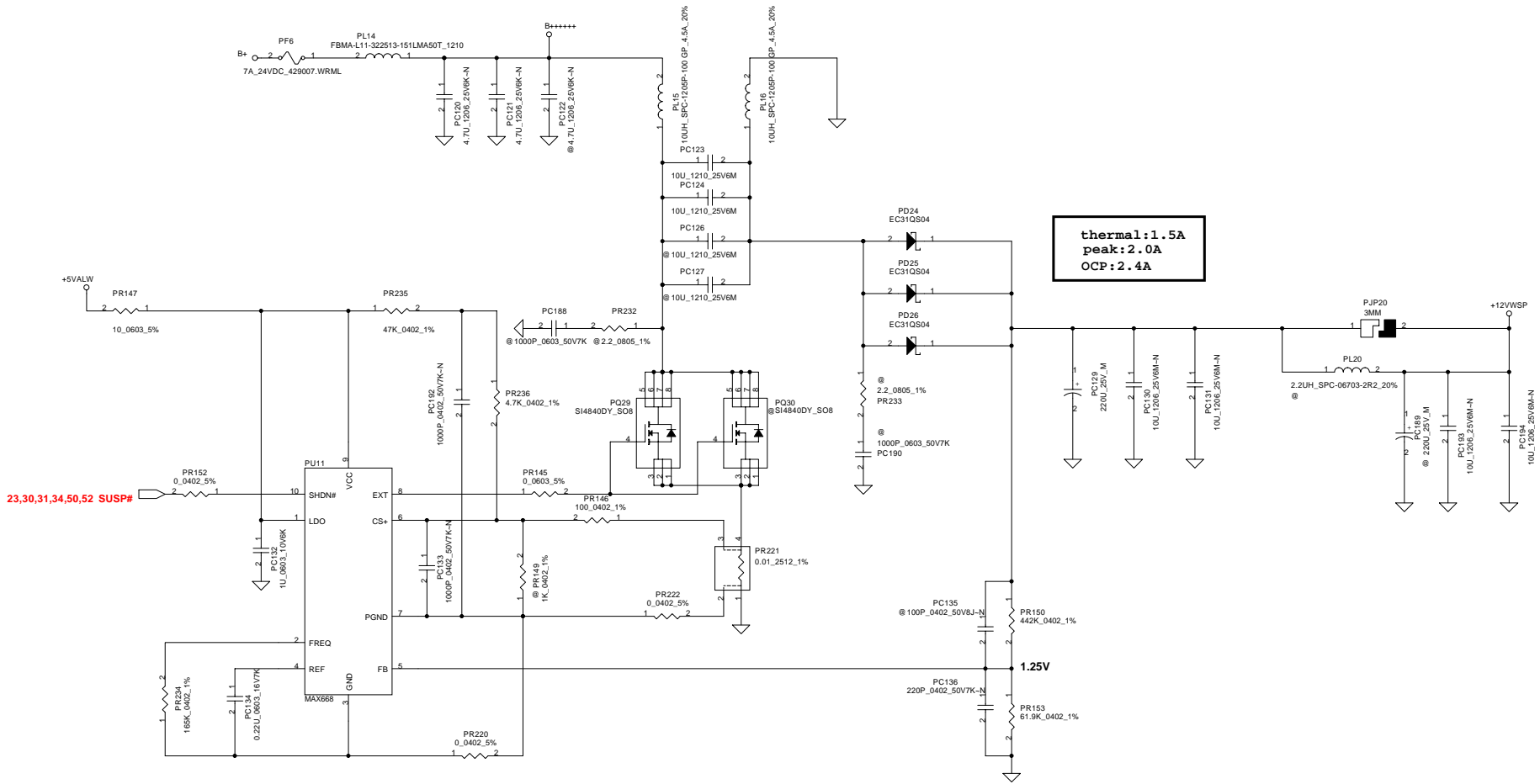
Typical: 6.67A

OCP: 8.67A

$$V_{out}=0.9V \cdot (1 + PR131/PR136) = 0.9V \cdot (1 + 7.32K/10K) = 1.5588V$$

$$V_{out}=0.9V \cdot (1 + PR132/PR135) = 0.9V \cdot (1 + 10.2K/10K) = 1.818V$$

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thermal:1.5A  
peak:2.0A  
OCP:2.4A

23,30,31,34,50,52 SUSP#

$$V_{out} = 1.25V \cdot (1 + PR150/PR153) = 1.25V \cdot (1 + 442K/49.9K) = 12.32V$$

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# CPU CORE

$\Delta I = (V_{in} - V_o) \cdot D/L \cdot f = [(19 - 1.308) \cdot (1.308/19)] / (0.56 \mu \cdot 300K) = 7.25A$

OCP = 35.1A(TYP), DCR = 1.4mOhm

Ilimit(min) per phase = 35.1 / 2 - 7.25 / 2 = 13.925A

$13.925A \cdot 1.4mOhm(DCR) \cdot 1.3(\text{temperature factor}) \cdot 20 = VLLIM(TYP) = 0.50687V$

Take PR178 = 237K, PR180 = 90.9K

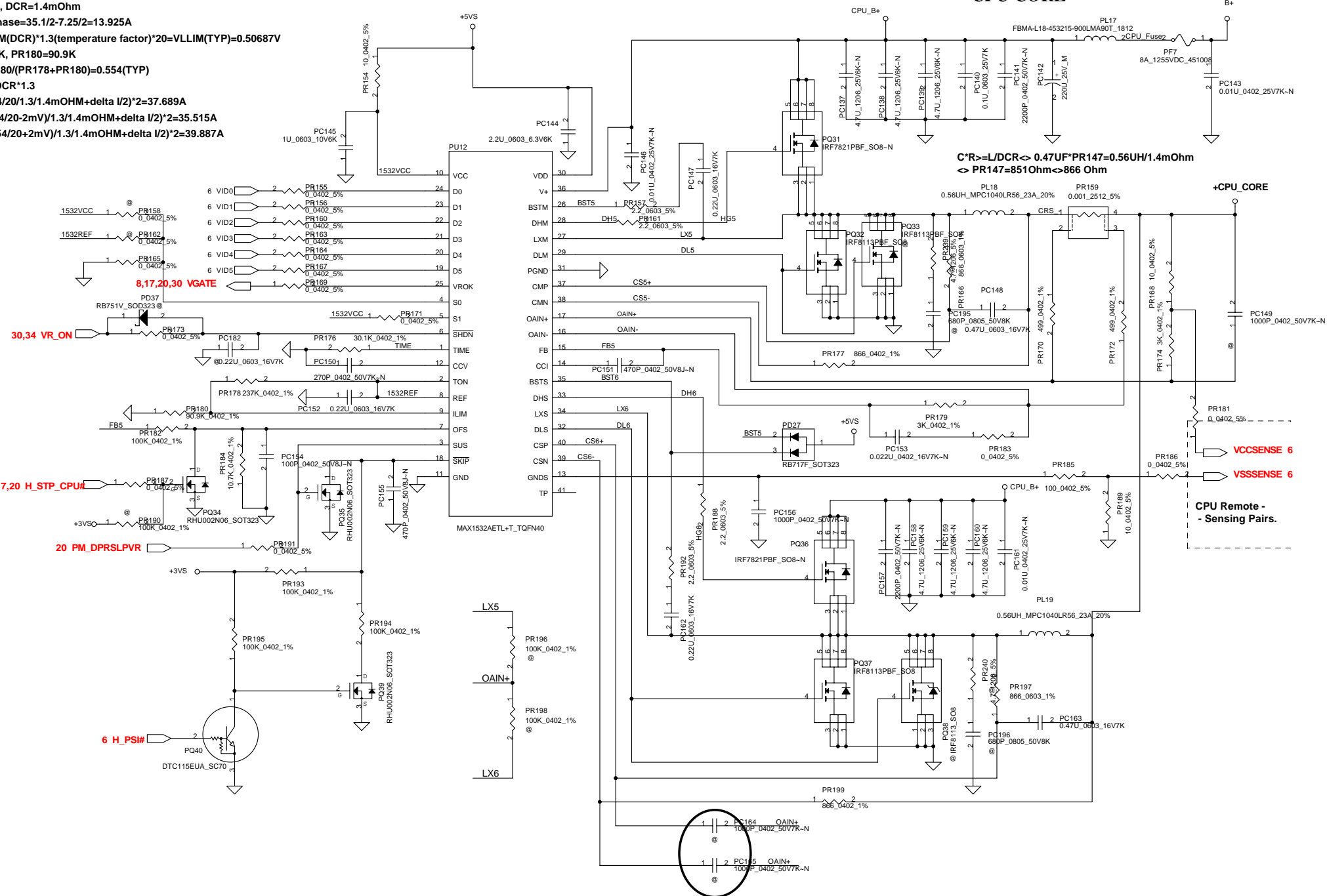
$VILIM = VREF \cdot PR180 / (PR178 + PR180) = 0.554(TYP)$

$VILIM / 20 = Ilimit \cdot DCR \cdot 1.3$

$OCP(TYP) = (0.554 / 20 - 2mV) / 1.3 / 1.4mOhm + \Delta I / 2 \cdot 2 = 37.689A$

$OCP(min) = ((0.554 / 20 - 2mV) / 1.3 / 1.4mOhm + \Delta I / 2) \cdot 2 = 35.515A$

$OCP(max) = ((0.554 / 20 + 2mV) / 1.3 / 1.4mOhm + \Delta I / 2) \cdot 2 = 39.887A$



$C^*R > L / DCR > 0.47 \mu F \cdot PR147 = 0.56 \mu H / 1.4mOhm$   
 $\diamond PR147 = 851 Ohm \diamond 866 Ohm$

+CPU\_CORE

CPU Remote -  
- Sensing Pairs.

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	+3V/5V	07/05	Compal	To improve EMI	To add PR237 and PR238 connect to High-side Gate	0.1
2	56	CPU_CORE	07/05	Compal	To improve EMI	To add PR239,PC196 and PR240,PC195 connect to Phase node	
3	50	CPU OTP function	07/05	Compal	To meet 87 degree C CPU OTP	To change PR57 to 1.96K and PR58 to 6.8K	
4	54	1.5V/1.8V	07/05	Compal	H/W ask to change 1.5V to 1.55V	To change PR131 to 7.32K	
5	49	Battery OTP function	08/01	Compal	To prevent mainpwn is pull low	To change PR52 pin2 connect to +3VALWP	
6	51	+3V/5V	08/05	Compal	To prevent choke is too hot	remove the +12VALWP function (remove PD16,PC63,PR84,PC62,PD15)	
7	49	charger	08/05	Compal	To prevent 5Vchoke is too hot	New add B+_BIAS function to replace +12VALWP(Add PR241,PR242 PQ43,PC197,PD38,PR243,PC198,PR244,PD39,PQ44)	
8	55	+12VWSP	08/15	NEC	Follow NEC required	To change PR153 to 61.9K	
10	49	charger	08/29	Compal	Change OTP@ charge to 68 degree C to avoid shut down on production line	To change PR50 to 332K	
11	51	+3V/5V	08/29	Compal	To prevent 3V/5Vchoke is too hot at S5 mode	Depop PR99 and Pop PR100	
12	51	+3V/5V	09/26	Compal	Batt OTP circuit has problem	Depop PD28	
13							
14							
15							
16							
17							

Next: PR238, PC202, PQ56, PD42, PJP21

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1		LVDS output EMI solution		15	Change R10,R11,R12,R13,R14,R15,R16,R17,R18,R19 to (L72,L73,L74,L75,L76)		
2		modify JLVDS1 to fit in new inverter		15	add JLVDS1 Pin35 connection to LCD_INVB+		
3		EC control PWR_LED#,BATT_LED#,CHARGE_LED#		15	Change Q37,Q38,Q39 to MMBT3904, add R947,R948,R949 330ohm,R611,R612,R613 change to 1M ohm then connect to GND		
4		PANEL Backlight only control by EC&NB		15	del U48		
5		CLK_33M_MPCI connect to MPCI & TV too long		17	CLK_33M_CBS connect to JTVMD1 pin74		
6		Buzzer is too quiet		27	change R820 to 100ohm		
7		U50 output left/right channel are wrong		29	swap U50 pin6&pin10(pin6 connect to LINE_IN_L) (pin10 connect to LINE_IN_R)		
8		control PANEL by EC		30	EC(U57)pin24 connect to LCD_VDD_EN pin70 connect to LCD_EN		
9	EC judge LID switch is not open, then can't boot by pwr button.	LID switch on/off		31	change JLSW1 pin4 connect from +3V to +3VALW		
10		EMI solution for MDC IAC_BITCLK		32	Add R940 (33ohm) and C944 (22pF)		
11	USB2.0 fail	DIODE using wrong		33	change D1,D5,D23,D24 from PSOT24C to BAT54A(SCSBAT540A0)		
12	LM358 issue	AK4363 sound output signal unstable.		46	change R225,R226 to 9.1k ohm, R198,R734 to 15k ohm add C945 220PF between U17A pin1&pin2, add C946 220PF between U17A pin6&pin7 U17A pin2 connect to R225, U17B pin6 connect to R226 R744,R198 connect to AMP_VREF		
13		U27 clock buffer EMI solution		47	Add R921,R922,R923 33ohm and C941,C942,C943 22PF		
14		Change touch pad from USB to PS2 interface		30,31	Del USBP5-;USBP5+ Add PSDAT3; PSCLK3		
15	It had POP noise when enter S4.	The subwoofer shut down timing to late		29	EAPD connect to U19 RESET pin		
16	The AUDIO can not turn off when the LCD close.	The EC can not control amplifier shutdown		28	EC_MUTE# connect to amplifier shutdown pin		
17	Video-Engine function abnormal	The EMVDCLK waveform break		35,47	Add R967,R968,R969,R970,R971 to smooth EMVDCLK waveform		
18	USB2.0 fail (0.4-->0.5)	ESD DIODE		16	Change D1,D5,D23,D24 package		
19	AW172A power sequence fail (0.4-->0.5)	+2.5VS too fast (0.4-->0.5)		39	Add one power regulator		
20		FUPL1,JSPK1 packake change(0.4-->0.5)		28,48	FUPL1,JSPK1 SMD-->DIP(0.4-->0.5)		
21	Improve voltage drop(0.4-->0.5)	Improve component DCR(0.4-->0.5)		44	change L22,L12,L11 package from 0603 to 0805(0.4-->0.5)		
22		Improve Lan test(0.4-->0.5)		23	Add L78,L79 0805(0.4-->0.5)		

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Version change list (P.I.R. List)

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1		Add two resistors to HSYNC,VSYNC		16	Add R1004,R1005,R1006,R1007		
2		Add resistors from EM8475_DAC_PDN to MUTE for noise resume S4		46	Add R999,R1000		
3		Add FB to VCC-CRT-DAC & VSS-CRT-DAC		11	Add L80,L81		
4		Power plan reservation for RRX6000		29	Add R1012,R1013		
5		Circuit reservation for TE7782		41	Add R1009,R1010		
6		Improve 2.5VS		26	Add C966,C967		
7		Improve EMVDCLK Layout		26	Delete C954		
8		EC pin 90 connect to ODD_ACT# (optional)		30	Add R1014		
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