

Model Name : ZIWB0/ZIWB1/ZIWE0

File Name :

# Compal Confidential

## ZIWB0/ZIWB1/ZIWE0 UMA M/B Schematics Document

Intel Bay Trail M

2014-02-10

REV:1.0

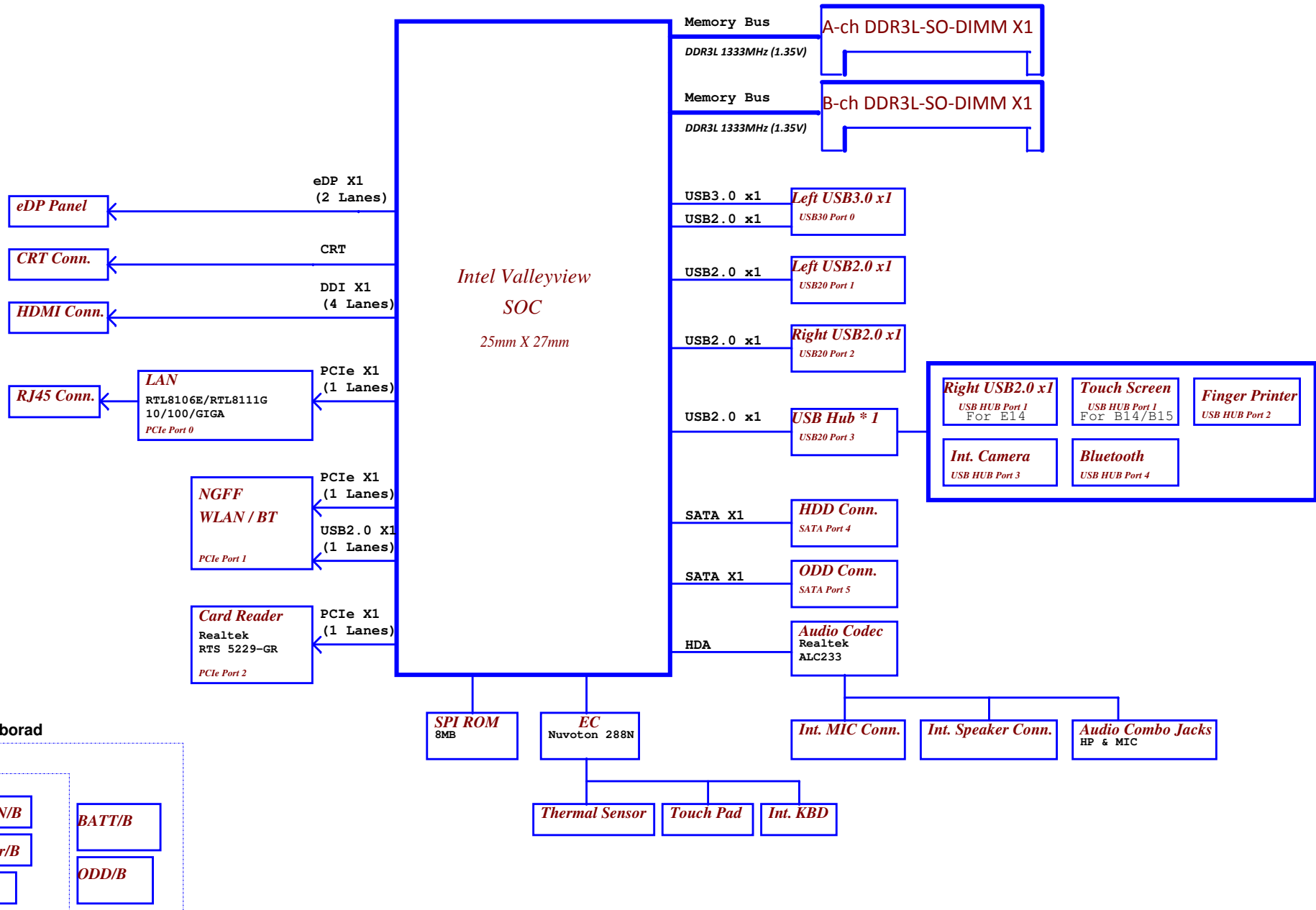
14PCB@  
DA1 PCB

Part Number	Description
DA60013Z010	REV1.0 M/B

15PCB@  
DA2 PCB

Part Number	Description
DA60013Z110	REV1.0 M/B

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				<b>Block Diagrams</b>
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## Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

## BOM Option Table

Item	BOM Structure
Unpop	@
Connector	ME@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Touch Screen	TS@
B/E series sku	B14@
B/E series sku	B15@
B/E series sku	E14@

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b
Charger	0b00010010 (0x12H)

Device	Address
GPU	0x9E
Thermal	1001_101xb

## SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

## 43 level BOM table

43 Level	Description	BOM Structure

USOC1  
N2920@

USOC1  
N3520@

USOC1  
N2815@

S IC FH8065301616203 SR1SF B3 1.86G C38!  
Part Number = SA00007E860

S IC FH8065301616103 SR1SE B3 2.17G C38!  
Part Number = SA00007E990

S IC FH8065301619509 SR1SJ B3 1.86G C38!  
Part Number = SA00007EO50

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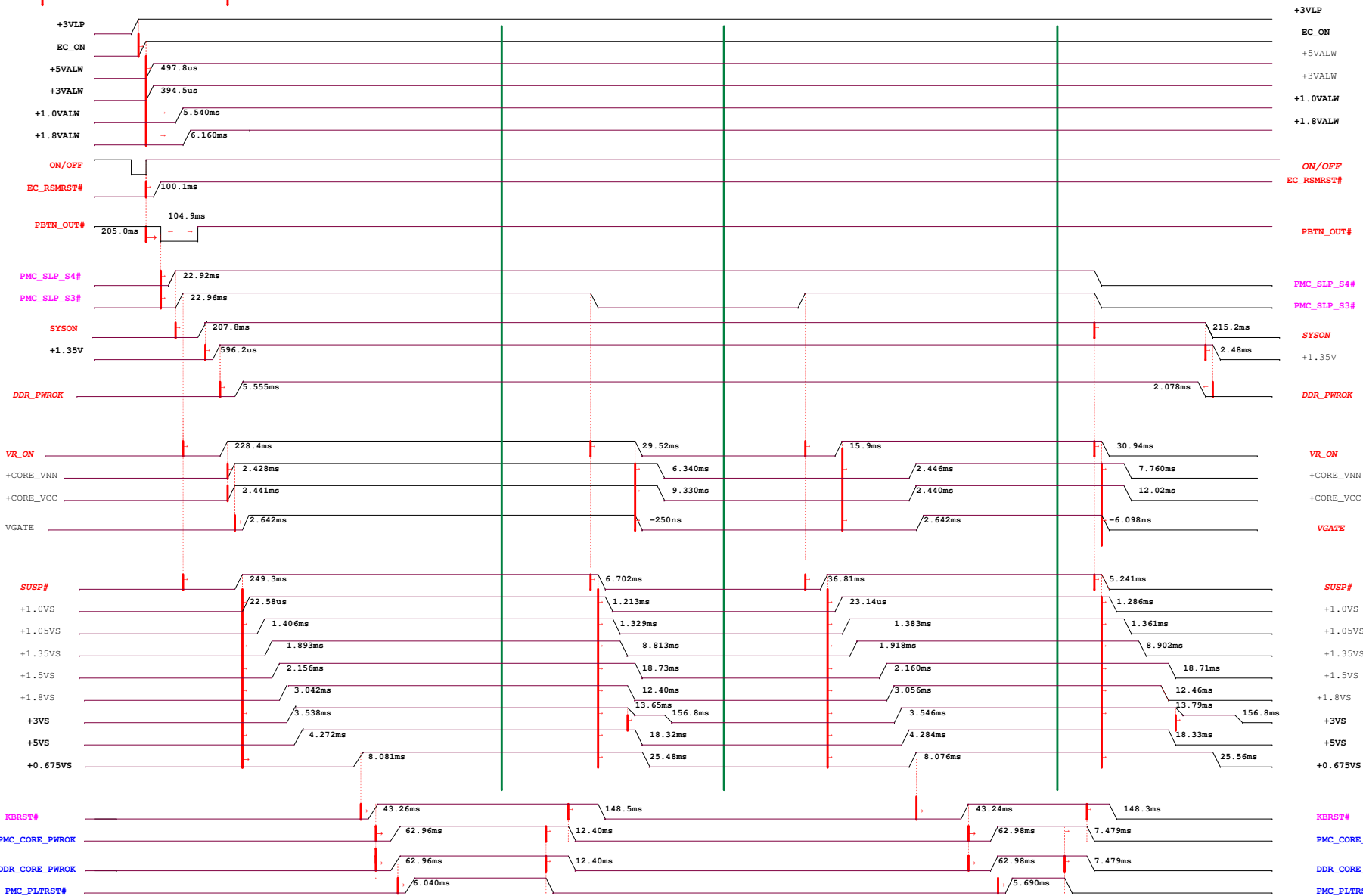
Power On

S3

S3 Resume

Power Off

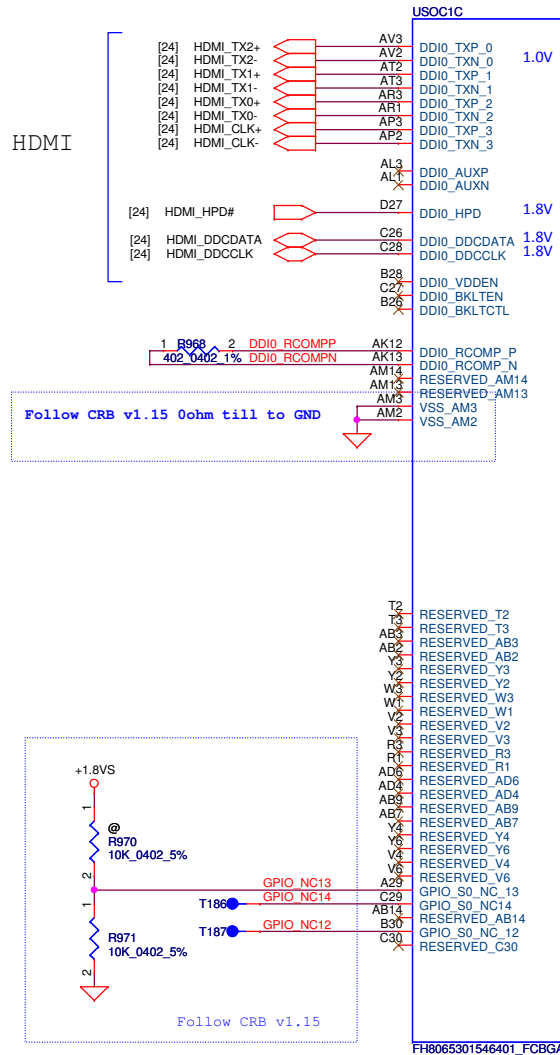
Plug in



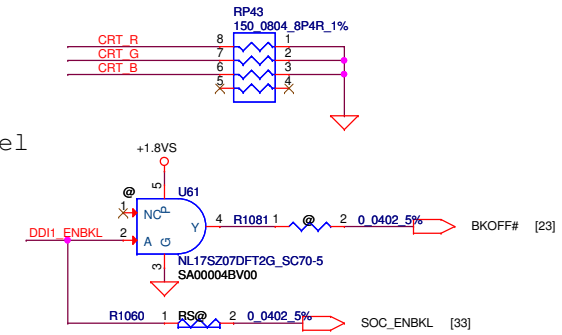
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Power Sequence
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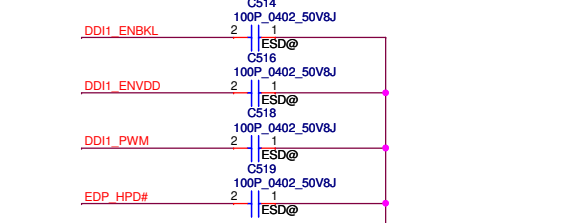
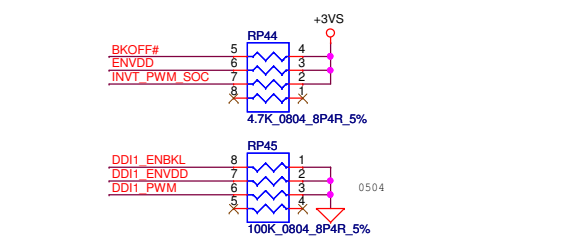
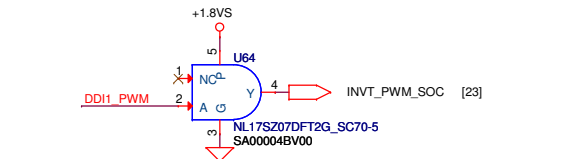
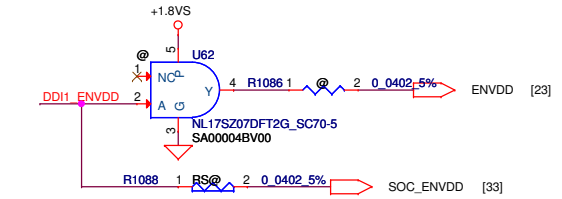
HDMI



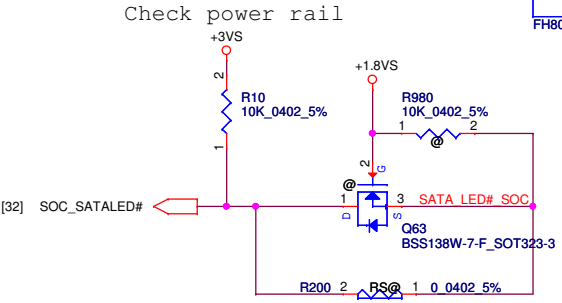
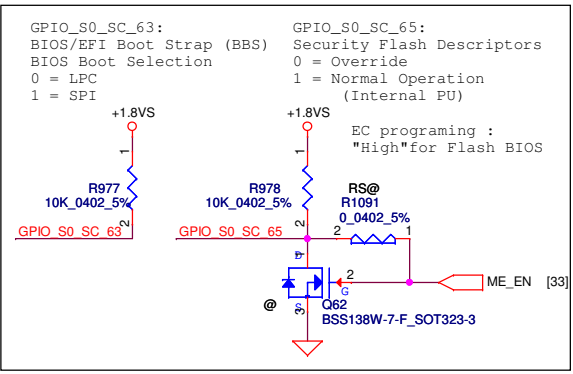
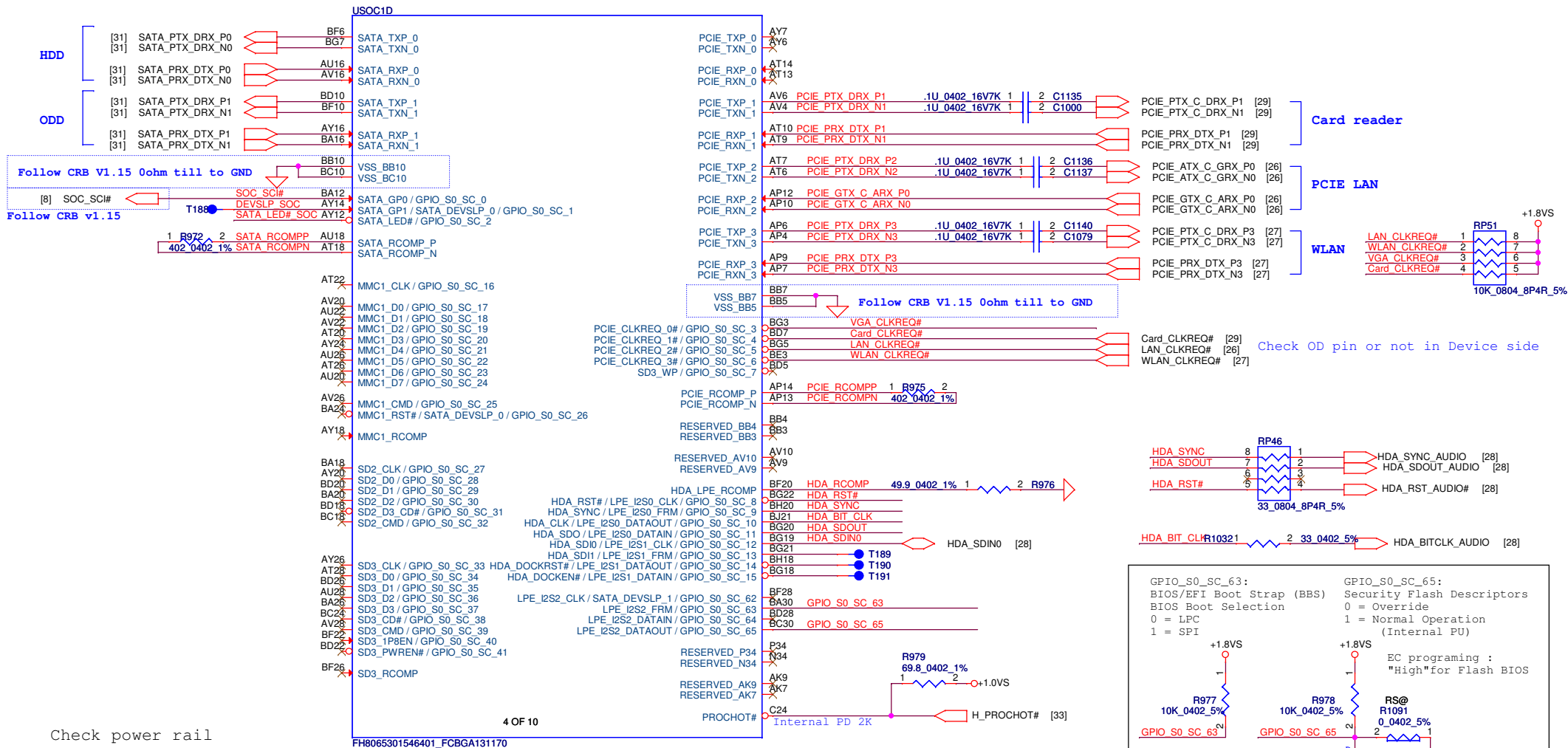
eDP Panel



CRT



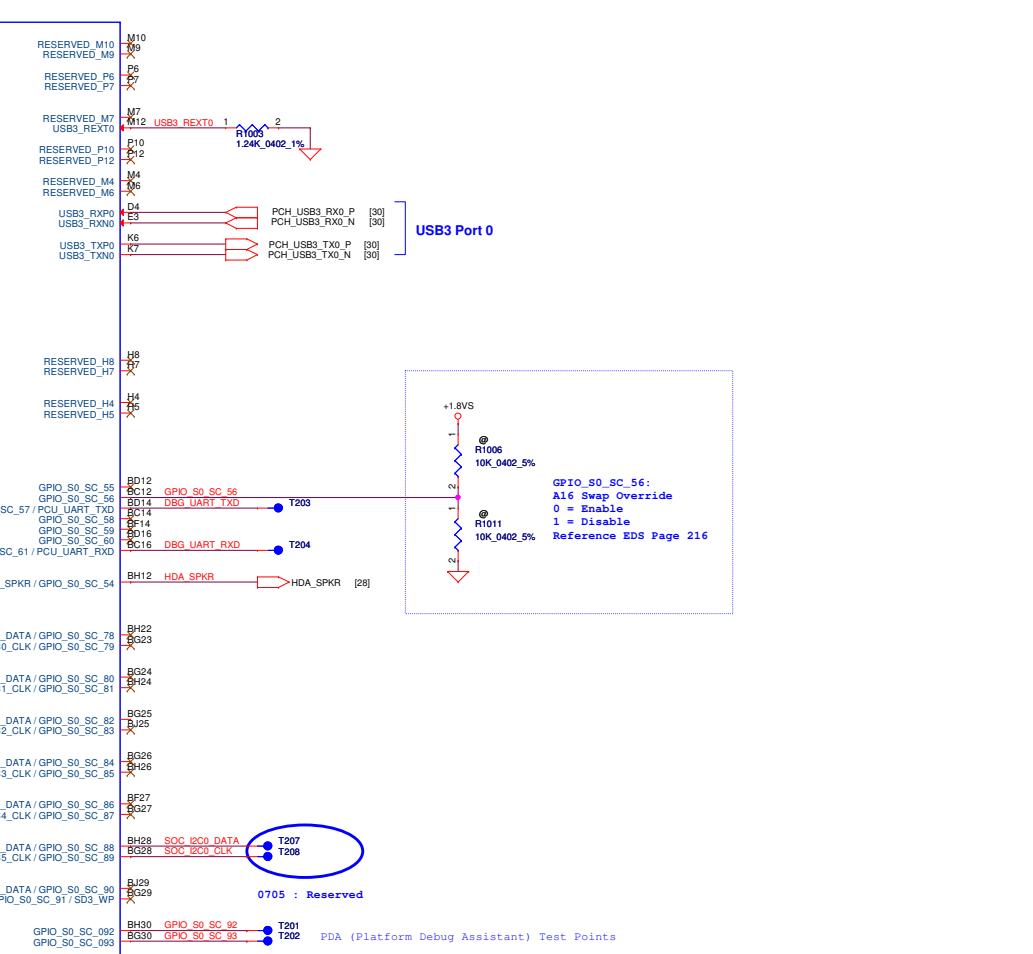
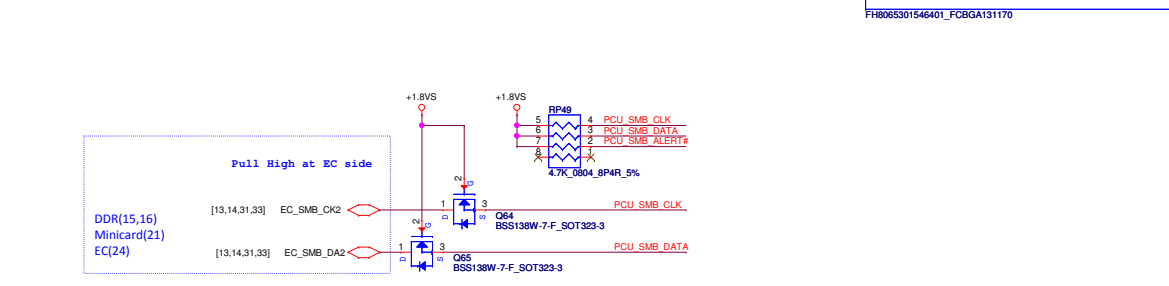
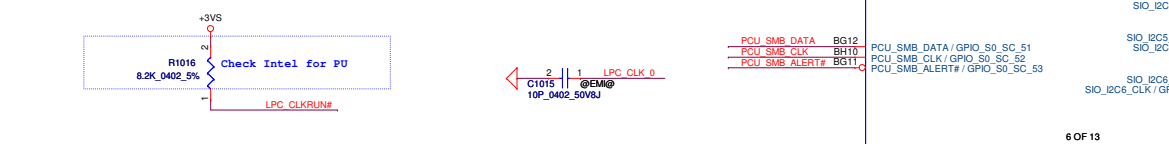
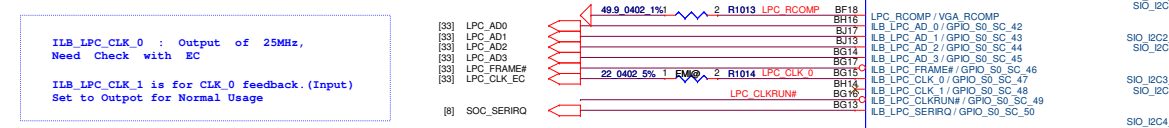
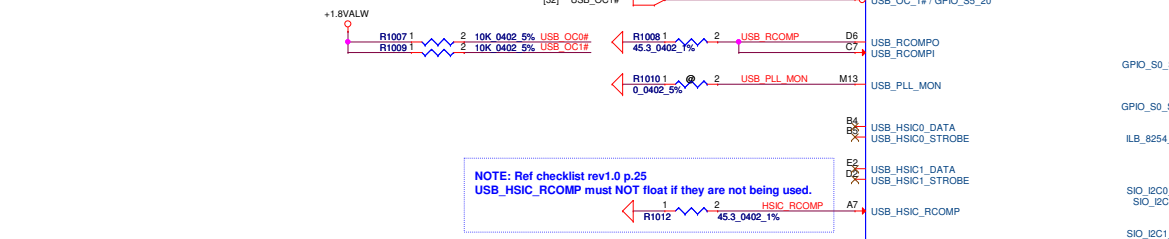
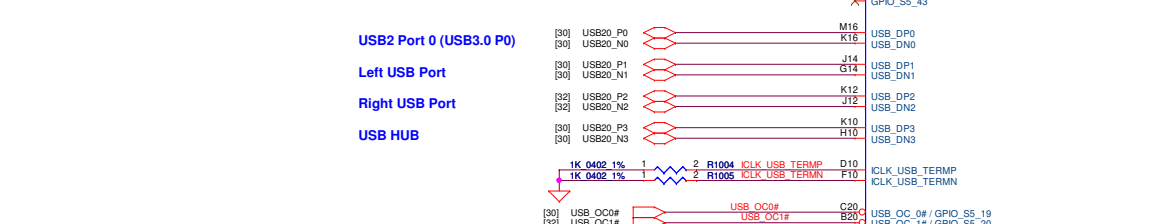
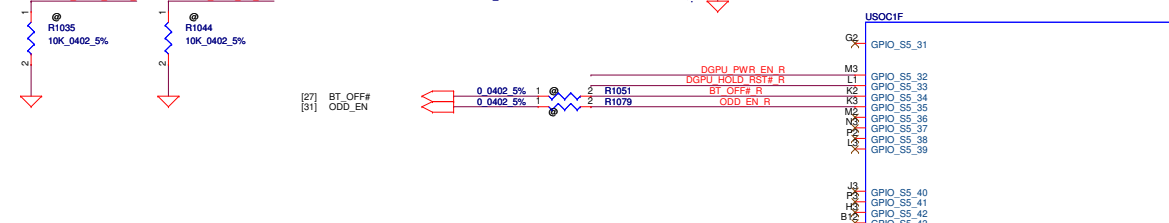
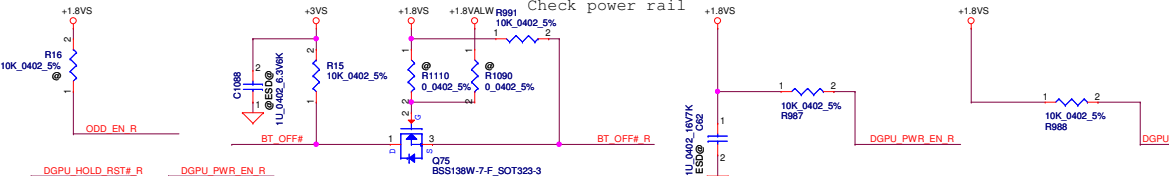
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				VLV-M SOC Display	
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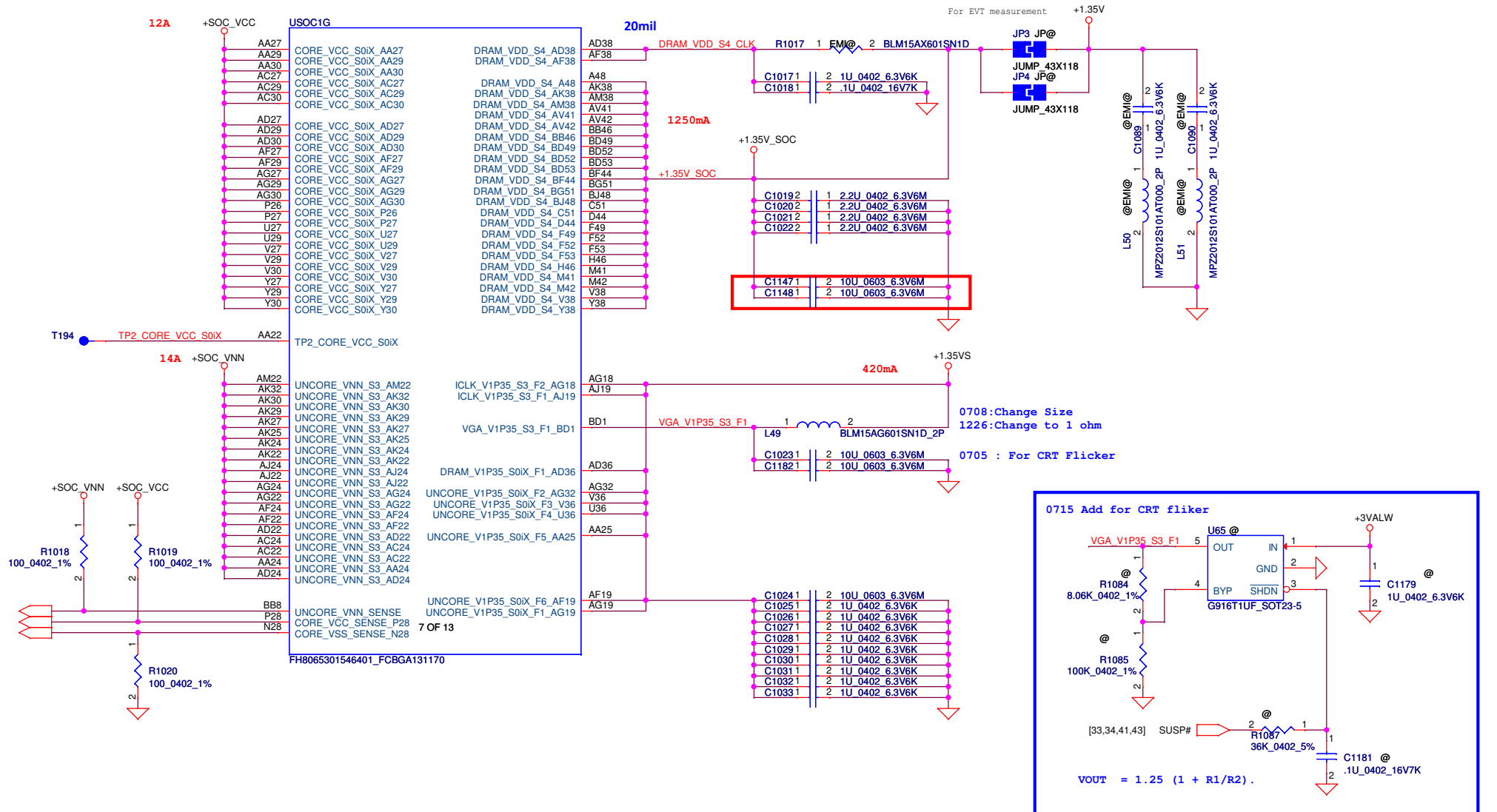


NOTE: Ref checklist rev1.0 p.25  
 USB\_HSIC\_RCOMP must NOT float if they are not being used.

ILB\_LPC\_CLK\_0 : Output of 25MHz,  
 Need Check with EC  
 ILB\_LPC\_CLK\_1 is for CLK\_0 feedback.(Input)  
 Set to Output for Normal Usage

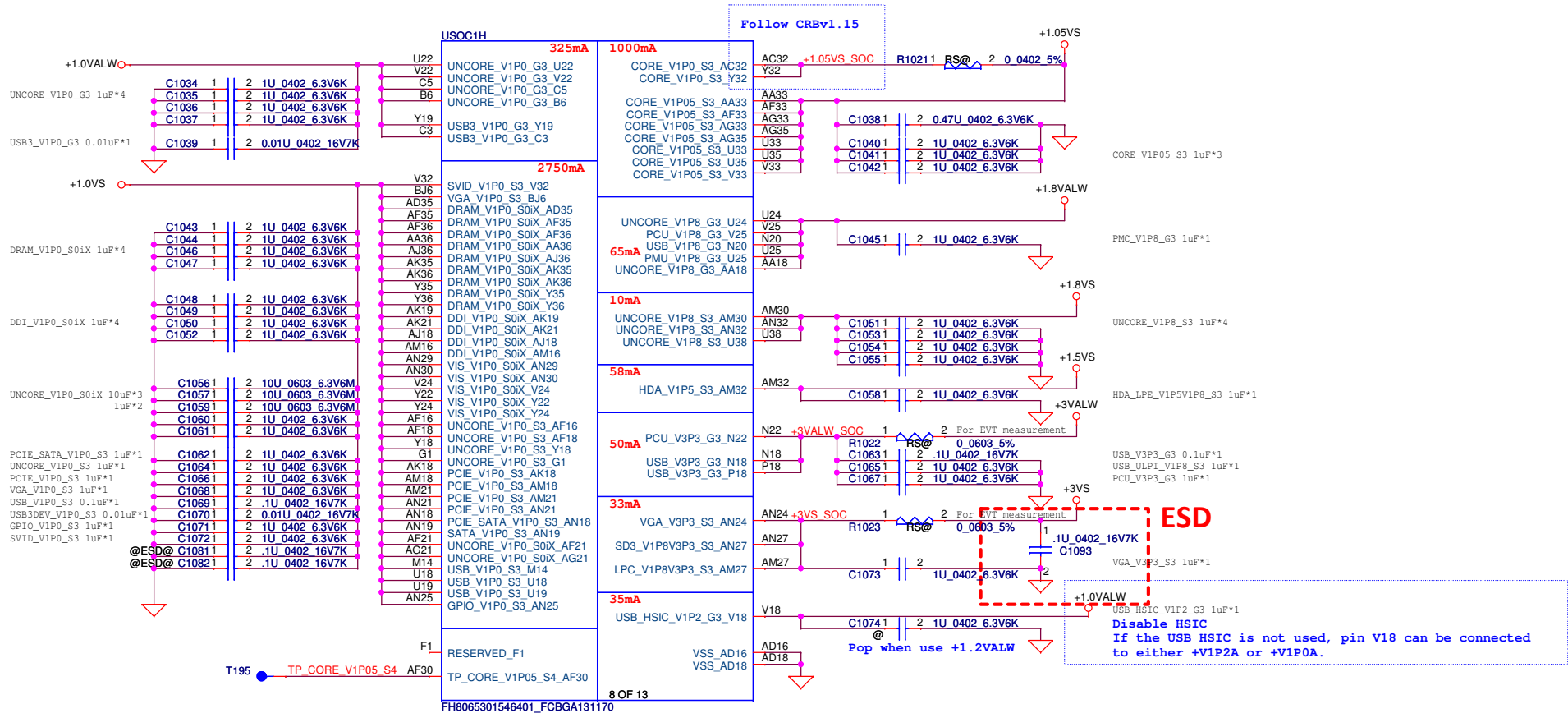
+1.8VSW  
 R1005 10K\_0402\_5%  
 R1011 10K\_0402\_5%  
 GPIO\_S0\_SC\_56:  
 A16 Swap Override  
 0 = Enable  
 1 = Disable  
 Reference EDS Page 216

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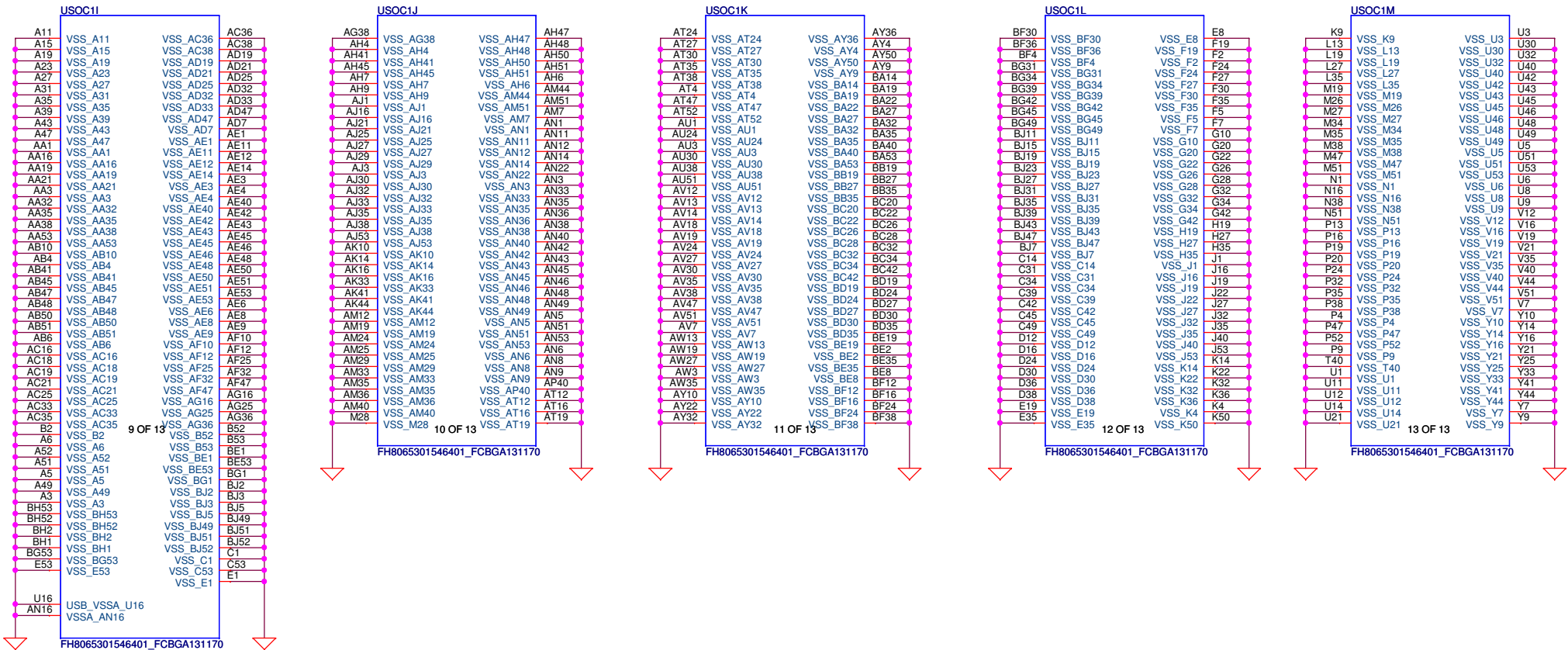


[45] VGFX\_VSNS  
 [45] VCORE\_VSNS  
 [45] VCORE\_GSNS

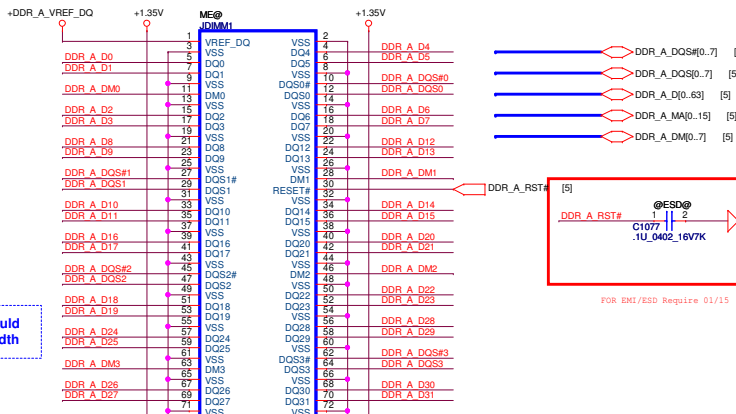
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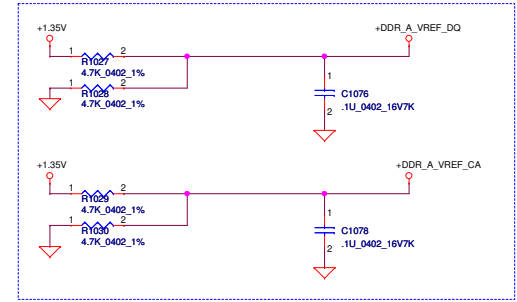
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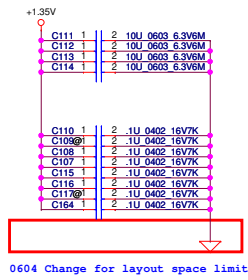


Signal voltage level = 0.675 V  
 PLACE TWO 4.7K RESISTORS CLOSE TO  
 DIMMS ON DIMM\_VREF\_CA / DIMM\_VREF\_DQ  
 Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.

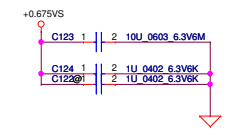


**Layout Note:**  
Place near JDIMM1

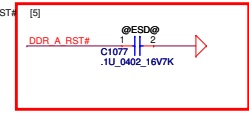
All VREF traces should have 10 mil trace width



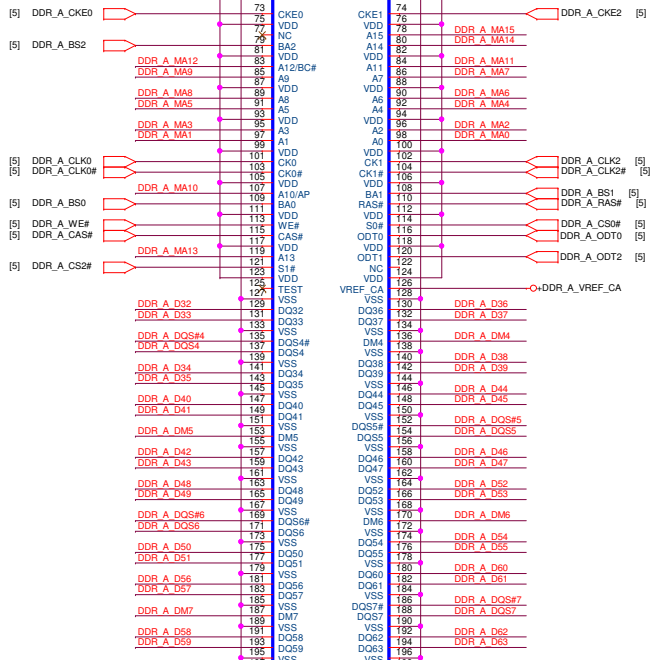
0604 Change for layout space limit



**Layout Note:**  
Place near JDIMM1.203,204



FOR EMI/ESD Require 01/15

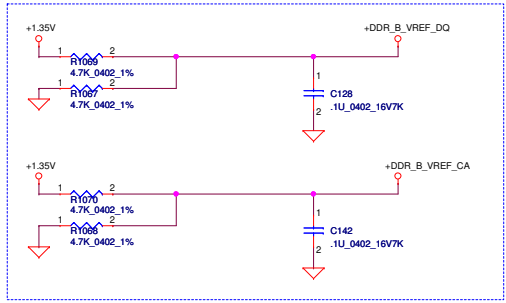
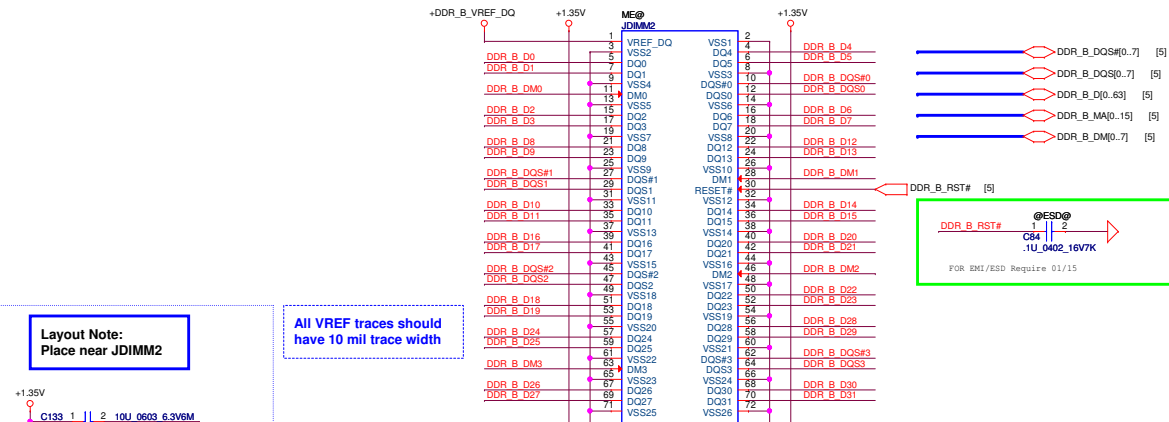


**Channel A**

<Address: SA1:SA0=00 (A0H)>  
**DIMM\_1 STD H:4mm**

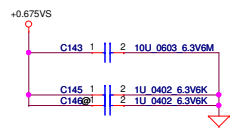
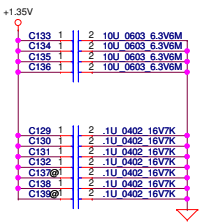
TYCO\_2-2013022-1  
 Part Number = SP0700JN10  
 PCB Footprint = TYCO\_2-2013022-1\_204P

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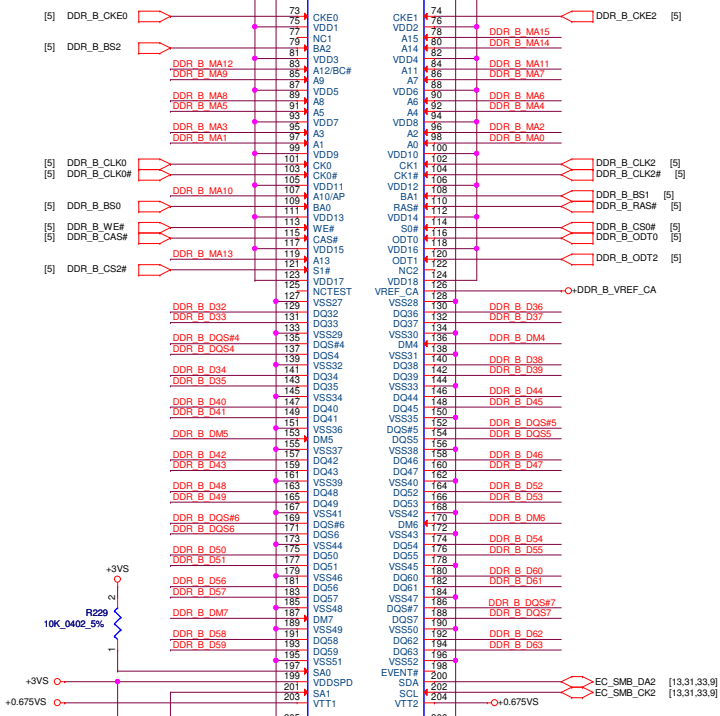


**Layout Note:**  
Place near JDIMM2

All VREF traces should have 10 mil trace width



**Layout Note:**  
Place near JDIMM2.203,204



**Channel B**

<Address: SA0:SA1=10 (A2H)>  
**DIMM\_2 REV H:4mm**

SA0/SA1 Follow INTEL demo board

TYCO\_2-2013287-1  
Part Number = SP0700KW00  
PCB Footprint = TYCO\_2-2013287-1\_204P

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Title			<b>DDR3L DIMMB</b>
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5

4

3

2

1

D

D

C

C

B

B

A

A

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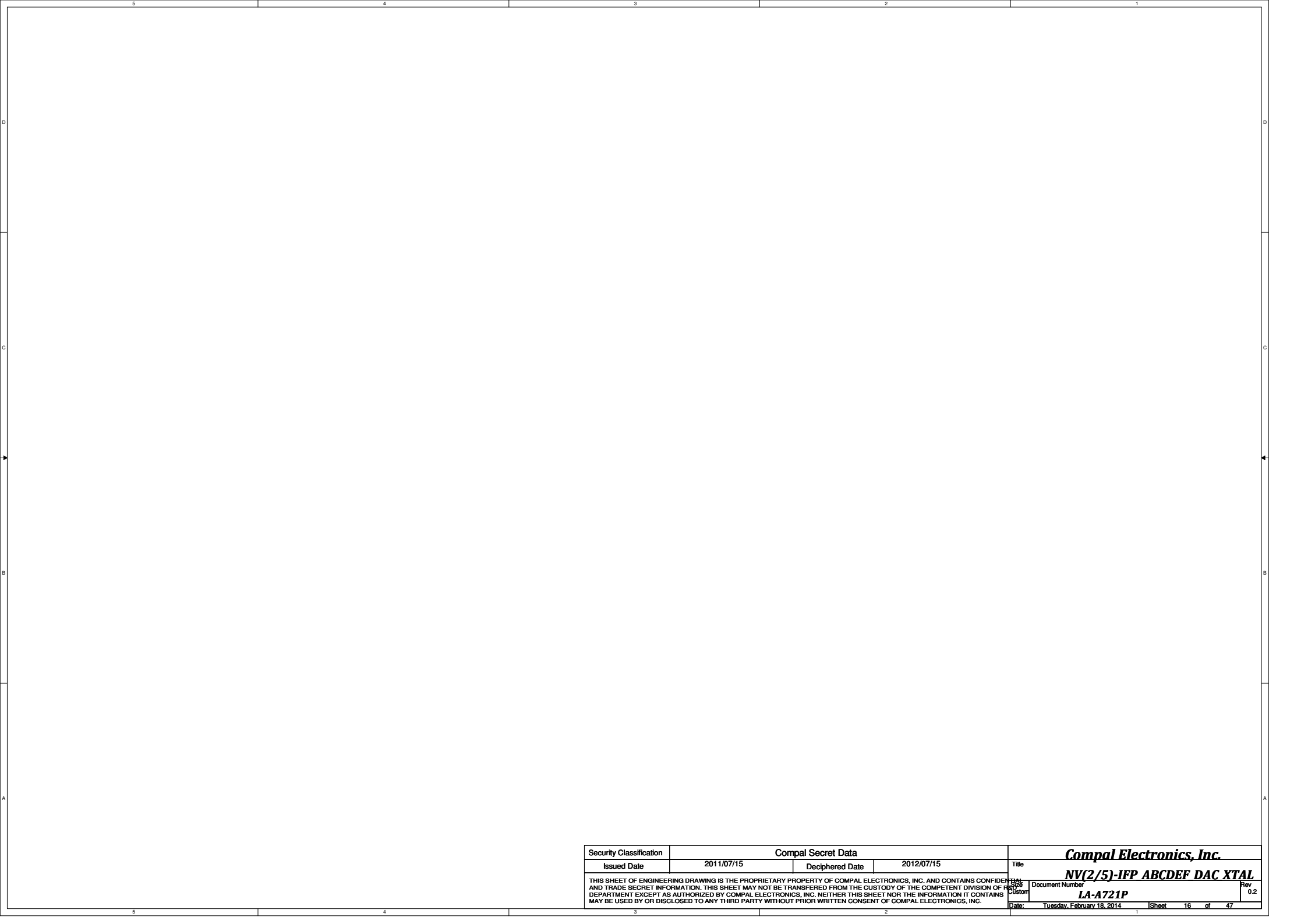
5

4

3

2

1



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5

4

3

2

1

D

D

C

C

B

B

A

A

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Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title
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5

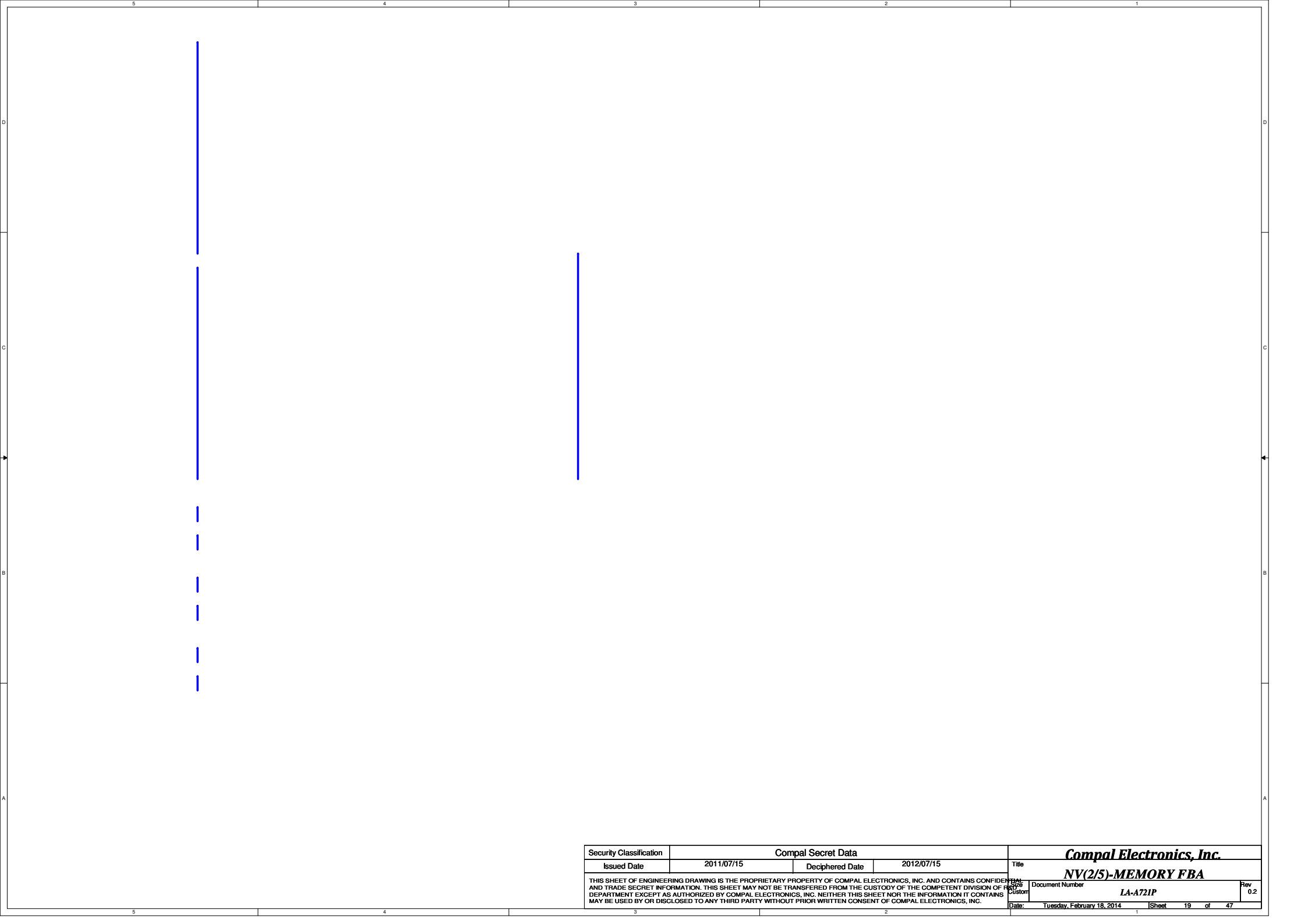
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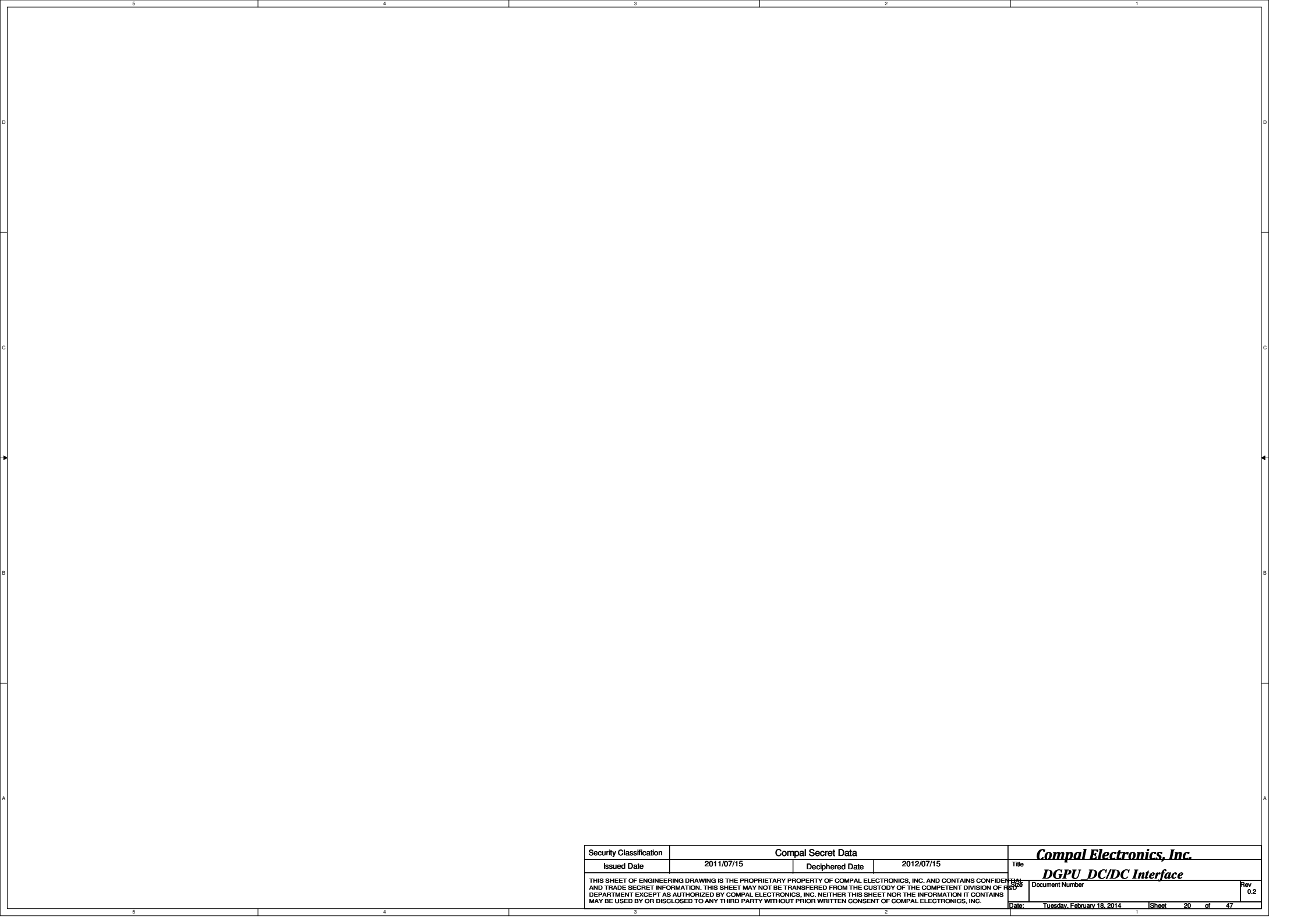
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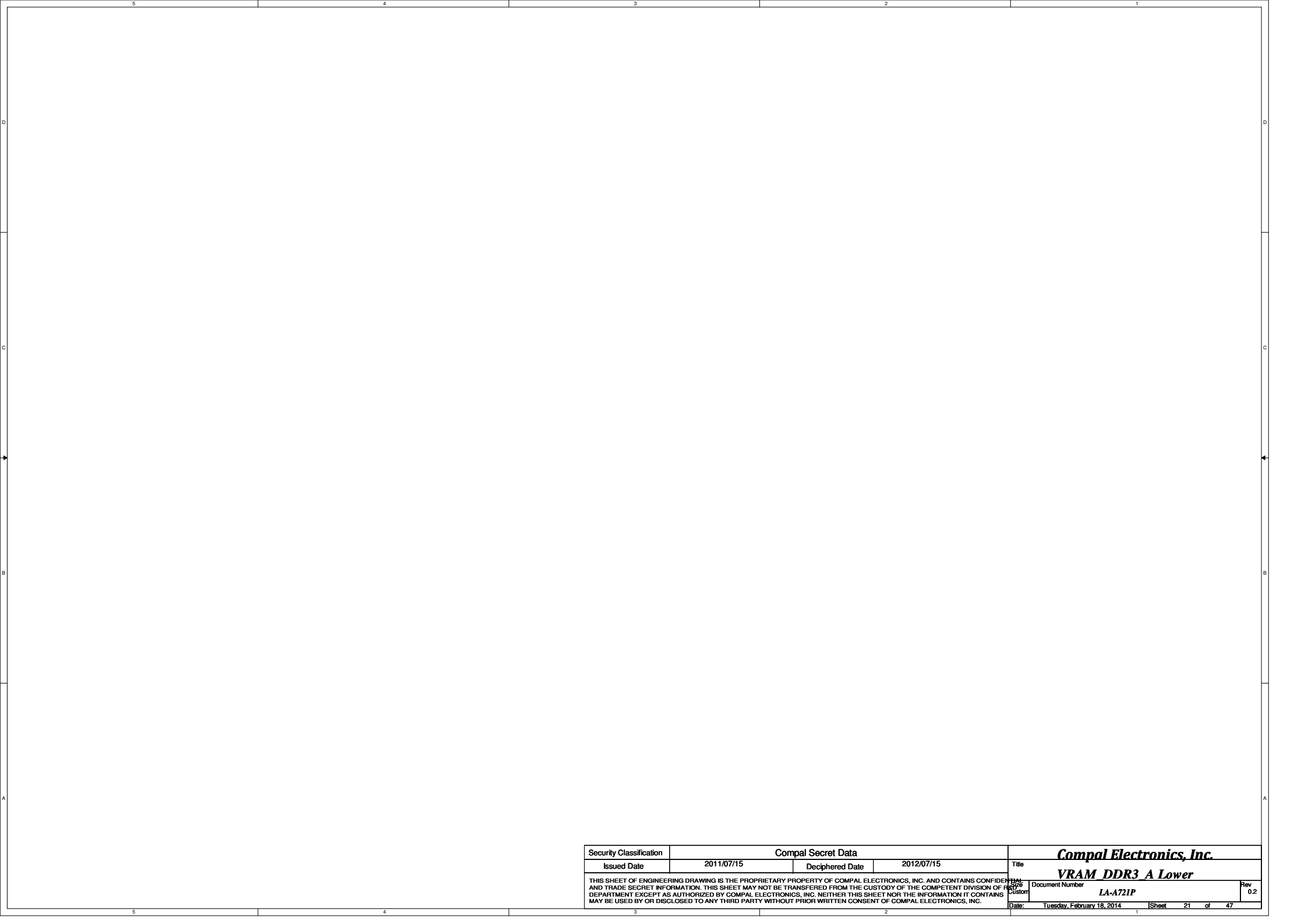
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Issued Date	2011/07/15	Deciphered Date	2012/07/15	
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			Document Number <b>LA-A721P</b>	Rev 0.2
			Sheet 18 of 47	



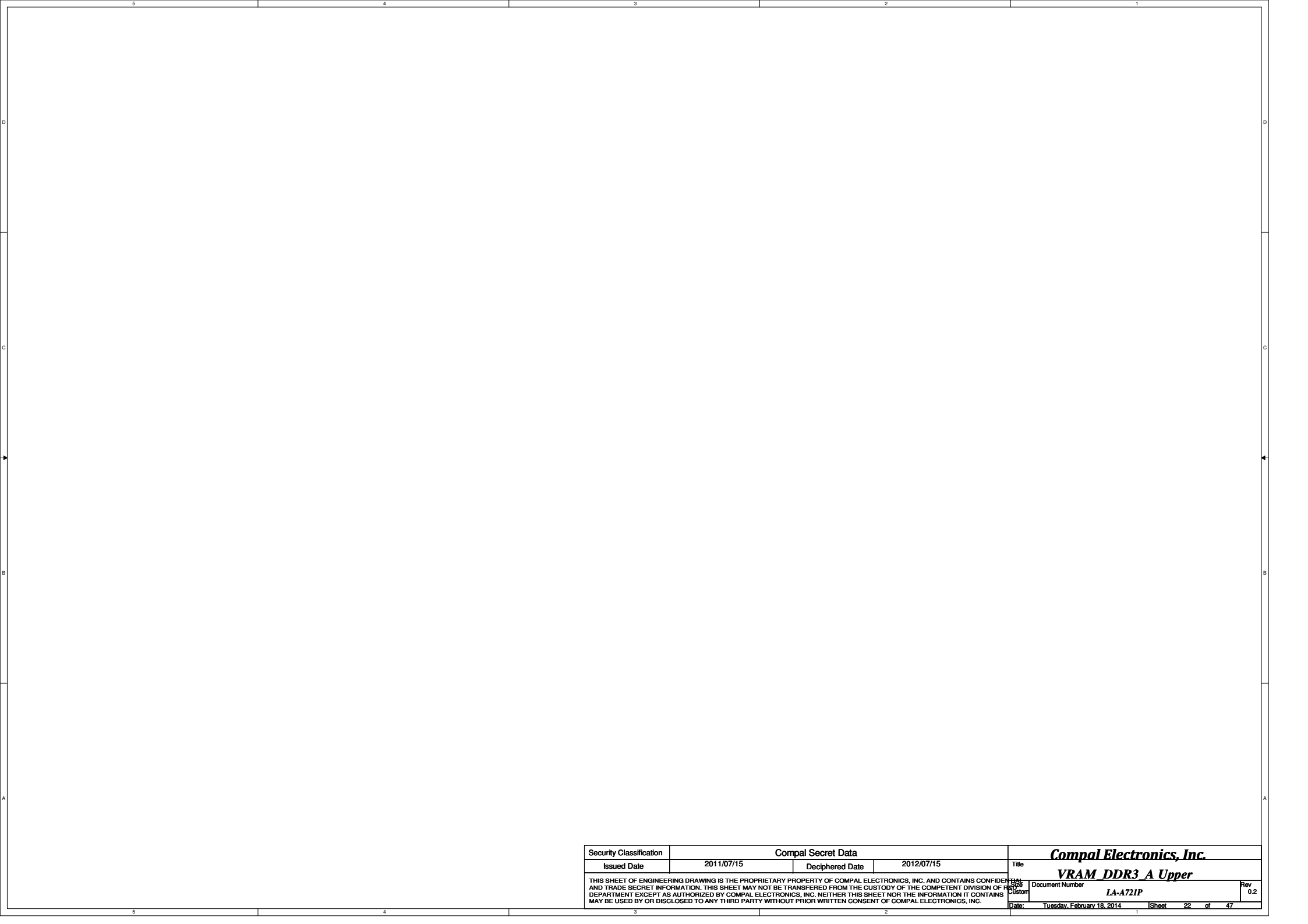
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Issued Date	2011/07/15	Deciphered Date	2012/07/15	NY(2/5)-MEMORY FBA	
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Date: Tuesday, February 18, 2014				Sheet 19 of 47	



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				Date:	Tuesday, February 18, 2014	Sheet	20 of 47

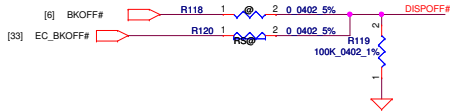
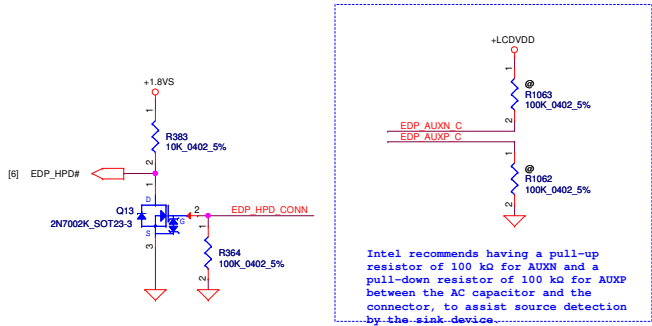
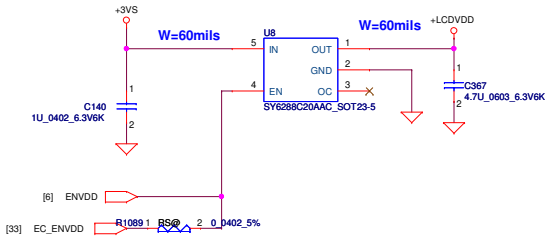


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				Customer	LA-A721P
Date: Tuesday, February 18, 2014				Sheet	21 of 47

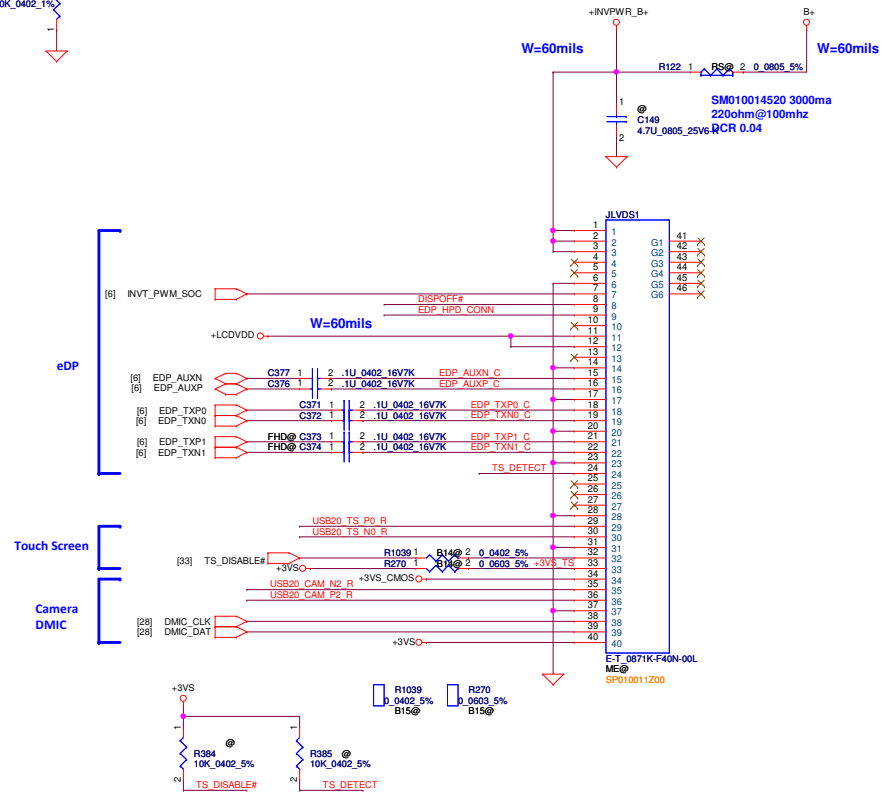


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				Document Number	0.2
Date: Tuesday, February 18, 2014				Sheet	22 of 47

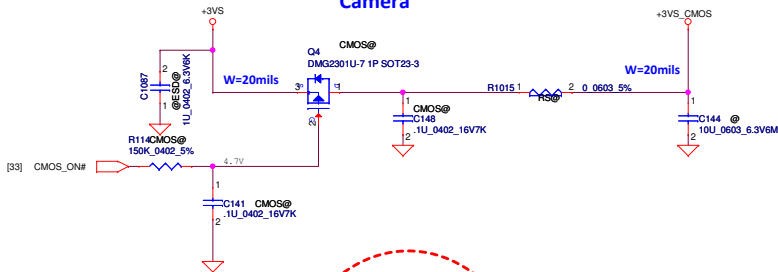
# LCD POWER CIRCUIT



# LCD/ LED PANEL Conn.

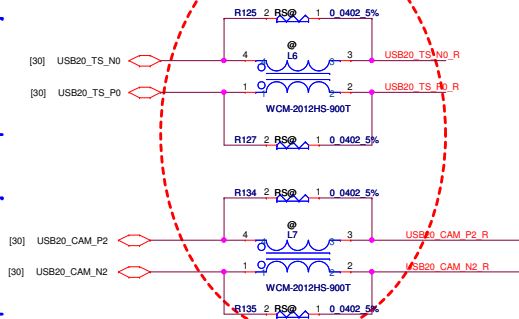


# Camera

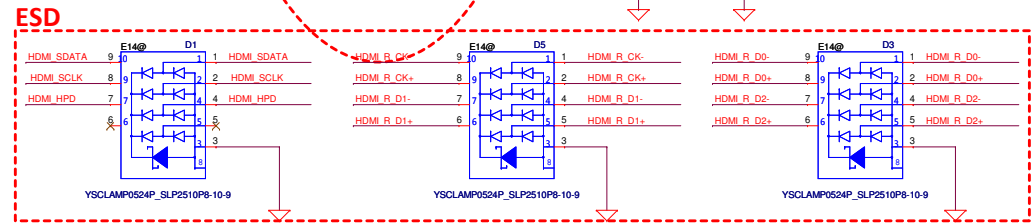
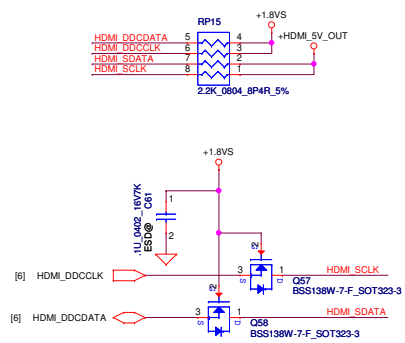
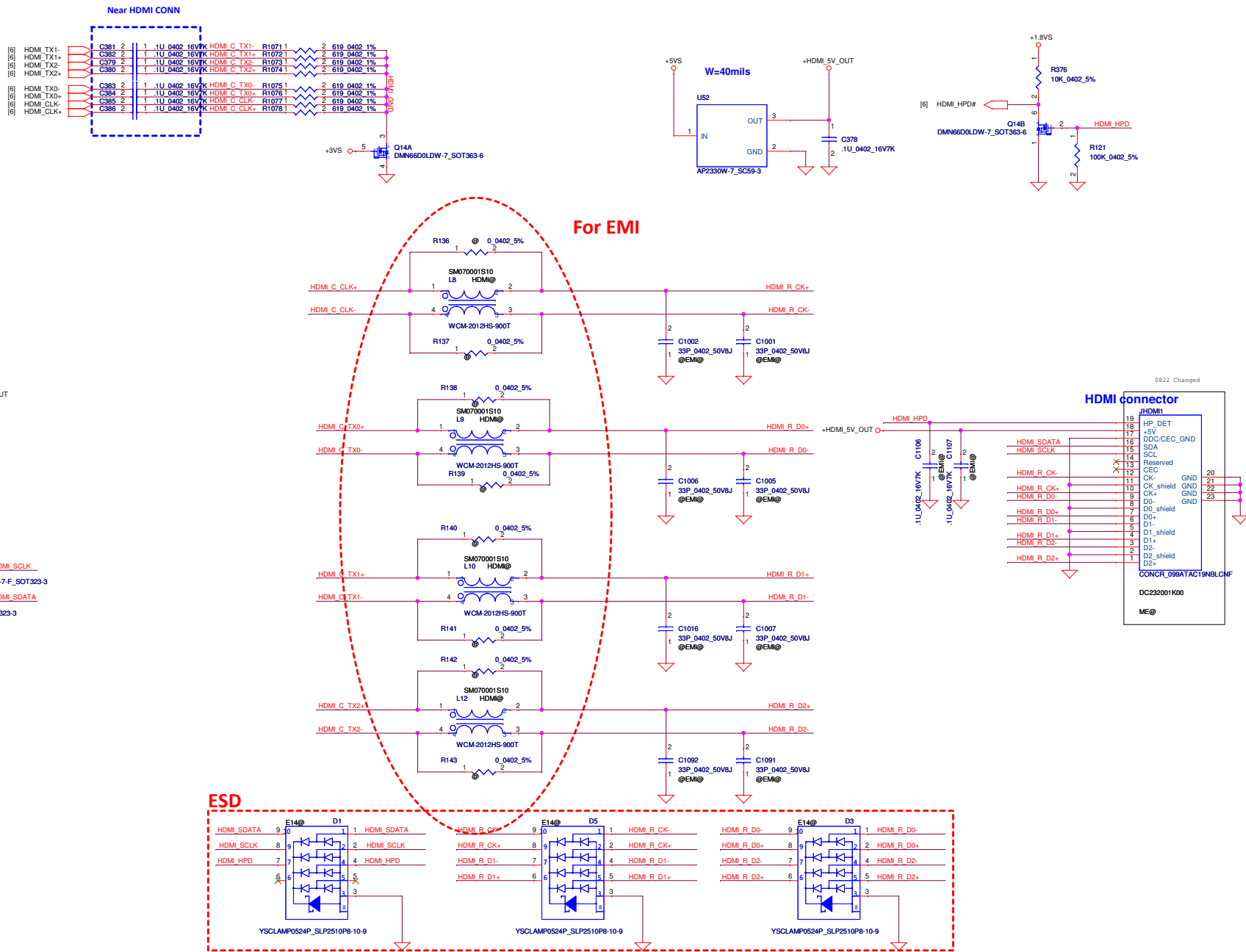


Camera

Touch Screen

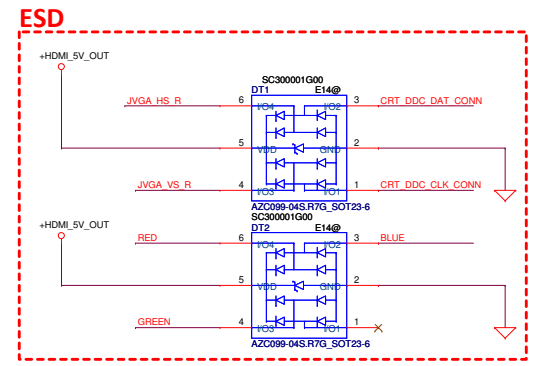
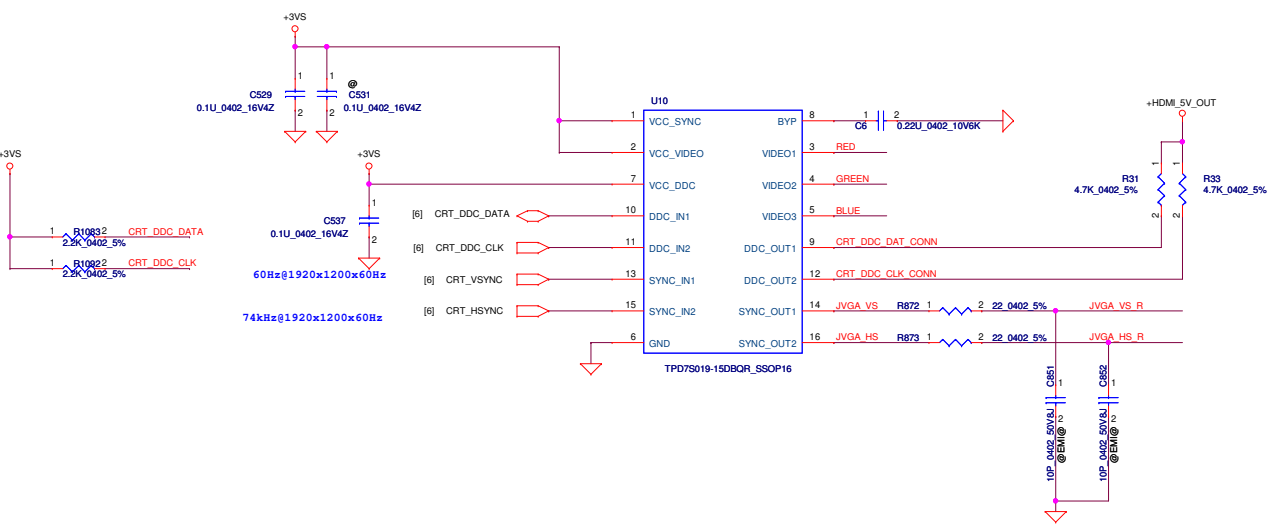
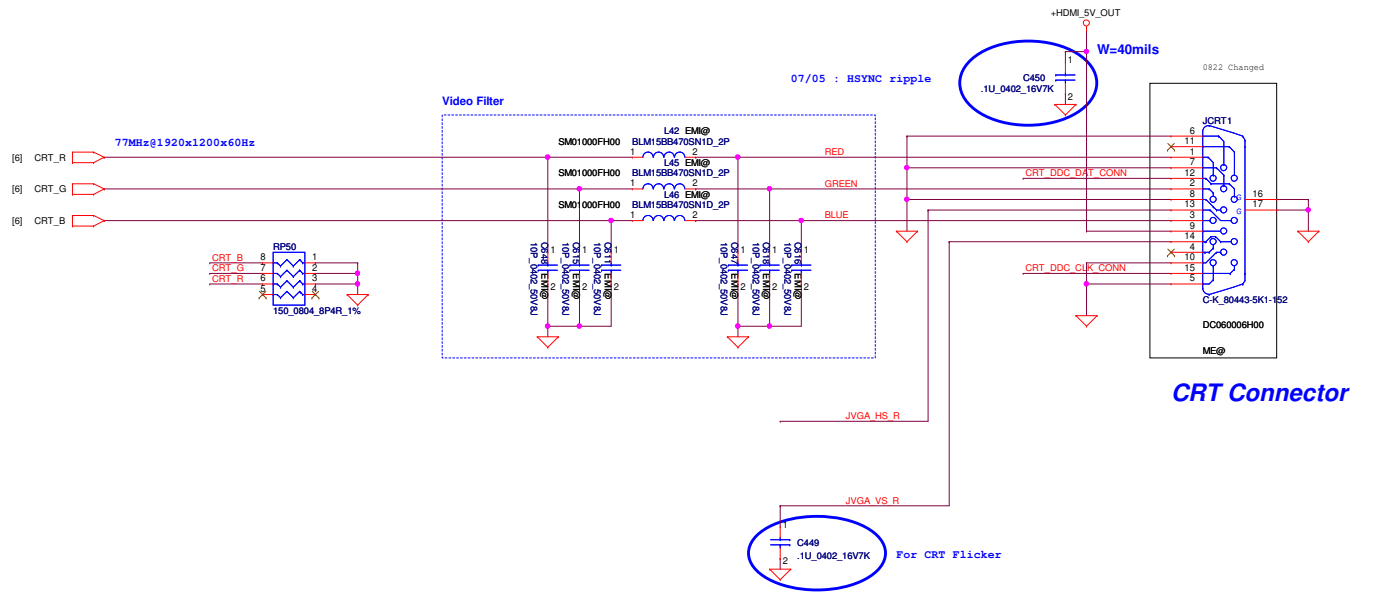


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Document Number	Customer		Rev 0.2
Date:	Tuesday, February 18, 2014	Sheet	23 of 47

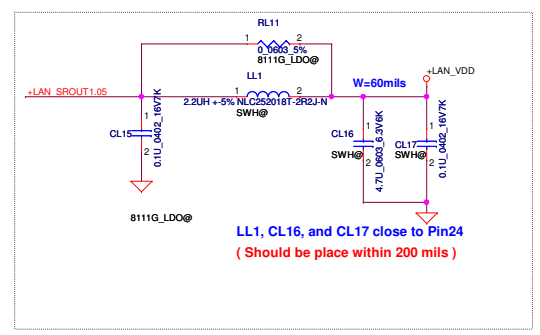
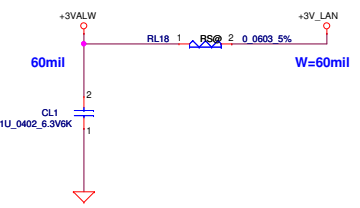


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			Customer	Intel BayTrail-M Platform	
			Date:	Tuesday, February 18, 2014	Sheet 24 of 47





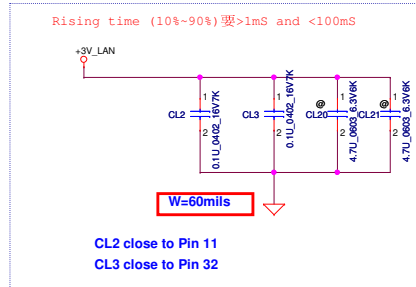
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Compal Electronics, Inc.
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Date:	Tuesday, February 18, 2014	Sheet	25	of 47



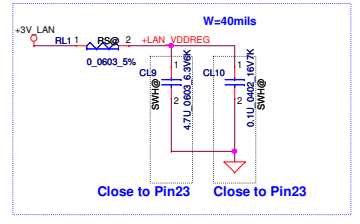
LL1, CL16, and CL17 close to Pin24  
(Should be place within 200 mils)

SA00005V700	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111G	LDO	X	X	X	O	O
RTL8111G	External	X	X	X	X	O
RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA000065Y00	LDO	X	X	X	X	X

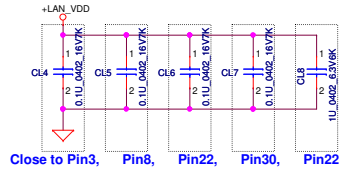
Please refer to the table above when using different 1.0V supply source.  
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.



CL2 close to Pin 11  
CL3 close to Pin 32

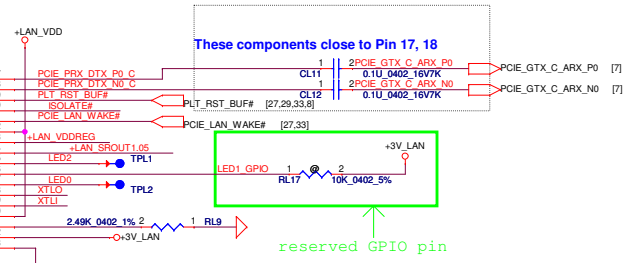
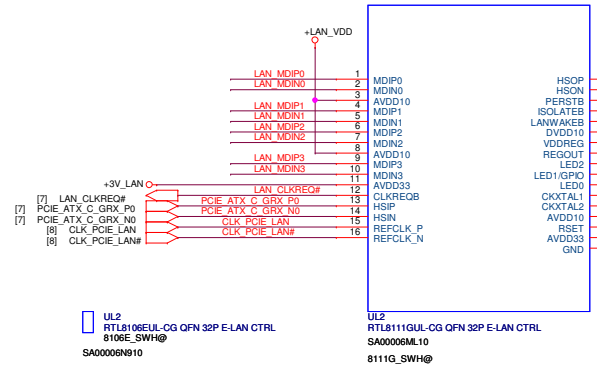
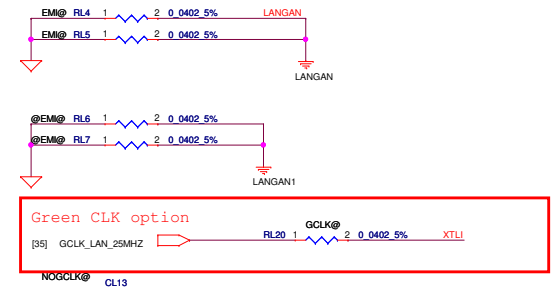
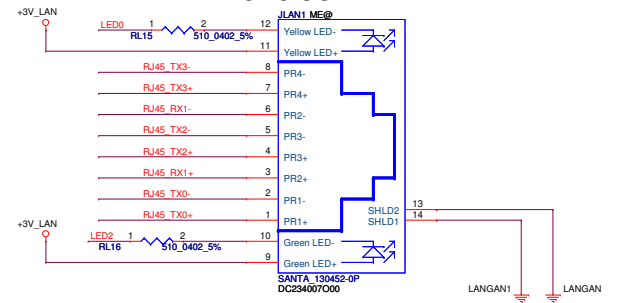


Close to Pin23 Close to Pin23



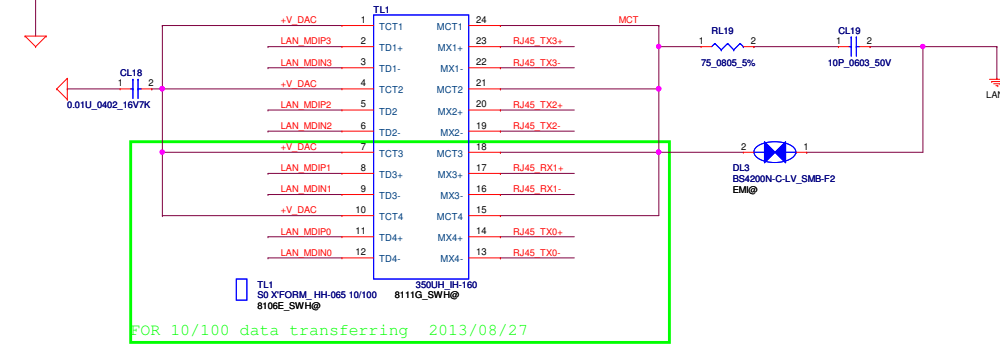
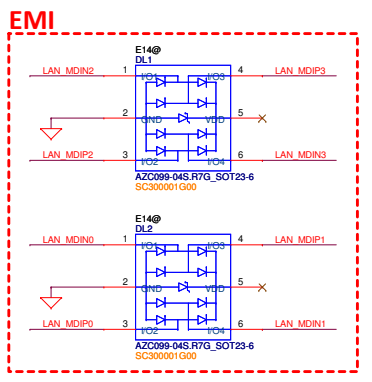
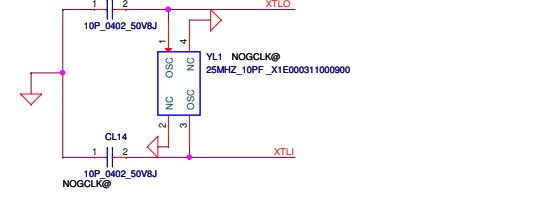
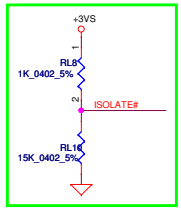
Close to Pin3, Pin8, Pin22, Pin30, Pin22

RJ-45 CONN.



These components close to Pin 17, 18

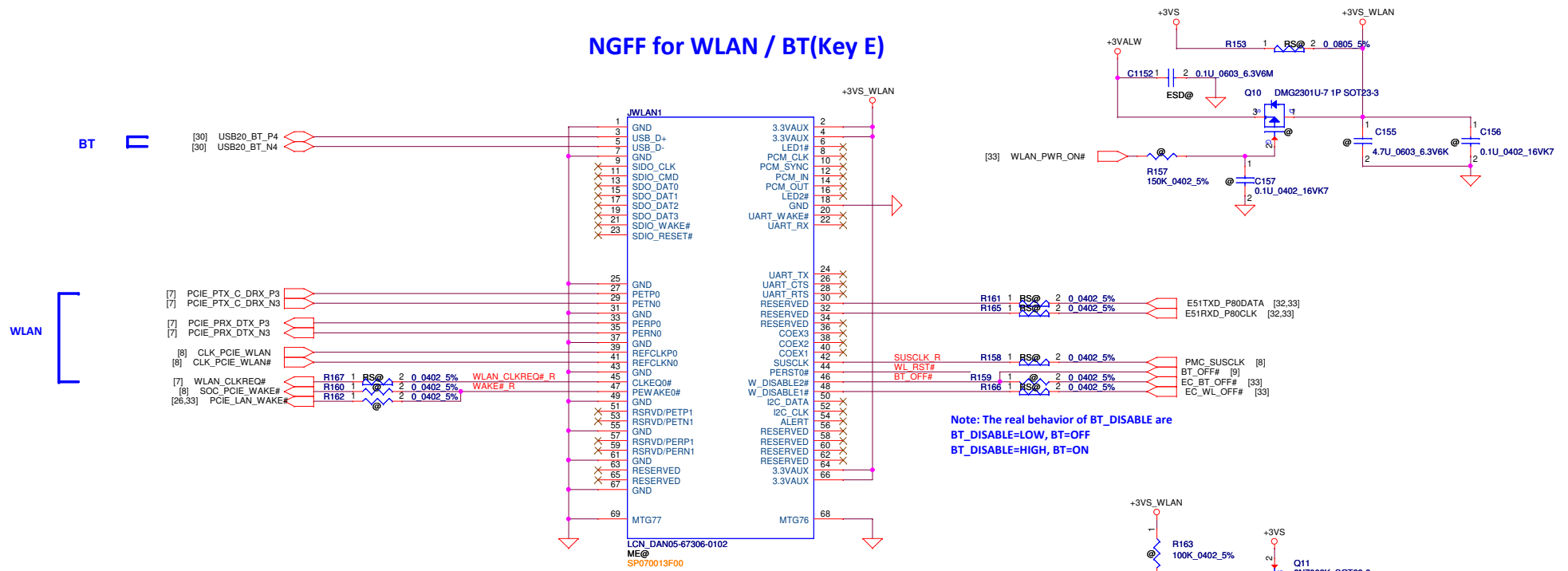
reserved GPIO pin



FOR 10/100 data transferring 2013/08/27

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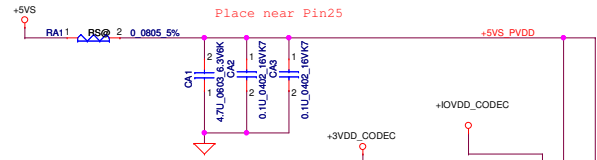
### NGFF for WLAN / BT(Key E)



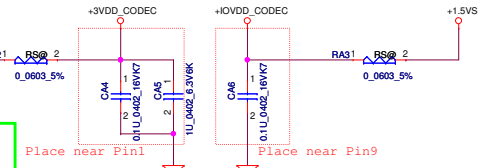
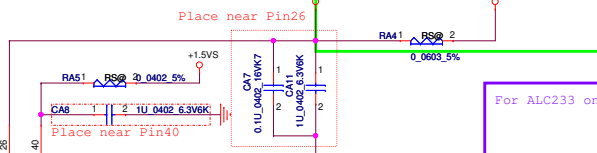
Note: The real behavior of BT\_DISABLE and BT\_DISABLE=LOW, BT=OFF  
BT\_DISABLE=HIGH, BT=ON

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				Customer	Intel BayTrail-M Platform
				Date	Tuesday, February 18, 2014
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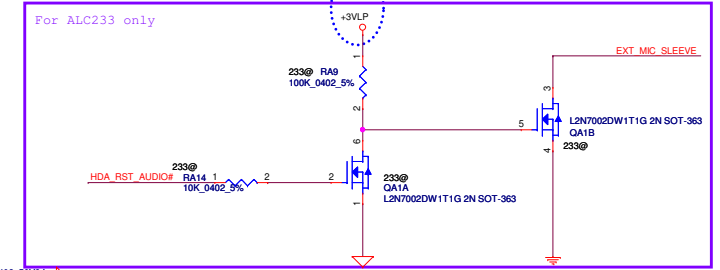
600ohms @100MHz 2A  
P/N: SM01000E200



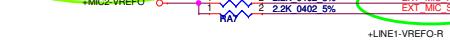
Place RA41 on AGND/DGND moat



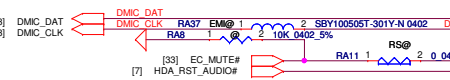
Change power rail from +CHGRIC to +3VLP



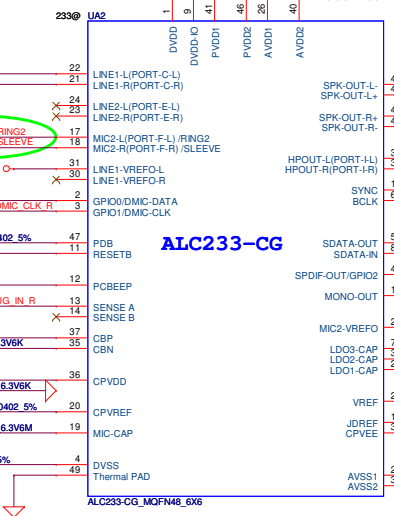
wide 40MIL



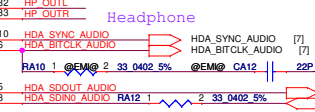
External DMIC



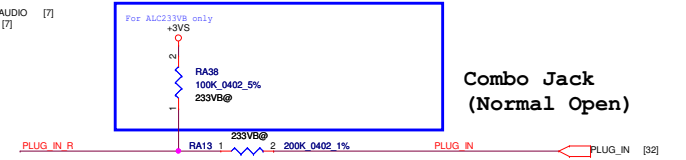
ALC233-CG



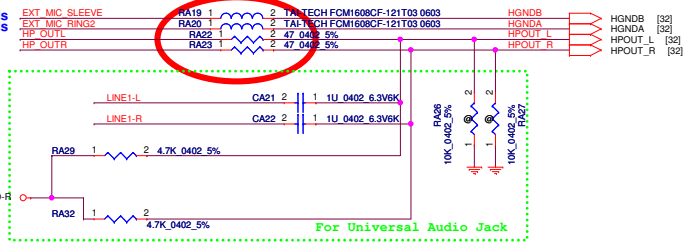
Headphone



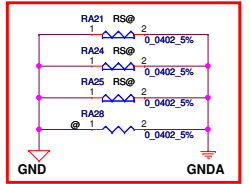
Combo Jack (Normal Open)



W=40mils



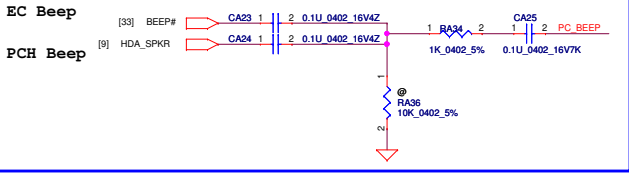
For EMI



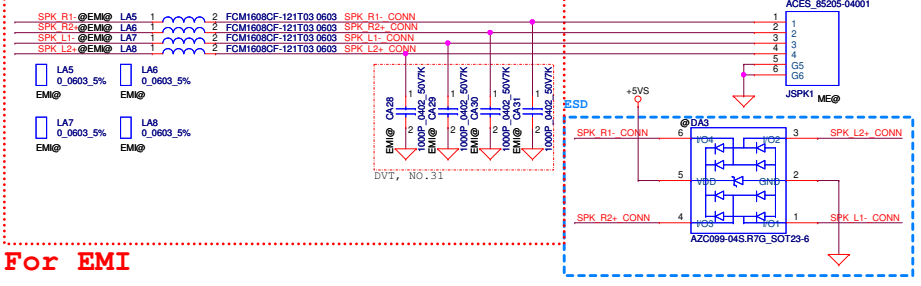
UA2  
ALC233-VB2-CG MOFN 48P  
233V@  
SA00007BF10

follow vendor suggest  
& reserve default design

PC Beep

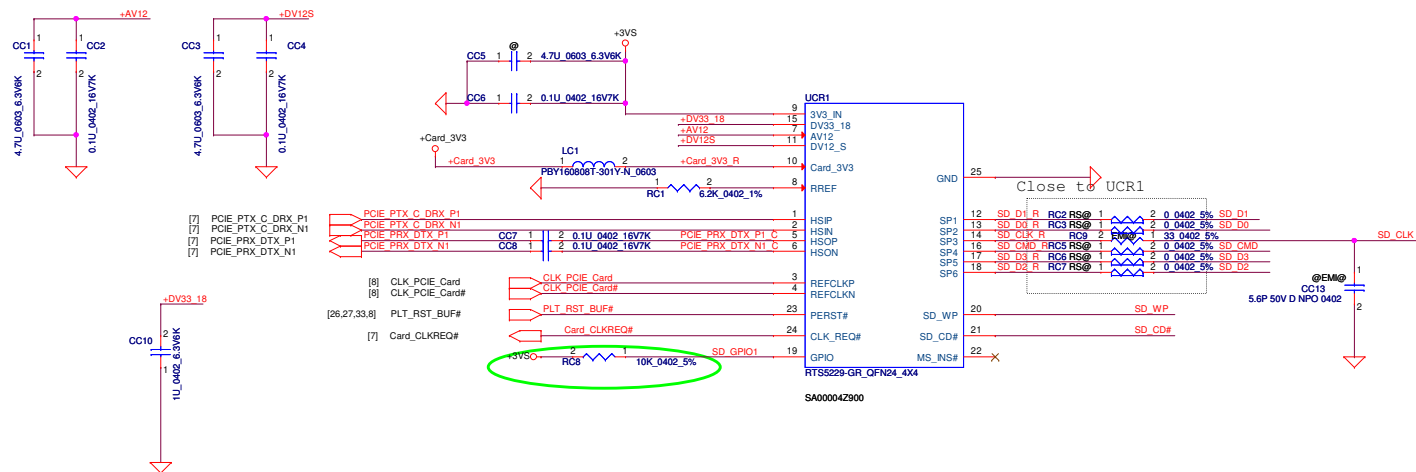


wide 40MIL

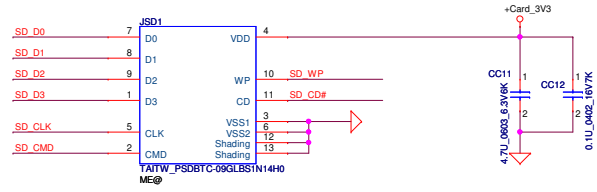


For EMI

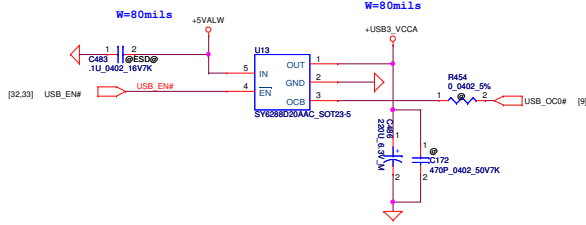
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<p>HD Audio Codec ALC3225</p>				<p>Rev 0.2</p>
<p>Sheet 28 of 47</p>				



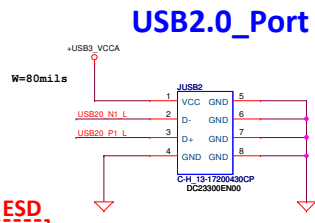
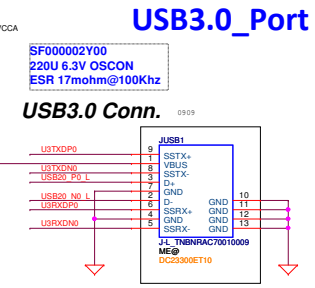
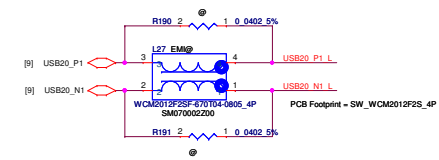
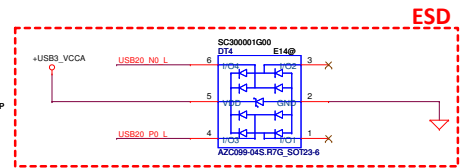
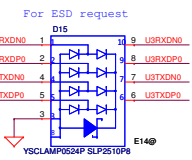
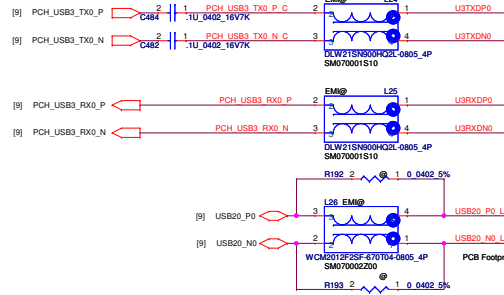
**SD/SDXC**



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Date:	Tuesday, February 18, 2014	Sheet	29	of 47

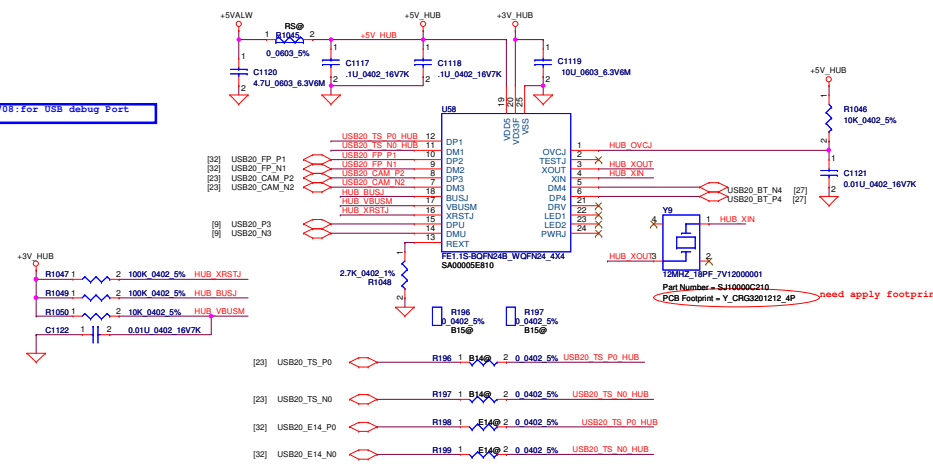


**SM07000S80 WCM2012F2SF-670T04 67ohm**



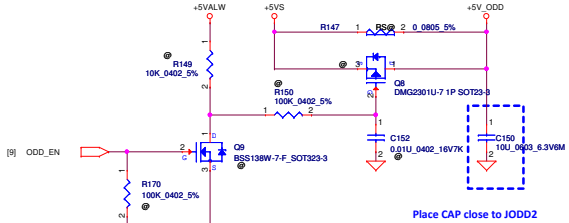
**USB2.0 HUB**

0709: for USB debug Port



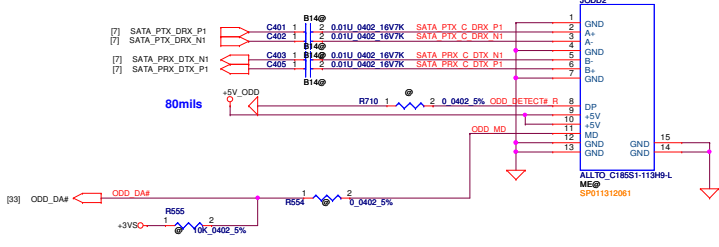
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12
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Size	Document Number	Rev	
Custom		0.2	
Date:	Tuesday, February 18, 2014	Sheet	30 of 47

ODD

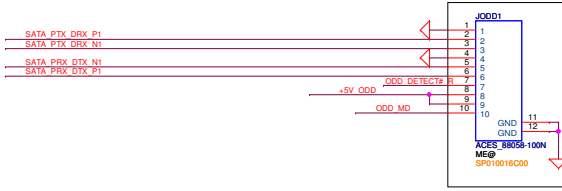


FOR 14"

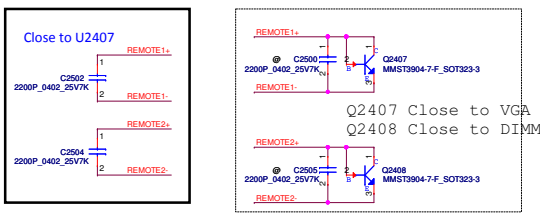
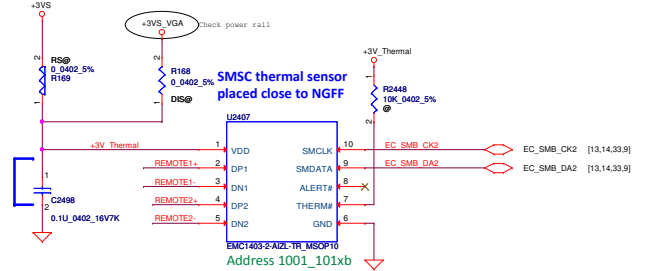
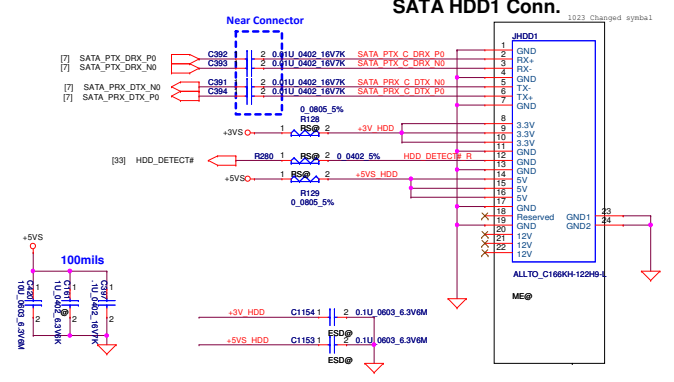
SATA ODD Conn.



FOR 15" SATA ODD FFC Conn.

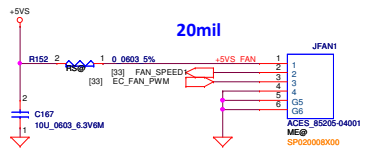


HDD

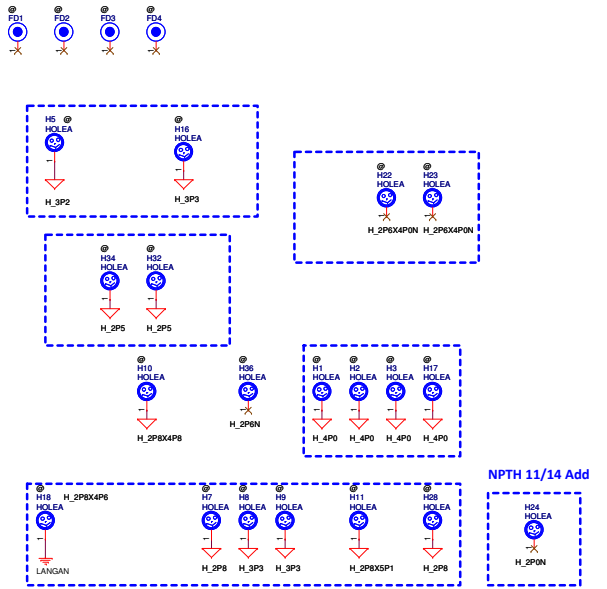
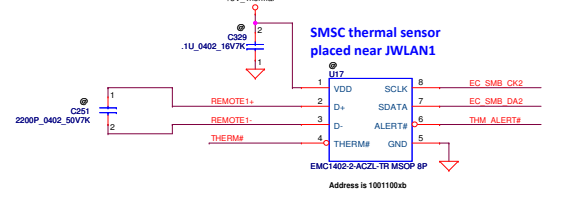


REMOTE1,2 (+/-): Trace width/space:10/10 mil Trace length:<8"

FAN Conn

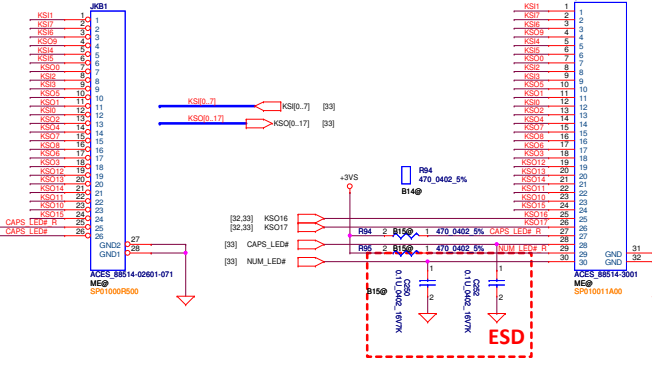


2 Channel

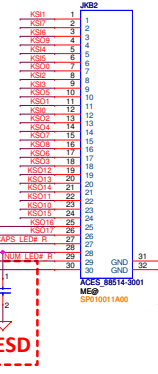


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Size	Document Number	Revision		Rev 0.2		
Date:	Tuesday, February 18, 2014	Sheet	31	of 47		

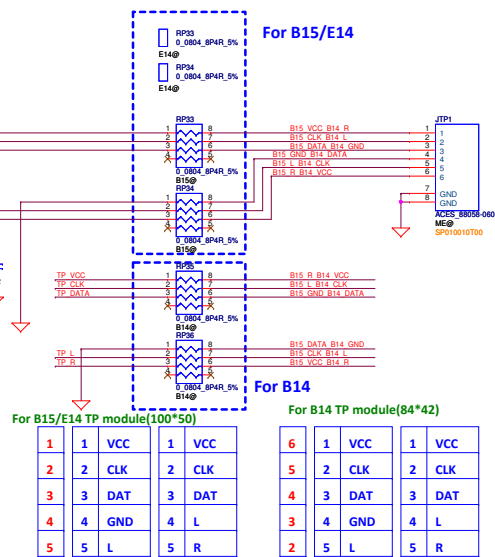
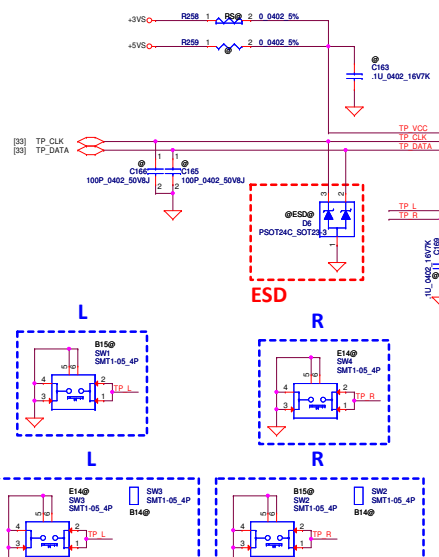
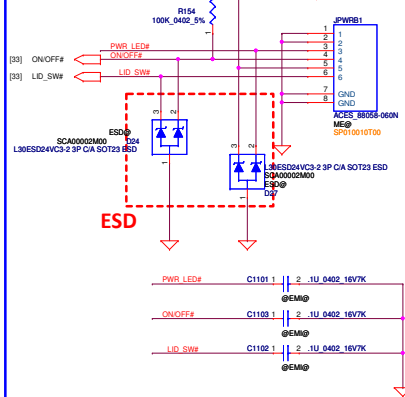
KB For B14/E14



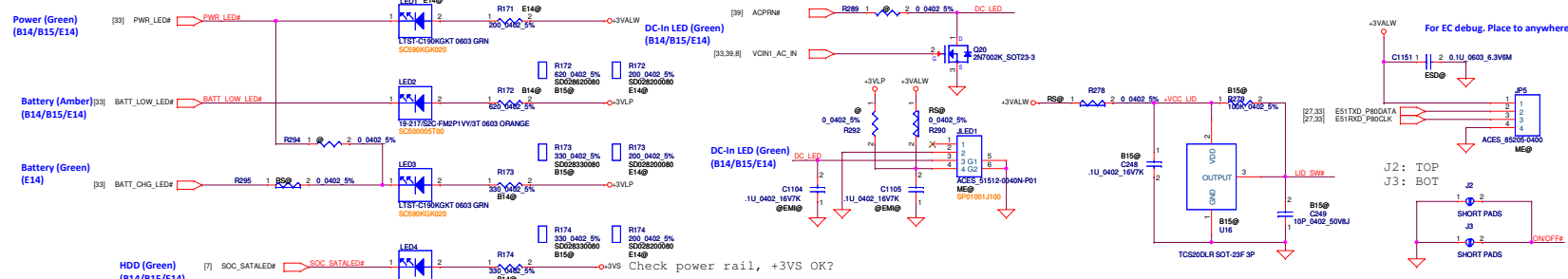
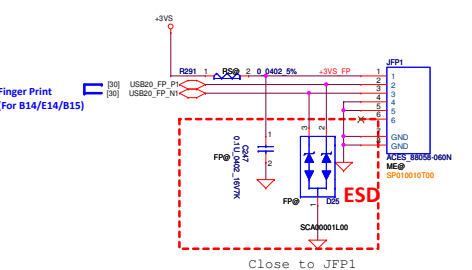
KB For B15



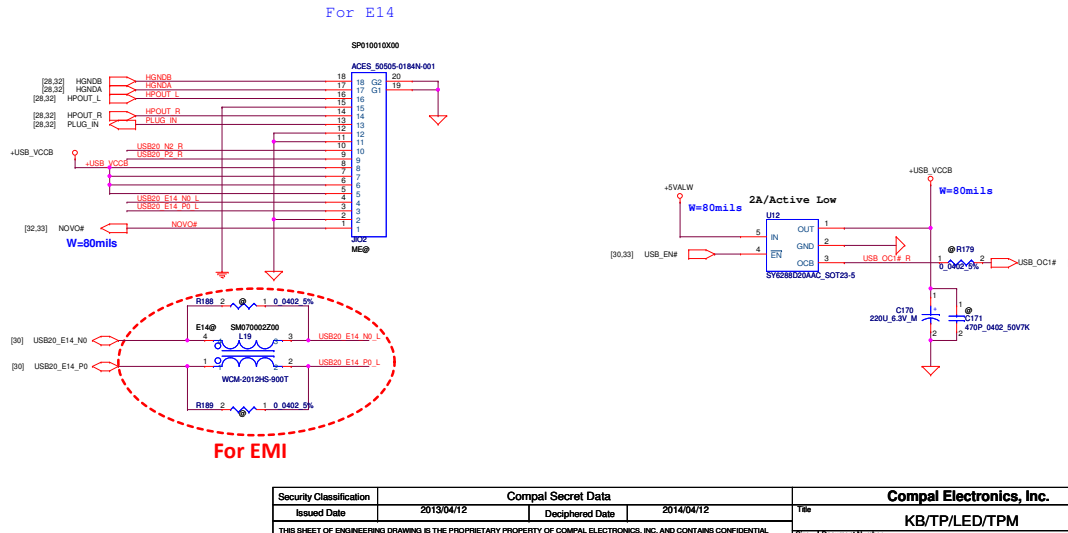
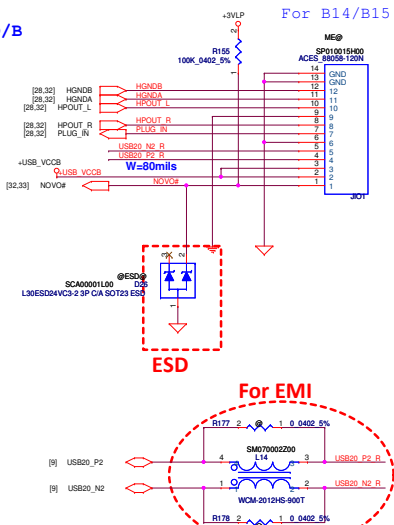
PWR/B conn.



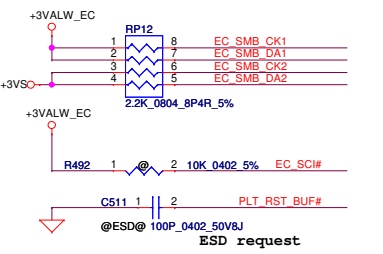
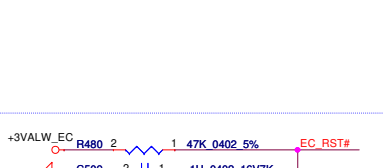
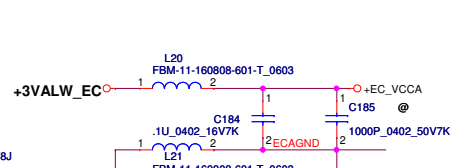
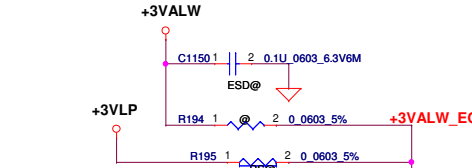
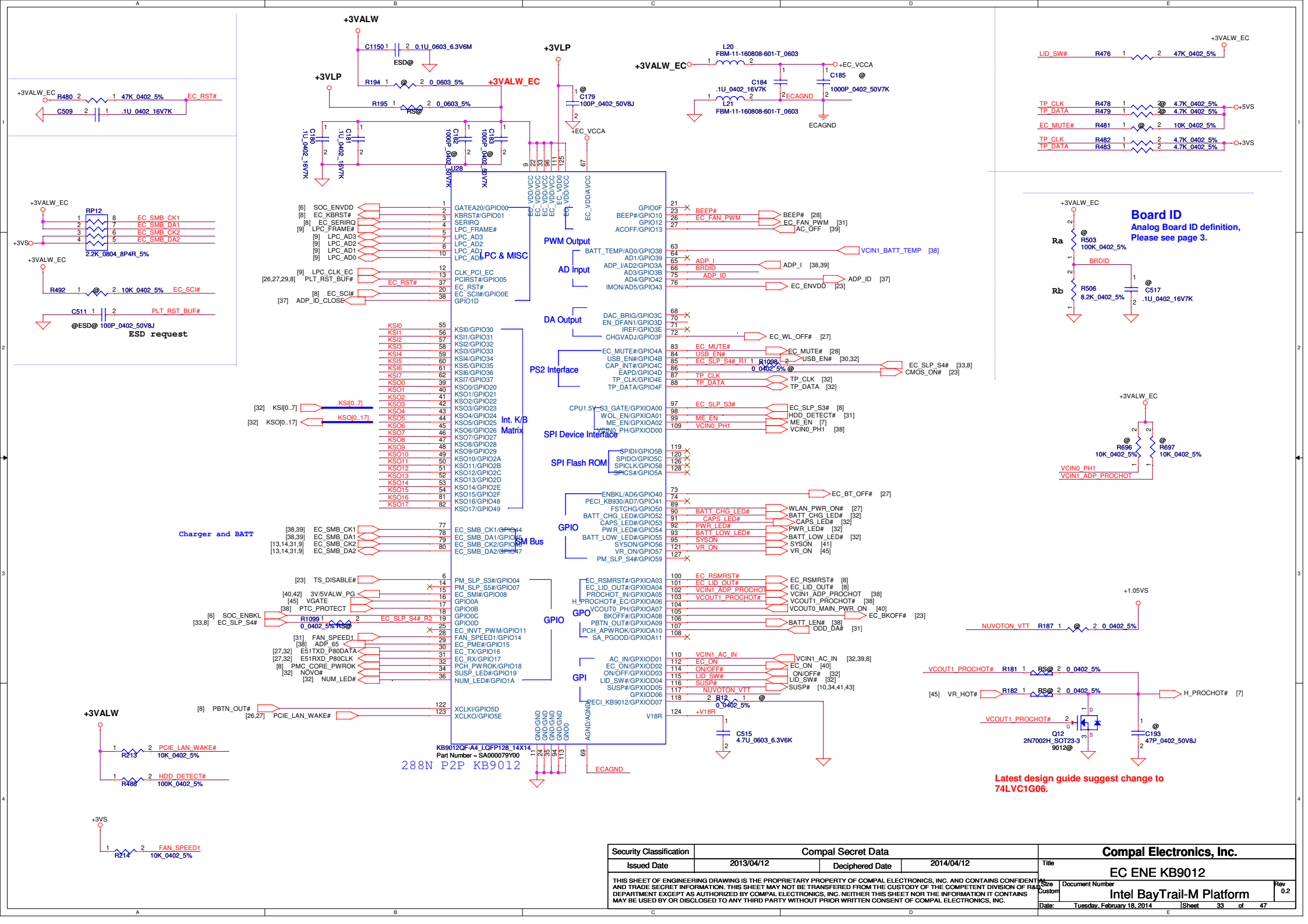
Finger Printer conn.



IO/B







**PC & MISC**

[6]	SOC_ENVDD	1	GATEA20/GPIO00
[8]	EC_KBRST#	2	KBRST#/GPIO01
[8]	EC_SERIRQ	3	SERIRQ
[5]	LPC_FRAME#	4	LPC_FRAME#
[9]	LPC_AD3	5	LPC_AD3
[9]	LPC_AD2	6	LPC_AD2
[9]	LPC_AD1	7	LPC_AD1
[9]	LPC_AD0	8	LPC_AD0
[9]	LPC_CLK_EC	12	CLK_PCL_EC
[26,27,29,8]	PLT_RST_BUF#	13	PCIRST#/GPIO05
[8]	EC_SCI#	37	EC_RST#
[37]	ADP_ID_CLOSE	20	EC_SCI#/GPIO0E
		38	GPIO1D

**Int. K/B Matrix**

[32]	KS1[0..7]	KS10	55	KS10/GPIO30
		KS11	56	KS11/GPIO31
		KS12	57	KS12/GPIO32
		KS13	58	KS13/GPIO33
		KS14	59	KS14/GPIO34
		KS15	60	KS15/GPIO35
		KS16	61	KS16/GPIO36
		KS17	62	KS17/GPIO37
		KS00	39	KS00/GPIO29
		KS01	40	KS01/GPIO21
		KS02	41	KS02/GPIO22
		KS03	42	KS03/GPIO23
		KS04	43	KS04/GPIO24
		KS05	44	KS05/GPIO25
		KS06	45	KS06/GPIO26
		KS07	46	KS07/GPIO27
		KS08	47	KS08/GPIO28
		KS09	48	KS09/GPIO29
		KS10	49	KS10/GPIO2A
		KS11	50	KS11/GPIO2B
		KS12	51	KS12/GPIO2C
		KS13	52	KS13/GPIO2D
		KS14	53	KS14/GPIO2E
		KS15	54	KS15/GPIO2F
		KS16	81	KS16/GPIO48
		KS17	82	KS17/GPIO49

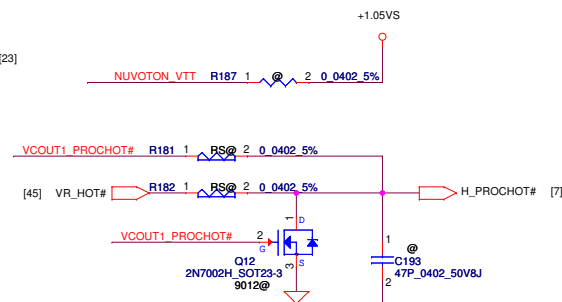
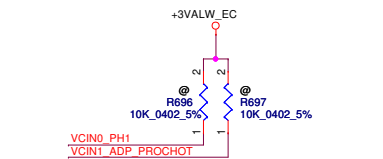
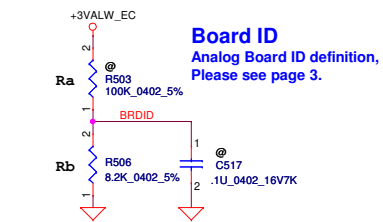
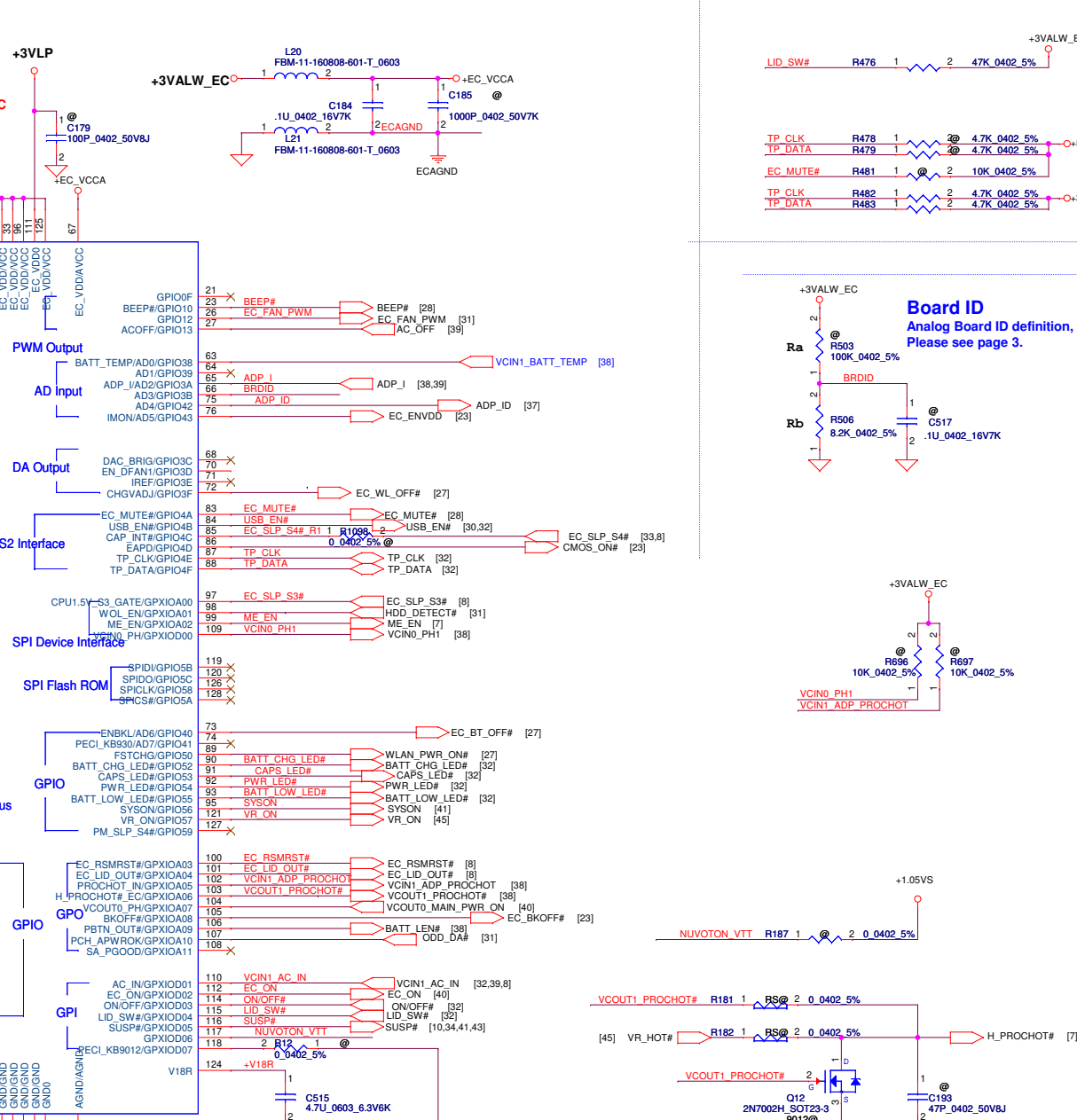
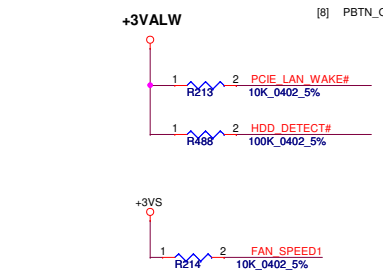
**Charger and BATT**

[38,39]	EC_SMB_CK1	77	EC_SMB_CK1/GPIO44
[38,39]	EC_SMB_DA1	78	EC_SMB_DA1/GPIO45
[13,14,31,9]	EC_SMB_CK2	79	EC_SMB_CK2/GPIO46
[13,14,31,9]	EC_SMB_DA2	80	EC_SMB_DA2/GPIO47

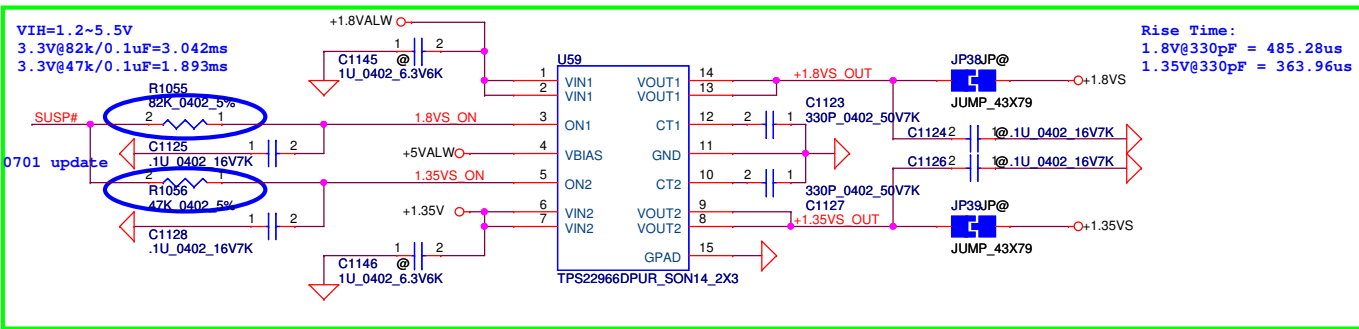
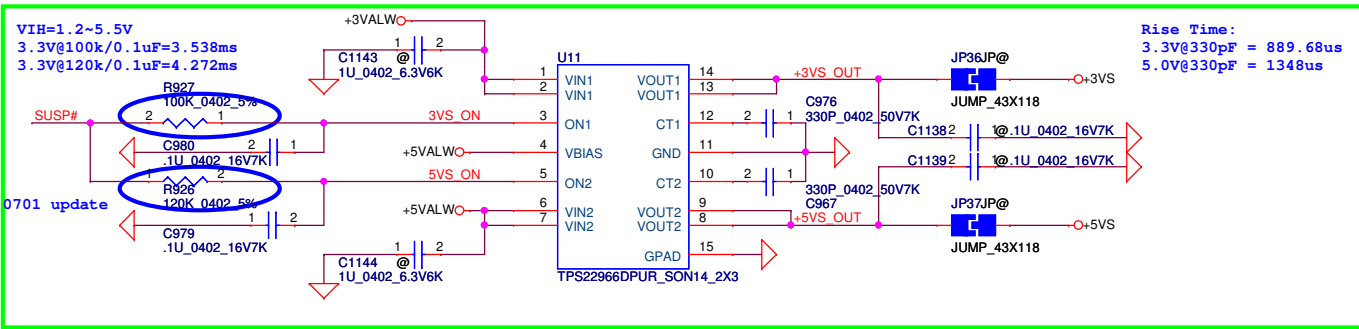
**GPIO**

[23]	TS_DISABLE#	6	PM_SLP_S3#/GPIO04
[40,42]	3V5VALW_PG	15	PM_SLP_S5#/GPIO07
[15]	VGATE	16	EC_SM#/GPIO08
[45]	PTC_PROTECT	17	GPIO0B
[6]	SOC_ENBK1	18	GPIO0C
[33,8]	EC_SLP_S4#	19	GPIO0D
[31]	FAN_SPEED1	28	GPIO0E
[38]	ADP_65	29	GPIO0F
[27,32]	E51TXD_P80DATA	30	GPIO10
[27,32]	E51RXD_P80CLK	31	GPIO11
[8]	PMC_CORE_PWROK	32	GPIO12
[32]	NOVOC	34	GPIO13
[32]	NUM_LED#	36	GPIO14



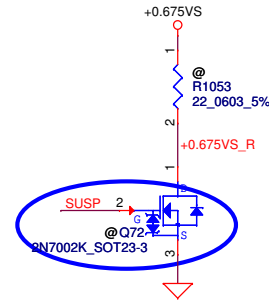
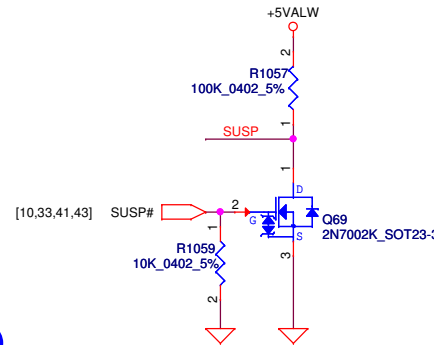
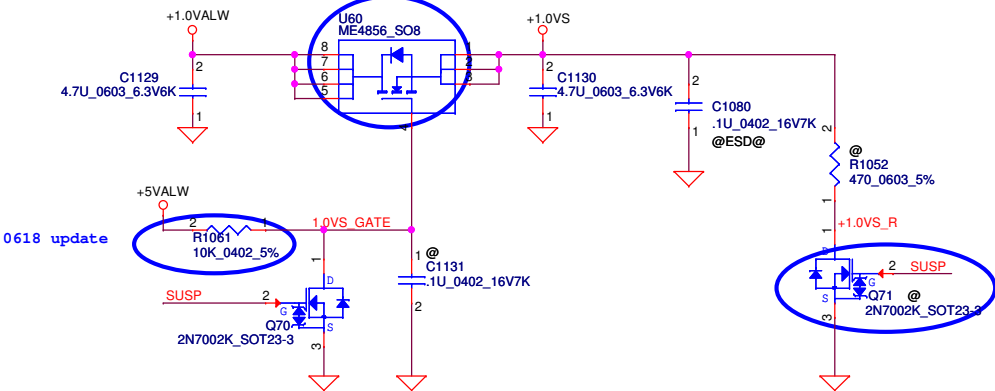
Latest design guide suggest change to 74LVC1G06.

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Title	Document Number	Rev 0.2		Intel BayTrail-M Platform	
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**+1.0VALW TO +1.0VS**

0708:Change to SB00000PZ00 / need apply footprint



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Date: Tuesday, February 18, 2014			Sheet 34 of 47	Rev 0.2

For UMA

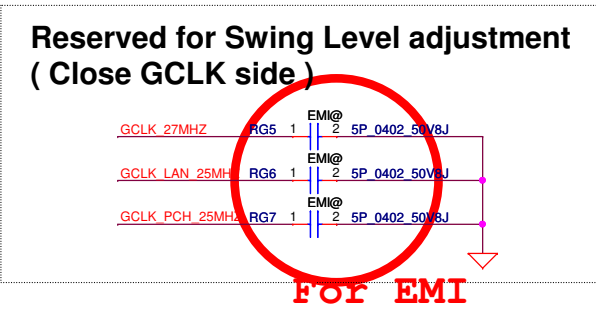
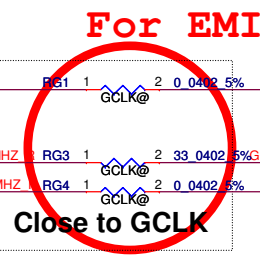
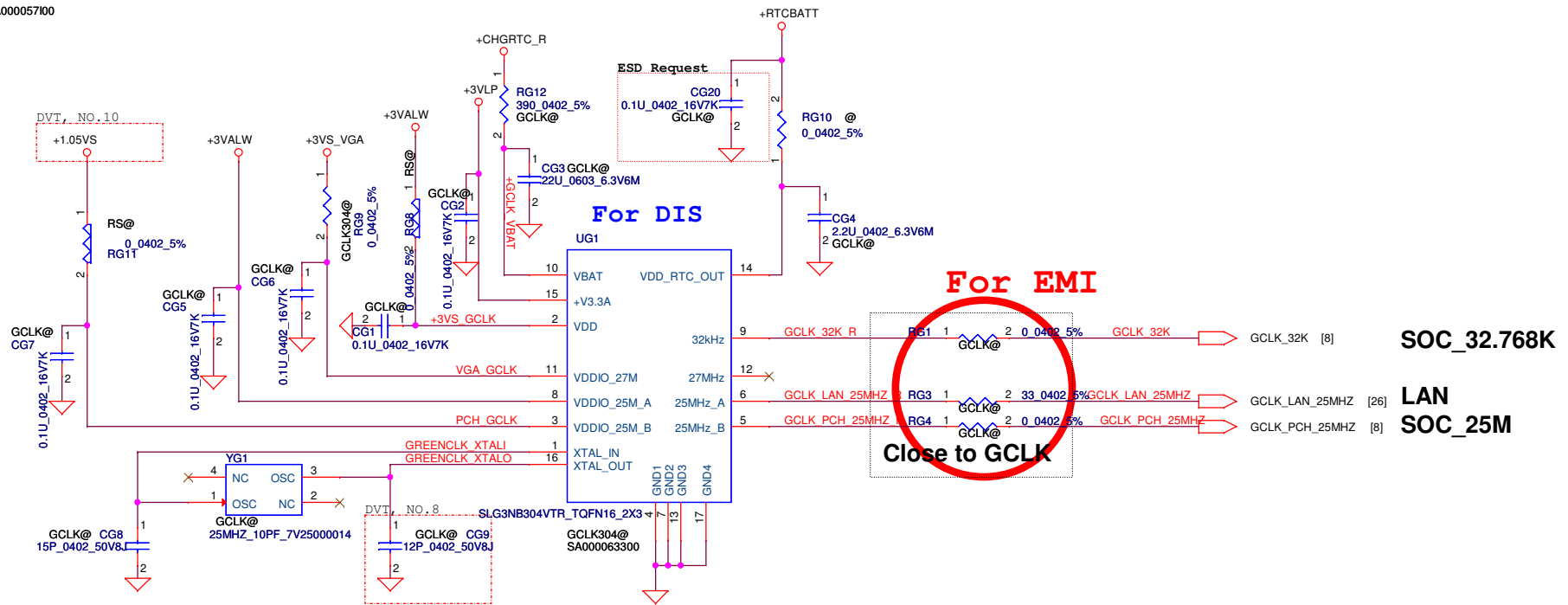
UG1 UMA@



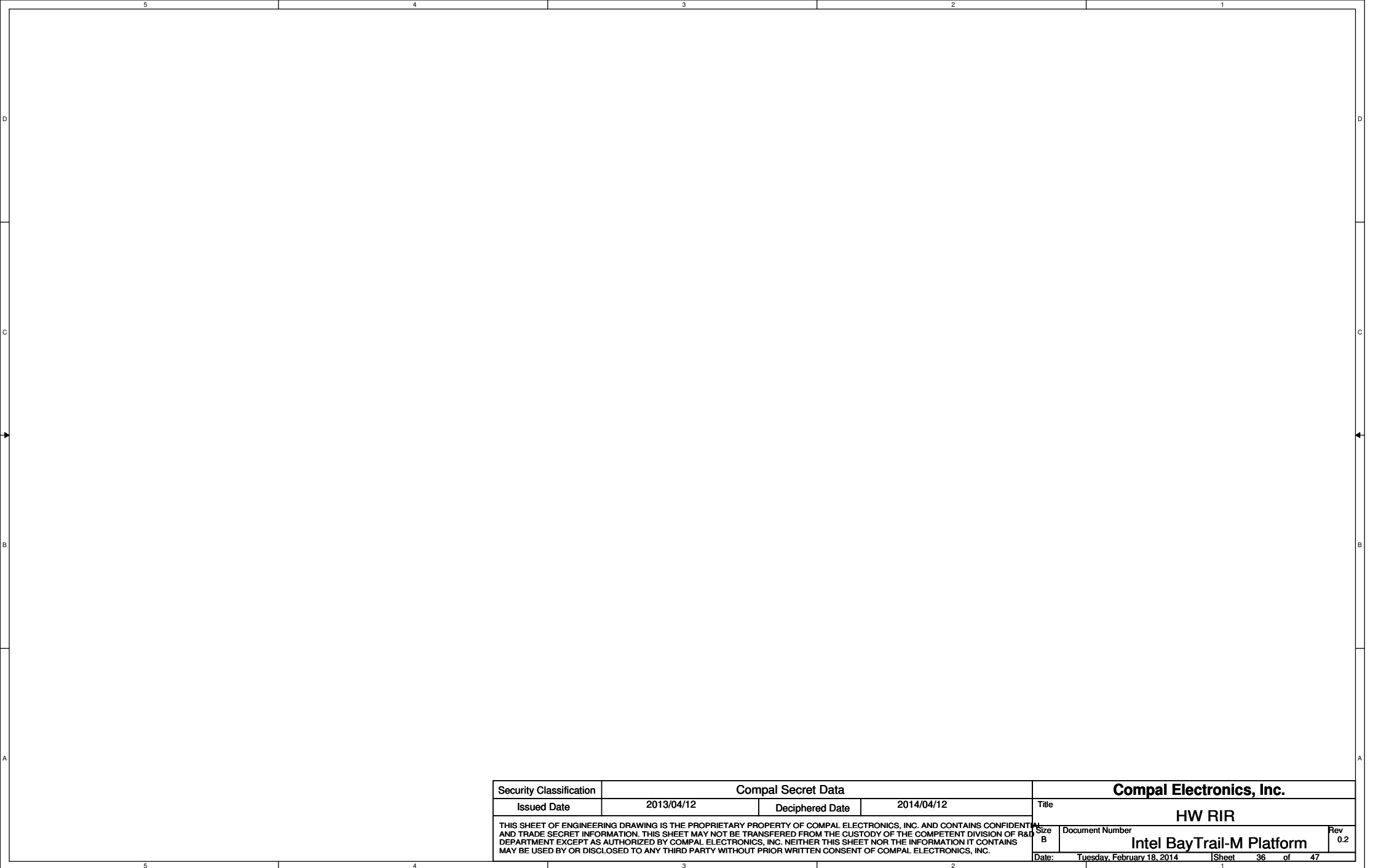
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SA000057100

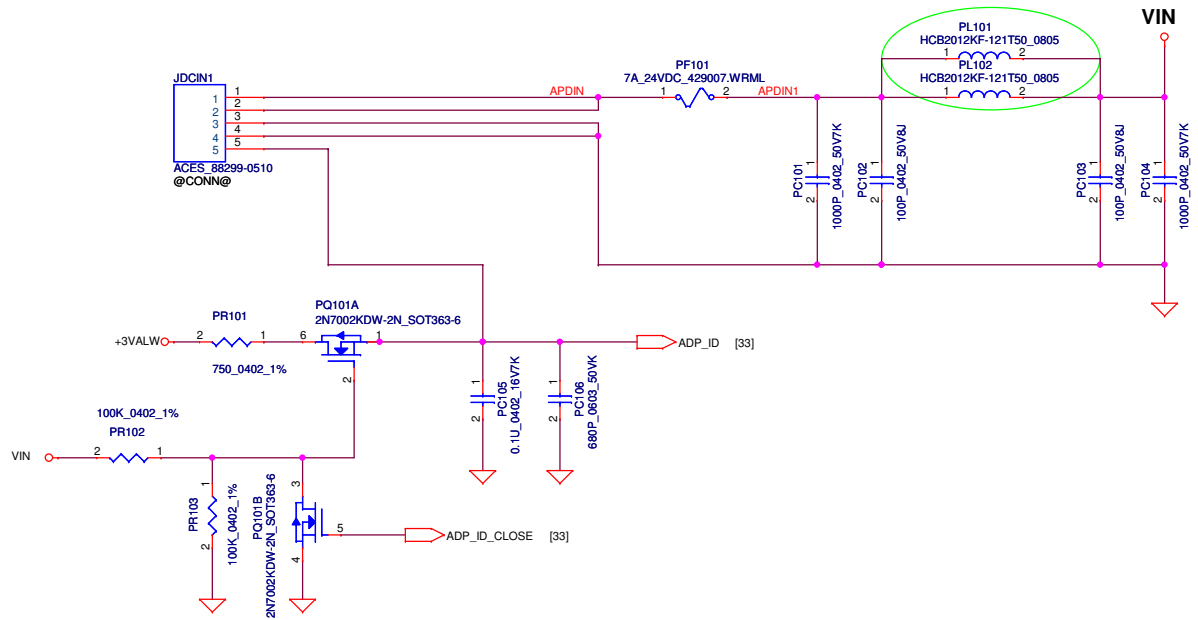
Every power trace need:  
W=20mils



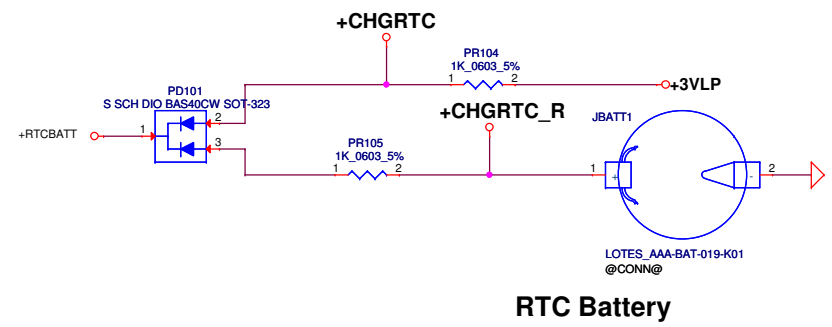
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Issued Date	2012/10/11	Deciphered Date	2014/10/11	Document Number	Rev 0.2
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				B	Intel BayTrail-M Platform	0.2
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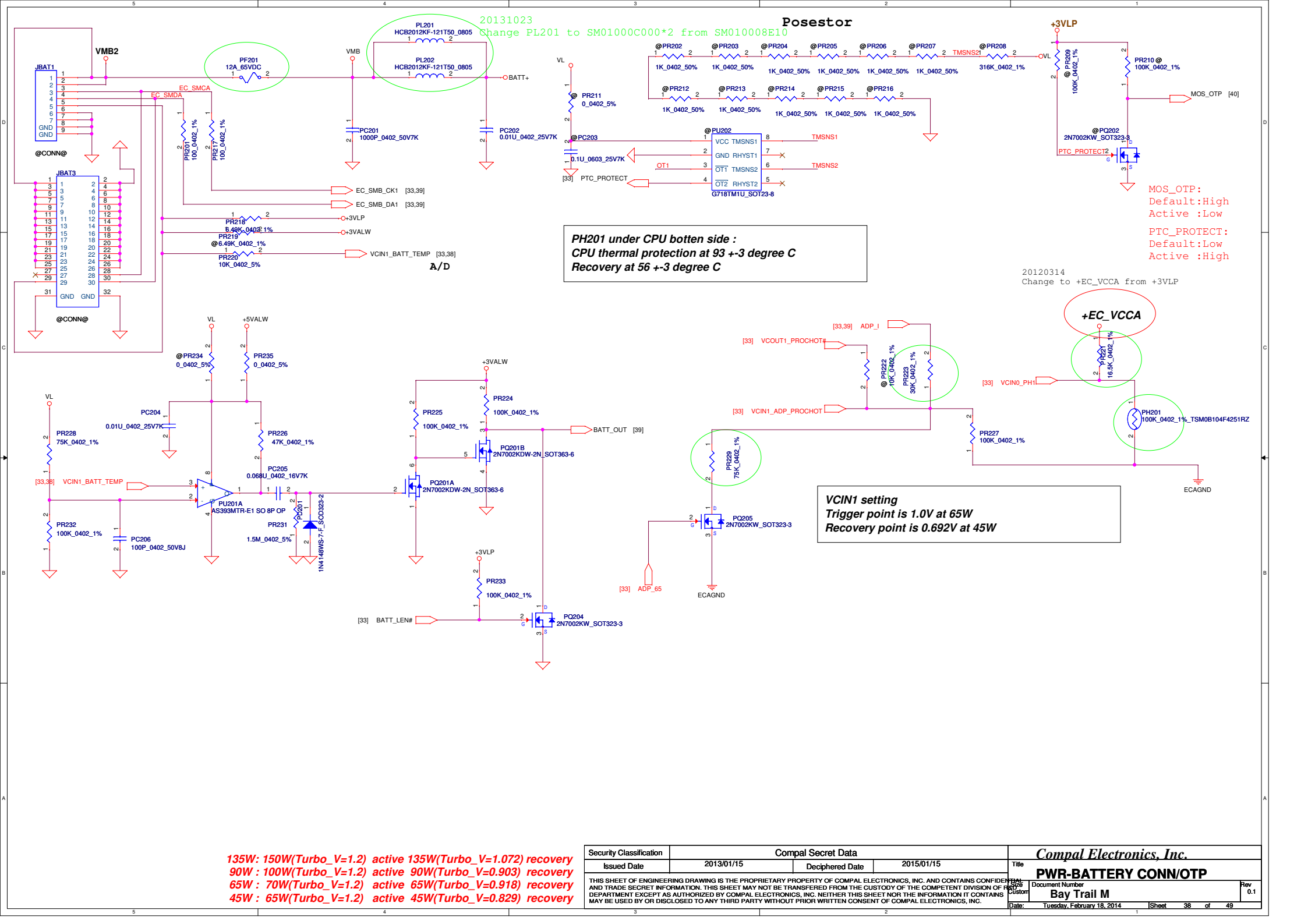


20131023  
Change PL101 to SM01000C000\*2 from SM010008E10



RTC Battery

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Date:		Sheet	37	of 49



**Posistor**

20131023  
Change PL201 to SM01000C000\*2 from SM010008E10

**PH201 under CPU bottom side :**  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C

**VCIN1 setting**  
Trigger point is 1.0V at 65W  
Recovery point is 0.692V at 45W

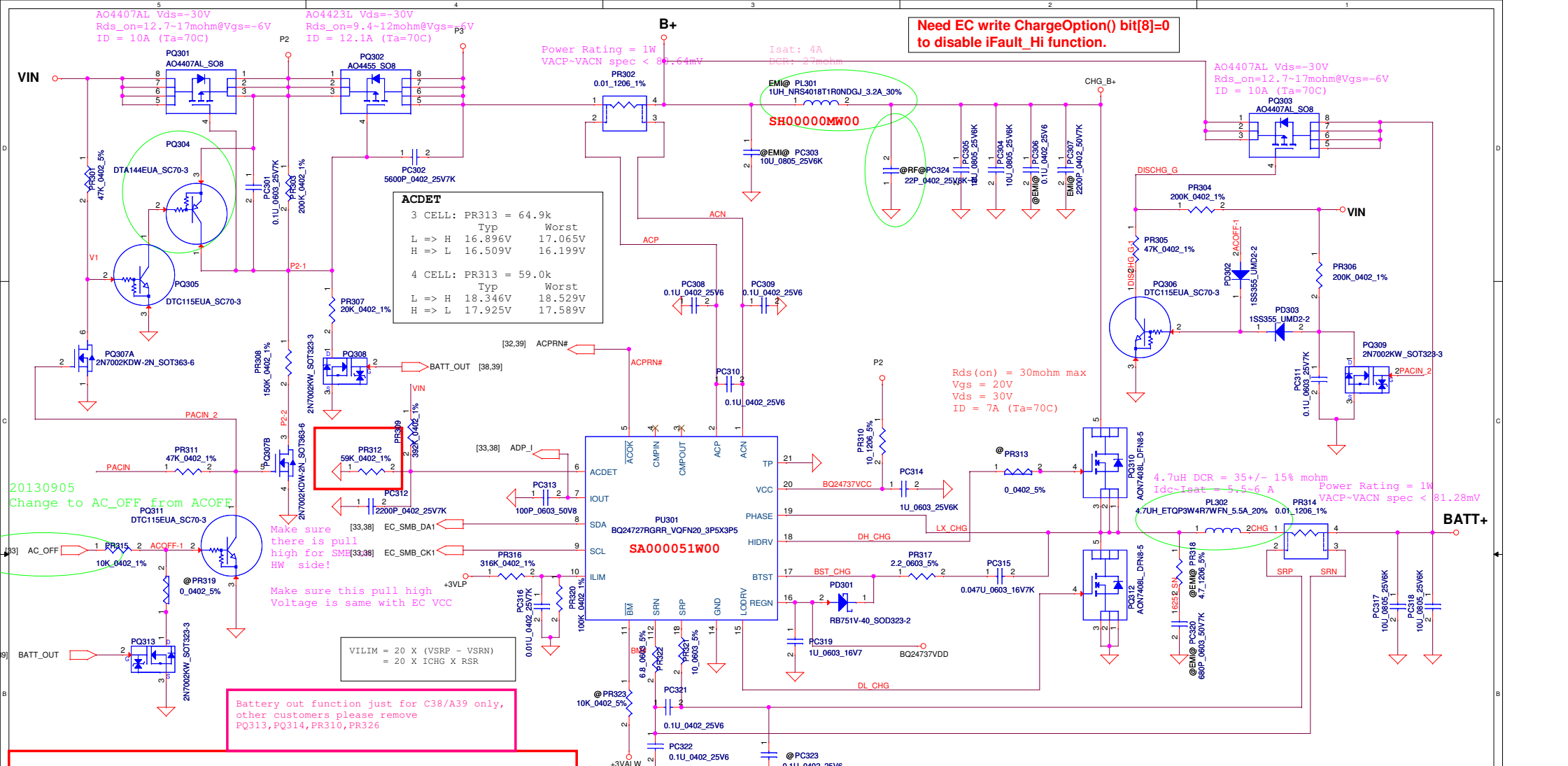
**MOS\_OTP:**  
Default:High  
Active :Low

**PTC\_PROTECT:**  
Default:Low  
Active :High

135W: 150W(Turbo\_V=1.2) active 135W(Turbo\_V=1.072) recovery  
90W : 100W(Turbo\_V=1.2) active 90W(Turbo\_V=0.903) recovery  
65W : 70W(Turbo\_V=1.2) active 65W(Turbo\_V=0.918) recovery  
45W : 65W(Turbo\_V=1.2) active 45W(Turbo\_V=0.829) recovery

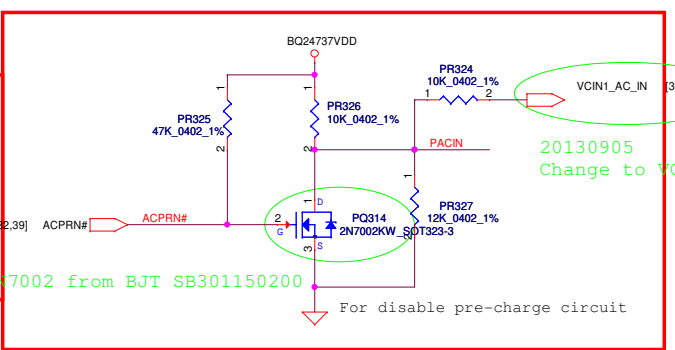
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Issued Date	2013/01/15	Deciphered Date	2015/01/15
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<b>Compal Electronics, Inc.</b>	
<b>PWR-BATTERY CONN/OTP</b>	
Document Number	Rev
<b>Bay Trail M</b>	0.1
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**\*\*Design Notes\*\***  
 Maximum Charging current 2.0A  
 Battery discharge power 55W.  
 #Register Setting  
 1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke  
 2. 0X12 bit3 set 1 (default 0) to enable turbo boost function  
 3. 0X12 bit[12:11] set 00 (default 11) to set BAT  
 Depletion Comparator Threshold  
 Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell)  
 4. Disable turbo when AC only  
 #Circuit Design  
 1. Make sure there is pull high for SMB on HW side  
 2. Use 10X10 choke and 3X3 H/L side MOSFET  
 Charge current 2.0A  
 Power loss : 1.82W  
 Power density : 0.81 (15X15)  
 3. If use 4S per cell 4.35V battery, need change PR313 to 59K for ACDET setting)  
 4. For hybrid design, need double check PQ301,PQ303,PQ309 component rating  
 #Protect function  
 1. AC0VP : ACDET voltage > 3.15V  
 2. Charger timeout : No communication within 175s(default)  
 3. ACOC : 3.33 X Input current DAC setting(default)  
 4. CHGOCP : 3/4.5/6A based on current setting  
 5. BATOVP : 104%  
 6. BATLOWV : 2.5V  
 7. TSHUT : 155C  
 8. IFAULT HI : 750mV (default)  
 9. IFAULT LOW : 135mV (default)

Module model information  
 BQ24737\_V1.mdd for dual layer  
 20131028  
 1.Change PQ314 to SB000009Q80 2N7002 from BJT SB301150200



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				BE_BDW	0.1
			Date:	Tuesday, February 18, 2014	Sheet 39 of 49

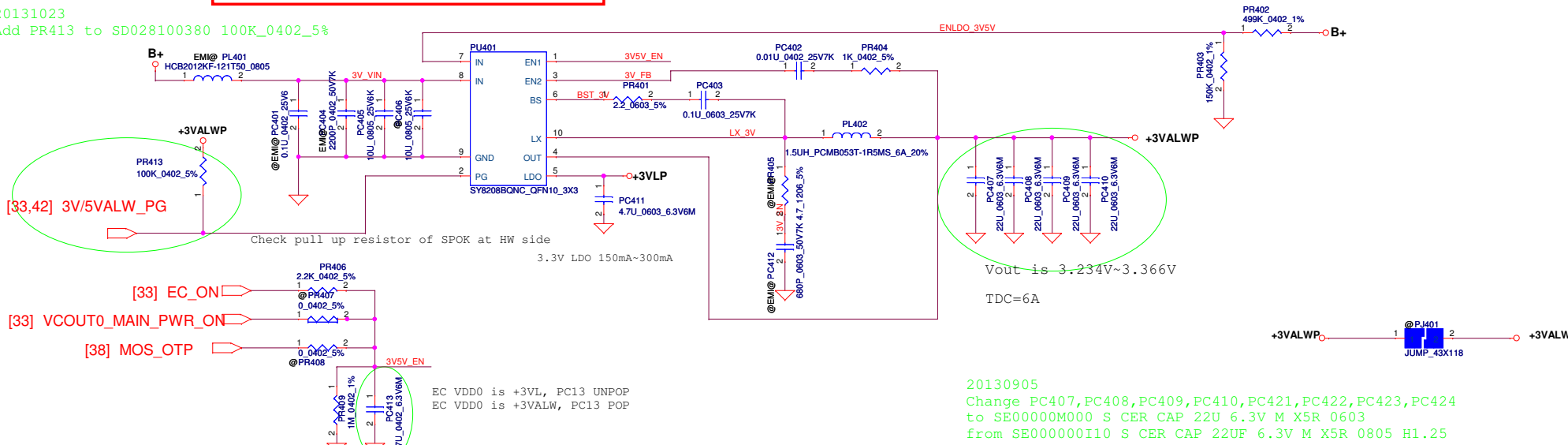
Module model information

SY8208E\_V2.mdd

EN1 and EN2 don't floating

20130905  
Change to 3V/5VALW\_PG from SPOK

20131023  
Add PR413 to SD028100380 100K\_0402\_5%



[33,42] 3V/5VALW\_PG

[33] EC\_ON

[33] VCOUT0\_MAIN\_PWR\_ON

[38] MOS\_OTP

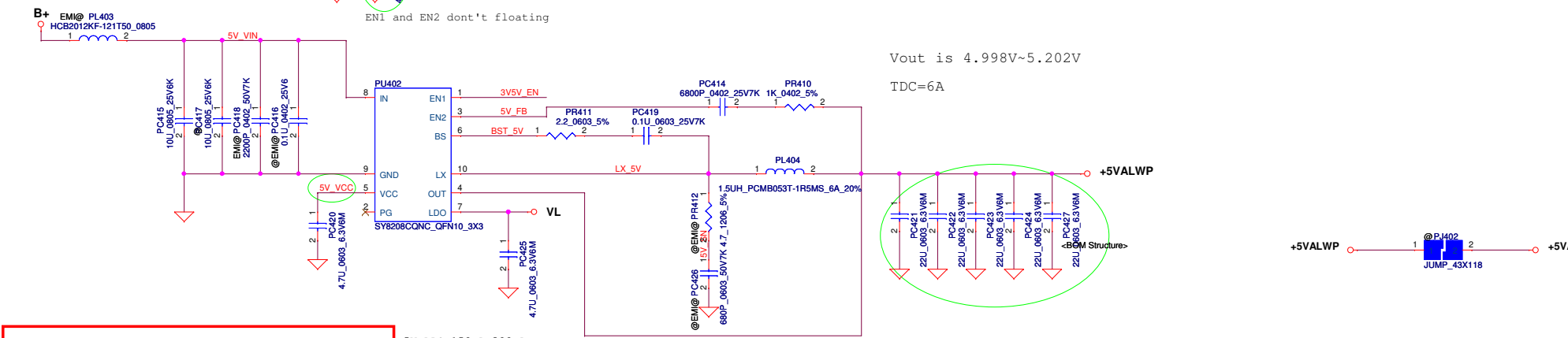
Check pull up resistor of SPOK at HW side

3.3V LDO 150mA~300mA

EC VDD0 is +3VL, PC13 UNPOP  
EC VDD0 is +3VALW, PC13 POP

20130905  
Change PC407,PC408,PC409,PC410,PC421,PC422,PC423,PC424  
to SE00000M000 S CER CAP 22U 6.3V M X5R 0603  
from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

EN1 and EN2 don't floating



Module model information

SY8208C\_V2.mdd

5V LDO 150mA~300mA

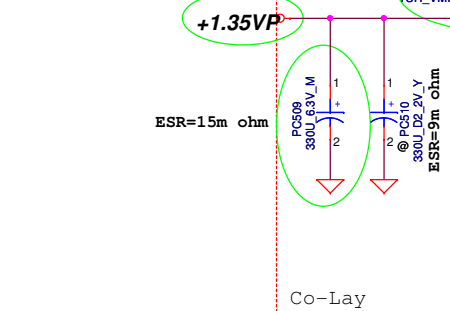
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
				<b>+3VALW/+5VALW</b>
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Module model information

RT8207M\_v1.mdd For Single layer  
RT8207M\_v2.mdd For Dual layer

20131023  
Change PC509 to SF000006B00 from SF000002000 for common part



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

20130906  
1. Change to DDR\_PWROK from PGOOD\_1.35V  
2. Change PR505 pull high to +1.35VS from 3VALW

MOSFET: 3x3 DFN  
H/S Rds (on): 27mohm (Typ), 34mohm (Max)  
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on): 9.9mohm (Typ), 13mohm (Max)  
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

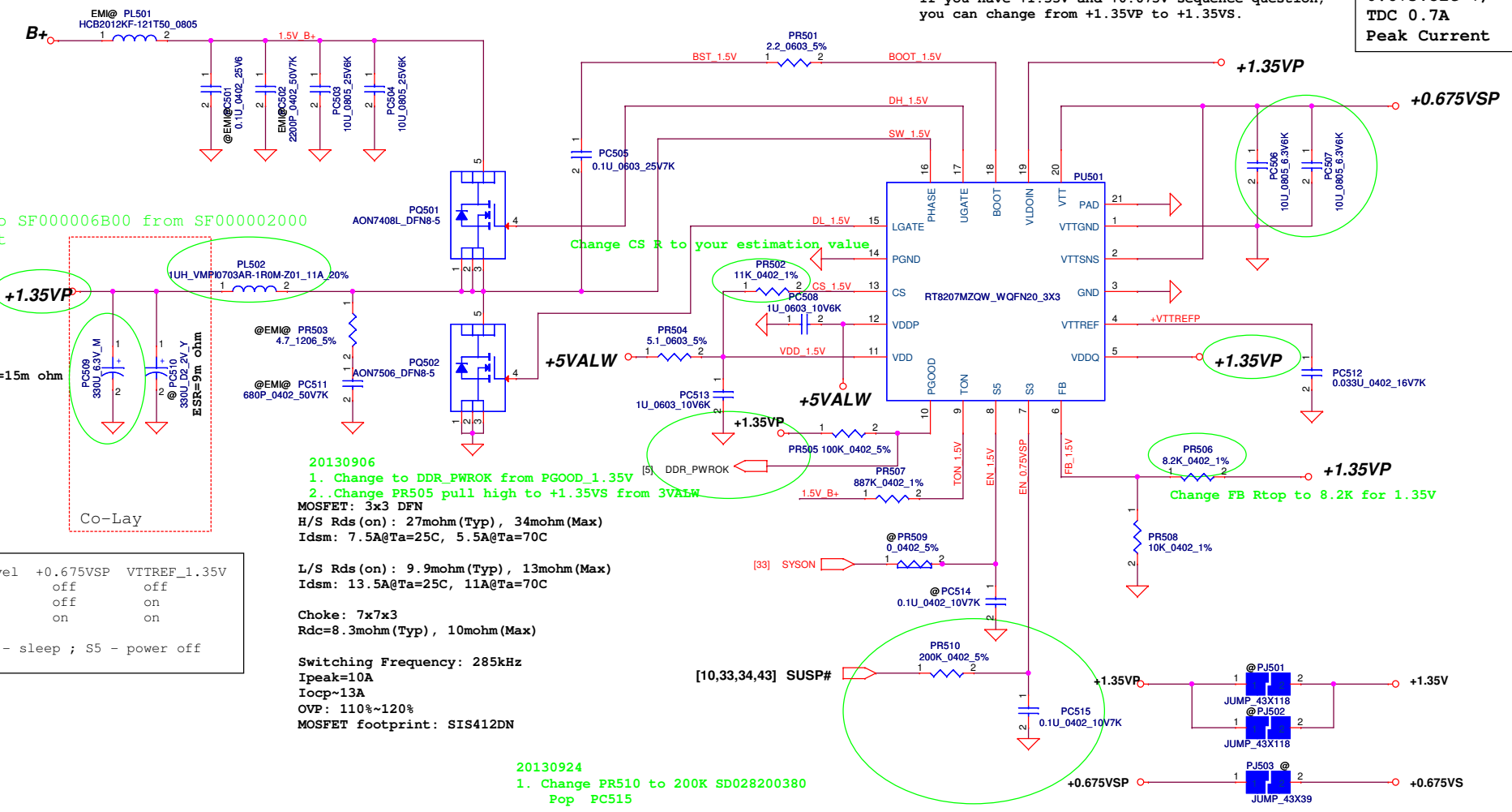
Choke: 7x7x3  
Rdc=8.3mohm (Typ), 10mohm (Max)

Switching Frequency: 285kHz  
Ipeak=10A  
Iocp~13A  
OVP: 110%~120%  
MOSFET footprint: SIS412DN

20130924  
1. Change PR510 to 200K SD028200380  
Pop PC515

Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A

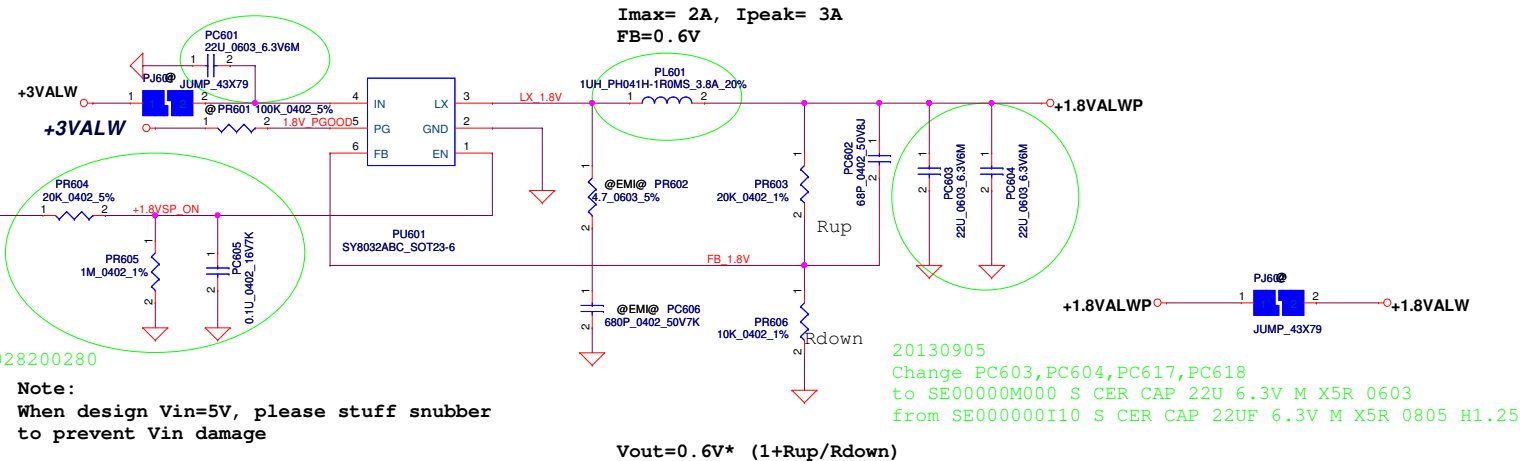


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				+1.35VSP	
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Module model information

SY8032\_V1.mdd

20130913  
Need to change PC702 to 0603 from 0805



20130905  
Change to 3V/5VALW\_PG from SPOK

20130924  
Change PR604 to 20K SD028200280  
Pop PC605 to 0.1u

Note:  
When design Vin=5V, please stuff snubber to prevent Vin damage

20130905  
Change PC603, PC604, PC617, PC618 to SE00000M000 S CER CAP 22U 6.3V M X5R 0603 from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

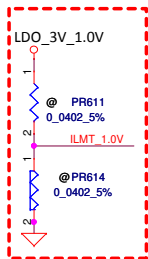
SY8206D\_V1.mdd

Module model information

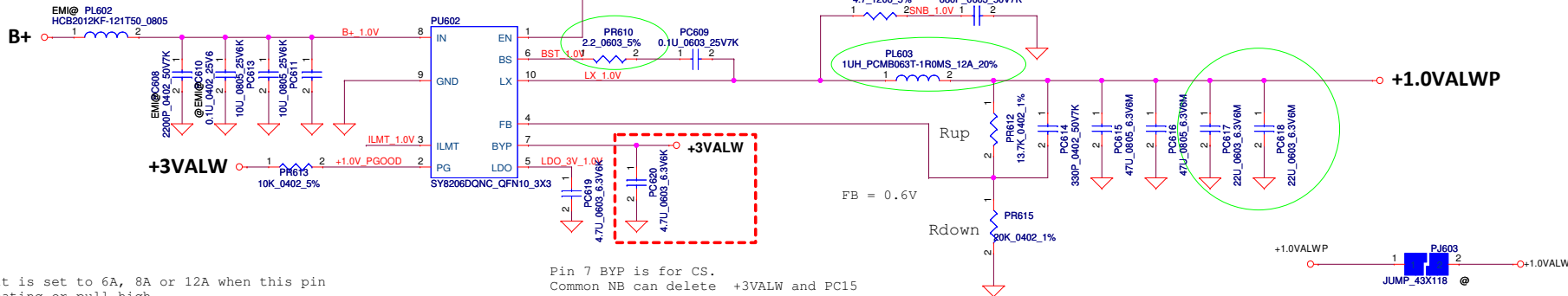
20130924  
1. Change PR607 to 10K SD028100280  
Pop PC607 to 0.1U\_0402\_16V7K SE076104K80

20130905  
Change to 3V/5VALW\_PG from SPOK

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high



Pin 7 BYP is for CS.  
Common NB can delete +3VALW and PC15

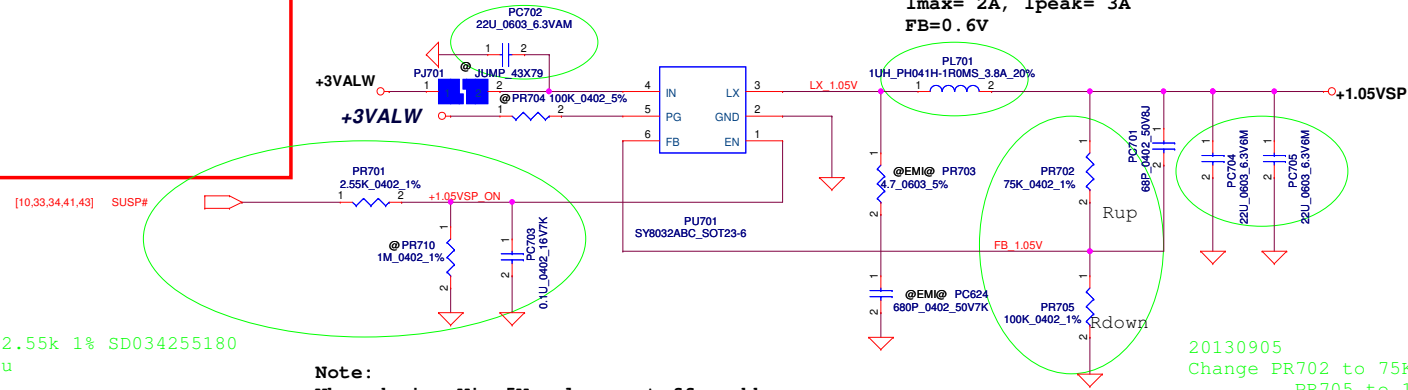
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Issued Date	2012/12/01	Deciphered Date	2013/07/10	Title <b>PWR-1.8VALW/1.0VALW</b>	
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Module model information

20130913  
Need to change PC702 to 0603 from 0805

Imax= 2A, Ipeak= 3A  
FB=0.6V

DIS:SY8003  
UMA:SY8032



20130924  
Change PR701 to 2.55k 1% SD034255180  
Pop PC703 to 0.1u  
unpop PR710

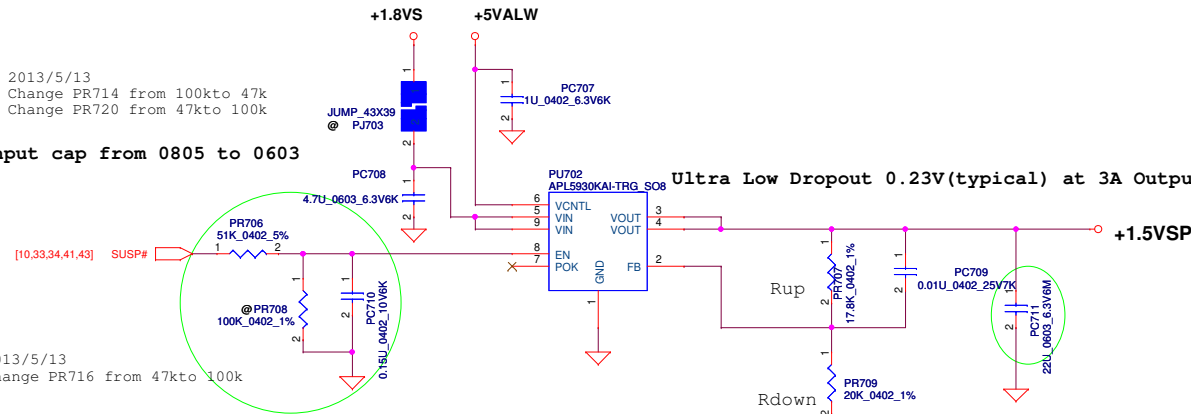
Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

20130905  
Change PR702 to 75K SD034750280  
PR705 to 100K SD034100380

20130905  
Change PC701, PC703, PC704, PC711  
to SE00000M000 S CER CAP 22U 6.3V M X5R 0603  
from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

2013/5/13  
Change PR714 from 100k to 47k  
Change PR720 from 47k to 100k  
change input cap from 0805 to 0603



VFB=0.6V  
Vout=0.6V\* (1+Rup/Rdown)  
Vout=1.011V

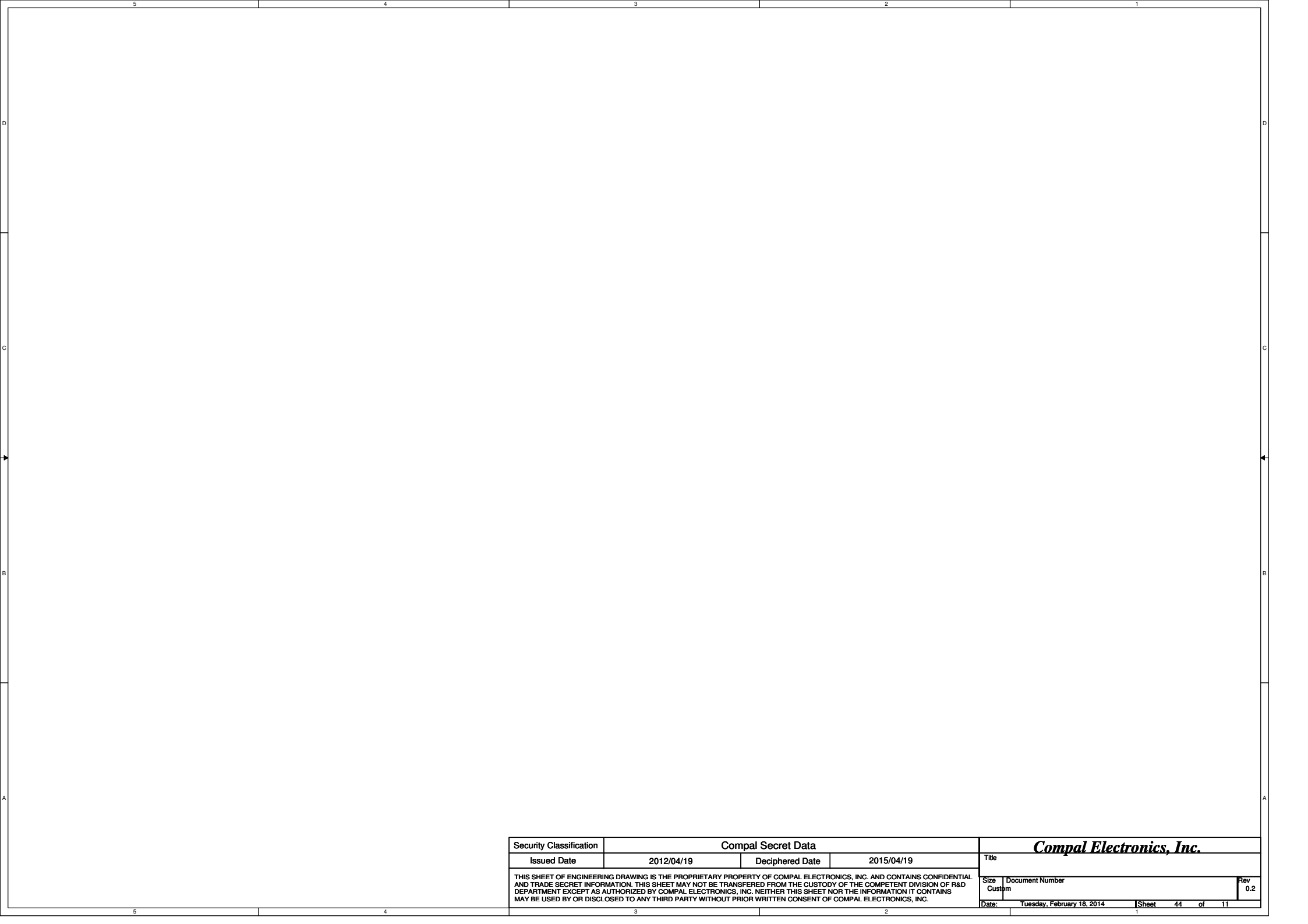
$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

$$V_{out} = 1.512V$$

2013/5/13  
Change PR716 from 47k to 100k

20130924  
Change PR706 to 51K SD028510280  
Pop PC710 0.15u\_0402\_10V6K SE00000H300  
unpop PR708

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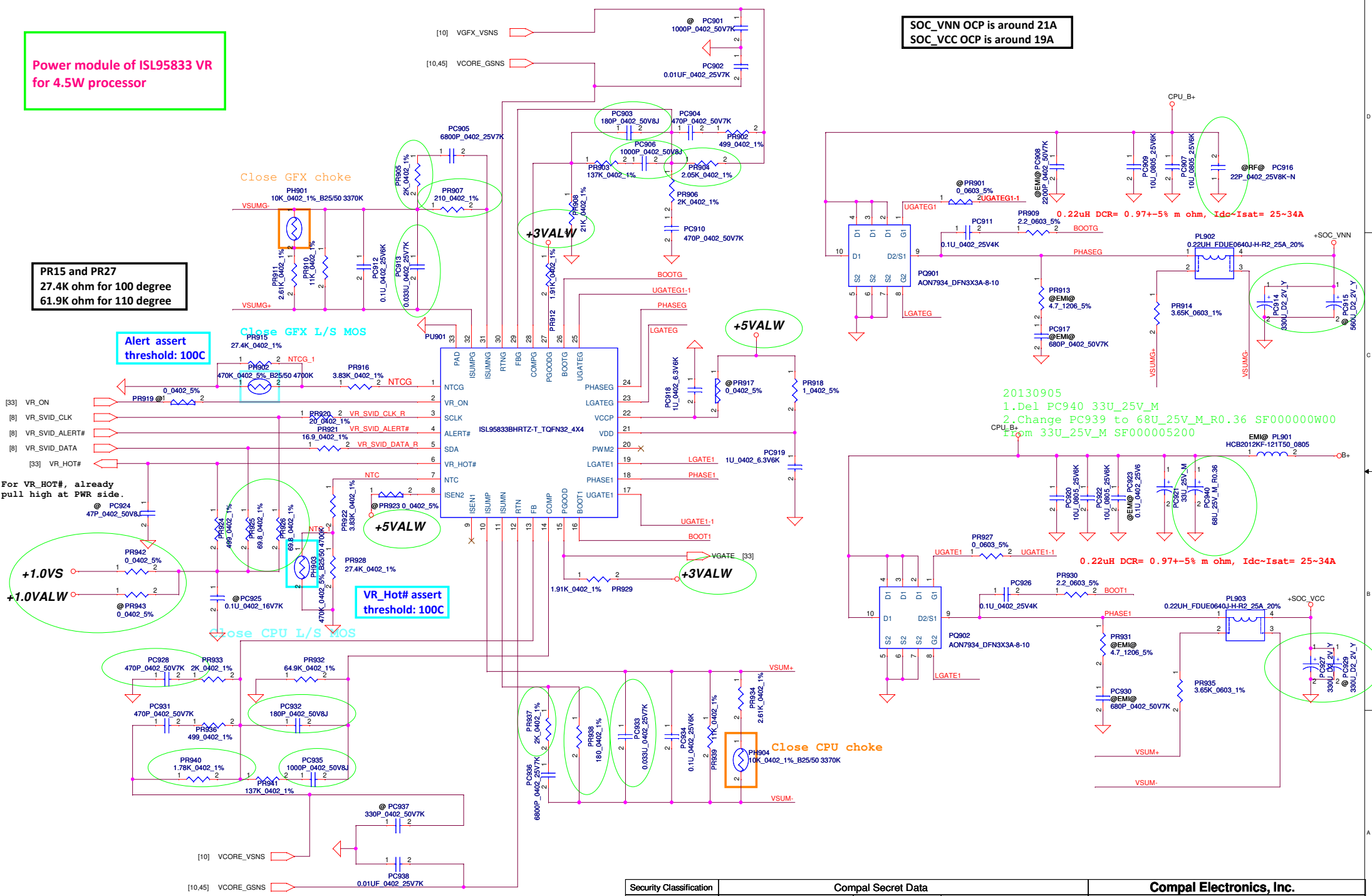
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Power module of ISL95833 VR for 4.5W processor

PR15 and PR27  
27.4K ohm for 100 degree  
61.9K ohm for 110 degree

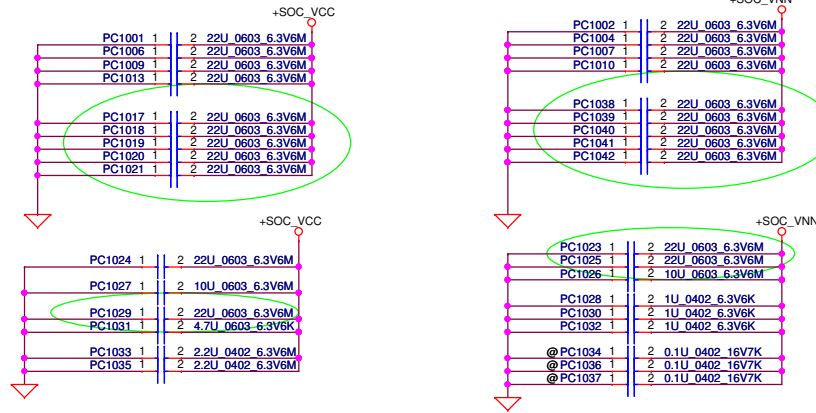
Alert assert  
threshold: 100C

For VR\_HOT#, already  
pull high at PWR side.



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# 22uF 0805 size change to 0603



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**Version change list (P.I.R. List)**

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							

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